

Fast-Convergent Expression for the Barrel-Plate Capacitance in the Physics-Based Via Circuit Model

Si-Ping Gao¹, *Member, IEEE*, Francesco de Paulis², *Member, IEEE*, En-Xiao Liu, *Senior Member, IEEE*, Antonio Orlandi, *Fellow, IEEE*, and Hui Min Lee, *Member, IEEE*

Abstract—The widely used analytical formula for the barrel-plate capacitance in the physics-based via circuit model involves an infinite summation, which requires a truncation during practical computations. Such a truncation is problem-dependent and prone to either underestimate the capacitance value or ruin the computation when truncating too late. This letter proposes a fast-convergent expression of the barrel-plate capacitance based on a convergence study of the original formula. The proposed expression comprises a well truncated and a closed-form part, whose computation is more efficient and free of truncation error. It is validated against quasi-static solutions and measurement.

Index Terms—Barrel-plate capacitance, convergence study, fast-convergent expression, physics-based via model.

I. INTRODUCTION

Vias have been extensively employed as interconnect to route signal traces on different layers or connect components to power or ground planes in multilayer printed circuit boards (PCBs) and packages [1]. However, as discontinuities in a signal link, vias can cause signal integrity (SI) issues [2]; parallel-plate waveguide modes can be excited by transient signals on vias, leading to serious voltage fluctuations in power distribution networks and strong edge radiations, which compromise both power integrity (PI) and electromagnetic compatibility (EMC) [3]. Therefore, electromagnetic modeling of via-plate-pair structures is essential for the analyses of SI, PI, and EMC of multilayer PCBs and packages.

Several different approaches for modeling via-plate-pair interaction have been developed [4]–[7], among which the physics-based via circuit model [4], [5] attracts much attention. In this model, the via-plate-pair structure is represented by a π -type circuit (see Fig. 1): the via barrel is a shorting branch; two shunt capacitors, each one comprising a barrel-plate capacitance C_b and a coaxial capacitance C_{coax} , account for capacitive couplings between via and plates; parallel plate impedance Z_{pp} serves as the load in the circuit return path. The model was validated by measurement and simulation [2], [8].

Manuscript received December 19, 2017; accepted March 1, 2018. Date of publication March 20, 2018; date of current version May 8, 2018. (Corresponding author: Si-Ping Gao.)

S.-P. Gao is with the NUSNNI-NanoCore and the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119077 (e-mail: nnigaos@nus.edu.sg).

F. de Paulis and A. Orlandi are with the UAq EMC Laboratory, Department of Industrial and Information Engineering and Economics, University of L'Aquila, 67100 L'Aquila, Italy (e-mail: francesco.depaulis@univaq.it; antonio.orlandi@univaq.it).

E.-X. Liu and H. M. Lee are with the Department of Electronics and Photonics, Institute of High Performance Computing, A*STAR, Singapore 138632 (e-mail: liuex@ihpc.a-star.edu.sg; leehm@ihpc.a-star.edu.sg).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LMWC.2018.2812639

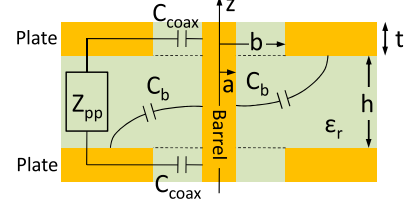


Fig. 1. Physics-based via circuit model for the via-plate-pair structure.

Besides C_{coax} and Z_{pp} [2]–[4], the most challenging calculation lies in the evaluation of C_b . An analytical formula [9] for C_b was derived based on the assumption that magnetic frill current exists at antipads. It was extended in [10] and [11]. The analytical formula allows for accurate evaluation of C_b ; however, requires a proper truncation of the infinite summation, which is problem-dependent. C_b can be easily underestimated by an early truncation; the arithmetic underflow may also arise and ruin the whole computation when truncating too late.

This letter proposes an elegant expression of C_b which converges faster than the original one. The proposed expression allows for efficient C_b evaluation and is free of truncation issues. It is validated against quasi-static solutions and measurements.

II. FAST-CONVERGENT EXPRESSION OF BARREL-PLATE CAPACITANCE

A. Convergence Study on Original Expression

The analytical formula of C_b for inner metallic and outer perfectly matched boundaries in [9] is recalled as follows:

$$C_b = \frac{8\pi\epsilon}{h \ln(b/a)} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{k_n^2} \left(\frac{H_0^{(2)}(k_n b)}{H_0^{(2)}(k_n a)} - 1 \right) \quad (1)$$

where a and b denote the radii of the via barrel and the antipad, respectively; a thin dielectric layer with thickness h and dielectric constant ϵ_r separates the plates (see Fig. 1). $H_0^{(2)}$ stands for the zero-order Hankel function of the second kind; k_n is the radial wavenumber for TM_{zn} modes

$$k_n = \sqrt{k^2 - (n\pi/h)^2}, \quad k = k_0 \sqrt{\epsilon_r}. \quad (2)$$

Depending on the via-plate-pair dimensions and material properties, the convergence of (1) behaves differently. Fig. 2 shows its convergence according to design parameters in Table I. From Cases A to E, (1) converges slower and slower because: 1) a larger radius of the via barrel a ; 2) a smaller radius of the antipad b ; 3) a larger separation h between plates; and 4) a larger dielectric constant ϵ_r . It can be explained from (1) that, when a and b are closer, the quotient of the two Hankel functions decays slower with n , which flattens the summation series; hence, more terms (modes) are

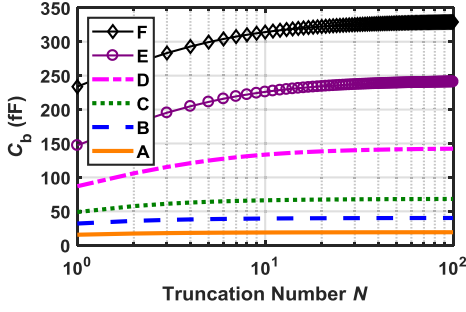


Fig. 2. Convergence of (1) according to the design parameters in Table I.

TABLE I
DESIGN PARAMETERS OF DIFFERENT CASES

Case	a (mil)	b (mil)	h (mil)	ϵ_r	f (GHz)
A	4	14	9	3.84	1
B	8	14	9	3.84	1
C	8	10	9	3.84	1
D	8	10	40	3.84	1
E	8	10	40	6.50	1
F	8	10	40	6.50	40

required to reach a convergence. Similarly, a larger h or ϵ_r slows the increase of $|k_n|$ with n [see (2)], which in turn slows the convergence. Note that C_b calculated by (1) is frequency-dependent, which is only obvious beyond a very high frequency (several tens of gigahertz) for practical cases (see [9, Fig. 12]); however, the convergence of (1) is almost frequency independent, as shown in Fig. 2 where the curves converge at almost the same rates for different frequencies, between 1 and 40 GHz (Cases E and F).

The problem-dependent convergence of (1) can easily cause underestimation due to early truncations. For example, $N = 31$ used in [9] can be a good truncation number for Cases A–C (see Fig. 2); however, it generates a large deviation of 2.3% for Case D. On the other hand, a late truncation may bring about the issue of “division by zero” (“ $x/0$ ” or “ $0/0$ ”) for the quotient term with two Hankel functions. Hankel functions at very large arguments are too small for floating-point numbers and thus are automatically truncated (i.e., arithmetic underflow).

B. Fast-Convergent Expression

To address the above issues, we first separate (1) into two summations

$$C_b = \frac{8\pi\epsilon}{h \ln(b/a)} \left(\sum_{n=1,3,5,\dots}^{\infty} S_n - \sum_{n=1,3,5,\dots}^{\infty} F_n \right) \quad (3)$$

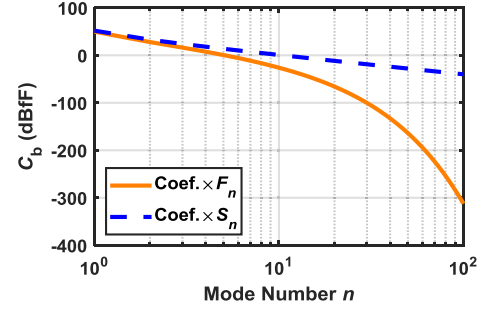
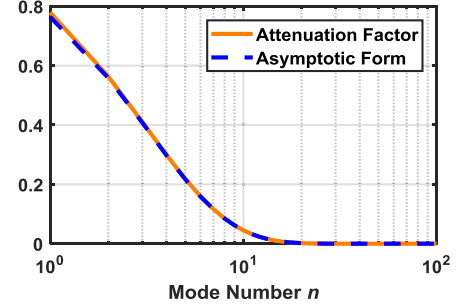
where S_n and F_n are

$$S_n = -\frac{1}{k_n^2}, \quad F_n = -\frac{1}{k_n^2} \frac{H_0^{(2)}(k_n b)}{H_0^{(2)}(k_n a)}. \quad (4)$$

The numerical experiment of the convergence for Case D (see Fig. 3) shows that S_n decays much slower than F_n , because the latter has an additional term: $H_0^{(2)}(k_n b)/H_0^{(2)}(k_n a)$ that serves as an *Attenuation Factor* (AF). To cater to the different convergence rates, we derive a closed-form formula for the slow-convergent S_n and devise a truncation scheme for the fast-convergent F_n .

Inspired by an extraordinary formula of cotangent

$$\cot x = \frac{1}{x} + \sum_{n=1}^{\infty} \frac{2x}{x^2 - n^2 \pi^2} \quad (5)$$

Fig. 3. Convergence of S_n and F_n for Case D.Fig. 4. AF and its asymptotic form against n for Case D.

we obtain a closed-form formula for the summation of S_n

$$\sum_{n=1,3,5,\dots}^{\infty} S_n = \frac{h}{4k} \tan(kh/2). \quad (6)$$

Equation (6) is undefined for $h = (2m+1)\lambda/2$, $m \in \mathbb{Z}$, but it causes no issue to any practical situation where h is very small compared to the wavelength. Given the difficulty in identifying a closed-form expression for the summation of F_n , we devise a proper truncation scheme for it. Based on the asymptotic form of the Hankel function of the second kind for large arguments, we obtain the asymptotic form of AF

$$\frac{H_0^{(2)}(k_n b)}{H_0^{(2)}(k_n a)} \sim \sqrt{\frac{a}{b}} e^{-|k_n|(b-a)} \quad (7)$$

$|k_n| \rightarrow \infty$

Fig. 4 shows that AF can be accurately represented by its asymptote. Most importantly, AF drops to zero at a larger mode number, so it is possible to truncate, without losing the accuracy, the summation of F_n when AF is sufficiently small. The truncation mode number is then derived based on (7)

$$N = \text{ceil} \left[\frac{h}{2\pi} \sqrt{\left(\frac{\ln(\sqrt{a/b}/\text{AF})}{b-a} \right)^2 + k^2} + \frac{1}{2} \right] \quad (8)$$

where function $\text{ceil}()$ rounds a number to the next larger integer.

Inserting (6) into (3) and truncating at N by (8) leads to the proposed fast-convergent expression of C_b

$$C_b = \frac{8\pi\epsilon}{h \ln(b/a)} \left[\frac{h}{4k} \tan(kh/2) - \sum_{n=1,3,5,\dots}^{2N-1} F_n \right]. \quad (9)$$

III. CASE STUDY

Case D (see Table I) is used here as the first example. Table II lists the results of the original and the proposed fast-convergent expressions at different truncation numbers. If the original formula is used, then it is only when N reaches 1000 that the value of C_b approaches that calculated by the

TABLE II
RESULTS USING ORIGINAL AND PROPOSED EXPRESSIONS

Expression	Truncation Number N	C_b (fF)
Original*	1000	143.24
Proposed	30	143.34

*Arithmetic underflow at very large N has been avoided.

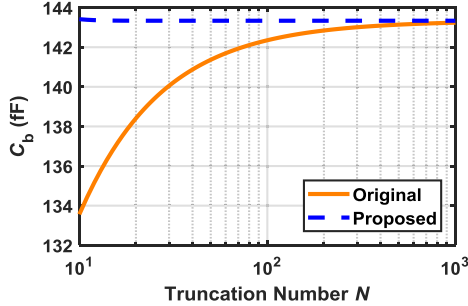


Fig. 5. C_b against truncation number N for Case D.

TABLE III
COMPARISON OF THE VIA-PLATE CAPACITANCE CALCULATION
($h_u = h_d = 0.2296$ mm, $t = 0.0254$ mm; $\epsilon_r = 3.84$)

Radii [mm]		C_{via} [fF] (No. of modes being summed up)		
a	b	Original	Proposed	Quasi-static
0.1016	0.5080	33.5 (40)	33.7 (2)	34.1
0.1524	0.4318	51.4 (40)	51.6 (2)	52.3
0.2032	0.3556	89.8 (40)	90.3 (3)	91.6

* C_{via} includes C_{coax} and C_b ; N is based on $AF = 10^{-4}$ for the proposed expression.

proposed fast-convergent expression, which requires a truncation mode number of $N = 30$ for $AF = 10^{-4}$. $N = 30$ for the original expression underestimates C_b by 2.3%. Fig. 5 further illustrates that unlike the original expression, the proposed one starts to converge as early as $N = 20$.

The second example is taken from a parametric study in [12] with quasi-static solutions. Table III shows that the results of the fast convergent expression are closer to the quasi-static solutions; furthermore, the proposed expression converge faster with much less modes needed in the summation.

In addition, the fast convergent expression is validated against measurement data within the physics-based circuit model framework. A square-shaped 16 layer PCB with surrounding via fence is considered, where a single through-via connects two striplines at layers three and five. The other design parameters are the same as in [8, Fig. 8]. Transmission coefficient is calculated using the physics-based via model, where C_b is evaluated by the original and proposed formulae. Considering the insignificant variation of C_b between 0 and 30 GHz for this case, i.e., 39.54–39.95 fF for Cavity D and 26.89–27.01 fF for other cavities, constant C_b values calculated at 1 GHz are used in the circuit model. Fig 6 shows that the results by both expressions agree well with the measurement data. Nevertheless, the C_b calculation time for the fast convergent expression is 0.4 ms with truncation numbers being two or three, which is in sharp contrast to the 3.0 ms taken by the original expression with a truncation number of 40. The saving in the calculation time seems small for this example, but in consideration of practical multilayer PCBs with hundreds or thousands of vias, the time saving by the proposed fast-convergent expression would be significant.

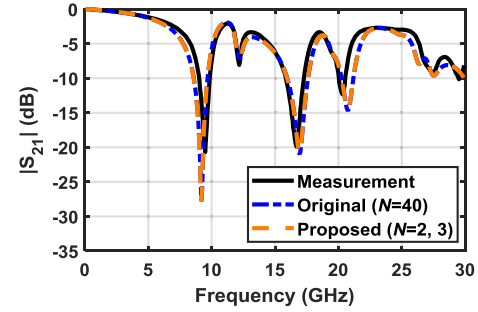


Fig. 6. Transmission coefficient from measurement and circuit models where C_b is obtained by the original and the fast convergent expressions (AF is set to 10^{-4} obtaining $N = 2$ for Cavity D and $N = 3$ for all the others, according to [8]).

IV. CONCLUSION

A fast-convergent expression of C_b has been proposed by improving the original expression. The original summation is divided into two parts. A truncation scheme is proposed for the rapidly decaying part and a closed-form formula for the slow-decaying one, leading to an improved expression with fast convergence. Furthermore, underestimations and arithmetic underflow arising from improper truncation are avoided. The fast-convergent expression can be directly integrated into existing electronic design automation tools for fast SI and PI analysis.

ACKNOWLEDGMENT

The authors would like to thank the EMC Laboratory, Missouri University of Science and Technology, for providing the measurement data.

REFERENCES

- [1] S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*. New York, NY, USA: Wiley, 2000.
- [2] F. de Paulis, Y.-J. Zhang, and J. Fan, "Signal/power integrity analysis for multilayer printed circuit boards using cascaded s-parameters," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 1008–1018, Nov. 2010.
- [3] M. Leone, "The radiation of a rectangular power-bus structure at multiple cavity-mode resonances," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 3, pp. 486–492, Aug. 2003.
- [4] C. Schuster, "Developing a 'physical' model for vias," in *Proc. DesignCon*, Santa Clara, CA, USA, Feb. 2006, pp. 1–24.
- [5] G. Selli, "Developing a 'physical' via model for vias—Part II: Coupled and ground return vias," in *Proc. DesignCon*, Santa Clara, CA, USA, Jan./Feb. 2007, pp. 1–22.
- [6] L. Tsang and D. Miller, "Coupling of vias in electronic packaging and printed circuit board structures with finite ground plane," *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 375–384, Nov. 2003.
- [7] Q. Gu, Y. E. Yang, and M. A. Tassoudji, "Modeling and analysis of vias in multilayered integrated circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 2, pp. 206–214, Feb. 1993.
- [8] R. Rimolo-Donadio *et al.*, "Signal integrity: Efficient, physics-based via modeling: Integration of striplines," *IEEE Electromagn. Compat. Mag.*, vol. 1, no. 2, pp. 74–81, 2nd Quart., 2012.
- [9] Y. Zhang, J. Fan, G. Selli, M. Cocchini, and F. de Paulis, "Analytical evaluation of via-plate capacitance for multilayer printed circuit boards and packages," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 9, pp. 2118–2128, Sep. 2008.
- [10] M. Friedrich, C. Bednarz, and M. Leone, "Improved expression for the via-plate capacitance based on the magnetic-frill model," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 6, pp. 1362–1364, Dec. 2013.
- [11] Y. J. Zhang and J. Fan, "An intrinsic circuit model for multiple vias in an irregular plate pair through rigorous electromagnetic analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 8, pp. 2251–2265, Aug. 2010.
- [12] Y.-J. Zhang, E.-P. Li, A. Chada, and J. Fan, "Calculation of the via-plate capacitance of a via with pad using finite difference method for signal/power integrity analysis," in *Proc. Int. Electromagn. Compat. Symp.*, Jul. 2009, pp. 20–24.