

Mode-Decomposition-Based Equivalent Model of High-Speed Vias up to 100 GHz

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Abstract—Via transitions in high-speed channels critically influence the signal integrity and power integrity of high-speed systems. In this article, a mode-decomposition-based equivalent model of a high-speed via that can be applied at frequencies up to 100 GHz is proposed for the first time. The equivalent model for modeling the via transition consists of upper and lower via-to-plate capacitances and equivalent parallel-plate impedances, owing to the fundamental mode and higher order modes for parallel-plate, all of which can be calculated from physical geometrical parameters. The via-to-plate capacitances are calculated by using the domain decomposition method in the antipad domain and via domain. The parallel-plate impedances representing via and parallel-plate coupling are calculated with the mode decomposition method for different parallel-plate modes (fundamental and higher order modes) in the parallel-plate domain. The proposed equivalent via model provides more accurate results in the high-frequency range than previously proposed methods. Because the impact of higher order modes on parallel-plate impedance is considered in the proposed mode-decomposition-based via model, and the effects of higher order modes are prominent at high frequencies for printed circuit board (PCB) vias with typical dimensions. The proposed model is validated with numerical examples, which show good correlation at frequencies as high as 100 GHz. The proposed model can be applied to high-speed via transitions in PCBs and packages.

Index Terms—Higher order mode, high-speed channel, mode-decomposition equivalent model, parallel plate, via.

I. INTRODUCTION

VERTICAL interconnectors, more commonly known as vias, play essential roles in modern high-speed digital systems for connecting signals in multilayer printed circuit boards (PCBs) and packages [1]. With increases in the number of integrated devices and the requirement for higher densities, vias have become ubiquitous in multilayer PCBs. Vias are used to route signals on different layers for different channels, which are typical discontinuous components in high-speed channels and can lead to severe signal integrity and power integrity problems.

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Therefore, accurate modeling of these interconnect components is necessary for high-speed channel design and optimization.

Various methods of via modeling have been developed in recent decades, including full-wave solvers based on the finite-difference time-domain method, finite-element method [2], [3], multiple scattering methods [4], [8], analytical and semianalytical approaches [9], [10], and equivalent circuit methods [16]. Full-wave solvers can provide accurate simulation results, but they require substantial computational power and time to simulate a multilayer board with many vias. Multiple scattering methods based on the Foldy–Lax approach have been used to model dense vias with rectangular ground plates [5], [6]. Improved multiple methods have been introduced for dense bias modeling with arbitrarily or irregularly shaped ground plates [7], [8]. In one study [8], the general multiple scattering method was proposed to model dense vias with axially anisotropic modes in an arbitrarily shaped plate pair. But it was only validated up to 50 GHz. In addition, the separation between vias and the distance of vias to plate edges should be sufficiently large to neglect the coupling of them by the higher order evanescent modes for saving the computational time. Analytical or semianalytical approaches can also be used to model dense vias with arbitrarily shaped plate pairs [9], [10], [12]; however, their upper frequency is limited, and these approaches do not provide sufficient physical insight for channel designers at higher bandwidths. Equivalent modeling methods of differential vias based on the PEEC method have been introduced [13], [14], [15]. In the equivalent circuit method, a via with parallel plates is first modeled by a π -type circuit with lumped elements [16], [17]. The associated models enable highly efficient simulation because the circuit elements can be calculated from analytical formulas. The topology of an equivalent circuit model provides physics-based insight for guidance in designing vias. To improve the accuracy of equivalent circuits, physics-based equivalent models have been proposed [18], [19], which use the parallel-plate impedance, Z_{pp} , to model the interconnection between the via and plates, on the basis of the fundamental mode (propagating mode) in parallel plates. The physics-based via model has been verified with measurements [20], [21]. In [22], and the capacitance coupling between the via and the parallel plate is represented by the transmission model. The closed-form expression of the parallel-plate impedance, Z_{pp} , due to the fundamental mode, has been analyzed in multiple studies [23], [24]. The fundamental parallel-plate mode is considered only for parallel-plate impedance calculation [25], [26], [27], [28]. On the basis of the

parallel-plate impedance, the inductance interaction of the via to the parallel plate can be extracted for power-ground plane design [29], [30]. Via modeling with the lossy material in real applications has been analyzed in [31] and [32]. To extend the physics-based via model for high-frequency applications, the higher order modes of the parallel plate have been introduced in [23], [24], and [33]. However, the physics-based via models still cannot work in the high-frequency range above 20 GHz for arbitrary types of vias, because an accurate consideration of higher order modes (nonpropagating/evanescent modes) in the vicinity of the via becomes critical with increasing cavity height and frequency [35], [37]. Williamson [24] and Zhang and Fan [23] have proposed more complex equivalent circuits for via structures by considering higher order modes in the vicinity of the via domain. However, extracting the circuit elements for the two models is complex, and the circuit models are not accurate beyond 40 GHz for typical PCB via dimensions [36]. Hybrid two-dimensional/three-dimensional finite-element methods have also been proposed to model vias with differently shaped antipads, to maintain accuracy while improving computational efficiency [38], [39], [40]. However, these approaches remain more time-consuming than equivalent circuit methods.

Herein, we propose mode-decomposition-based equivalent model for the via structure, which considers higher order modes in the parallel-plate domain, on the basis of mode decomposition. The mode decomposition method used herein differs from the previous use of modal decomposition [11] to separately model the parallel-plate mode and the strip-line mode. Our decomposition method separates the higher order modes from the fundamental mode of the parallel-plate modes. The equivalent model includes via-plate capacitance and parallel-plate impedance, owing to different parallel-plate modes, corresponding to different domains of the via structure. In contrast to the conventional physics-based via model, the higher order modes in the parallel-plate domain are also modeled by using a higher order mode impedance, Z' , herein. All elements of the proposed equivalent model can be calculated from the physical parameters of the via structure. The key contributions of this article can be summarized as follows.

- 1) A mode-decomposition-based equivalent model for high-speed via is proposed. The equivalent model for higher order modes in the parallel-plate domain is analyzed, and the higher order mode impedance is used to model the interaction between the via and plates, for the first time. The higher order mode impedance is calculated with the mode decomposition method.
- 2) The field distribution and modes are analyzed. The physical meaning for all elements of the via equivalent model is analyzed and explained on the basis of the electric field distribution, thus greatly facilitating via design and optimization.
- 3) Full-wave simulations are presented to verify the proposed mode-decomposition-based equivalent model of a high-speed via up to 100 GHz.

The proposed equivalent model can predict S -parameters of via structures in the high-frequency range, and the results are

compared with those of previous methods [20], [24], [36]. The remainder of this article is organized as follows. Section II details the proposed equivalent model and the formulas for via-plate capacitances and parallel-plate impedances. Fields and mode analysis are described in Section III to show the physical meaning of the equivalent model and why higher order modes should be considered. Higher order modes are shown to exist in the vicinity of the via between parallel plates and may be prominent at high frequencies. Section IV presents simulation examples verifying the accuracy and applicability of the proposed equivalent model, and conclusions are given in Section V.

II. PROPOSED MODELING METHOD

On the basis of the conventional physics-based method, a via can be modeled by using a π -type equivalent circuit with two capacitors and the parallel-plate impedance [20], [36]. Fig. 1 shows the proposed equivalent model for the fundamental cell of a via, which corresponds to via segments crossing a cavity enclosed by two reference plates. The equivalent model includes two capacitors and the parallel-plate impedance Z_{p0} and Z' . Z_{p0} and Z' arise from the fundamental mode and higher order modes in the parallel-plate domain, respectively. Two capacitors represent the coupling between the via and the top or bottom plate. Unlike the conventional physics-based model, the proposed equivalent model considers the effects of higher order modes, thereby allowing for more accurate modeling of the via at high frequencies.

A. Via-Plate Capacitance

In Fig. 1, C_t and C_b are the via-top plate capacitance and via-bottom plate capacitance, respectively. The via-plate capacitance consists of the coaxial capacitance of the antipad and the via barrel-plate capacitance, according to domain decomposition. Many methods have been developed for calculating the via-plate capacitance of a via structure [41], [42], [43], [44], [45]. Herein, the antipad capacitance and via barrel-plate capacitance are calculated as follows.

A transverse electromagnetic coaxial mode can be assumed in the antipad aperture [41]. The antipad capacitance can be calculated by

$$C_a = \frac{2\pi\epsilon_0\epsilon_r t}{\ln\left(\frac{r_a}{r_p}\right)} \quad (1)$$

where r_a and r_p are the antipad and pad radii, respectively; ϵ_0 and ϵ_r are the free space permittivity and relative permittivity, respectively; and t is the plate thickness.

The via barrel-plate capacitance can be calculated from the magnetic frill current [43] as

$$C'_b = \frac{j4\pi^2\epsilon_0\epsilon_r}{\left(\ln\left(\frac{r_a}{r_p}\right)\right)^2 h} \sum_{n=1,3,5}^{\infty} \frac{\tilde{K}_n}{\tilde{k}_n} \quad (2)$$

where

$$\tilde{k}_n = -\frac{jn\pi}{h} \quad (3)$$

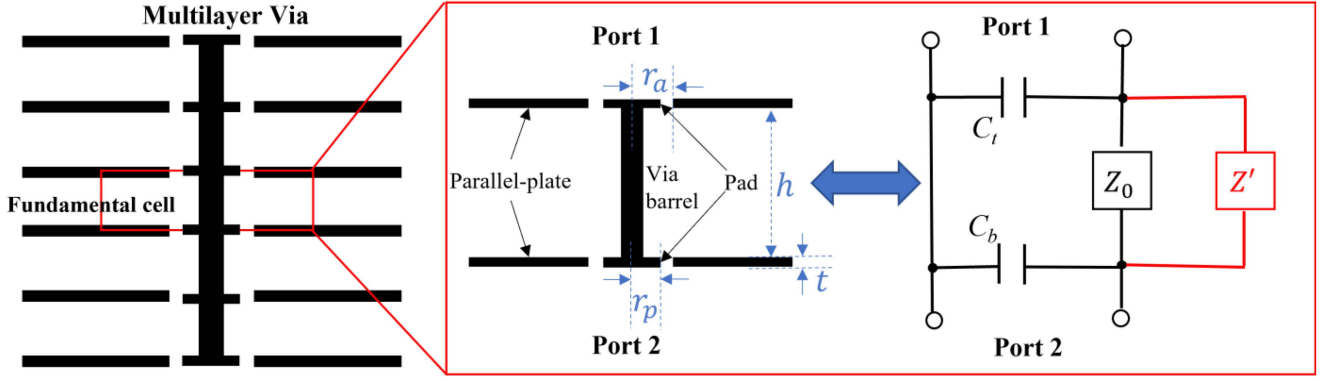


Fig. 1. Proposed equivalent model of the via (fundamental cell).

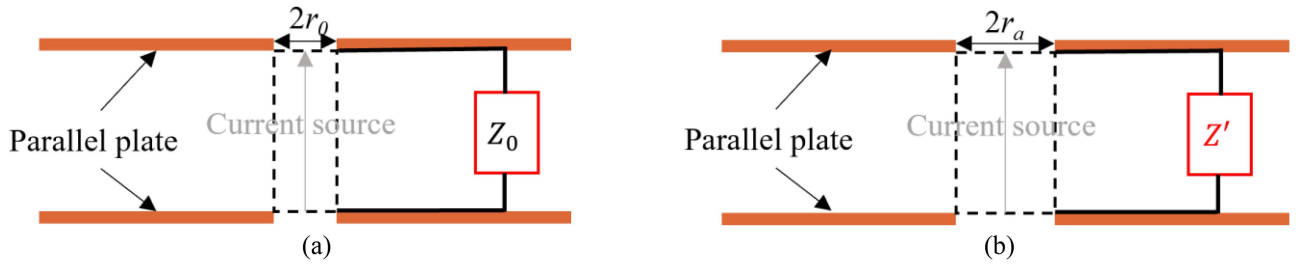


Fig. 2. Equivalent mode of parallel plate impedance based on mode decomposition (\$r_0\$ and \$r_a\$ are the via and antipad radii, respectively, and \$Z_0\$ and \$Z'\$ are the parallel-plate impedance due to the fundamental mode and higher order modes in the parallel-plate domain, respectively). (a) Equivalent model for the fundamental mode. (b) Equivalent model for higher order modes.

$$\tilde{K}_n = \frac{1}{\tilde{k}_n} \times \left(-H_0^2 \left(\tilde{k}_n r_p \right) J_0 \left(\tilde{k}_n r_p \right) + 2H_0^2 \left(\tilde{k}_n r_a \right) J_0 \left(\tilde{k}_n r_p \right) + \frac{J_0 \left(\tilde{k}_n r_0 \right)}{H_0^2 \left(\tilde{k}_n r_0 \right)} \left(H_0^2 \left(\tilde{k}_n r_a \right) - H_0^2 \left(\tilde{k}_n r_p \right) \right)^2 \right). \quad (4)$$

Here, \$h\$ and \$r_0\$ are the dielectric height and via radius, respectively, and \$H_0^2\$ and \$J_0\$ are the zero-order Hankel function of the second kind and the zero-order Bessel function, respectively.

The via-top plate capacitance and via-bottom plate capacitance are represented as

$$C_t = C_b = C_a + C'_b \quad (5)$$

B. Parallel-PLATE IMPEDANCE for the Fundamental Mode

In the conventional via modeling method, the parallel-plate impedance \$Z_{p0}\$ represents coupling between the via and parallel-plate due to fundamental mode. As shown in Fig. 2(a), the equivalent model for the fundamental mode consists of a current source and a parallel plate. The radius of the current source is the same as the via radius; thus, the fundamental mode is excited at the via boundary. When the parallel plate is infinitely large, or the boundary condition of the plate consists of perfectly matched layers (PMLs), the parallel-plate impedance \$Z_{p0}\$ can

be calculated as [30], [31]

$$Z_{p0} = \frac{V_0}{I_0} = \frac{-E_z^0 h}{2\pi r_0 H_0^0} \quad (6)$$

where \$V_0\$ and \$I_0\$ are the voltage and current at the via-barrel boundary due to the fundamental mode; \$h\$ is the dielectric height in the parallel plate; and \$E_z^0\$ and \$H_0^0\$ represent the electric and magnetic fields at the via-barrel boundary due to the fundamental mode:

$$E_z^0(r_0) = k_0^2 a_0 H_0^2(k_0 r_0) \quad (7)$$

$$H_0^0(r_0) = j\omega\epsilon_0\epsilon_r k_0 a_0 H_1^2(k_0 r_0). \quad (8)$$

Here, \$k_0 = k' - jk''\$, which is a complex wavenumber; \$k' = \omega\sqrt{\mu_0\epsilon_0\epsilon_r}\$; \$k'' = \omega\sqrt{\mu_0\epsilon_0\epsilon_r}(\tan\delta + \frac{d_s}{h})/2\$; \$\omega\$ is the angular frequency; \$\mu_0\$ is the permeability of free space; \$\tan\delta\$ is the loss tangent of the material; \$d_s = \sqrt{2/\omega\mu_0\sigma}\$ is the skin depth of the conductor with conductivity of \$\sigma\$; \$a_0\$ is a constant coefficient that does not need to be determined; and \$H_1^2\$ is the first-order Hankel function of the second kind. The derivation of (7) and (8) is detailed in the appendix.

If the parallel plate is finite, or the boundary condition of the plate is a perfect electric or magnetic conductor (PEC or PMC) boundary, the parallel-plate impedance \$Z_{p0}\$ can be calculated with the cavity method [34]. The closed-form expression for the

parallel-plate impedance of a rectangular plate pair is given as

$$Z_{p0} = \frac{j\omega\mu_0 h}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{C_m^2 C_n^2 f_{bc} f_p}{k_{mn}^2 - k_0^2} \quad (9)$$

where a and b are the dimensions of the rectangular parallel plate; μ is the permeability of the dielectric material between the plates; $k_{mn} = \sqrt{(m\pi/a)^2 + (n\pi/b)^2}$; and m and n represent the mode number. In addition, C_m and $C_n = 1$ when m and $n = 0$; otherwise, C_m and $C_n = \sqrt{2}$. f_p and f_{bc} are terms correlated with the dimensions and shape of the via and the plate, respectively [33].

On the basis of the assumption that the via is circular, and the plate is rectangular, f_p and f_{bc} are expressed as follows:

$$f_p = J_0(k_{mn}r_0)^2 \quad (10)$$

$$f_{bc} = \begin{cases} \cos^2\left(\frac{m\pi x}{a}\right) \cos^2\left(\frac{n\pi y}{b}\right) & \text{PMC boundary} \\ \sin^2\left(\frac{m\pi x}{a}\right) \sin^2\left(\frac{n\pi y}{b}\right) & \text{PEC boundary} \end{cases} \quad (11)$$

where $x = a/2$, $y = b/2$, and f_{bc} differs when the boundary of the parallel plate is either a PMC or PEC boundary.

C. Parallel-Plate Impedance for Higher Order Modes

The parallel-plate impedance due to higher order modes can be calculated with mode decomposition. When the waves enter the domain of the parallel plate, the higher order modes can be excited at the antipad boundary, which is discontinuous. The equivalent model for higher order modes is shown in Fig. 2(b). The model contains an equivalent current source and a parallel plate, similarly to the equivalent model for the fundamental mode. The radius of this equivalent source is the same as the antipad radius; thus, the higher order modes are excited at the antipad boundary. Similarly to the parallel-plate impedance of the fundamental mode, the higher order mode impedance can also be calculated by using the voltage and current at the antipad boundary due to the higher order modes

$$Z' = \frac{V_a}{I_a}. \quad (12)$$

Here, V_a and I_a are the voltage and current at the antipad boundary due to the higher order modes in the parallel-plate domain. These terms can be calculated according to the electric fields and magnetic fields at the antipad boundary. For the higher order modes, only TM_{0n} modes are considered herein. Because the via structure considered is a circle, which is symmetric, and only TM_{0n} modes (higher order modes/axially isotropic modes) are excited [7], [8]. The total electric and magnetic fields E_z^N and H_θ^N from TM_{0n} modes at the antipad boundary are expressed as

$$E_z^N(r_a, z) = \sum_{n=1}^N k_n^2 (a_0 H_0^2(k_n r_a)) \cos \frac{n\pi z}{h} \quad (13)$$

$$H_\theta^N(r_a, z) = \sum_{n=1}^N j\omega\epsilon_0\epsilon_r k_n (a_0 H_1^2(k_n r_a)) \cos \frac{n\pi z}{h} \quad (14)$$

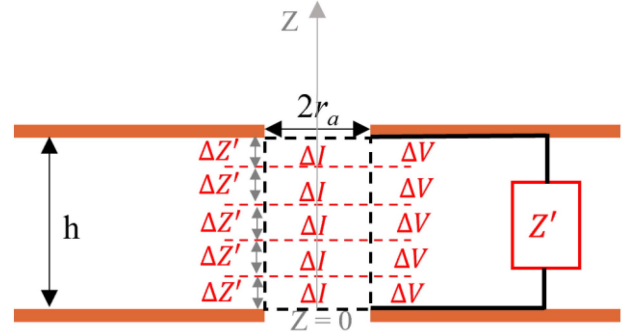


Fig. 3. Current source of the equivalent model for high-order modes is discretized.

where $k_n = \sqrt{k_0^2 - (n\pi/h)^2}$; n represents the mode number; N is the total number of higher order modes considered for the via modeling; and z is the coordinate in the vertical direction. The derivation of (13) and (14) is detailed in the appendix.

According to (13) and (14), electric fields and magnetic fields from higher order modes vary along the z -axis. To accurately calculate the Z' at antipad boundary from higher order modes, the discretization method is used herein. The current source is discretized into small parts, as shown in Fig. 3. For any small discretized current source, the corresponding impedance can be calculated as

$$\Delta Z' = \frac{\Delta V}{\Delta I} = \frac{\int_0^{\Delta z} E_z^N(r_a, z) dz}{\int_0^{2\pi} H_\theta^N(r_a, z) d\theta} = \frac{E_z^N(r_a, z) \times \Delta z}{2\pi r_a H_\theta^N(r_a, z)}. \quad (15a)$$

When Δz is sufficiently small, e.g., Δz is less than 5% of the wavelength pertinent to the maximum frequency, the electric fields and the magnetic fields can be considered constant in the length of Δz . Thus, the integration (15a) can be rewritten as

$$\begin{aligned} \Delta Z' &= \frac{E_z^N(r_a, z) \times \Delta z}{2\pi r_a H_\theta^N(r_a, z)} \\ &= \frac{\sum_{n=1}^N k_n^2 (a_0 H_0^2(k_n r_a)) \times \Delta z}{2\pi r_a \sum_{n=1}^N j\omega\epsilon_0\epsilon_r k_n (a_0 H_1^2(k_n r_a))}. \end{aligned} \quad (15b)$$

The variable of $\cos \frac{n\pi z}{h}$ in the field expression of higher order modes is eliminated in (15b). Then, for the total current source, the serialized impedance is calculated by integration as

$$Z' = \frac{h \sum_{n=1}^N k_n H_0^2(k_n r_a)}{j2\pi r_a \omega\epsilon_0\epsilon_r \sum_{n=1}^N H_1^2(k_n r_a)}. \quad (16)$$

The fundamental cell of the via model, as illustrated in Fig. 1, is modeled by using the capacitance and parallel-plate impedance due to different parallel-plate modes, according to the domain decomposition method. From the mode decomposition method, the impedance due to different parallel-plate modes is modeled with different equivalent models. The proposed new mode-decomposition-based equivalent model is more accurate at high frequencies than the conventional physics-based circuit

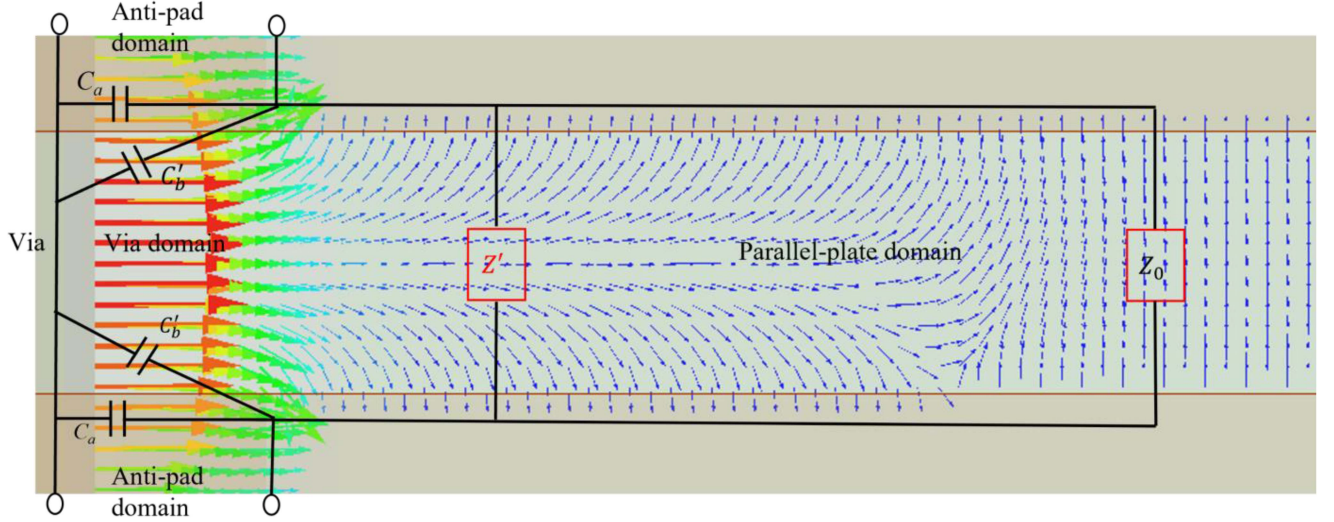


Fig. 4. Simulated electric field distribution at 100 GHz in a via structure by HFSS and corresponding electrical elements, according to the domain decomposition method and mode decomposition method ($r_0 = 4$ mil, $r_a = 15$ mil, $h = 15.3$ mil, and PML boundary for the parallel plate).

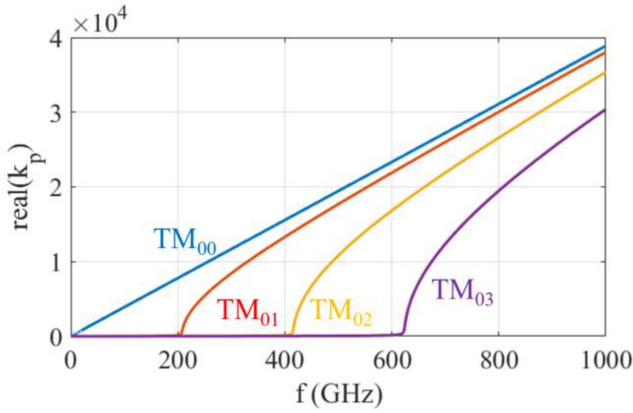


Fig. 5. Cut-off frequencies of TM_{00} , TM_{01} , TM_{02} , and TM_{03} mode for a fundamental cell of a via with dielectric material of $\epsilon_r = 3.68$, $\tan\delta = 0.02$, $r_0 = 4$ mil, $r_a = 15$ mil, $h = 15.3$ mil, PML boundary for the parallel plate.

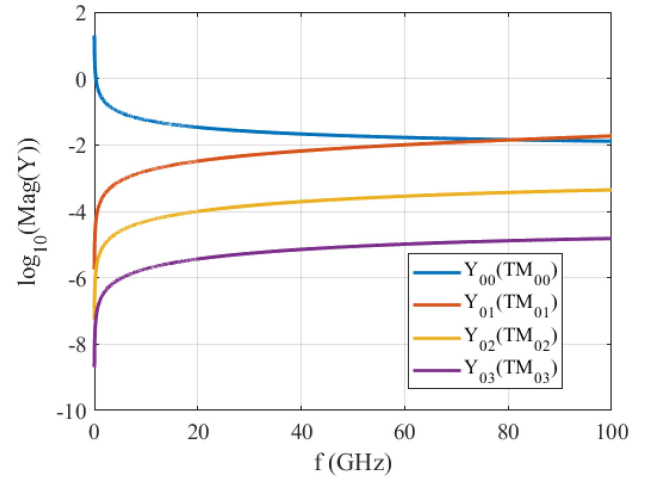


Fig. 6. Comparison of admittance from different parallel-plate modes for the via model of case 1 ($Y_0 = 1/Z_0$ and $Y' = 1/Z'$): magnitude of Y_0 and Y' for different parallel-plate modes ($r_0 = 4$ mil, $r_a = 15$ mil, $h = 15.3$ mil, $\epsilon_r = 3.68$, $\tan\delta = 0.02$, PML boundary for the parallel plate).

model, because it considers the effects of higher order modes, which may be prominent in the high-frequency range.

III. FIELD AND MODE ANALYSIS

An electric field distribution simulated by high-frequency simulation software (HFSS) at 100 GHz is shown in Fig. 4. As shown, a transverse electromagnetic mode arises in the antipad domains of the top and bottom parts, which can be represented by the via-to-plate capacitance C_a [41]. In the via-hole domain, the fields should be modeled by using the capacitance C'_b of the via barrel to the top and bottom plates [23], [41]. In the parallel-plate domain, the fundamental mode and higher order modes of parallel-plate exist. The fundamental mode is a propagating mode, whereas the higher order modes are evanescent modes that quickly vanish with propagating distance, thereby explaining why higher order modes are observed only in the vicinity of the via domain. The parallel-plate impedance Z_0 represents the

fundamental mode. Meanwhile, the parallel-plate impedance Z' is used to model higher order modes. In Fig. 4, the fields are modeled with corresponding electrical elements. In the conventional physics-based equivalent model, only the fundamental mode is considered for low-frequency modeling. However, higher order modes may be dominant in the high-frequency range. Therefore, the proposed model is more accurate at high frequencies.

Fig. 5 shows the propagation constant in the ρ direction for some primary transverse magnetic (TM) modes. The cut-OFF frequency for higher order modes (TM_{01} , TM_{02} , and TM_{03}) is very high. Even for the TM_{01} mode, the cut-OFF frequency is beyond 200 GHz. This result indicates that those higher order modes are evanescent and cannot propagate in the ρ direction. This finding also explains why these modes are observed only in the vicinity of the via domain.

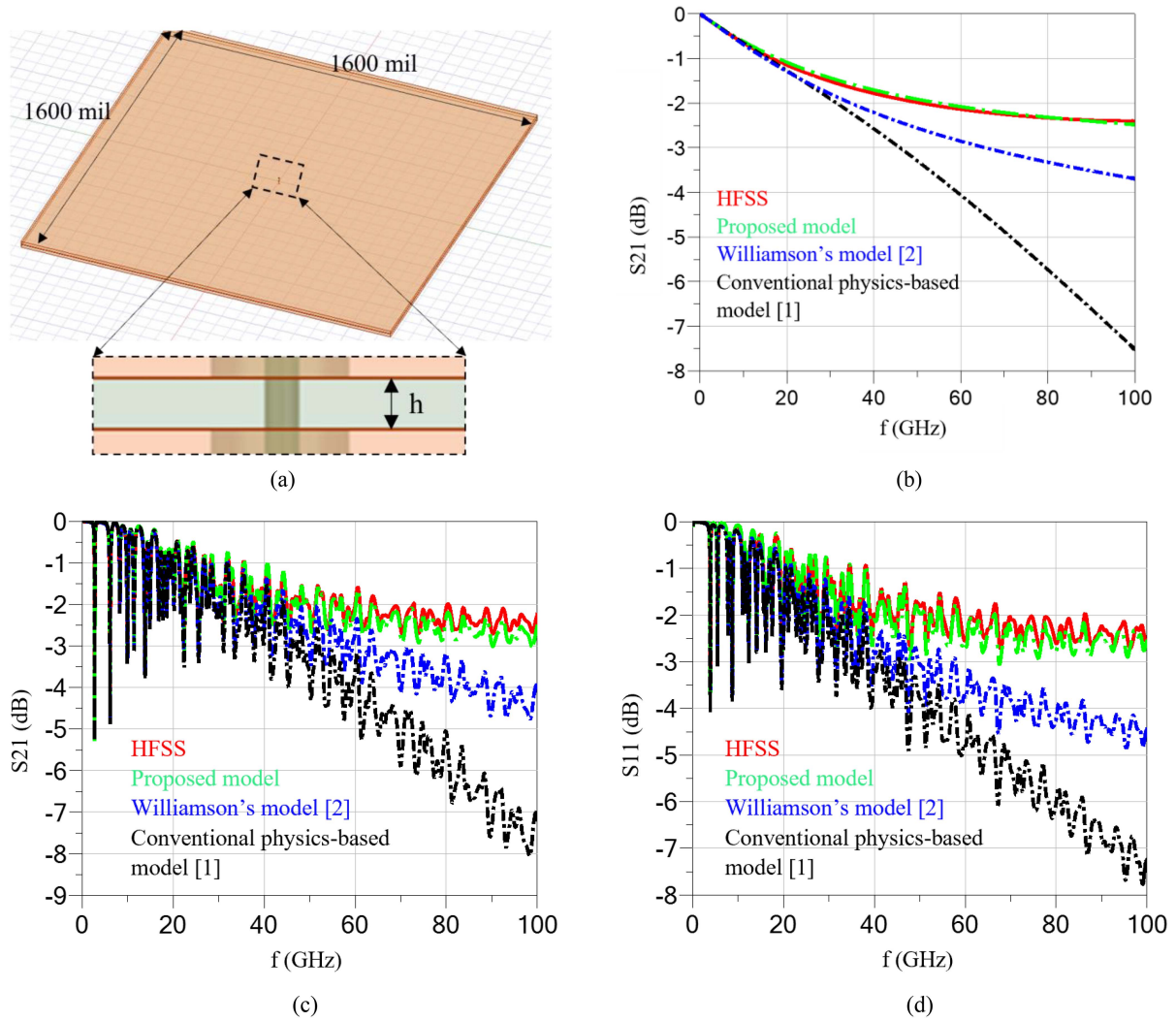


Fig. 7. Case 1: via model with two plates. (a) Cross-sectional view of the via model. (b) Insertion loss comparison for a PML boundary. Case 1: via model with two plates. (c) Insertion loss comparison for a PEC boundary. (d) Insertion loss comparison for a PMC boundary.

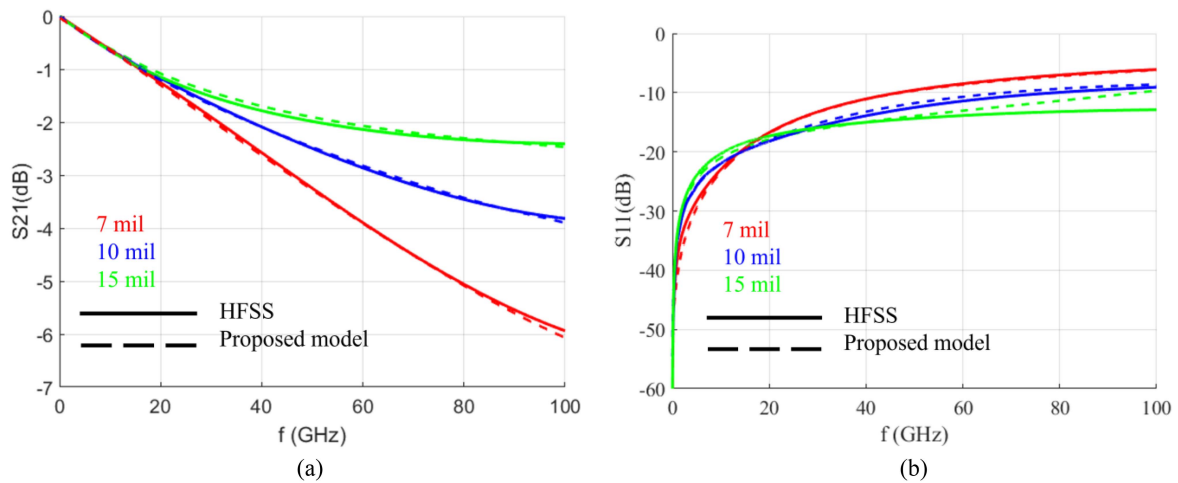


Fig. 8. Case 2: S-parameter comparison for different antipad radii (PML boundary). (a) Insertion loss comparison. (b) Return loss comparison.

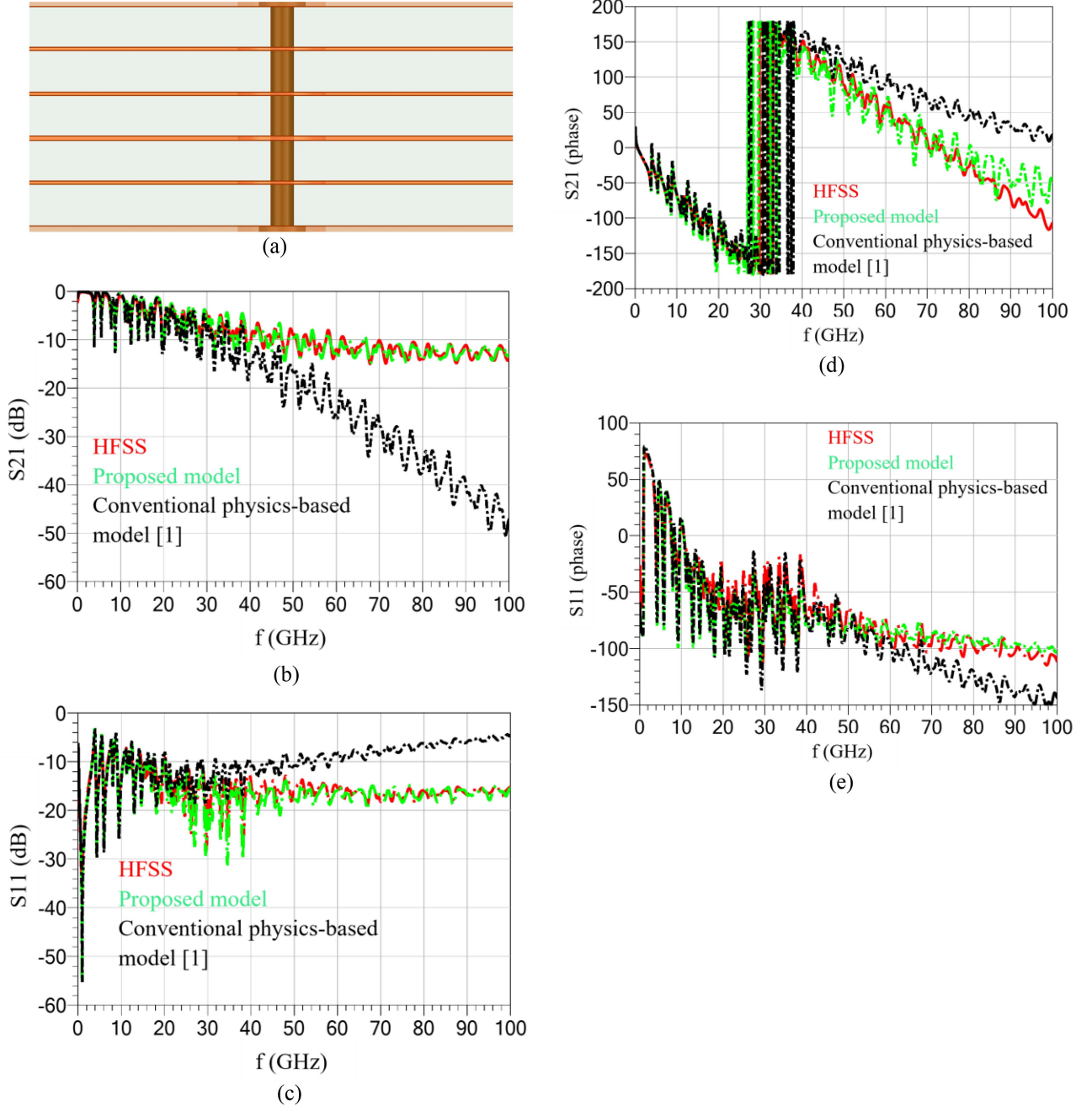


Fig. 9. Case 3: via model with six layers (PMC boundary). (a) Cross-sectional view of the via model. (b) Insertion loss comparison. (c) Return loss comparison. (d) Phase comparison of insertion loss. (e) Phase comparison of return loss.

The admittance $Y = 1/Z$ from different parallel-plate modes for the via model of case 1 in the numerical examples section is compared in Fig. 6. The admittance Y is detailed in the appendix. The higher order mode admittance is very small with respect to the fundamental mode admittance at frequencies below 20 GHz. However, the higher order mode admittance can reach the same level as the fundamental mode admittance at high frequencies. This finding supports our analysis result showing that higher order modes can be prominent in the high-frequency range. As shown in Fig. 6(b), the contribution to the parallel-plate

admittance from the higher order modes decreases as the mode order increases, in agreement with the properties of higher order modes. Thus, (15) and (16) can converge very rapidly. For the via model considered in this article, the impedance due to the TM_{01} mode is dominant, and a parallel-plate mode coefficient N of 3 is chosen, which is sufficient.

IV. NUMERICAL EXAMPLES

In this section, the proposed equivalent model of a via is verified with numerical simulations. A simple case for a via with

two plates is first examined. Subsequently, models with different antipad radii are shown to present the applicable range of the proposed model. Finally, a model with multiple plates is shown to present the efficiency of the proposed model. Comparisons of S -parameter results from different methods and simulations for different models indicate the accuracy of the proposed method, particularly at frequencies above 40 GHz.

Case 1 is a fundamental case consisting of a via with two layers. This model represents a fundamental cell for a via model with multiple plates. The insertion loss of the via for different boundary conditions is compared in Fig. 7. Fig. 7(a) shows the cross-section of the via model for a rectangular plate with dimensions of 1600 mil by 1600 mil. The via radius r_0 is 4 mil, the antipad radius r_a is 15 mil, the plate thickness t is 1.3 mil, and the parallel-plate cavity height h is 15.3 mil. The relative permittivity ϵ_r and the loss tangent of material are 3.68 and 0.02 at 1 GHz with Djordjevic model. The conductivity of the copper plate is 5.8×10^7 . Fig. 6(b)–(d) shows insertion loss comparisons for a via with PML, PEC, and PMC boundaries, respectively, according to different methods and HFSS. A large difference is observed between the conventional physics-based model [20] and HFSS for all boundary cases at frequencies above 20 GHz. Williamson's model [24], as compared with the conventional physics-based model, improves the results, but still cannot work in a high frequency range above 40 GHz. However, the results from the proposed model match the simulation results very well throughout the entire frequency range as high as 100 GHz for all three boundary cases. For the PEC and PMC boundary cases, the resonance of insertion loss due to a finite plate size is also accurately predicted throughout the entire frequency range.

To further verify the applicable range of the proposed equivalent model, the antipad radius was swept from 7 to 15 mil in case 2, which is based on the model in case 1. Fig. 8(a) shows insertion loss comparisons for HFSS and the proposed circuit model for different antipad radii. An excellent correlation is shown for all cases. For the return loss comparison shown in Fig. 8(b), the results of the proposed circuit match well with the simulation results when the antipad radius is 7 or 10 mil. However, when the antipad radius increases to 15 mil, the return loss does not match well at frequencies above 70 GHz. However, the results from the proposed model remain better than the results from a conventional physics-based model. When the antipad radius is very large, mode conversion at the antipad boundary is more complex, and via self-inductance should be considered. We will focus on this situation in a future publication.

Case 3 is a via model with six layers. The geometry and dimensions of the via and plate in this model are the same as those in case 1. Thus, case 3 is a layered extension of case 1. On layers 1 and 6, there are pads of radius with radius of 8 mil. The insertion loss and return loss of the via for the PMC boundary condition are compared in Fig. 9. A cross-sectional view of the via with six layers is shown in Fig. 9(a). Fig. 9(b) and (c) compare the insertion loss and return loss, respectively. The conventional physics-based circuit method is accurate only up to 30 GHz, but the results from the proposed model match the full-wave simulation results throughout the entire frequency range, up to 100 GHz. The computational memory and time cost of case 3 are compared between the proposed model and the HFSS, run on a

server with 3.45 GHz CPU speed and 512 GB memory. HFSS simulated the model of case 3 with 29.5 GB memory in 11.5 h, whereas the proposed method required only 256 MB memory and 10.5 s. It validates that the proposed method is more efficient than full wave simulation.

V. CONCLUSION

A mode-decomposition-based equivalent model of a high-speed via is first proposed for the first time in this article and is shown to provide accurate results up to 100 GHz. In our model, in contrast to the conventional physics-based via model [20], higher order modes in the parallel-plate domain improve the accuracy of the model of the via at high frequencies. On the basis of the domain decomposition method, the via structure can be divided into an antipad domain, via domain, and parallel-plate domain. We use different equivalent electrical elements to model each domain. The capacitance values between the via and plates represent the fields in the antipad and via domain. A fundamental mode (propagating mode TM_{00}) and higher order modes (evanescent modes TM_{0n}) are considered in the parallel-plate domain. The parallel-plate impedance Z and Z' for different parallel-plate modes is used to model the interactions between the via and plates, which are calculated with the mode decomposition method. From the field distribution and mode analysis, we find that the higher order modes in the parallel-plate domain can be dominant at high frequencies. This finding explains why the proposed equivalent model is more accurate than the conventional physics-based model, and also provides a physical meaning that should be useful in via design and optimization.

Numerical examples were used to verify the proposed model. Only cases of a single-via model were analyzed and verified to avoid the effects of other vias and traces. Full-wave simulation (HFSS) results validated the superior accuracy and applicability of the proposed equivalent model to those of the conventional physics-based model and Williamson's model, particularly at high frequencies. Meanwhile, the electrical elements in the proposed circuit can be easily extracted on the basis of the physical parameters of the via, in contrast to the equivalent circuits proposed by Williamson [24] and Zhang and Fan [23]. The applicable range of the proposed method was determined by sweeping of the antipad size. The insertion loss can be accurately predicted when the ratio of the antipad radius to the via radius is between 1.75 and 3.75. When the antipad radius is significantly larger than the via radius, the insertion loss can still be predicted accurately by the proposed model, whereas the return loss has a poor correlation above 70 GHz between the proposed model and HFSS simulation. In addition, the proposed method has better performance than the conventional physics-based method. We will investigate this situation in a future publication.

On the basis of the analysis herein, the proposed analytical model is useful up to 100 GHz, particularly for cases with a longer via length and smaller antipad radius to the via barrel radius ratio. The proposed parallel-plate impedance could also be applied to model an arbitrary number of vias when the distance between vias is sufficiently large, such that the evanescent parallel-plate modes from one via do not affect neighboring vias.

A mode-decomposition-based equivalent model for multiple vias that considers higher order modes will be introduced in a future publication.

APPENDIX

The formulas below show general expressions of electric and magnetic fields in cylindrical coordinates for a radial parallel-plate waveguide. The details of their derivation have been described in the book [46].

For the TE_{mn}^z modes

$$H_\rho = -jk_z k_\rho \left(a_0 H_m^{2'}(k_\rho \rho) + a_1 H_m^{1'}(k_\rho \rho) \right) \cos(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A1})$$

$$H_\theta = jk_z \frac{m}{\rho} \left(a_0 H_m^2(k_\rho \rho) + a_1 H_m^1(k_\rho \rho) \right) \sin(m\theta) \cos \frac{n\pi z}{h} \quad (\text{A2})$$

$$H_z = -jk_\rho^2 \left(a_0 H_m^2(k_\rho \rho) - a_1 H_m^1(k_\rho \rho) \right) \cos(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A3})$$

$$E_\rho = \omega \mu_0 \frac{m}{\rho} \left(a_0 H_m^2(k_\rho \rho) - a_1 H_m^1(k_\rho \rho) \right) \sin(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A4})$$

$$E_\theta = \omega \mu_0 k_\rho \left(a_0 H_m^{2'}(k_\rho \rho) - a_1 H_m^{1'}(k_\rho \rho) \right) \cos(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A5})$$

$$E_z = 0. \quad (\text{A6})$$

For the TM_{mn}^z modes,

$$E_\rho = -k_z k_\rho \left(a_0 H_m^{2'}(k_\rho \rho) + a_1 H_m^{1'}(k_\rho \rho) \right) \cos(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A7})$$

$$E_\theta = k_z \frac{m}{\rho} \left(a_0 H_m^2(k_\rho \rho) + a_1 H_m^1(k_\rho \rho) \right) \sin(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A8})$$

$$E_z = k_\rho^2 \left(a_0 H_m^2(k_\rho \rho) + a_1 H_m^1(k_\rho \rho) \right) \cos(m\theta) \cos \frac{n\pi z}{h} \quad (\text{A9})$$

$$H_\rho = -j\omega \varepsilon_0 \varepsilon_r \frac{m}{\rho} \left(a_0 H_m^2(k_\rho \rho) + a_1 H_m^1(k_\rho \rho) \right) \sin(m\theta) \cos \frac{n\pi z}{h} \quad (\text{A10})$$

$$H_\theta = -j\omega \varepsilon_0 \varepsilon_r k_\rho \left(a_0 H_m^{2'}(k_\rho \rho) + a_1 H_m^{1'}(k_\rho \rho) \right) \cos(m\theta) \cos \frac{n\pi z}{h} \quad (\text{A11})$$

$$H_z = 0 \quad (\text{A12})$$

where $k_\rho = \sqrt{k_0^2 - (n\pi/h)^2}$ is the wavenumber in the ρ -direction; $k_z = n\pi/h$ is the wavenumber in the z -direction; a_0 and a_1 are constant coefficients; the Hankel functions of the first kind H_m^1 represent radial waves propagating in the negative ρ -direction; and the Hankel functions of the second kind H_m^2 describe radial waves propagating in the positive ρ -direction.

On the basis of the assumption that the parallel plate is infinite, only radial waves propagate in the positive ρ -direction. Thus, the Hankel functions of the first kind H_m^1 should be eliminated

and consequently, $a_1 = 0$. For TM_{0n}^z modes, the expression of electric and magnetic fields can be simplified from (23) to (28) as

$$E_\rho = k_z k_\rho \left(a_0 H_0^2(k_\rho \rho) \right) \cos(m\theta) \sin \frac{n\pi z}{h} \quad (\text{A13})$$

$$E_\theta = 0 \quad (\text{A14})$$

$$E_z = k_\rho^2 \left(a_0 H_0^2(k_\rho \rho) \right) \cos \frac{n\pi z}{h} \quad (\text{A15})$$

$$H_\rho = 0 \quad (\text{A16})$$

$$H_\theta = j\omega \varepsilon_0 \varepsilon_r k_\rho \left(a_0 H_1^2(k_\rho \rho) \right) \cos \frac{n\pi z}{h} \quad (\text{A17})$$

$$H_z = 0. \quad (\text{A18})$$

For the case of a finite parallel plate, the waves of higher order modes still propagate only in the positive ρ -direction. Because the higher order modes are evanescent, they cannot reach the edge of the parallel plate to produce waves in the negative ρ -direction.

The equations of admittance for higher order modes (TM_{01} , TM_{02} , and TM_{03}) are as follows:

$$Y' = \sum_{p=1}^{\infty} Y'_{0p} = \frac{1}{Z'} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \sum_{p=1}^{\infty} (H_1^2(k_p r_a))}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))} \quad (\text{A19})$$

$$Y'_{01} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r (H_1^2(k_1 r_a))}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))} \quad \text{for } TM_{01} \text{ mode} \quad (\text{A20})$$

$$Y'_{02} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r (H_1^2(k_2 r_a))}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))} \quad \text{for } TM_{02} \text{ mode} \quad (\text{A21})$$

$$Y'_{03} = \frac{j2\pi r_a \omega \varepsilon_0 \varepsilon_r (H_1^2(k_3 r_a))}{h \sum_{n=1}^{\infty} k_n (H_0^2(k_n r_a))} \quad \text{for } TM_{03} \text{ mode.} \quad (\text{A22})$$

REFERENCES

- [1] S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices*. Hoboken, NJ, USA: Wiley, 2000, ch. 5, pp. 94–116.
- [2] A. E. Engin, K. Bharath, and M. Swaminathan, “Multilayered finitedifference method (MFDM) for modeling of package and printed circuit board planes,” *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 2, pp. 441–447, May 2007, doi: [10.1109/TEMC.2007.893331](https://doi.org/10.1109/TEMC.2007.893331).
- [3] K. Bharath, J. Y. Choi, and M. Swaminathan, “Use of the finite element method for the modeling of multi-layered power/ground planes with small features,” in *Proc. Electron. Compon. Technol. Conf.*, 2009, pp. 1630–1635.
- [4] C.-C. Huang, L. Tsang, and C. H. Chan, “Multiple scattering among vias in lossy planar waveguides using SMCG method,” *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 181–188, May 2002, doi: [10.1109/TADVP.2002.803262](https://doi.org/10.1109/TADVP.2002.803262).
- [5] L. Tsang and D. Miller, “Coupling of vias in electronic packaging and printed circuit board structures with finite ground plane,” *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 375–384, Nov. 2003, doi: [10.1109/TADVP.2003.821081](https://doi.org/10.1109/TADVP.2003.821081).
- [6] C.-J. Ong, D. Miller, L. Tsang, B. Wu, and C.-C. Huang, “Application of the Foldy–Lax multiple scattering method to the analysis of vias in ball grid arrays and interior layers of printed circuit boards,” *Microw. Opt. Technol. Lett.*, vol. 49, no. 1, pp. 225–231, Jan. 2007.
- [7] Y.-J. Zhang, A. R. Chada, and J. Fan, “An improved multiple scattering method for via structures with axially isotropic modes in an irregular plate pair,” *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 2, pp. 457–465, Apr. 2012, doi: [10.1109/TEMC.2011.2162524](https://doi.org/10.1109/TEMC.2011.2162524).
- [8] Y.-J. Zhang and J. Fan, “A generalized multiple scattering method for dense vias with axially anisotropic modes in an arbitrarily shaped plate pair,” *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 7, pp. 2035–2045, Jul. 2012, doi: [10.1109/MTT.2012.2195195](https://doi.org/10.1109/MTT.2012.2195195).

- [9] H. Chen, Q. Lin, L. Tsang, C.-C. Huang, and V. Jandhyala, "Analysis of a large number of vias and differential signaling in multilayered structures," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 818–829, Mar. 2003, doi: [10.1109/TMTT.2003.808616](#).
- [10] Z. Z. Oo et al., "A semi-analytical approach for system-level electrical modeling of electronic packages with large number of vias," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 267–274, May 2008, doi: [10.1109/TADVP.2008.923379](#).
- [11] Z. Z. Oo, E.-P. Li, X.-C. Wei, E.-X. Liu, Y.-J. Zhang, and L.-W. J. Li, "Hybridization of the scattering matrix method and modal decomposition for analysis of signal traces in a power distribution network," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 3, pp. 784–791, Aug. 2009, doi: [10.1109/TEMC.2009.2022543](#).
- [12] Z. Guo and G. Pan, "On simplified fast modal analysis for through silicon vias in layered media based upon full-wave solutions," *IEEE Trans. Adv. Packag.*, vol. 33, no. 2, pp. 517–523, May 2010, doi: [10.1109/TADVP.2009.2033034](#).
- [13] S. Wu and J. Fan, "Analytical prediction of crosstalk among vias in multilayer printed circuit boards," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 2, pp. 413–420, Apr. 2012, doi: [10.1109/TEMC.2011.2179658](#).
- [14] H. Wang and J. Fan, "Modeling local via structures using innovative PEEC formulation based on cavity green's functions with wave port excitation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1748–1757, May 2013, doi: [10.1109/TMTT.2013.2253791](#).
- [15] X. Sun, T. Huang, L. Ye, Y. Sun, S. Jin, and J. Fan, "Analyzing multiple vias in a parallel-plate pair based on a nonorthogonal PEEC method," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 5, pp. 1602–1611, Oct. 2019, doi: [10.1109/TEMC.2018.2870645](#).
- [16] R. Abhari, G. V. Eleftheriades, and E. van Deventer-Perkins, "Physics based CAD models for the analysis of vias in parallel-plate environments," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 10, pp. 1697–1707, Oct. 2001, doi: [10.1109/22.954773](#).
- [17] G. Selli, C. Schuster, and Y. Kwark, "Model-to-hardware correlation of physics based via models with the parallel plate impedance included," in *Proc. IEEE Symp. Electromagn. Compat.*, 2006, pp. 781–785, doi: [10.1109/ISEMC.2006.1706416](#).
- [18] C. Schuster, Y. H. Kwark, G. Selli, and P. Muthana, "Developing a 'physical' model for vias," Feb. 6–9, 2006.
- [19] G. Selli, C. Schuster, Y. H. Kwark, M. B. Ritter, and J. L. Drewniak, "Developing a 'physical' model for vias—Part II: Coupled and ground return vias," 2007.
- [20] R. Rimolo-Donadio et al., "Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009, doi: [10.1109/TMTT.2009.2025470](#).
- [21] X. Gu et al., "Validation and application of physics-based via models to dense via arrays," 2011.
- [22] S.-P. Gao, F. de Paulis, E.-X. Liu, and Y.-X. Guo, "Transmission line representation of the capacitive via-plate interaction toward a capacitor-free via model," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 11, pp. 2248–2256, Nov. 2019, doi: [10.1109/TCPMT.2019.2926792](#).
- [23] Y.-J. Zhang and J. Fan, "An intrinsic circuit model for multiple vias in an irregular plate pair through rigorous electromagnetic analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 8, pp. 2251–2265, Aug. 2010, doi: [10.1109/TMTT.2010.2052956](#).
- [24] A. G. Williamson, "Radial-line/coaxial-line junctions: Analysis and equivalent circuits," *Int. J. Electron.*, vol. 58, no. 1, pp. 91–104, 1985, doi: [10.1080/00207218508939005](#).
- [25] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*. Berlin, Germany: Springer, 1985, ch. 2, pp. 10–42.
- [26] G. T. Lei, R. W. Techtentin, P. R. Hayes, D. J. Schwab, and B. K. Gilbert, "Wave model solution to the ground/power plane noise problem," *IEEE Trans. Instrum. Meas.*, vol. 44, no. 2, pp. 300–303, Apr. 1995, doi: [10.1109/19.377836](#).
- [27] M. Xu and T. H. Hubing, "The development of a closed-form expression for the input impedance of power-return plane structures," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 3, pp. 478–485, Aug. 2003, doi: [10.1109/TEMC.2003.815531](#).
- [28] A. R. Chada, Y. Zhang, G. Feng, J. L. Drewniak, and J. Fan, "Impedance of an infinitely large parallel-plate pair and its applications in engineering modelling," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2009, pp. 78–82, doi: [10.1109/ISEMC.2009.5284626](#).
- [29] C. Wang et al., "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Trans. Adv. Packag.*, vol. 29, no. 2, pp. 320–334, May 2006, doi: [10.1109/TADVP.2006.871202](#).
- [30] J. Trinkle and A. Cantoni, "Impedance expressions for unloaded and loaded power ground planes," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 2, pp. 390–398, May 2008, doi: [10.1109/TEMC.2008.919036](#).
- [31] R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Hybrid approach for efficient calculation of the parallel-plate impedance of lossy power/ground planes," *Microw. Opt. Technol. Lett.*, vol. 51, no. 9, pp. 2051–2056, Sep. 2009.
- [32] X. Duan, R. Rimolo-Donadio, H. Bruns, B. Archambeault, and C. Schuster, "Special session on power integrity techniques: Contour integral method for rapid computation of power/ground plane impedance," Feb. 2010.
- [33] Y.-J. Zhang, G. Feng, and J. Fan, "A novel impedance definition of a parallel plate pair for an intrinsic via circuit model," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3780–3789, Dec. 2010, doi: [10.1109/TMTT.2010.2083870](#).
- [34] X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Circular ports in parallel-plate waveguide analysis with isotropic excitations," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 3, pp. 603–612, Jun. 2012, doi: [10.1109/TEMC.2011.2170998](#).
- [35] R. Rimolo-Donadio, S. Müller, X. Duan, M. Kotzev, H.-D. Bruns, and C. Schuster, "Signal integrity: Efficient, physics-based via modeling: Principles and methods," *IEEE Electromagn. Compat. Mag.*, vol. 1, no. 1, pp. 55–61, Jan.–Mar. 2012, doi: [10.1109/MEMC.2012.6244946](#).
- [36] S. Müller et al., "Accuracy of physics-based via models for simulation of dense via arrays," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 5, pp. 1125–1136, Oct. 2012, doi: [10.1109/TEMC.2012.2192123](#).
- [37] J. Fan, A. Hardock, R. Rimolo-Donadio, S. Müller, Y. H. Kwark, and C. Schuster, "Signal integrity: Efficient, physics-based via modeling: Return path, impedance, and stub effect control," *IEEE Electromagn. Compat. Mag.*, vol. 3, no. 1, pp. 76–84, Jan.–Mar. 2014, doi: [10.1109/MEMC.2014.6798802](#).
- [38] Y. J. Zhang et al., "An efficient hybrid finite-element analysis of multiple vias sharing the same anti-pad in an arbitrarily shaped parallel-plate pair," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 883–890, Mar. 2015, doi: [10.1109/TMTT.2015.2389257](#).
- [39] P. Li, L. J. Jiang, Y. J. Zhang, S. Xu, and H. Bagci, "An efficient mode based domain decomposition hybrid 2D/Q-2D finite-element time-domain method for power/ground plate-pair analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4357–4366, Oct. 2018, doi: [10.1109/TMTT.2018.2851216](#).
- [40] P. Li, L. J. Jiang, M. Tang, Y. J. Zhang, S. Xu, and H. Bagci, "A novel sub-domain 2D/Q-2D finite element method for power/ground plate-pair analysis," *IEEE Trans. Electromagn. Compat.*, vol. 62, no. 5, pp. 2217–2226, Oct. 2020, doi: [10.1109/TEMC.2019.2942328](#).
- [41] Y. Zhang, J. Fan, G. Selli, M. Cocchini, and F. Paulis, "Analytical evaluation of via-plate capacitance for multilayer printed circuit boards and packages," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 9, pp. 2118–2128, Sep. 2008, doi: [10.1109/TMTT.2008.2002237](#).
- [42] M. Friedrich, M. Leone, and C. Bednarz, "Exact analytical solution for the via-plate capacitance in multi-layer structures," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 5, pp. 1097–1104, Oct. 2012, doi: [10.1109/TEMC.2012.2189573](#).
- [43] M. Friedrich, C. Bednarz, and M. Leone, "Improved expression for the via-plate capacitance based on the magnetic-frill model," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 6, pp. 1362–1364, Dec. 2013, doi: [10.1109/TEMC.2013.2265041](#).
- [44] H. H. Park, C. Hwang, K.-Y. Jung, and Y. B. Park, "Mode matching analysis of via-plate capacitance in multilayer structures with finite plate thickness," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 5, pp. 1188–1196, Oct. 2015, doi: [10.1109/TEMC.2015.2440299](#).
- [45] S.-P. Gao, F. de Paulis, E.-X. Liu, A. Orlandi, and H. M. Lee, "Fast-convergent expression for the barrel-plate capacitance in the physics-based via circuit model," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 368–370, May 2018, doi: [10.1109/LMWC.2018.2812639](#).
- [46] P. Russer, "Transmission-lines and waveguides," in *Electromagnetics, Microwave Circuit and Antenna Design for Communications Engineering*, 2th ed. Norwood, MA, USA: Artech House, 2006, ch. 7, pp. 300–307.