Analytical Evaluation of Via-Plate Capacitance for Multilayer Printed Circuit Boards and Packages

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***Abstract*—The via-plate capacitance for a via transition to a multilayer printed circuit board is evaluated analytically in terms of higher order parallel-plate modes. The Green's function in a bounded coaxial cavity for a concentric magnetic ring current is first derived by introducing reflection coefficients for cylindrical waves at the inner and outer cavity walls. These walls can be perfect electric conductor (PEC)/perfect magnetic conductor (PMC) or a nonreflective perfectly matched layer. By further assuming a magnetic frill current on the via-hole in the metal plate, an analytical formula is derived for the via barrel-plate capacitance by summing the higher order modes in the bounded coaxial cavity. The convergence of the formula with the number of modes, as well as with the radius of the outer PEC/PMC wall is discussed. The analytical formula is validated by both quasi-static numerical methods and measurements. Furthermore, the formula allows the investigation of the frequency dependence of the via-plate capacitance, which is not possible with quasi-static methods.**

***Index Terms*—Analytical formula, Green's function in a coaxial cavity, multilayer package/printed circuit board (PCB), signal integrity, via-holes, via-plate capacitance.**

I. Introduction

VIAS ARE one of the common structures used in multilayer packages or printed circuit boards (PCBs) to connect signal traces residing on different layers [1]–[4]. High-speed currents along vertical vias can excite parallel-plate waveguide modes between power/ground plates of a power distribution network. This may cause serious power integrity concerns and significant coupling to adjacent vias. Therefore, a simple, yet accurate model for via-plane interactions is highly desirable for analysis and design of high-speed and high-density multilayer interconnects.

The propagation characteristics of a via-hole have been investigated using full wave methods such as the finite difference time domain (FDTD) [5] and method of moments (MoM) [6]. On the other hand, a π-type lumped-circuit model, consisting of two excess capacitances and one excess inductance, is usually employed for a via-hole in a plane [7]. The quasi-static integral-equation method is widely used to extract the excess capacitances [7]–[11]. Analytical solutions are also proposed to calculate the excess capacitance for a via in a multilayered media [12]. In addition, microwave network theory is developed in [13] to construct a single via model in plate pair structures and then extended to coupling analysis between two vias [14].

Recently, a novel full-wave method based on the Foldy–Lax multiple scattering method has been proposed to obtain an admittance matrix for many vias in parallel-plate structures [4], [15]–[17]. In the Foldy–Lax method, the boundary conditions on vias are rigorously satisfied, but those counterparts along the plate pair edges are difficult to be enforced. While the perfect electric conductor (PEC) boundary can be modeled by densely distributed stitching vias, the Foldy–Lax method is hard to handle the perfect magnetic conductor (PMC) boundary, a popular approximation adopted for sidewalls of power/ground planes [18]–[22]. This makes the method be restricted to either infinite or finite circular plate pair structures [15].

Different from the full-wave Foldy–Lax method, a physics-based model is proposed to combine the lumped circuit of vias with the impedance of the plate pair [23]–[26]. Due to the separation of vias and the plate pair, this model can treat an arbitrary shaped plate pair. Based on physical intuition, a simple (perhaps too simple) via lumped circuit is used, which contains a shorting circuit for the via barrel and two via-plate capacitances to take into account the displacement currents between the via and two plates. Simulation and measurements in [23]–[25] have demonstrated the feasibility of the physics-based via-plane model, although the boundary condition on vias has not been rigorously addressed. The purpose of this paper is to derive an analytical formula using electromagnetic (EM) analysis for the evaluation of the via-plate capacitances, which have been calculated by numerical methods in previous publications [23]–[25]. It should be pointed out that the via-plate capacitance studied herein is different from the above-mentioned excess capacitances of via-holes in [7]–[11]. They correspond to different via transition structures. The via-plate capacitances are for vias crossing at least one plate pair, while the excess capacitances are parasitics for vias crossing a single plate from one side to the other. The field distributions in the two structures are quite different. For vias crossing only a single plane, there is no reference plane change for traces.

The top part of Fig. 1(a) shows a schematic of a via in a multilayer plane structure. The entire structure can be viewed as a special coaxial line that the inner conductor is the via itself and the multilayer parallel plates construct the deformed outer conductor. While the signal current flows through the via, the multilayer parallel plates provide its return path. The bottom part of Fig. 1(a) shows the geometry of one of the parallel-plate pair

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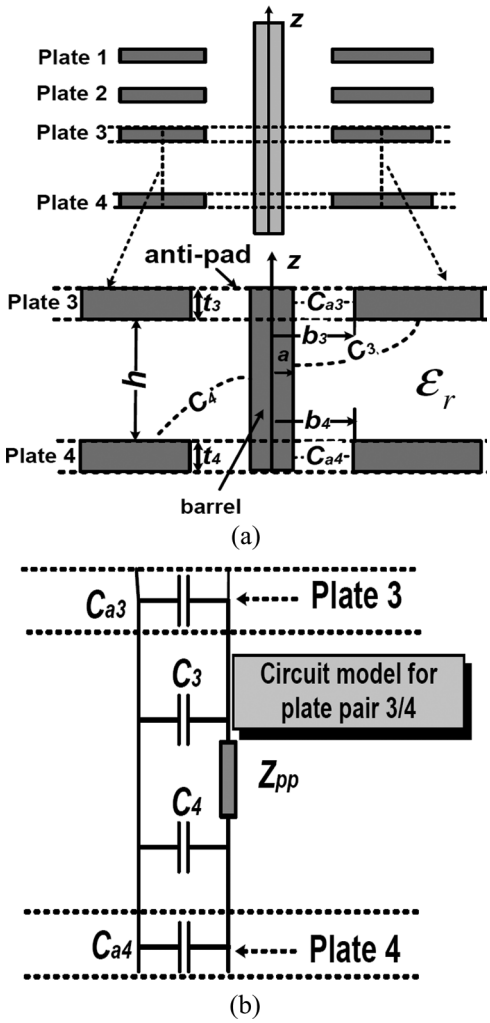

Fig. 1. (a) Via in a multilayer parallel-plate structure, and the geometry of the via and Plate-pair 3/4. (b) Equivalent circuit model for Plate-pair 3/4 as an example in a cascaded π-circuit model for a via in a multilayer parallel-plate structure.

comprised of Plate 3 and Plate 4. The radii of the antipad (the hole in metal plate), and the plate thickness of Plate 3 and Plate 4 are denoted as b_3, t_3 and b_4, t_4, respectively. The separation of the plate pair or the height of the via portion between the plates is h. The via barrel is embedded in the dielectrics with a relative permittivity of ε_r and the via radius is denoted as a.

In the via/plate-pair structure shown in Fig. 1(a), a field of the TEM coaxial mode in the antipad of Plate 3 is converted to the parallel-plate TM_z modes in the plate pair, and then converted back into the coaxial mode in the antipad of Plate 4. According to the physical model proposed in [23] and [24], a corresponding equivalent circuit model for Plate-pair 3/4 is given in Fig. 1(b). To facilitate the following description, the via-plate capacitance in [23] and [24] is divided into two parts: the coaxial and the barrel-plate capacitances. The coaxial capacitances due to the finite plate thickness are denoted as C_{a3} and C_{a4}. In addition, C_3 and C_4 are used to represent the capacitances between the via barrel to Plates 3 and 4, respectively. The following sections will show that these via barrel-plate capacitances are due to the higher order parallel-plate TM_z modes. On the other hand, the impedance of the plate pair Z_{pp} characterizes the return path impedance of the plate pair for the dominant or propagating parallel-plate TM_{z0} mode.

The impedance of a plate pair, Z_{pp}, has been extensively studied by various methods. The cavity model with a segmentation method is the most popular approach adopted thus far [18]–[22]. However, very little research has been devoted to the evaluation of the via-plate capacitances, which includes both the coaxial (e.g., C_{a3} and C_{a4}) and the barrel-plate capacitances (e.g., C_3 and C_4).

This paper presents an analytical expression for the via barrel-plate capacitances (an analytical expression for the coaxial capacitances is already known and will be introduced in Section II). The Green's function is first derived for a concentric magnetic ring current in a general bounded coaxial cavity with various inner or outer boundaries such as the PEC, PMC, and nonreflective surface or perfectly matched layer (PML). The Green's function is expressed as a summation of all the TM_z modes of the parallel-plate waveguide in which multiple scattering of cylindrical waves between inner and outer walls have been taken into account. The presence of the outer boundary in a via model makes this paper different from the previous analytical efforts given in [13]. The outer boundary helps separate the via model itself from the impedance of the plate pair while [13] does not differentiate the models of the vias and plate pair.

The general bounded coaxial cavity is excited with the magnetic frill currents that are obtained from the coaxial TEM mode in the antipad apertures. This TEM mode assumption is commonly adopted [27], [28]. The magnetic field in the general bounded coaxial cavity can be obtained by the convolution of the magnetic frill currents with the derived Green's function. This enables the calculations of the vertical currents along the via. As shown later, the vertical currents on the top and bottom plates of each via portion are different. According to the current continuity principle, the displacement currents between the via barrel and the plates contribute to the difference of these two currents. Based on this observation, the barrel-plate capacitances are derived analytically in terms of the higher order TM_z modes. As the separation of the parallel plates is normally electrically small, these higher order modes decay rapidly in the radial direction from the via. Further investigation proves that the analytical formula converges quickly with very few summation terms of the higher order modes. Thus, this approach is more efficient than any numerical method and can be easily integrated in a circuit simulator. Furthermore, the analytical formula can provide the frequency-dependent properties of the via barrel-plate capacitance, which is beyond the capability of any quasi-static method.

II. General Bounded Coaxial Cavity and the Magnetic Frill Current

To derive the analytical formula for the barrel-plate capacitance of a via, a plate pair is considered here as shown in Fig. 2. The radii of the via and antipad are denoted as a and b, respectively. The separation of the plate pair is represented as h. An outer circular wall $\rho = R$ is introduced to help the investigation of the attenuation of the higher order parallel-plate modes. The boundary condition on this outer wall can be PEC, PMC,

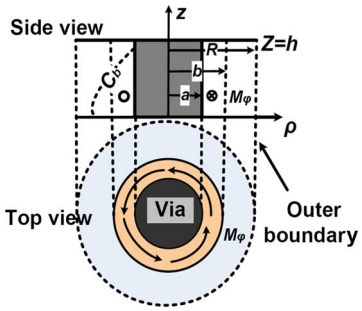

Fig. 2. Excitation of magnetic frill current in a bounded coaxial cavity.

or nonreflective PML. Therefore, the structure under investigation ($a \le \rho \le R$ and $0 \le z \le h$) becomes a general bounded coaxial cavity.

The magnetic frill current M_ϕ in the antipad aperture in the $z = z'$ plate is considered first. Here, an assumption is adopted that only the dominant coaxial TEM mode is considered in the antipad aperture. This is justified by the fact that the cutoff wavelength of the higher order E-modes of a coaxial waveguide can be approximated as [29]

$$\lambda_c \simeq \frac{2(b-a)}{n} \tag{1}$$

where integer $n = 1, 2, \ldots$, is the higher coaxial mode index. Normally $b-a$ is less than 20 mil in practical designs. Thus, for the first higher mode $(n = 1)$, the cutoff wavelength is about 40 mil, i.e., the cutoff frequency is about 300 GHz, well beyond 40 GHz, the maximum frequency of interest in this paper. Therefore, all the higher order coaxial modes are neglected herein. In addition, [27] and [28] have also indicated that the TEM approximation for a coaxial probe provides accurate results over a wide range of parameters, presenting additional justification of the assumption.

The TEM coaxial mode assumption in the antipad aperture results in the expression of the magnetic frill current M_ϕ as

$$M_\phi = -\frac{V_0}{\rho' \ln(b/a)} \delta(z - z') \tag{2}$$

where V_0 is the voltage between the via and antipad, and $\delta(z - z')$ is a Dirac's delta function.

With the TEM assumption, the calculation of the coaxial capacitance C_a between the via and plate, due to the finite thickness of the plate, is

$$C_a = \frac{2\pi\varepsilon_r\varepsilon_0 t}{\ln\dfrac{b}{a}} \tag{3}$$

where t is the plate thickness and ε_r is the relative permittivity of the dielectrics in which the via is embedded.

III. Green's Function in a Bounded Coaxial Cavity for a Concentric Magnetic Ring Current

To obtain the fields excited by the magnetic frill current M_ϕ, the Green's function for a concentric magnetic ring current needs to be derived first for the general bounded coaxial cavity, as shown in Fig. 2. The Green's function of a magnetic ring current in an unbounded parallel-plate waveguide is given as [30]

$$G_\phi^{(m)}(\rho, z; \rho', z') = -\frac{j\pi\rho'}{h} \sum_{n=0}^{\infty} \frac{1}{1+\delta_{n0}} g_n(\rho_<, \rho_>) \cdot \cos\left(\frac{n\pi}{h} z\right) \cos\left(\frac{n\pi}{h} z'\right) \tag{4}$$

where δ_{n0} is the Kronecker delta and the radial function $g_n(\cdot)$ is given as

$$g_n(\rho_<, \rho_>) = J_1(k_n\rho_<) H_1^{(2)}(k_n\rho_>) \tag{5}$$

$$\rho_< = \min\{\rho, \rho'\}$$

$$\rho_> = \max\{\rho, \rho'\} \tag{6}$$

and $J_1(\cdot)$, $H_1^{(2)}(\cdot)$ denote the first-order Bessel function of the first kind and the first-order Hankel function of the second kind, respectively, ρ and ρ' are the observation and source points, and

$$k_n = \sqrt{k_0^2\varepsilon_r - \left(\frac{n\pi}{h}\right)^2} \tag{7}$$

is the radial wavenumber of the TM_{zn} mode in a parallel-plate waveguide.

To extend (4) to a general coaxial cavity bounded by the inner and outer boundaries at $\rho = a$ and $\rho = R$ in a parallel-plate waveguide, as shown in Fig. 2, reflection coefficients for any TM_{zn} mode are introduced with different boundary conditions at the boundaries of $\rho = a$ and $\rho = R$ as

$$\Gamma_R^{(n)} = \begin{cases} -\dfrac{H_0^{(2)}(k_nR)}{J_0(k_nR)}, & \rho = R \quad \text{PEC} \\ -\dfrac{H_1^{(2)}(k_nR)}{J_1(k_nR)}, & \rho = R \quad \text{PMC} \\ 0, & \rho = R \quad \text{PML} \end{cases} \tag{8}$$

$$\Gamma_a^{(n)} = \begin{cases} -\dfrac{J_0(k_na)}{H_0^{(2)}(k_na)}, & \rho = a \quad \text{PEC} \\ -\dfrac{J_1(k_na)}{H_1^{(2)}}(k_na), & \rho = a \quad \text{PMC} \\ 0, & \rho = a \quad \text{PML}. \end{cases} \tag{9}$$

For a metal via, note that only PEC boundary should be used for the $\rho = a$ boundary. By considering multiple scattering of all the TM_{zn} modes $(n = 0, 1, 2, \ldots)$ between the two boundaries at $\rho = a$ and $\rho = R$, the Green's function for a magnetic ring current in a bounded coaxial cavity can be derived as

$$\tilde{G}_\phi^{(m)}(\rho, z; \rho', z') = -\frac{j\pi\rho'}{h} \sum_{n=0}^{\infty} \frac{1}{1+\delta_{n0}} \tilde{g}_n(r, R; \rho_<, \rho_>) \cdot \cos\left(\frac{n\pi}{h} z\right) \cos\left(\frac{n\pi}{h} z'\right) \tag{10}$$

where the radial function is changed into

$$\tilde{g}_n(a, R; \rho_<, \rho_>) = \left(1 - \Gamma_R^{(n)}\Gamma_a^{(n)}\right)^{-1} \times \left[J_1(k_n\rho_<) + \Gamma_a^{(n)} H_1^{(2)}(k_n\rho_<)\right] \cdot \left[H_1^{(2)}(k_n\rho_>) + \Gamma_R^{(n)} J_1(k_n\rho_>)\right]. \tag{11}$$

Note that (10) can be simplified to (4) if both the inner and outer boundaries do not exist, i.e., they are nonreflective PML boundaries ($\Gamma_R^{(n)} = 0$ and $\Gamma_a^{(n)} = 0$).

IV. Via Barrel-Plate Capacitance Formulation

The magnetic field in the bounded coaxial cavity due to the magnetic frill current M_ϕ can be obtained by the following convolution [30]:

$$H_\phi(\rho,z) = -j\omega\varepsilon \int_a^b M_\phi(\rho',z')\tilde{G}_\phi^{(m)}(\rho,z;\rho',z')d\rho'. \quad (12)$$

Substituting (2) into (12), we have for $\rho \geq b$,

$$\begin{aligned} H_\phi(\rho,z) = &-\frac{\omega\varepsilon\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n(1+\delta_{n0})} \\ &\cdot\Big\{[J_0(k_nb)-J_0(k_na)] \\ &\quad +\Gamma_a^{(n)}\left[H_0^{(2)}(k_nb)-H_0^{(2)}(k_na)\right]\Big\} \\ &\cdot\left[H_1^{(2)}(k_n\rho)+\Gamma_R^{(n)}J_1(k_n\rho)\right] \\ &\cdot\cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \end{aligned} \quad (13)$$

and for $\rho \leq a$,

$$\begin{aligned} H_\phi(\rho,z) = &-\frac{\omega\varepsilon\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n(1+\delta_{n0})} \\ &\cdot\Big\{\left[H_0^{(2)}(k_nb)-H_0^{(2)}(k_na)\right] \\ &\quad +\Gamma_R^{(n)}\left[J_0(k_nb)-J_0(k_na)\right]\Big\} \\ &\cdot\left[J_1(k_n\rho)+\Gamma_a^{(n)}H_1^{(2)}(k_n\rho)\right] \\ &\cdot\cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right). \end{aligned} \quad (14)$$

The magnetic field expressions derived above are reduced to [30, eq. (25)] for the unbounded parallel-plate pair when $\Gamma_a^{(n)} = 0$ and $\Gamma_R^{(n)} = 0$ are used.

The electric current flowing on the via surface can be expressed as

$$I_z(z)|_{z'} = 2\pi a H_\phi(a,z). \quad (15)$$

Substituting (14) into (15) and using $\rho = a$, $\Gamma_a^{(n)} = -J_0(k_na)/H_0^{(2)}(k_na)$ yields

$$\begin{aligned} I_z(z)|_{z'} = &\, j\omega\frac{4\pi\varepsilon V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2(1+\delta_{n0})H_0^{(2)}(k_na)} \\ &\cdot\Big\{\left[H_0^{(2)}(k_nb)-H_0^{(2)}(k_na)\right] \\ &\quad +\Gamma_R^{(n)}\left[J_0(k_nb)-J_0(k_na)\right]\Big\} \\ &\cdot\cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \end{aligned} \quad (16)$$

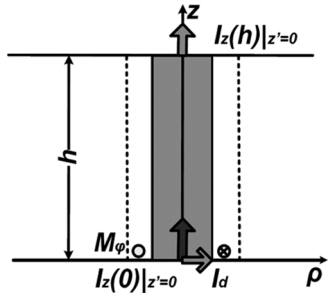

Fig. 3. Displacement current I_d and the vertical current I_z generated by the magnetic frill current M_b ($z' = 0$) at the bottom ($z = 0$) and top ($z = h$) end of the via in a plate pair.

in which the Wronskian identity $J_1(z)H_0^{(2)}(z) - J_0(z)H_1^{(2)}(z) = -2j/(\pi z)$ is employed. Thus the vertical current (16) includes the currents of all the TM_{zn} modes. It is worth noting that (16) is consistent with [4, eqs. (6) and (7)] in the case of $\Gamma_R^{(n)} = 0$. This further validates the Green's function derived in (10).

Suppose the magnetic frill current M_ϕ is located on the bottom plate of the $z' = 0$ plane, as shown in Fig. 3. The vertical currents along the via caused by M_ϕ can then be obtained from (16) as

$$\begin{aligned} I_z(z)|_{z'=0} = &\, j\omega\frac{4\pi\varepsilon V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2(1+\delta_{n0})H_0^{(2)}(k_na)} \\ &\cdot\Big\{\left[H_0^{(2)}(k_nb)-H_0^{(2)}(k_na)\right] \\ &\quad +\Gamma_R^{(n)}\left[J_0(k_nb)-J_0(k_na)\right]\Big\}\cos\left(\frac{n\pi}{h}z\right). \end{aligned} \quad (17)$$

A careful observation from (17) found that the vertical current at the bottom end of the via, $I_z(0)|_{z'=0}$, and the vertical current at the top end of the via, $I_z(h)|_{z'=0}$, are different. The difference can be accounted for by the displacement current I_d from the via barrel to the metal plate at $z = 0$, as illustrated in Fig. 3. Thus, we have

$$I_d = I_z(0)|_{z'=0} - I_z(h)|_{z'=0}. \quad (18)$$

Substituting (17) into (18) yields

$$\begin{aligned} I_d = &\, j\omega V_0\frac{8\pi\varepsilon}{h\ln(b/a)}\sum_{n=1,3,5\ldots}^{\infty}\frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2H_0^{(2)}(k_na)} \\ &\cdot\Big\{\left[H_0^{(2)}(k_nb)-H_0^{(2)}(k_na)\right] \\ &\quad +\Gamma_R^{(n)}\left[J_0(k_nb)-J_0(k_na)\right]\Big\}. \end{aligned} \quad (19)$$

The via barrel-plate capacitance can be defined as

$$C_b = \frac{I_d}{j\omega V_0}. \quad (20)$$

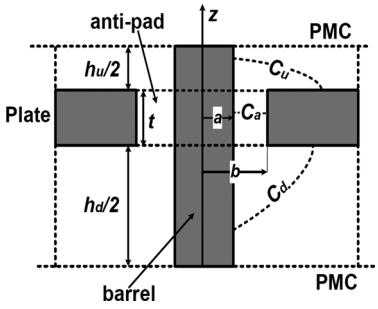

Fig. 4. Computational domain for the via-plate capacitance using electrostatic numerical methods.

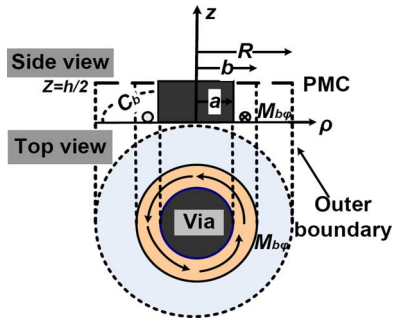

Fig. 5. Via barrel-plate capacitance with half via height and the PMC boundary.

Therefore, from (19), the analytical expression for the via barrel-plate capacitance is derived as

$$C_b = \frac{8\pi\varepsilon}{h\ln(b/a)} \sum_{n=1,3,5\ldots}^{2N-1} \frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2 H_0^{(2)}(k_n a)} \cdot \left\{ \left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a) \right] + \Gamma_R^{(n)} \left[J_0(k_n b) - J_0(k_n a) \right] \right\} \tag{21}$$

where N denotes the number of modes used in the actual calculations. The convergence of (21) with N, as well as other properties of the expression will be discussed later.

It should be noted that the via barrel-plate capacitance between the via and top plate can be similarly derived using a magnetic frill current in the $z' = h$ plate. It can be shown that the via barrel-plate capacitance has the same analytical expression as (21).

V. Via-Plate Capacitance Calculation

Although the via barrel-plate capacitance, combined with the coaxial capacitance, is enough to build the circuit model of a via in a parallel-plate pair, as shown in Fig. 1(b), a via-plate capacitance concept is further used to validate the barrel-plate capacitance formula (21). In [24] and [25], the via-plate capacitance associated with a specific plate is defined in the region bounded by two PMC boundaries placed in the middle of the two adjacent plates. As an example, Fig. 4 gives the via-plate capacitance domain associated with a plate. The dashed boundaries are specified as PMC, which are required by numerical methods to calculate the via-plate capacitance. This section discusses the relationship of the via-plate capacitance and the via barrel-plate and the coaxial capacitances so that analytical formula (21) can be validated.

According to the assumption of the TEM mode in the antipad aperture, the via-plate capacitance in the capacitance domain shown in Fig. 4 contains three parts, i.e.: 1) the coaxial capacitance C_a and two barrel-plate capacitances C_u and C_d.

Without losing generality, the structure shown in Fig. 5 is studied. The following discussion will demonstrate that the barrel-plate capacitance, denoted as C_b in this structure, is exactly the same as the barrel-plate capacitance C_b, shown in Fig. 2, which can be evaluated using (21).

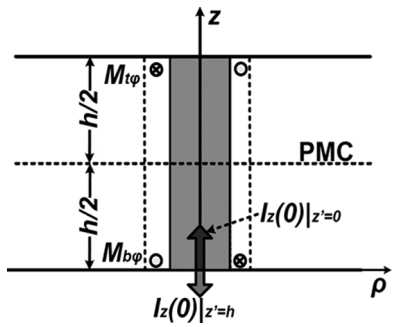

Fig. 6. Vertical currents excited by frill magnetic currents M_b and M_t located at the bottom and the top of a via.

Fig. 6 shows the bottom magnetic frill current $M_{b\phi}$ and its image counterpart $M_{t\phi}$ at $z = h$. This satisfies the PMC boundary condition at the $z = h/2$ plane. According to (2), the image frill magnetic current $M_{t\phi}$ can be expressed as

$$M_{t\phi} = -\frac{-V_0}{\rho'\ln(b/a)}\delta(z-h). \tag{22}$$

Replacing V_0 in (16) with $-V_0$ and $z' = h$, the vertical current generating by the magnetic frill current $M_{t\phi}$ is

$$I_z(z)|_{z'=h} = j\omega\frac{4\pi\varepsilon(-V_0)}{h\ln(b/a)} \sum_{n=0}^{\infty} \frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2(1+\delta_{n0})H_0^{(2)}(k_n a)} \cdot \left\{ \left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a) \right] + \Gamma_R^{(n)} \left[J_0(k_n b) - J_0(k_n a) \right] \right\} \cdot \cos\left(\frac{n\pi}{h}z\right)(-1)^n. \tag{23}$$

Therefore, the vertical current at the bottom end of the via excited by both $M_{b\phi}$ and $M_{t\phi}$ can be obtained by adding (17) and (23) together and setting $z = 0$

$$\begin{aligned} I_z(0) &= I_z(0)|_{z'=0} + I_z(0)|_{z'=h} \\ &= j\omega V_0 \frac{8\pi\varepsilon}{h\ln(b/a)} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2 H_0^{(2)}(k_n a)} \\ &\quad \cdot \left\{ \left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a) \right] + \Gamma_R^{(n)} \left[J_0(k_n b) - J_0(k_n a) \right] \right\}. \end{aligned} \tag{24}$$

The total vertical current at the bottom end of the via $I_z(0)$ is not zero. As shown in Fig. 6, $I_z(0)$ must be accounted for by the displacement current from the barrel to the plate in order to satisfy the current continuity condition. Note that this displacement current is exactly the same as the displacement current given in (19). This proves that the barrel-plate capacitance C_b, as shown in Fig. 5, is the same as the barrel-capacitance C_b derived in the previous section. The analytical expression of the barrel-plate capacitance (21) can then be used to evaluate the via-plate capacitance defined in Fig. 4 as

$$C_{via} = C_u + C_d + C_a \tag{25}$$

where C_a is the coaxial capacitance due to the finite thickness of the metal plate using (3); C_u and C_d are upper and bottom barrel-plate capacitances, which can be evaluated analytically using (21) as

$$C_{u(d)} = \frac{8\pi\varepsilon}{h_{u(d)}\ln(b/a)} \sum_{n=1,3,5\ldots}^{2N-1} \frac{\left(1-\Gamma_a^{(n)}\Gamma_R^{(n)}\right)^{-1}}{k_n^2 H_0^{(2)}(k_n a)} \cdot \left\{ \left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a)\right] + \Gamma_R^{(n)}\left[J_0(k_n b) - J_0(k_n a)\right] \right\} \tag{26}$$

and

$$k_n = \sqrt{k_0^2\varepsilon_r - \left(\frac{n\pi}{h_{u(d)}}\right)^2}. \tag{27}$$

Note that the full height h_u or h_d is used in (26), although the half heights h_u and h_d are depicted in Fig. 4 for the computational domains of barrel-plate capacitances using numerical methods.

VI. Validation and Numerical Results

The analytical formula (25) of the via-plate capacitance, evaluated by both (3) and (21), is first validated with electrostatic numerical methods. Table I presents the comparisons of the via-plate capacitances obtained by the Q3D Extractor (Ansoft Corporation, Pittsburgh, PA) in [23], the CST EM Studio Electro-Static solver, and those by (25) using $N = 31$ in (21). The differences between the analytic formula and those electrostatic solvers are only a few femtofarads. The computational time using CST EM Studio and the analytical formula are also listed in Table I (on a PC with a genuine Intel 3391-MHz CPU and 2-GB memory). As expected, the analytical formula takes a fraction of second (using MATLAB code) to evaluate the via-plate capacitance, while the numerical solver costs several hundred seconds.

The analytical formula of the via-plate capacitance is also validated with measurements. Fig. 7(a) and (b) shows the top and side views of a test board geometry. It contains eight power/ground square plates with a side length of 9.144 mm (360 mil). Stitch vias along the boundaries of these plates construct seven cascaded cavities with PEC sidewalls. A via is located at $(3.937, 3.937)$ mm of the board from the lower left corner to connect the two striplines in the top and bottom plate pair. The separations of the different plate pair are $h_1 = 0.3048$ mm and $h_2 = 0.2032$ mm, as shown in Fig. 7(b). All dielectric layers have a dielectric constant of 3.5 and a loss tangent of 0.02. There are three different via-plate capacitances as $C_1 = 30.5$ fF, $C_2 = 52$ fF, and $C_3 = 61$ fF obtained by the analytical formula (25). Fig. 7(b) also shows the cascaded equivalent circuits based on the physical via-plate model [23], [24]. Note that each stripline is modeled by two microstrip lines, as proposed in [24]. The circuit model is analyzed using the Advanced Design System (ADS), a circuit simulator from Agilent Technologies, Palo Alto, CA.

The S-parameters of the test case were measured using Agilent Technologies' vector network analyzer (VNA) E8364A

TABLE I
COMPARISON OF THE VIA-PLATE CAPACITANCE VALUE CALCULATED BY ELECTROSTATIC SOLVERS Q3D [23], CST EM STUDIO, AND THE ANALYTICAL FORMULA (25) ($h_u = h_d = 0.2286$ mm (9 mil), $t = 0.0254$ mm (1 mil), $\varepsilon_r = 3.84$

case	radii (mm)		C_{via} (fF) (Elapsed time:seconds)		
	a	b	Q3D [23]	CST EM Studio	(25)
1	0.1016	0.3556	41	40.7 (303)	42.6 (0.15)
2	0.1016	0.4318	37	36.2 (301)	37.2 (0.15)
3	0.1016	0.5080	33	32.8 (308)	33.4 (0.15)
4	0.1524	0.3556	56	58.2 (380)	61.7 (0.15)
5	0.1524	0.4318	50	48.9 (365)	51.2 (0.15)
6	0.1524	0.5080	44	43.2 (308)	44.6 (0.15)
7	0.2032	0.3556	83	84.7 (431)	89.6 (0.15)
8	0.2032	0.4318	66	66.1 (425)	69.9 (0.15)
9	0.2032	0.5080	56	55.7 (365)	58.4 (0.15)

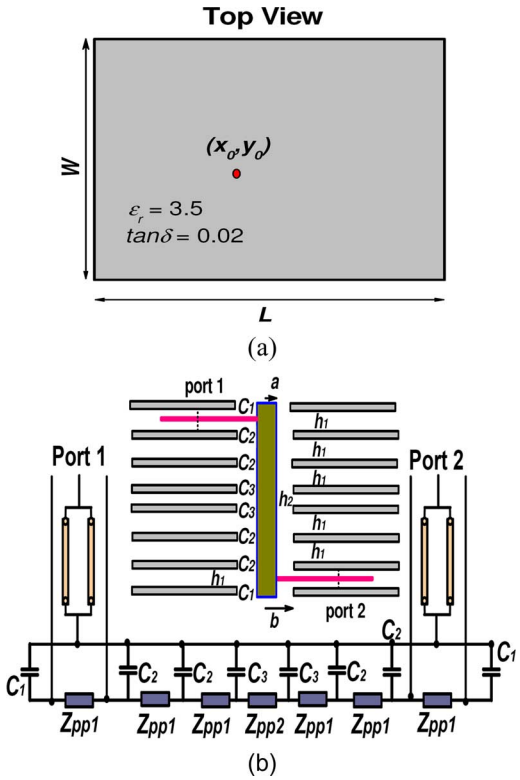

Fig. 7. Test geometry with a via of $a = 0.1270$ mm (5 mil), $b = 0.3810$ mm (15 mil) in a stack up with $h_1 = 0.3048$ (12 mil), $h_2 = 0.2032$ mm (8 mil), $L = W = 9.144$ mm (360 mil), and $x_0 = y_0 = 3.937$ mm (155 mil). (a) Top view. (b) Side view of the stack up and its equivalent-circuit model for simulation.

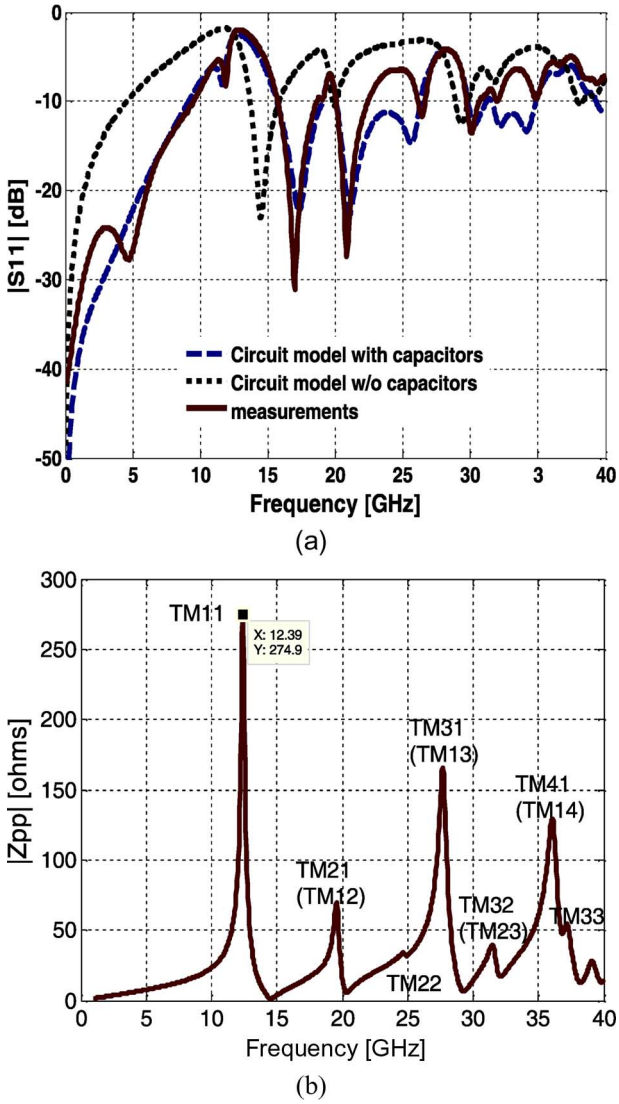

Fig. 8. (a) Comparison of return loss with or without including via-plate capacitances with the measurement results. (b) Impedance of one of the plate pair of stack-up structure (height: 0.3048 mm).

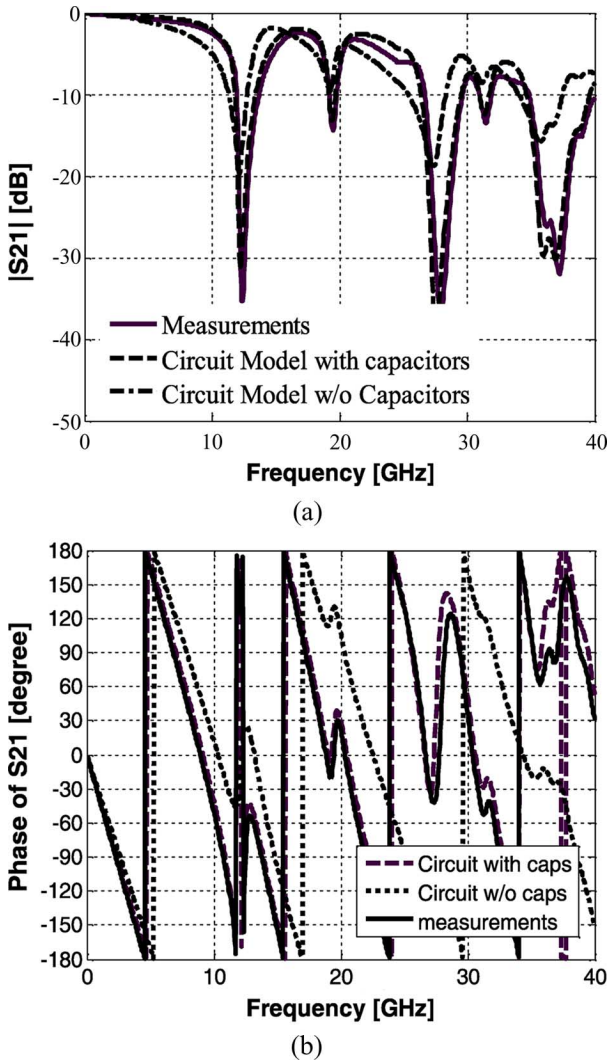

Fig. 9. Comparison of the simulations of transmission coefficient with/without the via-plate capacitances with the measurements. (a) Amplitude of S_{21}. (b) Phase of S_{21}.

with a frequency band from 45 MHz to 50 GHz. The microwave probes used were made by GGB Industries Inc., Naples, FL, model 40A G–S and S–G with a 225-μm pitch. The short-open-load-thru (SOLT) calibration was conducted using a CS-14 calibration substrate, also made by GGB Industries Inc.

Fig. 8(a) shows the impact of the via-plate capacitances on return loss and the comparison of the simulation and measurement results. Obvious difference can be observed if the via-plate capacitances are not considered in the circuit model. After the via-plate capacitances are added, a good agreement is found between the measurement and simulation. The discrepancies at the frequencies higher than 20 GHz are possibly due to the signal launch that has not completely accounted for in the measurement and the trace-to-via discontinuities that are not included in the modeling. Fig. 8(b) provides the impedance profile of one of the plate pair (Z_{pp1}) using [24, eq. (1)]. It can be seen that the peaks of Z_{pp} are correlated to the peaks of the return loss.

Fig. 9(a) and (b) presents the comparison of the simulation and measurement results of the amplitude and phase of the transmission coefficient S_{21} between the two ports at the ends of stripline traces. Again, it can be clearly seen that the simulation result without including the effect of the via-plate capacitances, shown as the dotted line, significantly deviates from the measurement, especially at high frequencies. On the other hand, the circuit model with the via-plate capacitances, shown as the dashed line, agrees very well with the measurement for both the amplitude (no more than a couple of decibels difference when the frequency is up to 20 GHz) and phase (no obvious difference up to 27 GHz) of the transmission coefficient. This further demonstrates that the via-plate capacitances cannot be neglected in the analysis of a multilayer structure.

The results given in Table I, as well as Figs. 8 and 9, validate the accuracy of the analytical expression of the via-plate capacitance. Fig. 10 shows the rapid convergence of the barrel-plate capacitance value with the increase of the modes used in (21).

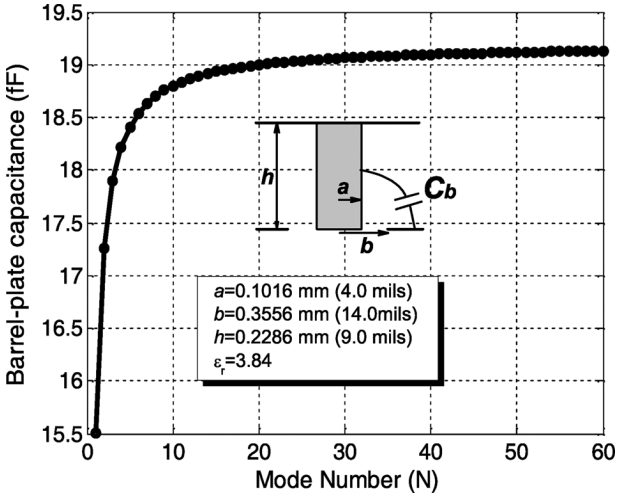

Fig. 10. Convergence of the barrel-plate capacitance in (21) with the increase of the mode number N.

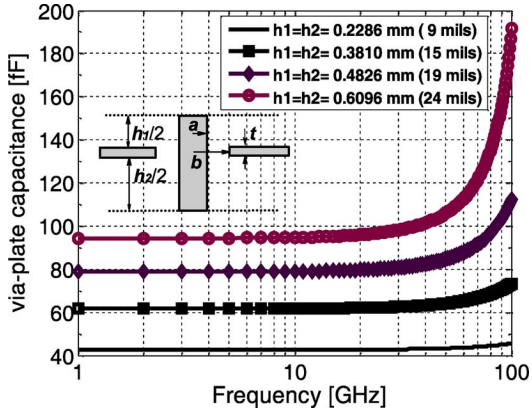

Fig. 12. Frequency-dependence of the via-plate capacitance in (25) with different via height ($a = 0.1016$ mm (4 mil), $b = 0.3556$ mm (14 mil), $t = 0.0254$ mm (1 mil), $\varepsilon_r = 3.84$).

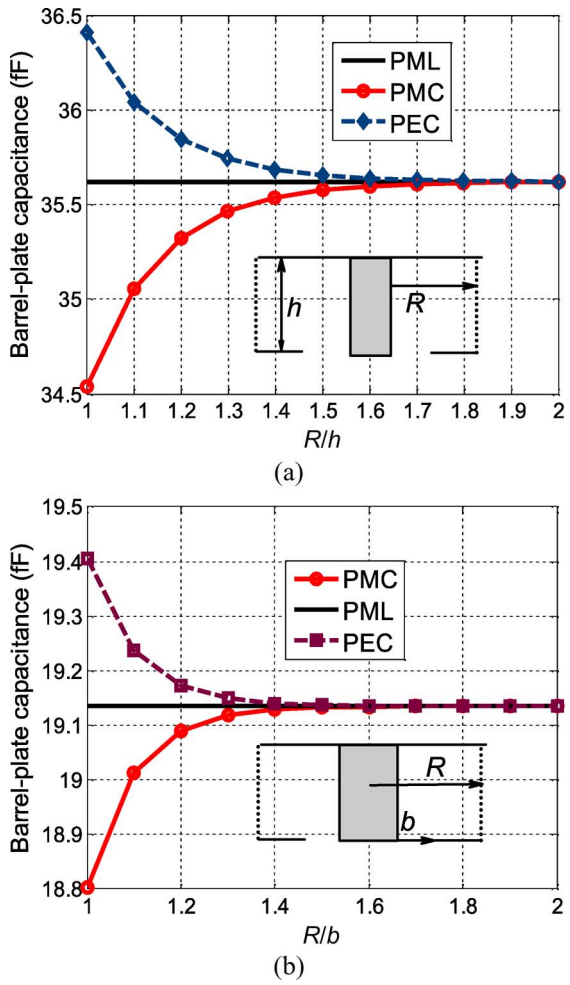

Fig. 11. Impact of the different radii of the outer boundaries on the via barrel-plate capacitance in (21). (a) $h = 0.4572$ mm (18 mil). (b) $h = 0.2286$ mm (9 mil) ($a = 0.1016$ mm (4 mil), $b = 0.3556$ mm (14 mil), $\varepsilon_r = 3.84$).

This demonstrates that the analytical formula is much more computationally efficient than numerical solutions.

The via height or separation of plane pair has a direct impact on the decay rate of the higher order modes. Fig. 11(a) presents the convergence of (21) with different radii and boundary conditions. In this example, the via height is larger than the radius of via antipad. It can be seen that with the increase of the outer boundary radius R, the via barrel-plate capacitances extracted by (21) for either PMC or PEC outer boundaries converge to that obtained for nonreflective PML boundary. The outer boundary condition has little impact on the barrel-plate capacitance evaluation when R is greater than $1.7h$. Fig. 11(b) shows another example geometry where the via antipad radius is larger than the via height. Similarly, the boundary condition of outer boundary R has a negligible impact on the evaluation of the barrel-plate capacitance when R is greater than $1.7b$. This is because the higher order TM_z modes excited by the magnetic frill currents decay rapidly in the radial direction in the parallel-plate waveguide. In this special case, when the condition $R \geq 1.7\max(h, b)$ is satisfied, all the higher order modes can be neglected at the outer boundary.

The introduction of outer boundary R in (21) provides an easy way to judge whether higher order modes are required to model coupling between two adjacent vias. In practical designs, when the via structures are the same, the distance between two vias is at least two times their antipad radii in most of the cases. This implies that, in these cases, only the dominate mode, i.e., TM_{z0}, is needed to determine the mutual via coupling. This justifies the via circuit model shown in Fig. 1(b), where each via is modeled individually and the mutual coupling is included in the parallel-plate impedance Z_{pp} that only considers the dominant TM_{z0} mode. However, when the separation of two adjacent vias, namely, d, is small enough that the barrel-plate capacitance cannot converge with different boundary conditions at $R = d$, the via coupling cannot be accurately described by the circuit model shown in Fig. 1(b). Then multiple scattering of the higher order modes must be considered by a more rigorous method such as the Foldy–Lax multiple scattering method [4], [15]–[17].

Fig. 12 shows the frequency-dependent via-plate capacitances for different via heights or separations of the plate pair. It can be seen that smaller via height results in weaker frequency dependence. In the case of a via height of 0.6096 mm (24 mil), the via-plate capacitance increases from 95 fF at 10 GHz to

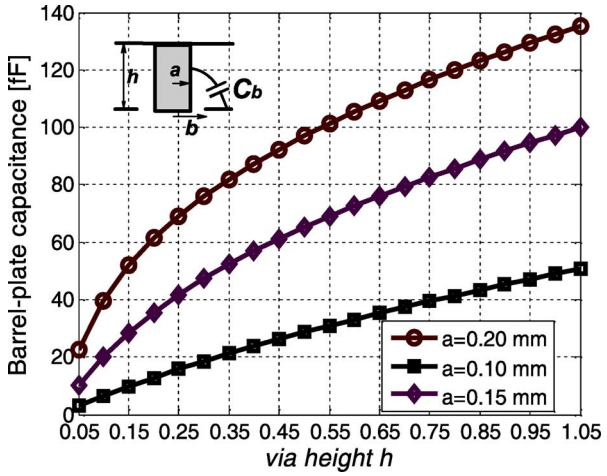

Fig. 13. Barrel-plate capacitance versus via height with a fixed antipad radius ($b = 0.25$ mm, $\varepsilon_r = 3.84$).

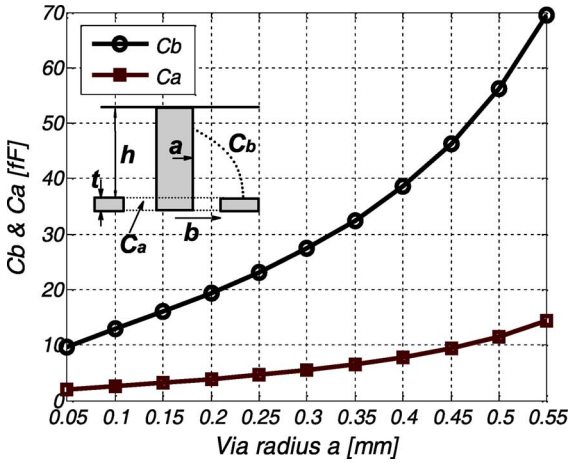

Fig. 14. Barrel-plate and coaxial capacitances versus the via radius with fixed antipad radius and via height ($b = 0.8$ mm, $h = 0.254$ mm, $t = 0.0254$ mm, $\varepsilon_r = 3.84$).

more than 195 fF at 100 GHz. Therefore, when the via height is large, the via-plate capacitance cannot be viewed as a constant value at high frequencies. A frequency-dependent capacitance must be adopted to ensure the accuracy of the circuit model. This is one of the main advantages of the analytical formula over a quasi-static approach. Note that the coaxial capacitance in (3) does not change with frequencies. Thus, the frequency dependence in the via-plate capacitance is solely caused by the barrel-plate capacitance in (21).

Fig. 13 shows the via barrel-plate capacitance versus via height. It indicates that the via barrel-plate capacitance increases monotonically with the via height, and, in the case of the same antipad radius, a larger via radius leads to a larger capacitance.

Fig. 14 compares the barrel-plate capacitance by (21) and the coaxial capacitance by (3) with the increase of the via radius. It can be seen that with the fixed antipad radius and via height, these capacitances increase steadily. Although the per unit length coaxial capacitance is larger than its barrel-plate counterpart, the barrel-plate capacitance is larger than the coaxial capacitance since the via height is usually much larger than the plate thickness.

Finally, it is worth mentioning that, in this paper, only one signal via is illustrated in a multilayer plate pair structure. However, as already demonstrated in [23] and [24], the via circuit model can be easily extended into multiple via cases. The impedance of plate pair Z_{pp} then becomes an $N \times N$ matrix if there are N vias in the plate pair. These vias can be either signal vias or power/ground vias. The impedance matrix Z_{pp} not only acts as a return path for each via, but also takes into account the via coupling among different vias due to the propagating TM_{z0} mode.

When vias are placed extremely close to each other, the higher order TM_z modes are not contained in a local region adjacent to each via any more. They could result in the coupling among the vias that is not considered in the via circuit model in [23] and [24].

VII. Conclusion

By introducing the reflection coefficients for the cylindrical waves from the inner and outer boundaries, the Green's function for a concentric magnetic ring current in a general bounded coaxial cavity is first derived as a summation of all the TM_z modes in a parallel-plate waveguide. The Green's function is valid for any general inner and outer boundaries with PEC/PMC or nonreflective PMLs. Previous studies have demonstrated that the TEM mode in a coaxial geometry is a good approximation for the tangential electric field in the antipad of a via. Based on this approximation, the vertical currents along the via can be obtained through the convolution of the magnetic frill current with the derived Green's function. By enforcing current continuity, a displacement current from the via barrel to the metal plate is obtained. Thus, an analytical formula is found based on the displacement current to calculate the via barrel-plate capacitance, which is expanded as a summation of all the odd TM_z modes. The analytical formula has been validated by the comparisons with quasi-static numerical solvers, as well as the measurement of a multilayer test board. The formula is demonstrated to be computationally efficient as only tens of the higher order modes are required to achieve a convergence. This is due to the fact that as the separation of the power/ground plates is electrically small, the higher order TM_z modes decay rapidly along the radial direction of a via. This also explains the fact that the via capacitance converges quickly with the increase of the radius of the outer boundary no matter which type of boundary condition is applied. In addition, the analytical formula gives the frequency dependence of the barrel-plate capacitance. Studies show that the frequency dependence of the barrel-plate capacitance has to be included for large via heights at high frequencies. This helps validate the frequency limitations of a via circuit model. The analytical formula for the via-plate capacitance is more convenient than any numerical methods in terms of its compatibility with circuit simulators.

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REFERENCES

[1] H. W. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. New York: Prentice-Hall, 1993, ch. 7.

[2] S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design-A Handbook of Interconnect Theory and Design Practices*. New York: Wiley, 2000, ch. 5.

[3] E. Laermans, J. Geest, D. Zutter, F. Olyslager, S. Sercu, and D. Morlion, "Modeling complex via hole structure," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 206–214, May 2002.

[4] H. Chen, Q. Lin, L. Tsang, C.-C. Huang, and V. Jandhyala, "Analysis of a large number of vias and differential signaling in multilayered structures," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 818–829, Mar. 2003.

[5] S. Maeda, T. Kashiwa, and I. Fukai, "Full wave analysis of propagation characteristics of a through hole using the finite-difference time-domain method," *IEEE Trans. Microw. Theory Tech.*, vol. 39, no. 12, pp. 2154–2159, Dec. 1991.

[6] S.-G. Hsu and R.-B. Wu, "Full-wave characterization of a through hole via in multilayered packaging," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 5, pp. 1073–1081, May 1995.

[7] T. Wang, R. F. Harington, and J. R. Mautz, "Quasi-static analysis of a microstrip via through a hole in a ground plane," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 6, pp. 1008–1013, Jun. 1988.

[8] P. Kok and D. De Zutter, "Capacitance of a circular symmetric model of a via hole including finite ground plane thickness," *IEEE Trans. Microw. Theory Tech.*, vol. 39, no. 7, pp. 1229–1234, Jul. 1991.

[9] P. A. Kok and D. D. Zutter, "Prediction of the excess capacitance of a via-hole through a multilayered board including the effect of connecting microstrips or striplines," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 12, pp. 2270–2276, Dec. 1994.

[10] K. S. Oh, J. E. Schutt-Aine, R. Mittra, and W. Bu, "Computation of the equivalent capacitance of a via in a multilayered board using the closed-form Green's function," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 2, pp. 347–349, Feb. 1996.

[11] A. W. Mathis, A. F. Peterson, and C. M. Butler, "Rigorous and simplified models for the capacitance of a circularly symmetric via," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 10, pp. 1875–1878, Oct. 1997.

[12] F. Tefiku and E. Yamashita, "Efficient method for the capacitance calculation of circularly symmetric via in multilayered media," *IEEE Microw. Guided Wave Lett.*, vol. 5, no. 9, pp. 305–307, Sep. 1995.

[13] Q. Gu, Y. E. Yang, and M. A. Tassoudji, "Modeling and analysis of vias in multilayered integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 2, pp. 206–214, Feb. 1993.

[14] Q. Gu, A. Tassoudji, S. Y. Poh, R. T. Shin, and J. A. Kong, "Coupled noise analysis for adjacent vias in multilayered digital circuits," *IEEE Trans. Circuits Syst.*, vol. 41, no. 12, pp. 796–804, Dec. 1994.

[15] L. Tsang and D. Miller, "Coupling of vias in electronic packaging and printed circuit board structures with finite ground plane," *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 375–384, Nov. 2003.

[16] C.-J. Ong, D. Miller, L. Tsang, B. Wu, and C.-C. Huang, "Application of the Foldy–Lax multiple scattering method to the analysis of vias in ball grid arrays and interior layers of printed circuit boards," *Microw. Opt. Technol. Lett.*, vol. 49, no. 1, pp. 225–231, Jan. 2007.

[17] X. Gu and M. B. Ritter, "Application of Foldy–Lax multiple scattering method to via analysis in multi-layered printed circuit board," in *DesignCon. 2008*, Santa Clara, CA, Feb. 4–7 2008, pp. 1–18, PCB and passive component technology, Track 5, 5-TA2.

[18] Y. T. Lo, D. Solomon, and W. F. Richards, "Theory and experiment on microstrip antennas," *IEEE Trans. Antennas Propag.*, vol. AP-27, no. 2, pp. 137–145, Mar. 1979.

[19] G.-T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, and B. K. Gilbert, "Wave model solution to the ground/power plane noise problem," *IEEE Trans. Instrum. Meas.*, vol. 44, no. 2, pp. 300–303, Apr. 1995.

[20] Z. L. Wang, O. Wada, Y. Toyota, and R. Koga, "Convergence acceleration and accuracy improvement in power bus impedance calculation with a fast algorithm using cavity modes," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 1, pp. 2–9, Feb. 2005.

[21] Y. Joeong, A. C. Lu, L. L. Wai, W. Fan, B. K. Lok, H. Park, and J. Kim, "Hybrid analytical modeling method for split power bus in multilayered package," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 82–94, Feb. 2006.

[22] C. Wang, J. Mao, G. Selli, S. Luan, L. Zhang, J. Fan, D. J. Pommerenke, R. E. DuBroff, and J. L. Drewniak, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Trans. Adv. Packag.*, vol. 29, no. 2, pp. 320–334, May 2006.

[23] C. Schuster, Y. Kwark, G. Selli, and P. Muthana, "Developing a 'physical' model for vias," in *DesignCon. 2006*, Santa Clara, CA, USA, Feb. 6–9, 2006, pp. 1–24, Multi-gigabit interconnect design, Track 8, 8-WA2.

[24] G. Selli, C. Schuster, Y. H. Kwark, M. B. Ritter, and J. L. Drewniak, "Developing a physical via model for vias—Part II: Coupled and ground return vias," in *DesignCon. 2007*, Santa Clara, CA, Jan. 29–Feb. 1 2007, pp. 1–22, PCB and package technology, Track 6, 6-TA3.

[25] G. Selli, C. Schuster, and Y. Kwark, "Model-to-hardware correlation of physics based via models with the parallel-plate impedance included," in *Proc. IEEE Electromagn. Compat. Symp.*, Portland, OR, Aug. 14–18, 2006, pp. 781–785.

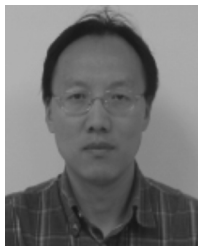
[26] M. Pajovic, J. Xu, and D. Milojkovic, "Analysis of via capacitance in arbitrary multilayer PCBs," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 3, pp. 722–726, Aug. 2007.

[27] J.-X. Zheng and D. C. Chang, "End-correction network of a coaxial probe for microstrip patch antennas," *IEEE Trans. Antennas Propag.*, vol. 39, no. 1, pp. 115–118, Jan. 1991.

[28] H. Xu, D. R. Jackson, and J. T. Williams, "Comparison of models for the probe inductance for a parallel plate waveguide and a microstrip patch," *IEEE Trans. Antennas Propag.*, vol. 53, no. 10, pp. 3229–3235, Oct. 2005.

[29] N. Marcuvitz, *Waveguide Handbook*, ser. Radiat. Lab. Cambridge, MA: MIT, 1951, ch. 2, p. 74.

[30] B. Tomasic and A. Hessel, "Electric and magnetic current sources in the parallel plate waveguide," *IEEE Trans. Antennas Propag.*, vol. AP-35, no. 11, pp. 1307–1310, Nov. 1987.



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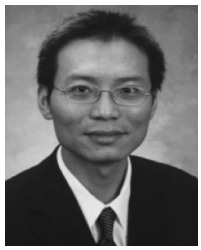

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