Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz

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***Abstract*—Analytical models for vias and traces are presented for simulation of multilayer interconnects at the package and printed circuit board levels. Vias are modeled using an analytical formulation for the parallel-plate impedance and capacitive elements, whereas the trace-via transitions are described by modal decomposition. It is shown that the models can be applied to efficiently simulate a wide range of structures. Different scenarios are analyzed including thru-hole and buried vias, power vias, and coupled traces routed into different layers. By virtue of the modal decomposition, the proposed method is general enough to handle structures with mixed reference planes. For the first time, these models have been validated against full-wave methods and measurements up to 40 GHz. An improvement on the computation speed of at least two orders of magnitude has been observed with respect to full-wave simulations.**

***Index Terms*—Modal decomposition, package, power distribution network (PDN), printed circuit board (PCB), via models.**

I. Introduction

MODERN high-speed digital systems often require thousands of off-chip interconnect elements to interface heterogeneous components such as processing units, memory, storage devices, and network interfaces. Several high-speed protocols for wired links have recently become industry standards, many of them targeting data rates in excess of 10 Gbits/s [1]. Off-chip interconnects—namely, package and printed circuit board (PCB) level interconnects—often constitute the bottleneck for the maximal achievable data rate since they introduce frequency-dependent degradation and distortions on signal paths [2]. Efficient modeling and simulation of off-chip interconnects become essential to assist the design process and to look for the best tradeoff between cost and performance. This is a challenging task because of the large number of interconnects that must be considered to model a realistic scenario.

Different modeling strategies can be found in the literature to address this problem (see, e.g., [3]–[5]). Most of them are based on numerical methods, whose computational burden rapidly grows as the size and complexity of the interconnect structure increase. To overcome this limitation, analytical models for power distribution networks (PDNs) have been proposed in the past [6], [7], and more recently, analytical and semianalytical techniques have been presented addressing different aspects of the problem from a system-level perspective (e.g., [8]–[10]). In our study, we extend the scope of previous publications with an efficient modeling strategy applicable to relatively complex via-to-via links over a broader frequency range and validated in several scenarios. Our method relies on physics-based models, which describe the interconnects in terms of equivalent circuits or network representations that can be scaled according to physical geometry and material properties. These analytical formulations are not only computationally efficient, they also lend insight into the structure under investigation and into the basic physical mechanisms involved. Since these models can be parameterized, they are suitable for rapid prototyping and design optimization.

In previous work of the authors, the physics-based via models have been presented [11]–[14] and cast in their microwave network parameter form [15]. The parallel-plate impedance is used to describe the interaction between the vias and propagating modes supported by the planes of the PDN. Capacitive elements are used to approximate the near-field interaction between the planes and vias. The models have been extended in [16] to include the traces routed between the vias by applying the modal decomposition technique presented in [17]. Here, the models are described in their general form for an arbitrary number of vias and traces. This approach can also be extended to an arbitrary number of layers by using segmentation techniques [18]. In summary, the main contributions of this paper are as follows.

1) The combined via and trace physics-based models are presented in their general form for an arbitrary number of elements, and a suitable framework for their utilization, considering multilayer structures, is introduced. The models are applied to simulate full pad-to-pad single-ended and differential links.

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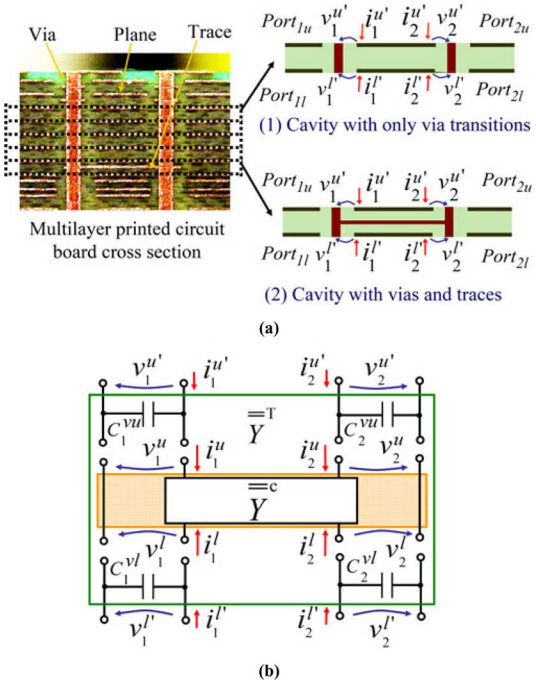

Fig. 1. Approach used to model multilayer board structures with vias and internal traces connecting vias. (a) Each cavity is modeled separately for both layers with only via transitions (1) or with vias and stripline transitions (2). (b) General equivalent network representation of the model, where the matrix Y^c corresponds to the parallel-plate model when only via transitions are present or to the superposition of the parallel-plate and stripline transmission line models when via and traces are present.

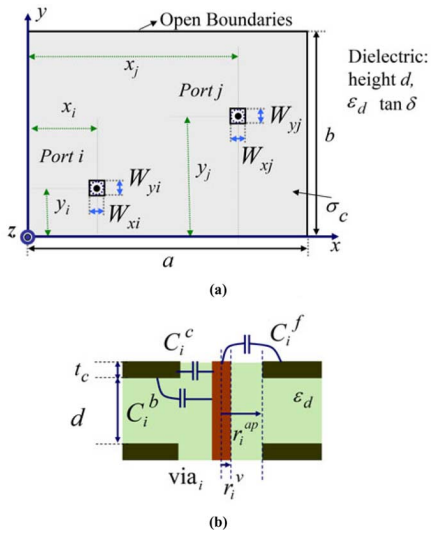

Fig. 2. Computation domains for the via model building blocks. (a) Parallel-plate impedance parameters of a rectangular board. (b) Via capacitance definition for a via segment (only top side shown).

2) A wide range of application examples is provided. It is demonstrated that the models can be applied to cases including thru-hole and buried vias, power vias, traces, and coupled conductors (e.g., differential links). In addition, the method is suitable to model structures containing mixed reference planes.
3) The models have been validated against full-wave methods and measurement up to 40 GHz. It is shown that the model efficiency is very good, making feasible fast and accurate modeling of links with realistic complexity.

II. Combined Model for Vias Connected by Traces

A. Via Model

The via model is inspired by previous solutions found in the literature [7], [19], [20], which make use of a layered partitioning approach (Fig. 1). Its basic cell corresponds to the via segments crossing a cavity enclosed by two reference planes, as illustrated in Fig. 1(a). Two different mechanisms are used to describe the via transitions (without considering traces) [9]: the parallel-plate impedance Z^{pp}, to describe the interaction between the via transitions and the reference planes in terms of cavity modes, and the via barrel-to-plane capacitance, to approximate the fringing fields in the near region around vias.

The parallel-plate impedance is calculated from closed-form expressions developed for planar circuits. For instance, a 2-D cavity resonator model can be used to calculate Z^{pp} at each via location [21], [22]. The impedance is computed by solving the 2-D Helmholtz equation with appropriate boundary conditions on the periphery of the cavity. With the definitions of Fig. 2(a), the impedance between two arbitrarily placed ports in a pair of rectangular planes can be written as [22]

$$Z_{ij}{}^{pp}(\omega) = \frac{j\omega\mu d}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty} c_m^2 c_n^2 \frac{f_{\text{B.C.}}\cdot f_P}{k_m{}^2 + k_n{}^2 - k^2} \quad (1)$$

where $c_m, c_n = 1$ for $m, n = 0$, and $c_m, c_n = \sqrt{2}$ for $m, n \neq 0$, $k_m = m\pi/a$, $k_n = n\pi/b$, and f_P equal to

$$f_P = \text{sinc}\left(\frac{k_m W_{xi}}{2}\right)\cdot\text{sinc}\left(\frac{k_n W_{yi}}{2}\right) \cdot\text{sinc}\left(\frac{k_m W_{xj}}{2}\right)\cdot\text{sinc}\left(\frac{k_n W_{yj}}{2}\right) \quad (1a)$$

with $\text{sinc}(x) = \sin(x)/x$. The size of the rectangular port in the cavity model formulation is adjusted to provide an equivalent circular via perimeter $W_{xi} = W_{yi} = \pi\cdot r_i^v/2$, where r_i^v stands for the via radius of the ith via. Applying perfect magnetic conductor (PMC) boundary conditions to the cavity edges, to approximate an open boundary, the function $f_{\text{B.C.}}$ becomes

$$f_{\text{B.C.}} = \cos(k_m x_i)\cdot\cos(k_n y_i)\cdot\cos(k_m x_j)\cdot\cos(k_n y_j). \quad (1b)$$

The complex waveguide number is defined as [21]

$$k = \omega\sqrt{\mu_d\varepsilon_d}\cdot\left(1 - j\left(\frac{(\tan\delta + d_s/d)}{2}\right)\right) \quad (1c)$$

to account for dielectric loss $(\tan\delta)$ and electric conductor loss $(d_s = \sqrt{2/\omega\mu_c\sigma_c})$ at high frequencies.

Further closed-form expressions to compute the parallel-plate impedance using the cavity model are available for regular shapes [21]—for which the Green's function is known, and for infinite planes, using radial waveguide theory [23]. In combination with image theory, the formulation for infinite planes can be adapted to model finite rectangular structures, as

detailed in [24]. For irregular planes, segmentation techniques can be used if the shape can be partitioned into regular ones [25]. The modeling of irregular shaped planes by contour-integral methods [26] constitutes another alternative that it is currently being investigated.

Since the computation of the parallel-plate impedance is time consuming for large boards and broad bandwidths, acceleration techniques are essential to improve the computation efficiency of the series. For rectangular plates, the double summation in (1) can be reduced to a single summation, as reported in [27]–[29].

For electrically small ports, Z^{pp} is interpreted as the impedance seen at the via locations, approximated as the ratio of voltage to current along each via barrel segment (v_i/i_i). Here, it is assumed that the fields inside the cavity do not vary with the z-coordinate, and therefore, the cavities should be electrically thin. The parallel-plate impedance formulas are used to construct the 2-D impedance matrix per frequency point

$$\overline{V} = \overline{\overline{Z}}^{pp} \cdot \overline{I} \tag{2}$$

where the vectors $\overline{V}$ and $\overline{I}$ contain the voltages and currents defined for each via segment, respectively. Since it is necessary to provide top and bottom connection nodes for the vias in order to interconnect the different cavities, the following voltage and current relations are applied on each port i [15]:

$$\begin{aligned} v_i &= {v_i}^u - {v_i}^l \\ i_i &= {i_i}^u = -{i_i}^l. \end{aligned} \tag{3}$$

The index u stands for the upper side and the index l stands for the lower side of the cavities. The resulting matrix in terms of microwave network parameters explicitly defines the ports on both sides. For instance, in terms of Y-parameters [16],

$$\begin{bmatrix} \overline{I}^u \\ \overline{I}^l \end{bmatrix} = \underbrace{\begin{bmatrix} \overline{\overline{Y}}^{pp} & -\overline{\overline{Y}}^{pp} \\ -\overline{\overline{Y}}^{pp} & \overline{\overline{Y}}^{pp} \end{bmatrix}}_{\overline{\overline{Y}}^c} \cdot \begin{bmatrix} \overline{V}^u \\ \overline{V}^l \end{bmatrix} \tag{4}$$

with $\overline{\overline{Y}}^{pp} = {\overline{\overline{Z}}^{pp}}^{-1}$.

For the inhomogeneous near-field region close to the vias, capacitances are used to approximate the effect of these fringing fields. These capacitances account for the displacement current between the via barrel and the planes, and it can be computed, for example, by means of static solvers, fitting formulas [12]–[14], or closed-form expressions [30]. The via barrel to plane capacitance can be calculated, as depicted in Fig. 2(b) for an upper via side, by

$${C_i}^v = {C_i}^c + {C_i}^b + {C_i}^f \tag{5}$$

where the via-plane coaxial capacitance is given by

$${C_i}^c = \frac{2\pi\varepsilon_d t_c}{\ln\left(\dfrac{{r_i}^{ap}}{{r_i}^v}\right)}. \tag{5a}$$

For adjacent cavities, the coaxial capacitance in (5a) is considered only once, whereas for thick reference planes, it can be replaced by a coaxial transmission line segment in order to map the plane thickness.

If the distance to plane edges is sufficient to assume infinite large planes, the via-plane lateral capacitance is computed from [30]

$${C_i}^b = \frac{8\pi\varepsilon_d}{d \cdot \ln\left(\dfrac{{r_i}^{ap}}{{r_i}^v}\right)} \sum_{n=1,3,5\ldots}^{2N-1} \frac{1}{{k_n}^2 {H_o}^{(2)}(k_n {r_i}^v)} \cdot \left\{ \left[{H_o}^{(2)}(k_n {r_i}^{ap}) - {H_o}^{(2)}(k_n {r_i}^v) \right] \right\} \tag{5b}$$

where $k_n = \pm\sqrt{\omega^2\mu_d\varepsilon_d - (n\pi/d)^2}$ and ${H_o}^{(2)}$ the Hankel function of second type and order 0. The series in (5b) shows a fast convergence: for the study cases, $N = 20$ was sufficient to achieve good results.

The fringing capacitance ${C_i}^f$ serves to approximate the aperture fields at via ends, and it is considered only for the first and last via segments. Static solvers are used to extract the value of this capacitance.

Including the via capacitances, the via model (see Fig. 1) can be seen as a π-network. In terms of Y-parameters, the contribution of the parallel-plate impedance and the capacitive elements can be clearly identified according to [16]

$$\begin{bmatrix} \overline{I}^{u'} \\ \overline{I}^{l'} \end{bmatrix} = \left(\underbrace{\begin{bmatrix} \overline{\overline{Y}}^{vu} & \overline{\overline{0}} \\ \overline{\overline{0}} & \overline{\overline{Y}}^{vl} \end{bmatrix}}_{\overline{\overline{Y}}^v} + \underbrace{\begin{bmatrix} \overline{\overline{Y}}^{pp} & -\overline{\overline{Y}}^{pp} \\ -\overline{\overline{Y}}^{pp} & \overline{\overline{Y}}^{pp} \end{bmatrix}}_{\overline{\overline{Y}}^c} \right) \cdot \begin{bmatrix} \overline{V}^{u'} \\ \overline{V}^{l'} \end{bmatrix}. \tag{6}$$

The capacitive elements are arranged in a diagonal matrix in which each entry is defined as ${Y_i}^v = 1/{Z_i}^v = j\omega {C_i}^v$ for the top and bottom sides. The vectors of size n, $\overline{V}^{u'}$ and $\overline{I}^{u'}$, denote the via voltages and currents defined on the upper cavity side, and the vectors $\overline{V}^{l'}$, $\overline{I}^{l'}$, on the lower side.

B. Via Model Including Stripline Transition

The model for vias can be extended to include traces connecting vias by accounting for the contribution of the stripline mode. Two modes are included in this case, the parallel-plate mode, discussed in Section II-A, and the stripline transmission line mode. Assuming that both modes are only coupled at via locations, it is possible to compute each one separately and apply modal decomposition to combine them by selecting suitable transformation matrices [31]. The problem of a stripline routed between nonideal reference planes has been previously solved in [17]. Defining the lower plane as the reference potential, the following transformation matrices can be found to couple/decouple the two modes at every via location [17]

$$\begin{pmatrix} {i_i}^u \\ {i_i}^s \end{pmatrix} = \begin{pmatrix} 1 & k_i \\ 0 & 1 \end{pmatrix} \begin{pmatrix} {i_i}^{pp} \\ {i_i}^{tl} \end{pmatrix} \tag{7a}$$

$$\begin{pmatrix} {\phi_i}^u - {\phi_i}^l \\ {\phi_i}^s - {\phi_i}^l \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -k_i & 1 \end{pmatrix} \begin{pmatrix} {v_i}^{pp} \\ {v_i}^{tl} \end{pmatrix}. \tag{7b}$$

The indices u and l denote the upper and lower planes, whereas the indices pp and tl are associated with the parallel-plate mode, and the stripline transmission line mode, respectively [see Fig. 3(a)].

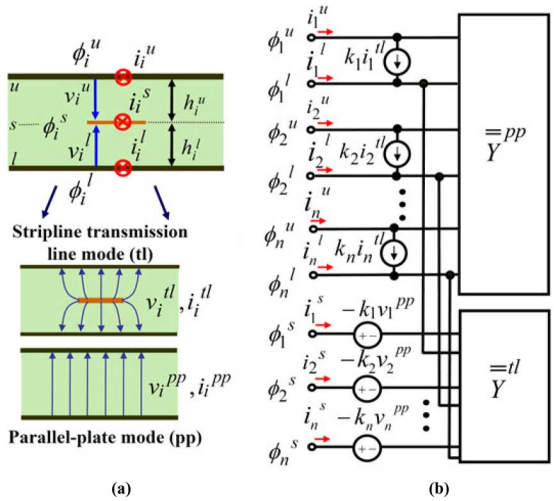

Fig. 3. Modal decomposition approach to model vias connected by traces. (a) Terminal and modal parameter definition. (b) Equivalent circuit for n-ports.

Neglecting the trace thickness, a simple formula for k can be obtained in terms of a dielectric height ratio [17]

$$k_i = -\frac{{h_i}^l}{{h_i}^l + {h_i}^u}. \tag{8}$$

The expressions in (7a) and (7b) can be translated to an equivalent circuit with n-ports, as illustrated in Fig. 3(b). From it, a system of equations can be derived for the upper and lower voltages with respect to the signal (via) terminal ${v_i}^u = {\phi_i}^u - {\phi_i}^s$, ${v_i}^l = {\phi_i}^l - {\phi_i}^s$, and the currents ${i_i}^u$, ${i_i}^l$, resulting in the following expression written in terms of Y-parameters [16]:

$$\begin{pmatrix} \overline{I}^u \\ \overline{I}^l \end{pmatrix} = \underbrace{\begin{pmatrix} k^2\overline{\overline{Y}}^{tl} + \overline{\overline{Y}}^{pp} & (-k^2-k)\overline{\overline{Y}}^{tl} - \overline{\overline{Y}}^{pp} \\ (-k^2-k)\overline{\overline{Y}}^{tl} - \overline{\overline{Y}}^{pp} & (k^2+2k+1)\overline{\overline{Y}}^{tl} + \overline{\overline{Y}}^{pp} \end{pmatrix}}_{\overline{\overline{Y}}^c} \cdot \begin{pmatrix} \overline{V}^u \\ \overline{V}^l \end{pmatrix}. \tag{9}$$

The port definition used allows the manipulation of single cavities as standalone blocks: (9) replaces (4) when traces are present. The matrices for the parallel-plate and stripline model are defined, respectively, as

$$\overline{I}^{pp} = \overline{\overline{Y}}^{pp}\overline{V}^{pp} \tag{10a}$$

$$\overline{I}^{\mathrm{tl}} = \overline{\overline{Y}}^{\mathrm{tl}}\overline{V}^{\mathrm{tl}}. \tag{10b}$$

The $\overline{\overline{Y}}^{\mathrm{tl}}$ term contains the transmission line admittance matrix assuming ideal planes. For example, for a simple case of two via transitions connected by a trace, it corresponds to a two-port network of a stripline with its input and output defined at the via port locations. The transmission line model can be computed with 3-D solvers, 2-D solvers if a uniform cross section serves as a good approximation, or closed-form expressions when available. It could be either coupled or uncoupled, which allows the modelling of, for instance, differential links and crosstalk coming from traces.

C. Generalized Model for Vias and Traces

Taking the admittance matrix in (9) and adding the capacitances of the via model in (6), a generalized model can be formulated for one cavity with n vias and m traces. In terms of Y-parameters, the block matrices are expressed as

$$\begin{aligned} \overline{\overline{Y}}^T = &\begin{pmatrix} \overline{\overline{Y}}^{vu} & \overline{\overline{0}} \\ \overline{\overline{0}} & \overline{\overline{Y}}^{vl} \end{pmatrix} + \begin{pmatrix} +\overline{\overline{Y}}^{pp} & -\overline{\overline{Y}}^{pp} \\ -\overline{\overline{Y}}^{pp} & +\overline{\overline{Y}}^{pp} \end{pmatrix} \\ &+ \begin{pmatrix} -k\overline{\overline{Y}}^{tl} & \overline{\overline{0}} \\ \overline{\overline{0}} & (k+1)\overline{\overline{Y}}^{tl} \end{pmatrix} \\ &+ \begin{pmatrix} (k^2+k)\overline{\overline{Y}}^{tl} & -(k^2+k)\overline{\overline{Y}}^{tl} \\ -(k^2+k)\overline{\overline{Y}}^{tl} & (k^2+k)\overline{\overline{Y}}^{tl} \end{pmatrix}. \end{aligned} \tag{11}$$

Equation (11) describes the general network-level building block depicted in Fig. 1(b). The contribution of four elements can be identified, namely, the via-to-plate capacitances, the parallel-plate impedance, the stripline mode—expressed as lines coupled with the top and bottom planes and related by the factor k, and a fourth factor, which results from the superposition of the parallel-plate impedance and stripline mode. A similar formulation to the one used here to model traces has been recently presented by Wei *et al.* in [9]. However, in their solution, the fourth term in (11) is neglected. We have concluded that the complete expression is more accurate at higher frequencies. For instance, for the case discussed in Section III-A, the effect of the fourth term starts to be noticeable for frequencies above 6 GHz. When this term is neglected, the magnitude of the S-parameters can show a deviation in the range of 2 dB and more.

For vias not connected by traces, the entries related to the transmission line model (third and fourth factors) become zero, and the expression is reduced to (6) for such elements. The factor k is assumed to be equal for all the elements inside the cavity. However, if this is not the case, the factor can be calculated independently for the different ports of the structure and k becomes a matrix. This makes possible to solve cases with more than one signal layer routed between two reference planes, provided that the coupling between the layers is properly mapped in the transmission line model.

D. Concatenation of Model Components

The presented model for vias and traces can be applied to compute the response for each cavity within a multilayer substrate assuming that the vias offer the only coupling path between cavities. Next, the partial results obtained for each cavity should be combined. The segmentation method [18] offers a general solution to carry out this task. The results computed for adjacent cavities can be arranged in terms of connected and disconnected ports, defining the appropriate port order. The matrices are then merged by ensuring voltage and current continuity at the connected ports.

Expressions to perform this operation are available in terms of S-, Z-, or Y- parameters [18]. Although the segmentation can

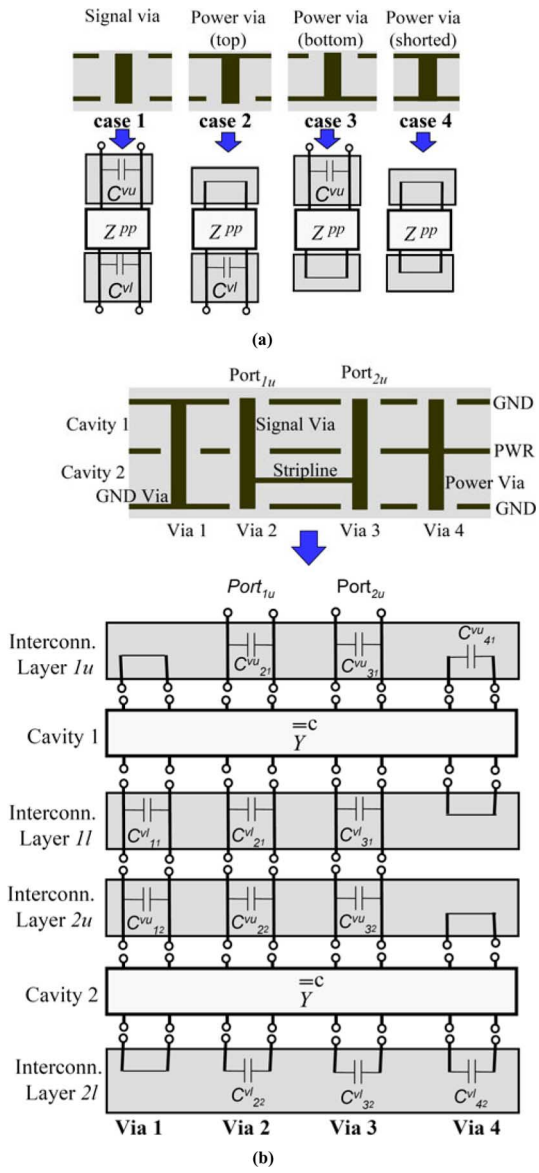

Fig. 4. Concatenation approach to model multilayer structures. (a) Via transition variants considering power vias. (b) Segmentation approach exemplified with a two-cavity four-via case.

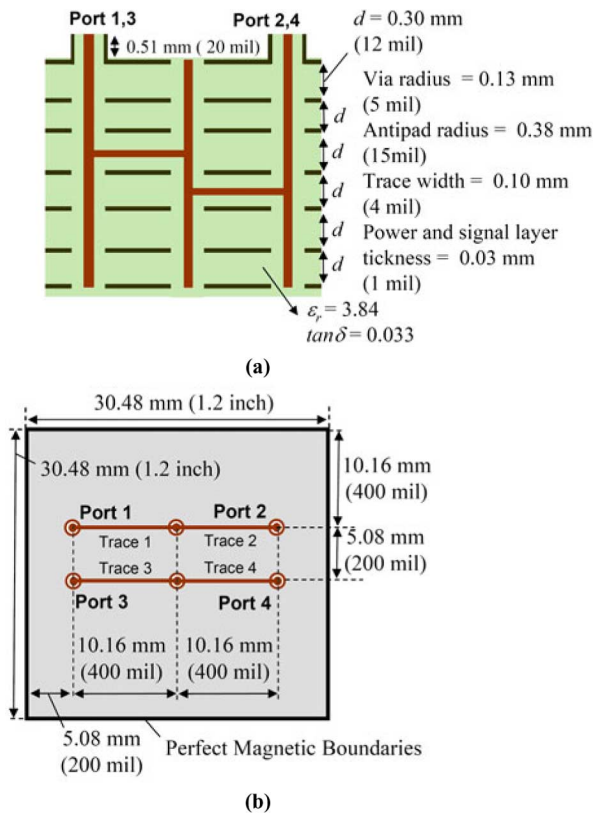

Fig. 5. Test case used to validate the model against full-wave methods. (a) Board stackup. (b) Upper view of the structure.

be more efficient in terms of impedance parameters, for complex structures, which may include power vias shorting planes or open terminations, the segmentation in terms of S-parameters shows better numerical stability.

In order to map power vias into the models, the matrix containing the via-to-plane capacitances needs to be extended to consider the connectivity of the vias as well. For this purpose, the matrix term is handled separately as interconnection layers (Fig. 4). Four different via connections are possible when accounting for power vias. In case the power via is touching the port, the via-to-plane capacitance is replaced with a short circuit. For via ends not defined as ports, the corresponding entry can be either terminated with the via segment to plane total capacitance or an open circuit. The segmentation process is illustrated in Fig. 4(b) with a simple two-layer example containing signal and power vias.

III. Application of the Models and Correlation to Full-Wave Simulation

The utilization of the models is discussed first with the structure described in Fig. 5. Two links are considered, made with single ended striplines routed in different cavities and connected by thru-hole vias in a six-cavity rectangular board. The ports are defined on the top of two vias, whereas all the other via ends were left open. The models were implemented in a software tool according to the method described in Section II. The frequency- and time-domain results are shown in Fig. 6. The transmission line models were obtained from available closed-form expressions for striplines [32] assuming a homogeneous and constant cross section. The cavity model was used to compute the parallel-plate impedance. The results were compared with respect to full-wave commercial tools in the time domain—finite integration technique (FIT) [33]—and in the frequency domain—finite-element method (FEM) [34]. The result conversion from frequency to time domain and vice versa was done by fast Fourier transform (FFT) and inverse FFT (IFFT), respectively. The feature-selective validation (FSV) method [35]–[37] was applied to quantitatively compare the results obtained between the different methods. Good agreement could be observed for the S-parameters results both in magnitude and phase. Metrics from excellent to good could be obtained for the magnitude of the S-parameters up to 20 GHz and between excellent and fair up to 40 GHz (see Fig. 6).

The computation times are summarized in Table I. The proposed models provide accurate results and drastically reduce

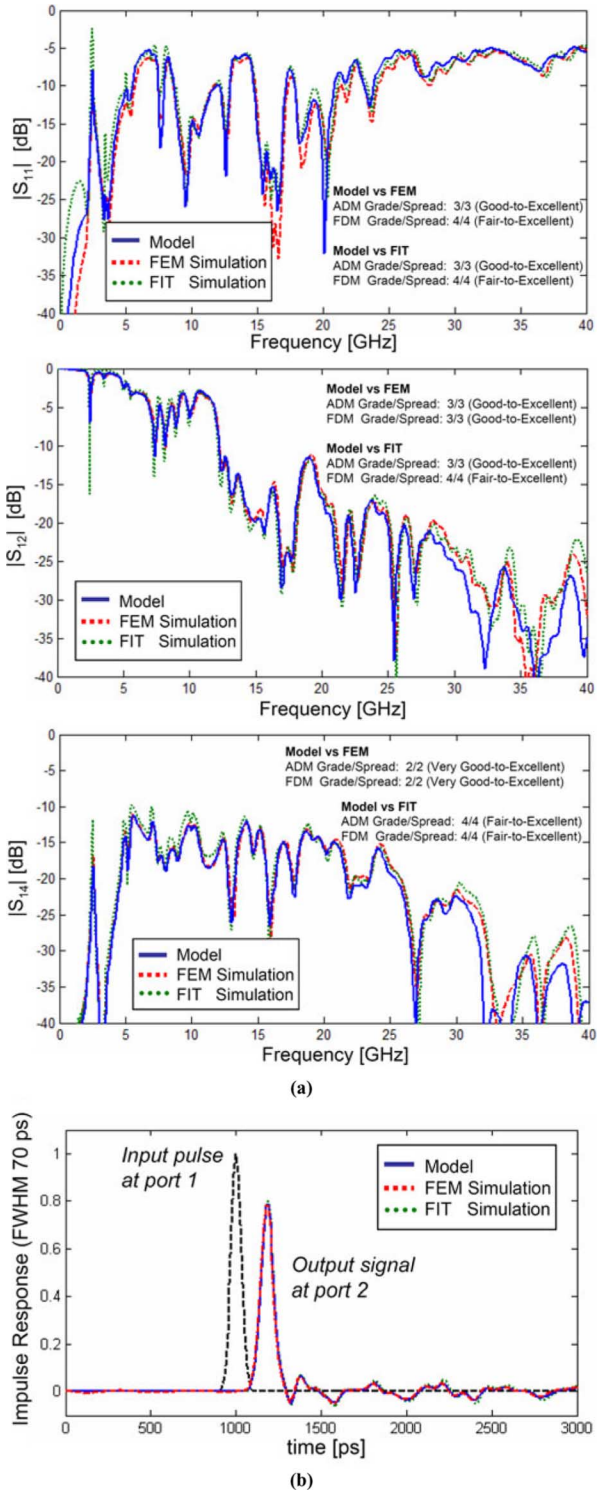

Fig. 6. Results obtained for the structure in Fig. 5 by the FIT, FEM, and the proposed models. (a) Magnitude of reflection (S_{11}), transmission (S_{12}), and far-end crosstalk (S_{14}). (b) Impulse response for a 70-ps full-width half-maximum (FWHM) pulse normalized to 1 V. Amplitude (ADM) and feature (FDM) difference metrics of the FSV method were included on the S-parameter graphs.

the computation time by about two orders of magnitude in a conservative estimate when compared to full-wave methods. In addition, acceleration methods to compute the parallel-plane impedance can be used to improve the overall efficiency. For the studied case, the simulation time could be reduced by more than 50% when the parallel-plate impedance was calculated with a single summation [27] formula instead of the double summation.

TABLE I
COMPUTATION TIME OBTAINED FOR THE DIFFERENT METHODS. FOR STRUCTURE OF FIG. 5, COMPUTED ON A DUAL CORE 3.0-GHz PC, 4-GB RAM

Finite element method simulation (200 freqs)	Finite integration technique simulation	Proposed models (200 freq. points)	
		Cavity model double sum 100x100 modes	Cavity model single sum 50 iterations
11 144 s (~3 h 5 min)	24 804 s (~4 h 53 min)	23 s	9 s

Several configurations, which can be commonly found in real board and package designs, have been modeled with the method presented here. Section III-A describe these test cases, which are derived from the baseline structure of Fig. 5.

A. *Effect of Power/Ground Vias*

It is well known that power and ground vias can improve the electrical performance of interconnects by providing additional return paths to the signals traveling along signal vias [38]. As mentioned before, the proposed method can also be used to model structures containing both signal and power/ground vias by accounting for their connectivity with the reference planes that are used for ground or for power distribution.

Power/ground vias connecting both top and bottom planes of a cavity can also be reduced right after the computation of the parallel-plate impedance by applying the Schur's complement. This operation can improve the overall efficiency of the computation since it reduces in an early stage the size of the matrices (for more details, see [15]). Signal to ground (S : G) via ratios of 1 : 1 and 1 : 2 were studied for the structure in Fig. 5, assuming that all reference planes correspond to ground planes [see Fig. 7(a)]. The models were able to capture the effect of ground vias, showing good agreement with respect to full-wave methods. In Fig. 7(b), it can be observed that the near-end crosstalk is reduced as the number of ground vias is increased. The plot also includes the comparative results obtained by the FEM simulations. The effectiveness of ground vias to improve the transmission and reduce the crosstalk is better for lower frequencies. In the study case, after 25 GHz it is difficult to differentiate between the three cases, as the crosstalk level predicted is similar for all of them. As frequency increases, more ground vias located in close proximity to the signal via become necessary to obtain an appreciable crosstalk reduction.

B. *Mixed Reference Power/Ground Planes*

In contrast to the cases discussed thus far, practical designs usually contain interleaved power and ground reference planes. The models and proposed method are flexible enough to handle these scenarios by the proper interpretation of the connectivity of the power vias with respect to the reference planes. This is an important advantage of the method since it allows the modeling of complex structures with arbitrary stackup definitions.

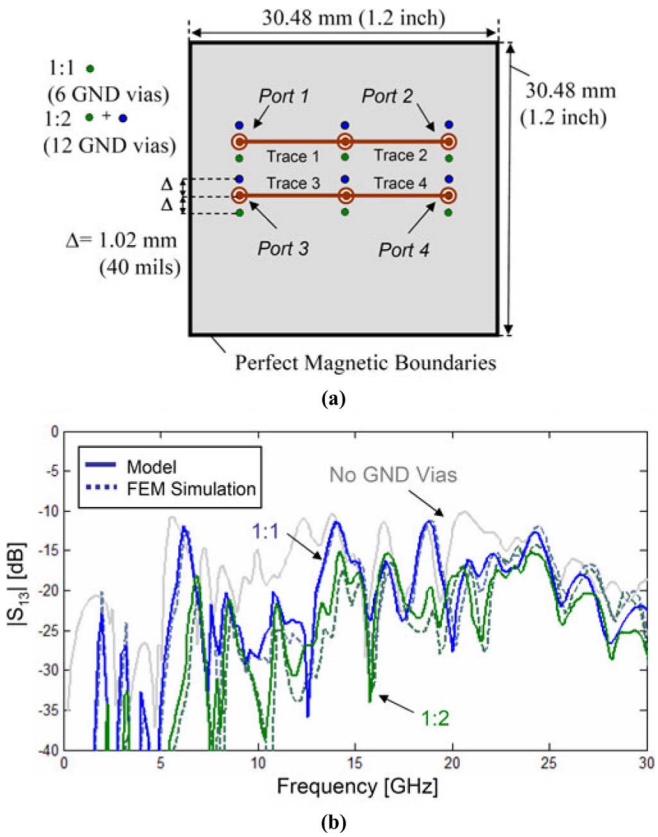

Fig. 7. Test case with ground vias. (a) Structure upper view. (b) Near-end crosstalk for different signal to ground via ratios, obtained by the models and FEM full-wave simulations. In this case, all the reference planes are defined as ground.

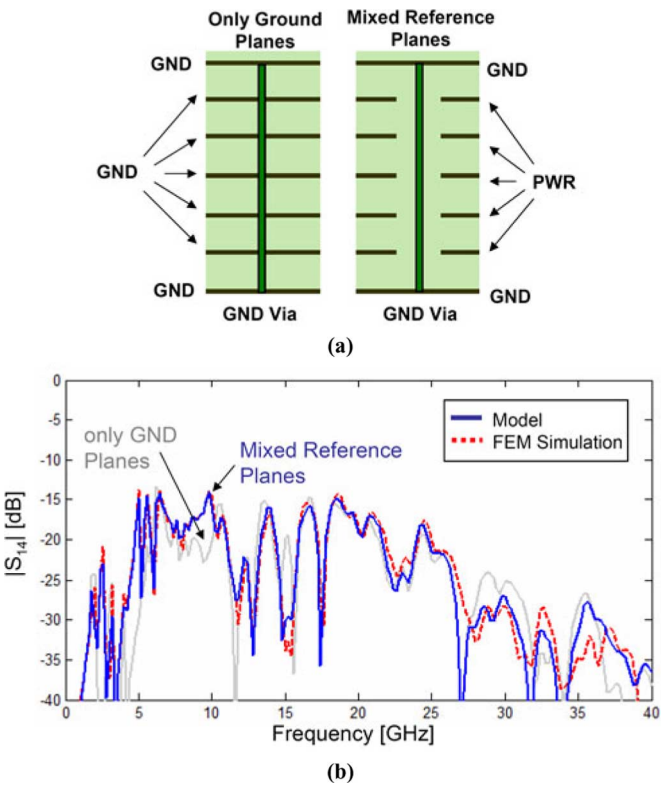

Fig. 8. Test cases with and without mixed reference planes. (a) Stackup cross-sectional views. (b) Far-end crosstalk for both cases and correlation to FEM full-wave simulation.

The impact of interleaved ground and power planes was investigated and compared with the case with all the reference planes assigned as ground. In the study case, the mixed reference planes considered all the inner planes as floating power planes and the top and bottom planes as ground [see Fig. 8(a)]. The models were able to capture with good accuracy the subtle differences in the response predicted by a full-wave simulation [see Fig. 8(b)].

Despite the number of floating planes, the difference in the results is small between the two cases. The return path provided by the ground vias is present even if the via does not touch some inner reference planes. The additional coupling paths between cavities provided by the clearance holes on planes (antipads) in the mixed reference case may explain the slight differences observed and the trend towards lower crosstalk for the case where all the planes are defined as ground. Alternative reference plane combinations were studied using the structure of Fig. 5. As expected, as more intermediate ground planes were added, the differences diminished in comparison to the case with all reference planes defined as ground.

C. Buried Vias

Another case of interest that can be addressed with the presented method is the modeling of non-thru-hole vias that only partially traverse the board cross section (e.g., back-drilled, blind, or buried vias). The validation carried out has shown that it is possible to simulate structures containing blind vias and/or buried vias crossing about one-half of the cavity with simple approximations for the fringing fields at the via transition. For these cases, the via model is applicable and it is only necessary to recalculate the via-to-plane capacitance for the last segment of the via. This idea is illustrated in Fig. 9(a), where the capacitance $C_{\rm bv}$ is the parameter to be extracted for a buried via. The test structure discussed here corresponds to the case in Fig. 5 replacing the thru-hole vias with buried vias. Fig. 9(b) shows that with this approximation, it is possible to achieve good results handling these special types of vias up to 20 GHz. A drawback of this approach is that the model will not be able to consider the attenuation on the parallel-plane modes due to the buried via transition, which starts to become important as the frequency increases. This may explain the discrepancy observed at frequencies beyond 20 GHz between the results predicted by the model and full-wave simulation.

D. Coupled Striplines

The modal decomposition approach gives the possibility to compute the transmission line model independently from the parallel-plate model. Assuming ideal conductor reference planes for the traces, it is possible to generate the models using conventional transmission line theory or any solver (3-D or 2-D) suitable for this purpose. For the validation of a case with coupled striplines, the reference example was modified by replacing the single-ended striplines with differential ones. The new structure [in Fig. 10(a)] has 12 vias and two differential

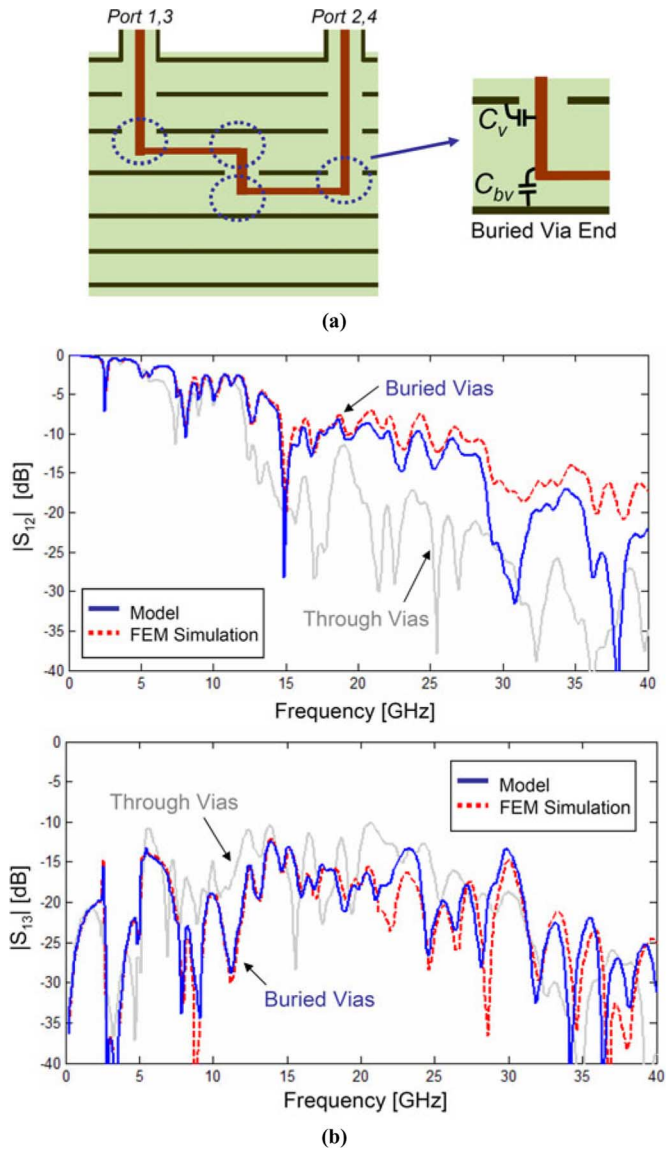

Fig. 9. Test structure replacing thru-hole signal vias of structure in Fig. 5 by buried vias. (a) Cross-section diagram and buried via end capacitance definition. (b) Transmission and near-end crosstalk obtained with the models and FEM full-wave simulations.

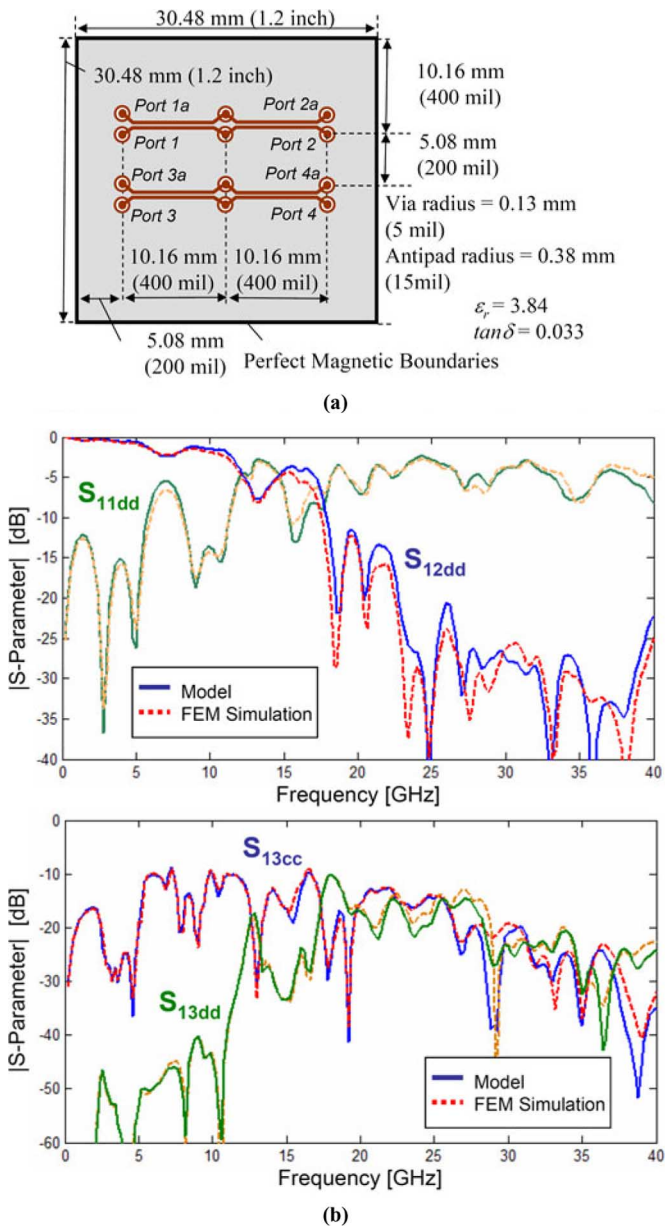

Fig. 10. Test structure with differential links (coupled conductors). (a) Structure upper view sketch. (b) Mixed-mode S-parameters for differential reflection and transmission, and differential and common-mode near-end crosstalk. Correlation to FEM simulations is shown.

links routed through the third and fourth cavities. The transmission line model was obtained for this case using a 3-D solver. Nonetheless, good results could be also achieved with a 2-D model derived from cross-sectional information. Fig. 10(b) details the results obtained in terms of mixed-mode S-parameters in comparison to a full-wave analysis. The agreement for both solutions is good and the improvement on the response is clear for the differential parameters in contrast to the common-mode ones. The differential crosstalk for frequencies below 15 GHz is substantially lower in comparison to the common-mode case.

IV. Correlation to Measurement

The model-to-hardware correlation was investigated with a complex link board having two via arrays designed for ball grid array (BGA) package/sockets and multiple links connected by differential striplines, as shown at the top of Fig. 11. The board profile has 12 cavities (although most vias are crossing only six of them), with 15-cm-long traces routed at the $S3$ layer. The measurements were carried out with microprobes placed on top of the board, which were previously calibrated on an impedance standard substrate.

In order to limit the complexity of the problem, the number of vias modeled was reduced to 74, considering only vias in the vicinity of the probed ports on both the east and west BGA via arrays. Two links running between the vias were simulated and all the vias not connected to one of the four traces were left open. It was assumed that the vias located further away and the board edges do not play a very important role determining the response of the measured links. The validity of these simplifications was tested first by computing the plane model by the cavity model assuming open boundaries at board edges. The results were then

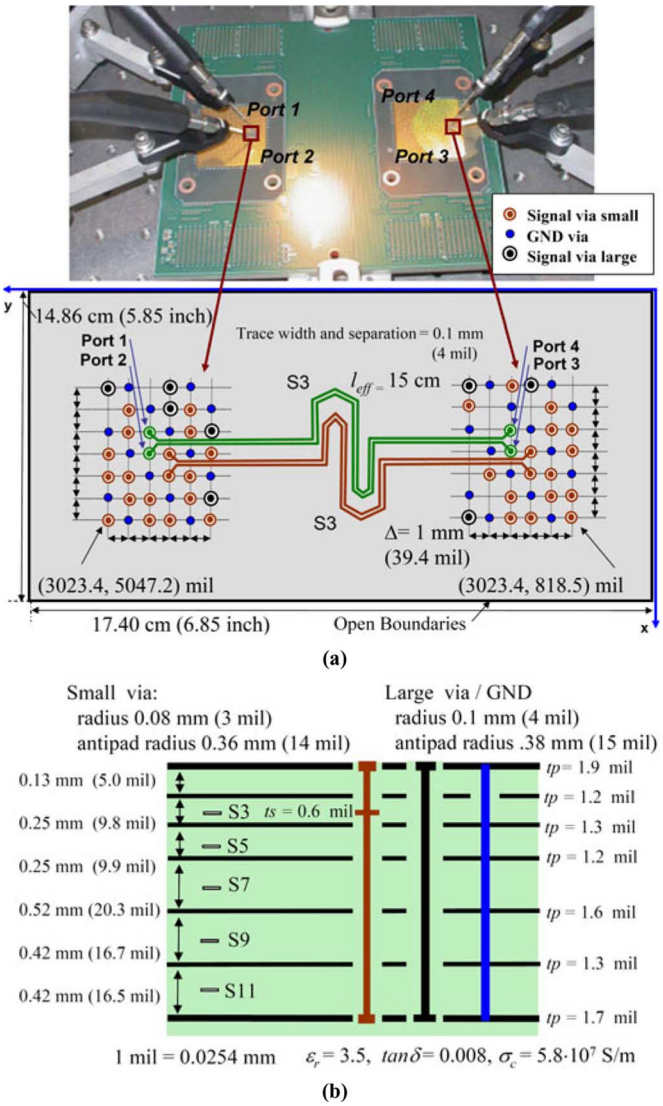

Fig. 11. Differential link board for model-to-hardware correlation. (a) Measured structure and modeled segment upper view sketch. (b) Board cross section for the first six cavities.

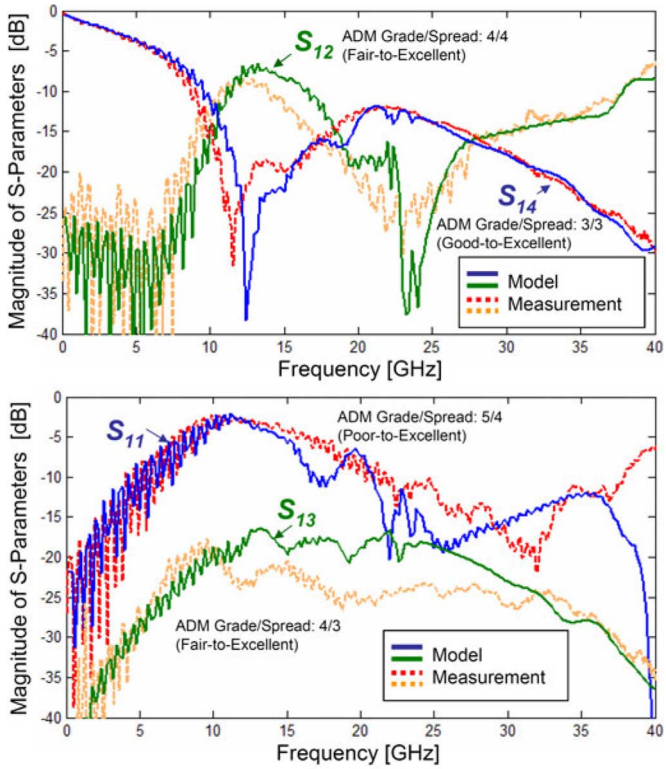

Fig. 12. Model-to-hardware correlation for a studied link. The plots show the magnitude of the single-ended S-parameters. Amplitude difference metrics (ADMs) of the FSV method were included.

computed assuming infinite planes according to the radial waveguide method, where the parallel-plate impedance can be calculated from [7], [23]

$$Z_{ij}{}^{PP}(\omega) = \frac{j\eta d}{2\pi\rho_0}\frac{H_0^{(2)}(k\rho_{ij})}{H_1^{(2)}(k\rho_0)} \tag{12}$$

with ρ_0 being the port radius, ρ_{ij} being the radial port separation, η being the complex wave impedance, and $H_0^{(2)}$, $H_1^{(2)}$ denoting the Hankel functions of second type and order 0 and 1, respectively. The good agreement between the cavity model and the infinite plane solutions leads to the conclusion that the effect of the boundaries can be neglected here without losing much accuracy. This observation is significant because it implies that for dense via arrays and test locations placed far away from board edges, the size and shape of the board are of minor importance. Moreover, the calculation of the parallel-plate impedance assuming infinite planes may noticeably improve the overall efficiency of the simulation since only one iteration of the algorithm is required per frequency point, in contrast to the cavity method, which requires many iterations to compute the response accurately.

The transmission line model was obtained from a 2-D solver using the cross-section information from the board stackup. The change in trace widths when entering into the via arrays, the trace coupling between different links and the effect of trace serpentine bends were neglected. A homogeneous relative permittivity and a constant loss tangent were assumed for the simulations with the proposed method. It should also be noted that conductor loss was considered, but the traces are not centered.

Despite the drastic model reductions and simplifications made for the sake of modeling efficiency, the comparison to measurements shows that the models were able to capture the salient features of the hardware response quite well (Fig. 12). Note that the resonance on the transmission parameters (e.g., S_{14}), present in both model and measurement, is a consequence of the via stubs [39].

In the following, possible causes for the model-to-measurement discrepancies are discussed.

1) The transmission line models were drastically simplified for the simulation. The board traces present multiple bends and are routed with many other lines. The change of trace width when the lines are entering into the via arrays and the coupling with other vias were also neglected. These simplifications can lead to errors calculating the crosstalk parameters and to underestimate the channel loss, in particular at high frequencies.
2) The real board contains many more elements that those being modeled. It was determined, for example, that

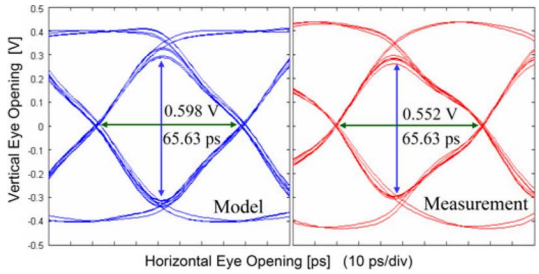

Fig. 13. Eye diagram for the transmission from ports 1 to 4, a data rate of 15 Gb/s and a rise/fall time (tr_{20-80}) of 10 ps, obtained with the proposed models and measurement.

the resonances present in the simulated results between 20–25 GHz are caused by the vias not connected to a trace. These resonances are damped when the model is extended to consider more adjacent (uncoupled) traces.

3) Although the microprobes used in the measurement were calibrated, they are likely to introduce additional parasitics that become more important at high frequencies. Moreover, the probes at the same link side must be placed in close proximity, which possibly results in probe-to-probe coupling. These two aspects were not modeled and may impact the correlation, in particular for reflections and near-end crosstalk parameters.
4) The models require many parameters that are difficult to calculate with good accuracy over a broad frequency range. The frequency dependency of the model coefficients was also neglected. Process variations and tolerances introduce more uncertainty for parameter estimation. These factors can impact negatively the computation of, for instance, material loss or via capacitances, which may lead to substantial discrepancies in the correlation.
5) The via arrays are quite dense and coupling through the near field of the vias might occur. This interaction cannot be mapped yet into the models. In addition, the validity of symmetric fields around vias may start to break down for the higher part of the frequency range.

In our opinion, the results are satisfactory considering the complexity of the real board structure and the model simplifications. With the simulation results, it is still possible to compute the time-domain response for data rates up to 15 Gb/s with good accuracy. The shape, vertical and horizontal opening of the eye diagram, agree well (within 10%) for the transmission parameter up to that speed (Fig. 13).

The computation on a dual core 3.0-GHz PC with 4-GB RAM consumed about 50 s calculating the six cavities independently with 200 frequency points, but not including the time required to obtain the 2-D transmission line model. The simulation of even this simple link is beyond the reach of full-wave simulators running on a single workstation. In contrast, the progress obtained thus far with the physics-based models has shown that it is feasible to apply it to realistic geometries without incurring onerous computational overhead. Moreover, preliminary comparisons done against commercial hybrid solvers have shown that the proposed method is faster by at least a factor of two.

V. Conclusion

The efficient simulation of end-to-end links on package and PCB structures using combined physics-based via and trace models has been discussed. Extensive validation of the models with respect to full-wave methods and hardware measurement has been carried out up to 40 GHz. It was demonstrated that the models and the proposed simulation method can be successfully applied to solve a wide variety of configurations with good accuracy, while maintaining very good numerical efficiency.

It is also important to recognize the intrinsic limitations of this approach and to look for opportunities for further refinement. The analytical formulations used to compute the parallel-plate impedance are valid only for propagating modes inside the cavity. As the via spacing shrinks, the interaction through the near field of the vias (i.e., evanescent modes), which cannot be mapped with these analytical solutions, will start to appear. If the near-field interaction in very dense arrays is not negligible, other solutions become necessary to compute the plane model (see, e.g., [4]).

Regarding the via-to-plane capacitance in the models, different formulas still need to be developed for some scenarios. The capacitive elements in the models correspond to approximations of the near fields, and it will be of limited accuracy with increasing frequency. In the analysis presented by Zhang *et al.* [30], it is shown that the via capacitance values are typically a weak function of the frequency below 40 GHz. This indicates that the models should be able to provide good accuracy at least within the discussed bandwidth.

The issues mentioned here are currently being investigated for further development of the models and successful application of the method for more complex and diverse scenarios.

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References

[1] D. G. Kam, M. B. Ritter, T. H. Beukema, J. F. Bulzacchelli, P. K. Pepeljugoski, Y. H. Kwark, L. Shan, X. Gu, C. W. Baks, R. A. John, G. Hougham, C. Schuster, R. Rimolo-Donadio, and B. Wu, "Is 25 Gb/s on-board signaling viable?," *IEEE Trans. Adv. Packag.*, vol. 32, no. 2, pp. 328–344, May 2009.

[2] V. Stojanovic and M. Horowitz, "Modeling and analysis of high-speed links," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2003, pp. 589–594.

[3] B. Archambeault and A. E. Ruehli, "Analysis of power/ground-plane EMI decoupling performance using the partial-element equivalent circuit technique," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 4, pp. 437–445, Nov. 2001.

[4] L. Tsang, H. Chen, C. C. Huang, and V. Jandhyala, "Modeling of multiple scattering among vias in planar waveguides using Foldy–Lax equations," *Microw. Opt. Technol. Lett.*, vol. 31, no. 4, pp. 375–384, Nov. 2004.

[5] A. E. Engin, K. Bharath, M. Swaminathan, M. Cases, B. Mutnury, N. Pham, D. N. de Araujo, and E. Matoglu, "Finite-difference modeling of noise coupling between power/ground planes in multilayered packages and boards," in *Proc. 56th Electron. Compon. Technol. Conf.*, Jun. 2006, pp. 1262–1267.

[6] N. Na, J. Jinseong, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and transient simulation of planes in electronic packages," *IEEE Trans. Adv. Packag.*, vol. 23, no. 3, pp. 340–352, Aug. 2000.

[7] R. Ito, R. W. Jackson, and T. Hongsmatip, "Modelling of interconnections and isolation within a multilayered ball grid array package," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 9, pp. 1819–1825, Sep. 1999.
[8] Z. Z. Oo, E. X. Liu, E. P. Li, X. Wei, Y. Zhang, M. Tan, L. W. J. Li, and R. Vahldieck, "A semi-analytical approach for system-level electrical modeling of electronic packages with large number of vias," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 267–274, May 2008.
[9] X. C. Wei, E. P. Li, E. X. Liu, and R. Vahldieck, "Efficient simulation of power distribution network by using integral-equation and modal-decoupling technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 10, pp. 2277–2285, Oct. 2008.
[10] J. Kim, Y. Jeong, J. Kim, J. Lee, C. Ryu, J. Shim, M. Shin, and J. Kim, "Modeling and measurement of interlevel electromagnetic coupling and fringing effect in a hierarchical power distribution network using segmentation method with resonant cavity model," *IEEE Trans. Adv. Packag.*, vol. 31, no. 3, pp. 544–557, Aug. 2008.
[11] C. Schuster, Y. H. Kwark, G. Selli, and P. Muthana, "Developing a physical model for vias," in *Proc. IEC Designcon Conf.*, Santa Clara, CA, Feb. 2006, pp. 1–24.
[12] G. Selli, C. Schuster, Y. Kwark, M. Ritter, and J. L. Drewniak, "Model-to-hardware correlation of physics based via models with the parallel plate impedance included," in *Proc. IEEE Electromagn. Compat. Symp.*, Portland, OR, Aug. 2006, pp. 781–785.
[13] C. Schuster, G. Selli, Y. H. Kwark, M. B. Ritter, and J. L. Drewniak, "Accuracy and application of physics-based circuit models for vias," in *Proc. IMAPS 39th Int. Microelectron. Symp.*, San Diego, CA, Oct. 2006, pp. 1–7.
[14] C. Schuster, G. Selli, Y. H. Kwark, M. B. Ritter, and J. L. Drewniak, "Progress in representation and validation of physics-based via models," in *Proc. 11th IEEE Signal Propag. on Interconnects Workshop*, Genova, Italy, May 2007, pp. 145–148.
[15] R. Rimolo-Donadio, A. J. Stepan, H.-D. Brüns, J. L. Drewniak, and C. Schuster, "Simulation of via interconnects using physics-based models and microwave network parameters," in *Proc. 12th IEEE Signal Propag. on Interconnects Workshop*, Avignon, France, May 2008, pp. 1–4.
[16] R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "Including stripline connections into network parameter based via models for fast simulation of interconnects," in *Proc. 20th Int. Electromagn. Compat. Symp.*, Zurich, Switzerland, Jan. 2009, pp. 345–348.
[17] A. E. Engin, W. John, G. Sommer, W. Mathis, and H. Reichl, "Modeling of striplines between a power and a ground plane," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 415–426, Aug. 2006.
[18] K. C. Gupta and M. D. Abouzahra, *Analysis and Design of Planar Microwave Components*. Piscataway, NJ: IEEE Press, 1994, pp. 75–86.
[19] Q. Gu, E. Yang, and M. A. Tassoudji, "Modeling and analysis of vias in multilayered integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 2, pp. 206–214, Feb. 1993.
[20] Q. Gu, A. Tassoudji, S. Y. Poh, R. T. Shin, and J. A. Kong, "Coupled noise analysis for adjacent vias in multilayered digital circuits," *IEEE Trans. Circuits Syst. I. Fundam. Theory Appl.*, vol. 41, no. 12, pp. 796–804, Dec. 1994.
[21] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*. Berlin, Germany: Springer-Verlag, 1985, ch. 2.
[22] G. T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, and B. K. Gilbert, "Wave model solution to the ground/power plane noise problem," *IEEE Trans. Instrum. Meas.*, vol. 44, no. 2, pp. 300–303, Apr. 1995.
[23] N. Marcuvitz, "Radial transmission lines," in *Principles of Microwave Circuits*, C. G. Montgomery, R. H. Dicke, and E. M. Purcell, Eds., rev ed. London, U.K.: IEE Press, 1987, vol. 25, ch. 8.
[24] J. C. Parker, Jr., "Via coupling within parallel rectangular planes," *IEEE Trans. Electromagn. Compat.*, vol. 39, no. 1, pp. 17–23, Feb. 1997.
[25] Z. L. Wang, O. Wada, Y. Toyota, and R. Koga, "Analysis of resonance characteristics of a power bus with rectangle and triangle elements in multilayer PCBs," in *Proc. Asia–Pacific Environ. Electromagn. Conf.*, Nov. 2003, pp. 73–76.
[26] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*. Berlin, Germany: Springer-Verlag, 1985, ch. 3.
[27] Z. L. Wang, O. Wada, Y. Toyota, and R. Koga, "Convergence acceleration and accuracy improvement in power bus impedance calculation with a fast algorithm using cavity modes," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 1, pp. 2–8, Feb. 2005.
[28] J. Trinkle and A. Cantoni, "Single summation expression for the rectangular power ground plane cavity," in *Proc. 16th Int. Electromagn. Compat. Symp.*, Zurich, Switzerland, Feb. 2005, pp. 247–250.
[29] M. Hampe, V. Palanisamy, and S. Dickmann, "Single summation expression for the impedance of rectangular PCB power-bus structures loaded with multiple lumped elements," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 1, pp. 58–67, Feb. 2007.
[30] Y. Zhang, J. Fan, G. Selli, M. Cocchini, and D. P. Francesco, "Analytical evaluation of via-plate capacitance for multilayer printed circuit boards and packages," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 9, pp. 2118–2128, Sep. 2008.
[31] C. R. Paul, *Analysis of Multiconductor Transmission Lines*. New York: Wiley, 1994, pp. 47–76, 187–245.
[32] B. C. Wadell, *Transmission Line Design Handbook*. Norwood, MA: Artech House, 1991.
[33] Microwave Studio. ver. 2008, CST Corporation, Darmstadt, Germany, Dec. 2008. [Online]. Available: http://www.cst.com
[34] HFSS. ver. 11, Ansoft Corporation, Pittsburgh, PA, Dec. 2008. [Online]. Available: http://www.ansoft.com
[35] A. P. Duffy, A. J. Martin, A. Orlandi, G. Antonini, T. M. Benson, and M. S. Woolfson, "Feature selective validation for validation of computational electromagnetics. Part I—The FSV method," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 3, pp. 449–459, Aug. 2006.
[36] *Standard for Validation of Computational Electromagnetics Computer Modeling and Simulation*, IEEE Standard P1597.1, 2008.
[37] "FSV routine," EMC Laboratory, Univ. L'Aquila, L'Aquila, Italy, Feb. 2, 2009. [Online]. Available: http://ing.univaq.it/uaqemc/FSV_4_0_3L
[38] S. Wu, X. Chang, C. Schuster, X. Gu, and J. Fan, "Eliminating via-plane coupling using ground vias for high-speed signal transitions," in *Proc. Elect. Perform. Electron. Packag.*, Oct. 2008, pp. 247–250.
[39] T. Kushta, K. Narita, T. Kaneko, T. Saeki, and H. Tohya, "Resonance stub effect in a transition from a through via hole to a stripline in multilayer PCBs," *IEEE Trans. Microw. Wireless Compon. Lett.*, vol. 13, no. 5, pp. 169–171, May 2003.

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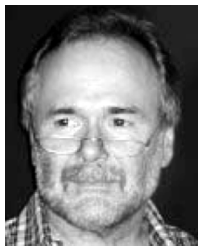

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