An Intrinsic Circuit Model for Multiple Vias in an Irregular Plate Pair Through Rigorous Electromagnetic Analysis

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***Abstract*—An irregular plate pair with multiple vias is analyzed by the segmentation method that divides the plate pair into a plate domain and via domains. In the via domains, all the parallel-plate modes are considered, while in the plate domain, only the propagating modes are included to account for the coupling among vias and the reflection from plate edges. Boundary conditions at both vias and plate edges are enforced and all parasitic components of via circuit are expressed analytically in terms of parallel-plate modes. The work presented in this paper indicates that a previous physics-based via circuit model from intuition is a low-frequency approximation. Analytical and numerical simulations, as well as measurements, have been used to validate the intrinsic via circuit model.**

***Index Terms*—Intrinsic via circuit model, parallel-plate modes, physics-based via circuit model, segmentation technique, signal and power integrity.**

I. Introduction

VIAS ARE widely used in multilayer high-speed printed circuit boards (PCBs) or packages to connect signal traces on different layers or connect devices to power and ground planes [1]–[4]. As discontinuities, vias may cause mismatch, crosstalk, mode conversion, and other signal integrity issues in a signal link path. Moreover, vias passing through a parallel power/ground plate pair could effectively pick up the power distribution network noise, resulting in degraded signal quality. Similarly, high-speed transient currents flowing along vertical vias could also excite the parallel plates they penetrate, causing serious voltage fluctuations in power distribution network or electromagnetic interference problems due to strong edge radiation. Therefore, modeling the electromagnetic behavior of vias in parallel plates plays a critical role in analyses of signal integrity, power integrity, and electromagnetic interference for multilayer PCBs and packages.

Via-plate interactions have been extensively studied. For vias crossing a single plate, either full-wave methods or quasi-static approaches are effective due to the localized field distribution near the vias [5]–[12]. For vias crossing a plate pair, however, quasi-static approximation and simple lumped circuit modeling are not suitable any more as the electromagnetic fields are not localized near vias. Although the higher order evanescent parallel-plate modes are localized in proximity to the vias as energy stored in the electric and magnetic fields, the propagating modes spread over the entire plate pair. This makes it more difficult to model a via crossing a plate pair than a via crossing a single plate.

An analytical method for the via–plate–pair interaction was first reported in [13] for a single via, and later extended to the coupling of two vias [14]. A magnetic frill current was assumed in a via-hole in a plate (the gap region between a via and a plate), and cylindrical waves were used to describe the parallel-plate modes. Boundary conditions at the vias were explicitly enforced. However, the analytical method cannot handle a plate pair with more than two vias. Moreover, the method is restricted to an infinitely large plate pair, and no edge reflection was considered.

Recently, an algorithm denoted by the Foldy–Lax multiple scattering method, was proposed to extend the analytical method to multiple vias in a plate pair [15]–[19]. The dyadic Green's function of an infinitely large plate pair or a finite circular plate pair, as well as the addition theorem of cylindrical harmonics, was used to analyze the multiple scattering among vias. All the via-holes in plates were regarded as ports of a multiport microwave network whose admittance matrix was obtained from current distributions in the ports. The multiple scattering method can be regarded as an efficient semianalytical method. However, the method is still restricted to either an infinite or a finite circular plate pair since an analytical dyadic Green's function is not available for an irregular finite plate pair.

Different from the rigorous multiple scattering method, an alternative solution denoted a physics-based via circuit model was proposed in [20]–[24]. In this model, the via–plate–pair interaction was represented simply by a π-type circuit. Each via barrel was viewed as a simple short circuit and the displacement currents between the via and the top/bottom plates were represented by two shunt capacitors. The impedance of the plate pair, widely studied in [25]–[32], was used as the return path for the signal current along the via barrel. The combination of the lumped via circuits and the full-wave plate pair impedance correctly reflects the fact that vias are usually electrically small, while the plate pair is comparable to the wavelength of interest. Moreover, the

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model is suitable for any irregular plate pair since its impedance matrix can be easily obtained from the cavity model and the segmentation technique [28], [30].

Despite its flexibility in handling edge boundaries, the physics-based via circuit model is based on physical intuition. The boundary conditions at the vias are not satisfied by the lumped via circuit. In addition, the coupling among vias is described by the parallel-plate impedance matrix (the TM_{z0} modes) only. Therefore, when vias are closely spaced and the coupling due to the higher order modes cannot be neglected, the accuracy of the physics-based via circuit model will start to deteriorate.

The purpose of this paper is to establish a theoretical foundation for the physics-based via circuit model for multiple vias in an irregular plate pair. An intrinsic via circuit model is derived from a rigorous electromagnetic analysis where boundary conditions at both the vias and the plate edges are explicitly enforced. The term "physics-based via circuit model" is used herein to refer to the model proposed in [20]–[24] based on physical intuition, while the term "intrinsic via circuit model" refers to the model presented in this paper based on rigorous electromagnetic analysis. Later, the physics-based via circuit model will be demonstrated to be an approximation of the intrinsic via circuit model at low frequencies.

Virtual circular boundaries can be introduced to divide the entire plate pair into via domains and a plate domain, as shown in Fig. 1, where a via domain associated with Via i is enlarged for illustration. The virtual circular boundaries are located where the higher order parallel-plate modes excited by scattering at each via are confined within the corresponding via domain, and, are negligibly small in the plate domain. The segmentation technique is then used to enforce the continuity of fields along these virtual circular boundaries. This paper focuses on the via domain modeling, and simply uses an impedance matrix to represent the plate domain behaviors. The details of the plate domain modeling will be addressed in a future publication.

To construct an intrinsic via circuit model in a via domain, the electric and magnetic components excited by a magnetic frill current in the via domain are obtained first using the same method discussed in [24]. The via domain is then regarded as a two-port network whose admittance matrix is expressed analytically in terms of the parallel-plate modes. An intrinsic via circuit model is obtained through a π-type equivalent-circuit representation of the two-port network. The equivalent circuit associated with both the evanescent and propagating modes are derived separately.

There are two main contributions of this paper, which are: 1) it establishes a rigorous theoretical foundation for the equivalent-circuit modeling of the via-plate-pair interaction and 2) it provides an empirical expression to determine the virtual circular boundary, within which the higher order modes are well confined. Further, the virtual circular boundary can be used to quantify the limitation of the equivalent-circuit modeling in practical engineering designs. When the spacing between vias is larger than two times the radius of the virtual circular boundary, which is usually the case in most practical PCB and package designs, the coupling between the vias is dominated by the zeroth-order waves. Thus, the equivalent-circuit modeling approach presented in this paper can accurately describe the via–plate–pair interaction, which, compared with other modeling approaches, is often preferred for its fast simulation speed, easy interface with other circuit elements, as well as clear physical meaning for analysis and design.

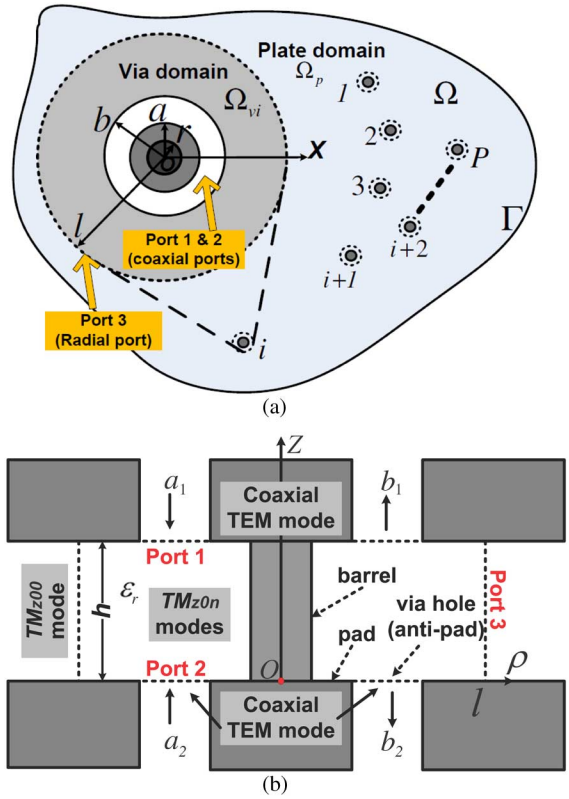

Fig. 1. Domain segmentation of an irregular plate pair with multiple vias. (a) Top view. (b) Side view.

II. Segmentation of Vias and a Plate Pair

The top view of an irregular plate pair loaded with P vias is shown in Fig. 1(a). Bounded by the edge Γ, the region of the entire via-plate structure is denoted Ω that is decomposed into $P+1$ separate regions: P via domains Ω_{vi}, $i=1,2,3,\ldots,P$ and one plate domain Ω_p, i.e., $\Omega=\Omega_p+\sum_{i=1}^{P}\Omega_{vi}$.

As an example, the via-domain for Via i, Ω_{vi}, is enlarged in Fig. 1(a) and (b), showing the top and side views. The barrel, pad, and via-hole radii of the via are denoted r, a, and b, respectively. The via height or the separation of the plates is h, and a dielectric layer is between the plates with a relative permittivity of ε_r. A local cylindrical coordinate system is set up with the origin at the center of the bottom plate surface in Ω_{vi}, as shown in Fig. 1. The virtual via boundary between the via domain and the plate domain is located at $\rho=l$.

The vertical (z-directional) electric field near the ith via can be expressed as

$$E_z=\sum_{m=-\infty}^{\infty}\sum_{n=0}^{\infty}\left[a_{mn}J_{mn}(\rho,\phi,z)+b_{mn}H_{mn}(\rho,\phi,z)\right] \quad (1)$$

where a_{mn} and b_{mn} are the expansion coefficients for the inward and outward TM_{zmn} parallel-plate modes $J_{mn}(\rho,\phi,z)$ and $H_{mn}(\rho,\phi,z)$, respectively, which are expressed as

$$J_{mn}(\rho,\phi,z) = J_m(k_n\rho)e^{jm\phi}\cos\left(\frac{n\pi}{h}z\right) \tag{2}$$

$$H_{mn}(\rho,\phi,z) = H_m^{(2)}(k_n\rho)e^{jm\phi}\cos\left(\frac{n\pi}{h}z\right) \tag{3}$$

where $J_m, H_m^{(2)}$ are the mth-order Bessel and Hankel (the second kind) functions, respectively, (ρ,ϕ,z) is the cylindrical coordinates of the via, and $k_n = \sqrt{k_0^2\varepsilon_r - (n\pi/h)^2}$ is the radial wavenumber. Only the TM_{zmn} parallel-plate modes are considered in this paper. The TE_{zmn} modes are negligible due to the specific excitations typical in a via geometry (a circular magnetic current in a via-hole, or a vertical electric current along a via barrel).

In most practical designs, the following assumptions are satisfied.

- Only the TEM mode is considered in the via-holes. In other words, magnetic frill currents are assumed to excite the parallel-plate pair, which have been widely used in [13]–[19], [24], [33], and [34]. This implies that sources in the via-holes only excite the $\mathrm{TM}_{z0n}, n \geq 0$ modes in the region between the two parallel plates, assuming vias and their corresponding via-holes are concentric.
- The height h is electrically small so that only the TM_{zm0} cylindrical waves can propagate. All the higher order modes $(\mathrm{TM}_{zmn}, n > 0)$ decay rapidly along the radial direction. Therefore, there is a virtual via boundary $\rho = l$ (in local coordinates) for each via beyond which all the higher order modes can be neglected. In other words, only the $\mathrm{TM}_{zm0}, m \in [-\infty, \infty]$ modes are considered in the plate domain outside the via domains.
- The virtual via boundary for each via is electrically small so that the azimuthal variation of fields due to the asymmetry of the via-plate structure is negligible. This means only the $\mathrm{TM}_{z0n}, n \geq 0$ modes need to be considered for the via domain modeling.

These assumptions indicate that each via domain is an electrically small region bounded by a virtual circular boundary. Thus, voltages and currents are well defined and circuit ports can be specified. As shown in Fig. 1, Ports 1 and 2 are defined as coaxial ports on the inner surface of the plates, between the vias and the plates, and across the via-holes. Port 3 is defined as a radial port at the virtual circular boundary between the two parallel plates. Furthermore, these assumptions determine that only the TM_{z00} waves need to be considered in the plate domain. Therefore, properly setting the virtual circular boundaries between the via domains and the plate domain is critical for the validity of the via circuit model derived later on.

In this paper, it is also assumed that the virtual circular boundaries do not overlap, as shown in Fig. 1. This guarantees that the higher order modes of one via do not illuminate another via. This assumption limits the approach presented herein to the cases where vias are not placed very closely to each other. Section IV will provide an empirical formula to determine the virtual via boundary, or in other words, the minimum spacing between two adjacent vias for the validity of the approach.

At Port 3 of Via i, the port voltage and current can be defined in terms of the TM_{z00} waves as

$$V_i = -E_{zi}h \tag{4}$$

$$I_i = 2\pi l H_{\phi i}. \tag{5}$$

The plate domain in Fig. 1(a) can then be modeled as a P-port network to describe the coupling among the P vias using the TM_{z00} modes. The impedance matrix of this P-port network is different to the conventional impedance matrix of a rectangular plate pair widely studied in [25]–[32]. The new impedance definition and calculations will be introduced in a future publication.

The via, inside its via domain, can be viewed as a three-port network, as shown in Fig. 1. Ports 1 and 2 can connect other layers in a multilayer PCB or package, and Port 3 connects to the network that describes the plate domain to ensure the continuity of the tangential fields at the virtual via boundary at $\rho = l$. This segmentation approach enforces the boundary conditions at both the via barrels and the plate edges, as explained later in detail.

III. Intrinsic Three-Port via Circuit Model

A via domain can be viewed as a via located at the center of a circular plate pair with a dimension of $\rho = l$. The field distributions excited by a magnetic frill current can then be derived using the same method as in [24].

A. Field Distributions Excited by a Magnetic Frill Current

Using the equivalence principle of electromagnetics, the TEM mode at Port 1 or Port 2 of a via, shown in Fig. 1(b) as an example, can be regarded as an equivalent magnetic frill current

$$M_\phi = -\frac{V_0}{\rho' \ln(b/a)}\delta(z - z') \tag{6}$$

where V_0 is the voltage across the via-hole at $z' = 0$ or $z' = h$.

The magnetic field distribution due to (6) has been derived as [24]

$$H_\phi(\rho,z) = -\frac{\omega\varepsilon\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty} G_n^S(\rho)\cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{7}$$

for $l \geq \rho \geq b$, and

$$H_\phi(\rho,z) = -\frac{\omega\varepsilon\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty} F_n^S(\rho)\cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{8}$$

for $r \leq \rho \leq a$, and the two auxiliary functions are defined as

$$\begin{aligned} G_n^S(\rho) = {} & \frac{\left(1 - \Gamma_r^{(n)}\Gamma_l^{(n)}\right)^{-1}}{k_n(1+\delta_{n0})} \\ & \cdot \Big\{ [J_0(k_n b) - J_0(k_n a)] \\ & \quad + \Gamma_r^{(n)}\left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a)\right]\Big\} \\ & \cdot \left[H_1^{(2)}(k_n\rho) + \Gamma_l^{(n)} J_1(k_n\rho)\right] \end{aligned} \tag{9}$$

$$F_n^S(\rho) = \frac{\left(1-\Gamma_r^{(n)}\Gamma_l^{(n)}\right)^{-1}}{k_n(1+\delta_{n0})} \cdot \left\{\left[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a)\right] + \Gamma_l^{(n)}\left[J_0(k_n b) - J_0(k_n a)\right]\right\} \cdot \left[J_1(k_n\rho) + \Gamma_r^{(n)} H_1^{(2)}(k_n\rho)\right] \tag{10}$$

where $\Gamma_r^{(n)}$ and $\Gamma_l^{(n)}$ are the reflection coefficients for the nth cylindrical waves from the via barrel ($\rho = r$) and the outer radial boundary ($\rho = l$), respectively, and given as

$$\Gamma_r^{(n)} = -\frac{J_0(k_n r)}{H_0^{(2)}(k_n r)} \tag{11}$$

$$\Gamma_l^{(n)} = \begin{cases} \Gamma_l\delta_{n0}, & \text{Irregular}, \quad S = I \\ -\frac{H_0^{(2)}(k_n l)}{J_0(k_n l)}, & \text{PEC}, \quad S = E \\ -\frac{H_1^{(2)}(k_n l)}{J_1(k_n l)} & \text{PMC}, \quad S = M \\ 0 & \text{PML}, \quad S = L \end{cases} \tag{12}$$

where $J_{0(1)}(\cdot), H_{0(1)}^{(2)}(\cdot)$ denote the zeroth (first)-order Bessel and Hankel function of the second kind, respectively, and k_n is the radial wavenumber for the TM_{z0n} modes as

$$k_n = \sqrt{k_0^2\varepsilon_r - \left(\frac{n\pi}{h}\right)^2}. \tag{13}$$

As shown in (12), the values of $\Gamma_l^{(n)}$ has four choices depending on the boundary conditions at $\rho = l$. The superscript S in the auxiliary functions G_n^S and F_n^S indicates one of the choices. PEC, PMC, and PML denote the perfect electric conductor, perfect magnetic conductor, and perfectly matched layer conditions, respectively.

According to the discussion in Section II, $S = I$ represents the case where all the higher order ($\mathrm{TM}_{z0n}, n > 0$) modes are well confined in the via domain. Therefore, in this case, only the reflection coefficient of the TM_{z00} waves, Γ_l, is nonzero. The other boundary conditions are introduced here for the determination of the virtual via boundary $\rho = l$ in the following sections.

The electrical-field components can be obtained from (7) and (8) from the magnetic field as

$$E_z(\rho,z) = \frac{j\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\partial\left[\rho G_n^S(\rho)\right]}{\rho\partial\rho} \cdot \cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{14}$$

$$E_\rho(\rho,z) = \frac{-j\pi V_0}{h\ln(b/a)}\sum_{n=1}^{\infty}\frac{n\pi}{h}G_n^S(\rho) \cdot \sin\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{15}$$

for $l \geq \rho \geq b$ and

$$E_z(\rho,z) = \frac{j\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty}\frac{\partial\left[\rho F_n^S(\rho)\right]}{\rho\partial\rho} \cdot \cos\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{16}$$

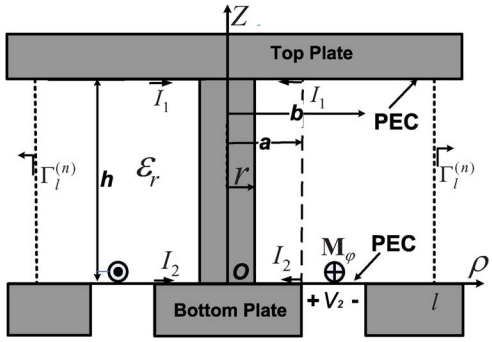

Fig. 2. Illustration of a via domain used for extracting an equivalent two-port network.

$$E_\rho(\rho,z) = \frac{-j\pi V_0}{h\ln(b/a)}\sum_{n=1}^{\infty}\frac{n\pi}{h}F_n^S(\rho) \cdot \sin\left(\frac{n\pi}{h}z\right)\cos\left(\frac{n\pi}{h}z'\right) \tag{17}$$

for $r \leq \rho \leq a$. The following identity can be used to obtain the explicit expression of E_z

$$\frac{d\left[\rho B_1(\rho)\right]}{\rho d\rho} = B_0(\rho) \tag{18}$$

where $B_{1(0)}$ is the first-order (zeroth-order) Bessel or Hankel functions.

B. Admittance Matrix of a Two-Port Network

A via domain, shown in Fig. 1(b) as an example, can be regarded as a two-port microwave network with the radial port (Port 3) terminated with the impedance of the plate domain, which is related to the reflection coefficient Γ_l as [27]

$$Z_l^+ = \frac{j\omega\mu h}{2\pi kl}\frac{H_0^{(2)}(kl) + \Gamma_l J_0(kl)}{H_1^{(2)}(kl) + \Gamma_l J_1(kl)}. \tag{19}$$

Therefore, an admittance matrix of the two-port network can be defined as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{20}$$

where (V_1, I_1) and (V_2, I_2) are the voltage and current pair of Ports 1 and 2, respectively. In practice, the dielectric material between the plate pair is normally reciprocal. As a result, the two-port via network satisfies reciprocity, i.e., $Y_{12} = Y_{21}$. Let $V_1 = 0$ and $V_2 = V_0$. Y_{12} and Y_{22} can then be calculated through the port currents, as shown in Fig. 2, with the top hole of the via closed by a perfect electric conductor (PEC) boundary and an equivalent magnetic frill current located at the bottom via-hole.

The magnetic field for $r \leq \rho \leq a$ in (8) leads to a description of the current distribution on the via barrel and pad as [15]

$$I(\rho,z) = 2\pi\rho H_\phi(\rho,z). \tag{21}$$

Substituting (8) into (21) using $V_0 = V_2$ and $z' = 0$ yields

$$I(\rho,z) = -\frac{\omega\varepsilon\pi V_2}{h\ln(b/a)}\sum_{n=0}^{\infty}2\pi\rho F_n^S(\rho)\cos\left(\frac{n\pi}{h}z\right). \tag{22}$$

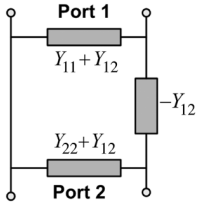

Fig. 3. π-type equivalent circuit for a reciprocal two-port network from its admittance matrix. The circuit is rotated by 90°, to be consistent to the ports illustrated in Fig. 1.

As shown in Fig. 2, the port currents can be obtained by letting $I_2 = I(a,0)$ and $I_1 = -I(a,h)$. The self-admittance Y_{22} and mutual admittance Y_{12} can then be obtained from (22) as

$$Y_{22} = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty} F_n^S(a) \tag{23}$$

$$Y_{12} = \frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty}(-1)^n F_n^S(a). \tag{24}$$

A reciprocal two-port network can be represented by a π-type equivalent circuit, as shown in Fig. 3 [35]. Using (23) and (24), the following shunt and series elements for the π-type equivalent circuit model can then be expressed as

$$Y_{12}+Y_{22} = -\frac{4\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=1,3,5,\ldots}^{\infty} F_n^S(a) \tag{25}$$

$$-Y_{12} = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty}(-1)^n F_n^S(a). \tag{26}$$

C. Via Circuit Components Due to Higher Order Modes

1) Shunt Capacitances: The shunt admittance $Y_{12}+Y_{22}$ has a clear physical meaning that it represents the capacitive coupling between the via (the barrel and pad) and the bottom plate. Thus, a shunt capacitance can be defined as

$$Y_{12}+Y_{22} = j\omega C_h. \tag{27}$$

Therefore, substituting (25) into (27) yields

$$C_h = \frac{j4\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=1,3,5,\ldots}^{2N-1} F_n^S(a) \tag{28}$$

where N is the mode number used to truncate the infinite summation in practical calculations.

The shunt capacitance C_h can be divided into two parts

$$C_h = C_b + C_p \tag{29}$$

where the barrel-plate capacitance C_b and the pad-plate capacitance C_p are expressed, respectively, as

$$C_b = \frac{j4\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=1,3,5,\ldots}^{2N-1} F_n^S(r) \tag{30}$$

$$C_p = \frac{j4\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=1,3,5,\ldots}^{2N-1}\left[F_n^S(a) - F_n^S(r)\right]. \tag{31}$$

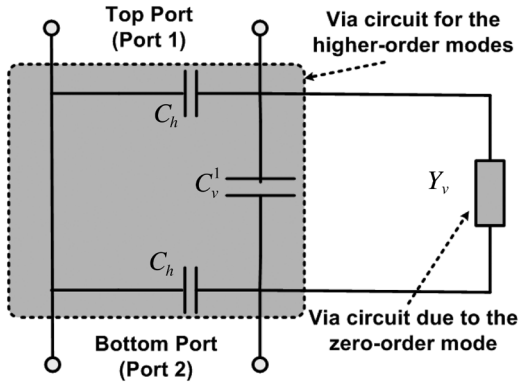

Fig. 4. Via circuit model due to the higher order modes with two shunt and one series parasitic capacitances.

In the case of a via without a pad, i.e., the pad radius is equal to the barrel radius ($a = r$), the pad-plate capacitance C_p vanishes, and the barrel-plate capacitance C_b in (30) is reduced to the analytical expression of the barrel-plate capacitance given in [24].

Similarly, the shunt capacitance from $Y_{11}+Y_{12}$ represents the capacitive coupling between the via and top plate. Its value is the same as C_h if the pad and via-hole dimensions are the same in both the top and bottom plates.

2) Series Capacitance: The series admittance in (26), $-Y_{12}$, is expressed in terms of both the zeroth-order propagating mode (TM_{z00}) and the higher order evanescent modes ($\mathrm{TM}_{z0n}, n \geq 1$). It can be separated into two parts

$$-Y_{12} = Y_v + j\omega C_v^1 \tag{32}$$

where the admittance Y_v represents the part due to the zeroth-order mode

$$Y_v = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}F_0^S(a) \tag{33}$$

and the series capacitance C_v^1 due to the higher order modes is expressed as

$$C_v^1 = \frac{j2\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=1}^{2N-1}(-1)^n F_n^S(a). \tag{34}$$

Note that the series capacitance C_v^1 is not included in the previous physics-based via circuit model in [20]–[22], [24], as it cannot be attributed to a static capacitance between two separate conductors. While the fields E_ρ in (15) and (17) lead to the capacitive element C_h, the higher order parts of the fields E_z in (14) and (16) are responsible for the parasitic capacitance C_v^1.

Equations (27) and (32) convert the general π-circuit shown in Fig. 3 into the via circuit model shown in Fig. 4. The parasitic capacitances C_h and C_v^1 characterize the energy stored in the electric field near the via due to the higher order parallel-plate modes.

D. Via Circuit Components Due to Zeroth-Order Waves

In the two-port via circuit model shown in Fig. 4, both C_h and C_v^1 are related to the higher order $n > 0$ modes, which are well confined in the via domain according to the assumptions in

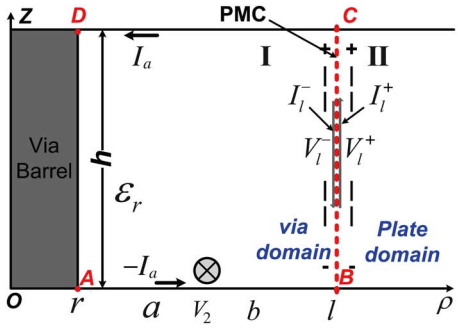

Fig. 5. Alternative derivation of Y_v by the segmentation technique.

Section II. Only the series admittance Y_v in (33), the component due to the zeroth-order waves, is then related to both the via and plate domains. An alternative derivation of Y_v is provided herein based on the segmentation of the via domain and the plate domain, as shown in Fig. 5. The derivation will show clearly how Y_v can be decomposed into an intrinsic part due to the via domain and an impedance due to the plate domain.

As discussed in Section II, the via domain I and the plate domain II are separated at $\rho = l$, as illustrated in Fig. 5. The boundary condition on the interface requires

$$I_l^- = -I_l^+ \tag{35}$$
$$V_l^- = V_l^+ \tag{36}$$

where $I_l^{\mp} = 2\pi l H_\phi(l^{\mp}, z)$ and $V_l^{\mp} = -E_z(l^{\mp}, z)h$ denote the left- and right-side port currents and voltages at the segmentation interface. These voltages and currents can be well defined similarly as in (4) and (5) because of the assumption that only the zeroth-order waves can reach the boundary between the via and plate domains.

According to the equivalence principle, a perfect magnetic conductor (PMC) boundary can be assumed for the interface at $\rho = l$ if the equivalent currents I_l^- and I_l^+ are impressed along both sides. In region I, the voltage V_l^- can then be obtained as

$$V_l^- = R_m V_2 + Z_l^- I_l^- \tag{37}$$

where

$$Z_l^- = -\frac{j\omega\mu h}{2\pi kl}\frac{J_0(kl) + \Gamma_r^{(0)} H_0^{(2)}(kl)}{J_1(kl) + \Gamma_r^{(0)} H_1^{(2)}(kl)} \tag{38}$$

and the voltage transform coefficient R_m relating V_2 to a part of V_l^-, which only results from the zeroth-order waves, is

$$R_m = \frac{j\pi}{\ln(b/a)}\left.\frac{\partial\left[\rho G_0^M(\rho)\right]}{\rho\partial\rho}\right|_{\rho=l}. \tag{39}$$

Equation (39) is obtained from the zeroth-order component of (14) at $\rho = l$ with a PMC boundary condition.

In region II, when there is only one via in the plate pair, the voltage V_l^+ is related to I_l^+ as

$$V_l^+ = Z_l^+ I_l^+ \tag{40}$$

where Z_l^+ is the impedance looking at Port 3 outward into the plate domain by definition, and has the same form as (19) for a circular plate pair. For an irregular plate pair, (40) is still valid and a generalized (19) will be derived in a future publication.

Substituting (40) and (37) into (36), as well as using (35), yields

$$I_l^- = -\frac{R_m V_2}{Z_l^+ + Z_l^-}. \tag{41}$$

The zeroth-order current component I_a flowing into the rim of the via pad at $\rho = a$ and $z = h$ is a combination of the effects of both V_2 and I_l^-. It can be obtained as

$$I_a = Y_a V_2 + R_e I_l^-. \tag{42}$$

The first term of the right-hand side of (42) is derived from the zeroth-order current component of (33) caused by V_2 with a PMC boundary at $\rho = l$, and

$$Y_a = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)} F_0^M(a). \tag{43}$$

The transform coefficient R_e reflects the magnetic field at $\rho = a$ excited by the current I_l^- at $\rho = l$ as

$$R_e = \frac{a\left[J_1(ka) + \Gamma_r^{(0)} H_1^{(2)}(ka)\right]}{l\left[J_1(kl) + \Gamma_r^{(0)} H_1^{(2)}(kl)\right]}. \tag{44}$$

Substituting (41) into (42), the series admittance Y_v is then derived as

$$Y_v = Y_a + \frac{-R_e R_m}{Z_l^+ + Z_l^-}. \tag{45}$$

When all the via geometrical dimensions are electrically small, the admittance Y_a behaves like a capacitance, i.e., $Y_a = j\omega C_v^0$, and the impedance Z_l^- acts as an inductance, i.e., $Z_l^- = j\omega L_v$. From (43) and (38), it can be derived that

$$C_v^0 = \frac{j2\varepsilon\pi^2 a}{h\ln(b/a)} F_0^M(a) \tag{46}$$

and

$$L_v = -\frac{\mu h}{2\pi kl}\frac{J_0(kl) + \Gamma_r^{(0)} H_0^{(2)}(kl)}{J_1(kl) + \Gamma_r^{(0)} H_1^{(2)}(kl)}. \tag{47}$$

The series admittance Y_v in (45) can then be rewritten as

$$Y_v = j\omega C_v^0 + \frac{R_v^2}{j\omega L_v + Z_l^+} \tag{48}$$

where the ideal transformation ratio R_v is defined as

$$R_v = \sqrt{-R_e R_m}. \tag{49}$$

Formula (48) implies an equivalent circuit shown in Fig. 6. A similar equivalent π-network has been proposed for the radial-line/coaxial-line junction in [36] and [37] with no circuit extraction.

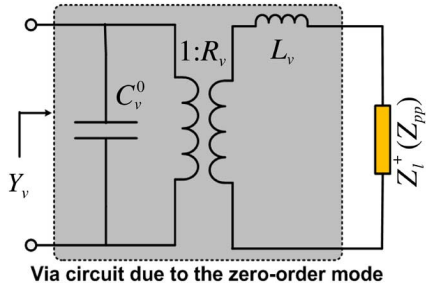

Fig. 6. Via circuit elements due to the zeroth-order mode.

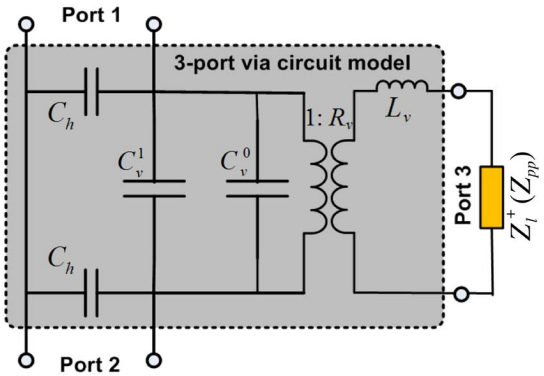

Fig. 7. Complete three-port via circuit model.

E. Complete Intrinsic Three-Port via Circuit Model

By combining the via circuits due to the higher order modes in Fig. 4 and the zeroth-order waves in Fig. 6, a complete three-port via circuit model and its connection to the impedance matrix of the plate domain Z_{pp} can be obtained, as shown in Fig. 7.

To demonstrate that all the parasitics C_h, C_v^1, C_v^0, L_v, and R_v are intrinsic to a via domain, and also to facilitate the usage of the derived intrinsic via circuit model, their expressions are given here again explicitly as

$$C_h = \left[\frac{j2\pi a}{h}\sum_{n=1,3,5,\ldots}^{2N-1} F_n^S(a)\right] C_a \tag{50}$$

$$C_v^1 = \left[\frac{j\pi a}{h}\sum_{n=1}^{2N-1}(-1)^n F_n^S(a)\right] C_a \tag{51}$$

where $C_a = 2\varepsilon_r\varepsilon_0\pi/\ln(b/a)$ is the per-unit-length capacitance of a coaxial geometry with inner and outer radii of a and b, respectively. The auxiliary function $F_n^S(a)$ can be expressed in a concise form as

$$F_n^S(a) = \frac{W_{10}(k_n a, k_n r)\,[W_{s0}(k_n l, k_n b) - W_{s0}(k_n l, k_n a)]}{k_n(1+\delta_{n0})W_{s0}(k_n l, k_n r)} \tag{52}$$

where $s = 1$ for $F_n^M(a)$, $s = 0$ for $F_n^E(a)$,

$$F_n^L(a) = \frac{H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a)}{k_n(1+\delta_{n0})H_0^{(2)}(k_n r)} W_{10}(k_n a, k_n r) \tag{53}$$

and $W_{mn}(x,y)$ is an auxiliary function defined as a determinant of the Bessel and Hankel functions as

$$W_{mn}(x,y) = \begin{vmatrix} J_m(x) & J_n(y) \\ H_m^{(2)}(x) & H_n^{(2)}(y) \end{vmatrix}. \tag{54}$$

$J_m(x)$ and $H_n^{(2)}(y)$ are the mth Bessel and nth second-order Hankel functions, respectively.

Similarly, the parameters due to the zeroth-order waves can be expressed in their concise forms as

$$L_v = -\frac{\mu h}{2\pi k b}\frac{W_{00}(kl,kr)}{W_{10}(kl,kr)} \tag{55}$$

$$C_v^0 = \frac{j\pi a W_{10}(ka,kr)}{2khW_{10}(kl,kr)}[W_{10}(kl,kb) - W_{10}(kl,ka)]\,C_a \tag{56}$$

$$R_v = \sqrt{-R_m R_e} \tag{57}$$

where

$$R_m = \frac{j\pi}{2\ln(b/a)}\frac{W_{10}(kl,kl)}{W_{10}(kl,kr)} \times [W_{00}(kl,kr) - W_{00}(ka,kr)] \tag{58}$$

$$R_e = \frac{a}{l}\frac{W_{10}(ka,kr)}{W_{10}(kl,kr)}. \tag{59}$$

It can be shown from the properties of $W_{mn}(x,y)$ provided in the Appendix that all the parasitic parameters from (50)–(59) are real values despite that the imaginary unit j may be included in some expressions. Moreover, at the low frequencies where $ka, kb, kr, kl \ll 1$, using the small argument approximations of $W_{10}(x,y)$ and $W_{00}(x,y)$ given in the Appendix, the static approximations of the parasitic parameters caused by the zeroth-order mode can be obtained as

$$L_v \simeq \frac{\mu h l}{2\pi b}\ln(l/r) \tag{60}$$

$$C_v^0 \simeq \frac{\varepsilon\pi}{h}\left[l^2 - \frac{b^2-a^2}{2\ln(b/a)}\right] \tag{61}$$

$$R_v \simeq \sqrt{\frac{\ln(l/a)}{\ln(b/a)}}. \tag{62}$$

Equations (50)–(59) provide analytical expressions for all the components in the intrinsic three-port via circuit model shown in Fig. 7. Clearly, all of them are only related to the via structure itself, i.e., are functions of r, a, l, h, and ε only. The impact of the plate edges is described by the impedance matrix of the plate domain only, which will be addressed in a future publication.

It is worth giving a brief explanation on the physical meaning of each parasitic component. The shunt capacitance C_h comes from the higher order E_ρ components in (15) and (17), the series capacitance C_v^1 is due to the higher order E_z components in (14) and (16), the capacitance C_v^0 reflects the effects of the zeroth-order E_z component between the two radial plates AB and CD in Fig. 5, the inductance L_v is due to the radial loop $CDAB$, and, the transformer ratio R_v is to relate the vertical voltage V_l^- to the horizontal excitation V_2.

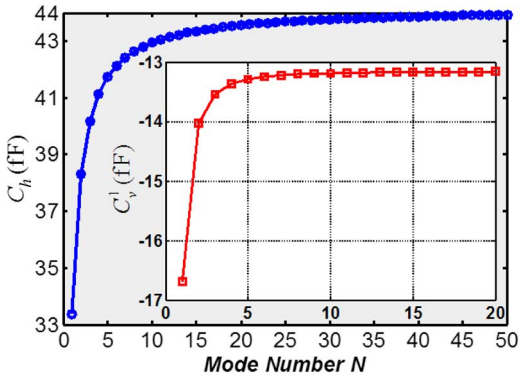

Fig. 8. Convergence of the via capacitances versus the mode number N ($r = 0.1$, $a = 0.4$, $b = 0.8$, $h = 0.8$, $R = 40$ (unit: millimeters); $\varepsilon_r = 3.84$; frequency $= 1.0$ GHz).

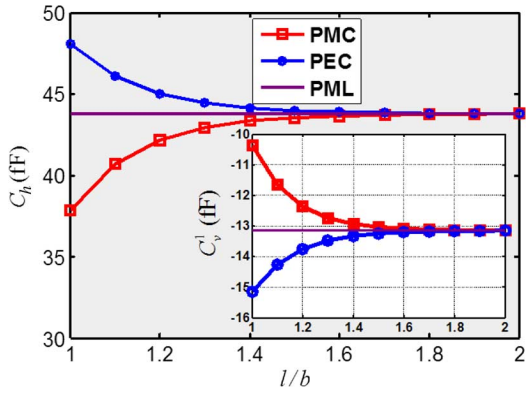

Fig. 9. Convergence of the via capacitances versus the radius of the virtual boundary with different boundary conditions ($r = 0.1$, $a = 0.4$, $b = 0.8$, $h = 0.8$ (unit: millimeters); $\varepsilon_r = 3.84$; mode number $N = 31$; frequency $=$ 1.0 GHz).

F. Properties of the Via Parasitic Components

The properties of C_h have been extensively studied in [24] for a via without a pad. Therefore, only convergence with the number of the parallel-plate modes, as well as the selection of the boundary condition at the virtual boundary at $\rho = l$, is discussed for both C_h and C_v^1.

An example of the convergence of the parasitic capacitances in (50) and (51) with the increase of N, the number of the higher order modes used in the calculations, is shown in Fig. 8. Here the outer boundary $\rho = l$ is selected to be 40 mm, far enough away from the via. It can be seen that only tens of the higher order modes are required to obtain the converged values. An interesting observation is that the series capacitance C_v^1 is negative, and its physical meaning is yet to be revealed.

The convergence of (50) and (51) with the increase of l is demonstrated in Fig. 9. The shunt and series capacitances C_h and C_v^1 converge to a constant value when l is approximately 1.6 times of the via-hole radius in this example, independent of the boundary condition applied at $\rho = l$. This is because the higher order modes decay very quickly from the via due to the small plate separation h. This demonstrates the previous assertion that there is a virtual via boundary $\rho = l$ to separate the via and plate domains. The plate size, shape, or other vias outside of the via domain have a negligible impact on the parasitic capacitances C_h and C_v^1.

In addition, the result shown in Fig. 9 implies that the difference in C_h or C_v^1 values with different boundary conditions at $\rho = l$ can be used to determine where the virtual boundary should be located in order to separate the via and plate domains. Based on this idea, an empirical formula will be developed in Section IV to determine the virtual boundary from geometrical dimensions.

From the discussion of the virtual boundary, it is clear that both the intrinsic and physics-based via circuit models are only valid when the distance between any two vias is larger than $2l$. Otherwise, the multiple higher order scattering among vias cannot be neglected. This is the limitation of this category of via circuit models.

The frequency-dependent properties of the parasitics due to the zeroth-order mode from (55)–(59) are shown in Fig. 10, where $l = b$ is used in the calculations. At the frequencies lower than 10 GHz, these parasitic parameters remain approximately constant in this example, which are consistent with the predictions of (60)–(62). However, beyond 10 GHz, the frequency dependence is significant, and a larger via-hole radius b results in a faster increase of their values with frequency.

IV. Determination of the Virtual via Boundary

The validity of the intrinsic via circuit model depends on the assumptions discussed in Section II. One of the most important ones is that all the circular via domains do not overlap. Therefore, the virtual circular boundary can be used to quantify the limitation of the intrinsic via circuit model in practical applications.

The via-plate capacitance C_h reflects the energy stored in the higher order electric fields adjacent to a via. Thus, it is used herein to quantify the size of a via domain.

From (50), different boundary conditions at $\rho = l$ will result in different values of C_h. However, when $\rho = l$ is far away from the via barrel, the C_h values for different boundary conditions converge to the one obtained using the PML boundary, as illustrated in Fig. 9. This implies that the higher order modes are negligible at the boundary and the boundary condition is not important any more. In other words, the virtual via boundary can be determined by examining whether the C_h values using different boundary conditions are close enough. To do so, a relative difference σ is introduced to define the difference in the C_h values with the PMC and PML boundary conditions at $\rho = l$ as

$$\sigma(l/b) = \frac{\sum_{n=1,3,\ldots}^{2N-1} \left[F_n^L(a) - F_n^M(a)\right]}{\sum_{n=1,3,\ldots}^{2N-1} F_n^L(a)} \tag{63}$$

where $F_n^M(a)$ and $F_n^L(a)$ are obtained by (52) and (53). For higher order modes at low frequencies, the wavenumber k_n in (13) can be approximated as a purely imaginary number, i.e., $k_n \simeq -jn\pi/h$. Therefore, $\sigma(l/b)$ is only related to l/b, h/b, and a/b, independent of the dielectric constant ε_r and frequency. Note that all the geometrical parameters are normalized to the via-hole radius b since l must be larger than or equal to $b (l \geq b)$.

Some examples with different h/b and a/b values for the relative difference σ are shown in Fig. 11. It can be seen that

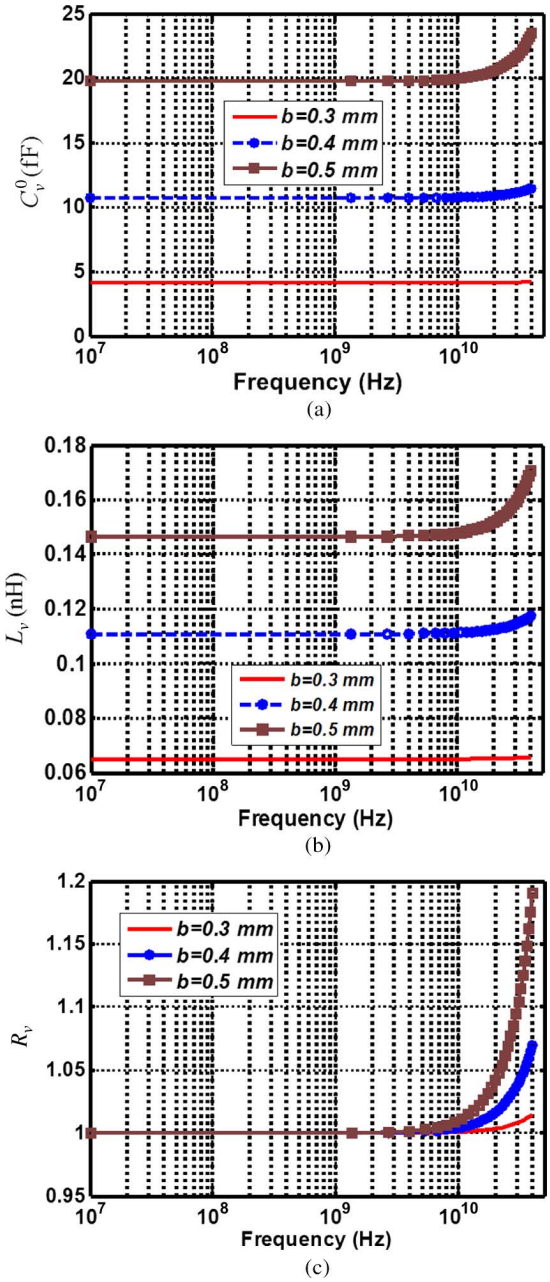

Fig. 10. Frequency-dependent properties of the parasitics due to the zeroth-order waves with different via-hole radii ($r = a = 0.2$ mm, $h = 0.8$ mm, $\varepsilon_r = 4.2$; $l = b$ is used here).

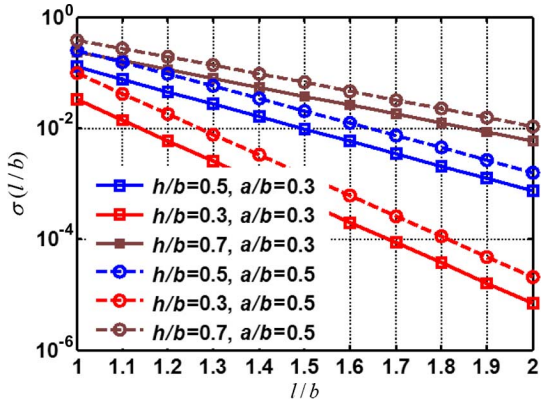

Fig. 11. Examples of the relative difference versus the radius of the virtual boundary ($r = 0.1, a = 0.4, b = 0.8$ (unit: millimeters); $\varepsilon_r = 3.84$; mode number $N = 31$; frequency $= 1.0$ GHz).

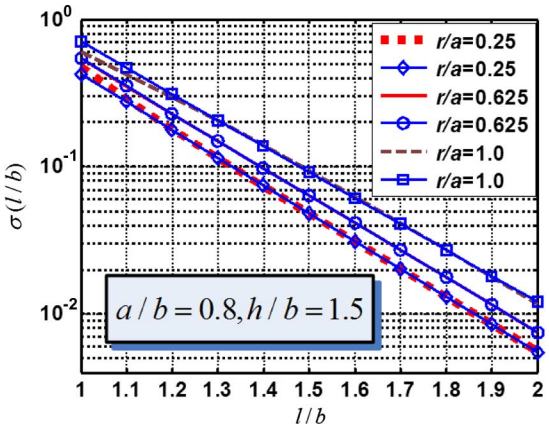

Fig. 12. Validation of the curve-fitting formula for the relative difference [lines without symbols: from (63); lines with symbols: from (64)].

σ in logarithmic scale decays approximately linearly with l/b. Therefore, σ can be approximated as

$$\sigma(l/b) \simeq \alpha e^{-\beta(l/b)} \tag{64}$$

where, for a specific via structure, α and β are two constant parameters that can be calculated by selecting two different l/b values in (63) as

$$\beta = -\frac{\ln\sigma(l_2/b) - \ln\sigma(l_1/b)}{l_2/b - l_1/b} \tag{65}$$

$$\ln\alpha = \frac{(l_1/b)\ln\sigma(l_2/b) - (l_2/b)\ln\sigma(l_1/b)}{l_1/b - l_2/b}. \tag{66}$$

In most practical designs, $l_2/b = 1.8$ and $l_1/b = 1.3$ are suitable choices for estimating β and α. The curve-fitting formula (64) and the accurate expression (63) of the relative difference for several vias with different barrel-to-pad radius are compared in Fig. 12. Note that although this is a relatively extreme case with large h/b and a/b values, good agreement is achieved between (63) and (64).

Using (64), the virtual via domain boundary at $\rho = l$ can be determined by specifying a small tolerance ϵ. This yields

$$l = b\left[\frac{\ln\alpha - \ln\epsilon}{\beta}\right]. \tag{67}$$

For signal integrity analyses, $0.05 \le \epsilon \le 0.1$ is an acceptable choice. The smaller the relative difference is required, the larger the value of the virtual via boundary l.

V. Complete Model for Multiple Vias in an Irregular Plate Pair

The intrinsic via circuit model for a single via, as shown in Fig. 7, can be easily extended to the cases involving multiple

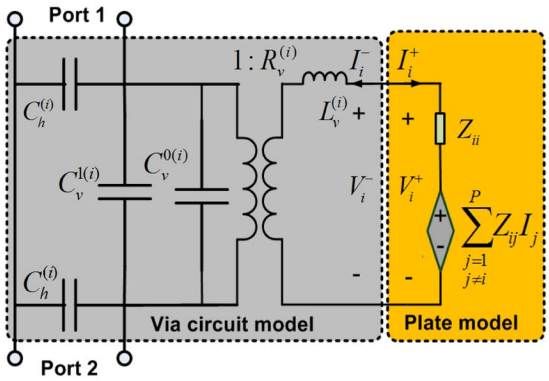

Fig. 13. ith via circuit model when P vias are present in a parallel-plate pair.

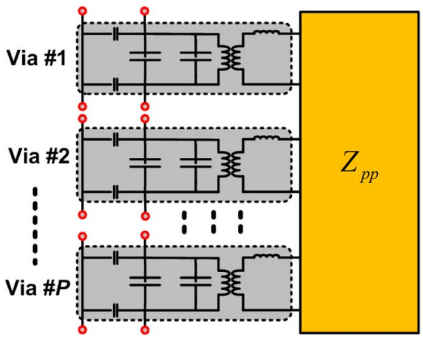

Fig. 14. Schematic of circuit model for P vias in an irregular parallel-plate pair.

vias. With P vias in a plate pair, the voltage and current relationship of (40) is replaced by

$$V_i = Z_{ii} I_i + \sum_{j=1, j\neq i}^{P} Z_{ij} I_j. \tag{68}$$

An impedance matrix Z_{pp} is used to describe port voltages as functions of port currents in the plate domain, as shown in Fig. 1(a).

Using (68) instead of (40), and following the same procedure in the derivation of the via circuit due to the zeroth-order waves, an equivalent-circuit model for the ith via can be obtained, as shown in Fig. 13, using the ideal transformer theory [38]. For any arbitrarily shaped plate pair with P vias, Fig. 13 is valid for each via, which leads to a complete circuit model shown in Fig. 14 for multiple vias in an irregular plate pair.

The impedance of a plate pair used in (40) or (68) is different from the conventional one defined in [26] where rectangular ports and area integration of the Green's function are used to analytically evaluate the impedance matrix in a rectangular plate pair. In this application, ports in a plate pair should be circular, as already pointed out in [32], and Z_{pp} should be the impedance matrix for the plate pair with multiple PMC holes (with the via domains excluded). The new Z_{pp} will be addressed in detail in a future publication.

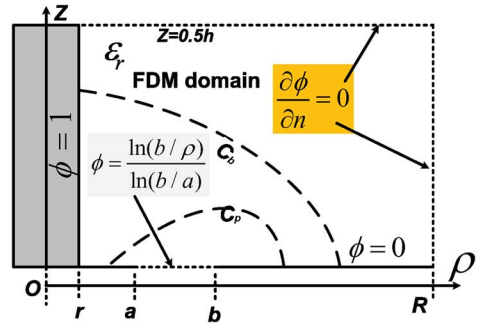

Fig. 15. Solution domain for the shunt capacitance C_h and the boundary conditions when the finite-difference method is applied.

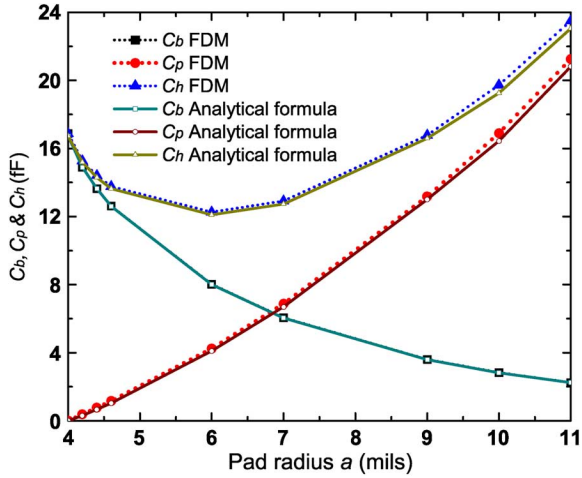

Fig. 16. Comparisons of the barrel-plate, pad-plate, and shunt capacitances using analytical formulas and the finite-difference method (FDM) ($r = 0.1016$, $b = 0.4318$, $h = 0.2286$, $R = 1.27$ (unit: millimeters); 1 mil = 0.0254 mm; frequency of 1.0 GHz is chosen in capacitance evaluations using analytical formula).

VI. Validation and Measurements

A. Evaluation of C_b, C_p, and C_h Using Finite-Difference Method

In the intrinsic via circuit model, the shunt capacitance C_h, including C_p and C_b, can be validated using quasi-static approximations. Due to the radial symmetry, the potential ϕ satisfies the 2-D Laplace equation

$$\frac{1}{\rho}\frac{\partial}{\partial \rho}\left(\rho \frac{\partial \phi}{\partial \rho}\right) + \frac{\partial^2 \phi}{\partial z^2} = 0. \tag{69}$$

The finite-difference method is used to solve (69), and the solution domain is defined in a rectangular $\rho - z$ region, as shown in Fig. 15, where the Neumann boundary condition is specified on the plane of $z = 0.5h$, as discussed in [24].

The details of the finite-difference method implementation have been given in [39]. The shunt capacitances C_p, C_b, and C_h obtained by analytical formulas (28), (30), and (31), as well as by the finite-difference method are compared in Fig. 16. When other parameters are fixed, with the increase of the pad radius

a, C_p increases and C_b decreases steadily; the combined capacitance C_h ($C_h = C_b + C_p$) decreases initially and then increases rapidly. The analytical evaluations and the numerical finite-difference simulations agree well. The meshing grid in the finite-difference method was chosen to be either 1.27×10^{-3} mm (0.05 mil) or 0.635×10^{-3} mm (0.025 mil), and convergence with mesh density was ensured.

B. Input Impedance of a Probe in a Circular Plate Pair

A probe can be viewed as a special via with its top coaxial port closed by a PEC, as shown in Fig. 2. Consequently, an equivalent probe circuit model can be obtained by shorting the top coaxial port (Port 1) in the three-port via circuit model given in Fig. 7. The input admittance of a centrally located probe in a circular plate pair can then be obtained as

$$Y_{\text{in}}^{C} = j\omega\left(C_h + C_v^1 + C_v^0\right) + \frac{R_v^2}{j\omega L_v + Z_l^+}. \tag{70}$$

Another expression for the input admittance of a probe in a circular plate pair seen from Fig. 4 is

$$Y_{\text{in}}^{A} = j\omega\left(C_h + C_v^1\right) + Y_v \tag{71}$$

where Y_v is obtained by (33). Equations (70) and (71) can be regarded as two different expressions for Y_{22} in (23), which can be further proven to be consistent with the formulas for a probe in an infinite plate pair derived in [15], [33], and [34] when $S = L$ is selected for $F_n^S(a)$ calculations. Therefore, Y_{22} in (23) can be viewed as a general analytical formula for the input admittance of a probe located in a circular plate pair.

The input admittance can also be obtained from the physics-based via circuit model as

$$Y_{\text{in}}^{P} = j\omega C_h + \frac{1}{Z_r} \tag{72}$$

where Z_r is calculated from (19) by replacing l with r, the via barrel radius [20]–[22]. This indicates for the physics-based via circuit model, the radial port (Port 3) should be defined at the barrel radius to minimize the parasitic effects due to C_v^0, C_v^1, R_v, and L_v instead of the virtual boundary of $\rho = l$ for the intrinsic via circuit model.

By numerically comparing the input admittances of a probe using (70) of the equivalent probe circuit, (71) of the analytical formula, and (72) of the physics-based circuit, the equivalence of (70) and (71) can be verified, and also the limitation of the physics-based via circuit model can be observed.

The input impedance results of a probe in an infinite plate pair using the three different expressions are compared in Fig. 17. The radii of the probe barrel and the via-hole are 0.254 mm (10 mil) and 0.8382 mm (33 mil), respectively. The separation of the plates is 1.4732 mm (58 mil). A Debye dielectric model, $\varepsilon_r = \varepsilon_\infty + (\varepsilon_s - \varepsilon_\infty)/(1 + j\omega\tau)$, is used for the permittivity of the dielectric material between the two plates. The relative static permittivity ε_s and the optical permittivity ε_∞ are set to be 4.3 and 4.1, respectively; and, the relaxation time τ is 3.1831×10^{-11}.

The input impedance calculated from (70) of the equivalent probe circuit agrees very well with (71) of the analytical formula for both the real and imaginary parts. The input impedance calculated from (72) of the physics-based via circuit model, however, matches (70) and (71) at low frequencies only. Moreover, the resonant frequency predicted from (72) is 15 GHz, as opposed to 20 GHz calculated from (70) and (71).

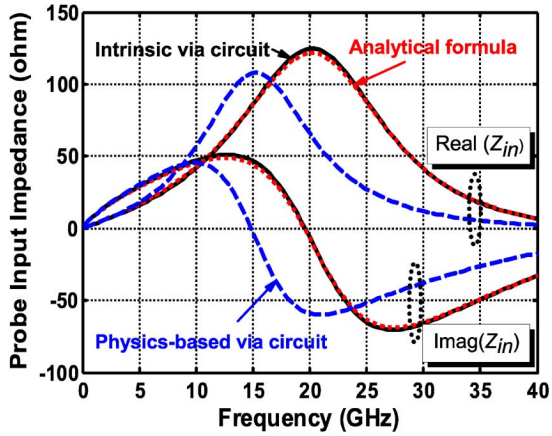

Fig. 17. Comparisons of the input impedance results of a probe in an infinite plate pair ($r = a = 0.254, b = 0.8382, h = 1.4732$, unit: mm).

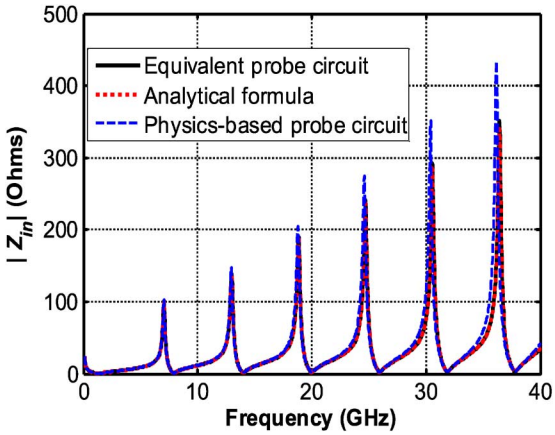

Fig. 18. Comparisons of the input impedance results of a probe in a finite circular plate pair. Via dimensions are the same as those in Fig. 17, and the radius of the plate pair is 10.2 cm.

The three different formulas to calculate the input impedance of a probe centered in a finite circular plate pair with a radius of 10.2 cm and a PMC edge boundary condition are compared in Fig. 18. Calculations from (70) and (71) match each other in the entire frequency band. Further, (72) agrees well with both (70) and (71) at the first several resonant frequencies, but deviates from them as frequency increases.

The comparisons in these two figures indicate that: 1) the new expression for Y_v in (48), which is key to derive the intrinsic three-port via circuit model, agrees very well with that in (33) and 2) the physics-based via circuit model can be viewed as an approximation of the intrinsic three-port via circuit model at low frequencies. The difference between these two models becomes larger with the increase of frequency and plate-pair sizes.

In practical applications, the physics-based circuit model is usually acceptable due to several reasons. First, only lowest resonant frequencies of a plate pair are usually critical for signal/

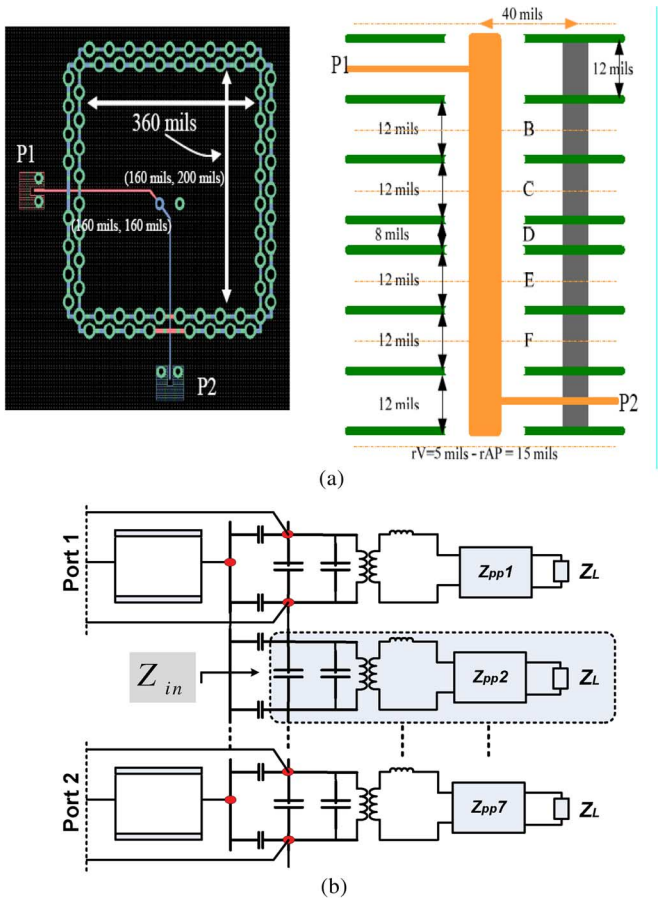

Fig. 19. (a) Test board geometry (courtesy of the authors of [21]) (1 mil = 0.0254 mm). (b) Equivalent circuit using the intrinsic three-port via model for the test board geometry shown in (a).

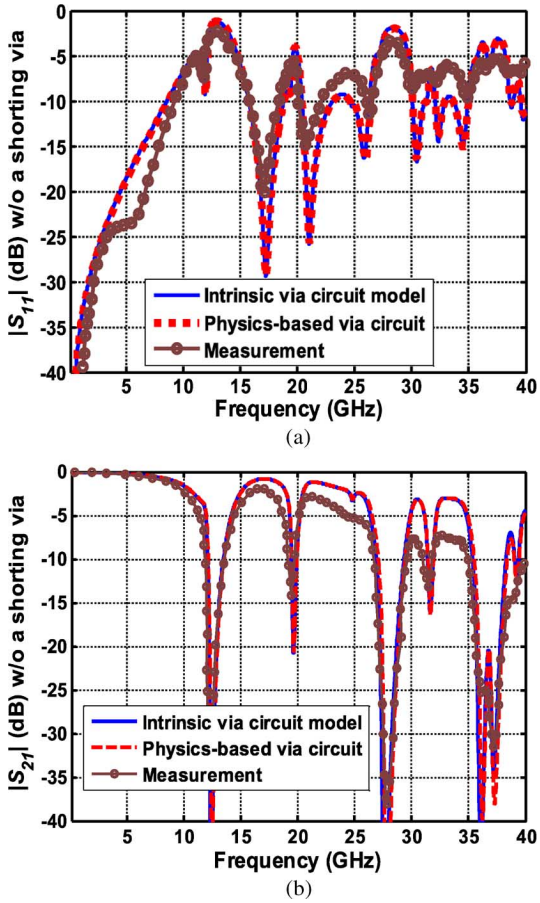

Fig. 20. Comparisons of the S-parameters obtained by the intrinsic via circuit model, the physics-based via circuit model, and measurements without a local shorting via.

power integrity analysis depending on the specific data rate and rise time. Secondly, a plate pair in practical PCBs is usually not large enough so that the approximation of using the physics-based equivalent circuit can still result in an acceptable accuracy. Thirdly, to provide a current return path, shorting vias or decoupling capacitors are often used in a plate pair, which in most cases reduces the impact of the plate-pair sizes. Therefore, the rigorous intrinsic via circuit model derived here justifies the engineering applications of the physics-based via circuit introduced in [20] and [21] at low frequencies in the cases with a relatively small plate pair, or a plate pair with dense shorting vias/decoupling capacitors.

C. Measurements

Fig. 19(a) illustrates a test board geometry measured to validate the intrinsic via circuit model. It contains seven plate pair with two striplines located in the top and bottom ones, respectively. The separations of the plate pair are 0.3048 mm (12 mil) or 0.2032 mm (8 mil). A signal via located at (4.064, 4.064) mm or (160, 160) mil, as shown in Fig. 19(a), connects these two striplines. The radii of the via barrel and via hole are 0.127 and 0.381 mm, respectively. For each plate pair, the fields are restricted inside a 9.144×9.144 mm^2 or 360×360 mil^2 cavity constructed by dense stitching vias connecting all the plates (an approximate PEC cavity). An additional shorting via is located at (4.064, 5.080) mm or (160, 200) mil to provide an adjacent return path for the signal via. The relative permittivity and loss tangent of the dielectric layers between the plates are 3.5 and 0.014, respectively.

The transmission property between Ports 1 and 2 of the test board geometry is simulated by the equivalent circuit shown in Fig. 19(b). Note that each stripline is split into two microstrip lines referenced to the top and bottom plates, as proposed in [21], in order to be connected to the intrinsic via circuit model. The length of the microstrip lines is assumed to be 6.35 mm (250 mil) in the simulation. The intrinsic via circuit models are connected to the impedance matrix of each plate pair, which is terminated by a load impedance Z_L. Two cases were studied: with and without the local shorting via at (4.064, 5.080) mm. $Z_L = 0$ is used for the case with the local shorting via while $Z_L = \infty$ is used for the case without the local shorting via.

The S-parameters calculated from the rigorous intrinsic via circuit model, the approximate physics-based via circuit model, and measurements for the cases with and without the local shorting via are compared in Figs. 20 and 21, respectively. The circuit models were simulated using the Advanced Design System (ADS), a circuit simulator from Agilent Technologies, Santa Clara, CA. The S-parameters of the test geometry were measured using an Agilent vector network analyzer (VNA)

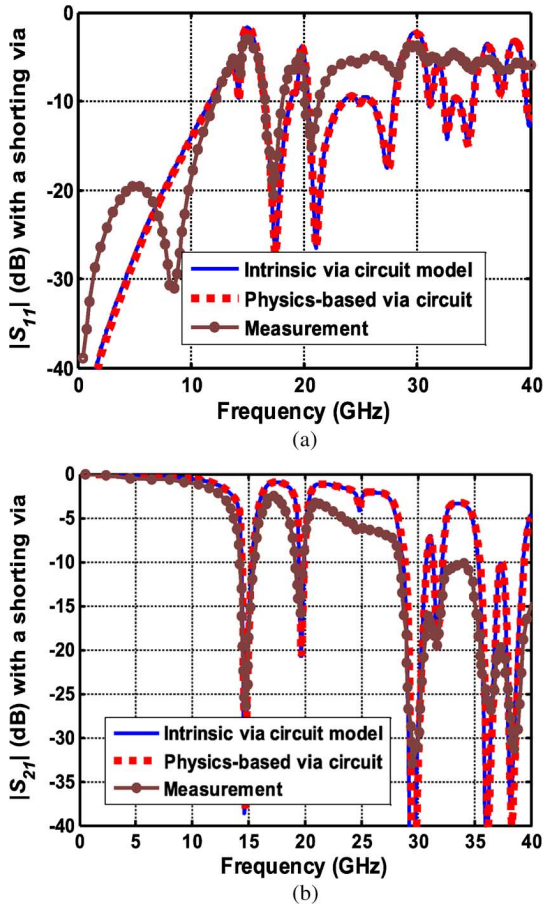

Fig. 21. Comparisons of the S-parameters obtained by the intrinsic via circuit model, the physics-based via circuit model and measurements when a local shorting via is present.

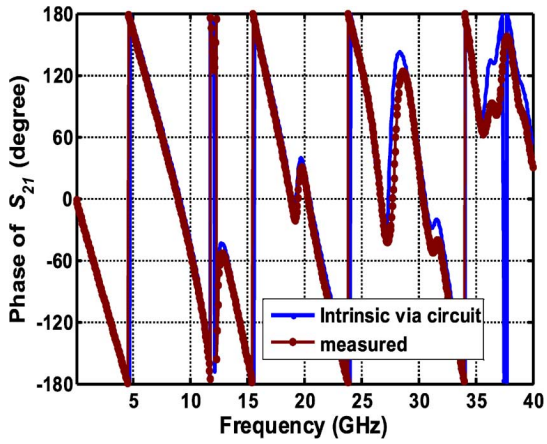

Fig. 22. Phase comparison of S_{21} obtained by the intrinsic via circuit model and measurements without a local shorting via.

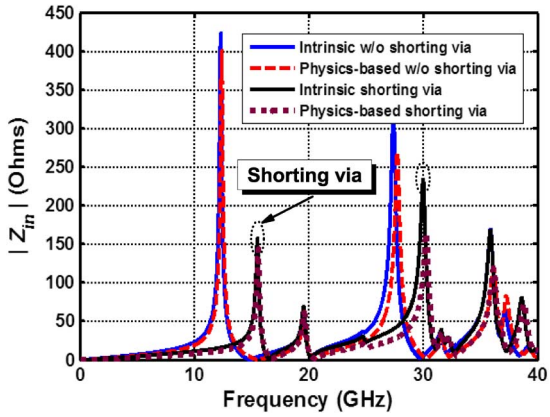

Fig. 23. Magnitudes of the input impedance calculated from the intrinsic via circuit and the physics-based via circuit models.

E8364A in the frequency band from 45 MHz to 40 GHz. Microwave probes, model 40A G-S and S-G with a 225-μm pitch, from GGB Industries Inc., Naples, FL, were used to minimize the effects of test fixtures. The short-open-load-thru (SOLT) calibration was conducted using a CS-14 calibration substrate, also from GGB Industries Inc.

There are only slight differences between the results obtained from the rigorous intrinsic via circuit model and the approximate physics-based via circuit model. These two models match the measured results very well up to 15 GHz. At higher frequencies, these two models can also predict the same trends of the S-parameters as the measurements, but with larger discrepancies. A possible reason for the discrepancies is that the trace-to-via discontinuities are neglected in the simulations.

In addition, Fig. 22 also shows good agreement up to 30 GHz between the phase of S_{21} obtained by the intrinsic via circuit model and the measurement.

The impedance of each plate pair, $Z_{\rm in}$, as illustrated in Fig. 19(b), is a critical parameter to understand the simulation results of S_{21}. A smaller Z_{pp} will result in a better transmission property between the two ports.

The impedance magnitudes of the second plate pair obtained from the intrinsic and physics-based via circuit models are compared in Fig. 23. These two models provide almost the same series impedances. As mentioned earlier for the input impedance of a probe, these two via circuit models result in quite similar results for a small plate pair at the first several resonant frequencies. The test board geometry in this example is very small in dimension. Therefore, at the frequencies of interest (less than 40 GHz), the physics-based via circuit is still a good approximation. This explains why these two models provide almost the same S-parameters in Figs. 20 and 21.

The resonant peaks in Fig. 23 lead to the minimum $|S_{21}|$ values in both Figs. 20(b) and 21(b). This is because $Z_{\rm in}$ is the impedance of the return current path of the signal via. At low frequencies, the surrounding stitching vias are an effective low-impedance return current path. Thus, the signal can easily pass through several layers of the plate pair. Another observation from Fig. 23 is that the local shorting via shifts the first resonant frequency from 12.35 to 14.58 GHz, enhancing the bandwidth of the signal channel.

VII. Conclusions

An intrinsic three-port via circuit model and its connection to the impedance matrix of a plate pair is derived rigorously through electromagnetic analysis. Both boundary conditions at vias and plate edges are satisfied explicitly. This provides a theoretical foundation for the physics-based via circuit model that

was developed ad hoc from physical intuition. Analytical formulas for the input impedance of a probe in a circular plate pair are used to verify the derived intrinsic via circuit model. It shows that the physics-based via circuit model is an acceptable approximation to the rigorous one derived in this paper for a relatively small plate pair or for a plate pair with dense shorting vias/decoupling capacitors. Furthermore, test boards with a signal via and a seven-plate pair with and without a local shorting via are employed to validate the intrinsic via circuit model with good agreement.

APPENDIX
PROPERTIES OF THE AUXILIARY FUNCTION $W_{mn}(x,y)$

- For real values of x and y, $W_{mn}(x,y)$ is imaginary as

$$W_{mn}(x,y) = -j \begin{vmatrix} J_m(x) & J_n(y) \\ Y_m(x) & Y_n(y) \end{vmatrix} \tag{73}$$

  where $Y_m(\cdot)$ is a Neumann function or mth-order Bessel function of the second kind.
- For real values of x and y, $W_{mn}(jx,jy)$ can be expressed as

$$W_{mn}(jx,jy) = \frac{2}{\pi} j^{n-m+1} \begin{vmatrix} I_m(x) & I_n(y) \\ K_m(x) & K_n(y) \end{vmatrix} \tag{74}$$

  where $I_m(\cdot)$ and $K_m(\cdot)$ are the mth-order modified Bessel functions of the first and second kind, respectively.
- Using small argument approximations of the Bessel and Hankel functions ($x \to 0$ and $y \to 0$), it can be shown that

$$W_{10}(x,y) \simeq -j\frac{2}{\pi}\left[\frac{1}{x} + \frac{x}{2}\ln y - \frac{y^2}{4x}\right] \tag{75}$$

$$W_{00}(x,y) \simeq j\frac{2}{\pi}\ln(x/y). \tag{76}$$

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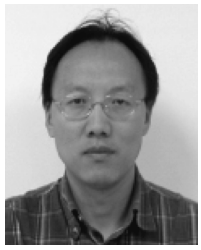

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