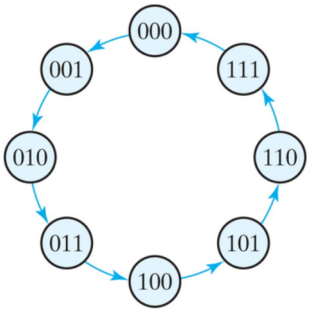
Homework 6

1. What follows is the VMLAB project information and AVR code for an 8-bit up/down counter, where the count direction is controlled by the state of PIN B, bit 0:

   Add the following onto the end of the project file:

   ```
   K0 PB0 VSS LATCHED
   R0 VDD PB0 5000
   ```

   And here is the AVR code:

   ```
   clr r16
   main:
   sbic PINB, 0
   inc r16
   sbis PINB, 0
   dec r16
   rjmp main
   ```

   Modify this code to create a 3-bit up counter that stops the count when PIN D, bit 1, is LOW. Use the 3 least significant bits of R16.

2. Design an 8-bit one-hot counter from a single 4-bit Johnson counter. Assume the counter is reset to all 0's before the sequence starts. What would be the problem with trying to build a 16-bit one-hot counter from a single 4-bit Johnson counter?

3. Modify the circuit from Homework 5, #5 so that Z produces N transitions in each 16-tick interval. The resulting circuit is called a binary rate multiplier and was once sold as a TTL MSI part, the 7497.

4. Search for a datasheet with the internal logic diagram for a 74162 synchronous decade counter. Write a state table and include its counting behavior in the normally unused states 10-15.

5. From the Wakerly textbook, problems 11.62