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ENGR 271

Lab 0xA: D/A Conversion (DAC)

Introduction

In this lab we explore Digital-To-Analog converters, also known as DACs (D/A, D2A, or D-to-A). These are circuits that convert a digital signal into an analog signal. There are different circuit architectures to achieve this. We will explore two different types, binary-weighted DAC and the R-2R DAC. We want to consider the following DAC performance characteristics.

Resolution: The number of possible discrete output values, or the number of bits used

Maximum sampling rate: The maximum speed the DACs circuity can operate and still produce correct output.

Monotonic: The ability of the analog output to move in only one direction, which is the same direction as the digital input. If the input increases, the output doesn't decrease before it increases.

Part A: Binary-Weighted DAC

In this section, we are tasked with building a Binary-Weighted DAC (BW-DAC). In the first section, we build a 4-bit BW-DAC and then in the second section, we create a 5-bit BW-DAC. The first thing we must do is use Figure 1: 4-bit BW-DAC and circuit analysis techniques to calculate the voltage contribution to the output of each bit. This was built in Multisim from the lab instructions.

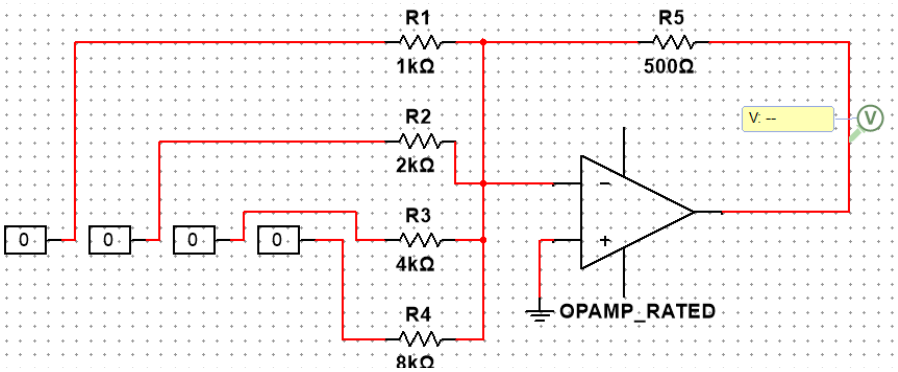

Figure 1: 4-bit Binary-Weighted DAC (BW-DAC)

Based on the hand calculations shown in Figure 2, we can see that each bit contributes voltage based on the gain factor on the OP AMP

$$Voltage(gain) = -(\frac{R5}{Rx}) * Vin,\ where\ Rx \rightarrow R1\ through\ R4\ and\ Vin = 5[V]$$

[Equation 1]

Using this formula, we can calculate the voltage contribution to the output from each bit, which can be

seen in Table 1 below. Vin is the input voltage, Rx is the resistor we are considering (R1 - R4) and Vo is the output voltage. The voltage is negative on the output side because we are using an inverting OP AMP. We will add components to have a positive output voltage later in Part A.

Vin [V]	Rx (Ω)	Vo [V]
5	1000	-2.5
5	2000	-1.25
5	4000	-0.625
5	8000	-0.3125

Table 1: Voltage Contribution to the output from each big

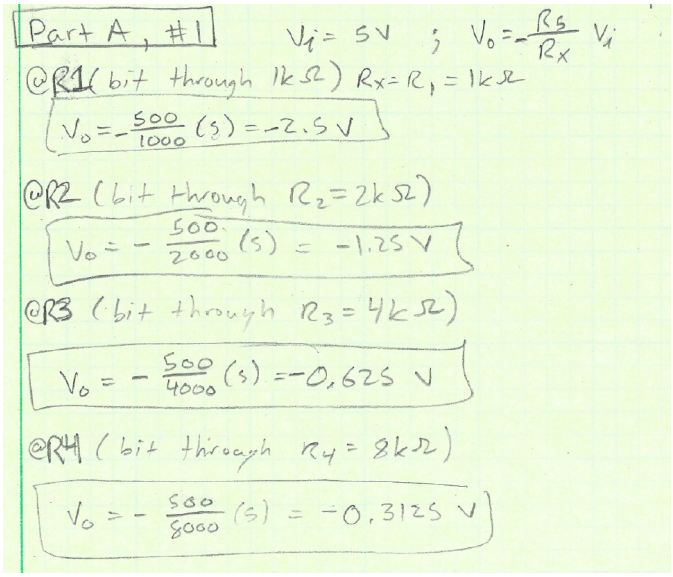

Figure 2: Hand Calculations, BW-DAC (Binary-Weighted DAC)

Based on these calculations, we can increase the number of bits used fairly easily. We can add more bits with resistors in series that are in parallel with the other resistors (R1 - R4). As seen in the calculations, each new resistor divides the previous output by ½ . We would run into issues with more bits once we divide the output voltage into a small enough number that the OP AMP will run into issues distinguishing between two bits. This will vary based on the architecture of the OP AMP. We do this in the next section, by creating a 5-bit BW-DAC, which can be seen in Figure 3 below on the next page

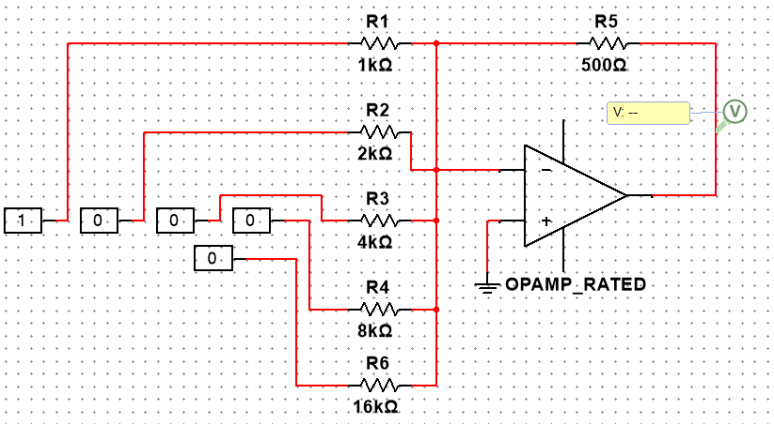

Figure 3: 5-bit BW-DAC

This circuit was tested and shown we have the values we expect at R1 - R4. Then, at R6 we would expect, using Equation 1, we have:

$$Vo = -\left(\frac{500}{16{,}000}\right) * 5 = -0.156\,[V]$$

Next we tested this circuit to show it works properly and is displayed in Figure 4a - 4c. Please reference Table 1 for expected Vo values. We can expect a +/- 10% tolerance on the output due to OP AMP internal architecture and resistor manufacturing tolerance. We can see that we get our expected values on the 1st, 3rd and 5th bit.

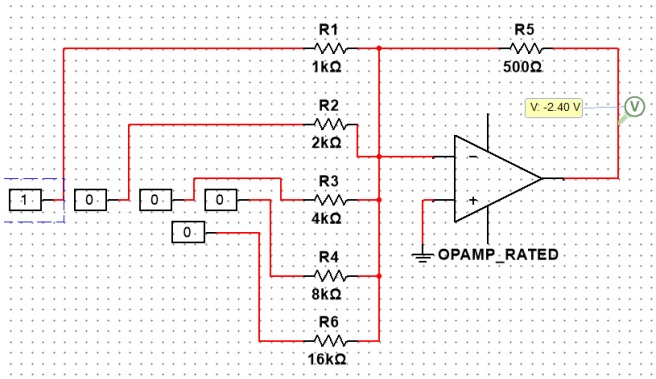

Figure 4a: Test 1, First Bit

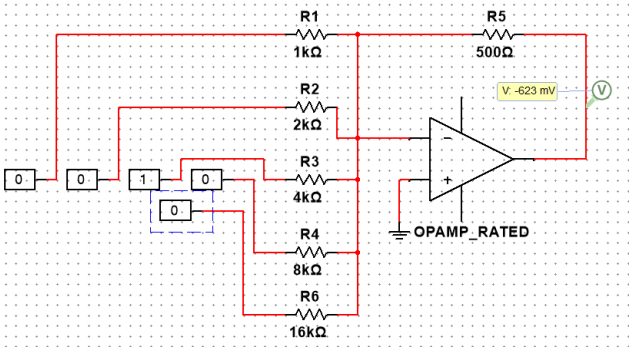

Figure 4b: Test 2, Third Bit

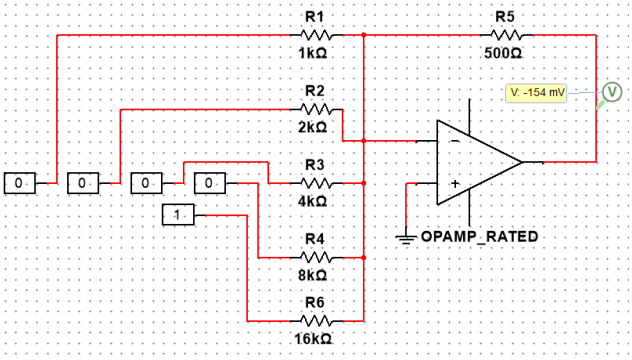

Figure 4c: Test 3, Fifth Bit

The next thing we were tasked with was adding components to this circuit to allow a positive voltage on the output and replace the q-bits with an up-counter. Below in Figure 5, we added another inverting OP AMP with a gain factor of 1, which changes the output voltage to a positive value. Below, Vo is the output from the 2nd OP AMP stage and the Vin is negative, because this is the output voltage from the 1st OP AMP stage. This can be seen on the probe values on the schematic. Since we are using a 5-bit BW-DAC, we needed two up-counters, and we had to reverse the order of the resistors before the 1st OP AMP stage to enable the correct stair-step up output we expect.

$$Vo = -\left(\frac{Rx2}{Rx1}\right) *- Vin$$

$$Vo = \frac{1000}{1000} * 5$$

$$Vo = 5\,[V]$$

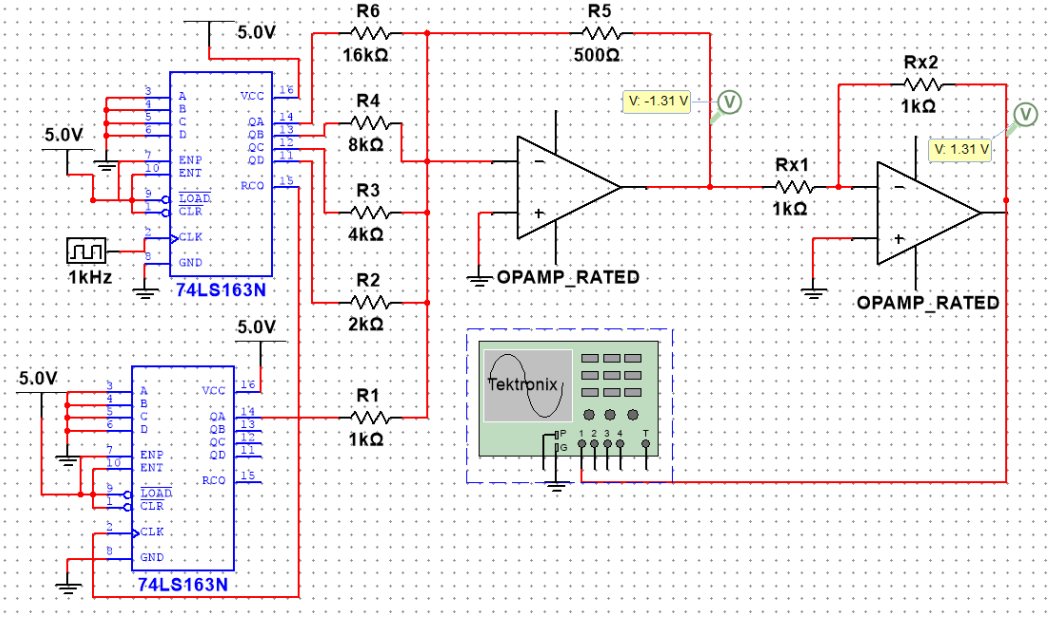

Figure 5: 5-bit BW-DAC with Up-Counters

In Figure 6, we can see the counter working properly and showing the correct output voltage that we expect to see from an up-counter connected to a 5-bit BW-DAC.

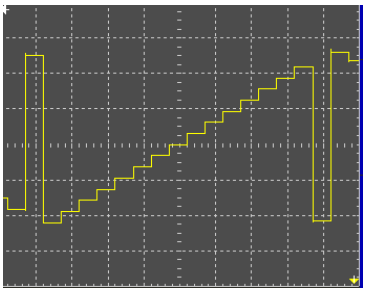

Figure 6: 5-bit BW-DAC
Oscilloscope Output Voltage (OP AMP Stage 2), Probe 1 (Yellow)

We need to consider some performance considerations and limiting factors when using a large number of bits. As we increase the number of bits, the voltage difference between bits is less. With a large number of bits, this can lead to issues with the OP AMP, as it could cause switching errors that would skip bits. This would be the ideal circuit build up until a certain point, where the OP AMP can't keep up.

Part B: R-2R DAC

In Part B, we build and test a different type of DAC. In this part, we use a R-2R DAC. This is just a simple circuit with resistors, that uses a concept from circuit analysis known as thevenin equivalent and a voltage divider, to cause each bit to have a different output voltage. Below in Figure 7a and 7b, we can see the hand calculations done to verify that the 4-bit R-2R DAC works in the same way that the BW-DAC works, with bit 1 being 2.5 [V], down to 0.3125 [V]. In this type of DAC, we don't have to worry about any negative voltages, as there is no inverting OP AMP being used. In Figure 8, we can see the circuit we used to calculate these values.

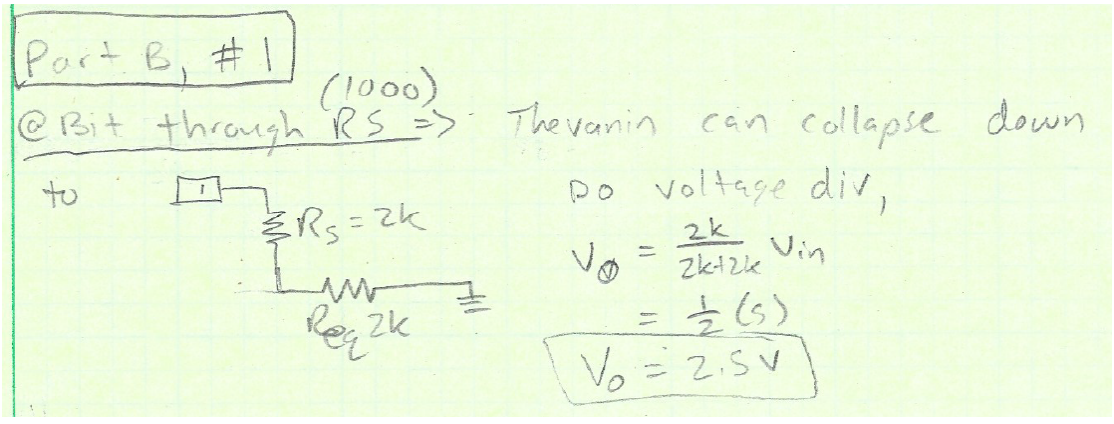

Figure 7a: Hand Calculations

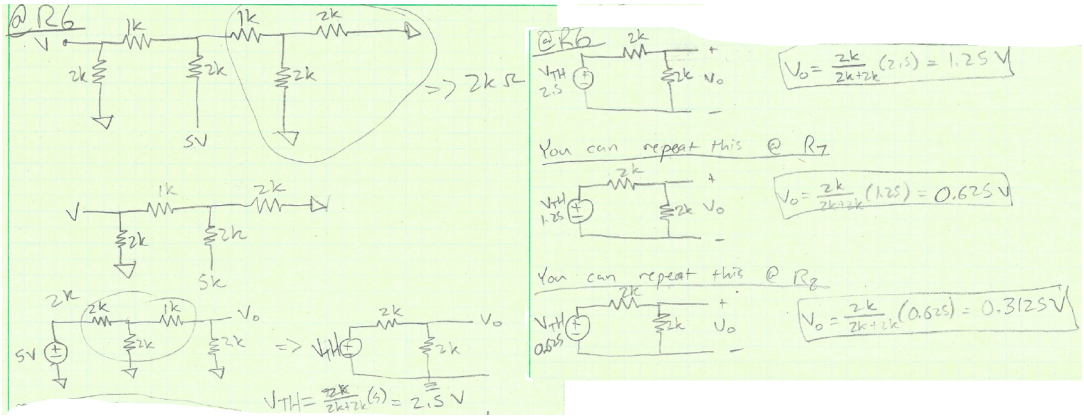

Figure 7b: Hand Calculations

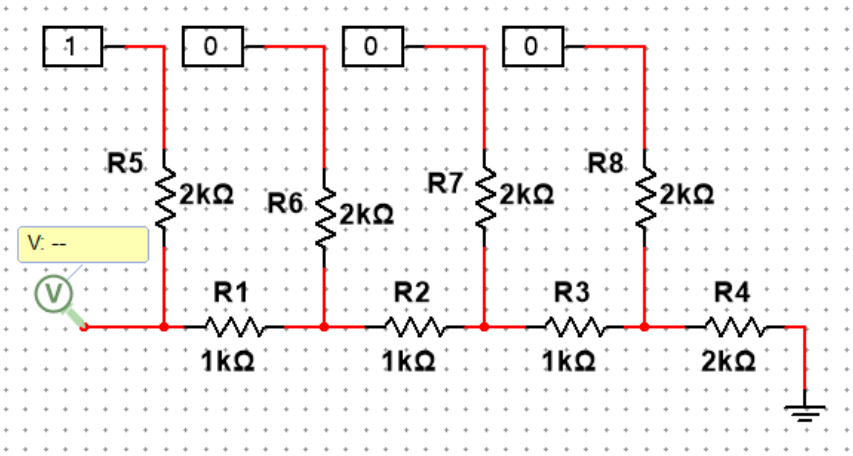

Figure 8: 4-bit R-2R DAC

Based on these calculations, we could add more stages between R8 and R4, that are a copy of the bit input, R8 and R3. This can be seen in Figure 9 below. In this example, we added two more stages between R8 and R4 from Figure 8.

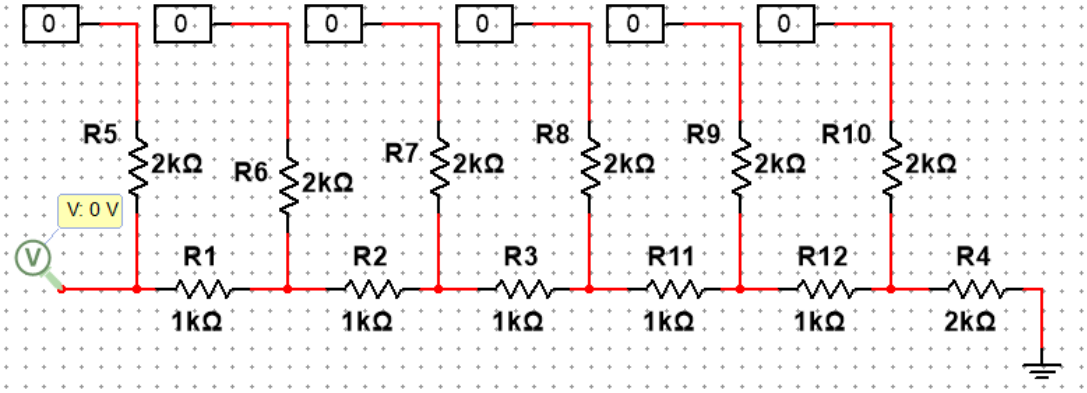

Figure 9: 6-bit R-2R DAC

Next, we tested a few different input combinations to show that the circuit works properly, which it does. This can be seen below in Figure 10a - 10c. We used test cases from R5, R6 and R7 so we can easily reference the hand calculations in Figure 7a and 7b, as they should be the same even with the additional stages added in. The additional stages will have half of the previous bits voltage, across the new resistor, for example, the voltage across R9 will have half that of the voltage across R8, and so on. This can also be seen, where the voltage at R6 is half that of the voltage at R5 and so on.

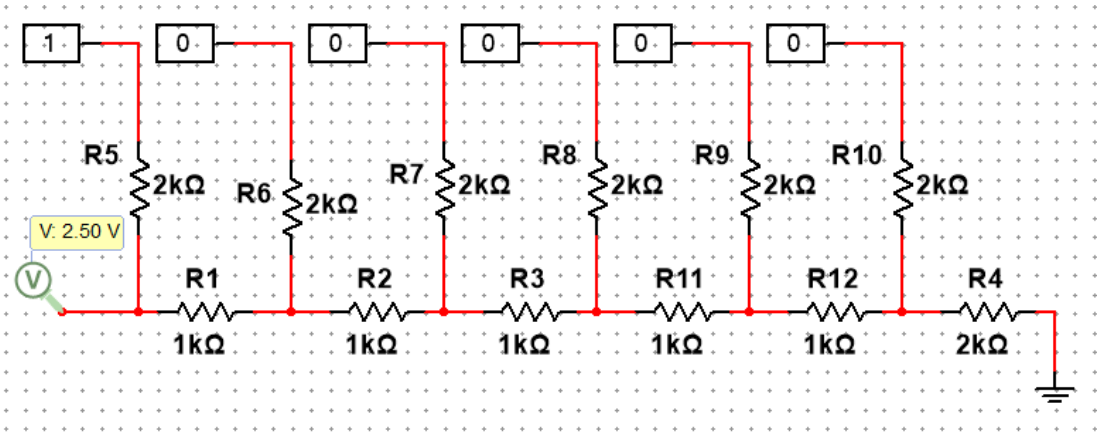

Figure 10a: Test Case 1

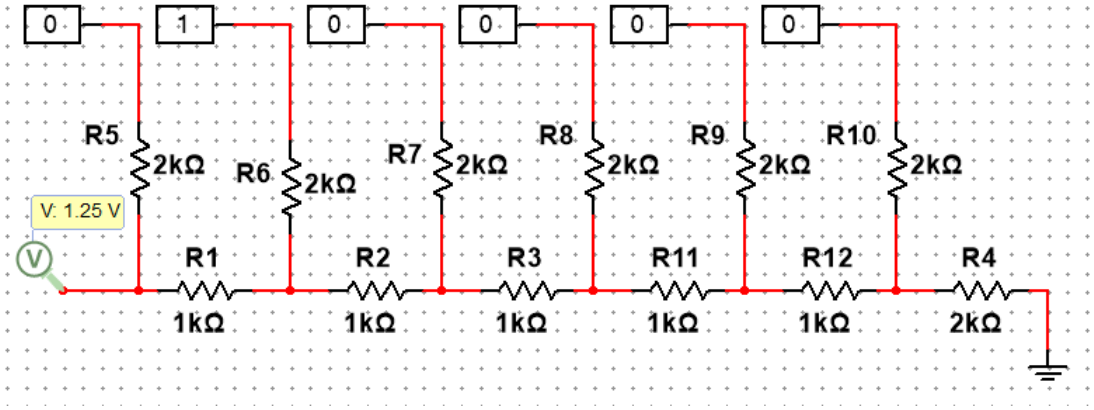

Figure 10b: Test Case 2

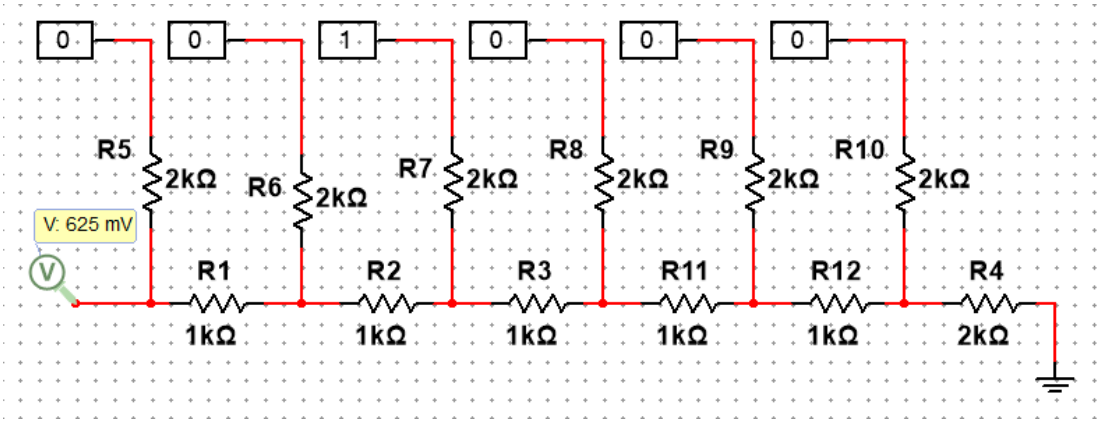

Figure 10c: Test Case 3

Finally, we are tasked with adding an input counter, output driver and an oscilloscope to the 6-bit R-2R DAC. In Figure 11, we can see the 6-bit R-2R DAC circuit with the additional components. Please note that the oscilloscope probe 1 is connected to the output of the R-2R DAC. Then, in Figure 12, we can see the oscilloscope output. It is what we expect to see.

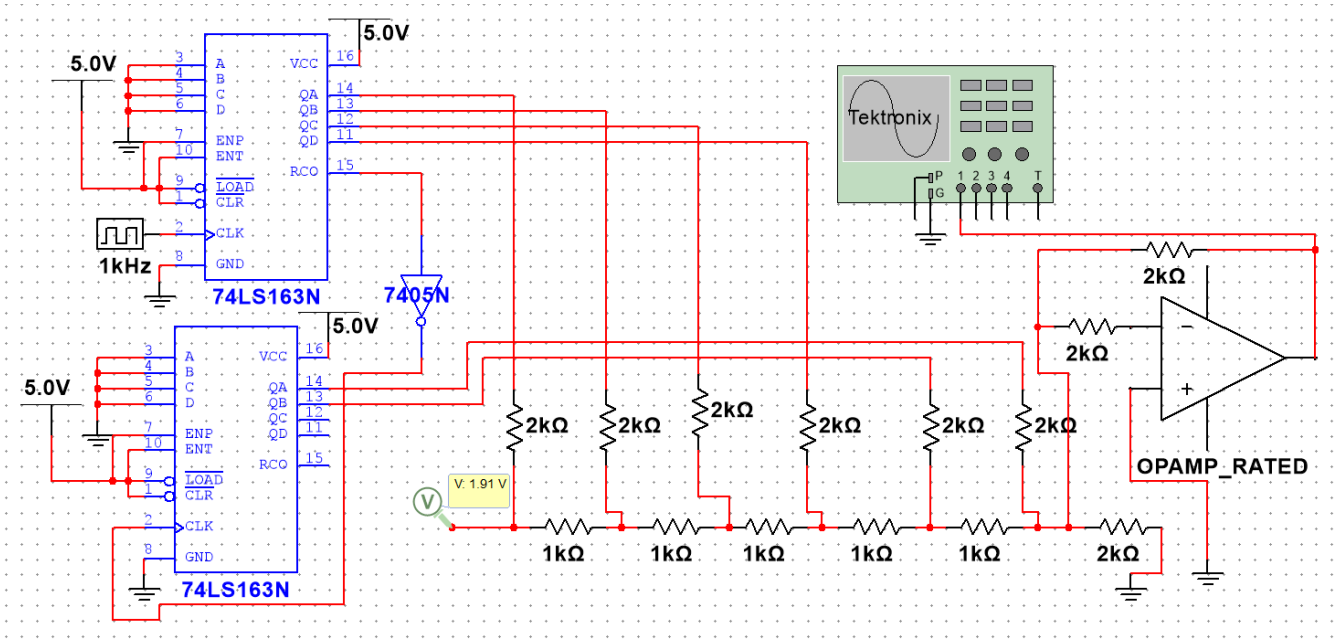

Figure 11: 6-bit R-2R DAC with input counter, output driver circuit and oscilloscope

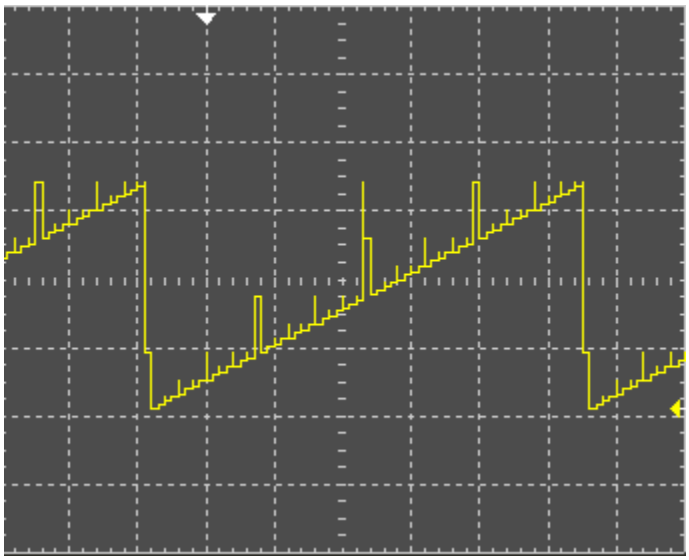

Figure 12: 6-bit R-2R DAC
Oscilloscope Output Voltage, Probe 1 (Yellow)

Part C: 4-Bit Binary-Weighted DAC with Up/Down Counter

In Part C (or procedure 9), we are asked to design a 4-bit input driver that counts up and then at max value, counts down, then repeats the cycle. We used the BW-DAC for this design, since the lab instructions did not specifically say we needed to use the R-2R DAC. We also utilized a D-FF (74LS74N) to signal the counter to reverse when the outputs all hit 0000 or 1111. Since the ~RCO on the 74LS169N is active LOW, we need to have an inverter between ~RCO on the counter and 1D on the D-FF to enable the D-FF to trigger properly. In Figure 13, we can see the finished circuit. Then, in Figure 14, we can see the expected output voltage stair stepping up and down, in yellow.

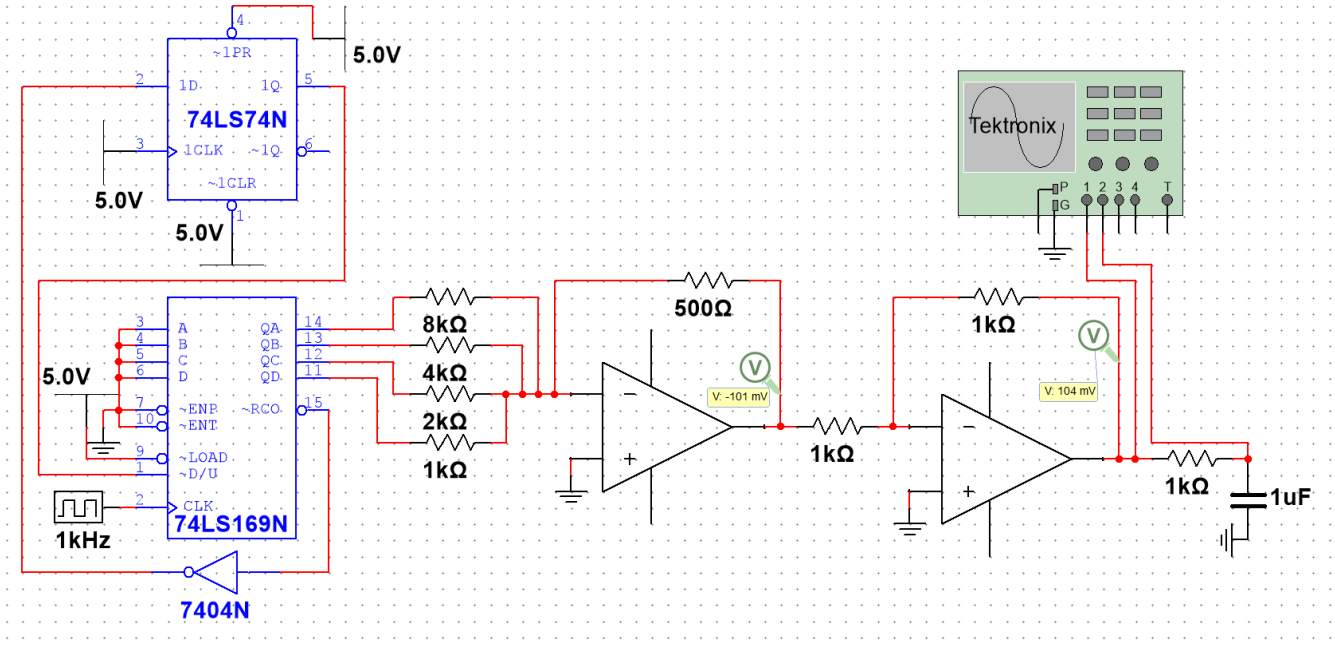

Figure 13: 4-bit BW-DAC with additional circuitry to cause count up/down

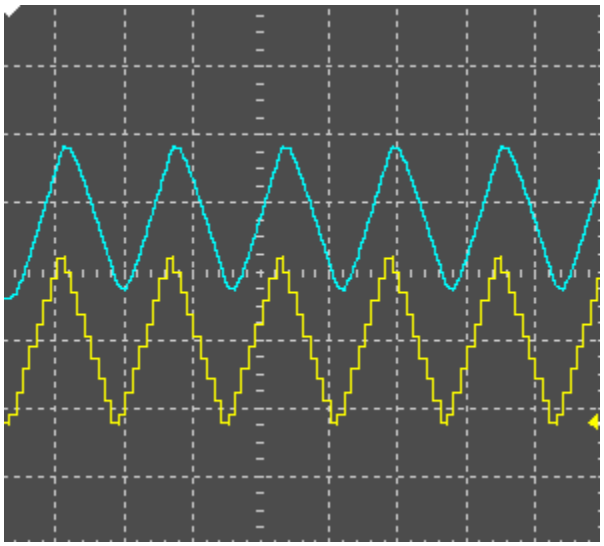

Figure 14: 4-bit BW-DAC with count up/down
Oscilloscope Output Voltage, Probe 1 (Yellow)
Output at Smoothing Cap, Probe 2 (Blue)

Conclusion

This was a very interesting lab to do and see how we can convert digital signals to analog signals. This is a very important aspect to know in digital logic. The need to convert both ways is important, especially since newer devices run off mostly digital signals, but still require analog signals internally to make everything work properly and efficiently.

When we compare the performance of both the BW-DAC and R-2R DAC, we can see that the BW-DAC is more reliable with a more predictable output, while the R-2R DAC requires less space since it is driven by only resistors and consumes less power since we do not need OP AMPs to run it.

In Figure 6, we can see a smoother, more consistent stair step from the BW-DAC, making it more reliable. We do also have errors in the BW-DAC that would need to be addressed, with the sudden drop and rise in voltage at the top of the stair step. This would increase the size, complexity and cost of the device, as well as the power consumption.

In Figure 12, we can see the R-2R DAC causes spikes in the output voltage that could cause errors depending on what it is fed into. We could add additional circuitry to fix these errors, but that would increase the size, complexity and cost of the device, as well as possibly causing more power consumption depending on what components are used.

Both the BW-DAC and R-2R DAC have their errors that need addressing. We would need to weigh our options when deciding which one is better to use and what errors are within an acceptable range for the device we are using. We would also want to evaluate the size, complexity and cost we are allowing within our design in addition to the power consumption.