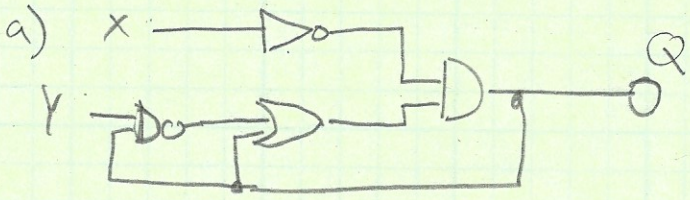
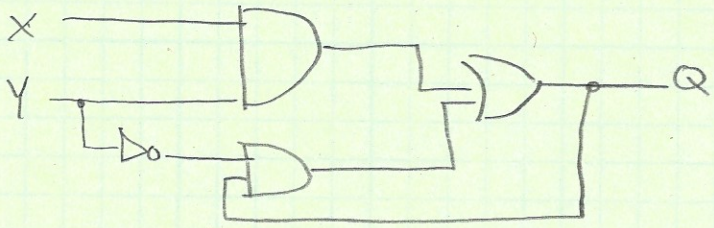
Given:

a)



b)

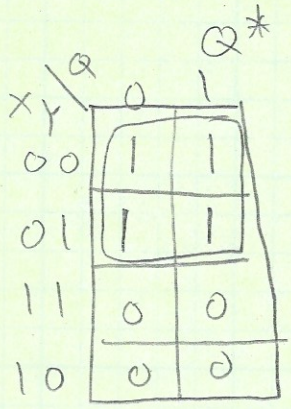


Find: Excitation table for a) & b). Simplify equations, if possible and comment on the effect of feedback

Solution

a)

Q	X	Y	Q*
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

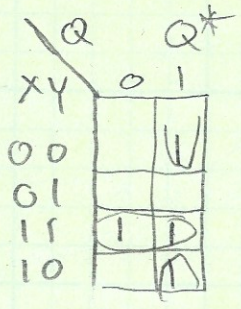


$$Q^* = \overline{X}$$

The feedback has no effect on Q*

b)

Q	X	Y	Q*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



$$Q^* = Q\overline{Y} + XY$$

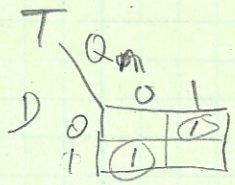
The feedback Q forces Q* to High unless X=0 & Y=1, meaning Q has the largest impact on the functionality of the circuit

Given: T-FF w/ EN & combinational logic

Find: Design a DFF. Show work and include schematic

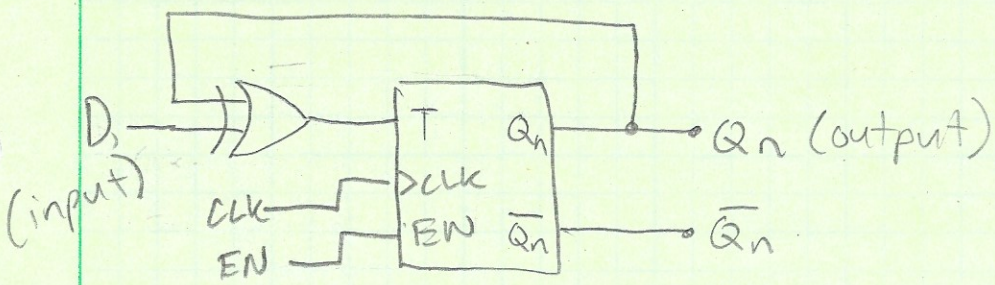
Solution:

D	Q_n	Q^*	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

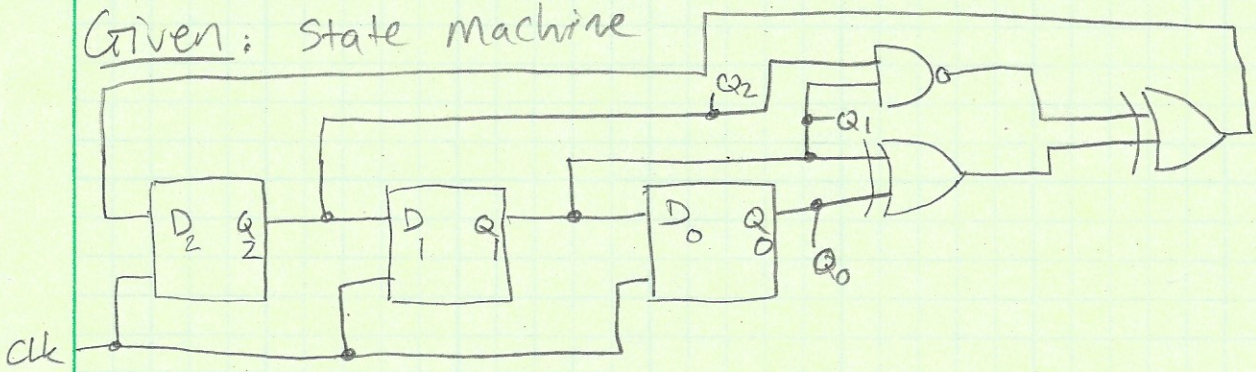


$T = \bar{D} Q_n + D \bar{Q}_n$

$\boxed{T = D \oplus Q_n}$



Given: State machine



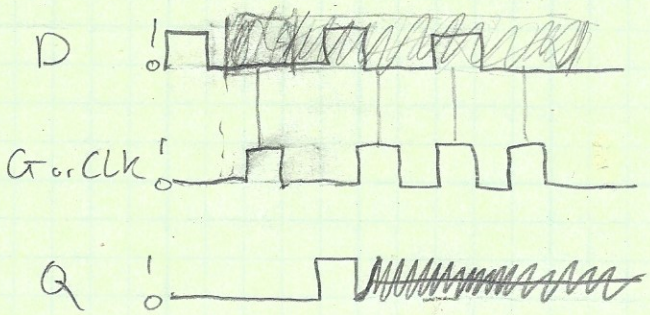
Find: excitation equations & state transition table

Solution: $D_0 = Q_1$ & $D_1 = Q_2$ & $D_2 = (Q_0 \oplus Q_1) \oplus \overline{(Q_1 Q_2)}$

Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1

Given: / Find: Determine and discuss a situation where the ouput of a D-Latch may become metastable. To what timing specification of a D-Latch does this situation relate?

Solution: If the CLK pulses too fast, it will cause a constant setup- & hold-time window, which will send Q output into metastability until the CLK slows down.



Metastability can also happen with high frequency circuits, which is more common nowadays and why dynamic latches are more widely used.