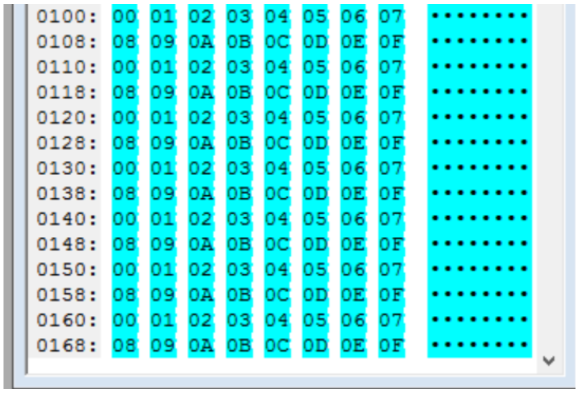
Given: Using VMLAB, write AVR that generates a multiplication table for SRAM addresses 0x0100 to 0x01FF. The value at each address is the product of the two least significant nibbles of the address. For example, at address 0x0123 the multiplicand is 3 and the multiplier is 2. Calculate the product (6 in this case) and store it at address 0x0123.

Find: AVR multiplication table described above
Solution:

AVR Code

```
.include "C:\VMLAB\include\m168def.inc"
ldi r27, 0x01
ldi r26, 0x00
ldi r30, 0xff
main:
mov r16, r26
andi r16,0x0f
mov r17,r27
andi r17,0xf0
swap r17
mul  r17, r16
st x+, r16
dec r30
brne main
```

Screenshot of affected SRAM memory after code runs



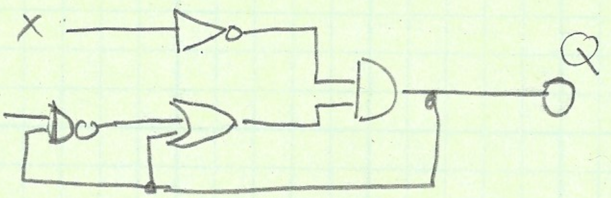
```
0100: 00 01 02 03 04 05 06 07  ........
0108: 08 09 0A 0B 0C 0D 0E 0F  ........
0110: 00 01 02 03 04 05 06 07  ........
0118: 08 09 0A 0B 0C 0D 0E 0F  ........
0120: 00 01 02 03 04 05 06 07  ........
0128: 08 09 0A 0B 0C 0D 0E 0F  ........
0130: 00 01 02 03 04 05 06 07  ........
0138: 08 09 0A 0B 0C 0D 0E 0F  ........
0140: 00 01 02 03 04 05 06 07  ........
0148: 08 09 0A 0B 0C 0D 0E 0F  ........
0150: 00 01 02 03 04 05 06 07  ........
0158: 08 09 0A 0B 0C 0D 0E 0F  ........
0160: 00 01 02 03 04 05 06 07  ........
0168: 08 09 0A 0B 0C 0D 0E 0F  ........
```

I cannot get it to work. I worked on this, with Ken and some others in the class, for multiple days and this is all we could come up with. It seems to multiply the 3rd and 1st least significant nibble in the first 2 rows, then repeat itself. We didn't do AVR in 2013/2014 when I took 171. It was not apart of the curriculum, so I tried my hardest on this and this is the farthest I could get.

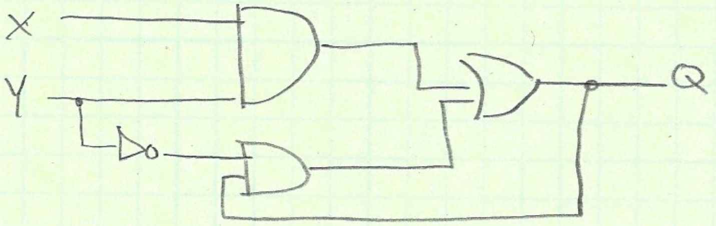
ENGR 271 HW#1 Problem #2 | Philip Nevins

Given:

a)



b)



Find: Excitation table for a) & b). Simplify equations, if possible and comment on the effect of feedback

Solution

a)

Q	X	Y	Q*
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Q*

XY \ Q	0	1
00	1	1
01	1	1
11	0	0
10	0	0

$$\boxed{Q^* = \overline{X}}$$

The feedback has no effect on Q*

b)

Q	X	Y	Q*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Q*

XY \ Q	0	1
00		1
01		
11	1	1
10		1

$$\boxed{Q^* = Q\overline{Y} + XY}$$

The feedback Q forces Q* to High unless X=0 & Y=1, meaning Q has the largest impact on the functionality of the circuit

Given: T-FF w/ EN & combinational logic

Find: Design a DFF. Show work and include schematic

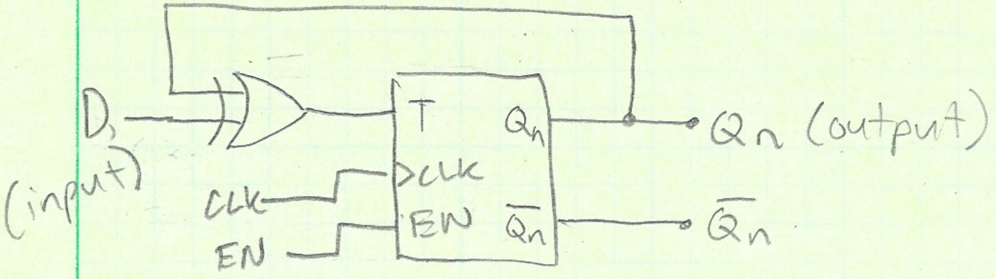
Solution:

D	Q_n	Q^*	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

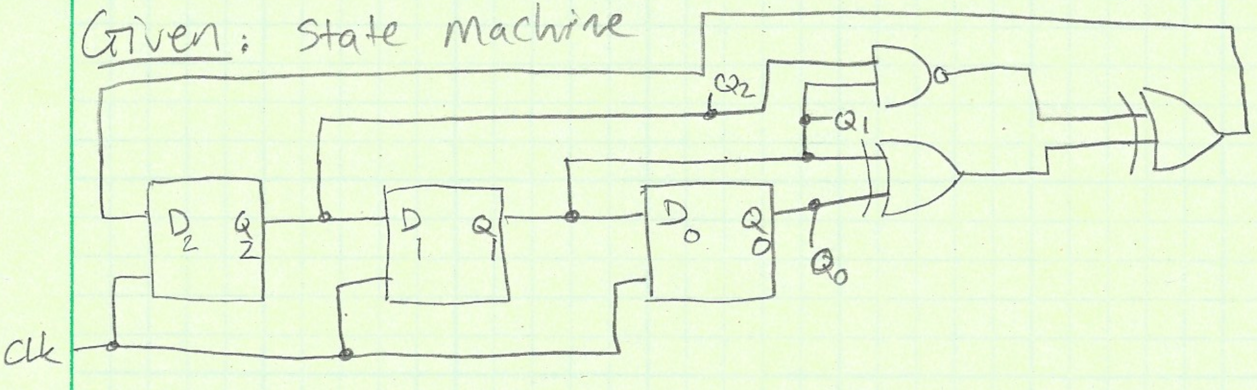
T: D \ Q_n	0	1
0		1
1	1	

$$T = \bar{D} Q_n + D \bar{Q}_n$$

$$\boxed{T = D \oplus Q_n}$$



Given: State machine



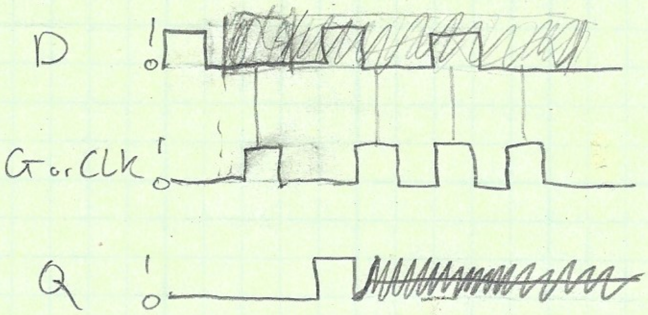
Find: excitation equations & State transition table

Solution: $D_0 = Q_1$ & $D_1 = Q_2$ & $D_2 = (Q_0 \oplus Q_1) \oplus \overline{(Q_1 Q_2)}$

Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1

Given: Find: Determine and discuss a situation where the ouput of a D-Latch may become metastable. To what timing specification of a D-Latch does this situation relate?

Solution: If the CLK pulses too fast, it will cause a constant setup- & hold-time window, which will send Q output into metastability, until the CLK slows down.



Metastability can also happen with high frequency circuits, which is more common now adays and why dynamic latches are more widely used.