Given: Design an 8-bit ring counter using only 2 74xx ICs and no other components

Find:

Solution:

I decided to use 2 74194N ICs. Using these, we can set Q_A (left most LED in example) to L and then shift that through the 74194N, using this line from the datasheet.

CLR	S1	S0	CLK	SL	SR	A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	L	H	↑	X	L	X	X	X	X	L	Q_{AN}	Q_{BN}	Q_{CN}

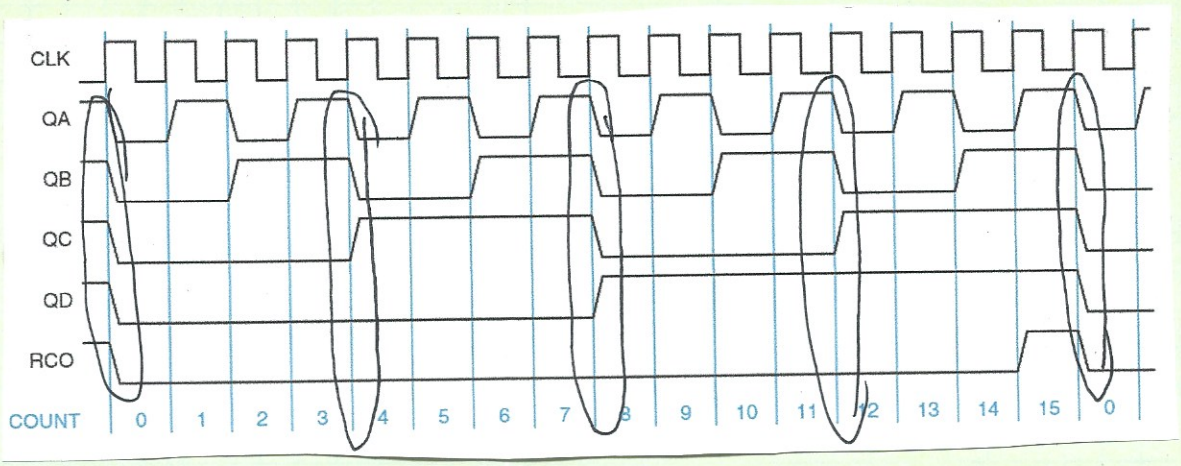
This will account for the first 4 LEDs. The next 4 can be done using another 74194N, with Q_D from #1 tied to SL+SR of #2. This was simulated in Multisim. I had to initialize all LEDs on, then "push" the switch twice to initiate the shift of the L through from the table above.

The schematic is on page 3

Given: Consider the divide by 16 counter timing diagram below.

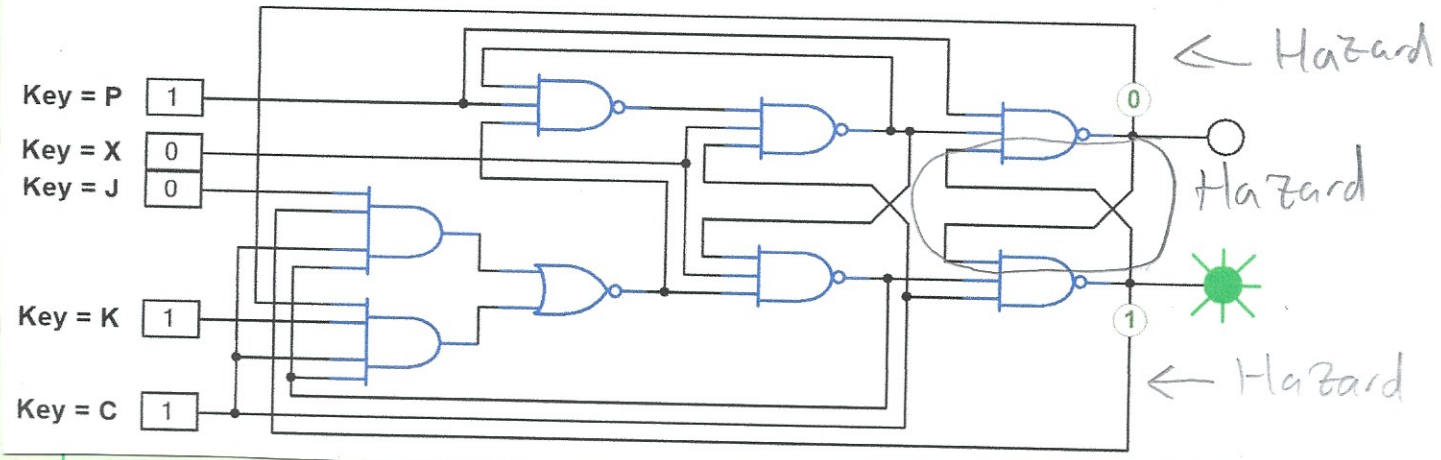
Find: Glitches for RCO? list them & explain

Solution: The 5 circled transitions are glitches. We know that when 2+ bits outside of $Q_a + Q_b$ transition at the same time, it is a potential glitch point. This is shown to us in the reading, on page 560, figure 11-9. These points are when we have 2+ transitions at the same time, outside $Q_a + Q_b$.



4. One day you decide to have some fun and put together your own JK flip-flop based on the 74109 IC. But during testing you find that the circuit goes into the wrong state because of a timing delay in one of the feedback loops (aka an essential hazard).

   From the following schematic identify where an essential hazard could be, simulate it and determine the minimum delay that causes the error. (The schematic shows the JKFF in hold mode.)



Solution: I simulated this in Multisim [schematic #1 on page 6]. Since the hazard shows up on "Stage 4" [U3A & U5A], you need to change the rise/fall delay to delay stage 4 until all other stages settle. All components, by default, have a rise/fall delay of 22n/15n. So to eliminate the hazard on stage 4, we need to change the r/f delay of stage 4 to delay until stage 1-3 settles, which is 3x stage 4 r/f delay, 66n/45n. Once the delay is changed, we run the simulation and clock any of the digital inputs and we have success! This can be seen on schematic #2

Given: Design a clocked synchronous circuit with four inputs, N3, N2, N1 and N0 that represent the integer N in the range 0-15. The circuit has a single output Z that is HIGH for exactly N clock ticks during any 16-tick interval. Include a schematic in your answer. (Hints: use a free-running 4-bit counter IC and combinational logic to decode the N bits. The ticks in which Z is HIGH should be spaced as evenly as possible. For example, every second tick when N = 8, every fourth when N = 4, and so on.)

Find:

Solution: