Given: Write AVR instructions that put the ASCII value for your initials (PN) starting at SRAM memory address 0x0100

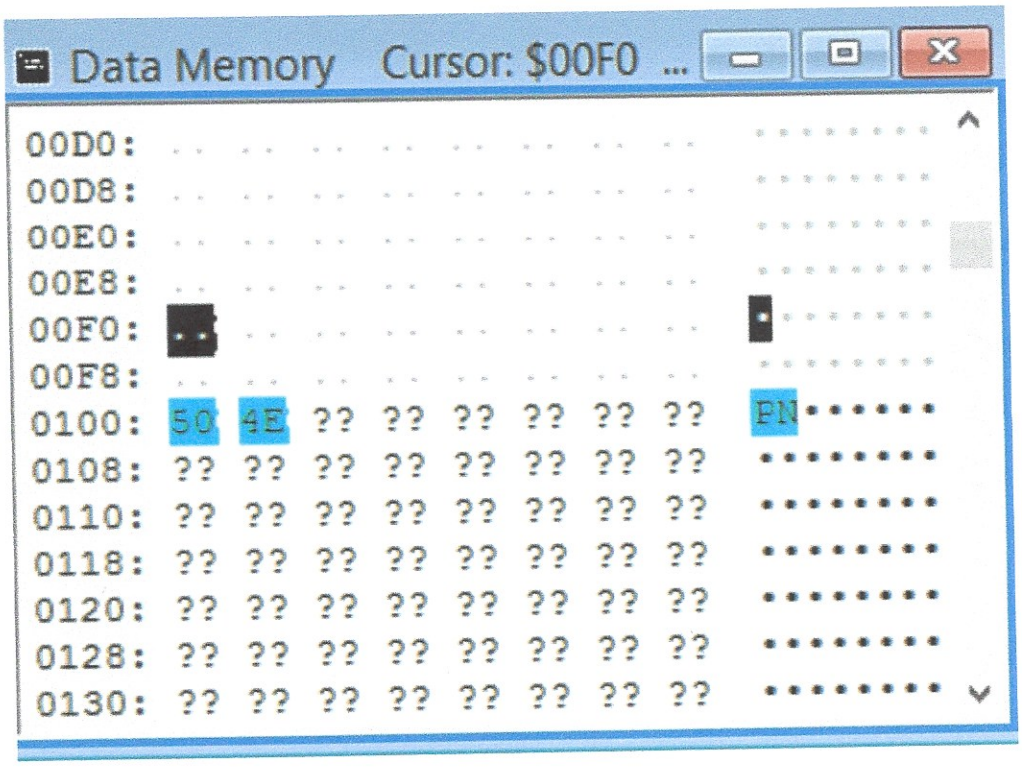
Find: ASCII value for PN, write code to insert this ASCII value into SRAM 0x0100

Solution:

AVR Code

```
clr r26
clr r27
ldi r26, 80
ldi r27, 78
sts 0x0100, r26
sts 0x0101, r27
```

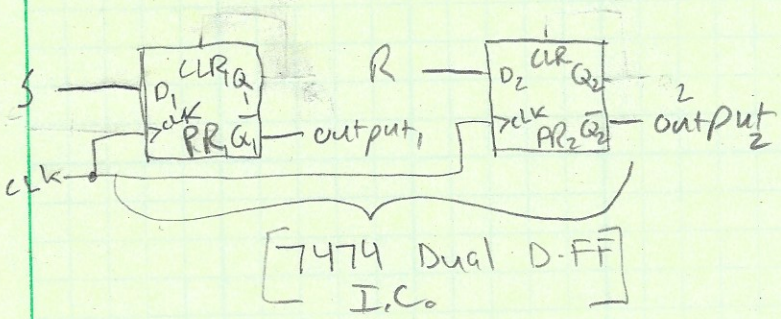
Screenshot of affected SRAM memory after code runs



Given: One 7474 D-Flip Flop

Find: Design an SR-Latch using only the given components

Solution:



7474 I.C. T-Table 1

D	CLK	Q	$\bar{Q}$
0	↑	0	1
1	↑	1	0
X	0	[last Q]	[last $\bar{Q}$]
X	1	[last Q]	[last $\bar{Q}$]

when CLR is 1, Q $\bar{Q}$ is 0 0

SR-Latch T-Table 2

S	R	Q	$\bar{Q}$
0	0	Last Q	Last $\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

T-Table 3, Above Setup

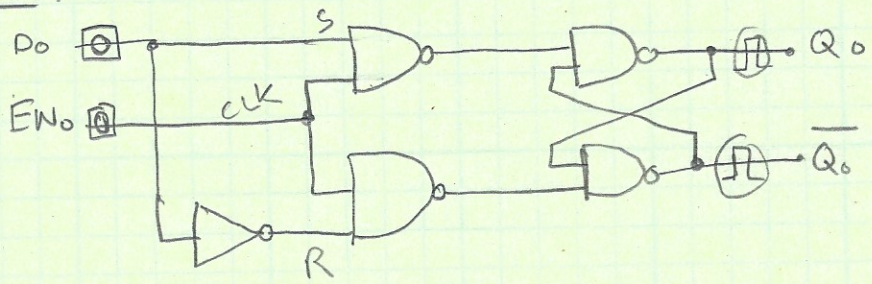
	S	R	CLR_1	CLR_2	Q_1	$\bar{Q}_1$	Q_2	$\bar{Q}_2$
clk ↑	0	0	1	1	0	1	0	1
	0	1	1	1	0	1	1	0
	1	0	1	1	1	0	0	1
	1	1	1	1	0	1	1	0
0	X	X	0	0	[Last Q]	[Last $\bar{Q}$]	[Last Q]	[Last $\bar{Q}$]
1	X	X	0	0	[Last Q]	[Last $\bar{Q}$]	[Last Q]	[Last $\bar{Q}$]

Reading outputs @ $\bar{Q}$, we have

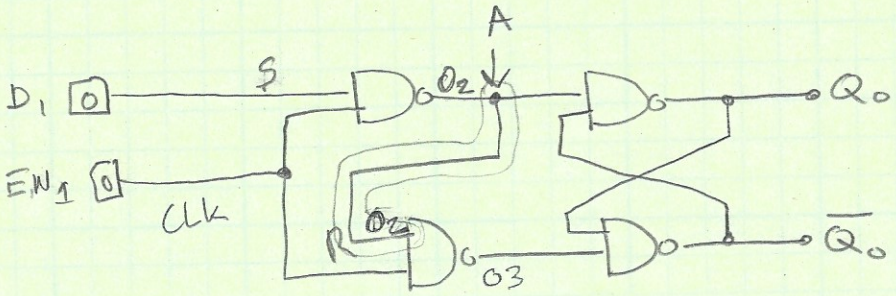
S	R	$\bar{Q}_1$	$\bar{Q}_2$	
0	0	1	1	→ last Q state
0	1	1	0	
1	0	0	1	
1	1	0	0	

Given:

1]



2]



Find: Compare functionality of the two sequential circuits shown. Which one performs better and why?

Solution: #1 is an SR FF, which we have seen in the book and in lecture.

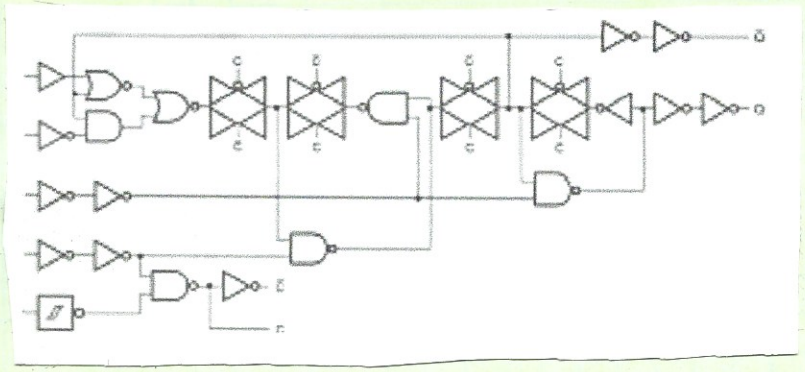
#2

D_1	EN1 = EN2	O_2	O_3		
0	0	0	1	1	X
0	1	1	1	0	
1	0	0	1	1	X
1	1	1	0	1	

we only have 2 valid states on #2, which also makes it SR FF

#1 will perform better because #2 will have a longer propegation delay @ circled point A which can cause major issues if not adjusted for. Assuming all I.C.s are normal, out of the box, we can assume this prop delay will cause issues.

Given:



Find: Analyze FF circuit shown. Determine and briefly describe the function of each input.

solution:

The circuit shown is a Jk Flip Flop with set, reset, and clock

Input	Function
V	J
W	K
X	set
Y	reset
Z	Clock (Smitd Trigger)
"C"	Passgate

V & W are inputs for the passgates that act as J & k inputs from a Jk FF

X is a set for the passgate

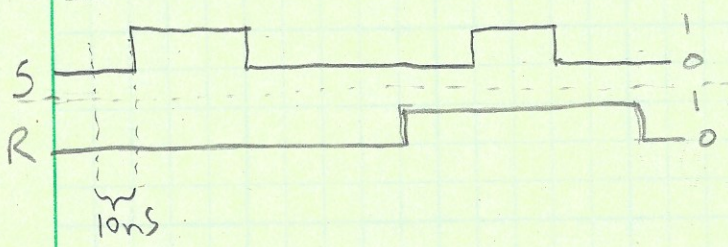
Y is a reset for the passgate

Z acts as an active low clock since a smitd trigger does an inversion, and feeds into the passgates as clk

This was determined from how passgates and Smitd triggers operate.

Problem 10.8

Given:

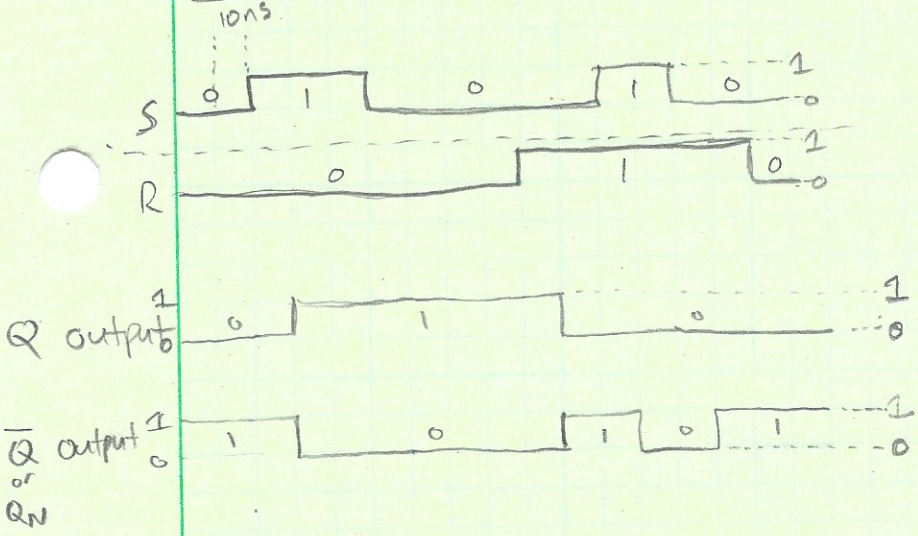


} Figure X 10.8

Find: Outputs of a SR-Latch [made with NOR Gates] for the given input waveforms shown in Figure X 10.8.

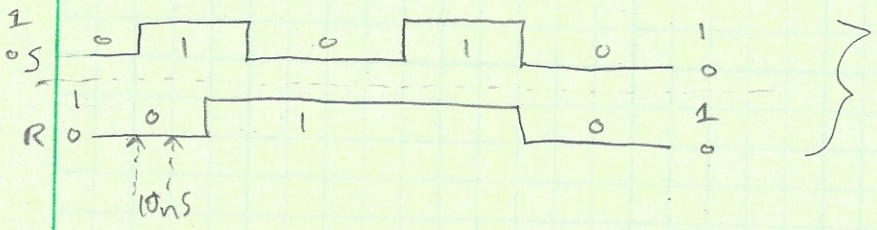
Assume: inputs & outputs rise & fall times are zero.
propegation delay of a NOR = 10nS
time division = 10nS

Solution:



Problem 10.9

Given:

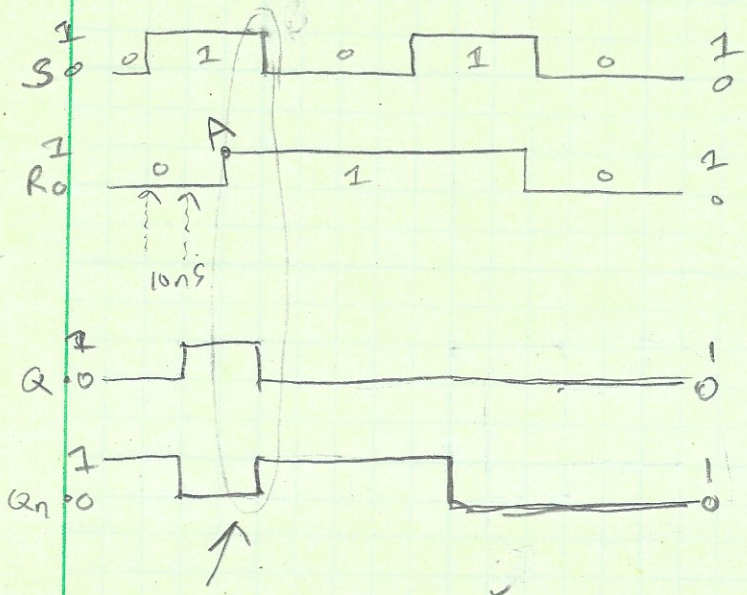


} Figure x10.9

Find: Outputs of a SR-Latch [made with NOR Gates] for the given input waveforms shown in Figure x10.9

Assume: I/O rise & fall times = 0
Propegation delay of NOR = 10ns
Time division = 10ns

Solution:



This is the point that seems impossible!

@ S=1, R=1, the truth table says $Q = Q_n = 0$ but with prop delay, this "skips"?