

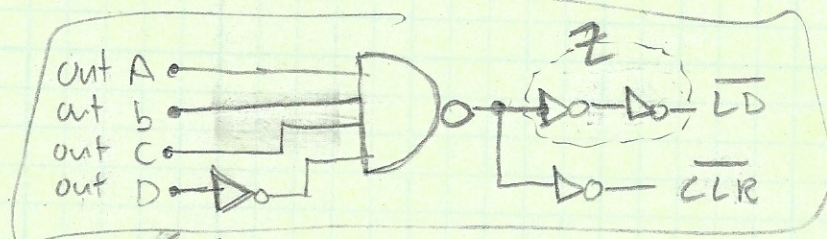
Given: Use a 74163 IC & any other combinational logic required to design a counter circuit that counts the following 11 states. 4, 5, 6, ..., 13, 14, 4

Find: Design counter [modulo-11]

Solution:

Modulo-11

(4)	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110



(when out = 1110, triggers 0  $\rightarrow$   $\overline{LD}$ , triggers 1  $\rightarrow$   $\overline{CLR}$ )

in C — VCC

From datasheet, when  $\overline{LD} = 0$  &  $\overline{CLR} = 1$ , it's the preset data mode, & it loads ABCD. Since 4 (0100) is lowest #, C  $\rightarrow$  VCC.

This also matches with doing the math to calculate modulo-11  $\Rightarrow$  (output) - (VCC input ties)  
 $15 - 4 = 11 \checkmark$

We can also put 2 inverters (Z) to ensure  $\overline{CLR}$  triggers first, then the 1s value is loaded.



Given: create an unambiguous state diagram for "sticky counter" state machine, with  $S_0$ - $S_7$ . Besides CLK, inputs  $\rightarrow$  RST, EN and output - DONE. Machine goes to  $S_0$  when RST is High. RST  $\&$  AND EN  $\rightarrow$  next state. Once it gets to  $S_7$ , stays unless RST = 1. DONE = 1 if only in state  $S_7$  & EN = 1.

Find: State Diagram

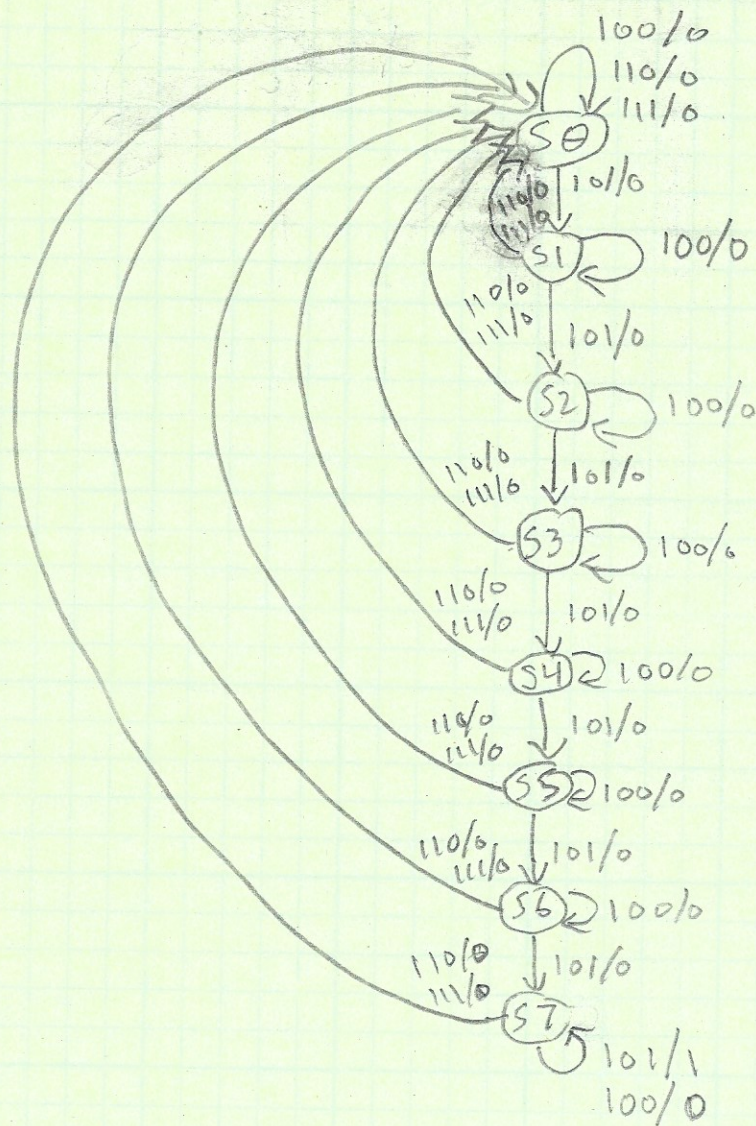
Solution:

RST = 1, EN = 0  $\rightarrow$  next state  $S_0$   
 $S_7$ , RST = 0  $\rightarrow$  next state  $S_7$   
 $S_7$ , EN = 1  $\rightarrow$  DONE = 1

INPUT: RST, EN  
 CLK

Output: DONE

values: CLK/RST/EN/  
 DONE





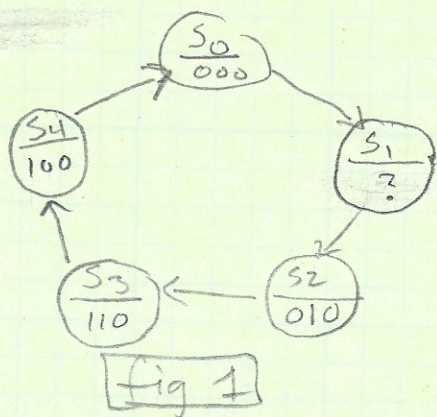
Given: Consider adjacency diagram w/ odd # states in a ring. If min. # state bits is used, is it possible to assign state bits w/o critical racing signals?

Find:

Solution: Let's consider 3 states, 2 qbits.

We set  $S_0 = 00$ ,  $S_1 = 01$  so we have no racing errors. If we set  $S_2 = 11$  to have no racing error at  $S_1 \rightarrow S_2$ , we have one at  $S_2(11) \rightarrow S_0(00)$ . If we set  $S_2 = 10$ , we have a racing error at  $S_1(01) \rightarrow S_2(10)$ .

Let's consider 5 states, 3 qbits.



We set  $S_0, S_2-4$  as follows in fig 1. Our only options open are 001, 011, 101, 111. To eliminate racing error  $S_0 \rightarrow S_1$ ,  $S_1 = 001$  only. All other options put a racing error  $S_0 \rightarrow S_1$ .

Now (001) won't work to eliminate racing errors at  $S_1(001) \rightarrow S_2(010)$ . This instance of having 1 racing error always occurs when we have an odd # of states.



Given: Design a counter w/ Jk FF to produce the following binary sequence: 9, 12, 11, 13, 15, 14, 10, 9...

Find: Design counter (show all design procedure steps)

Solution: Largest # = 15  $\Rightarrow$  1111  $\therefore$  we need 4 FFs

	Present				Next				$J_4$ $K_4$		$J_3$ $K_3$		$J_2$ $K_2$		$J_1$ $K_1$	
	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$Q_4^*$	$Q_3^*$	$Q_2^*$	$Q_1^*$								
9	1	0	0	1	1	1	0	0	X	0	1	X	0	X	X	1
12	1	1	0	0	1	0	1	1	X	0	X	1	1	X	1	X
11	1	0	1	1	1	1	0	1	X	0	1	X	X	1	X	0
13	1	1	0	1	1	1	1	1	X	0	X	0	1	X	X	0
15	1	1	1	1	1	1	1	0	X	0	X	0	X	0	X	1
14	1	1	1	0	1	0	1	0	X	0	X	1	X	0	0	X
10	1	0	1	0	1	0	0	1	X	0	0	X	X	1	1	X

$P \Rightarrow N$

1  $\rightarrow$  1  $J_X, K_0$

0  $\rightarrow$  1  $J_1, K_X$

$P \Rightarrow N$

0  $\rightarrow$  0  $J_0, K_X$

1  $\rightarrow$  0  $J_X, K_1$

\*Using Jk FF truth table\*

$$J_4 = X, K_4 = 0$$

$J_3$

$Q_4 Q_3$	$Q_2 Q_1$	00	01	11	10
00		0	1	3	2
01		4	5	7	6
11		X	X <sup>13</sup>	X <sup>13</sup>	X <sup>14</sup>
10			1 <sup>9</sup>	1 <sup>11</sup>	10

$$J_3 = Q_4 Q_1$$

$K_3$

$Q_4 Q_3$	$Q_2 Q_1$	00	01	11	10
00					
01					
11		1			1
10			X	X	X

$$K_3 = Q_4 Q_3 \bar{Q}_1$$

$J_2$

$Q_4 Q_3$	$Q_2 Q_1$	00	01	11	10
00					
01					
11		1	1	X	X
10			X		X

$$J_2 = Q_4 Q_3$$

$K_2$

$Q_4 Q_3$	$Q_2 Q_1$	00	01	11	10
00					
01					
11		X	X		
10			X	1	1

$$K_2 = Q_4 \bar{Q}_3 Q_2$$



$J_1$ $Q_4 Q_3$	$Q_2 Q_1$			
	00	01	11	10
00				
01				
11	1	x	x	
10		x	x	1

$$J_1 = Q_4 Q_3 \bar{Q}_2 \bar{Q}_1 + Q_4 \bar{Q}_3 Q_2 \bar{Q}_1$$

$$J_1 = Q_4 \bar{Q}_1 (Q_3 \oplus Q_2)$$

$K_1$ $Q_4 Q_3$	$Q_2 Q_1$			
	00	01	11	10
00				
01				
11	x		1	x
10		1		x

$$K_1 = Q_4 \bar{Q}_3 \bar{Q}_2 Q_1 + Q_4 Q_3 Q_2 Q_1$$

$$K_1 = Q_4 Q_1 (Q_3 \oplus Q_2)$$

