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ENGR 271

Lab 0x9: Iterative Arithmetic Circuits

Introduction

In this lab, 0x9 Iterative Arithmetic Circuits (IACs), we are building and testing two different IACs. One is an iterative multiplier circuit, where two 4-bit numbers are input as a multiplicand and multiplier. Then the circuit outputs an 8-bit product. The other circuit is a divider circuit, which is an iterative divider circuit, where two 4-bit numbers are input as a dividend and divisor. Then the circuit outputs a 4-bit quotient. The divider circuit also outputs a remainder in the form of twos complement, if we have one. We will discuss this more in Part B

Part A: Iterative Multiplier

In this section, we are tasked with building an Iterative Multiplier circuit. Figure 1 shows the base circuit that we copied from the lab instructions. We were tasked with testing that this circuit worked properly. I decided to choose four different test cases, which can be seen in Figure 2. The product is displayed at the top, under P7 - P0

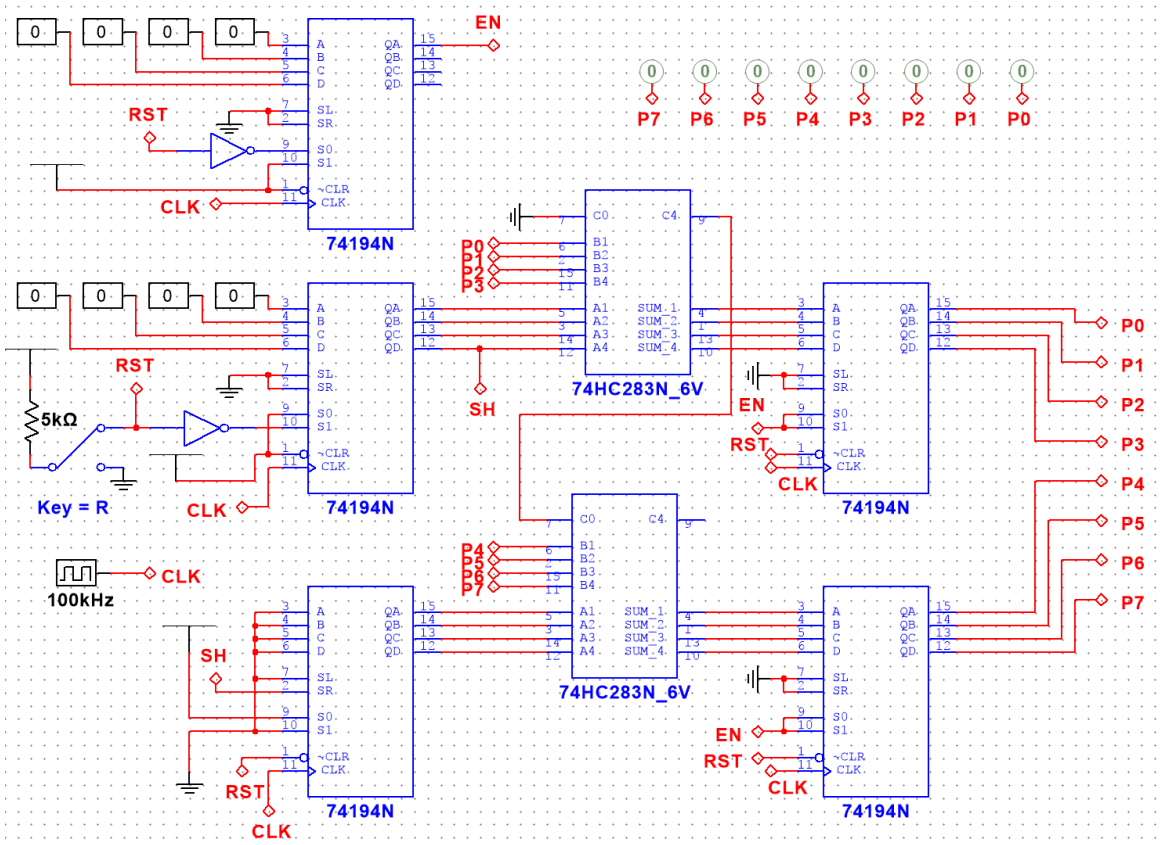

Figure 1: Iterative Multiplier Circuit

Test Case #, Equation	Multiplicand	Multiplier	Product
#1, 2x2 = 4	0010	0010	00000100
#2, 7x6 = 42	0111	0110	00101010
#3, 9x8 = 72	1001	1000	01001000
#4, 5x6 = 30	0101	0110	00011110

Figure 2: Table of Test Cases for Iterative Multiplier

I decided to pick these values for a couple of reasons, The first case is a simple one. The next two (#2 and #3) are progressively higher numbers with a higher multiplicand and multiplier values, that produces different combinations of 0/1's in the product. All test cases were also chosen so there was no overlap in the multiplicand and multiplier, to ensure proper operation. Below, in Figure 3a-d, you can see each test case produces the proper product.

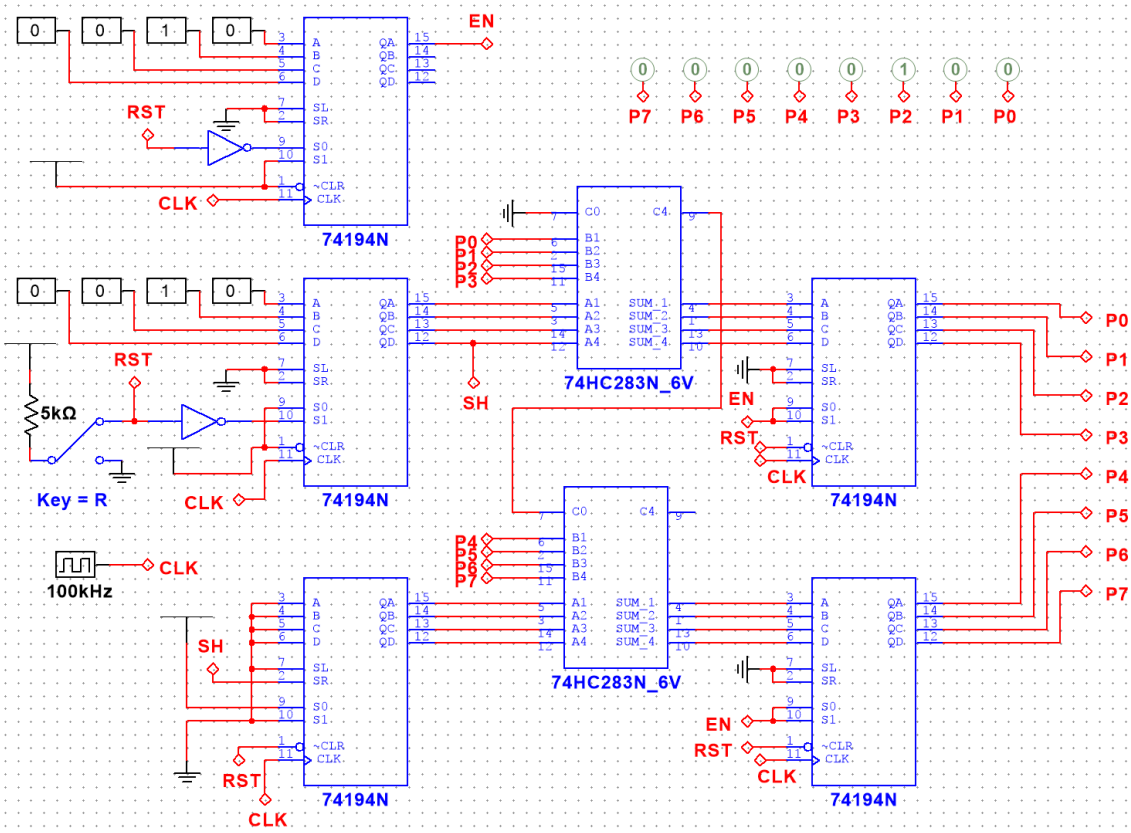

Figure 3a: Test Case #1

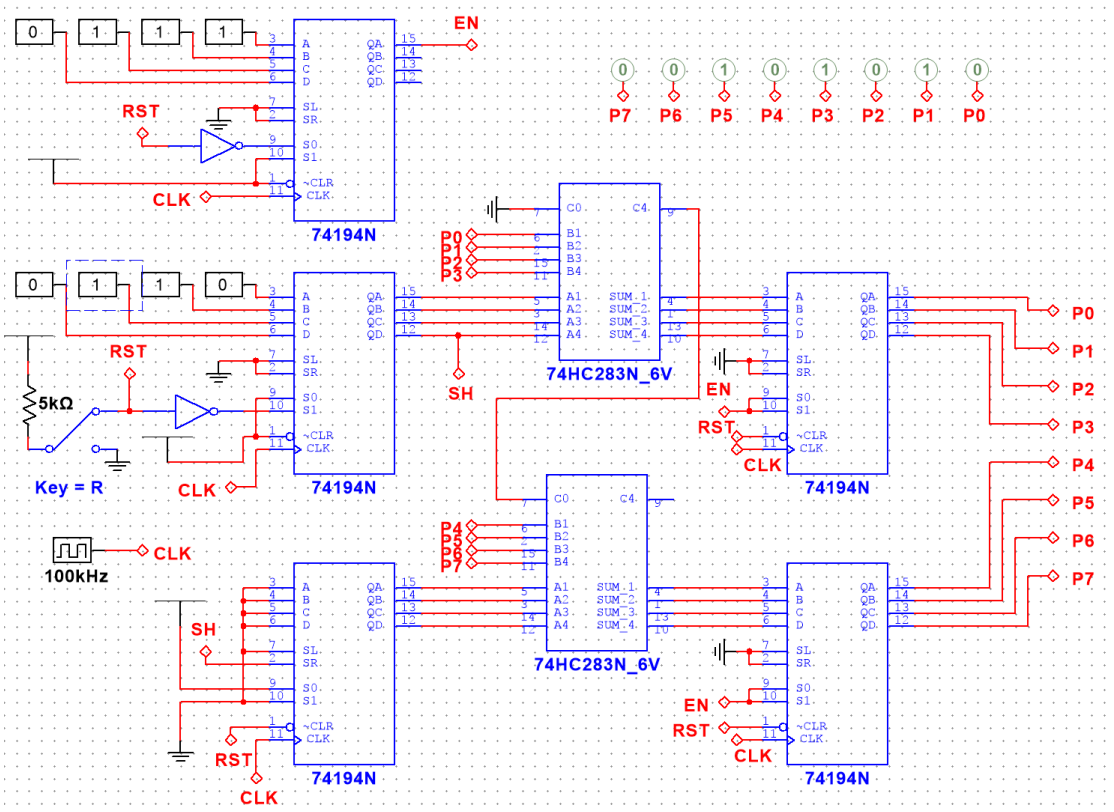

Figure 3b: Test Case #2

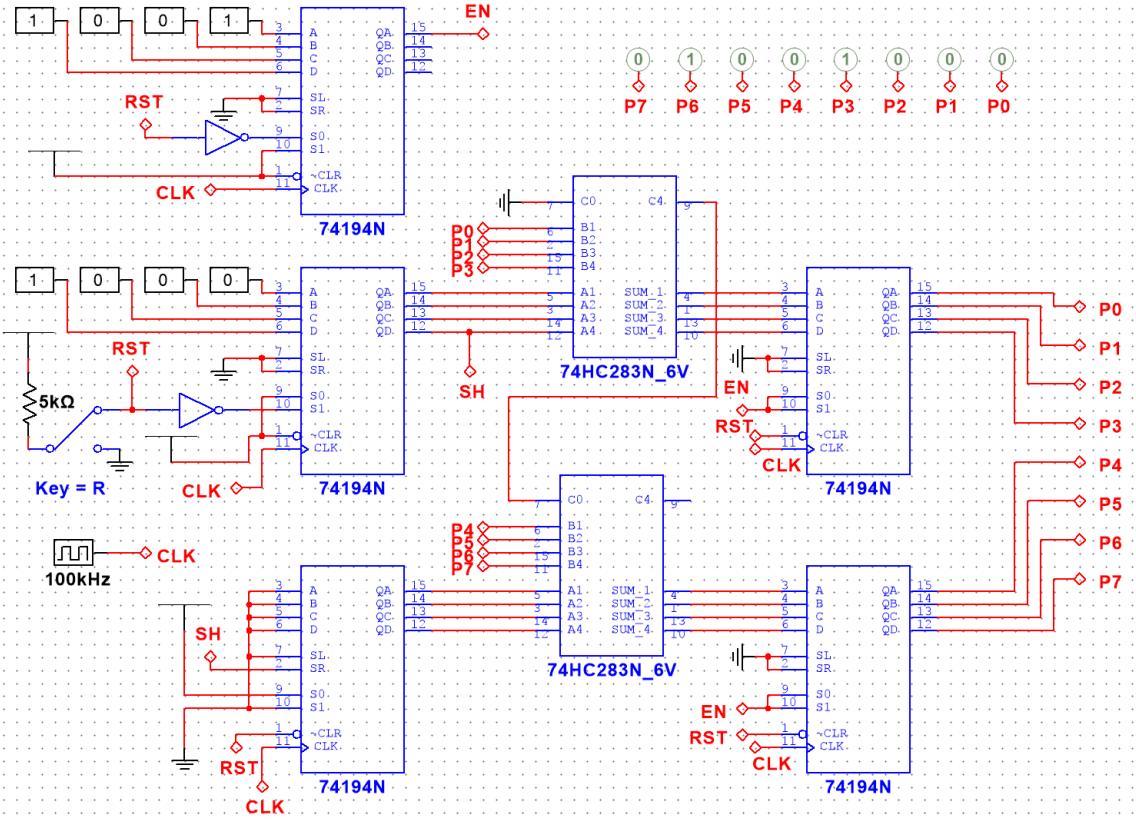

Figure 3c: Test Case #3

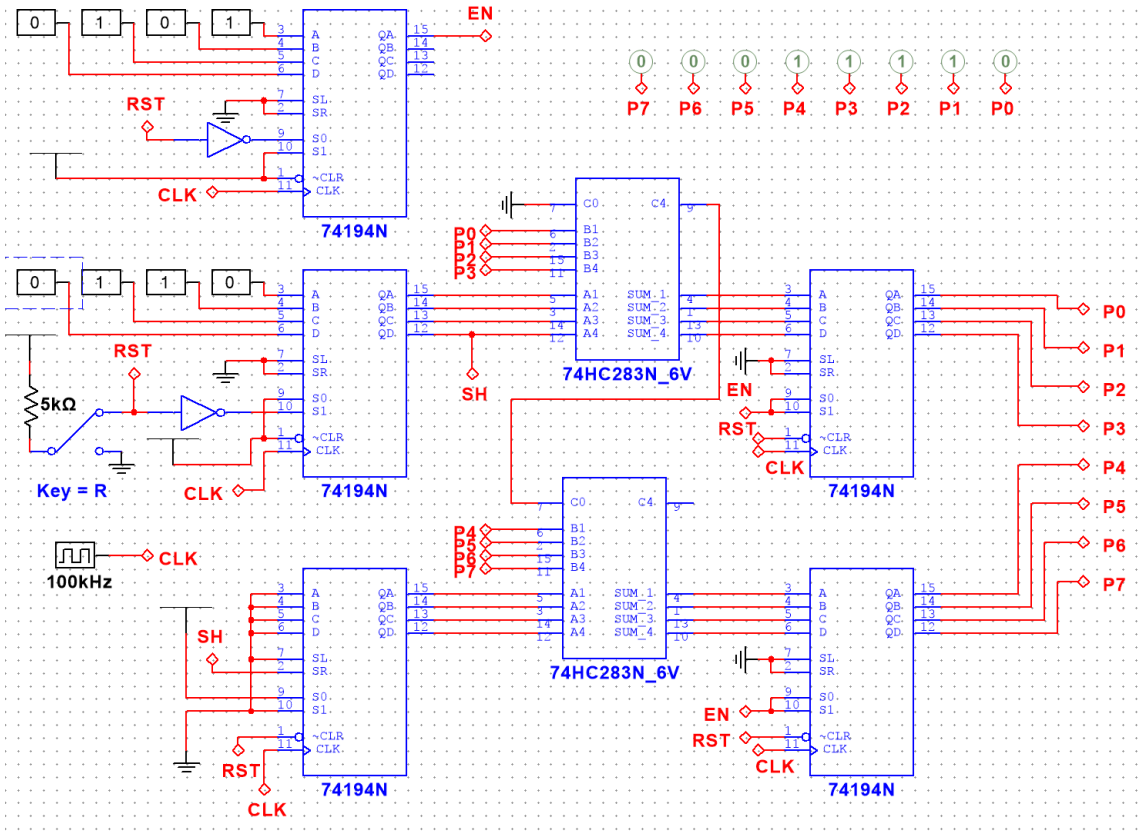

Figure 3d: Test Case #4

It is not possible to reduce the number of ICs in this design without reducing the number of multiplicand and multiplier bits. One example to prove this, is a test case of 15x15 = 225. 225 in binary is 11100001. If we remove any of the ICs, we would have to reduce the number of multiplicand and multiplier bits, as well as the product bit, and we wouldn't have enough bits on the product to display the maximum possible product of 15x15 = 225 (11100001)

Part B: Iterative Divider

In this section, we are tasked with building an Iterative Divider circuit. Figure 4 shows the base circuit that we copied from the lab instructions. We were tasked with testing that this circuit worked properly. I decided to choose four different test cases, which can be seen in Figure 5. Each test case has no remainder, to show that the circuit works properly. Later in this section, I explain step-by-step as to how this circuit works, as well as where the remainder, if there is one, shows up in the circuitry. We do not need extra circuitry to display this, we just need to display the 0/1 from a specific location. The Quotient is displayed on the output of the top 74194N, at QA - QD, with QA being the MSB and QD being the LSB. The top 4-bit input is the dividend (IC1) and the second 4-bit input is the divisor (IC2).

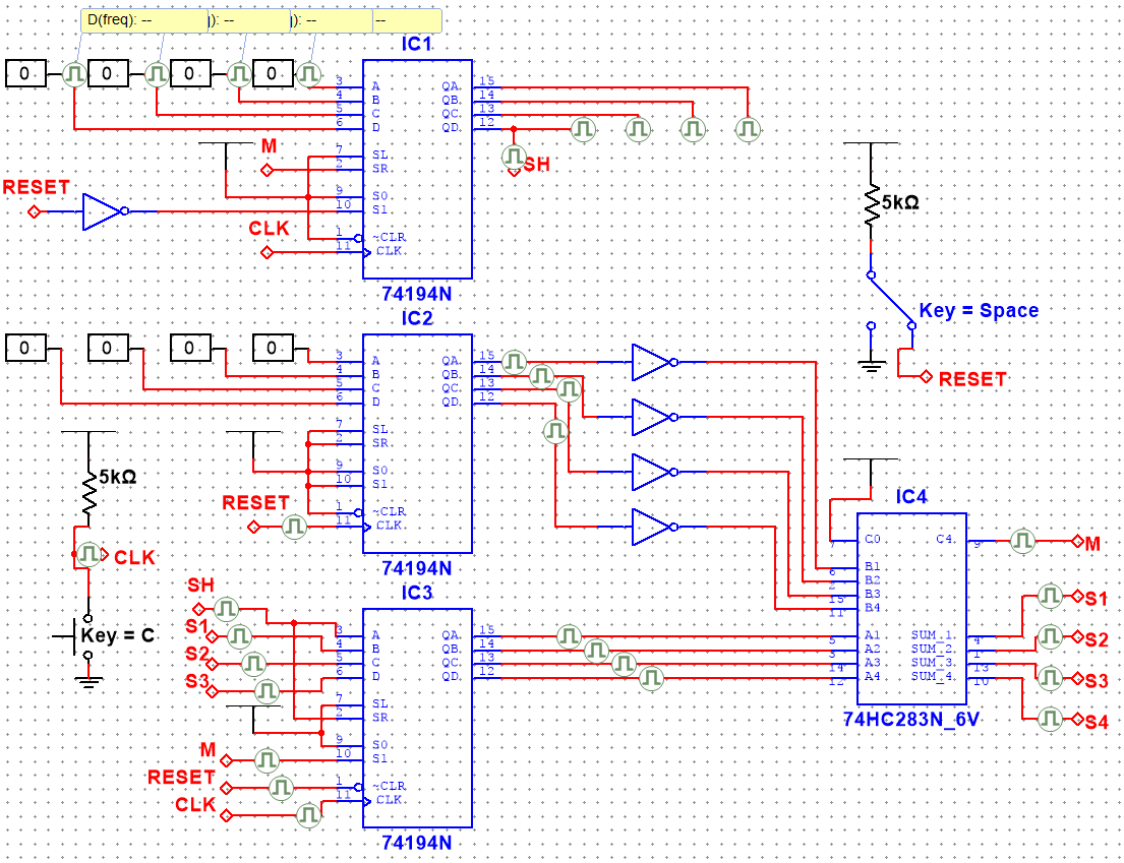

Figure 4: Iterative Divider Circuit

Test Case #, Equation	Dividend	Divider	Quotient
#1, 2/2 = 1	0010	0010	0001
#2, 10/3 = 3	1010	0011	0011
#3, 15/3 = 5	1111	0011	0101
#4, 12/3	1100	0011	0100

Figure 5: Table of Test Cases for Iterative Divider

Below in Figure 6a1/2 - d1/2, you can see each test case with the corresponding quotient. After this section, I will explain how it works step-by-step. Figure 6a1 will show the test case being loaded into the Quotient section (load) and then 6a2 will show the Quotient answer (answer).

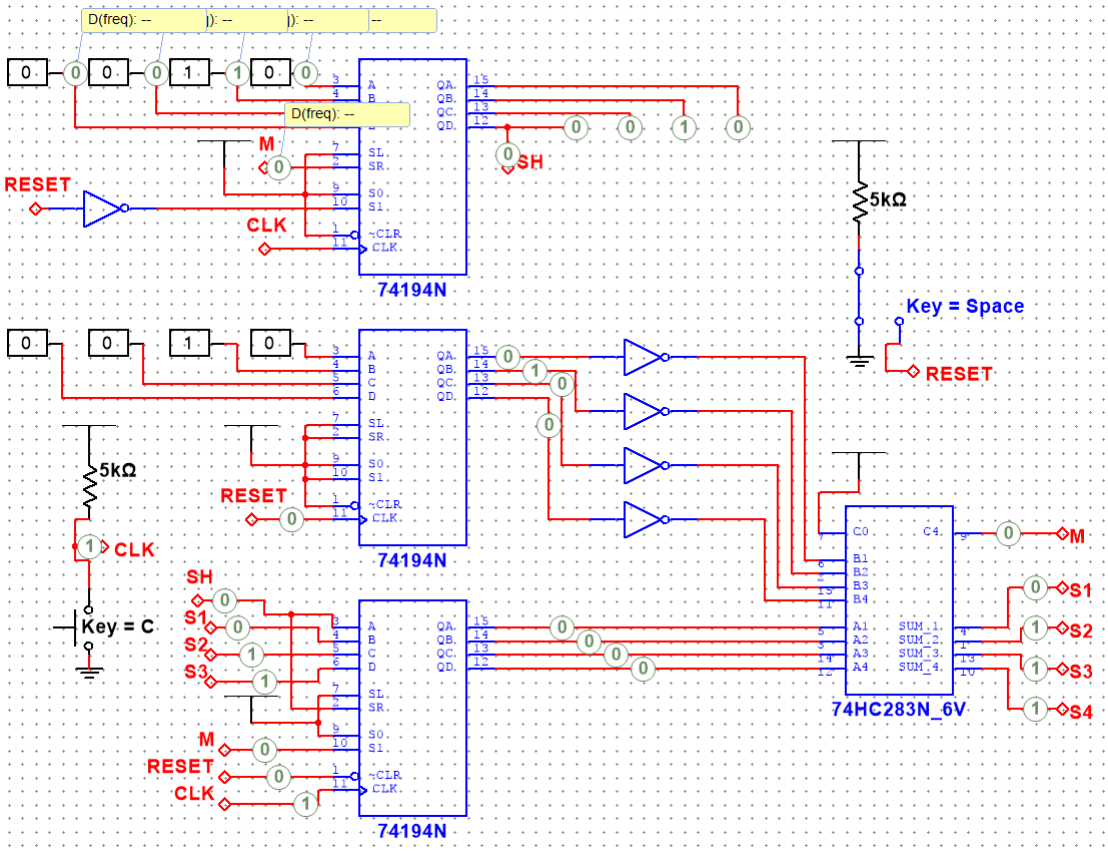

Figure 6a1: Test Case #1, Load

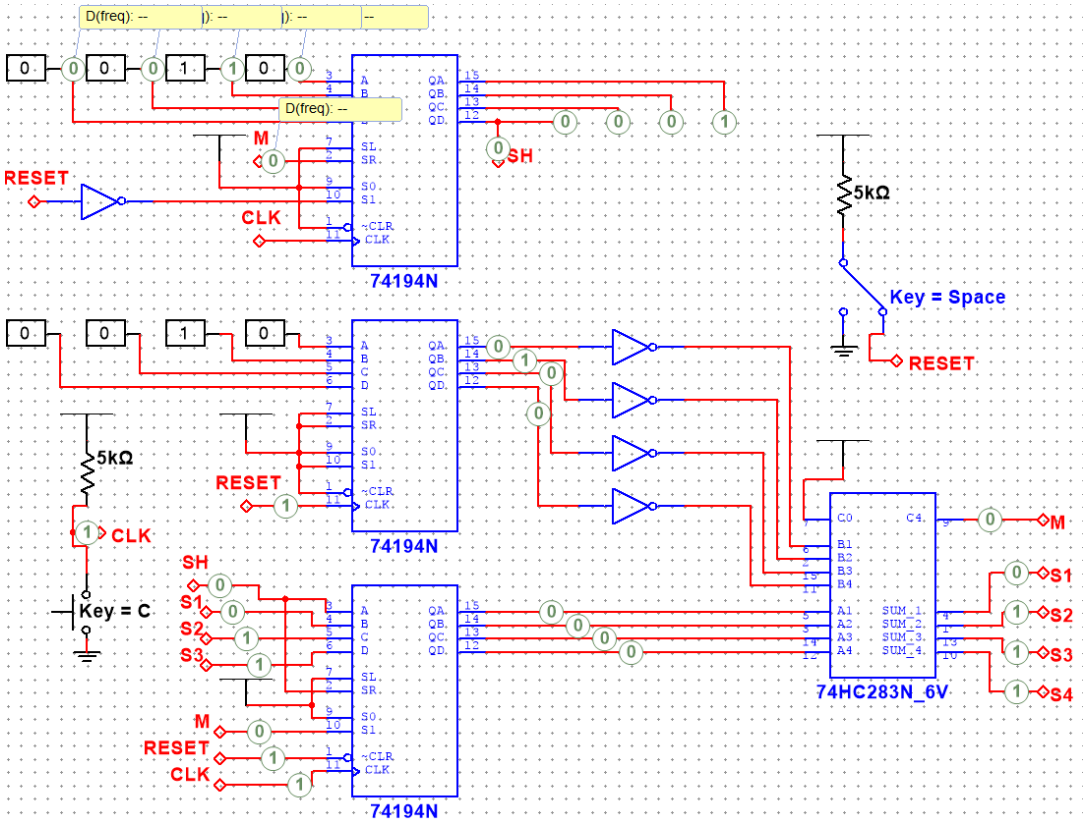

Figure 6a2: Test Case #1, Answer

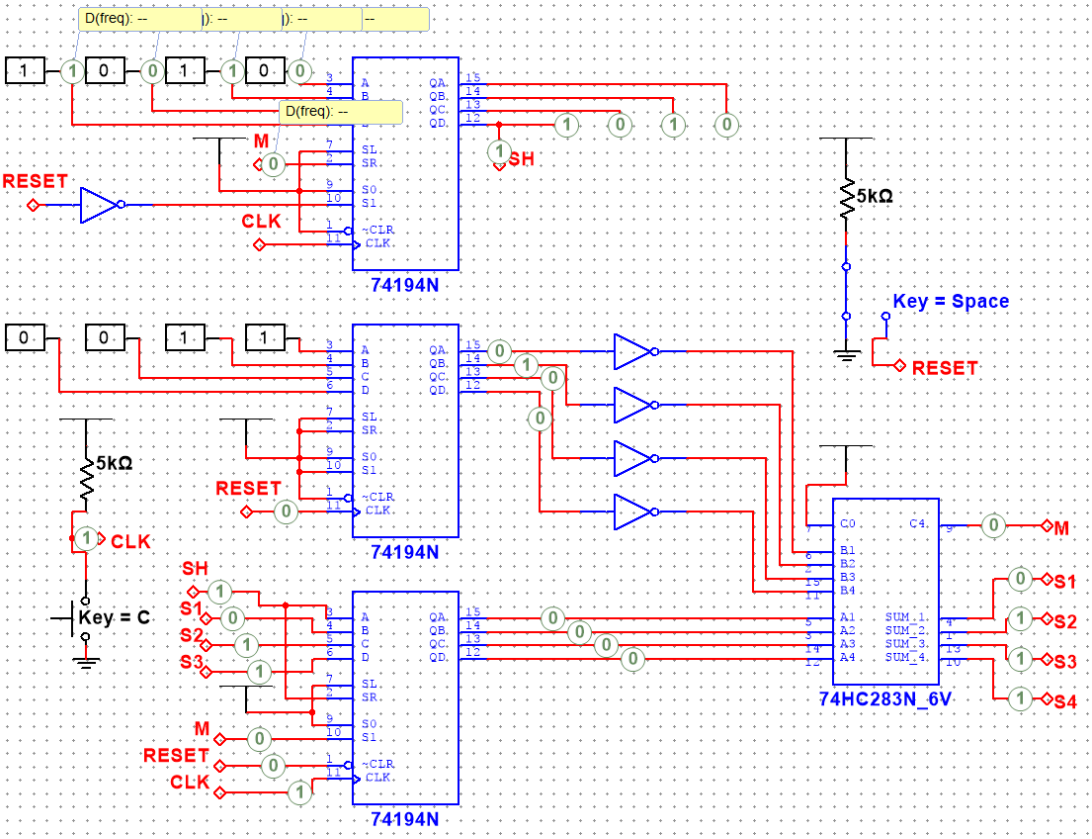

Figure 6b1: Test Case #2, Load

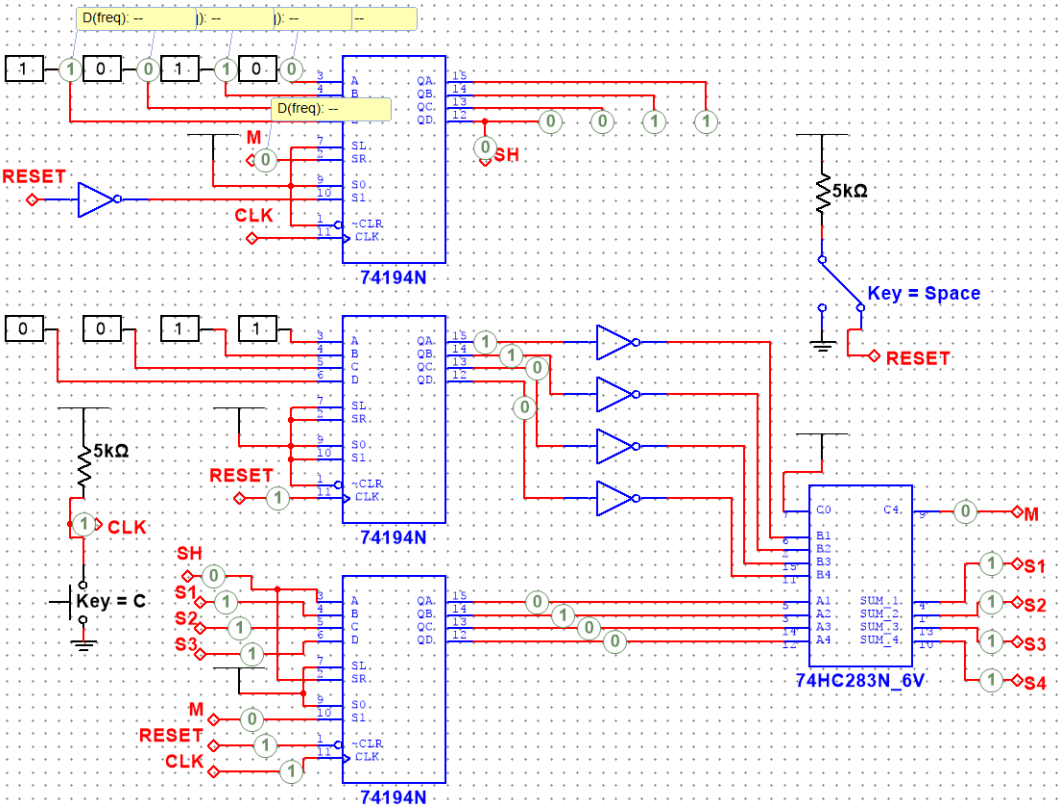

Figure 6b2: Test Case #2, Answer

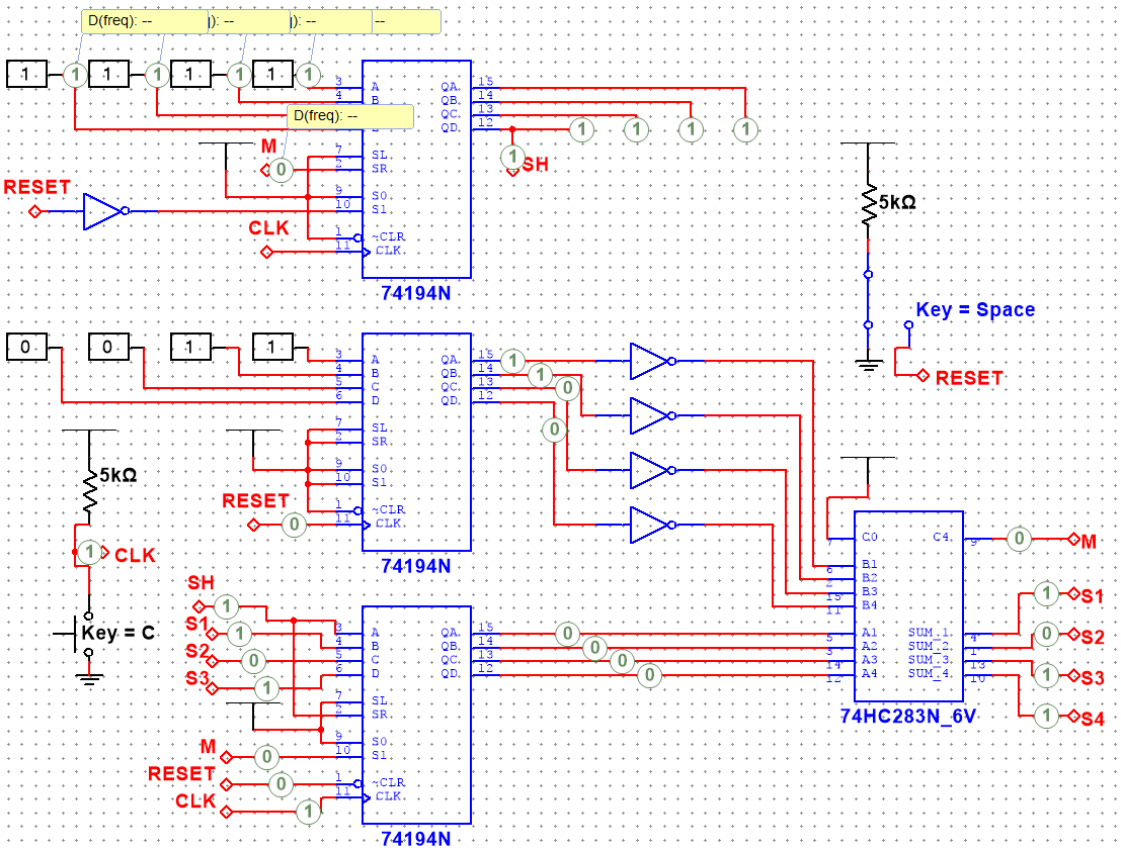

Figure 6c1: Test Case #3, Load

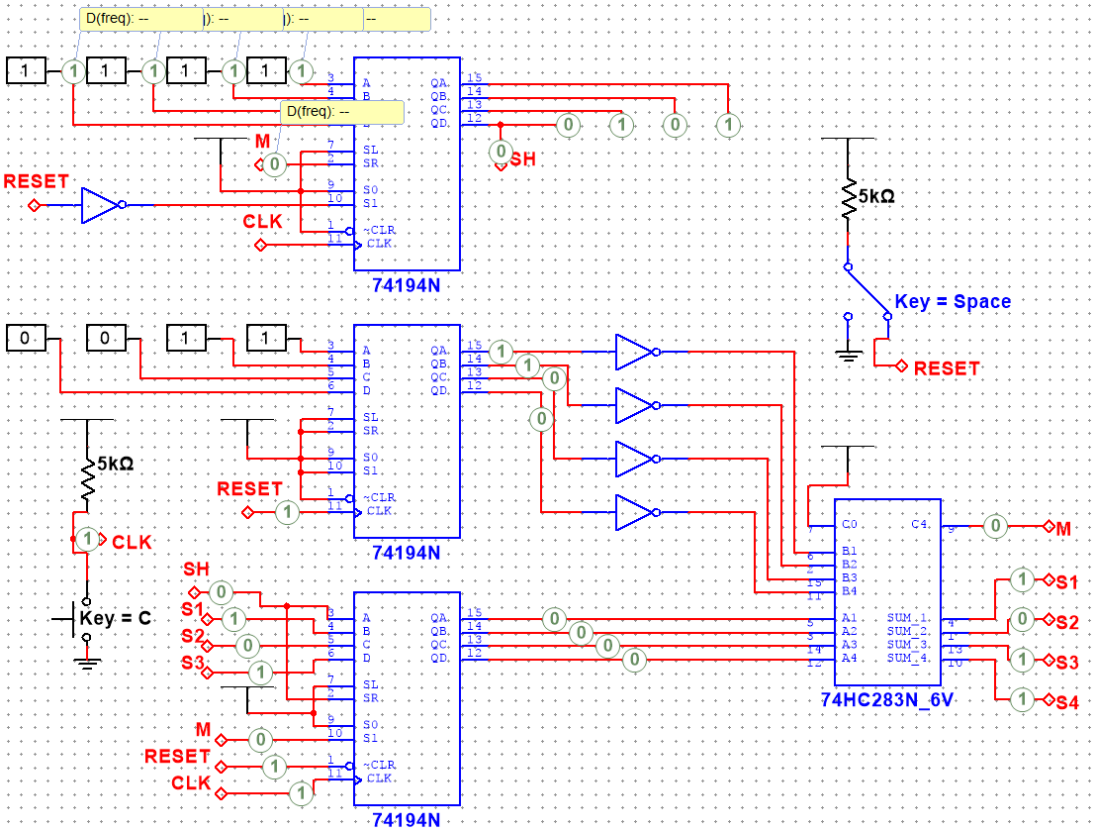

Figure 6c2: Test Case #3, Answer

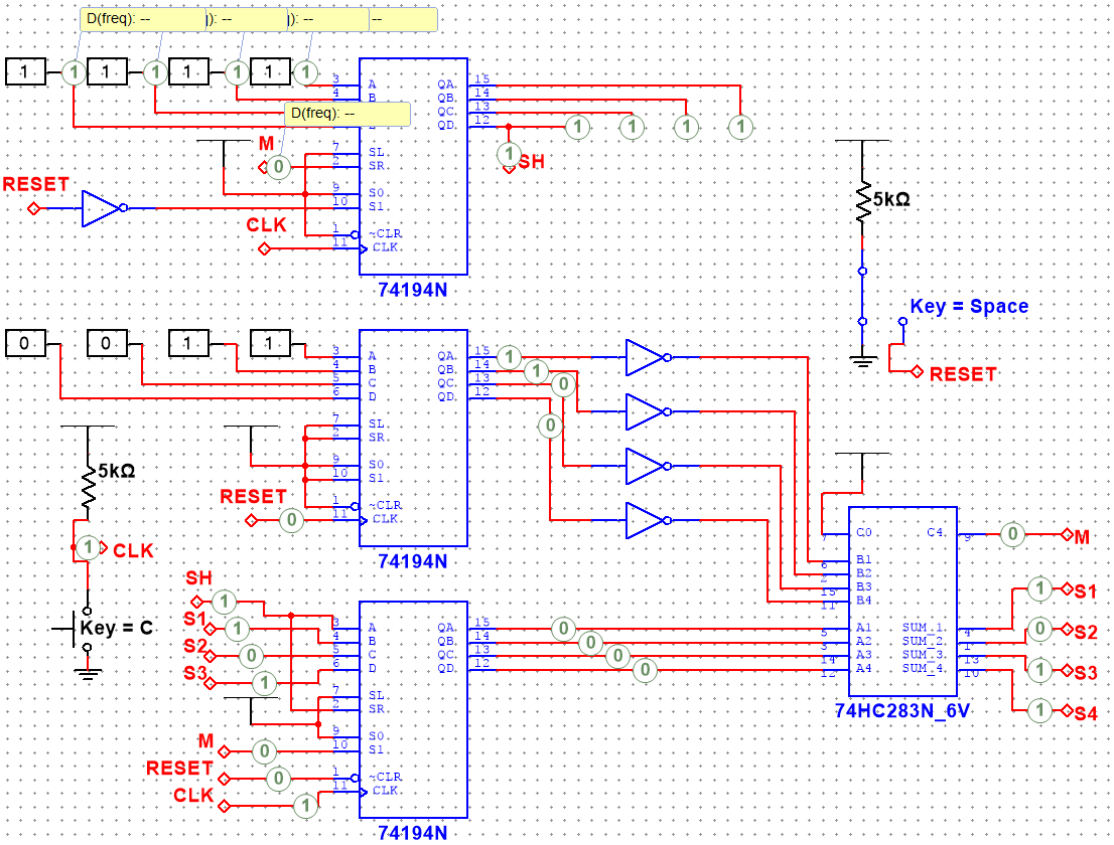

Figure 6d1: Test Case #4, Load

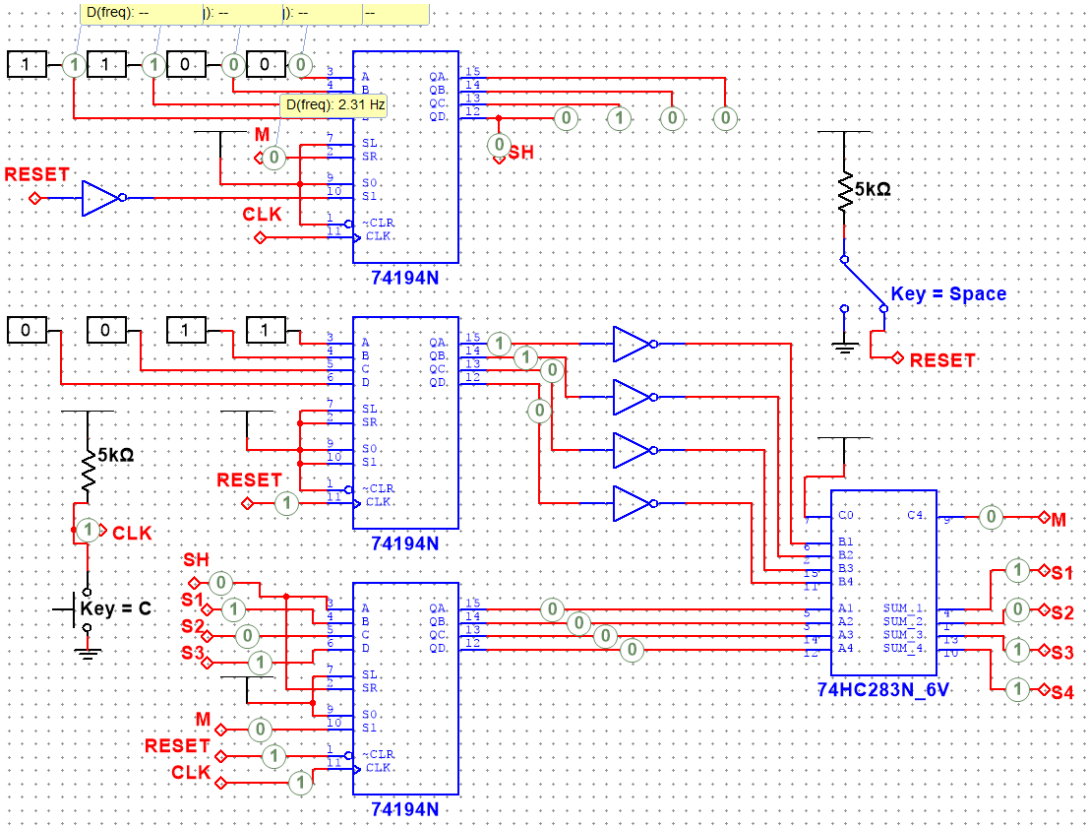

Figure 6d2: Test Case #4, Answer

Here is where I go step-by-step to explain how this circuit works. First step is to select your dividend and divider. Once you have these selected, you press [Space] to toggle the reset, which will load the quotient with the dividend and load the divisor into IC2. We have inverters on the output of IC2 to make sure the MSB and LSB are correct on the output of IC2. As you can see on the Load in Figure 6..1, this is the case. Then you must run through the Clock 4 times to shift the quotient through the output pin SH, from IC1 to IC3. Once IC3 is loaded, the clock is pressed until the output of IC3 is 0000, then the quotient will display the correct answer. IC1 controls the dividend, loads it into IC3, IC2 controls the divisor, and IC4 does the subtraction of the dividend - divisor. Each clock cycle does another subtraction, until the dividend is 0000.

Between IC3 and IC4 is where the remainder is displayed, on QB(LSB) - QD (MSB). QA shows if the sign of the remainder is positive or negative, (0 = positive). This can be seen in Figure 7. The test case I used is 13/3 = 4 with a remainder of 1. So we would expect QB to be 1 and the rest to be 0 when we have a remainder of 1, which is what is shown. There was no additional circuitry, outside of a digital probe, that was needed, to display the remainder.

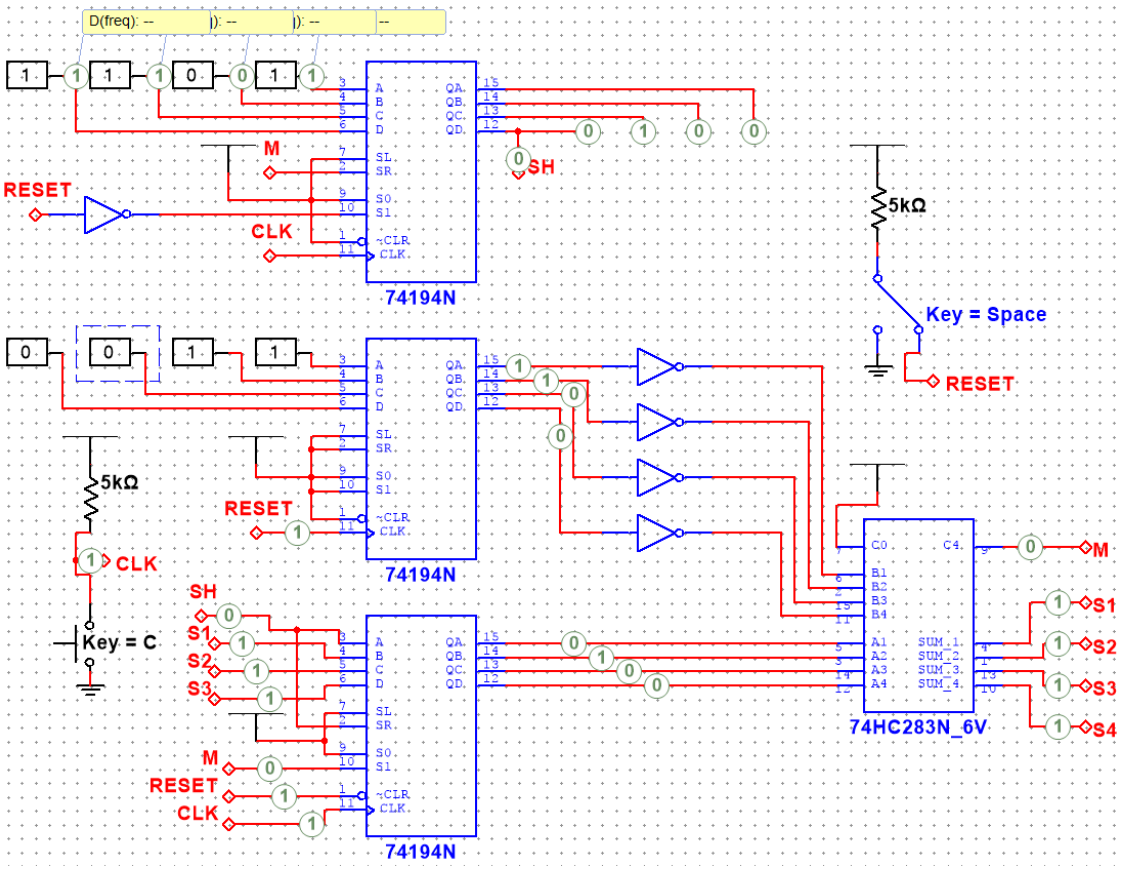

Figure 7: Remainder Test Case

Conclusion

This was one of the more difficult labs I have had to do. I am unfamiliar with how these specific ICs work, so I had to read the data sheets and hopefully I understood them correctly. It was very interesting seeing how to do division, we just do subtraction multiple times. It was also interesting seeing how you can load an IC with another and then do arithmetic. I also had a lot of issues getting the product and quotient to display correctly, so it gave me practice at debugging circuits and reading the data sheets. It has been a good review of basic circuit analysis techniques as well, having to watch the 0/1s shift through the different ICs and how they interact with each other. It has been years since I have used these skills, so it was a nice refresher.