ECE 540 Final Project Proposal

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We're building a digit recognition system on the **Nexys A7-100T FPGA** using the **RVfpga (RISC-V) soft-core processor**. The user will draw numbers on a **4.0" capacitive touchscreen display** that communicates with the FPGA over SPI (for the screen) and I2C (for the touch controller). Once a digit is drawn, our system will process the input, scale it down to 28×28 pixels, and run it through a lightweight **pretrained MNIST neural network model**—all written in C and running directly on the RVfpga CPU.

The core of the project involves writing low-level **SPI and I2C drivers in Verilog**, integrating them into our existing RVfpga SoC design via a Wishbone bus, and handling the display and touch input. On the software side, we'll port a small neural net model to run on the RISC-V CPU using fixed-point math for efficiency. The goal is to display both the drawing canvas and the predicted digit on the screen in real-time, showing how embedded systems and AI can come together in a compact, self-contained FPGA design.