



**Portland State**  
UNIVERSITY

## **ECE 425 Lab 2: Inverter**

**Authors:**

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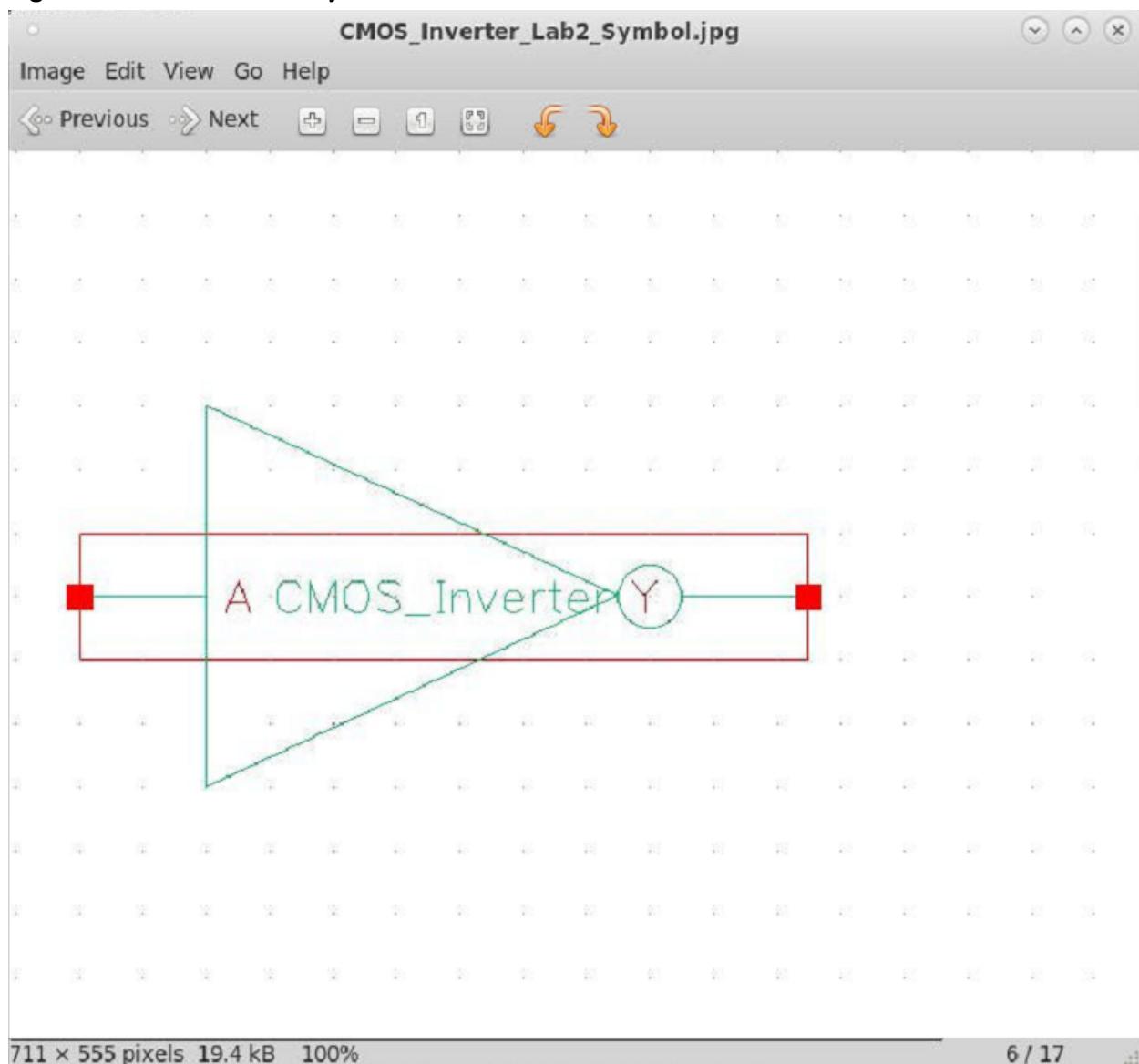
**Daniel Anishchenko**

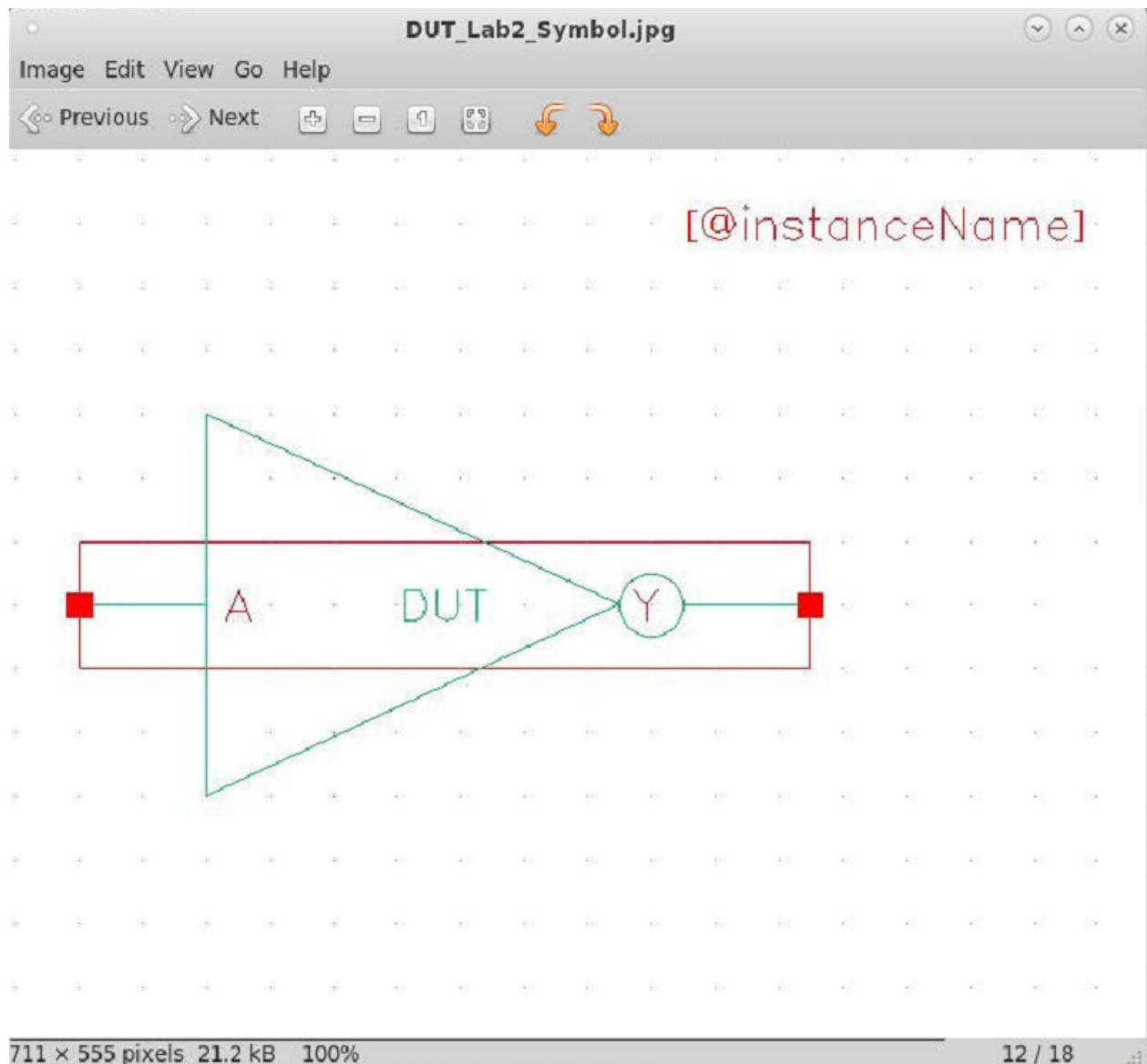
## 1) Cell Description:

The CMOS (Complementary Metal-Oxide-Semiconductor) inverter is a digital logic gate that performs the logical NOT operation. The CMOS inverter has one input and one output. When the input is at a low logic level, the NMOS transistor is off (open), and the PMOS transistor is on (closed). This allows current to flow from the power supply voltage ( $V_{dd}$ ) to the output, driving it to a high logic level. The CMOS inverter is built using one NMOS and one PMOS transistor connected in series through their drains. The input of the CMOS inverter is connected to the gates of both transistors. The output of the CMOS transistor is connected to the drains of both PMOS and NMOS. The source for the NMOS is connected to ground and the source of PMOS is connected to the power supply ( $V_{DD}$ ).

## 2) Cell Symbol:

Figure 1: CMOS Inverter Symbol





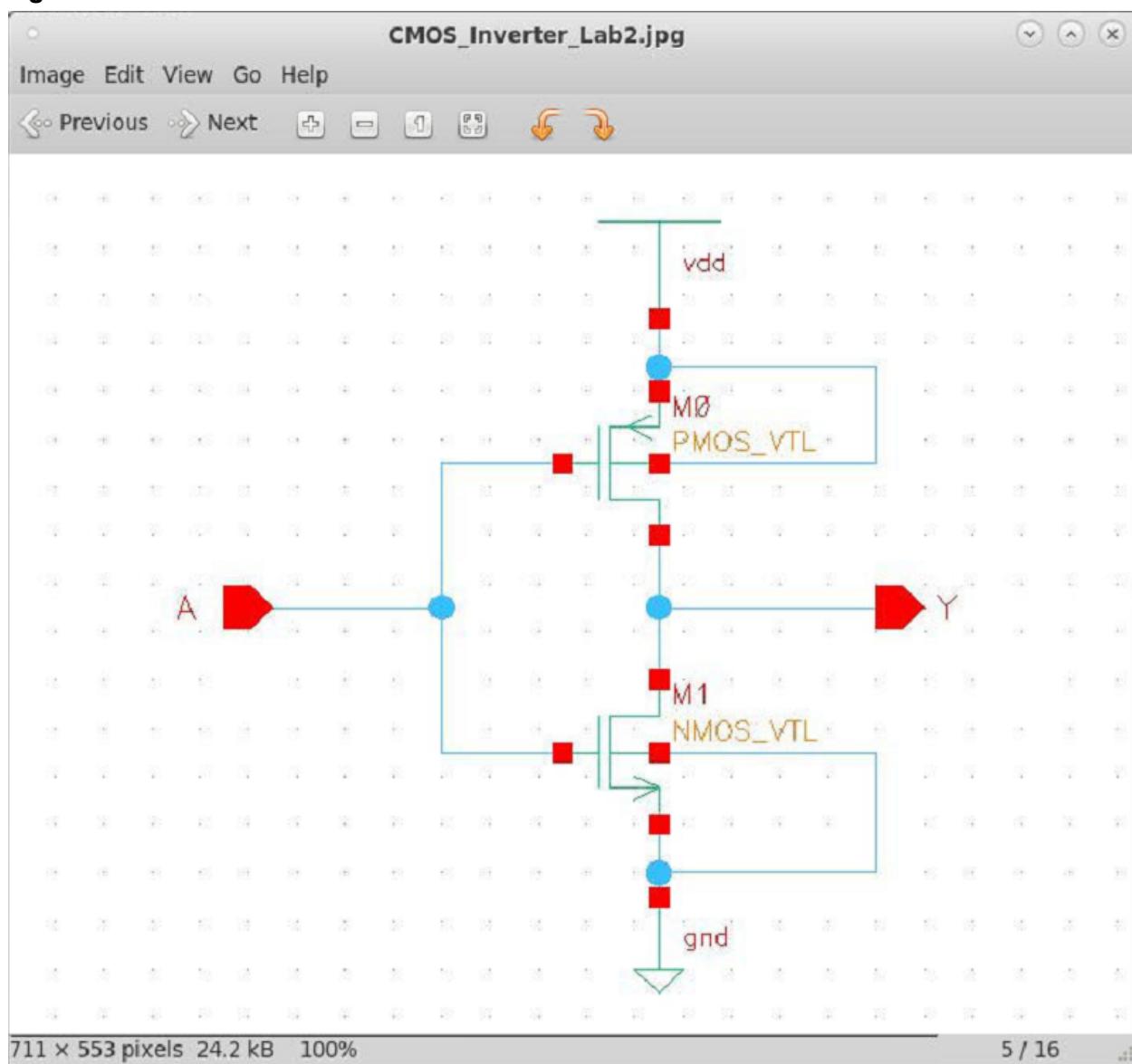
### 3) Cell Truth Table:

Table 1: CMOS Inverter Truth Table

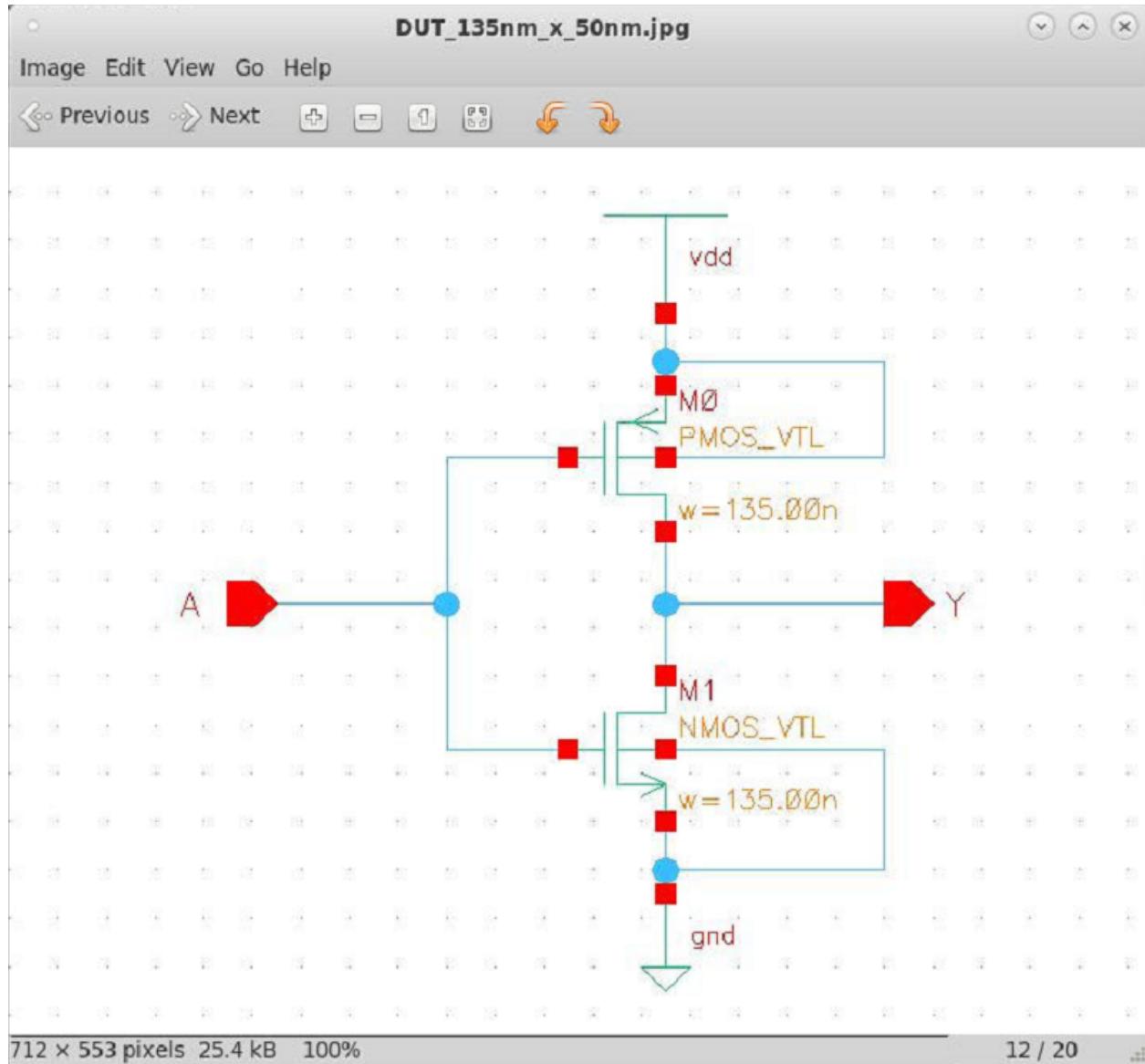
Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

**4) Cell Schematic Diagram:**

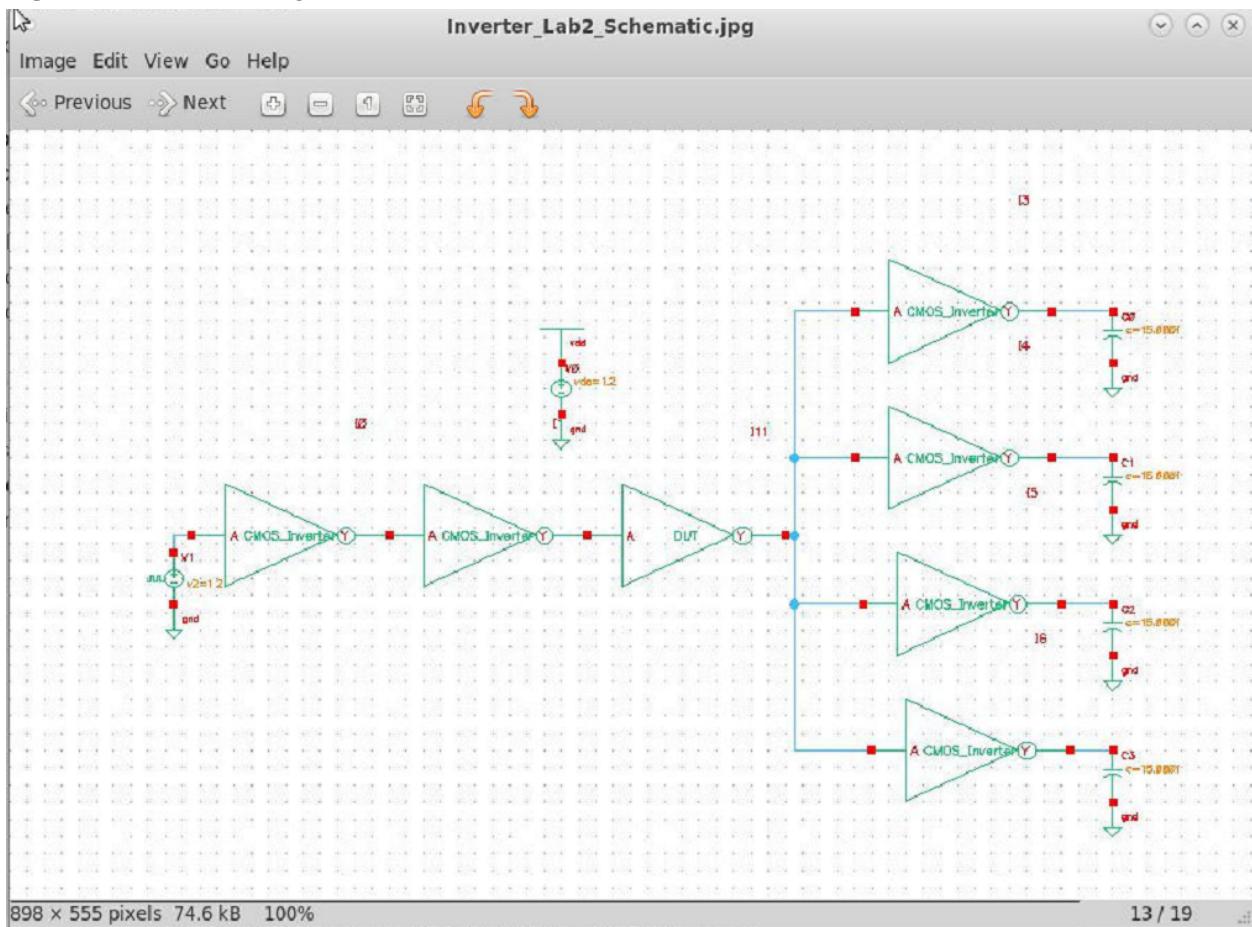
**Figure 1:** CMOS Inverter Schematic



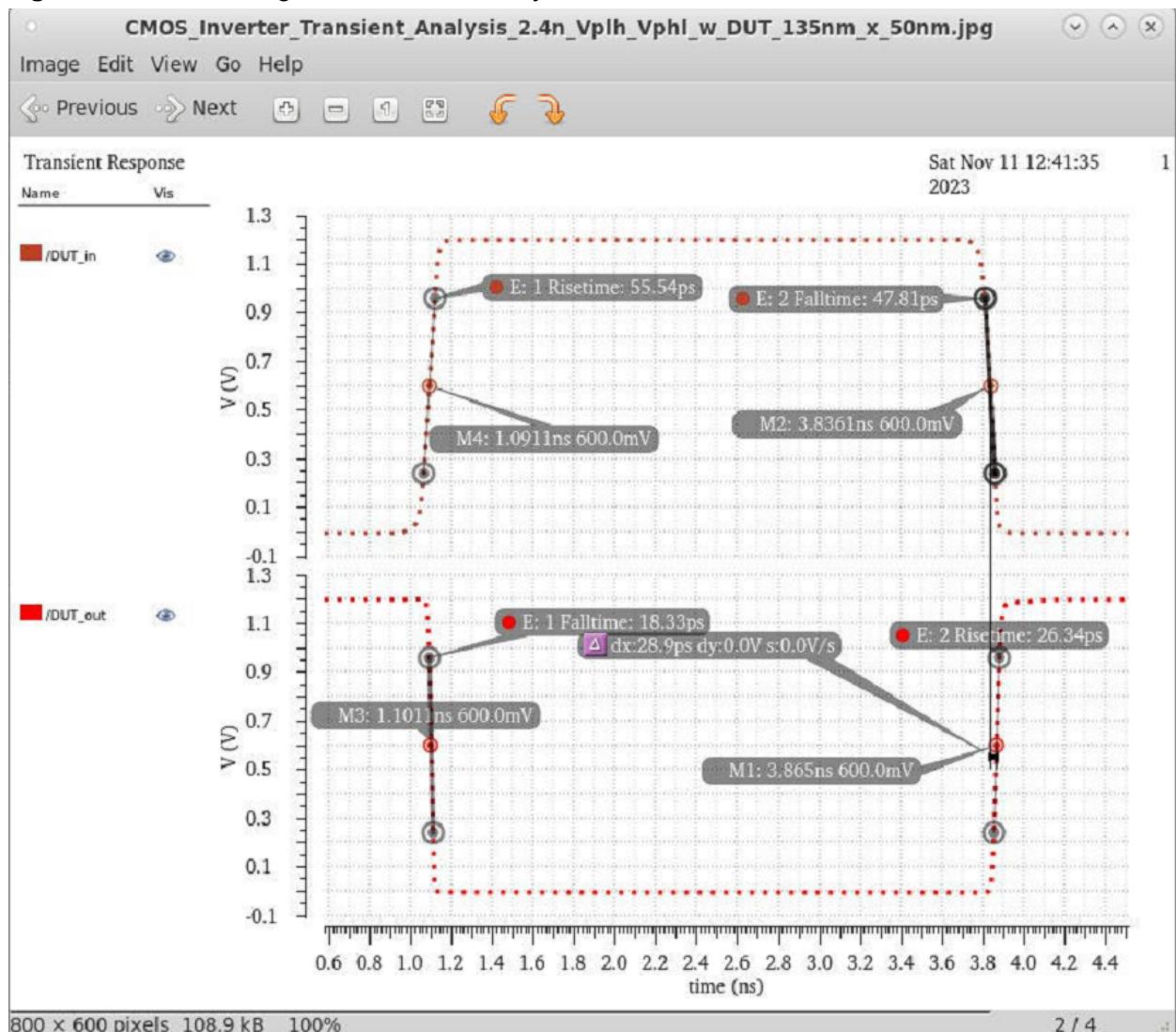
**Figure 2.** DUT 135nmx50nm



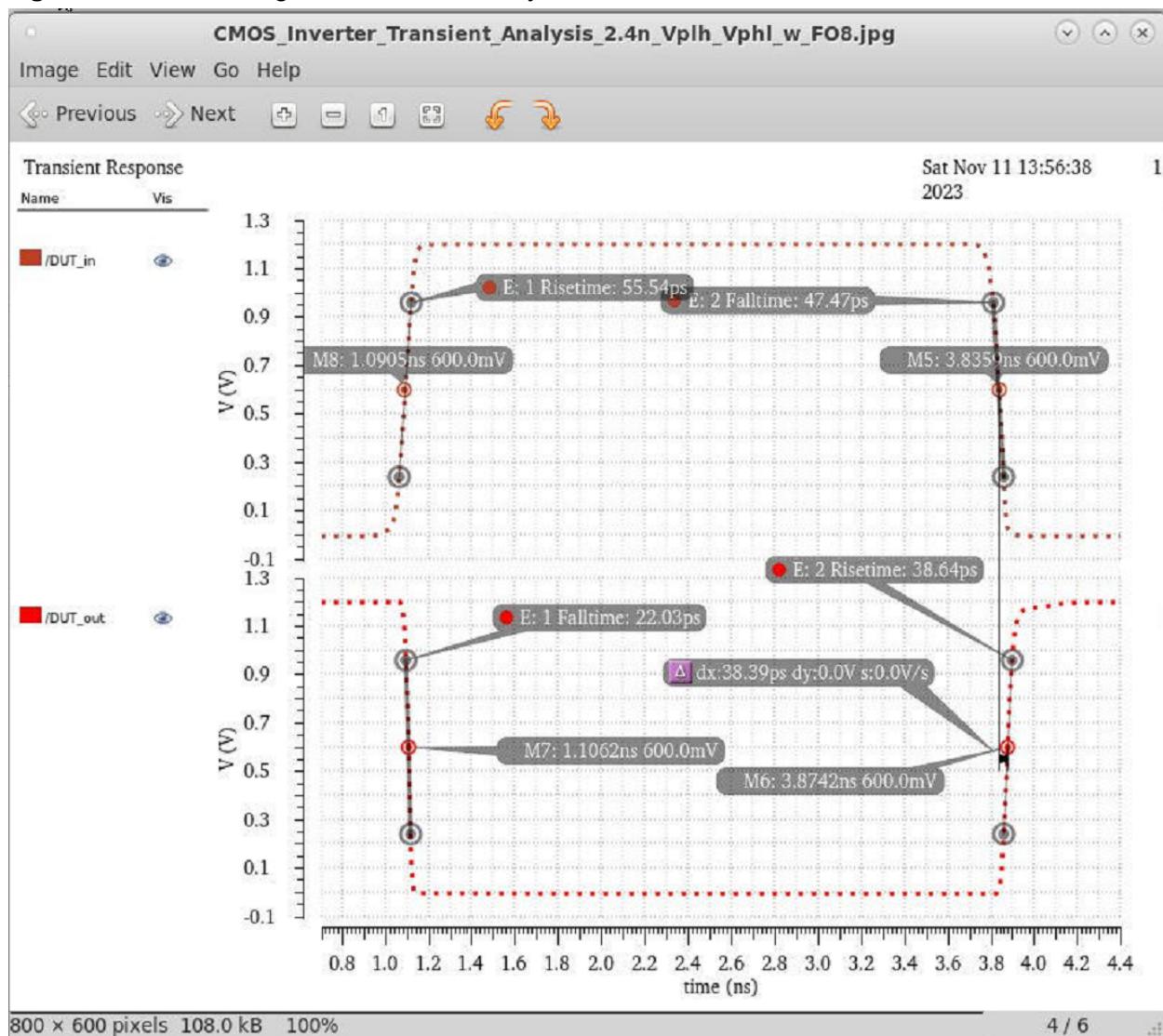
**Figure 3.** Non-Inverting Buffer w/ DUT Schematic FO4



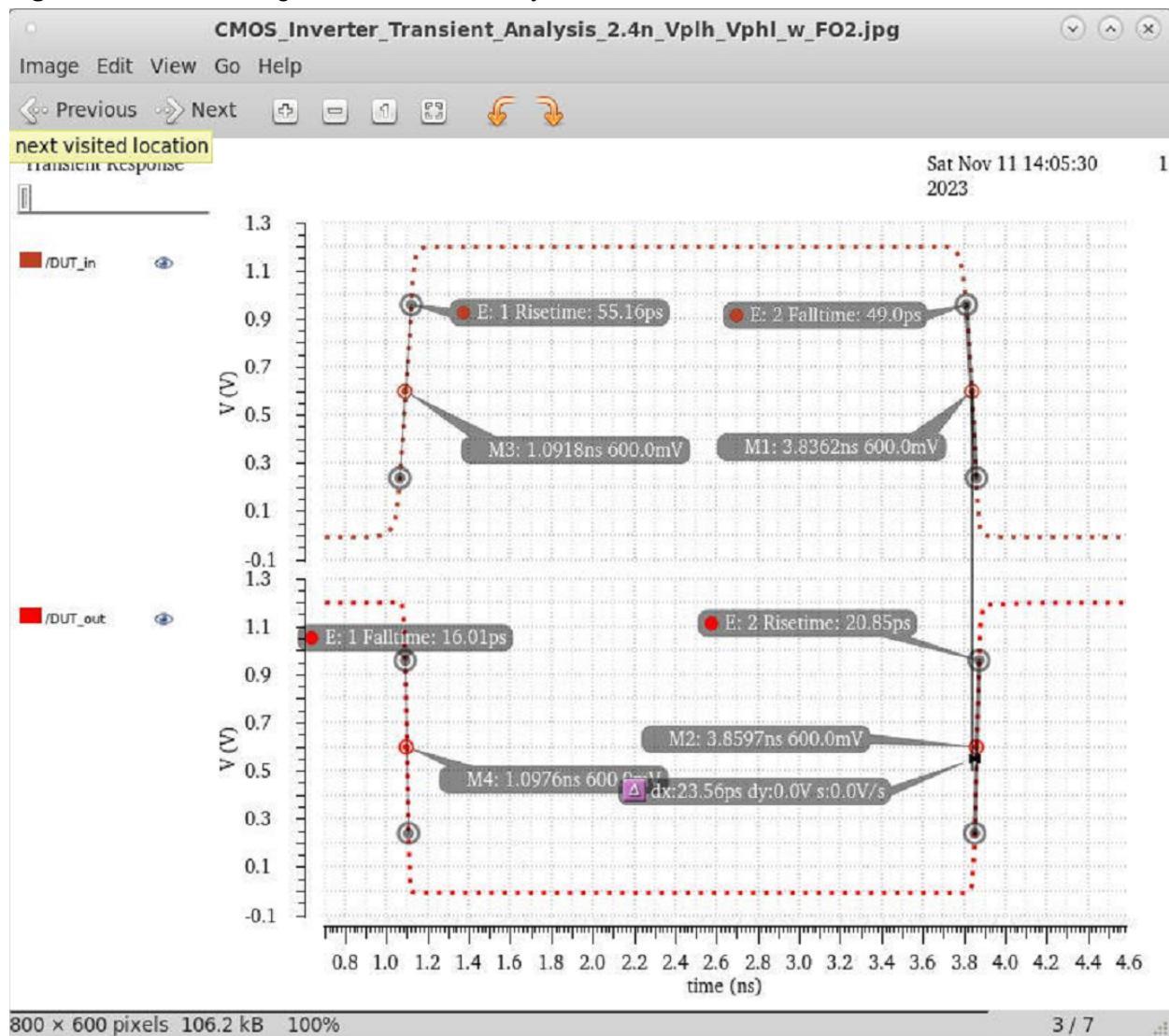
**Figure #.** Non-Inverting Buffer w/ FO4 Analysis



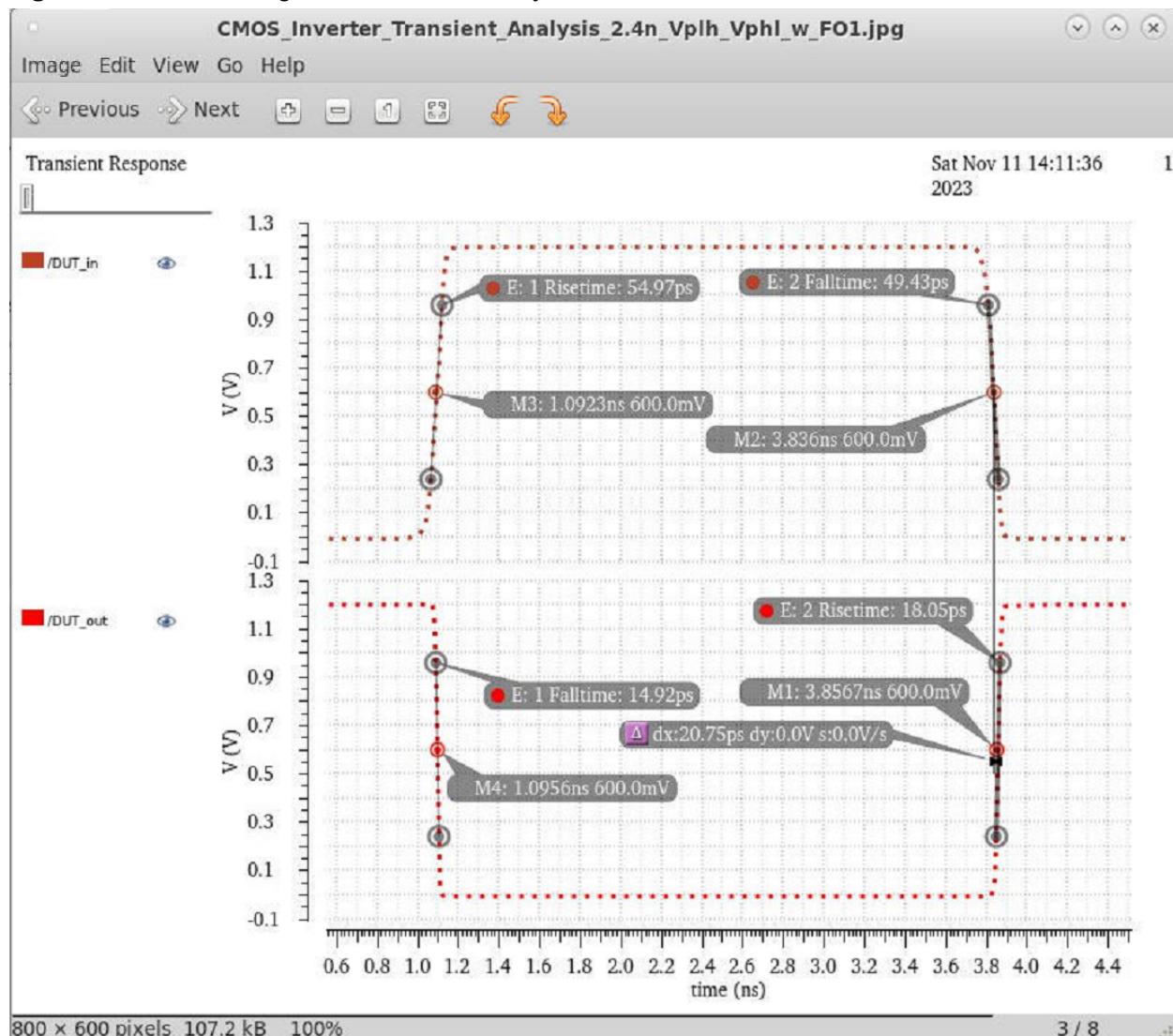
**Figure #.** Non-Inverting Buffer w/ FO8 Analysis



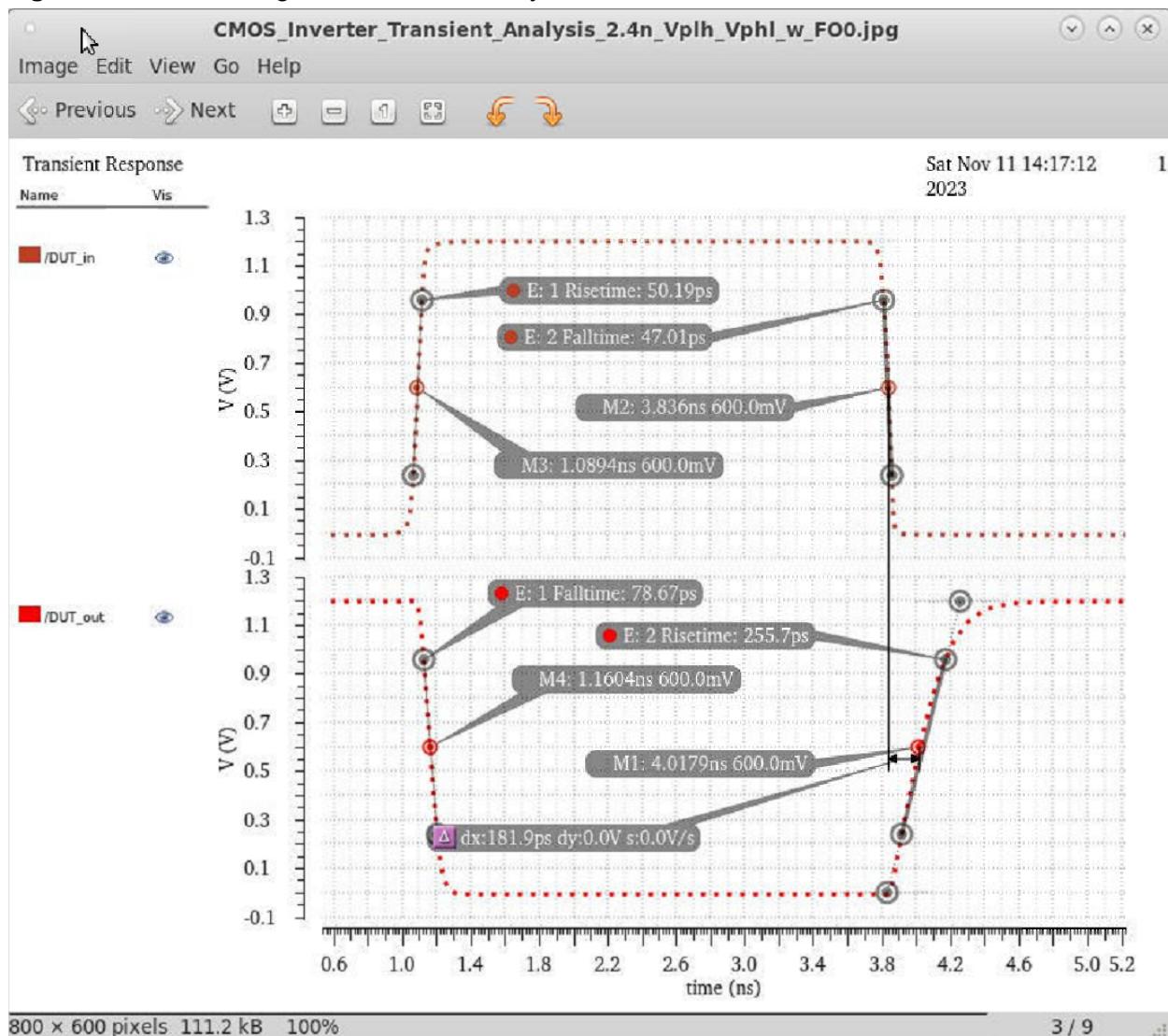
**Figure #.** Non-Inverting Buffer w/ FO2 Analysis



**Figure #.** Non-Inverting Buffer w/ FO1 Analysis



**Figure #.** Non-Inverting Buffer w/ FO0 Analysis



**5) Cell Layout Diagram and Dimension:**

**Table 2:** Cell and Transistor Dimensions for CMOS

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS_VTL	90	50
NMOS_VTL	90	50

**6) Rise and Fall Times:**

**Table 3:** Transistor Rise Time for CMOS Inverter

Input X: Output Rise Time Data $t_r$					
Input rise/fall time (ns)	Output Load (FO <sub>X</sub> )				
	0	1	2	4	8
0.05	0.226	0.0181	0.0209	0.0263	0.0386
					-

**Table 4:** Transistor Fall Time for CMOS Inverter

Input X: Output Fall Time Data $t_f$					
Input rise/fall time (ns)	Output Load (FO <sub>X</sub> )				
	0	1	2	4	8
0.05	0.0787	0.0149	0.0160	0.0183	0.0220

**7) Propagation Delays:**

**Table 5:** Data Worst Case Low to High Propagation Delay  $t_{ph}$  (ns) for CMOS Inverter

Data Worst Case Low to High Propagation Delay $t_{ph}$ (ns)					
Input rise/fall time (ns)	Output Load (FO <sub>X</sub> )				
	0	1	2	4	8
0.05	4.02	0.0208	0.0235	0.0289	0.0384

**Table 6:** Data Worst Case High to Low Propagation Delay  $t_{phl}$  (ns) for CMOS Inverter

Data Worst Case Low to High Propagation Delay $t_{phl}$ (ns)					
Input rise/fall time (ns)	Output Load (FO <sub>X</sub> )				
	0	1	2	4	8
0.05	0.071	0.0033	0.0058	0.0100	0.0157

**8) CMOS Inverter PMOS and NMOS width variation**

CMOS Inverter PMOS and NMOS width variation table					
DUT		Rise Fall and Delay (ps)			
W <sub>p</sub> (nm)	W <sub>n</sub> (nm)	T <sub>r</sub>	T <sub>f</sub>	T <sub>phl</sub>	T <sub>phl</sub>
135	135	26.34	18.33	28.9	10.0

**9) What is the role and responsibility of each member of your team? Who did what part of the lab? Please list the individual contribution to the lab.**

**Cody Reid** - Worked on the non-inverting buffer circuit and DUT analysis

**Ken Sutter** - Worked on formal report, answering lab questions, doing circuit calculations, documenting team work, helping design circuits.

**Phil Nevins** - Worked on the CMOS circuit and assisted with inverter analysis

**Daniel Anishchenko** - Worked on CMOS gate circuit logic, assisted with schematic design

**10) Conclusion -**

In pursuit of meeting the timing specifications given in the lab document ( $T_{phl}$  and  $T_{phl} < 0.04\text{ns}$ ; and  $T_r$  and  $T_f < 0.030\text{ns}$ ), we employed a iteration strategy, progressively increasing the size of PMOS and NMOS transistors within the Digital Circuit Under Test (DUT) by 45nm at a time. Our focus was on identifying the optimal transistor dimensions that could effectively meet our timing requirements.

The stepwise increment in transistor sizes was motivated by the idea to boost the circuit's speed and align with the given timing constraints. This approach highlights the inherent trade-offs in semiconductor design, where altering transistor dimensions has a nuanced impact on various pieces of the circuit performance. The adjustment of the transistor parameters was needed to achieve the specified timing criteria.