Ken Sutter
Phil Nevins
Cody Reid
Daniel Anishchenko

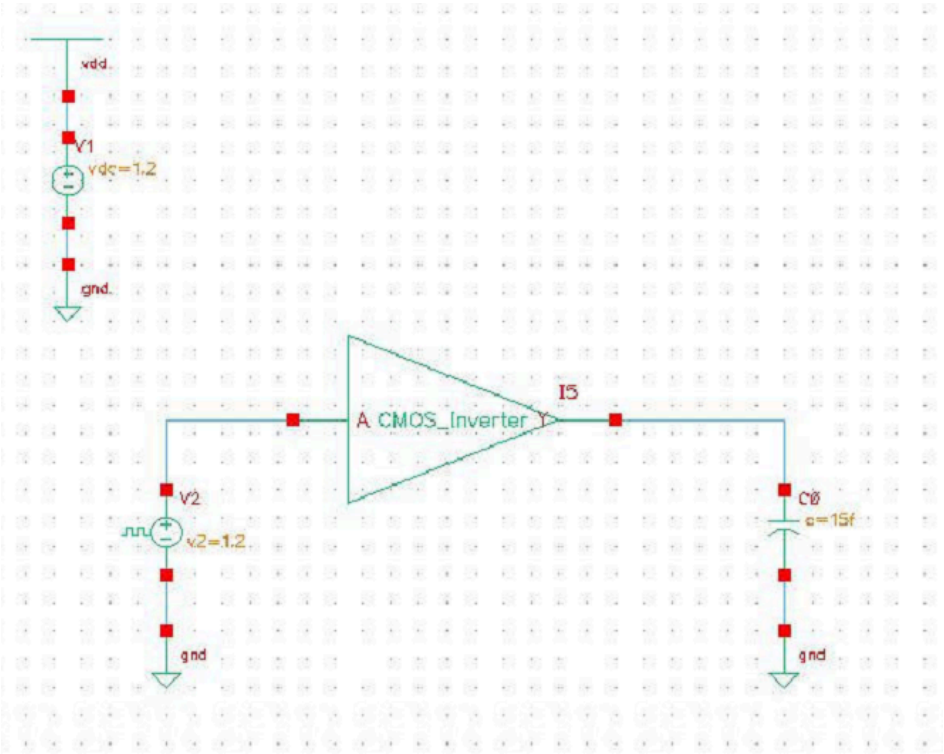
ECE-425 Lab 1 CMOS Inverter

1) Cell Description: CMOS Inverter

The CMOS (Complementary Metal-Oxide-Semiconductor) inverter is a digital logic gate that performs the logical NOT operation. The CMOS inverter has one input and one output. When the input is at a low logic level, the NMOS transistor is off (open), and the PMOS transistor is on (closed). This allows current to flow from the power supply voltage (Vdd) to the output, driving it to a high logic level.The CMOS inverter is built using one NMOS and one PMOS transistor connected in series through their drains. The input of the CMOS inverter is connected to the gates of both transistors. The output of the CMOS transistor is connected to the drains of both PMOS and NMOS. The source for the NMOS is connected to ground and the source of PMOS is connected to the power supply (VDD).

2) Cell Symbol:

Figure 1: 50x90 CMOS Inverter TB Schematic



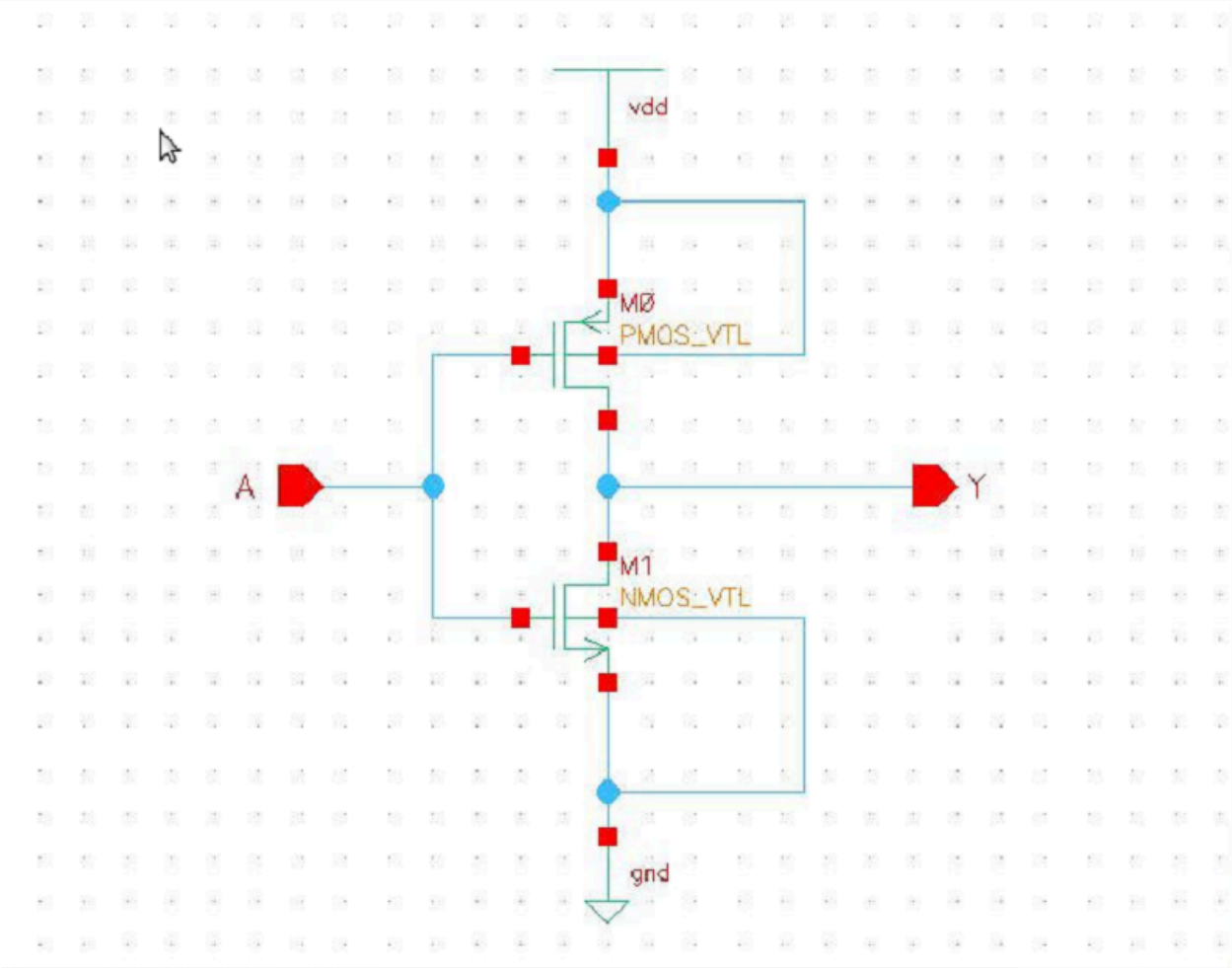
3) Cell Truth Table:

Table 1: CMOS Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 2: 50x90 CMOS Inverter TB Schematic



5) Transistor Dimensions:

Table 2: Cell and Transistor Dimensions for CMOS

Cell Physical Dimensions		
	X	Y
Cell Dimension in μm	50	90
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS_VTL	50	90
NMOS_VTL	50	90

6) Input X: Output Rise Time Data t_r (ns):

Table 3: Transistor Rise Time for CMOS Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.3949	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 4: Transistor Fall Time for CMOS Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.1155	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 5: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for CMOS Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.0937	-

9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 6: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for CMOS Inverter

Data Worst Case Low to High Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.270	-

10) Transient Analysis

Figure 3: 50x90 CMOS Inverter Transient Analysis - 1

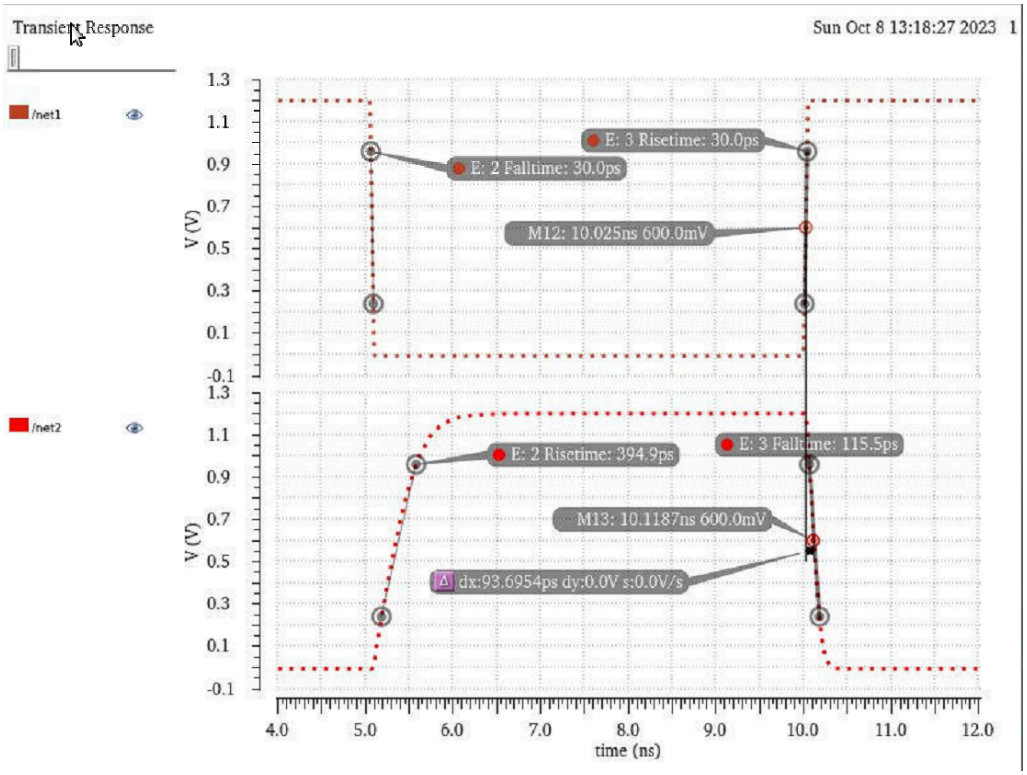
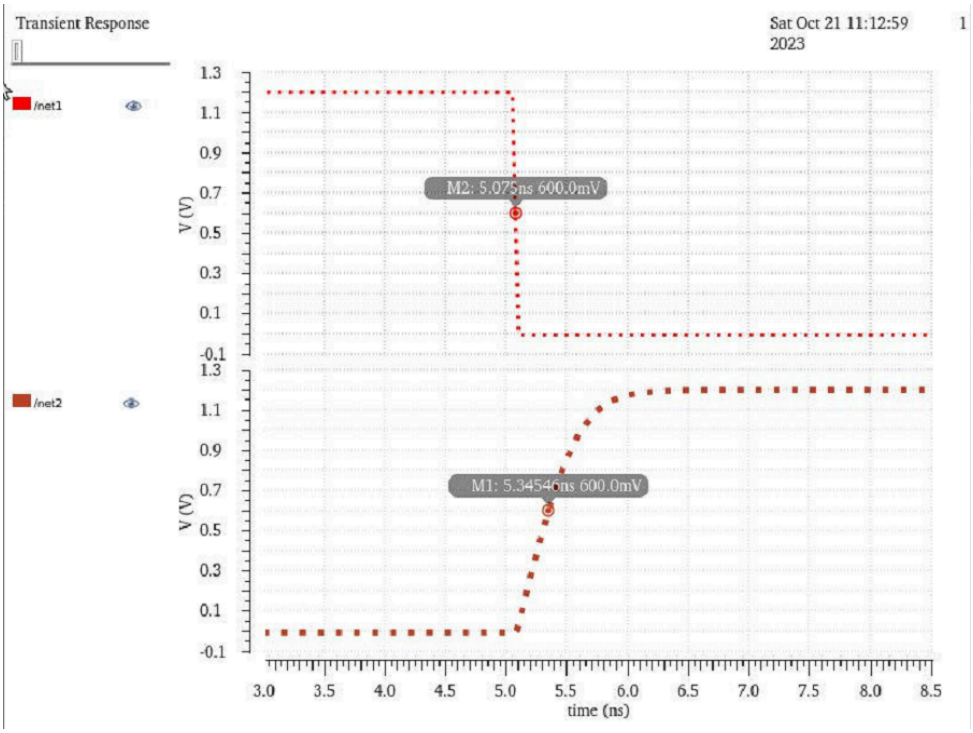
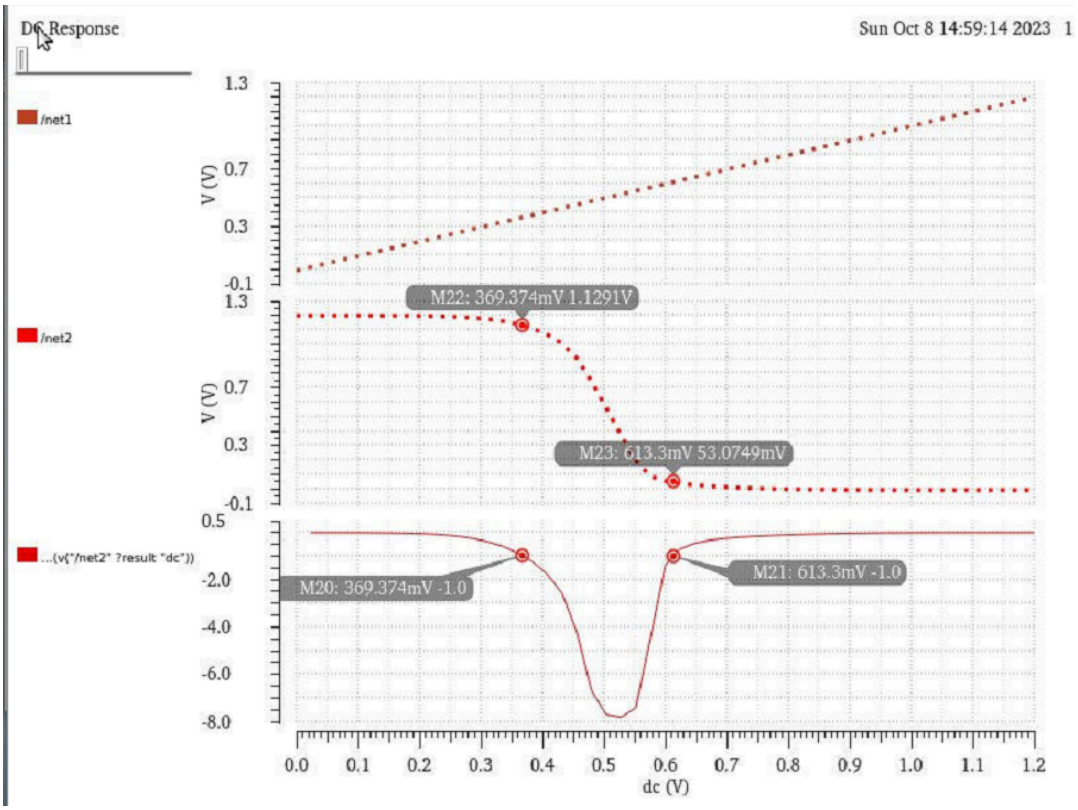


Figure 4: 50x90 CMOS Inverter Transient Analysis - 2



11) DC analysis

Figure 5: 50x90 CMOS Inverter DC Analysis

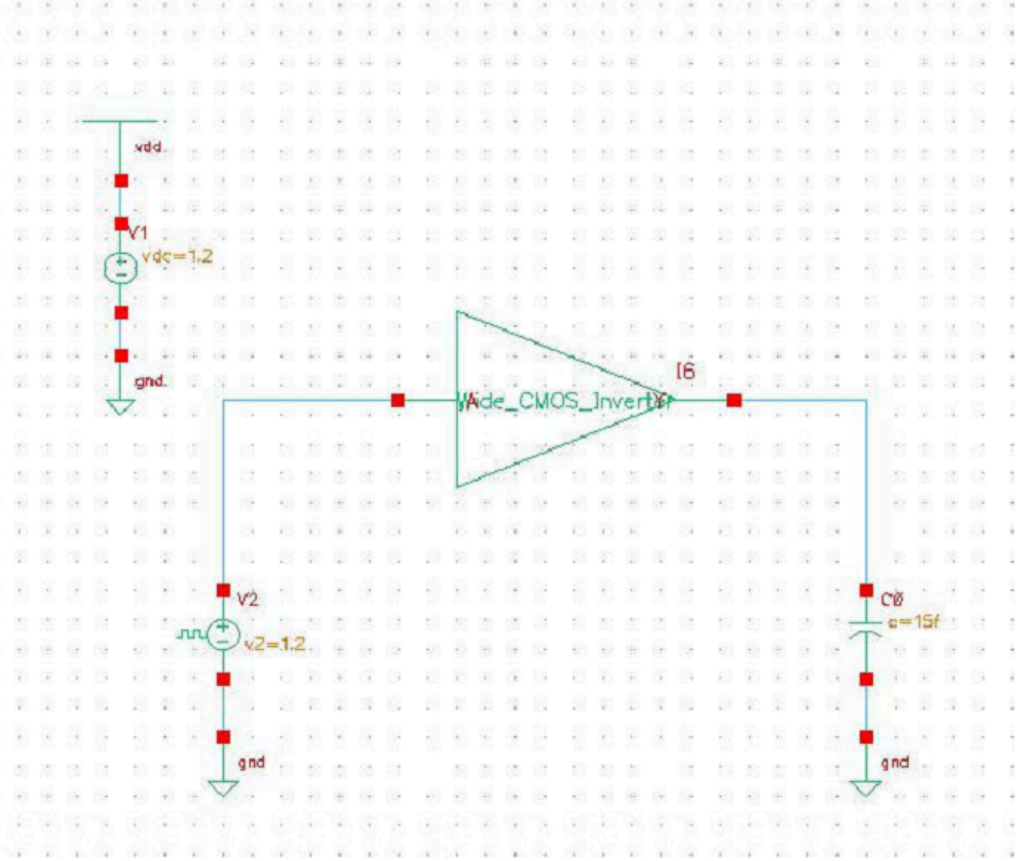


1) Cell Description: CMOS Wide Inverter

The CMOS (Complementary Metal-Oxide-Semiconductor) Wide inverter is a digital logic gate that performs the logical NOT operation. The CMOS Wide inverter has one input and one output. When the input is at a low logic level, the NMOS transistor is off (open), and the PMOS transistor is on (closed). This allows current to flow from the power supply voltage (Vdd) to the output, driving it to a high logic level. The CMOS Wide inverter is built using one NMOS and one PMOS transistor connected in series through their drains. The input of the CMOS Wide inverter is connected to the gates of both transistors. The output of the CMOS Wide transistor is connected to the drains of both PMOS and NMOS. The source for the NMOS is connected to ground and the source of PMOS is connected to the power supply (VDD). The CMOS inverter is known for its low power consumption, high input impedance, and high output impedance, making it a fundamental component in modern digital integrated circuits.

2) Cell Symbol:

Figure 6: CMOS Wide Inverter Cell Symbol



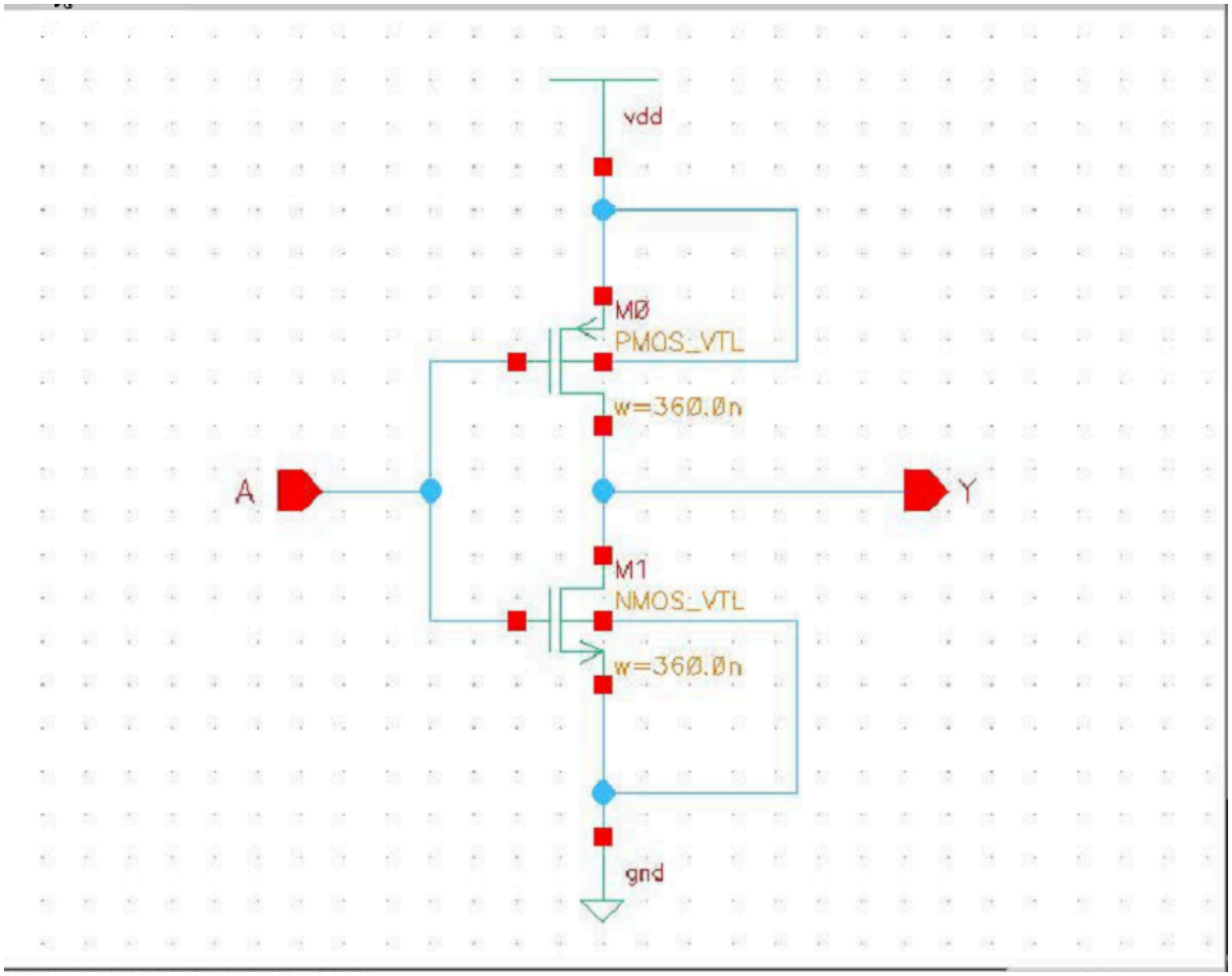
3) Cell Truth Table:

Table 7: CMOS Wide Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 7: 50x360 CMOS Wide Inverter Schematic



5) Transistor Dimensions:

Table 8: Cell and Transistor Dimensions for CMOS Wide Inverter

Cell Physical Dimensions		
	X	Y
Cell Dimension in μm	50	360
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS_VTL	50	360
NMOS_VTL	50	360

6) Input X: Output Rise Time Data t_r (ns):

Table 9: Transistor Rise Time for CMOS Wide Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.0943	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 10: Transistor Fall Time for CMOS Wide Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.0301	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 11: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for CMOS Wide Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.0292	-

9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 12: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for CMOS Wide Inverter

Data Worst Case Low to High Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.0733	-

10) Transient Analysis

Figure 8: 50x360 Wide CMOS Transient Analysis Waveform - 1

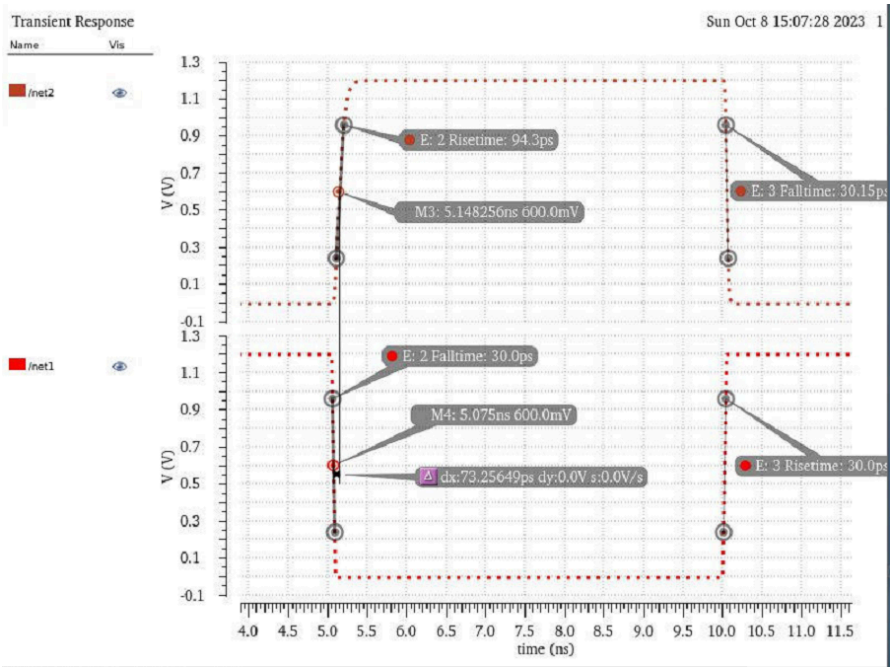
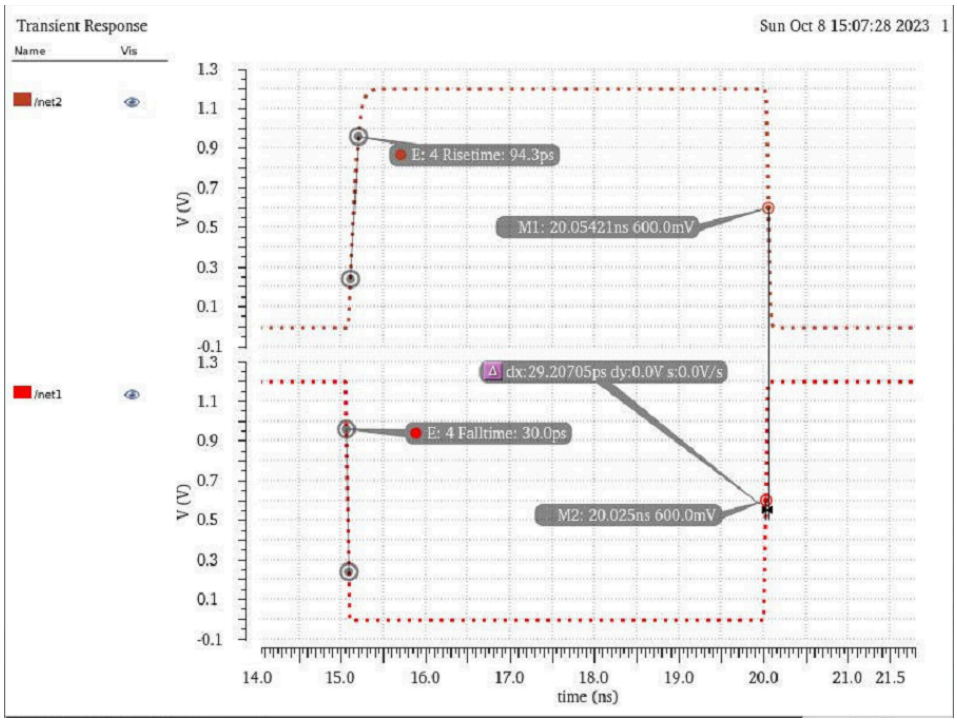
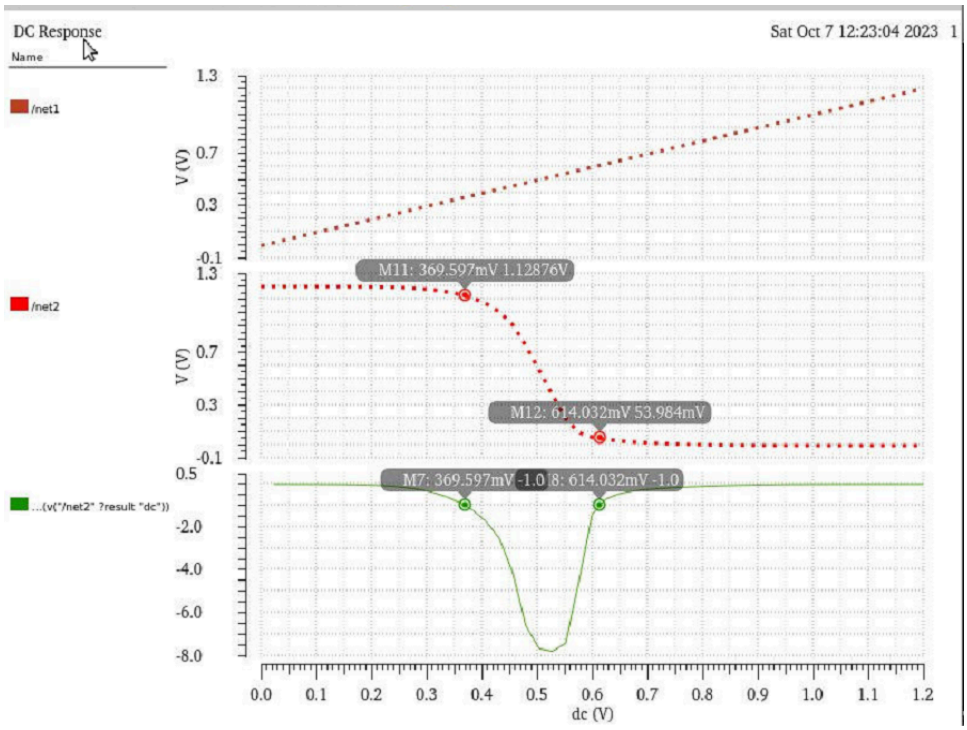


Figure 9: 50x360 Wide CMOS Transient Analysis Waveform - 2



11) DC analysis

Figure 10: 50x360 Wide CMOS DC Analysis Waveform



Ken Sutter
Phil Nevins
Cody Reid
Daniel Anishchenko

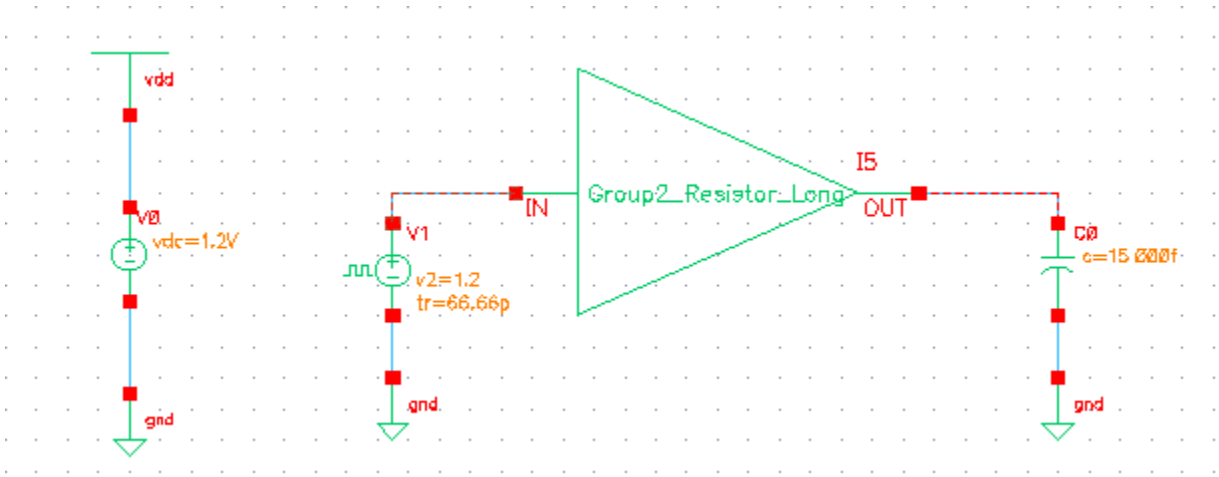
ECE-425 Lab 1 Resistive Load Inverter

1) Cell Description: Resistive Load Inverter

The Resistive Load Inverter is a type of CMOS inverter that uses a passive resistive load instead of an active load. This acts as a digital logic gate that performs the logical NOT operation. The Resistive Load Inverter has one input and one output.When the input is at a high logic level, the NMOS transistor is on (closed), and the PMOS transistor is off (open). This interrupts the current path through the resistive load, causing the output to be pulled to a low logic level. The Resistive Load inverter is built using one NMOS and one PMOS transistor connected in series through their drains. The input of the Resistive Load inverter is connected to the gates of both transistors. The output of the Resistive Load transistor is connected to the drains of both PMOS and NMOS. The source for the NMOS is connected to ground and the source of PMOS is connected to the power supply (VDD). The Resistive Load inverter offers advantages in terms of power consumption and area efficiency compared to some other load configurations.

2) Cell Symbol:

Figure 11: Resistive Inverter Cell symbol



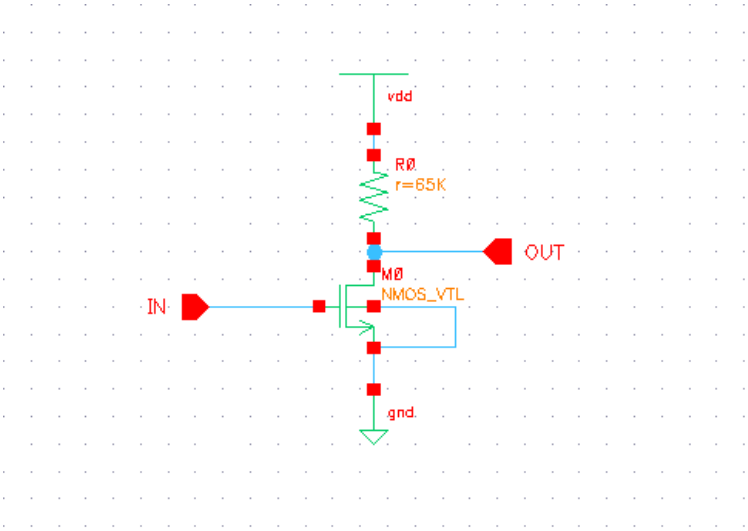
3) Cell Truth Table:

Table 13: Resistive Load Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 12: Resistive Inverter Schematic



5) Transistor Dimensions:

Table 14: Cell and Transistor Dimensions for Resistive Load Inverter

Cell Physical Dimensions		
	X	Y
Cell Dimension in μm	50	90
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
R1	65k Ω	-
NMOS_VTL	50	90

6) Input X: Output Rise Time Data t_r (ns):

Table 15: Transistor Rise Time for Resistive Load Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	1.279	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 16: Transistor Fall Time for Resistive Load Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.1185	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 17: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for Resistive Load Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.099	-

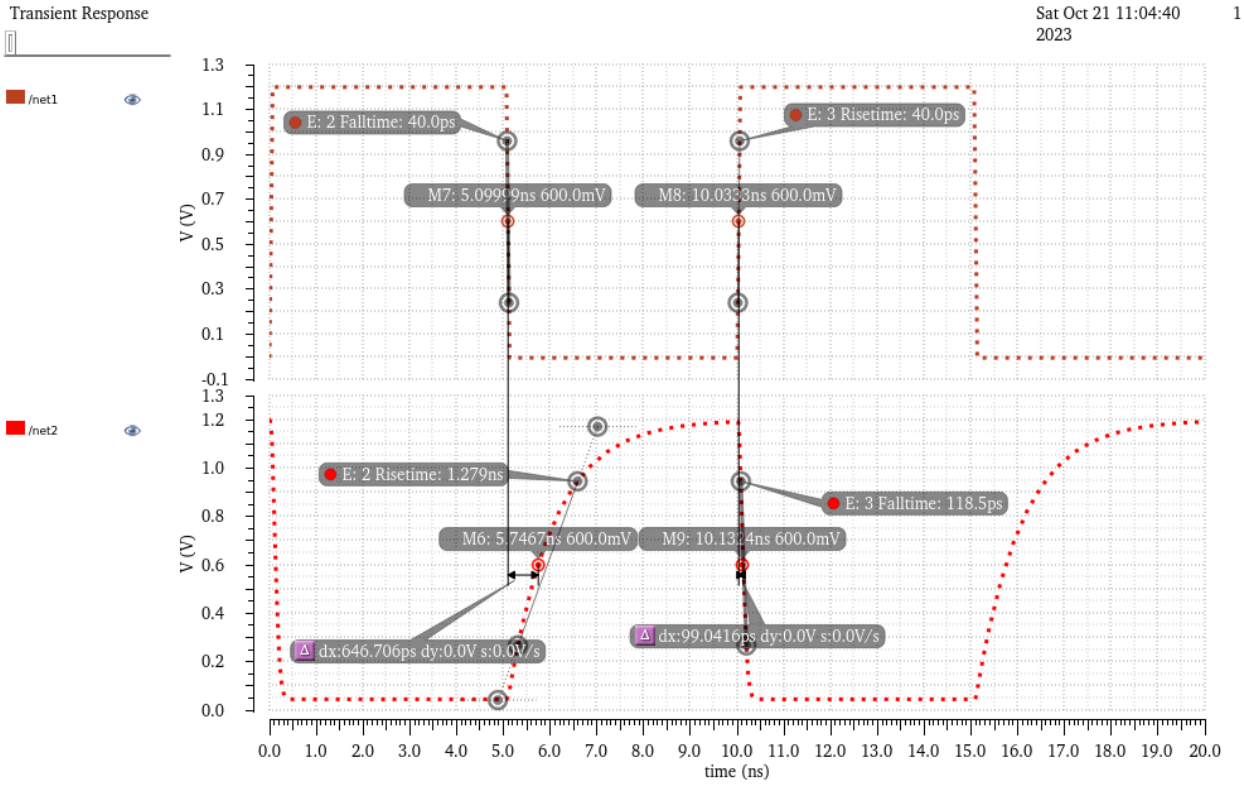
9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 18: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for Resistive Load Inverter

Data Worst Case Low to High Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.646	-

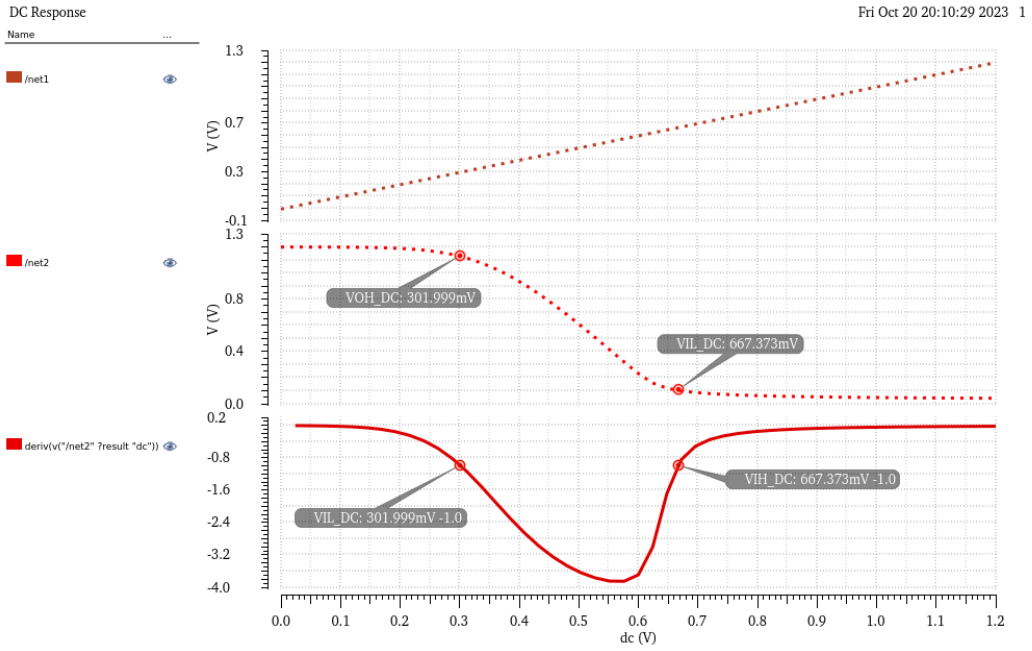
10) Transient Analysis

Figure 13: Resistive Inverter Transient analysis



11) DC analysis

Figure 14: Resistive Inverter DC analysis

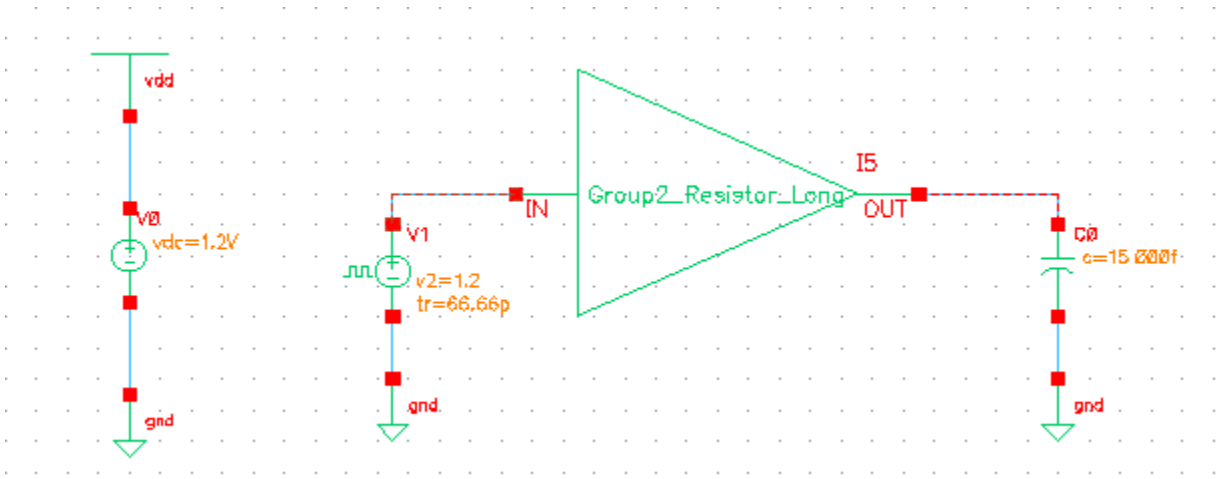


1) Cell Description: Long Resistive Load Inverter

The Long Resistive Load Inverter is a type of CMOS inverter that uses a passive resistive load instead of an active load. This acts as a digital logic gate that performs the logical NOT operation. The Long Resistive Load Inverter has one input and one output. When the input A is at a high logic level, the NMOS transistor is on (closed), and the PMOS transistor is off (open). This interrupts the current path through the resistive load, causing the output to be pulled to a low logic level.The Long Resistive Load inverter uses long transistor dimensions. The Long Resistive Load inverter is built using one NMOS and one PMOS transistor connected in series through their drains. The input of the Long Resistive Load inverter is connected to the gates of both transistors. The output of the Long Resistive Load transistor is connected to the drains of both PMOS and NMOS. The source for the NMOS is connected to ground and the source of PMOS is connected to the power supply (VDD). The Long Resistive Load inverter offers advantages in terms of power consumption and area efficiency compared to some other load configurations.

2) Cell Symbol:

Figure 15: Long resistive Inverter Cell symbol



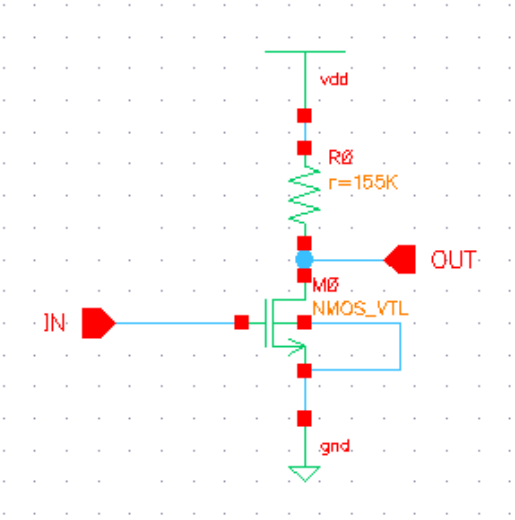
3) Cell Truth Table:

Table 19: Long Resistive Load Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 16: Long resistive Inverter schematic



5) Transistor Dimensions:

Table 20: Cell and Transistor Dimensions for Long Resistive Load Inverter

Cell Physical Dimensions		
	X	Y
Cell Dimension in µm	50	90
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
R1	155k Ω	-
NMOS_VTL	50	90

6) Input X: Output Rise Time Data t_r (ns):

Table 21: Transistor Rise Time for Long Resistive Load Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	1.964	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 22: Transistor Fall Time for Long Resistive Load Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.104	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 23: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for Long Resistive Load Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.077	-

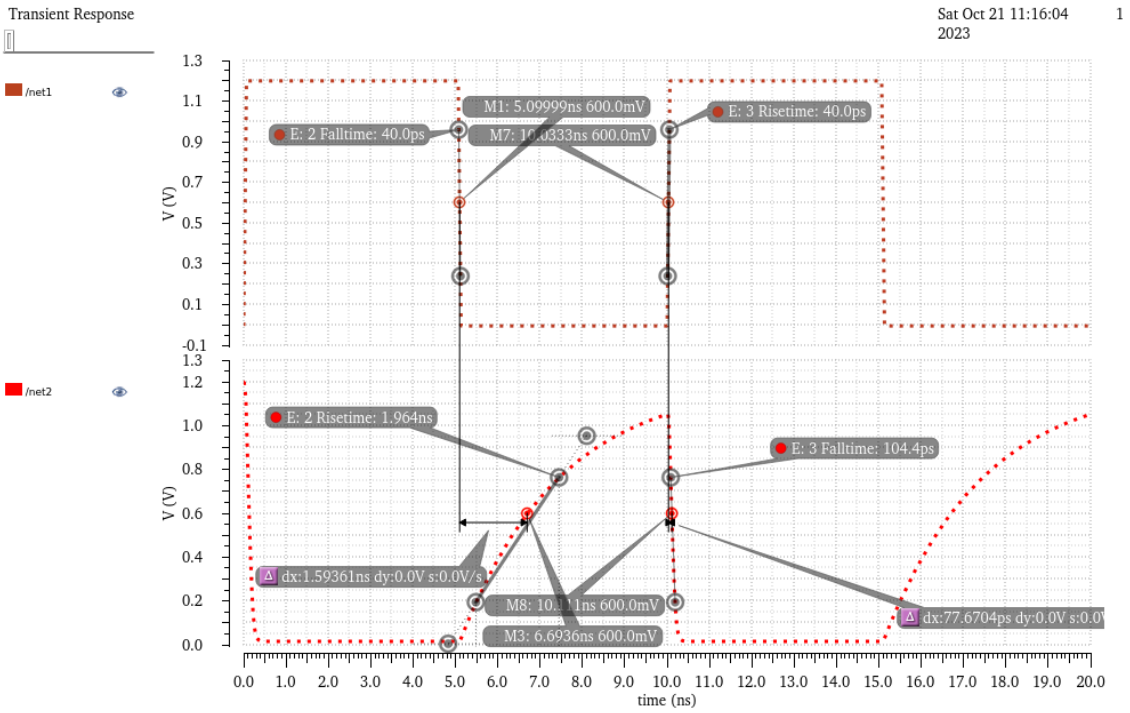
9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 24: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for Long Resistive Load Inverter

Data Worst Case Low to High Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	1.593	-

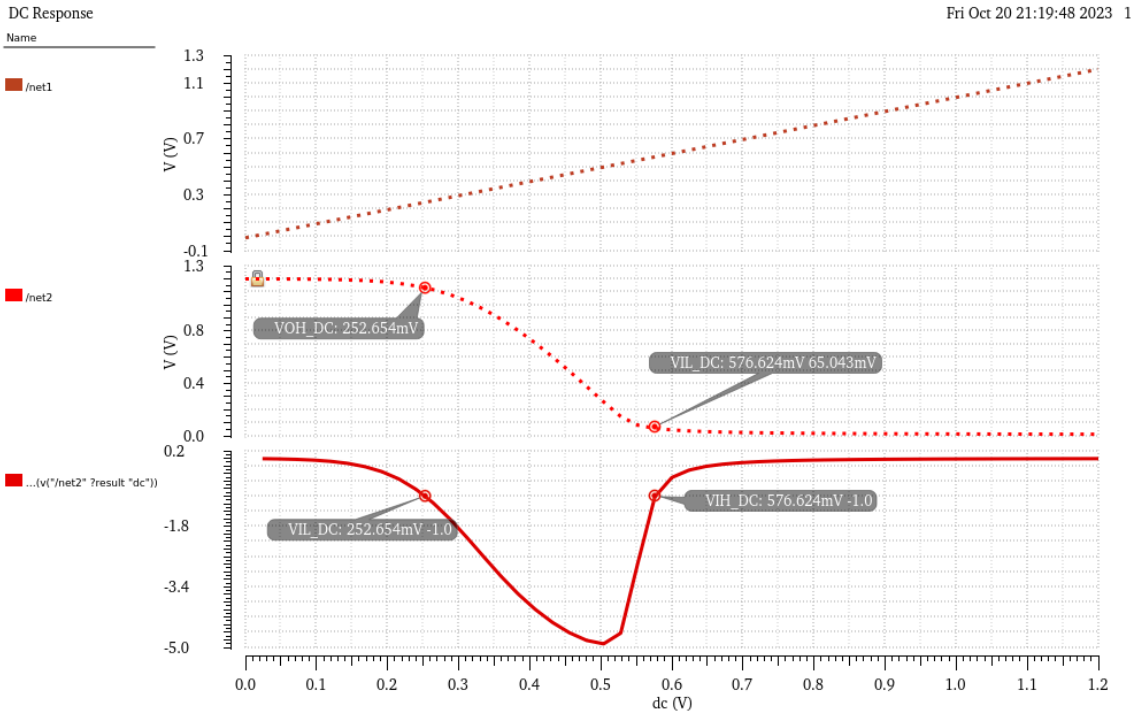
10) Transient Analysis

Figure 17: Long resistive Inverter Transient Analysis



11) DC analysis

Figure 18: Long resistive Inverter DC analysis



Ken Sutter
Phil Nevins
Cody Reid
Daniel Anishchenko

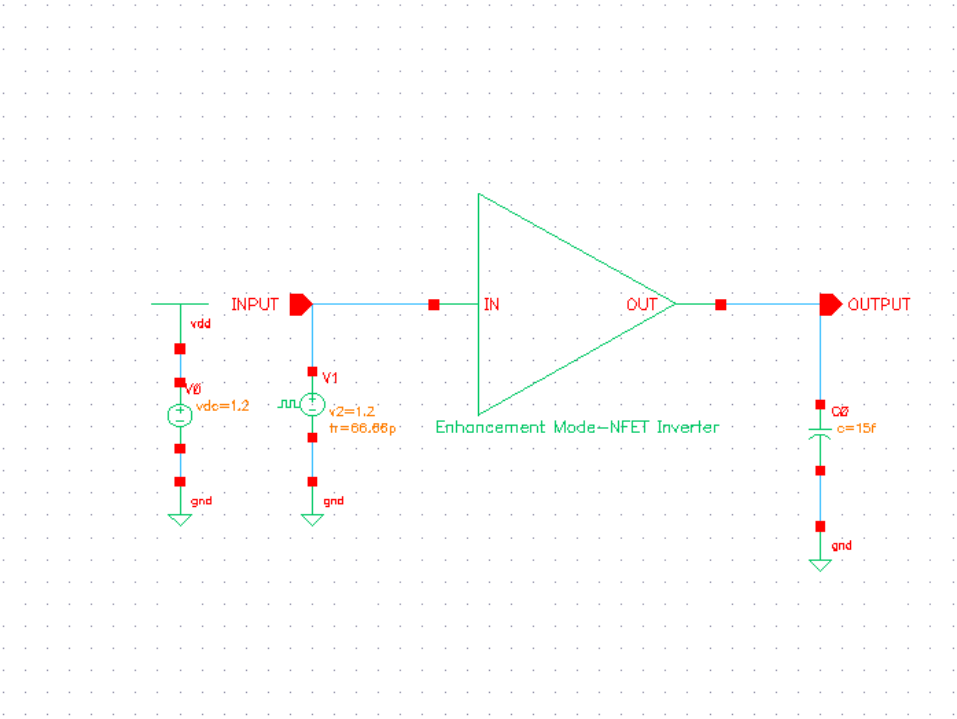
ECE-425 Lab 1 Enhancement Mode NFET Inverter

1) Cell Description: Enhancement Mode NFET Inverter (Short)

The Enhancement Mode NFET (N-Channel Field-Effect Transistor) inverter is a digital logic gate that uses a single N-channel MOSFET for inverting the input signal. The Enhancement Mode NFET inverter is a digital logic gate that performs the logical NOT operation. It has one input and one output. When input is high, output is low, and when input is low, output is high.When the input is at a high logic level, the NFET is on (closed). This allows current to flow from the drain to the source, connecting the output Y to ground (GND) and pulling it to a low logic level. The Enhancement Mode NFET is built with source connected to ground, drain connected to the output and the gate connected to the input. The Enhancement Mode NFET inverter is relatively simple and is often used in low-power applications or as part of more complex digital circuits. It is commonly found in integrated circuits where N-channel MOSFETs are used for their simplicity and efficient operation when driving a low impedance output.

2) Cell Symbol:

Figure 19: 350x90 Enhancement NFET Inverter TB Schematic



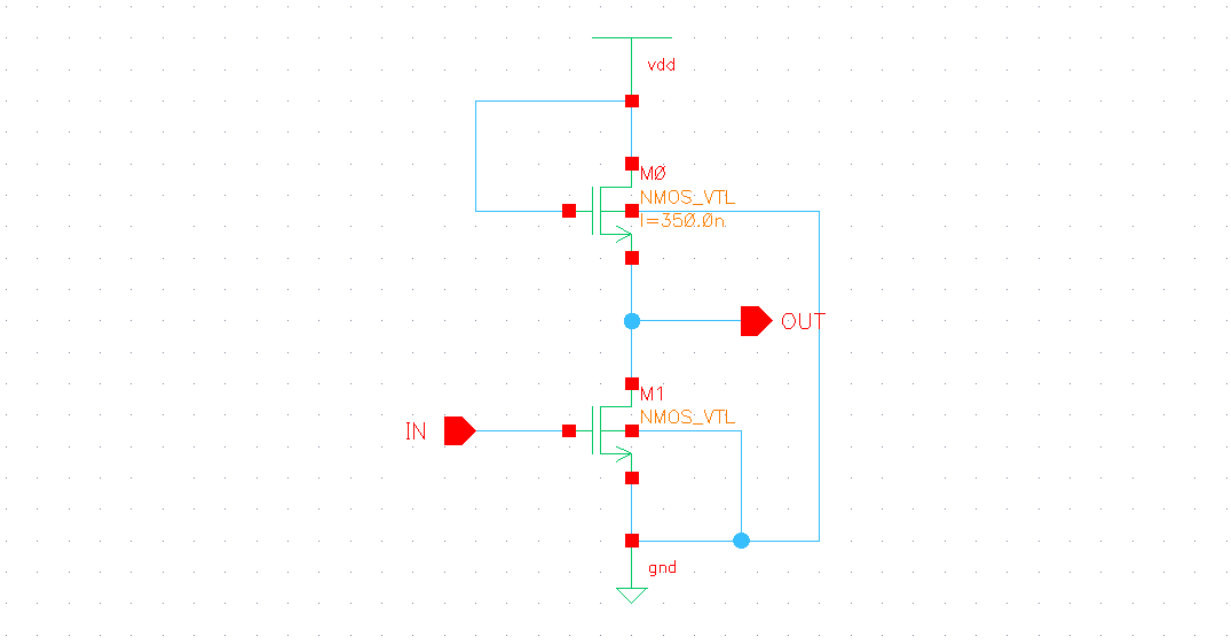
3) Cell Truth Table:

Table 25: Enhancement mode NFET Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 20: 350x90 Enhancement NFET Inverter TB Schematic



5) Transistor Dimensions:

Table 26: Cell and Transistor Dimensions Enhancement Mode NFET Inverter

Cell Physical Dimensions		
	X	Y
Cell Dimension in µm	50	90
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS_VTL (pull up)	50	90
NMOS_VTL (pull down)	350	90

6) Input X: Output Rise Time Data t_r (ns):

Table 27: Transistor Rise Time for Enhancement Mode NFET Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	1.241	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 28: Transistor Fall Time for Enhancement Mode NFET Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.07648	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 29: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for Enhancement Mode NFET Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.3516	-

9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 30: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for Enhancement Mode NFET Inverter

Data Worst Case High to Low Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.06284	-

10) Transient Analysis

Figure 21: 350x90 Enhancement NFET Inverter Transient - 1

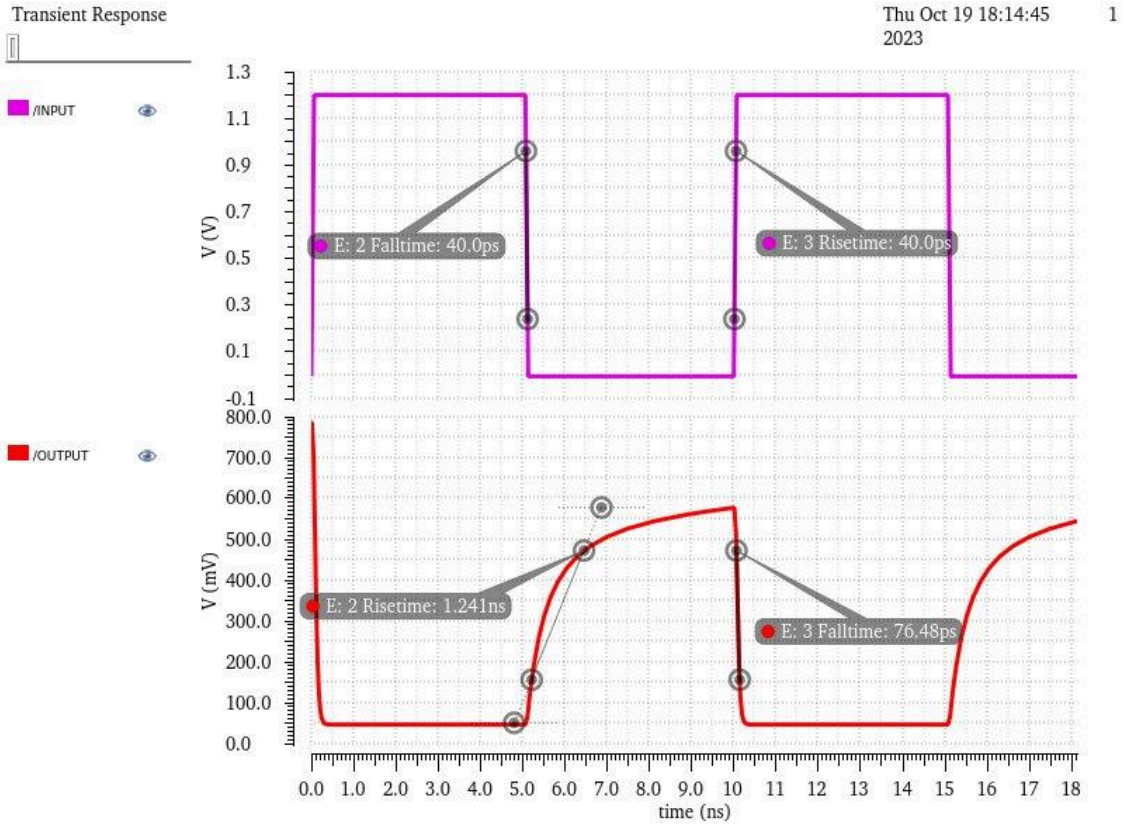
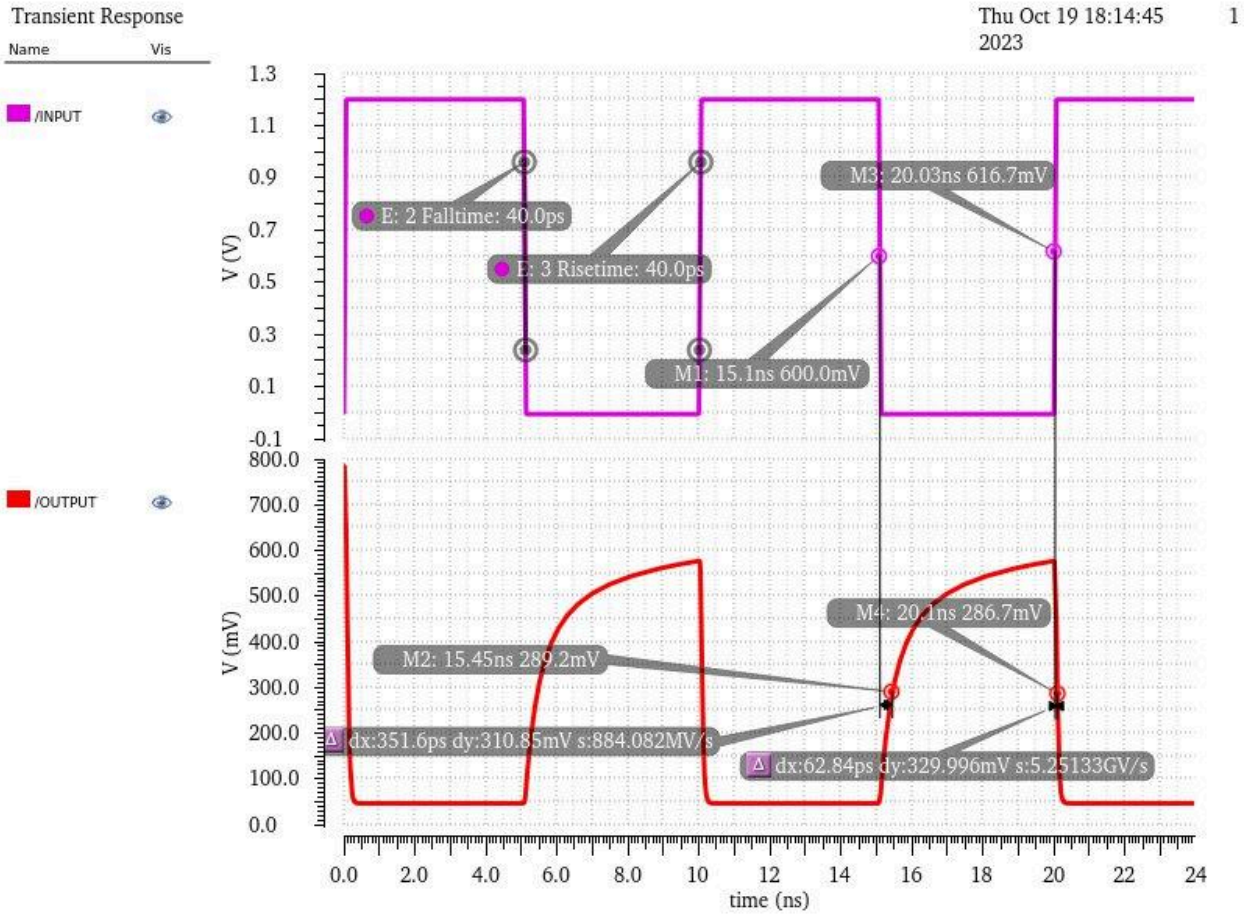
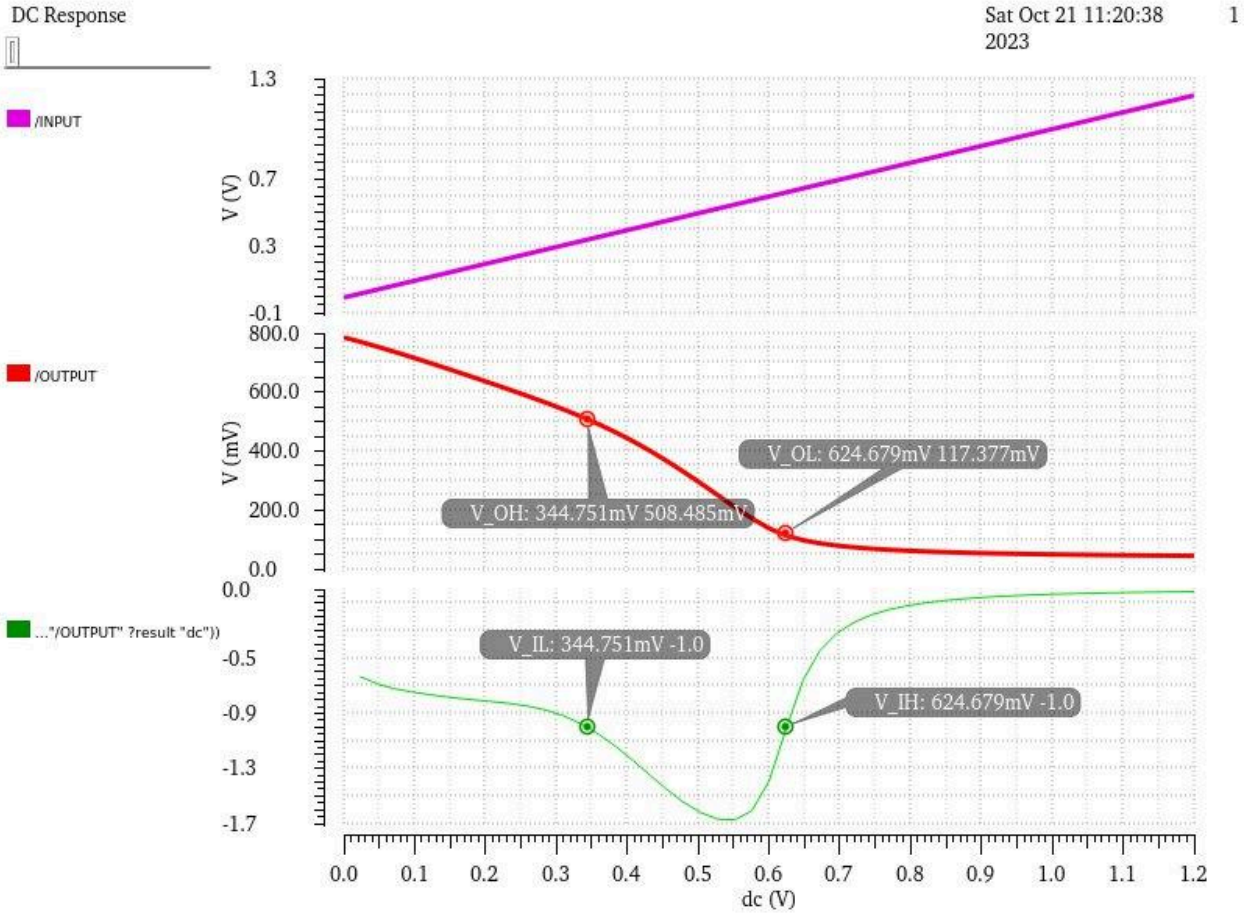


Figure 22: 350x90 Enhancement NFET Inverter Transient - 2



11) DC analysis

Figure 23: 350x90 Enhancement NFET Inverter DC Analysis

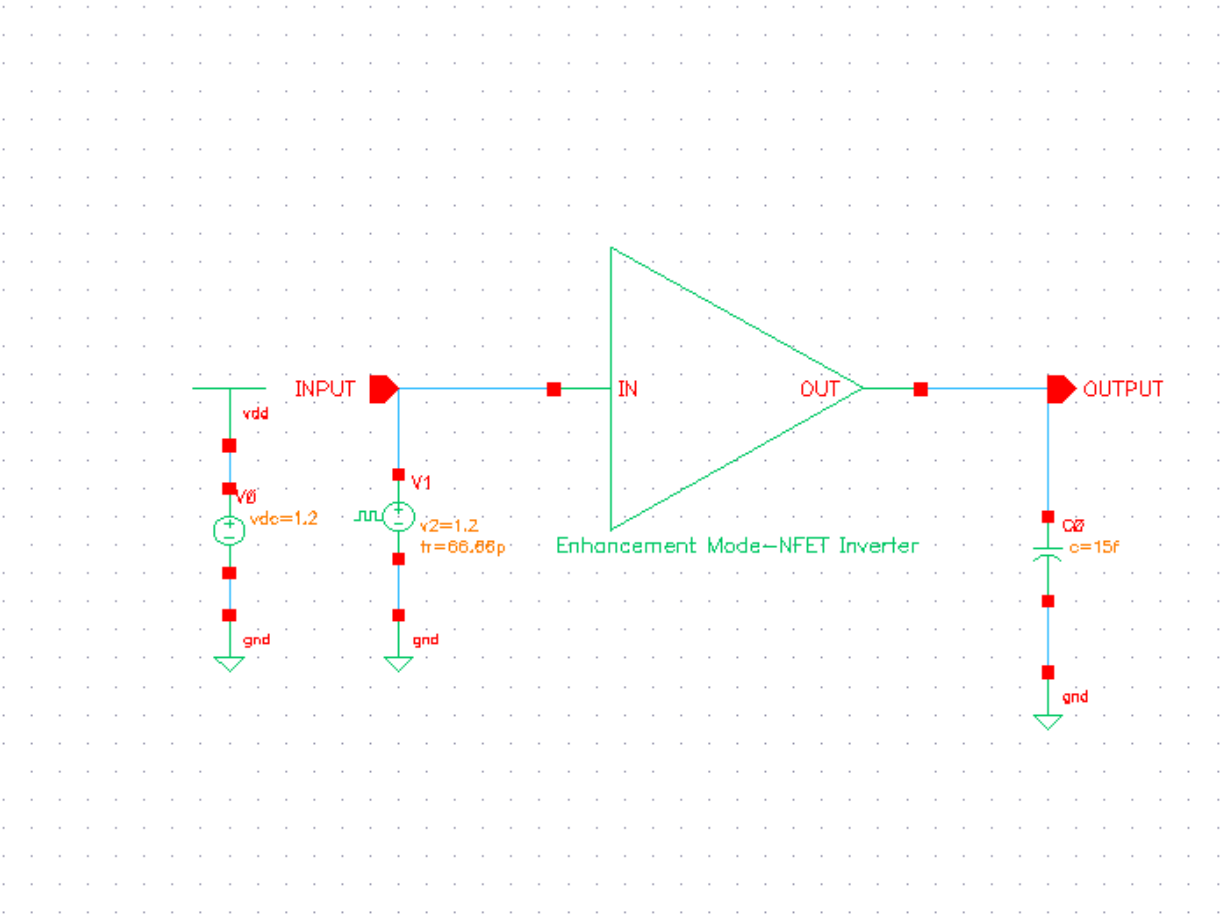


1) Cell Description: Long Enhancement Mode NFET Inverter (Long)

The Long Enhancement Mode NFET (N-Channel Field-Effect Transistor) inverter is a digital logic gate that uses a single N-channel MOSFET for inverting the input signal. The Long Enhancement Mode NFET inverter is a digital logic gate that performs the logical NOT operation. It has one input and one output. When the input is at a high logic level, the NFET is on (closed). This allows current to flow from the drain to the source, connecting the output Y to ground (GND) and pulling it to a low logic level. The Long Enhancement Mode NFET inverter uses long transistor dimensions. The Long Enhancement Mode NFET is built with source connected to ground, drain connected to the output and the gate connected to the input. The Long Enhancement Mode NFET inverter is relatively simple and is often used in low-power applications or as part of more complex digital circuits. It is commonly found in integrated circuits where N-channel MOSFETs are used for their simplicity and efficient operation when driving a low impedance output.

2) Cell Symbol:

Figure 24: 1000x90 Enhancement NFET Inverter TB Schematic



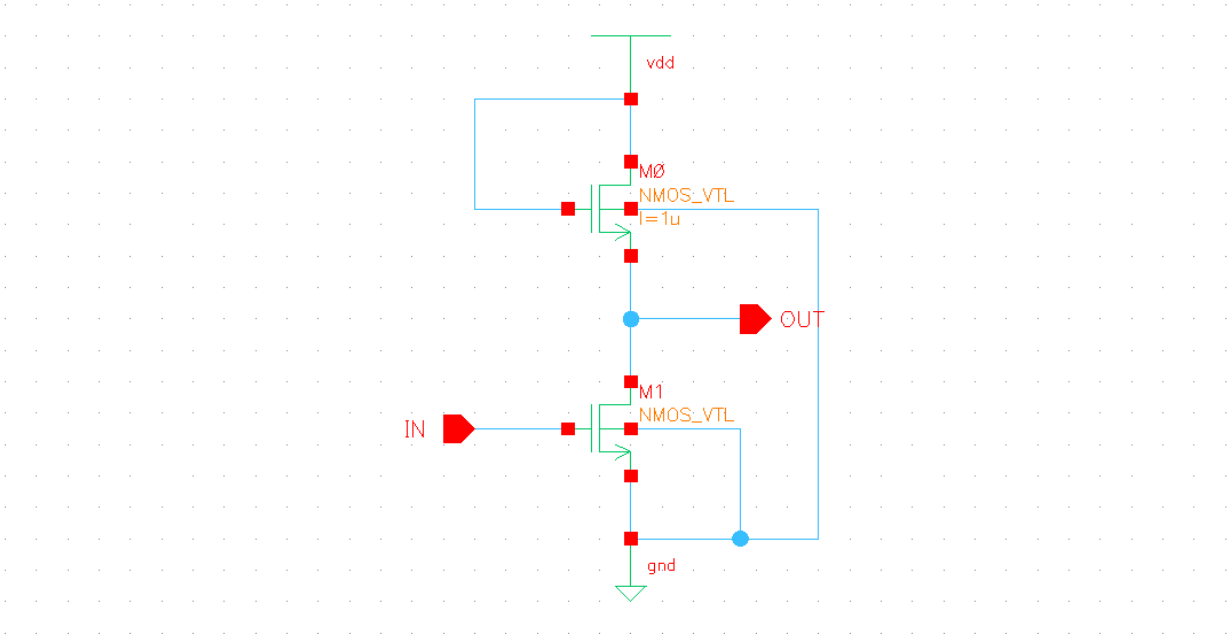
3) Cell Truth Table:

Table 31: Long Enhancement mode NFET Inverter Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {H,L}
0	H
1	L

4) Cell Schematic Diagram:

Figure 25: 1000x90 Enhancement NFET Inverter TB Schematic



5) Transistor Dimensions:

Table 32: Cell and Transistor Dimensions for Long Enhancement Mode NFET Inverter

Cell Physical Dimensions		
	X	Y
Cell Dimension in µm	50	90
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS_VTL (Pull Down)	50	90
NMOS_VTL (Pull Up)	1000	90

6) Input X: Output Rise Time Data t_r (ns):

Table 33: Transistor Rise Time for Long Enhancement Mode NFET Inverter

Input X: Output Rise Time Data t_r					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	1.998	-

7) Stack S, Input X: Output Fall Time Data t_f (ns):

Table 34: Transistor Fall Time for Long Enhancement Mode NFET Inverter

Input X: Output Fall Time Data t_f					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.08068	-

8) Data Worst Case Low to High Propagation Delay tp_{lh} (ns):

Table 35: Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for Long Enhancement Mode NFET Inverter

Data Worst Case Low to High Propagation Delay tp_{lh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.8283	-

9) Data Worst Case High to Low Propagation Delay tp_{hl} (ns):

Table 36: Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for Long Enhancement Mode NFET Inverter

Data Worst Case High to Low Propagation Delay tp_{hl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	-	-	-	0.05982	-

10) Transient Analysis

Figure 26: 1000x90 Enhancement NFET Inverter Transient - 1

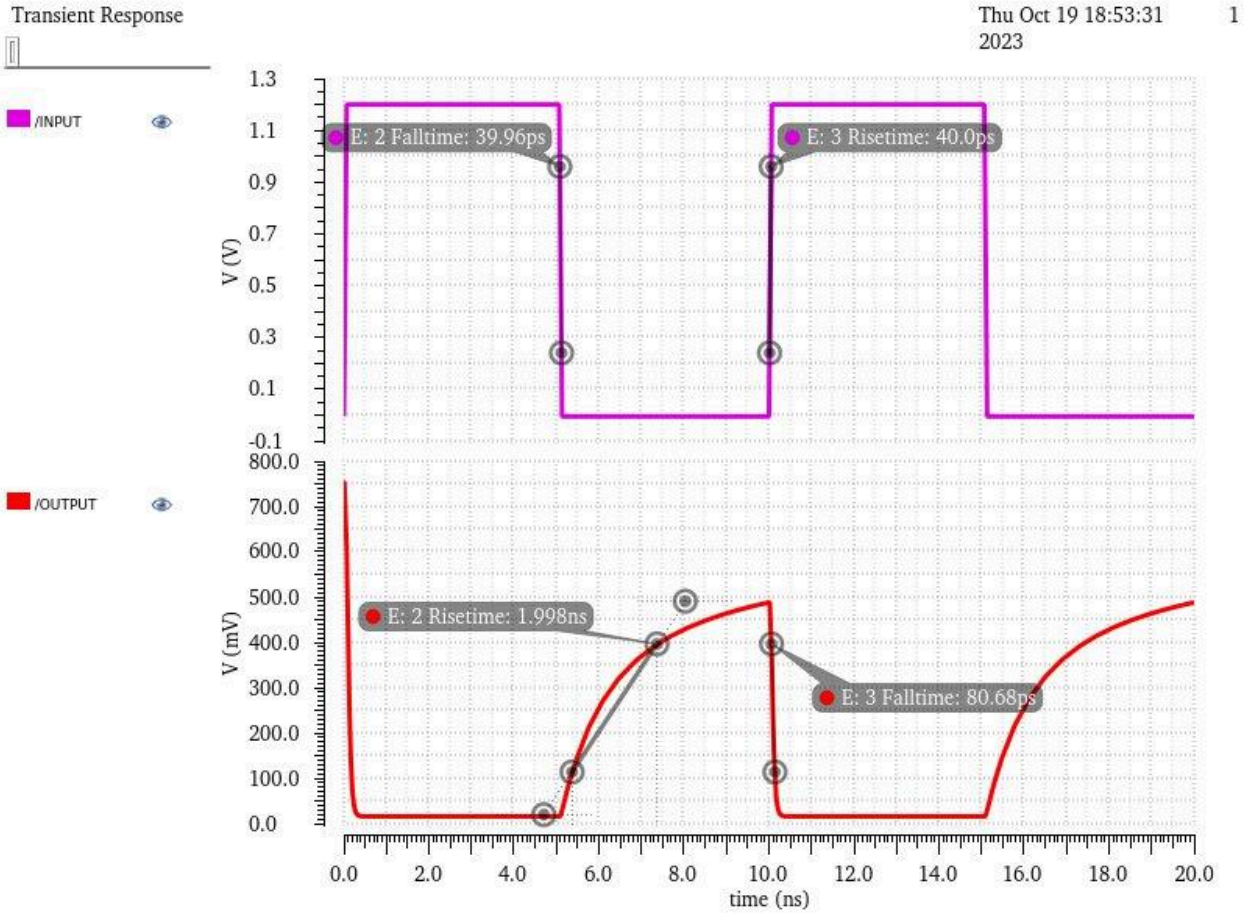
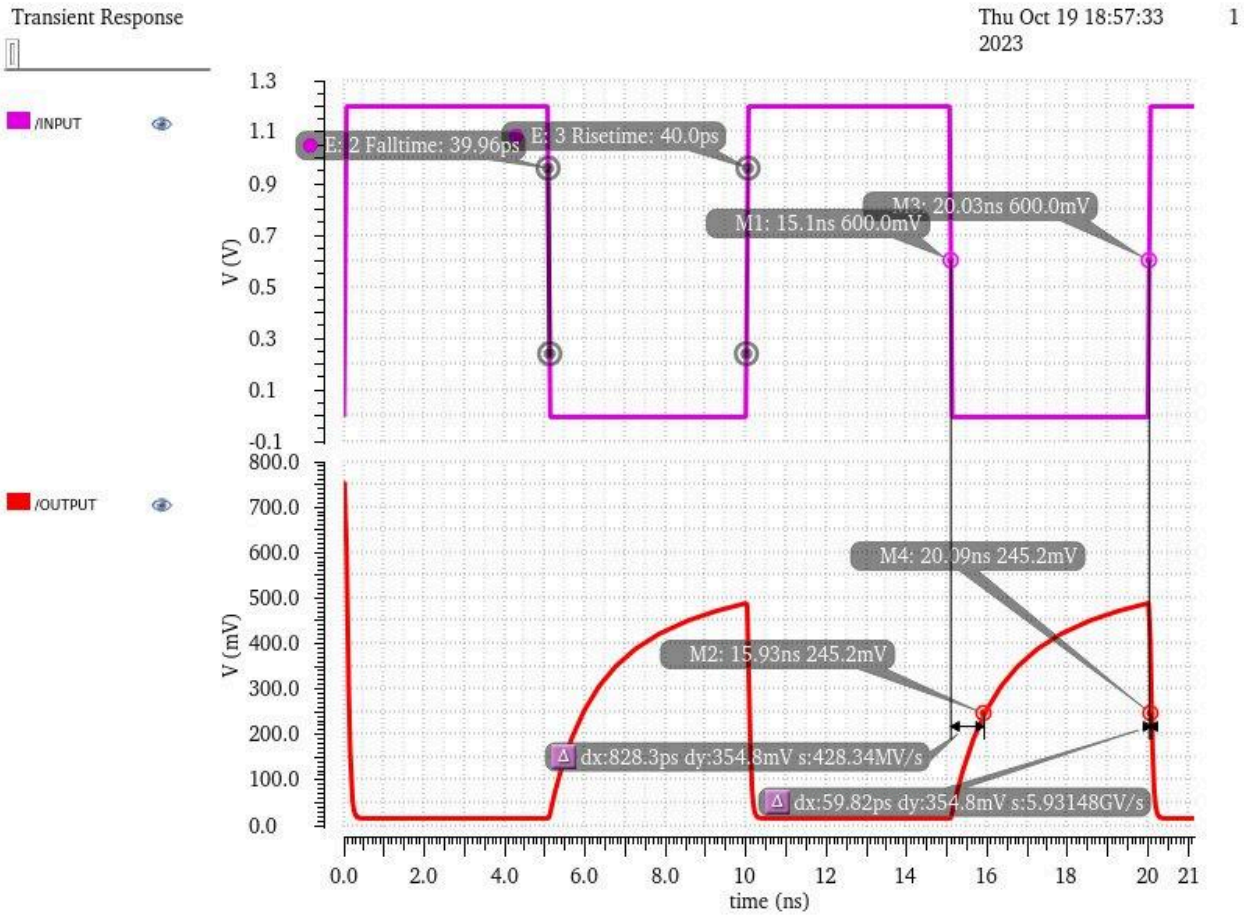
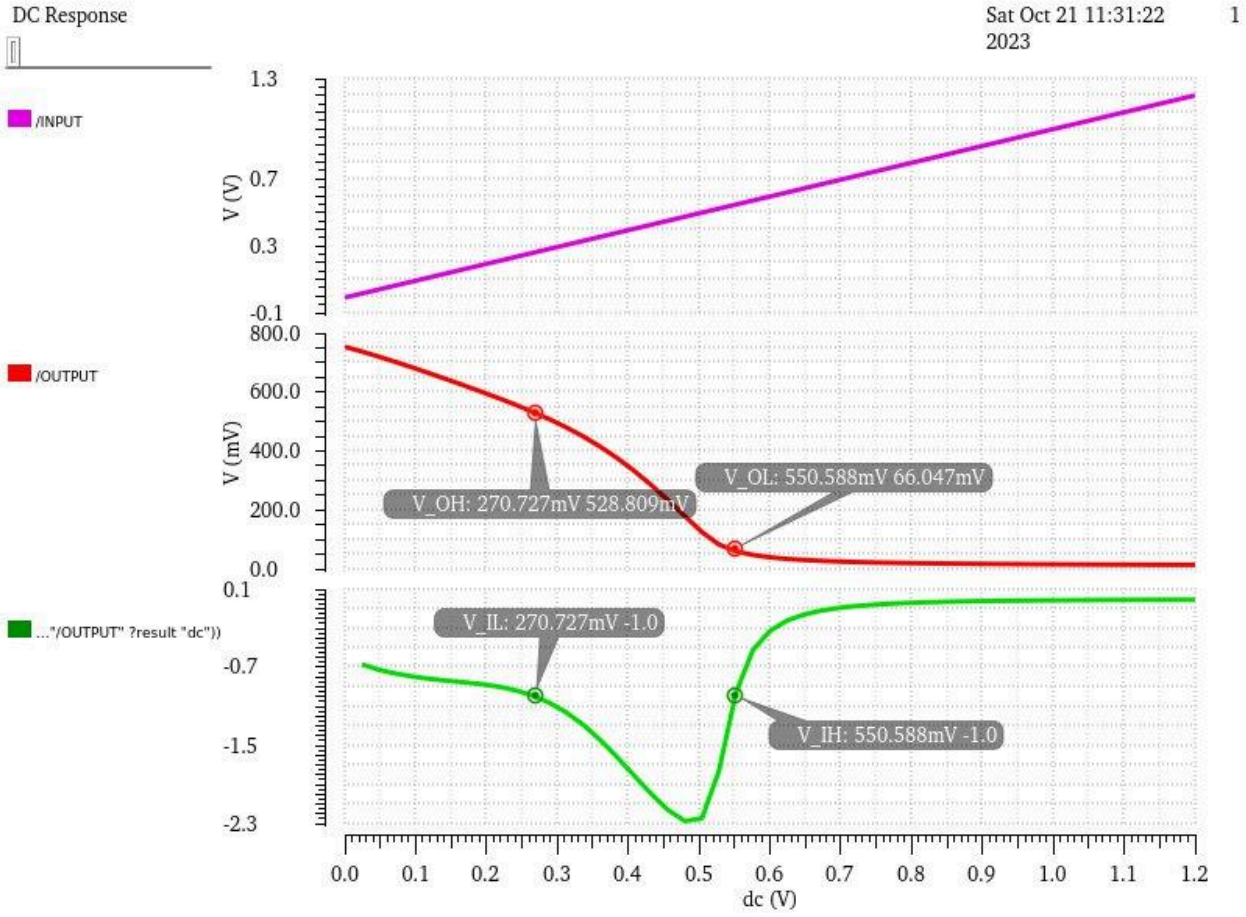


Figure 27: 1000x90 Enhancement NFET Inverter Transient - 2



11) DC analysis

Figure 28: 1000x90 Enhancement NFET Inverter DC



Ken Sutter
Phil Nevins
Cody Reid
Daniel Anishchenko

ECE-425 Lab 1 Questions and Comparison

Inverter comparison by performance

Prepare two additional tables (shown below) comparing the performance of the six inverters.

Table 37: Transient Analysis Comparison (ns)

Type	tp_{lh}	tp_{hl}	t_r	t_f
CMOS	0.0736	0.0937	0.3949	0.1155
CMOS_Wide	0.0292	0.0270	0.0943	0.0301
Enhancement mode NFET_Short	0.3516	0.06284	1.241	0.07648
Enhancement mode NFET_Long	0.8283	0.05982	1.998	0.08068
Resistive Load	1.593	0.6467	1.279	0.1185
Resistive Load_Long	0.077	1.593	1.964	0.104

Table 38: DC Analysis Comparison (mV)

Type	V_{IH_DC}	V_{IL_DC}	V_{OH_DC}	V_{OL_DC}
CMOS	613.3	369.374	369.374	613.3
CMOS_Wide	614.032	369.597	369.597	614.032
Enhancement mode NFET_Short	624.679	344.751	508.485	117.377
Enhancement mode NFET_Long	550.588	270.727	528.809	66.047
Resistive Load	667.373	301.999	301.999	667.373
Resistive Load_Long	576.624	252.654	252.654	576.624

Part 5: Questions for Lab 1

Answer the following questions and include them in your report.

1. Explain in your own words the variation of the DC output voltages VOH and VOL for the four inverters? In particular focus on the differences noted earlier in the NFET connected inverters and explain in your own words the variation of the switching times for all the inverters?

CMOS Inverter:

The VOH of a standard CMOS inverter is relatively close to the supply voltage; this makes it ideal for logic high levels. The VOL is close to the ground voltage, which is suitable for logic low levels. CMOS inverters generally offer fast switching times due to their complementary structure.

CMOS Wide Inverter:

This is a variation of the CMOS inverter with wider transistors, which can help reduce resistive losses and improve performance. VOH and VOL typically remain close to VDD and GND, similar to the standard CMOS inverter. The wider transistors can lead to slightly faster switching times and better performance.

NFET Resistive Load Inverter:

The VOH of an NFET resistive load inverter may be lower than the supply voltage VDD due to the voltage drop across the load resistor. The VOL is close to GND. These inverters tend to have slower switching times compared to CMOS inverters because the load resistor introduces additional capacitance.

Long NFET Resistive Load Inverter:

Similar to the NFET resistive load inverter but with longer NFET transistors. VOH and VOL are affected similarly to the standard NFET resistive load inverter. Longer NFET transistors can further increase the switching times due to their increased capacitance.

NFET Enhancement Mode Inverter:

The VOH of an NFET enhancement mode inverter is typically lower than VDD due to the voltage drop across the NFET transistor when it's on. The VOL is close to GND. These inverters tend to have slower switching times compared to CMOS inverters because of the characteristics of enhancement-mode transistors.

Long NFET Enhancement Mode Inverter:

Same as the NFET enhancement mode inverter but with longer NFET transistors. VOH and VOL are affected similarly to the standard NFET enhancement mode inverter. Longer NFET

transistors can further increase the switching times due to their increased capacitance and the nature of enhancement-mode transistors.

The key differences in VOH and VOL among these inverters are from their transistor configurations and load types. The switching times are affected by transistor characteristics, gate capacitance, and resistive or capacitive loads. CMOS-based inverters tend to offer faster switching times and more defined high and low voltage levels compared to NFET-based inverters.

2. List out the major drawbacks and benefits of using a NFET load and resistor for signal inversion from area, VTC (Voltage Transfer Characteristic), noise margin, leakage and fabrication point of view. Why do you think CMOS has become so popular in recent times?

Using an NFET load and a resistor for signal inversion in digital circuits, as opposed to CMOS logic, has both advantages and disadvantages in terms of area, VTC, noise margin, leakage, and fabrication.

The NFET load and resistor for signal inversion:

NFET load and resistor configurations can be smaller in size compared to CMOS inverters. This is helpful when you have an area constraint issue. The circuit design using an NFET load and resistor is simpler, it uses fewer components and can create a more simplified design. NFET inverters can provide better performance in analog applications, as they have a more linear voltage transfer characteristic (VTC) compared to CMOS

Disadvantages of NFET load and resistor for signal inversion:

NFET load inverters typically have lower noise margins compared to CMOS, making them more susceptible to noise interference and signal degradation. NFET transistors can have higher leakage current compared to their CMOS counterparts, leading to higher static power consumption. NFET load inverters may have slower switching speeds due to the higher resistance of the load resistor, which can be a downside in high-speed digital applications. NFET inverters are not ideal for digital logic because of their reduced noise margins and slower switching speeds. CMOS is much more efficient for this application.

Why CMOS has become popular in recent times:

CMOS technology has gained popularity and become the main choice for digital integrated circuits. CMOS logic is known for its power efficiency. It consumes little power when not switching. CMOS logic provides high noise margins, making it work well against noise and is great for high-performance digital applications CMOS can achieve high-speed operation, making it useful for a wide range of digital applications. CMOS technology can be scaled down to smaller feature sizes, allowing for the integration of a large number of transistors on a single chip, which is essential for modern semiconductor technology.

3. What happens if PMOS and NMOS are interchanged in an inverter connection? Where should you measure the output to get the desired inverted signal after interchanging their positions?

If you interchange the PMOS and NMOS transistors in an inverter connection, it reverses the behavior of the circuit. Instead of producing a logical NOT output, it will produce a logical NOT of the original input signal. In other words, it will act as a buffer, or non-inverting gate. To measure the output of the circuit to get the inverted signal after switching the positions of the PMOS and NMOS transistors, you should measure the voltage at the output node of the circuit. This is the same place the output signal is taken in a normal inverter. The voltage at the output node will be the logical NOT of the input signal, and it will provide the desired inverted output.

4. What are the roles and responsibilities of each member of your lab team? Who did what part of the lab?

Cody Reid: Configured and analyzed both CMOS 50x90 and CMOS 50x360 circuits. Assisted with lab write up, figures, and formatting.

Daniel Anishchenko: Built and simulated the resistive circuits as well worked on the formal report.

Ken Sutter: Working on formal report, answering lab questions, doing circuit calculations, documenting team work, helping design circuits.

Phil Nevins: Built and simulated enhancement mode NFET as well as formal report