Portland State
UNIVERSITY

ECE 425 Lab 2: CMOS Compound Gates

Authors:
Cody Reid
Ken Sutter
Phil Nevins
Daniel Anishchenko

Cell Description

A complementary metal-oxide-semiconductor (CMOS) compound gate is a fundamental building block in digital electronic circuits that serves a specific logic function by combining basic gates, typically NAND and NOR gates. They are implemented using CMOS technology. These compound gates are designed to provide efficient and optimized solutions for specific logic operations and are commonly used in the design of integrated circuits, such as microprocessors, memory chips, and various other digital devices.

Cell Symbol

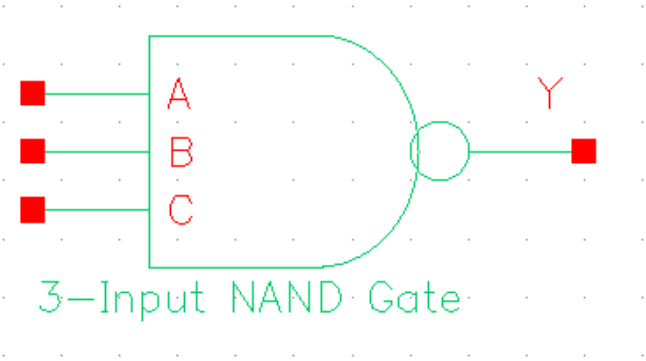


Figure 1: Cell Symbol

Cell Truth Table

CMOS Compound Gate Truth Table			
A (Input)	**B (Input)**	**C (Input)**	**Y (Output)**
0	**0**	**0**	**1**
0	**0**	**1**	**1**
0	**1**	**0**	**1**
0	**1**	**1**	**1**
1	**0**	**0**	**1**
1	**0**	**1**	**1**
1	**1**	**0**	**1**
1	**1**	**1**	**0**

Cell Schematic Diagram

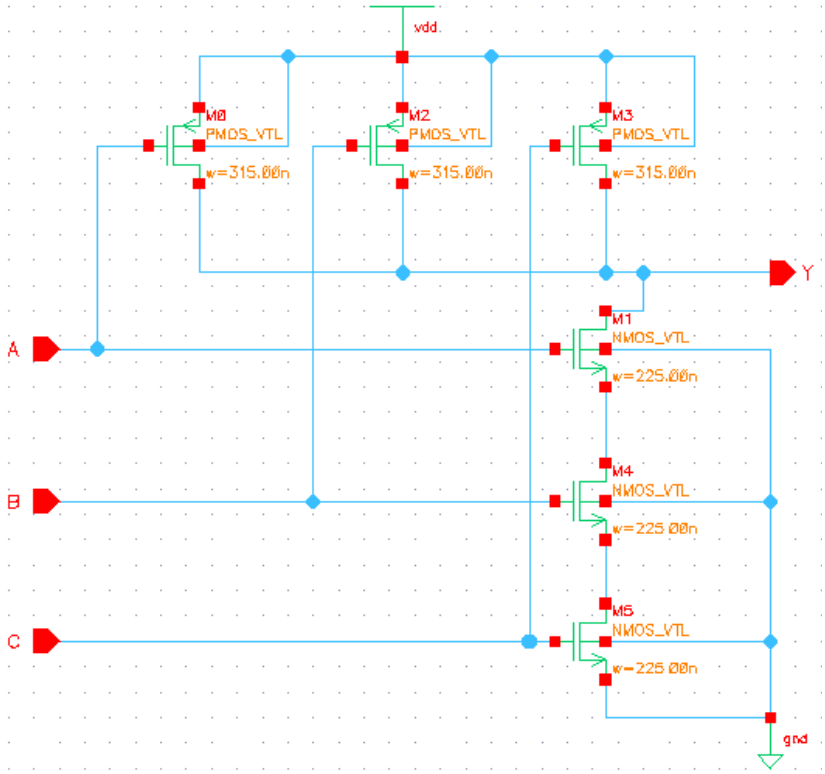


Figure 2: Cell Schematic

Cell Layout Diagram and Dimension

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS_VTL	50	315
NMOS_VTL	50	225

Fan Out 4 (Tuned using FO4)

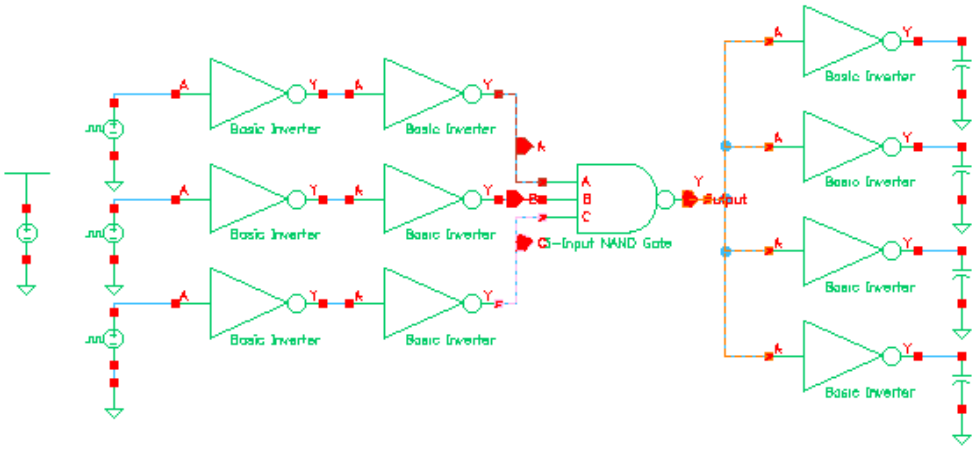


Figure 3: FanOut 4 (Tuned DUT using FO4) DUT Test Bench

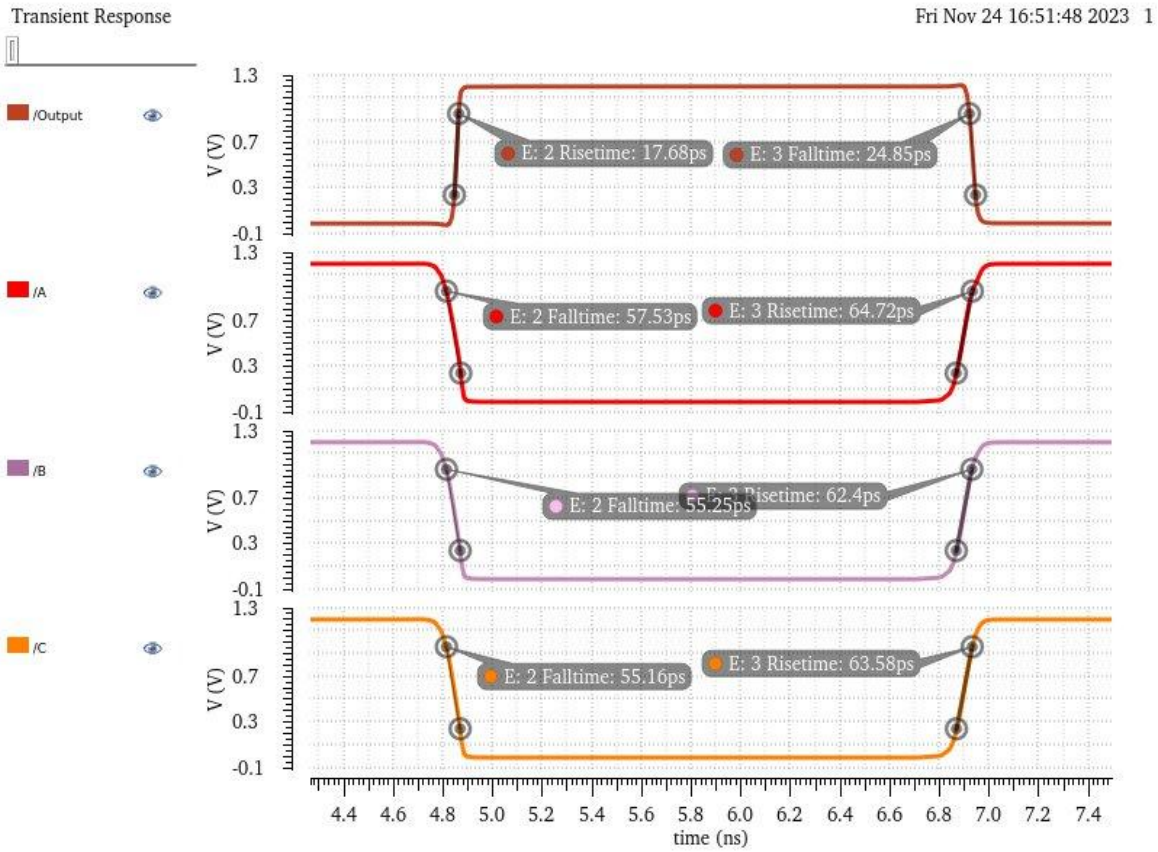


Figure 4: FanOut 4 (Tuned DUT using FO4) DUT Rise & Fall Time

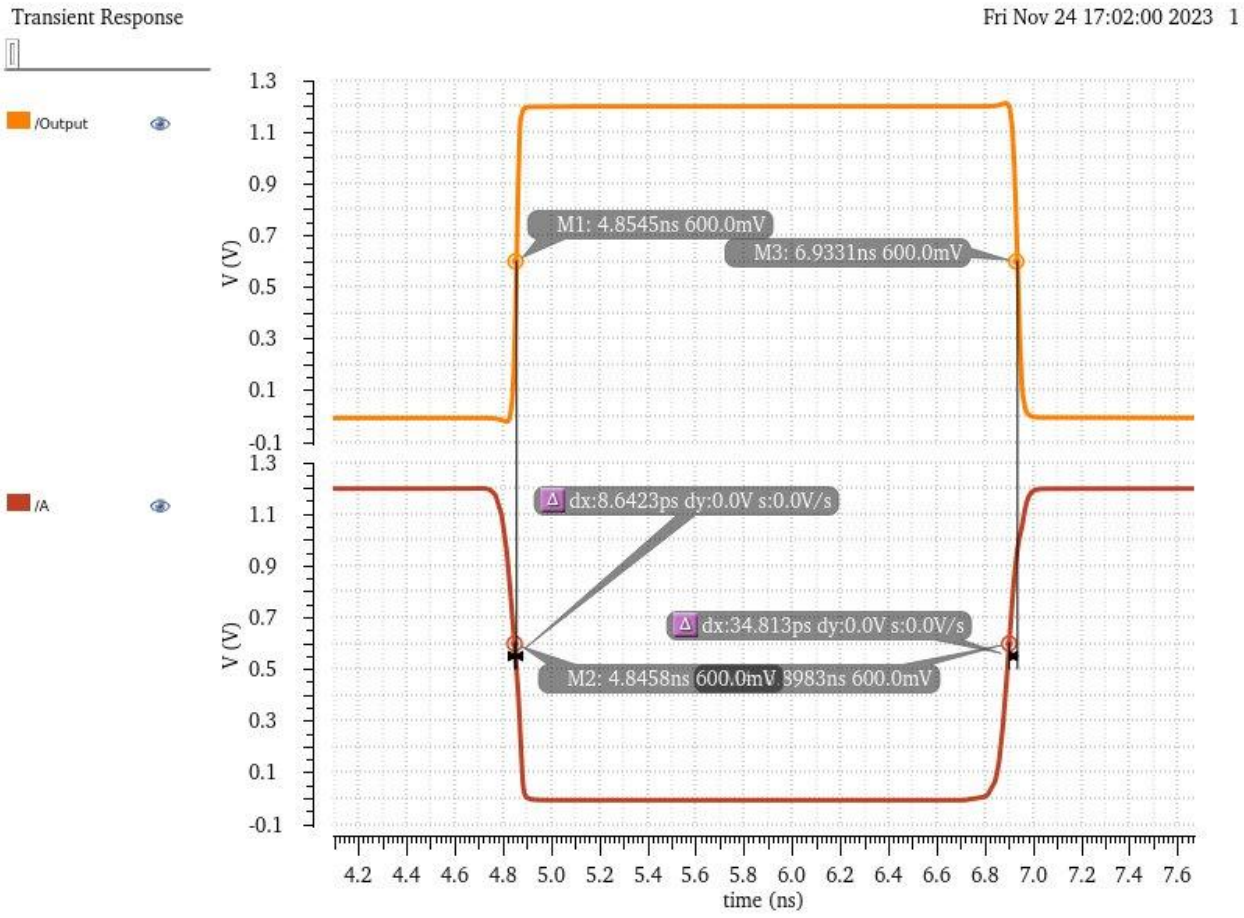


Figure 5: FanOut 4 (Tuned DUT using FO4) DUT T_plh & T_phl

Fan Out 0

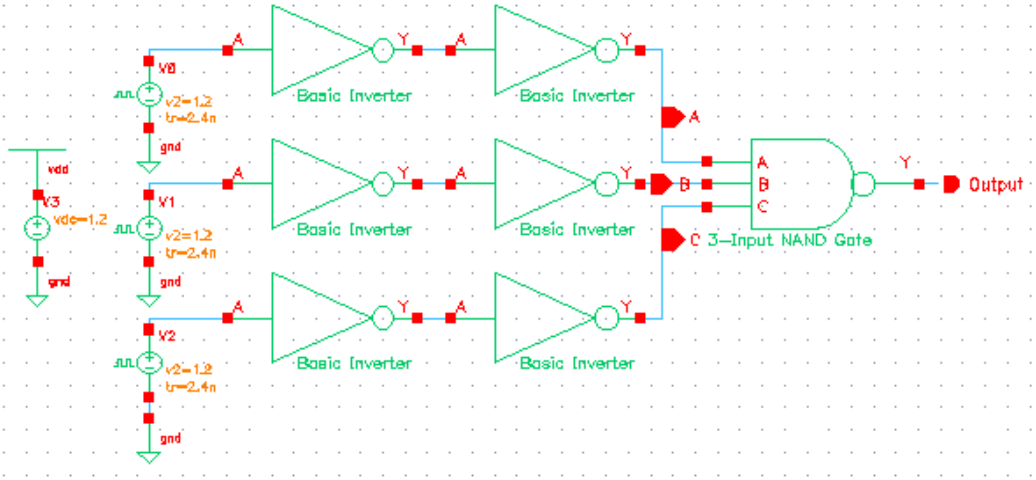


Figure 6: FanOut 0 DUT Test Bench

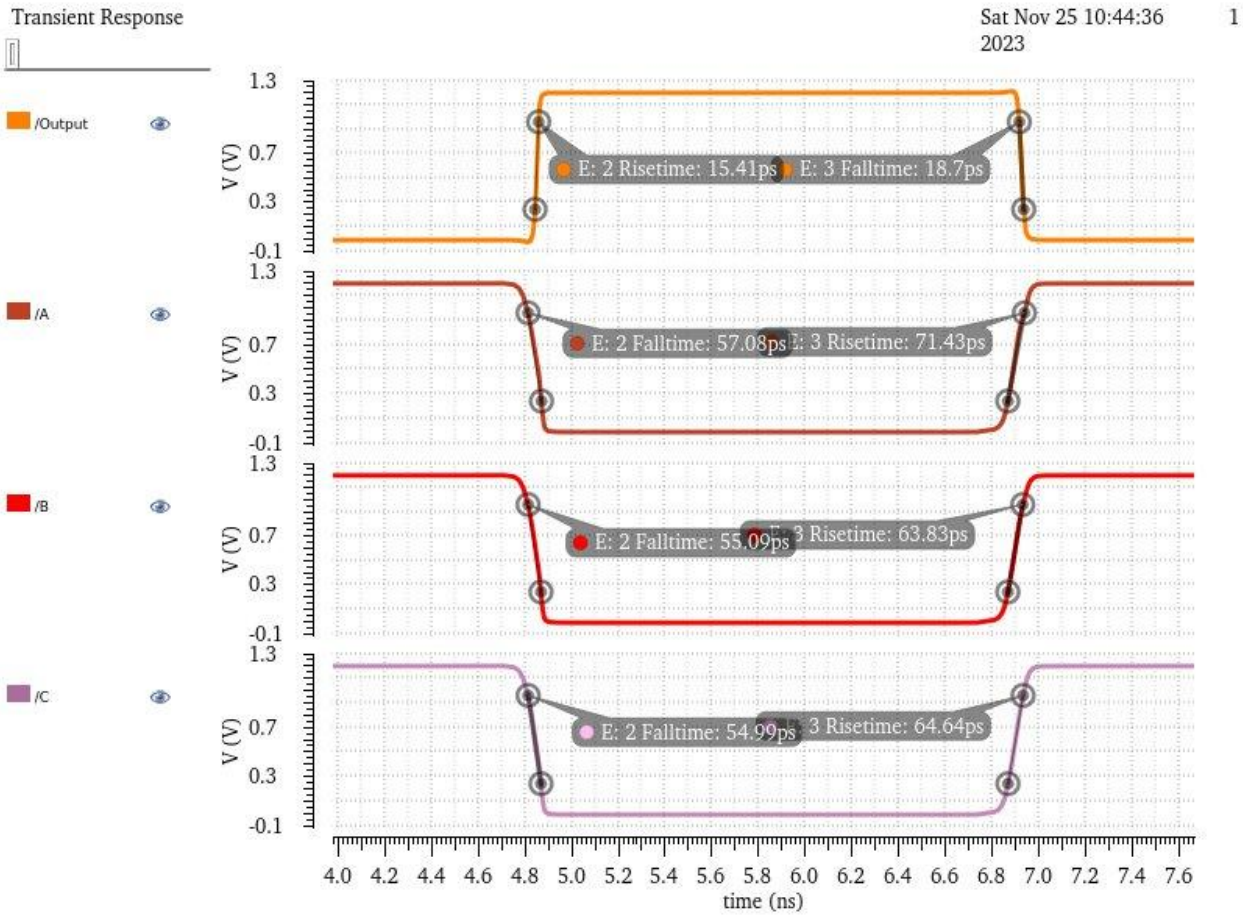


Figure 7: FanOut 0 DUT Rise & Fall Time

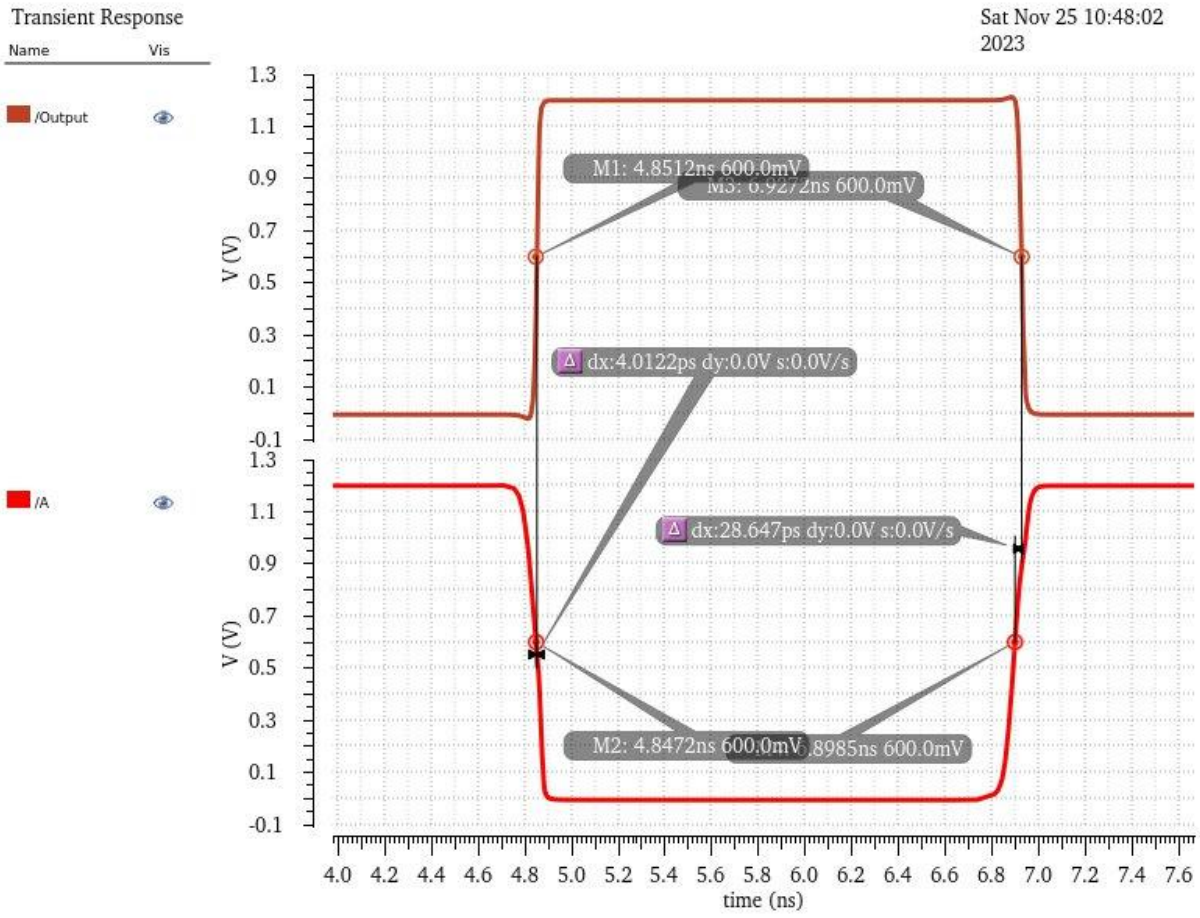


Figure 8: FanOut 0 DUT T_plh & T_phl

Fan Out 1

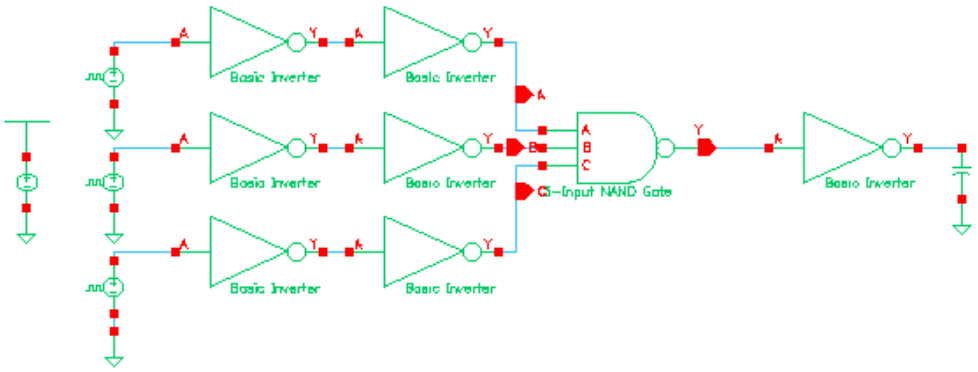


Figure 9: FanOut 1 DUT Test Bench

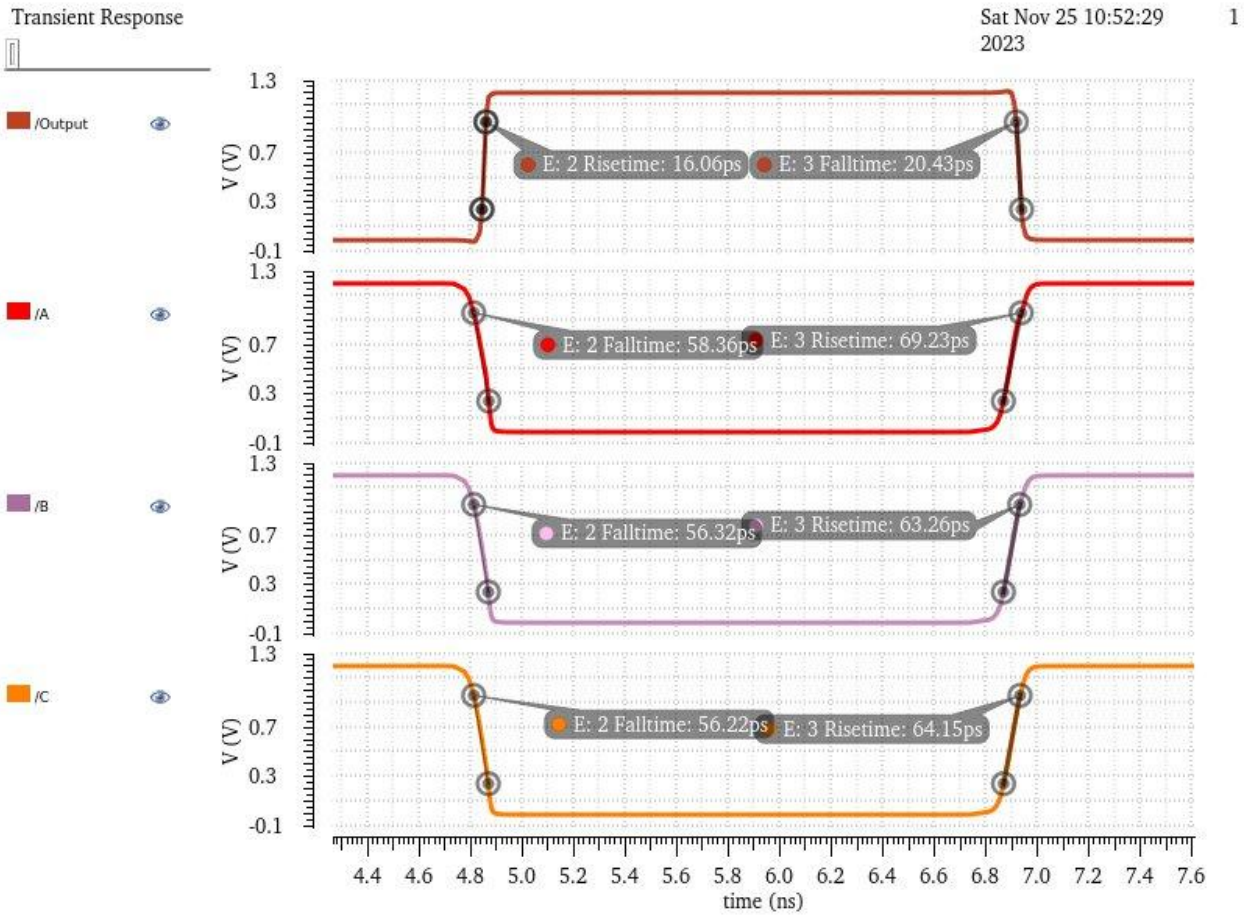


Figure 10: FanOut 1 DUT Rise & Fall Time

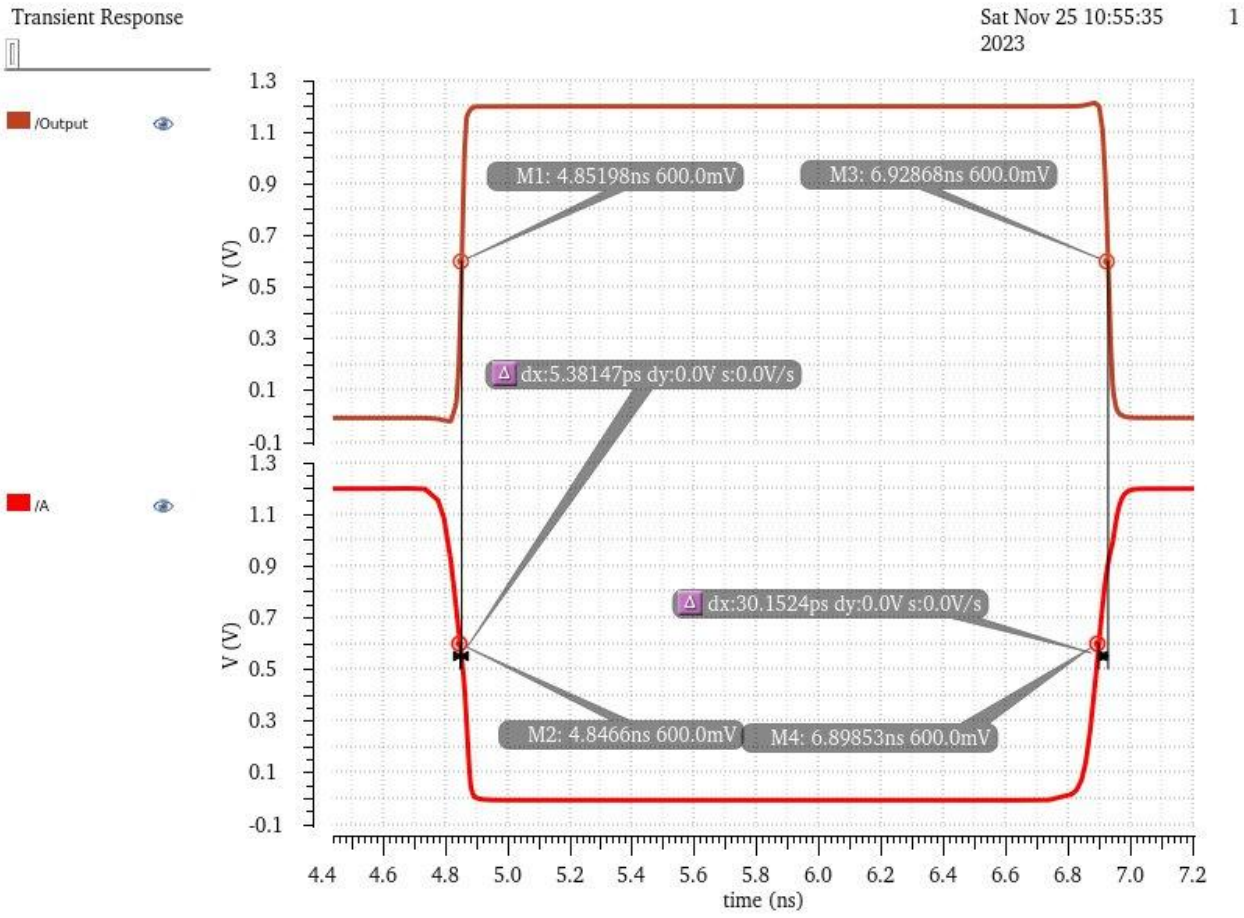


Figure 11: FanOut 1 DUT T_plh & T_phl

Fan Out 2

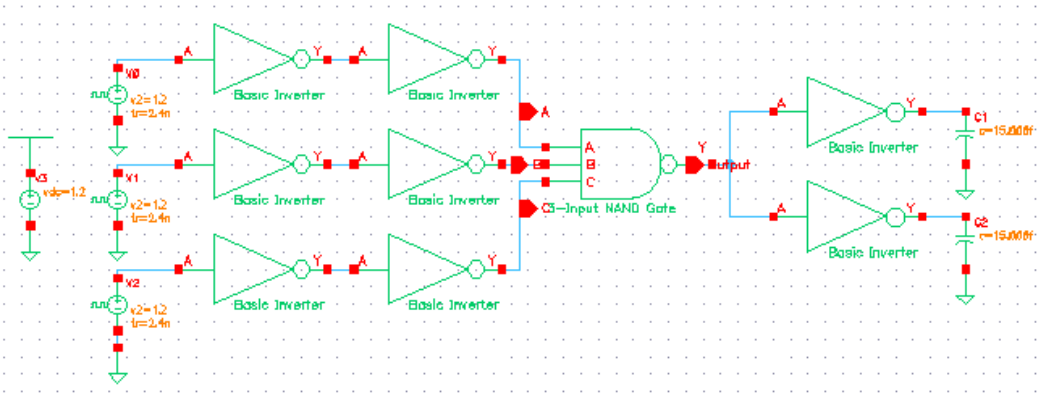


Figure 12: FanOut 2 DUT Test Bench

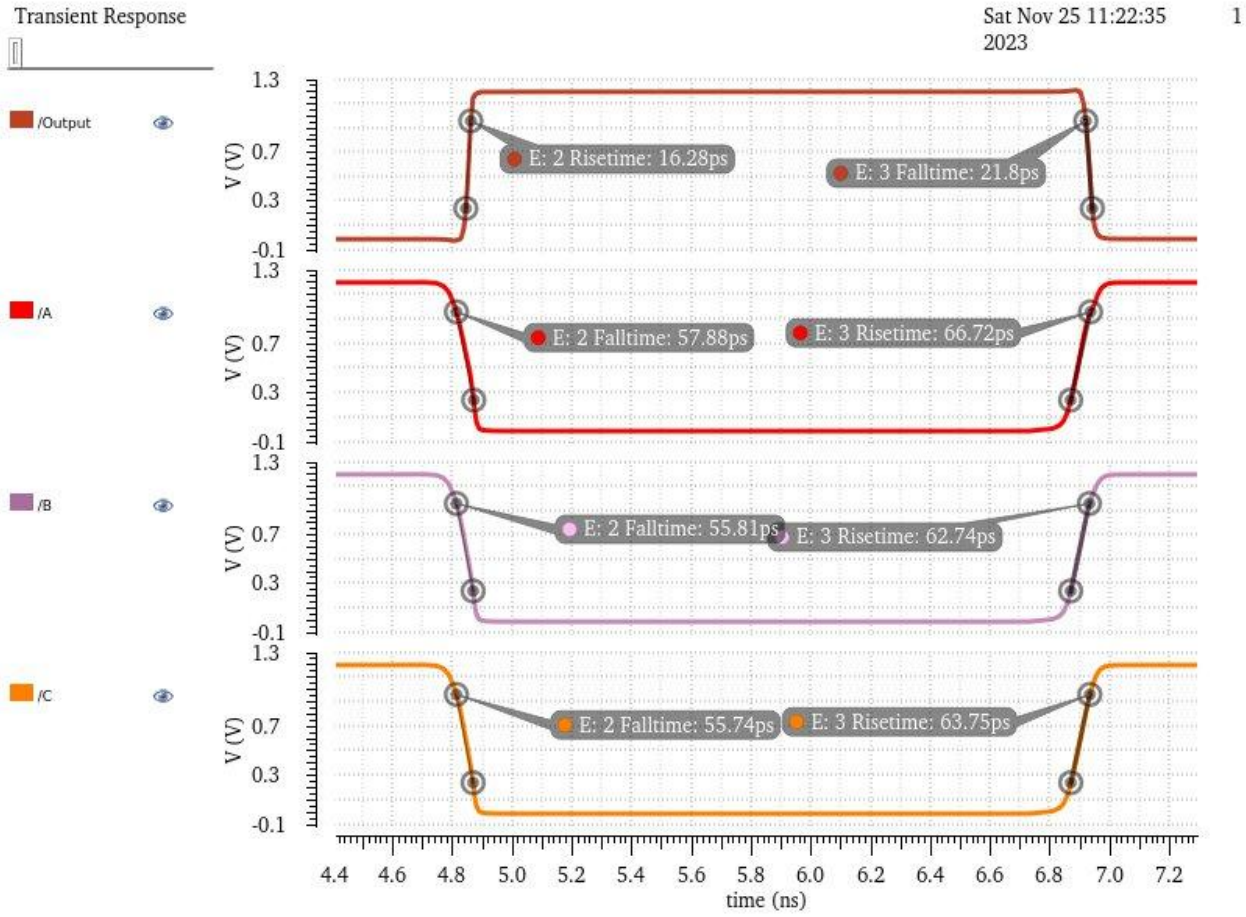


Figure 13: FanOut 2 DUT Rise & Fall Time

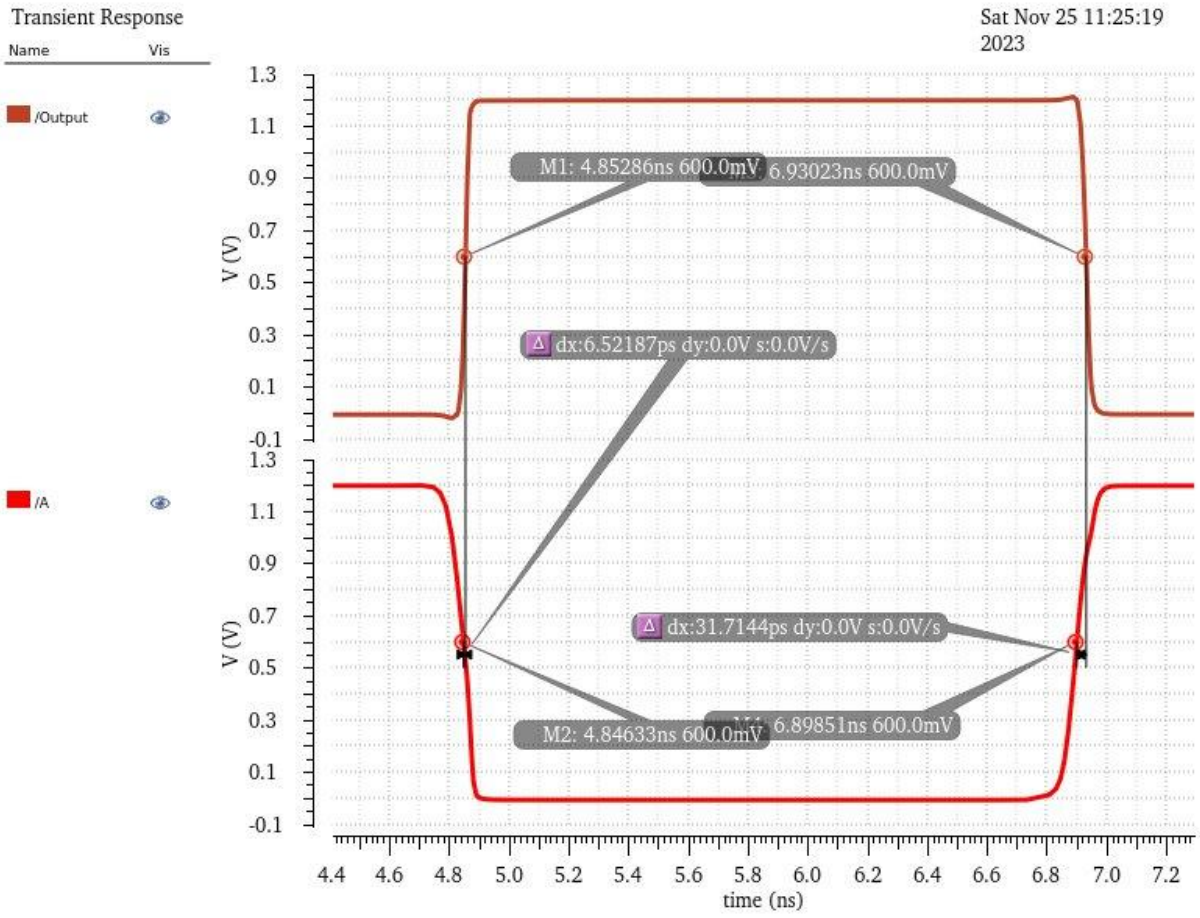


Figure 14: FanOut 2 DUT T_plh & T_phl

Fan Out 8

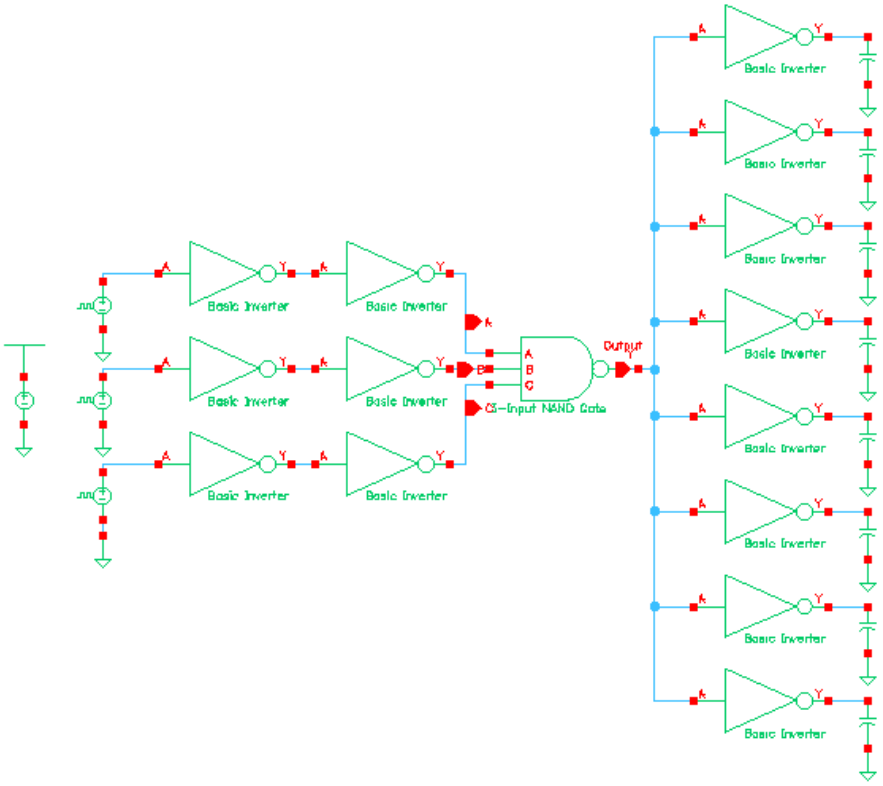


Figure 15: FanOut 8 DUT Test Bench

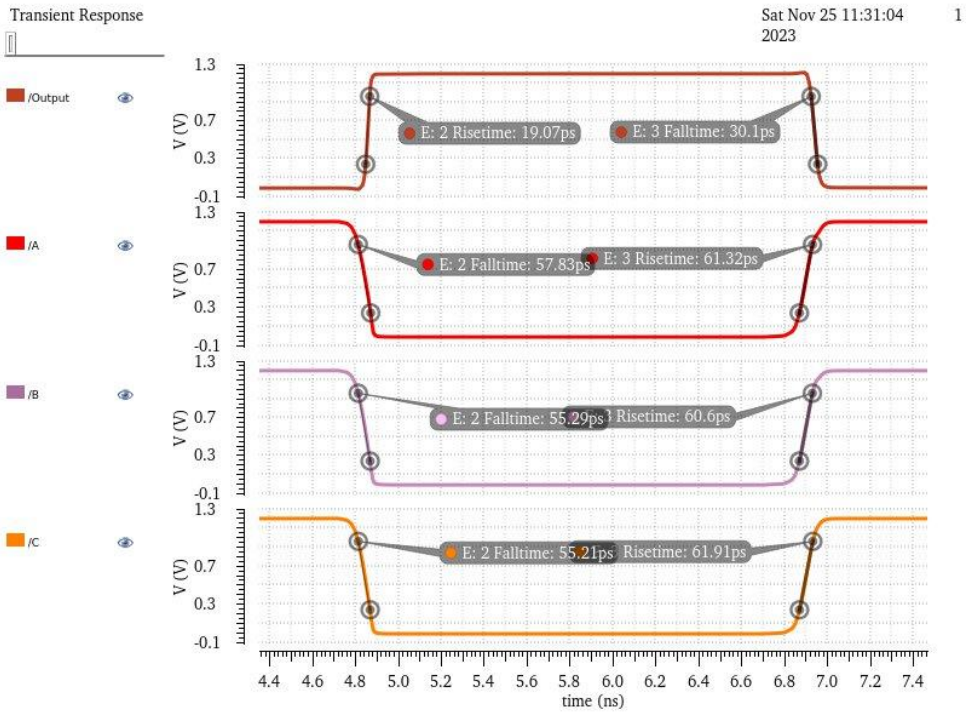


Figure 16: FanOut 8 DUT Rise & Fall Time

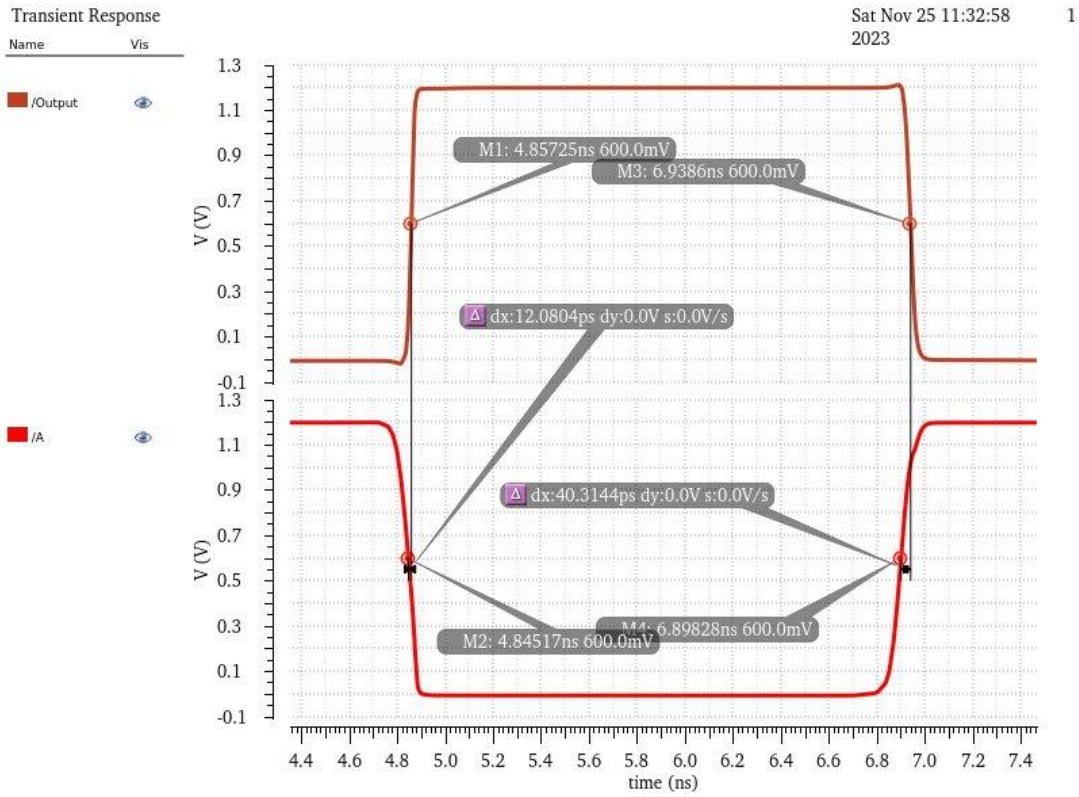


Figure 17: FanOut 8 DUT T_plh & T_phl

Rise and Fall Times

Transistor Rise Time for CMOS Compound Gate

Input A: Output Rise Time Data t_r (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	71.43	69.23	66.72	64.72	61.32

Transistor Rise Time for CMOS Compound Gate

Input B: Output Rise Time Data t_r (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	63.83	63.26	62.74	62.4	60.6

Transistor Rise Time for CMOS Compound Gate

Input C: Output Rise Time Data t_r (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	64.64	64.15	63.75	63.58	61.91

Transistor Fall Time for CMOS Compound Gate

Input A: Output Fall Time Data t_f (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	57.08	58.36	57.88	57.53	57.83

Transistor Fall Time for CMOS Compound Gate

Input B: Output Fall Time Data t_f (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	55.09	56.32	55.81	55.25	55.29

Transistor Fall Time for CMOS Compound Gate

Input C: Output Fall Time Data t_f (ps)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	54.99	56.22	55.74	55.16	55.21

Propagation Delays (All screenshots are in Appendix A for the following Toggle A/B/C)

Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for CMOS Compound Gate

Data Worst Case High to Low Propagation Delay tp_{hl} (ps) (Toggle A)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	16.1357	17.8592	19.3115	22.5744	27.9575

Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for CMOS Compound Gate

Data Worst Case Low to High Propagation Delay tp_{lh} (ps) (Toggle A)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	18.5385	20.00098	21.3708	23.9702	28.8464

Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for CMOS Compound Gate

Data Worst Case High to Low Propagation Delay tp_{hl} (ps) (Toggle B)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	18.1912	19.7946	21.4903	24.4195	29.7625

Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for CMOS Compound Gate

Data Worst Case Low to High Propagation Delay tp_{lh} (ps) (Toggle B)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	22.674	23.9907	25.2506	27.5994	31.9826

Propagation Delays

Data Worst Case Low to High Propagation Delay tp_{lh} (ns) for CMOS Compound Gate

Data Worst Case High to Low Propagation Delay tp_{hl} (ps) (Toggle C)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	17.7636	19.1837	20.5897	23.2505	28.1625

Data Worst Case High to Low Propagation Delay tp_{hl} (ns) for CMOS Compound Gate

Data Worst Case Low to High Propagation Delay tp_{lh} (ps) (Toggle C)					
Input rise/fall time (ps)	Output Load (FOx)				
	0	1	2	4	8
50	25.8141	26.9835	27.9622	30.3912	34.4937

Table 7: CMOS Compound Gate width variation table

CMOS Compound Gate width variation table					
DUT		Rise/Fall and Delay Time (n)s			
W_p(nm)	W_n(nm)	T_r	T_f	T_{plh}	T_{phl}
315	225	17.68	24.85	34.813	8.6423
270	180	17.52	26.06	18.33	34.7
360	270	17.85	23.93	10.395	31.722

225	135	17.9	29.58	11.82	37.951

We chose Wp = 315nm and Wn = 225nm because it is within our specifications with faster times and smaller footprint compared to other footprints that are also within specification.

Wp = 360nm and Wn = 270nm is faster but it is also much larger. We would need to weigh the need for a faster Tp low to high or faster Tp high to low or size, and whichever of these characteristics is most important could change our selection. We made our decision in the context of needing the smallest size with the fastest Tp high to low time.

Conclusion

9) What is the role and responsibility of each member of your team? Who did what part of the lab? Please list the individual contribution to the lab.

Cody Reid
Worked on the Inverter and assisted with CMOS circuit debugging

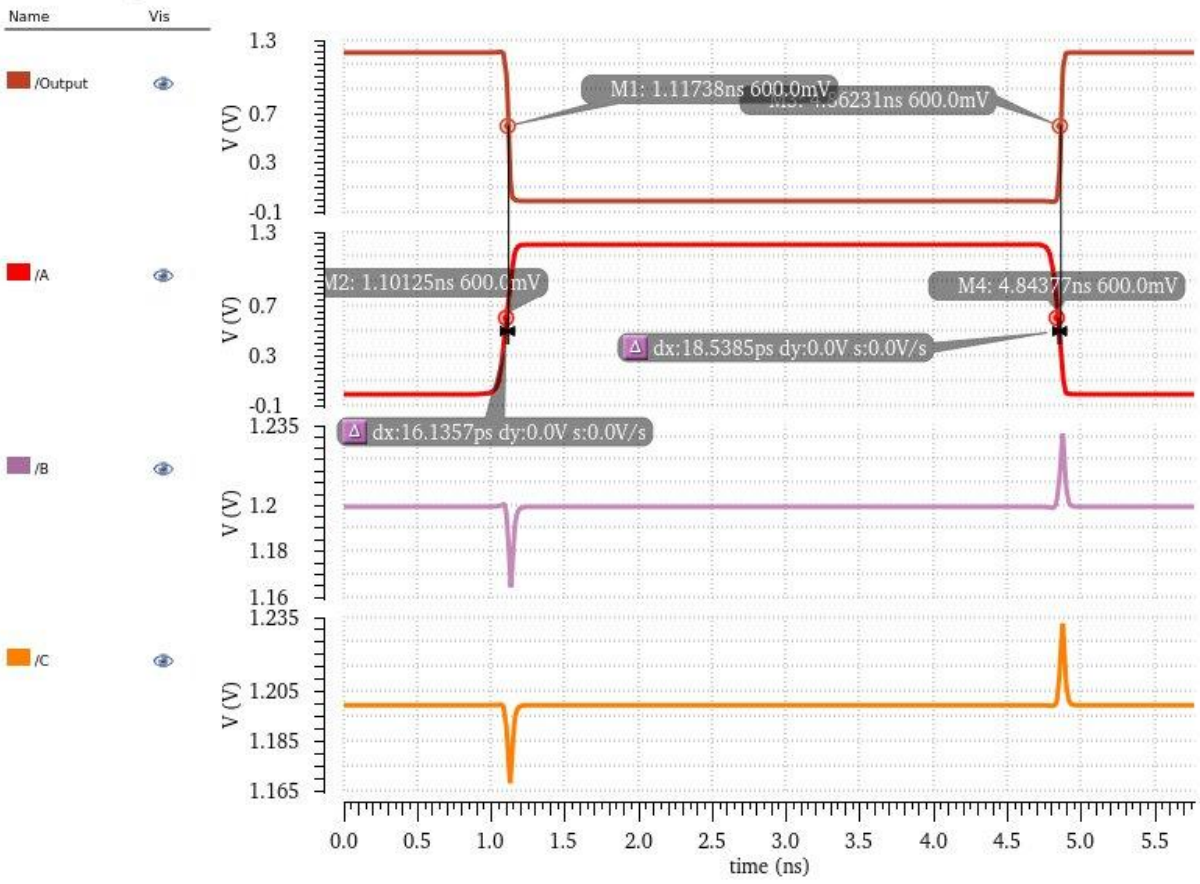
Ken Sutter
Wrote the report and assisted in both circuits

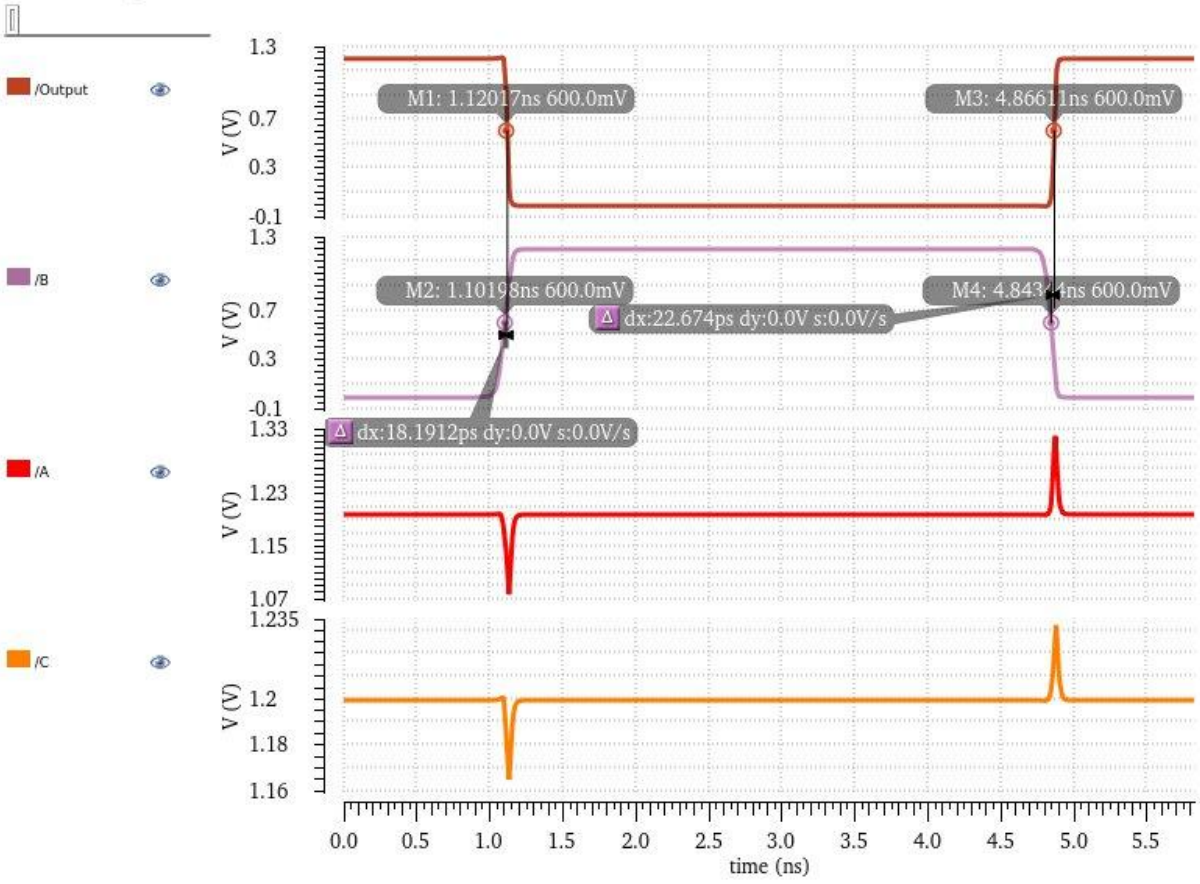
Phil Nevins
Worked on the CMOS circuit

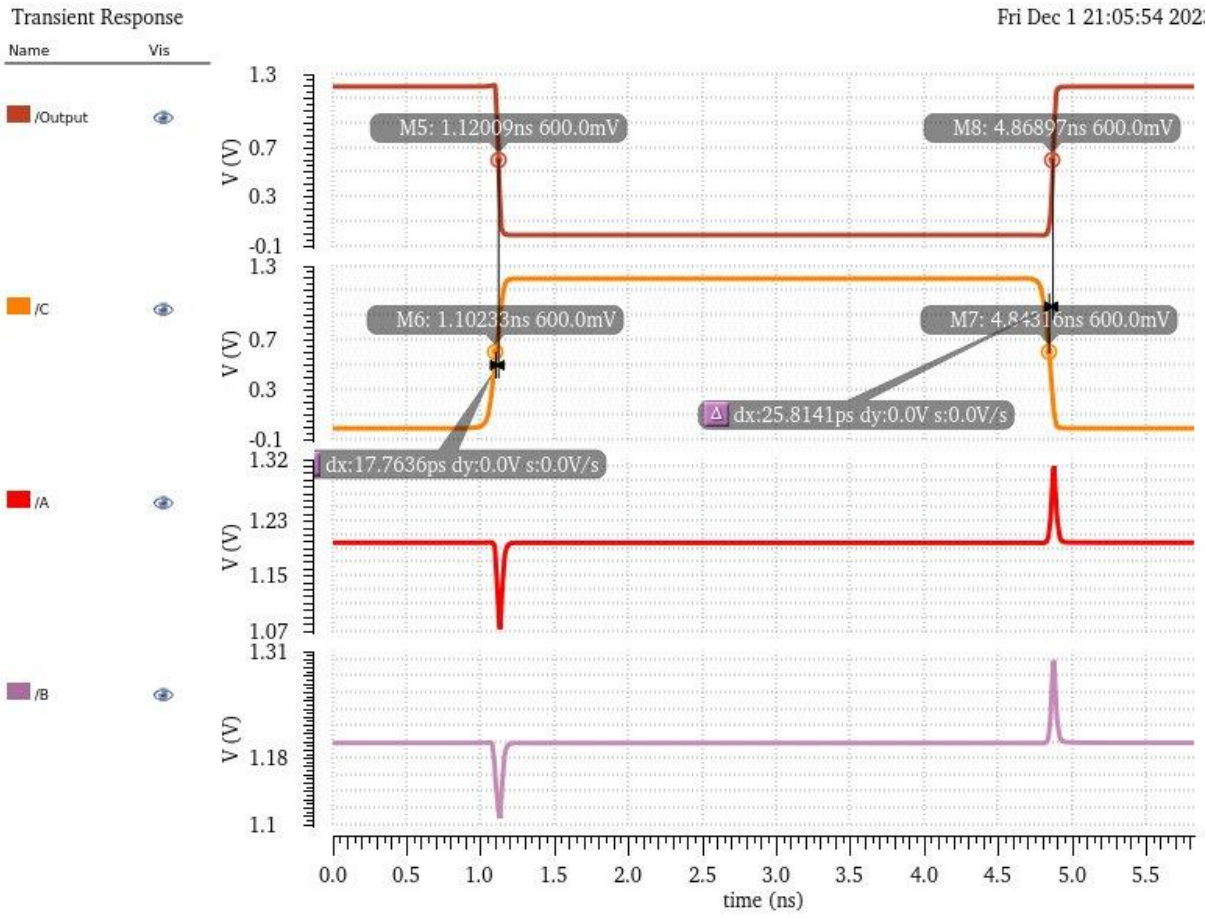
Daniel Anishchenko
Worked on boolean calculations and on the Compound Logic FET circuit

Appendix A

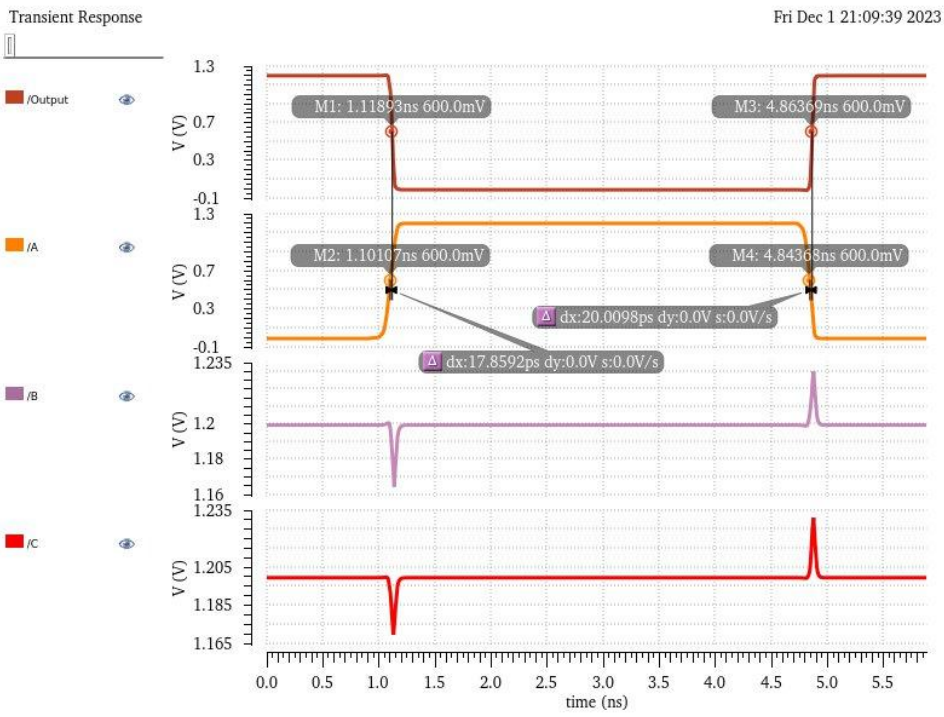
FO0

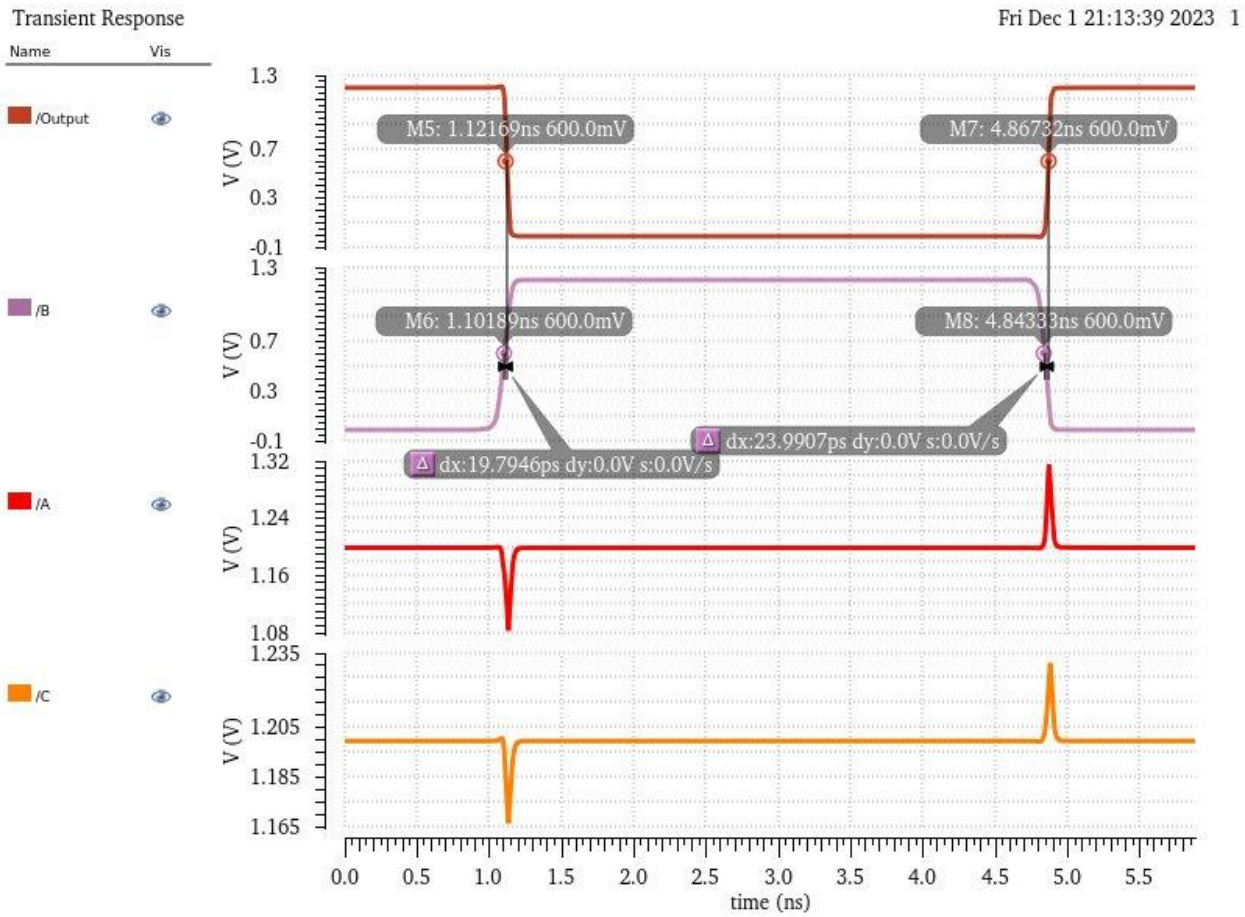

Name
Vis
/Output
/A
/B
/C
M1: 1.11738ns 600.0mV
M2: 1.10125ns 600.0mV
M4: 4.84377ns 600.0mV
dx:18.5385ps dy:0.0V s:0.0V/s
dx:16.1357ps dy:0.0V s:0.0V/s
V (V)
time (ns)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5

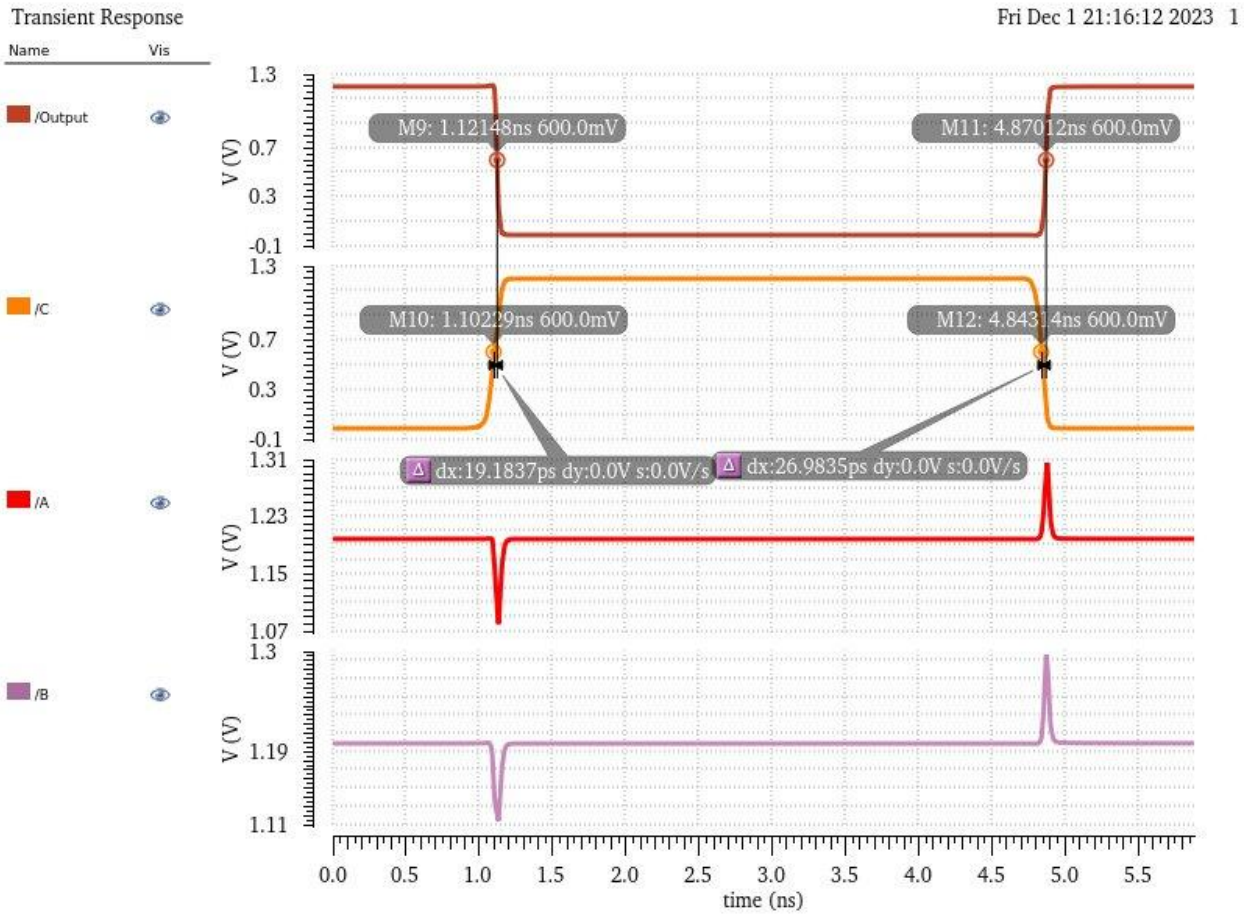

/Output
/B
/A
/C
V (V)
1.3
0.7
0.3
-0.1
M1: 1.12017ns 600.0mV
M3: 4.86611ns 600.0mV
M2: 1.10198ns 600.0mV
M4: 4.84344ns 600.0mV
dx:22.674ps dy:0.0V s:0.0V/s
dx:18.1912ps dy:0.0V s:0.0V/s
1.33
1.23
1.15
1.07
1.235
1.2
1.18
1.16
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)


Transient Response
Fri Dec 1 21:05:54 2023 1
Name
Vis
/Output
/C
/A
/B
M5: 1.12009ns 600.0mV
M8: 4.86897ns 600.0mV
M6: 1.10233ns 600.0mV
M7: 4.84316ns 600.0mV
dx:25.8141ps dy:0.0V s:0.0V/s
dx:17.7636ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.32
1.23
1.15
1.07
1.31
1.18
1.1
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)

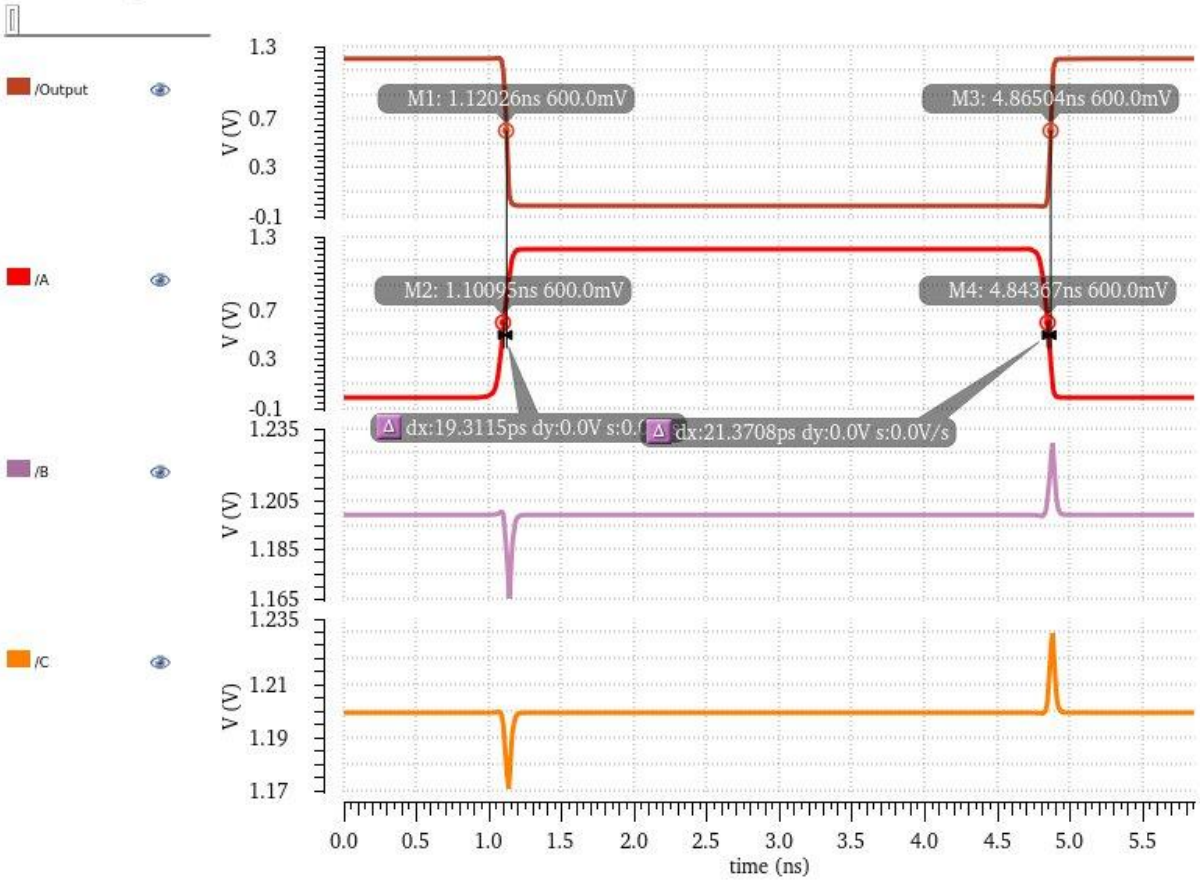
F01

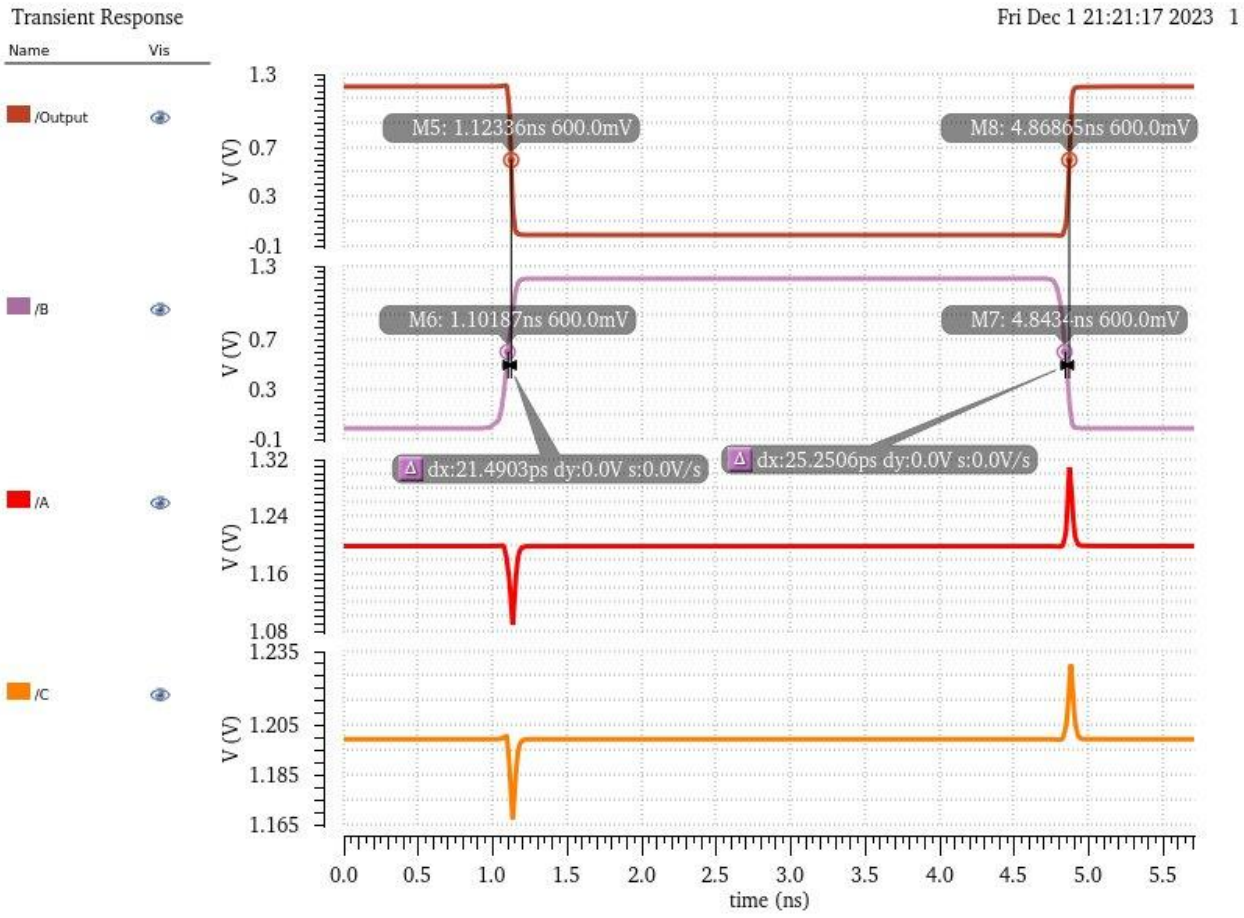

Transient Response
Fri Dec 1 21:09:39 2023 1
/Output
/A
/B
/C
M1: 1.11893ns 600.0mV
M3: 4.86369ns 600.0mV
M2: 1.10107ns 600.0mV
M4: 4.84368ns 600.0mV
dx:20.0098ps dy:0.0V s:0.0V/s
dx:17.8592ps dy:0.0V s:0.0V/s
V (V)
time (ns)

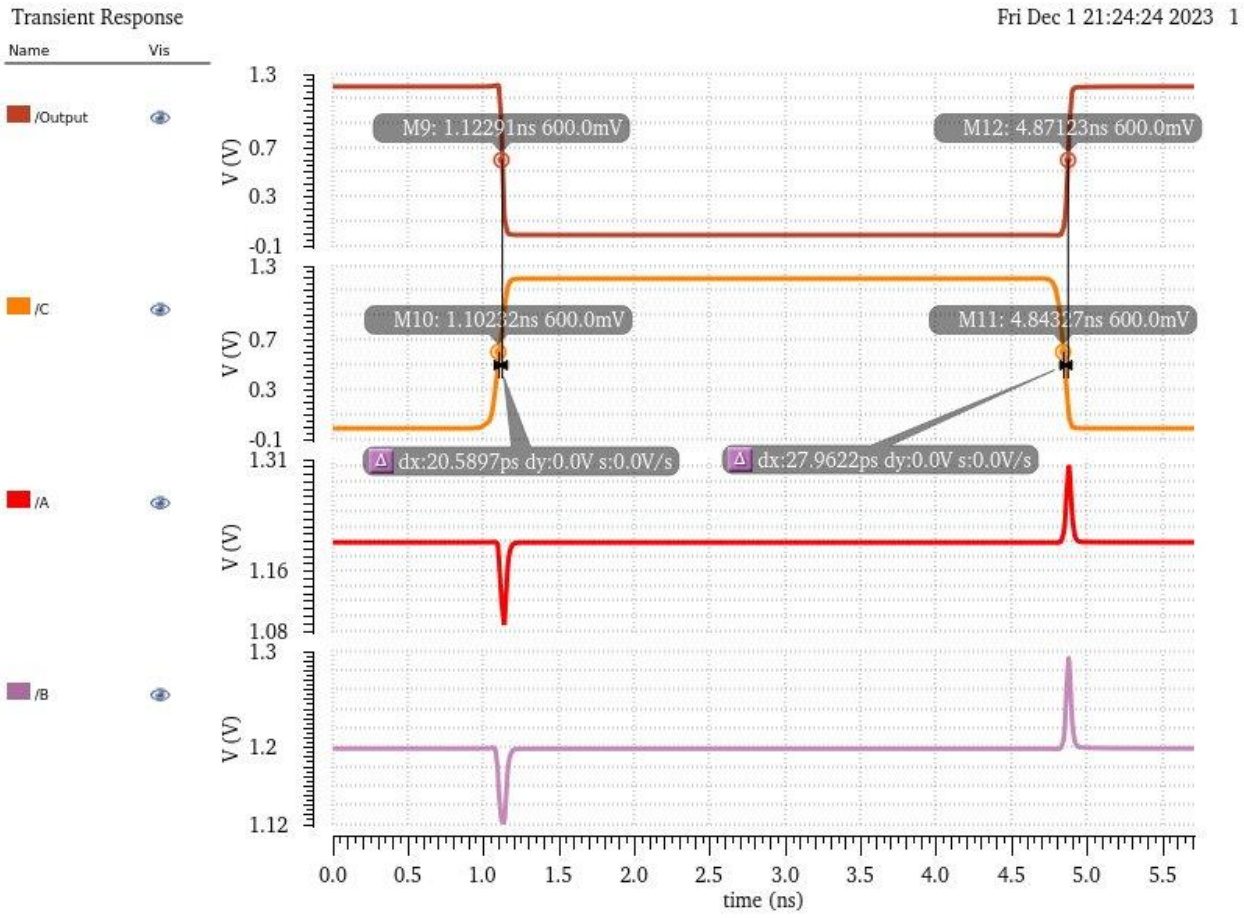

Transient Response
Fri Dec 1 21:13:39 2023 1
Name
Vis
/Output
/B
/A
/C
M5: 1.12169ns 600.0mV
M7: 4.86732ns 600.0mV
M6: 1.10189ns 600.0mV
M8: 4.84333ns 600.0mV
dx:23.9907ps dy:0.0V s:0.0V/s
dx:19.7946ps dy:0.0V s:0.0V/s
V (V)
time (ns)


Transient Response
Fri Dec 1 21:16:12 2023 1
Name
Vis
/Output
/C
/A
/B
M9: 1.12148ns 600.0mV
M11: 4.87012ns 600.0mV
M10: 1.10229ns 600.0mV
M12: 4.84314ns 600.0mV
dx:19.1837ps dy:0.0V s:0.0V/s
dx:26.9835ps dy:0.0V s:0.0V/s
V (V)
time (ns)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5

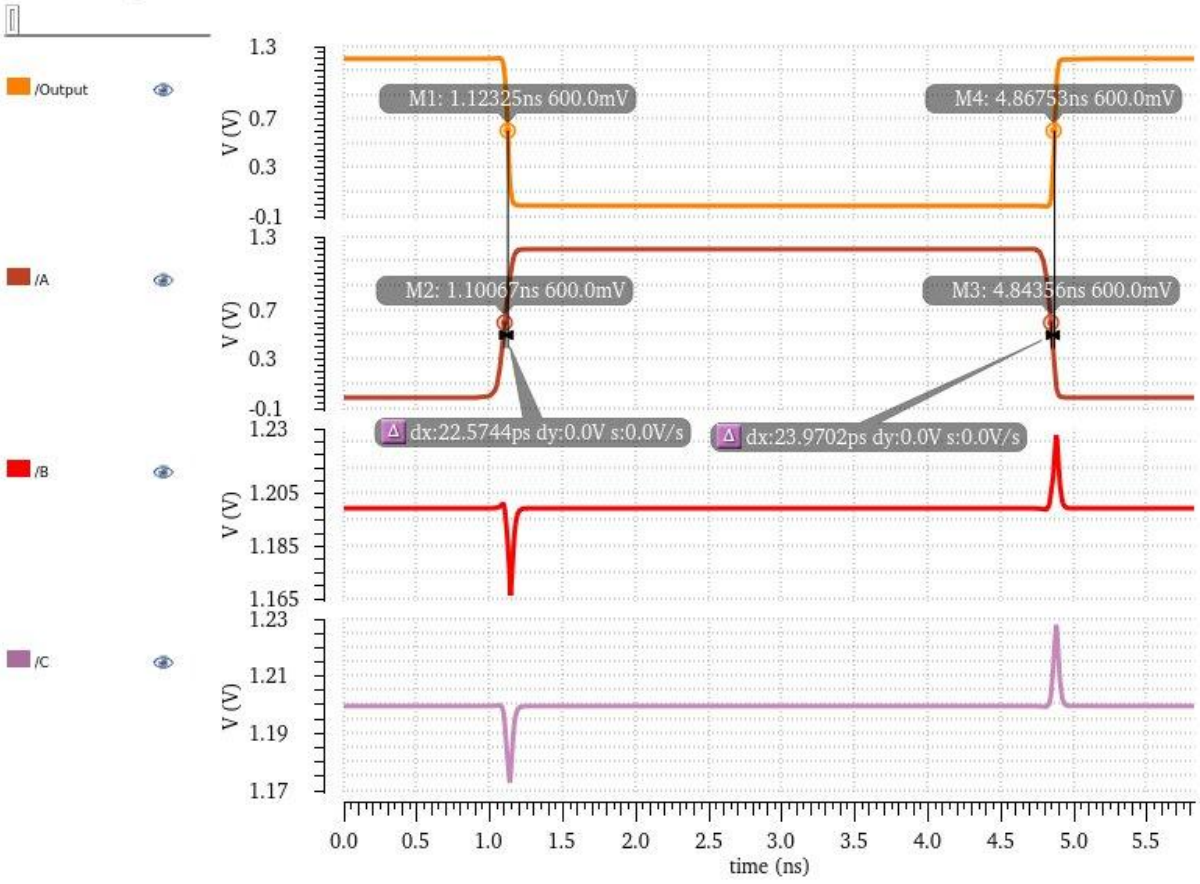
FO2

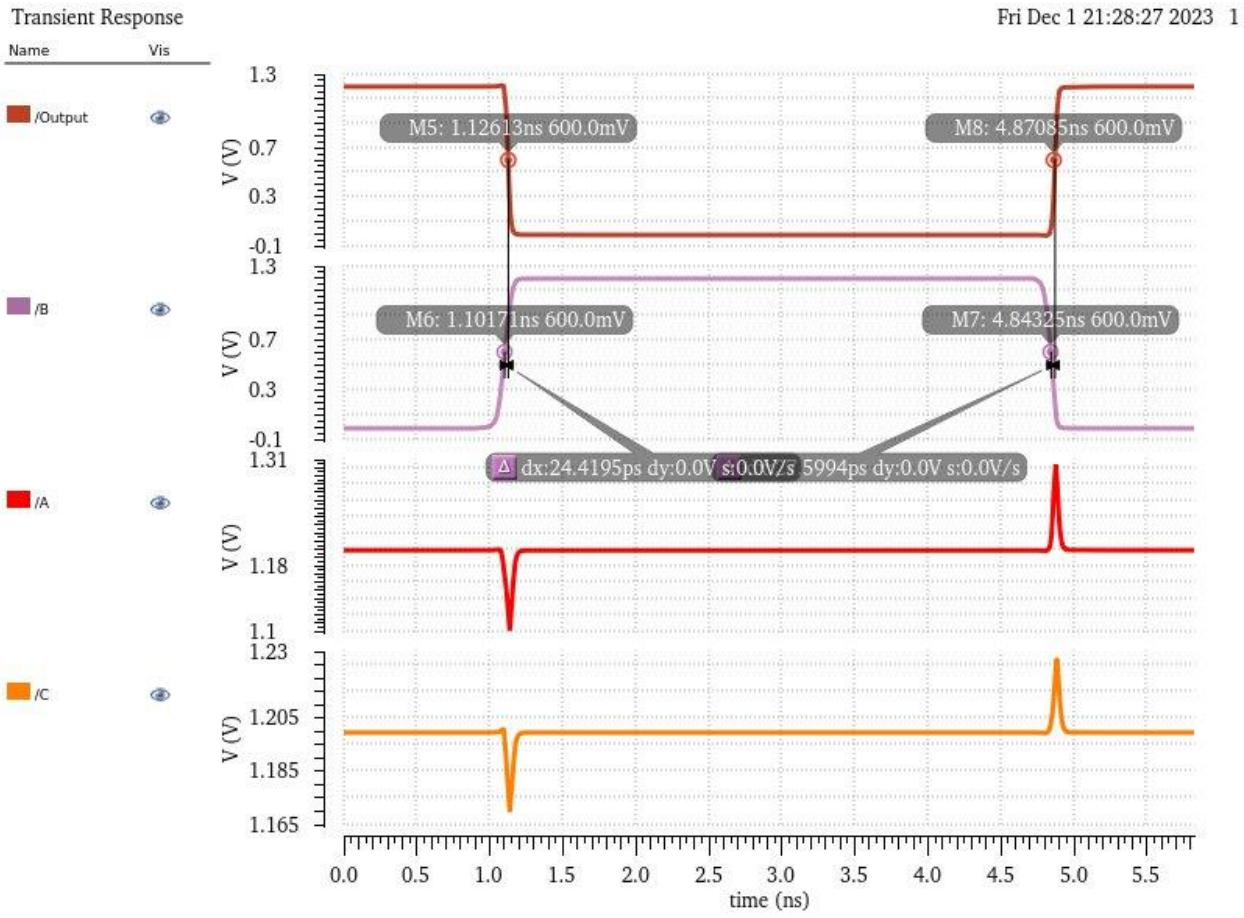

/Output
/A
/B
/C
V (V)
1.3
0.7
0.3
-0.1
M1: 1.12026ns 600.0mV
M3: 4.86504ns 600.0mV
M2: 1.10095ns 600.0mV
M4: 4.84367ns 600.0mV
dx:19.3115ps dy:0.0V s:0.0
dx:21.3708ps dy:0.0V s:0.0V/s
1.235
1.205
1.185
1.165
1.21
1.19
1.17
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)

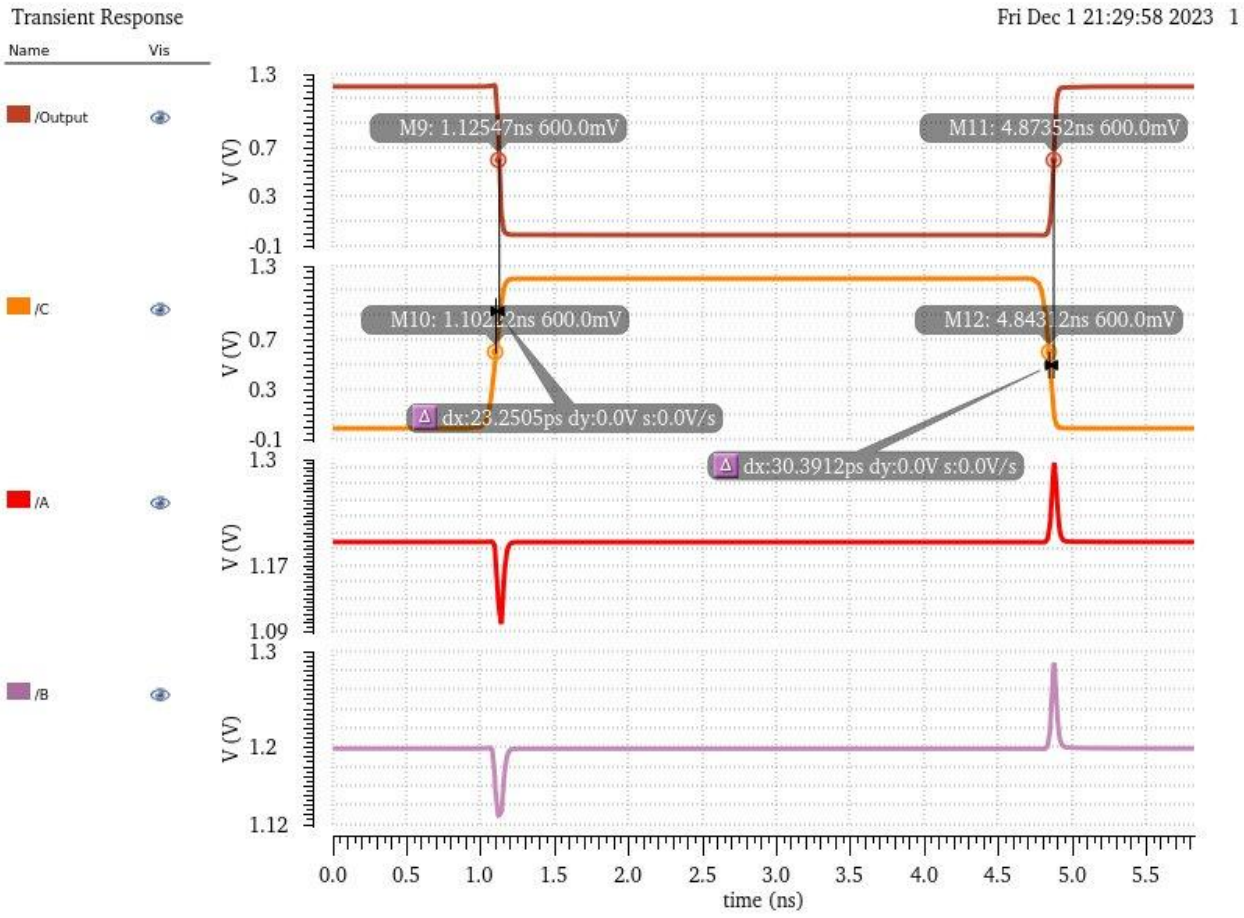

Transient Response
Fri Dec 1 21:21:17 2023 1
Name
Vis
/Output
/B
/A
/C
M5: 1.12336ns 600.0mV
M8: 4.86865ns 600.0mV
M6: 1.10187ns 600.0mV
M7: 4.8434ns 600.0mV
dx:21.4903ps dy:0.0V s:0.0V/s
dx:25.2506ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.32
1.24
1.16
1.08
1.235
1.205
1.185
1.165
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)


Transient Response
Fri Dec 1 21:24:24 2023 1
Name
Vis
/Output
/C
/A
/B
M9: 1.12291ns 600.0mV
M12: 4.87123ns 600.0mV
M10: 1.10232ns 600.0mV
M11: 4.84327ns 600.0mV
dx:20.5897ps dy:0.0V s:0.0V/s
dx:27.9622ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.31
1.16
1.08
1.2
1.12
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)

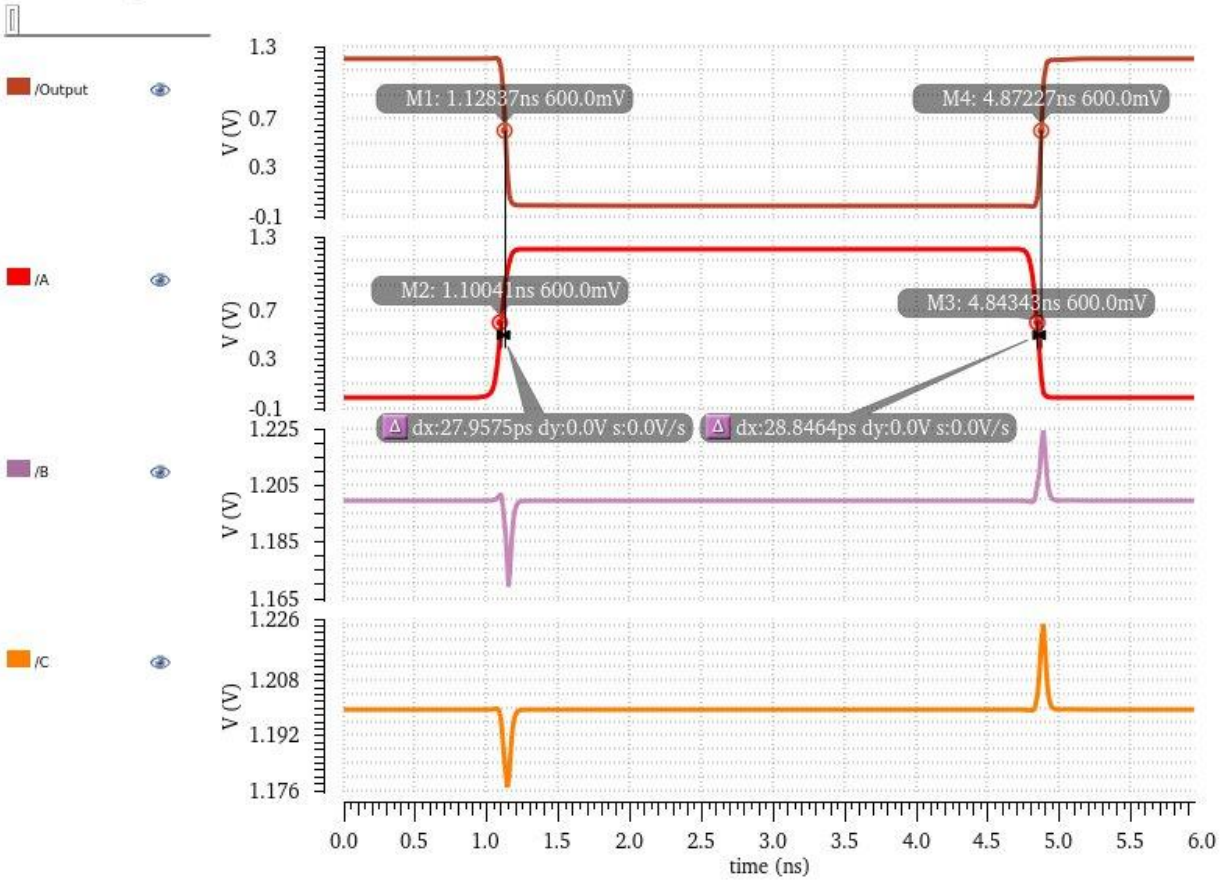
FO4

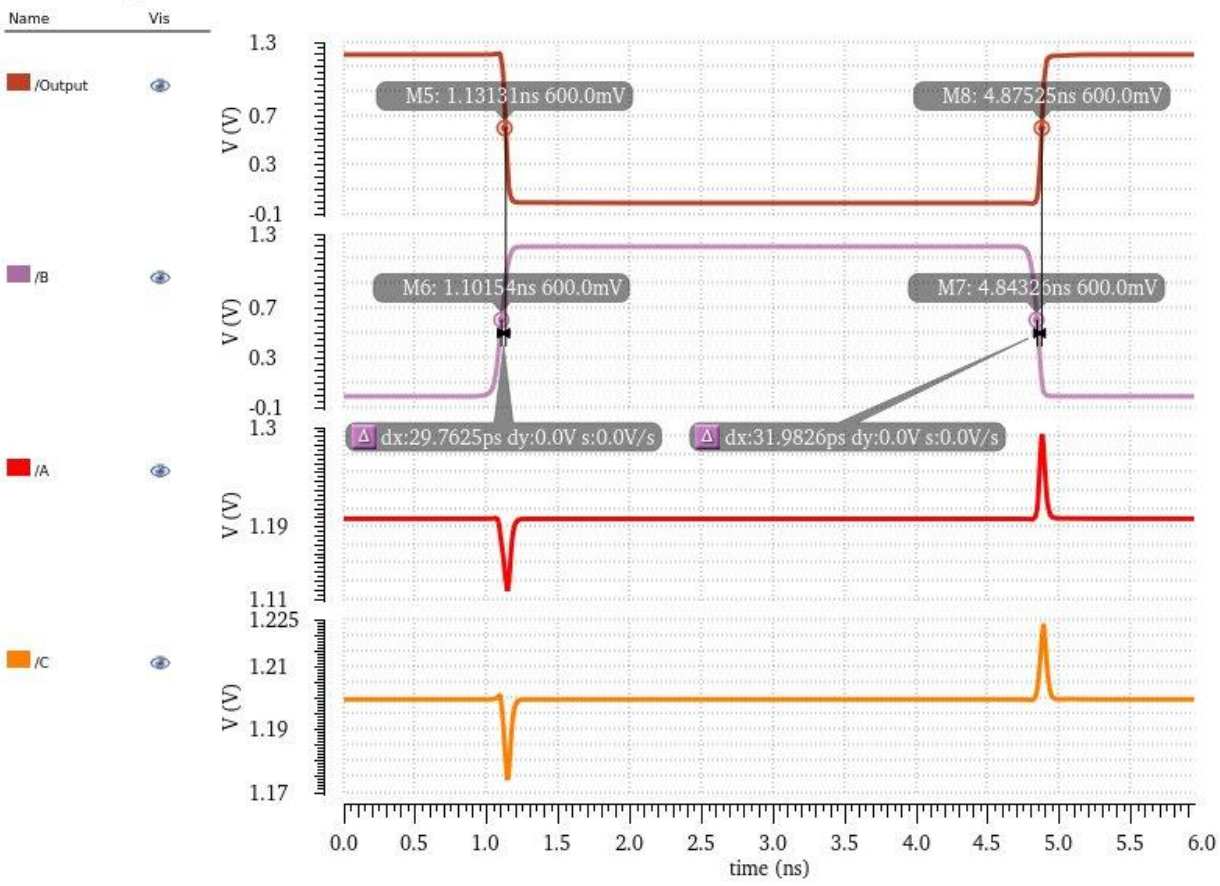

/Output
/A
/B
/C
V (V)
1.3
0.7
0.3
-0.1
M1: 1.12325ns 600.0mV
M4: 4.86753ns 600.0mV
M2: 1.10067ns 600.0mV
M3: 4.84356ns 600.0mV
dx:22.5744ps dy:0.0V s:0.0V/s
dx:23.9702ps dy:0.0V s:0.0V/s
1.23
1.205
1.185
1.165
1.21
1.19
1.17
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)

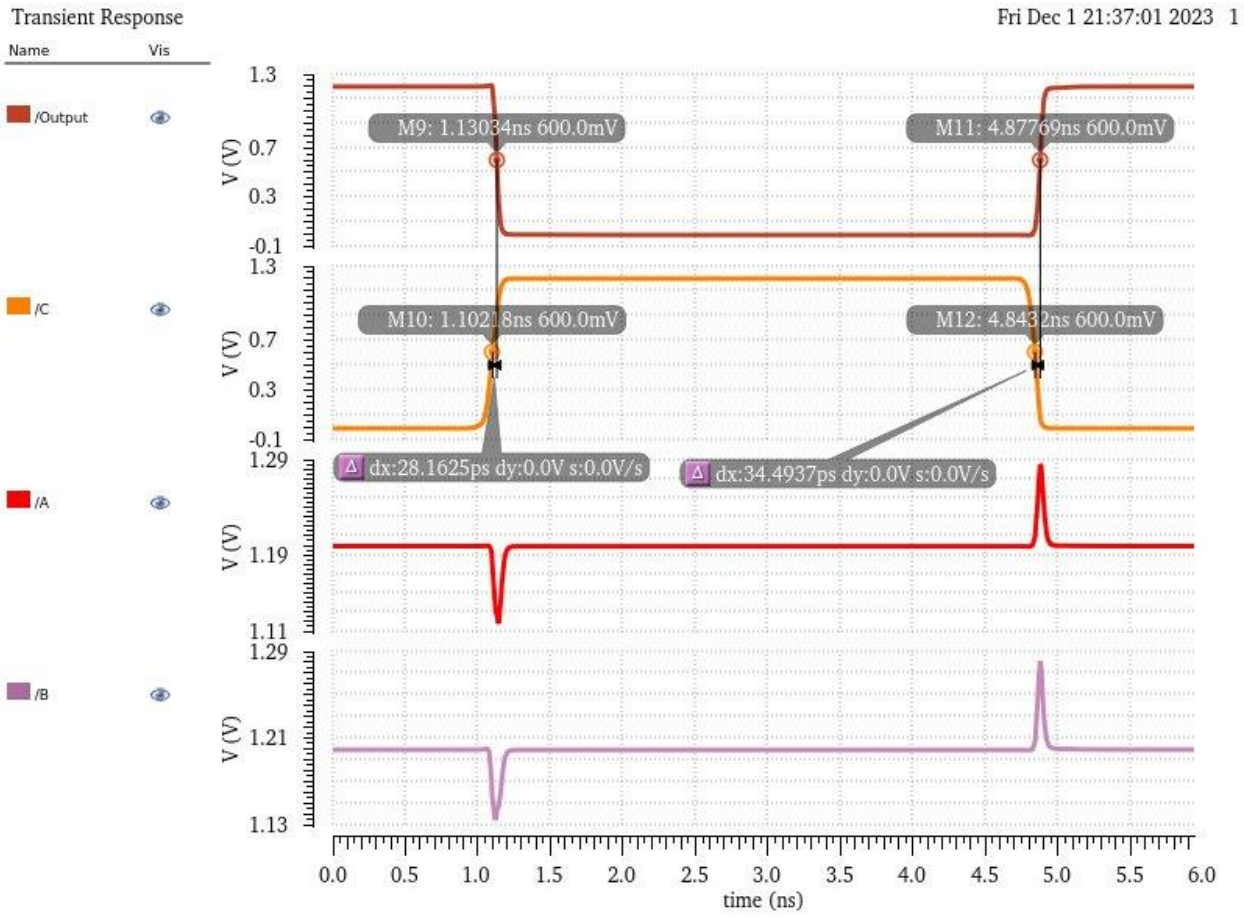

Transient Response
Fri Dec 1 21:28:27 2023 1
Name
Vis
/Output
/B
/A
/C
M5: 1.12613ns 600.0mV
M8: 4.87085ns 600.0mV
M6: 1.10171ns 600.0mV
M7: 4.84325ns 600.0mV
Δ dx:24.4195ps dy:0.0V s:0.0V/s
5994ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.31
1.18
1.1
1.23
1.205
1.185
1.165
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)


Transient Response
Fri Dec 1 21:29:58 2023 1
Name
Vis
/Output
/C
/A
/B
M9: 1.12547ns 600.0mV
M11: 4.87352ns 600.0mV
M10: 1.102
2ns 600.0mV
M12: 4.843
2ns 600.0mV
dx:23.2505ps dy:0.0V s:0.0V/s
dx:30.3912ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.17
1.09
1.2
1.12
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
time (ns)

FO8


/Output
/A
/B
/C
M1: 1.12837ns 600.0mV
M4: 4.87227ns 600.0mV
M2: 1.10041ns 600.0mV
M3: 4.84343ns 600.0mV
dx:27.9575ps dy:0.0V s:0.0V/s
dx:28.8464ps dy:0.0V s:0.0V/s
V (V)
time (ns)
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0


Transient Response
Name
Vis
/Output
/B
/A
/C
M5: 1.13131ns 600.0mV
M8: 4.87525ns 600.0mV
M6: 1.10154ns 600.0mV
M7: 4.84325ns 600.0mV
dx:29.7625ps dy:0.0V s:0.0V/s
dx:31.9826ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.19
1.11
1.225
1.21
1.17
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
time (ns)


Transient Response
Fri Dec 1 21:37:01 2023 1
Name
Vis
/Output
/C
/A
/B
M9: 1.13034ns 600.0mV
M11: 4.87769ns 600.0mV
M10: 1.10218ns 600.0mV
M12: 4.84332ns 600.0mV
dx:28.1625ps dy:0.0V s:0.0V/s
dx:34.4937ps dy:0.0V s:0.0V/s
V (V)
1.3
0.7
0.3
-0.1
1.29
1.19
1.11
1.21
1.13
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
time (ns)