[This file was provided by Wim Osterholt (2:512/56 or wim@djo.wtm.tudelft.nl).]
Last Change: 11/6/94

XT, AT and PS/2 I/O port addresses

Do NOT consider this information as complete and accurate.
If you want to do harware programming check ALWAYS the
appropriate data sheets. Be aware that erroneously programming
can put your hardware or your data at risk.

There is a memory mapped address in use for I/O functions of which I
think it should be mentioned here. See at the end of this list.

0000-001F ---- DMA 1   (first Direct Memory Access controller 8237)

0000 r/w DMA channel 0 address byte 0, then byte 1.
0001 r/w DMA channel 0 word count byte 0, then byte 1.
0002 r/w DMA channel 1 address byte 0, then byte 1.
0003 r/w DMA channel 1 word count byte 0, then byte 1.
0004 r/w DMA channel 2 address byte 0, then byte 1.
0005 r/w DMA channel 2 word count byte 0, then byte 1.
0006 r/w DMA channel 3 address byte 0, then byte 1.
0007 r/w DMA channel 3 word count byte 0, then byte 1.

0008 r DMA channel 0-3 status register
 bit 7 = 1 channel 3 request
 bit 6 = 1 channel 2 request
 bit 5 = 1 channel 1 request
 bit 4 = 1 channel 0 request
 bit 3 = 1 channel terminal count on channel 3
 bit 2 = 1 channel terminal count on channel 2
 bit 1 = 1 channel terminal count on channel 1
 bit 0 = 1 channel terminal count on channel 0

0008 w DMA channel 0-3 command register
 bit 7 = 1 DACK sense active high
       = 0 DACK sense active low
 bit 6 = 1 DREQ sense active high
       = 0 DREQ sense active low
 bit 5 = 1 extended write selection
       = 0 late write selection
 bit 4 = 1 rotating priority
       = 0 fixed priority
 bit 3 = 1 compressed timing
       = 0 normal timing
 bit 2 = 1 enable controller
       = 0 enable memory-to-memory

0009 w DMA write request register

000A r/w DMA channel 0-3 mask register
 bit 7-3 = 0   reserved
 bit 2   = 0   clear mask bit
         = 1   set mask bit
 bit 1-0 = 00 channel 0 select
         = 01 channel 1 select
         = 10 channel 2 select
         = 11 channel 3 select

000B w DMA channel 0-3 mode register
 bit 7-6 = 00 demand mode
         = 01 single mode
         = 10 block mode
         = 11 cascade mode
 bit 5   = 0   address increment select
         = 1   address decrement select
 bit 3-2 = 00 verify operation
         = 01 write to memory

```
                        = 10  read from memory
                        = 11  reserved
                 bit 1-0 = 00  channel 0 select
                        = 01  channel 1 select
                        = 10  channel 2 select
                        = 11  channel 3 select

000C    w       DMA clear byte pointer flip-flop
000D    r       DMA read temporary register
000D    w       DMA master clear
000E    w       DMA clear mask register
000F    w       DMA write mask register

--------------------------------------------------------------------------------
0010-001F ----  DMA controller (8237) on PS/2 model 60 & 80

--------------------------------------------------------------------------------
0018    w       PS/2 extended function register

--------------------------------------------------------------------------------
001A            PS/2 extended function execute

--------------------------------------------------------------------------------
0020-003F ----  PIC 1   (Programmable Interrupt Controller 8259)

0020    w       PIC initialization command word ICW1
                 bit 7-5 = 0  only used in 80/85 mode
                 bit 4   = 1  ICW1 is being issued
                 bit 3   = 0  edge triggered mode
                        = 1  level triggered mode
                 bit 2   = 0  successive interrupt vectors use 8 bytes
                        = 1  successive interrupt vectors use 4 bytes
                 bit 1   = 0  cascade mode
                        = 1  single mode, no ICW3 needed
                 bit 0   = 0  no ICW4 needed
                        = 1  ICW4 needed

0021    w       PIC  ICW2,ICW3,ICW4 after ICW1 to 0020
                ICW2:
                 bit 7-3 = address lines A0-A3 of base vector address for PIC
                 bit 2-0 = reserved
                ICW3:
                 bit 7-0 = 0  slave controller not attached to corresponding
                              interrupt pin
                        = 1  slave controller attached to corresponding
                              interrupt pin
                ICW4:
                 bit 7-5 = 0  reserved
                 bit 4   = 0  no special fully-nested mode
                        = 1  special fully-nested mode
                 bit 3-2 = 0x nonbuffered mode
                        = 10 buffered mode/slave
                        = 11 buffered mode/master
                 bit 1   = 0  normal EOI
                        = 1  Auto EOI
                 bit 0   = 0  8085 mode
                        = 1  8086/8088 mode

0021    r/w     PIC master interrupt mask register
                OCW1:
                 bit 7 = 0  enable parallel printer interrupt
                 bit 6 = 0  enable diskette interrupt
                 bit 5 = 0  enable fixed disk interrupt
                 bit 4 = 0  enable serial port 1 interrupt
                 bit 3 = 0  enable serial port 2 interrupt
                 bit 2 = 0  enable video interrupt
                 bit 1 = 0  enable keyboard, mouse, RTC interrupt
                 bit 0 = 0  enable timer interrupt

0020    r       PIC  interrupt request/in-service registers by OCW3
                request register:
```

```
                bit 7-0 = 0  no active request for the corresponding int. line
                        = 1  active request for corresponding interrupt line
               in-service register:
                bit 7-0 = 0  corresponding line not currently being serviced
                        = 1  corresponding int. line currently being serviced

0020    w       OCW2:
                bit 7-5 = 000  rotate in auto EOI mode (clear)
                        = 001  nonspecific EOI
                        = 010  no operation
                        = 011  specific EOI
                        = 100  rotate in auto EOI mode (set)
                        = 101  rotate on nonspecific EOI command
                        = 110  set priority command
                        = 111  rotate on specific EOI command
                bit 4   = 0    reserved
                bit 3   = 0    reserved
                bit 2-0        interrupt request to which the command applies

0020    w       PIC OCW3
                bit 7   = 0   reserved
                bit 6-5 = 0x  no operation
                        = 10  reset special mask
                        = 11  set special mask
                bit 4   = 0   reserved
                bit 3   = 1   reserved
                bit 2   = 0   no poll command
                        = 1   poll command
                bit 1-0 = 0x  no operation
                        = 10  read int.request register on next read at 0020
                        = 11  read int.in-service register on next read 0020

--------------------------------------------------------------------------------
0022-002B ----  Intel 82355, part of chipset for 386sx
                initialisation in POST will disable these addresses,
                only a hard reset will enable them again.

0022    r/w     82335 MCR memory configuration register
0024            82335 RC1 roll compare register
0026            82335 RC2 roll compare register
0028            82335 CC0 compare register
002A            82335 CC1 compare register

                  values for CC0 and CC1:
                  00F9,0000  enable range compare CC0 0-512K  CC1 disable
                  00F1,0000  enable range compare CC0 0-1024K CC1 disable
                  00F1,10F9  enable range compare CC0 0-1M    CC1 1M-1M5
                  00E1,0000  enable range compare CC0 0-2M    CC1 disable
                  00E1,0000  enable range compare CC0 0-2M    CC1 disable
                  00C1,0000  enable range compare CC0 0-4M    CC1 disable
                  00C1,40E1  enable range compare CC0 0-4M    CC1 4M-6M
                  0081,0000  enable range compare CC0 0-8M    CC1 disable

--------------------------------------------------------------------------------
0022-0023 ----  Chip Set Data

0022    w       index for accesses to data port
0023    r/w     chip set data

--------------------------------------------------------------------------------
0022-0023 ----  Cyrix Cx486SLC/DLC processor Cache Configuration Registers

0022    w       index for accesses to next port
                C0h CR0
                C1h CR1
                C4h non-cacheable region 1, start address bits 31-24
                C5h non-cacheable region 1, start address bits 23-16
                C6h non-cacheable region 1, start addr 15-12, size (low nibble)
                C7h non-cacheable region 2, start address bits 31-24
                C8h non-cacheable region 2, start address bits 23-16
                C9h non-cacheable region 2, start addr 15-12, size (low nibble)
```

```
                CAh non-cacheable region 3, start address bits 31-24
                CBh non-cacheable region 3, start address bits 23-16
                CCh non-cacheable region 3, start addr 15-12, size (low nibble)
                CDh non-cacheable region 4, start address bits 31-24
                CEh non-cacheable region 4, start address bits 23-16
                CFh non-cacheable region 4, start addr 15-12, size (low nibble)
0023    r/w     cache configuration register array (indexed by port 0022h)

                non-cacheable region sizes:
                 00h  disabled
                 01h  4K
                 02h  8K
                 03h  16K
                 04h  32K
                 05h  64K
                 06h  128K
                 07h  256K
                 08h  512K
                 09h  1M
                 0Ah  2M
                 0Bh  4M
                 0Ch  8M
                 0Dh  16M
                 0Eh  32M
                 0Fh  4G

                Configuration Register 0 format:
                 bit 0  "NC0" first 64K of each 1M noncacheable in real/V86
                 bit 1  "NC1" 640K-1M noncacheable
                 bit 2  "A20M" enables A20M# input pin
                 bit 3  "KEN"  enables KEN# input pin
                 bit 4  "FLUSH" enables KEN# input pin
                 bit 5  "BARB" enables internal cache flushing on bus holds
                 bit 6  "C0" cache direct-mapped instead of 2-way associative
                 bit 7  "SUSPEND" enables SUSP# input and SUSPA# output pins

                Configuration Register 1 format;
                 bit 0  "RPL" enables output pins RPLSET and RPLVAL#

--------------------------------------------------------------------------------
0026-0027 ----  Power Management

0026    w       index for data port
0027    r/w     power management data

--------------------------------------------------------------------------------
0038-003F ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

--------------------------------------------------------------------------------
0040-005F ----  PIT  (Programmable Interrupt Timer  8253, 8254)
                 XT & AT uses 40-43    PS/2 uses 40, 42,43,44, 47

0040    r/w     PIT  counter 0, counter divisor       (XT, AT, PS/2)
0041    r/w     PIT  counter 1, RAM refresh counter   (XT, AT)
0042    r/w     PIT  counter 2, cassette & speaker    (XT, AT, PS/2)

0043    r/w     PIT  mode port, control word register for counters 0-2
                 bit 7-6 = 00  counter 0 select
                         = 01  counter 1 select   (not PS/2)
```

```
                        = 10  counter 2 select
                 bit 5-4 = 00  counter latch command
                        = 01  read/write counter bits 0-7 only
                        = 10  read/write counter bits 8-15 only
                        = 11  read/write counter bits 0-7 first, then 8-15
                 bit 3-1 = 000 mode 0 select
                        = 001 mode 1 select - programmable one shot
                        = x10 mode 2 select - rate generator
                        = x11 mode 3 select - square wave generator
                        = 100 mode 4 select - software triggered strobe
                        = 101 mode 5 select - hardware triggered strobe
                 bit 0   = 0   binary counter 16 bits
                        = 1   BCD counter

0044    r/w     PIT  counter 3 (PS/2, EISA)
                used as fail-safe timer. generates an NMI on time out.
                for user generated NMI see at 0462.

0047    w       PIT  control word register counter 3 (PS/2, EISA)
                 bit 7-6 = 00  counter 3 select
                        = 01  reserved
                        = 10  reserved
                        = 11  reserved
                 bit 5-4 = 00  counter latch command counter 3
                        = 01  read/write counter bits 0-7 only
                        = 1x  reserved
                 bit 3-0 = 00

0048            EISA
0049            8254 timer 2, not used (counter 1)
004A            EISA programmable interval timer 2
004B            EISA programmable interval timer 2

--------------------------------------------------------------------------------
0060-006F ----  Keyboard controller 804x (8041, 8042)  (or PPI (8255) on PC,XT)
                 XT uses 60-63,  AT uses 60-64

                 AT keyboard controller input port bit definitions
                  bit 7   = 0  keyboard inhibited
                  bit 6   = 0  CGA, else MDA
                  bit 5   = 0  manufacturing jumper installed
                  bit 4   = 0  system RAM 512K, else 640K
                  bit 3-0      reserved

                 AT keyboard controller input port bit definitions by Compaq
                  bit 7   = 0  security lock is locked
                  bit 6   = 0  Compaq dual-scan display, 1=non-Compaq display
                  bit 5   = 0  system board dip switch 5 is ON
                  bit 4   = 0  auto speed selected, 1=high speed selected
                  bit 3   = 0  slow (4MHz), 1 = fast (8MHz)
                  bit 2   = 0  80287 installed, 1= no NDP installed
                  bit 1-0      reserved

                 AT keyboard controller output port bit definitions
                  bit 7 =    keyboard data output
                  bit 6 =    keyboard clock output
                  bit 5 = 0  input buffer full
                  bit 4 = 0  output buffer empty
                  bit 3 =    reserved (see note)
                  bit 2 =    reserved (see note)
                  bit 1 =    gate A20
                  bit 0 =    system reset
                Note:   bits 2 and 3 are the turbo speed switch or password
                          lock on Award/AMI/Phoenix BIOSes.  These bits make
                          use of nonstandard keyboard controller BIOS
                          functionality to manipulate
                            pin 23 (8041 port 22) as turbo switch for AWARD
                            pin 35 (8041 port 15) as turbo switch/pw lock for
                                Phoenix

0060    r/w     KB controller data port or keyboard input buffer (ISA, EISA)
```

```
                should only be read from after status port bit0 = 1
                should only be written to if status port bit1 = 0
                keyboard commands (data also goes to port 0060):
                 E6     sngl  set mouse scaling to 1:1
                 E7     sngl  set mouse scaling to 2:1
                 E8     dbl   set mouse resolution
                                (00h = 1/mm,01h = 2/mm,02h = 4/mm,03h = 8/mm)
                 E9     sngl  get mouse information
                                read two status bytes:
                                  byte 0
                                        bit 7 unused
                                        bit 6 remote rather than stream mode
                                        bit 5 mouse enabled
                                        bit 4 scaling set to 2:1
                                        bit 3 unused
                                        bit 2 left button pressed
                                        bit 1 unused
                                        bit 0 right button pressed
                                  byte 1: resolution
                 ED     dbl   set/reset mode indicators Caps Num Scrl
                                bit 2 = CapsLk, bit 1 = NumLk, bit 0 = ScrlLk
                 EE     sngl  diagnostic echo. returns EE.
                 EF     sngl  NOP (No OPeration). reserved for future use
                 F0     dbl   get/set scan code set
                                00h get current set
                                01h scancode set 1 (except Type 2 ctrlr)
                                02h scancode set 2 (default)
                                03h scancode set 3
                 F2     sngl  read keyboard ID (read two ID bytes)
                 F2     sngl  read mouse ID (read two ID bytes)
                 F3     dbl   set typematic rate/delay
                 F3     dbl   set mouse sample rate in reports per second
                 F4     sngl  enable keyboard
                 F4     sngl  enable mouse
                 F5     sngl  disable keyboard. set default parameters
                 F5     sngl  disable mouse, set default parameters
                 F6     sngl  set default parameters
                 F7     sngl  [MCA] set all keys to typematic (scancode set 3)
                 F8     sngl  [MCA] set all keys to make/release
                 F9     sngl  [MCA] set all keys to make only
                 FA     sngl  [MCA] set all keys to typematic/make/release
                 FB     sngl  [MCA] set al keys to typematic
                 FC     dbl   [MCA] set specific key to make/release
                 FD     dbl   [MCA] set specific key to make only
                 FE     sngl  resend last scancode
                 FF     sngl  perform internal power-on reset function
                 FF     sngl  reset mouse
                Note:   must issue command D4h to port 64h first to access
                          mouse functions


0060    r       KeyBoard or KB controller data output buffer (via PPI on XT)

0061    w       KB controller port B (ISA, EISA)   (PS/2 port A is at 0092)
                system control port for compatibility with 8255
                 bit 7  (1= IRQ 0 reset )
                 bit 6-4    reserved
                 bit 3 = 1  channel check enable
                 bit 2 = 1  parity check enable
                 bit 1 = 1  speaker data enable
                 bit 0 = 1  timer 2 gate to speaker enable

0061    r       KB controller port B control register (ISA, EISA)
                system control port for compatibility with 8255
                 bit 7   parity check occurred
                 bit 6   channel check occurred
                 bit 5   mirrors timer 2 output condition
                 bit 4   toggles with each refresh request
                 bit 3   channel check status
                 bit 2   parity check status
                 bit 1   speaker data status
```

```
                bit 0   timer 2 gate to speaker status

0061    w       PPI  Programmable Peripheral Interface 8255 (XT only)
                system control port
                 bit 7 = 1  clear keyboard
                 bit 6 = 0  hold keyboard clock low
                 bit 5 = 0  I/O check enable
                 bit 4 = 0  RAM parity check enable
                 bit 3 = 0  read low switches
                 bit 2      reserved, often used as turbo switch
                 bit 1 = 1  speaker data enable
                 bit 0 = 1  timer 2 gate to speaker enable

0062    r/w     PPI (XT only)
                 bit 7 = 1  RAM parity check
                 bit 6 = 1  I/O channel check
                 bit 5 = 1  timer 2 channel out
                 bit 4      reserved
                 bit 3 = 1  system board RAM size type 1
                 bit 2 = 1  system board RAM size type 2
                 bit 1 = 1  coprocessor installed
                 bit 0 = 1  loop in POST

0063    r/w     PPI (XT only) command mode register  (read dipswitches)
                 bit 7-6 = 00  1 diskette drive
                         = 01  2 diskette drives
                         = 10  3 diskette drives
                         = 11  4 diskette drives
                 bit 5-4 = 00  reserved
                         = 01  40*25 color (mono mode)
                         = 10  80*25 color (mono mode)
                         = 11  MDA 80*25
                 bit 3-2 = 00  256K (using 256K chips)
                         = 01  512K (using 256K chips)
                         = 10  576K (using 256K chips)
                         = 11  640K (using 256K chips)
                 bit 3-2 = 00  64K  (using 64K chips)
                         = 01  128K (using 64K chips)
                         = 10  192K (using 64K chips)
                         = 11  256K (using 64K chips)
                 bit 1-0       reserved

0064    r       KB controller read status (ISA, EISA)
                 bit 7 = 1 parity error on transmission from keyboard
                 bit 6 = 1 receive timeout
                 bit 5 = 1 transmit timeout
                 bit 4 = 0 keyboard inhibit
                 bit 3 = 1 data in input register is command
                         0 data in input register is data
                 bit 2   system flag status: 0=power up or reset  1=selftest OK
                 bit 1 = 1 input buffer full (input 60/64 has data for 8042)
                 bit 0 = 1 output buffer full (output 60 has data for system)

0064    r       KB controller read status (MCA)
                 bit 7 = 1 parity error on transmission from keyboard
                 bit 6 = 1 general timeout
                 bit 5 = 1 mouse output buffer full
                 bit 4 = 0 keyboard inhibit
                 bit 3 = 1 data in input register is command
                         0 data in input register is data
                 bit 2   system flag status: 0=power up or reset  1=selftest OK
                 bit 1 = 1 input buffer full (input 60/64 has data for 804x)
                 bit 0 = 1 output buffer full (output 60 has data for system)

0064    r       KB controller read status by Compaq
                 bit 7 = 1 parity error detected (11-bit format only). If an
                           error is detected, a Resend command is sent to the
                           keyboard once only, as an attempt to recover.
                 bit 6 = 1 receive timeout. transmission didn't finish in 2mS.
                 bit 5 = 1 transmission timeout error
                            bit 5,6,7  cause
```

```
                    1 0 0  No clock
                    1 1 0  Clock OK, no response
                    1 0 1  Clock OK, parity error
               bit 4 = 0 security lock engaged
               bit 3 = 1 data in OUTPUT register is command
                       0 data in OUTPUT register is data
               bit 2   system flag status: 0=power up or reset  1=soft reset
               bit 1 = 1 input buffer full (output 60/64 has data)
               bit 0 = 0 no new data in buffer (input 60 has data)

0064    w      KB controller input buffer (ISA, EISA)
               KB controller commands (data goes to port 0060):
                20     read  read byte zero of internal RAM, this is the
                             last KB command send to 804x
                     Compaq  Put current command byte on port 0060
                               command structure:
                               bit 7   reserved
                               bit 6 = 1 convert KB codes to 8086 scan codes
                               bit 5 = 0 use 11-bit codes, 1=use 8086 codes
                               bit 4 = 0 enable keyboard, 1=disable keyboard
                               bit 3 = 1 ignore security lock state
                               bit 2     this bit goes into bit2 status reg.
                               bit 1 = 0 reserved
                               bit 0 = 1 generate int. when output buffer full
                21-3F  read  reads the byte specified in the lower 5 bits of
                             the command in the 804x's internal RAM
                60-7F  dbl   writes the data byte to the address specified in
                             the 5 lower bits of the command.

                             Alternate description KB IO command 60 summary:
                              bit7 = 0 reserved
                              bit6 =   IBM PC compatibility mode
                              bit5 =   IBM PC mode
                              bit4 =   disable kb
                              bit3 =   inhibit override
                              bit2 =   system flag
                              bit1 = 0 reserved
                              bit0 =   enableoutput buffer full interrupt

                60   Compaq  Load new command (60 to [64], command to [60])
                A1   Compaq  unknown speedfunction ??
                A2   Compaq  unknown speedfunction ??
                A3   Compaq  Enable system speed control
                A4     MCA   check if password installed
                A4   Compaq  Toggle speed
                A5     MCA   load password
                A5   Compaq  Special reed. the 8042 places the real values
                             of port 2 except for bits 4 and 5 wich are given
                             a new definition in the output buffer. No output
                             buffer full is generated.
                               if bit 5 = 0, a 9-bit keyboard is in use
                               if bit 5 = 1, an 11-bit keyboard is in use
                               if bit 4 = 0, outp-buff-full interrupt disabled
                               if bit 4 = 1, output-buffer-full int. enabled
                A6     MCA   check password
                A6   Compaq  unknown speedfunction ??
                A7     MCA   disable mouse port
                A8     MCA   enable mouse port
                A9     MCA   test mouse port
                AA     sngl  initiate self-test. will return 55 to data port
                     Compaq  Initializes ports 1 and 2, disables the keyboard
                             and clears the buffer pointers. It then places
                             55 in the output buffer.
                AB     sngl  initiate interface test. result values:
                              0 = no error
                              1 = keyboard clock line stuck low
                              2 = keyboard clock line stuck high
                              3 = keyboard data line is stuck low
                              4 = keyboard data line stuck high
                     Compaq   5 = Compaq diagnostic feature
                AC     read  diagnostic dump. the contents of the 804x RAM,
```

```
                    output port, input port, status word are send.
                AD     sngl  disable keyboard (sets bit 4 of commmand byte)
                AE     sngl  enable keyboard  (resets bit 4 of commmand byte)
                AF     AWARD Enhanced Command: read keyboard version
                C0     read  read input port
                     Compaq  Places status of input port in output buffer. use
                             this command only when the output buffer is empty
                C1     MCA   Enhanced Command: poll input port Low nibble
                C2     MCA   Enhanced Command: poll input port High nibble
                D0     read  read output port
                     Compaq  Places byte in output port in output buffer. use
                             this command only when the output buffer is empty
                D1     dbl   write output port. next byte written  to 0060
                             will be written to the 804x output port; the
                             original IBM AT and many compatibles use bit 1 of
                             the output port to control the A20 gate.
                     Compaq  The system speed bits are not set by this command
                             use commands A1-A6 (!) for speed functions.
                D2     MCA   Enhanced Command: write keyboard output buffer
                D3     MCA   Enhanced Command: write pointing device out.buf.
                D4     MCA   write to mouse
                D4     AWARD Enhanced Command: write to auxiliary device
                DD     sngl  disable address line A20 (HP Vectra only???)
                             default in Real Mode
                DF     sngl  enable address line A20 (HP Vectra only???)
                E0     read  read test inputs.
                               bit0 = kbd clock, bit1 = kbd data
                Exxx   AWARD Enhanced Command: active output port
                ED   Compaq  This is a two part command to control the state
                             of the NumLock CpasLock and ScrollLock LEDs
                             The second byte contains the state to set LEDs.
                               bit 7-3    reserved. should be set to 0.
                               bit 2 = 0  Caps Lock LED off
                               bit 1 = 0  Num Lock LED off
                               bit 0 = 0  Scroll Lock LED off
                F0-FF  sngl  pulse output port low for 6 microseconds.
                             bits 0-3 contain the mask for the bits to be
                             pulsed. a bit is pulsed if its mask bit is zero.
                             bit0=system reset. Don't set to zero. Pulse only!

general note:    Keyboard controllers are widely different from each other.
                 You cannot generally exchange them between different machines.
note on Award:   Derived from Award's Enhanced KB controller advertising sheet.
note on Compaq:  Derived from the Compaq Deskpro 386 Tech. Ref. Guide.

0065    r       communications port (Olivetti M24)

0068    w       HP-Vectra  control buffer (HP commands)
0069    r       HP-Vectra  SVC (keyboard request SerViCe port)
006A    w       HP-Vectra  clear processing, done

006C-006F       HP-HIL  (Human Interface Link = async. serial inputs 0-7)

------------------------------------------------------------------------------
0065      ----  AT&T 6300+ high/low chip select

------------------------------------------------------------------------------
0065      ----  ???

0065    r/w     ???
                bit 2: A20 gate control (set = A20 enabled, clear = disabled)

------------------------------------------------------------------------------
0066-0067 ----  AT&T 6300+ system configuration switches

------------------------------------------------------------------------------
0068      ----  C&T chipsets, turbo mode control

------------------------------------------------------------------------------
006B-006F ----  SSGA control registers
```

```
006B    ?       RAM enable/remap
006C-006F       undocumented

------------------------------------------------------------------------------
0070-007F ----  CMOS RAM/RTC (Real Time Clock  MC146818)

0070    w       CMOS RAM index register port (ISA, EISA)
                 bit 7   = 1  NMI disabled
                         = 0  NMI enabled
                 bit 6-0      CMOS RAM index (64 bytes, sometimes 128 bytes)

                any write to 0070 should be followed by an action to 0071
                or the RTC wil be left in an unknown state.

0071    r/w     CMOS RAM data port (ISA, EISA)
                RTC registers:
                00    current second in BCD
                01    alarm second   in BCD
                02    current minute in BCD
                03    alarm minute   in BCD
                04    current hour in BCD
                05    alarm hour   in BCD
                06    day of week  in BCD
                07    day of month in BCD
                08    month in BCD
                09    year  in BCD (00-99)
                0A    status register A
                       bit 7 = 1  update in progress
                       bit 6-4 divider that identifies the time-based
                                frequency
                       bit 3-0 rate selection output  frequency and int. rate
                0B    status register B
                       bit 7 = 0  run
                             = 1  halt
                       bit 6 = 1  enable periodic interrupt
                       bit 5 = 1  enable alarm interrupt
                       bit 4 = 1  enable update-ended interrupt
                       bit 3 = 1  enable square wave interrupt
                       bit 2 = 1  calendar is in binary format
                             = 0  calendar is in BCD format
                       bit 1 = 1  24-hour mode
                             = 0  12-hour mode
                       bit 0 = 1  enable daylight savings time. only in USA.
                                  useless in Europe. Some DOS versions clear
                                  this bit when you use the DAT/TIME command.
                0C    status register C
                       bit 7 =    interrupt request flag
                       bit 6 =    peridoc interrupt flag
                       bit 5 =    alarm interrupt flag
                       bit 4 =    update interrupt flag
                       bit 3-0    reserved
                0D    status register D
                       bit 7 = 1  Real-Time Clock has power
                       bit 6-0    reserved
                0E    diagnostics status byte
                       bit 7 = 0  RTC lost power
                       bit 6 = 1  CMOS RAM checksum bad
                       bit 5 = 1  invalid configuration information at POST
                       bit 4 = 1  memory size error at POST
                       bit 3 = 1  fixed disk/adapter failed initialization
                       bit 2 = 1  CMOS RAM time found invalid
                       bit 1 = 1  adapters do not match configuration (EISA)
                       bit 0 = 1  time out reading an adapter ID (EISA)
                0F    shutdown status byte
                       00 = normal execution of POST
                       01 = chip set initialization for real mode reentry
                       04 = jump to bootstrap code
                       05 = issue an EOI an JMP to Dword ptr at 40:67
                       06 = JMP to Dword ptrv at 40:67 without EOI
                       07 = return to INT15/87 (block move)
                       08 = return to POST memory test
```

```
       09 = return to INT15/87 (block move)
       0A = JMP to Dword ptr at 40:67 without EOI
       0B = return IRETS through 40:67
10    diskette drive type for A: and B:
       bit 7-4  drive type of drive 0
       bit 3-0  drive type of drive 1
                = 0000      no drive
                = 0001      360K
                = 0010      1M2
                = 0011      720K
                = 0100      1M44
                = 0101-1111 reserved
11    reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS)
       bit 7   = 1     Typematic Rate Programming
       bit 6-5 = 00    Typematic Rate Delay 250 mSec
       bit 4-0 = 00011 Typematic Rate 21.8 Chars/Sec
12    fixed disk drive type for drive 0 and drive 1
       bit 7-4  drive type of drive 0
       bit 3-0  drive type of drive 1
                if either of the nibbles equals 0F, then bytes
                19 an 1A are valid
13    reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS)
       bit 7 = 1  Mouse Support Option
       bit 6 = 1  Above 1 MB Memory Test disable
       bit 5 = 1  Memory Test Tick Sound disable
       bit 4 = 1  Memory Parity Error Check enable
       bit 3 = 1  Hit <ESC> Message Display disabled
       bit 2 = 1  Hard Disk Type 47 Data Area at address 0:300
       bit 1 = 1  Wait For <F1> If Any Error enabled
       bit 0 = 1  System Boot Up Num Lock is On
14    equipment byte
       bit 7-6   diskette drives installed
                = 00  1 drive installed
                = 01  2 drives installed
                = 10  reserved
                = 11  reserved
       bit 5-4   primary display
                = 00  adapter card with option ROM
                = 01  40*25 color
                = 10  80*25 color
                = 11  monochrome
       bit 3-2   reserved
       bit 1   = 1  coprocessor installed (non-Weitek)
       bit 0        diskette drive avaliable for boot
15    LSB of systemn base memory in Kb
16    MSB of systemn base memory in Kb
17    LSB of total extended memory in Kb
18    MSB of total extended memory in Kb
19    drive C extension byte
1A    drive D extension byte
1B-27 reserved
1B/1C word to 82335 RC1 roll compare register at [24]
        (Phoenix)
1D/1E word to 82335 RC2 roll compare register at [26]
        (Phoenix)
28    HP-Vectra checksum over 29-2D
29-2D reserved
29/2A word to Intel 82335 CC0 compare register at
        [28](Phoenix)
2B/2C word send to 82335 CC1 compare register at [2A]
        (Phoenix)
2D    AMI Extended CMOS setup (AMI Hi-Flex BIOS)
      (Phoenix BIOS checks for the values AA or CC)
       bit 7 = 1  Weitek Processor Absent
       bit 6 = 1  Floppy Drive Seek At Boot disabled
       bit 5 = 1  System Boot Up Sequence  C:, A:
       bit 4 = 1  System Boot Up Speed is high
       bit 3 = 1  Cache Memory enabled
       bit 2 = 1  Internal Cache Memory  <1>
       bit 1-0    reserved
2E    CMOS MSB checksum over 10-2D
```

```
                2F    CMOS LSB checksum over 10-2D
                30    LSB of extended memory found above 1Mb at POST
                31    MSB of extended memory found above 1Mb at POST
                32    date century in BCD
                33    information flags
                       bit4 = bit4 from CPU register CR0   (Phoenix)
                              this bit is only known as INTEL RESERVED
                34-3F reserved
                34     bit4 bit5 (Phoenix BIOS)
                3D/3E word to 82335 MCR memory config register at
                        [22](Phoenix)
                3D     bit3      base memsize 512/640  (Phoenix)
                3E     bit7 = 1  relocate enable       (Phoenix)
                       bit1 = 1  shadow video enable   (Phoenix)
                       bit0 = 1  shadow BIOS enable    (Phoenix)


                User Definable Drive Parameters are also stored in CMOS RAM:

                AMI (386sx BIOS 1989) first user definable drive (type 47)
                 1B  L cylinders
                 1C  H cylinders
                 1D  heads
                 1E  L Write Precompensation Cylinder
                 1F  H Write Precompensation Cylinder
                 20  ??
                 21  L cylinders parking zone
                 22  H cylinders parking zone
                 23  sectors

                AMI (386sx BIOS 1989) second user definable drive (type 48)
                 24  L cylinders
                 25  H cylinders
                 26  heads
                 27  L Write Precompensation Cylinder
                 28  H Write Precompensation Cylinder
                 29  ??
                 2A  L cylinders parking zone
                 2B  H cylinders parking zone
                 2C  sectors

                Phoenix (386BIOS v1.10.03 1988) 1st user definable drv (type48)
                 20  L cylinders
                 21  H cylinders
                 22  heads
                 23  L Write Precompensation Cylinder
                 24  H Write Precompensation Cylinder
                 25  L cylinders parking zone
                 26  H cylinders parking zone
                 27  sectors

                Phoenix (386BIOS v1.10.03 1988) 2nd user definable drv (type49)
                (when PS/2-style password option is not used)
                 35  L cylinders
                 36  H cylinders
                 37  heads
                 38  L Write Precompensation Cylinder
                 39  H Write Precompensation Cylinder
                 3A  L cylinders parking zone
                 3B  H cylinders parking zone
                 3C  sectors

- - - - - - - - ----------------------------------------------------------------
0073      ----  Intel Pentium motherboard ("Neptune" chipset)

0073    r/w     bit 7: ???

- - - - - - - - ----------------------------------------------------------------
0074-0076       secondary CMOS (Compaq)

0074    w       secondary CMOS RAM index (Compaq)
```

```
0076    r/w     secondary CMOS RAM (Compaq)

- - - - - - - - ------------------------------------------------------------
0078            HP-Vectra  Hard Reset: NMI enable/disable
                 bit 7 = 0  disable & clear hard reset from HP-HIL controller
                       = 1  enable hard reset from HP-HIL controller chip
                 bit 6-0    reserved

--------------------------------------------------------------------------------
0078-007F ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

--------------------------------------------------------------------------------
007C-007D ----  HP-Vectra  PIC 3   (Programmable Interrupt Controller 8259)
                cascaded to first controller.
                used for keyboard and input device interface.
007C    r/w     HP-Vectra  PIC 3  see at 0020  PIC 1
007D    r/w     HP-Vectra  PIC 3  see at 0021  PIC 1

--------------------------------------------------------------------------------
0080    w       Manufacturing Diagnostics port

--------------------------------------------------------------------------------
0080-008F ----  DMA page registers   (74612)

0080    r/w     extra page register (temporary storage)
0081    r/w     DMA channel 2 address byte 2
0082    r/w     DMA channel 3 address byte 2
0083    r/w     DMA channel 1 address byte 2
0084    r/w     extra page register
0085    r/w     extra page register
0086    r/w     extra page register
0087    r/w     DMA channel 0 address byte 2
0088    r/w     extra page register
0089    r/w     DMA channel 6 address byte 2
0089    r/w     DMA channel 7 address byte 2
0089    r/w     DMA channel 5 address byte 2
008C    r/w     extra page register
008D    r/w     extra page register
008E    r/w     extra page register
008F    r/w     DMA refresh page register

--------------------------------------------------------------------------------
0084      ----  Compaq POST Diagnostic

--------------------------------------------------------------------------------
0084      ----  EISA Synchronize Bus Cycle

--------------------------------------------------------------------------------
0090-009F ----  PS/2 POS (Programmable Option Select)

0090            Central arbitration control port
0091    r       Card selection feedback

0092    r/w     PS/2 system control port A  (port B is at 0061)
                 bit 7-6   any bit set to 1 turns activity light on
                 bit 5     reserved
                 bit 4 = 1 watchdog timout occurred
                 bit 3 = 0 RTC/CMOS security lock (on password area) unlocked
```

```
                      = 1 CMOS locked (done by POST)
                bit 2     reserved
                bit 1 = 1 indicates A20 active
                bit 0 = 0 system reset or write
                        1 pulse alternate reset pin (alternate CPU reset)

0094    w       system board enable/setup register
                bit 7 = 1  enable functions
                      = 0  setup functions
                bit 5 = 1  enables VGA
                      = 0  setup VGA

0095            reserved

0096    w       adapter enable /setup register
                bit 3 = 1  setup adapters
                      = 0  enable registers

0097            reserved

--------------------------------------------------------------------------------
00A0-00AF ----  PIC 2   (Programmable Interrupt Controller 8259)

00A0    r/w     NMI mask register (XT)

00A0    r/w     PIC 2  same as 0020 for PIC 1
00A1    r/w     PIC 2  same as 0021 for PIC 1 except for OCW1:
                bit 7 = 0  reserved
                bit 6 = 0  enable fixed disk interrupt
                bit 5 = 0  enable coprocessor exception interrupt
                bit 4 = 0  enable mouse interrupt
                bit 3 = 0  reserved
                bit 2 = 0  reserved
                bit 1 = 0  enable redirect cascade
                bit 0 = 0  enable real-time clock interrupt

--------------------------------------------------------------------------------
00B0-00BF ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

--------------------------------------------------------------------------------
00C0      ----  TI  SN746496 programmable tone/noise generator  PCjr

--------------------------------------------------------------------------------
00C0-00DF ----  DMA 2   (second Direct Memory Access controller 8237)

00C0    r/w     DMA channel 4 memory address bytes 1 and 0 (low) (ISA, EISA)
00C2    r/w     DMA channel 4 transfer count bytes 1 and 0 (low) (ISA, EISA)
00C4    r/w     DMA channel 5 memory address bytes 1 and 0 (low) (ISA, EISA)
00C6    r/w     DMA channel 5 transfer count bytes 1 and 0 (low) (ISA, EISA)
00C8    r/w     DMA channel 6 memory address bytes 1 and 0 (low) (ISA, EISA)
00CA    r/w     DMA channel 6 transfer count bytes 1 and 0 (low) (ISA, EISA)
00CC    r/w     DMA channel 7 memory address byte 0 (low), then 1 (ISA, EISA)
00CE    r/w     DMA channel 7 transfer count byte 0 (low), then 1 (ISA, EISA)

00D0    r       DMA channel 4-7 status register (ISA, EISA)
                bit 7 = 1  channel 7 request
                bit 6 = 1  channel 6 request
                bit 5 = 1  channel 5 request
                bit 4 = 1  channel 4 request
```

```
                bit 3 = 1  terminal count on channel 7
                bit 2 = 1  terminal count on channel 6
                bit 1 = 1  terminal count on channel 5
                bit 0 = 1  terminal count on channel 4

00D0    w       DMA channel 4-7 command register (ISA, EISA)
                bit 7 = 1  DACK sense active high
                      = 0  DACK sense active low
                bit 6 = 1  DREQ sense active high
                      = 0  DREQ sense active low
                bit 5 = 1  extended write selection
                      = 0  late write selection
                bit 4 = 1  rotating priority
                      = 0  fixed priority
                bit 3 = 1  compressed timing
                      = 0  normal timing
                bit 2 = 0  enable controller
                bit 1 = 1  enable memory-to-memory transfer
                bit 0      .....

00D2    w       DMA channel 4-7 write request register (ISA, EISA)

00D4    w       DMA channel 4-7 write single mask register (ISA, EISA)
                bit 7-3      reserved
                bit 2   = 0  clear mask bit
                        = 1  set mask bit
                bit 1-0 = 00 channel 4 select
                        = 01 channel 5 select
                        = 10 channel 6 select
                        = 11 channel 7 select

00D6    w       DMA channel 4-7 mode register (ISA, EISA)
                bit 7-6 = 00  demand mode
                        = 01  single mode
                        = 10  block mode
                        = 11  cascade mode
                bit 5   = 0   address increment select
                        = 1   address decrement select
                bit 4   = 0   autoinitialisation disable
                        = 1   autoinitialisation enable
                bit 3-2 = 00  verify operation
                        = 01  write to memory
                        = 10  read from memory
                        = 11  reserved
                bit 1-0 = 00  channel 4 select
                        = 01  channel 5 select
                        = 10  channel 6 select
                        = 11  channel 7 select

00D8    w       DMA channel 4-7 clear byte pointer flip-flop (ISA, EISA)
00DA    r       DMA channel 4-7 read temporary register (ISA, EISA)
00DA    w       DMA channel 4-7 master clear (ISA, EISA)
00DC    w       DMA channel 4-7 clear mask register (ISA, EISA)
00DE    w       DMA channel 4-7 write mask register (ISA, EISA)

--------------------------------------------------------------------------------
00E0-00E7 ----  Microchannel

00E0    r/w     split address register, memory encoding registers PS/2m80 only
00E1    r/w     memory register
00E3    r/w     error trace
00E4    r/w     error trace
00E5    r/w     error trace
00E7    r/w     error trace

--------------------------------------------------------------------------------
00F0-00F5 ----  PCjr Disk Controller

00F0            disk controller
00F2            disk controller control port
00F4            disk controller status register
```

```
00F5            disk controller data port

------------------------------------------------------------------------------
00F0-00FF ----  coprocessor (8087..80387)

00F0    w       math coprocessor clear busy latch
00F1    w       math coprocessor reset
00F8    r/w     opcode transfer
00FA    r/w     opcode transfer
00FC    r/w     opcode transfer

------------------------------------------------------------------------------
00F9-00FF ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

------------------------------------------------------------------------------
0100-010F ----  CompaQ Tape drive adapter. alternate address at 0300

------------------------------------------------------------------------------
0100-0107 ----  PS/2 POS (Programmable Option Select)

0100    r       POS register 0  Low adapter ID byte
0101    r       POS register 1  High adapter ID byte

0102    r/w     POS register 2  option select data byte 1
                 bit 0 is card enable (CDEN)

0103    r/w     POS register 3  option select data byte 2
0104    r/w     POS register 4  option select data byte 3
0105    r/w     POS register 5  option select data byte 4
                 bit 7  channel active (-CHCK)
                 bit 6  channel status

0106    r/w     POS register 6  Low subaddress extension
0107    r/w     POS register 7  High subaddress extension

------------------------------------------------------------------------------
0108-010F ----  8 digit LED info panel on IBM PS/2

010F    w       leftmost character on display
010E    w       second character
....    w
0108    w       eighth character

------------------------------------------------------------------------------
0130-013F ----  CompaQ SCSI adapter. alternate address at 0330

------------------------------------------------------------------------------
0130-0133 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0134, 0230, 0234, 0330 and 0334

------------------------------------------------------------------------------
0134-0137 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0230, 0234, 0330 and 0334

------------------------------------------------------------------------------
0138-013F ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
```

```
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

--------------------------------------------------------------------------------
0140-014F ----  SCSI (alternate Small Computer System Interface) adapter
                (1st at 0340-034F)

--------------------------------------------------------------------------------
0140-0157 ----  RTC (alternate Real Time Clock for XT)   (1st at 0340-0357)

--------------------------------------------------------------------------------
015F      ----  ARTEC Handyscanner A400Z.  alternate address at 35F.

--------------------------------------------------------------------------------
0170-0177 ----  HDC 2   (2nd Fixed Disk Controller)   same as 01Fx (ISA, EISA)

--------------------------------------------------------------------------------
0178-0179 ----  Power Management

0178    w       index selection for data port
0179    r/w     power management data

--------------------------------------------------------------------------------
0178-017F ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

--------------------------------------------------------------------------------
01E8-01EF ----  System Control. Laptop chipset: Headland HL21 & Acer M5105

01ED    r/w     select internal register. Data to/from 01EF
01EE    r
01EF    r/w     reg.
                5  = 1000xxxx  for low CPU clock speed (4MHz on Morse/Mitac)
                   = 0xxxxxxx  for high CPU clock speed (16MHz on Morse/Mitac)

--------------------------------------------------------------------------------
01F0-01F7 ----  HDC 1   (1st Fixed Disk Controller)   same as 017x (ISA, EISA)

01F0    r/w     data register

01F1    r       error register
                diagnostic mode errors:
                 bit 7-3        reserved
                 bit 2-1 = 001  no error detected
                         = 010  formatter device error
                         = 011  sector buffer error
                         = 100  ECC circuitry error
                         = 101  controlling microprocessor error
                 operation mode:
                  bit 7  = 1  bad block detected
                         = 0  block OK
                  bit 6  = 1  uncorrectable ECC error
                         = 0  no error
```

```
                 bit 5       reserved
                 bit 4  = 1  ID found
                        = 0  ID not found
                 bit 3       reserved
                 bit 2  = 1  command completed
                        = 0  command aborted
                 bit 1  = 1  track 000 not found
                        = 0  track 000 found
                 bit 0  = 1  DAM not found
                        = 0  DAM found (CP-3022 always 0)

01F1    w       WPC/4  (Write Precompensation Cylinder divided by 4)

01F2    r/w     sector count
01F3    r/w     sector number
01F4    r/w     cylinder low
01F5    r/w     cylinder high

01F6    r/w     drive/head
                 bit 7   = 1
                 bit 6   = 0
                 bit 5   = 1
                 bit 4   = 0  drive 0 select
                         = 1  drive 1 select
                 bit 3-0      head select bits

01F7    r       status register
                 bit 7 = 1  controller is executing a command
                 bit 6 = 1  drive is ready
                 bit 5 = 1  write fault
                 bit 4 = 1  seek complete
                 bit 3 = 1  sector buffer requires servicing
                 bit 2 = 1  disk data read successfully corrected
                 bit 1 = 1  index - set to 1 each disk revolution
                 bit 0 = 1  previous command ended in an error

01F7    w       command register
                commands:
                 98 E5   check power mode       (IDE)
                 90      execute drive diagnostics
                 50      format track
                 EC      identify drive         (IDE)
                 97 E3   idle                   (IDE)
                 95 E1   idle immediate         (IDE)
                 91      initialize drive parameters
                 1x      recalibrate
                 E4      read buffer            (IDE)
                 C8      read DMA with retry    (IDE)
                 C9      read DMA without retry (IDE)
                 C4      read multiplec         (IDE)
                 20      read sectors with retry
                 21      read sectors without retry
                 22      read long with retry
                 23      read long without retry
                 40      read verify sectors with retry
                 41      read verify sectors without retry
                 7x      seek
                 EF      set features           (IDE)
                 C6      set multiple mode      (IDE)
                 99 E6   set sleep mode         (IDE)
                 96 E2   standby                (IDE)
                 94 E0   standby immediate      (IDE)
                 E8      write buffer           (IDE)
                 CA      write DMA with retry   (IDE)
                 CB      write DMA with retry   (IDE)
                 C5      write multiple         (IDE)
                 E9      write same             (IDE)
                 30      write sectors with retry
                 31      write sectors without retry
                 32      write long with retry
                 33      write long without retry
```

```
                3C      write verify            (IDE)
                9A      vendor unique           (IDE)
                C0-C3   vendor unique           (IDE)
                8x      vendor unique           (IDE)
                F0-F4   EATA standard           (IDE)
                F5-FF   vendor unique           (IDE)

------------------------------------------------------------------------------
01F8      ----  ???

01F8    r/w     ???
                bit 0: A20 gate control (set = A20 enabled, clear = disabled)

------------------------------------------------------------------------------
01F9-01FF ----  PC radio by CoZet Info Systems
                The I/O address range is dipswitch selectable from:
                   038-03F and 0B0-0BF
                   078-07F and 0F0-0FF
                   138-13F and 1B0-1BF
                   178-17F and 1F0-1FF
                   238-23F and 2B0-2BF
                   278-27F and 2F0-2FF
                   338-33F and 3B0-3BF
                   378-37F and 3F0-3FF
                All of these addresses show a readout of FF in initial state.
                Once started, all of the addresses show  FB, whatever might
                happen.

------------------------------------------------------------------------------
0200-020F ----  Game port reserved I/O address space
0200-0207 ----  Game port, eight identical addresses on some boards

0201    r       read joystick position and status
                 bit 7  status B joystick button 2 / D paddle button
                 bit 6  status B joystick button 1 / C paddle button
                 bit 5  status A joystick button 2 / B paddle button
                 bit 4  status A joystick button 1 / A paddle button
                 bit 3  B joystick Y coordinate    / D paddle coordinate
                 bit 2  B joystick X coordinate    / C paddle coordinate
                 bit 1  A joystick Y coordinate    / B paddle coordinate
                 bit 0  A joystick X coordinate    / A paddle coordinate

        w       fire joysticks four one-shots

------------------------------------------------------------------------------
0200-02FF ----  Sunshine uPW48, programmer for EPROM version CPU's 8748/8749
                (4 bit DIP switch installable in the range 20x-2Fx)
0200-0203       adresses of the 8255 on the uPW48
0208-020B       adresses of ??? on the uPW48 (all showing zeros)


------------------------------------------------------------------------------
0210-0217 ----  Expansion unit (XT)

0210    w       latch expansion bus data
        r       verify expansion bus data
0211    w       clear wait, test latch
        r       High byte data address
0212    r       Low byte data address
0213    w       0=enable,  1=disable expansion unit
0214    w       latch data  (receiver card port)
        r       read data   (receiver card port)
0215    r       High byte of address, then Low byte   (receiver card port)

------------------------------------------------------------------------------
0220-0223 ---- Sound Blaster / Adlib port

0220    r/w     Left speaker -- Status / Address port
0221    w       Left speaker -- Data port
0222    r/w     Right speaker -- Status / Address port
                Address:
```

```
                   01 -- Enable waveform control
                   02 -- Timer #1 data
                   03 -- Timer #2 data
                   04 -- Timer control flags
                   08 -- Speech synthesis mode
                  20-35 -- Amplitude Modulation / Vibrato
                  40-55 -- Level key scaling / Total level
                  60-75 -- Attack / Decay rate
                  80-95 -- Sustain / Release rate
                  A0-B8 -- Octave / Frequency Number
                  C0-C8 -- Feedback / Algorithm
                  E0-F5 -- Waveform Selection
0223    w       Right speaker -- Data port

SeeAlso: 0388-0389

--------------------------------------------------------------------------------
0220-0227 ----  Soundblaster PRO and SSB 16 ASP

--------------------------------------------------------------------------------
0220-022F ----  Soundblaster PRO 2.0

--------------------------------------------------------------------------------
0220-022F ----  Soundblaster PRO 4.0
0220    r       left FM status port
0220    w       left FM music register address port (index)
0221    r/w     left FM music data port
0222    r       right FM status port
0222    w       right FM music register address port (index)
0223    r/w     right FM music data port
0224    w       mixer register address port (index)
0225    r/w     mixer data port
0226    w       DSP reset
0228    r       FM music status port
0228    w       FM music register address port (index)
0229    w       FM music data port
022A    r       DSP read data (voice I/O and Midi)
022C    w       DSP write data / write command
022C    r       DSP write buffer status (bit 7)
022E    r       DSP data available status (bit 7)

                The FM music is accessible on 0388/0389 for compatibility.

--------------------------------------------------------------------------------
0230-0233 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0330 and 0334

--------------------------------------------------------------------------------
0234-0237 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0330 and 0334

--------------------------------------------------------------------------------
0240-024F ----  Gravis Ultra Sound by Advanced Gravis
         The I/O address range is dipswitch selectable from:
           0200-020F and 0300-030F
           0210-021F and 0310-031F
           0220-022F and 0320-032F
           0230-023F and 0330-033F
           0240-024F and 0340-034F
           0250-025F and 0350-035F
           0260-026F and 0360-036F
           0270-027F and 0370-037F

0240    w       Mix Control register
                 bit 6     Control Register Select (see 024B)
                 bit 5     Enable MIDI Loopback
                 bit 4     Combine GF1 IRQ with MIDI IRQ
                 bit 3     Enable Latches
                 bit 2     Enable MIC IN
                 bit 1     Disable LINE OUT
                 bit 0     Disable LINE IN
```

```
0241    r       Read Data
        w       Trigger Timer
0246    r       IRQ Status Register
                 bit 7     DMA TC IRQ
                 bit 6     Volume Ramp IRQ
                 bit 5     WaveTable IRQ
                 bit 3     Timer 2 IRQ
                 bit 2     Timer 1 IRQ
                 bit 1     MIDI Receive IRQ
                 bit 0     MIDI Transmit IRQ
0248    r/w     Timer Control Reg
                 Same a ADLIB Board (look at 0200)
0249    w       Timer Data
                 bit 7     Reset Timr IRQ
                 bit 6     Mask Timer 1
                 bit 5     Mask Timer 2
                 bit 1     Timer 2 Start
                 bit 0     Timer 1 Start
024B    w       IRQ Control Register (0240 bit 6 = 1)
                 bit 6     Combine Both IRQ
                 bit 5-3   MIDI IRQ Selector
                           = 000  No IRQ
                           = 001  IRQ 2
                           = 010  IRQ 5
                           = 011  IRQ 3
                           = 100  IRQ 7
                           = 101  IRQ 11
                           = 110  IRQ 12
                           = 111  IRQ 15
                 bit 2-0   GF1 IRQ Selector
                           = 000  No IRQ
                           = 001  IRQ 2
                           = 010  IRQ 5
                           = 011  IRQ 3
                           = 100  IRQ 7
                           = 101  IRQ 11
                           = 110  IRQ 12
                           = 111  IRQ 15
                DMA Control Register (0240 bit 6 = 0)
                 bit 6     Combine Both IRQ
                 bit 5-3   DMA Select Register 2
                           = 000  No DMA
                           = 001  DMA 1
                           = 010  DMA 3
                           = 011  DMA 5
                           = 100  DMA 6
                           = 101  DMA 7
                 bit 2-0   DMA Select Register 1
                           = 000  No DMA
                           = 001  DMA 1
                           = 010  DMA 3
                           = 011  DMA 5
                           = 100  DMA 6
                           = 101  DMA 7
024F    r/w     Register Controls (rev 3.4+)

SeeAlso: 0340-034F, 0746

--------------------------------------------------------------------------------
0240-0257 ----  RTC (alternate Real Time Clock for XT)   (1st at 0340-0357)
                (used by TIMER.COM v1.2 which is the 'standard' timer program)

--------------------------------------------------------------------------------
0258-025F ----  Intel Above Board

--------------------------------------------------------------------------------
0278-027E ----  parallel printer port, same as 0378 and 03BC

0278    w       data port
0279    r/w     status port
027A    r/w     control port
```

```
------------------------------------------------------------------------------
02A0-02A7 ----  Sunshine EW-901BN, EW-904BN
                EPROM writer card (release 1986) for EPROMs up to 27512
02A0-02A3       adresses of the 8255 on the EW-90xBN


------------------------------------------------------------------------------
02A2-02A3 ----  MSM58321RS clock

------------------------------------------------------------------------------
02B0-02BF ----  Trantor SCSI adapter

------------------------------------------------------------------------------
02B0-02DF ----  alternate EGA,  primary EGA at 03C0

------------------------------------------------------------------------------
02C0-02Cx ----  AST-clock

------------------------------------------------------------------------------
02E0-02EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)
                (GAB 0 on XT)
02E1            GPIB (adapter 0)
02E2
02E3

------------------------------------------------------------------------------
02E0-02EF ----  data aquisition  (AT)

02E2            data aquisition (adapter 0)
02E3            data aquisition (adapter 0)

------------------------------------------------------------------------------
02E8      ----  S3 86C928 video controller (ELSA Winner 1000)

------------------------------------------------------------------------------
02E8-02EF ----  serial port, same as 02F8, 03E8 and 03F8

------------------------------------------------------------------------------
02E8-02EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

02E8    r       display status
02E8    w       horizontal total
02EA    w       DAC mask
02EB    w       DAC read index
02EC    w       DAC write index
02ED    w       DAC data

------------------------------------------------------------------------------
02EA      ----  S3 86C928 video controller (ELSA Winner 1000)

------------------------------------------------------------------------------
02F8-02FF ----  serial port, same as 02E8, 03E8 and 03F8

02F8    w       transmitter holding register
02F8    r       receiver buffer register
        r/w     divisor latch, low byte   when DLAB=1
02F9    r/w     divisor latch, high byte  when DLAB=1
        r/w     interrupt enable register when DLAB=0
02FA    r       interrupt identification register
02FB    r/w     line control register
02FC    r/w     modem control register
02FD    r       line status register
02FF    r/w     scratch register

------------------------------------------------------------------------------
0300      ---- Award POST Diagnostic

------------------------------------------------------------------------------
0300-0301 ---- Soundblaster 16 ASP MPU-Midi
```

```
--------------------------------------------------------------------------------
0300-0303 ----  Panasonic 52x CD-ROM SCSI Miniport
                Alternate addresses at 0320, 0340, 0360, and 0380

--------------------------------------------------------------------------------
0300-030F ----  Philips CD-ROM player CM50

--------------------------------------------------------------------------------
0300-030F ----  CompaQ Tape drive adapter. alternate address at 0100

--------------------------------------------------------------------------------
0300-031F ----  prototype cards
                Periscope hardware debugger

--------------------------------------------------------------------------------
0310-031F ----  Philips CD-ROM player CM50

--------------------------------------------------------------------------------
0320-0323 ----  XT HDC 1   (Hard Disk Controller)

0320    r/w     data register

0321    w       reset controller
        r       read controller hardware status
                 bit 7-6 = 0
                 bit 5        logical unit number
                 bit 4-2 = 0
                 bit 1   = 0  no error
                 bit 0   = 0

0322    r       read DIPswitch setting on XT controller card
        w       generate controller-select pulse
0323    w       write pattern to DMA and INT mask register

0324-0327 ----  XT HDC 2   (Hard Disk Controller)
0328-032B ----  XT HDC 3   (Hard Disk Controller)
032C-032F ----  XT HDC 4   (Hard Disk Controller)

--------------------------------------------------------------------------------
0330-0331 ----  MIDI interface

--------------------------------------------------------------------------------
0330-0333 ----  Adaptec 154xB/154xC SCSI adapter. default address.
                alternate address at 0130, 0134, 0230, 0234 and 0334

--------------------------------------------------------------------------------
0330-033F ----  CompaQ SCSI adapter. alternate address at 0130

--------------------------------------------------------------------------------
0330-033F ----  Philips CD-ROM player CM50

--------------------------------------------------------------------------------
0334-0337 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0234 and 0330

--------------------------------------------------------------------------------
0338      ----  AdLib soundblaster card

--------------------------------------------------------------------------------
0340-034F ----  Philips CD-ROM player CM50

--------------------------------------------------------------------------------
0340-034F ----  SCSI (1st Small Computer System Interface) adapter
                (alternate at 0140-014F)

--------------------------------------------------------------------------------
0340-034F ----  Gravis Ultra Sound by Advanced Gravis
         The I/O address range is dipswitch selectable from:
           0200-020F and 0300-030F
           0210-021F and 0310-031F
           0220-022F and 0320-032F
```

```
           0230-023F and 0330-033F
           0240-024F and 0340-034F
           0250-025F and 0350-035F
           0260-026F and 0360-036F
           0270-027F and 0370-037F

0340    w       MIDI Control
                 bit 7     Receive IRQ (1 = enabled)
                 bit 5-6   Xmit IRQ
                 bit 0-1   Master Reset (1 = enabled)
        r       MIDI Status
                 bit 7     Interrupt pending
                 bit 5     Overrun Error
                 bit 4     Framing Error
                 bit 1     Transmit Register Empty
                 bit 0     Receive Register Empty
0341    w       MIDI Transmit Data
        r       MIDI Receive Data
0342    r/w     GF1 Page Register / Voice Select
0343    r/w     GF1/Global Register Select

                 Global Registers, NOT voice specific:
                 41   r/w   DRAM DMA Control
                             bit 7       Invert MSB
                             bit 6       Data Size (8/16 bits)
                             bit 5       DMA Pending
                             bit 3-4     DMA Rate Divider
                             bit 2       DMA Channel Width (8/16 bits)
                             bit 1       DMA Direction (1 = read)
                             bit 0       DMA Enable
                 42   w     DMA Start Address
                             bits 15-0   DMA Address Lines 19-4
                 43   w     DRAM I/O Address LOW
                 44   w     DRAM I/O Address HIGH
                             bits 0-3    Upper 4 Address Lines
                 45   r/w   Timer Control
                             bit 3       Enable Timer 2
                             bit 2       Enable Timer 1
                 46   w     Timer 1 Count (granularity of 80 micro sec)
                 47   w     Timer 2 Count (granulatity of 320 micro sec)
                 48   w     Sampling Frequency
                             rate = 9878400 / (16 * (FREQ + 2))
                 49   r/w   Sampling Control
                             bit 7       Invert MSB
                             bit 6       DMA IRQ pending
                             bit 5       DMA IRQ enable
                             bit 2       DMA width (8/16 bits)
                             bit 1       Mode (mone/stereo)
                             bit 0       Start Sampling
                 4B   w     Joystick Trim DAC
                 4C   r/w   RESET
                             bit 2       GF1 Master IRQ Enable
                             bit 1       DAC Enable
                             bit 0       Master Reset

                 Voice specific registers:
                 00   w     Voice Control
                             bit 7       IRQ pending
                             bit 6       Direction
                             bit 5       Enable WAVE IRQ
                             bit 4       Enable bi-directional Looping
                             bit 3       Enable Looping
                             bit 2       Size data (8/16 bits)
                             bit 1       Stop Voice
                             bit 0       Voice Stopped
                 01   w     Frequency Control
                             bit 15-10   Integer Portion
                             bit 9-1     Fractional Portion
                 02   w     Start Address HIGH
                             bit 12-0    Address Lines 19-7
                 03   w     Start Address LOW
```

```
                    bit 15-9    Address Lines 6-0
                    bit 8-5     Fractional Part of Start Address
                04  w       End Address HIGH
                    bit 12-0    Address Lines 19-7
                05  w       End Address LOW
                    bit 15-9    Address Lines 6-0
                    bit 8-5     Fractional Part of End Address
                06  w       Volume Ramp Rate
                    bit 5-0     Amount added
                    bit 7-6     Rate
                07  w       Volume Ramp Start
                    bit 7-4     Exponent
                    bit 3-0     Mantissa
                08  w       Volume Ramp End
                    bit 7-4     Exponent
                    bit 3-0     Mantissa
                09  w       Current Volume
                    bit 15-12   Exponent
                    bit 11-4    Mantissa
                0A  w       Current Address HIGH
                    bit 12-0    Address Lines 19-7
                0B  w       Current Address LOW
                    bit 15-9    Address Lines 6-0
                    bit 8-0     Fractional Position
                0C  w       Pan Position
                    bit 3-0     Pan Postion
                0D  w       Volume Control
                    bit 7       IRQ Pending
                    bit 6       Direction
                    bit 5       Enable Volume Ramp IRQ
                    bit 4       Enable bi-directional Looping
                    bit 3       Enable Looping
                    bit 2       Rollover Condition
                    bit 1       Stop Ramp
                    bit 0       Ramp Stopped
                0E  w       Active Voices
                    bit 5-0     #Voices -1  (allowed 13 - 31)
                0F  w       IRQ Source Register
                    bit 7       WaveTable IRQ pending
                    bit 6       Volume Ramp IRQ pending
                    bit 4-0     Voice Number
                80  r       Voice Control (see 00)
                81  r       Frequency Control (see 01)
                82  r       Start Address HIGH (see 02)
                83  r       Start Address LOW (see 03)
                84  r       End Address HIGH (see 04)
                85  r       End Address LOW (see 05)
                86  r       Volume Ramp Rate (see 06)
                87  r       Volume Ramp Start (see 07)
                88  r       Volume Ramp End (see 08)
                89  r       Current Volume (see 09)
                8A  r       Current Address HIGH (see 0A)
                8B  r       Current Address LOW (see 0B)
                8C  r       Pan Position (see 0C)
                8D  r       Volume Control (see 0D)
                8E  r       Active Voices (see 0E)
                8F  r       IRQ Status (see 0F)

0344    r/w     GF1/Global Data Low Byte (16 bits)
0345    r/w     GF1/Global Data High Byte (8 bits)
0346    w       Mixer Data Port
0347    r/w     GF1 DRAM
                 Direct Read Write at Loction pointed with regs 43 and 44

SeeAlso: 0240-024F, 0746

--------------------------------------------------------------------------
0340-0357 ----  RTC (1st Real Time Clock for XT), (alternate at 0240-0257)
                (used by TIMER.COM v1.2 which is the 'standard' timer program)

0340    r/w     0.01 seconds  0-99
```

```
0341    r/w     0.1 seconds   0-99
0342    r/w     seconds       0-59
0343    r/w     minutes       0-59
0343    r/w     hours         0-23
0345    r/w     day of week   1-7
0346    r/w     day of month  1-31
0347    r/w     month         1-12
0348
0349    r/w     year          0-99
034A
034B
034C
034D
034E
034F
0350    r       status?
0351
0352
0353
0354    r       status?
0355
0356
0357
```

0348-0357 ---- DCA 3278

034C-034F ---- Gravis UltraMax by Advanced Gravis

The I/O address range is dipswitch selectable from:

- 0200-020F and 0300-030F
- 0210-021F and 0310-031F
- 0220-022F and 0320-032F
- 0230-023F and 0330-033F
- 0240-024F and 0340-034F
- 0250-025F and 0350-035F
- 0260-026F and 0360-036F
- 0270-027F and 0370-037F

035A-035B ---- Adaptec AH1520 jumper settings

```
035A    r       bit 7:    SCSI parity disabled
                bits 6-5: DMA channel
                        (00 = channel 0, 01 = 5, 10 = 6, 11 = 7)
                bits 4-3: IRQ number
                        (00 = IRQ9, 01 = IRQ10, 10 = IRQ11, 11 = IRQ12)
                bits 2-0: SCSI ID
035B    r       bit 7: DMA transfer mode (clear for PIO)
                bit 6: boot enabled
                bits 5-4: boot type
                        00 ???
                        01 boot from floppy
                        10 print configured options
                        11 boot from hard disk
                bit 3: enable sync negotiation
                bit 2: enable target disconnection
                bits 1-0: unused???
```

035F   ---- ARTEC Handyscanner A400Z. alternate address at 15F.

0360-036F ---- PC network (AT)
0360-0367 ---- PC network (XT only)

0360-036F ---- National Semiconductor DP8390(1)C/NS3249C network chipset

Note: cards based on this IEEE 802.3 networking chipset can use any range of 16 consecutive addresses, and provide a total of four pages of sixteen register

Page 0 r

			w	
00	Command reg.	CR	Command reg.	CR
01	current local DMA address 0	CLDA0	page start reg.	PSTART
02	current local DMA address 1	CLDA1	page stop reg.	PSTOP
03	boundary pointer	BNRY	boundary pointer	BNRY
04	transmit status reg.	TSR	Tx page start address	TPSR
05	number of collisions reg.	NCR	Tx byte count reg.0	TBCR0
06	FIFO		Tx byte count reg.1	TBCR1
07	interrupt status reg.	ISR	interrupt status reg.	ISR
08	current remote DMA address 0	CRDA0	remote start addr.reg.0	RSAR0
09	current remote DMA address 1	CRDA1	remote start addr.reg.1	RSAR1
0A	reserved		remote byte count reg.0	RBCR0
0B	reserved		remote byte count reg.1	RBCR1
0C	receive status reg.	RSR	Rx configuration reg.	RCR
0D	tally counter 0 (frame errors)	CNTR0	Tx configuration reg.	TCR
0E	tally counter 1 (CRC errors)	CNTR1	data configuration reg.	DCR
0F	tally counter 2 (missed pkt)	CNTR2	interrupt mask reg.	IMR

Page 1 r/w

00	Command	CR
01	physical address reg.0	PAR0
02	physical address reg.1	PAR1
03	physical address reg.2	PAR2
04	physical address reg.3	PAR3
05	physical address reg.4	PAR4
06	physical address reg.5	PAR5
07	current page reg.	CURR
08	multicast address reg.0	MAR0
09	multicast address reg.1	MAR1
0A	multicast address reg.2	MAR2
0B	multicast address reg.3	MAR3
0C	multicast address reg.4	MAR4
0D	multicast address reg.5	MAR5
0E	multicast address reg.6	MAR6
0F	multicast address reg.7	MAR7

Page 2 r w

diagnostics page - should never be modfied under normal operation.

00	Command	CR	Command	CR
01	page start reg.	PSTART	current local DMA addr.0	CLDA0
02	page stop reg.	BPSTOP	current local DMA addr.1	CLDA1
03	remote next packet pointer		remote next packet pointer	
04	Tx page start address	TPSR	reserved	
05	local next packet pointer		local next packet pointer	
06	address counter (upper)		address counter (upper)	
07	address counter (lower)		address counter (lower)	
08	reserved		reserved	
09	reserved		reserved	
0A	reserved		reserved	
0B	reserved		reserved	
0C	Rx configuration reg.	RCR	reserved	
0D	Tx configuration reg.	TCR	reserved	
0E	data configuration reg.	DCR	reserved	
0F	interrupt mask reg.	IMR	reserved	

Page 3 r w

Test Page - should never be modified !

00 Command CR Command CR

bit0=1 software reset command. 1=offline 0=online
bit1=0 activate NIC after reset command
bit2=1 start transmision of a packet
bit3-5 remote DMA command
 000 not allowed
 001 remote read
 010 remote write

```
                 011 send packet
                 1xx abort/complete rmote DMA
        bit 6,7 page select
                 00 register page 0
                 01 register page 1
                 10 register page 2
                 11 register page 3

--------------------------------------------------------------------------------
0370-0377 ----  FDC 2  (2nd Floppy Disk Controller)     first FDC at 03F0
                (8272, 8272A, NEC765)
                (82072, 82077AA for perpendicular recording at 2.8Mb)

0370    r       diskette Extra High Density controller board jumpers (AT)
0370    r       diskette controller status A (PS/2, PS/2 model 30)
0371    r       diskette controller status B (PS/2, PS/2 model 30)
0372    w       diskette controller DOR (Digital Output Register)
0374    r       diskette controller main status register
0374    w       diskette controller datarate select register
0375    r/w     diskette controller command/data register
0376    r/w     (2nd FIXED disk controller data register)
0377    r       diskette controller DIR (Digital Input Register)
0377    w       select register for diskette data transfer rate

--------------------------------------------------------------------------------
0378-037A ----  parallel printer port, same as 0278 and 03BC

0378    w       data port
0379    r/w     status port
037A    r/w     control port

--------------------------------------------------------------------------------
0380-038F ----  2nd Binary Synchronous Data Link Control adapter (see 03A0)

0380    r/w      on board 8255 port A, internal/external sense
0381    r/w      on board 8255 port B, external modem interface
0382    r/w      on board 8255 port C, internal control and gating
0383    r/w      on board 8255 mode register
0384    r/w      on board 8253 channel square wave generator
0385    r/w      on board 8253 channel 1 inactivity time-out
0386    r/w      on board 8253 channel 2 inactivity time-out
0387    r/w      on board 8253 mode register
0388    r/w      on board 8273 read: status  write: command
0389    r/w      on board 8273 read: response  write: parameter
038A    r/w      on board 8273 transmit interrupt status
038B    r/w      on board 8273 receiver interrupt status
038C    r/w      on board 8273 data

--------------------------------------------------------------------------------
0388-0389 ---- Sound Blaster / Adlib port

0388    r/w     Both Speakers -- Status / Address port
                Address:
                     01 -- Enable waveform control
                     02 -- Timer #1 data
                     03 -- Timer #2 data
                     04 -- Timer control flags
                     08 -- Speech synthesis mode
                   20-35 -- Amplitude Modulation / Vibrato
                   40-55 -- Level key scaling / Total level
                   60-75 -- Attack / Decay rate
                   80-95 -- Sustain / Release rate
                   A0-B8 -- Octave / Frequency Number
                   C0-C8 -- Feedback / Algorithm
                   E0-F5 -- Waveform Selection
0389    w       Data port

SeeAlso: 0220-0223

--------------------------------------------------------------------------------
0388-0389 ---- Soundblaster PRO FM-Chip
```

```
0388-038B ---- Soundblaster 16 ASP FM-Chip

------------------------------------------------------------------------------
0390-0397 ----  Sunshine EW-901B, EW-904B
                EPROM writer card for EPROMs up to 27512
0390-0393       adresses of the 8255 on the EW-90xB

------------------------------------------------------------------------------
0390-039F ----  Cluster adapter (AT)

0390-0393       (adapter 0)     (XT)

------------------------------------------------------------------------------
03A0-03AF ----  1st SDLC (Binary Synchronous Data Link Control adapter)

03A0    r/w      on board 8255 port A, internal/external sense
03A1    r/w      on board 8255 port B, external modem interface
03A2    r/w      on board 8255 port C, internal control and gating
03A3    r/w      on board 8255 mode register
03A4    r/w      on board 8253 counter 0 unused
03A5    r/w      on board 8253 channel 1 inactivity time-out
03A6    r/w      on board 8253 channel 2 inactivity time-out
03A7    r/w      on board 8253 mode register
03A8    r/w      on board 8251 data
03A9    r/w      on board 8251 command/mode/status register

------------------------------------------------------------------------------
03B0-03BF ----  MDA  (Monochrome Display Adapter based on 6845)

03B0            same as 03B4
03B1            same as 03B5
03B2            same as 03B4
03B3            same as 03B5
03B4    w       MDA CRT index register   (EGA/VGA)
                selects which register (0-11h) is to be accessed through 3B5
03B5    r/w     MDA CRT data register    (EGA/VGA)
                selected by port 3B4. registers C-F may be read
                 00  horizontal total
                 01  horizontal displayed
                 02  horizontal sync position
                 03  horizontal sync pulse width
                 04  vertical total
                 05  vertical displayed
                 06  vertical sync position
                 07  vertical sunc pulse width
                 08  interlace mode
                 09  maximum scan lines
                 0A  cursor start
                 0B  cursor end
                 0C  start address high
                 0D  start address low
                 0E  cursor location high
                 0F  cursor location low
                 10  light pen high
                 11  light pen low
03B6            same as 03B4
03B7            same as 03B5
03B8    r/w     MDA mode control register
                 bit 7 not used
                 bit 6 not used
                 bit 5 enable blink
                 bit 4 not used
                 bit 3 video enable
                 bit 2 not used
                 bit 1 not used
                 bit 0 high resolution mode

03B9            reserved for color select register on color adapter

03BA    r       CRT status register      EGA/VGA: input status 1 register
                 bit 7   (MSD says) if this bit changes within 8000h reads then
```

```
                  bit 6-4 = 000 = adapter is Hercules or compatible
                            001 = adapter is Hercules+
                            101 = adapter is Hercules InColor
                                  else: adapter is unknown
                  bit 3   black/white video
                  bit 2-1 reserved
                  bit 0   horizontal drive

03BA    w       EGA/VGA feature control register

03BB            reserved for light pen strobe reset

--------------------------------------------------------------------------------
03BC-03BF ----  parallel printer port, same as 0278 and 0378

03BC    w       data port
03BD    r/w     status port
                  bit 7 = 0  busy
                  bit 6 = 0  acknowledge
                  bit 5 = 1  out of paper
                  bit 4 = 1  printer is selected
                  bit 3 = 0  error
                  bit 2 = 0  IRQ has occurred
                  bit 1-0    reserved

03BE    r/w     control port
                  bit 7-5    reserved
                  bit 4 = 1  enable IRQ
                  bit 3 = 1  select printer
                  bit 2 = 0  initialize printer
                  bit 1 = 1  automatic line feed
                  bit 0 = 1  strobe

--------------------------------------------------------------------------------
03BF    r/w     Hercules configuration switch register
                  bit 7-2
                  bit 1 = 0  disables upper 32K of graphics mode buffer
                          1  enables upper 32K of graphics mode buffer
                  bit 0 = 0  prevents graphics mode
                          1  allows graphics mode

--------------------------------------------------------------------------------
03C0-03C7 ----  Sunshine EW-901, EW-901A, EW-904, EW-904A
                EPROM writer card for EPROMs up to 27512
03C0-03C3       adresses of the 8255 on the EW-90x

--------------------------------------------------------------------------------
03C0-03CF ----  EGA  (1st Enhanced Graphics Adapter)    alternate at 02C0

03C0    (r)/w   EGA VGA ATC index/data register
03C1    r       VGA     other attribute register
03C2    r       EGA VGA input status 0 register
        w       VGA     miscellaneous output register
03C3    r/w     VGA     video subsystem enable (see also port 46E8h)
                        for IBM, motherboard VGA only
03C4    w       EGA     TS index register
        r/w     VGA     sequencer index register
03C5    w       EGA     TS data register
        r/w     VGA     other sequencer register
03C6    r/w     VGA     PEL mask register
03C7    r/w     VGA     PEL address read mode
        r       VGA     DAC state register
03C8    r/w     VGA     PEL address write mode
03C9    r/w     VGA     PEL data register
03CA    w       EGA     graphics 2 position register
        r       VGA     feature control register
03CC    w       EGA     graphics 1 position register
        r       VGA     miscellaneous output register
03CE    w       EGA     GDC index register
        r/w     VGA     graphics address register
03CF    w       EGA     GDC data register
```

```
        r/w     VGA     other graphics register

--------------------------------------------------------------------------------
03CE-03CF ----  Compaq Qvision - Functionality Level

03CE    w       graphics address register (index for next port)
03CF    r/w     other graphics register
                Index
                 0Ch    r       controller version
                                2Fh Advanced VGA
                                37h early QVision 1024
                                71h QVision 1280 or later QVision 1024
                 0Dh            extended controller version
                 0Eh            extended controller capabilities
                 0Fh            environment info
                 54h            available memory
                 55h            phase-locked-loop clock
                 56h-57h        controller capabilities

--------------------------------------------------------------------------------
03D0-03DF ----  CGA   (Color Graphics Adapter)

03D0            same as 03D4
03D1            same as 03D5
03D2            same as 03D4
03D3            same as 03D5
03D4    w       CRT (6845) index register   (EGA/VGA)
                selects which register (0-11h) is to be accessed through 3B5
03D5    w       CRT (6845) data register    (EGA/VGA)
                selected by port 3B4. registers C-F may be read
                 (for registers see at 3B5)
03D6            same as 03D4
                (under OS/2, reads return 0 if full-screen DOS session,
                nonzero if windowed DOS session)
03D7            same as 03D5
03D8    r/w     CGA mode control register  (except PCjr)
                 bit 7-6      not used
                 bit 5   = 1  blink enabled
                 bit 4   = 1  640*200 graphics mode
                 bit 3   = 1  video enabled
                 bit 2   = 1  monochrome signal
                 bit 1   = 0  text mode
                         = 1  320*200 graphics mode
                 bit 0   = 0  40*25 text mode
                         = 1  80*25 text mode

03D9    r/w     CGA palette register
                 bit 7-6      not used
                 bit 5   = 0 active color set: red, green brown
                         = 1 active color set: cyan, magenta, white
                 bit 4       intense colors in graphics, background colors text
                 bit 3       intense border in 40*25, intense background in
                             320*200, intense foreground in 640*200
                 bit 2       red border in 40*25, red background in 320*200,
                             red foreground in 640*200
                 bit 1       green border in 40*25, green background in
                             320*200, green foreground in 640*200
                 bit 0       blue border in 40*25, blue background in 320*200,
                             blue foreground in 640*200

03DA    r       CGA status register     EGA/VGA: input status 1 register
                 bit 7-4     not used
                 bit 3 = 1   in vertical retrace
                 bit 2 = 1   light pen switch is off
                 bit 1 = 1   positive edge from light pen has set trigger
                 bit 0 = 0   do not use memory
                       = 1   memory access without interfering with display

03DA    w       EGA/VGA feature control register

03DB    w       clear light pen latch
```

```
03DC    r/w     preset light pen latch

03DF            CRT/CPU page register  (PCjr only)

--------------------------------------------------------------------------------
03E8-03EF ----  serial port, same as 02E8, 02F8 and 03F8

--------------------------------------------------------------------------------
03F0-03F7 ----  FDC 1  (1st Floppy Disk Controller)     second FDC at 0370
                (8272, 8272A, NEC765)
                (82072, 82077AA for perpendicular recording at 2.8Mb)

03F0    r       diskette EHD controller board jumper settings (82072AA)
                 bit 7-6      drive 3
                 bit 5-4      drive 2
                 bit 3-2      drive 1
                 bit 1-0      drive 0
                         = 00  1.2Mb
                         = 01  720Kb
                         = 10  2.8Mb
                         = 11  1.4Mb

03F0    r       diskette controller status A (PS/2)
                 bit 7   interrupt pending
                 bit 6   -DRV2  second drive installed
                 bit 5   step
                 bit 4   -track 0
                 bit 3   head 1 select
                 bit 2   -index
                 bit 1   -write protect
                 bit 0   +direction

03F0    r       diskette controller status A (PS/2 model 30)
                 bit 7   interrupt pending
                 bit 6   DRQ
                 bit 5   step F/F
                 bit 4   -track 0
                 bit 3   head 1 select
                 bit 2   +index
                 bit 1   +write protect
                 bit 0   -direction

03F1    r       diskette controller status B (PS/2)
                 bit 7-6  =1 reserved
                 bit 5    drive select (0=A:, 1=B:)
                 bit 4    write data
                 bit 3    read data
                 bit 2    write enable
                 bit 1    motor enable 1
                 bit 0    motor enable 0

03F1    r       diskette controller status B (PS/2 model 30)
                 bit 7    -DRV2 second drive installed
                 bit 6    -DS1
                 bit 5    -DS0
                 bit 4    write data F/F
                 bit 3    read data F/F
                 bit 2    write enable F/F
                 bit 1    -DS3
                 bit 0    -DS2

03F2    w       diskette controller DOR (Digital Output Register)
                 bit 7-6    reserved on PS/2
                 bit 7 = 1  drive 3 motor enable
                 bit 6 = 1  drive 2 motor enable
                 bit 5 = 1  drive 1 motor enable
                 bit 4 = 1  drive 0 motor enable
                 bit 3 = 1  diskette DMA enable (reserved PS/2)
                 bit 2 = 1  FDC enable  (controller reset)
                       = 0  hold FDC at reset
                 bit 1-0    drive select (0=A 1=B ..)
```

```
03F3            tape drive register (on the 82077AA)
                 bit 7-2      reserved, tri-state
                 bit 1-0      tape select
                         = 00  none, drive 0 cannot be a tape drive.
                         = 01  drive1
                         = 10  drive2
                         = 11  drive3

03F4    r       diskette controller main status register
                 bit 7 = 1  RQM  data register is ready
                         0  no access is permitted
                 bit 6 = 1  transfer is from controller to system
                         0  transfer is from system to controller
                 bit 5 = 1  non-DMA mode
                 bit 4 = 1  diskette controller is busy
                 bit 3 = 1  drive 3 busy (reserved on PS/2)
                 bit 2 = 1  drive 2 busy (reserved on PS/2)
                 bit 1 = 1  drive 1 busy (= drive is in seek mode)
                 bit 0 = 1  drive 0 busy (= drive is in seek mode)
                Note:   in non-DMA mode, all data transfers occur through
                          port 03F5h and the status registers (bit 5 here
                          indicates data read/write rather than than
                          command/status read/write)

03F4    w       diskette controller data rate select register
                 bit 7-2      reserved on 8272
                 bit 7   = 1  software reset (self clearing)    82072/82077AA
                 bit 6   = 1  power down                        82072/82077AA
                 bit 5   = 0  reserved on 8272 and 82077AA
                              PLL select bit on 82072
                 bit 4-2      write precompensation value, 000 default
                 bit 1-0      data rate select
                         = 00  500 Kb/S MFM     250 Kb/S FM
                         = 01  300 Kb/S MFM     150 Kb/S FM
                         = 10  250 Kb/S MFM     125 Kb/S FM
                         = 11  1Mb/S    MFM     illegal  FM on 8207x

03F5    r       diskette command/data register 0 (ST0)
                 bit 7-6      last command status
                         = 00  command terminated successfully
                         = 01  command terminated abnormally
                         = 10  invalid command
                         = 11  terminated abnormally by change in ready signal
                 bit 5   = 1  seek completed
                 bit 4   = 1  equipment check occurred after error
                 bit 3   = 1  not ready
                 bit 2   = 1  head number at interrupt
                 bit 1-0 = 1  unit select (0=A 1=B .. )
                              (on PS/2  01=A  10=B)

                status register 1 (ST1)
                 bit 7      end of cylinder; sector# greater then sectors/track
                 bit 6 = 0
                 bit 5 = 1  CRC error in ID or data field
                 bit 4 = 1  overrun
                 bit 3 = 0
                 bit 2 = 1  sector ID not found
                 bit 1 = 1  write protect detected during write
                 bit 0 = 1  ID address mark not found

                status register 2 (ST2)
                 bit 7 = 0
                 bit 6 = 1  deleted Data Address Mark detected
                 bit 5 = 1  CRC error in data
                 bit 4 = 1  wrong cylinder detected
                 bit 3 = 1  scan command equal condition satisfied
                 bit 2 = 1  scan command failed, sector not found
                 bit 1 = 1  bad cylinder, ID not found
                 bit 0 = 1  missing Data Address Mark
```

status register 3 (ST3)
 bit 7 fault status signal
 bit 6 write protect status
 bit 5 ready status
 bit 4 track zero status
 bit 3 two sided status signal
 bit 2 side select (head select)
 bit 1-0 unit select (0=A 1=B ..)

03F5 w diskette command register. The commands summarized here are mostly multibyte commands. This is for brief recognition only.

MFM = MFM mode selected, opposite to MF mode.
HDS = head select
DS = drive select
MT = multi track operation
SK = skip deleted data address mark

Command	# bytes	D7	6	5	4	3	2	1	0
read track	9	0	MFM	0	0	0	0	1	0
		0	0	0	0	0	HDS	DS1	DS0
specify	3	0	0	0	O	O	O	1	1
sense drive status	2	0	0	0	0	0	1	0	0
		0	0	0	0	0	HDS	DS1	DS0
write data	9	MT	MFM	0	0	0	1	0	1
		0	0	0	0	0	HDS	DS1	DS0
read data	9	MT	MFM	SK	0	0	1	1	0
		0	0	0	0	0	HDS	DS1	DS0
recalibrate	2	0	0	0	0	0	1	1	1
		0	0	0	0	0	0	DS1	DS0
sense interrupt status	1	0	0	0	0	1	0	0	0
write deleted data	9	MT	MFM	0	0	1	0	0	1
		0	0	0	0	0	HDS	DS1	DS0
read ID	2	0	MFM	0	0	1	0	1	0
		0	0	0	0	0	HDS	DS1	DS0
read deleted data	9	MT	MFM	SK	0	1	1	0	0
		0	0	0	0	0	HDS	DS1	DS0
format track	10	0	MFM	0	0	1	1	0	1
		0	0	0	0	0	HDS	DS1	DS0
dumpreg **	1	0	0	0	0	1	1	1	0
seek	3	0	0	0	0	1	1	1	1
		0	0	0	0	0	HDS	DS1	DS0
version **	1	0	0	0	1	0	0	0	0
scan equal *	9	MT	MFM	SK	1	0	0	0	1
		0	0	0	0	0	HDS	DS1	DS0
perpendicular mode **	2	0	0	0	1	0	0	1	0
		0	0	0	0	0	0	WGATE	GAP
configure **	4	0	0	0	1	0	0	1	1
		0	0	0	0	0	0	0	0
verify	9	MT	MFM	SK	1	0	1	1	0
		EC	0	0	0	0	HDS	DS1	DS0
scan low or equal *	9	MT	MFM	SK	1	1	0	0	1
		0	0	0	0	0	HDS	DS1	DS0
scan high or equal *	9	MT	MFM	SK	1	1	1	0	1
		0	0	0	0	0	HDS	DS1	DS0
relative seek **	3	1	DIR	0	0	1	1	1	1
		0	0	0	0	0	HDS	DS1	DS0

BEWARE: not every invalid command is treated as invalid!
* Note: the scan commands aren't mentioned for the 82077AA.
** Note: EHD controller commands.

03F6 reserved on FDC

03F6 r/w FIXED disk controller data register
 bit 7-4 reserved
 bit 3 = 0 reduce write current
 1 head select 3 enable
 bit 2 = 1 disk reset enable
 0 disk reset disable
 bit 1 = 0 disk initialization enable

```
                        1  disk initialization disable
                 bit 0      reserved

03F7    r/w     harddisk controller
                 bit 6     FIXED DISK write gate
                 bit 5     FIXED DISK head select 3 / reduced write current
                 bit 4     FIXED DISK head select 2
                 bit 3     FIXED DISK head select 1
                 bit 2     FIXED DISK head select 0
                 bit 1     FIXED DISK drive 1 select
                 bit 0     FIXED DISK drive 0 select

03F7    r       diskette controller DIR (Digital Input Register, PC/AT mode)
                 bit 7 = 1 diskette change
                 bit 6-0   tri-state on FDC

03F7    r       diskette controller DIR (Digital Input Register, PS/2 mode)
                 bit 7   = 1 diskette change
                 bit 6-3 = 1
                 bit 2       datarate select1
                 bit 1       datarate select0
                 bit 0   = 0 high density select (500Kb/s, 1Mb/s)

 conflicts with  bit 0     FIXED DISK drive 0 select

03F7    r       diskette controller DIR (Digital Input Register, PS/2 model 30)
                 bit 7   = 0 diskette change
                 bit 6-4 = 0
                 bit 3       -DMA gate (value from DOR register)
                 bit 2       NOPREC (value from CCR register)
                 bit 1       datarate select1
                 bit 0       datarate select0

 conflicts with  bit 0     FIXED DISK drive 0 select

03F7    w       configuration control register (PC/AT, PS/2)
                 bit 7-2       reserved, tri-state
                 bit 1-0 = 00  500 Kb/S mode (MFM)
                         = 01  300 Kb/S mode (MFM)
                         = 10  250 Kb/S mode (MFM)
                         = 11  1   Mb/S mode (MFM) (on 82072/82077AA)

 conflicts with  bit 0     FIXED DISK drive 0 select

03F7    w       configuration control register (PS/2 model 30)
                 bit 7-3       reserved, tri-state
                 bit 2         NOPREC (has no function. set to 0 by hardreset)
                 bit 1-0 = 00  500 Kb/S mode (MFM)
                         = 01  300 Kb/S mode (MFM)
                         = 10  250 Kb/S mode (MFM)
                         = 11  1   Mb/S mode (MFM) (on 82072/82077AA)

 conflicts with  bit 0     FIXED DISK drive 0 select

--------------------------------------------------------------------------------
03F8-03FF ----  serial port (8250,8251,16450,16550,16550A,etc.)
                same as 02E8,02F8 and 03E8

03F8    w       serial port, transmitter holding register, which contains the
                character to be sent. Bit 0 is sent first.
                 bit 7-0   data bits when DLAB=0 (Divisor Latch Access Bit)
        r       receiver buffer register, which contains the received character
                Bit 0 is received first
                 bit 7-0   data bits when DLAB=0 (Divisor Latch Access Bit)
        r/w     divisor latch low byte when DLAB=1

03F9    r/w     divisor latch high byte when DLAB=1
        r/w     interrupt enable register when DLAB=0
                 bits 7-4   reserved
                 bit 3 = 1  modem-status interrupt enable
                 bit 2 = 1  receiver-line-status interrupt enable
```

```
                bit 1 = 1  transmitter-holding-register empty interrupt enable
                bit 0 = 1  received-data-available interrupt enable
                               (also 16550(A) timeout interrupt)

              - 16550(A) will interrupt with a timeout if data exists in the
                FIFO and isn't read within the time it takes to receive four
                bytes or if no data is received within the time it takes to
                receive four bytes

03FA    r       interrupt identification register. Information about a pending
                interrupt is stored here. When the ID register is addressed,
                the highest priority interrupt is held, and no other interrupts
                are acknowledged until the CPU services that interrupt.
                 bit 7-6 = 00  reserved on 8250, 8251, 16450
                         = 01  if FIFO queues enabled (16550 only)
                         = 11  if FIFO queues are enabled (16550A only)
                 bit 5-4 = 0 reserved
                 bit 3   = 0 reserved  8250, 16450
                         = 1 16550  timeout int. pending
                 bit 2-1 identify pending interrupt with the highest priority
                  = 11  receiver line status interrupt. priority=highest
                  = 10  received data available register interrupt. pr.=second
                  = 01  transmitter holding register empty interrupt. pr.=third
                  = 00  modem status interrupt. priority=fourth
                 bit 0 = 0  interrupt pending. contents of register can be used
                            as a pointer to the appropriate int.service routine
                         1  no interrupt pending

              - interrupt pending flag uses reverse logic, 0=pending, 1=none
              - interrupt will occur if any of the line status bits are set
              - THRE bit is set when THRE register is emptied into the TSR


03FA    w       16650 FCR  (FIFO Control Register)
                 bit 7-6 = received data available interrupt trigger level
                        00  1 byte
                        01  4 bytes
                        10  8 bytes
                        11 14 bytes
                 bit 5-4 = 00 reserved
                 bit 3   = 1  change RXRDY  TXRDY pins from mode 0 to mode 1
                 bit 2   = 1  clear XMIT FIFO
                 bit 1   = 1  clear RCVR FIFO
                 bit 0   = 1  enable clear XMIT and RCVR FIFO queues

              - bit 0 must be set in order to write to other FCR bits
              - bit 1 when set  the RCVR FIFO is cleared and this bit is reset
                 the receiver shift register is not cleared
              - bit 2 when set  the XMIT FIFO is cleared and this bit is reset
                 the transmit shift register is not cleared
              - due to a hardware bug, 16550 FIFOs don't work correctly (this
                was fixed in the 16550A)

03FB    r/w     line control register
                 bit 7 = 1  divisor latch access bit (DLAB)
                         0  receiver buffer, transmitter holding, or interrupt
                            enable register access
                 bit 6 = 1  set break enable. serial ouput is forced to spacing
                            state and remains there.
                 bit 5 =    stick parity
                 bit 4 = 1  even parity select
                 bit 3 =    parity enable
                         1  even number of ones are sent and checked in the
                            data word bits and parity bit
                         0  odd number of ones are sent and checked
                 bit 2 = 0  one stop bit
                         1  zero stop bit
                 bit 1-0 00 word length is 5 bits
                         01 word length is 6 bits
                         10 word length is 7 bits
                         11 word length is 8 bits
```

```
03FC    r/w     modem control register
                 bit 7-5 = 0  reserved
                 bit 4 = 1  loopback mode for diagnostic testing of serial port
                            output of transmitter shift register is looped back
                            to receiver shift register input. In this mode
                            transmitted data is received immediately so that
                            the CPU can verify the transmit data/receive data
                            serial port paths.
                 bit 3 = 1  auxiliary user-designated output 2
                 bit 2 = 1  auxiliary user-designated output 1
                 bit 1 = 1  force request-to-send active
                 bit 0 = 1  force data-terminal-ready active

03FD    r       line status register
                 bit 7 = 0  reserved
                 bit 6 = 1  transmitter shift and holding registers empty
                 bit 5 = 1  transmitter holding register empty. Controller is
                            ready toaccept a new character to send.
                 bit 4 = 1  break interrupt. the received data input is held in
                            in the zero bit state longer than the time of start
                            bit + data bits + parity bit + stop bits.
                 bit 3 = 1  framing error. the stop bit that follows the last
                            parity or data bit is a zero bit.
                 bit 2 = 1  parity error. Character has wrong parity
                 bit 1 = 1  overrun error. a character was sent to the receiver
                            buffer before the previous character in the buffer
                            could be read. This destroys the previous
                            character.
                 bit 0 = 1  data ready. a complete incoming character has been
                            received and sent to the receiver buffer register.

03FE    r       modem status register
                 bit 7 = 1  data carrier detect
                 bit 6 = 1  ring indicator
                 bit 5 = 1  data set ready
                 bit 4 = 1  clear to send
                 bit 3 = 1  delta data carrier detect
                 bit 2 = 1  trailing edge ring indicator
                 bit 1 = 1  delta data set ready
                 bit 0 = 1  delta clear to send

              - bits 0-3 are reset when the CPU reads the MSR
              - bit 4 is the Modem Control Register RTS during loopback test
              - bit 5 is the Modem Control Register DTR during loopback test
              - bit 6 is the Modem Control Register OUT1 during loopback test
              - bit 7 is the Modem Control Register OUT2 during loopback test

03FF    r/w     scratch register

--------------------------------------------------------------------------------

                Adresses above 03FF apply to EISA machines only !

                        1000-1FFF      slot 1 EISA
                        2000-2FFF      slot 2 EISA
                        3000-3FFF      slot 3 EISA
                        4000-4FFF      slot 4 EISA
                        5000-5FFF      slot 5 EISA
                        6000-6FFF      slot 6 EISA
                        7000-7FFF      slot 7 EISA

--------------------------------------------------------------------------------
0401-04D6 ----  used by EISA systems only

0401    r/w     DMA channel 0 word count byte 2 (high)
0403    r/w     DMA channel 1 word count byte 2 (high)
0405    r/w     DMA channel 2 word count byte 2 (high)
0407    r/w     DMA channel 3 word count byte 2 (high)

040A    w       extended DMA chaining mode register, channels 0-3
```

```
                bit 7-5      reserved
                bit 4   = 0  generates IRQ13
                        = 1  generates terminal count
                bit 3   = 0  do not start chaining
                        = 1  programming complete
                bit 2   = 0  disable buffer chaining mode (default)
                        = 1  enable buffer chaining mode
                bit 1-0      DMA channel select

040A    r       channel interrupt (IRQ13) status register
                bit 7-5  interrupt on channels 7-5
                bit 4    reserved
                bit 3-0  interrupt on channels 3-0

040B    w       DMA extended mode register for channels 3-0.
                bit settings same as 04D6
                bit 7   = 0  enable stop register
                bit 6   = 0  terminal count is an output for this channel
                               (default)
                bit 5-4      DMA cycle timing
                        = 00 ISA-compatible (default)
                        = 01 type A timing mode
                        = 10 type B timing mode
                        = 11 burst DMA mode
                bit 3-2      Address mode
                        = 00 8-bit I/O, count by bytes (default)
                        = 01 16-bit I/O, count by words, address shifted
                        = 10 32-bit I/O, count by bytes
                        = 11 16-bit I/O, count by bytes
                bit 1-0      DMA channel select

-------------------------------------------------------------------------------
0461    r/w     Extended NMI status/control register
                bit 7 = 1  NMI pending from fail-safe timer (read only)
                bit 6 = 1  NMI pending from bus timeout NMI status (read
only)
                bit 5 = 1  NMI pending (read only)
                bit 4      reserved
                bit 3 = 1  bus timeout NMI enable (read/write)
                bit 2 = 1  fail-safe NMI enable (read/write)
                bit 1 = 1  NMI I/O port enable (read/write)
                bit 0      RSTDRV. bus reset (read/write)
                      = 0  NORMAL bus reset operation
                      = 1  reset bus asserted

0462    w       Software NMI register. writing to this register causes an NMI
                if NMI's are enabled
                bit 7 = 1  generates an NMI

0464    r       bus master status latch register (slots 1-8). identifies the
                last bus master that had control of the bus
                bit 7 = 0  slot 8 had control last
                bit 6 = 0  slot 7 had control last
                bit 5 = 0  slot 6 had control last
                bit 4 = 0  slot 5 had control last
                bit 3 = 0  slot 4 had control last
                bit 2 = 0  slot 3 had control last
                bit 1 = 0  slot 2 had control last
                bit 0 = 0  slot 1 had control last

0465    r       bus master status latch register (slots 9-16)
                bit 7 = 0  slot 16 had control last
                bit 6 = 0  slot 15 had control last
                bit 5 = 0  slot 14 had control last
                bit 4 = 0  slot 13 had control last
                bit 3 = 0  slot 12 had control last
                bit 2 = 0  slot 11 had control last
                bit 1 = 0  slot 10 had control last
                bit 0 = 0  slot 9  had control last

-------------------------------------------------------------------------------
```

```
0481-048B ---- EISA DMA page registers

0481    r/w     DMA channel 2 address byte 3 (high)
0482    r/w     DMA channel 3 address byte 3 (high)
0483    r/w     DMA channel 1 address byte 3 (high)
0487    r/w     DMA channel 0 address byte 3 (high)
0489    r/w     DMA channel 6 address byte 3 (high)
048A    r/w     DMA channel 7 address byte 3 (high)
048B    r/w     DMA channel 5 address byte 3 (high)

--------------------------------------------------------------------------------
04C6-04CF ---- EISA DMA count registers

04C6    r/w     DMA channel 5 word count byte 2 (high)
04CA    r/w     DMA channel 6 word count byte 2 (high)
04CE    r/w     DMA channel 7 word count byte 2 (high)

--------------------------------------------------------------------------------
04D0-04D1 ---- EISA IRQ control

04D0    w       IRQ 0-7 interrupt edge/level registers
                 bit 7 = 1  IRQ 7 is level sensitive
                 bit 6 = 1  IRQ 6 is level sensitive
                 bit 5 = 1  IRQ 5 is level sensitive
                 bit 4 = 1  IRQ 4 is level sensitive
                 bit 3 = 1  IRQ 3 is level sensitive
                 bit 2-0    reserved

04D1    w       IRQ 8-15 interrupt edge/level registers
                 bit 7 = 1  IRQ 15 is level sensitive
                 bit 6 = 1  IRQ 14 is level sensitive
                 bit 5 = 1  reserved
                 bit 4 = 1  IRQ 12 is level sensitive
                 bit 3 = 1  IRQ 11 is level sensitive
                 bit 2 = 1  IRQ 10 is level sensitive
                 bit 1 = 1  IRQ 9  is level sensitive
                 bit 0      reserved

--------------------------------------------------------------------------------
04D4-04D6 ---- EISA DMA control

04D4    r       DMA chaining status

04D4    w       extended DMA chaining mode register, channels 4-7
                 bit 7-5 = 0  reserved
                 bit 4   = 0  generates IRQ 13
                         = 1  generates terminal count
                 bit 3   = 0  do not start chaining
                         = 1  programming complete
                 bit 2   = 0  disable buffer chaining mode (default)
                         = 1  enable buffer chaining mode
                 bit 1-0      DMA channel select

04D6    w       DMA extended mode register for channels 4-7
                bit settings same as 04B
                 bit 7   = 0  enable stop register
                 bit 6   = 0  terminal count is an output for this channel
                                (default)
                 bit 5-4      DMA cycle timing
                         = 00 ISA-compatible (default)
                         = 01 type A timing mode
                         = 10 type B timing mode
                         = 11 burst DMA mode
                 bit 3-2      Address mode
                         = 00 8-bit I/O, count by bytes (default)
                         = 01 16-bit I/O, count by words, address shifted
                         = 10 32-bit I/O, count by bytes
                         = 11 16-bit I/O, count by bytes
                 bit 1-0      DMA channel select

--------------------------------------------------------------------------------
```

```
04E0-04FF ---- EISA DMA stop registers

04E0-04E2 r/w   channel 0
04E4-04E6 r/w   channel 1
04E8-04EA r/w   channel 2
04EC-04EE r/w   channel 3
04F4-04F6 r/w   channel 5
04F8-04FA r/w   channel 6
04FC-04FE r/w   channel 7

--------------------------------------------------------------------------------
0530-0533 ----  Gravis Ultra Sound Daughter Card by Advanced Gravis
         The I/O address range is dipswitch selectable from:
           0530-0533
           0604-0607
           0E80-0E83
           0F40-0F43

0530    r/w     Address Select
0531    r/w     Data
0532    r/w     Status
0533    r/w     PIO

--------------------------------------------------------------------------------
0601    w       System control. Laptop chipset: Headland HL21 & Acer M5105
                 bit 7 = 1  power led on
                 bit 6 = 1  LCD backlight off
                 bit 5
                 bit 4
                 bit 3
                 bit 2 = 1  video chips disabled, screen blanked.
                 bit 1
                 bit 0 = 1  will lock up your machine!

        r        bit 7 = 0  if screen enabled always these values
                 bit 6 = 0
                 bit 5 = 0
                 bit 4 = 0
                 bit 3 = 0
                 bit 2 = 1  (=0 at low power)
                 bit 1 = 0  power OK
                 bit 0 = 0

--------------------------------------------------------------------------------
0620-0627 ----  PC network (adapter 1)
0628-062F ----  PC network (adapter 2)

--------------------------------------------------------------------------------
0680      ----  Microchannel POST Diagnostic (write only)

--------------------------------------------------------------------------------
06E2-06E3 ----  data aquisition (adapter 1)

--------------------------------------------------------------------------------
06E8      ----  S3 86C928 video controller (ELSA Winner 1000)

--------------------------------------------------------------------------------
06E8-06EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

06E8    w       horizontal displayed

        See also 02E8-02EF, 0AE8, 96E8, 9AE8

--------------------------------------------------------------------------------
0746      ----  Gravis Ultra Sound by Advanced Gravis

0746    r       Board Version (rev 3.7+)
                 FF       Pre 3.6 boards, ICS mixer NOT present
                 05       Rev 3.7 with ICS Mixer. Some R/L: flip problems.
                 06-09    Revision 3.7 and above. ICS Mixer present
                 0A-      UltraMax. CS4231 present, no ICS mixer
```

```
        w       Mixer Control Port

SeeAlso: 0240-024F, 0340-034F

--------------------------------------------------------------------------
0790-0793 ----  cluster (adapter 1)

--------------------------------------------------------------------------
0800-08FF ----  I/O port access registers for extended CMOS RAM or SRAM
                (256 bytes at a time)
                Sometimes plain text can be seen here.

--------------------------------------------------------------------------
0800-08FF ----  reserved for EISA system motherboard

--------------------------------------------------------------------------
0A20-0A23 ----  Token Ring (adapter 1)
0A24-0A27 ----  Token Ring (adapter 2)

--------------------------------------------------------------------------
0AE2-0AE3 ----  cluster (adapter 2)

--------------------------------------------------------------------------
0AE8      ----  S3 86C928 video controller (ELSA Winner 1000)

--------------------------------------------------------------------------
0AE8-0AEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

0AE8    w       horizontal sync start

--------------------------------------------------------------------------
0B90-0B93 ----  cluster (adapter 2)

--------------------------------------------------------------------------
0C00    r/w     page register to write to SRAM or I/O

--------------------------------------------------------------------------
0C00-0CFF ----  reserved for EISA system motherboard

--------------------------------------------------------------------------
0C7C            bit 7-4 (Compaq)

--------------------------------------------------------------------------
0C80-0C83 ----  EISA system board ID registers

--------------------------------------------------------------------------
0CF8      ----  Intel Pentium motherboard ("Neptune" chipset)

--------------------------------------------------------------------------
0CFA      ----  Intel Pentium motherboard ("Neptune" chipset)

--------------------------------------------------------------------------
0EE8      ----  S3 86C928 video controller (ELSA Winner 1000)

--------------------------------------------------------------------------
0EE8-0EEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

0EE8    w       horizontal sync width

--------------------------------------------------------------------------
1000-10FF ----  available for EISA slot 1

--------------------------------------------------------------------------
12E8-12EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

12E8    w       vertical total

--------------------------------------------------------------------------
1390-1393 ----  cluster (adapter 3)

--------------------------------------------------------------------------
```

```
1400-14FF ----  available for EISA slot 1

--------------------------------------------------------------------------------
16E8-16EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

16E8    w       vertical displayed

--------------------------------------------------------------------------------
1800-18FF ----  available for EISA slot 1

--------------------------------------------------------------------------------
1AE8-1AEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

1AE8    w       vertical sync start

--------------------------------------------------------------------------------
1C00-1CFF ----  available for EISA slot 1

--------------------------------------------------------------------------------
1C80-1C8F ----  VESA XGA Video in EISA slot 1

1C80-1C83 r/w   EISA Video ID
1C84    r/w     EISA Video expansion board control
1C85    r/w     EISA Setup control
1C88    r/w     EISA Video Programmable Option Select 0
1C89-1C8F r/w   EISA Video Programmable Option Select 1-7

--------------------------------------------------------------------------------
1C80-1C83       EISA board product ID (board in slot 1)

--------------------------------------------------------------------------------
1C85            Compaq Qvision EISA - Virtual Controller ID

--------------------------------------------------------------------------------
1EE8-1EEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

1EE8    w       vertical sync width

--------------------------------------------------------------------------------
2000-20FF ----  available for EISA slot 2

--------------------------------------------------------------------------------
2100-210F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (first installed)
2110-211F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (second installed)
2120-212F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (third installed)
2130-213F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (fourth installed)
2140-214F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (fifth installed)
2150-215F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (sixth installed)
2160-216F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (seventh installed)
2170-217F ----  IBM XGA (eXtended Graphics Adapter  8514/A) (eighth installed)

--------------------------------------------------------------------------------
2100      ----  XGA Video Operating Mode Register

Note:   this port is for the first XGA in the system; 2110-2170 are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2101      ----  XGA VIdeo Aperture Control

Note:   this port is for the first XGA in the system; 2111-2171 are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2102-2103 ----  XGA ???

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2104      ----  XGA Video Interrupt Enable
```

```
Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2105      ----  XGA Video Interrupt Status

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2106      ----  XGA Video Virtual Memory Control

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2107      ----  XGA Video Virtual Memory Interrupt Status

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2108      ----  XGA Video Aperture Index

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2109      ----  XGA Video Memory Access Mode

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
210A      ----  XGA Video Index for Data

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
210B      ----  XGA Video Data (byte)

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
210C-210F ----  XGA Video Data (word/dword)

Note:   this port is for the first XGA in the system; 211x-217x are used for
          the second through eighth XGAs

--------------------------------------------------------------------------------
2110-217F ----  secondary XGA adapters (see individual entries above)

--------------------------------------------------------------------------------
22E8-22EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

22E8    w       display control

--------------------------------------------------------------------------------
2390-2393 ----  cluster (adapter 4)

--------------------------------------------------------------------------------
23C0-23CF ----  Compaq QVision - BitBLT engine

--------------------------------------------------------------------------------
2400-24FF ----  available for EISA slot 2

--------------------------------------------------------------------------------
27C6    r/w     LCD timeout in minutes (Compaq LTE Lite)
```

```
------------------------------------------------------------------------------
2800-28FF ----  available for EISA slot 2

------------------------------------------------------------------------------
28E9      ----  8514/A - WD Escape Functions

------------------------------------------------------------------------------
2C80-2C8F ----  VESA XGA Video in EISA slot 2 (see 1C80-1C8F)

------------------------------------------------------------------------------
2C80-2C83       EISA board product ID (board in slot 2)

------------------------------------------------------------------------------
3000-30FF ----  available for EISA slot 3

------------------------------------------------------------------------------
3220-3227 ----  serial port 3, description same as 03F8
3228-322F ----  serial port 4, description same as 03F8

------------------------------------------------------------------------------
33C0-33CF ----  Compaq QVision - BitBLT engine

------------------------------------------------------------------------------
3400-34FF ----  available for EISA slot 3

------------------------------------------------------------------------------
3540-354F ----  IBM SCSI (Small Computer System Interface) adapter
3550-355F ----  IBM SCSI (Small Computer System Interface) adapter
3560-356F ----  IBM SCSI (Small Computer System Interface) adapter
3570-357F ----  IBM SCSI (Small Computer System Interface) adapter

------------------------------------------------------------------------------
3800-38FF ----  available for EISA slot 3

------------------------------------------------------------------------------
3C00-3CFF ----  available for EISA slot 3

------------------------------------------------------------------------------
3C80-3C8F ----  VESA XGA Video in EISA slot 3

3C80-3C83 r/w   EISA Video ID
3C84    r/w     EISA Video expansion board control
3C85    r/w     EISA Setup control
3C88    r/w     EISA Video Programmable Option Select 0
3C89-3C8F r/w   EISA Video Programmable Option Select 1-7

SeeAlso: 1C80-1C8F,2C80-2C8F,7C80-7C8F

------------------------------------------------------------------------------
3C80-3C83       EISA board product ID (board in slot 3)

------------------------------------------------------------------------------
4000-40FF ----  available for EISA slot 4

------------------------------------------------------------------------------
4220-4227 ----  serial port, description same as 03F8
4228-422F ----  serial port, description same as 03F8

------------------------------------------------------------------------------
42E0-42EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

42E1    r/w     GPIB (adapter 2)

------------------------------------------------------------------------------
42E8      ----  8514/A and hardware-compatible video cards

42E8    r       Subsystem Status
42E8    w       Subsystem Control

------------------------------------------------------------------------------
```

```
4400-44FF ----  available for EISA slot 4

--------------------------------------------------------------------------
46E8      ----  VGA video adapter enable

46E8    r/w     enable flags
                bits 7-5 unused or vendor-specific
                bit 4: setup for POS registers (MCA)
                bit 3: enable video I/O ports and video buffer
                bits 2-0 unused or vendor-specific

Note:   IBM uses this port for adapter-card VGAs only, and port 03C3 for
          motherboard VGA only

SeeAlso: 03C3

--------------------------------------------------------------------------
46E8      ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

46E8    w       ROM page select

--------------------------------------------------------------------------
4800-48FF ----  available for EISA slot 4

--------------------------------------------------------------------------
4AE8-4AEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

4AE8    w       Advanced function control
                (02h = VGA mode, 03h = 480-line mode, 07h = 768-line mode)

--------------------------------------------------------------------------
4C00-4CFF ----  available for EISA slot 4

--------------------------------------------------------------------------
4C80-4C83       EISA board product ID (board in slot 4)

--------------------------------------------------------------------------
4C80-4C8F ----  VESA XGA Video in EISA slot 4 (see 3C80-3C8F)

SeeAlso: 1C80-1C8F,6C80-6C8F

--------------------------------------------------------------------------
5000-50FF ----  available for EISA slot 5

--------------------------------------------------------------------------
5220-5227 ----  serial port, description same as 03F8
5228-522F ----  serial port, description same as 03F8

--------------------------------------------------------------------------
5400-54FF ----  available for EISA slot 5

--------------------------------------------------------------------------
5800-58FF ----  available for EISA slot 5

--------------------------------------------------------------------------
5C00-5CFF ----  available for EISA slot 5

--------------------------------------------------------------------------
5C80-5C8F ----  VESA XGA Video in EISA slot 5

5C80-5C83 r/w   EISA Video ID
5C84    r/w     EISA Video expansion board control
5C85    r/w     EISA Setup control
5C88    r/w     EISA Video Programmable Option Select 0
5C89-5C8F r/w   EISA Video Programmable Option Select 1-7

SeeAlso: 2C80-2C8F,4C80-4C8F,6C80-6C8F

--------------------------------------------------------------------------
5C80-5C83       EISA board product ID (board in slot 5)
```

```
--------------------------------------------------------------------------------
6000-60FF ----  available for EISA slot 6

--------------------------------------------------------------------------------
62E0-62EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

62E1    r/w     GPIB (adapter 3)

--------------------------------------------------------------------------------
63C0-63CF ----  Compaq QVision - BitBLT engine

--------------------------------------------------------------------------------
6400-64FF ----  available for EISA slot 6

--------------------------------------------------------------------------------
6800-68FF ----  available for EISA slot 6

--------------------------------------------------------------------------------
6C00-6CFF ----  available for EISA slot 6

--------------------------------------------------------------------------------
6C80-6C83       EISA board product ID (board in slot 6)

--------------------------------------------------------------------------------
6C80-6C8F ----  VESA XGA Video in EISA slot 1

6C80-6C83 r/w   EISA Video ID
6C84    r/w     EISA Video expansion board control
6C85    r/w     EISA Setup control
6C88    r/w     EISA Video Programmable Option Select 0
6C89-1C8F r/w   EISA Video Programmable Option Select 1-7

SeeAlso: 1C80-1C8F,2C80-2C8F,5C80-5C8F

--------------------------------------------------------------------------------
7000-70FF ----  available for EISA slot 7

--------------------------------------------------------------------------------
7400-74FF ----  available for EISA slot 7

--------------------------------------------------------------------------------
7800-78FF ----  available for EISA slot 7

--------------------------------------------------------------------------------
7C00-7CFF ----  available for EISA slot 7

--------------------------------------------------------------------------------
7C80-7C83       EISA board product ID (board in slot 7)

--------------------------------------------------------------------------------
7C80-7C8F ----  VESA XGA Video in EISA slot 7

7C80-7C83 r/w   EISA Video ID
7C84    r/w     EISA Video expansion board control
7C85    r/w     EISA Setup control
7C88    r/w     EISA Video Programmable Option Select 0
7C89-7C8F r/w   EISA Video Programmable Option Select 1-7

SeeAlso: 1C80-1C8F, 6C80-6C8F

--------------------------------------------------------------------------------
8000-80FF ----  available for EISA slot 8

--------------------------------------------------------------------------------
82E0-82EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

82E1    r/w     GPIB (adapter 4)

--------------------------------------------------------------------------------
82E8-82EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)
```

```
82E8    w       current Y position

--------------------------------------------------------------------------------
82F8-82FF ----  serial port, description same as 03F8
83F8-83FF ----  serial port, description same as 03F8

--------------------------------------------------------------------------------
83C0-83CF ----  Compaq QVision - Line Draw Engine

--------------------------------------------------------------------------------
83C4      ----  Compaq Qvision EISA - Virtual Controller Select

--------------------------------------------------------------------------------
83C6-83C9 ----  Compaq Qvision EISA - DAC color registers

--------------------------------------------------------------------------------
8400-84FF ----  available for EISA slot 8

--------------------------------------------------------------------------------
86E8-86EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

86E8    w       current X position

--------------------------------------------------------------------------------
8800-88FF ----  available for EISA slot 8

--------------------------------------------------------------------------------
8AE8-8AEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

8AE8    w       destination Y position / axial step constant

--------------------------------------------------------------------------------
8C00-8CFF ----  available for EISA slot 8

--------------------------------------------------------------------------------
8C80-8C83       EISA board product ID (board in slot 8)

--------------------------------------------------------------------------------
8EE8-8EEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

8EE8    w       destination X position / axial step constant

--------------------------------------------------------------------------------
9000-90FF ----  available for EISA slot 9

--------------------------------------------------------------------------------
92E8-92EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

92E8    w       error term

--------------------------------------------------------------------------------
9400-94FF ----  available for EISA slot 9

--------------------------------------------------------------------------------
96E8-96EF ----  8514/A and hardware-compatible video cards

96E8    r       Enter WD Enhanced Mode
96E8    w       major axis pixel count

--------------------------------------------------------------------------------
9800-98FF ----  available for EISA slot 9

--------------------------------------------------------------------------------
9AE8h-9AE9h ----  8514/A Graphics Processor Status

9AE8w   r       bit 9: hardware busy
9AE8    w       command

--------------------------------------------------------------------------------
9C00-9CFF ----  available for EISA slot 9
```

```
--------------------------------------------------------------------------------
9C80-9C83       EISA board product ID (board in slot 9)

--------------------------------------------------------------------------------
A220      ????  soundblaster support in AMI Hi-Flex BIOS  ????

--------------------------------------------------------------------------------
A2E0-A2EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

A2E1    r/w     GPIB (adapter 5)

--------------------------------------------------------------------------------
A2E8-A2EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

A2E8    w       background color

--------------------------------------------------------------------------------
A6E8-A6EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

A6E8    w       foreground color

--------------------------------------------------------------------------------
AAE8-AAEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

AAE8    w       write mask

--------------------------------------------------------------------------------
AEE8-AEEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

AEE8    w       read mask

--------------------------------------------------------------------------------
AFFF    r/w     plane 0-3 system latch (video register)

--------------------------------------------------------------------------------
B220-B227 ----  serial port, description same as 03F8
B228-B22F ----  serial port, description same as 03F8

--------------------------------------------------------------------------------
B2E8-B2EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

B2E8    w       color compare

--------------------------------------------------------------------------------
B6E8-B6EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

B6E8    w       background mix

--------------------------------------------------------------------------------
BAE8-BAEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

BAE8    w       foreground mix

--------------------------------------------------------------------------------
BEE8-BEEF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

BEE8    w       multi-function control

--------------------------------------------------------------------------------
C008      ----  Intel Pentium motherboard ("Neptune" chipset)

--------------------------------------------------------------------------------
C050      ----  Intel Pentium motherboard ("Neptune" chipset)

C050    r/w     bit 2: ???

--------------------------------------------------------------------------------
C052      ----  Intel Pentium motherboard ("Neptune" chipset)

C052    r/???   bits 6,7: ???
```

```
-------------------------------------------------------------------------------
C220-C227 ----  serial port, description same as 03F8
C228-C22F ----  serial port, description same as 03F8

-------------------------------------------------------------------------------
C2E0-C2EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

C2E1    r/w     GPIB (adapter 6)

-------------------------------------------------------------------------------
D220-D227 ----  serial port, description same as 03F8
D228-D22F ----  serial port, description same as 03F8

-------------------------------------------------------------------------------
E2E0-E2EF ----  GPIB (General Purpose Interface Bus, IEEE 488 interface)

E2E1    r/w     GPIB (adapter 7)

-------------------------------------------------------------------------------
E2E8-E2EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

E2E8    w       pixel data transfer

-------------------------------------------------------------------------------

MEMORY-MAPPED ADDRESSES

-------------------------------------------------------------------------------
80C00000  Compaq Deskpro 386 system memory board register

80C00000 w      RAM relocation register
                bit 7-2    Reserved, always write 1's.
                bit 1 = 0  Write-protect 128-Kbyte RAM at FE0000.
                      = 1  Do not write-protect RAM at FE0000.
                bit 0 = 0  Relocate 128-Kbyte block at FE0000 to address 0E0000
                      = 1  128-Kbyte RAM is addressed only at FE0000.

80C00000 r      Diagnostics register
                bit 7   = 0  memory expansion board is installed
                bit 6   = 0  second 1 MB of system memory board is installed
                bit 5-4 = 00 base memory set to 640 KB
                          01 invalid
                          10 base memory set to 512 KB
                          11 base memory set to 256 KB
                bit 3   = 0  parity error in byte 3
                bit 2   = 0  parity error in byte 2
                bit 1   = 0  parity error in byte 1
                bit 0   = 0  parity error in byte 0 (in 32-bit double word)

-------------------------------------------------------------------------------
C0000000-C000FFFF       Weitek "Abacus" math coprocessor

-------------------------------------------------------------------------------




-------------CREDITS--------------------------
Chuck Proctor <71534.2302@CompuServe.COM>
Richard W. Watson  <73042.1420@CompuServe.COM>

[Some of the information in this list was extracted from Frank van Gilluwe's
_The_Undocumented_PC_, a must-have book for anyone programming down to the
"bare metal" of a PC.]

[Some of the information in this list from the shareware version of Dave
Williams' DOSREF, v3.0]

[8514/A hardware ports found in FractInt v18.0 source file FR8514A.ASM]

[Compaq QVision info from the _COMPAQ_QVision_Graphics_System_Technical_
```

_Reference_Guide_, second edition (October 1993). Compaq part number 073A/0693. Much more to come!]