

# **CMP305**

# **Very Large Scale Integrated**

# **Circuit**

Lab 3

Place & Route (Part 1)

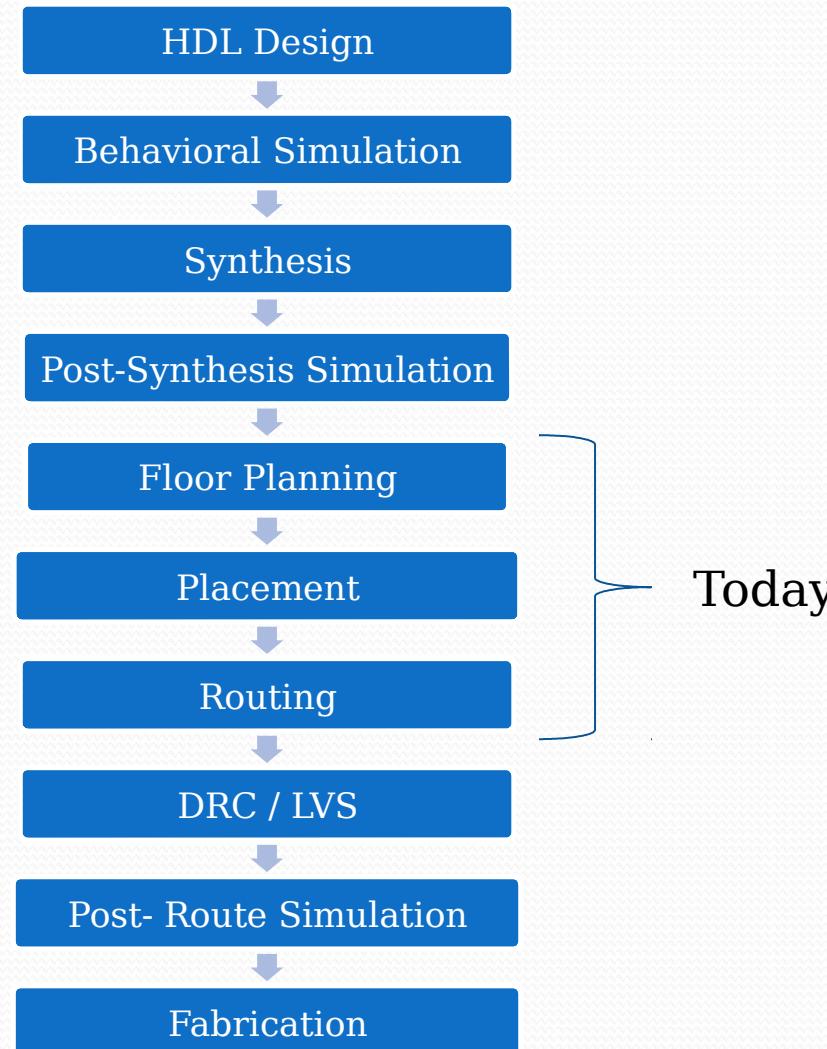
# Last 2 labs

- We Discussed ASIC Design Flow
- We applied Synthesis Step
- We Learned about Timing Analysis
- We applied design constraints
- We used Tcl script instead of GUI
- We performed post-synthesis simulation

# Objectives

- Understand:
  - Floor Planning
  - Placement of cells
  - Power & Wire Routing
  - Layout Reports & Generation (GDSII file)
  
- Learn:
  - Use Pyxis
  - Post-Layout Simulation

# ASIC Design Flow



# Place & Route Flow



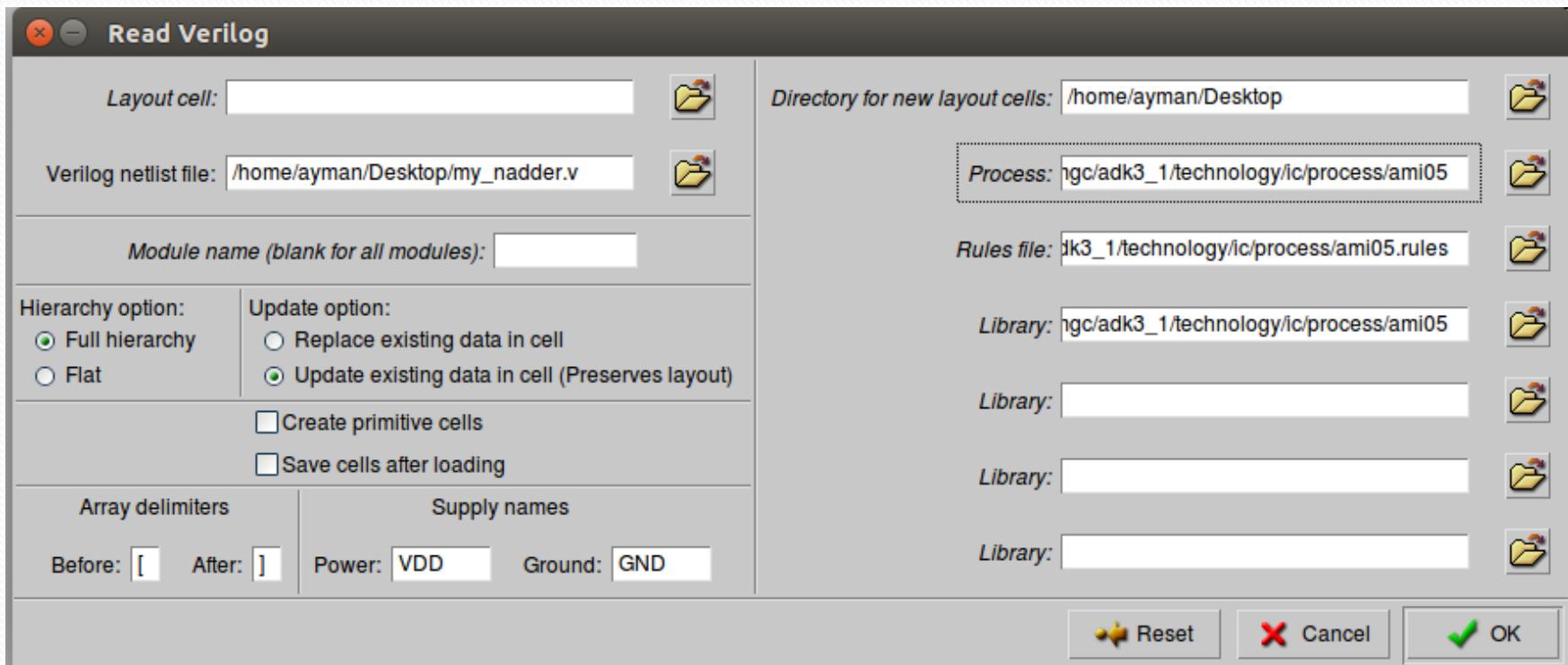
# Opening Pyxis

- Open the “Pyxis Layout Editor” from the Terminal

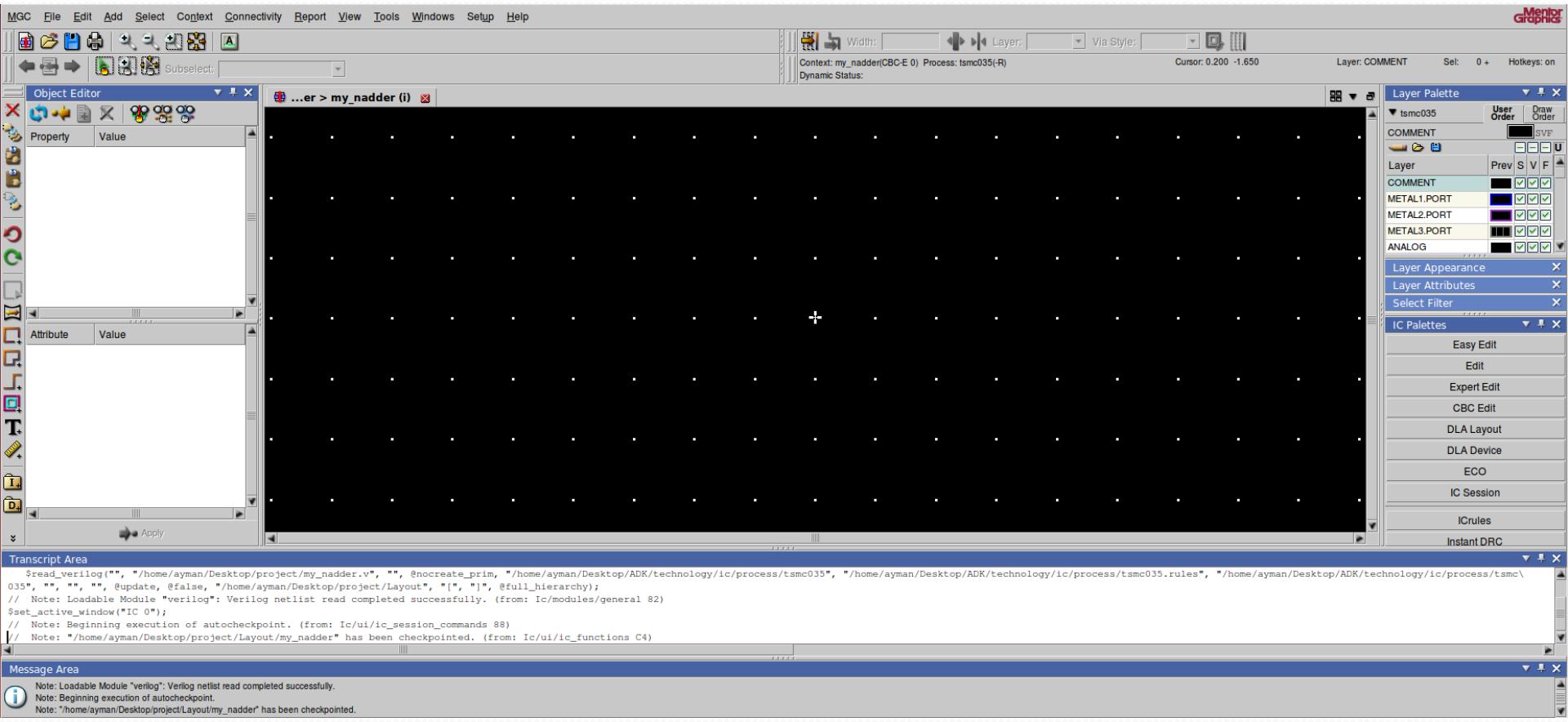
```
/> ic >> IC_run.log
```

# Step1&2: Import Netlist

- Click “File”
- Hover on “Import” then Click on “Verilog”
- Fill the window as follows



# Pyxis Window

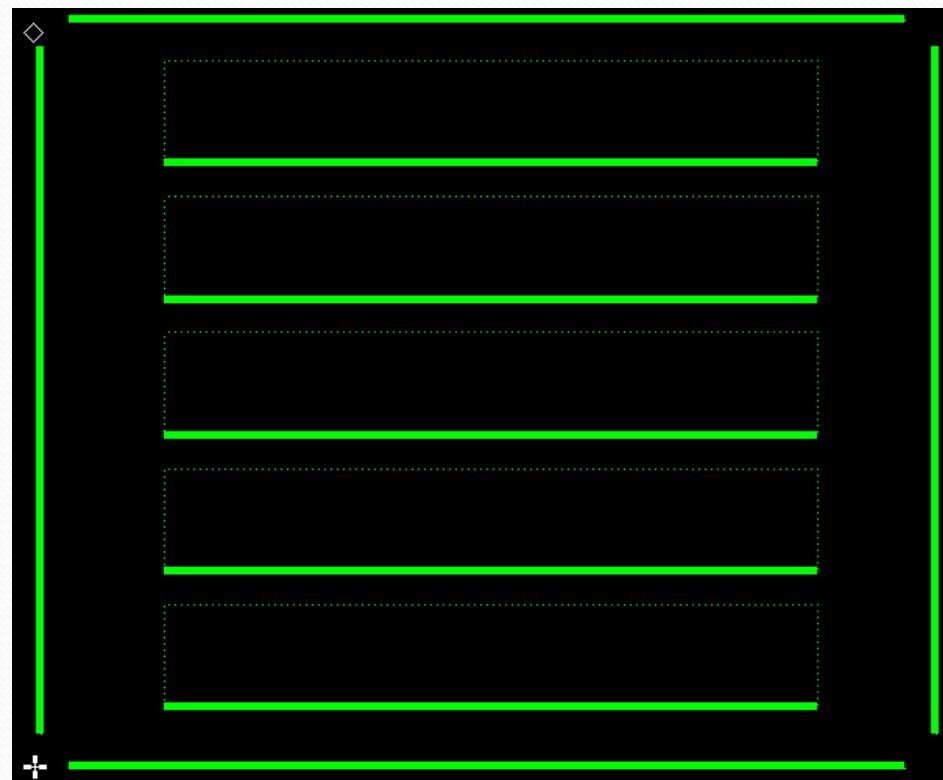


# Place & Route Flow



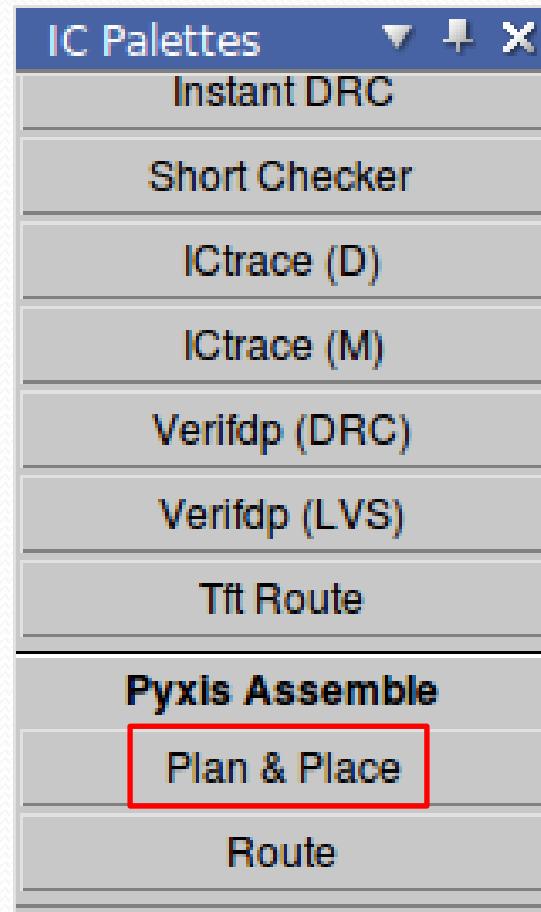
# Step3: Floor Planning

- Set estimate/required chip area
- Creates the chip Rows, Boundaries & Pads



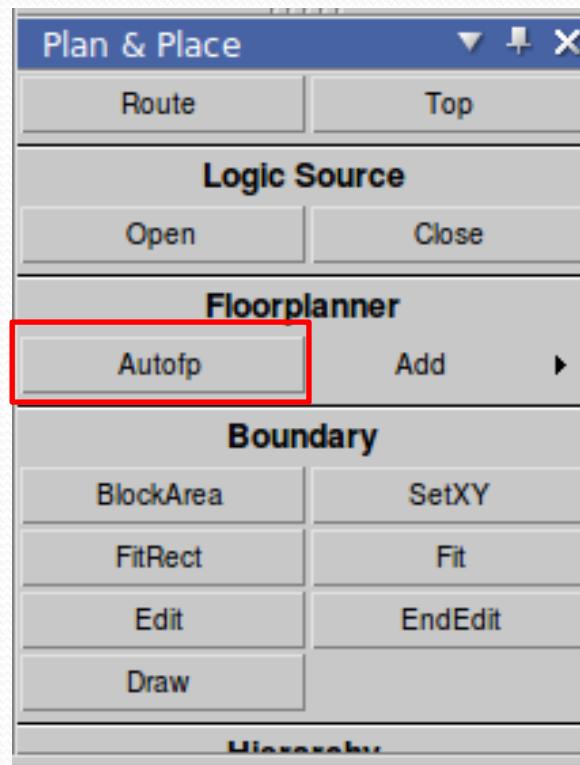
# Step3: Floor Planning

- From “IC Palettes” Scroll & Select “Plan & Place”



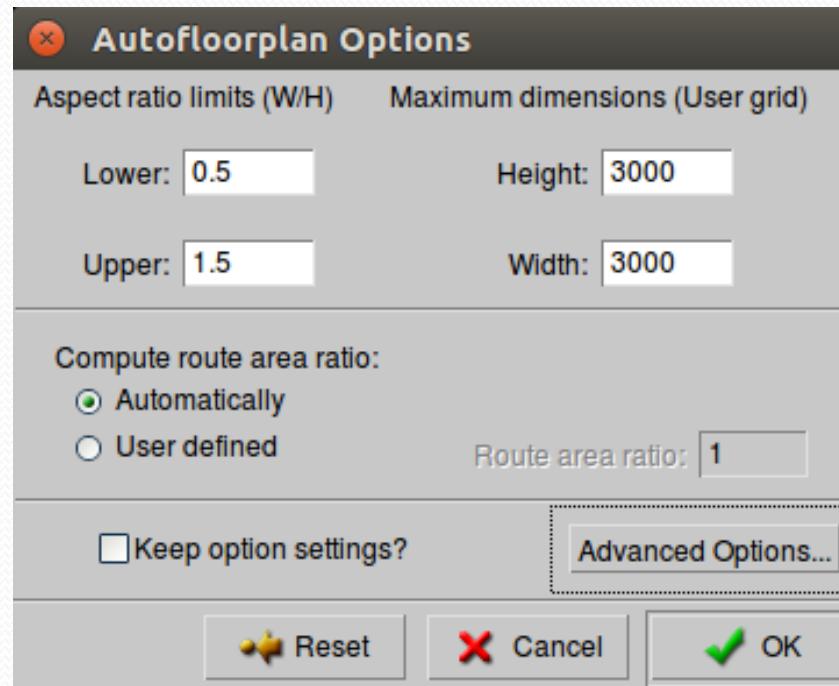
# Step3: Floor Planning

- From “Floorplanner” Select “Auto fp”



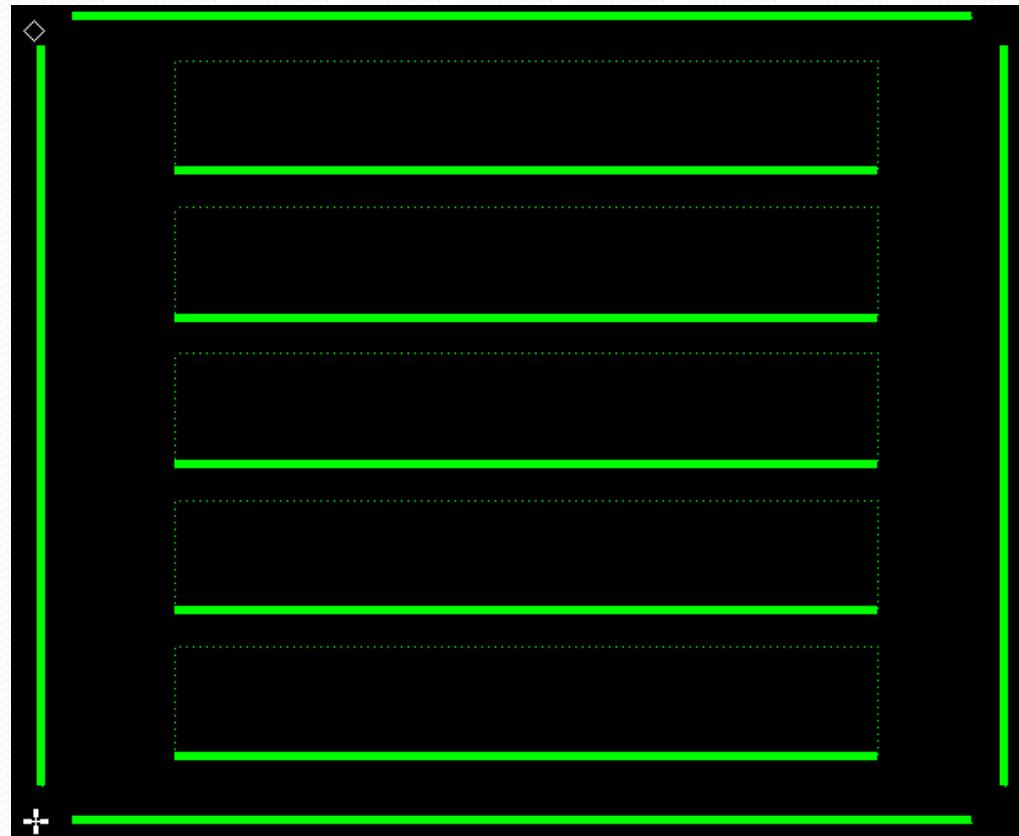
# Step3: Floor Planning

- You will have to set the Maximum Area of your chip & its aspect ratio limits



# Step3: Floor Planning

- IC Station will automatically set the chip boundaries & cell rows



# Step3: Floor Planning

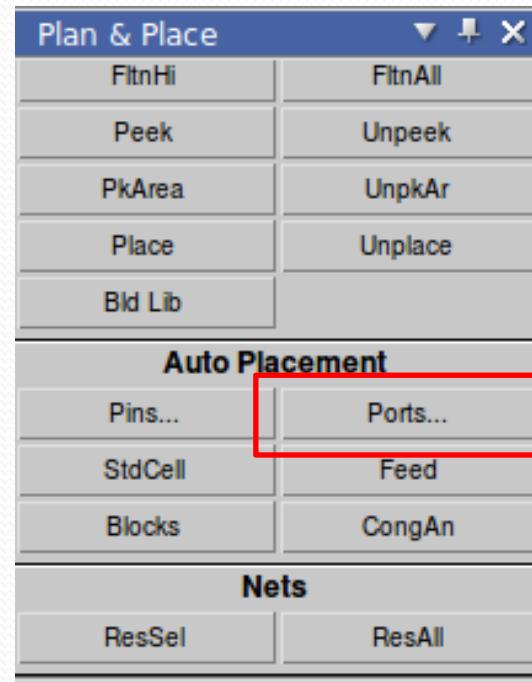
- The Floor Planning report will be at the working directory  
“FLOORPLAN\_‘cell\_name’.rpt”
- The report has:
  - Total Area
  - Row Details
  - Spacing
  - Gap Area
  - ...

# Place & Route Flow



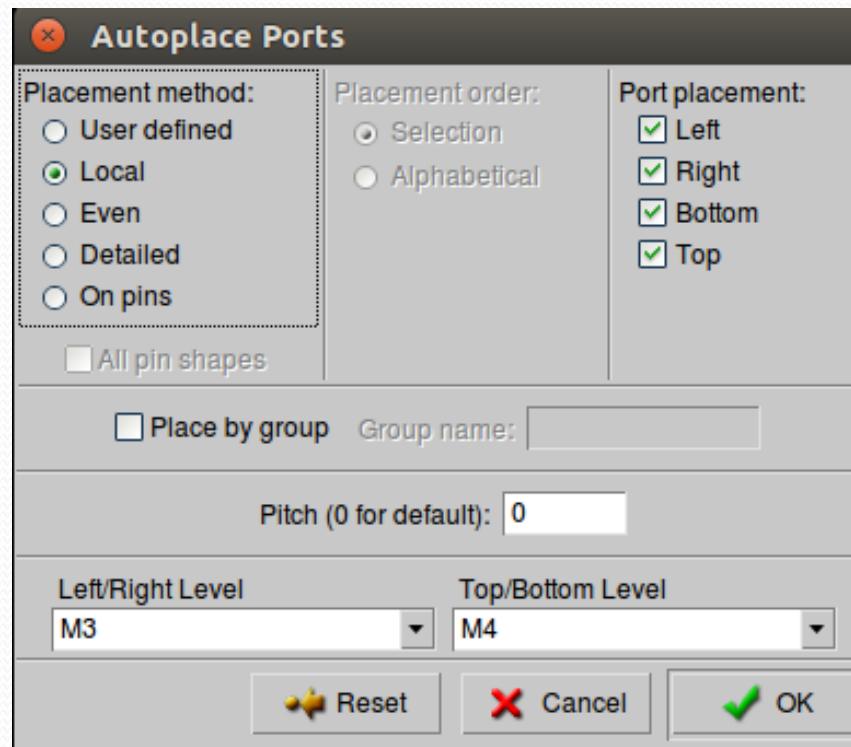
# Step4: Add Ports

- To place the design ports, select “Ports” from “Auto Placement”



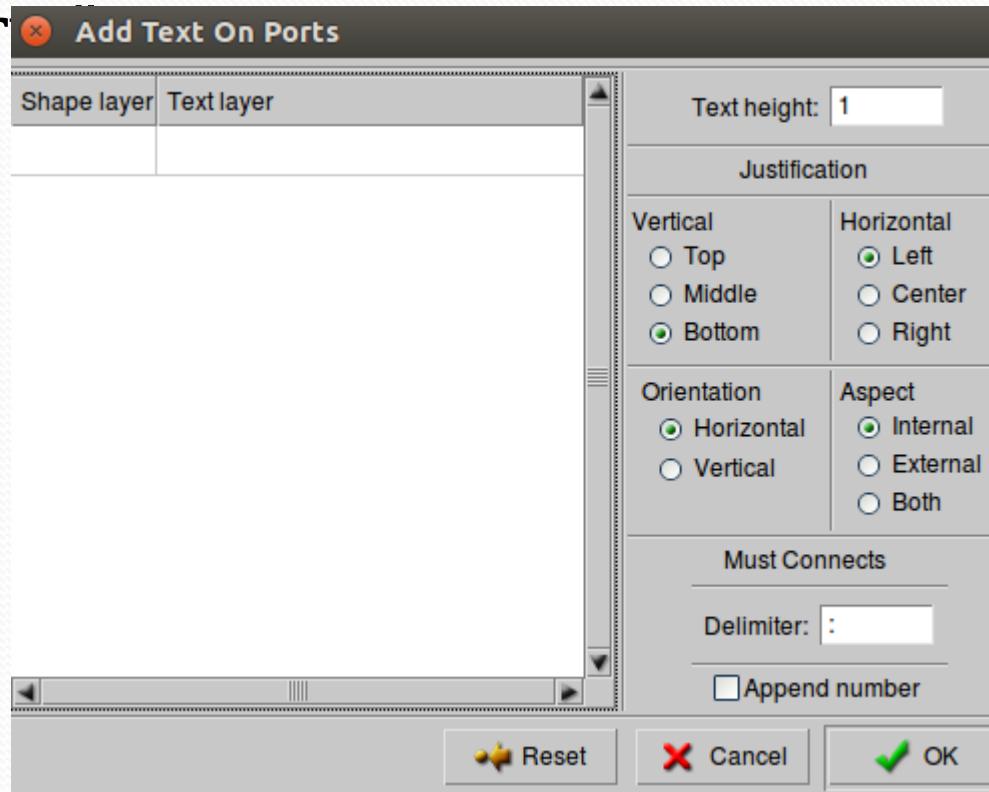
# Step4: Add Ports

- You could set the sides of the ports & the Metal Layers of each side



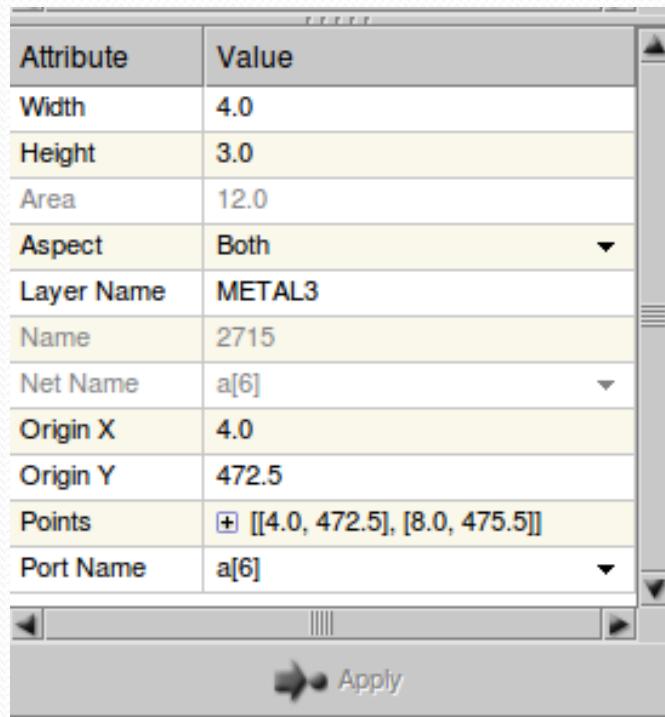
# Step4: Add Ports

- Add Labels to Ports
  - Click “Add” in the Top Bar Then Click on “Text on Port”



# Step4: Add Ports

- Zoom to the boundary to see the ports & its properties



# Ports & Pads

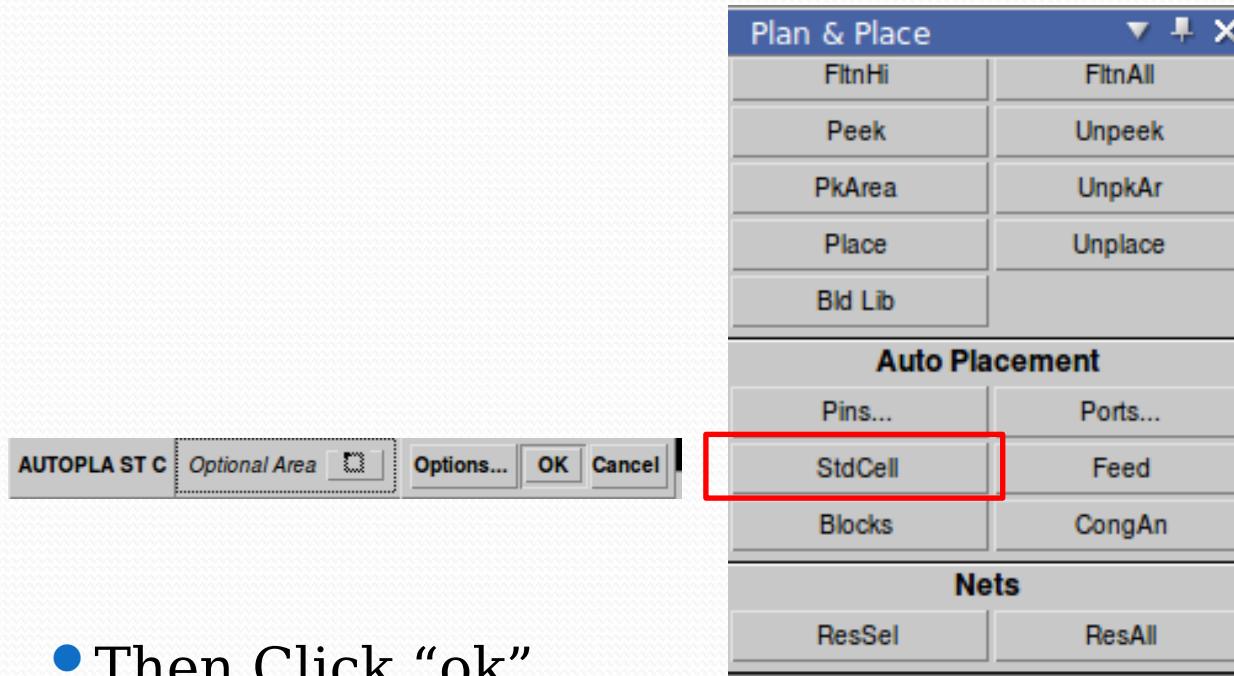
- To add the pads in the layout, you should add the pads in the Verilog Netlist file first
- Then add it to the design schematic
- We will create a schematic & add the pads in the next lab

# Place & Route Flow



# Step5: Place Std Cells

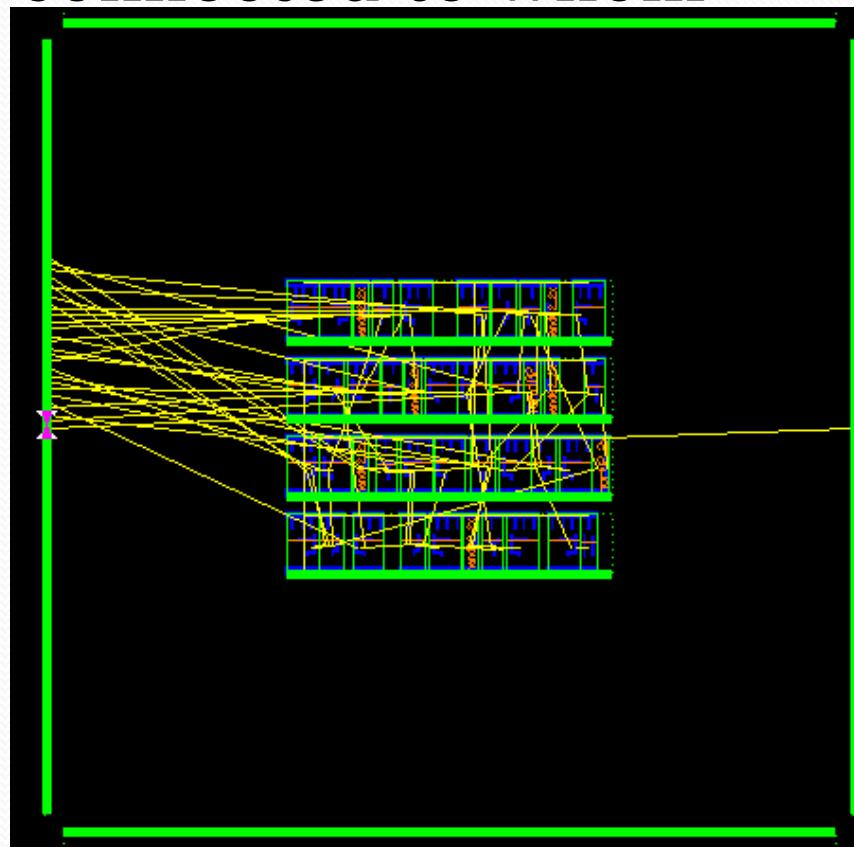
- To place the technology cells “the mapped design”
  - Select “StdCell” from “Auto Placement”



- Then Click “ok”

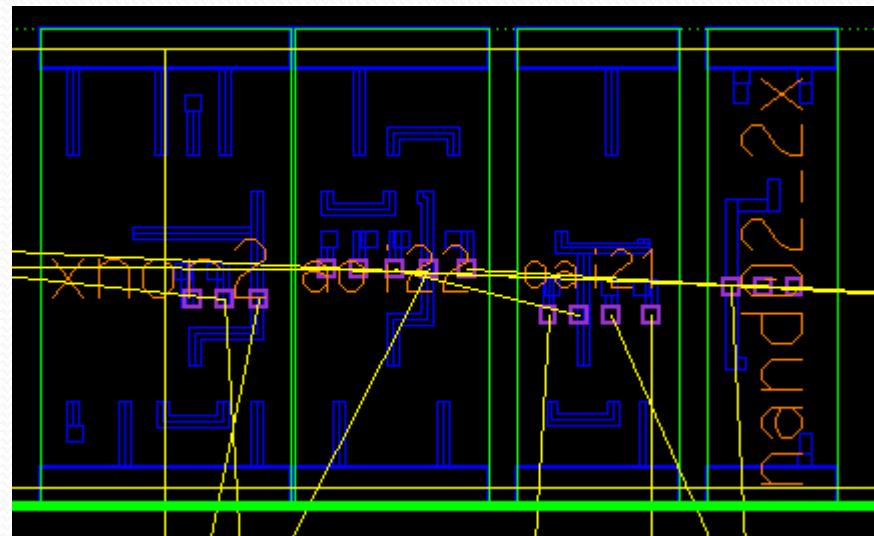
# Step5: Place Std Cells

- You could see the cells are placed & each pin should be connected to whom



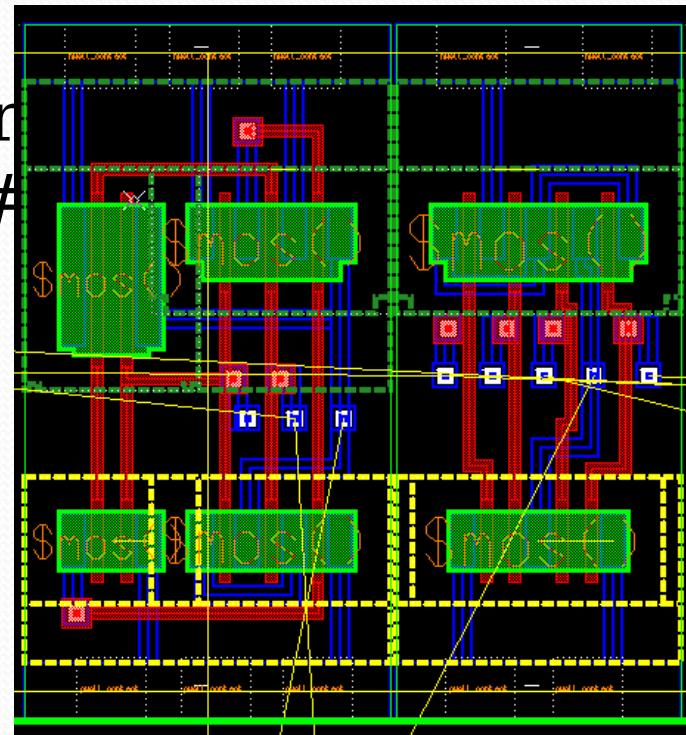
# Step5: Place Std Cells

- You could see the cells in each row by zooming in
- Note that you can see the cell name and the pins but you can't see the layout



# Step5: Place Std Cells

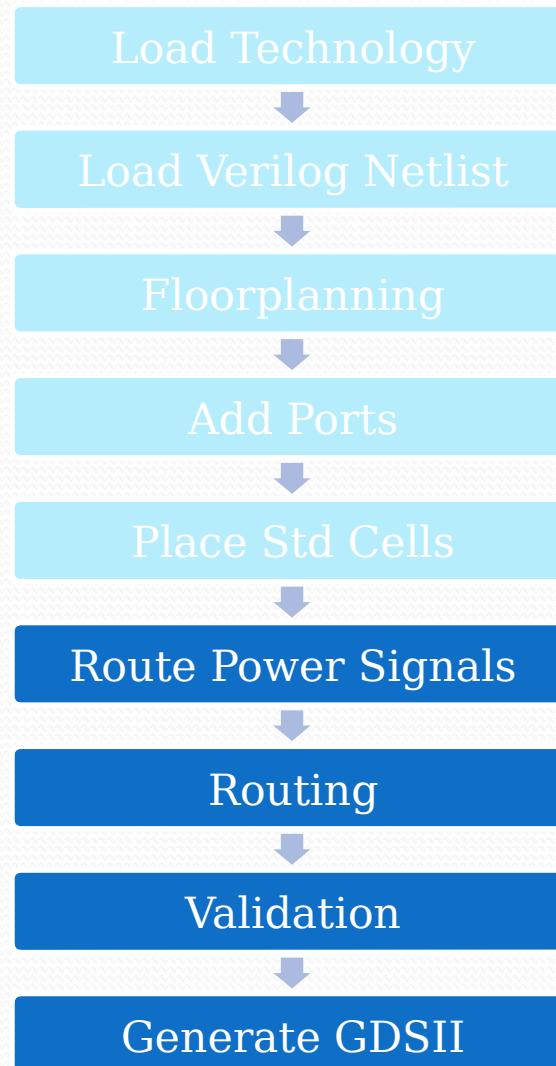
- You could the cells layout by peeking to a specific area
- Click on “View” & hover on “Peek” then click on Peek
- Select the area you want to peek into, then specify the #



# Step5: Place Std Cells

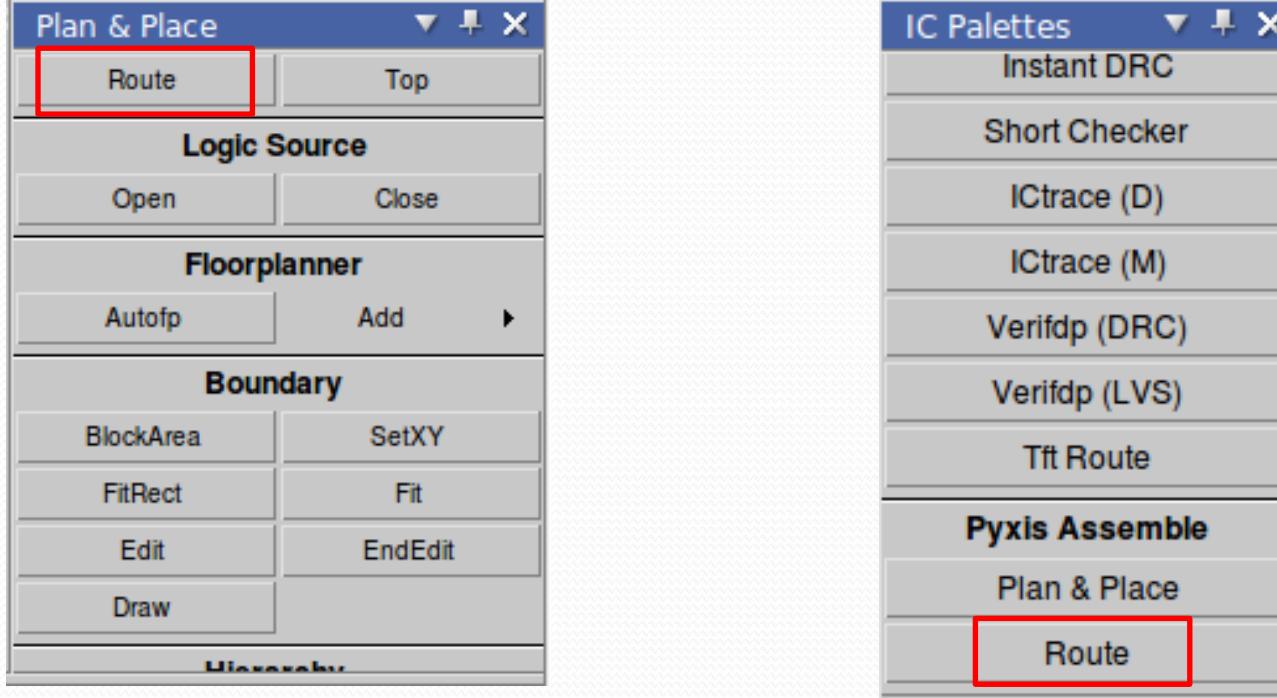
- The Placement report will be at the working directory “PLACER\_‘cell\_name’.rpt”
- The report has:
  - Number of Iterations
  - Estimate Wire Length

# Place & Route Flow



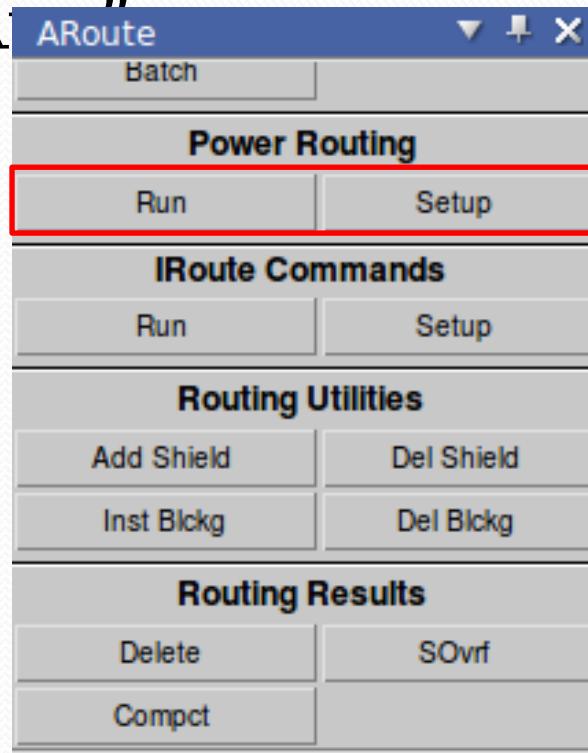
# Step6: Route Power Signals

- Go to the routing panel
  - Select Route from “Plan & Place”
  - Or select Route from the top panel



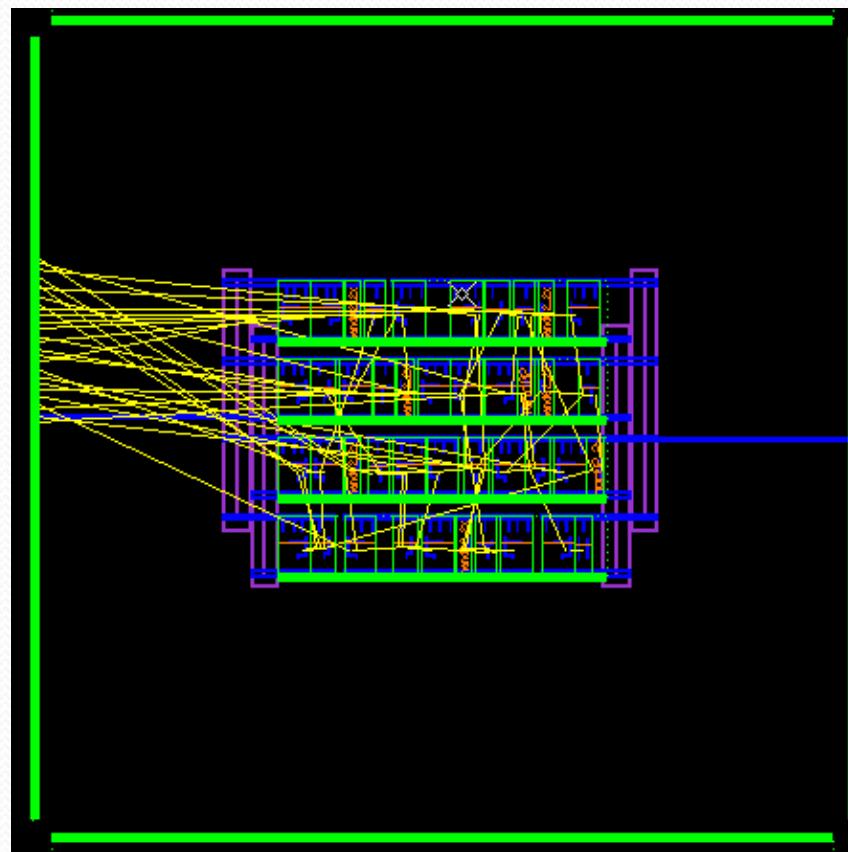
# Step6: Route Power Signals

- Select “Setup” from “Power Routing” to set details
- Then Click “Run”



# Step6: Route Power Signals

- IC Station will add Vertical & Horizontal wires for VDD & GND



# Clock Tree Synthesis

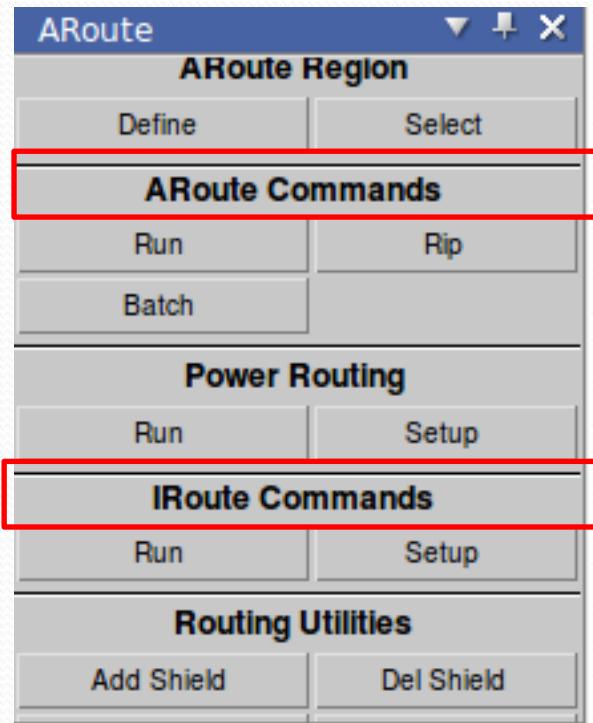
- Some Tools perform Clock Tree Synthesis (CTS) before the wire routing
  - Route the Clock signals
- Clock Tree are built to meet the design constraints while balancing the loads & min clock skew
- Clock Tree can be built using H-Tree or Clock Mesh

# Place & Route Flow



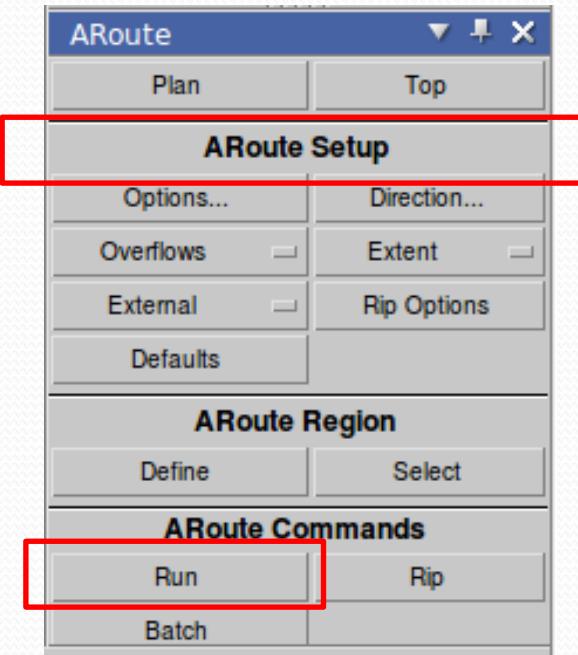
# Step7: Routing

- You could Route a signal Manually (IRoute)
- Or you could Route the signals automatically (ARoute)

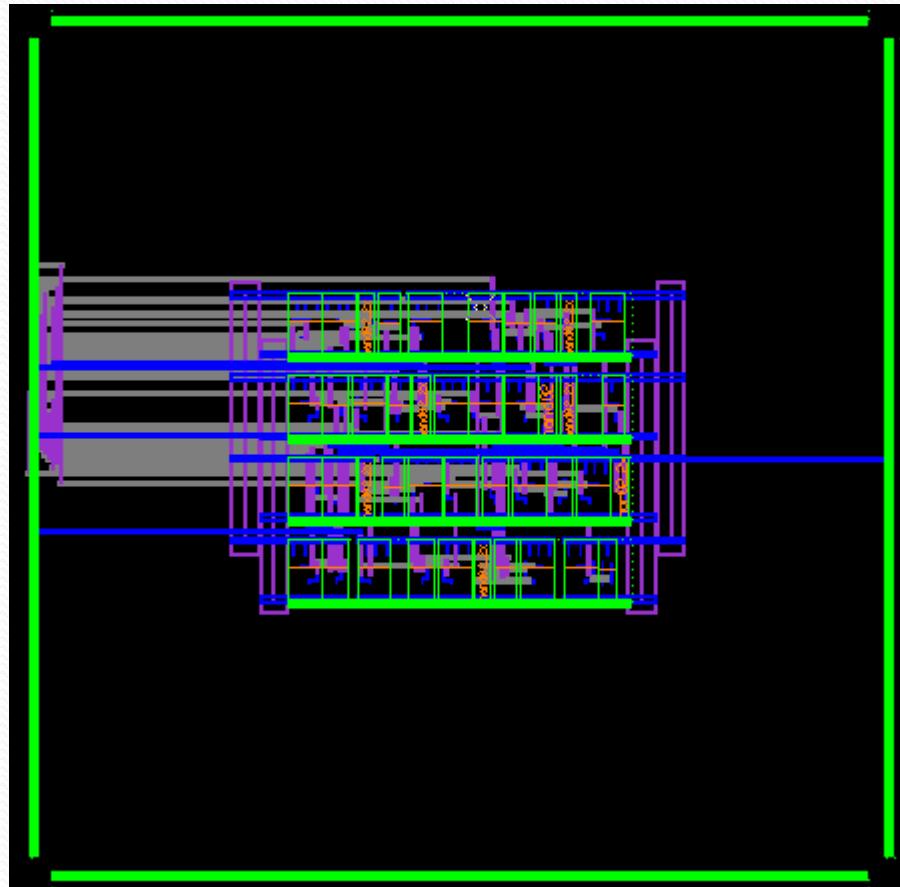


# Step7: Routing

- Select “Options” & “Direction” from “ARoute Setup” to set routing details
- Then Click “Run” in “ARoute Commands”



# Step7: Routing



# Place & Route Flow



# Step8: Validation

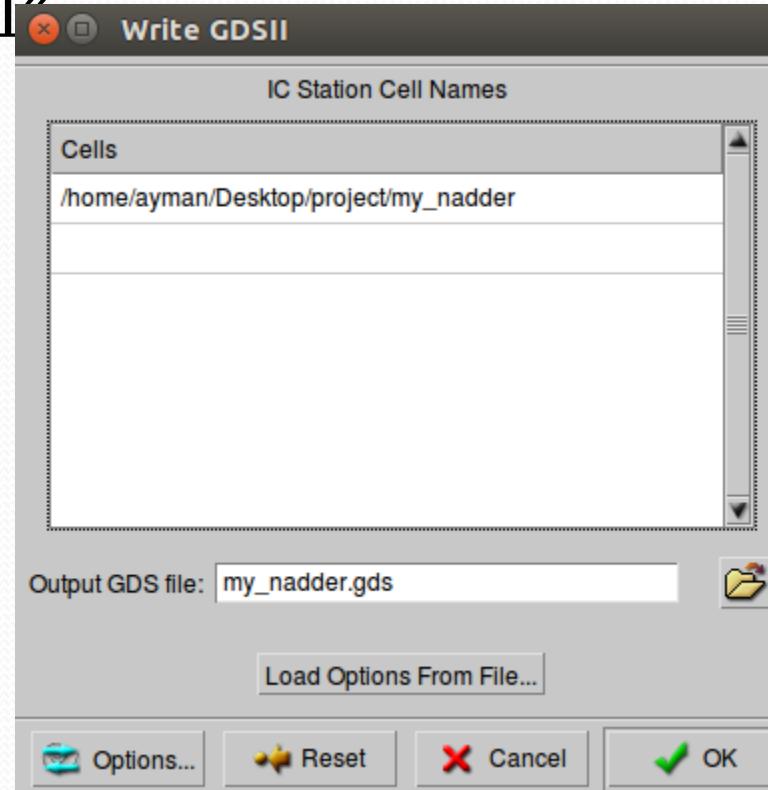
- We will talk about Validation next lab

# Place & Route Flow



# Step9: Generate GDSII

- To save the layout in GDSII format
  - Click “file” Then hover on “Export” and click on “GDSII”



# Note

- We didn't generate Timing or Power Reports
  - Pyxis don't generate these reports
  - So we use 3<sup>rd</sup> party tools to generate these reports
- Other Vendor Tools (Synopsys & Cadence) generate these reports
  - In these tools we check for timing violations after each of the following steps:
    - Placement
    - Clock Tree Synthesis
    - Routing