ECSE 2920: Design Methodology

Deliverable #11

Group #11

04/02/2025

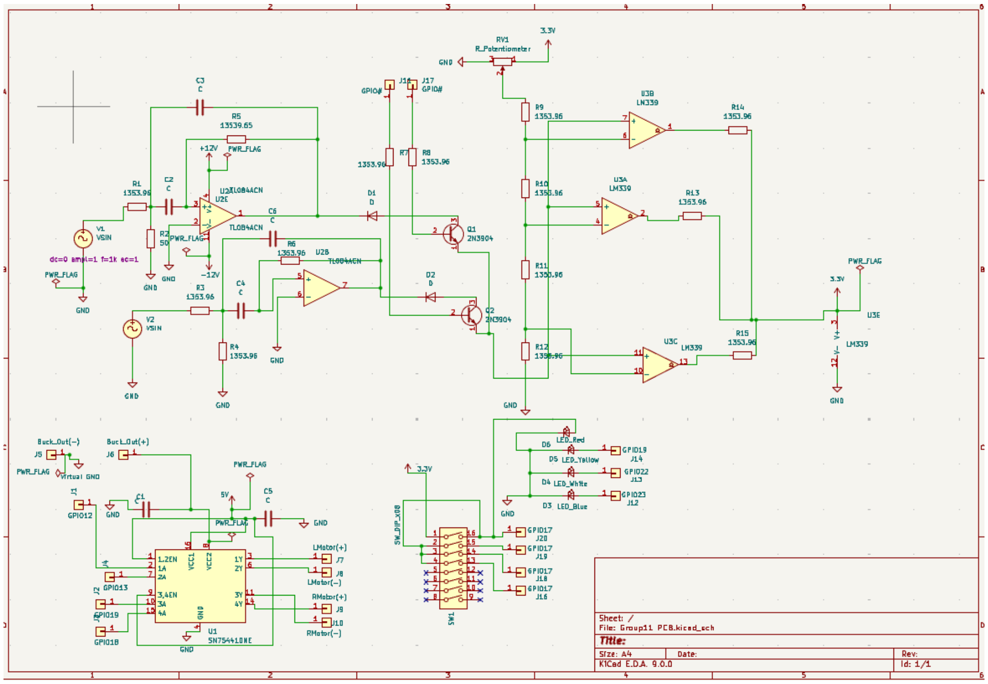
Part 1: PCB Schematic and Board Layout

Requirements:

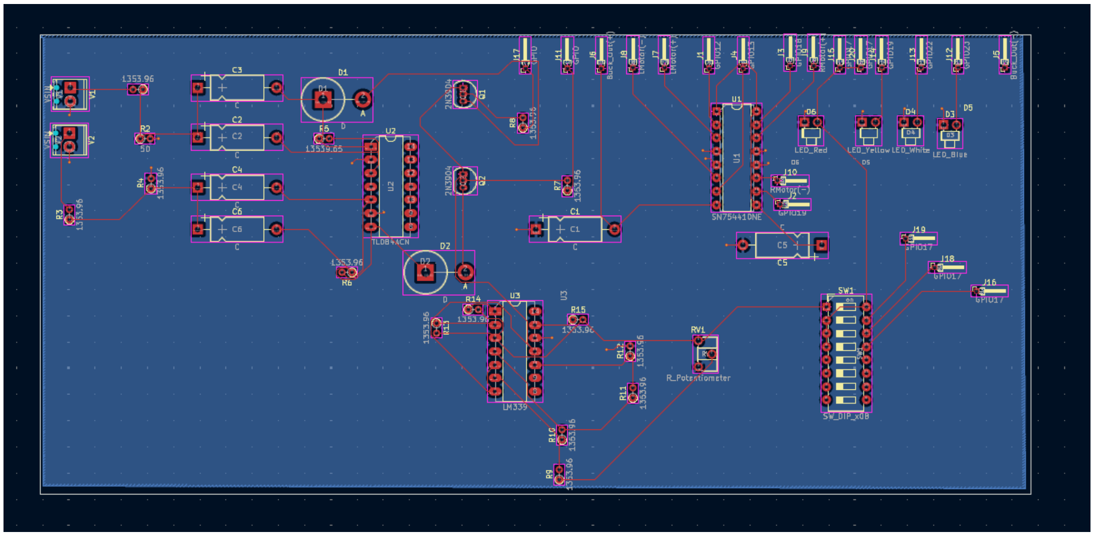
- **Create a complete electrical schematic of the project's circuitry**
- **Translate your schematic into a PCB board layout**
- **Include all custom-designed parts of the circuitry (apart from push/pull)**
- **Ensure all components used are purchasable and compatible**
- **Pass all Design Rule Checks (DRC) within the software**
- **Include pictures of electrical schematic and PCB board layout**
- **Write up a paragraph justifying the overall layout, trace width sizing and routing choices, input/output pots and expected signal paths.**

Our PCB features a dual-filter setup to isolate both C6 and C8 frequencies, each connected to a dedicated microphone. These signals are routed through active bandpass filters implemented using a quad op-amp package and then passed through half-wave rectifiers to a 2-bit Flash ADC. The ADC uses LM339 open-collector comparators, which account for the pull-up behavior required by the RP4 GPIO. Each ADC output is routed to header pins for RP4 connectivity. Additional features include an onboard DIP switch array and an H-Bridge that interfaces with the GPIO system for logic control. The board assumes regulated +/- 12V inputs with clearly labeled terminals for easy connection.
The layout prioritizes short and direct traces from the filters to the ADC to reduce noise susceptibility. We carefully moved components that connect to each other on the 2D PCB design until all traces did not overlap which would allow easy pathing for the traces on the PCB. Filter components are grouped logically around their respective op-amps for clean routing. All ground lines route to a common ground plane which connects to a copper ground reference to reduce wiring and connect the grounds. Though trace width was determined using KiCAD's default settings, all lines passed the DRC checks. There is not much current going through the traces on the PCB because their current is not very high. I/O ports are placed on the board edge to simplify wiring to external components (e.g., microphones, motors, and RP4 GPIO headers).

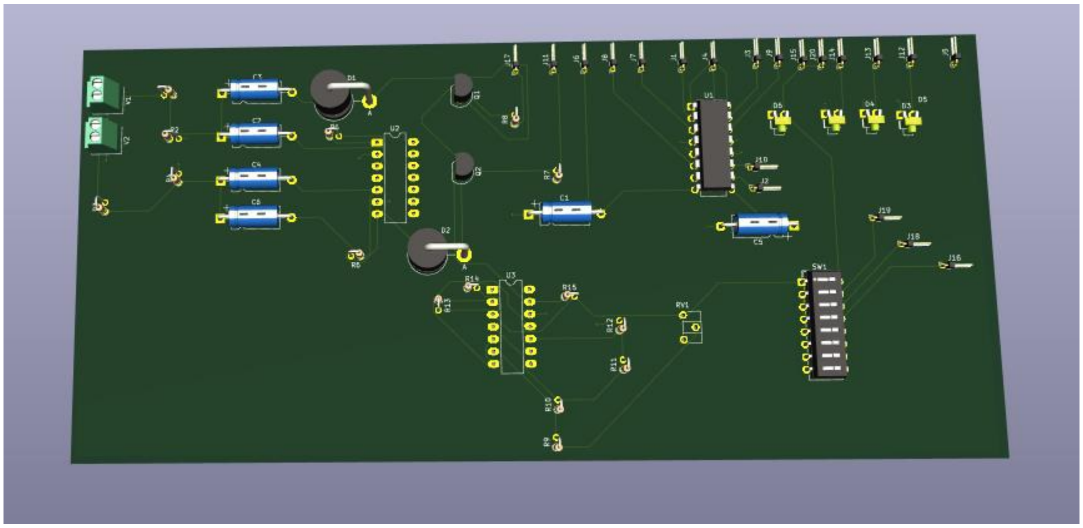
Picture(s)



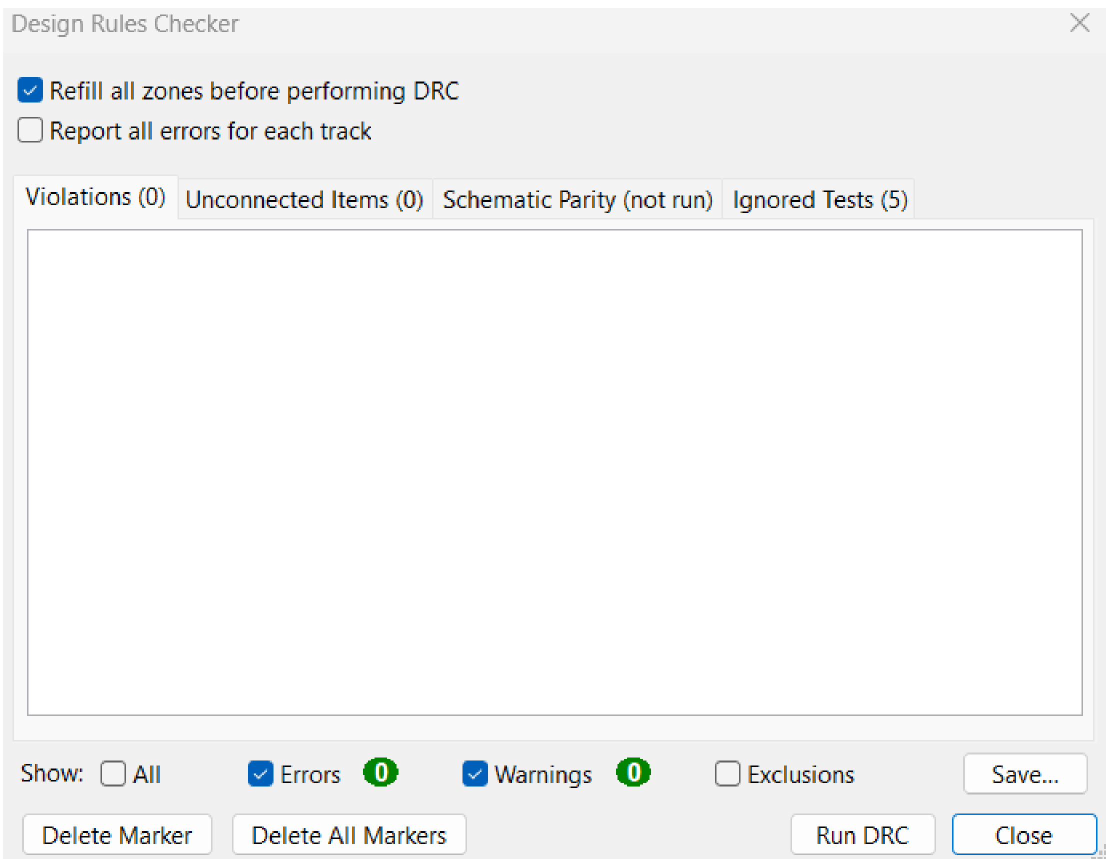
(**Figure 1:** Electrical Schematic for PCB.)



(**Figure 2:** PCB Board Layout.)



(**Figure 3:** 3D Render of Board.)



(**Figure 4:** Screenshot showing the Board passed the DRC.)

Key Design Decision(s)

- What did your team clarify about the design?
    - Proper signal routing from dual filter inputs to Flash ADC for C6/C8 detection
- What were the competing choices in the design?

    - The designs included on the PCB were the final designs for our project, so no competing choices.
- Ultimately what did your team choose and why?
    - Used 2 filters with isolated op-amp channels to ensure clean, parallel processing of both mic signals; simplified logic via seperate transistor paths.

TEST… Test… test

- What aspects of the design need to be tested?
    - Software?
        - DRC checker (Passed)
    - Hardware?
        - We are not fabricating our PCB, but it is prepared for fabrication.
- Who is responsible for testing?
    - Tests ran?
        - Electrical rule check (ERC), design rule check (DRC), and trace visual inspection
    - Conclusions from testing?
        - The board is manufacturable, all custom logic and analog subsystems have been included.

summary/part conclusion (make sure you address all parts of the requirements)

- The PCB schematic and layout meet all project requirements. Traces are not very large because of lower current. Each subsystem was modeled to reflect the existing breadboarded circuit design and then optimized for real-world fabrication. All components used are standard through-hole or DIP, ensuring simple soldering and debugging. This PCB will serve as the base for signal analysis and control logic in our audio-seeking vehicle.

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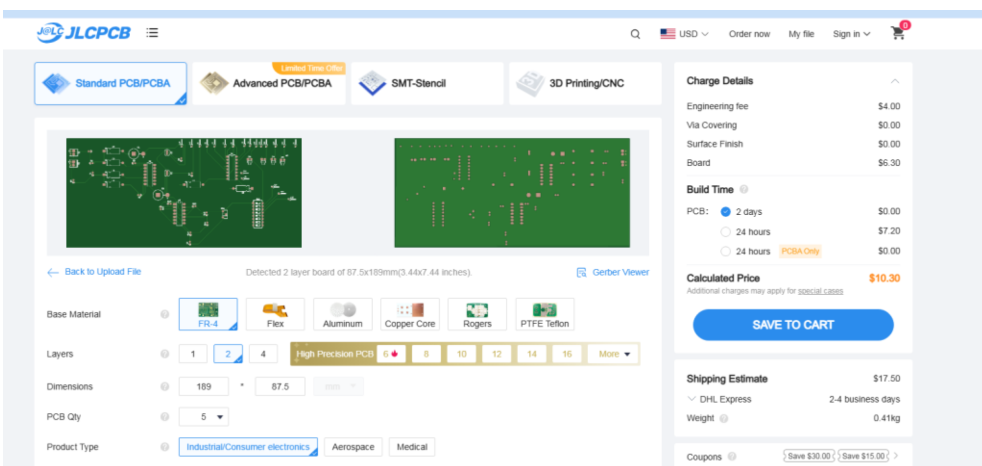
<u>Part 2: BOM, Fabrication Quote, and Manufacturer Readiness</u>

Requirements:

- **Create a Bill of Materials (BOM) that includes component names, part numbers, quantity, unit price, and total price (with hyperlinks to the sources)**
- **Export PCB design into Gerber files**
- **Upload files to a PCB manufacturer and complete the manufacturer's DRC verification, select components for fabrication, and obtain a cost quote and include a screenshot**

Our BOM includes all components needed to populate the PCB. The major parts include a quad-operational amplifier setup, LM339 comparators for Flash ADC logic, various resistors and capacitors for bandpass filters and signal conditioning, DIP switches, transistors for signal routing, and headers for GPIO and motor interfacing. All parts were chosen from standard suppliers and matched with part numbers to ensure availability. We used JLCPCB for our fabrication quote and confirmed that our board passed DRC verification.
The Gerber files were exported from KiCAD and uploaded to JLCPCB, where the fabrication quote was $10.30 for 5 boards (not including shipping). This confirms that the board is ready for manufacturing and all routing and component footprints are compatible with standard processes.

Picture(s)



(**Figure 1:** JLCPCB Quote Screenshot.)

<u>Part</u>	<u>Number</u>	<u>Quantity</u>	<u>Cost per Unit</u>	<u>Total Cost</u>
Capacitor	MAL202119101E3	6	$3.40	$20.40
Diode	5KP7.5A	2	$2.45	$4.90
Red_LED	WP424IDT	1	$0.31	$0.31
Blue_LED	151051BS04000	1	$0.24	$0.24
White_LED	C512A-WNS-CZ0B0152CT-ND	1	$0.26	$0.26

Yellow_LED	754-1212-ND	1	$0.25	$0.25
Pins	FIT0100	2X20	$4.68	$4.68
Dip Switch	124204	1	$0.60	$0.60
Transistor	2N3904	2	$0.13	$0.26
Potentiometer	18STS25K	1	$0.90	$0.90
LM339	LM339N/NOPB	1	$1.29	$1.29
TL084	TL084ACN	1	$1.23	$1.23
Resistor	MFR-25FRF52-13K	15	$0.02	$0.32
JLCPCB	Custom PCB	1	$10.90	$10.90
Terminal Block	1725656	2	$0.95	$1.89 **TOTAL: $47.83**

(**Figure 2:** Bill Of Materials.)

TEST… Test… test

- What aspects of the design need to be tested?
  - Software?
    - JLCPCB's online DRC and quote generator
  - Hardware?
    - N/A
- Who is responsible for testing?
  - Tests ran?
    - Visual cross-check of footprints, online DRC pass at JLCPCB
  - Conclusions from testing?
    - Board is fully manufacturable; all parts sourced and priced; ready for ordering if needed

summary/part conclusion (make sure you address all parts of the requirements)

- We successfully generated a complete BOM and confirmed our design is ready for fabrication. All parts are matched with sources, and our board passed both KiCAD and JLCPCB DRC checls. This ensures that our custom analog and digital systems will be reliably manufactured and support our audio tracking car in checkpoint A-. We have decided to stick with what we have despite the PCB being helpful because our design is working and keeping our design simple.

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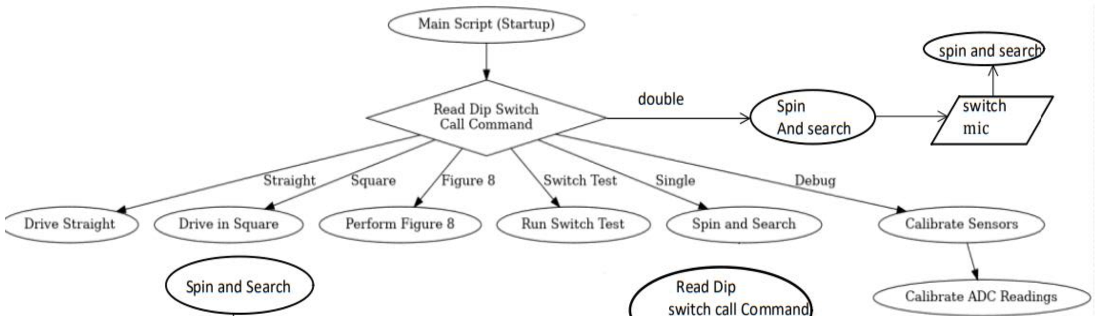
Part 3: Code Architecture and Flow

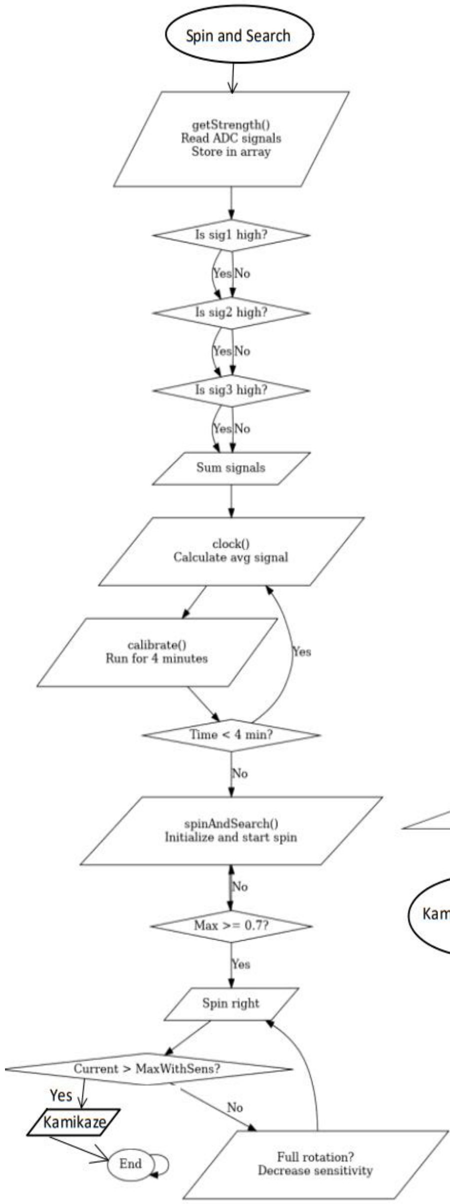
Requirements:

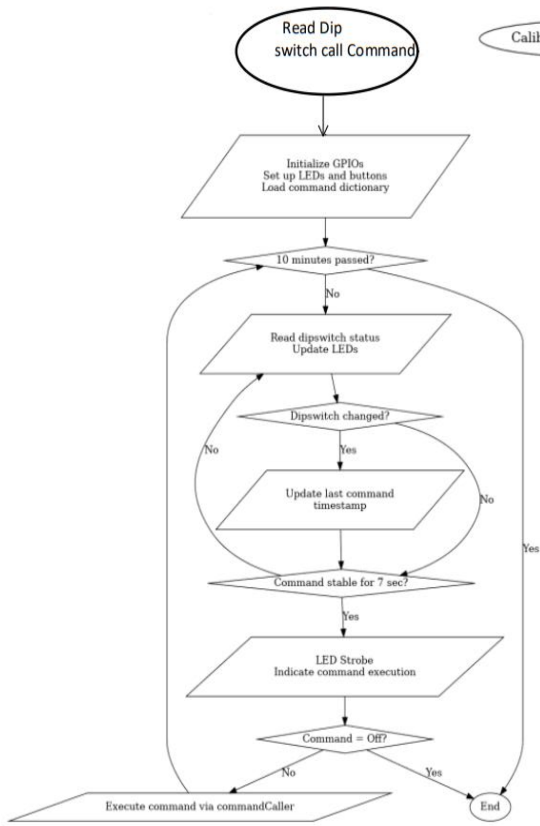
- **Provide a black diagram and/or flow chart of the project's software:**
  - **Should reflect current codebase status**
  - **Include top-level modules and their relationships**
  - **Use a hierarchical structure, not flat**
- **Optionally, add state machine diagrams for complex modules**
- **Focus on logic, data flow, and timing – this is not a code dump**

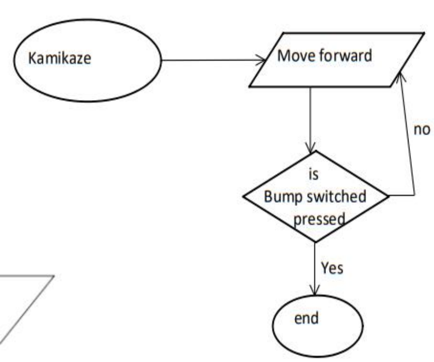
The group has provided a flow chart that organizes all the code for the project in a hierarchical structure. It shows the start of the main program which then immediately goes into a portion of the code that reads the dip switch, and calls the command that corresponds to the dip switch input. The flow chart for reading the dip switches and calling the command is shown below. Based off the input for the switch, the flow chart then goes to the action that corresponds to this input. All these actions are very simple and don't require a further breakdown of the code except for single and double frequency detection. Both call a process called spin and search, which the flow chart for this process is shown below and spin and search calls a process called kamikaze, which the flow chart for this process is also shown.

Picture(s)


Main Script (Startup)
Read Dip Switch
Call Command
double
Spin
And search
switch
mic
spin and search
Straight
Square
Figure 8
Switch Test
Single
Debug
Drive Straight
Drive in Square
Perform Figure 8
Run Switch Test
Spin and Search
Calibrate Sensors
Calibrate ADC Readings


Spin and Search
getStrength()
Read ADC signals
Store in array
Is sig1 high?
Yes
No
Is sig2 high?
Yes
No
Is sig3 high?
Yes
No
Sum signals
clock()
Calculate avg signal
calibrate()
Run for 4 minutes
Yes
Time < 4 min?
No
spinAndSearch()
Initialize and start spin
No
Max >= 0.7?
Yes
Spin right
Current > MaxWithSens?
Yes
Kamikaze
End
No
Full rotation?
Decrease sensitivity


Read Dip
switch call Command
Initialize GPIOs
Set up LEDs and buttons
Load command dictionary
10 minutes passed?
No
Read dipswitch status
Update LEDs
Dipswitch changed?
No
Yes
Update last command
timestamp
No
Yes
Command stable for 7 sec?
Yes
LED Strobe
Indicate command execution
Command = Off?
No
Yes
Execute command via commandCaller
End


Kamikaze
Move forward
no
is
Bump switched
pressed
Yes
end

(**Figure 1:** Code Flow Diagram.)

summary/part conclusion (make sure you address all parts of the requirements)

In conclusion the group provided a block diagram for project code that reflects the current state of the code for our audio car. We included top – level modules and how they relate, for example the spin and search module relating to the main program calling single and double frequency detection. We included a hierarchal structure we the main program being at the top and the different sub programs being shown below. The group put an emphasis on the timing, logic, and flow of data throughout the program.

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Conclusion and Participation (REQUIRED)

1. **Include a selfie/photo from your group meeting/zoom call.**

2. **When did you meet? we met 4/2 and 3/31**
3. **Who was present? Everyone – Cade showed up later but he was there**
4. **Who was not present? no one**
5. **What were the main ideas discussed or major decisions (1-2 sentences/bullet points)**
   We discussed what to do next for checkpoint A-. We are planning to test soon and hopefully be ready by the end of today or by Monday.