ECSE 2920: Design Methodology

Deliverable #7

Group #11

02/19/2025

Part 1: Power Supply Design

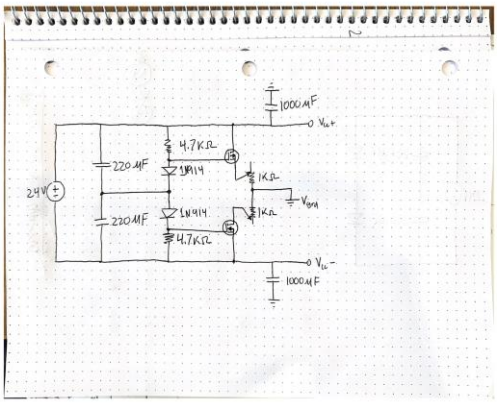
Requirements:

- Update the power supply simulation using Multisim
- Demonstrate a working +/- 12V DC supply in a standalone environment
- Validate performance with and without an appropriate load
- Provide a schematic and document any design improvements
- Include a video showing the power supply build and measured outputs

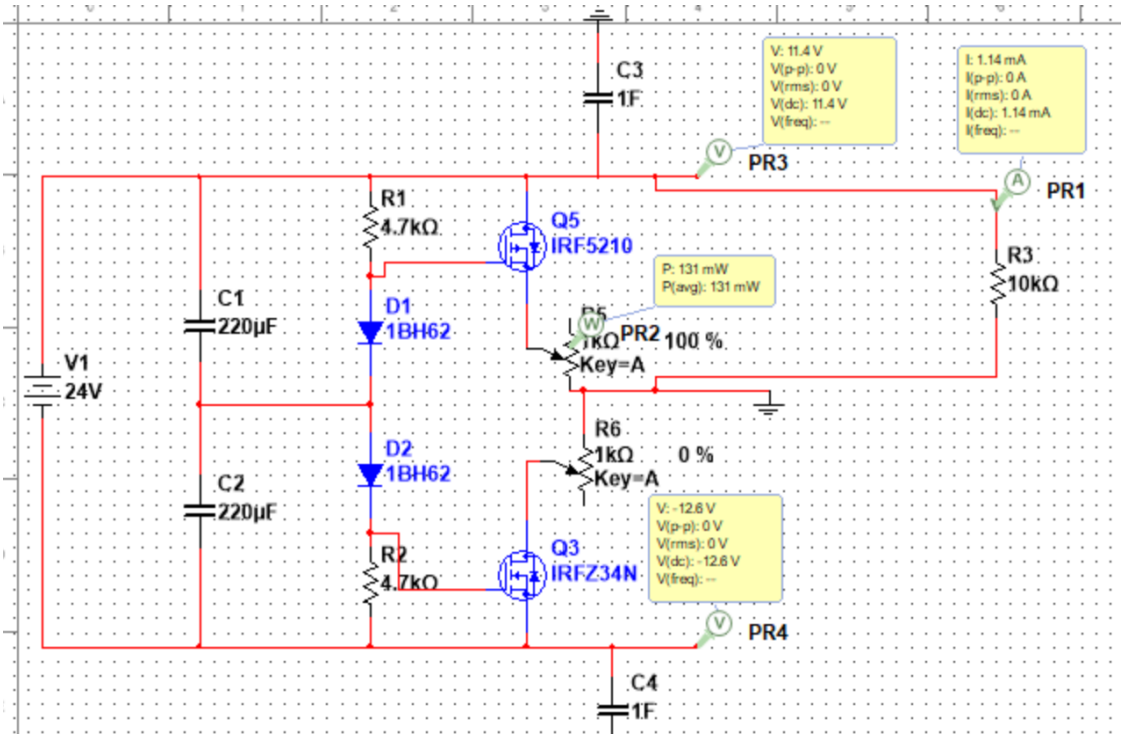
Our power supply design utilizes MOSFETs to efficiently generate a stable +/-12V from a 24V DC input. This setup allows us to effectively power key circuit components such as operational amplifiers and other analog devices. To enhance testing flexibility, we have incorporated potentiometers into the design, enabling us to dynamically adjust resistance values. This facilitates easier optimization for different load conditions and helps us explore maximum power transfer by experimenting with high-wattage potentiometers. The inclusion of capacitors ensures smooth voltage regulation and minimizes ripple, making the supply more reliable under fluctuating load conditions.

A key consideration in our design was handling the high current draw from the 24V 5A power source. This required careful selection of resistors to limit excessive current through the MOSFETs. The decision to avoid using an op-amp in the push-pull configuration was based on potential stability issues and complexity in implementation. Using an op-amp in this design could introduce additional feedback loops that may lead to unwanted oscillations, making it difficult to maintain stable voltage outputs. Instead, we opted for a simpler yet effective MOSFET-driven approach.

Picture(s)



(**Figure 1:** Paper design of our push/pull)



(**Figure 2:** Multisim simulation of our push/pull)

Video of Physical Simulation Uploaded on ELC

Key Design Decision(s)

- What did your team clarify about the design?

    - Ensuring the circuit effectively manages high current draw from the 24V 5A supply while maintaining stable voltage output.
- What were the competing choices in the design?
    - Push-Pull with Op-Amp: initially considered but rejected due to potential instability and difficulty in tuning feedback loops
    - MOSFET-Based Push-Pull: Chosen for simplicity, efficiency, and ease of implementation
- Ultimately what did your team choose and why?
    - Implementing a MOSFET-based push-pull with adjustable potentiometers for easy tuning and current management.

TEST… Test… test

- What aspects of the design need to be tested?
    - Software?
        - Multisim simulation to analyzer performance under different loads
    - Hardware?
        - Tested using a DC supply with current limiting to observe initial power on behavior
        - Physical testing with a real load to validate expected performance
- Who is responsible for testing?
    - Tests ran?
        - We tested our push/pull both on multisim and physically
    - Conclusions from testing?
        - Our theoretical design in Multisim produced 11.4/-12.6 voltage
        - While our physical design produced around a 11.5/-12.5 voltage

summary/part conclusion (make sure you address all parts of the requirements)

Our power supply design successfully provides the necessary +/-12V for the system, with minor deviations in output voltage that are within acceptable limits. The addition of potentiometers has significantly improved our ability to fine-tune the circuit for different conditions, making the testing and optimization process more efficient. The challenges of managing high current draw were addressed by careful resistor selection and iterative testing, leading to a stable and reliable design.

Part 2: Preliminary Filter Design

Requirements:

- Create a paper design for the filter supporting C8 frequency
- Implement a computer-simulated design with a Bode plot
- Document filter design decisions and justifications

For our project, we require an audio car that can detect a specific frequency (C8) and respond accordingly. To achieve this, we designed an active bandpass filter that isolates the C8 frequency, ensuring that the system accurately picks up and processes the target frequency while rejecting unwanted signals. The chosen filter allows us to fine-tune the frequency response and improve performance by eliminating background noise.

Our design follows the standard bandpass filter equation:

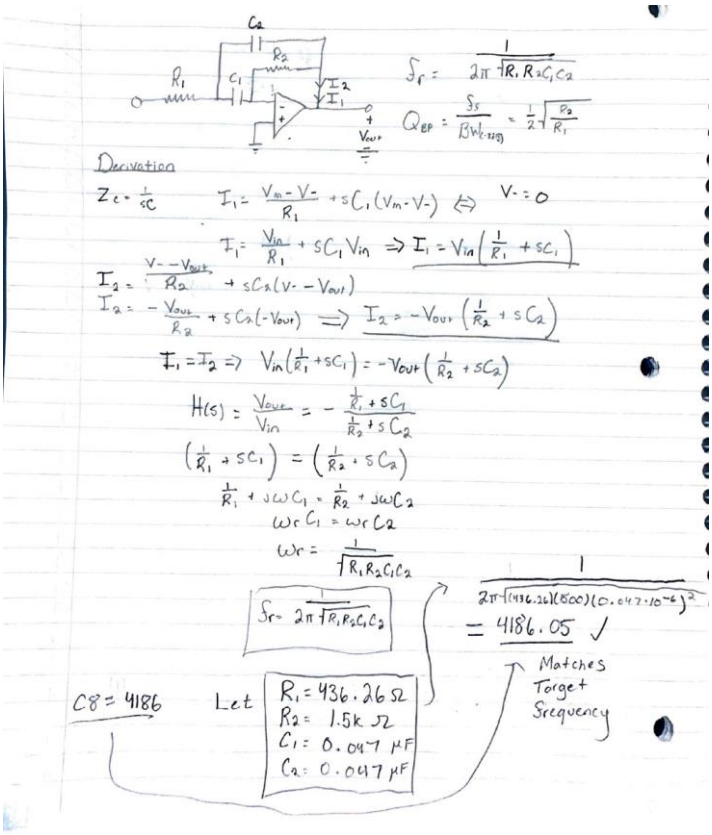
$$fr = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Using this equation, we selected the following component values to achieve a center frequency of 4186 Hz (C8)

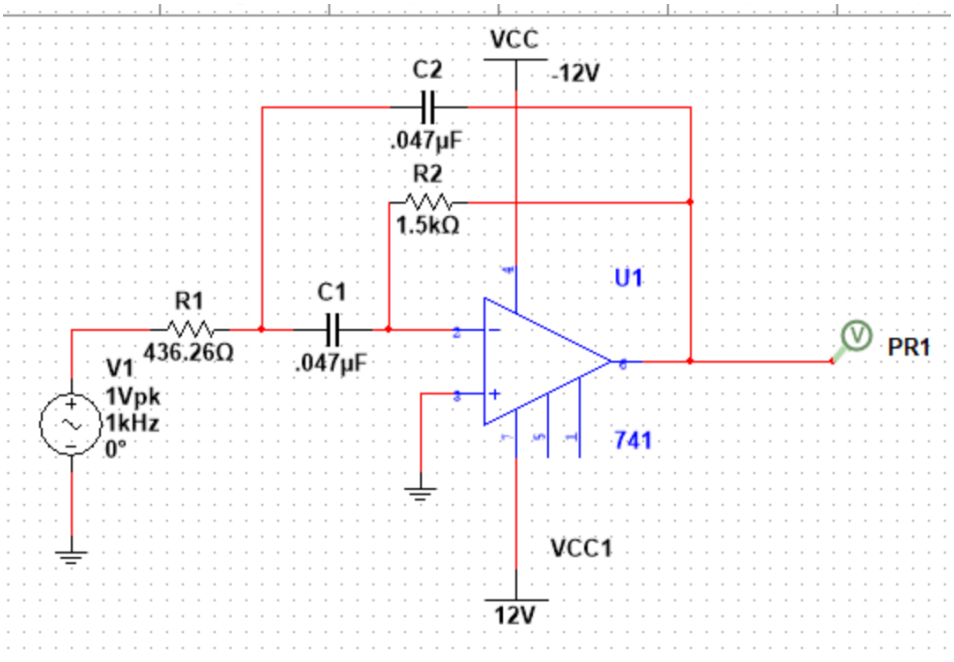
- R1 = 436.26 ohms
- R2 = 1.5k ohms
- C1 = 0.047 uF
- C2 = 0.047 uF

By substituting these values into the equation, we obtained a theoretical center frequency of 4186.05 Hz, which precisely matches our target frequency. This validation ensures that our design is theoretically sound and will function as intended in simulation and real-world implementation.

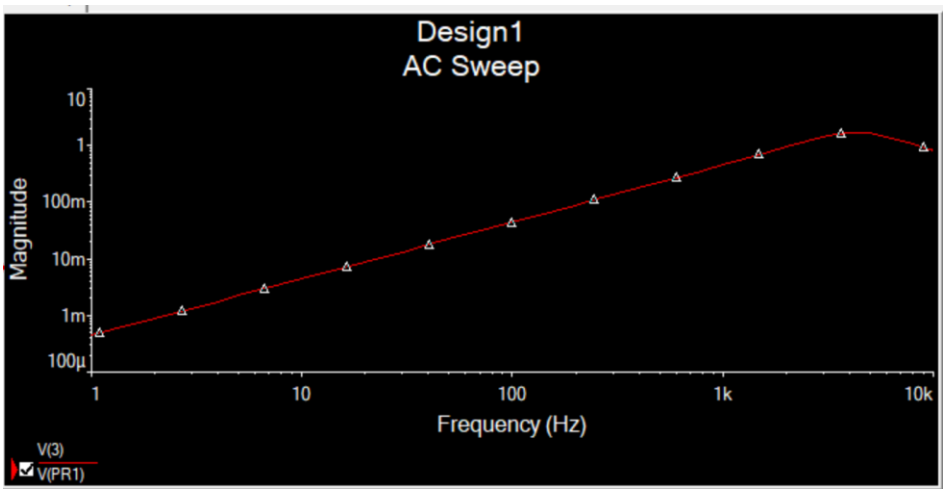
Picture(s)



(**Figure 3:** Paper Design of our filter.)



(**Figure 4:** Filter constructed in Multisim.)



(**Figure 5:** Bode plot our filter arrived at.)

Key Design Decision(s)

- What did your team clarify about the design?
    - Designed the filter to isolate the C8 frequency (4186 Hz) for accurate audio tracking.
- What were the competing choices in the design?
    - A passive filter was considered but dismissed due to lack of gain and lower performance
    - The active bandpass filter was chosen due to its enhanced frequency response and better control over gain and attenuation
- Ultimately what did your team choose and why?
    - Implemented an active bandpass filter using an operational amplifier to improve signal clarity and minimize noise.

TEST… Test… test

- What aspects of the design need to be tested?
    - Software?
        - Simulated in Multisim to confirm theoretical frequency response.
    - Hardware?
        - Not yet implemented – physical testing will be conducted in the next phase
- Who is responsible for testing?
    - Tests ran?
        - Simulated our filter design in multisim and created a bode plot
    - Conclusions from testing?
        - Our bode plot does match the requirements, it peaks at a C8 frequency and ignores unwanted signals

summary/part conclusion (make sure you address all parts of the requirements)

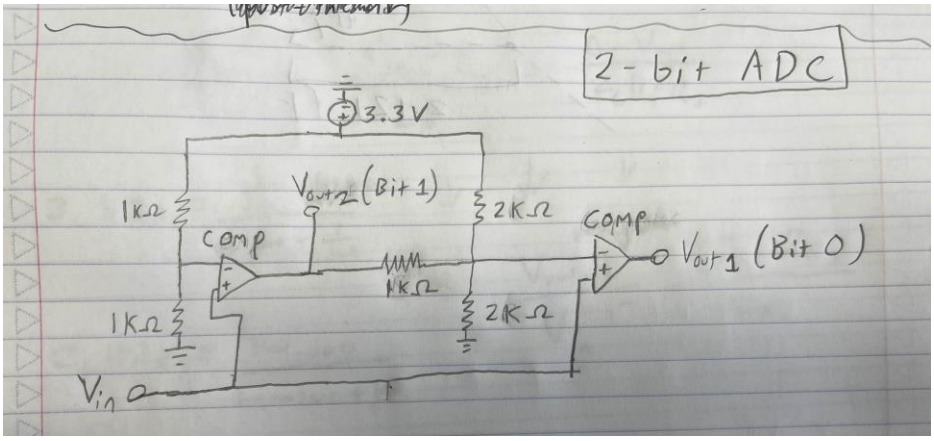
The active bandpass filter successfully isolates the C8 frequency as required for our project. Simulation results confirm that the design matches the theoretical expectations. Future work involves building and testing the circuit physically to ensure that unwanted frequencies are effectively rejected and that real-world performance aligns with simulation

Part 3: Preliminary ADC Design

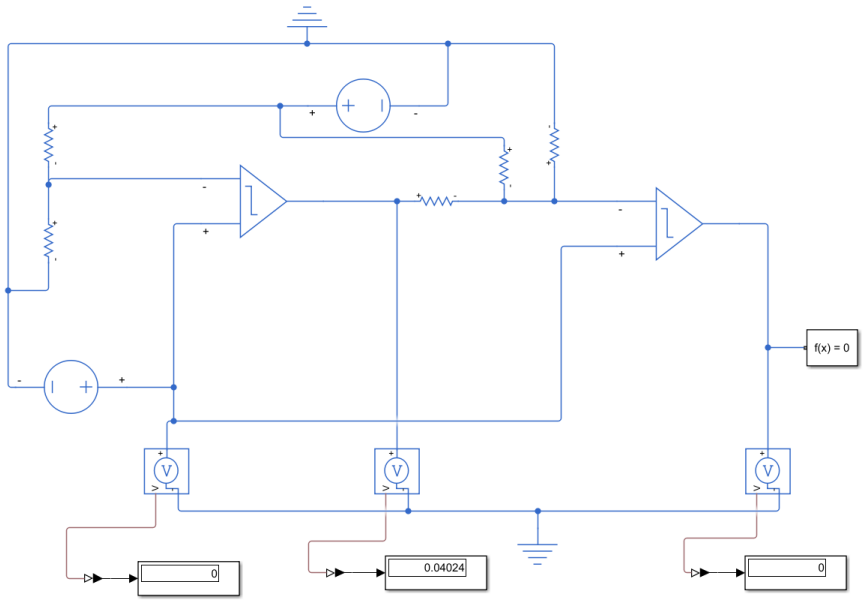
Requirements:

- Develop a paper design for an ADC interfacing with the RP4.
- Simulate ADC functionality with sample inputs.
- Document design choices and bit resolution mapping.

We plan to use two 2-bit ADCs for each targeted frequency. What we plan to achieve is measuring how far our analog signal is above a certain default threshold, which should be achievable through some voltage division. Since each comparator IC has 4 comparators, we plan to fit both ADCs into one chip as well. Each digital output should be giving ~3.3V, and we might shoot slightly lower just to ensure that the GPIO isn't overvolted. At least in simulation, I was able to achieve the functionality of a 2-Bit ADC without using any transistors/logic and only using comparators and a series of R-2R Ladders.

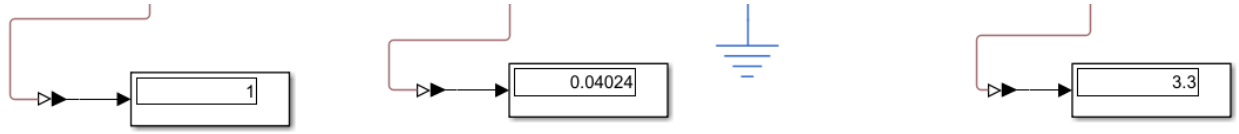


(**Figure 6:** Paper Design for 2-Bit ADC using R-2R ladders and comparators)

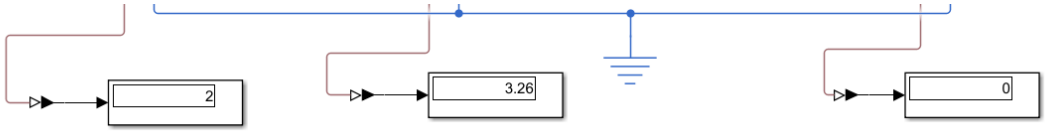


(**Figure 7:** ADC Simulation Circuit and Result for bitmap 00)

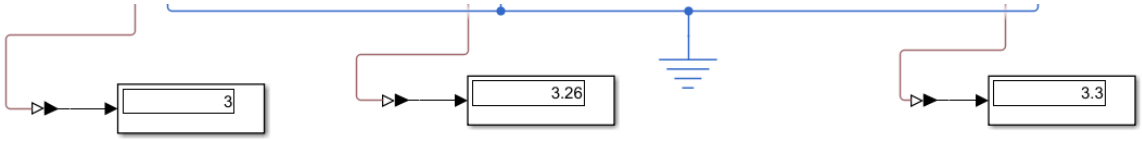
Displayed Values from left to right: Input Voltage, “Bit 1” Voltage, “Bit 0” Voltage



^ ADC Simulation Result for bitmap 01



^ ADC Simulation Result for bitmap 10



^ ADC Simulation Result for bitmap 11

The input voltage thresholds to achieve each bit are given below:

V_{in} < 0.825 -> 00

0.825 < V_{in} < 1.65 -> 01

1.65 < V_{in} < 2.475 -> 10

2.475 < Vin -> 11

Key Design Decision(s)

- What did your team clarify about the design?
  - While it was discussed that an ADC would be required, what information are we transferring?
  - How complicated/redundant do we want the ADC to be?
- What were the competing choices in the design?
  - Digital Logic vs. Resistor Ladders
  - 2-bit (For Each), 3-bit (For each or both), 4-bit (For both)

- Ultimately what did your team choose and why?

We ended up choosing to use a pair of 2-bit ADCs that use a single LM339 Comparator IC and a multitude of 1kOhm/2kOhm resistors. Each 2-bit ADC will be linked at the end of their respective filter chains for the frequencies they target.

We aim to try the simpler designs first. If those don't work, then we can always scale up. We've found it more efficient to do so and we're continuing with that mentality. There is a chain of events that could go wrong here, so if each design is at its simplest to achieve its task, then it's easier to diagnose and debug.

TEST… Test… test

- What aspects of the design need to be tested?
    - Software?
        - The ADC needed to be tested on Simulink
        - GPIO Input Python Script need to be tested for appropriate pins
    - Hardware?
        - Even though the deliverable is due next week, we're testing this hardware version of the ADC now.
- Who is responsible for testing? Michael See
    - Tests ran?
        - Simulink digital twin works as expected and changes correct bit values at theoretical voltage thresholds
        - Designated GPIO pins recognize input in python (when in pulldown)
        - Physical ADC works but isn't changing bits at the expected voltage values.
    - Conclusions from testing?
      Software-wise we are ready to go, but the hardware side of the ADC is still putting up a fight. The comparators in Simulink don't have open collector outputs so it caused a translation issue when building the physical model. When implementing a pull-up resistor, we realized that the resistor ladder is now affected to some degree. We will either mitigate this issue or switch to an ADC design that implements digital logic.

We have designed one of two identical 2-bit ADC's that we intend to use on our audio car. Each ADC consists of two comparators and a resistor ladder. While we were able to get the simulation to work perfectly, we are currently working on bringing our idea to life while taking into account the functional difference between Simulink's comparator and the LM339.

Conclusion and Participation (REQUIRED)

1. **Include a selfie/photo from your group meeting/zoom call.**

2. **When did you meet?**

- 2/14 and 2/17

3. **Who was present?**

- Everyone was present this week:
- Dawson, Michael, Cade, Finn

4. **Who was not present?**

- Everyone was present for at least one meeting

5. **What were the main ideas discussed or major decisions (1-2 sentences/bullet points)**

- Discussed power supply testing approach and potential improvements (added potentiometers)
- Discussed filter design and conducted simulation (active band-pass)
- Considered potential refinements for ADC implementation to improve signal mapping.