ECSE 2920: Design Methodology

Deliverable 10

Group 11

03/26/2025

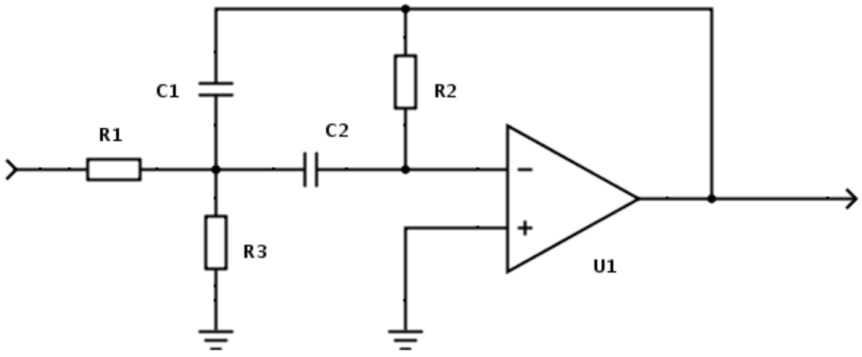
Part 1: Multifilter Design

Requirements:

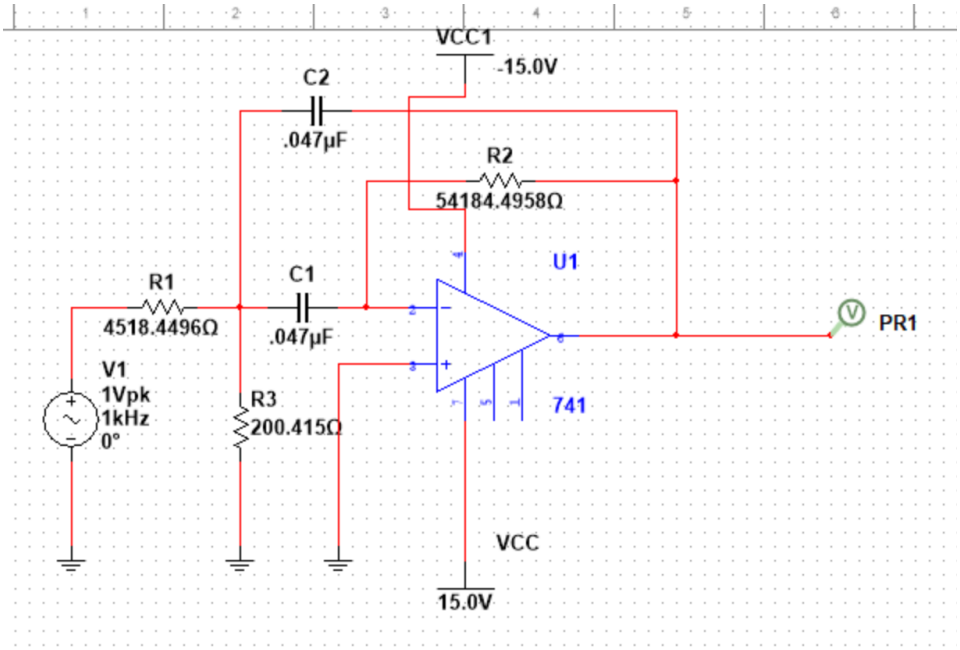
- Implement a multifilter design that can differentiate C8 (4186 Hz) and C6 (1046 Hz) +/- 250Hz
- The system must ignore other frequencies while detecting and responding to C8 first, then C6
- Provide justification for the chosen filter topology, including an explanation of its working principles
- Include simulation results demonstrating proper discrimination of C8 and C6, along with Bode plots for both frequencies
- Show circuit topology schematics with appropriate filtering techniques

Our team plans on using 2 microphones and 2 separate filters for the C6 and C8 frequencies. This is because we don't want to have to worry about the phase difference between the 2 signals and we don't want to have to worry about splitting the already weak microphone signal. For the C6 filter our team decided to use the narrow band pass filter, just like we did for C8. We are using the filter topology because it worked for the C8 signal, and it should work for the C6 as well. To handle the design requirement of going the C8 first then the C6 we are doing some transistor logic, which will be discussed in our ADC design. This filter works by using resistors and capacitors configured in a way that blocks low and high frequencies and only lets frequencies that are perfect for those select resistor/capacitor values. A high-level explanation can be achieved with just simple phasor domain. When the angular frequency is 0 the capacitors have infinite impedance (1/jwC), this creates an open circuit at both C1 and C2 and based of golden rules we can see the output would be 0V. When the angular frequency is infinite the impendence of the capacitor because 0 (1/jwC), and the capacitors become short circuit. Then based off of golden rules you can easily tell that the output is 0V. So, somewhere in-between 0Hz and infinity Hz is a peak output voltage. This peak output voltage is determined by the values of the resistors and capacitors in the circuit.

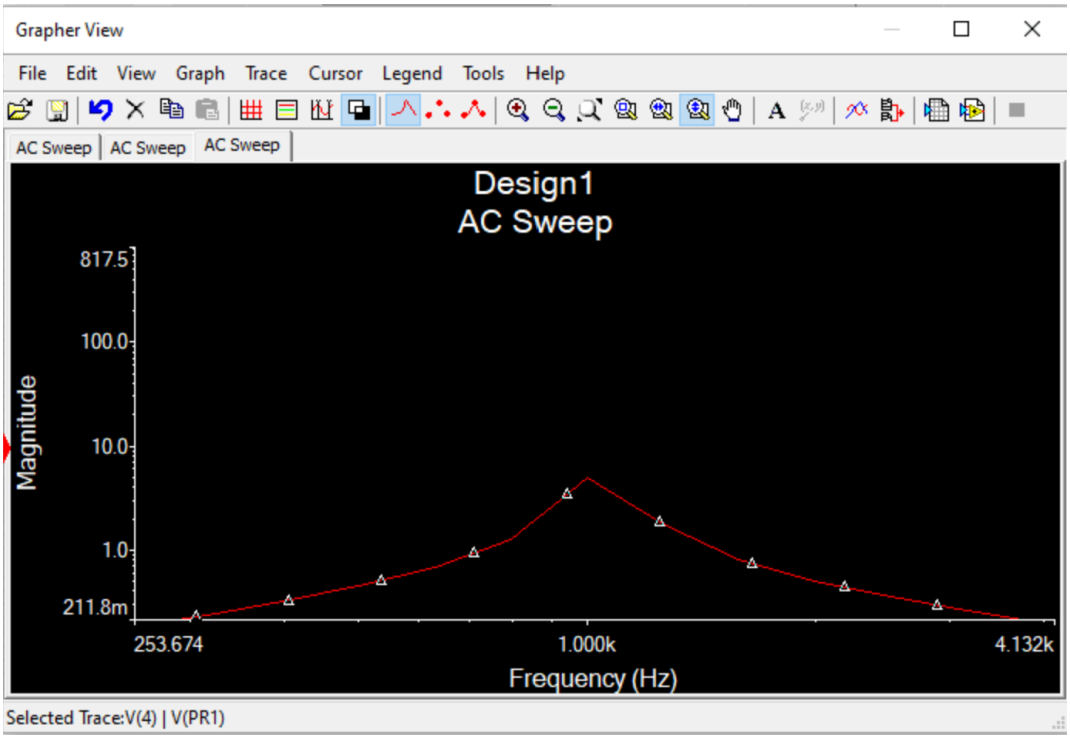
As for signal processing the only thing that needs to be done is rectification for the ADC. We do not need to add any extra gain as we are using an active filter that will provide all the gain that we need. We need to rectify because if not the comparator would be comparing an AC signal and a DC signal, which is possible, it's just the output of the comparator would keep flipping from high to low, which we don't want. We plan on using a simple half bridge rectifier with a capacitor for smoothing, because it's the simplest solution, and it worked for the C8 frequency.



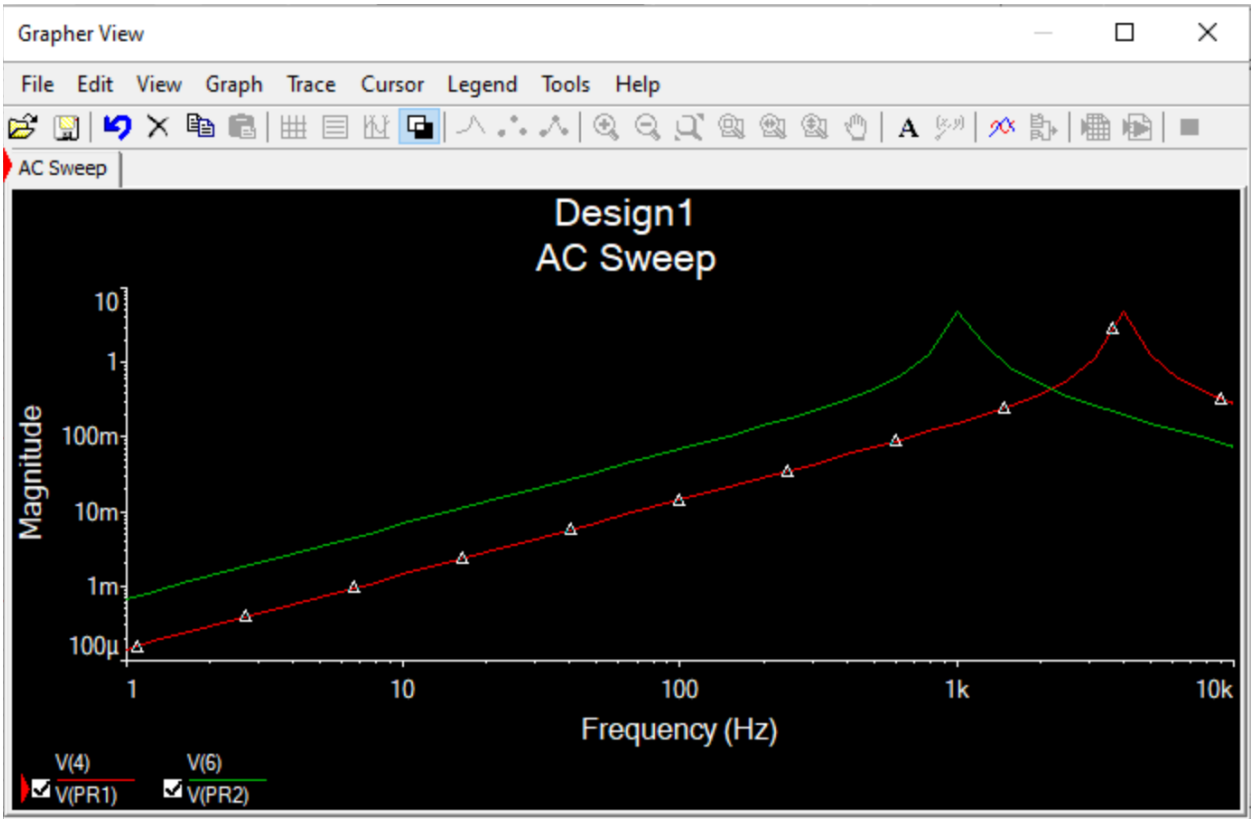
(**Figure 1:** Filter Circuit Diagram.)



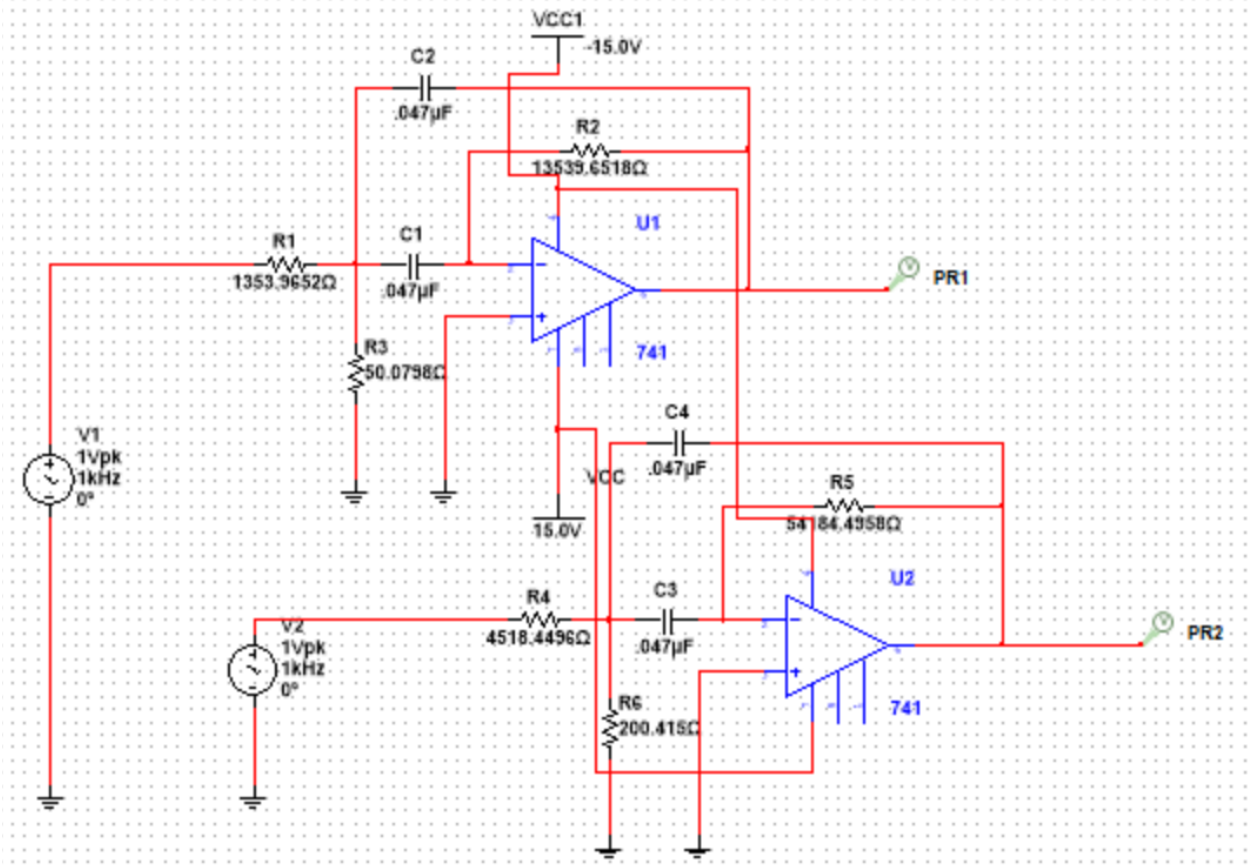
(**Figure 2:** Filter Topology)



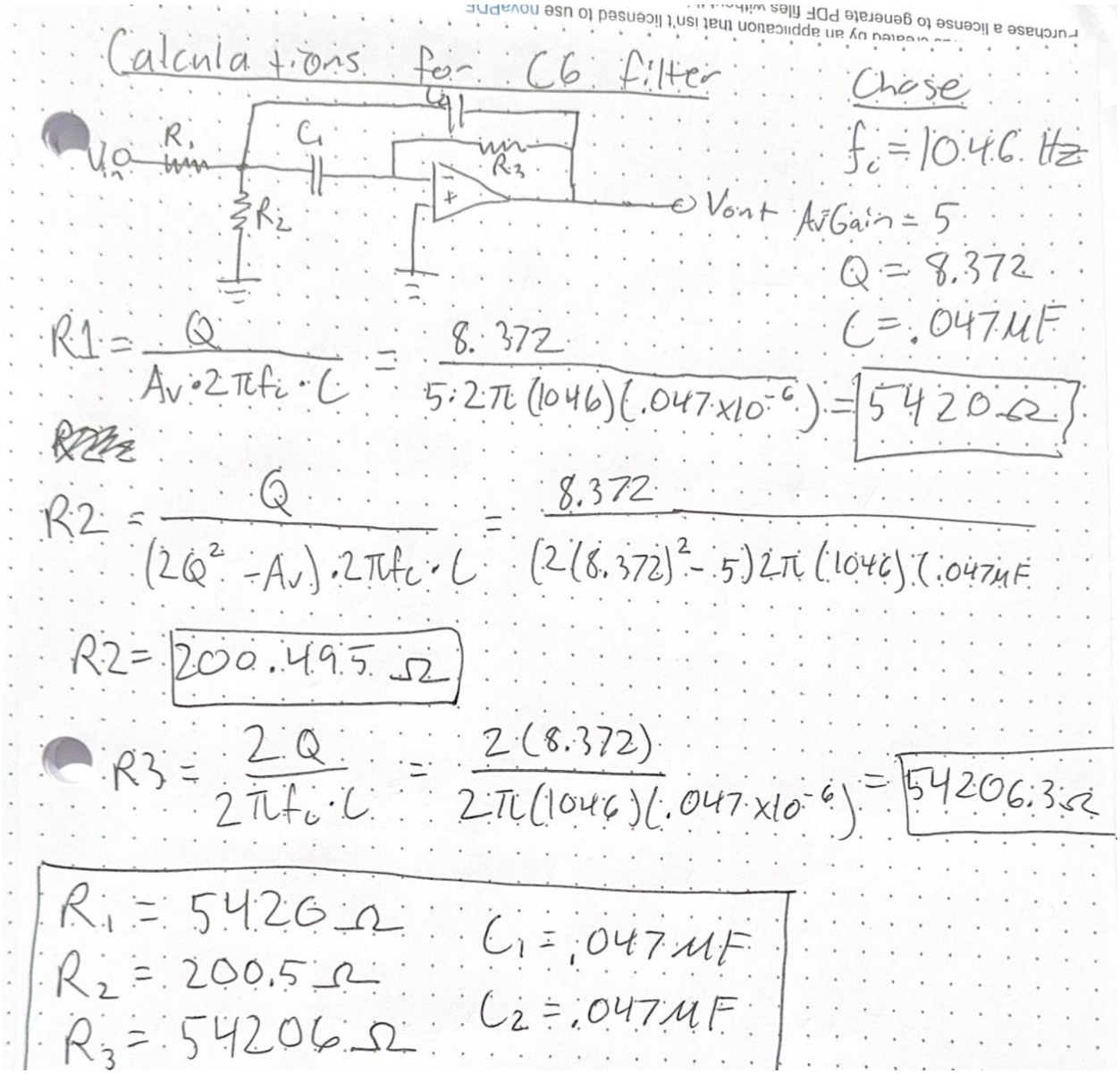
(**Figure 3:** Simulated bode plot for the C6 frequency)



(**Figure 4:** Bode plot with both frequencies)



(**Figure 5:** Multi Filter topology)



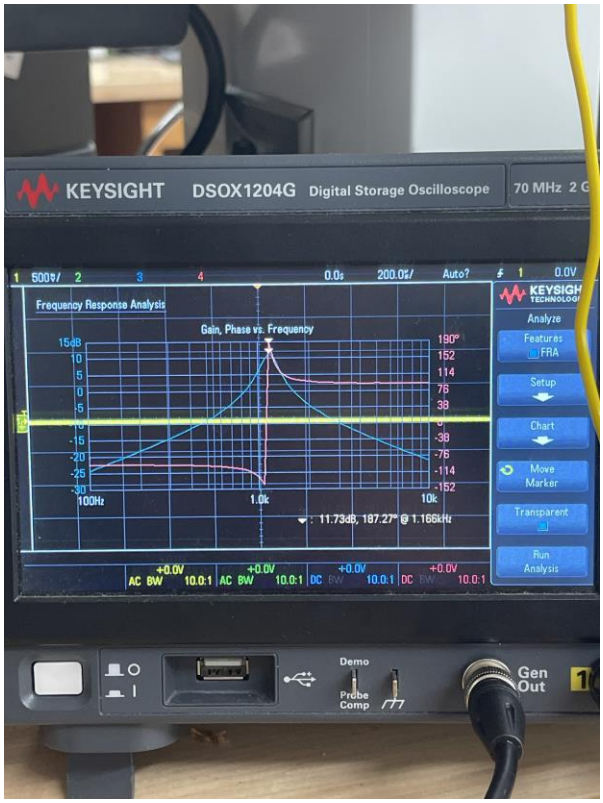
(Hand calculations for C6 filter)

Key Design Decision(s)

- What did your team clarify about the design?
    - The team clarified that we would be using the narrow band pass filter – the same one we used for the C8 frequency.
- What were the competing choices in the design?
    - The only competing choices would be to research another band pass filter instead of sticking with the same filter design from the C8.
- Ultimately what did your team choose and why?

- The team ultimately decided to go with the same design (narrow band pass filter) that we used for the C8, because it worked well for the C8, we have experience with it, it has a narrow band width, and high gain.

TEST… Test… test

- What aspects of the design need to be tested?
  - The frequency response of the filter and the gain, which can be tested simply by using the spectrum analyzer on the digital oscilloscope in the lab.
- Who is responsible for testing? Cade and Michael
  - Tests ran?
    - Used the spectrum analyzer on the digital oscilloscope to view the frequency response.
  - Conclusions from testing?
    - 

    - As you can see here the gain is fine at 11.73db but the center frequency is too high. This is just a matter of changing R3 to a higher resistance and this should lower our center frequency.
    - The band width on the filter is >500Hz, which is good for the +/- 250Hz however a smaller bandwidth might be needed to sufficiently block the frequencies outside the +/-250 Hz range.
    - This will require testing with the mic and ADC to determine if the bandwidth is good enough.

summary/part conclusion (make sure you address all parts of the requirements)

- In conclusion we updated the bode plots to show the new C6 frequency. This was tested in shown in simulation and physically in the lab. We justified why we are using the narrow band pass filter topology because we have experience with it, we know it works, it has high gain, and narrow band width. We also provided a high-level explanation of how the filter works using the phasor domain. We showed the filter topology in simulation in isolation and with the C8 filter. We also described how we would process the signal from our filter to make it ready for our ADC, by rectifying our signal – taking it from AC to DC – using a half bridge rectifier and capacitor for smoothing.

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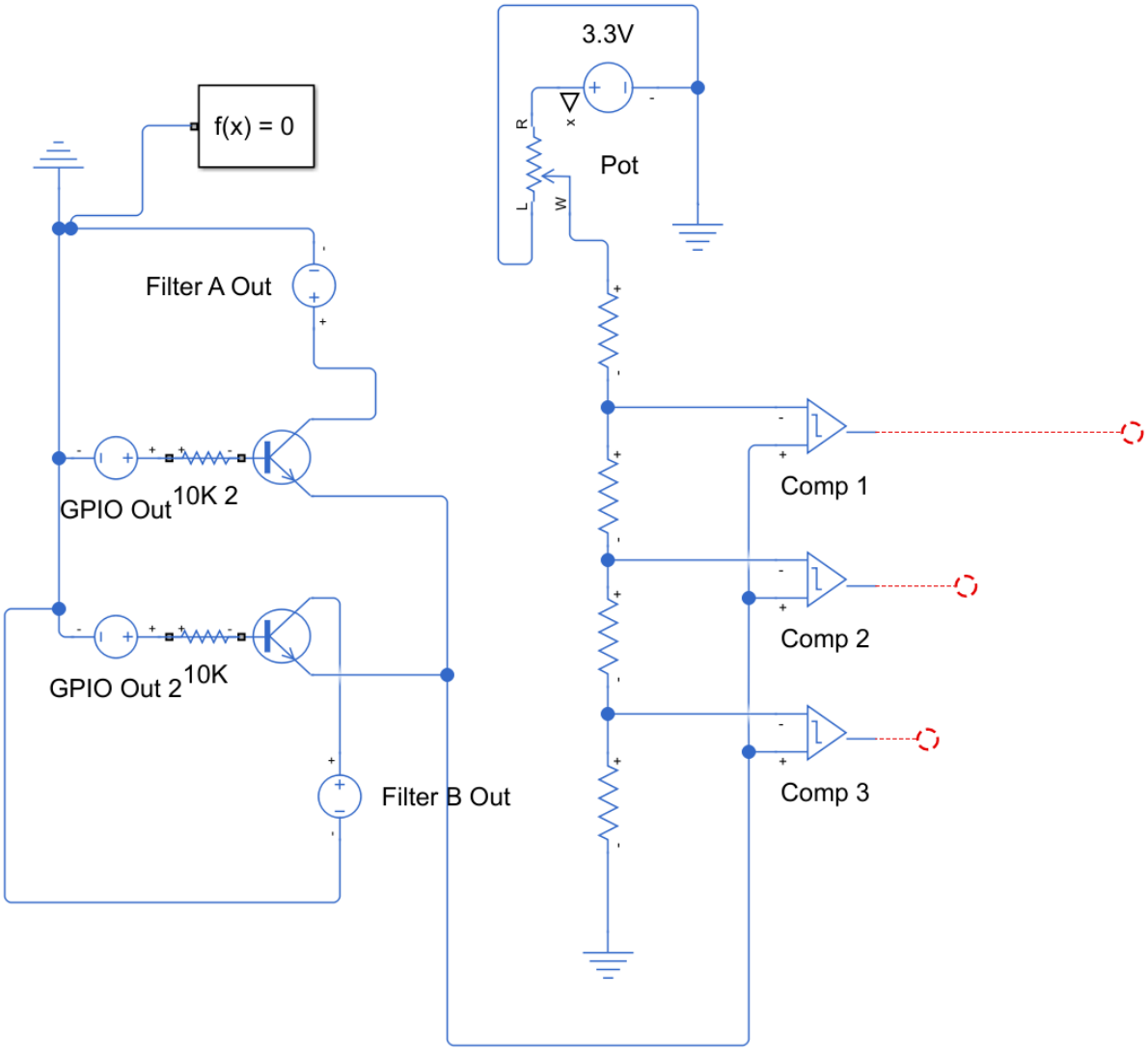
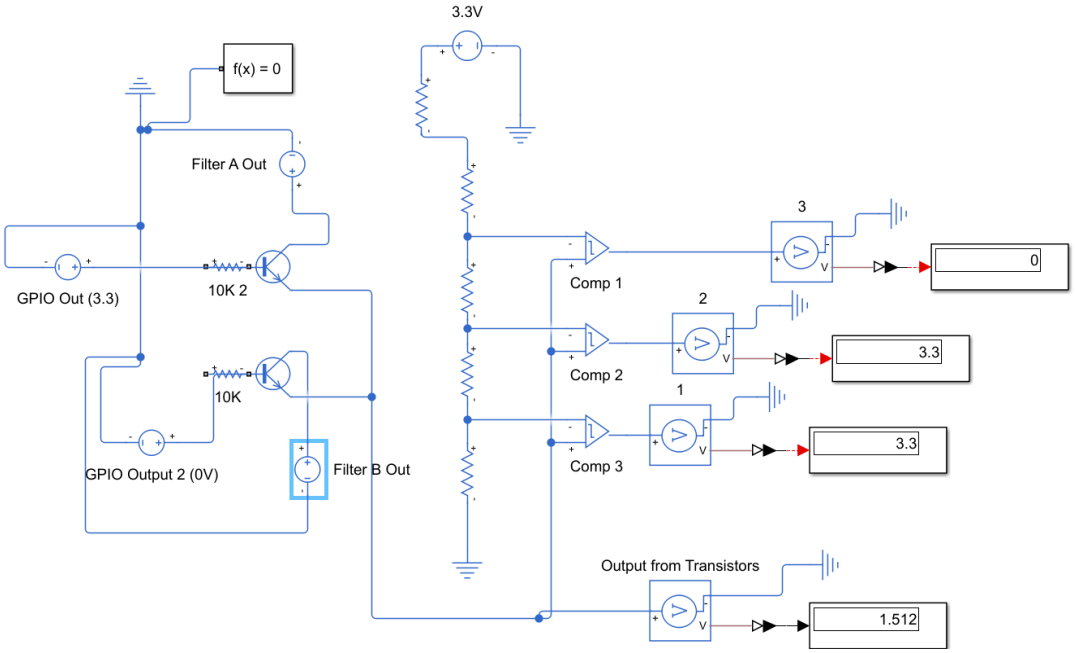
Part 2: ADC

Requirements:

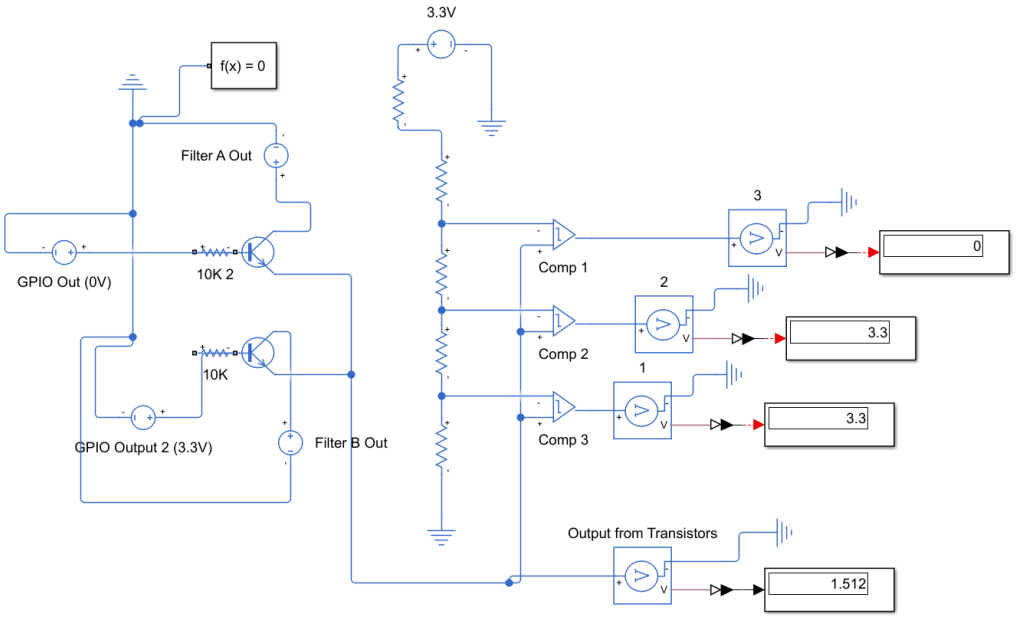
- **Update the ADC design to accommodate data for two filter paths**
- **Implement signal processing techniques (gain adjustment, shaping, etc.) to prepare signals for ADC conversion.**
- **Justify the data acquisition approach for handling both filters' outputs**
- **Provide simulation results for the ADC modifications**
- **Include a schematic of the updated ADC circuit**



ADC Updated Schematic ^



Here both filter outputs are outputting 1.5V (Approximate filter output when pointing to source).
5K potentiometer above resistor ladder is replaced with 2500k resistor (mid sensitivity)
One GPIO should be on at a time here. Both signals should never pass through.
As shown, we get an equivalent value of 2, which is what we desire since values of 3 can come with data inaccuracies.



All that changes here is that the GPIO outputs are switched. What this displays is that both signals can accurately be transported to the ADC with barely any modification from the original signal.

Key Design Decision(s)

- What did your team clarify about the design?
    - **There needs to be a way for the pi to obtain data about both filter outputs.**
- What were the competing choices in the design?
    - **Two separate ADCs for each filter output**
    - **Using comparators to select filter output to one ADC**
    - **Using transistors to select filter outputs in one ADC**

- Ultimately what did your team choose and why?
    - **We chose to use transistors to select which filter is being read by the ADC in any given moment. Originally, we were going to have two separate chains and two separate ADCs, but we ended up switching for a couple reasons. First of all, we're gunning for the most compact build out of any design group. If we built another ADC, it would cause a need for things to be rearranged on the car, which could cause other issues soon after. Secondly, if we had two ADCs, we would have two adjustable potentiometers on each, which might make testing/troubleshooting more complicated. Lastly, the transistor option would take up the least amount of GPIO ports and resources out of the three options listed above. They also don't require as many connections as comparators do.**

TEST… Test… test

- What aspects of the design need to be tested?
    - Software?
        - **Are there two GPIO ports available on the pi that can interact with python?**
    - Hardware?
        - **Are the signals still intact after passing through the transistors?**
        - **Are the signals being properly isolated?**
- Who is responsible for testing? **Michael, Cade, Finn, and Dawson**
    - Tests ran?
        - **Each "Filter Output" was simulated as a sawtooth wave from the function generator. This simulates a rectified AC signal. Each "GPIO" was simulated as a DC 3.3V signal. We had both signals feeding into the collectors of the transistors and switched the "GPIOs" on individually.**
    - Conclusions from testing?
        - **The signals have a slight boost in V_{pp} due to the extra base current supplied by the transistor (when on), but the potentiometer on the ADC should be able to mitigate it.**

- **When both signals are off, nothing comes out of the output (which is a connection between both emitters and the + pin of the comparators). This means that each signal is isolated from the rest of the system. It is imperative that the pi only reads the desired signal when tracking each frequency.**

To accommodate for both filter paths, we have decided to make a primitive version of an OR gate that uses two transistors to select which signal is being fed into our singular ADC. Gain adjustment was already implemented in checkpoint B and consists of a potentiometer in series to adjust the reference voltage of the comparators. Based on the testing we have done so far; we believe that this design will work with the other components we already have created. For the most part, each signal is nearly identical to how it looked before the transistors and when a signal isn't passed through a transistor, it is blocked from interfering with the other signal being read.

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Conclusion and Participation (REQUIRED)

1. **Include a selfie/photo from your group meeting/zoom call.**

2. **When did you meet? 3/21/2025**
3. **Who was present? Cade, Dawson, Finn, Michael**
4. **Who was not present? Everyone was present**
5. **What were the main ideas discussed or major decisions (1-2 sentences/bullet points)**

We discussed and confirmed plans for the new ADC while building and testing the filter for checkpoint A.