mux21_1 Design Specification

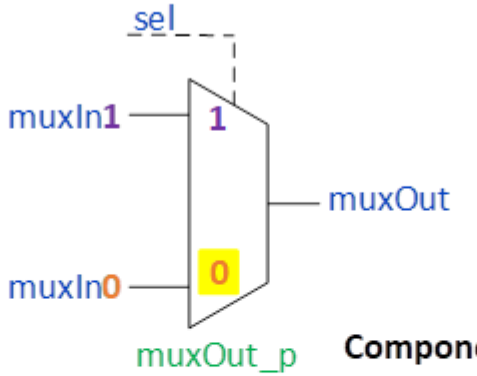
Component Name mux21_1
Title 2-to-1 multiplexer, 1-bit data

Description
muxOut = muxIn0 (default)
Assertion of sel selects muxOut = muxIn1

Component signal dictionary
sel datapath select,
'0'/'1' passes muxIn1/0 data to muxOut
muxIn1 datapath 1, 1-bit data
muxIn0 datapath 0, 1-bit data
muxOut output data, 1-bit data

Internal signal dictionary
None

2-to-1 Multiplexer, 1-bit data (mux21_1)



Component Symbol

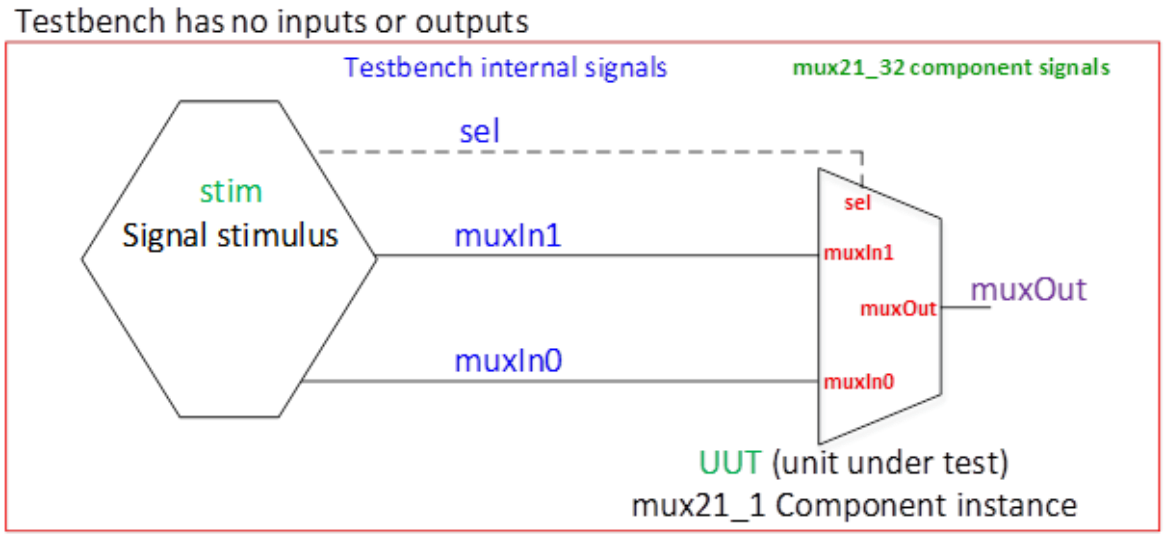
sel	muxOut
0	muxIn0
1	muxIn1

Function Table

Signal Name	input/ output	Signal description
sel	in	datapath select, '0'/'1' passes muxIn1/0 data to muxOut
muxIn1	in	datapath 1, 1-bit data
muxIn0	in	datapath 0, 1-bit data
muxOut	out	output data, 1-bit data

Signal Dictionary

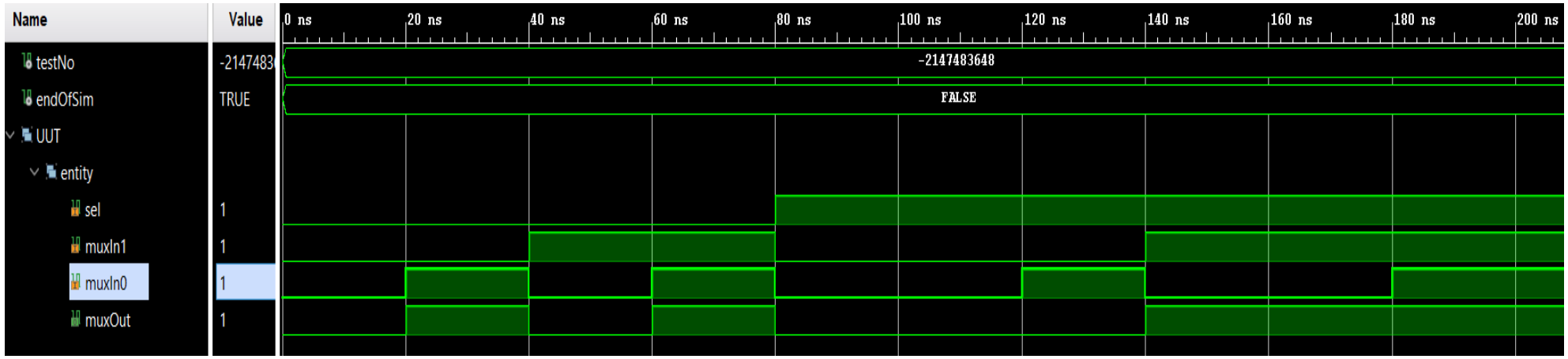
mux21_1
Test Specification



Testbench diagram

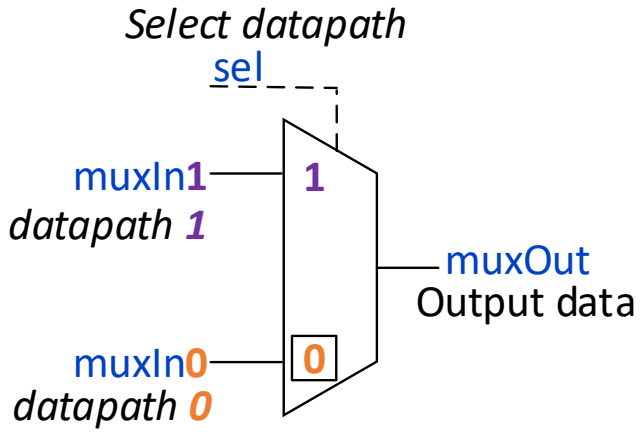
TestNo	Input signals sel binary	muxIn1 hexadecimal	muxIn0 hexadecimal	delay	Output signals muxOut hexadecimal	Note
1	0	0	0	(1*period)	0	
2	0	0	1	(1*period)	1	
3	0	1	0	(1*period)	0	
4	0	1	1	(1*period)	1	
5	1	0	0	(1*period)	0	datapath 1 active
6	1	0	1	(1*period)	0	
7	1	1	0	(1*period)	1	datapath 1 active
8	1	1	1	(1*period)	1	

Testplan



Simulation waveform

2-to-1 Multiplexer (mux21_1), 1-bit data



Component Symbol

Signal dictionary

sel	datapath select, '0'/'1' passes muxIn1/0 data to muxOut
muxIn1	datapath 1
muxIn0	datapath 0
muxOut	output data

Description (process description)

muxOut = muxIn0 (default)

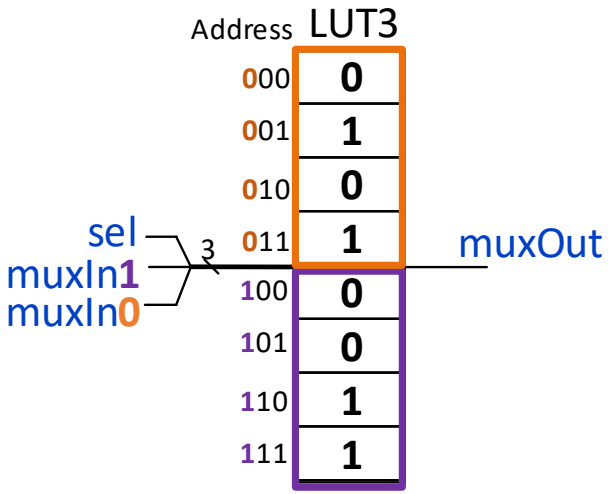
Assertion of sel selects muxOut = muxIn1

sel	muxOut
0	muxIn0
1	muxIn1

Function Table

Address	sel	muxIn1	muxIn0	muxOut
000	0	0	0	0
001	0	0	1	1
010	0	1	0	0
011	0	1	1	1
100	1	0	0	0
101	1	0	1	0
110	1	1	0	1
111	1	1	1	1

Truth Table



3-Input Lookup Table (LUT3)

Input signal sequence sel, muxIn1, muxIn0