

Laboratório 3

- CPU MIPS Uniciclo -

GRUPO 6

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Objetivos

- Treinar o aluno com a linguagem de descrição de *hardware Verilog*;
- Familiarizar o aluno com a plataforma de desenvolvimento *FPGA DE2* da *Altera* e o software *QUARTUS II*;
- Desenvolver a capacidade de análise e síntese de sistemas digitais usando uma Linguagem de Descrição de *Hardware*;
- Apresentar ao aluno a implementação de uma *CPU MIPS*.

Ferramentas

Todos os códigos escritos neste laboratório podem ser encontrados no repositório <https://github.com/Dayof/OAC172> do *GitHub*.

- FPGA DE2 da Altera
- QUARTUS-II
- Verilog HDL

Exercícios - PARTE A

Exercício 4. Diagrama de fluxo para tratamento de exceção

O tratamento de exceção obtém a causa através de um registrador especial denominado ”CAUSE” ”\$13”, o endereço de retorno é armazenado em outro registrador, o EPC ”\$14” (exception programmer counter). Esses registradores especiais não fazem parte do conjunto de registradores de uso geral do MIPS, eles ficam em um local especial , chamado de coprocessor 0. As instruções usadas para acessar esses registradores são o mfc0 e o mtc0.

Abaixo você encontrara o diagrama completo da rotina de tratamento de exceção do MIPS, que foi baseada no systemv54.s . Os números conectam o diagrama, fechando o ciclo no número ”12”.

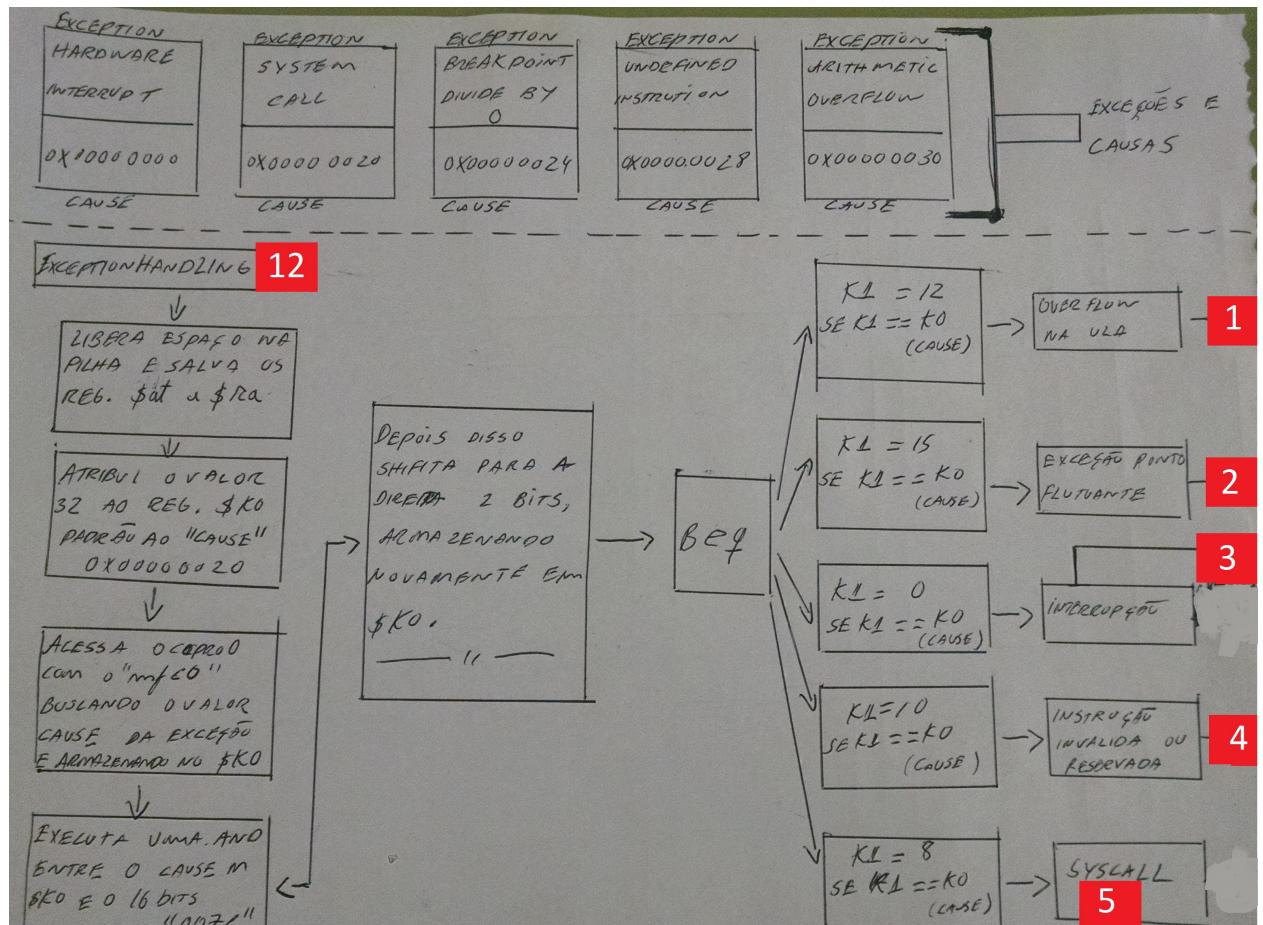


Figure 1. Parte 1.

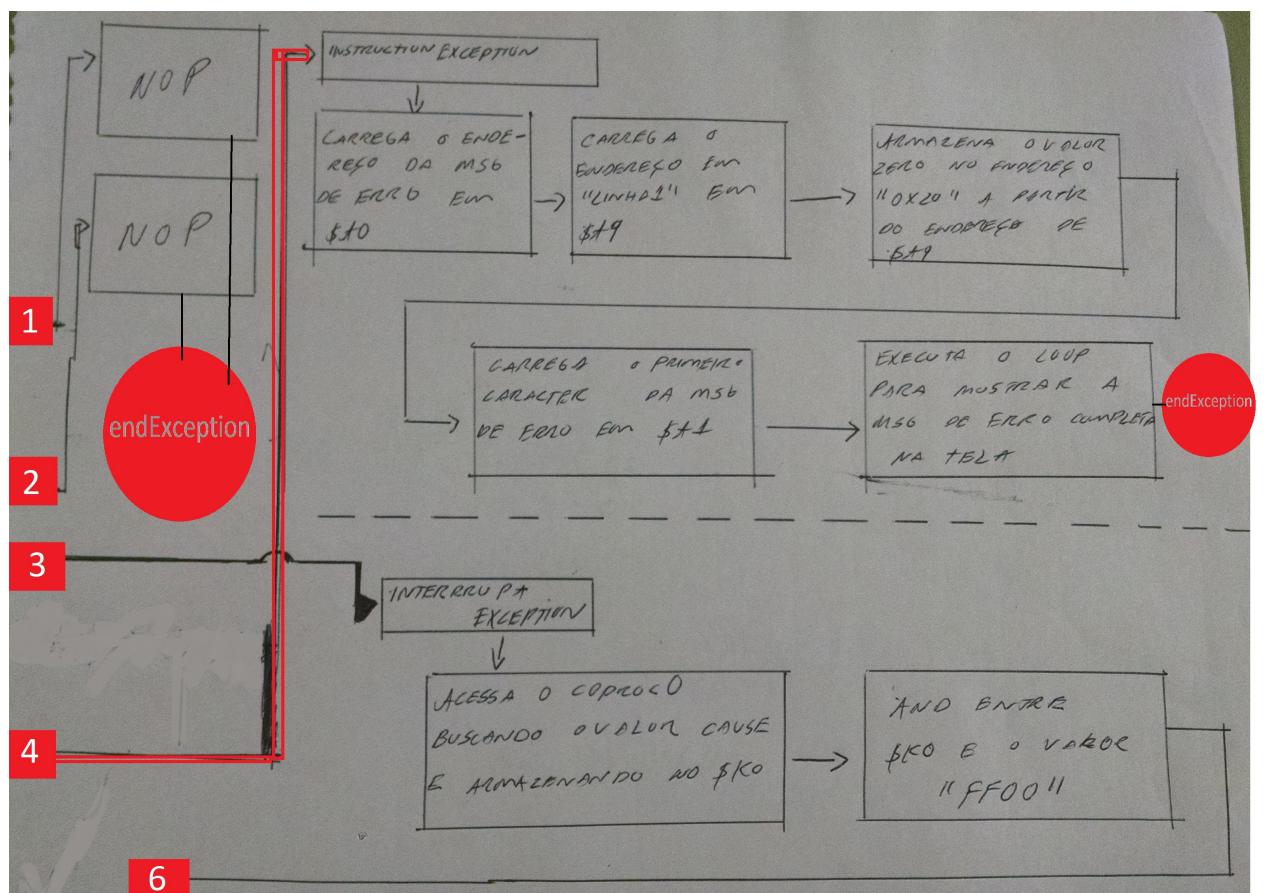


Figure 2. Parte 2.

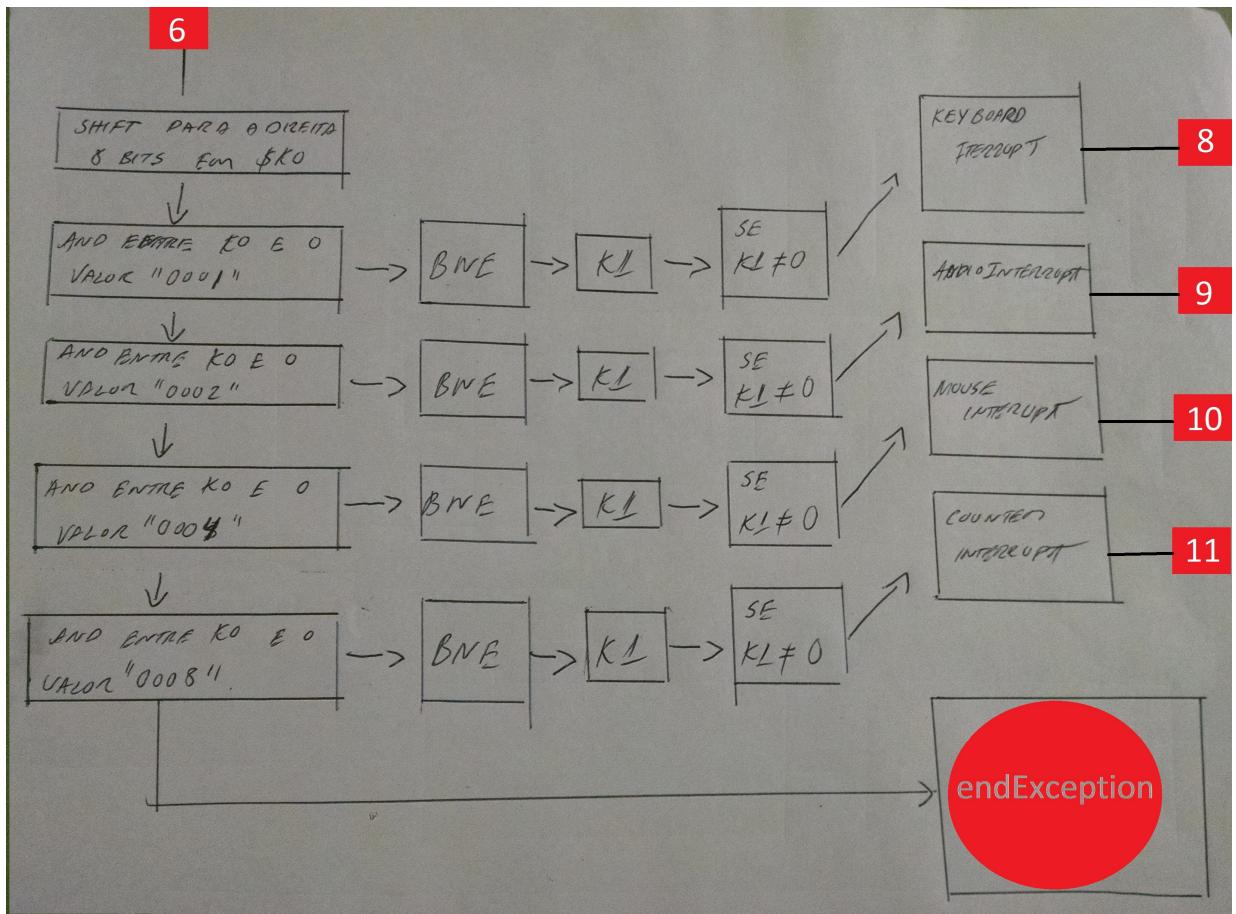


Figure 3. Parte 3.

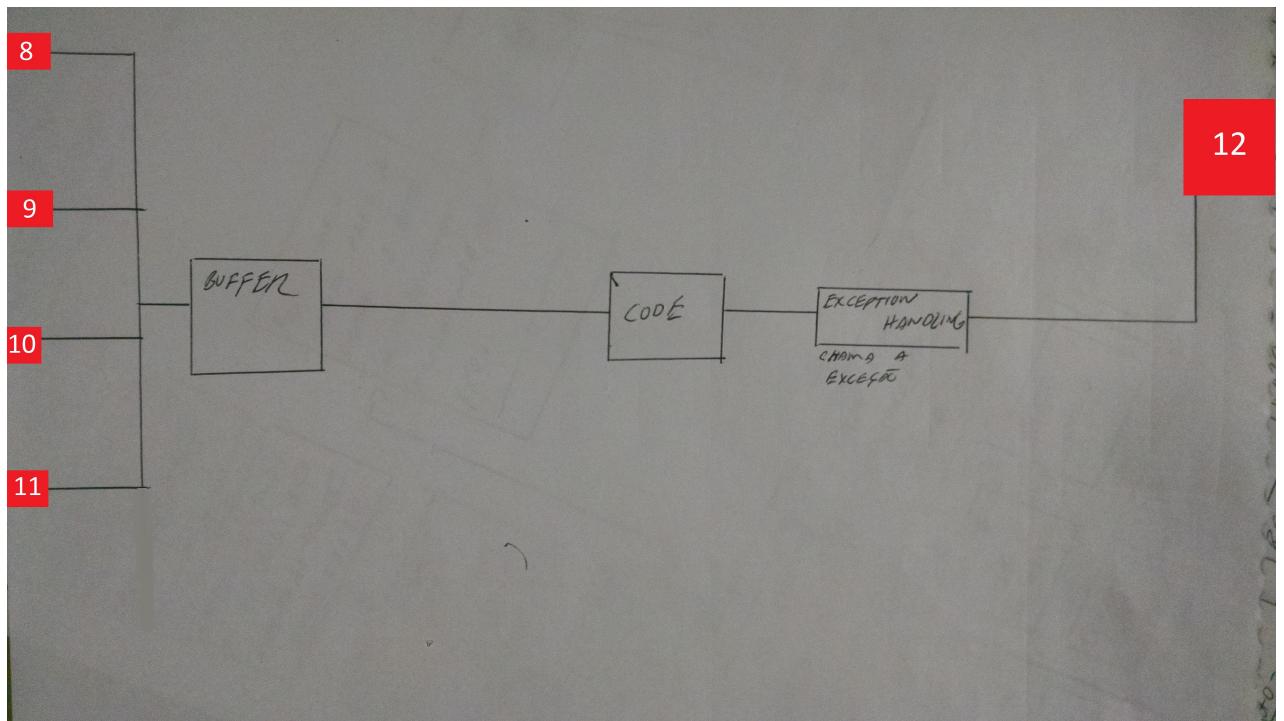


Figure 4. Parte 4.

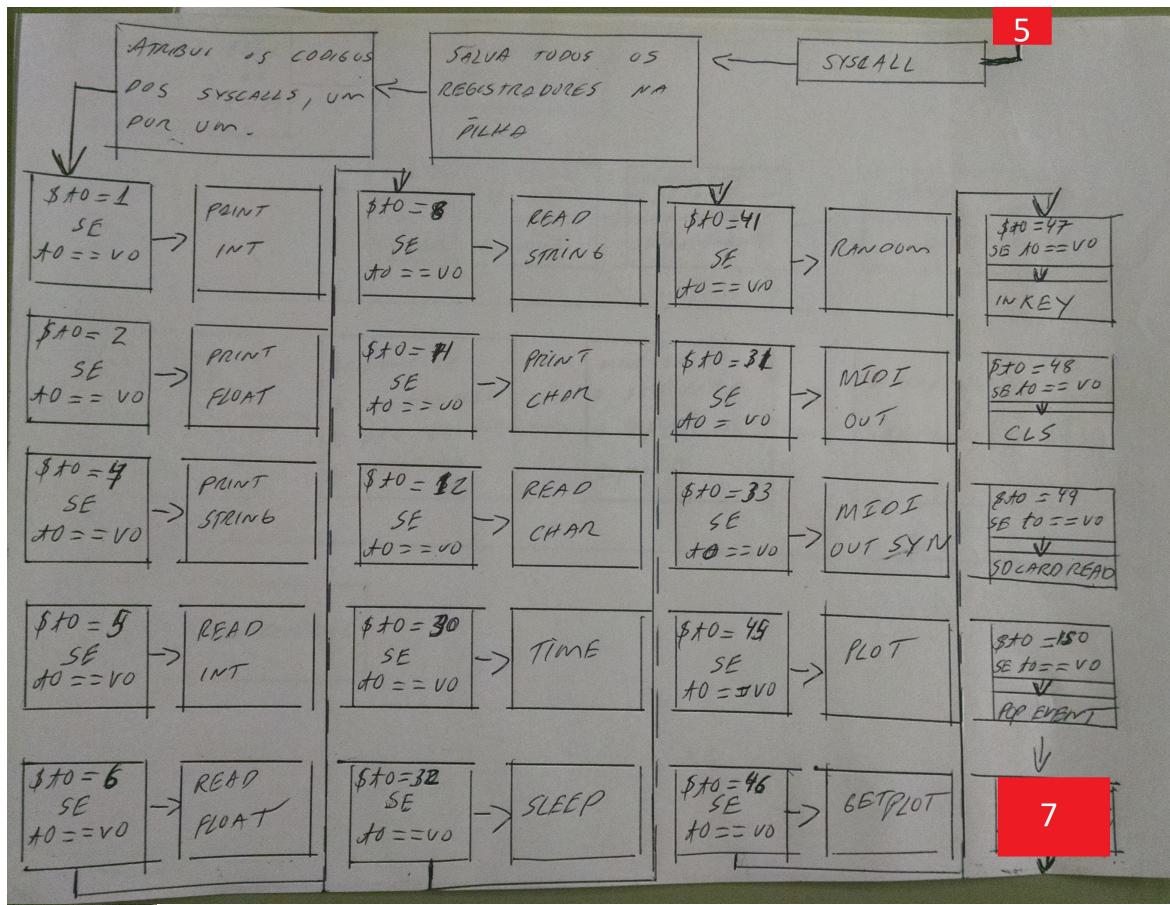


Figure 5. Parte 5.

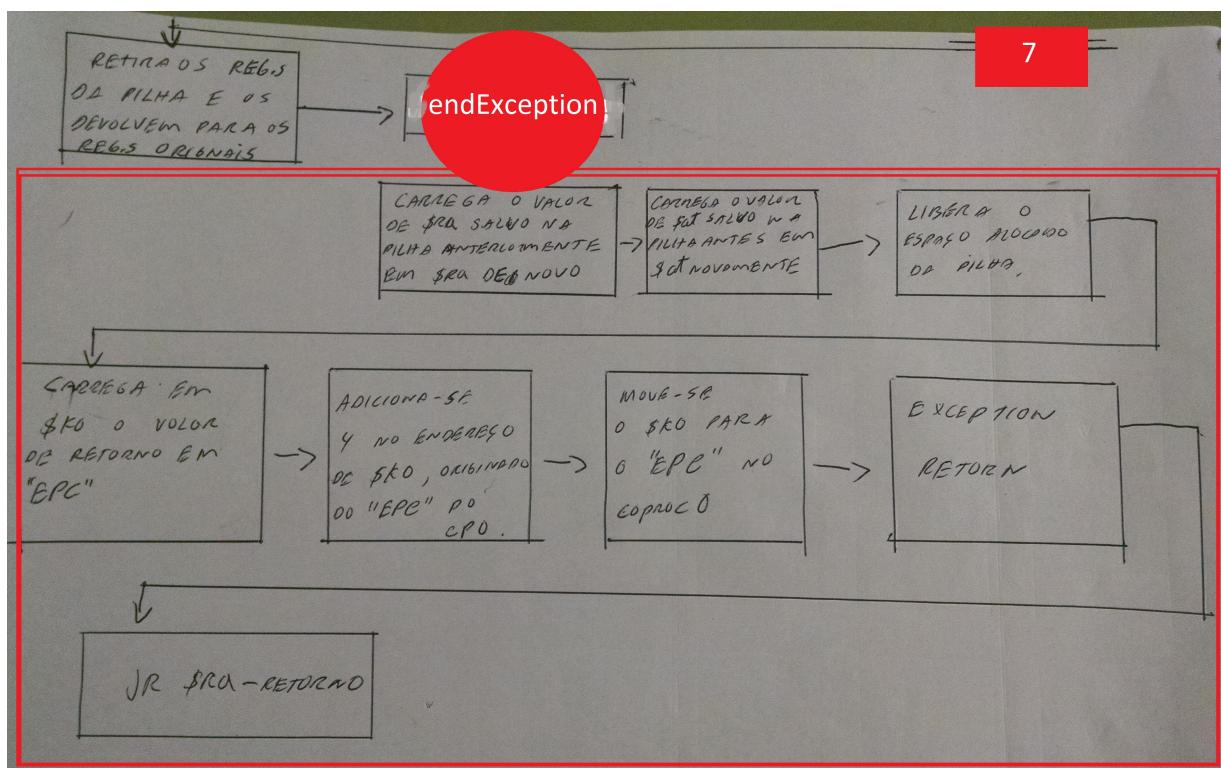


Figure 6. Parte 6.

Exercício 5. Software de lançamento de bola de canhão na FPGA

Abaixo, segue o vídeo demonstrativo da simulação do lançamento de bola de canhão executado na FPGA desenvolvido no laboratório 1:

Vídeo Demonstrativo

Exercícios - PARTE B

Exercício 7. Processador MIPS PUMv.5.1 UNICICLO

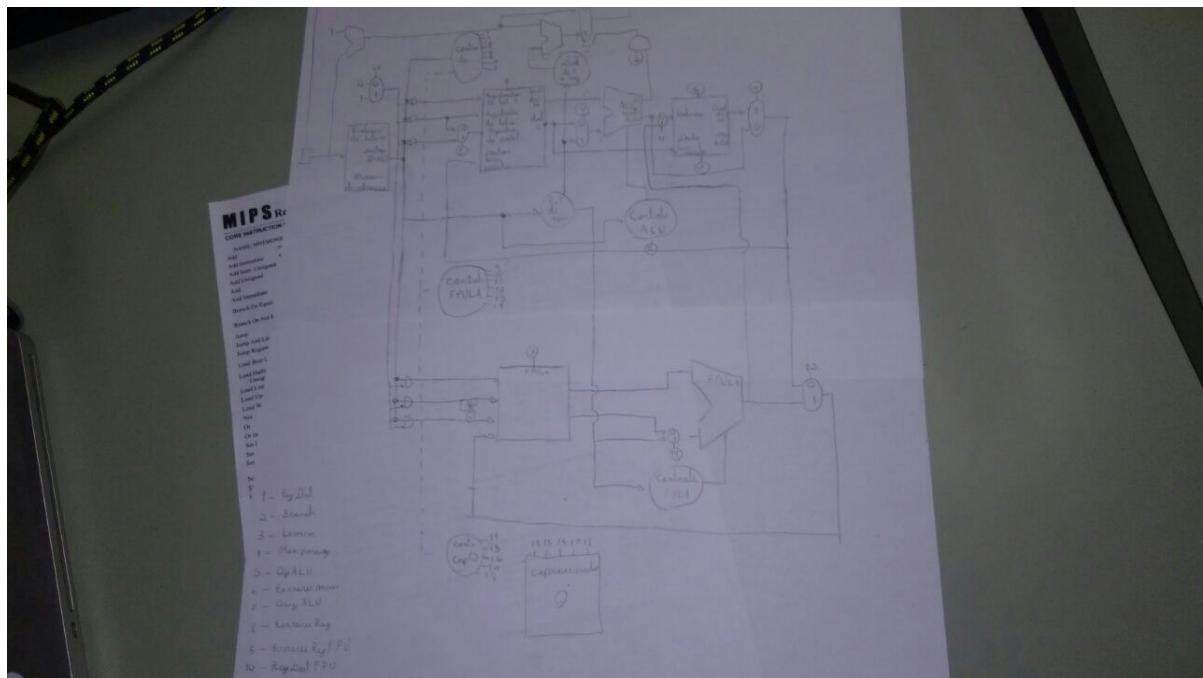


Figure 7. Diagrama de blocos do Caminho de Dados.

	oRegDst	oOrigALU	oMemforReg	oWriteReg	oReadMem	oWriteMem
ADD/SUB	01	00	000	1	0	0
ADDU/SUBU	01	00	000	1	0	0
SW/SH/SB	00	01	000	0	0	1
LBU/LHU	00	01	110	1	1	0
LB/LH	00	01	110	1	1	0
LW	00	01	110	1	1	0
BEQ	00	00	000	0	0	0
BNE	00	00	000	0	0	0
JR	00	00	000	0	0	0
SYS	00	00	000	0	0	0
SLL/SRL/SRA	01	00	000	1	0	0
MFHI/MFLO	01	00	000	1	0	0
MTHI/MTLO	01	00	000	1	0	0
MUL/DIV	01	00	000	1	0	0
MULT/DIVU	01	00	000	1	0	0
ADDU/SUBU	01	00	000	1	0	0
AND/OR	01	00	000	1	0	0
XNOR/NOR	01	00	000	1	0	0
SLT/SLTU	01	00	000	1	0	0
SLLV/SRLV	01	00	000	1	0	0

SRAV	01	00	000	1	0	0
JMP	01	00	000	0	0	0
JAL	10	11	010	1	0	0
ADDI	00	01	000	1	0	0
ADDIU	00	01	000	1	0	0
SLTI/SLTIU	00	01	000	1	0	0
ANDI	00	10	000	1	0	0
XORI/ORI	00	10	000	1	0	0
LUI	00	00	011	1	0	0
MTC	00	00	000	0	0	0
MFC	00	00	100	1	0	0
BC1-0	00	00	000	0	0	0
BC1-1	00	00	000	0	0	0
ADDS/SUBS	00	00	000	0	0	0
MULS/DIVS	00	00	000	0	0	0
CVTSW	00	00	000	0	0	0
SQRT	00	00	000	0	0	0
ABS/NEG	00	00	000	0	0	0
CVTWS	00	00	000	0	0	0
CEILWS	00	00	000	0	0	0
FLOORWS	00	00	000	0	0	0
ROUNDWS	00	00	000	0	0	0
CEQ/CLT/CLE	00	00	000	0	0	0
MOV	00	00	000	0	0	0
SWC1	00	01	000	0	0	1
LWC1	00	01	000	0	1	0
BGEZ	00	11	000	0	0	0
BGEZAL	10	11	010	1	0	0
BLTZ	00	11	000	0	0	0
BLTZAL	11	11	010	1	0	0
BLEZ	00	11	000	0	0	0
BGTZ	00	11	000	0	0	0
MFC	00	00	101	1	0	0
MTC	00	00	000	0	0	0
ERET	00	00	000	0	0	0

Table 1: Tabela verdade das operações da ISA.

	oOrigPC	oOpALU	oWRegFPU	oRDFPU	oFPUpMem	oDRFPU
ADD/SUB	000	11	0	00	00	00
ADDU/SUBU	000	11	0	00	00	00
SW/SH/SB	000	00	0	00	10	00
LBU/LHU	000	00	0	00	00	00
LB/LH	000	00	0	00	00	00

LW	000	00	0	00	00	00
BEQ	001	01	0	00	00	00
BNE	101	01	0	00	00	00
JR	011	00	0	00	00	00
SYS	100	00	0	00	00	00
SLL/SRL/SRA	000	10	0	00	00	00
MFHI/MFLO	000	10	0	00	00	00
MTHI/MTLO	000	10	0	00	00	00
MUT/DIV	000	10	0	00	00	00
MUTU/DIVU	000	10	0	00	00	00
ADDU/SUBU	000	10	0	00	00	00
AND/OR	000	10	0	00	00	00
XNOR/NOR	000	10	0	00	00	00
SLT/SLTU	000	10	0	00	00	00
SLLV/SRLV	000	10	0	00	00	00
SRAV	000	10	0	00	00	00
JMP	010	00	0	00	00	00
JAL	010	11	0	00	00	00
ADDI	000	11	0	00	00	00
ADDIU	000	11	0	00	00	00
SLTI/SLTIU	000	11	0	00	00	00
ANDI	000	11	0	00	00	00
XORI/ORI	000	11	0	00	00	00
LUI	000	00	0	00	00	00
MTC	000	00	1	10	01	00
MFC	000	00	0	00	00	00
BC1-0	111	00	0	00	00	00
BC1-1	110	00	0	00	00	00
ADDS/SUBS	000	00	1	00	00	00
MULS/DIVS	000	00	1	00	00	00
CVTSW	000	00	1	00	00	00
SQRT	000	00	1	00	00	00
ABS/NEG	000	00	1	00	00	00
CVTWS	000	00	0	00	00	00
CEILWS	000	00	0	00	00	00
FLOORWS	000	00	0	00	00	00
ROUNDWS	000	00	0	00	00	00
CEQ/CLT/CLE	000	00	0	00	00	00
MOV	000	00	1	11	00	00
SWC1	000	00	0	00	00	01
LWC1	000	00	1	01	10	00
BGEZ	001	11	0	00	00	00
BGEZAL	001	11	0	00	00	00
BLTZ	101	11	0	00	00	00

BLTZAL	101	11	0	00	00	00
BLEZ	001	11	0	00	00	00
BGTZ	101	11	0	00	00	00
MFC	000	00	0	00	00	00
MTC	000	00	0	00	00	00
ERET	000	00	0	00	00	00

Table 2: Tabela verdade das operações da ISA.

	oFPFW	oWRCOPO	oEretCOPO	oExOCOPO	oBDCOPO	oExCCOPO
ADD/SUB	0	0	0	wALUExcept.	0	wALUExccod.
ADDU/SUBU	0	0	0	wIntExcept.	0	EXCODEINT
SW/SH/SB	0	0	0	wIntExcept.	0	EXCODEINT
LBU/LHU	0	0	0	wIntExcept.	0	EXCODEINT
LB/LH	0	0	0	wIntExcept.	0	EXCODEINT
LW	0	0	0	wIntExcept.	0	EXCODEINT
BEQ	0	0	0	wIntExcept.	1	EXCODEINT
BNE	0	0	0	wIntExcept.	1	EXCODEINT
JR	0	0	0	wIntExcept.	1	EXCODEINT
SYS	0	0	0	wNotExclLvl.	0	EXCODESYS
SLL/SRL/SRA	0	0	0	wIntExcept.	0	EXCODEINT
MFHI/MFLO	0	0	0	wIntExcept.	0	EXCODEINT
MTHI/MTLO	0	0	0	wIntExcept.	0	EXCODEINT
MUT/DIV	0	0	0	wIntExcept.	0	EXCODEINT
MUTU/DIVU	0	0	0	wIntExcept.	0	EXCODEINT
ADDU/SUBU	0	0	0	wIntExcept.	0	EXCODEINT
AND/OR	0	0	0	wIntExcept.	0	EXCODEINT
XNOR/NOR	0	0	0	wIntExcept.	0	EXCODEINT
SLT/SLTU	0	0	0	wIntExcept.	0	EXCODEINT
SLLV/SRLV	0	0	0	wIntExcept.	0	EXCODEINT
SRAV	0	0	0	wIntExcept.	0	EXCODEINT
JMP	0	0	0	wIntExcept.	1	EXCODEINT
JAL	0	0	0	wIntExcept.	1	EXCODEINT
ADDI	0	0	0	wALUExcept.	0	wALUExccod.
ADDIU	0	0	0	wIntExcept.	0	EXCODEINT
SLTI/SLTIU	0	0	0	wIntExcept.	0	EXCODEINT
ANDI	0	0	0	wIntExcept.	0	EXCODEINT
XORI/ORI	0	0	0	wIntExcept.	0	EXCODEINT
LUI	0	0	0	wIntExcept.	0	EXCODEINT
MTC	0	0	0	wIntExcept.	0	EXCODEINT
MFC	0	0	0	wIntExcept.	0	EXCODEINT
BC1-0	0	0	0	wIntExcept.	1	EXCODEINT
BC1-1	0	0	0	wIntExcept.	1	EXCODEINT
ADDS/SUBS	0	0	0	wFPALUExcpt.	0	wFPALUEcd.

MULS/DIVS	0	0	0	wFPALUExcpt.	0	wFPALUEcd.
CVTSW	0	0	0	wFPALUExcpt.	0	wFPALUEcd.
SQRT	0	0	0	wIntExcept.	0	EXCODEINT
ABS/NEG	0	0	0	wIntExcept.	0	EXCODEINT
CVTWS	0	0	0	*	0	**
CEILWS	0	0	0	*	0	**
FLOORWS	0	0	0	*	0	**
ROUNDWS	0	0	0	*	0	**
CEQ/CLT/CLE	0	0	0	wIntExcept.	0	EXCODEINT
MOV	0	0	0	wIntExcept.	0	EXCODEINT
SWC1	0	0	0	wIntExcept.	0	EXCODEINT
LWC1	0	0	0	wIntExcept.	0	EXCODEINT
BGEZ	0	0	0	wIntExcept.	1	EXCODEINT
BGEZAL	0	0	0	wIntExcept.	1	EXCODEINT
BLTZ	0	0	0	wIntExcept.	1	EXCODEINT
BLTZAL	0	0	0	wIntExcept.	1	EXCODEINT
BLEZ	0	0	0	wIntExcept.	1	EXCODEINT
BGTZ	0	0	0	wIntExcept.	1	EXCODEINT
MFC	0	0	0	iUserMode	0	EXCODEINST
MTC	0	***	0	iUserMode	0	EXCODEINST
ERET	0	0	***	iUserMode	0	EXCODEINST

Table 3: Tabela verdade das operações da ISA.

1 2 3

Exercício 8. Teste do funcionamento das instruções da ISA

Exercício 9. Novas instruções usando a ISA MIPS

References

¹* - (*iFPALUOverflow* || *wInterruptNotZero*) AND *wNotExcLevel*

²** - *iFPALUOverflow* ? EXCODEFPALU : EXCODEINT

³*** - *wNotUserMode*