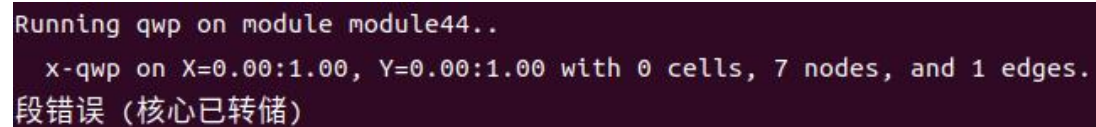


## Memory overflow during the layout process leading to Yosys crash

My Yosys command is as follows:

```
yosys -p "  
read_verilog rtl.v  
hierarchy  
proc;  
opt;  
opt_expr -undriven; opt_clean; opt_share; opt_reduce;  
fsm;  
opt_clean; opt_reduce;  
memory;  
opt_mem;  
opt;  
abc;  
qwp -ltr;  
write_verilog syn_yosys.v"
```

I am using Yosys to read an RTL code file and perform some optimization operations with "opt". Then, I use "techmap" to map gate-level netlist to target technology library cells and perform layout with "qwp -ltr". However, during the execution, it seems that there is a memory overflow issue, which leads to a crash of Yosys (as shown in the screenshot below).



```
Running qwp on module module44..  
x-qwp on X=0.00:1.00, Y=0.00:1.00 with 0 cells, 7 nodes, and 1 edges.  
段错误 (核心已转储)
```