

### Signal and Expression Concatenation Errors During Synthesis

I encountered an inconsistency issue while using Vivado in non-project mode. My system is Linux, and the Vivado version is 2023.1. In Vivado non-project mode, during synthesis, I made some parameter changes instead of using Vivado's default settings. Specifically, I used the following synthesis command: 'synth\_design -top top -flatten\_hierarchy none -bufg 6 -directive AlternateRoutability -fsm\_extraction auto -resource\_sharing auto -control\_set\_opt\_threshold 1 -shreg\_min\_size 8 -max\_bram\_cascade\_height -1 -max\_uram\_cascade\_height -1 -cascade\_dsp force -incremental\_mode aggressive -retiming -no\_lc'. These parameter adjustments were aimed at achieving resource sharing and optimization without affecting code consistency.

However, during synthesis, I encountered signal and expression concatenation errors, leading to issues during the assignment phase of 'reg84' (line 1129 in the attached rtl.v). This subsequently affected the consistency of simulation output. To better reproduce the problem and identify the root cause, I plan to document my steps in detail:

vivado.tcl and new\_vivado.tcl are script files for synthesis and simulation using default and modified synthesis parameters, respectively.

In the Linux system, open a new terminal and enter 'vivado -mode batch -source vivado.tcl' for default synthesis parameters and 'vivado -mode batch -source new\_vivado.tcl' for modified synthesis parameters.

Directly observing the terminal output reveals inconsistency in the middle portion of the fifth line of the simulation results (the simulation results are in binary, and I intended to print them in hexadecimal in no-project mode. However, I did not find the corresponding command. To facilitate the comparison of different sections, I marked them with red boxes in the image). The values are '000000000' and '111111111,' as shown in the terminal display in the following figure:

[illegible]

Figure 1: Before Modification

