Specific Configuration of the control_set_opt_threshold and Other Comprehensive Parameters Resulted in Inversion Operation Error

I encountered an inconsistency while using Vivado in non-project mode. Here are the details: My system is Linux, and I'm using Vivado version 2023.1. While working in non-project mode, during synthesis, I opted for a non-default synthesis flow and adjusted various synthesis settings. Specifically, I used the following synthesis command: "synth design -top top -flatten hierarchy none -gated clock conversion -bufg 14 -directive Area Map Large Shift Reg To BRAM-fsm extraction -resource sharing grav -control set opt threshold 12 -shreg min size 6 -cascade dsp -max bram tree

The intention was to enhance synthesis efficiency by utilizing the quick incremental mode. However, these changes should not affect code consistency. Nevertheless, after synthesis, an error occurred in the inversion operation, impacting the assignment of reg41 (line 566 in the attached rtl.v file). This issue subsequently led to signal inconsistencies observed during simulation.

-incremental mode quick -no srlextract -no lc -assert".

To accurately reproduce and pinpoint the root cause of this problem, I decided to provide a more detailed description of the steps I executed:

- 1. The files vivado.tcl and new_vivado.tcl are scripts used for synthesis and simulation with default and modified synthesis parameters, respectively.
- 2. The testbench.v file references files like cells_cmos.v and cells_cyclone_v.v, which I have attached.
- 3.I opened a terminal on the Linux system and executed the commands "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new vivado.tcl".

By executing the above commands directly in the terminal, it's evident that there's a discrepancy in the middle portion of the simulation result's fourth line, with "0100" and "0000" appearing differently. The terminal output is shown in the screenshot below:



Figure 1: Before Modification

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01100110
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Figure 2: After Modification