Inconsistent Simulation Results Due to Logic Synthesis Optimization Issue

I encountered an inconsistency issue while using Vivado in non-project mode. My system is Linux, and the Vivado version is 2023.1.

In Vivado non-project mode, during synthesis, I made some changes to the parameters instead of using Vivado's default settings. Specifically, I used the following command:

"synth_design -top top -flatten_hierarchy none -gated_clock_conversion on -bufg 15 -directive AreaMapLargeShiftRegToBRAM -fsm_extraction sequential -resource_sharing auto -control_set_opt_threshold 33 -shreg_min_size 50 -max_bram 17 -max_uram 28 -max_bram_cascade_height 2 -max_uram_cascade_height 34 -cascade_dsp auto -incremental_mode off -assert -retiming -no_lc".

During the synthesis process, the simulation results showed inconsistency due to the synthesis parameters. To better reproduce the issue and identify the root cause, I plan to document my steps in detail.

vivado.tcl and new_vivado.tcl are script files used for synthesis and simulation with default synthesis parameters and modified synthesis parameters, respectively.

1.In a Linux terminal, I executed "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new_vivado.tcl".

2.By directly observing the terminal output, you can see that the simulation results on lines 19 and 20 are inconsistent (highlighted in red boxes in the images), displaying "40" and "60" respectively. The terminal output is as shown in the attached image.

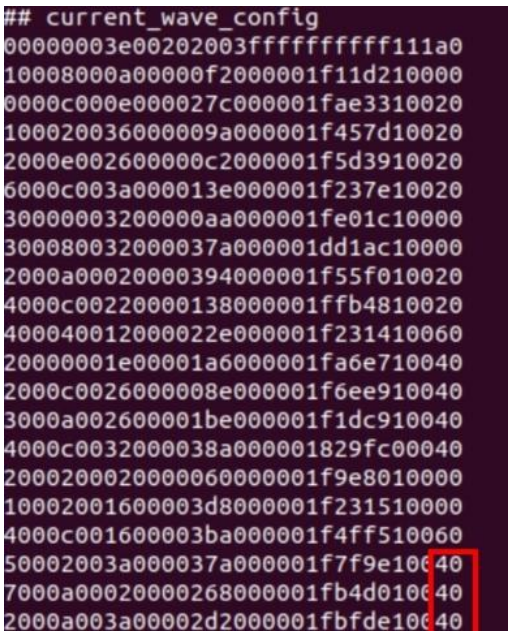

Figure 1: Synthesis with Default Parameters

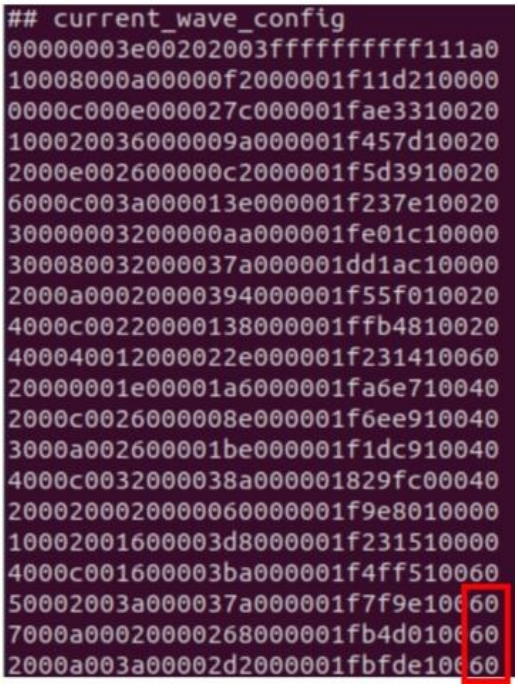

Figure 2:Modified some Parameter Values