Shift Operation Error Occurs in the Synthesis Process

I encountered an inconsistency issue while using Vivado in non-project mode:

My system is Linux, and the Vivado version is 2023.1.

In Vivado non-project mode, I did not follow Vivado's default synthesis flow. I adjusted a series of synthesis setting parameters as follows: "synth_design -top top -flatten_hierarchy rebuilt -directive AreaOptimized_medium -fsm_extraction gray -resource_sharing off -control_set_opt_threshold 10 -shreg_min_size 10 -max_bram -1 -max_uram -1 -cascade_dsp force -incremental_mode aggressive -retiming -no_srlextract". My goal was to achieve a better balance between resource utilization and performance through customizing these parameters, but these changes should not affect the consistency of the code. However, during synthesis, there was an issue with shift operations. Specifically, an error occurred during the assignment to reg205 (please refer to the attached rtl.v file, located at line 1230). This error further led to inconsistency in the output signals during simulation.

To better reproduce the problem and identify the root cause, I will describe my operation steps in detail.

1.vivado.tcl and new_vivado.tcl are script files for synthesis and simulation using default synthesis parameters and modified synthesis parameters, respectively.

2.testbench.v references files such as cells_cmos.v and cells_cyclone_v.v, which I have attached.

3.On a Linux system, I opened a terminal and entered "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new_vivado.tcl".

4.You can directly observe the inconsistency in the middle part of the 4th line of the simulation result. They are "0000" and "0100" respectively. The terminal display is as shown in the attached image：

Figure 1: Before Modification

Figure 2: After Modification