Inconsistency Issue Arising from Interactions of Parameters like max_bram and max_uram

I encountered an inconsistency issue while using Vivado in non-project mode. My system environment is Linux, and I'm using Vivado version 2023.1.

During synthesis, I selected non-default synthesis settings with the following specific parameters: "synth_design -top top -flatten_hierarchy full -gated_clock_conversion on -bufg 8 -fsm_extraction one_hot -resource_sharing auto -control_set_opt_threshold 2 -shreg_min_size 2 -max_bram_cascade_height 2 -max_uram_cascade_height 1 -cascade_dsp force -incremental_mode aggressive -retiming -assert". I intended to achieve better optimization and resource sharing by adjusting these parameters, but these changes shouldn't impact the code's consistency.

However, after synthesis completion, I discovered an error in a ternary operation. The issue specifically arose during the assignment to 'reg129' (please refer to the rtl.v file in the attached files, line 432). This problem further led to inconsistencies in the output signals during simulation.

To more accurately reproduce the problem I encountered and identify the root cause, I plan to provide more detailed steps:

1."vivado.tcl" and "new_vivado.tcl" are script files for synthesis and simulation using default synthesis parameters and modified synthesis parameters, respectively.("testbench.v" references files like "cells_cmos.v" and "cells_cyclone_v.v," which I have attached.)

2.In a Linux terminal, I will enter the commands "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new_vivado.tcl."

By running these commands directly in the terminal, it's apparent that the initial parts of the second and third lines of the simulation result are inconsistent. They are "00000" and "00001," respectively. The terminal display is shown in the following image:

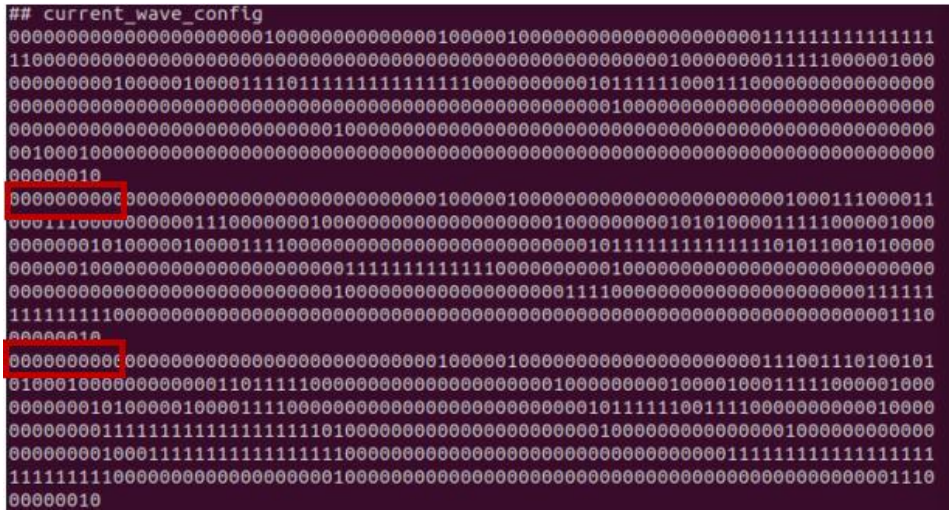

Figure 1: Before Modification

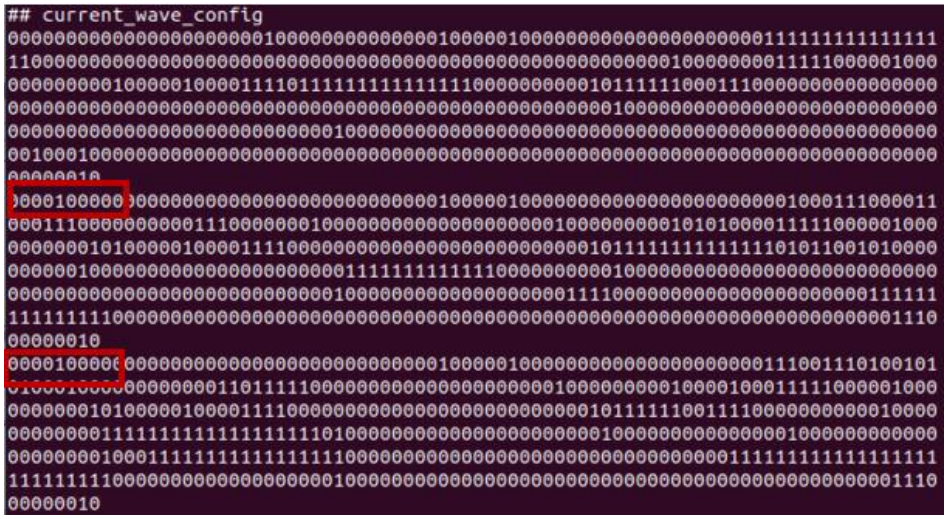

Figure 2: After Modification