Inconsistency Issue with Comprehensive Parameter shreg_min_size Leading to Errors in Post-Synthesis Simulation Results

I encountered an inconsistency issue during the usage of Vivado in non-project mode. My system is Linux, and the Vivado version is 2023.1. In non-project mode, while synthesizing, I made some parameter changes instead of using Vivado's default settings. Specifically, I used the following synthesis command: 'synth_design -top top -gated_clock_conversion on -bufg 19 -directive RuntimeOptimized -fsm_extraction one_hot -resource_sharing off -shreg_min_size 13'.

By adjusting these parameters, I aimed to find a better balance between resource utilization and performance without affecting code consistency. However, during synthesis, due to the influence of the synthesis parameter 'shreg_min_size,' inconsistencies appeared in the simulation results. The inconsistency has been traced back to the 'shreg_min_size' parameter. If this parameter is removed from the command, simulation results show consistency.

To better reproduce the issue and identify the root cause, I plan to document my steps as follows:

1.vivado.tcl and new_vivado.tcl are script files for synthesis and simulation using default and modified synthesis parameters, respectively.

2.In the Linux system, open a new terminal and enter 'vivado -mode batch -source vivado.tcl' for default synthesis parameters and 'vivado -mode batch -source new_vivado.tcl' for modified synthesis parameters.

Directly observing the terminal output reveals inconsistency in the end portion of the simulation results' fifth line, displaying '1110010' and '1110011' respectively. The terminal output is as shown in the following figure:

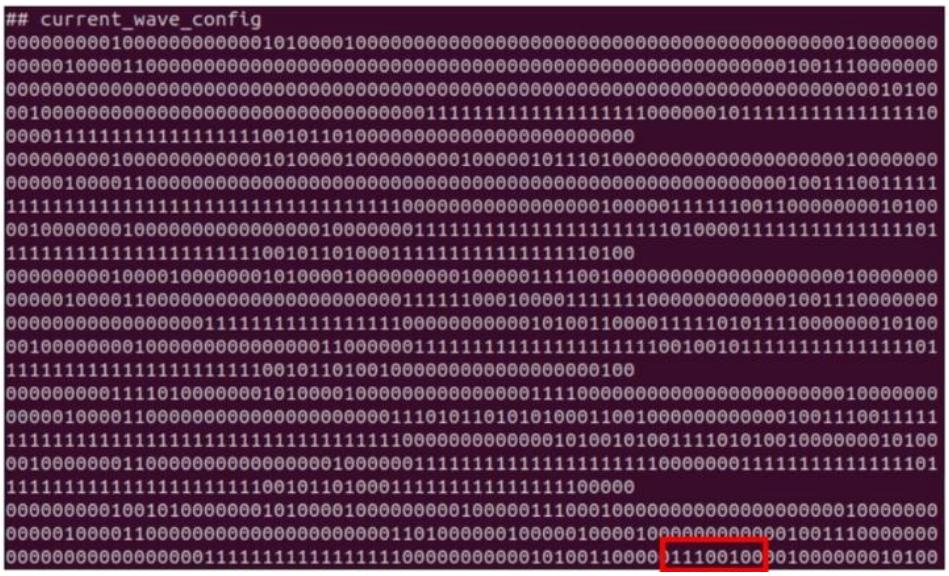

Figure 1: Before Modification

Figure 2: After Modification