Synthesis optimization error, inconsistent simulation results

I have come across an inconsistency problem during the synthesis process while using Yosys:
Version: Icarus Verilog version 13.0, Yosys 0.30+48

In our synthesis flow, we have deviated from using Yosys's default synthesis process and have incorporated additional optimization steps aimed at enhancing the performance, area efficiency, and other key metrics of our design. However, these changes should not affect the consistency of the code.

The two synthesis processes are as follows:

1.Using Yosys's default synthesis process:
read_verilog rtl.v
synth
write_verilog syn_yosys.v

2.Customized synthesis process:
read_verilog rtl.v
hierarchy;
flatten;
proc -norom;
proc -noopt;
fsm_extract; opt_share; opt_reduce; wreduce; opt_mem_feedback; opt_dff -keepdc; opt_dff -sat; opt_reduce -full; opt_clean; opt_expr -mux_bool; opt_dff -nodffe; opt_expr -keepdc; opt_dff -nodffe; opt_reduce -fine; opt_expr; opt_expr -fine;
techmap;
abc;
write_verilog syn_yosys.v

After obtaining synthesis files from both of the above processes, I performed simulation verification using the Iverilog simulator. However, I observed inconsistencies in the output signals during simulation, as highlighted in the red-boxed section in the image below. Displaying "00000" and "10111" respectively. The terminal output is as shown in the attached image.

Default synthesis process，the third line of output is:

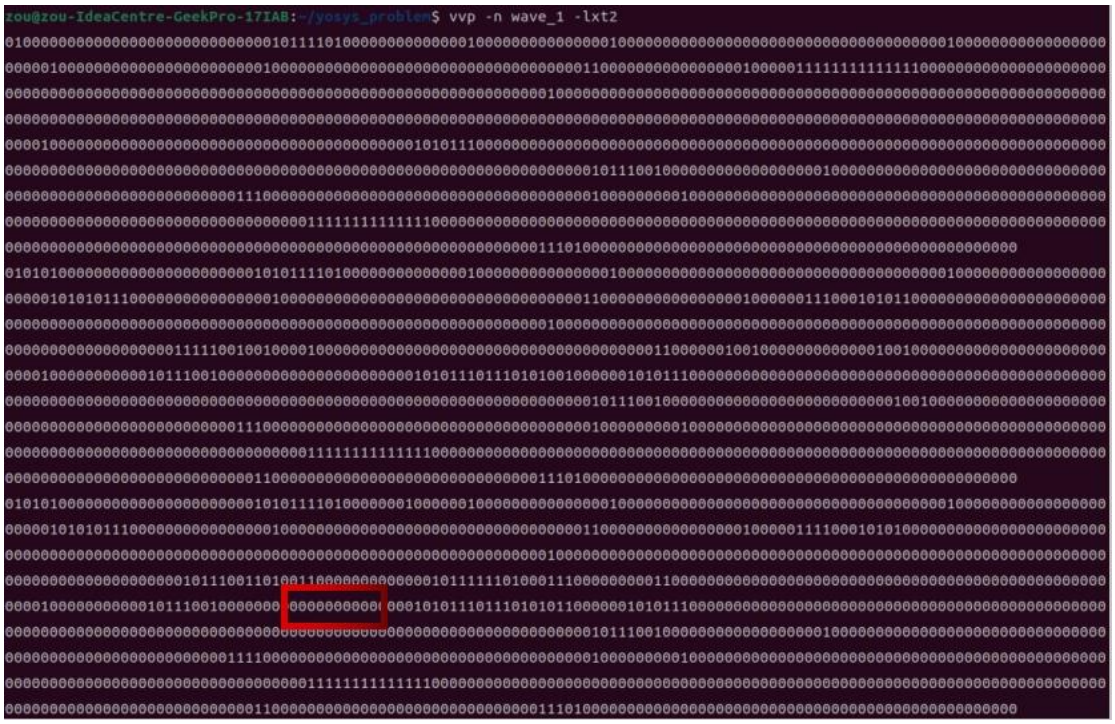

Figure 1: Before Modification

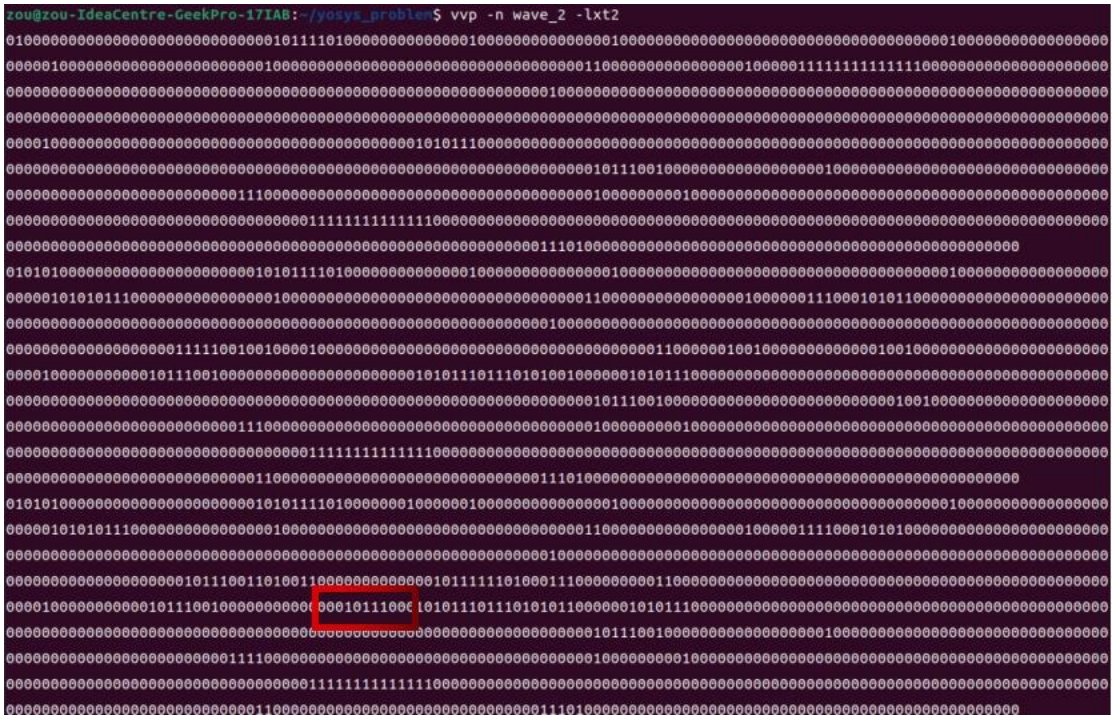

Figure 2: After Modification