Inconsistency Issue in Synthesis and Simulation Results after Custom Synthesis Flow with fsm -norecodec and opt_expr -fine Pass in Yosys

I encountered an inconsistency issue during the Yosys synthesis process. My versions are Icarus Verilog version 13.0 and Yosys version 0.30+48.

In our synthesis flow, we opted for a custom synthesis process instead of using Yosys' default synthesis flow. Initially, we used the fsm -norecodec command to optimize the state machine by removing state register encoding and optimizing the logic part of the state machine to reduce the number of logic gates and delays.

Next, we applied the opt_expr -fine command for expression-level optimization. During this step, we performed deeper optimizations on the logic expressions in the gate-level netlist to further reduce the gate-level netlist's size and delay. With this custom synthesis flow, we expected to achieve higher-quality synthesis results, particularly in terms of optimizing the state machine and logic expressions, leading to better performance and resource utilization.

However, these changes should not affect the consistency of the code.

The two synthesis processes are as follows:

1、Using Yosys' default synthesis process：

```
read_verilog rtl.v
synth
write_verilog syn_yosys.v
```

2、After FSM optimization, using the opt_expr -fine pass， the synthesis process is as follows：

```
read_verilog rtl.v
hierarchy
proc;
opt_clean; opt_reduce; opt_share; opt_expr; opt_merge; opt_clean -purge; opt_dff;
fsm;
opt_expr -fine; opt_clean; opt_reduce; opt_clean;
memory;
abc;
opt_reduce; opt_clean;
write_verilog new_syn_yosys.vv
```

We obtained the synthesis files from both of the above processes and conducted simulations using the Iverilog simulator for verification. During simulation, we observed inconsistencies in the output signals (as indicated by the red boxes in the image below).

Default synthesis process，the first line of output is：

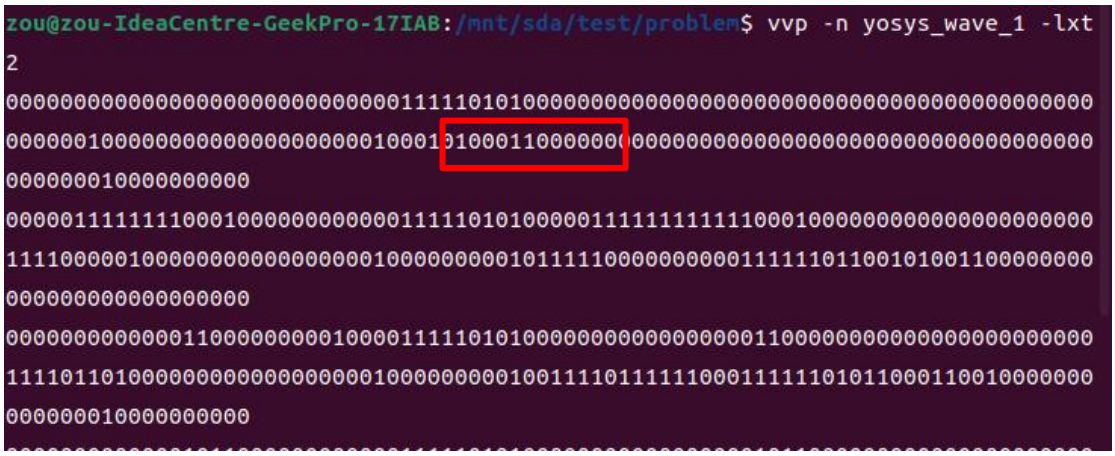

Figure 1: Before Modification

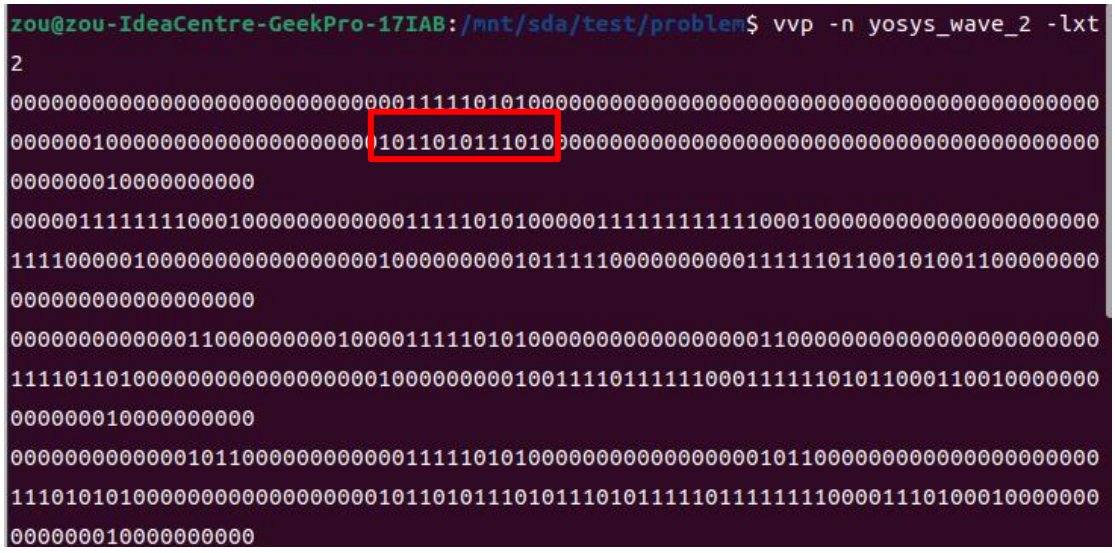

Figure 2: After Modification