Assignment Operation Error Leading to Inconsistent Simulation Results

I encountered an inconsistency issue while using Vivado in non-project mode. My system is Linux, and the Vivado version is 2023.1.

During synthesis in Vivado non-project mode, I selected parameter settings different from Vivado's default synthesis process. Specifically, I used the following parameters: 'synth_design -top top -bufg 22 -directive AreaMultThresholdDSP -fsm_extraction gray -resource_sharing on -control_set_opt_threshold 7 -shreg_min_size 10 -max_bram 10 -max_uram 4 -max_dsp 18 -max_bram_cascade_height 10 -max_uram_cascade_height 10 -cascade_dsp force -incremental_mode aggressive -retiming -keep_equivalent_registers -assert -no_srlextract -no_lc'. The modifications to these parameters were intended to improve design performance but should not affect code consistency.

However, after synthesis, an assignment operation error occurred, affecting the assignment of certain wires within module9 (see line 361 and onward in the attached rtl.v). This resulted in consistency issues in the simulation output signals.

To better replicate and analyze the root cause of the problem, I will provide more detailed steps:

1.vivado.tcl and new_vivado.tcl are script files for synthesis and simulation using default and modified synthesis parameters, respectively. (testbench.v references files such as cells_cmos.v, cells_cyclone_v.v, etc., which I have attached.)

2.In the Linux system, open a new terminal and enter 'vivado -mode batch -source vivado.tcl' for default synthesis parameters and 'vivado -mode batch -source new_vivado.tcl' for modified synthesis parameters.

Directly observing the terminal output reveals inconsistency in the middle portion of the second line of the simulation results, with values '0100' and '0000' respectively, as shown in the terminal display in the following figure:

Figure 1: Before Modification

Figure 2: After Modification