

The parameter "flatten_hierarchy" during logic synthesis leads to incorrect simulation results

In using Vivado's non-project mode, I encountered an inconsistency issue. My operating system is Linux, and the Vivado version is 2023.1.

Under Vivado's non-project mode, I made modifications to certain parameters rather than using Vivado's default settings. Specifically, I utilized the following command for synthesis:

```

“synth_design -top top -flatten_hierarchy none -gated_clock_conversion auto -bufg 16 -directive
Default -fsm_extraction off -resource_sharing off -control_set_opt_threshold 47 -shreg_min_size 24
-max_bram 14 -max_uram 11 -max_dsp 33 -max_bram_cascade_height 20 -max_uram_cascade_height 1
-cascade dsp force -incremental_mode off -no_lc -retiming -assert-keep equivalent_registers”.

```

The adjustment of these parameters was intended to achieve resource sharing and optimization. However, contrary to my expectations, these changes should not impact the code's consistency. Yet, during synthesis, due to the influence of the synthesis parameter `flatten_hierarchy`, I observed consistency issues in the simulation results. I have confirmed that this problem is caused by the `flatten_hierarchy` parameter. If `flatten_hierarchy` is removed from the command, the consistency issue does not occur.

To better reproduce the problem and identify its root cause, I plan to meticulously document my steps:

1.vivado.tcl and new_vivado.tcl are scripts for synthesis and simulation with default and modified synthesis parameters, respectively.

2. In a new terminal under the Linux system, I will input the commands "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new_vivado.tcl".

Directly in the terminal, it is evident that there is inconsistency in the simulation results, specifically in lines 3 to 5, where values are "400" and "000" respectively. I have marked these inconsistencies with red boxes in the terminal display, as shown in the attached image:

```
## current_wave_conrlg  
00000000000000000000000080000000000010000000000800000000000000000010002080f  
4000001000000020002a0000000000000000000000000000ff5100000  
00000000000020007ffffffe  
0000000000000067ffffffd000fff40000000010000000000800000003fffc0000008002080f  
4000001000000020002a0fffe00000000000000000000000000000000000000000000000000000  
000000000000004023ffc8e  
0000000000000008028000000000fff400000000000000000800000003fffc00003ff002080f  
4000001000000020002a0008e00000000000000000000000000000000000000000000200000f  
0000000000000000005b7fd6c  
00000000000000080280000000fff4000000000000000000800000003fffc0000230002080f  
4000001000000020002a0016c000000200002a0016c0000000000000000000000000300000f  
000000000000000003fac7feb0  
00000000000000080280000000fff4000000000000000000800000003fffc00005b8002080f  
4000001000000020002a0feb0000000000000000000000000000000000000000300000f  
0000000000000000005cdfd72  
00000000000000080280000000fff4000000000000000000800000003fffc00003ac8002080f  
4000001000000020002a001720000000000000000000000000000000000000000200000f  
0000000000002000405d7fd74  
00000000000000080280000000fff800000001000000000800000003fffc00005c0002080f  
4000001000000020002a001740000000000000000000000000000000000000000100000f  
000000000000200040737fdc  
00000000000000080280000000fff40000000010000000000800000003fffc00005d8002080f  
4000001000000020002a001cc00000000000000000000000000000000000000000100000f
```

Figure 1: Before Modification

