Incorrect Functionality of unsigned() System Function Due to Selection of Synthesis Parameters such as bufg

I have encountered an inconsistency issue while using Vivado in non-project mode on Linux with version 2022.2. After modifying certain parameters in the synthesis settings using the 'synth_design' command, specifically, 'synth_design -top top -flatten_hierarchy none -gated_clock_conversion off -bufg 10 -directive AlternateRoutability -fsm_extraction sequential -resource_sharing on', we intended to improve the code optimization efficiency through these parameter modifications. However, these changes should not affect the code consistency. Nevertheless, after synthesis, we observed errors in the functionality of functions like 'unsigned,' which led to an error during assignment to 'wire145' (line 227 in the attached 'rtl.v' file). Consequently, this inconsistency resulted in discrepancies in the output signals during simulation (line 9 in the simulation results), as shown in the attached image：

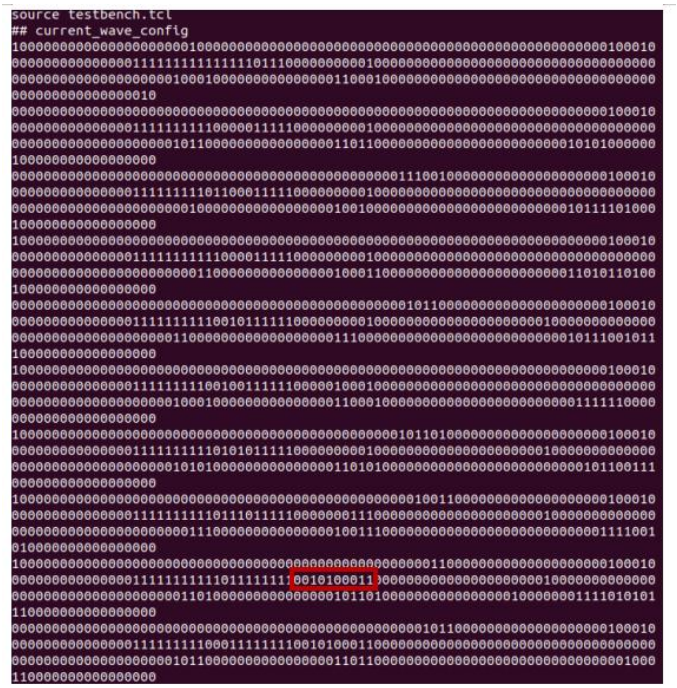

Figure 1: Before Modification

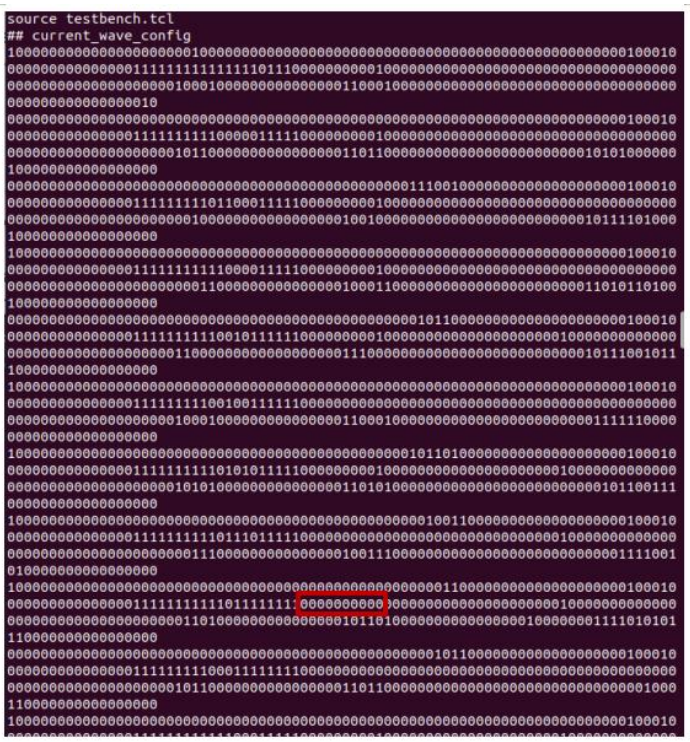

Figure 2: After Modification