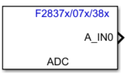
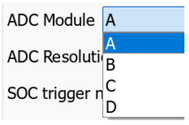
In this laboratory, the ADC is used only as a 12-bit single-ended ADC.
The input voltage range is 0–3 V, corresponding to a digital output range from 0 to 4095.





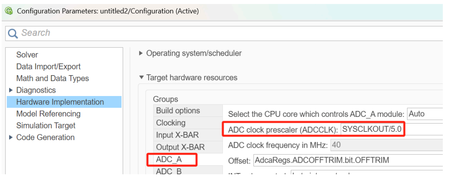
There are four modules available: A, B, C, and D. These four modules independently perform sampling according to their own SOC sequences (with 0 being the earliest and higher numbers sampled later). Therefore, with proper design, channels of the same priority across the four modules can be sampled synchronously.

SOC trigger numbers: Each module has sixteen options numbered 0 to 15. In Round-Robin mode, all SOCs have equal priority but are executed sequentially in a circular manner, first from 0 to 15, then from 15 back down to 0, and so on.

SOC acquisition window: The number of ADCCLK cycles allowed for the ADC to complete sampling.

min. SOC acquisition window = min. sampling time * ADCCLK -1

ADCCLK can be set in the model configuration. For example, in the picture below, it's 200 MHz/5 = 40 MHz.



while min. sampling time can be estimated using the following equation: 9 x (Rs x 3.5pF), where Rs is the output equivalent resistance of the signal source, the higher, the slower.

Example: With ADCCLK = 40 MHz and a minimum sampling time of 150 ns, at least 5 ADCCLK cycles are required. Setting the acquisition window to 15 is a more conservative choice and can accommodate most signal sources.

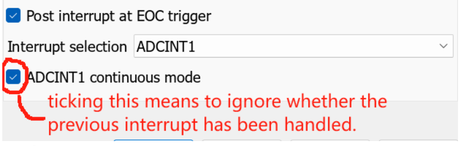
Impact of Incorrect Settings:

- Too short acquisition window: RC charging is incomplete, resulting in incomplete sampling and reduced accuracy.
- Too long acquisition window: Wastes conversion time and reduces system throughput.

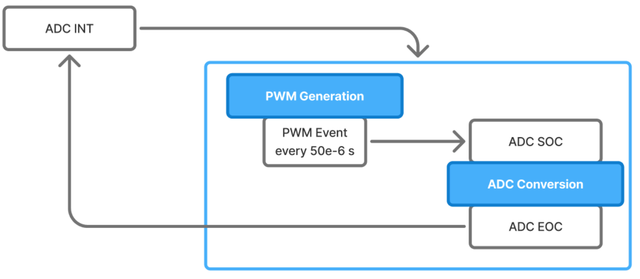
SOC trigger source: to decide when to start the conversion.

- **software**: not scheduled, based on software. a sample time must be set.
- **ePWM**: scheduled based on specific ePWM triggers at fixed times. In the ePWM configuration, the SOC trigger must be enabled and properly set. usually the sampling is done in an ISR, so the sample time needs to be set to -1 to be inherit.

Interrupt at the end of conversion (EOC)



One typical use of the interrupt is as follow:



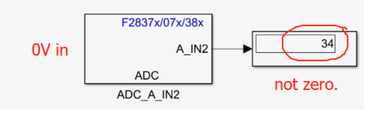
How to achieve synchronous sampling

- Same trigger source
- Same SOC acquisition window
- Same SOC number across different modules

Perform offset calibration through software initialization

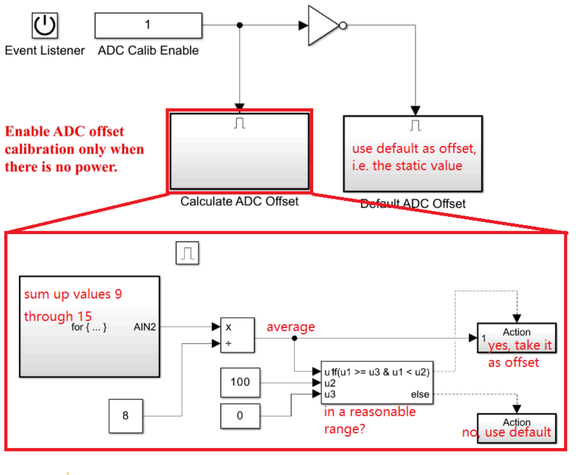
1. static

When the input is 0V, measure and record the digital output as the default value when the dynamic detection condition is not met.

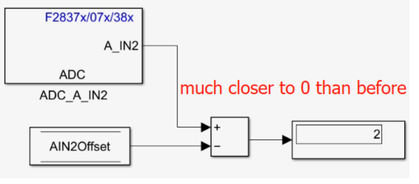


2. dynamic

This occurs **once each time the program is loaded**: discard the first 8 values, calculate the average of values 9 through 15, and if the result is within a reasonable range, update the offset; otherwise, use the default value.



Once the offset is updated, during normal program execution, subtract the ADC value by the offset to obtain a more accurate result.



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