

The time settings of the ePWM block can be configured using either a **clock** or a **time value**, but it is recommended that professional users use the **clock** option to achieve precise control.

F2837x07x004x

ePWM1

Each ePWM block corresponds to one module and can generate two PWM signals: ePWMA and ePWMB, which are typically used to control the upper and lower switches of the same bridge leg.

## 1. switching frequency fs

Before we begin, we need to understand a few configuration parameters:

- EPWMCLK (model configuration)
- TBCLK prescaler divider K1 (ePWM block configuration)
- HSPCLKDIV prescaler divider K2 (ePWM block configuration)

**EPWMCLK** is generated from the 200 MHz system clock, optionally divided by a prescaler. It serves as the base clock for all ePWM modules. By default,  $EPWMCLK = SYSCLKOUT/2 = 100 \text{ MHz}$ .

**K1** and **K2** are further prescaler dividers to slow down EPWMCLK for the final clock **CLK**. By default they are both 1.

$$CLK = EPWMCLK/K1/K2$$

Target hardware resources

Groups

Build options

EPWM clock divider (EPWMCLKDIV): SYSCLKOUT/2 **EPWMCLK**

Time base clock (TBCLK) prescaler divider: 1 **K1**

High speed time base clock (HSPCLKDIV) prescaler divider: 1 **K2**

To correctly and accurately set the switching period (**fsw**) for the PWM, we first choose clock cycles as the unit of time.

Then, select the shape of the carrier waveform: sawtooth wave (up or down) or triangle wave (up-down).

Finally, determine the maximum value of the carrier counter **TBPRD** based on the final PWM clock (**CLK**) and the given switching frequency (**fsw**).

If it is a sawtooth wave carrier, the calculation is as follows:

$$TBPRD = CLK/fsw - 1 = EPWMCLK/K1/K2/fsw - 1$$

If it is a triangle wave carrier, the calculation is as follows:

$$TBPRD = CLK/fsw/2 = EPWMCLK/K1/K2/fsw/2$$

For example, if  $fsw = 20 \text{ kHz}$  and a triangular wave is chosen as the carrier, the following settings can be applied:

Build options

Desired CPU Clock in MHz: 200

Clocking

☐ Use internal oscillator

EPWM clock divider (EPWMCLKDIV): SYSCLKOUT/2

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink TBPRD Not Linked

Timer period units: Clock cycles ☒

Specify timer period via: Specify via dialog

Timer period: 100E6/20E3/2

Active period register load option (PRDL) Counter equals to zero

Counting mode: Up-Down

Synchronization action: Disable

☐ Specify software synchronization via input port (SWFSYNC)

☐ Enable digital compare A event1 synchronization (DCAEVT1)

☐ Enable digital compare B event1 synchronization (DCBEVT1)

Synchronization output (SYNCO): Disable

Peripheral synchronization event (PWMSYNCSSEL): Counter equals to period (CTR=PRD)

Time base clock (TBCLK) prescaler divider: 1 ☒

High speed time base clock (HSPCLKDIV) prescaler divider: 1 ☒

☐ Enable swap module A and B

20 kHz

For example, if  $fsw = 20 \text{ kHz}$  and a sawtooth wave is chosen as the carrier, the following settings can be applied:

Build options

Desired CPU Clock in MHz: 200

Clocking

☐ Use internal oscillator

EPWM clock divider (EPWMCLKDIV): SYSCLKOUT/1

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink TBPRD Not Linked

Timer period units: Clock cycles ☒

Specify timer period via: Specify via dialog

Timer period: 200E6/20E3-1

Active period register load option (PRDL) Counter equals to zero

Counting mode: Up ☒

Synchronization action: Disable

☐ Specify software synchronization via input port (SWFSYNC)

☐ Enable digital compare A event1 synchronization (DCAEVT1)

☐ Enable digital compare B event1 synchronization (DCBEVT1)

Synchronization output (SYNCO): Disable

Peripheral synchronization event (PWMSYNCSSEL): Counter equals to period (CTR=PRD)

Time base clock (TBCLK) prescaler divider: 1 ☒

High speed time base clock (HSPCLKDIV) prescaler divider: 1 ☒

☐ Enable swap module A and B

## 2. duty cycle

The following are common settings for **triangle carrier** duty cycle control:

- When the duty cycle (comparator value) changes, the change will be updated when the carrier is at zero;
- when the comparator value meets the rising slope of the carrier, the output is pulled low;
- when the comparator value meets the falling slope of the carrier, the output is pulled high;
- no action is taken at other times.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink TBPRD Not Linked

Timer period units: Clock cycles

Specify timer period via: Specify via dialog

Timer period: 100E6/20E3/2

Active period register load option (PRDL) Counter equals to zero ☒

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink CMPA Not Linked

CMPA units: Clock cycles ☒

Specify CMPA via: Input port

CMPA initial value: 0

Reload for compare A Register (SHDWAMODE): Counter equals to zero (CTR=Zero) ☒

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1A

Action when counter=ZERO: Do nothing

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Clear ☒

Action when counter=CMPA on down-count (CAD): Set ☒

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

Diagram showing a triangle carrier and a comparator block (K-) with inputs 0.4 and [0,1], outputting to WA and ePWM1.

Diagram showing a triangle carrier and a comparator block (K-) with inputs 0.4 and [0,1], outputting to WA and ePWM1.

The following are common settings for **sawtooth carrier (rising)** duty cycle control:

- When the duty cycle (comparator value) changes, the change will be updated when the carrier is at zero;
- when the carrier is back to 0, the output is pulled high;
- when the comparator value meets the rising slope of the carrier, the output is pulled low;
- no action is taken at other times.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink TBPRD Not Linked

Timer period units: Clock cycles

Specify timer period via: Specify via dialog

Timer period: 100E6/20E3-1

Active period register load option (PRDL) Counter equals to zero ☒

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

ePWMLink CMPA Not Linked

CMPA units: Clock cycles ☒

Specify CMPA via: Input port

CMPA initial value: 0

Reload for compare A Register (SHDWAMODE): Counter equals to zero (CTR=Zero) ☒

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM. The number of available ePWM modules vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1A

Action when counter=ZERO: Set ☒

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Clear ☒

Action when counter=CMPB on up-count (CBU): Do nothing

Diagram showing a sawtooth carrier and a comparator block (K-) with inputs 0.4 and [0,1], outputting to WA and ePWM1.

Diagram showing a sawtooth carrier and a comparator block (K-) with inputs 0.4 and [0,1], outputting to WA and ePWM1.

## 3. ePWMA & ePWMB

A PWM module has two outputs, A and B, which can be coupled for complementary control (suitable for the upper and lower switches of the same bridge leg), or decoupled for independent control.

For example, CMPA can be used to control ePWMA and CMPB to control ePWMB, enabling a pair of PWM outputs with the same period but different phase shifts and duty cycles. The carrier is set to triangle wave.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1A

Action when counter=ZERO: Do nothing

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Clear ☒

Action when counter=CMPA on down-count (CAD): Set ☒

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1B

Action when counter=ZERO: Do nothing

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Do nothing

Action when counter=CMPA on down-count (CAD): Do nothing

Action when counter=CMPB on up-count (CBU): Clear ☒

Action when counter=CMPB on down-count (CBD): Set ☒

Diagram showing two comparators (K-) with inputs 0.2 and 0.3, outputting to WA and WB, which are connected to ePWM1.

Diagram showing two comparators (K-) with inputs 0.2 and 0.3, outputting to WA and WB, which are connected to ePWM1.

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

However, in most applications, ePWMA and ePWMB are configured as complementary outputs to drive the high-side and low-side switches of the same half-bridge leg, with dead time insertion to prevent shoot-through. The following example demonstrates one possible configuration of this control method.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1A

Action when counter=ZERO: Do nothing

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Clear

Action when counter=CMPA on down-count (CAD): Set

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1B

Action when counter=ZERO: Do nothing

Action when counter=period (PRD): Do nothing

Action when counter=CMPA on up-count (CAU): Set

Action when counter=CMPA on down-count (CAD): Clear

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Use deadband for ePWM1A

☒ Use deadband for ePWM1B

☐ Enable half-cycle clocking

Deadband polarity: Active high complementary (AHC) ☒

Signal source for falling edge (RED): ePWMxA ☒

Signal source for rising edge (FED): ePWMxB ☒

Deadband period units: Clock cycles ☒

Deadband period source: Specify via dialog

Deadband falling edge (RED) period (0~16383): 100E6/(1/100E6)

Deadband rising edge (FED) period (0~16383): 100E6/(1/100E6)

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

## 4. event and interrupt

ePWMA and ePWMB can each generate events to trigger ADC modules A and B, respectively, and the trigger points can be configured to occur at specific positions within the PWM carrier cycle.

Typically, a single event triggering one ADC SOC is sufficient to initiate the necessary related processing.

Additionally, the ePWM module can also generate interrupts to trigger an ISR (Interrupt Service Routine).

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1A

Number of event for start of conversion A (SOCA) to be generated: First event

Start of conversion for module A event selection: Counter equals to zero (CTR=Zero)

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM1B

Number of event for start of conversion B (SOB) to be generated: First event

Start of conversion for module B event selection: Counter equals to zero (CTR=Zero)

General ePWMA ePWMB Counter Compare Deadband unit

Module: ePWM1

☒ Enable ePWM interrupt

Number of event for interrupt to be generated: First event

Interrupt counter match event condition: Counter equals to zero (CTR=Zero)

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

Diagram showing two complementary PWM signals, ePWMA and ePWMB, with a 1us gap.

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