

The time settings of the ePWM block can be configured using either a **clock** or a **time value**, but it is recommended that professional users use the **clock** option to achieve precise control.

F2837x/07x/004x ePWM1

Each ePWM block corresponds to one module and can generate two PWM signals: ePWMA and ePWMB, which are typically used to control the upper and lower switches of the same bridge leg.

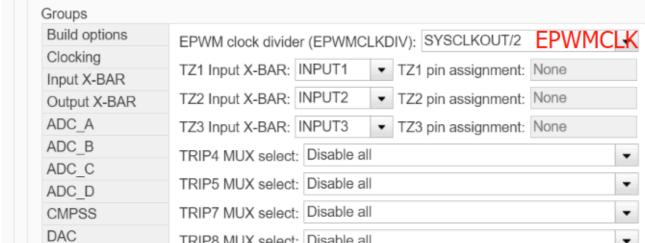
## 1. switching frequency fs

Target hardware resources

- Before we begin, we need to understand a few configuration parameters:
- EPWMCLK (model configuration) TBCLK prescaler divider K1 (ePWM block configuration)
- HSPCLKDIV prescaler divider K2 (ePWM block configuration)
- EPWMCLK is generated from the 200 MHz system clock, optionally divided by a prescaler. It serves as the base clock for all ePWM modules. By default, EPWMCLK = SYSCLKOUT/2 = 100 MHz.

K1 and K2 are futher prescaler dividers to slow down EPWMCLK for the final clock CLK. By default they are both 1.

CLK = EPWMCLK/K1/K2



Time base clock (TBCLK) prescaler divider: 1 High speed time base clock (HSPCLKDIV) prescaler divider: 1

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM)

The number of available ePWM modules vary between C2000 processors.

max. counter value

Active period register load option (PRDLD) Counter equals to zero

Counter Compare

Deadband unit

Block Parameters: ePWM

General

Module: ePWM1

Timer period:

ePWM Type 1-4 (mask) (link)

ePWMLink TBPRD Not Linked

Counting mode: Up-Down

Timer period units: Clock cycles 🗸

Specify timer period via: Specify via dialog

PWM, we first choose clock cycles as the unit of time. Then, select the shape of the carrier waveform: sawtooth wave (up

To correctly and accurately set the switching period (fsw) for the

TRIP8 MUX select: Disable all

\_TRIP9 MUX select: Disable all

or down) or triangle wave (up-down).

Finally, determine the maximum value of the carrier counter TBPRD based on the final PWM clock (CLK) and the given switching

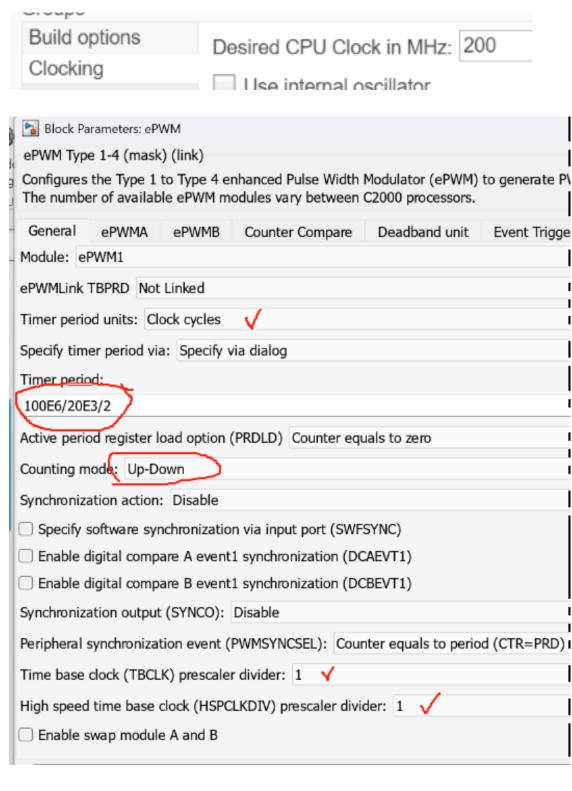
frequency (fsw). If it is a sawtooth wave carrier, the calculation is as follows:

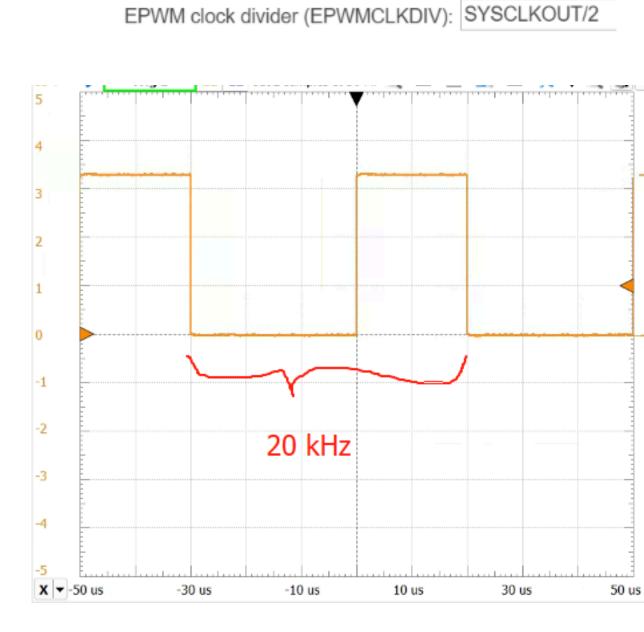
If it is a triangle wave carrier, the calculation is as follows:

TBPRD = CLK/fsw/2 = EPWMCLK/K1/K2/fsw/2

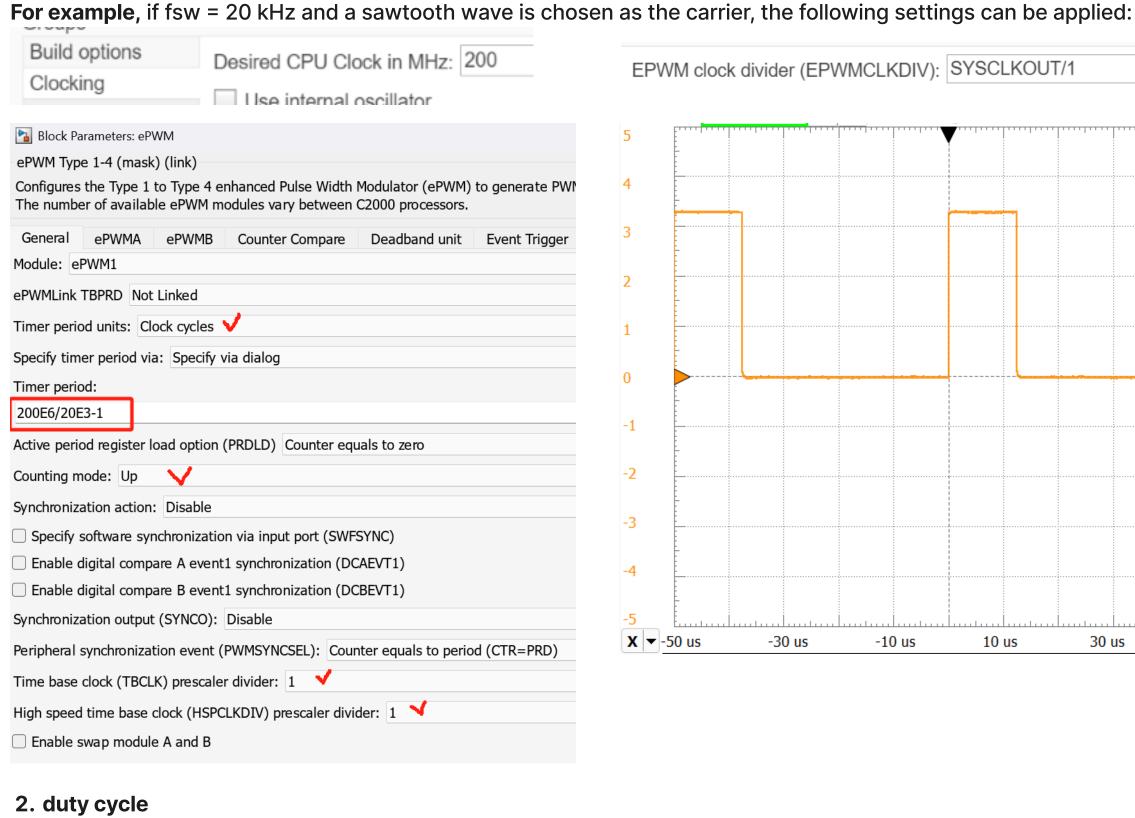
TBPRD = CLK/fsw - 1 = EPWMCLK/K1/K2/fsw - 1

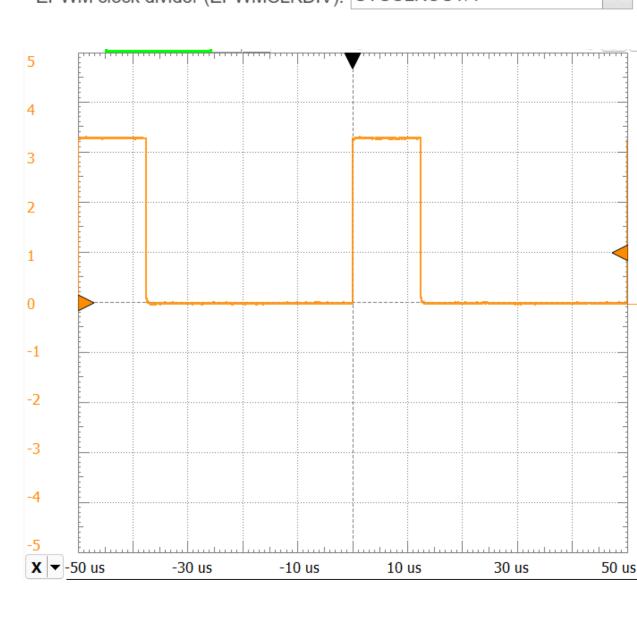
**For example,** if fsw = 20 kHz and a triangular wave is chosen as the carrier, the following settings can be applied:





EPWM clock divider (EPWMCLKDIV): SYSCLKOUT/1 Clocking Use internal oscillator





## When the duty cycle (comparator value) changes, the change will be updated when the carrier is at zero;

ePWMLink TBPRD Not Linked

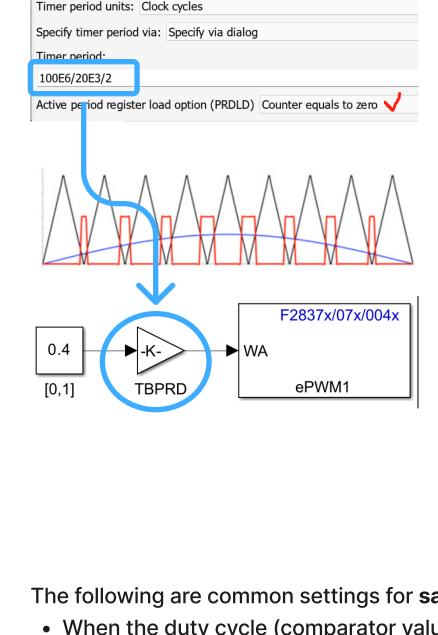
 when the comparator value meets the rising slope of the carrier, the output is pulled low; when the comparator value meets the falling slope of the carrier, the output is pulled high;

The following are common settings for **triangle carrier** duty cycle control:

 no action is taken at other times. General

The number of available ePWM modules vary between C2000 processors.

🚹 Block Parameters: ePWM ePWMA ePWMB Counter Compare Module: ePWM1 ePWM Type 1-4 (mask) (link) Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM v

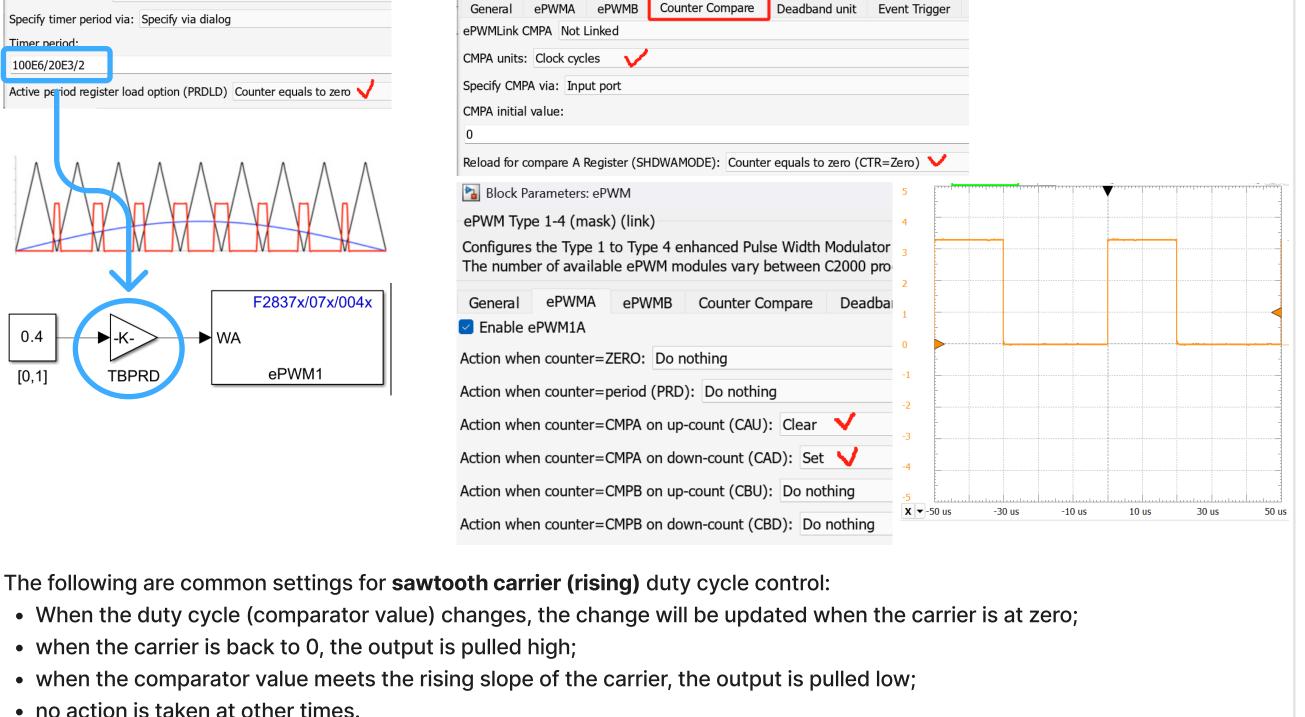


no action is taken at other times.

Specify timer period via: Specify via dialog

Timer period:

100E6/20E3-1



Block Parameters: ePWM ePWMB Counter Compare Deadband unit ePWM Type 1-4 (mask) (link) Module: ePWM1 Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM ePWMLink TBPRD Not Linked The number of available ePWM modules vary between C2000 processors. Timer period units: Clock cycles

General ePWMA ePWMB

ePWMLink CMPA Not Linked

CMPA units: Clock cycles V

Specify CMPA via: Input port

Active period register load option (PRDLD) Counter equals to zero CMPA initial value: Reload for compare A Register (SHDWAMODE): Counter equals to zero (CTR=Zero) source signals Block Parameters: ePWM ePWM Type 1-4 (mask) (link) Configures the Type 1 to Type 4 enhanced Pulse Width Modul The number of available ePWM modules vary between C2000 PWM signal General ePWMA ePWMB Counter Compare Dea Enable ePWM1A Time Action when counter=ZERO: Set F2837x/07x/004x Action when counter=period (PRD): Do nothing 0.4 **▶** WA -K-Action when counter=CMPA on up-count (CAU): Clear ePWM1 [0,1]**TBPRD** Action when counter=CMPB on up-count (CBU): Do nothing 3. ePWMA & ePWMB A PWM module has two outputs, A and B, which can be coupled for complementary control (suitable for the upper and lower switches of the same bridge leg), or decoupled for independent control. For example, CMPA can be used to control ePWMA and CMPB to control ePWMB, enabling a pair of PWM outputs with the same period but different phase shifts and duty cycles. The carrier is set to triangle wave. ePWMA Counter Compare Deadband un General **ePWMA** ePWMB Counter Compare Deadband unit Ev General ePWMB Enable ePWM1B

Counter Compare Deadband unit Event Trigger

Action when counter=ZERO: Do nothing

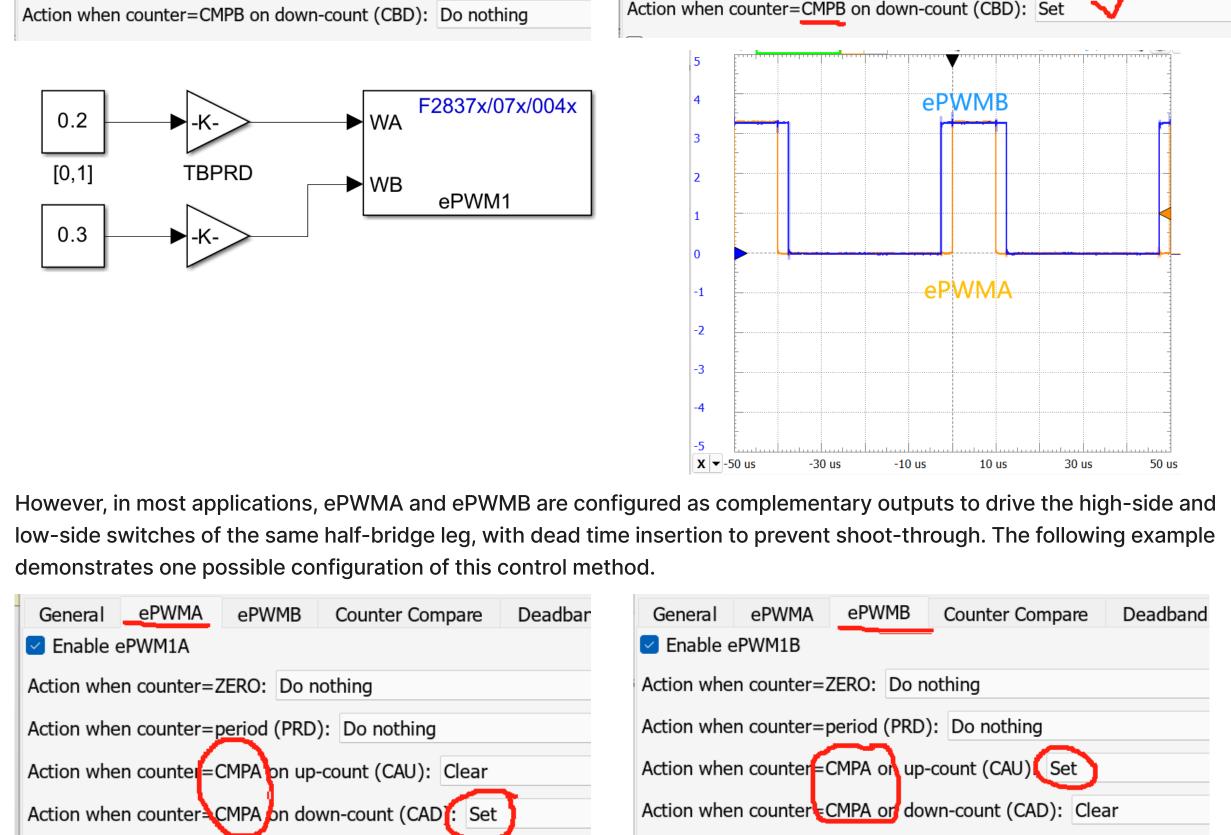
Action when counter=period (PRD): Do nothing

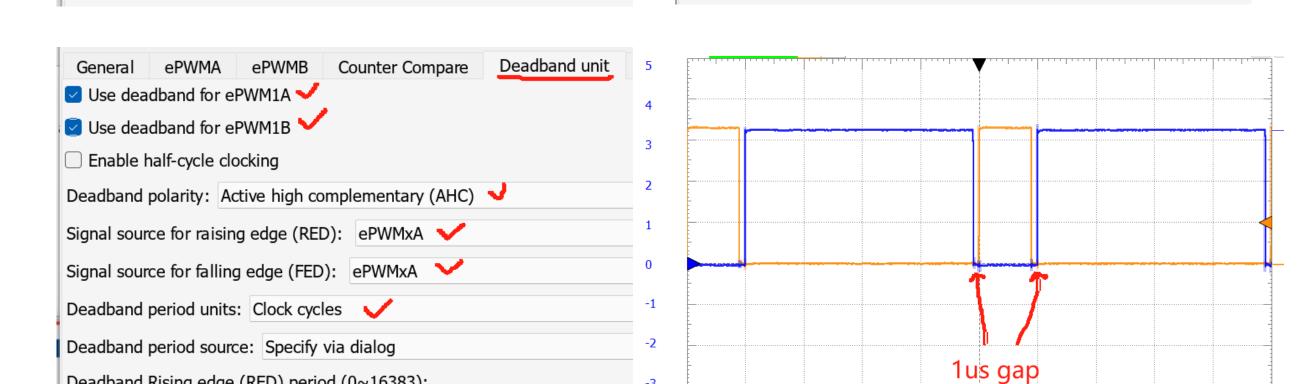
Action when counter=CMPA on up-count (CAU): Do nothing

Action when counter=ZERO: Do nothing Action when counter=period (PRD): Do nothing Action when counter=CMPA on up-count (CAU): Clear 💙

Enable ePWM1A

Action when counter=CMPA on down-count (CAD): Set V Action when counter=CMPA on down-count (CAD): Do nothing Action when counter=CMPB on up-count (CBU): Clear Action when counter=CMPB on up-count (CBU): Do nothing





-3

**X** ▼ -50 us

-30 us

-10 us

## 4. event and interrupt ePWMA and ePWMB can each generate events to trigger

uint16(1e-6/(1/100e6))

uint16(1e-6/(1/100e6))

Deadband Rising edge (RED) period (0~16383):

ADC modules A and B, respectively, and the trigger points can be configured to occur at specific positions within the PWM carrier cycle. Typically, a single event triggering one ADC SOC is

Deadband Falling edge (FED) period (0~16383). edge delay

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

sufficient to initiate the necessary related processing. Additionally, the ePWM module can also generate interrupts to trigger an ISR (Interrupt Service Routine).

**Event Trigger** ePWMA Counter Compare Deadband unit Enable ADC start of conversion for module A Number of event for start of conversion A (SOCA) to be generated: First event Start of conversion for module A event selection: Counter equals to zero (CTR=Zero) Enable ADC start of conversion for module B Number of event for start of conversion B (SOCB) to be generated: First event Start of conversion for module B event selection: Counter equals to zero (CTR=Zero) Enable ePWM interrupt Number of event for interrupt to be generated: First event Interrupt counter match event condition: Counter equals to zero (CTR=Zero)

10 us

Action when counter=CMPB on up-count (CBU): Do nothing

Action when counter=CMPB on down-count (CBD): Do nothing

30 us

50 us