Alternative Representation, KCL-KVL, Nodal Analysis

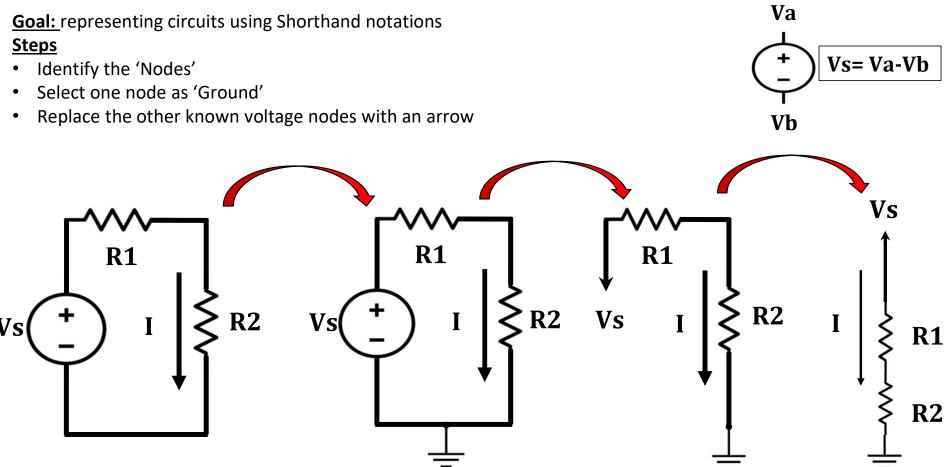
Lecture 2

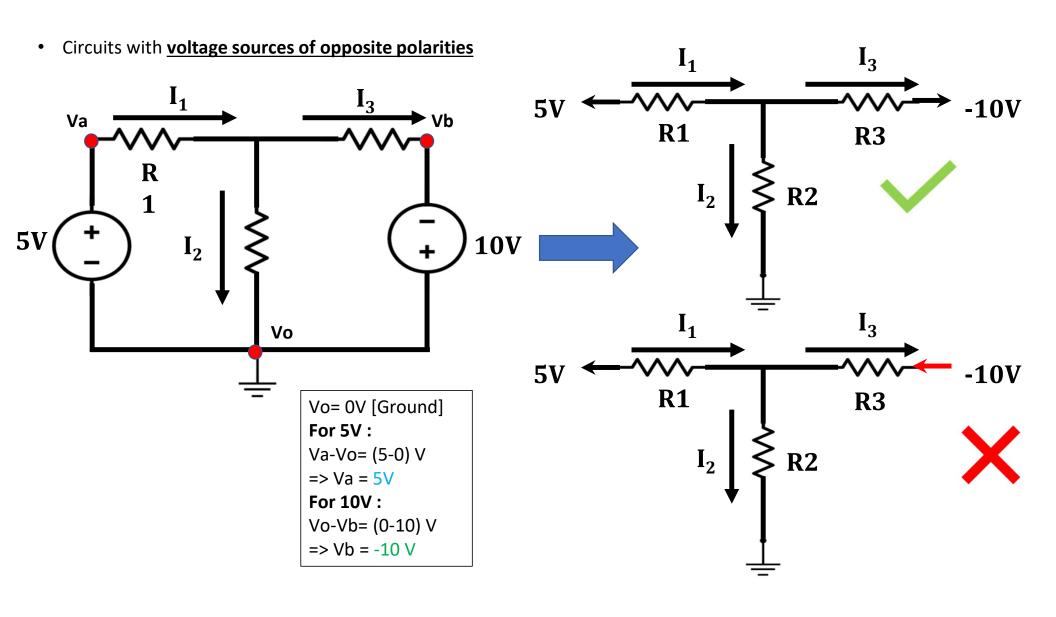
Course No: CSE 251

Course Title: Electronic Devices and Circuits

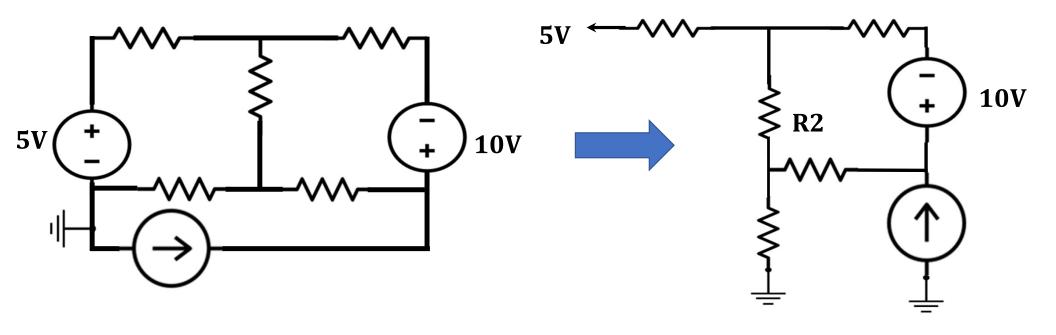
Alternative Circuit Representation: Line diagrams

Goal: representing circuits using Shorthand notations



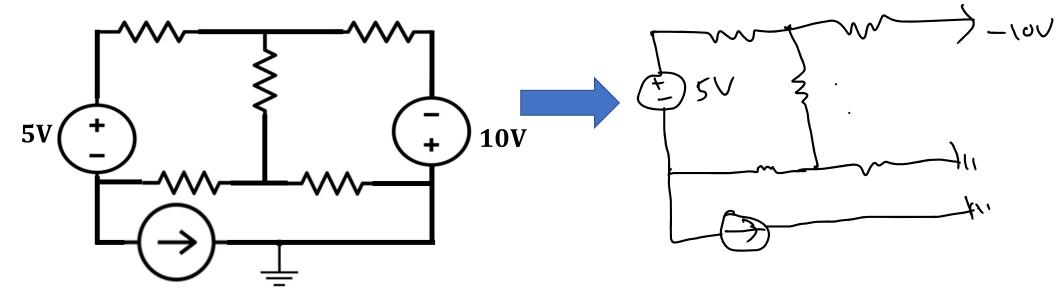


• Circuit with a current source/ floating voltage source: Keep them as they are!



• **Floating voltage sources:** None of the terminals of the voltage source is connected to the reference i.e. ground node

Practice Problem



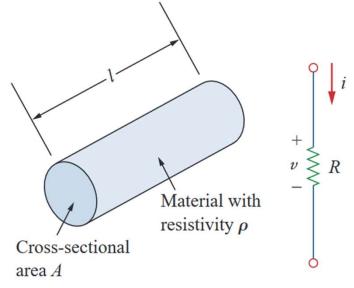
The fundamentals ...

Ohm's Law -

• the voltage $oldsymbol{v}$ across a resistor is **directly proportional** to the current $oldsymbol{i}$

flowing through the resistor (R)

 $v \propto i$ v = iR



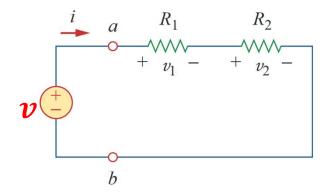
Series Resistors and Voltage Division

The **equivalent resistance** of any number of resistors connected in **series** is the <u>sum of the individual resistances</u>.

Principle of voltage division

Source voltage v - is divided among the resistors in <u>direct proportion to their</u> resistances; the larger the resistance, the larger the voltage drop.

$$v_1 = \frac{R_1}{R_1 + R_2} v$$
 $v_2 = \frac{R_2}{R_1 + R_2} v$



KCL: Kirchhoff's Current Law

The algebraic sum of the currents entering a node (closed

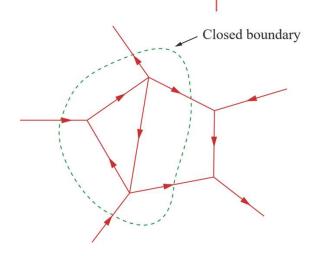
boundary) is equal to the sum of the currents leaving the node.

$$i_1 + (-i_2) + i_3 + i_4 + (-i_5) = 0$$

Current Entering node: Positive

Current Exiting node: Negative

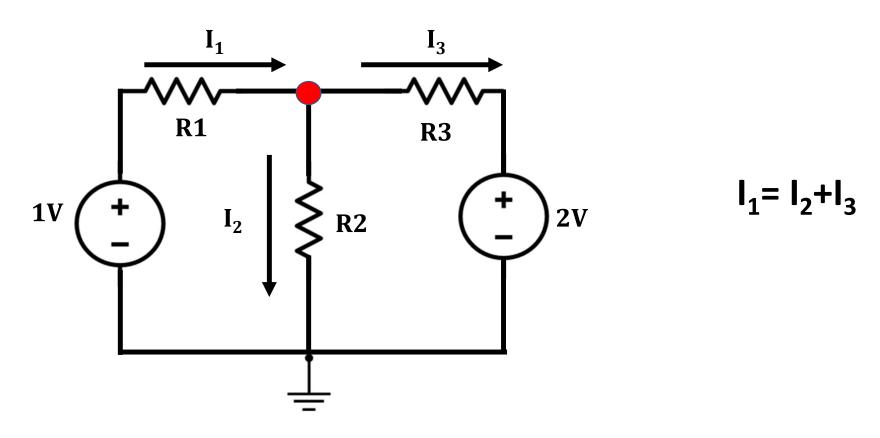
Or vice versa...



 i_2

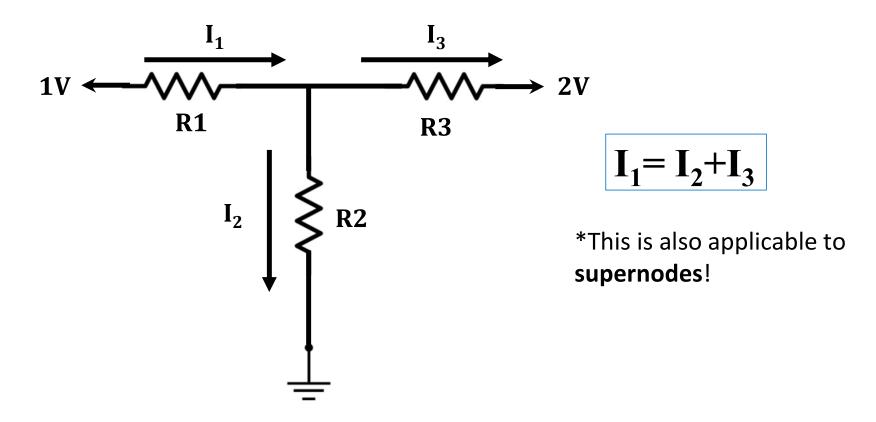
Kirchhoff's Current Law (KCL):

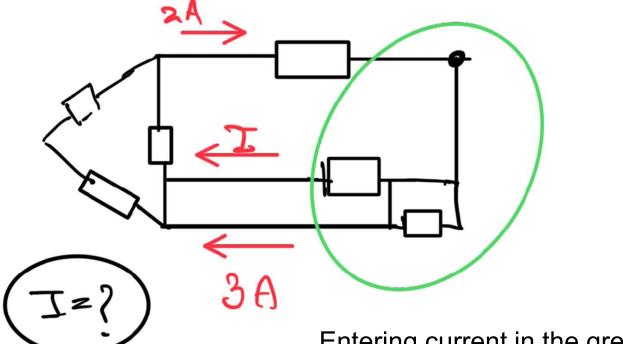
- "The algebraic sum of all currents entering and exiting a node must equal zero."
- "Currents flowing into a node (or a junction) must be equal to the currents flowing out of it."



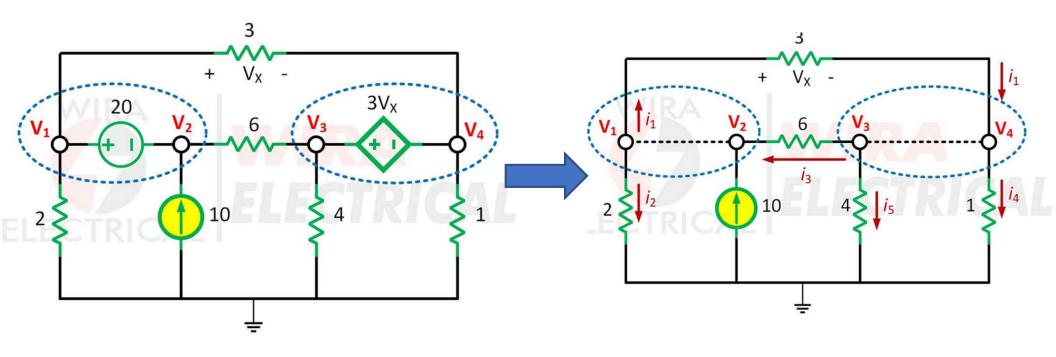
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Entering current in the green closed region= 2A Leaving current from the closed region= I & 3A



KCL for Super node 1:

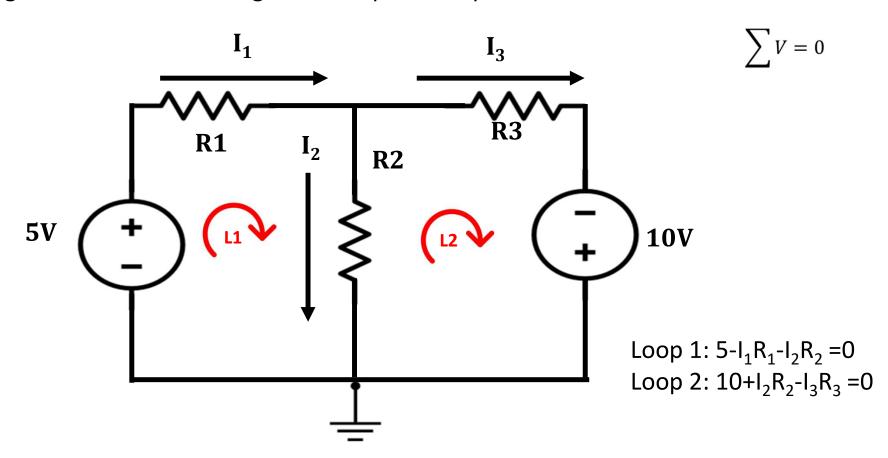
$$i_1 + i_2 = i_3 + 10A$$

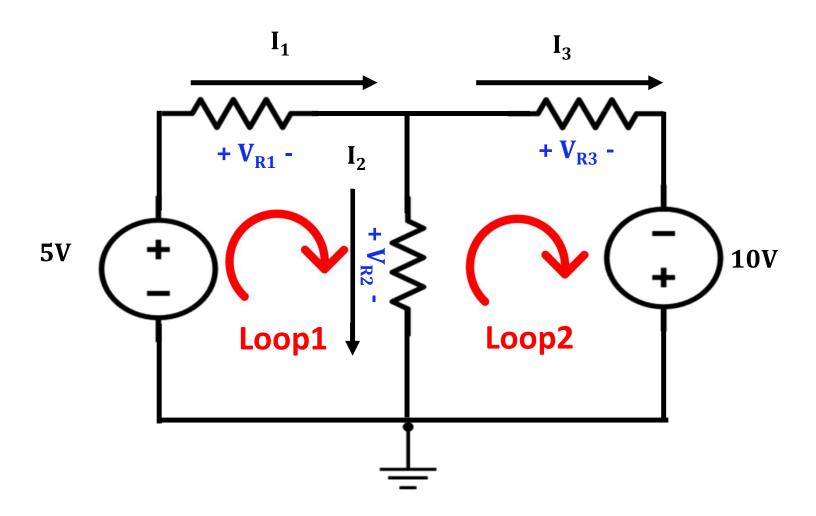
KCL for Super node 2:

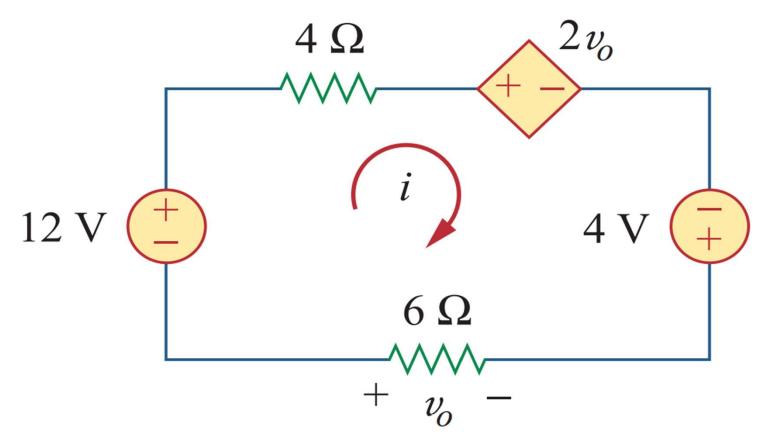
$$i_1 = i_3 + i_4 + i_5$$

Kirchhoff's Voltage Law (KVL)

The algebraic sum of all voltages in a loop must equal zero





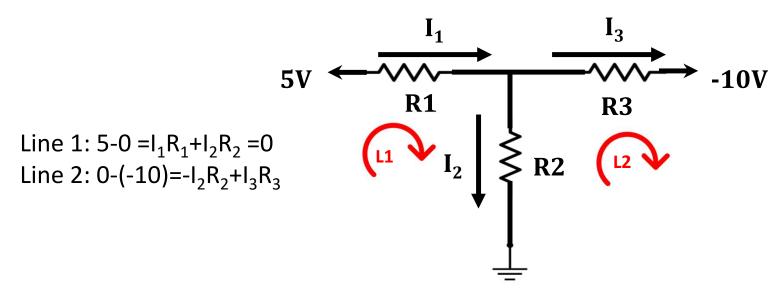


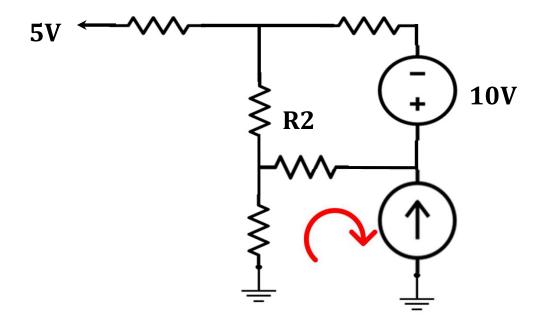
Hint:

KVL:
$$-12V + 4i + 2v_0 - 4V - v_0 = 0 --- (1)$$

 $v_0 = -6i --- (2)$

 $\sum V$ [along line] = V oltage at the starting of the node – V oltage at the ending of the node

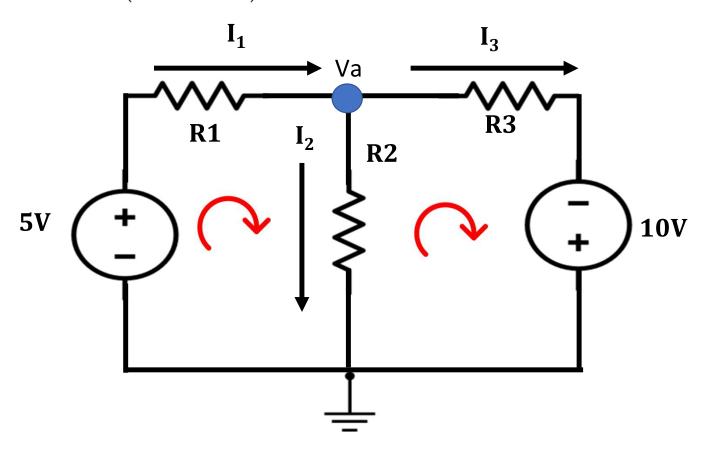


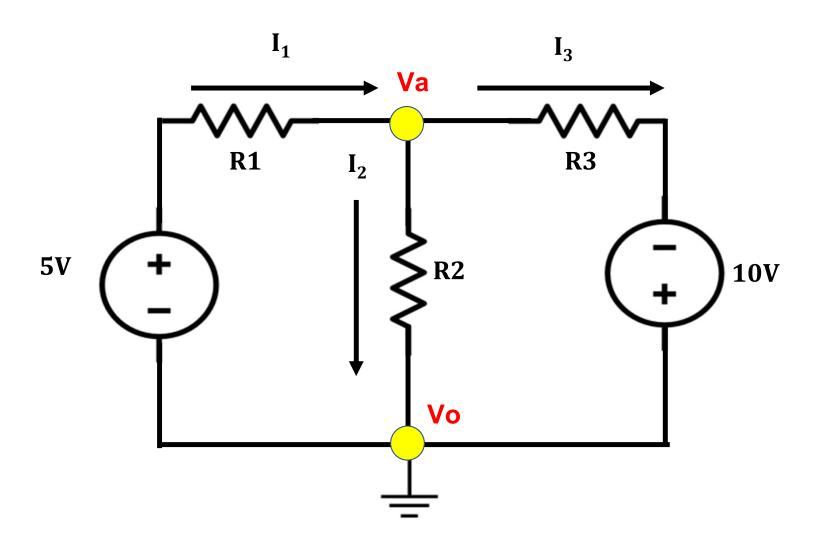


Can you write a KVL equation along this line?

Nodal analysis:

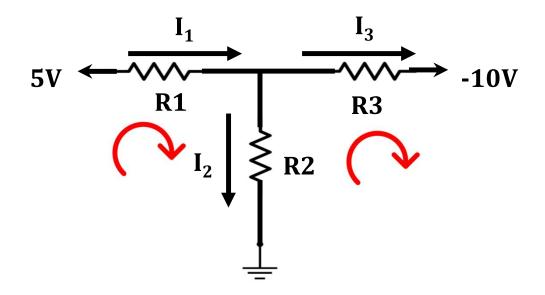
$$V_a\left(\frac{1}{R1}+\frac{1}{R2}+\frac{1}{R3}\right)-\frac{5}{R1}-\frac{0}{R2}-\frac{-10}{R3}=0$$
; Derived from applying KCL at node V_a



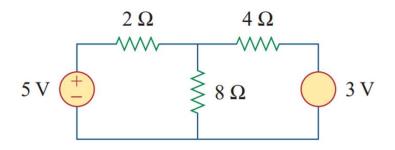


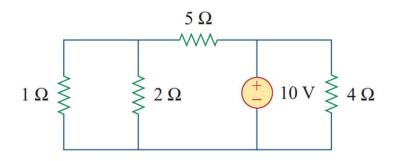
Nodal analysis:

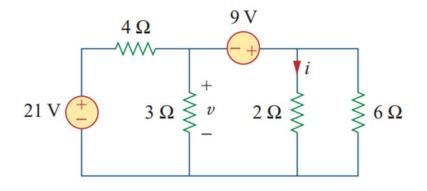
$$V_a \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} \right) - \frac{5}{R1} - \frac{0}{R2} - \frac{-10}{R3} = 0$$

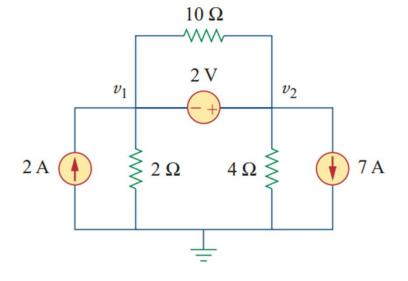


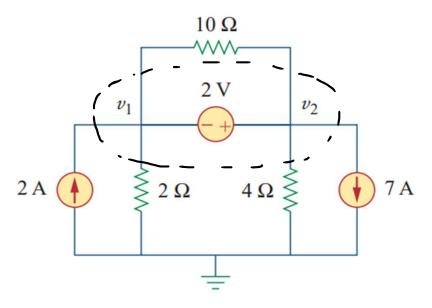
Practice Problems: i) Draw Alternative Circuit Diagrams , ii) Write down KCL equations, iii) Write down KVL equations and iv) Nodal equation











Nodal Analysis:

$$\frac{V1-0}{2} + (-2A) + \frac{V2-0}{4} + 7A = 0 ----(1)$$

$$V1 - V2 = -2$$
 -----(2)

Thank You