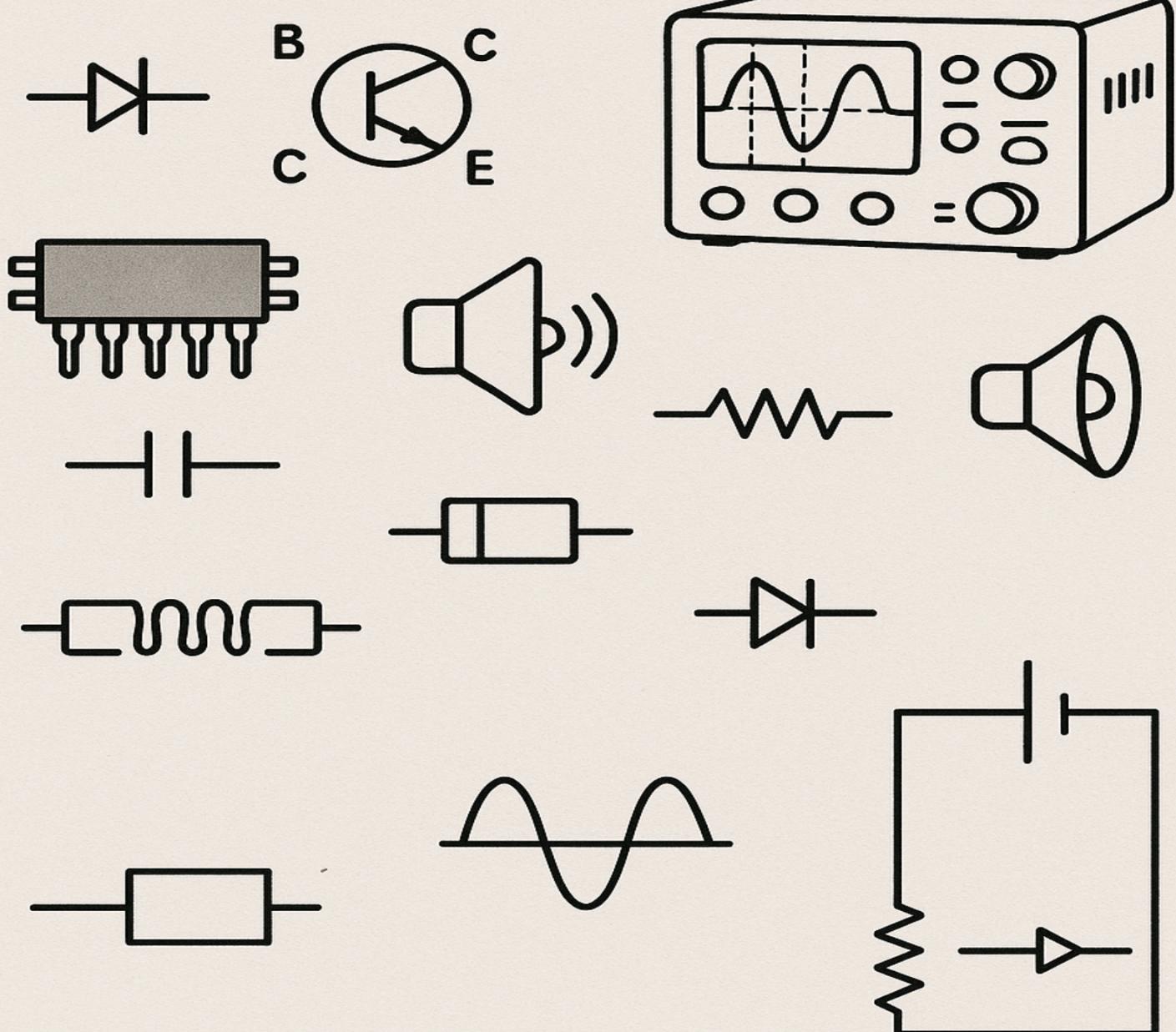


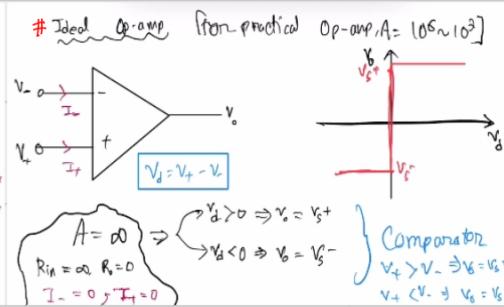
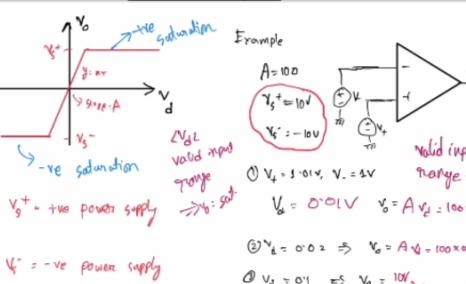
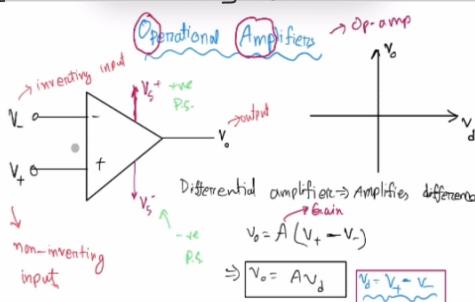
CSE 251

ELECTRONIC DEVICES AND CIRCUITS

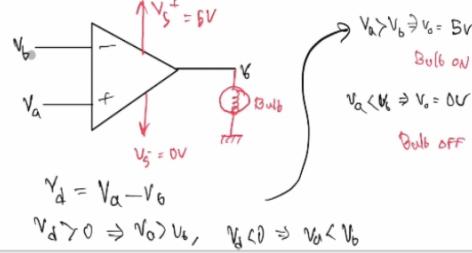


[Mohammad Atif Abrar - YT] [ABA]

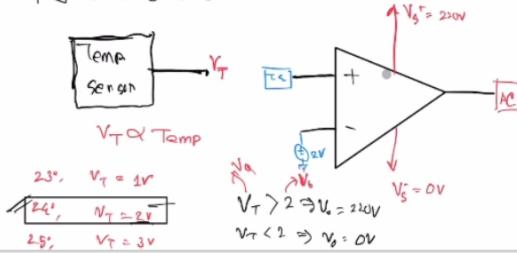
Lecture-1D



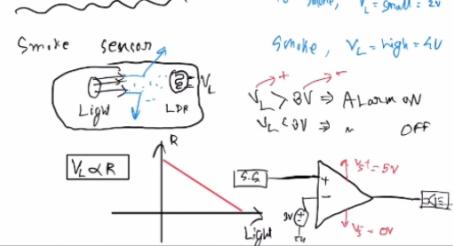
① Comparator (Open loop)



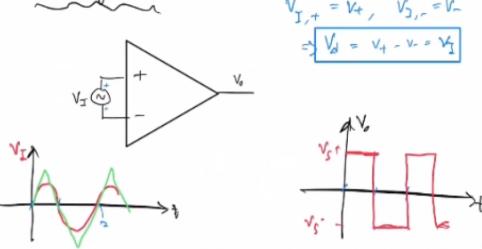
② Turn ON AC automatically



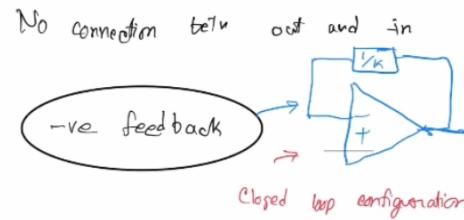
③ Smoke Detector



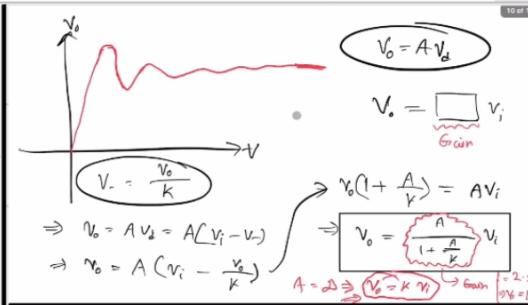
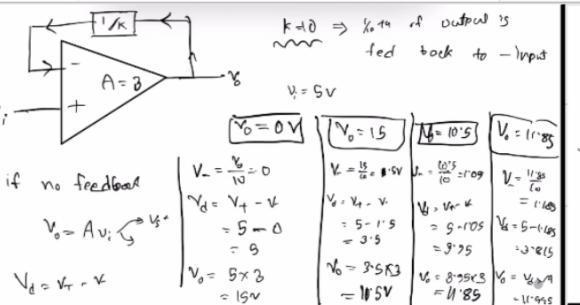
④ Pulse generator



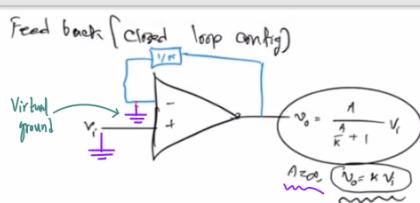
Open Loop config



Little tie in input results in V_d^+ . Same for -ve
 Output is unstable, main reason is that ideal
 OpAmp gain is ∞ .
 Thus for proper control \rightarrow -ve Feedback

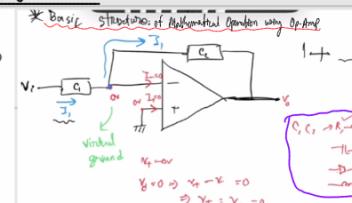


Lecture-20



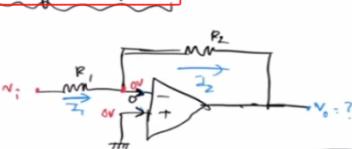
$$V_d = A V_d \Rightarrow V_d = \frac{V_o}{A} = \frac{3}{\infty} = 0$$

\therefore In neg feedback, $V_d > 0 \Rightarrow V_+ - V_- > 0 \Rightarrow V_+ = V_-$
 $I_+ = 0, I_- = 0$



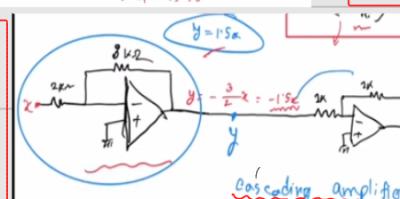
- Steps:
- ① $V_d = 0 \Rightarrow V_+ = V_- = ?$
 - ② $I_+ = ?$
 - ③ $I_+ = I_-$
 - ④ $V_d = k V_L / \text{Ohm's law}$

① Inverting amplifier



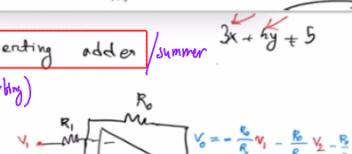
$$I_1 = \frac{V_i - 0}{R_1} = \frac{V_i}{R_1}, I_2 = 0 + I_2 \Rightarrow V_d = -I_2 R_2$$

$$I_2 = I_1 = \frac{V_i}{R_1}, I_2 = \frac{0 - V_d}{R_2} \Rightarrow V_d = -\left(\frac{R_2}{R_1}\right) V_i$$

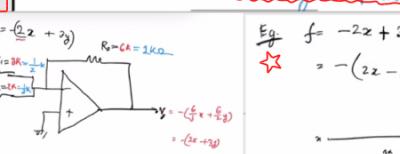


$$y = 4x$$

② Inverting adder / summer (inverting)

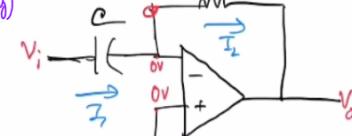


$$V_d = -R_o \left(\frac{1}{R_1} V_1 + \frac{1}{R_2} V_2 + \frac{1}{R_3} V_3 \right)$$



$$y = -2x + 3y - 4z$$

Differentiation (inverting)



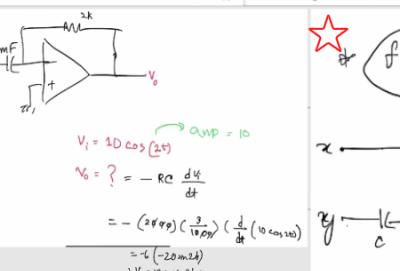
$$V_d = V_i - 0 = V_i \Rightarrow V_d = -RC \frac{dV_i}{dt}$$

$$i_c = C \frac{dV_c}{dt} = C \frac{dV_i}{dt} = I_1$$

$$I_2 = I_1 = I_c = C \frac{dV_i}{dt}$$

$$I_2 = \frac{0 - V_d}{R} \Rightarrow V_d = -I_2 R$$

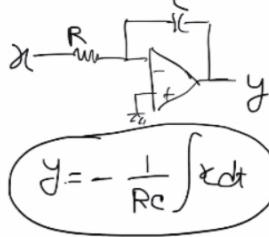
$$\Rightarrow V_d = -I_2 R$$



$$f = -2x - 3 \frac{dy}{dt}$$

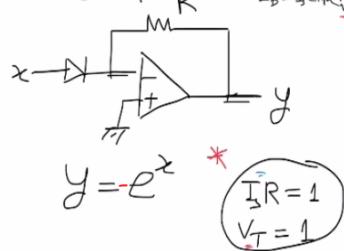
$$y = -2x + 2z - 4x$$

② Integrator



$$f = xy$$

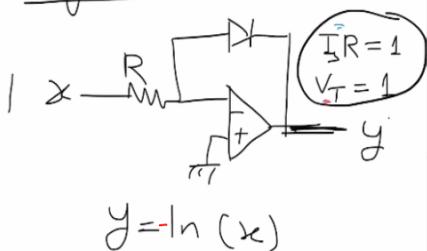
* Exponential



$$Y = e^x$$

$$I_D = I_S \exp\left(\frac{V_D}{V_T}\right)$$

* Logarithm



$$Y = -\ln(x)$$

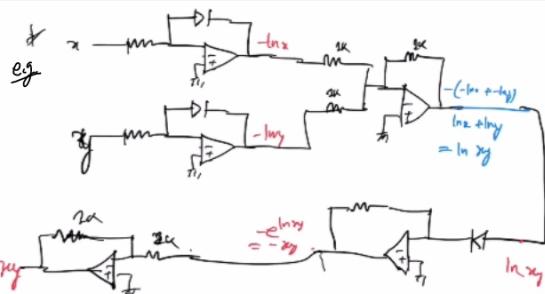
$$\textcircled{1} \ln(\exp(x)) = x, \quad e^{\ln x} = x$$

$$\textcircled{2} \ln(ab) = \ln a + \ln b$$

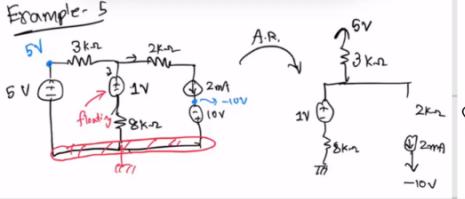
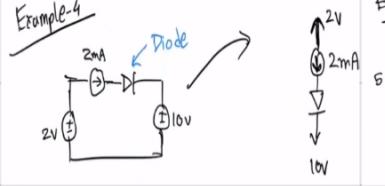
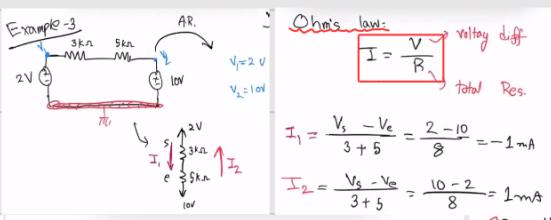
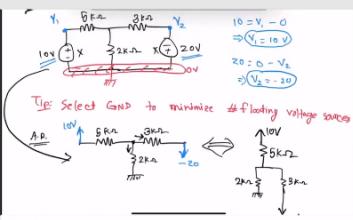
$x \rightarrow \ln x$

$$\begin{aligned} & y \rightarrow \ln y \\ & z \rightarrow \ln z \end{aligned}$$

$$\ln x + \ln y \rightarrow \ln xy \rightarrow \exp \cdot xy$$



Line Diagram



① Draw the alternative representations of the following circuits. Select GND in such a way that the # of floating voltage sources is minimized.

AC / Large electrical devices use 1/2 A currents
Transistors / MOSFET / Complex electronic devices uses mA currents
Currents in A (instead of mA) will cause these devices to burn.

milili-kilo conversion

$$\text{mA} \times \text{k}\Omega = \text{V}$$

$$10^{-3} \times 10^3 = 1$$

KCL, KVL (Mesh & Nodal Analysis)

KCL

Convention: $I_{out} = +ve$
 $I_{in} = -ve$

$V_z = I_1 - I_2 - I_3 = 0$ both corners

Node: $\sum I = 0$

$$V_1: -I_1 + I_2 + I_3 = 0$$

loop: $\sum V = 0$

Res: If my dir = dir of V $\Rightarrow +ve$
else $\Rightarrow -ve$

Voltage source: Polarity of first node visited

$$L_2 + 3I_3 - 20 - 2I_2 = 0$$

$$= L_2 + 5I_1 + 3I_3 - 20 - 10 = 0$$

$$I_3 = L_1 + L_2$$

Loop \Leftrightarrow Line

lines $\sum V = V_{line} - V_{line}$

$L_1: +5I_1 + 2I_2 = 10 - 0$

$L_2: -2I_1 + 5I_2 + 3I_3 = 0 - (-20)$

$L_3: +5I_2 + 3I_3 = 10 - (-20)$

If we can do anything, if needed

Nodal

$V_1: V_1 \left(\frac{1}{2} + \frac{1}{3} + \frac{1}{4} \right) - \frac{10}{2} - \frac{V_2}{3} - \frac{0}{4} = 0$

$V_2: V_2 \left(\frac{1}{3} + \frac{1}{2} \right) - \frac{V_1}{3} - \frac{0}{8} = 0$

$V_3: V_3 \left(\frac{1}{4} + \frac{1}{3} \right) - \frac{V_2}{4} - \frac{0}{8} = 0$

Using nodal analysis, find V_A , V_B , and I_T .

Domino

Using ONLY following equations, find i_1, i_2, i_3, V_a , and V_b . You cannot use mesh/KVL.

① $V_i = R$
② $V_e = V_+ - V_-$
③ $\sum I = 0$

If there is a current source along line, cannot write KVL

- ① Write down KCL for node a.
② Write down KVL for L_1 , L_2 , and L_3 .
③ Solve the equations to find I_1 , I_2 , and I_3 .

④ [20]

$x = 5 + \text{last 2 digits of your ID}$
 $y = x + 3^{\text{rd}} \text{ digit of your ID}$
 $z = y + 2^{\text{nd}} \text{ digit of your ID}$

- ① Write down KCL for node a.
② Write down KVL for L_1 and L_2 .
③ Solve the equations to find I_1 , I_2 , and I_3 .

⑤ [20]

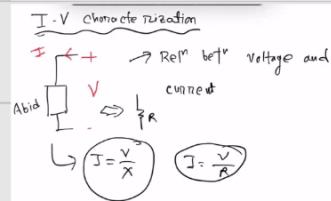
$x = 5 + \text{last 2 digits of your ID}$
 $y = x + 3^{\text{rd}} \text{ digit of your ID}$
 $z = y + 2^{\text{nd}} \text{ digit of your ID}$

- Domino
- Using ONLY following equations, find i_1, i_2, i_3, V_a , and V_b . You cannot use mesh/KVL.
- ① $V_i = R$
② $V_e = V_+ - V_-$
③ $\sum I = 0$

$x = 5 + \text{last 2 digits of your ID}$
 $y = x + 3^{\text{rd}} \text{ digit of your ID}$
 $z = y + 2^{\text{nd}} \text{ digit of your ID}$

Topics

- Lumped Matter Abstraction \rightarrow Making things easier
- IV characteristics
- IV char. of simple linear devices
- IV char. of compound linear devices
- Equivalent circuit and IV char.



① Tabular form

V(V)	I(mA)
1	0.5
2	1
-2	-1
3	1.5

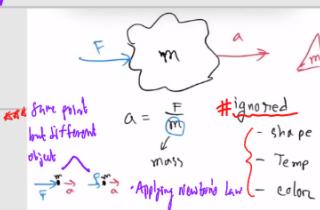
② Functional form

$I = f(V)$ on $V = g(I)$

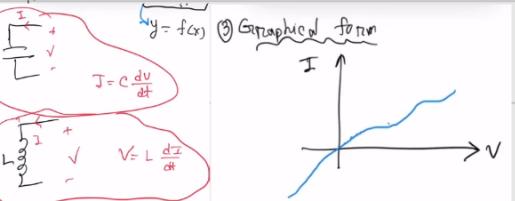
$f(x) = ?$

$I = \frac{1}{R}V$

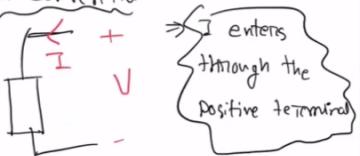
$y = f(x) = \frac{1}{R}x$

Lumped Member Abstraction

"Actual way" \rightarrow Maxwell's eqn
"Easy way" - Ohm's law

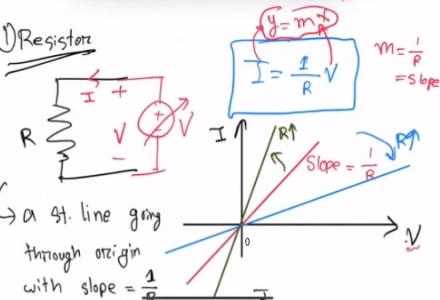


Sign convention

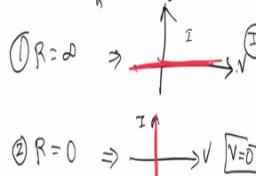
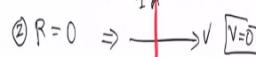
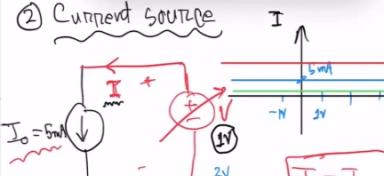


How to find IV

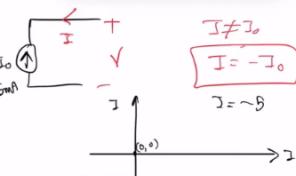
resistor is added so that too much current don't pass. Otherwise, it'll burn the device

IV Characteristics of Simple Linear Devices① Resistor

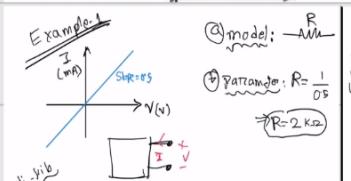
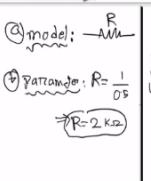
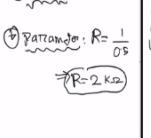
a st. line going through origin with slope $\frac{1}{R}$

① $R=2$ ② $R=0$ ② Current SOURCE

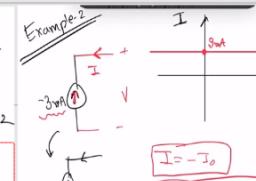
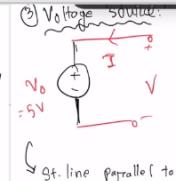
st. line parallel to x axis (voltage axis) that cuts the y axis (current axis) at I_0



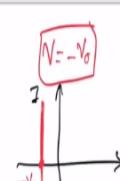
$I \neq I_0$
 $I = -5$

Example 1④ model: $-AV$ ⑤ parameter: $R = \frac{1}{0.5}$ 

Equivalent ckt
 \Rightarrow I.P.F. they have same JV

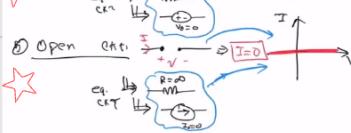
Example 2③ Voltage SOURCE

st. line parallel to y axis (current axis) that cuts the x axis (voltage axis) at V_0

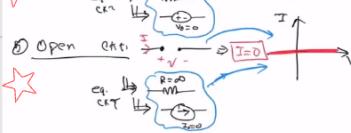
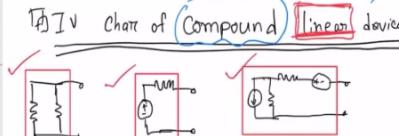
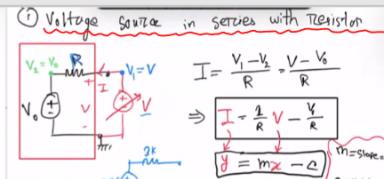


opposite polarity

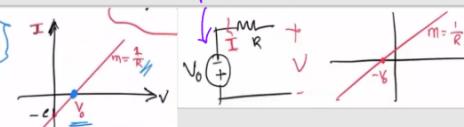
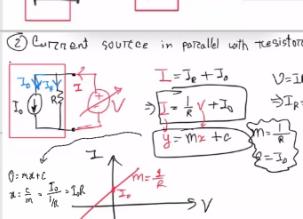
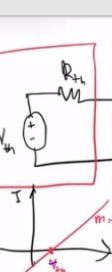
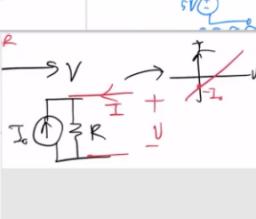
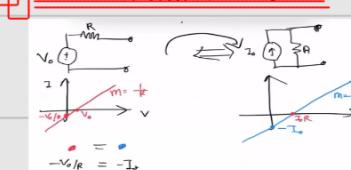
⑥ Short ckt: $\Rightarrow V=0$



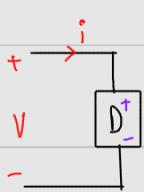
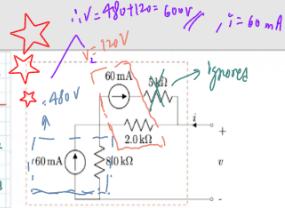
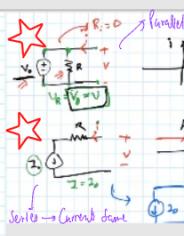
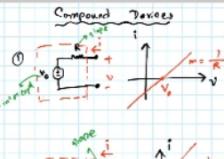
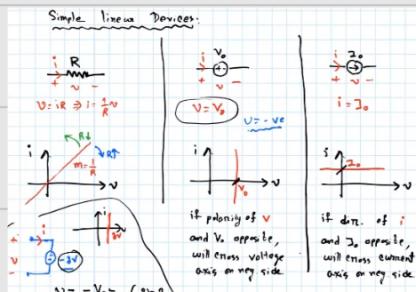
⑦ Open ckt: $\Rightarrow I=0$

IV Char. of Compound Linear devices① Voltage source in series with resistance

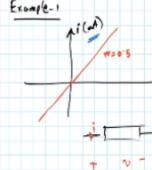
$$\begin{aligned} I &= \frac{V_1 - V_2}{R} = \frac{V_0}{R} \\ \Rightarrow I &= \frac{1}{R}V - \frac{V_0}{R} \\ y &= mx - c \quad (m = \text{slope} = \frac{1}{R}) \\ c &= y - mx = -\frac{V_0}{R} \end{aligned}$$

② Current source in parallel with resistorThenevin and IVSource Transformation & IV

Convention:

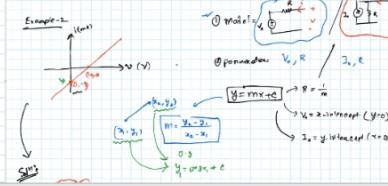
Compound Device = Σ Simple devices

- A. $V_0 = 120.0V$ $I_0 = 63.63614mA$
 B. $V_0 = 600.0V$ $I_0 = 40.0mA$
 C. $V_0 = 360.0V$ $I_0 = 40.0mA$
 D. $V_0 = 600.0V$ $I_0 = 60.0mA$
 E. $V_0 = 600.0V$ $I_0 = 63.63614mA$



$$\textcircled{1} \text{ model: } i = \frac{v}{R}$$

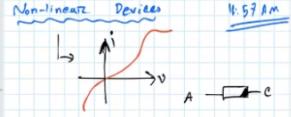
$$\textcircled{2} \text{ parameters: } R = \frac{1}{m} = \frac{1}{0.5} = 2k\Omega$$



$$\begin{aligned} & \text{Slope: } m = \frac{y_2 - y_1}{x_2 - x_1} = \frac{0 - (-5)}{10 - 0} = \frac{5}{10} = 0.5 \\ & y = mx + c \\ & 0 = 0.5 \cdot 0 + c \Rightarrow c = 0 \\ & y = 0.5x + 0 \end{aligned}$$

$$\begin{aligned} & \text{At } v=0 \Rightarrow y = -5 \Rightarrow I_o = -5 \\ & \text{At } v=10 \Rightarrow y = 5 \Rightarrow I_o = 5 \\ & R = 2k\Omega \quad R = 2k\Omega \end{aligned}$$

Non-Linear Devices

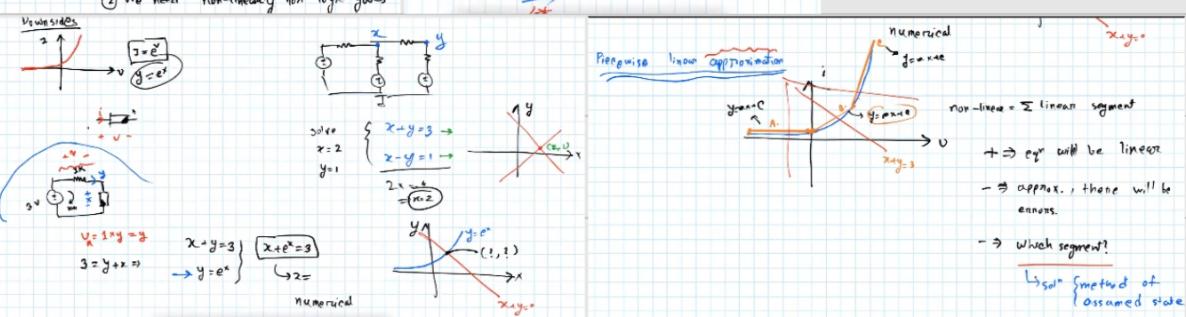
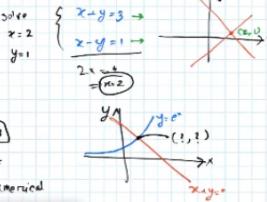
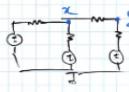


Why? - $\textcircled{1}$ linear devices have limited application
 \hookrightarrow linear operation $mx+by=0$

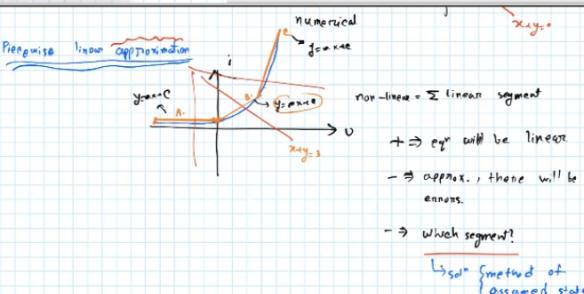
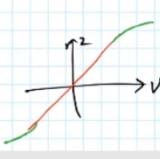
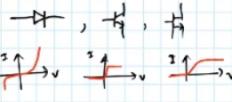
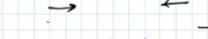
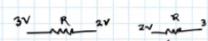
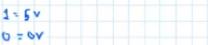
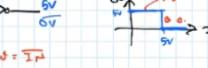
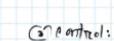
$$(xy+bx+0=0)$$

$$e^x, \sin x \propto x$$

$\textcircled{2}$ we need non-linearity for logic gates

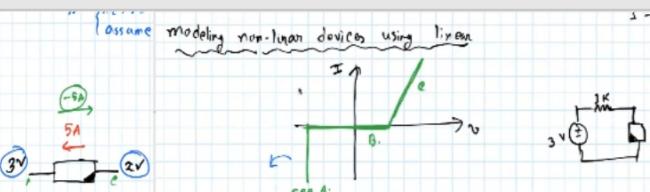
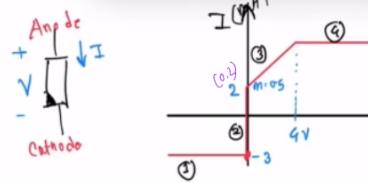
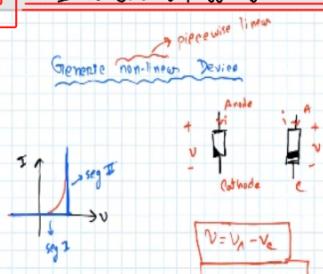


We need non-linearity for logic gates

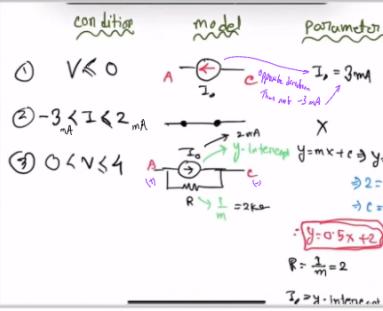


Lecture - 5

Introduction to Diode

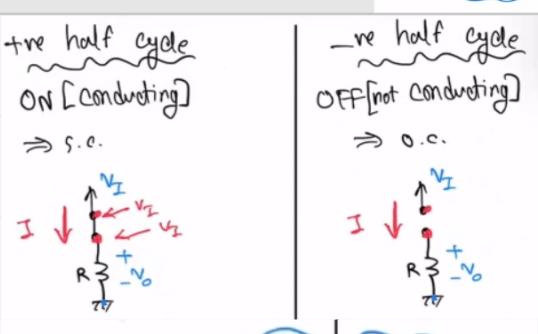
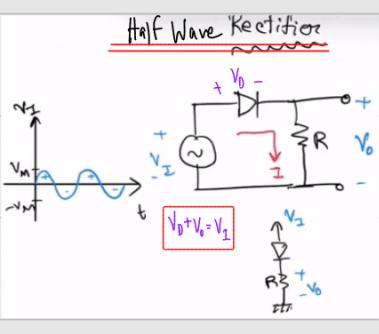
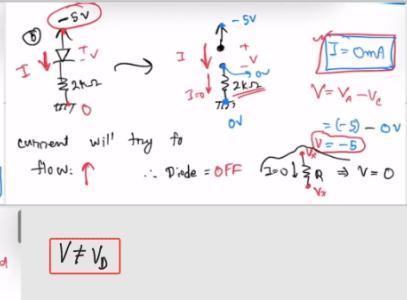
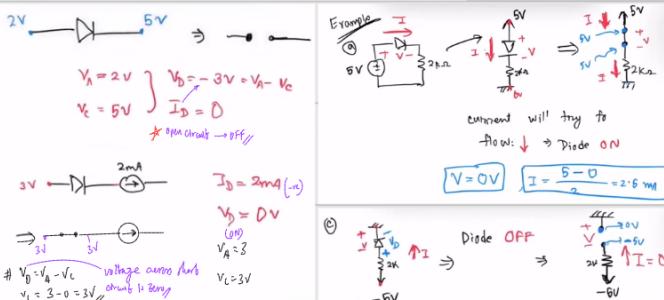
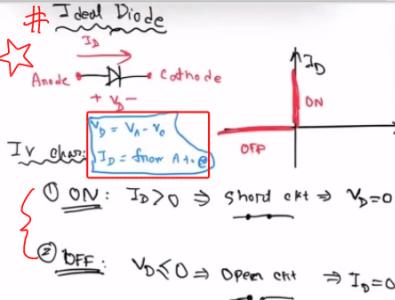
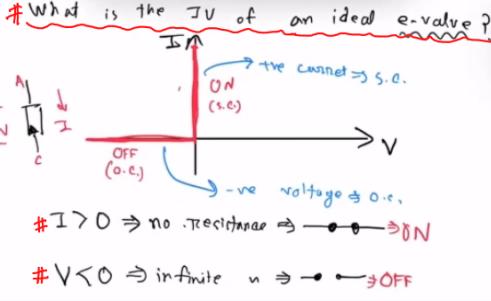
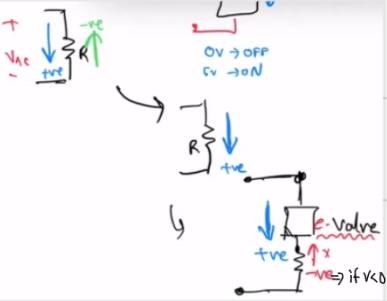
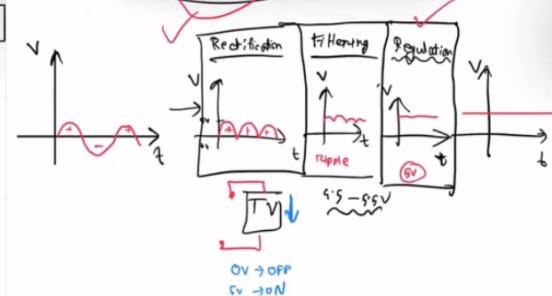
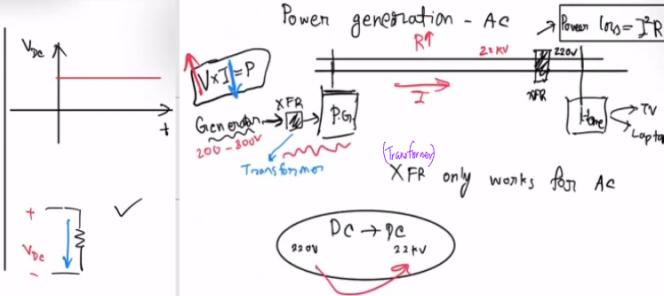
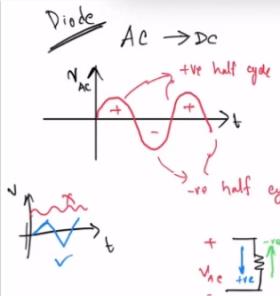
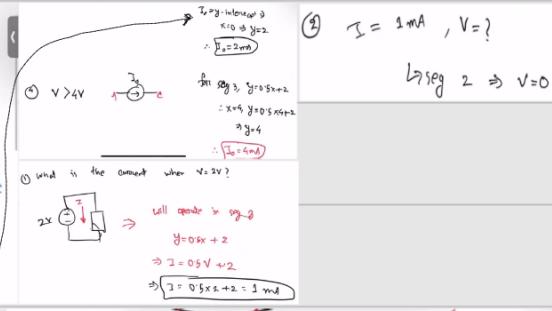


Short circuit has no parameters



$$\textcircled{4} \quad I = 1 \text{ mA}, V = ?$$

$$\textcircled{5} \quad \text{seg 2} \Rightarrow V = 0$$



DC to DC transmission is expensive

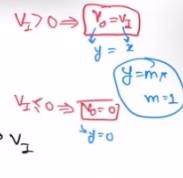
Transfer Characteristics

↳ Graph

↳ x-axis \rightarrow Input current (V/I)

↳ y-axis \rightarrow Output voltage (V/I)

Voltage Transfer Characteristics (VTC of a Half-Wave Rectifier)

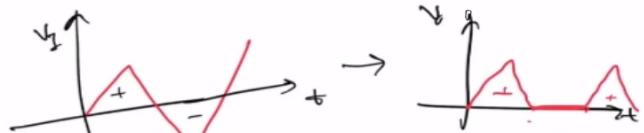
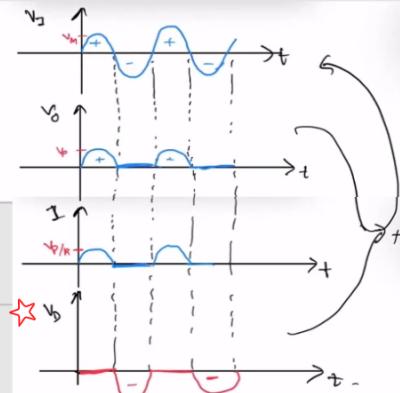


Waveform

↳ Graph

↳ x-axis \rightarrow time

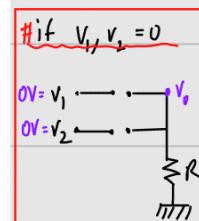
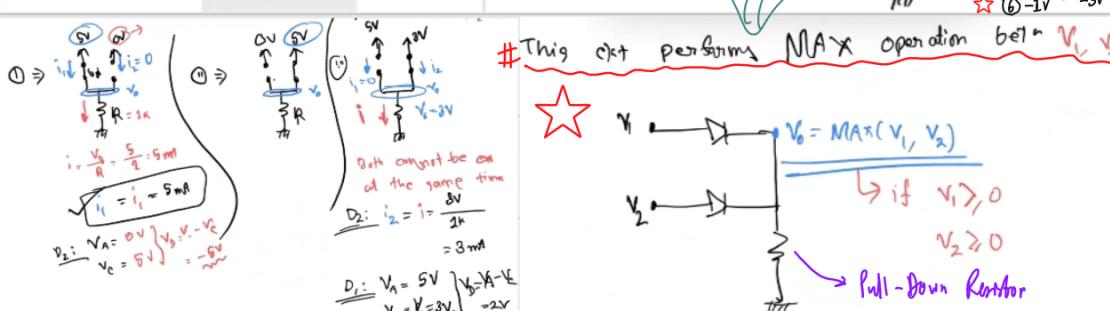
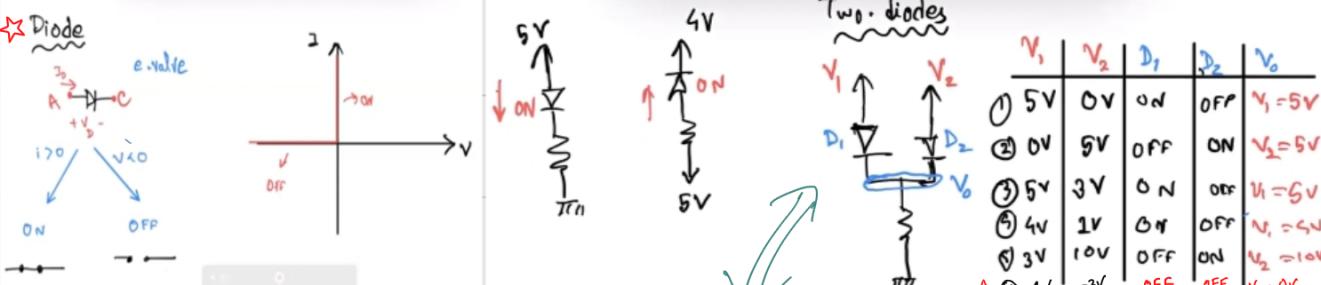
↳ y-axis \rightarrow V/I



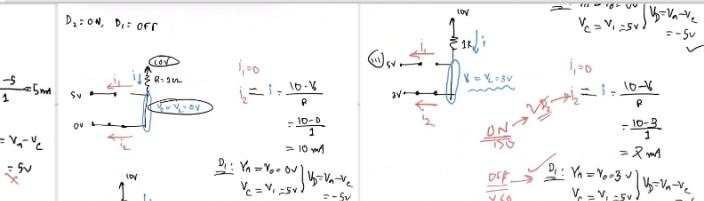
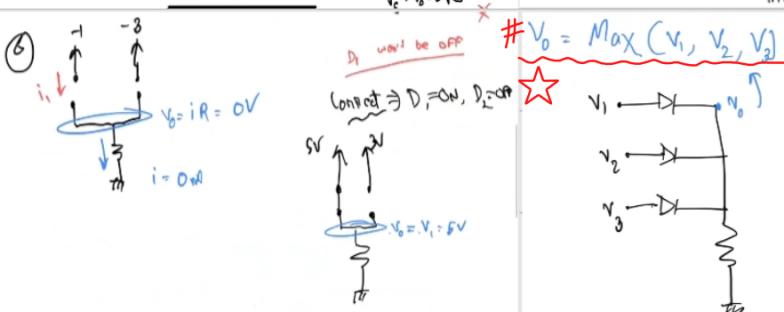
Lecture-6

16/03/2025

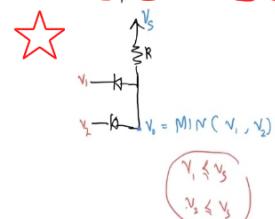
Monday



As $V_1, V_2 = 0$, V_o would be floating node. In floating mode, voltage is undefined. Whenever both diodes are zero, the resistor pulls down the node and makes it zero.



This circuit performs MIN operation between V_1, V_2



$$V_o = \text{MIN}(V_1, V_2)$$

★

Pull-Up Resistor

$$V_o = \text{MIN}(V_1, V_2, V_3)$$

Logics GATES Using Diode

#How to represent boolean variables in ckt?

Boolean variable
 $x, y \rightarrow 1, 0$
 $\text{Ans} \rightarrow x \cdot y$
 $\text{OR} \rightarrow x + y$
 $\text{NOT} \rightarrow \bar{x}, x'$

Voltage
① Current
② State
0 → 0V
1 → 5V

memory

most common
 $Z = x + y$
 $V_Z = \text{OR}(V_x, V_y)$
 $= \text{MAX}(V_x, V_y)$

OR

$Z = x + y$
 $V_Z = \text{OR}(V_x, V_y)$
 $= \text{MAX}(V_x, V_y)$

$\begin{array}{|c|c|c|c|} \hline x & y & Z=x+y & \\ \hline 0 & 0 & 0 & \\ \hline 0 & 1 & 1 & \\ \hline 1 & 0 & 1 & \\ \hline 1 & 1 & 1 & \\ \hline \end{array}$

$\begin{array}{|c|c|c|c|} \hline x & y & V_x & V_y & V_Z \\ \hline 0 & 0 & 0V & 0V & 0V \\ \hline 0 & 1 & 0V & 5V & 5V \\ \hline 1 & 0 & 5V & 0V & 5V \\ \hline 1 & 1 & 5V & 5V & 5V \\ \hline \end{array}$

$Z = x + y = \text{OR}(x, y)$

Pull down R

$\text{memory} \downarrow$
random can be changed using magnet

AND

$Z = x \cdot y$
 $V_Z = \text{MIN}(V_x, V_y)$
 $= \text{MIN}(V_x, V_y)$

$\begin{array}{|c|c|c|c|} \hline x & y & Z=x \cdot y & \\ \hline 0 & 0 & 0 & \\ \hline 0 & 1 & 0 & \\ \hline 1 & 0 & 0 & \\ \hline 1 & 1 & 1 & \\ \hline \end{array}$

$\begin{array}{|c|c|c|c|} \hline x & y & V_x & V_y & V_Z \\ \hline 0 & 0 & 0V & 0V & 0V \\ \hline 0 & 1 & 0V & 5V & 0V \\ \hline 1 & 0 & 5V & 0V & 0V \\ \hline 1 & 1 & 5V & 5V & 5V \\ \hline \end{array}$

MIN

$\text{OUT} = x \cdot y \cdot z$

Example-1 Implement using ideal diodes:
 $\text{DUT} = x + y \cdot z$ boolean

Equivalent

Example-2 $w, x, z \rightarrow \text{boolean}$
FIND OUT as a function of w, x, z
Then simplify.

$\text{DUT} = w \cdot x + x + z$

$\star = (w+1)x + z$
 $= 1 \cdot x + z$
 $= x + z$

Lecture-7

Topics

- Review
- Construction of real diode
- Piecewise Linear Models of real diode
- Method of assumed state

Ideal Diode

e-value
A → e
+ y -

OFF → 0
ON → 1

mode cond. model ear

ON	$I_D > 0$	$V_D = 0$
OFF	$V_D < 0$	$I_D = 0$

③ Prediction

④ MIN/MAX → $V_D = \text{Min}(V_x, V_y)$
 $V_x = k_1 \cdot I_x$
 $V_y = k_2 \cdot I_y$

How to make a Diode

① Vacuum tube
Group IV

② Semiconductor
Si, Ge
Glass, wood
Cu, Fe

Conductivity
 $\alpha \frac{1}{R}$
Intrinsic (Pure) Si, Ge

Extrinsic (Doped) → Group II (P-type)
Group III (N-type)

P-n Junction Diode

$F = qE$

Junction
Depletion region

$E_{\text{diff}} \propto \Delta \text{density}$

$E_{\text{diff}} = E_{\text{diff}}^0 \left(\frac{N_p}{N_n} \right)^{1/2}$

Forward Bias
The barrier decreases
 $I_D \approx 0$

Reverse Bias
The barrier increases
 $I_D \approx 0$

Real Diode

$I_D = I_s [\exp(\frac{V_D}{V_T}) - 1]$

$V_T = 0.5 - 0.02V$
 $G_e = 0.2 - 0.3V$

Reverse saturation current
 $I_s = 10^{-9} A$

Saturation current
 $I_s = 10^{-9} A$

ON: $I_D > 0 \rightarrow V_D < 0 \rightarrow V_D = V_{D0} + I_D \cdot R_D$

OFF: $V_D < V_{D0} \rightarrow V_D = 0$

CVD Model

Piecewise Linear Model of a Real Diode

CVD: Constant Voltage Drop

Ideal Diode

OFF → 0
ON ($I_D > 0$) → 1
OFF ($V_D \leq 0$) → 0

CVD Model

OFF → 0
ON ($I_D > 0$) → 1
OFF ($V_D \leq V_{D0}$) → 0

CVD+P model

ON ($I_D > 0$) → 1
OFF ($V_D \leq V_{D0} + I_D \cdot R_D$) → 0

We can approximate the I-V characteristics of a real diode with that of an ideal diode.

$r = \frac{1}{\text{slope}}$ Steeper slope → less R

Example

Find I_D using

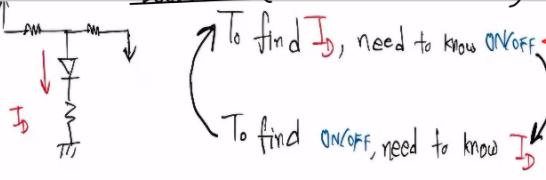
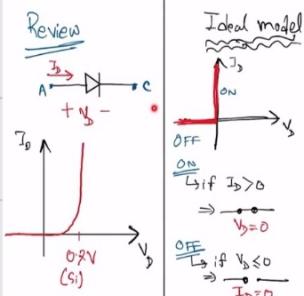
- ① Ideal diode model
- ② CVD model with $V_{D0} = 0.3V$
- ③ CVD+P model with $V_{D0} = 0.3V$ and $R = 0.01k\Omega$

① $I_D = \frac{5}{2k} = 2.5 \text{ mA}$

② $0.2 = V_T - V_D$
 $0.2 = 5 - 0.3$
 $V_D = 4.3V$
 $I_D = \frac{4.3}{2k} = 2.15 \text{ mA}$

③ $\sum V_{\text{drop}} = V_{\text{Shunt}} - V_{\text{load}}$
 $0.9 + 0.01I_D + 2I_D = 5 - 0$
 $I_D (0.01 + 2) = 5 - 0.9$
 $I_D = \frac{5 - 0.9}{0.01 + 2}$
 $I_D = 2.139 \text{ mA}$

Lecture-8 (Method of Assumed State)



Method of assumed state

- Step 1: Assume \rightarrow ON \rightarrow OFF
- Step 2: Solve \rightarrow ON \rightarrow OFF, $I_D=?$
- Step 3: Verify \rightarrow ON \rightarrow OFF, $V_D \leq V_{D0}$
- If FALSE, go to step 1

Solution) Method of assumed state

Example 1

Find I_1, I_2, I_3, V . Use CVD with $V_{D0} = 1V$

Assumption CORRECTED

Step 1: $V_D = 1V$ ON

Step 2: $V_1 - V_2 = 1V$ $I_1 = I_2$

Step 3: $D_1 \rightarrow$ ON $\Rightarrow I_{D1} = 0.5 > 0$

$I_1 + I_2 = I_3 \Rightarrow I_1 = I_3 - I_2$

Example 2

Find I_1, I_2, I_3, V . Use CVD with $V_{D0} = 1V$

Assumption WRONG!

Step 1: ON, ON

Step 2: $V_1 - V_2 = 1V$ $I_1 = I_2$

Step 3: $D_1 \rightarrow$ ON $\Rightarrow I_{D1} = 0.5 > 0$

Step 1: OFF, ON

Step 2: KVL along $I_1 \Rightarrow$

$5I_2 + 1 + 20I_3 = 10 \quad (1)$

KCL $\Rightarrow I_1 + I_2 = I_3 \Rightarrow I_2 = I_3 - I_1$

Step 3: $D_1 \rightarrow$ OFF $\Rightarrow V_D = 20I_3 - 5 = 6.2V$

$V_D = V_A - V_C = D - 6.2 = -6.2V$

And (1) $\Rightarrow 5I_2 + 1 + 20I_3 = 15$

$I_2 = (15 - 1) / (5 + 20) = 0.56mA$

$D_2 \rightarrow$ ON $\Rightarrow I_{D2} = 0.56 > 0$

Assumption correct!

Example 3

Find I_1, I_2, I_3, V . Use CVD, $V_{D0} = 1V$

Step 1: ON, OFF

Step 2: $V_1 - V_2 = 1V$

Nodal \Rightarrow

$V_1 - V_2$ supernode

$V_1(\frac{1}{2}) + V_2(\frac{1}{2}) - \frac{1}{2} - \frac{1}{5} = 0$

$\Rightarrow (2V_1 + 6)V_2 = 3 - 1$

$V_1 - V_2$ constraint

$V_1 - V_2 = 1V$

$\Rightarrow V_1 + (-1)V_2 = 1 \quad (1)$

Solving (1) and (2) \Rightarrow

$V_1 = 4.5V$

$V_2 = 3.5V$

Assumption wrong!

$\therefore I_1 = \frac{6 - V_1}{2} = 0.2mA$

$I_2 = 0 \quad (\because D_2 = \text{OFF})$

$I_3 = \frac{V_1 - 1}{5} = 0.32mA$

$V_{D1} = V_A - V_C = V_2 - 1 = 2.5V$

Step 1: $V_1 - V_2 = 1V$

Step 2: $V_1 - V_2 = 1V$

Example 3

Nodal \Rightarrow

$V_1 - V_2 - V_3$ supernode

$V_1(\frac{1}{2}) + V_2(\frac{1}{2}) + V_3(\frac{1}{2}) - \frac{1}{2} - \frac{1}{2} = 0$

$\Rightarrow (2V_1 + 5)V_2 + (2V_3 + 5)V_3 = 3.5 - 1$

$V_1 - V_2$ constraint

$V_1 - V_2 = 1V$

$\Rightarrow V_1 + (-1)V_2 = 1 \quad (1)$

$V_2 - V_3$ constraint

$V_2 - V_3 = 2V$

$\Rightarrow 0.5V_1 + 0.5V_2 + (-1)V_3 = 1 \quad (2)$

Solving (1) & (2) \Rightarrow

$V_1 = 3.5V$, $V_2 = 2.5V$, $V_3 = 1.5V$

Exercise-1

Find I_1, I_2, I_3, V . Use CVD with $V_{D0} = 0.5V$

Step 1: $V_1 - V_2 = 1V$

Step 2: $V_1 - V_2 = 1V$

$\therefore R = 1k\Omega$

$\therefore R = 5k\Omega$

Exercise-2

Find I_1, I_2 . Use CVD with $V_{D0} = 0.5V$

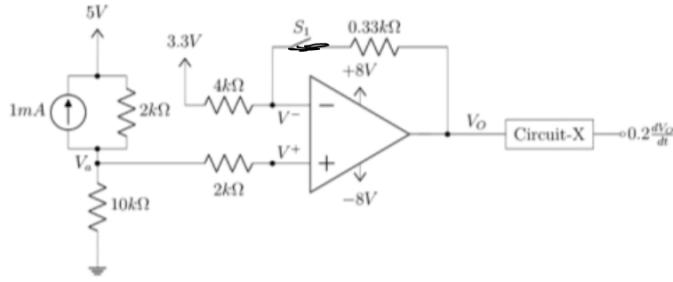
Step 1: $V_1 - V_2 = 1V$

Step 2: $V_1 - V_2 = 1V$

Exercise-2

Mid Term Practice

The circuit diagram has a switch S_1 which is shown to be 'open' in the figure. The output V_O is passed through an unknown block of 'Circuit-X' and a differentiated result is generated.



- [1 mark] State the equation of gain of an inverting amplifier.
- [3 marks] Calculate the values of V_a and V_+ .
- [2 marks] Determine V_O when the switch S_1 is closed.
- [2 marks] Determine V_O when the switch S_1 is open.
- [2 marks] Design the 'Circuit-X'. Assume any value if necessary.

$$(a) (V_T - V_+) A = V_O \quad \text{gain} = -\frac{R_f}{R_i}$$

$$\therefore V^+ = 2.5V$$

$$V^- = 3.3V$$

$$\therefore V^+ > V^-$$

$$\therefore V_O = -8V$$

$$(c) V_b = -\frac{6.33}{4} \times 3.3 = -0.27V$$

$$V^- \left(\frac{1}{A} + \frac{1}{R_f} \right) - \frac{3.3}{4} - \frac{V_o}{0.33} = 0$$

$$\star V^+ = V^- = 2.5V$$

Question: 01

An automatic AC switching system using an Op-Amp comparator that will turn on automatically whenever the temperature is higher than 20° Celsius. The output waveform of an Op-Amp comparator should be between the voltage range of [-4V 5V]. The temperature sensor used with the circuit produces a voltage signal of 1.5V for a temperature value of 20° Celsius.

- Design and draw the comparator circuit with the required inputs. [3]
- Draw the VTC curve for your designed comparator. [2]

Question: 02

Design an **automatic room heater** switching system using an Op-Amp comparator that will turn on automatically whenever the temperature is lower than 20° Celsius. The output waveform of the comparator should be between the voltage range of [-4V 5V]. The temperature sensor produces a voltage signal of 2.5V for a temperature value of 20° Celsius.

- Design and draw the comparator circuit with the required inputs. [3]
- Draw the VTC curve for your designed comparator. [2]

* Linear Amplification only takes place within a valid input range otherwise output will be distorted \rightarrow saturation

The limiting factor of Linear amplification is determined by the power supply to the amplifier.

Features of Ideal Op-Amp

i) Input Resistance ∞ (very high) \rightarrow Input Current 0

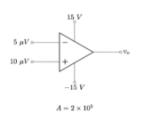
ii) Output Resistance Very low (0)

iii) Amplification factor is very high (∞)

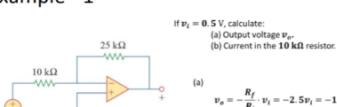
(x)

Op-Amp: Examples

(Ideal Op-Amp)



Example - 1



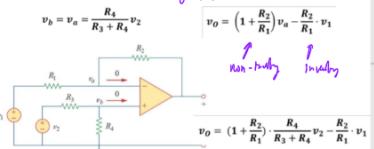
If $V_i = 0.5V$, calculate:
(a) Output voltage V_{op}
(b) Current in the $10k\Omega$ resistor.

$$(a) V_o = -\frac{R_f}{R_i} V_i = -2.5V = -1.25V$$

(b) Current through the $10k\Omega$ resistor is $I = \frac{V_i}{R_i} = \frac{0.5}{10} = 50\mu A$

Difference Amplifier

Very Important Principle



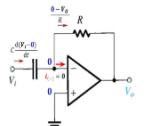
$$v_b = v_a = \frac{R_4}{R_3 + R_4} v_2$$

$$v_o = \left(1 + \frac{R_2}{R_1} \right) v_a - \frac{R_2}{R_1} \cdot v_1$$

Non-inverting
Inverting

Op Amp as Differentiator

Since ideal op-amp, $i_+ = i_- = 0$, so $i_L = i_S$



Review - Capacitor

Since ideal op-amp, $i_+ = i_- = 0$, so $i_L = i_S$

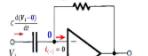
$i_L = \frac{C}{R} \frac{dV_o}{dt} = \frac{C}{R} \frac{d(V_i - V_o)}{dt}$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{1}{R} \frac{dV_o}{dt}$$

$$\Rightarrow V_o = -\frac{1}{RC} \int V_i(t) dt$$

Op Amp as Integrator

Since ideal op-amp, $i_+ = i_- = 0$, so $i_L = i_S$



Review - Capacitor

Since ideal op-amp, $i_+ = i_- = 0$, so $i_L = i_S$

$i_L = \frac{C}{R} \frac{dV_o}{dt} = \frac{C}{R} \frac{d(V_i - V_o)}{dt}$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{1}{R} \frac{dV_o}{dt}$$

$$\Rightarrow V_o = -\frac{1}{RC} \int V_i(t) dt$$

Example 8

Observe the following Figure. If $V_i = 5 \sin(6t)$. Find the value of V_o

$$V_o = -i_L \frac{dV_o}{dt}$$

$$\Rightarrow V_o = -\frac{1}{R} \frac{dV_o}{dt}$$

$$\Rightarrow V_o = -\frac{1}{R} \frac{dV_o}{dt}$$

$$\Rightarrow V_o = -\frac{1}{RC} \int V_i(t) dt$$

$$\Rightarrow V_o = -\frac{1}{RC} \int 5 \sin(6t) dt$$

$$\Rightarrow V_o = -\frac{1}{RC} \left[-\frac{5}{6} \cos(6t) \right]$$

$$\Rightarrow V_o = \frac{5}{6} \frac{1}{RC} \cos(6t)$$

$$\Rightarrow V_o = \frac{5}{6} \frac{1}{1 \mu F \cdot 1 M\Omega} \cos(6t)$$

$$\Rightarrow V_o = 8.33 \cos(6t)$$

Lecture-9

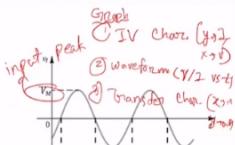
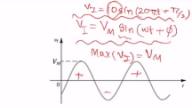
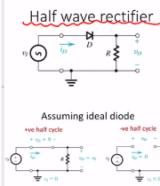
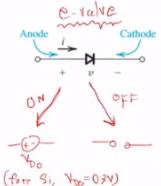
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Monday

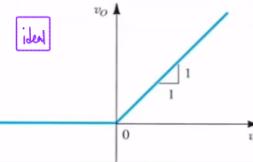
Diode ON: $i > 0, v = V_D$

Diode OFF: $v \leq V_D, i = 0$

Application
① Rectifier
② Logic gate



Reminder: Transfer characteristics is a plot for a circuit's output vs input
For $v_I > 0, v_O = v_I \Rightarrow y = x$
For $v_I \leq 0, v_O = 0 \Rightarrow y = 0$



Half wave rectifier

$$I_D = \frac{v_i - v_D}{R}$$

So diode on when $I_D > 0$ hence when $v_i > v_D$
When ON, i.e., $v_i > v_D, v_o = v_i - v_D = y = x - v_D$

Half wave rectifier

$$I_D = \frac{v_i - v_D}{R}$$

So diode on when $I_D > 0$ hence when $v_i > v_D$
When ON, i.e., $v_i > v_D, v_o = v_i - v_D \Rightarrow y = x - v_D$
When OFF, i.e., $v_i \leq v_D, v_o = 0 \Rightarrow y = 0$

Real diode

$$I = 0, v_D = 0.7 \text{ V}$$

Half wave rectifier

$$I_D = \frac{v_i - v_D}{R}$$

Standard: Use to utilize the -ve half cycle even though no power loss.

Half wave rectifier (Real)

$$I_D = \frac{v_i - v_D}{R}$$

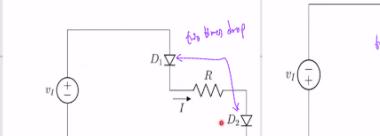
So diode on when $I_D > 0$ hence when $v_i > v_D$
When ON, i.e., $v_i > v_D, v_o = v_i - v_D = y = x - v_D$
When OFF, i.e., $v_i \leq v_D, v_o = 0 \Rightarrow y = 0$

Half wave rectifier

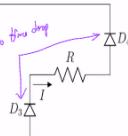
$$I_D = \frac{v_i - v_D}{R}$$

Standard: Use to utilize the -ve half cycle even though no power loss.

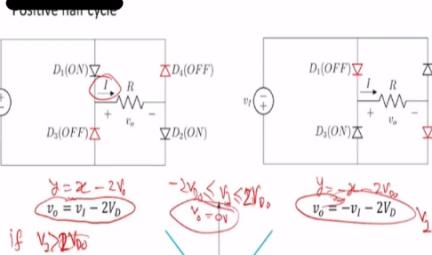
First improvement: Full wave rectifier
Positive half cycle



First improvement: Full wave rectifier
Negative half cycle



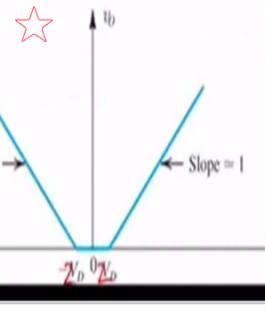
First improvement: Full wave rectifier
Positive half cycle



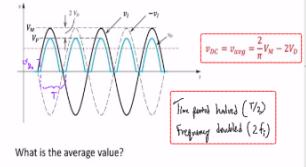
Half wave rectifier

What is the average value? Derivation

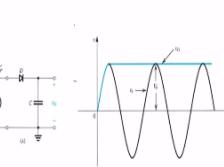
$$\begin{aligned} v_{DC} &= v_{avg} = \frac{1}{T} \int_0^T v_o dt \\ &= \frac{1}{T} \int_0^{T/2} (V_M \sin \omega t - V_D) dt + \frac{1}{T} \int_{T/2}^T 0 dt \\ &= \frac{1}{T} \int_0^{T/2} (V_M \sin \omega t - V_D) dt - \frac{1}{T} \int_{T/2}^T V_D dt \\ &= \frac{1}{T} V_M \times \frac{T}{\pi} - \frac{1}{T} [V_D \times \frac{T}{2}] \\ &= \frac{1}{\pi} V_M - \frac{1}{2} V_D \end{aligned}$$



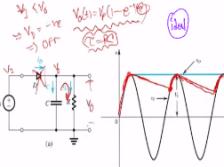
First improvement: Full wave rectifier



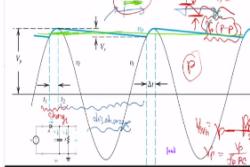
Second improvement: Capacitor smoothing



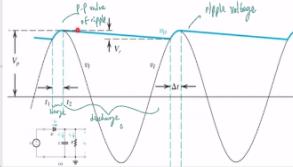
Second improvement: Capacitor smoothing



Second improvement: Capacitor smoothing



Second improvement: Capacitor smoothing



When $v_o > v_{out}$
 $\Rightarrow v_o = v_c$
Block OFF
- capacitor can't charge
to its charging
 $v_o(t) = v_p(1 - e^{-t/\tau})$
 $\tau = RC$

Second improvement: Capacitor smoothing

Second improvement: Capacitor smoothing

Summary

Without Capacitor

With Capacitor

$$\text{Ripple Factor, } r = \frac{V_r(\text{rms})}{V_{dc}}$$

$$V_{rms} = \frac{V_p}{\sqrt{2}} \quad (\text{of sine wave plot of the ripple})$$

$$V_r(\text{rms}) = \frac{V_p(1-R)}{2\sqrt{2}} \quad (\text{peak voltage dropping})$$

$$I_{DC} = \frac{V_{dc}}{R}$$

Only if $V_d < V_m$ A measure of the fluctuating components is given by the ripple factor r , which is defined as

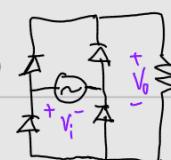
$$r = \frac{\text{rms value of alternating components of the output wave (multimeter in AC mode)}}{\text{average value of the output wave (multimeter in DC mode)}}$$

Larger ripple factor means the AC components of the output wave is larger compared to the DC components. Hence, there fluctuation in the output wave is large. Smaller ripple factor means the AC components of the output wave is smaller compared to the DC components. Hence, there fluctuation in the output wave is small. So, the lower the value of the ripple factor, the better the rectifier.

Example - Analysis (Circuit will be given. Find parameters)

A voltage waveform $v_i = 8\sin(200\pi t)$ is input to a full-wave rectifier. A resistance of $R = 500\Omega$ is connected at the load. [Assume that the diodes used in the circuit have a forward drop of 0.8V].

- (a) Draw the circuit of the full wave rectifier. Label the input and output voltages properly. [1]
- (b) Draw the waveforms of the input and output voltages. What are the peak values of input and output? Show them in the graph. [1+1]
- Now a 10 μF capacitor is connected in parallel with the load.
- (c) Find the frequency of the input signal and the frequency of the ripple. [0.5+0.5]
- (d) Find the peak-to-peak voltage of the output voltage. [1.5]
- (e) Find the DC value of the output voltage. [1.5]
- (f) If we want to reduce the ripple to 1% of the input peak voltage what value of capacitor should we use? [2]



Without Capacitor	With Capacitor
Output Peak, V_p	$V_p = V_{dc}$
Output average, V_{avg}	$V_m = \frac{V_p}{2}$
Peak to Peak ripple, V_{pp}	$V_{pp} = \frac{V_p}{2}$
RMS of Ripple, V_{rms}	$V_{rms} = \frac{V_p}{\sqrt{2}}$
Output average, V_{avg}	$V_{avg} = V_p - \frac{V_{rms}}{2}$

$$\text{less ripple factor means better rectifier}$$

better rectifier

$$I_{DC} = \frac{V_{dc}}{R}$$

Only if $V_d < V_m$

$$(b) V_m = 8V \quad (\text{input})$$

$$V_p = V_m - 2V_0$$

$$= 8 - 2(0.8)$$

$$= 6.4V \quad (\text{output})$$

$$V_{rms} = \frac{V_p}{\sqrt{2}} = \frac{6.4}{\sqrt{2}} = 4.5V$$

$$V_{avg} = \frac{V_p}{2} = \frac{6.4}{2} = 3.2V$$

$$(c) \omega = 200\pi \quad \therefore f_r = 2\pi f \quad (d) V_R(P-L) = \frac{V_p}{f_R R C} = \frac{6.4}{2000 \times 50 \times 10^3 \times 10 \times 10^{-6}} = 0.0069 \quad (e) V_{DC} = V_p - \frac{V_R(P-L)}{2} = 6.4 - \frac{0.0069}{2} = 6.39V$$

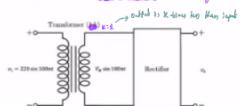
$$2000\pi = 2\pi f \quad = 2 \times 1000 \quad \therefore f_r = 1000 \text{ Hz}$$

$$= 2000 \text{ Hz}$$

$$(f) V_m = 8V \quad 0.08 = \frac{V_p}{f_R R C} = \frac{6.4}{2000 \times 50 \times 10^3 \times 10^{-6}}$$

$$V_R(P-L) = 8 \times 10^{-6} \quad \therefore 0.08V \quad \therefore C = 0.8 \mu F$$

Example - Design → Design a circuit



Here the input v_i is connected to the wall outlet with maximum voltage of 220 V and a frequency f_i of 50 Hz (hence $\omega_i = 2\pi f_i = 314\text{ rad/s}$). The function of the transformer is to reduce the voltage v_i by a factor of 4 while keeping the signal shape intact. This means that the output of the transformer (hence the input of the rectifier) will still be a sinusoid with frequency $f_i = 50\text{ Hz}$ but with amplitude

$$V_M = \frac{220}{4} = 55V$$

The output of the rectifier is connected to the phone to be charged. The output voltage, v_{o1} , must have the following criteria:

- Average or DC voltage, $V_{DC} = V_{o1} = 6V$
- Maximum output peak to peak ripple voltage, $V_{pp(o1)} = 0.5V$
- Output ripple frequency, $f_r = 50\text{ Hz}$

Question:
a. Which type of zener diode you can use here? Why?
b. Assuming $R = 10\text{ k}\Omega$ design the rectifier, i.e., find the value of C of the transformer and C for the zener.

$$(a) \text{ so } f_r = f_i = 50 \text{ Hz}$$

hence half wave rectifier



$$\cdot V_{DC} = 6V \quad \cdot f_r = 50\text{ Hz} \quad \cdot V_{DC} = V_p - \frac{V_R(P-L)}{2} \quad \cdot k = \frac{220}{V_m} = \frac{220}{55} = 4$$

$$\cdot V_R(P-L) = 0.5V$$

$$\# 6 = V_p - \frac{0.5}{2} \quad \# 0.5 = \frac{6.3}{50 \times R_C}$$

$$V_p = 6.3V$$

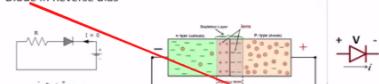
$$\therefore V_m = V_p + V_0 = 6.3 + 0.7 = 7V$$

$$R_L = \frac{6.3}{50 \times 0.6} = 0.12\text{ k}\Omega$$

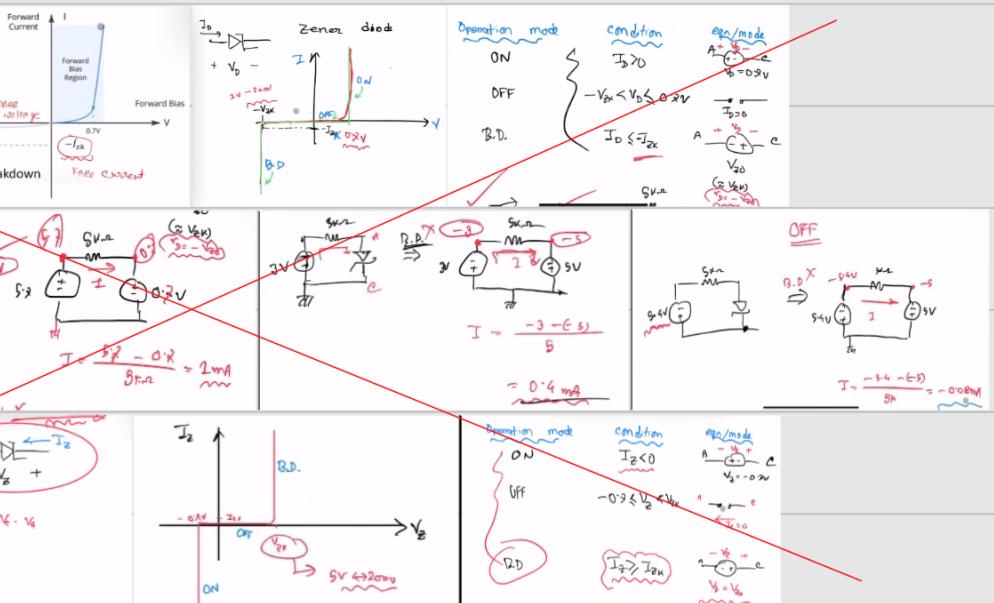
$$C = 1\text{ mF} \quad (\text{usually } 1\text{ mF})$$

$$\therefore R = 10\text{ k}\Omega$$

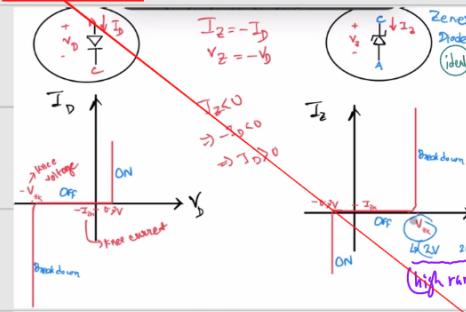
Diode in Reverse Bias



$$I = I_s \left(\exp \frac{V_d}{nV_T} - 1 \right) \approx -I_s$$

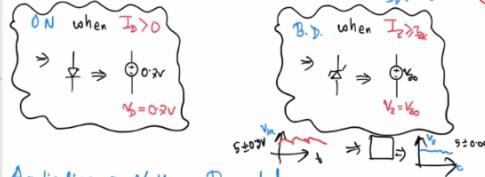


Zener Diode

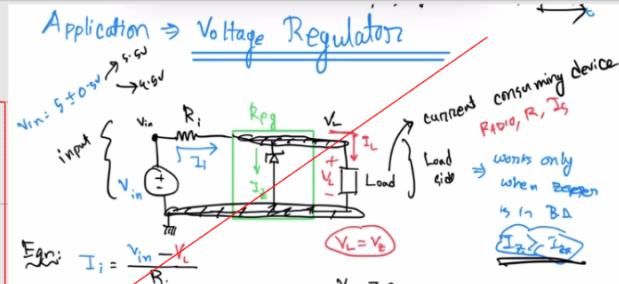


L-11 | Part-01

Out of Syllabus



when using diode V_D , its constant e.g. 0.7V which might not be enough for the load, hence we need a higher voltage! Zener diode behaves like a voltage source in breakdown region but the voltage can be controlled during fabrication.



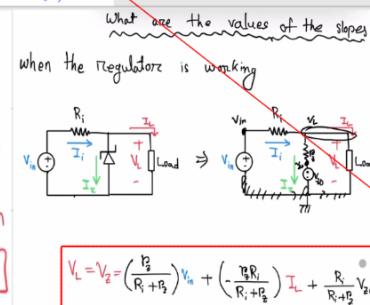
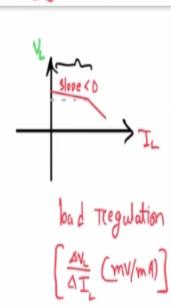
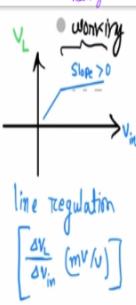
For regulators to work, Zener MUST be in Breakdown $\Rightarrow I_Z > I_{ZK}$

This means $\begin{cases} \textcircled{1} V_{in} \text{ should be high} \\ \textcircled{2} I_L \text{ should be low} \end{cases} \quad \left\{ \text{For regulation to work properly} \right.$



Remember: $V_{in} \uparrow \Rightarrow I_Z \uparrow$
 $I_L \uparrow \Rightarrow I_Z \downarrow$

Design Guideline: Make sure regulator works even in the worst case scenario



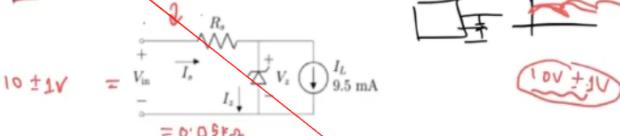
$$V_L = V_2 = \frac{R_2}{R_1 + R_2} V_{in} + \left(-\frac{R_2 R_1}{R_1 + R_2} \right) I_L + \frac{R_1}{R_1 + R_2} V_{Z0}$$

performance measure

L-11 | Part-2

Example

The output of rectifier has a DC value of 10 V and a fluctuation of ± 1 V. This voltage is fed as the input V_{in} into the voltage regulator shown below:



The zener diode is specified as $r_z = 50 \Omega$ and $V_{z0} = 8$ V. The knee current of the zener is 0.5 mA.

(a) What can be the minimum and maximum values of the input voltage V_{in} ?

(b) In worst case condition, find the zener current I_z and the zener voltage V_z .

(c) What is the maximum value of R_s that we can use if the zener has to stay in breakdown even in the worst case condition?

Hint: What is the voltage and current of R_s in the worst case conditions?

(d) Calculate the value of line regulation and load regulation for this regulator.

(e) If the load current increases by 0.5 mA, by how much will the load voltage decrease?

$$\textcircled{1} \min(V_{in}) = 10 - 1 = 9V$$

$$\max(V_{in}) = 10 + 1 = 11V$$

\textcircled{2} worst case

$$V_{in} = \min(V_{in}) = 9V$$

$$\textcircled{3} I_L = \max(I_L) = 9.5mA$$

$$\textcircled{4} I_z = I_{ZK} = 0.5mA$$

$$R_s = \frac{1V}{10mA} = 0.1k\Omega$$

$$I_S = I_z + I_L = 0.5 + 9.5 = 10mA$$

$$\frac{V_s}{R_s} = \frac{V_s}{0.1k\Omega} = 10V$$

$$\textcircled{5} I_z = I_{ZK} = 0.5mA$$

$$V_2 = V_{z0} + I_z R_s = 8 + 0.5 \times 0.05 \approx 8.025V \approx 8V$$

$$\textcircled{6} \text{line regulation} = \frac{\Delta V_L}{\Delta V_{in}} = \frac{1V}{10V} = \frac{0.1}{10} = 0.01 = 1\%$$

$$= \frac{0.05}{0.05 + 0.1} = 0.333V/V$$

$$= 333mV/V$$

$$\text{load regulation} = \frac{\Delta V_L}{\Delta I_L} = \frac{-R_s}{R_s + R_L} = \frac{-0.05}{0.05 + 10} = -0.005 = -0.5\%$$

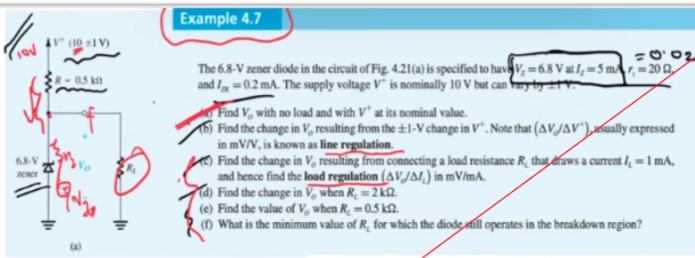
$$= \frac{-0.05 \times 0.5}{0.05 + 0.5} = -0.049 = -4.9\%$$

$$= -33.3mV/mA$$

$$\Delta I_L = 0.5mA$$

$$\Rightarrow \Delta V_L = -33.3 \times 0.5 = -16.65mV$$

$$= -33.3 \times 0.5 = -16.65mV$$



$$\textcircled{1} V_o = 6.8 = V_{z0} + I_z R_s$$

$$\Rightarrow 6.8 = V_{z0} + 5 \times 0.02$$

$$\Rightarrow V_{z0} = 6.8V$$

$$R_s = 0.02k\Omega$$

$$I_z = \frac{10 - 6.8}{0.5 + 0.02} = 6.35mA$$

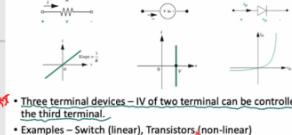
$$V_o = V_{z0} + I_z R_s = 6$$

$$R_s = \frac{0.02}{0.02} = 100\Omega$$

Zener must be in breakdown for regulator to work

Lecture - 13Three terminal devices

- Two terminal devices have fixed IV characteristics

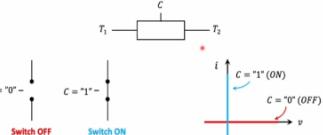


Key: Three terminal devices - IV of two terminal can be controlled using the third terminal.

- Examples - Switch (linear), Transistors (non-linear)

Switch - IV Characteristics

- IV characteristics between terminal T_1 and T_2 is controlled by C



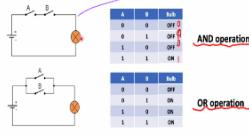
Key: $C = 0^*$ - Switch OFF $C = \infty^*$ - Switch ON $C = 0$ - Switch ON

Switch - Types

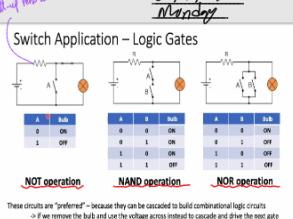
- Depending on the control, the switch can be
 - Analog: Controlled using physical toggle/button
 - Digital: Controlled using voltage or current. Example - MOSFET (voltage controlled), BJT (current controlled)

Switch Application - Logic Gates

- We can use switches to build logic gates



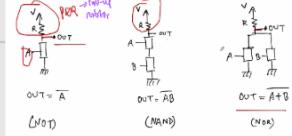
Key: $A = 0$, $B = 0$ → OUT = 0
 $A = 1$, $B = 0$ → OUT = 1
 $A = 0$, $B = 1$ → OUT = 1
 $A = 1$, $B = 1$ → OUT = 1



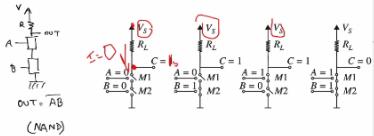
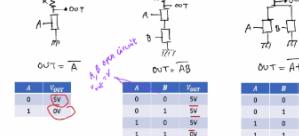
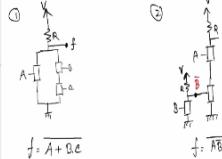
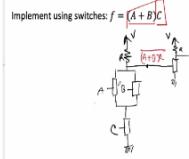
These circuits are "preferred" because they can be cascaded to build combinational logic circuits
or if we remove the bulb and use the voltage across instead to cascade and drive the next gate

Switch Application – Logic Gates

Alternative representations:

Switch Application – Logic Gates

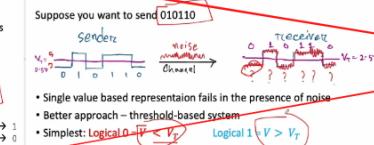
Alternative representations:

Switch Application – Logic GatesSwitches (Transistor)ExamplesExampleDigital Representation

- Binary → Two states (0/False, 1/True)

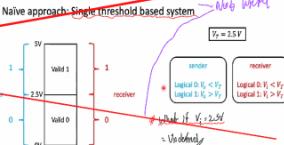
- Binary variables in circuit, need to use two states of device/parameters

Voltage	Current	State
5V → 1	2mA → 1	ON → 1
0V → 0	3mA → 0	OFF → 0
0V → 1	Low resistance → 1	
3.3V → 0	High resistance → 0	

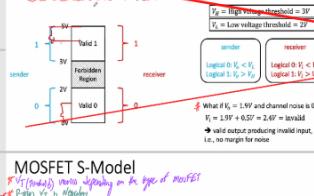
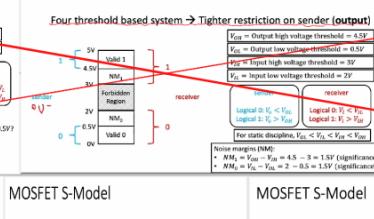
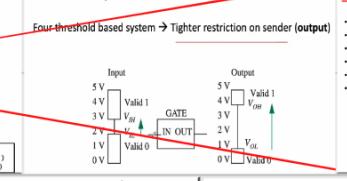
Digital RepresentationStatic Discipline

- Specification for digital devices
 - Requires devices to adhere to common representation to ensure that valid input produces valid output

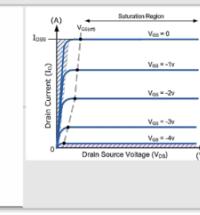
- This means, if
 - Sender sends "0" → Receiver interprets as "0"
 - Sender sends "1" → Receiver interprets as "1"

Static Discipline

Key: $V_d = 3.5V$
Out of syllabus: Static Discipline Out of syllabus

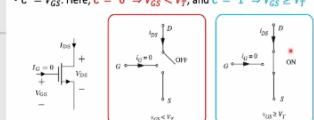
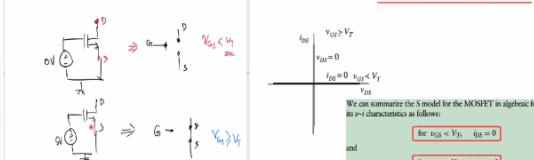
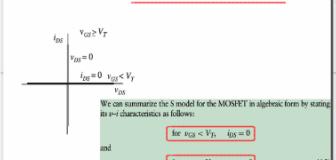
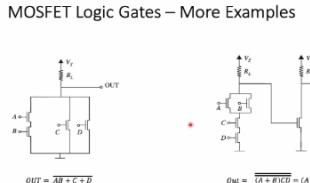
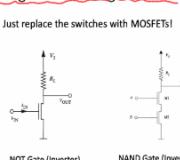
Static DisciplineDouble threshold based systemStatic DisciplineStatic DisciplineTransistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types - Voltage Controlled, Current Controlled
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are voltage controlled
- Control, $C = V_{GS}$. The IV characteristics ($I_{DS} \text{ vs } V_{DS}$) depends on V_{GS}
- Actual dependency is complex
- Will start with a simple (but approximate one - 5 Model (Switch Model))
- See notes for more details

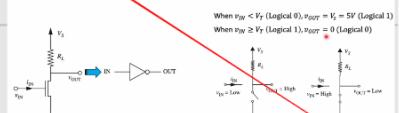
MOSFET S-Model

Key: V_{GS} (gate-to-source voltage) is the type of mosfet

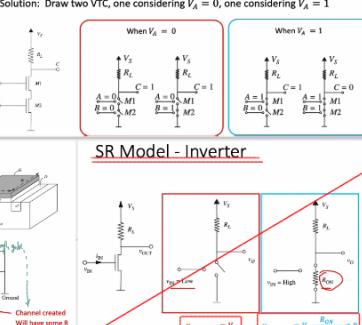
- The MOSFET (approximately) behaves like a switch

MOSFET S-ModelMOSFET S-ModelLogic Gates using MOSFETVoltage Transfer Characteristics (VTC)

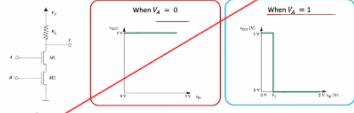
- Reminder: VTC is a graph where x axis = input voltage, y axis = output voltage
- Why? Design logic gates to follow a given static discipline

VTC of NAND gate

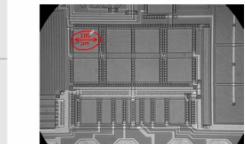
- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering $V_A = 0$, one considering $V_A = 1$

VTC of NAND gate

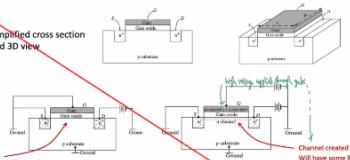
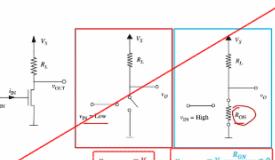
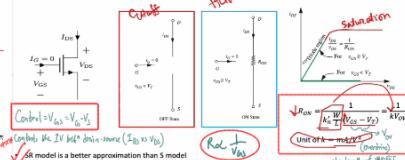
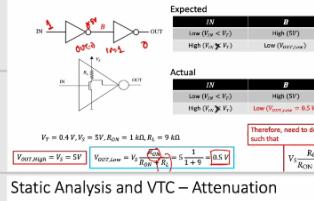
- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering $V_A = 0$, one considering $V_A = 1$



Key: When MOSFET is ON, it behaves like a resistor $\propto \frac{1}{V_{ds}}$

Construction of Real MOSFET

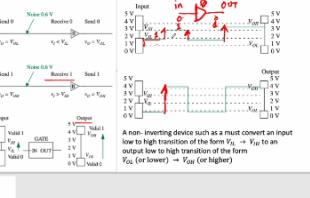
Top view of several real channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a total length of 100 μm. (Photograph Courtesy of Maxim Integrated Products.)

Construction of Real MOSFETSR Model - InverterSR ModelDesign of logic gatesDesign of logic gates - Example

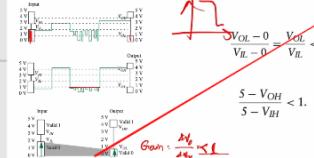
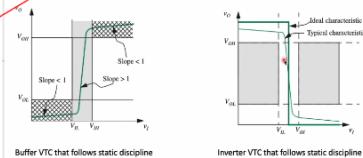
Assume the following values for the inverter circuit parameters: $V_{DD} = 5V$, $V_T = 1V$, $R_{IN} = 10k\Omega$. Assume, further, that $\frac{I_{DS}}{I_{DS(on)}} < 3$ for the MOSFET. Determine the size of the MOSFET so that the inverter gate output for a logical 0 is able to switch off the MOSFET of another inverter.

Static Analysis

- General design principle - design in such a way that the device adheres to static discipline
- Valid input must produce valid output
- How to check? Analyze the voltage transfer characteristics.
- In short, the VTC should (1) provide $|Gain| > 1$ during transition (2) provide attenuation other time (3) be non-linear

Static Analysis and VTC - Gain

Key: $V_{DD} > V_{DS} - V_{GS}$, $\Delta V = V_{DD} - V_{DS}$.

Static Analysis and VTC - AttenuationStatic Discipline and VTCStatic Discipline and VTC - Example

The device company Yehia Microelectronics, Inc. has developed a new process technology that is able to produce large quantities of CMOS logic inverters that have a static discipline. The VTC at given drain voltages is shown below. Yehia sales team finds that the VTC is very similar to the SR model. However, the SR model does not take into account the following threshold voltages:
 1. $V_{DS(on)} = 3.5V$, $V_{GS(on)} = 1.5V$, $V_{TP} = 4V$
 2. $V_{DS(on)} < V_{DS} < V_{DS(off)}$
 3. $V_{GS(on)} < V_{GS} < V_{GS(off)}$
 4. $V_{TP} < V_{DS} < V_{TP(on)}$
 Yehia sales team asks their development engineers to determine whether the VTC satisfies the static discipline under which DISCO's system operates.

Help the Sales team make the decision

$$NM_D = V_{DS(on)} - V_{DS} \quad NM_G = V_{GS(on)} - V_{GS}$$

$$NM_D = V_{DS(on)} - V_{DS} \quad NM_G = V_{GS(on)} - V_{GS}$$

Key: $V_{DD} > V_{DS} - V_{GS}$, $\Delta V = V_{DD} - V_{DS}$.

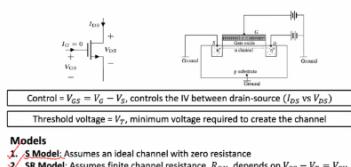
Key: $V_{DD} > V_{DS} - V_{GS}$, $\Delta V = V_{DD} - V_{DS}$.

Key: $V_{DD} > V_{DS} - V_{GS}$, $\Delta V = V_{DD} - V_{DS}$.

Real MOSFET Equation and Method of Assumed State

1-15

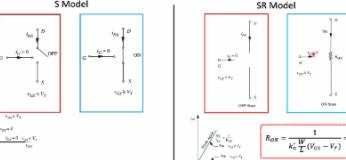
Review - MOSFET



Models

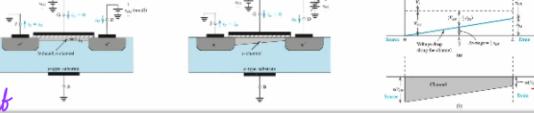
- 1. S Model: Assumes an ideal channel with zero resistance
- 2. SR Model: Assumes finite channel resistance, R_{DN} , depends on $V_{GS} - V_T = V_{OV}$

MOSFET Linear Models



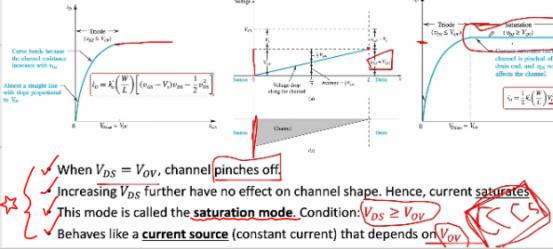
Real MOSFET

- Why $R_{DN} = \frac{1}{k_n \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{k V_{OV}}$? Because channel width $\propto V_{OV}$, and $R \propto \frac{1}{\text{width}}$
- For small V_{DS} , uniform channel, hence fixed R_{DN} , therefore SR model valid.
- As V_{DS} is increased, channel becomes tapered cause $V_{GD} \downarrow$. Resistance \uparrow , slope \downarrow .
- This mode is called the **triode mode**. Condition: $V_{DS} < V_{OV}$

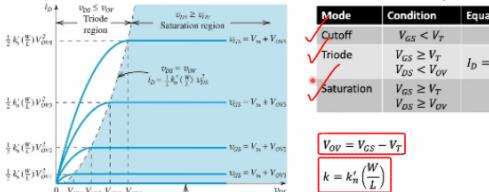


MOSFET acts as a switch in triode region (On) and cutoff region (Off)
 Saturation is generally not used for switch applications. → Information is for amplification → behaves like a current source, is almost constant

Real MOSFET



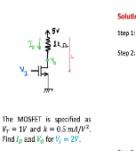
IV Characteristics of Real MOSFET



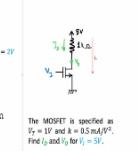
Solving Circuits with MOSFET

- Use Method of Assumed State!
- Three steps:
 - Assume: One of the modes (Cutoff, Triode, Saturation)
 - Solve: Use corresponding equation and KCL+KVL
 - Verify: Check if the conditions of V_{GS} and V_{DS} are satisfied. If not, repeat.
- Might need to solve quadratic equation ($ax^2 + bx + c = 0$).
- If we get two roots, choose the one that's *favorable* to your assumption

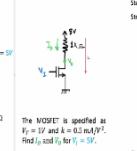
Example 1



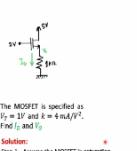
Example 2



Example 2



Example 3



Practice

Question #4 [CO1, CO4]

Analyze the following circuit and find the value of I_D and V_{GS} using the Method of Assumed State. You must validate your assumptions.Hint: Use $I_D = k \frac{W}{L} (V_{GS} - V_T)^2 V_{DS}$ and $V_{GS} = V_D - V_S$ in terms of V_D .

$$\text{No load assume saturation: } I_D = \frac{k}{2} V_{DS}^2 = \frac{3}{2} (1-0)^2 = \frac{3}{2} \text{ mA}$$

And if you assume triode:
 $I_D = k \frac{W}{L} V_{GS} V_{DS} = \frac{3}{2} (1-0)(1-0) = \frac{3}{2} \text{ mA}$

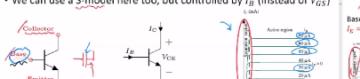
Hint Explanation:
 Assume $I_D = x$. For STD, $I_D = \frac{1}{2} V_{DS}^2$. Here, $V_{DS} = 10 - 5x = 10 - 5x$.
 For STD, $I_D = \frac{1}{2} V_{DS}^2$. Here, $V_{DS} = 10 - 5x = 10 - 5x$.
 Therefore, $I_D = 10 - 5x = 2x$. Solving, $x = 2$. Since $x = 2$ is favorable, smaller value of x is favorable.
 Therefore, $I_D = 10 - 5(2) = 0$. Solving, $I_D = 0$. Therefore, assumption correct.

Current without logic gate not work as (can't switch)
 (No SR Model in BJT)

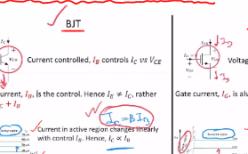
L-16

Bipolar Junction Transistor BJT

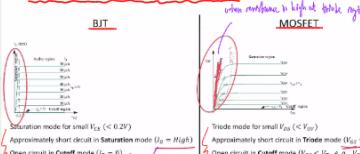
- Current-controlled transistor, 3 terminals - Base Emitter Collector
- IV between C and E (I_C vs V_{CE}) is controlled by base current, I_B
- IV quite similar to MOSFET, but there are some differences
- We can use a S-model here too, but controlled by I_B (instead of V_{GS})



BJT vs MOSFET - Differences

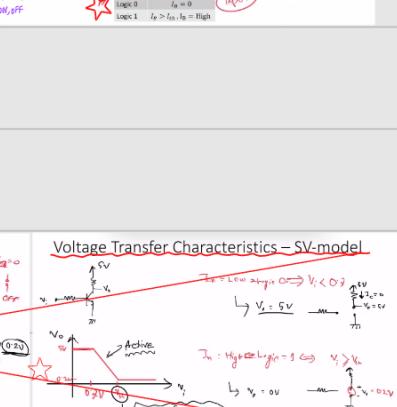


BJT vs MOSFET - Similarities

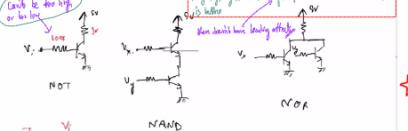


BJT S-Model

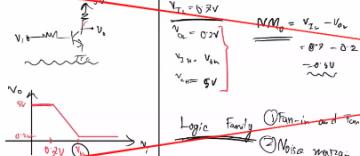
- The BJT (approximately) behaves like a switch \times (V_{CE} small)
- $C = I_B$. Here, $C = "0" \Rightarrow I_B = 0$, and $C = "1" \Rightarrow I_B \geq I_{sat}$
- $I_B = 0$, short circuit. $I_B = High$, open circuit.



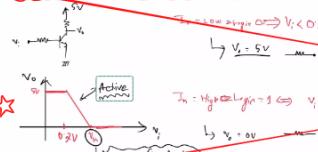
Voltage Controlled Logic Gates



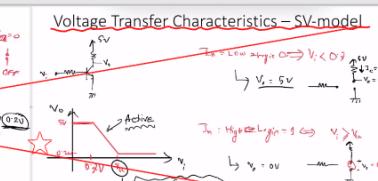
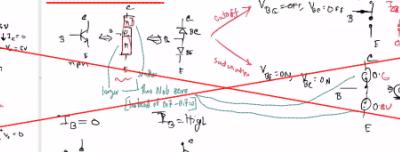
Improving Noise Margin - BJT Inverter



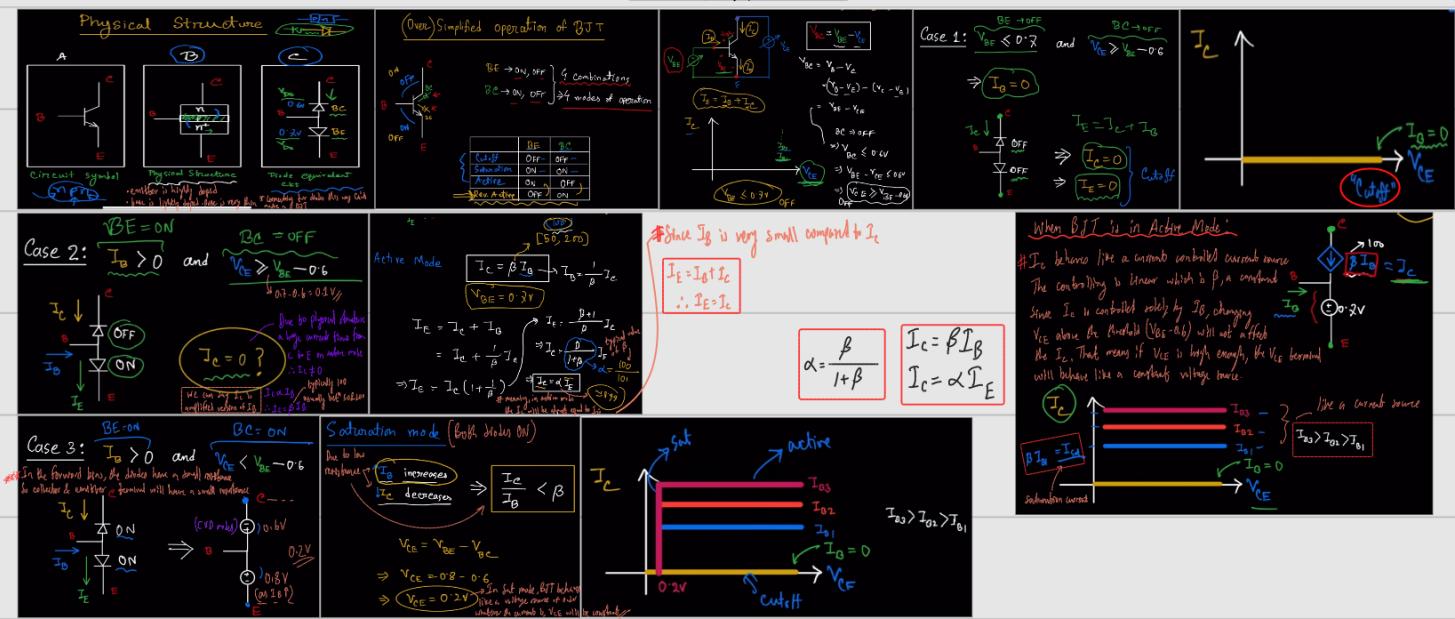
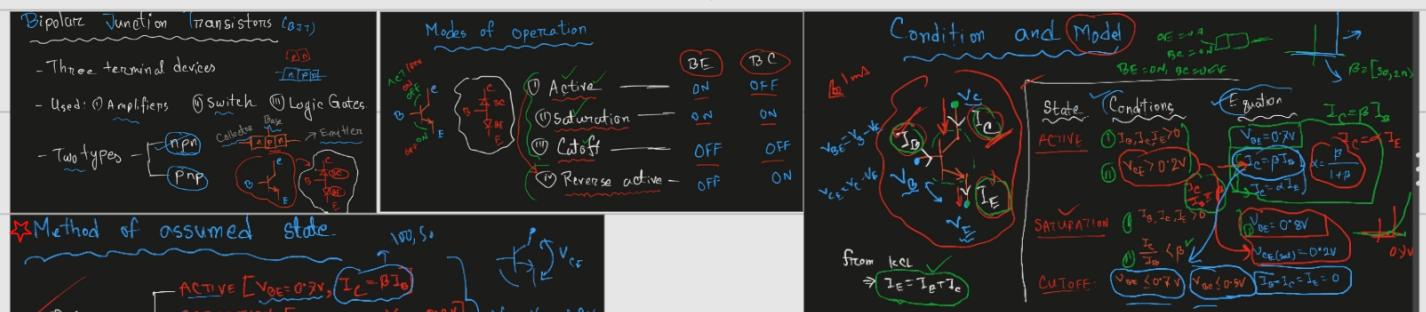
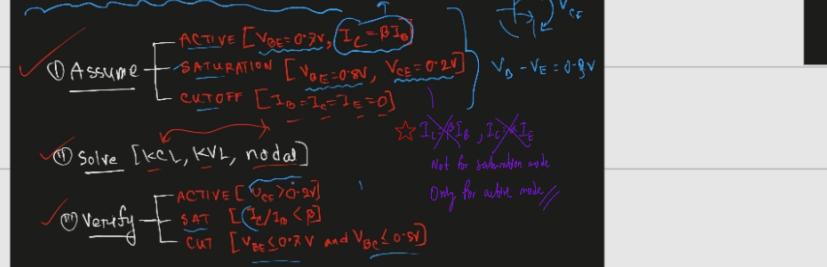
Voltage Transfer Characteristics - S-model



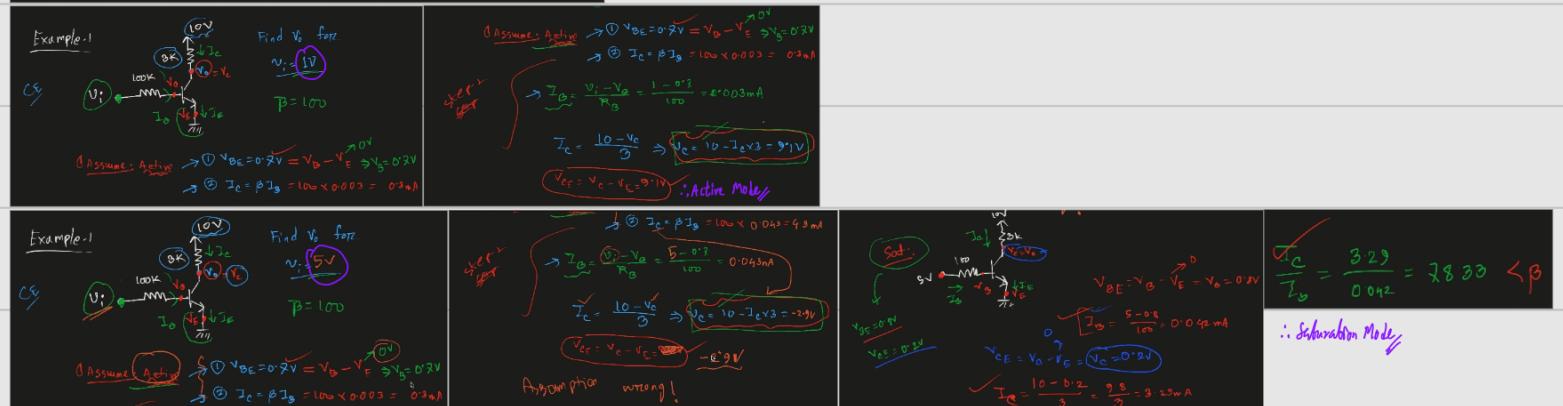
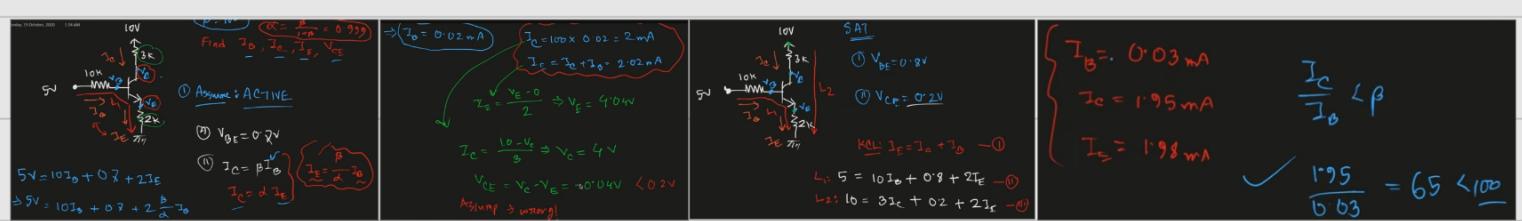
BJT SV Model



BJT acts as a switch in saturation mode (ON) and cutoff region (OFF)
 Active region is used for amplification

L-17 | Part-02**Method of assumed state**

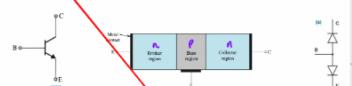
$$I_E = \frac{\beta}{\alpha} I_B$$

**Example**

Amplifiers Using Transistors

Lecture - 18

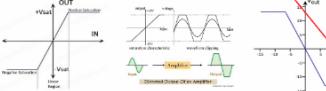
BJT Review



- Cutoff: BE = OFF, BC = OFF
- Active: BE = ON, BC = OFF
- Saturation: BE = ON, BC = ON

Transfer Characteristics of Amplifiers

- $y = mx$, hence straight line going through origin. Here, $m = k$ = gain
- Saturation due to limited power supply. Output cannot be greater than P.S.
- Input must be within a valid input range, otherwise output will be distorted
- For inverting amplifiers, gain is negative. Hence $y = -mx$



BJT Review

- IV between C and E (I_C vs V_{CE}) is controlled by I_B
- When $I_B = 0$, Cutoff, $I_C = I_E = 0$
- When $I_B > 0$, BE will be ON. It will be Active or Saturation.
 - When V_{CE} is High, I_C will be ON. Active mode. Works like a current controlled current source with $I_C = \beta I_B$
 - When V_{CE} is Low, I_C will be ON. Saturation mode. Works like a voltage source $V_{CE} = 0.2V$. Since I_C is fixed and I_C reduces $\frac{I_C}{\beta}$, I_B



BJT Review

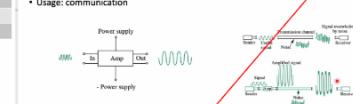
Summary

Mode	Condition	Equation
Cutoff	$I_B = 0$	$I_C = I_E = 0$
Active	$I_B > 0$, and $V_{CE} > 0.2$	$I_C = \beta I_B$
Saturation	$I_B > 0$, and $I_C / I_B < \beta$	$V_{CE} = 0.2V$

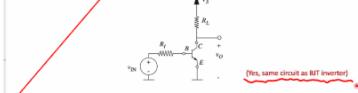


Amplifier

- Linear amplifier $\Rightarrow \text{OUT} = k \times \text{IN}$ k is called the gain of the amplifier
- OUT/IN can be voltage or current
- Amplifier must provide power gain ($P_{OUT} > P_{IN}$), hence need power supply
- Usage: communication



BJT Common Emitter Amplifier



* When BJT is in active mode, $I_{out} = \beta I_{in}$. Here $I_{in} = I_B$ and $I_{out} = I_C$

- R_I converts input voltage (v_{in}) to input current I_B
- R_L converts output current I_C to output voltage (v_o)
- But how does it work? Need to know relation between v_o and v_{in}

Finding VTC of CE Amplifier

KVL: $v_o = V_{CE} = V_S - I_C \times R_L$ (True for any mode)

KVL: $v_{in} = I_B R_I + v_{BE}$ (True for any mode) $\Rightarrow I_B = \frac{v_{in} - v_{BE}}{R_I} = \frac{v_{in} - 0.7}{R_I}$

Cutoff: $I_B = 0 \Rightarrow v_{BE} \leq 0.7V \Rightarrow v_{in} \leq 0.7V$

$v_o = V_S - 0.7 \times R_L = V_S$ (since in cutoff $I_C = 0$)

Active: $v_{CE} = v_o > 0.2V$

$v_s - I_C R_L > 0.2V \Rightarrow I_C < (V_S - 0.2) / R_L$

Since $I_C = \beta I_B \Rightarrow I_C < (V_S - 0.2) / \beta R_L$

Since $v_{in} = I_B R_I + 0.7 \Rightarrow v_{in} < 0.7 + \left(\frac{V_S - 0.2}{\beta R_L}\right) R_I$

So as long as $0.7 < v_{in} < 0.7 + \left(\frac{V_S - 0.2}{\beta R_L}\right) R_I$ BJT will be in Active and

$v_o = V_S - I_C R_L \Rightarrow v_o = V_S - \beta I_B \times R_L$

$\Rightarrow v_o = V_S - \frac{\beta(v_{in} - 0.7)}{R_I} \Rightarrow v_o = \left(V_S + \frac{0.7\beta R_L}{R_I}\right) - \frac{\beta R_L}{R_I} v_{in}$

Saturation: $v_{in} > 0.7 + \left(\frac{V_S - 0.2}{\beta R_L}\right) R_I \Rightarrow v_o = v_{CE} = 0.2V$

VTC of CE Amplifier



Assume that $R_I = 100 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, $\beta = 100$, and $V_S = 10 \text{ V}$.

$$\Rightarrow 0.7 + \left(\frac{V_S - 0.2}{\beta R_L}\right) R_I = 0.7 + \left(\frac{10 - 0.2}{100 \times 10 \text{ k}\Omega}\right) 100 \text{ k}\Omega = 1.68 \text{ V}$$

And $v_o = \left(V_S + \frac{0.7\beta R_L}{R_I}\right) - \frac{\beta R_L}{R_I} v_{in} \Rightarrow v_o = 17 - 10 v_{in}$

$v_{in} < 0.7 \quad v_o = 10 \quad \text{Cutoff mode}$

$0.7 < v_{in} < 1.68 \quad v_o = 17 - 10 v_{in} \quad \text{Active mode}$

$v_{in} \geq 1.68 \quad v_o = 0.2 \quad \text{Saturation mode}$

Example 1

Consider the BJT common emitter circuit with $\beta = 100$, $R_I = 100 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, and $V_S = 10 \text{ V}$

We want to set bias the point in such a way that the DC portion of the input, i.e., $v_x = 1.2 \text{ V}$.

Under small signal approximation, if the input $v_{in} = v_x + v_i(t)$, the output will be $v_o = v_y + v_i(t)$.

This means the output will be some DC value v_y plus the amplified version of the small signal $v_i(t)$.

Here assume that $v_i = 0.1 \cos \omega t$.

• What is the value of DC part of the output, i.e., v_y ?

$$v_x = 1.2, \text{ therefore } v_y = \left(V_S + \frac{0.7\beta R_L}{R_I}\right) - \frac{\beta R_L}{R_I} v_x = 5$$

• What will be the value of gain k under small signal approximation?

$$k = -\frac{\beta R_L}{R_I} = -10$$

• What is amplitude (peak-to-peak) of the input small signal waveform $v_i(t)$?

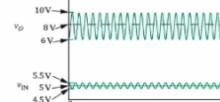
$$\max = 0.1 \text{ V}, \min = -0.1 \text{ V}. \text{ Therefore, peak-to-peak amplitude} = 0.2 \text{ V}$$

• What is amplitude (peak-to-peak) of the output small signal waveform?

$$\text{Amplitude of output} = |k| \times \text{Amplitude of input} \Rightarrow 10 \times 0.2 = 2 \text{ V}$$

Example 2

The input voltage of a common source amplifier is given as $v_{in} = V_x + v_i(t)$ and the output voltage is given $v_o = V_y + v_i(t)$. Here, $v_i(t)$ is a sinusoidal voltage with amplitude a , V_x is the input DC offset voltage, V_y is the output DC offset voltage. The input and output waveforms are given below. Notice the output small signal is inverted compared to input small signal. Hence, the small signal gain, k , will be negative.



• Design the circuit, i.e., find the value of V_S , R_I , and R_L to achieve given input-output voltage relation. Given $\beta = 100$.

$$k = -4 = -\frac{\beta R_L}{R_I} = \frac{\beta R_L}{R_I} = 4 \Rightarrow R_L = 0.04 \text{ k}\Omega$$

$$\text{Let } R_I = 100 \text{ k}\Omega \Rightarrow R_I = 4 \text{ k}\Omega$$

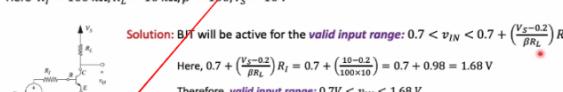
$$V_y = \left(V_S + \frac{0.7\beta R_L}{R_I}\right) - \frac{\beta R_L}{R_I} V_x = 8 = (V_S + 0.7 \times 4) - 4 \times 5$$

$$\Rightarrow V_S = 8 + 20 = 28 = 25.2 \text{ V}$$

Example 3

Choose an operating point for the amplifier below to maximize the input voltage swing.

Here $R_I = 100 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, $\beta = 100$, $V_S = 10 \text{ V}$

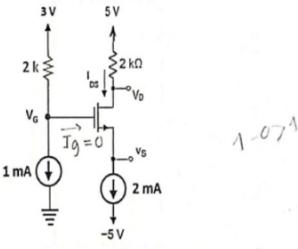


- What is the amplitude of the input small signal $v_i(t)$? 0.5 V
- What is the amplitude of the output small signal? 2 V
- Hence, what is the small signal gain k ? $k = -\frac{2}{0.5} = -4$
- From the above graph, what is the value of input DC voltage V_x and the output DC voltage V_y ?

$$V_x \approx 5, V_y = 8$$

Note: $V_y = 5$ is midway between the valid output range: $0.2 \leq v_o \leq 10$

Question 01 (CO3) points)

Refer to the MOSFET in the figure below where $V_T = 1 \text{ V}$ and $K = k' W/L = 4 \text{ mA/V}^2$.

Practice

(a) $V_D \left(\frac{1}{2} \right) - \frac{3}{2} + 1 = 0$

$V_D = 1 \text{ V}$

$I_{DS} = 2 \text{ mA}$

(b) $\frac{5 - V_D}{2} = I_{DS}$

$\therefore V_D = 1 \text{ V}$

(c) Assume saturated

$V_{DS} > V_T$

$I_{DS} = \frac{1}{2} K V_{DS}^2$

$= V_D - V_S - V_T$

$= 1 - 1 - 1$

$V_{DS} = -V_D$

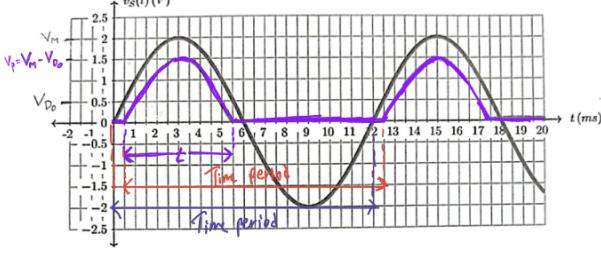
$\therefore V_{DS} = -1 \text{ V}$

If $V_D = 1 \text{ V}$ # If $V_D = -1 \text{ V}$

$V_{DS} = 1 - 1 < V_T \quad V_{DS} = -(-1) = 2$

- (a) [CO1] Calculate the value of the gate voltage V_G and the drain-source current I_{DS} .
 (b) [CO2] Calculate the drain voltage V_D .
 (c) [CO2] Analyze the circuit to find the source voltage V_S . [Use the method of assumed states.]

Question 01 Out of 02:

 $v_S(t)$ is the input voltage to a half wave rectifier without filter capacitor.

- (a) [4 marks] Assuming a cut-in voltage of 0.5 V for the diode used in the rectifier, approximately draw the output voltage waveform on the same grid.
 (b) [2 marks] Determine the approximate average of the output voltage, V_{avg} or V_{DC} .
 (c) [2 marks] Determine the fraction of time within a cycle the diode is conducting [Determine from the above graph]

Bonus: Determine the average or DC voltage if a capacitor of $1 \mu\text{F}$ is connected in parallel with the load resistor. [2] $R_L = 10 \text{ k}\Omega$

Question 02 Out of 02:

- (a) Draw the IV curve of a MOSFET considering the S-model only. [2]
 (b) Design a circuit using ideal MOSFETs (S-model) to implement the logic function: [3]

(1) $F = (A + B) \cdot (\bar{B} + B \cdot C)$

1) (a) $V_P = V_m - V_{D0}$
 $= 2.05$
 $= 1.5V$

2) (a) i_D ON $V_{G1} > V_T$
 $V_{D1} = 0$
 $i_D = 0$ OFF
 $V_{G1} < V_T$

(b) $V_{DC} = \frac{V_m}{\pi} - \frac{V_{D0}}{2}$

$= \frac{2}{\pi} - \frac{0.5}{2}$

$= 0.387V$

(b) $F = (A + \bar{B}) \cdot (\bar{B} + B \cdot C)$

$= (A + \bar{B}) \cdot (\bar{B} + B \cdot C)$

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Problem 1

- Give a switch-MOSFET implementation of the following logic functions. A, B, C, D, E , and F are Boolean inputs.

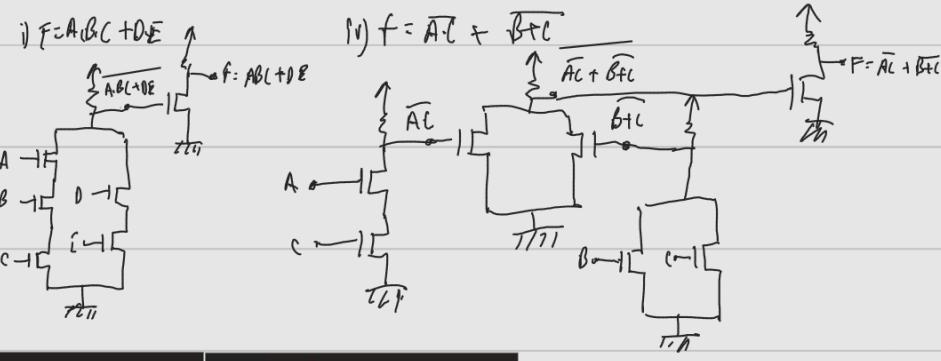
$I. \quad f = A \cdot B \cdot C + D \cdot E$	$VIII. \quad f = (A + B) \cdot (C + D)$
$II. \quad f = \overline{A} \cdot \overline{B} \cdot (\overline{C} + \overline{D})$	$IX. \quad f = (A \cdot B + C) \cdot (E + F)$
$III. \quad f = A \cdot B + \overline{A} \cdot \overline{B}$	$X. \quad f = A \oplus B$
$IV. \quad f = \overline{A} \cdot \overline{C} + \overline{B} \cdot \overline{C}$	$XI. \quad f = \overline{C \cdot (A + B)} \cdot (A + \overline{B} + C)$
$V. \quad f = (A \cdot B + C) \cdot D$	
$VI. \quad f = A \cdot B + C \cdot D$	
$VII. \quad f = A \cdot B \cdot C + D$	★

$$A+B = \bar{A} \cdot \bar{B}$$

$$C \cdot C = C$$

$$\overline{AB} = \overline{A} + \overline{B}$$

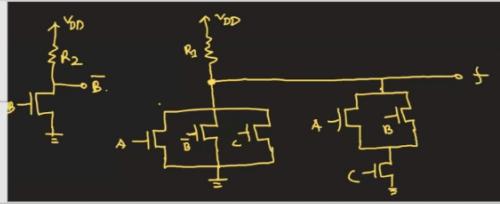
De Morgan's



18/05/2025
Sunday

$$\begin{aligned}
 f &= \overline{AC} + \overline{B+C} = \overline{\overline{AC} + \overline{B+C}} = \overline{\overline{AC}} \cdot \overline{\overline{B+C}} \\
 &= \overline{AC \cdot (B+C)} = \overline{ABC + AC \cdot C} = \overline{A+B} = \\
 &= \overline{ABC + AC} = \overline{AC(B+1)} = \overline{AC}
 \end{aligned}$$

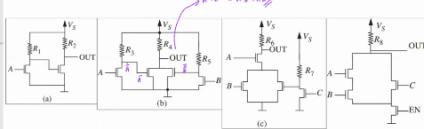
$$\begin{aligned}
 (x) \quad F &= c \cdot \overline{(A+B)} \cdot (A+\overline{B}+C) \\
 &= \overline{c(A+B)} \cdot (A+\overline{B}+C) \\
 &= \overline{c(A+B)} + \overline{(A+\overline{B}+C)}
 \end{aligned}$$



X) $f = A \oplus B = \bar{A}B + A\bar{B}$

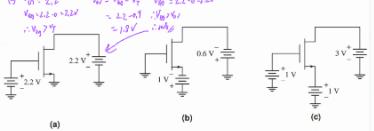
Problem 2

- Write a Boolean expression that describes the function of each of the circuits below



Problem 10

- The threshold voltage for each of the transistors in the following circuit is -0.4 V . Determine the operating region of the transistor in each circuit.



Problem 13

- The transistor in the following circuit has parameters $V_{TN} = 0.5\text{ V}$ and $k_n' = k_p' = 1.6 \text{ mA/V}^2$. Determine V_D .

Analysis:

$V_{DN} = V_D - V_T$ $\forall i > 0$

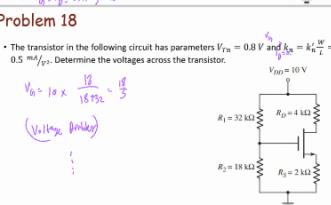
$I_D = I_S \left(\frac{V_D - V_T}{R_D} \right)^2$

$\frac{I_D}{I_S} = \frac{1}{R_D} + L \left(\frac{V_D - V_T}{R_D} - 0.5 \right)^2$

$\frac{I_D}{I_S} = \frac{18 - V_D}{150} + L \left(\frac{V_D - 0.5}{150} - 0.5 \right)^2$

$\therefore I_D = \frac{18 - V_D}{150} \cdot 1.6 \left(\frac{V_D - 0.5}{150} - 0.5 \right)^2$

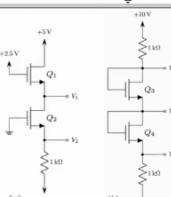
$\therefore V_D = 0.5 \pm \sqrt{18.8V}$



Problem 23

- For the transistors in the following circuits, $V_{TN} = 1\text{V}$ and $k_n = k_p \frac{W}{L} = 2 \frac{\text{mA}}{\text{V}^2}$. Determine V_1 through V_5 .

[Hint: Form simultaneous equations consisting of voltage variables for circuit in (b).]



For the transistors in the following circuits, $V_{BE} = 1V$, $I_{CQ} = \frac{I_B}{\beta}$, $I_C = \beta I_B$, $\alpha = \frac{\beta}{\beta + 1}$. Determine V_1 through V_5 . List four simultaneous equations consisting of voltage variables for circuit in (b).

(a)

(b)

$I_{D1} = \frac{10 - V_3}{1} \text{ A}$

$I_{D2} = \frac{V_5 - 0}{1} = V_5 \text{ A}$

(b) $I_{D1} = \frac{1}{2} \times 2 (V_3 - V_4 - 1)^2 \text{ A}$

$V_3 - V_4 - 1 = V_4 - V_3 - 1$

$V_5 = 2V_4 - V_3$

$\therefore V_4 = 5V$

$V_5 = 10 - V_3$

$V_5 = (V_4 - V_3 - 1)^2$

$V_3 - V_4 - 1 = \pm (V_4 - V_3 - 1)$

$V_3 = 2.45V, 6.55V$

sat: $V_{BS} \uparrow V_J \downarrow$ if $V_{SD} \downarrow$

$\boxed{V_3 = 2.45V}$

$V_5 = 10 - V_3$

$V_3 = 7.55V$

\checkmark

$(83) \quad V_{D1} > \frac{V_{G1} - V_T}{7.5 - 5 - 1} = 2.55$

\checkmark

$(84) \quad \text{frame problem}$

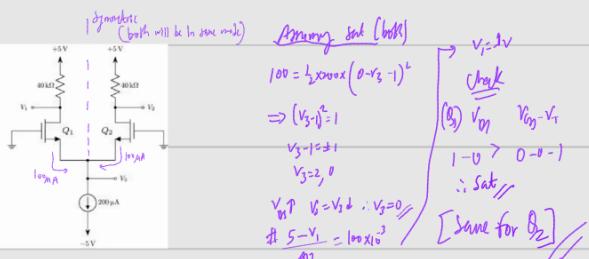
Ans

If (-)
 $V_3 = 6V, V_5 = 4V, V_4 = 9V$

Condition must be $V_3 > V_4 > V_5$
 but $V_3 < V_4$

Problem 24

For the transistors in the following circuits, $V_{BE} = 1\text{V}$, $k_n = k_p \frac{W}{L} = 200 \mu\text{A}/\text{V}_G$, and $\left(\frac{V}{I}\right)_n = \left(\frac{V}{I}\right)_p = 20$. Determine V_1 through V_3 .



(both will be in saturation)

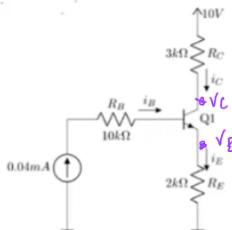
$$\begin{aligned} 100 &= \frac{1}{40} \times 100x(0 - v_3 - 1)^2 \\ \Rightarrow (v_3)^2 &= 1 \\ v_3 &\approx 0 \\ v_3 &\approx 2 \\ v_3 &\approx 0 \end{aligned}$$

$\therefore \text{Sat}$

[Same for Q2]

Bjt Problems

Analyze the following circuit to find the values of i_B , i_C , i_E and v_{CE} .



$$\begin{aligned} \beta &= 100 \\ \alpha &= 0.99 \\ v_{BE}(\text{Active}) &= 0.7\text{V} \\ v_{BE}(\text{Saturation}) &= 0.8\text{V} \\ v_{CE}(\text{Saturation}) &= 0.2\text{V} \end{aligned}$$

Assuming Active

$$\begin{aligned} v_{BE} &= 0.7, \quad I_c = \beta I_b, \quad I_e = \frac{\beta + 1}{2} I_b \\ I_b &= 0.04, \quad I_e = \alpha I_b, \quad v_{CE} \approx 0.8 \\ I_b &= \beta I_b = 100 \times 0.04 = 4 \quad \text{sat} \\ \frac{V_E - 0}{2} &= 4 \times 0.99 \\ \therefore I_E &= 4 + 0.99 = 4.99 \end{aligned}$$

$v_{CE} = V_C - V_E$

$$\begin{aligned} &= -2 - 0.08 \\ &= -2.08 \end{aligned}$$

$$= -10.08 \text{V}$$

$$v_{CE} > v_{CE} \text{ sat}$$

$$-10.08 > 0.2$$

∴ Assumption wrong

Assuming Sat

$$\begin{aligned} v_{BE} &= 0.8 \\ \frac{I_C}{I_B} &< \beta \\ v_{CE} &= 0.12 \end{aligned}$$

$$I_B = 0.04$$

$$\begin{aligned} &10 - 0 = i_c(3) + v_{CE} + i_E(2) \\ &10 = 3I_c + 0.2 + 2(I_c + 0.04) \end{aligned}$$

$$I_c = 1.98 \text{ mA}$$

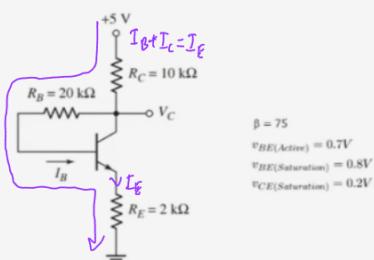
$$\therefore \frac{I_c}{I_B} = 48.6 < \beta \therefore \text{Active mode Assumption wrong}$$

$$\begin{aligned} &\frac{V_E - 0}{2} = I_E \quad \# \frac{5 - V_L}{10} = I_E \\ &V_E = 0.1702 \quad V_L = 1.179 \text{V} \end{aligned}$$

$$\therefore V_{CE} = 1.179 - 0.1702 = 0.998 > 0.2 \text{V}$$

$$\therefore \text{Active mode}$$

Determine the values of V_C and I_B .



$$\begin{aligned} \beta &= 75 \\ v_{BE}(\text{Active}) &= 0.7\text{V} \\ v_{BE}(\text{Saturation}) &= 0.8\text{V} \\ v_{CE}(\text{Saturation}) &= 0.2\text{V} \end{aligned}$$

Assuming Active

$$\begin{aligned} v_{BE} &= 0.7, \quad I_c = \frac{\beta}{2} I_b = (\beta + 1) I_b \\ \beta &= 75 \\ \# 5 - 0 &= 10(I_B + I_C) + 20I_B + 0.7 + 2I_E = 0 \\ 5 - 0.7 &= 10(I_B + \beta I_B) + 20I_B + 2(\beta + 1)I_E \\ \therefore I_B &= 4.61 \text{ mA} \end{aligned}$$

Assuming Active

$$\begin{aligned} v_{BE} &= 0.8 \\ V_E &= 0.17 \text{V} \end{aligned}$$

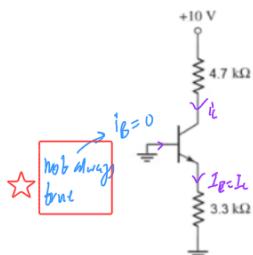
$$V_E = -0.17$$

$$I_E = -0.17 \text{ mA}$$

$$I_E < 0$$

$$\therefore \text{Not Active}$$

Determine the collector to emitter voltage.



$$\begin{aligned} \beta &= 75 \\ v_{BE}(\text{Active}) &= 0.7\text{V} \\ v_{BE}(\text{Saturation}) &= 0.8\text{V} \\ v_{CE}(\text{Saturation}) &= 0.2\text{V} \end{aligned}$$

Assuming Active mode

$$\begin{aligned} v_{BE} &= 0.7 \\ V_E &= 0 - 0.7 = -0.7 \text{V} \\ I_E &= \frac{-0.7 - 0}{3.3} = -0.21 \text{ mA} \\ \text{*** } I_E &\text{ cannot be negative as current flows from collector to emitter Active mode} \\ \therefore \text{Not active} \end{aligned}$$

Cut off Condition

$$v_{BE} \leq 0.7, \quad V_E \leq 0.5$$

$$I_C = 0, \quad I_B = 0, \quad I_E = 0$$

$$V_C = 10 \text{V}, \quad V_B = 0 \text{V}$$

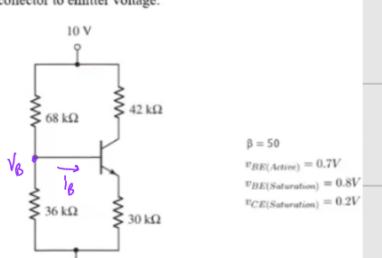
$$V_E = 0 \text{V}$$

$$\therefore V_{BE} < 0.7 \checkmark$$

$$V_{BC} = 0 - 10 = -10 < 0.5 \checkmark$$

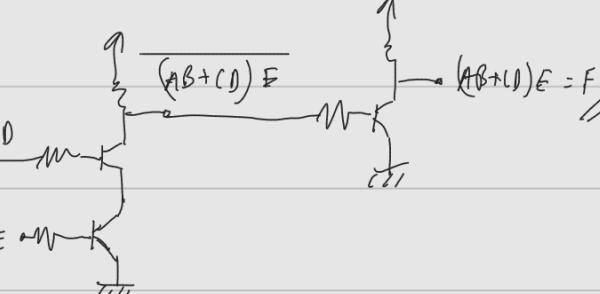
$$\therefore \text{Cut-off}$$

Determine the collector to emitter voltage.

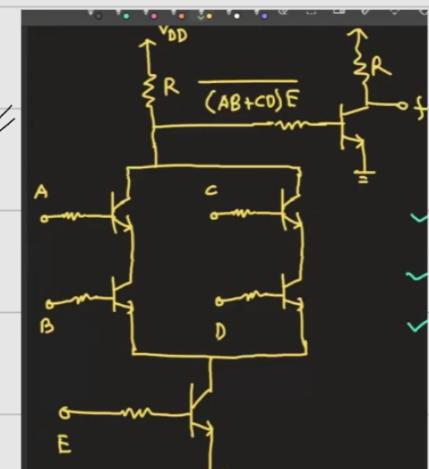


$$\begin{aligned} \beta &= 50 \\ v_{BE}(\text{Active}) &= 0.7\text{V} \\ v_{BE}(\text{Saturation}) &= 0.8\text{V} \\ v_{CE}(\text{Saturation}) &= 0.2\text{V} \end{aligned}$$

$$\begin{aligned} &10 = 68 \left(\frac{1}{68 + 36} \right) + 12 \left(\frac{1}{12 + 36} \right) - \frac{10}{68} - \frac{5}{36} = 0 \\ &V_B = \frac{5}{36} \text{V} \\ &\text{KVL} \end{aligned}$$

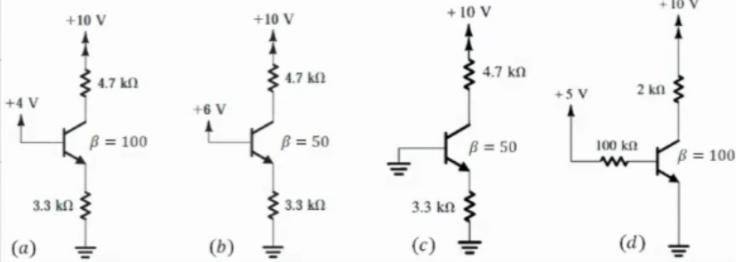


$$(AB + CD)E = F$$



Problem 3

- Determine and verify the operating region for each of the transistors in the following circuits. Assume $V_{BE,active} = 0.7 V$, $V_{BE,sat} = 0.8 V$, and $V_{CE,sat} = 0.2 V$.



(b) Assuming Active

$$V_{BE} = 0.7 V$$

$$\beta = 50$$

$$V_B = 6 V$$

$$i: V_{BE} = V_B - V_E$$

$$0.7 = 6 - V_E$$

$$i: V_E = 5.3 V$$

$$I_E = \frac{V_E - 0}{3.3} = \frac{5.3}{3.3} = 1.61 \text{ mA}$$

$$I_E = (\beta + 1) I_B$$

$$1.61 = 51 I_B$$

$$I_B = \frac{1.61}{51} = 0.032 \text{ mA}$$

$$I_C = \beta I_B = 1.6 \text{ mA}$$

$$\frac{10 - V_C}{4.7} = I_C$$

$$\frac{10 - V_C}{4.7} = 1.6$$

$$V_C = 2.48 \text{ V}$$

$$i: V_{CE} = 2.48 - 0.2 = 2.26 \text{ V}$$

$$\therefore \text{Not Active}$$

Assuming Sat

$$V_{BB} = 0.8 \text{ V}$$

$$V_{BE} = V_B - V_E$$

$$I_E = \frac{5.2 - 0}{3.3} = \frac{5.2}{3.3} = 1.58 \text{ mA}$$

$$I_E = I_B + I_C$$

$$1.58 = 0.6 + I_C$$

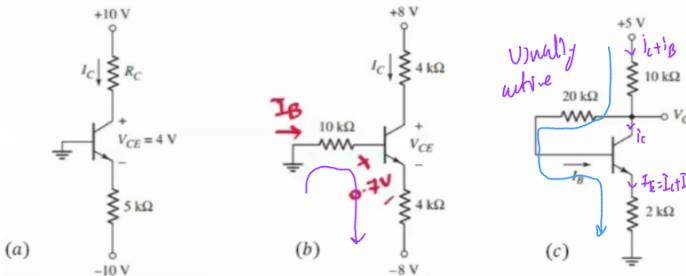
$$I_C = 0.98 \text{ mA}$$

$$\frac{0.98}{0.6} = 1.63 > \beta$$

$$\therefore \text{Sat mode}$$

Problem 4

- For the NPN transistors in the following circuit, $\beta = 75$, $V_{BE,active} = 0.7 V$, $V_{BE,sat} = 0.8 V$, and $V_{CE,sat} = 0.2 V$. Determine the labeled quantities.



(b) Assuming Active

$$V_{BE} = 0.7 V$$

$$\beta = 75, \beta = 75$$

$$0 - (-8) = I_B(10) + V_{BE} + 4I_E$$

$$8 = 10I_B + 0.7 + 4(75I_B)$$

$$8 = 385I_B + 0.7$$

$$I_B = 0.023 \text{ mA}$$

$$I_C = \beta I_B = 1.74 \text{ mA}$$

$$I_E = I_B + I_C = 1.763 \text{ mA}$$

$$\frac{V_E - (-8)}{4} = I_E$$

$$V_E = -6.998 \text{ V}$$

$$\frac{8 - r_e}{4} = I_E = 1.74$$

$$V_C = 1.04 \text{ V}$$

$$\therefore \text{Active}$$

(c) Assuming Active

$$5 - 0 = I_0(I_C + I_B) + 20I_B + 0.7 + 2I_E$$

$$5 = 10 \times (75I_B) + 20I_B + 0.7 + 2(75I_B)$$

$$5 = 1000I_B + 20I_B + 0.7 + 150I_B$$

$$5 = 1170I_B + 0.7$$

$$I_B = 0.00416 \text{ mA}$$

$$I_C = \beta I_B = 0.35 \text{ mA}$$

$$\frac{V_E - 0}{2} = I_E$$

$$V_E = 0.354 \text{ V}$$

$$\frac{5 - V_C}{10} = I_E$$

$$V_C = 1.459 \text{ V}$$

Check

$$V_{CE} = 0.3546 - 0.2 = 0.1546 \text{ V}$$

$$V_{CE} > 0.2 \text{ V}$$

$\therefore \text{Active}$

