

Transistors:

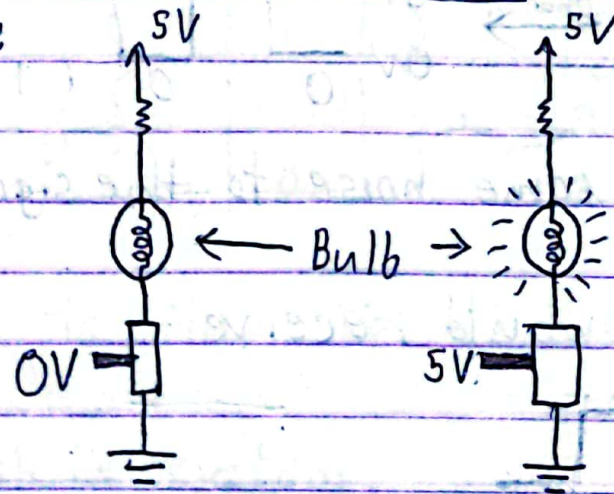
- * They are 3 terminal devices, (Input, Output and Control).
- * The I-V characteristics of this device can be changed by using the ^{control} terminal.
- * 2 types of Transistors:

① BJT - Bipolar Junction Transistor



② MOSFET - Metal Oxide Semi-conductor Field Effect Transistor

Application of Transistors:

① Switch:



② Logic gates: AND, OR, NOT, NAND, NOR

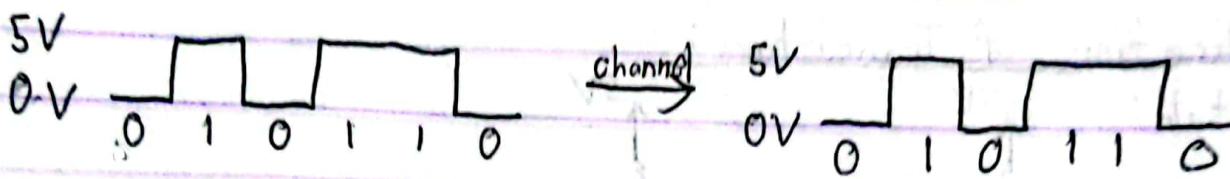
③ Amplifiers:  \rightarrow Amp \rightarrow 

* Binary \rightarrow 2 states
 x, y
 0 False
 1 True

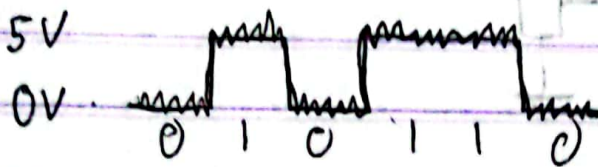
Voltage V	Current	Diode State	Resistance
1 \rightarrow 5V, 0V	1 \rightarrow 6mA	1 \rightarrow ON	1 \rightarrow low res
0 \rightarrow 0V, 3.3V	0 \rightarrow 3mA	0 \rightarrow OFF	0 \rightarrow high "

* Sender \rightarrow 010110

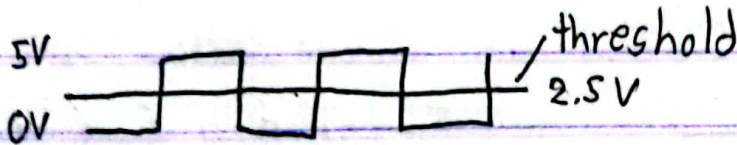
receiver



- The channel may add some noise to the signal being sent,
- Therefore the receiver would receive:



- Having just 2 levels of signal would cause problem as the received signal is nearly at 0V or 5V level.
- To solve this issue a threshold voltage is considered



- If at a point the voltage is above the threshold voltage it will be considered 5V and vice versa.

$$V_{received} (V_r) < 2.5 \Rightarrow 0, 0V$$

$$(V_r) > 2.5 \Rightarrow 1, 5V$$

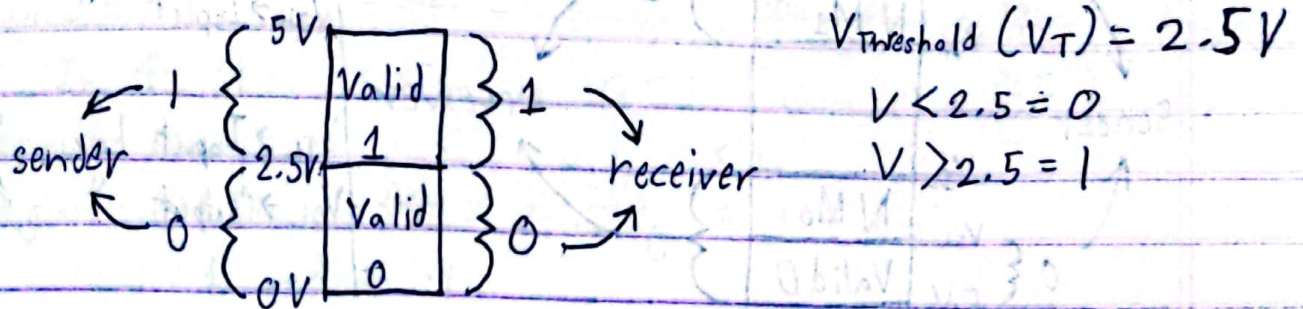
Static Discipline:

* Specification for digital devices

* Requires devices to adhere to common representation Valid \rightarrow Valid

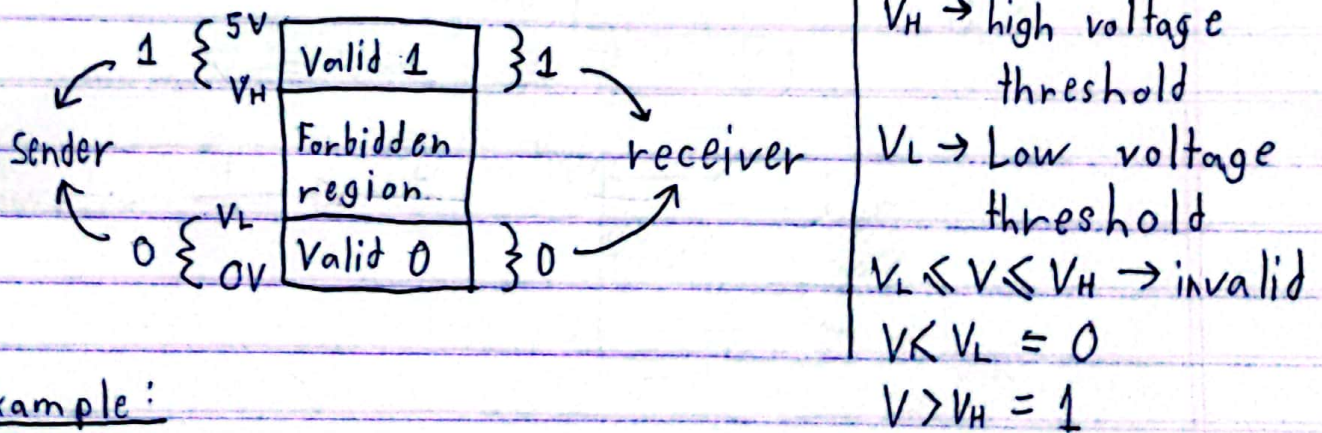
Send '0' $\xrightarrow{\text{noise}}$ receive '0'
" '1' $\xrightarrow{\text{noise}}$ " '1'

① naive approach \rightarrow single threshold



• Problem is when $V_r = 2.5V$

② 2 Threshold system:



• Example:

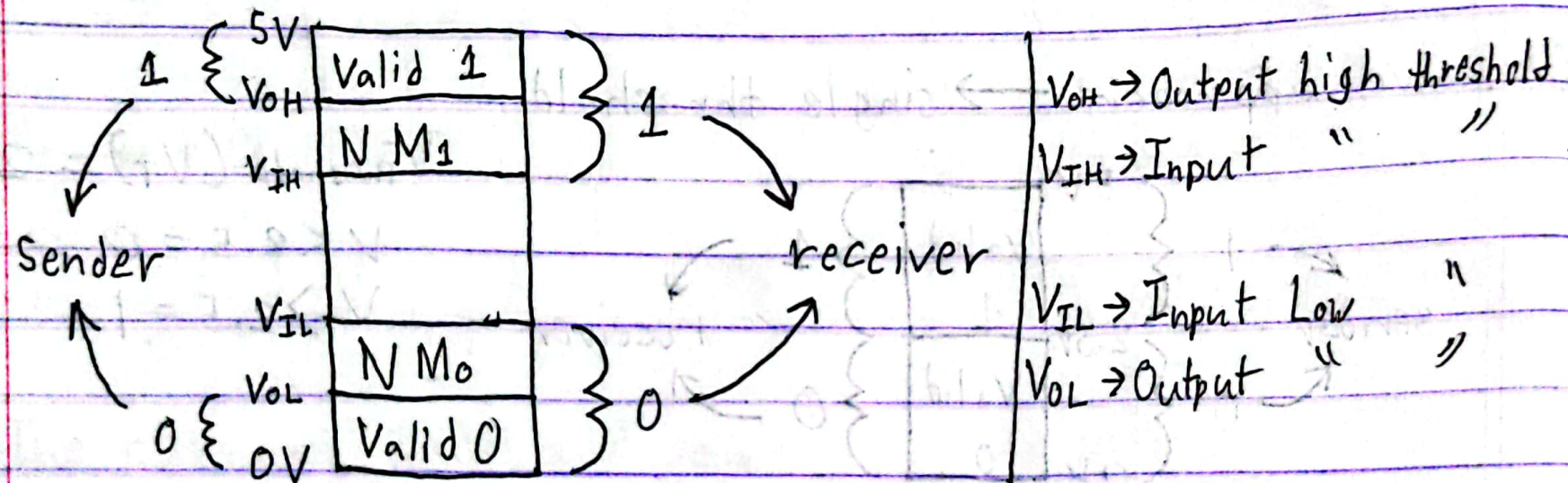
Logic 0: $0V \leq V \leq 2V$

" 1: $3V \leq V \leq 5V$

* Problem here is there is no margin for noise. So even if transmitted signal is valid received signal can become invalid,

③ Tighter restriction on sender (4 threshold levels):

Sender (Output(O))	Receiver (Input(I))
Logic 0: $[0V, 0.5V] \xrightarrow{V_{OL}}$	Logic 0: $[0V, 2V] \xrightarrow{V_{IL}}$
" 1: $[4.5V, 5V] \xrightarrow{V_{OH}}$	" 1: $[3V, 5V] \xrightarrow{V_{IH}}$

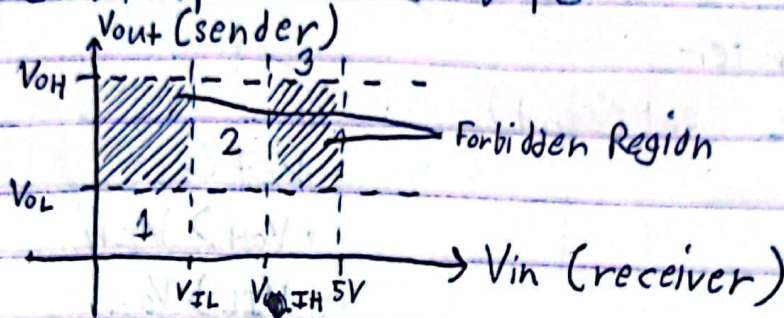


* $V_{OH} > V_{IH}$ and $V_{IL} > V_{OL}$

* Noise Margin for Logical 1 (NM₁) = $V_{OH} - V_{IH}$

* " " " " 0 (NM₀) = $V_{IL} - V_{OL}$

Static Discipline and VTC



Restrictions:

Logic 0: $V_{OL} < V_{IL}$

" 1: $V_{OH} > V_{IH}$

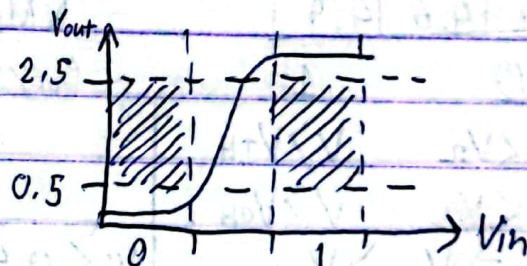
$$V_{OL} = V_{IL} - \Delta_1 \quad \text{--- (1)}$$

$$V_{OH} = V_{IH} + \Delta_2$$

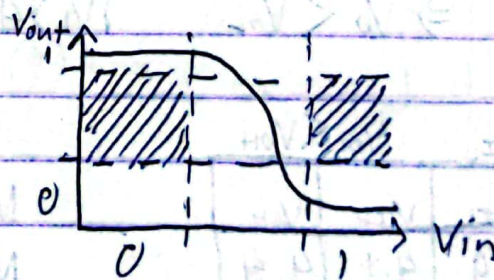
- Region - ①: Slope = $\frac{\Delta y}{\Delta x} = \frac{V_{OL} - 0}{V_{IL} - 0} = \frac{V_{IL} - \Delta_1}{V_{IL}} = \frac{V_{IL}}{V_{IL}} - \frac{\Delta_1}{V_{IL}} = 1 - \Delta_1'$
 \therefore In ①, Slope, $S < 1$ or $G < 1$ [Gain, $G = \frac{V_{out}}{V_{in}}$]
- Region - ②: Slope, $S < 1$ and $G < 1$.
- Region - ③: Slope = $\frac{\Delta y}{\Delta x} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} = 1 + \Delta_3'$
 \therefore Slope > 1 and $G > 1$

* Examples:

① Buffer



② inverter

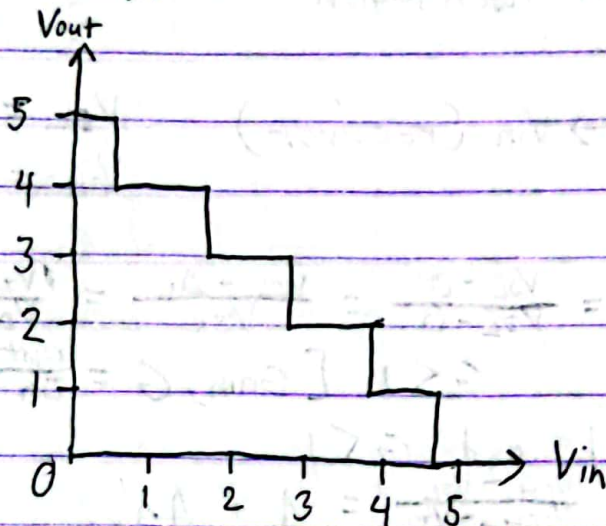


* Since the slope changes these devices are non-linear.

* Example:

● Not Gate / Inverter

I_n (Receive) 0/1 \rightarrow I_o 1/0 out (send)



VTC

• $V_{OH} > V_{IH}$

• $V_{IL} > V_{OL}$

• Valid input \Rightarrow Valid Output

①

$V_{OL} < V_{IL}$		$V_{IH} < V_{OH}$	
V_{OL}	V_{IL}	V_{IH}	V_{OH}
0.1	0.4	4.6	4.9
0		1	

$NM_0 = V_{IL} - V_{OL} = 0.3$

$NM_1 = V_{OH} - V_{IH} = 0.3$

Obeys static discipline = Yes

input $V < V_{IL}$ $V > V_{IH}$

output $V < V_{OL}$ $V > V_{OH}$

$V_i < V_{IL} \Rightarrow V_o > V_{OH}$

$V_i > V_{IH} \Rightarrow V_o < V_{OL}$

$V_i < 0.4 \Rightarrow V_o = 5V > V_{OH}$

$V_i > 4.6 \Rightarrow V_o = 0V < V_{OL}$

②

$V_{OL} < V_{IL}$		$V_{IH} < V_{OH}$	
V_{OL}	V_{IL}	V_{IH}	V_{OH}
0.6	0.9	4.1	4.4

$NM_0 = 0.3V$

$NM_1 = 0.3V$

Obeys static discipline = No

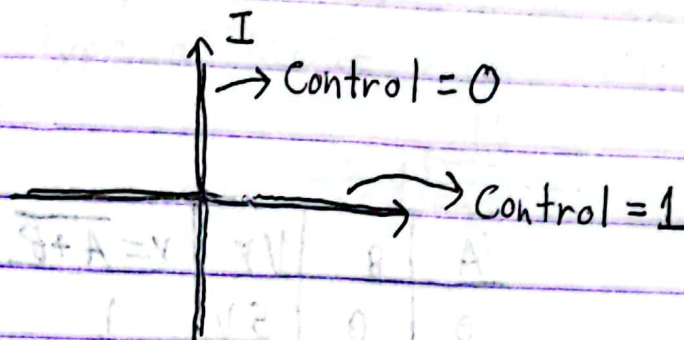
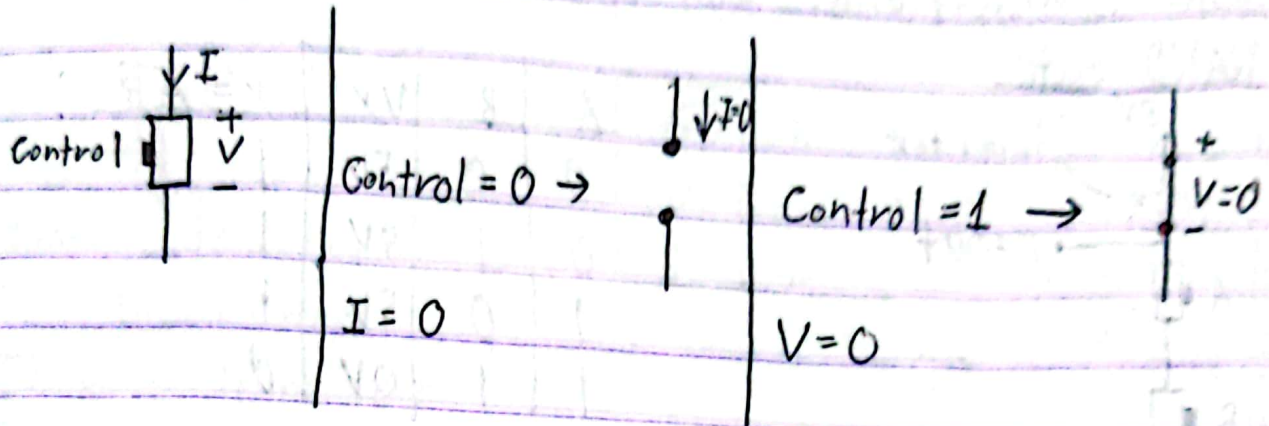
$V_i < V_{IL} \Rightarrow V_o > V_{OH}$

$V_i > V_{IH} \Rightarrow V_o < V_{OL}$

$V_o \geq 4V \nless 4.4V$ X

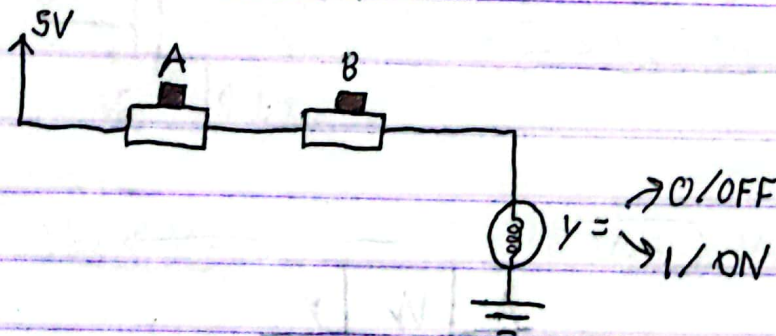
X

SWITCHES:



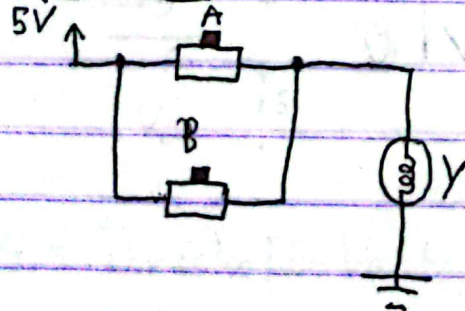
Steering Logic gates using switch:

① AND Gate:



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

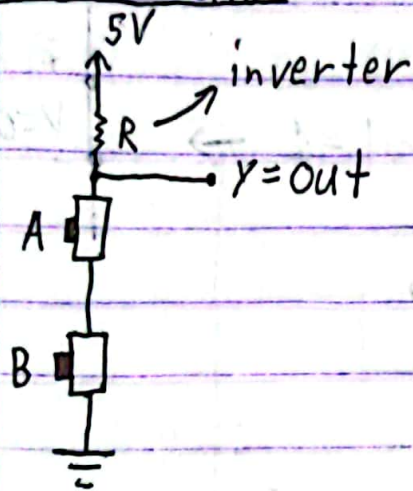
② OR Gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

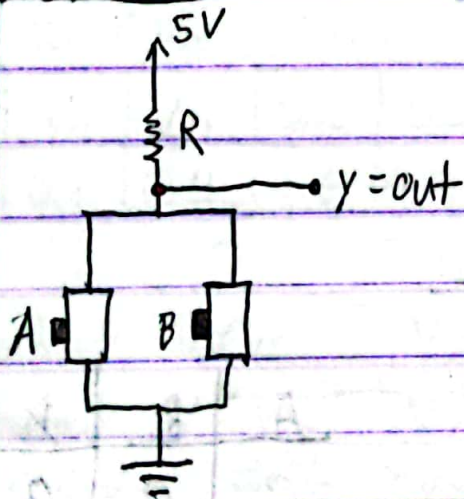
Semi Combinational Logic gates:

① NAND Gate:



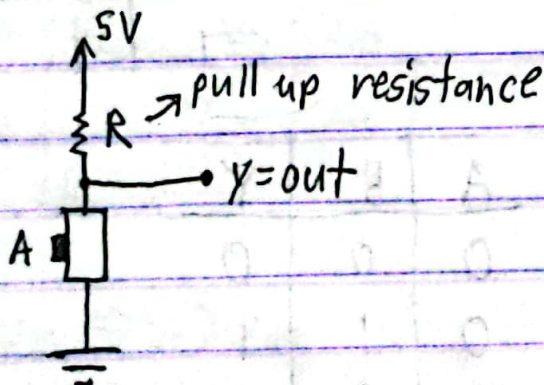
A	B	V _y	$y = \overline{AB}$
0	0	5V	1
0	1	5V	1
1	0	5V	1
1	1	0V	0

② NOR Gate:



A	B	V _y	$y = \overline{A+B}$
0	0	5V	1
0	1	0V	0
1	0	0V	0
1	1	0V	0

③ NOT Gate:



A	V _y	y
0	5V	1
1	0V	0