Video 04

(1) In a system there are 3 processes. P1 (10 bytes) P2 (6 bytes) P3 (8 bytes) with page size = 2 byte. main memory = 32 byte.

Page table:

Page table					
P1		P2		P3	
page	frame	page	frame	page	frame
0	7	0	15	0	2
1	12	1	13	1	6
2	1	2	9	2	3
3	5			3	8
4	4				

Find the physical address of logical address.

P1 page = 10/2 = 5 page

P2 page = 6/2 = 3 page

P3 page = 8/2 = 4 page

offset -) 2 => 2^1 => n = 1 bit.

P1

Page 5 =) 2^3 =) Page.no = 3 bit

padding	Page no	offset
1	3	1

memory address 32 bit.
to represent 32 bit = 2⑤ → bit.

a) 01001.
Page no ↵ ↳ offset
4 1.

Frame	offset
4	1

Physical address = (Frame no x Page size) + offsed.
= (4 x 2) + 1
= 8 + 1
= 9 → means 01001 main memory 9th byte 9 Store

=) 01001 9 Store

b) 00100 of P1.

0010 | 0

Page number ↵ 2 | 0 ↳ offset

=) frame : 1
offset : 0

Physical address = (Frame no x Page size) + offset

= (1 x 2) + 0

= 2 + 0

= 2

তার মানে 00100 main memory তে 2nd byte এ থাকবে।

c) 00111 of P1.

~~000~~ 0011 | 1

3 ↵ ↳ offsed.

=) frame : 5
offsed : 1.

Physical address = (5 x 2) + 1 = 11

d) 00001 of P2.

0000 | 1

Page number ↵ | ↳ offset.

0 | 1

Frame | Offset

15 | 1.

Physical address = (15×2) + 1

= 30 + 1

= 31

e) 00100 of P2.

0010 | 0

Page number ↵ | ↳ offset.

2 | 0

Frame | Offset.

9 | 0

Physical address = (9×2) + 0

= 18

f) 10101 of P2.

1010 | 1

Page no ↵ ↳ offset

10 | 1

invalid page no

g) 00010 of P3.

0001 | 0

Page ↵ ↳ offset.

no

1

Frame offset

1 | 0

Physical address = (1×2) + 0

= 2

h) 11011 of P3.

1101 | 1

Page number ↵ ↳ offset.

13

invalid page number.

i) 00110 of P3.

0011 | 0

Page number ↵ ↳ offset

3 0

frame offset

8 0.

Physical address = (8 × 2) + 0

= 16

(Ans).

2) During TLB,

associative lookup time = 3 ns , TLB.

hit ratio, α = 70%

miss ratio, = 30%

memory access = 80 ns , TRAM

EAT = ?

$$EAT = \alpha(TLB + TRAM) + (1-\alpha)(TLB + 2\,TRAM)$$

$$= .7(3+80) + .3(3+160)$$

$$= .7(83) + .3(163)$$

$$= 107 \text{ ns}.$$

(Ans).

(3) During TLB,

T TLB = 5ns

hit ratio = 65.5 %

TRAM = 200ns

miss ratio = 34.5

EAT = ?

$$EAT = \alpha (TLB + TRAM) + (1-\alpha)(TLB + 2\,TRAM)$$

$$= .655 (5+200) + .345 (5 + 2 \cdot 200)$$

$$= .655 (205) + .345 (405)$$

$$= 274 \text{ ns}$$

(Ans).

4) Logical address = 118 bits.

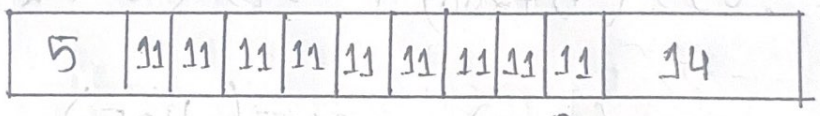
page size = 16 kB.

entry size = 8 byte.

page size = 16 × 1024

= 16384

= 2^{14}



= 118 bits.

Number of rows = $\frac{\text{page size}}{\text{entry size}}$

= $\frac{16\ kB}{8\ B}$

= 2^{11}

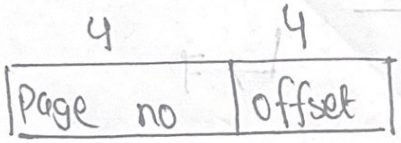
5) Single paging

logical address space = 8 bits

Page size = 16 bytes

main memory = 512 bytes.

Page size = 16 Bytes = 2^{4}



Total : 8

Frames in RAM = $\frac{512}{16}$ = 32 frames in RAM

3, 90, 167, 241

physical address

	frame	offset
3 = 0000 0011	= 5	3

0 ↵ Page no

↳ 3 offset

physical address = (5 × 16) + 3

= 80 + 3 = 83

(Frame no × Page size) + offset.

90 = 0101 1010 frame offset

Page no ↵ ↳ offset.

5 no page which is invalid.

167 = 1010 0111 frame offset

10 ↵ ↳ 7 7 7.

physical address = (7 x 16) + 7

= 112 + 7

= 119

241 = 1111 0001 frame offset

Page no ↵ ↳ offset 14 1.

15 1

physical address = (14 x 16) + 1

= 224 + 1

= 225

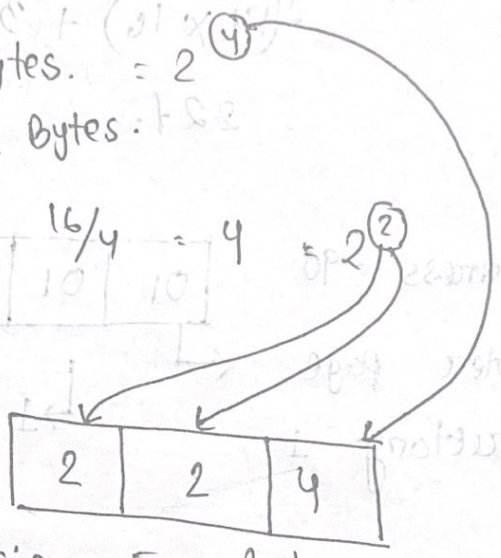
6) multi level paging

Logical address space = 8 bits.

Page size = 16 Bytes. = 2^4

per entry size = 4 Bytes.

~~Frames in RAM~~ No of Rows = $16/4 = 4 = 2^2$

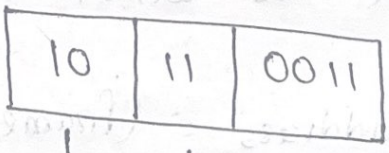


main memory size = 512 Bytes.

Frames in RAM = $\frac{512}{16}$ = 32 frames in RAM.

logical address = 179

=



Page directory ← 3 → 3

outer page table.

2.

page 2 offset 3

Outer table. →

Page 2 points to frame 11 and that is valid.

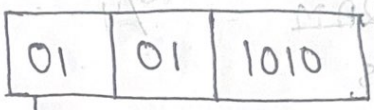
Now, inner frame 11's offset 3 has 14 which is valid.

Physical address = (frame nox page size) + offset.

$= (14 \times 16) + 3$

$= 227.$

logical address = 90



Outer page directory ← 01 (1) → offset.

outer page

1 has pointer to frame 6 and is valid.

inner table frame 6's ~~offset~~ 1 page refers to frame 20 which is also valid.

physical address = (frame nox page size) + offset.

$= (20 \times 16) + 10$

$= 320 + 10$

$= 330.$

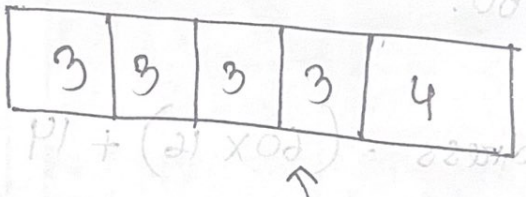
(Ans)

7) Logical address space = 16 bits

page size = 16 bytes = 2^4

each entry = 2 bytes

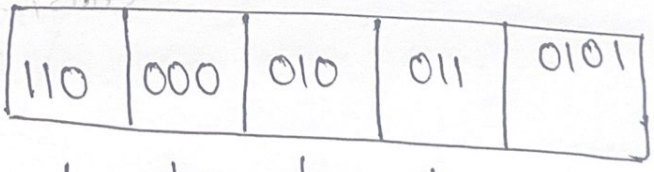
main memory = 1 kB = 1 x 1024 = 2^{10} bytes



no of rows = 16/2

= 8 = 2^3

49461 →



6 (3rd outer) → 0 (2nd outer) → 2 (1st outer) → 3 (inner) → offset 5

Frame no = 56

Physical address = (56 x 16) + 5

= 901.

13742 → 001 101 011 010 1110 → 14 offset.

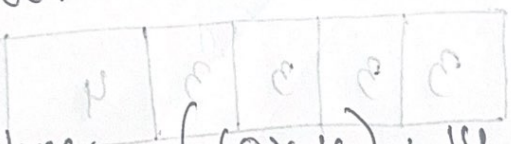
3rd outer table ← 1

2nd outer → 5

3rd outer → 3

inner → 2

Frame = 60.

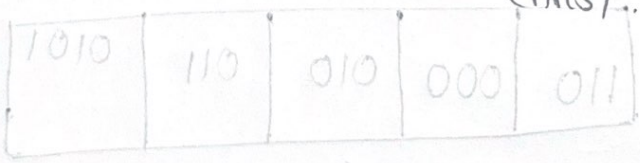


Physical address = (60 x 16) + 14

= 960 + 14

= 974.

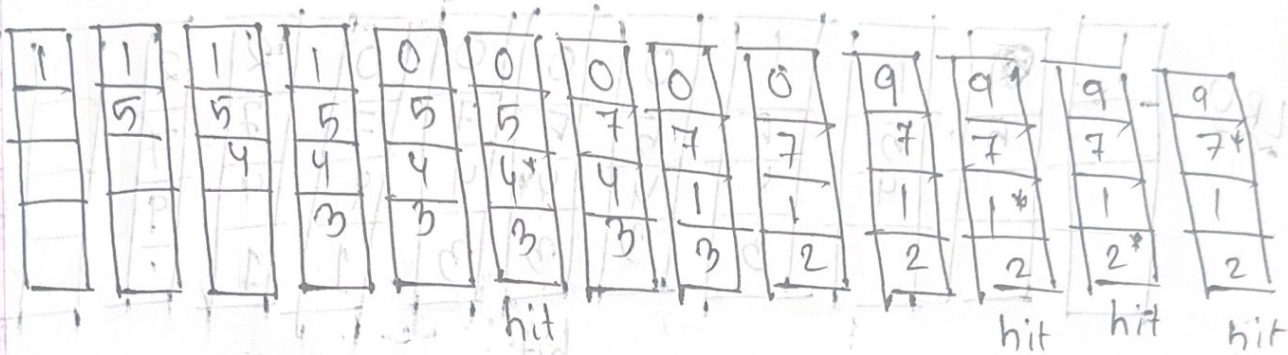
(Ans).

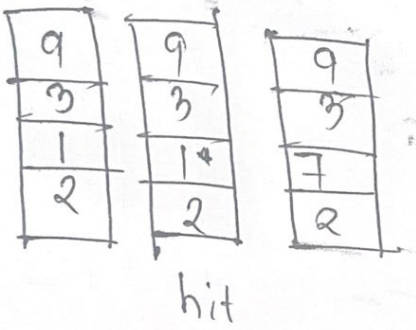


Practice 8

1 5 4 3 0 5 4 3 0 7 4 3 0 7 1 3 0 7 1 2 9 7 1 2 9 7 1 2 9 7 1 2

FIFO

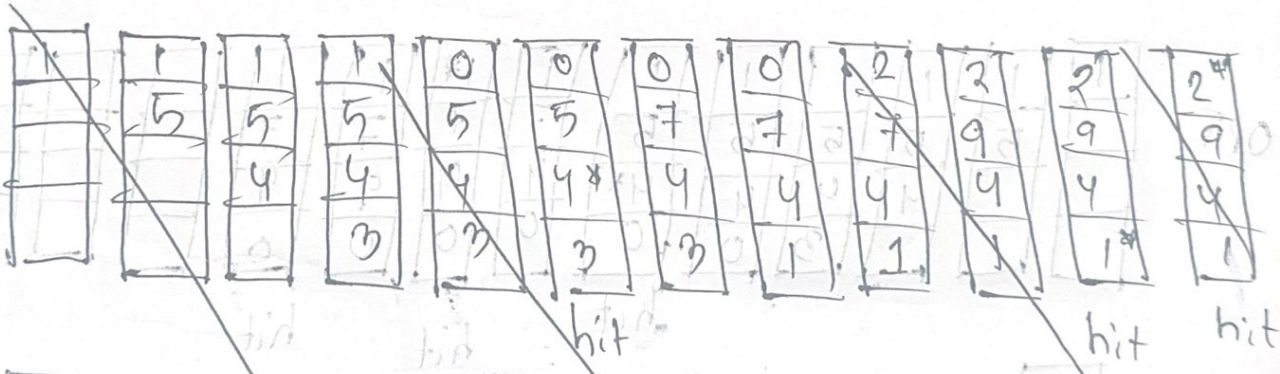


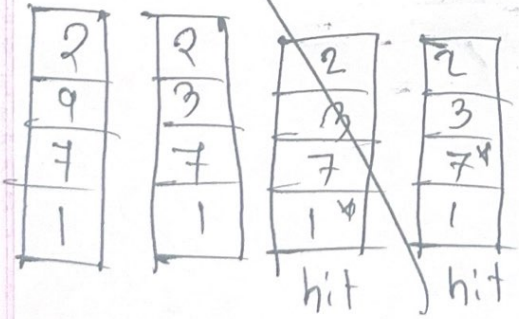


hit = 5/16 = 31.25 %.

miss = 11/16 = 68.75 %.

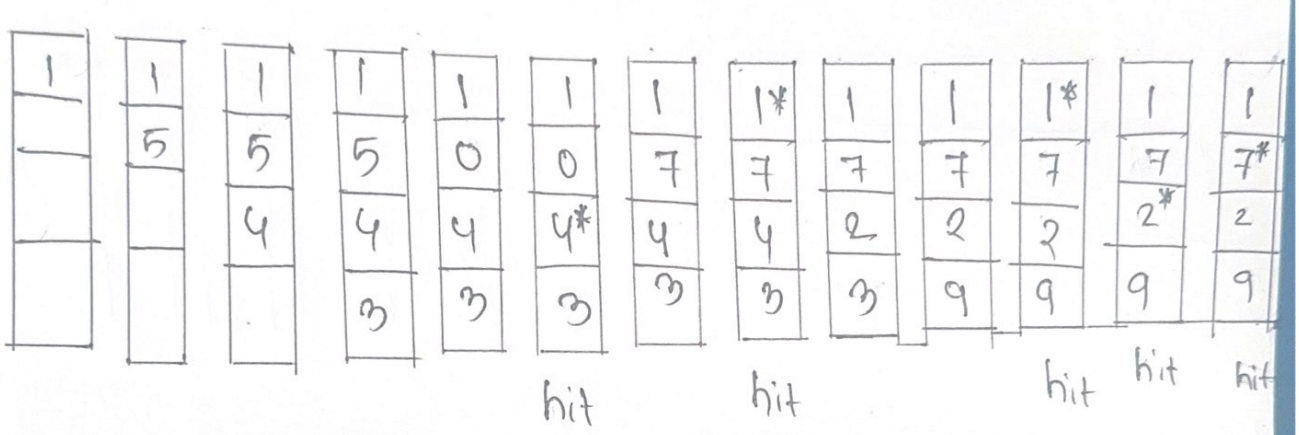
LRU

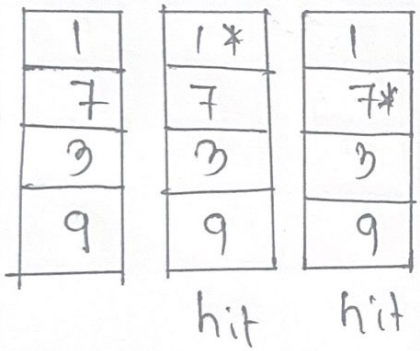




Optimal

1 5 4 3 0 4 7 1 2 9 1 2 7 3 1 7





hit ratio = $\frac{7}{16}$ = 43.7%.

miss ratio = 9/16 = 56.2%.