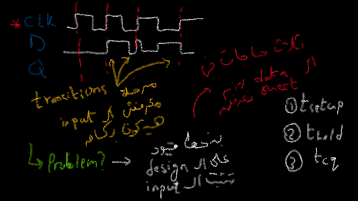
Lecture 9

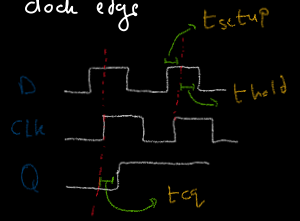


⇒ time parameters:

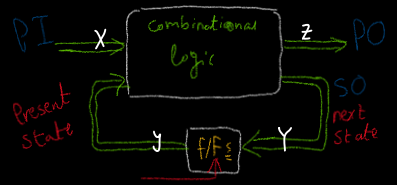
1] t setup: minimum time during which the input is kept stable **before** arrival of clock edge

2] t hold: minimum time during which the input is kept stable **after** arrival of clock edge

3] t_{cq}: delay time after which the output Q changes after the arrival of the clock edge



⇒ Designing of sequential circuits :



⇒ Steps of designing :

① draw a **state** diagram

② convert state diagram into state **table**

Present state (y)	next state (Y)		output (z)	
	In=0	In=1	0=0	0=1

③ State optimization

① exclude present state column
② if two rows are identical, then their present states are equivalent & we can remove one of them
③ Repeat the optimization after removing → then it called [reduced table]

↳ 3-a State encoding

Assign binary code to every state & replace them in the table

⇒ f/f stores the state of the machine with it's binary code

no. of bits = no. of used f/f

$y_1, y_2, y_3 \dots y_n$

Unused bits → don't cares

Next Step

④ State equations

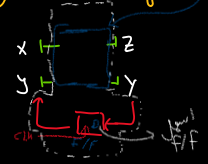
↳ Construct a k-map of two inputs

↳ Search for when Y = 1

⑤ output equations

↳ Same as before but for Z

⑥ Circuit diagram



معلومات عامة :

ال Sequential circuit لها عدة اسماء

→ finite state machine (FSM) ← منها

→ Finite Automata

اي حاجة في الدنيا ممكن تتوصف بال ↖

وتقدر تعملي