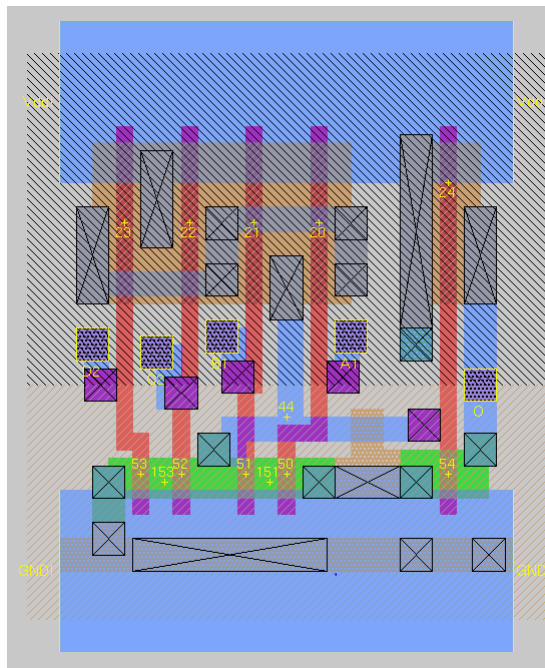# Integrated Circuit Design
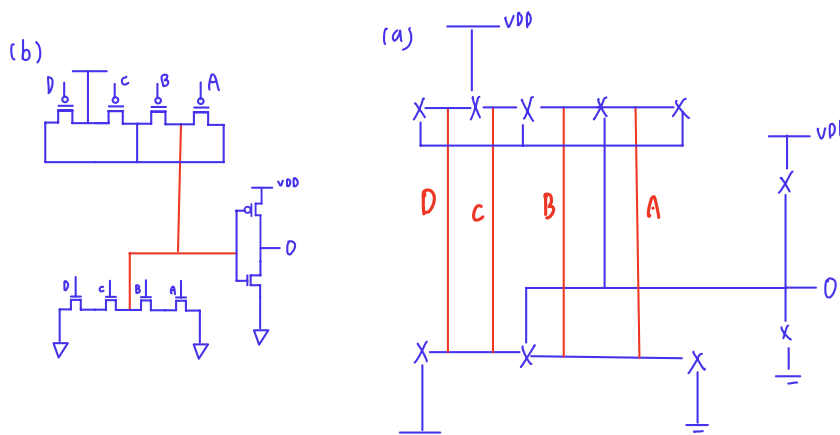## Homework #1
Layout Reading

Deadline: Sep. 27

For the following layouts, please

(a) Draw the associated sticky diagram.

(b) Draw the circuit in transistor level.

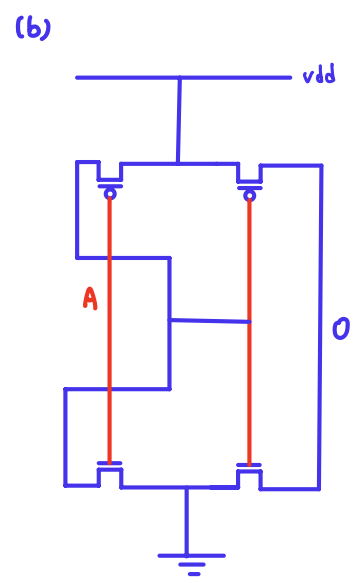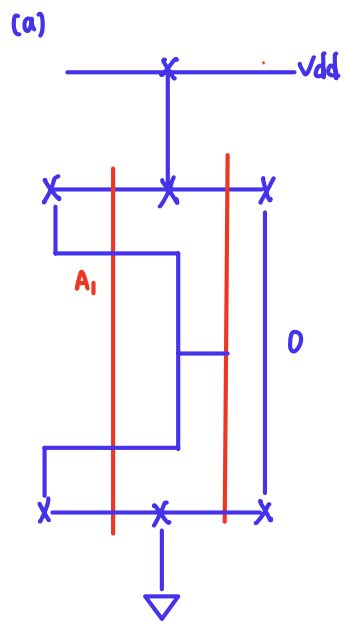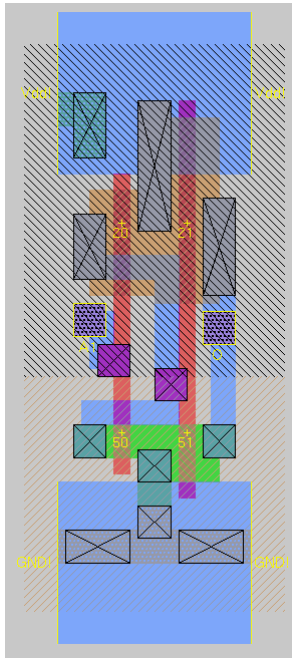(c) Describe the function of the circuits. (You can use Boolean equations or other descriptions)
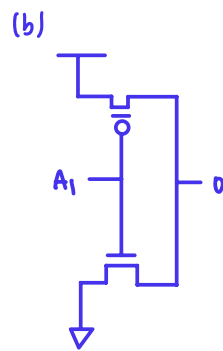
1.

(c)

$$O = DC + AB$$

(b)

(a)

2.

(a)

A_1

O

Vdd

(b)

A

O

Vdd

(c) $\stackrel{A}{\rightarrow}$ buffer   ∴

A	O
0	0
1	1

3.

(a)

A_1 O

(b)

A_1 O

(c)

$O = \overline{A_1}$

4.

(a)

W

A

O

(c)

O = $\overline{A}$

(b)

A

O

5.

(a)

sel2 Q $\overline{Q}$ PG1

(b)

sel$_2$ Q $\overline{Q}$ PG1

(c) SR latch

6.

(a)

(b)

sel$_3$ A$_1$ B$_2$ O

(c) mux

(a)

(c) $O_1 = (ABCD)'$

$O_2 = ABCD$

7.
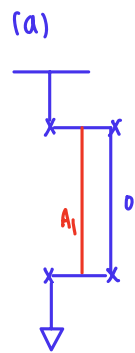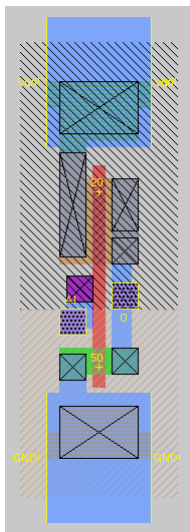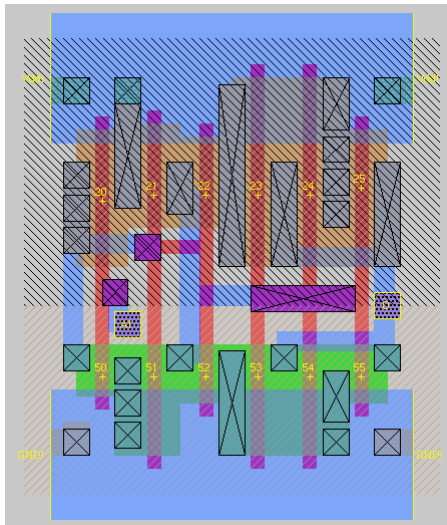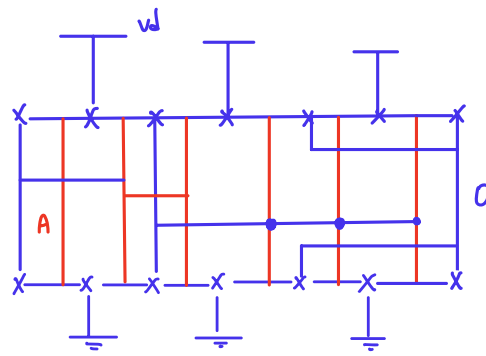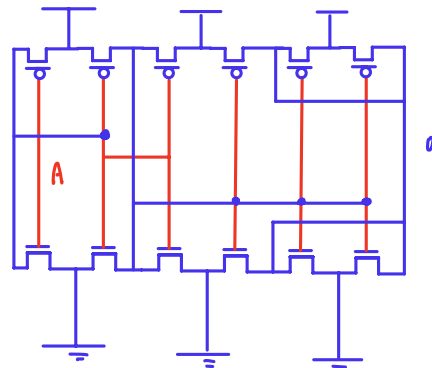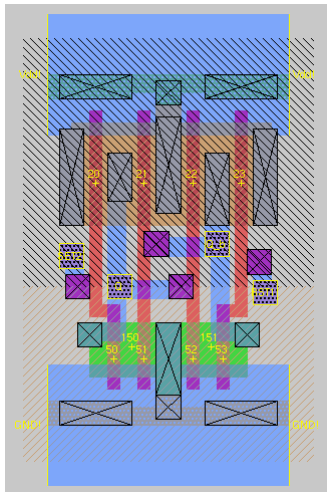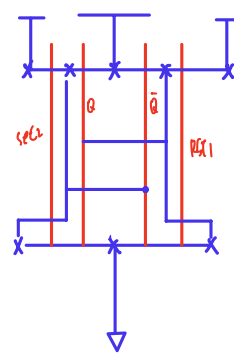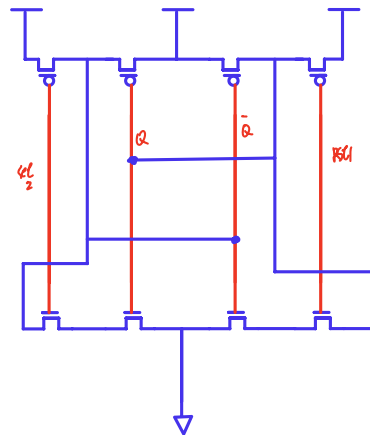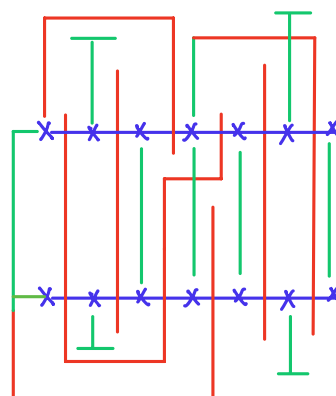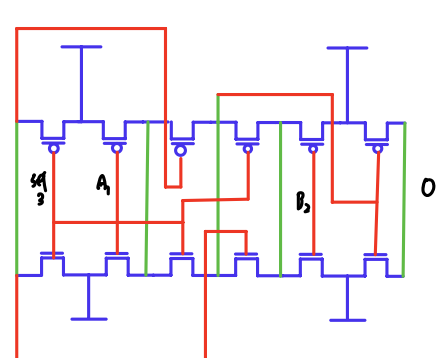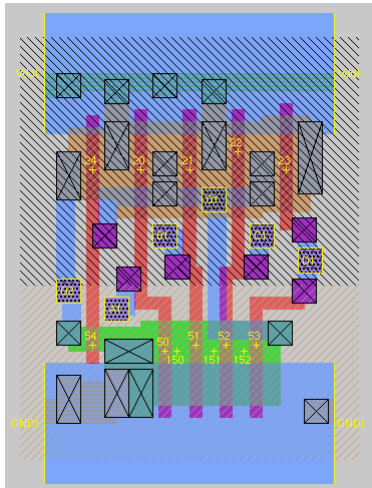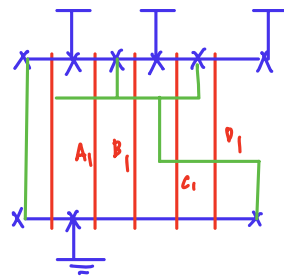
(b)
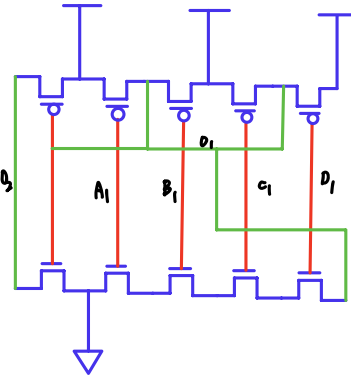
8.
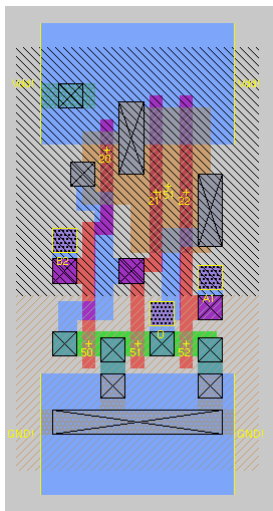
(a)

(b)
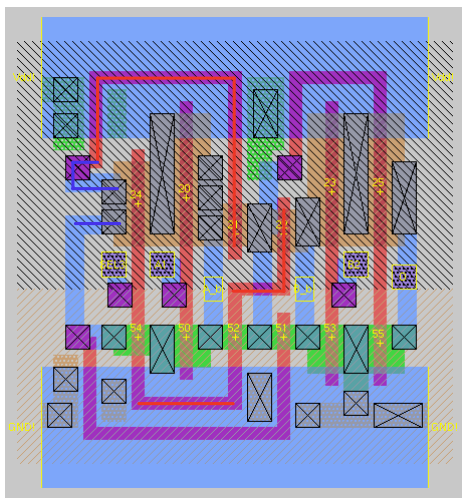

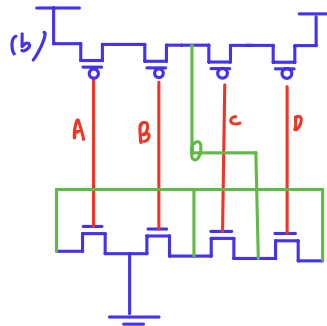
(c)
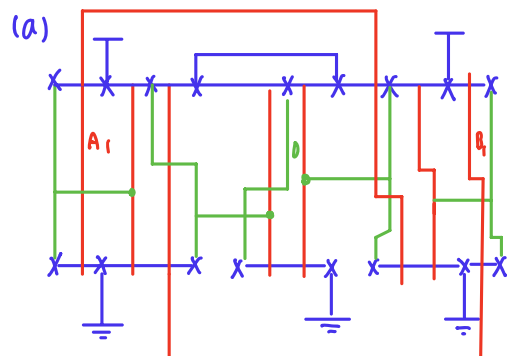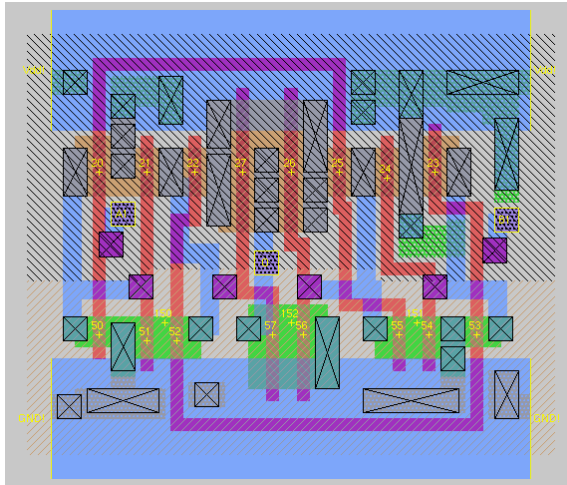
$O = A'B$

9.

(a)

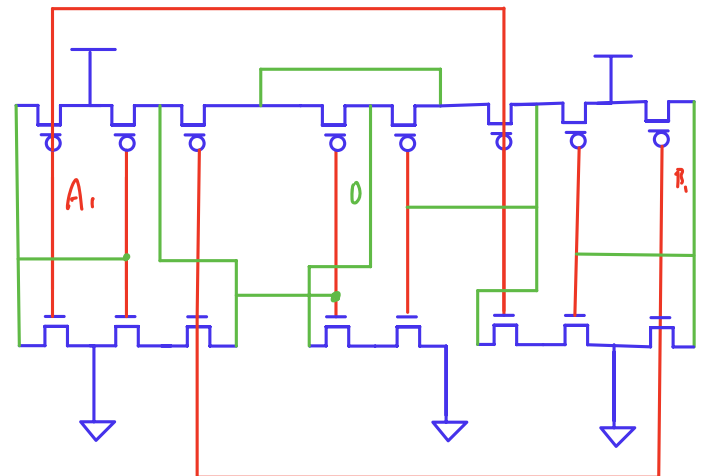**(c)**

$$O = \overline{((A_1 + B_1) \cdot (C_2 + D_2))}$$

(b)

10.

(a)

(b)

(c) $D = A_1' B_1 + A_1 B_1'$