Electronics 315

Practical 3 Report

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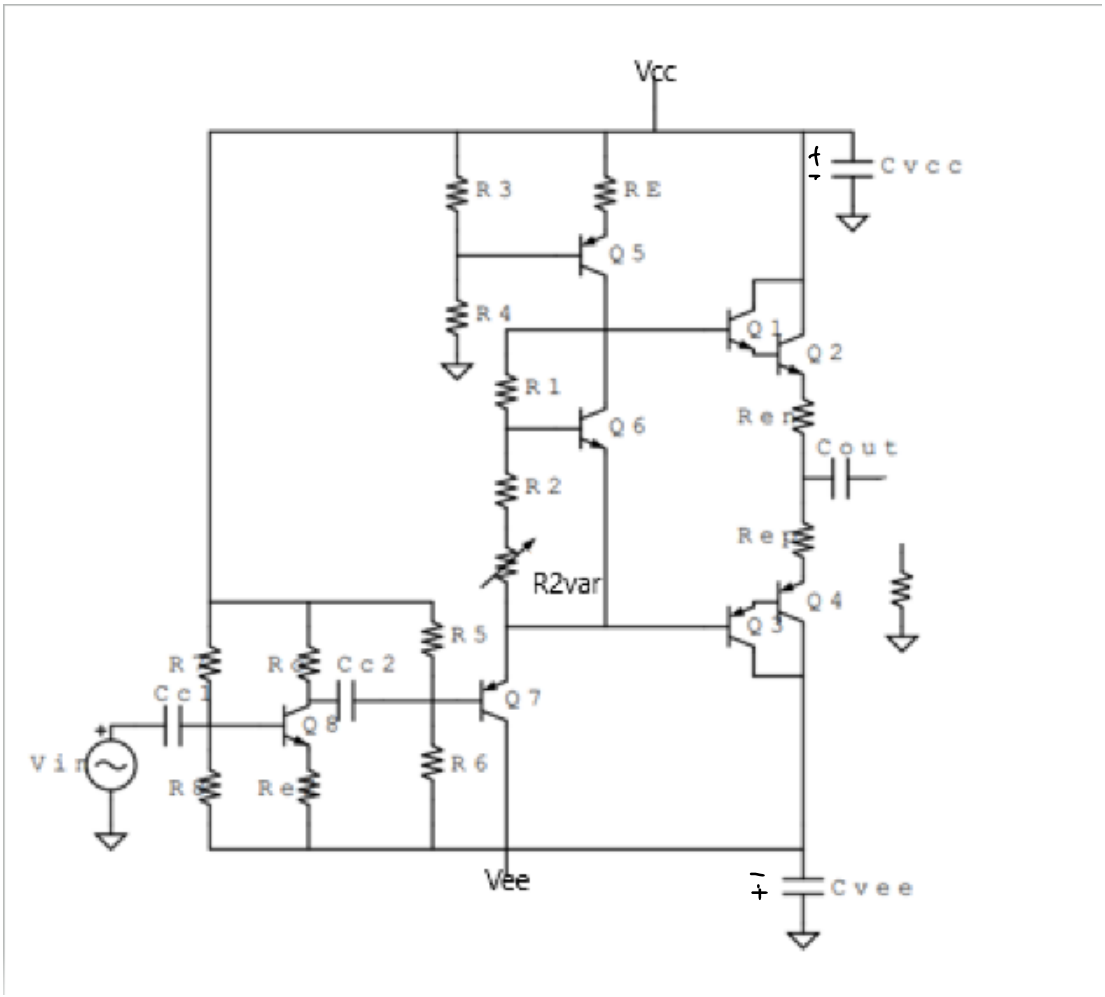
Circuit Diagram:



Transistor	Choice
Q1	2N2219A
Q2	TIP41C
Q3	2N2905A
Q4	TIP42C
Q5	2N2905A
Q6	2N2219A
Q7	2N2905A
Q8	2N2219A

Resistor	Designed	Actual
R1	4k	3947
R2	1.2k	900
R2var	0-1000	300

R3	1.2k	1202
R4	25k	24.93k
R5	1M	1M
R6	640k	640k
R7	370k	390k
R8	12k	11.88k
RE8	1,1k	1077.8k
RC8	42k	41.767k
Ren	0.5	0.5
Rep	0.5	0.5
RE	120	118
Capacitors		
Cout	4700u	4700u
Cc1	10u	10u
Cc2	10u	10u
Cvcc	100u	100u
Cvee	100u	100u

Table 1: Resistors, capacitors and transistor choices

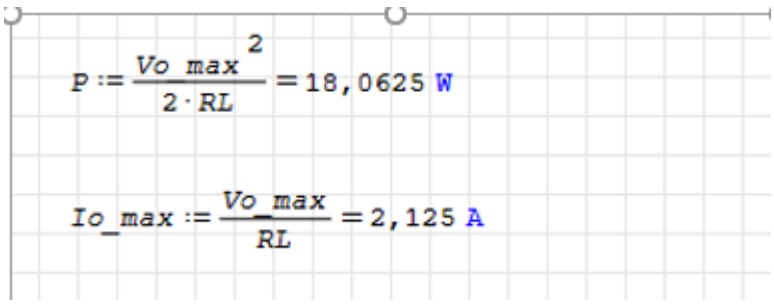
Power Amplifier Design:

We first calculate the maximum voltage we can get using the 20V power supply.

We choose VRE and VREN to be 0.2V.

$$Vo\_max := Vcc - Vce5\_sat - Vbe1\_on - Vbe2\_on - VRE - VREN = 17,9$$

For error margin we design for 17V ∎



Here we see the maximum power we can achieve is 18W which meets specification requirements and the maximum current is 2.125A which also meets specification requirements.

Due to Darlington pair configuration we can calculate IB1(max) using Io(max).

We also choose ic6(min) to be small enough for it to be on.

ic6(min)=0.6mA

$$iB1\_max := \frac{Io\_max}{(B1+1)\cdot B2} = 0,0004\ A$$

$$iC6\_max := ic6\_min + iB1\_max = 0,001\ A$$

$$iB6\_max := \frac{iC6\_max}{B6} = 1,0208\cdot 10^{-5}\ A$$

Choose IR1>>iB6(max)

We thus chose IR1=500µA

$$Ic5 := IR1 + ic6\_min + iB1\_max = 0,0015\ A$$

$$RE := \frac{VRE}{Ic5} = 131,5104\ \Omega$$

Choose to design for RE = 120Ω because of standard resistor values in lab.

$$RB := 0,1\cdot B5\cdot RE = 1200\ \Omega$$

$$IB5 := \frac{Ic5}{B5} = 1,5208\cdot 10^{-5}\ A$$

$$Vth := Vcc - VRE - Veb5\_on - IB5\cdot RB = 19,0818\ V$$

$$R3 := Vcc\cdot\frac{RB}{Vth} = 1257,7462\ \Omega$$

Choose R3= 1.2kΩ

$$R4 := \frac{R3\cdot Vth}{Vcc - Vth} = 24936,6871\ \Omega$$

Choose R4 =25kΩ

<u>VBE-Multiplier</u>:

$$Vbb := Vbe1\_on + Vbe2\_on + Veb3\_on + Veb4\_on = 2,6\ V$$

$$IR1 = \frac{Vbb}{R1+R2}$$

$$R2 := 5200\ \Omega - R1$$

$$Vbb = \left(1+\frac{R1}{R2}\right)\cdot Veb4\_on$$

$$R1 := 4\ k\Omega$$

$$R2 = 1200\ \Omega$$

We test the R2 value in spice and lower it until it reached a high enough temperature operating temperature of atleast 130 °C. This got us to a new R2 value of 900Ω.

```
Safe Op. Area (@1kHz): PASS | NULL | BJTs within SOA | BJTs inside SOA
T(power npn).........: PASS | NULL | Below 150 C.... | 132.318 C
T(power pnp).........: PASS | NULL | Below 150 C.... | 134.076 C
```

Then We choose R2 in series with a variable resistor R2var of 0-1000 Ω which can later be adjusted in case of crossover distortion.

$$IB7\_max := \frac{Ic5}{B7+1} = 1,5057 \cdot 10^{-5}\ A$$

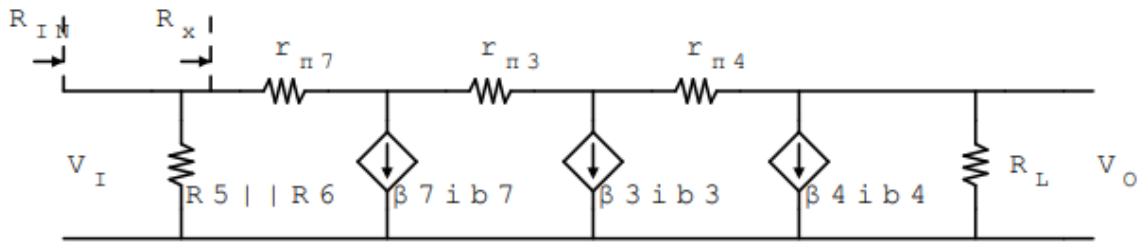
$$IR6 := 2 \cdot IB7\_max = 3,0115 \cdot 10^{-5}\ A$$

$$VB7\_max := -(Veb4\_on + Veb3\_on + Veb7\_on) = -2\ V$$

$$R6 := \frac{Vcc + VB7\_max}{IR6} = 5,9771 \cdot 10^{5}\ \Omega$$

$$R5 = 1 \cdot 10^{6}\ A$$

We want the voltage at the base of Q7 to be -2V allowing the output to optimally and symmetrically swing. Using a R6 value of 600kΩ and spice analysis we found the value at the base of Q7 to be around -2.4V after adjusting R6 to 640kΩ we get a value closer to -2V and thus chose to design based off of that.



The resistance seen by the amplifier Rx was calculated as 9MΩ using small signal analysis this lead to a design choice of R5 = 1MΩ because it was the highest resistor obtainable from the lab choices.

Preamplifier Design:

The preamp sees a load resistance of 360kΩ . We choose a 2N2219 transistor because of its high voltage gain. The input signals max current is limited to 1mA therefore we need a large input resistance and a common emitter configuration would be the best design choice seeing as it fits the specifications of large input resistance.

We need to choose a collector current for our transistor to design for. The current IC8 needs to supply enough current to load the input resistance of the power amplifier. Seeing as the resistance seen by the pre amp is very high the required current is very small and 0.5mA should be enough. Thus IC8=0.5mA

$$Av := -\frac{Vo}{Vin} = -34$$

$$IB8 := \frac{IC8}{B8 + 1} = 4,9505 \cdot 10^{-6}\ A$$

$$RE8 := \frac{Vcc - Vee - Vce5\_sat}{IC8 \cdot (1 - 2 \cdot Av)} = 1147,8261\ \Omega$$

$$Vbb8 := Vee + IC8 \cdot RE8 + Vbe8\_on = -18,7261\ V$$

$$RC8 := RE8 \cdot (-Av) = 39026,087\ \Omega$$

$$Rth := 0,1 \cdot (B8 + 1) \cdot RE8 = 11593,0435\ \Omega$$

$$Rth = \frac{R7 \cdot R8}{R7 + R8}$$

$$Vth = \frac{R8}{R7 + R8} \cdot (Vcc - Vee) - Vee$$

$$R7 := 370\ k\Omega$$

$$R8 := 12\ k\Omega$$

Adjusting RC8 to 42kΩ provides us with the best gain for our circuit and thus it was chosen to change the RC8 value to 42kΩ.

Frequency Analysis and Capacitor Design:

The following results for the total harmonic distortion at full power for different frequencies were obtained from the spice analysis. This is within specifications and is thus satisfactory.

```
THD @ 1kHz (full pwr): PASS |  ..1.  | Below 4 %..... | 1.67889 %
THD @ 40Hz (full pwr): PASS |  ..1.  | Below 4 %..... | 1.46564 %
THD @ 20kHz (fll pwr): PASS |  ..1.  | Below 4 %..... | 2.63698 %
```

Capacitor design:

Low frequency cutoff:

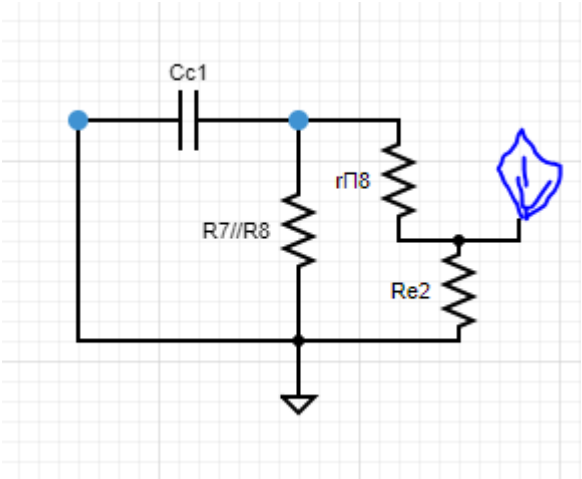
C_{c1}:

Our circuit should cut off frequencies lower or equal to 20Hz as set by the specifications.

We have been provided with 10 uF, 100 uF and 4700 uF capacitors.

We thus perform frequency analysis to see which of these capacitor would work best.

We first look at Cc1.



The capacitor sees the following equivalent circuit. The resistance Req can then be calculated as [R7||R8||(rπ8 + [β8 + 1]RE2].

Req = 10.57 kΩ

For f_L = 20 Hz we need a time constant τ_{CC1} = 7.95ms

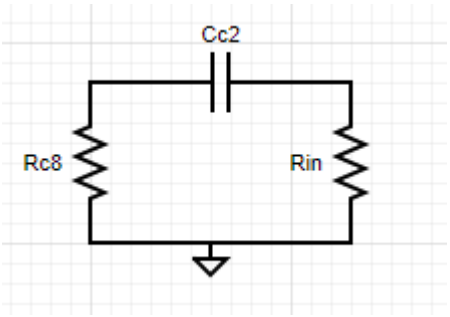
Thus using τ_{Cc1} = Cc1[R7||R8||(rπ8 + [β8 + 1]RE2]

We get Cc1 = 0.72 uF

This is far lower than our lowest provided capacitor of 10uF. However if we use Cc1 = 10uF we get a time constant of 105.7ms which gives us a cutoff frequency of 1.5Hz, which is still far within specifications and can thus be used.

C_{c2}:

Equivalent circuit



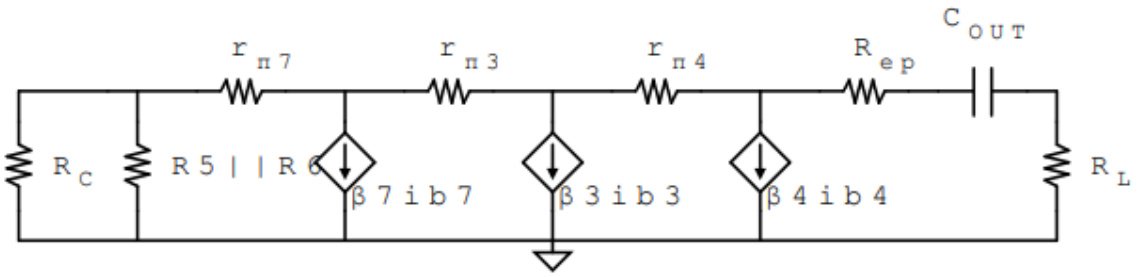
$\tau_{CC2} = C_{C2}(RIN + RC)$

using the given capacitance of 10uF we get a time constant of τ_{CC2} = 4.01s

this gives us a cutoff of 0.03959 Hz which is well within specification

Cout:

We will choose the Cout capacitor as 4700uF capacitor provided.



$$\tau_{OUT} = C_{out}(R_L + R_{ep} + \frac{\frac{\frac{r_{\pi 7}+(R_c||R_5||R6)}{(\beta_7+1)}+r_{\pi 3}}{(\beta_3+1)} + r_{\pi 4}}{(\beta_4+1)})$$

Calculating the time constant using the Cout value of 4700uF gives us τ_{OUT} = 0.038s.

Which gives us a cutoff of 4.2Hz which is below the specification of 20Hz. Thus the capacitor of 4700uF would be sufficient for use.

Gain Analysis:

Theoretically we designed for an output voltage of 17V peak with a 0.5V peak input signal

$$Av := -\frac{Vo}{Vin} = -34$$

However after some of the above values were adjusted and spice analysis we noticed a peak output voltage of 12.2V on the designed values.

This lead to a new gain of 24.4 after spice analysis.

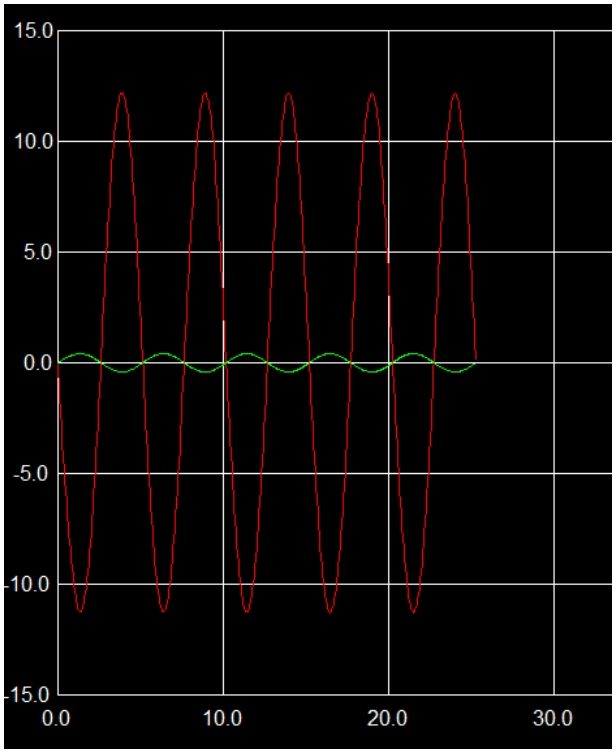


Figure 3.1

Upon testing of the circuit in practice we got an output voltage of 12.8V pk-pk using the 10X probe to measure the output from a 0.5Vpk-pk 1kHz signal and thus a gain of 25.6. which agrees much more with the spice results obtained than the theoretical calculations.

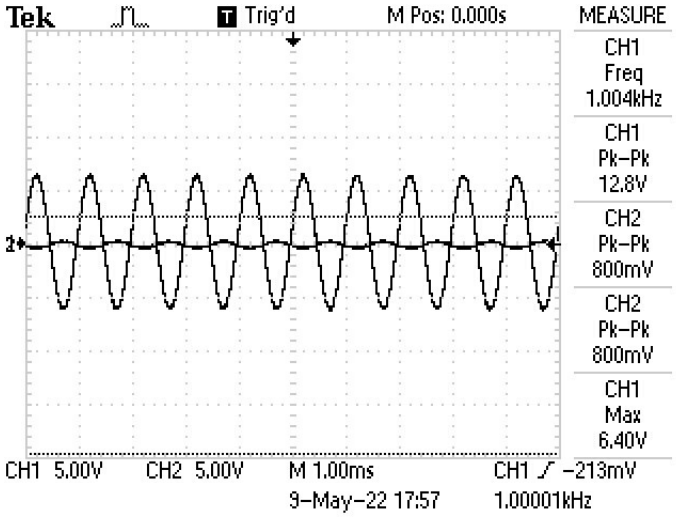


Figure 3.2

Power and Thermal Analysis:

Power Analysis

For Transistors we use the equation:

$P_Q = V_{CE} * I_C$

For Resistors we use the equation:

$P_R = V_R \hat{} 2/R$

Transistor	Power dissipated (mW)
Q1	41.3
Q2	4701
Q3	45.5
Q4	4115
Q5	29.7
Q6	3.26
Q7	27.3
Q8	5.60

Resistor	Power dissipated (mW)
R1	0.828
R2	0.386
R2var	1.16
R3	0.675
R4	14.59
R5	0.650
R6	0.728
R7	0.00373
R8	0.114
RE8	0.318
RC8	165
Ren	0.0327
Rep	0.0348
RE	0.33

We see that the maximum power dissipation in all the 2N2219A and 2N2905A are low , however the TIP41/42C transistors have a relatively high power dissipation compared to the rest. We will perform thermal analysis to see whether this high power dissipation has a significant effect on the way we design our circuit. No thermal failure for the resistors are expected as they all dissipate very low maximum power.

Thermal Analysis

2N2219A and 2N2905A

We find that the junction to ambient thermal resistances of the 2N2219A and 2N2905A are 190 K/W and 292 ◦C/W respectively from the datasheets. We assume an ambient temperature of 30 ◦ C.

2N2219A

$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	190	K/W

2N2905A

$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	292	437.5	°C/W

Thus $T_{2N2219A} = \theta_{amb} + \theta_{2N2219A\ (j-a)} P_{2N2219A\ (max)}$

$= 37.828\ ^\circ C$

AND

$T_{2N2905A} = \theta_{amb} + \theta_{2N2905A\ (j-a)} P_{2N2905A\ (max)}$

$= 43.29\ ^\circ C$

The max operating junction temperature for the 2N2219A and 2N2905A are however 200◦C , which is well above the calculated temperatures of the transistors. This means that heat sinks are not required to use for the 2N2219A and 2N2905A transistors.

TIP41C and TIP42C

Calculating from datasheet and using the power derating curve.

T_J	Max. operating junction temperature	150	°C

(T_{case} = 25°C; unless otherwise specified)

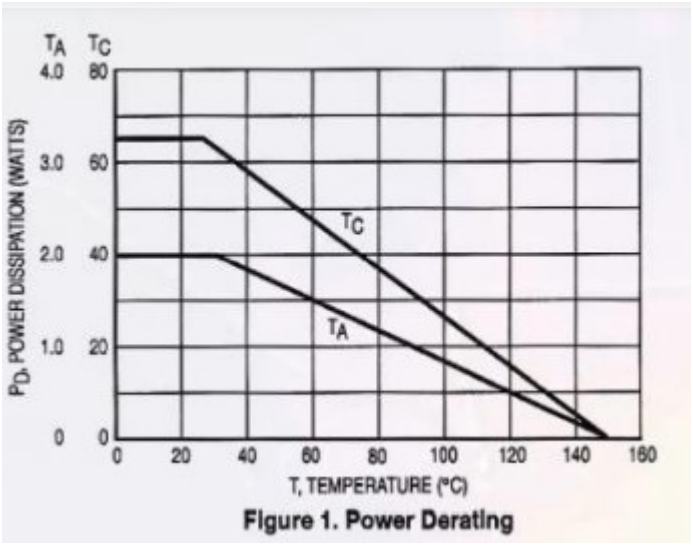


Figure 1. Power Derating

$\theta_{j-c} = (Tj-Tc)/P = (150-25)/65 = 1.92\ ^\circ C/W$

$\theta_{j-a} = (Tj-Ta)/P = (150-30)/2 = 60^\circ C/W$

thus $\theta_{c-a} = 58.08\ ^\circ C/W$

at maximum power the transistors reach a temperature of

$T_{TIP41/42C} = \theta_{amb} + \theta_{TIP41/42C\,(j-a)} P_{TIP41/42C\ (max)}$

$= 312^{\circ}C$

However the max operating temperature of the transistors are 150◦C. This means that the temperatures far exceed the max operating temperature we need to lower the thermal resistance between device and ambient and thus heat sinks will need to be implemented.

Assuming thermal paste is applied appropriately we can say θ_{c-s} = 1◦C/W. The heat sink plates are secified as Aluminium plates, 80x50x2 mm.

Using online calculator and above specifications we get

Θ_{s-a} = 11.5◦C/W

thus

$Tj = \theta_{amb} + (\theta_{j-c} + \theta_{c-s} + \theta_{s-a}) P_{Q(max)}$

We can now calculate the new operating temperatures of our TIP41/42C transistors.

Q2 = 97.87◦C

Q4 = 89.33◦C

This falls within the operating temperature of 150◦C and thus it is safe to use Q4 and Q2 with heat sinks. After spice analysis the following temperatures were obtained by running it through the testbench

```
-----------------------------+------+------------------+--------------------
Safe Op. Area (@1kHz): PASS | NULL | BJTs within SOA | BJTs inside SOA
T(power npn).....: PASS | NULL | Below 150 C.... | 95.3583 C
T(power pnp).....: PASS | NULL | Below 150 C.... | 97.1441 C
```

As we can see the spice code passed the valid operating temperatures and thus our calculations are valid and satisfactory. We assumed that it is thus safe to build our circuit.

Results and Conclusions:

Results:

Upon rigorously calculating all the above values and running the tests through spice it is safe to assume that we can build our circuit using all the above values. The practical circuit performed fairly close to our spice results with similar gain as well as temperatures not getting too hot and transistors and resistors not blowing up from thermal failure. Any discrepancies in values could be explained by varying beta values in some transistors compared to theoretically predicted values. The use of long wires to connect certain parts of our circuits where the magnetic fields running through the wires can have an effect on the e-fields of other wires not running through the same node. As well as longer wires having a higher resistance which in effect can affect the currents of our circuit.

Our spice results from the given testbench were as follows

```
Power amplifier test results

+----------------------------+------+----------------+-----------------------------+
|Smoke test (Hard P/F): P/F. | .... | ..Hard limit... | .......Test result......... |
+----------------------------+------+----------------+-----------------------------+
|Safe Op. Area (@1kHz): PASS | NULL | BJTs within SOA | BJTs inside SOA
|T(power npn).........: PASS | NULL | Below 150 C.... | 95.3583 C
|T(power pnp).........: PASS | NULL | Below 150 C.... | 97.1441 C
+----------------------------+------+----------------+-----------------------------+
|Test param. (scoring): P/F. | Mark | ...Benchmark... | .......Test result......... |
+----------------------------+------+----------------+-----------------------------+
|ii(max)..............: PASS | ..1. | Below 1 mA..... | 0.0404621 mA
|Psig(speaker) @ 40Hz : PASS | ..1. | Above 8 W...... | 12.4421 W
|Psig(speaker) @ 1kHz : PASS | ..1. | Above 8 W...... | 12.6111 W
|Psig(speaker) @ 20kHz: PASS | ..1. | Above 8 W...... | 10.2097 W
|Psig(spk) (vi=1mV)...: PASS | ..1. | Above 0.5E-5 W. | 5.37529E-05 W
|Pwr efficiency @ 1kHz: PASS | ..1. | Above 45 %..... | 53.9605 %
|THD @ 1kHz (full pwr): PASS | ..1. | Below 4 %...... | 1.67889 %
|THD @ 40Hz (full pwr): PASS | ..1. | Below 4 %...... | 1.46564 %
|THD @ 20kHz (fll pwr): PASS | ..1. | Below 4 %...... | 2.63698 %
|THD @ 1kHz (vi=1mV)..: PASS | ..1. | Below 0.2 %.... | 0.00564239 %
+============================+======+================+=============================+
|FINAL RESULT.........: PASS | .10 .| ... Achievement score: 126.973
+============================+======+
```

Conclusion:

To conclude our circuit satisfied all the specifications required but could still be improved by pushing the limits of our circuit, better build to further improve the efficiency and get a closer result to our theoretically calculated circuit.