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Course Hero

CSEE W4823 Advanced Logic Design
Lab Assignment #7

1. Write the RTL code in Verilog (.v) for the all the memory blocks such as IMEM, CMEM, and registers. Use the memory complier to generate SRAM arrays that should be instantiated in those memory blocks. Write the testbench to verify its functionalities

2. Synthesize the above RTL to get the gate-level netlist (nl.v). Verify the functionality by using the testbench that is similar to the one used above.

3. Perform timing and power analysis using PrimeTime. Include the VCD files for accurate power estimation.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab_7.zip" through Courseworks. The .zip file should contain the following:

- Report for the above tasks. Please include figures to support.
- .v files for your RTL code and ModelSim testbench.
- .nl.v files from the logic synthesis
- .tcl file for the logic synthesis
- .tcl file for your PrimeTime script
- .vcd file from QuestaSim