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CSEE W4823 Advanced Logic Design
Homework Assignment #2

1. Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.

2. Determine the number of gates needed to implement an n-bit carry-lookahead adder, assuming no fan-in constraints. Use AND, OR, and XOR gates with any number of inputs.

3. An arithmetic logic unit (ALU) is a logic circuit that performs various Boolean and arithmetic operations on n-bit operands. The table below specifies the functionality of a simple ALU. This ALU has 2 four-bit data inputs, A and B, a three-bit select input, S, and a four-bit output F. As the table shows, F is defined by various arithmetic or Boolean operations on the inputs A and B. Each Boolean operation is done in a bitwise fashion. For example, F = A AND B produces the four-bit results $f_0=a_0b_0$, $f_1=a_1b_1$, $f_2=a_2b_2$, and $f_3=a_3b_3$. Please describe this ALU in Verilog. Please use the case statement.

Operation	Inputs $s_2\ s_1\ s_0$	Outputs F
Clear	0 0 0	0 0 0 0
B–A	0 0 1	$B - A$
A–B	0 1 0	$A - B$
ADD	0 1 1	$A + B$
XOR	1 0 0	A XOR B
OR	1 0 1	A OR B
AND	1 1 0	A AND B
Preset	1 1 1	1 1 1 1