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Course He

CSEE W4823 Advanced Logic Design
Lab Assignment #2

1. Synthesize the RTL code from the Lab Assignment #1 (adder) through Design Compiler to get the gate-level netlist (.nl.v).

2. Compare the results between using larger (1 pF) vs. smaller (0.01 pF) output loading. Are there any differences in the synthesized netlist? In each case, what is the approximate area of your design? Run the Questrasim/ModelSim simulation of your synthesized netlist and check the functionality of synthesized result. (Hint: you need to include the standard cell library to simulate synthesized netlist, which is located at /courses/ee6321/share/ibm13rflpvt/verilog/ibm13rflpvt.v)

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab2.zip" through Courseworks. The .zip file should contain the following:

- .nl.v files from the logic synthesis
- .tcl file used in the logic synthesis
- Brief report for the above questions. Please include supporting figures, such as the screenshots of the ModelSim results (waveform and automatic result matching) and Design Compiler's reports.