Appendix I
Synthesizable and Non-Synthesizable Verilog Constructs

The list of synthesizable and non-synthesizable Verilog constructs is tabu-lated in the following Table

Verilog Constructs	Used for	Synthesizable construct	Non-Synthesizable Construct
module	The code inside the module and the endmodule consists of the declarations and functionality of the design	Yes	No
Instantiation	If the module is synthesizable then the instantiation is also synthesizable	Yes	No
initial	Used in the test benches	No	Yes
always	Procedural block with the reg type assignment on LHS side. The block is sensitive to the events	Yes	No
assign	Continuous assignment with wire data type for modeling the combinational logic	Yes	No
primitives	UDP's are non-synthesizable whereas other Verilog primitives are synthesizable	Yes	No
force and release	These are used in test benches and non-synthesizable	No	Yes
delays	Used in the test benches and synthesis tool ignores the delays	No	Yes
fork and join	Used during simulation	No	Yes
ports	Used to indicate the direction, input, output and inout. The input is used at the top module	Yes	No
parameter	Used to make the design more generic	Yes	No
time	Not supported for the synthesis	No	Yes

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real	Not supported for synthesis	No	Yes
functions and task	Both are synthesizable. Provided that the task does not have the timing constructs	Yes	No
loop	The for loop is synthesizable and used for the multiple iterations.	Yes	No
Verilog Operators	Used for arithmetic, bitwise, unary, logical, relational etc are synthesizable	Yes	No
Blocking and non-blocking assignments	Used to describe the combinational and sequential design functionality respectively	Yes	No
if-else, case, casex, casez	These are used to describe the design functionality depending on the priority and parallel hardware requirements	Yes	No
Compiler directives (‘ifdef,‘undef, ‘define)	Used during synthesis	Yes	No
Bits and part select	It is synthesizable and used for the bit or part select	Yes	No