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CSEE W4823 Advanced Logic Design
Lab Assignment #1

1. Write the Matlab code (.m) for the 12-bit adder function. The adder takes two 12 bit inputs and produce one 12 bit outputs, all in the two's complement format. Please design the adder to have input flip-flops to stores input but no output flip-flops. Make the testbench in Matlab to test the adder function with randomly generated 100 data and produce the results of the adder's operation to a text file.

2. Write the RTL code in Verilog (.v) for the above adder circuit and write the testbench to simulate your code through QuestaSim (Modelsim). Are your results matching to the results from the Matlab code? Make the testbench automatically compare the result to the Matlab's result file.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab1.zip" through Courseworks. The .zip file should contain the following:

- .m files for your Matlab code
- .v files for your RTL code and ModelSim testbench.
- Brief report for the above questions. Please include the screenshots/figures of the Matlab and ModelSim simulations to support your report.