
DO NOT SHARE
SLIDES AND CLASS MATERIALS
ON ONLINE SITES
Course He

CSEE W4823 Advanced Logic Design
Lab Assignment #4

1. Write the RTL code in Verilog (.v) for the SRAM memory block of 16 kB by instantiating multiple memory-compiler-generated SRAM modules. Write a testbench that performs and verify the write and read operation of the entire memory.

2. Synthesize the above RTL to get the gate-level netlist (nl.v). Treat the memory-complier-generated SRAM modules as a black-box (i.e., don't synthesize those modules into the netlist). Verify the functionality by using the testbench that is similar to the one used above.

3. Perform timing and power analysis using PrimeTime. Include the VCD files for accurate power estimation.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab4.zip" through Courseworks. The .zip file should contain the following:

- .v files for your RTL code and ModelSim testbench.
- .nl.v files from the logic synthesis
- .tcl file for the logic synthesis
- .tcl file for your PrimeTime script
- .vcd file from QuestaSim
- Brief report for the above tasks. Please include some figures to support your report, such as the screenshots of PrimeTime timing/power reports. Please also report the throughput of your memory.