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Course Hero

Advanced Logic Design
FPGA

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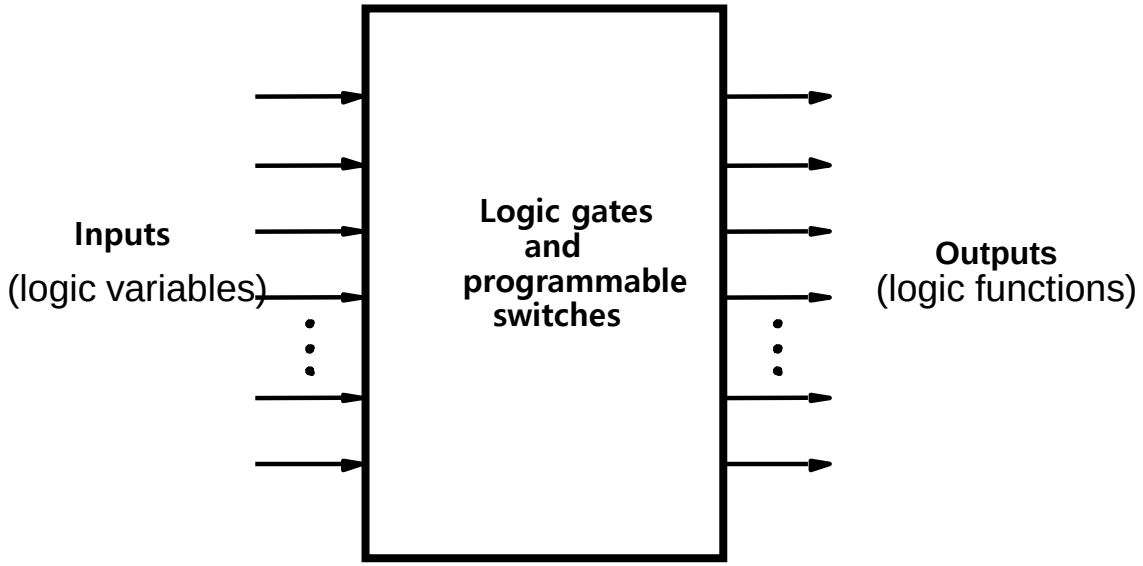
Columbia University

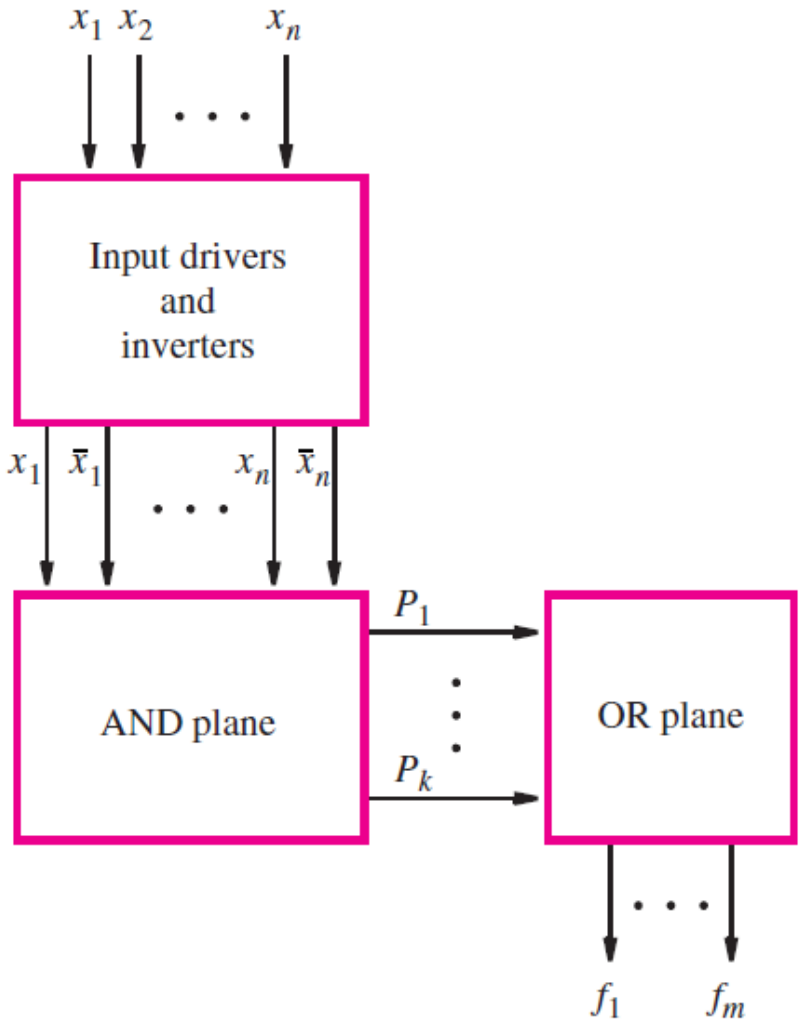
(1) BV: Secs. B.6, B.10; (2) J. F. Wakerly “Digital Design: Principles and Practices,” 4th Edition, Prentice Hall (2006), pp.850-862

Programmable Logic Array

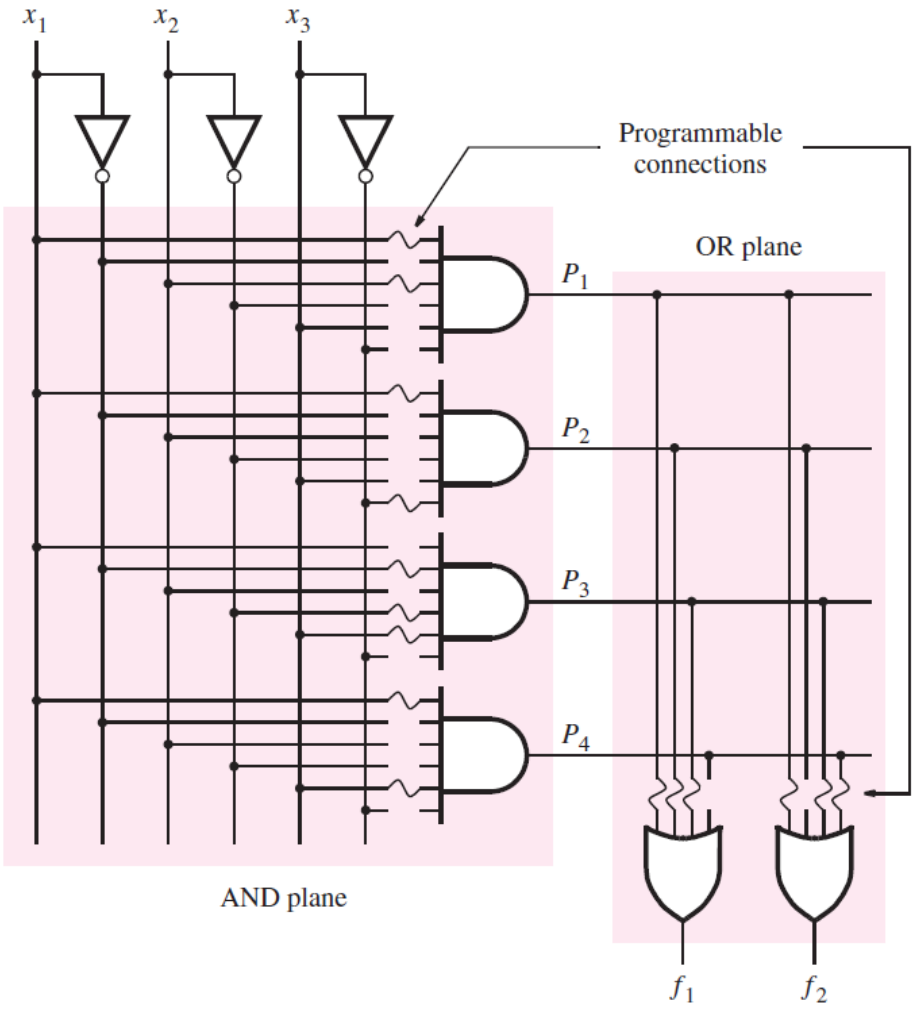


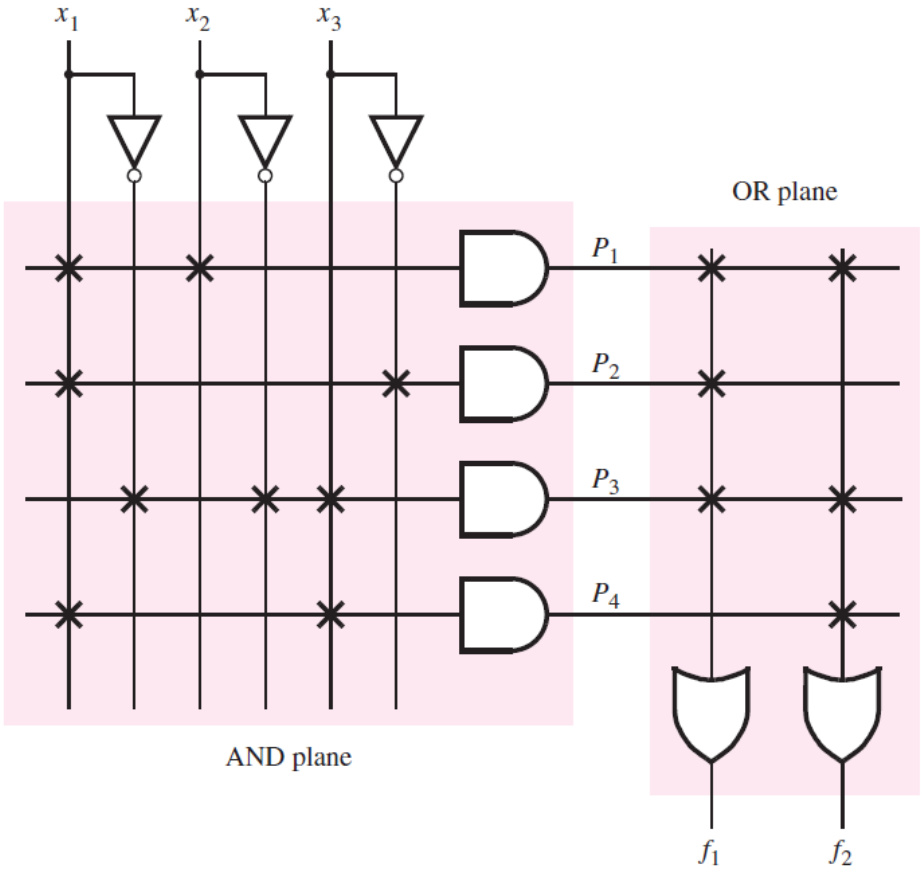
- A early version of FPGA, which allows users to program a rather complicated logic function in a single chip

General Structure of a PLA

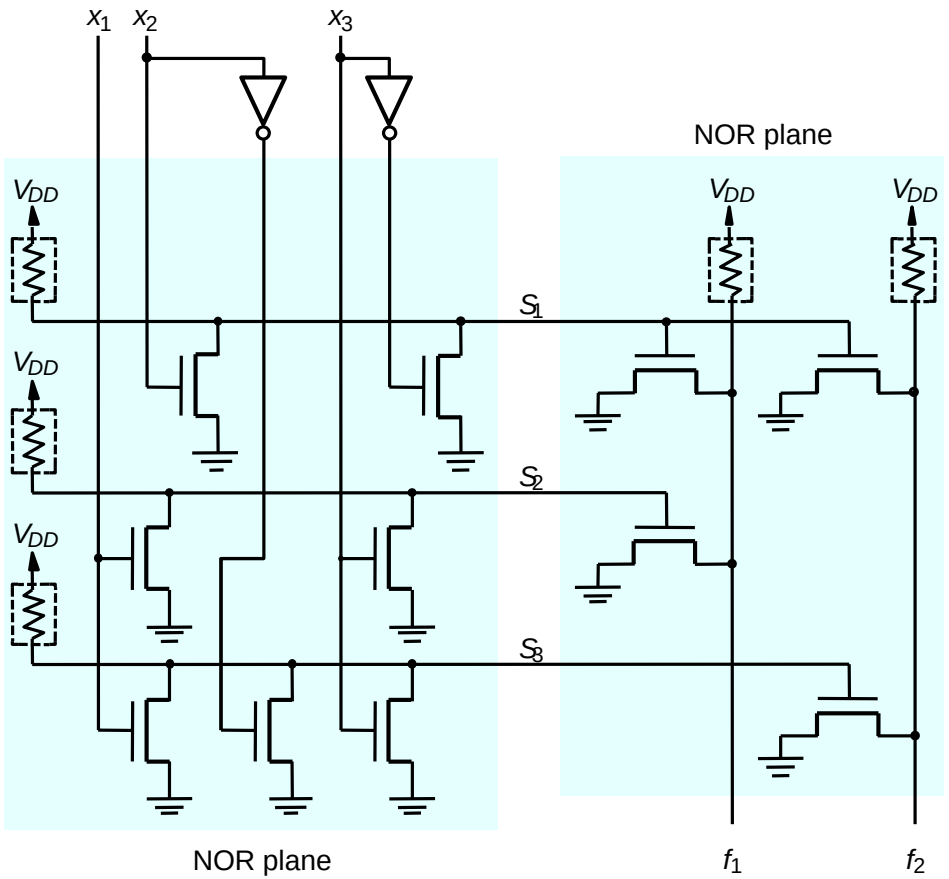


PLA: Detail


x_1
x_2
x_3
Programmable connections
OR plane
P_1
P_2
P_3
P_4
AND plane
f_1
f_2

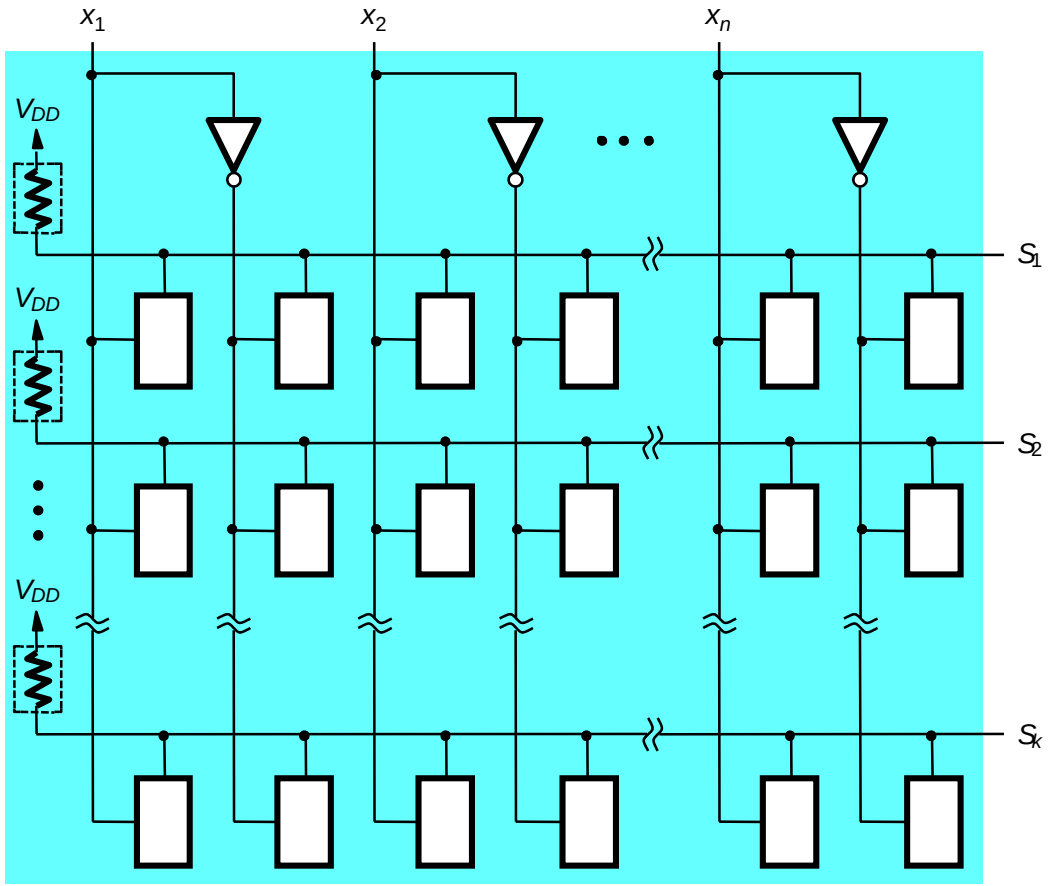

x_1
x_2
x_3
OR plane
P_1
P_2
P_3
P_4
AND plane
f_1
f_2

NOR-NOR PLA

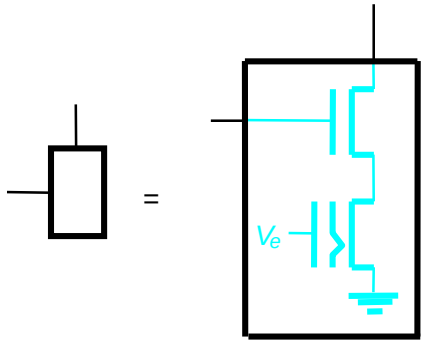


- NOR is preferred for large fan-in gates
- Resistor-load is preferred over CMOS

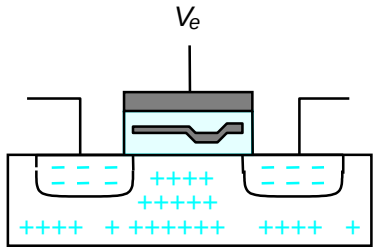
F(ield)PLA



(a) Programmable NOR-plane

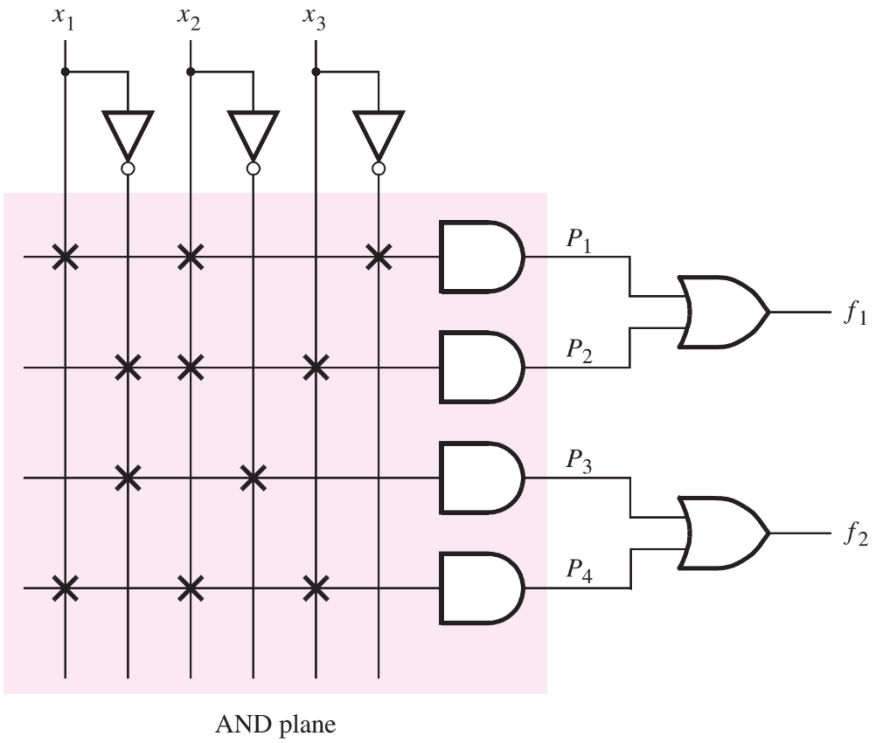


(b) A programmable switch



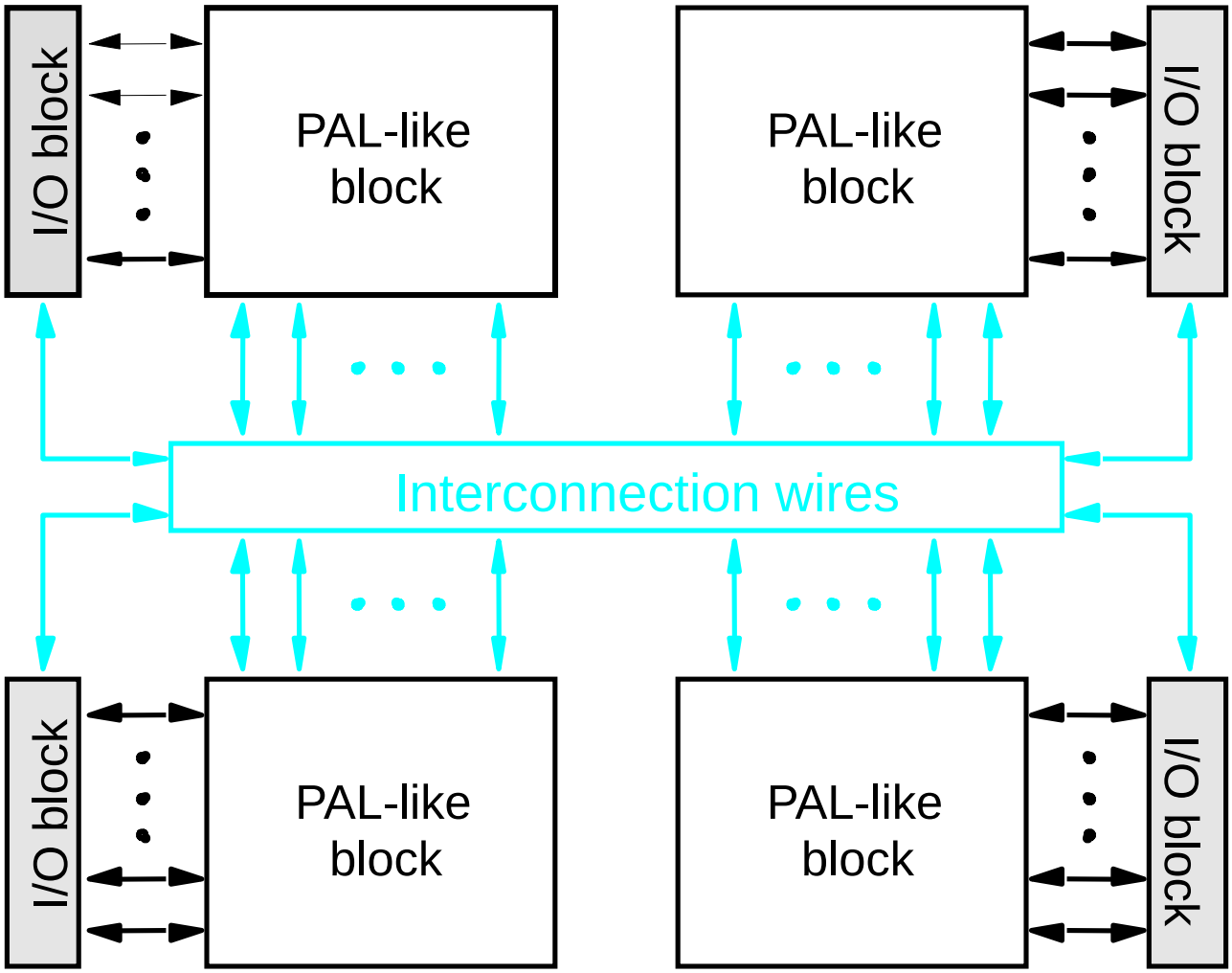
(c) EEPROM transistor

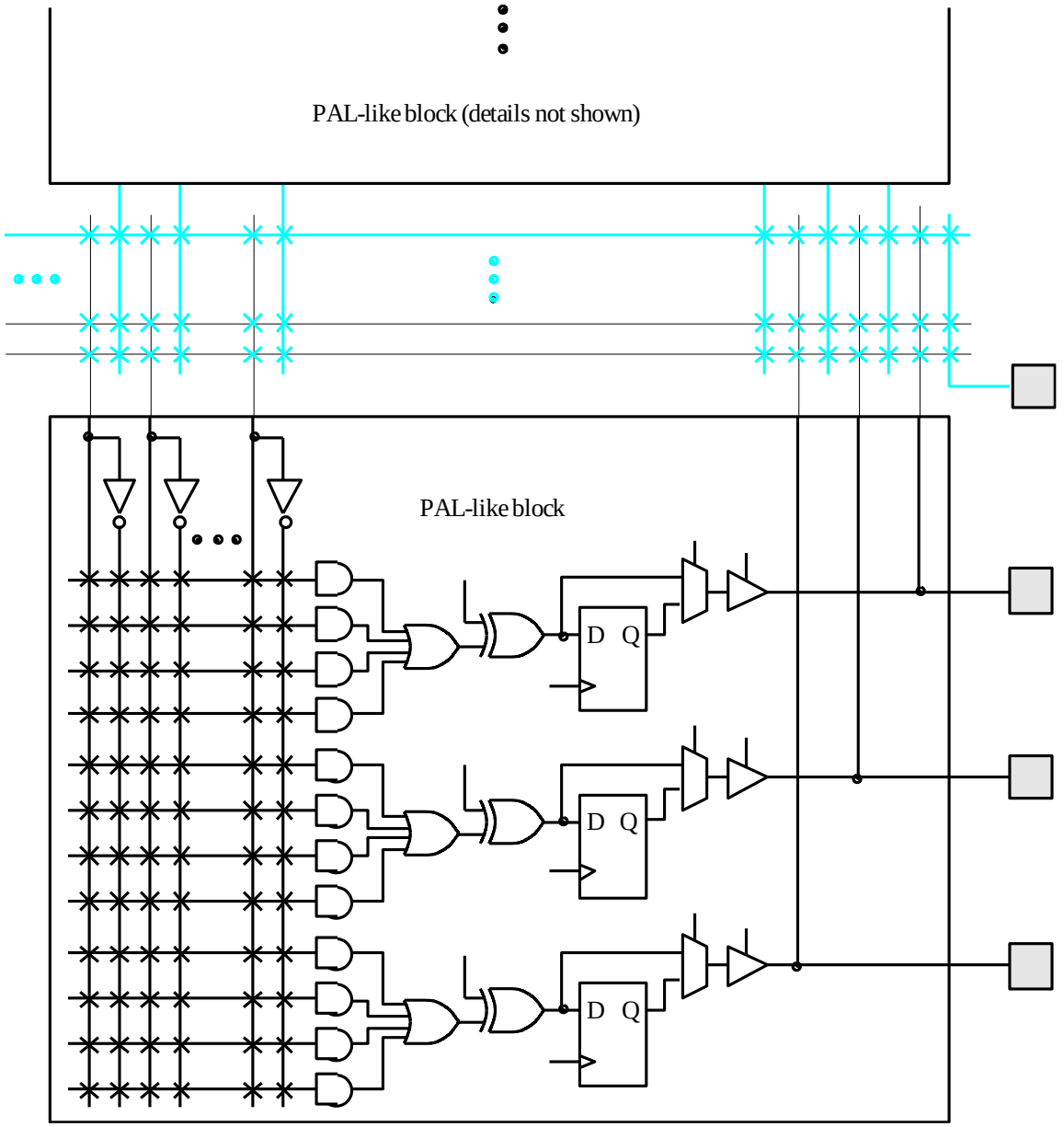
PAL: Programmable Array Logic



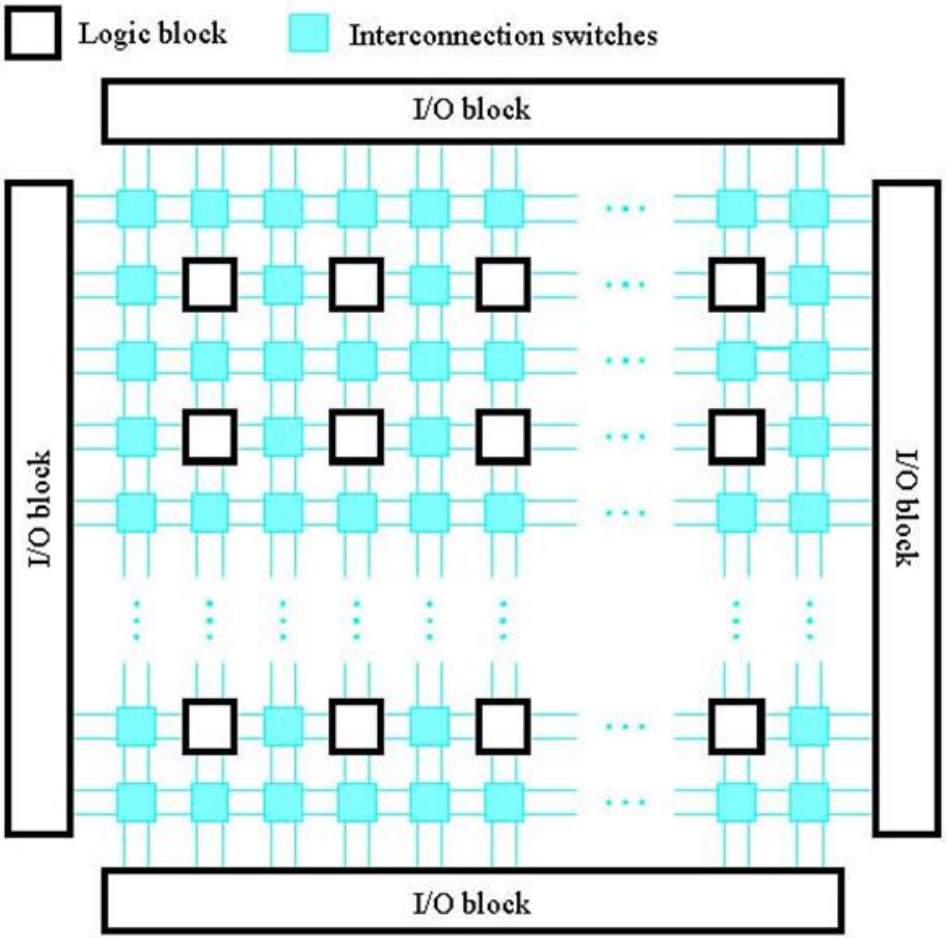
- The AND plane is programmable but the OR plane is fixed.
- To relieve the fabrication complexity of programmable switches

Complex PLD

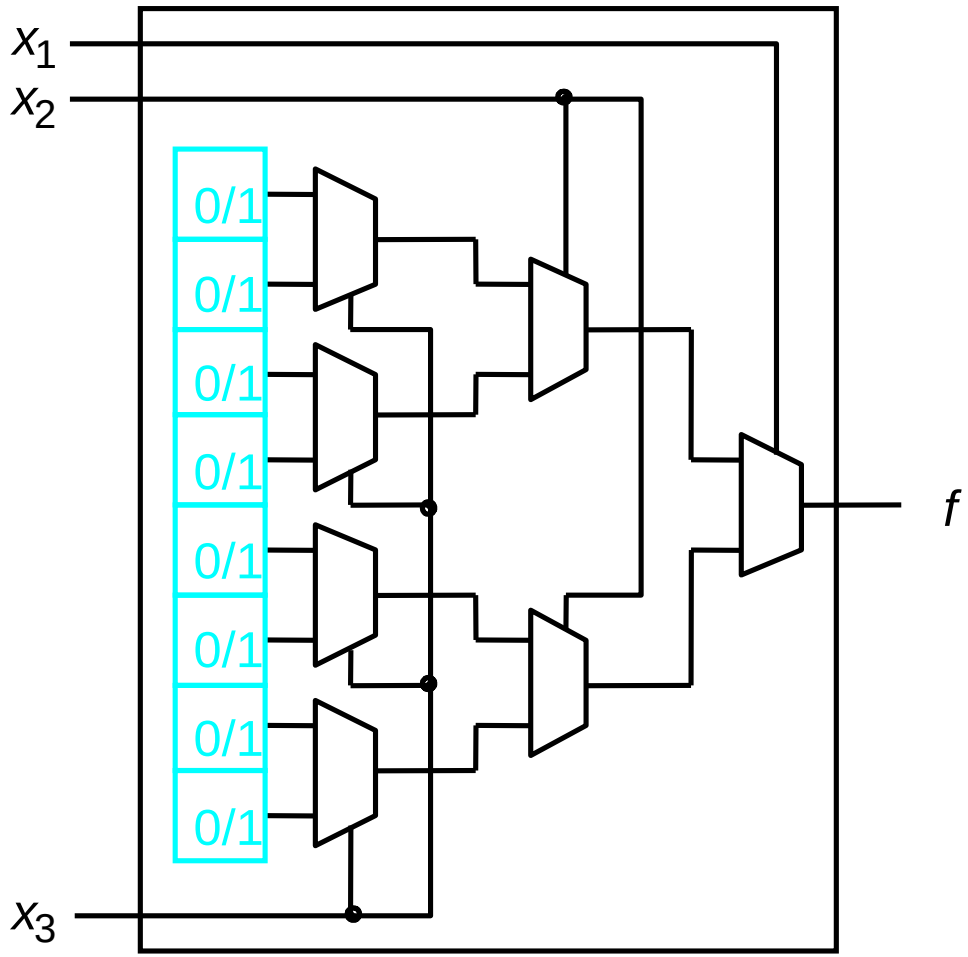

I/O block
PAL-like block
PAL-like block
I/O block
Interconnection wires
I/O block
PAL-like block
PAL-like block
I/O block


PAL-like block (details not shown)
PAL-like block
D Q
D Q
D Q

Field Programmable Gate Array

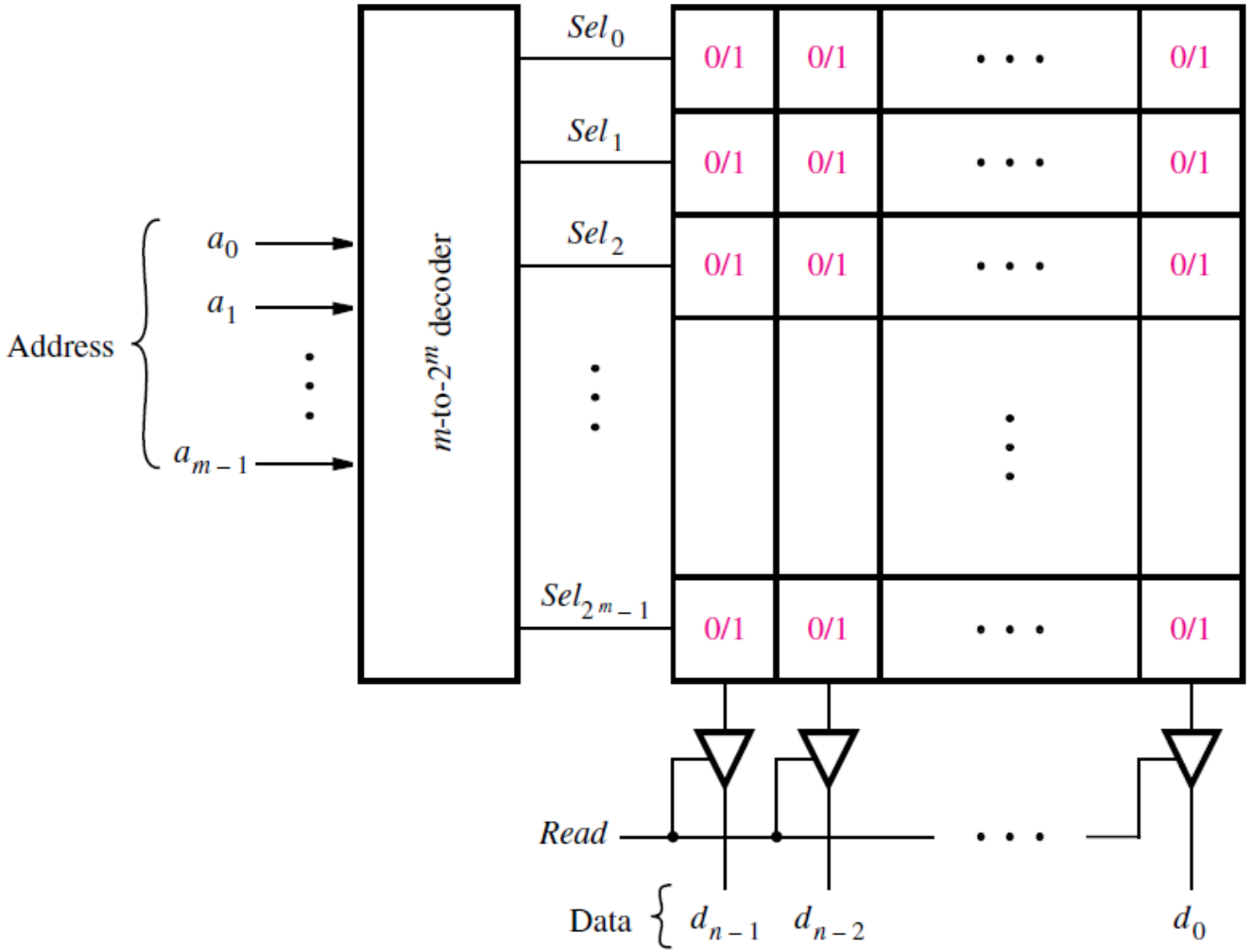


LUT for Logic Function

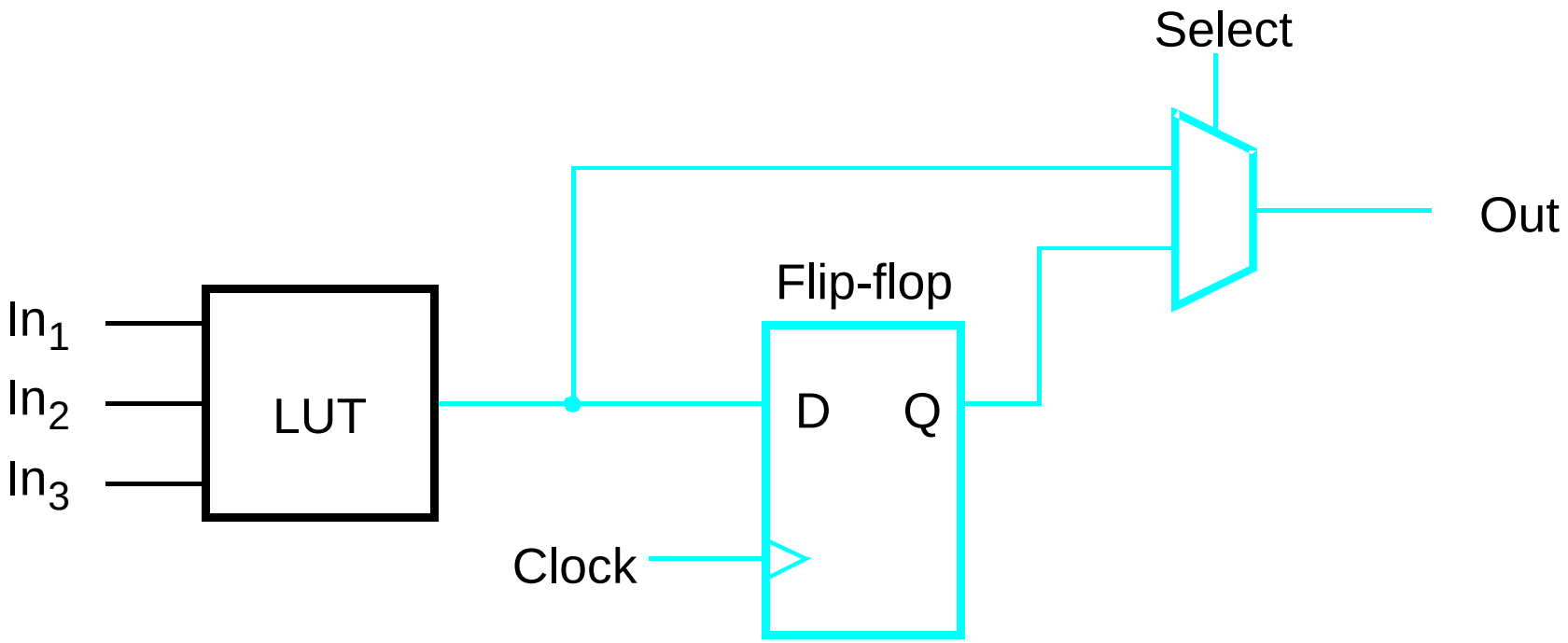


- 3 inputs: 8-W latches
- 4 inputs: 16-W latches
- 5 inputs: 32-W latches
- Granularity vs overhead → 4 to 6 inputs are commonly found

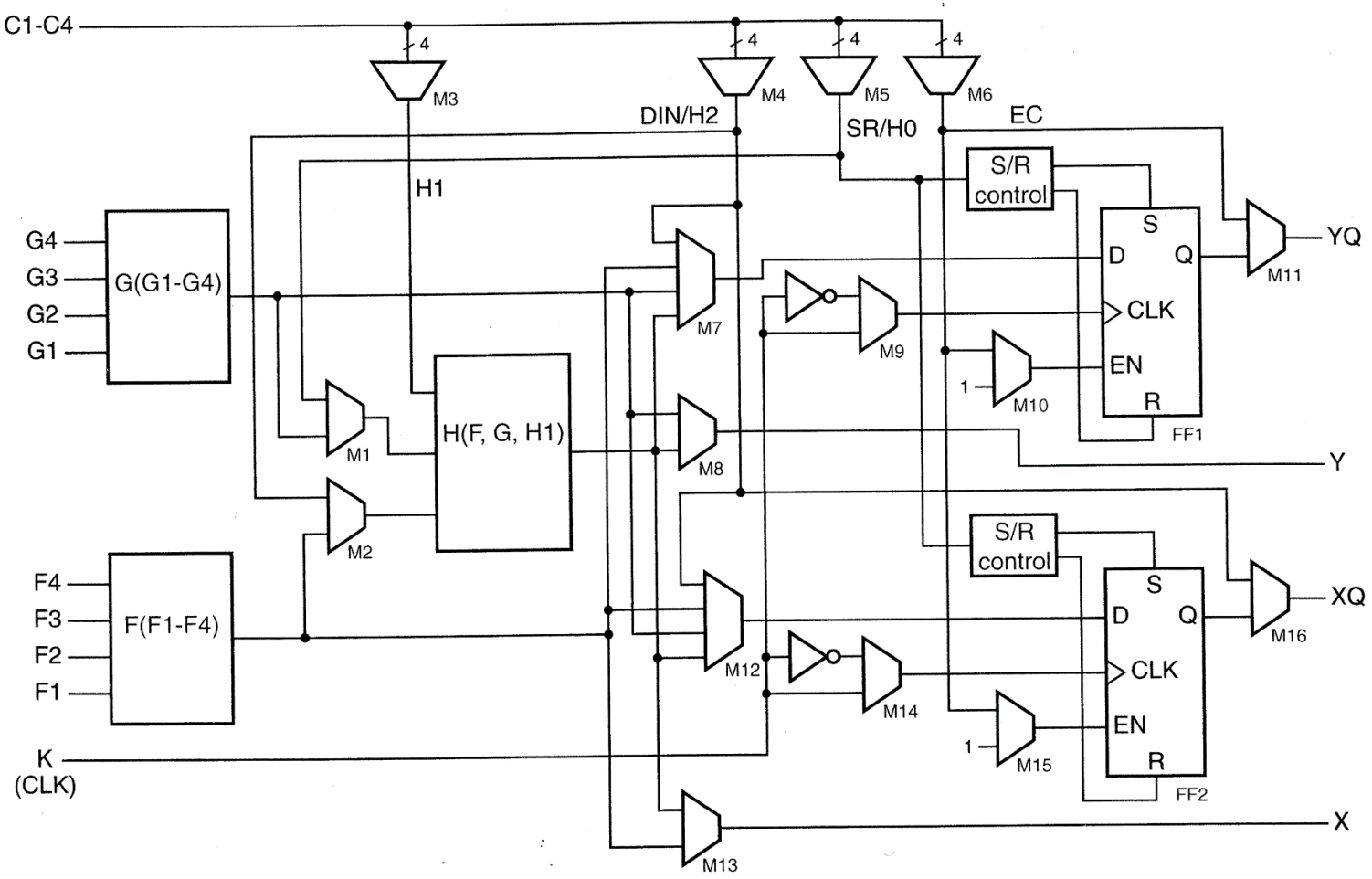
Another LUT Implementation



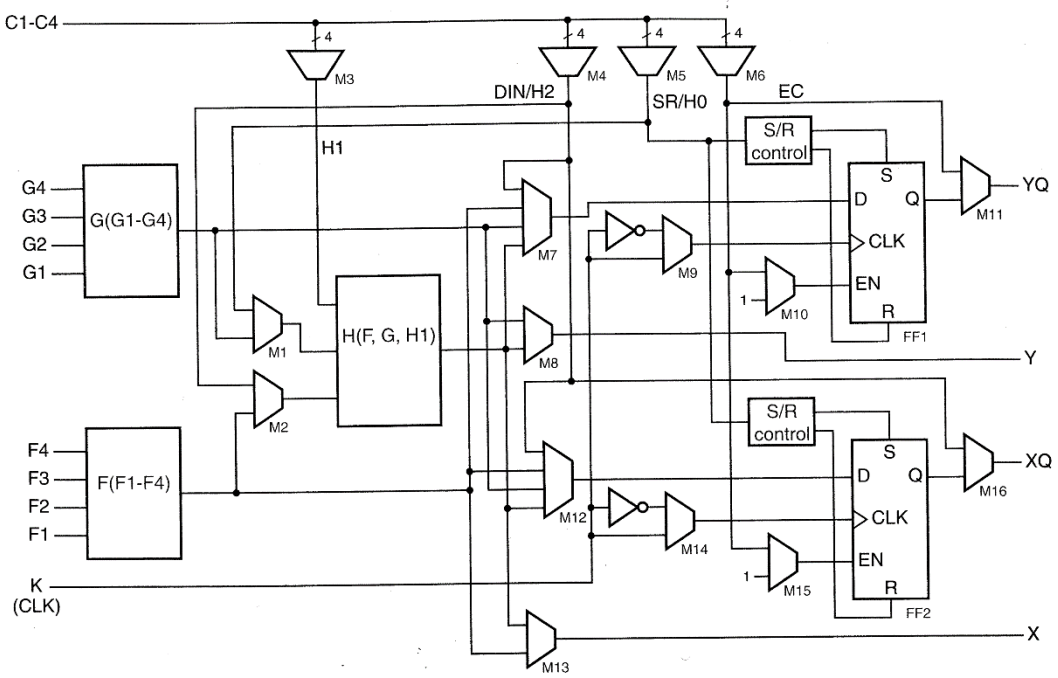
Pipelining/Sequencing



Configurable Logic Block (CLB)

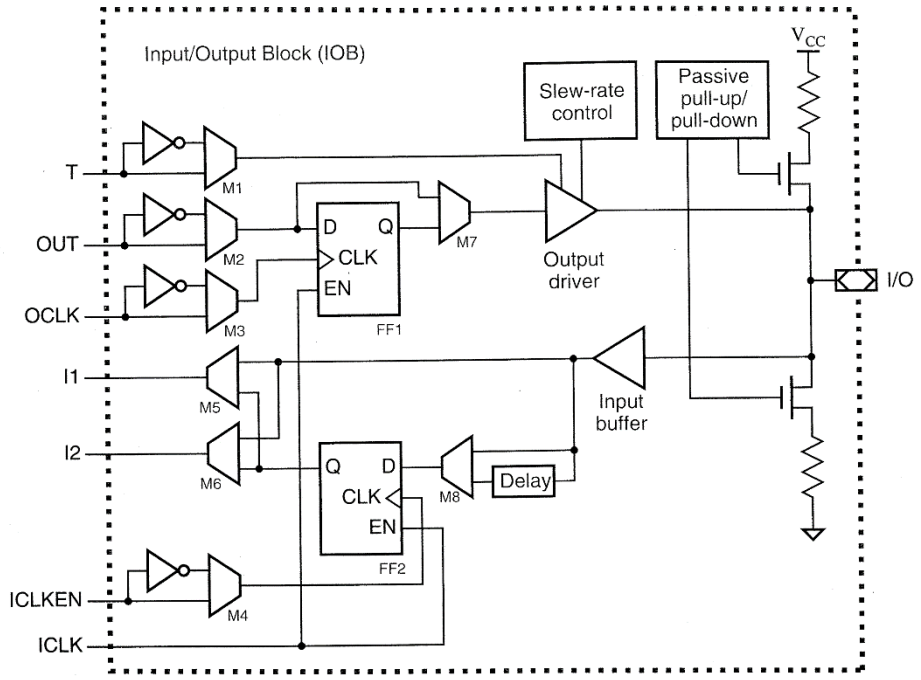


Configurable Logic Block (CLB)



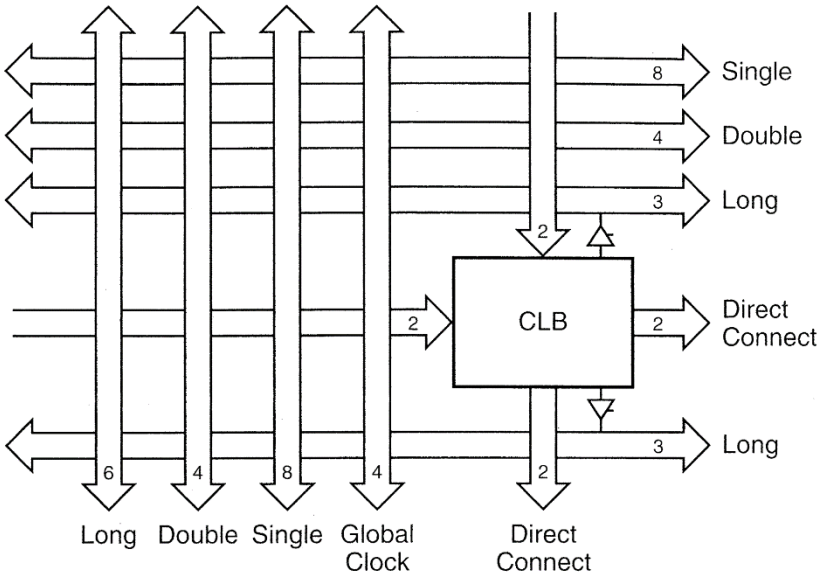
- 12 inputs, 4 outputs, 1 clock
- Three LUTs (G, F, H); 4-input and 3-input
- M9, M14 for rising, falling edge selection
- S/R: set and reset control
- Clocked and non-clocked output support
- LUTs can be programmed as a data storage during the start-up

IO Block



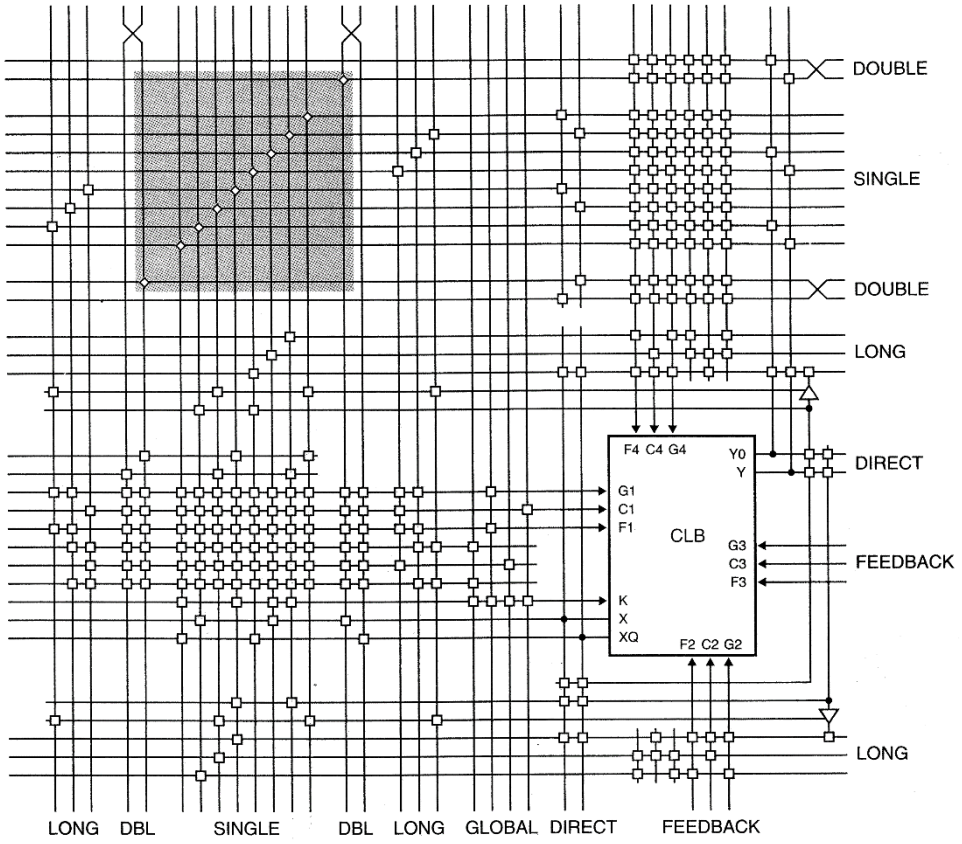
- M5, M7: clocked input and output selection
- Delay: slow down the input data relative to ICLK (FPGA internal clock) to avoid hold time violation
- M1-M4: polarity inversion
- Analog control: slew rate and passive pull-up and –down selection

Interconnect

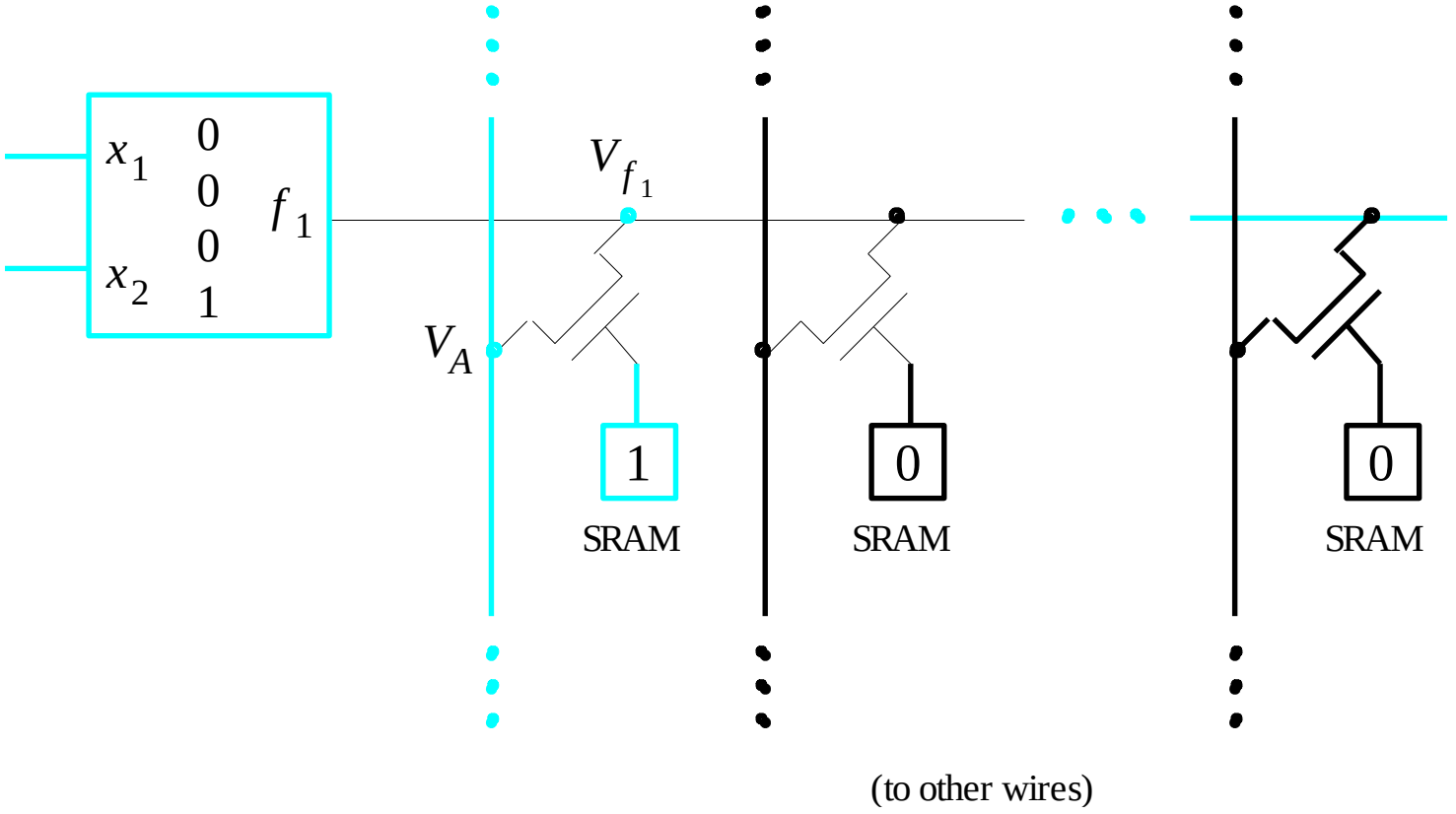


- Direct: direct connection to nearby CLBs; unidirectional
- Double and single: respectively have hops (programmable switches) in every two and every CLBs
- Long: data travels all the way across a row or a column without hops, and driven by tri-state drivers near CLBs (something like a bus)

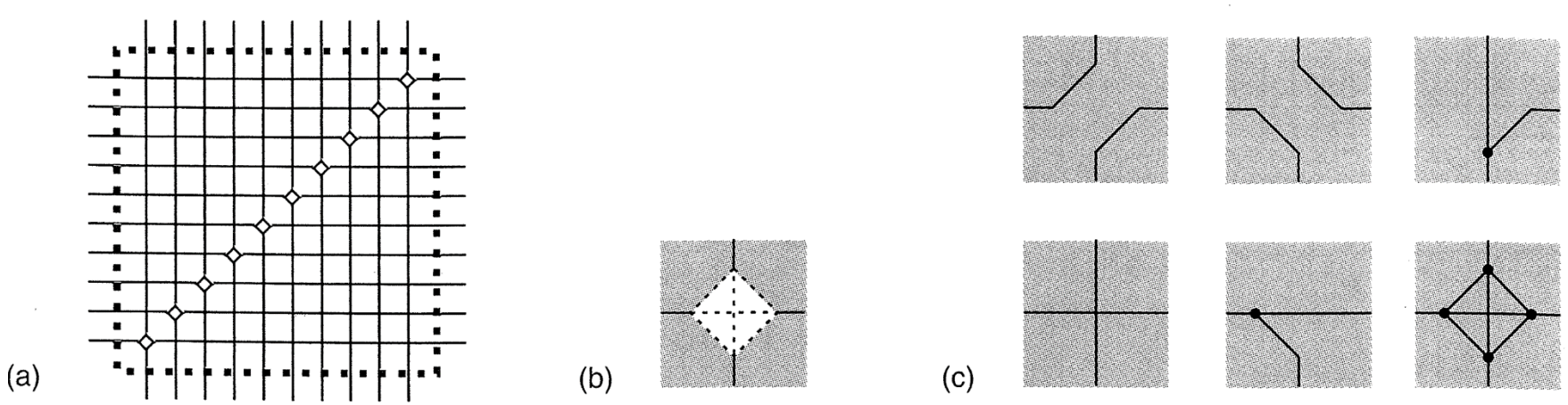
Interconnect



Connecting Interconnects

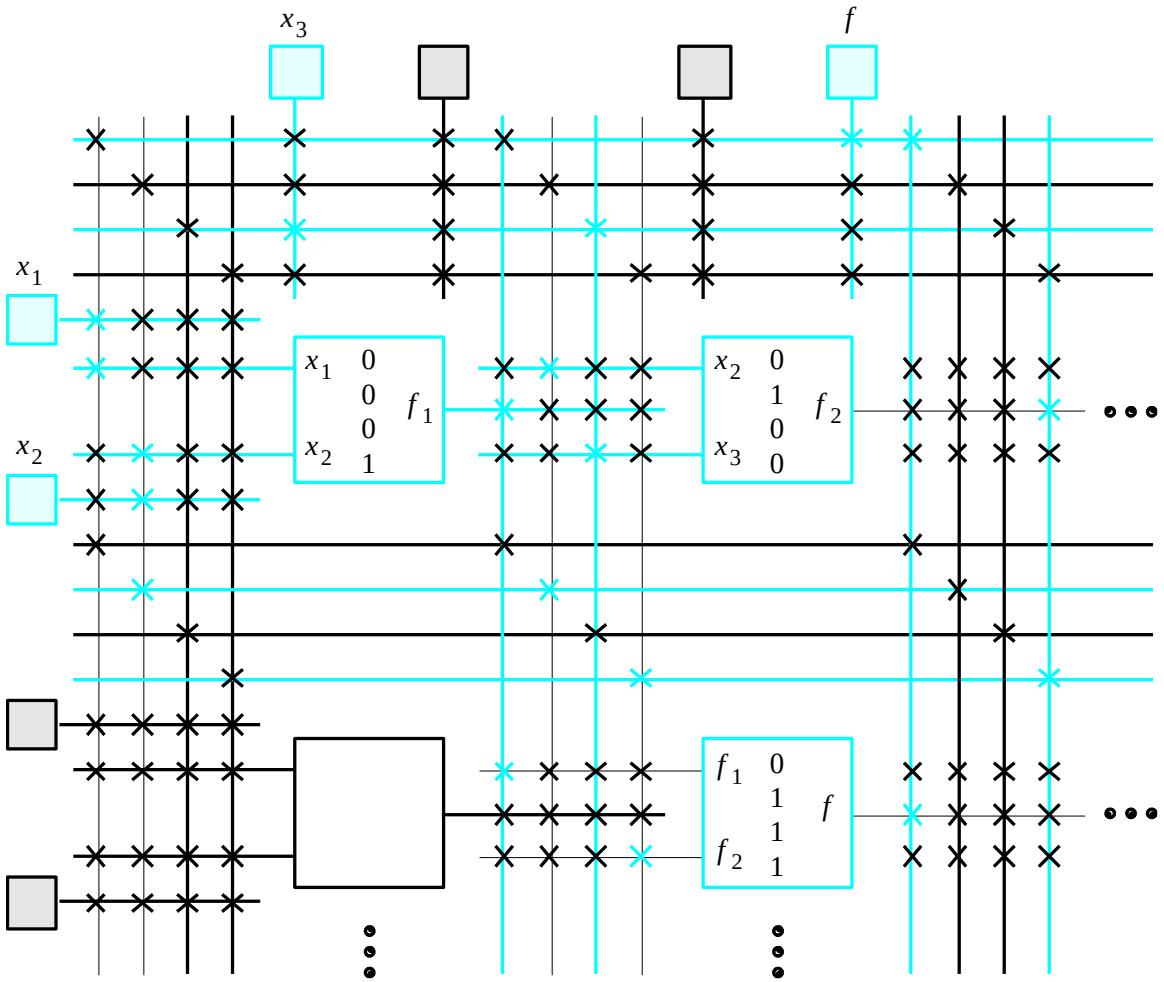


PSM: Programmable Switch Matrix



- Connecting the four wires in various ways
- Six exemplary connections

FPGA Programming Example



- f_1=?
- f_2=?
- f=?