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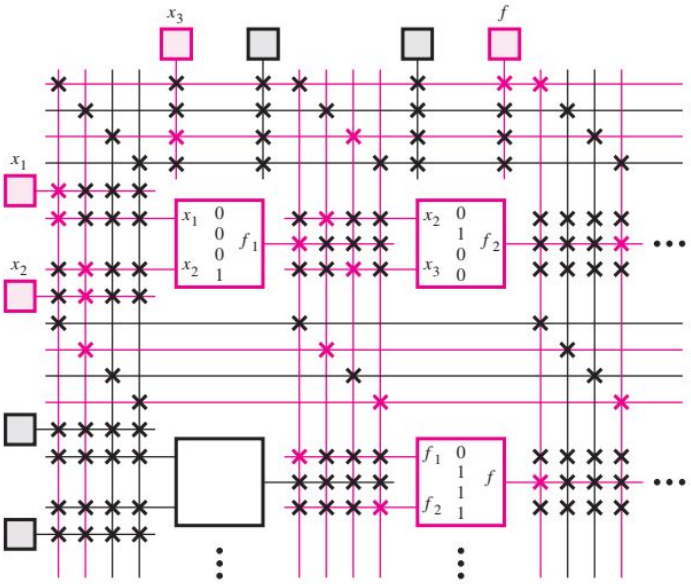
CSEE W4823 Advanced Logic Design
Homework Assignment #5

1. Consider the function $f(x_1, x_2, x_3) = x_1x_2' + x_1x_3 + x_2x_3'$. Show a circuit using 5 two-input lookup-tables (LUTs) to implement this expression. As shown in the figure below, give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.



2. Consider the circuit in the figure below. Are all single stuck-at-0 and stuck-at-1 faults in this circuit detectable? If not, explain why.