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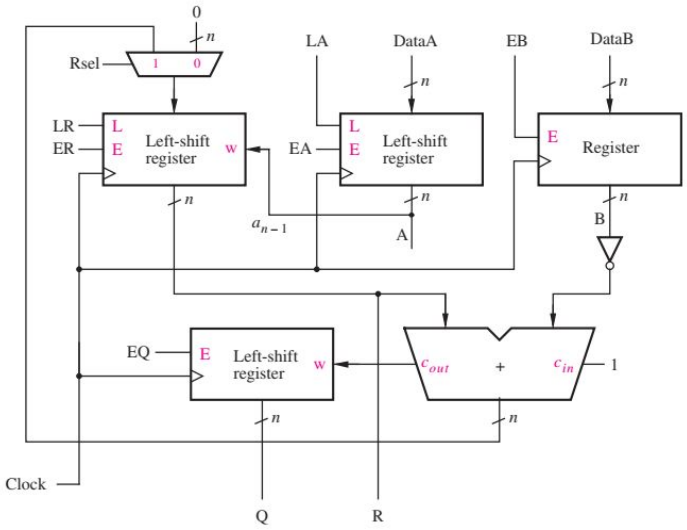
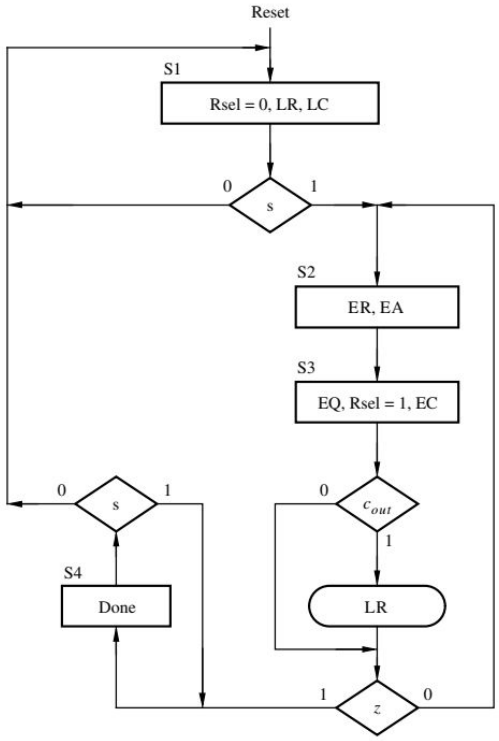
Course He

CSEE W4823 Advanced Logic Design
Homework Assignment #3

1. Write Verilog code for the divider circuit that has the datapath below and the control circuit represented by the ASM chart below.





2. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?