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Course Hero

CSEE W4823 Advanced Logic Design
Lab Assignment #9

1. Write the RTL code in Verilog (.v) for the FIR core. Use the building blocks that you created in the previous labs.

2. Synthesize the above RTL to get the gate-level netlist (nl.v). Verify the functionality by using the testbench that is similar to the one used above.

3. Perform timing and power analysis using PrimeTime. Include the VCD files for accurate power estimation.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab_9.zip" through Courseworks. The .zip file should contain the following:

- Final report:
  - Three power point slides
    - Page 1: Title slide: include the team name and the UNIs of the members
    - Page 2: Architecture: the top-level architecture of your FIR core in the testbench
    - Page 3: the metrics. Please refer the L07 slide pp. 9. Include both methods and results
  - A final report of the project which contains the details of your design. Please write the report in IEEE double-column format. The template could be found in this link: https://www.ieee.org/conferences/publishing/templates.html
- .v files for your RTL code and ModelSim testbench.
- nl.v files from the logic synthesis
- .tcl file for the logic synthesis
- .tcl file for your PrimeTime script
- .vcd file from QuestaSim