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Course Hero

Advanced Logic Design
Project Guideline

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Project

$$y[n] = \sum_{i=0}^{N} b_i \cdot x[n-i]$$

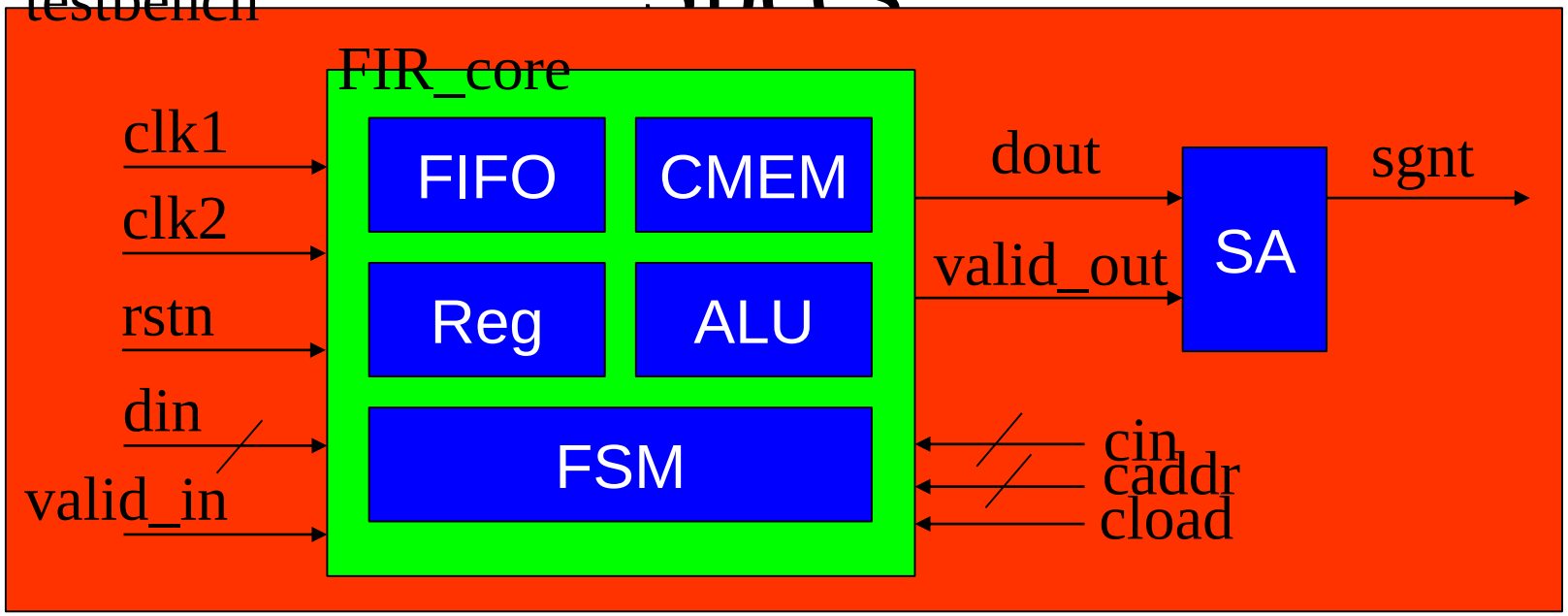
x[n] is the input signal, *y[n]* is the output signal, *N* is the filter order (number of taps), b_i is the filter coefficient

- Goal: Design a 64-tap 16-bit FIR filter
- This computation is also known as discrete convolution

Matlab Code

- https://www.mathworks.com/matlabcentral/fileexchange/31085-design-and-implementation-of-fir-filter
- https://www.mathworks.com/help/fixedpoint/examples/implement-fir-filter-algorithm-for-floating-point-and-fixed-point-types-using-cast-and-zeros.html
- https://www.mathworks.com/help/signal/ug/fir-filter-design.html

Specs



- Only coeff. are pre-loaded (using cin, caddr, and cload I/Os)
- Inputs go to the FIFO/synchronizer at 10 kS/s; Inputs are 16b fixed point (FX)
- Output throughput: 10 kS/s; outputs are 16b floating point (FP)
- din comes at clk1 (10 kHz) and the core runs at clk2 (you choose the freq)
- Phases of clk1 and clk2 are not synchronized

Building Blocks

- Dual-clock FIFO and/or synchronizer
- Coefficient memory, CMEM (64 x 2B)
- ALU and FX2FP converter
  - Somewhere, FX16 needs to be converted to FP16
  - Either FX or FP ALU
  - FP16: IEEE754 half-precision binary floating-point format
- Register file
- FSM
- Testbench needs to
  - Provide input at clk1
  - Provide clk1 and clk2
  - The spec for clk1 is 10 kHz; that for clk2 is designer-specified
  - Perform the signature analyzer

Milestones/Reports

- Submit the report for each milestone (LA5 – LA9)
- LA9 is the final report that summarizes all

W	Labs and project	LA
1	NDA & lab setting	
2	NDA & lab setting	
3	LB0: Design flow	
4	LB1: Verilog simulation	LA1
5	LB2: Synthesis	LA2
6	LB3: STA	LA3
7	--	
8	LB4: Memory complier	LA4
9	LB5: Golden block, architecture	LA5
10	LB6: ALU (FP), FX2FP converter	LA6
11	LB7: IMEM, CMEM, Reg	LA7
12	LB8: FIFO/synchronizer	LA8
13	LB9: Core	
14	LB10: Core continue	
15	Finalize	LA9

Milestones/Reports

LA5: Golden block in Matlab; Architect the FIR core;

LA6: Develop **ALU**: RTL coding, logic synthesis, func. test, PPA analysis

LA7: Develop **IMEM & CMEM**: RTL coding, logic synthesis, func. test, PPA analysis; Develop **Register file**: RTL coding, logic synthesis, func. test, PPA analysis

LA8: Develop **FIFO/synchronizer**: RTL coding, logic synthesis, func. test, PPA analysis, metastability analysis (optional)

LA9: Develop **the FIR core**: RTL coding, logic synthesis, func. test, PPA analysis; Iterate till meeting the PPA target; Finalize; document the design details and metric

Metrics to Include

- Methods
  - Input: randomly generated 10k 16-bit real-valued numbers
  - RTL coding from scratch: ***Yes***
  - Throughput: PT with DC-gen. sdf annotation
  - Maximum clock frequency: PT with DC-gen. sdf annotation
  - Energy efficiency: PT with the DC-gen. sdf and QS-gen. vcd annotations
  - Area: DC-gen report
  - Accuracy: RMSE against Matlab results in 32-b floating point numbers. Inputs are 16-bit and generated by the random function of Matlab
- Results
  - Throughput: [kS/s]
  - Maximum clock frequency: [MHz]
  - Energy efficiency: [pJ/S]
  - Area: [mm^2]
  - Accuracy: Worst case: % | Average: %