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Course He

CSEE W4823 Advanced Logic Design
Lab Assignment #3

Using the files that you produced in the Lab Assignments #1 and #2,

1. Generate a SDF file from Design Compiler and re-run the ModelSim simulation with the delay annotation. Do you see any difference? Please elaborate in the report.

2. Modify the PrimeTime script to run the timing analysis. Generate the timing reports for checking the hold & setup time violations. What is the critical path delay of your circuit? What is the shortest path delay?

3. Generate a power report in PrimeTime for the testbench you have created in ModelSim. Please generate and use the VCD file that contains the cycle-accurate switching activities.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab3.zip" through Courseworks. The .zip file should contain the following:

- .tcl file for your PrimeTime script
- Brief report for the above questions. Please include figures to support your report such as the screenshots of PrimeTime timing/power reports.