Columbia University
Department of Electrical Engineering
Department of Computer Science
CSEE W4823 Spring 2018
Mid Exam

Name: _____ **UID**: _____

Problem	Full Credit	Your Points
Total	100	

Note: For full credit, (1) show the pertinent work leading to your answers and (2) avoid unnecessarily long elaboration on answers.

1. (10) Find the minimum-cost SOP and POS forms for the function:

$$f(x_1,x_2,x_3,x_4) = \sum m(0,2,8,9,10,15) + D(1,3,6,7)$$

2. (10) In a ternary number system there are three digits: 0, 1, and 2. Right figure defines a ternary half-adder. Design a logic circuit that implement this half-adder using binary-encoded signals such that two bits are used for each ternary digit. Let A=a_1a_0, B=b_1b_0, and Sum=s_1s_0; note that Carry is just a binary signal. Use the following encoding: 00=$(0)_3$, 01=$(1)_3$, and 10=$(2)_3$. Minimize the cost of the circuit.

A B	Carry	Sum
0 0	0	0
0 1	0	1
0 2	0	2
1 0	0	1
1 1	0	2
1 2	1	0
2 0	0	2
2 1	1	0
2 2	1	1

3. (20) Design a 4-b shift register that shifts 1 bit per clock cycle. Use *latch* and other logic circuits. Derive two different circuit diagrams.

4. (10) Given a 100-MHz clock signal, derive a circuit using D flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.

5. (10) Write a Verilog code that represents a T flip-flop with an asynchronous clear input. Use behavior code, rather than structural code.

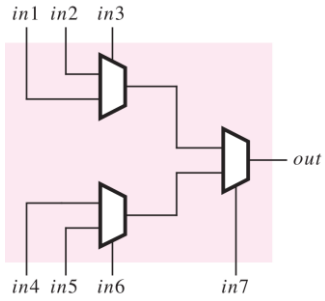
6. (15) Draw the logic circuit diagram represented by the code below. What is its counting sequence?

```
module lfsr (R, L, Clock, Q);
   input [0:2] R;
   input L, Clock;
   output reg [0:2] Q;

   always @(posedge Clock)
      if (L)
         Q < = R;
      else
      begin
         Q[0] = Q[2];
         Q[1] = Q[0];
         Q[2] = Q[1] ^ Q[2];
      end

endmodule
```

7. (10) Transform the following single-precision floating point number into decimal and hexadecimal number.

10100011101010111011101000111011

8. (15) Assume that a gate array contains the type of logic cell depicted in the figure below. The inputs $in_1,\ldots,in_7$ can be connected to either 1 or 0, or to any logic signal.



(a) Show how the logic cell can be used to realize $f=x_1x_2 + x_3$

(b) Show how the logic cell can be used to realize $f=x_1x_3 + x_2x_3$