CSEE 4823 Lab#4

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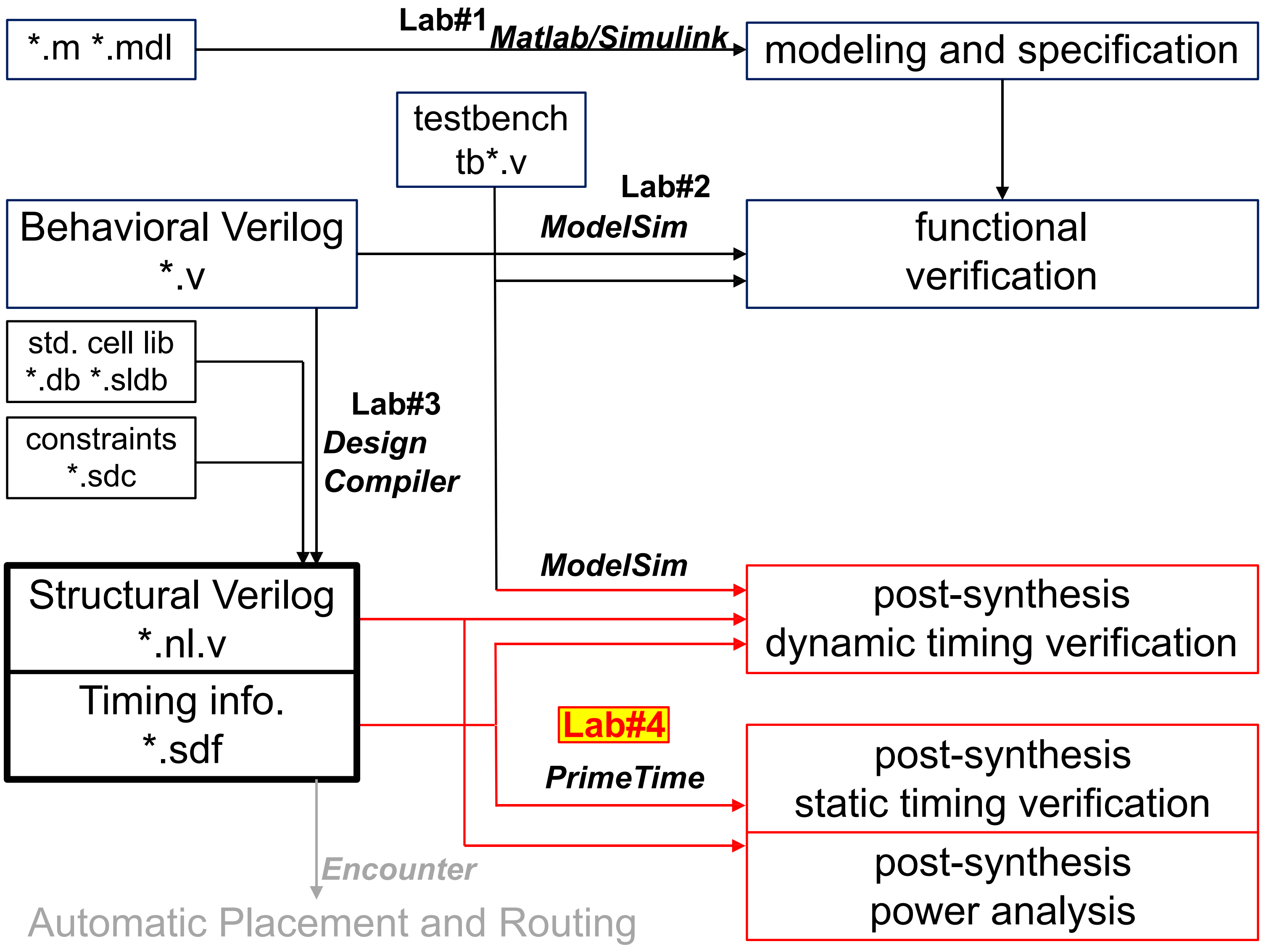
Acknowledgement: Mingoo Seok & Jaebin Choi, Columbia

Topics covered in lab sessions

- Lab#1: Design flow & Matlab®
- Lab#2: Verilog HDL / ModelSim®
- Lab#3: Synthesis / Design Compiler®
- Lab#4: Timing and power analysis / PrimeTime®
- Lab#5: Memory Compiler®

Semi-Custom Flow



After synthesis, what to do next?

- Post-synthesis dynamic timing verification
  - CAD tool: QuestaSim
  - Back-annotation
  - Compare with RTL-level verification, what's the difference?

- Post-synthesis static timing and power verification
  - CAD tool: Primetime
  - What you get:
    - the worst-case delay path
    - power consumption with detailed switching activities
    - setup/hold time violations

1 - ModelSim Simulation with Back Annotation

- copy qsim_dc folder to your local space

  /courses/ee6321/share/4823-fall2020/qsim_dc/

  check your file structure

```
[any, default is your home folder
~]    |____matlab
      |       |________ lfsr1
      |____rtl
      |       |________ lfsr1
      |____dc
      |       |________ lfsr1
      |____qsim_rtl
      |       |________ lfsr1
      |____qsim_dc
      |       |________ lfsr1
      |____pt  ------------> will be created later today
              |________ lfsr1
```

Example: in *.tcl file
../../rtl/$top_level/$top_level.v

You can have your own file structure style, but you need to

(1) know what/where changes should be made in CAD tool scripts
(2) make sure it is compatible with other colleagues’ codes when you are doing a group project!

1 - ModelSim Simulation with Back Annotation

/qsim/lfsr1/runsim.do

```
vlib work
vmap work work

# Include Netlist and Testbench
vlog +acc -incr ../../rtl/lfsr1/lfsr1.v
vlog +acc -incr test_lfsr.v

# Run Simulator
vsim -voptargs=+acc -t ps -lib work testbench
do waveformat.do
run -all
```

RTL code

/qsim_dc/lfsr1/runsim.do

```
#Setup
 vlib work
 vmap work work

#Include Netlist and Testbench
 vlog +acc -incr /courses/ee6321/share/ibm13rflpvt/verilog/ibm13rflpvt.v
 vlog +acc -incr ../../dc/lfsr1/lfsr1.nl.v
 vlog +acc -incr test_lfsr.v

#Run Simulator
#SDF from DC is annotated for the timing check
vsim -voptargs=+acc -t ps -lib work -sdftyp lfsr_0=../../dc/lfsr1/lfsr1.syn.sdf testbench
 do waveformat.do
 run -all
```

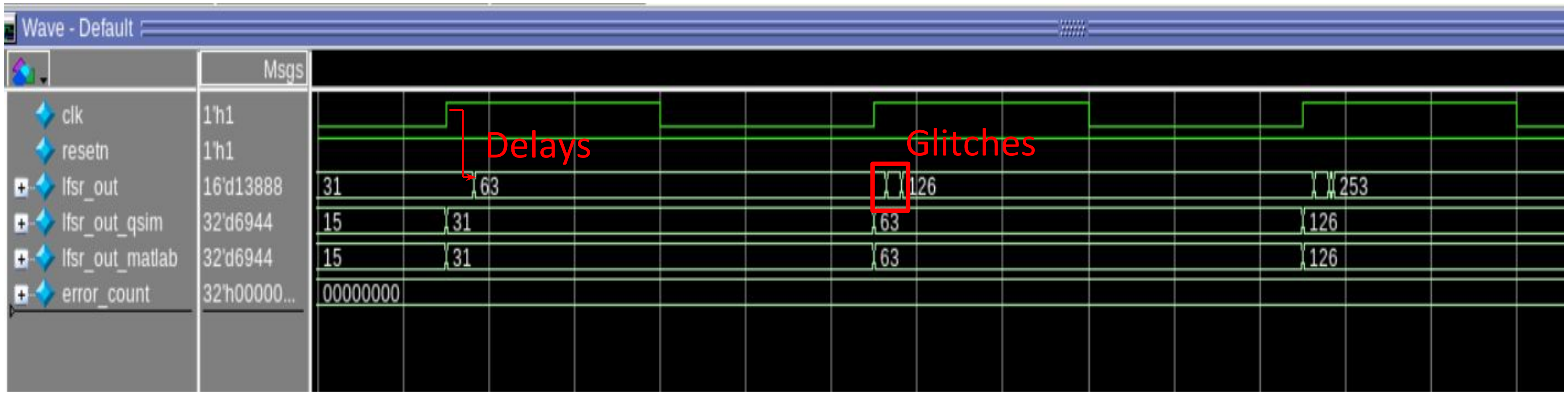
std. cell Verilog library

gate-level netlist

timing *.sdf

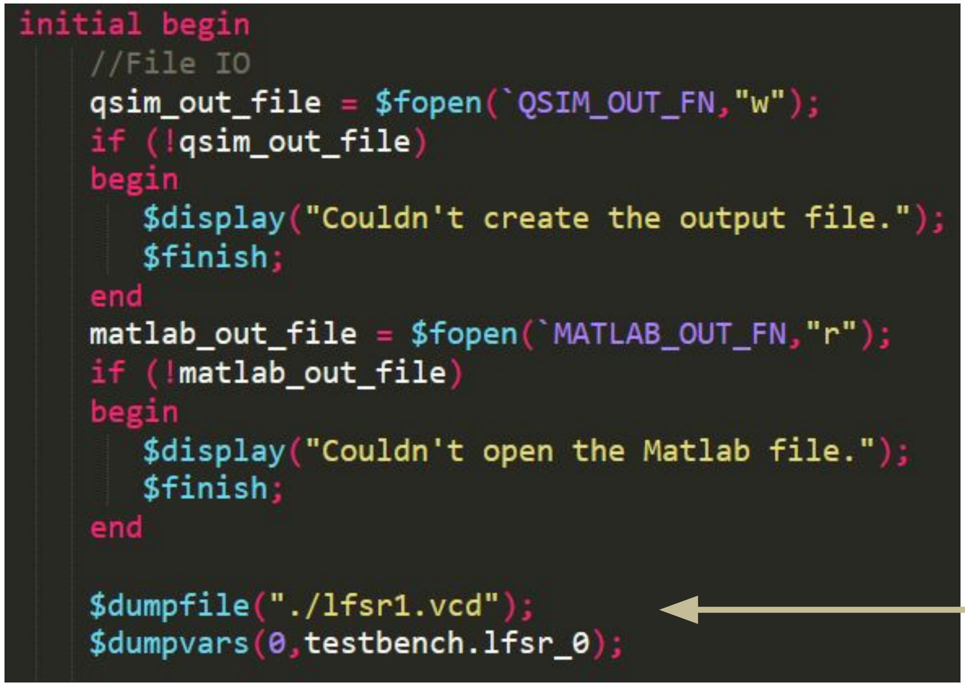
- For simple verification, you can share same testbench file.
- Please run ModelSim and check the waveform.
- See the transcript for any timing violations

What’s New in Waveform

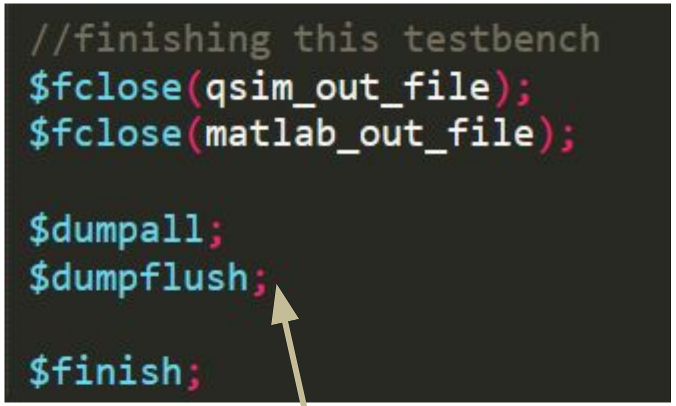


- If you cannot observe delay, try to change time unit to ps

Switching Activity from Modelsim Simulation



```
initial begin
    //File IO
    qsim_out_file = $fopen(`QSIM_OUT_FN,"w");
    if (!qsim_out_file)
    begin
        $display("Couldn't create the output file.");
        $finish;
    end
    matlab_out_file = $fopen(`MATLAB_OUT_FN,"r");
    if (!matlab_out_file)
    begin
        $display("Couldn't open the Matlab file.");
        $finish;
    end

    $dumpfile("./lfsr1.vcd");
    $dumpvars(0,testbench.lfsr_0);
```



```
//finishing this testbench
$fclose(qsim_out_file);
$fclose(matlab_out_file);

$dumpall;
$dumpflush;

$finish;
```

Modify the testbench
Create the vcd file

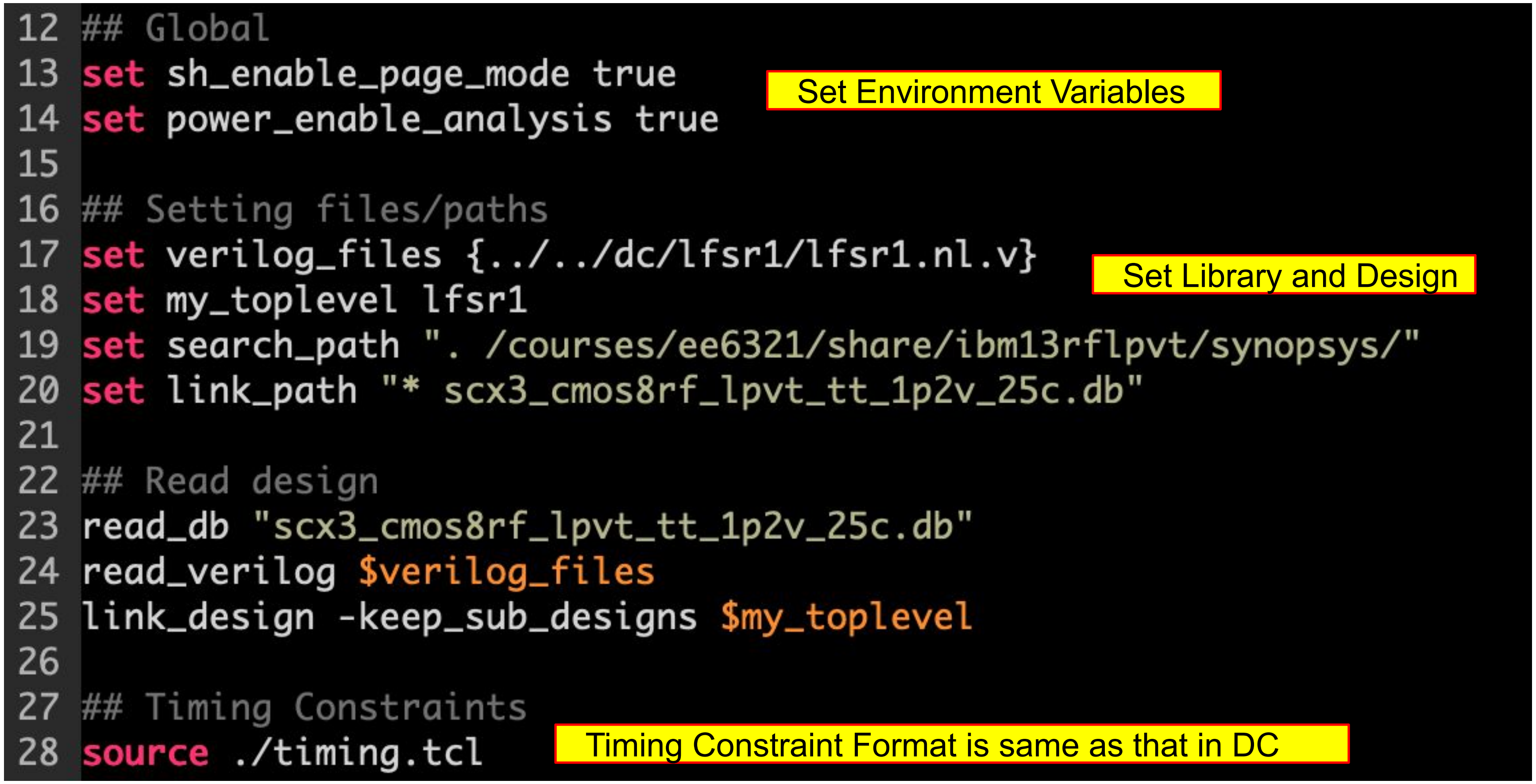
- Look up the usage of $dumpvars command
- .vcd file contains the switching activity for the inputs provided
- .vcd file will be used to obtain an estimate of power using pt
- To obtain realistic estimate of power given proper inputs
- You should find ***lfsr1.vcd*** generated after you run ***run.sh***

2 - Post-synthesis static timing/power verification

- Copy pt (Primetime) folder to your local space

  /courses/ee6321/share/4823-fall2020/pt/
- Main files
  - lfsr1.tcl (CAD tool script)
  - timing.tcl (define timing)
  - run_sta.sh (script to run pt)
  - lfsr1_pt.rpt (report file)
  - lfsr1.log (log file for pt, contains instructions and results)
  - Nuke.sh (delete all files generated by pt, run it before you run pt)
- Go back to compile phase if any violations occurs
- Check power, timing

lfsr1.tcl (1)



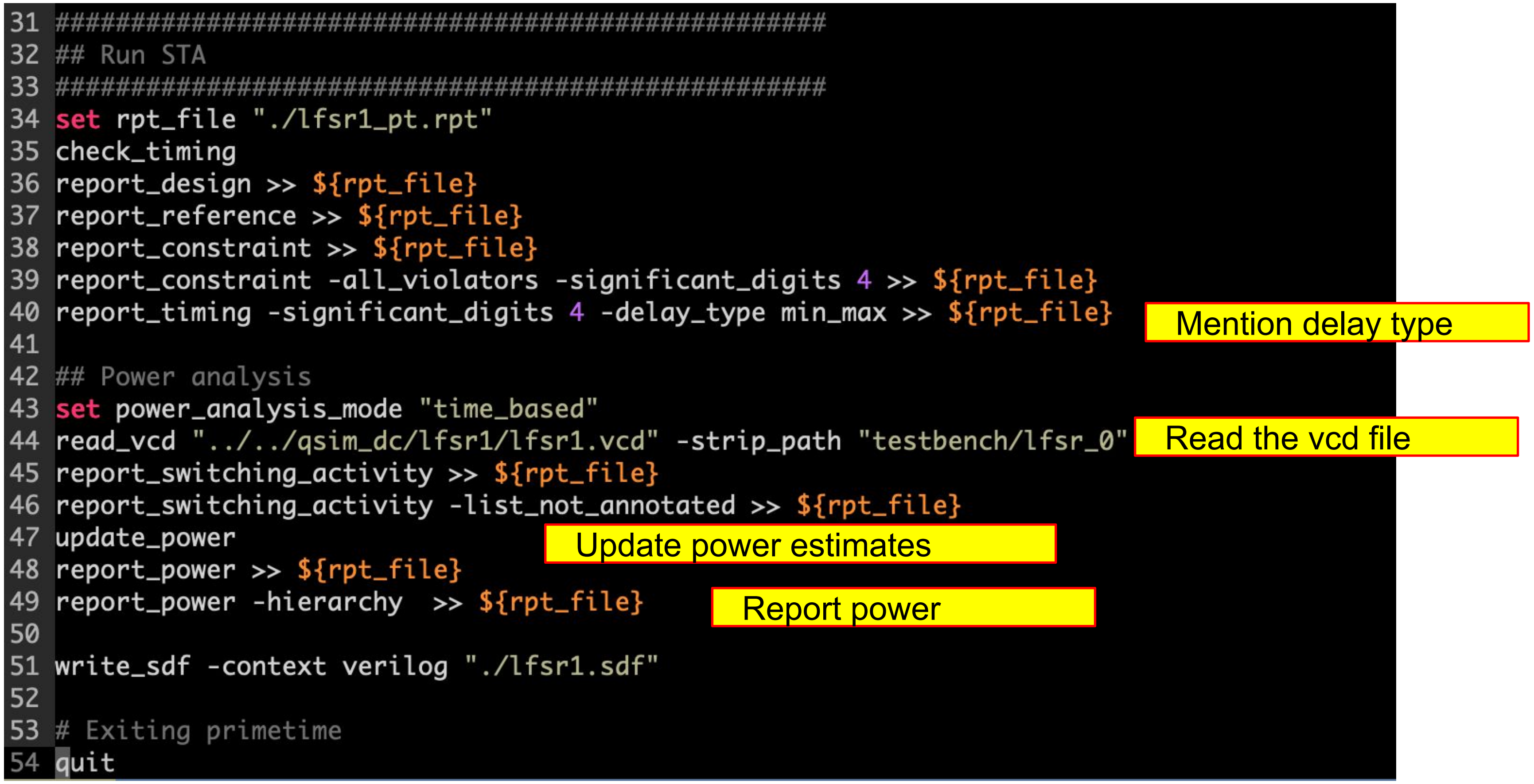
```
## Global
set sh_enable_page_mode true
set power_enable_analysis true

## Setting files/paths
set verilog_files {../../dc/lfsr1/lfsr1.nl.v}
set my_toplevel lfsr1
set search_path ". /courses/ee6321/share/ibm13rflpvt/synopsys/"
set link_path "* scx3_cmos8rf_lpvt_tt_1p2v_25c.db"

## Read design
read_db "scx3_cmos8rf_lpvt_tt_1p2v_25c.db"
read_verilog $verilog_files
link_design -keep_sub_designs $my_toplevel

## Timing Constraints
source ./timing.tcl
```

Set Environment Variables
Set Library and Design
Timing Constraint Format is same as that in DC

.db File in Post-synthesis Verification

- The .db file is compiled version of .lib file
- Look at .lib file to get a sense of the kind of information present in .db file
- /courses/ee6321/share/ibm13rflpvt/synopsys/scx3_cmos8rf_lpvt_tt_1p2v_25c.lib
- Contains :
  - Units that will be used by the tool for time, voltage, etc.
  - The operating conditions
  - Models for timing and power of the standard cells
- The unit for area is um^2 for the technology libraries we are using

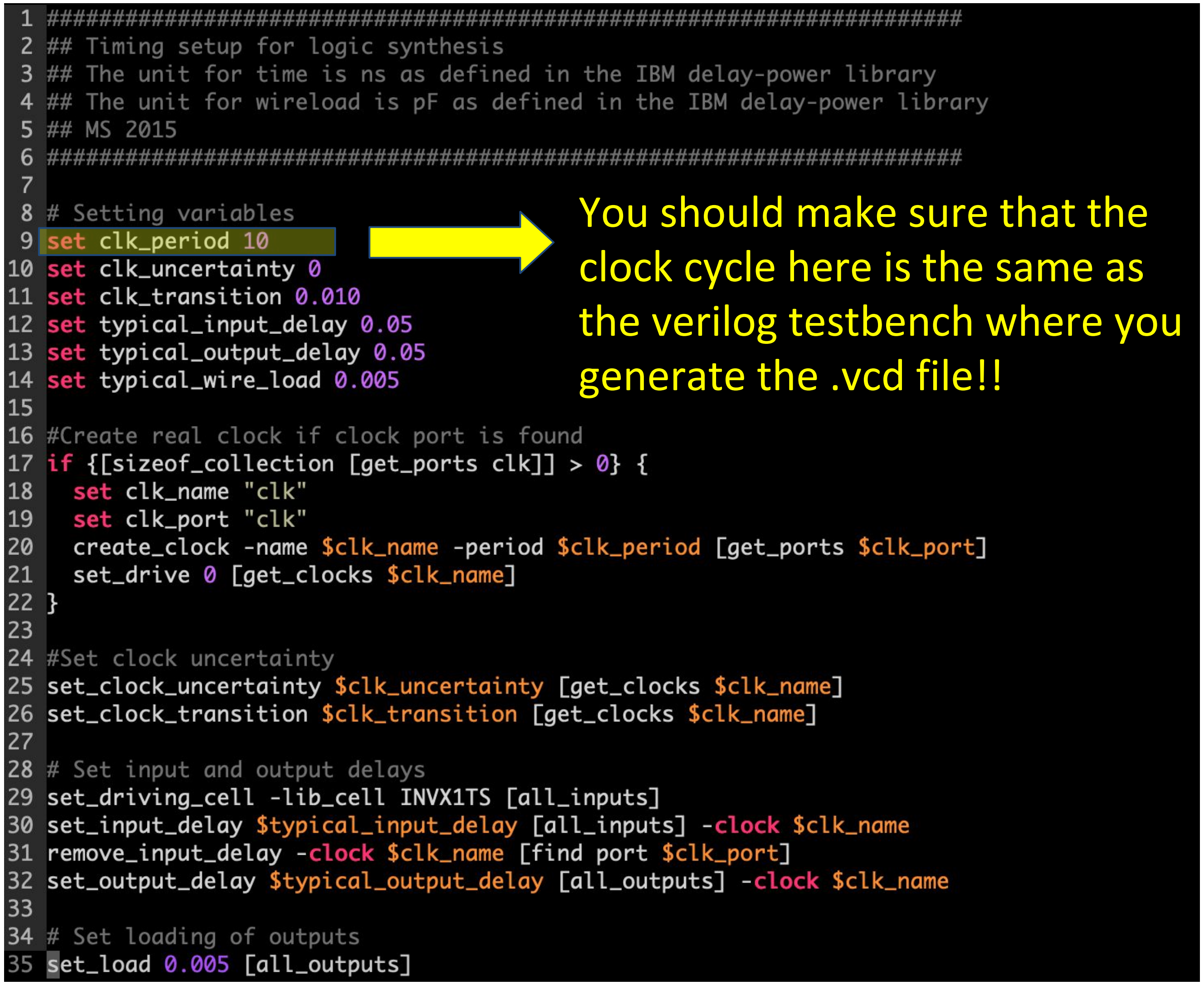
lfsr1.tcl (2)



```
###################################################
## Run STA
###################################################
set rpt_file "./lfsr1_pt.rpt"
check_timing
report_design >> ${rpt_file}
report_reference >> ${rpt_file}
report_constraint >> ${rpt_file}
report_constraint -all_violators -significant_digits 4 >> ${rpt_file}
report_timing -significant_digits 4 -delay_type min_max >> ${rpt_file}

## Power analysis
set power_analysis_mode "time_based"
read_vcd "../../qsim_dc/lfsr1/lfsr1.vcd" -strip_path "testbench/lfsr_0"
report_switching_activity >> ${rpt_file}
report_switching_activity -list_not_annotated >> ${rpt_file}
update_power
report_power >> ${rpt_file}
report_power -hierarchy  >> ${rpt_file}

write_sdf -context verilog "./lfsr1.sdf"

# Exiting primetime
quit
```

- Use man command in pt_shell to understand usage of commands
- Or type “primetime” in command line to open up the tool’s gui, then look at help

timing.tcl



```
######################################################################
## Timing setup for logic synthesis
## The unit for time is ns as defined in the IBM delay-power library
## The unit for wireload is pF as defined in the IBM delay-power library
## MS 2015
######################################################################

# Setting variables
set clk_period 10
set clk_uncertainty 0
set clk_transition 0.010
set typical_input_delay 0.05
set typical_output_delay 0.05
set typical_wire_load 0.005

#Create real clock if clock port is found
if {[sizeof_collection [get_ports clk]] > 0} {
  set clk_name "clk"
  set clk_port "clk"
  create_clock -name $clk_name -period $clk_period [get_ports $clk_port]
  set_drive 0 [get_clocks $clk_name]
}

#Set clock uncertainty
set_clock_uncertainty $clk_uncertainty [get_clocks $clk_name]
set_clock_transition $clk_transition [get_clocks $clk_name]

# Set input and output delays
set_driving_cell -lib_cell INVX1TS [all_inputs]
set_input_delay $typical_input_delay [all_inputs] -clock $clk_name
remove_input_delay -clock $clk_name [find port $clk_port]
set_output_delay $typical_output_delay [all_outputs] -clock $clk_name

# Set loading of outputs
set_load 0.005 [all_outputs]
```

You should make sure that the clock cycle here is the same as the verilog testbench where you generate the .vcd file!!

Report File: lfsr1_pt.rpt (1)

Min path

```
****************************************
Report : timing
        -path_type full
        -delay_type min_max
        -max_paths 1
        -sort_by slack
Design : lfsr1
Version: P-2019.03-SP2
Date   : Thu Oct 15 21:40:06 2020
****************************************


  Startpoint: lfsr_out_reg_0_
               (rising edge-triggered flip-flop clocked by clk)
  Endpoint: lfsr_out[0]
               (output port clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                                    Incr       Path
  
---------------------------------------------------------------------------
--
  clock clk (rise edge)                                  0.0000     0.0000
  clock network delay (ideal)                            0.0000     0.0000
  lfsr_out_reg_0_/CK (DFFHQX4TS)                         0.0000     0.0000 r
  lfsr_out_reg_0_/Q (DFFHQX4TS)                          0.2738     0.2738 r
  lfsr_out[0] (out)                                      0.0000     0.2738 r
  data arrival time                                                 0.2738

  clock clk (rise edge)                                  0.0000     0.0000
  clock network delay (ideal)                            0.0000     0.0000
  clock reconvergence pessimism                          0.0000     0.0000
  output external delay                                 -0.0500    -0.0500
  data required time                                               -0.0500

---------------------------------------------------------------------------
--
  data required time                                               -0.0500
  data arrival time                                                -0.2738

---------------------------------------------------------------------------
--
  slack (MET)                                                       0.3238
```

Report File: lfsr1_pt.rpt (2)

Max path

```
Startpoint: lfsr_out_reg_5_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: lfsr_out_reg_0_
            (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                 0.0000     0.0000
clock network delay (ideal)                           0.0000     0.0000
lfsr_out_reg_5_/CK (DFFQX1TS)                         0.0000     0.0000 r
lfsr_out_reg_5_/Q (DFFQX1TS)                          0.7417     0.7417 f
U50/Y (XOR2X1TS)                                      0.2572     0.9988 r
U51/Y (XOR2X1TS)                                      0.2823     1.2811 f
U52/Y (AO22X1TS)                                      0.4487     1.7298 f
lfsr_out_reg_0_/D (DFFHQX4TS)                         0.0000     1.7298 f
data arrival time                                                1.7298

clock clk (rise edge)                                10.0000    10.0000
clock network delay (ideal)                           0.0000    10.0000
clock reconvergence pessimism                         0.0000    10.0000
lfsr_out_reg_0_/CK (DFFHQX4TS)                                  10.0000 r
library setup time                                   -0.2619     9.7381
data required time                                               9.7381
-----------------------------------------------------------------------------
data required time                                               9.7381
data arrival time                                               -1.7298
-----------------------------------------------------------------------------
slack (MET)                                                      8.0083
```

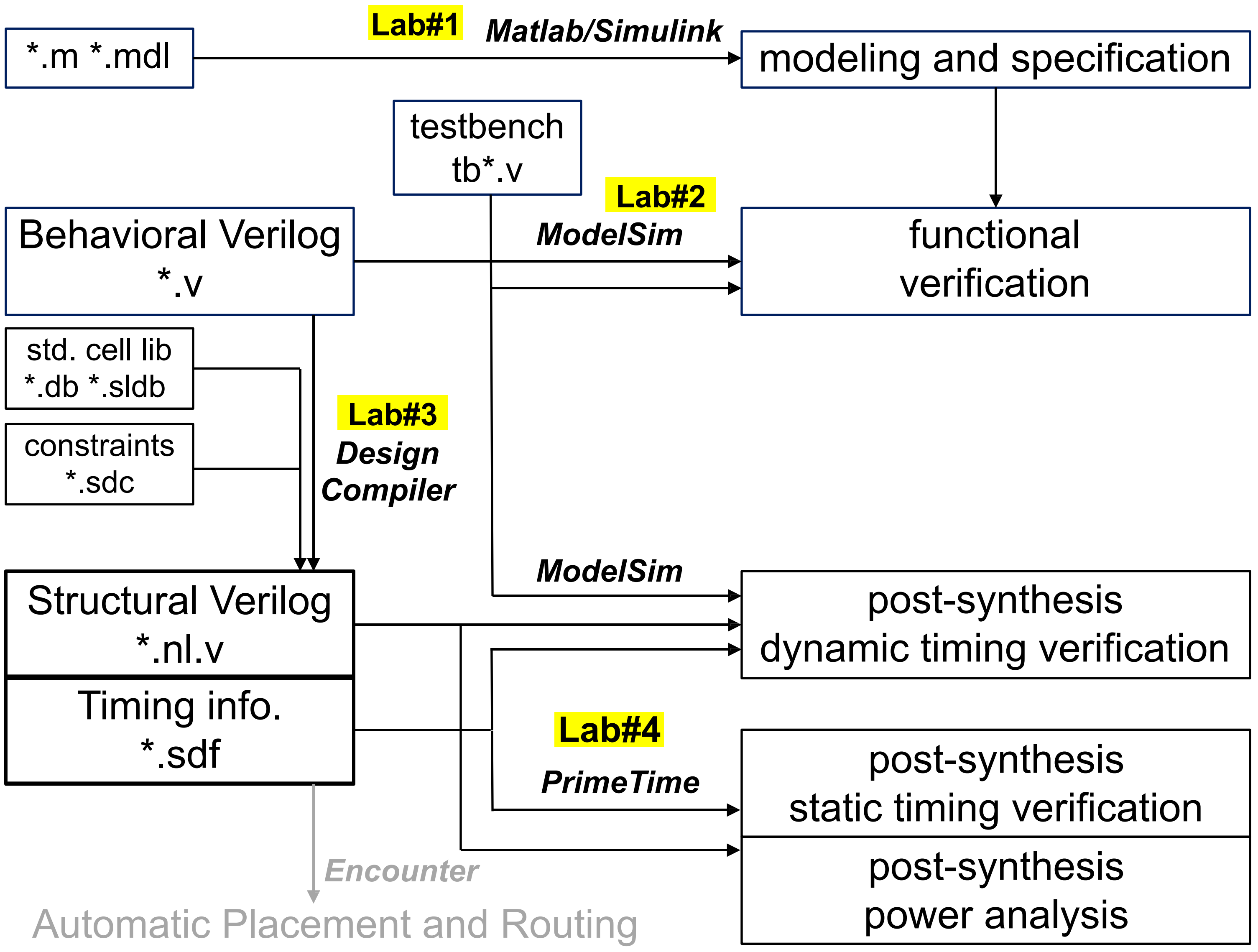
Report File: lfsr1_pt.rpt (3)

Power

```
****************************************
Report : Time Based Power
Design : lfsr1
Version: P-2019.03-SP2
Date   : Thu Oct 15 21:40:06 2020
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           3.973e-05    0.0000    0.0000 3.973e-05 (63.16%)  i
register                1.323e-05 3.830e-06 5.856e-10 1.706e-05 (27.12%)
combinational           5.048e-06 1.068e-06 2.489e-10 6.117e-06 ( 9.72%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 4.898e-06   ( 7.79%)
  Cell Internal Power  = 5.801e-05   (92.21%)
  Cell Leakage Power   = 8.345e-10   ( 0.00%)
                         ---------
Total Power            = 6.290e-05  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 4.143e-03
Peak Time              =   865.000
```

- Internal power : Power consumed to switch parasitic caps (major portion) + short-circuit power (typically very small)
- Switching power : Power used for switching gate cap

Summary of 4 lab sessions



Lab#1
Matlab/Simulink
*.m *.mdl
modeling and specification
testbench tb*.v
Lab#2
ModelSim
Behavioral Verilog *.v
functional verification
std. cell lib *.db *.sldb
constraints *.sdc
Lab#3
Design Compiler
ModelSim
Structural Verilog *.nl.v
Timing info. *.sdf
post-synthesis dynamic timing verification
Lab#4
PrimeTime
post-synthesis static timing verification
post-synthesis power analysis
Encounter
Automatic Placement and Routing