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Course Hero

**CSEE W4823 Advanced Logic Design**
**Lab Assignment #6**

1. Write the RTL code in Verilog (.v) for the ALU block(s) in your FIR core. Write the testbench to verify its functionalities with randomly-generated fixed-point inputs

2. Synthesize the above RTL to get the gate-level netlist (nl.v) of the ALU. Verify the functionality by using the testbench.

3. Perform timing and power analysis using PrimeTime. Include the VCD files for accurate power estimation.

**Deliverables:**

Please create and submit a .zip file with the name "your_uni_lab6.zip" through Courseworks. The .zip file should contain the following:

- Report for the above tasks. Please include the figures and plots to support.
- .v files for your RTL code and ModelSim testbench.
- .nl.v files from the logic synthesis
- .tcl file for the logic synthesis
- .tcl file for your PrimeTime script
- .vcd file from QuestaSim