
DO NOT SHARE
SLIDES AND CLASS MATERIALS
ON ONLINE SITES
Course He

CSEE W4823 Advanced Logic Design
Homework Assignment #4

1. For a CMOS inverter, assume that the load capacitance is C = 150 fF and VDD = 5 V. The inverter is cycled through the low and high voltage levels at an average rate of f = 75 MHz

(a) Calculate the dynamic power dissipated in the inverter

(b) For a chip that contains the equivalents of 250,000 inverters, calculate the total dynamic power dissipated if 20 percent of the gates change values at any given time

2. How many errors can be detected by a code with minimum distance *d*?

3. What is the minimum number of parity bits required to obtain a distance-4, two-dimentional code with n information bits?

4. Show how to construct a distance-6 code with four information bits. Write a list of its code words