CSEE W4823 Advanced Logic Design
Lab Assignment #8

1. Write the RTL code in Verilog (.v) for the dual-clock FIFO. clk1 is the input sampling clock. Its frequency is 10 kHz, matching to the input and output rate (10 kS/s). clk2 is the core clock. Set the frequencies of the clk2 accordingly. Assume the phase difference between two clocks is fixed (static, not changing over time). You can set the phase difference arbitrarily.

2. Synthesize the above RTL to get the gate-level netlist (nl.v). Verify the functionality by using the testbench.

3. Perform timing and power analysis using PrimeTime. Include the VCD files for accurate power estimation.

Deliverables:

Please create and submit a .zip file with the name "your_uni_lab_number.zip" through Courseworks. The .zip file should contain the following:

- Report for the above tasks. Please include supporting figures.
- .v files for your RTL code and ModelSim testbench.
- .nl.v files from the logic synthesis
- .tcl file for the logic synthesis
- .tcl file for your PrimeTime script
- .vcd file from QuestaSim