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Course Hero

Advanced Logic Design
Lecture 3: Sequential Circuits

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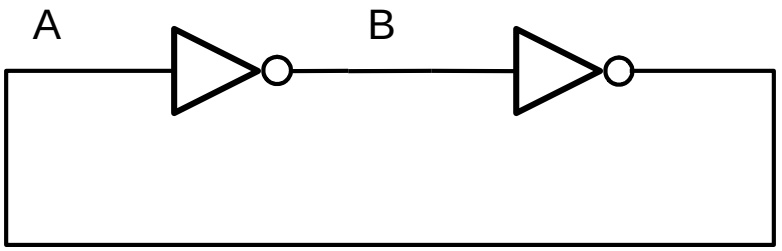
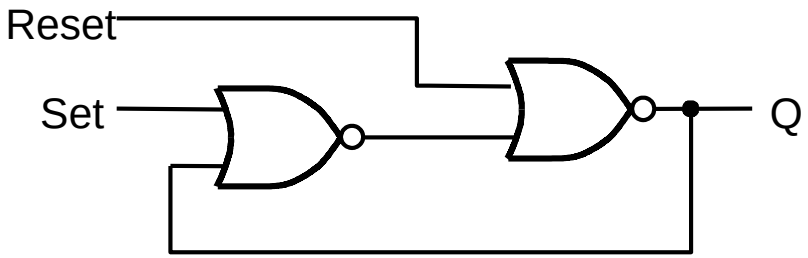
BV: Secs. 5.1, 5.4, 5.8-5.10, 5.15, 7.8

Sequential Circuit Definition

- **Combinational circuit:** the output depends solely on the input of logic circuits (Lecture 2)
- **Sequential circuit:** the output depends on both the input and the *past state* of the circuit
- Past state = memory
- The circuit changes through a *sequence* of states as a result of changes in the inputs → ***sequential circuits***
- Sequence is also related to the order of operations and sometimes includes the notion of ***pipelining***

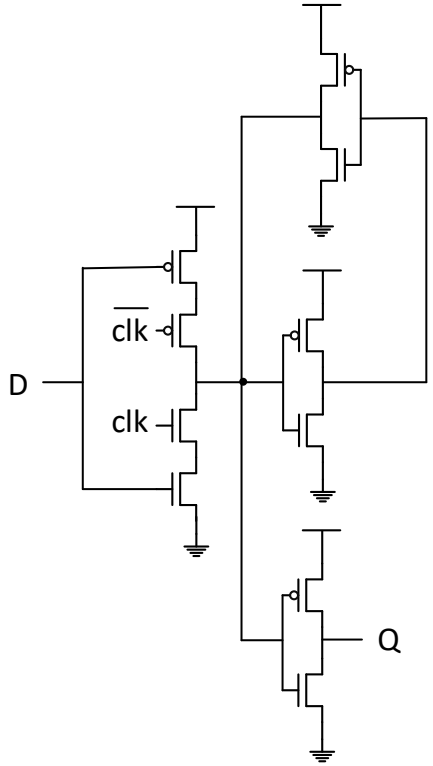
Rudimentary Memory Element





- Back-to-back inverters (= cross-coupled inverters) can store binary (1 or 0) information
- It needs additional circuits to read and write data

D Latch

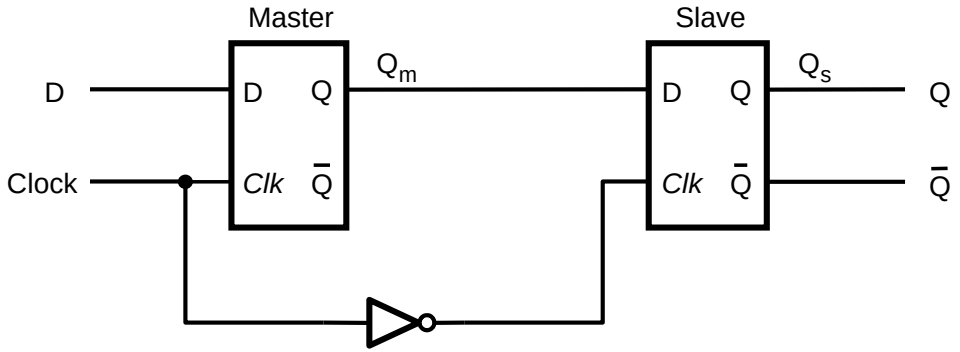


- Transparent-high latch
  - Latch is sensitive to the *level* of clk signal
- Fig. 5.7 in the BV book is not the most popular form

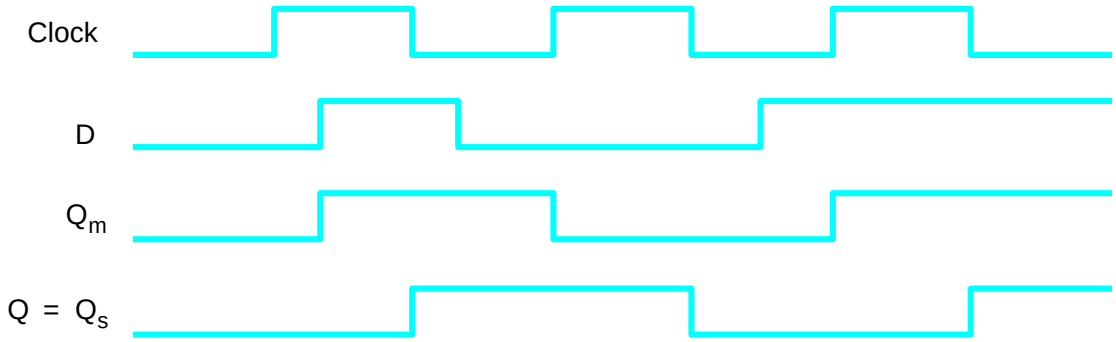
Setup and Hold Time

- Defined w/r/t the *falling* edge of Clk for the transparent-*high* latch

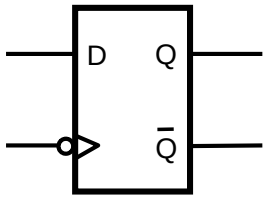
Master-Slave Flip-Flop



(a) Circuit

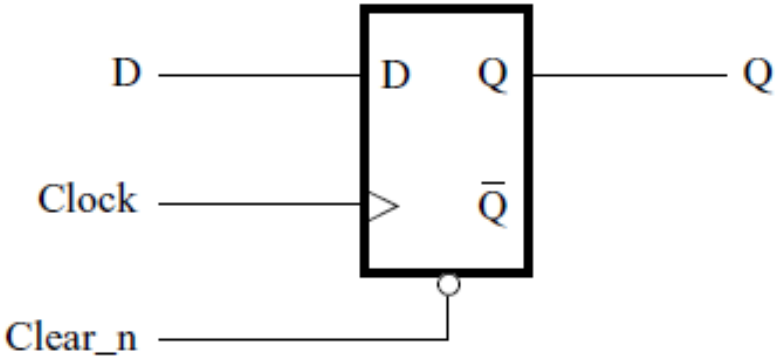


(b) Timing diagram

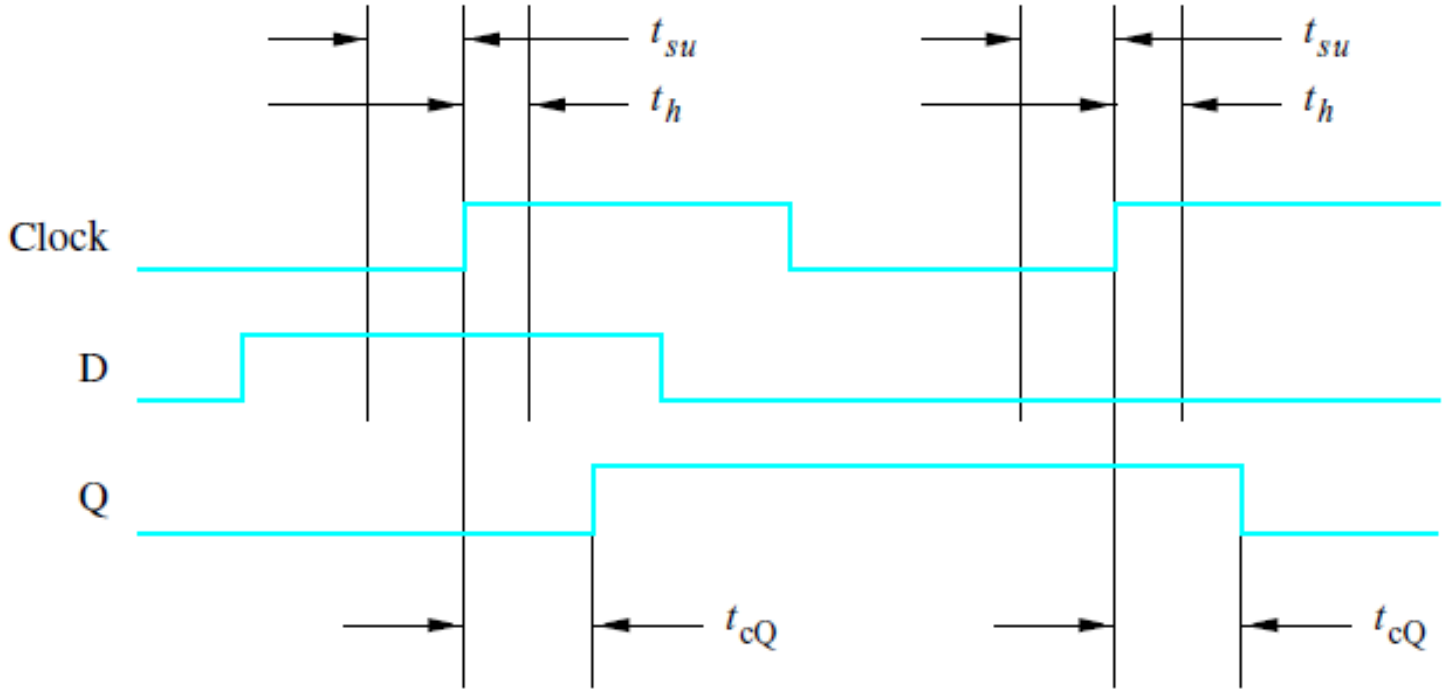


(c) Graphical symbol

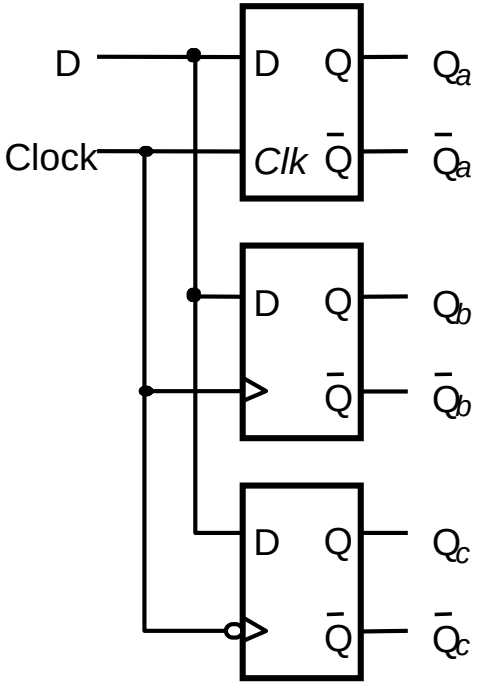
- Sensitive to the edge, rather than the level, of clock signal
- Robust
- Where is t_s and t_h?



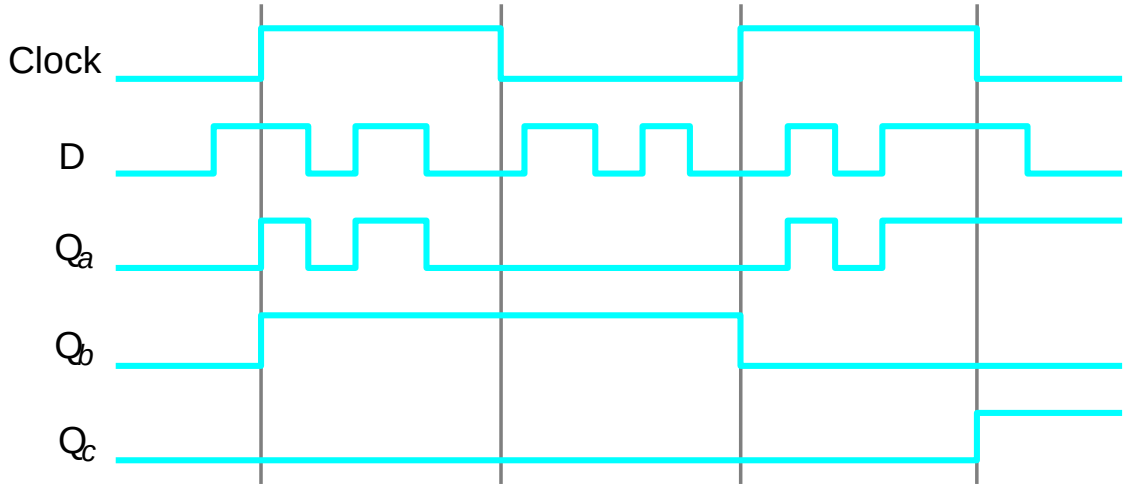
(a) D flip-flop with asynchronous clear



(b) Timing diagram

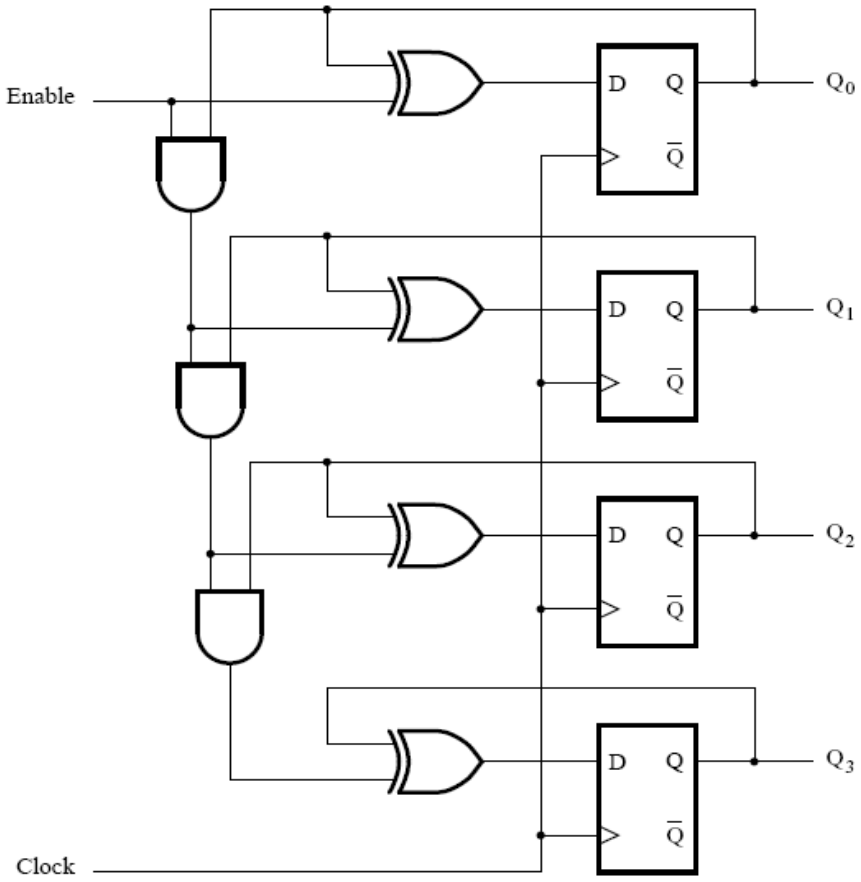


(a) Circuit



(b) Timing diagram

Setup & Hold Constraints

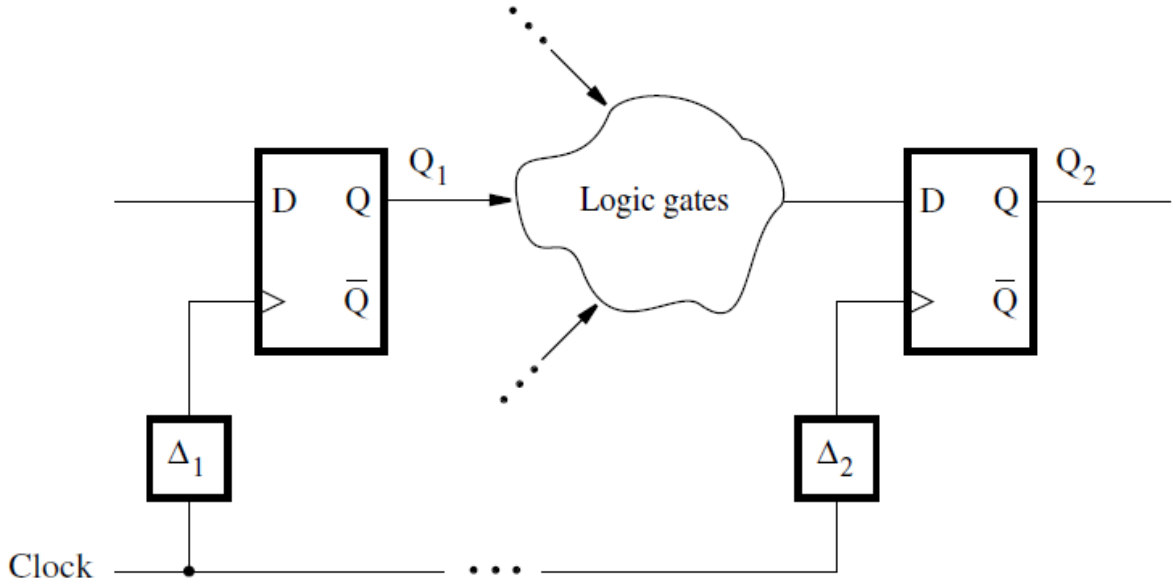


- Critical path
- Short path
- Setup violation
- Hold violation

$T_{min} = t_{cq} + 3 \cdot t_{AND} + t_{XOR} + t_{setup}$

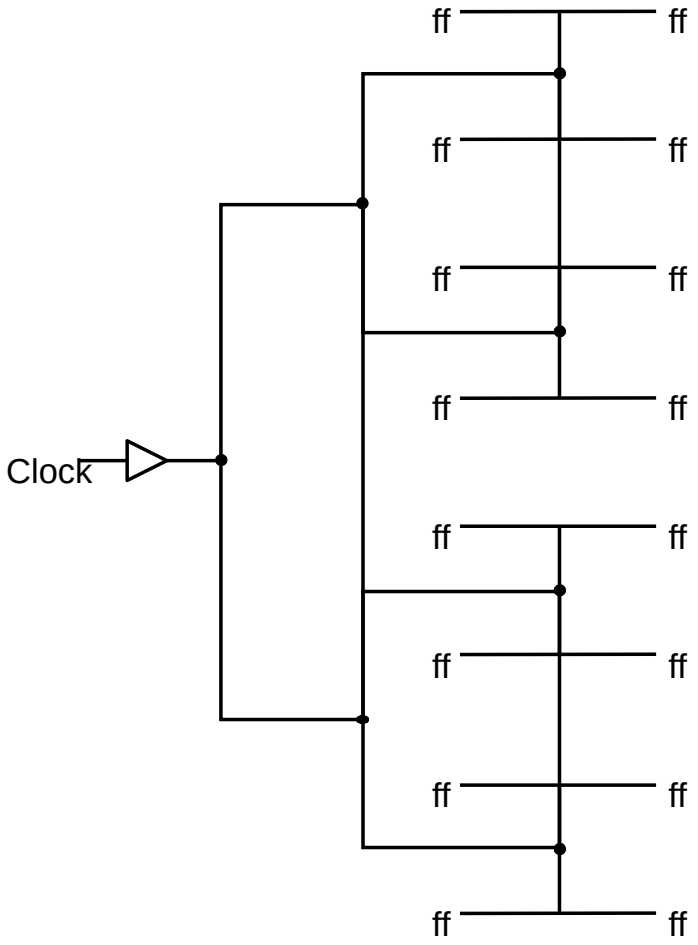
$t_{cq} + t_{XOR} > t_{hold}$

Clock Skew



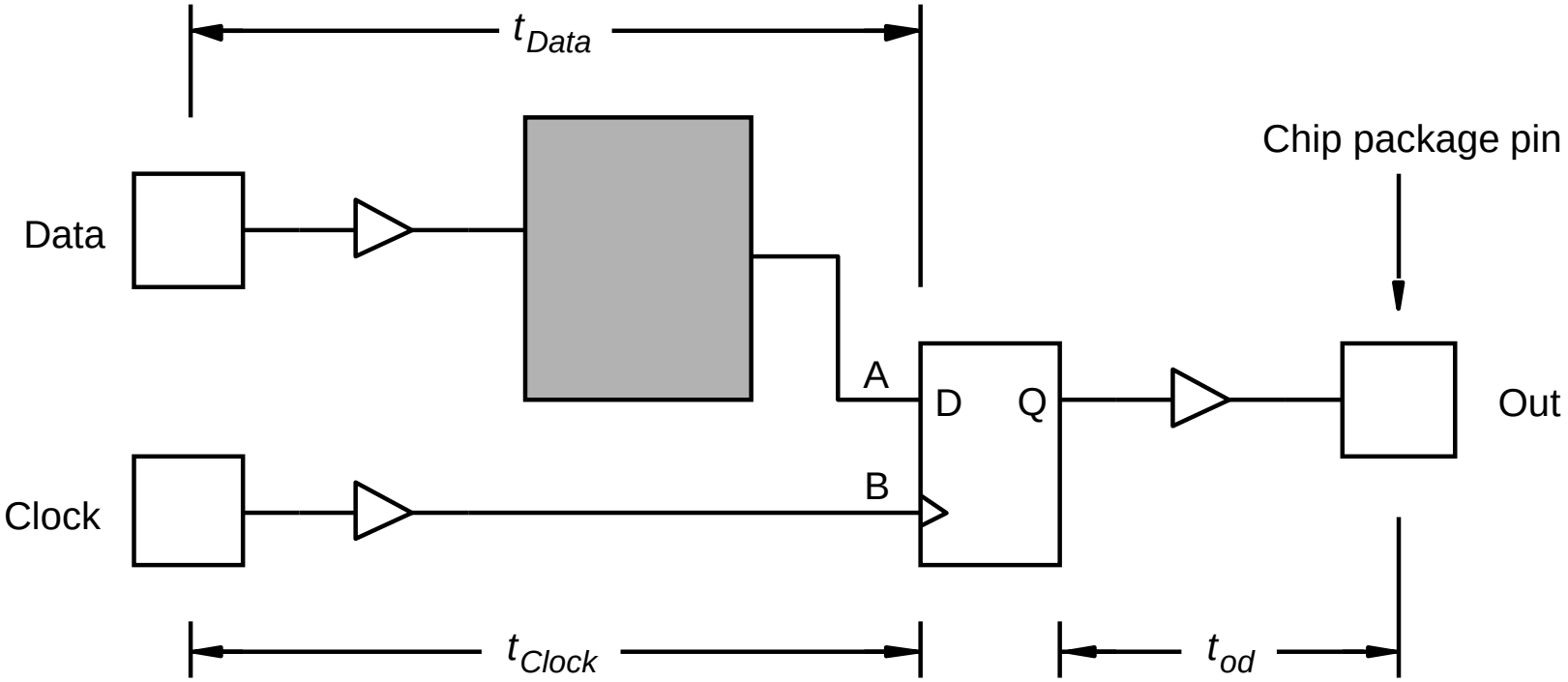
- Pos. clock skew ($d_2 > d_1$): relax setup, worsen hold
- Neg. clock skew ($d_2 < d_1$): worsen setup, relax hold

Clock Tree

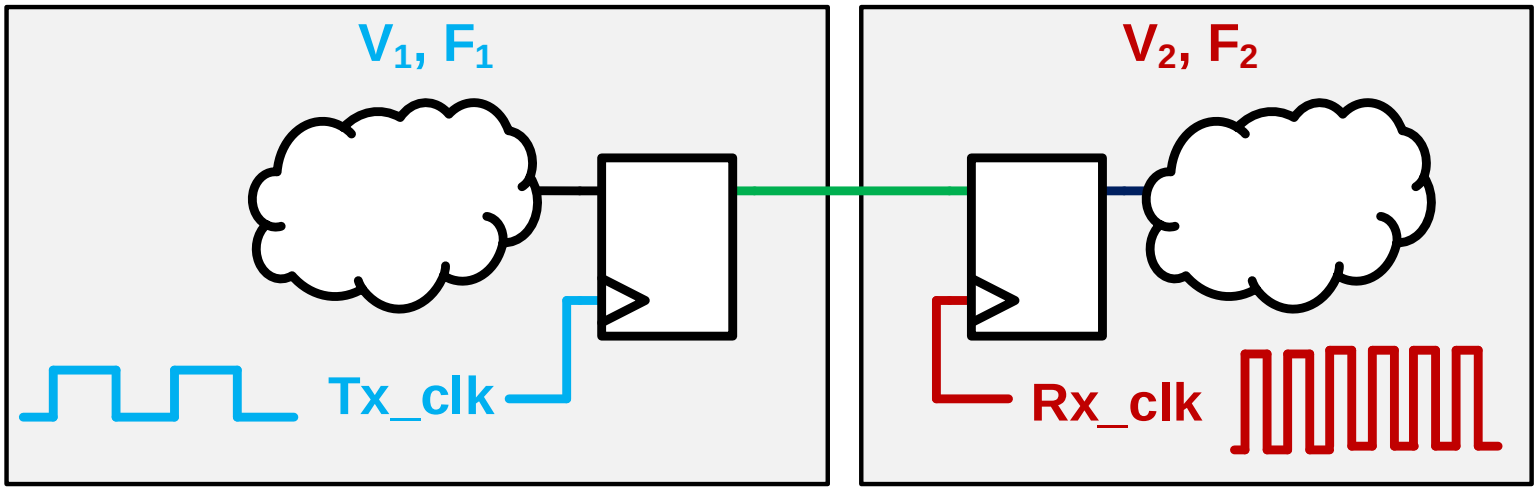


- Important to minimize clock skew
- Balance (not shorten) clock signal delay from the *source* to each *sink* via a H-shape tree
- However, often you need to shorten the delay. Why?

Output and Input Delay



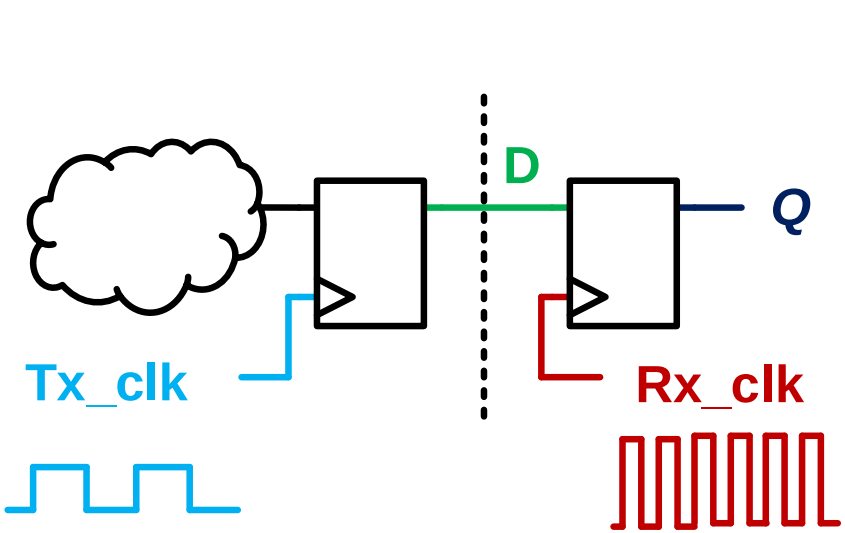
Clock Domain Crossing (CDC)

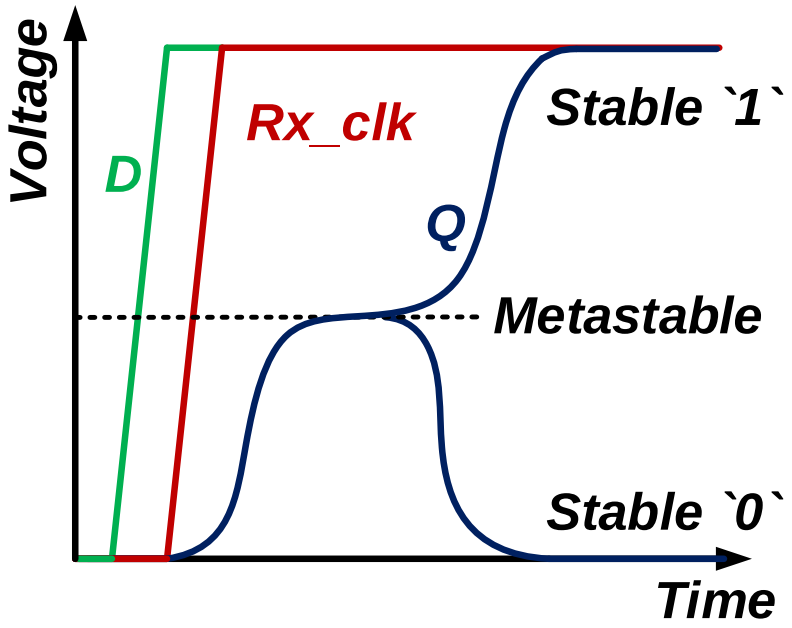


- Data exchange between two clock domains
- TX and RX clocks may have unknown and time-varying phase and frequency relationships

[C. Lin, ISSCC'20]

Metastability in Clock Domain Crossing

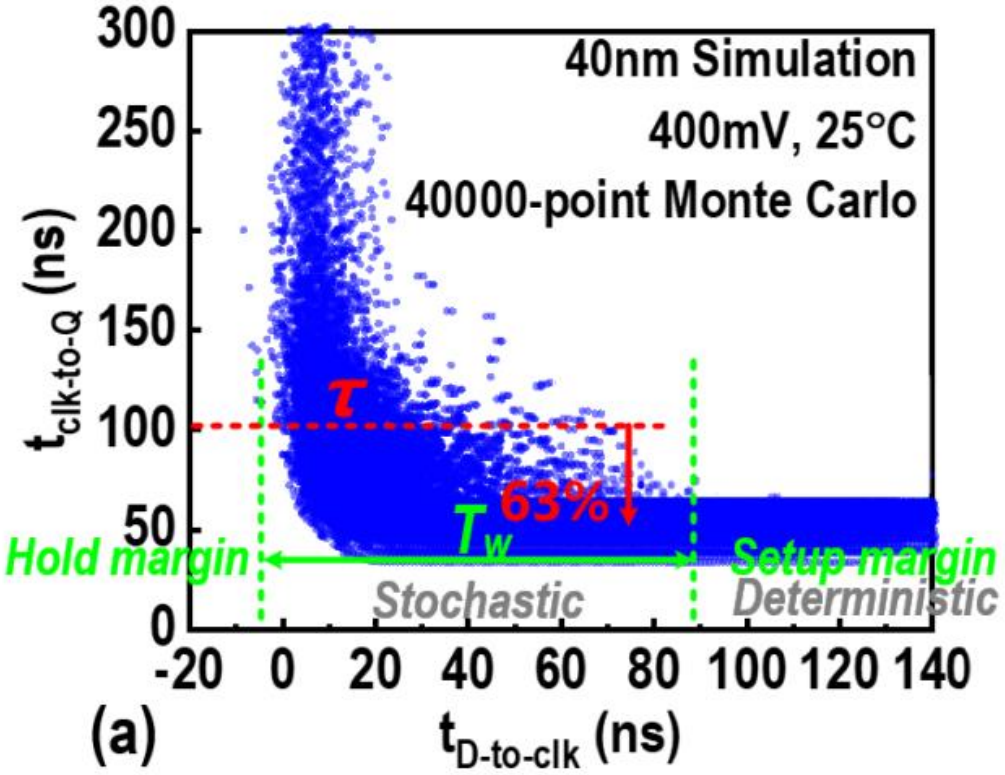




- If D arrives too close to the RX clock edge, it will cause metastability

[C. Lin, ISSCC'20]

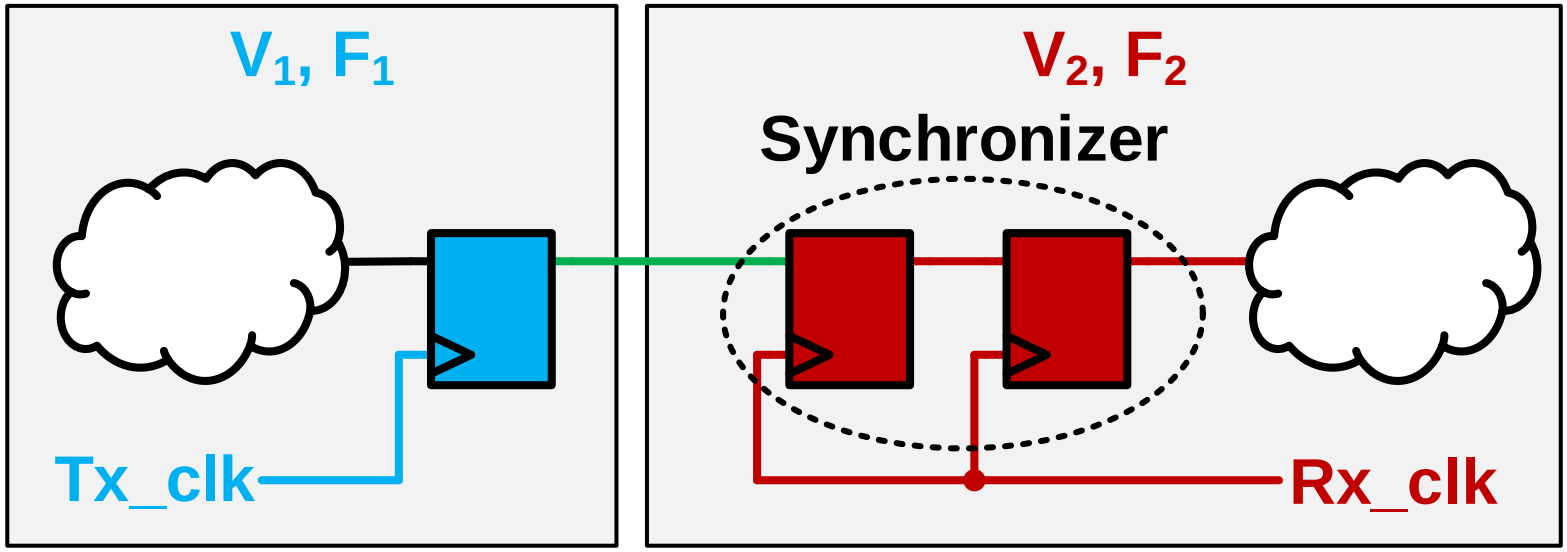
Metastability in Clock Domain Crossing



- The metastability in the RX flip-flop results in longer clk-to-q delay

[C. Lin, JSSC'23]

Synchronizer



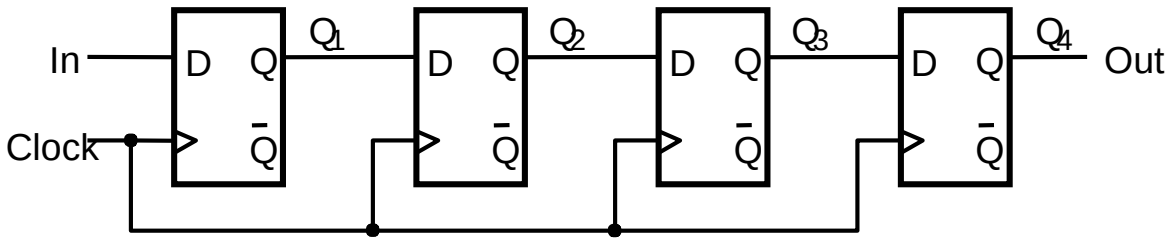
- Synchronizers are used to reduce the probability of metastability
- Give one extra cycle for the first flop to resolve the metastability
- Latency varies by one cycle
- Used to the req and ack signals
- However, it cannot guarantee to eliminate metastability
- It cannot provide long-term mitigation, i.e., D can still arrive close to Rx_clk edge at any moment

[C. Lin, ISSCC'20]

Register

- One flip-flop (or one latch) stores 1 bits
- Multiple flip-flops storing n bits are called ***a register***
- Register is a microarchitecture term
- Flip-flops and latches are an circuit term

Shift Register



(a) Circuit

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

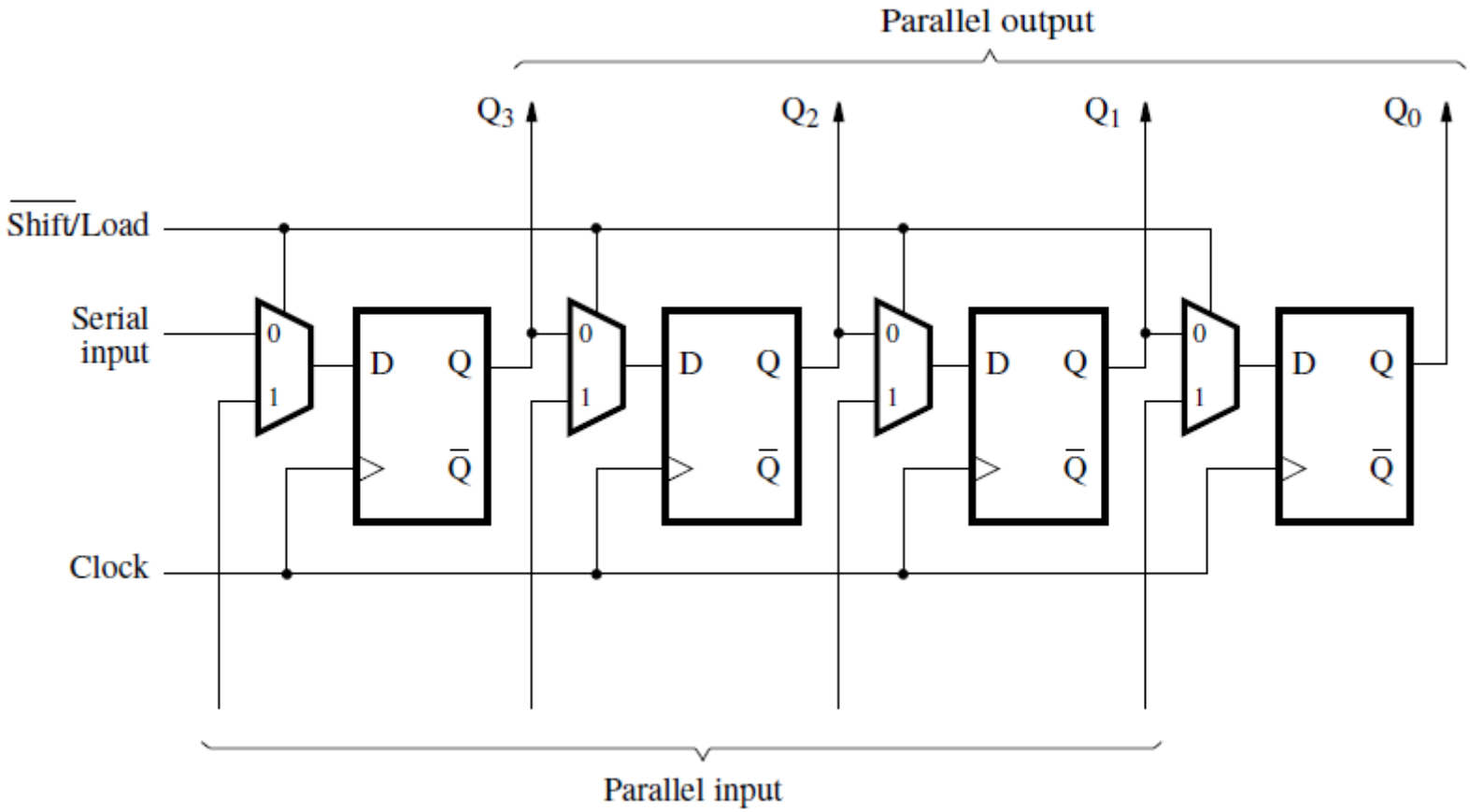
(b) A sample sequence

- A register that provides the ability to shift its contents is called shift register
- ← 4-bit shift register
- Can we make one using ***latches***?

Latch Shift Register

- Single-clock? Hold time?
- Two phase clock?

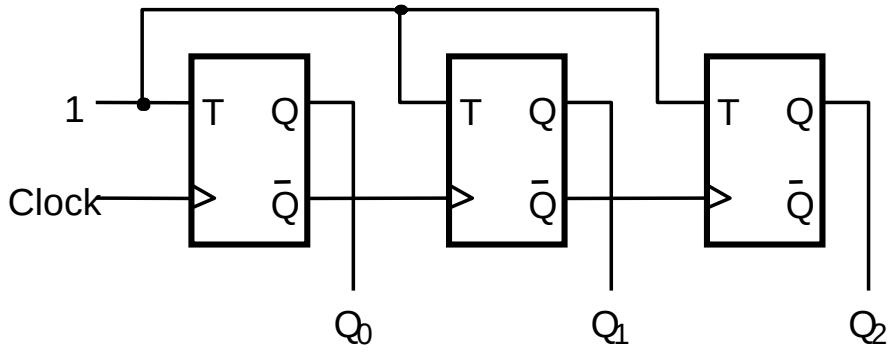
Parallel-Access Shift Register



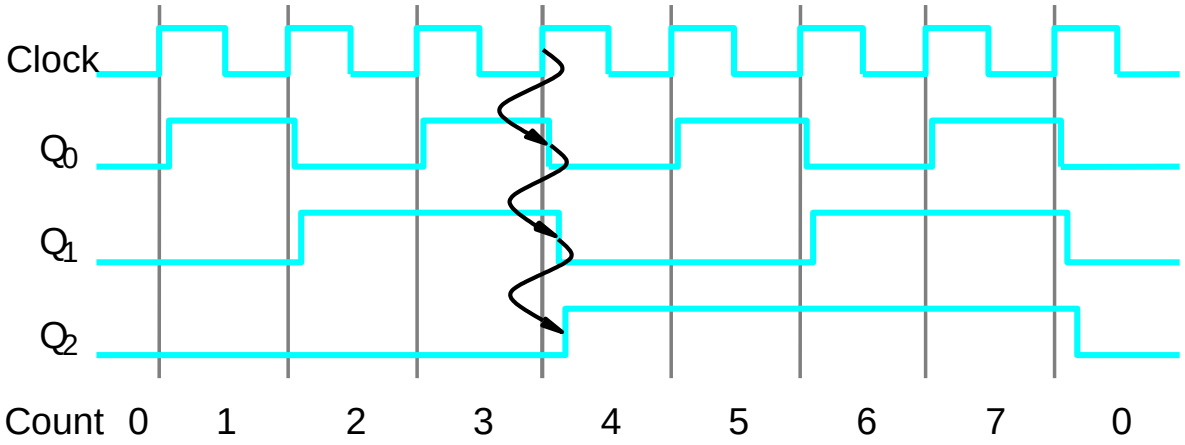
Toggle Flip-Flop

- Can be made out of the edge-triggered D flip-flop w/ some logic gate

Asynchronous Counter

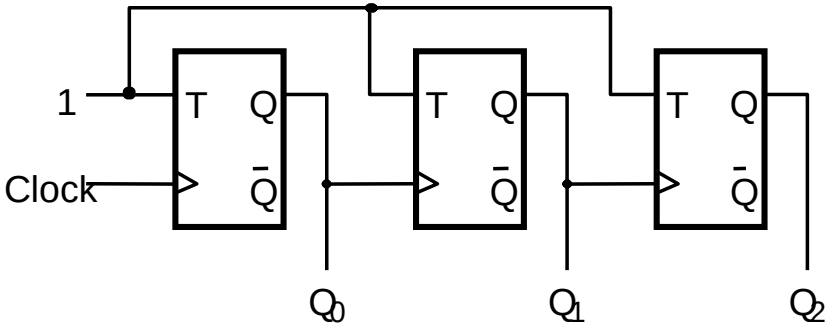


(a) Circuit

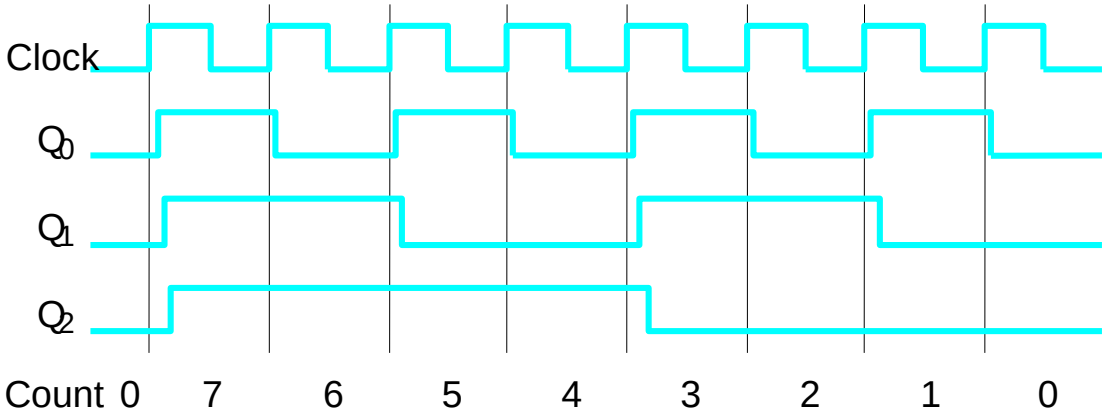


(b) Timing diagram

Another Asynchronous Counter

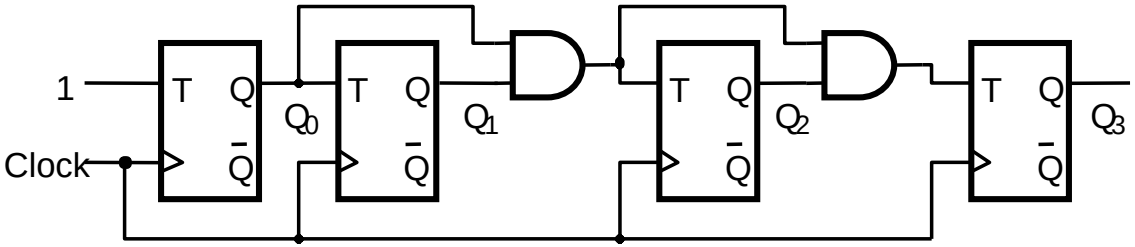


(a) Circuit

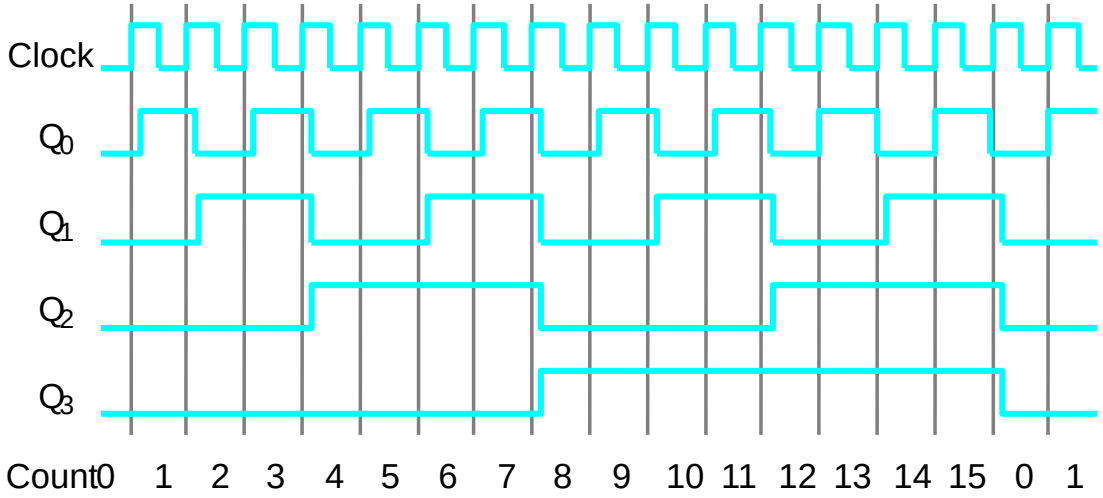


(b) Timing diagram

Synchronous Counter – Better?



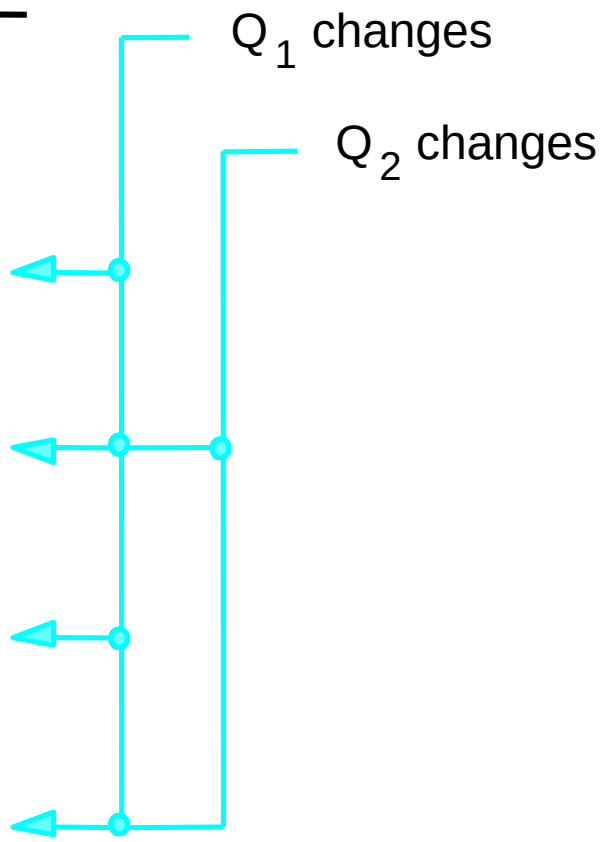
(a) Circuit



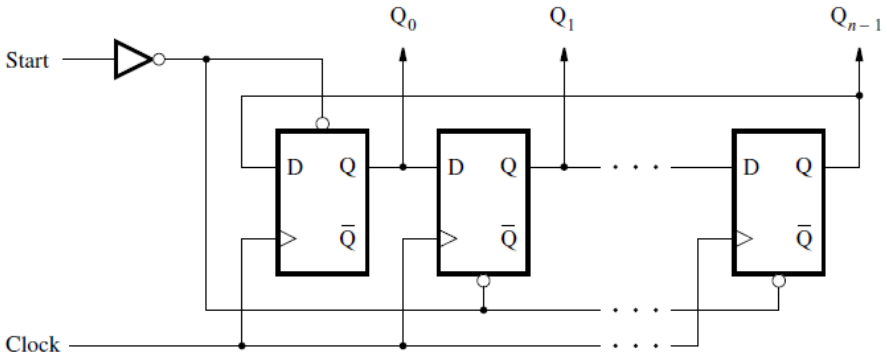
(b) Timing diagram

Synchronous Counter

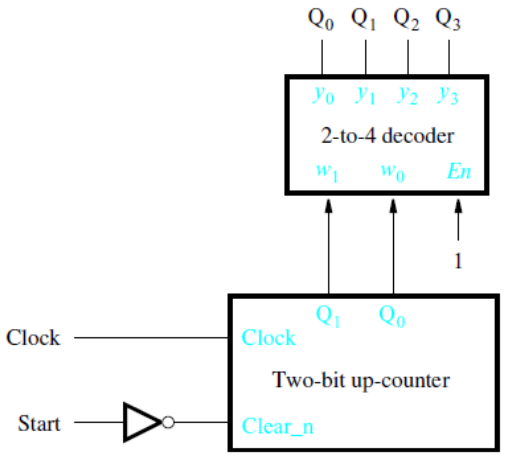
Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



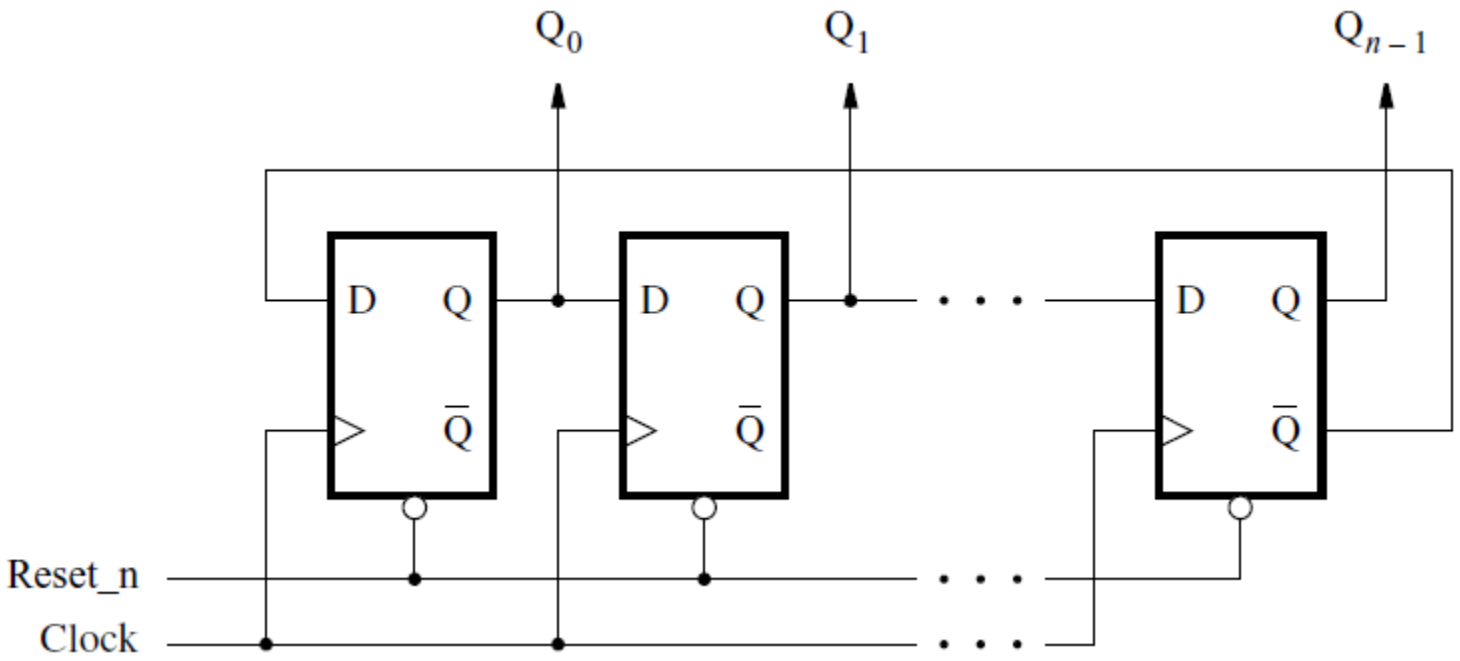
Ring Counter



(a) An *n*-bit ring counter



Johnson Counter

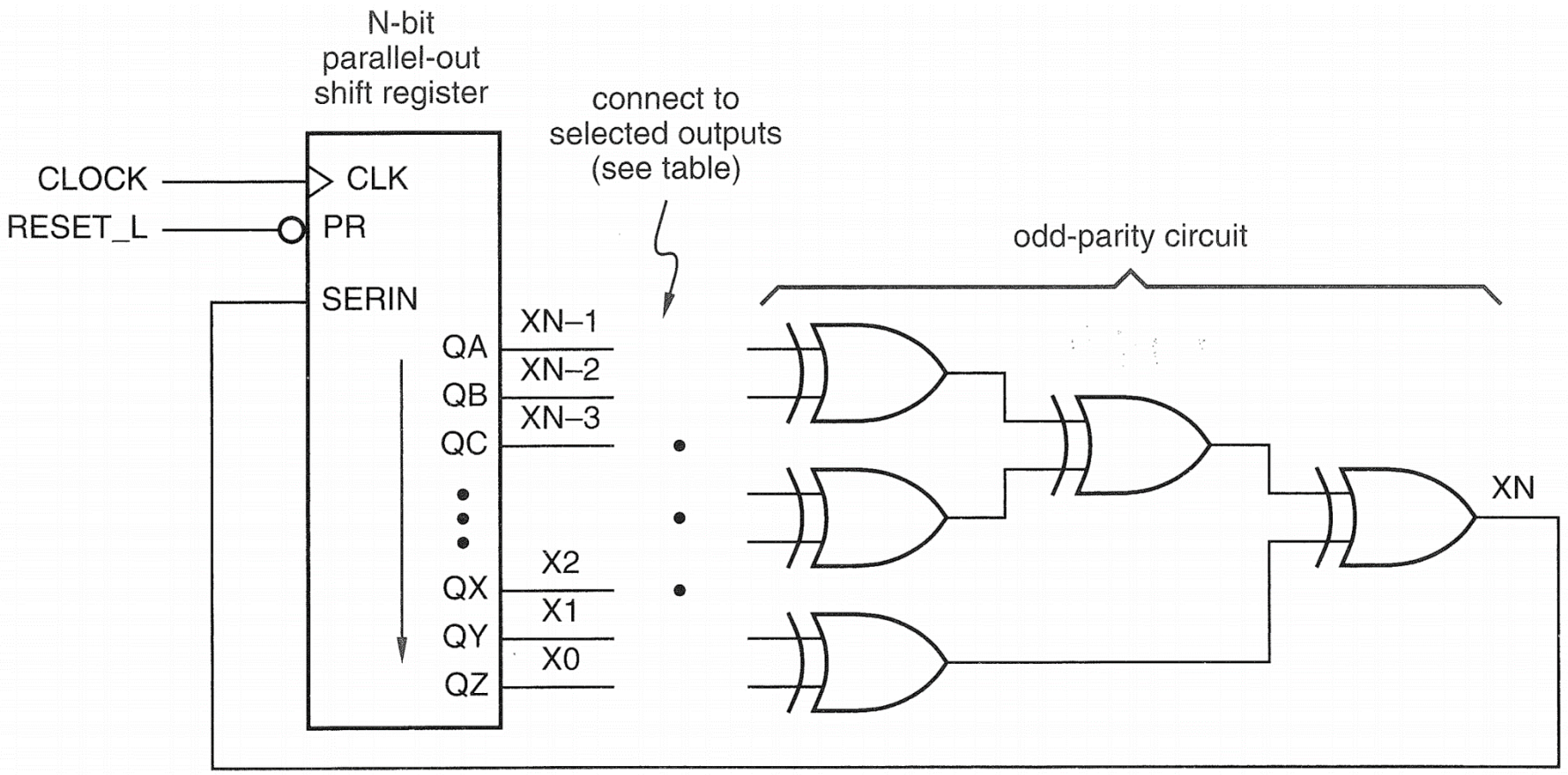


- A variation of the ring counter
- 0000 → 1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001 → 0000

LFSR

- The n-bit shift register we have shown have far less than the maximum of 2^n states.
- An n-bit linear feedback shift-register (LFSR) can have 2^n-1 states; such is also called a maximum-length sequence generator
- The design of the LFSR is based on the theory of finite fields (by Evariste Galois, 1811-1832) shortly before he was killed in a duel with a political opponent

LFSR


N-bit
parallel-out
shift register
connect to
selected outputs
(see table)
odd-parity circuit
CLOCK
RESET_L
CLK
PR
SERIN
QA
QB
QC
QX
QY
QZ
XN–1
XN–2
XN–3
X2
X1
X0
XN

LFSR

n	*Feedback Equation*
2	$X2 = X1 \oplus X0$
3	$X3 = X1 \oplus X0$
4	$X4 = X1 \oplus X0$
5	$X5 = X2 \oplus X0$
6	$X6 = X1 \oplus X0$
7	$X7 = X3 \oplus X0$
8	$X8 = X4 \oplus X3 \oplus X2 \oplus X0$
12	$X12 = X6 \oplus X4 \oplus X1 \oplus X0$
16	$X16 = X5 \oplus X4 \oplus X3 \oplus X0$
20	$X20 = X3 \oplus X0$
24	$X24 = X7 \oplus X2 \oplus X1 \oplus X0$
28	$X28 = X3 \oplus X0$
32	$X32 = X22 \oplus X2 \oplus X1 \oplus X0$

- ← lists feedback equations that yield maximum length sequences for selected values of n
- Many others are available for n > 3
- The initial state stored in the register matters

LFSR

- Used to generate pseudo random sequences
- Digital test circuits
- Error detecting and correcting codes
- Scrambling and descrambling codes in data communications
- Real random number generators, typically in the form of analog circuits, are more complex, large, and power-consuming