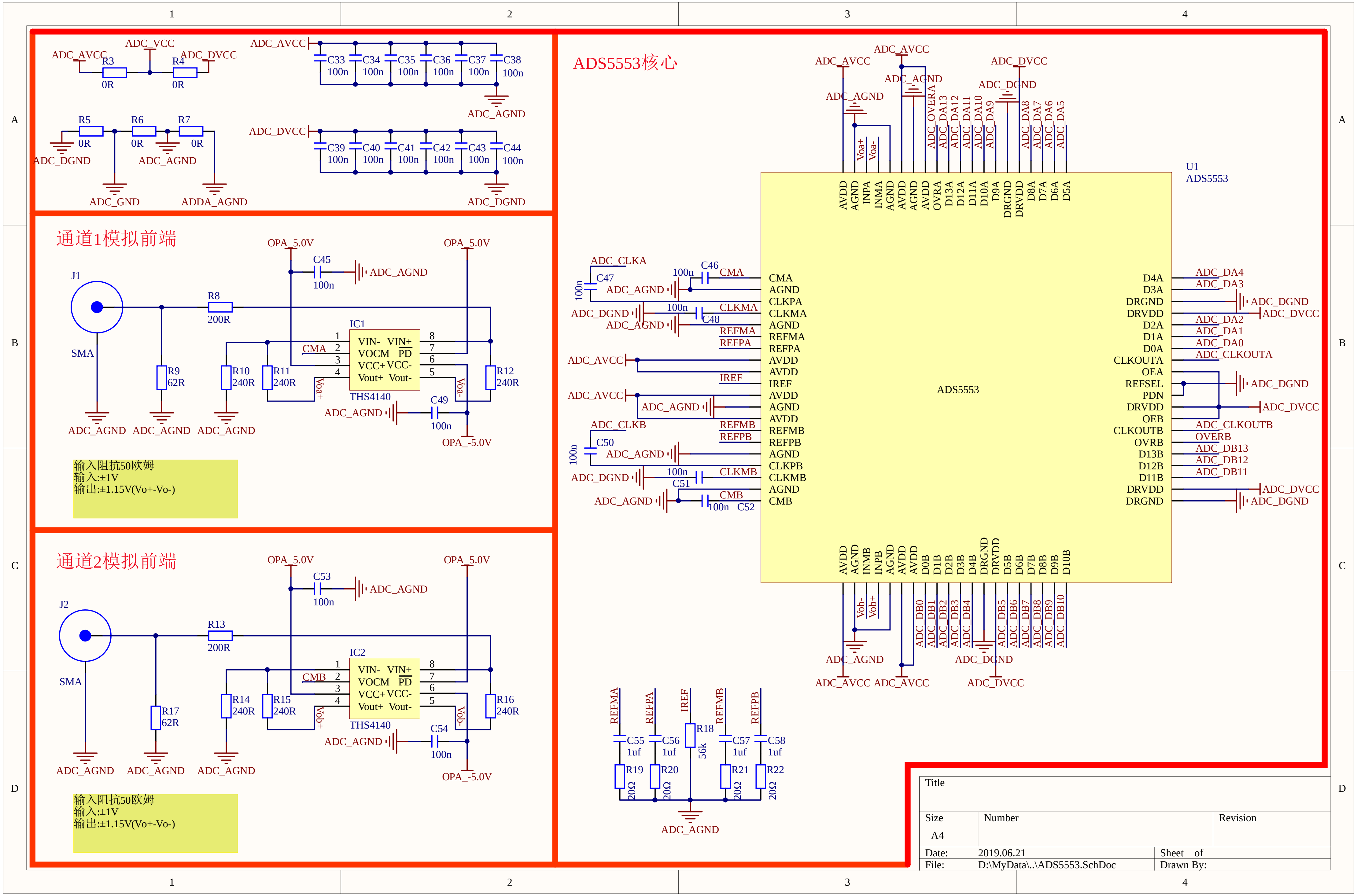
ADS5553核心
通道1模拟前端
通道2模拟前端
输入阻抗50欧姆
输入:±1V
输出:±1.15V(Vo+-Vo-)
输入阻抗50欧姆
输入:±1V
输出:±1.15V(Vo+-Vo-)
ADC_AVCC
ADC_VCC
ADC_DVCC
ADC_AGND
ADC_DGND
ADC_GND
ADDA_AGND
OPA_5.0V
OPA_-5.0V
J1
J2
SMA
IC1
IC2
THS4140
VIN- VIN+
VOCM PD
VCC+ VCC-
Vout+ Vout-
U1
ADS5553
CMA
CMB
CLKMA
CLKMB
REFMA
REFPA
REFMB
REFPB
IREF
ADC_CLKA
ADC_CLKB
ADC_CLKOUTA
ADC_CLKOUTB
OVERB
Title
Size
A4
Number
Revision
Date: 2019.06.21
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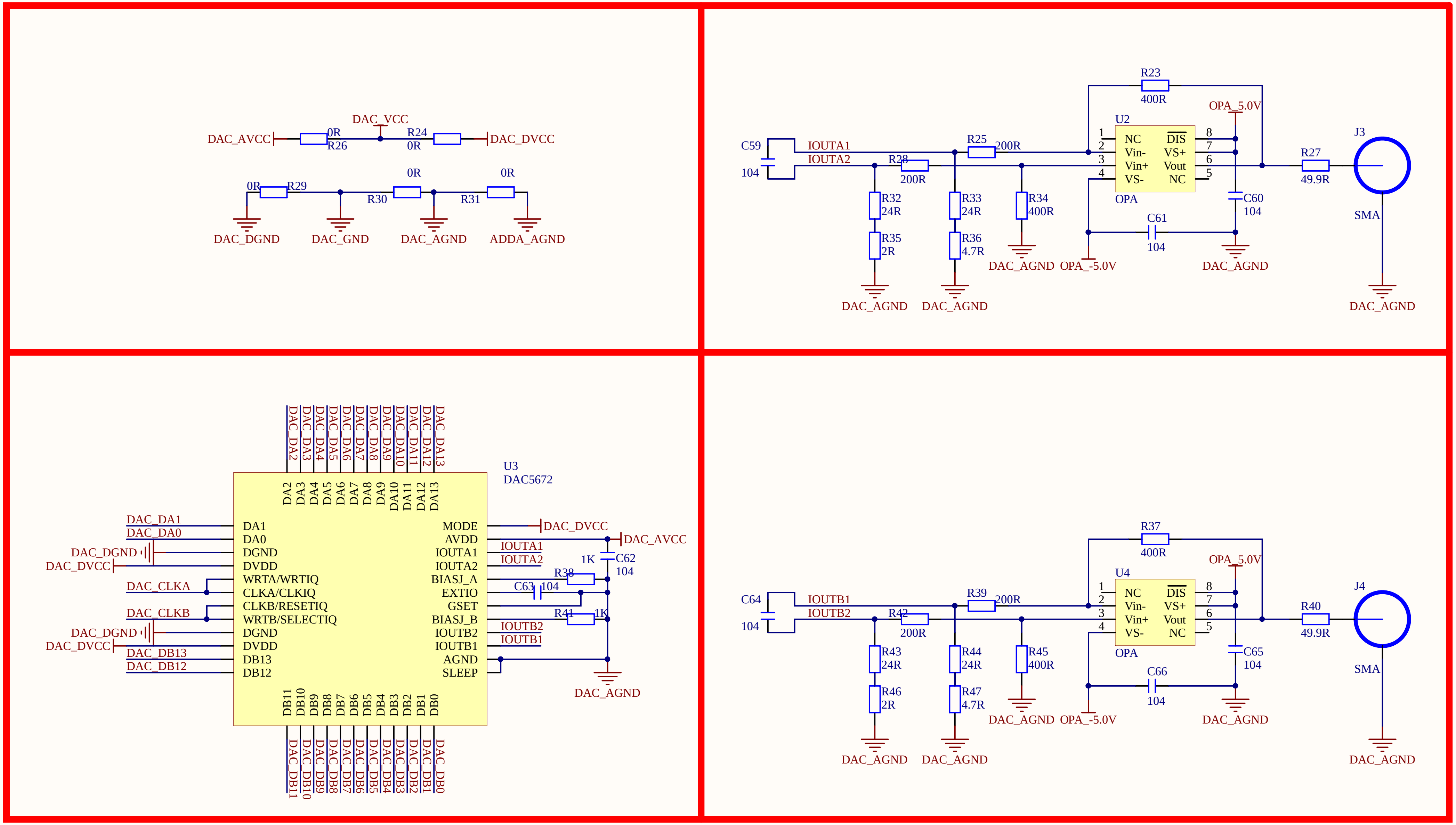

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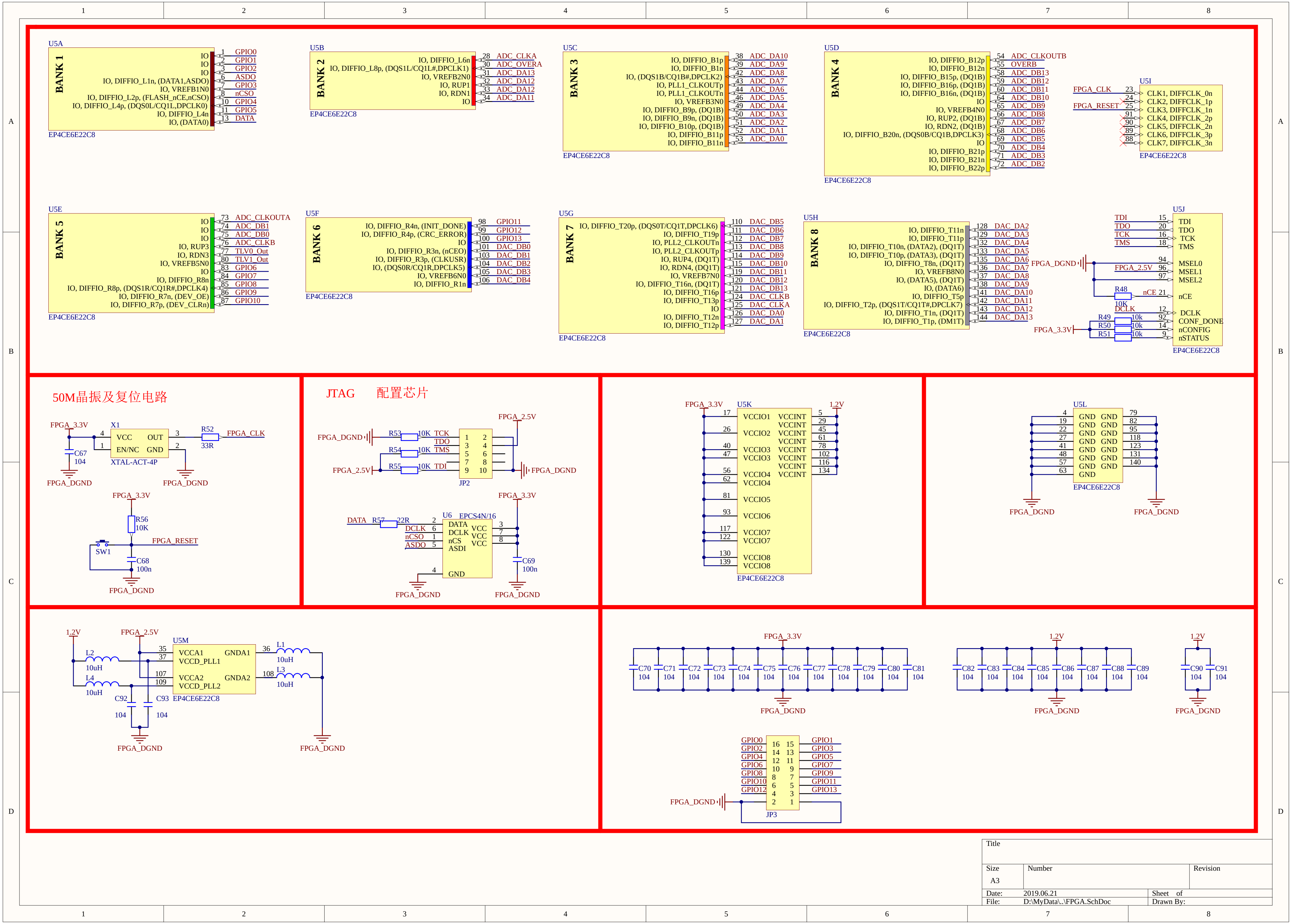

50M晶振及复位电路
JTAG
配置芯片
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7
BANK 8
EP4CE6E22C8
FPGA_3.3V
FPGA_2.5V
1.2V
FPGA_DGND
FPGA_CLK
FPGA_RESET
XTAL-ACT-4P
EPCS4N/16
JP2
JP3
Title
Size
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Number
Revision
Date: 2019.06.21
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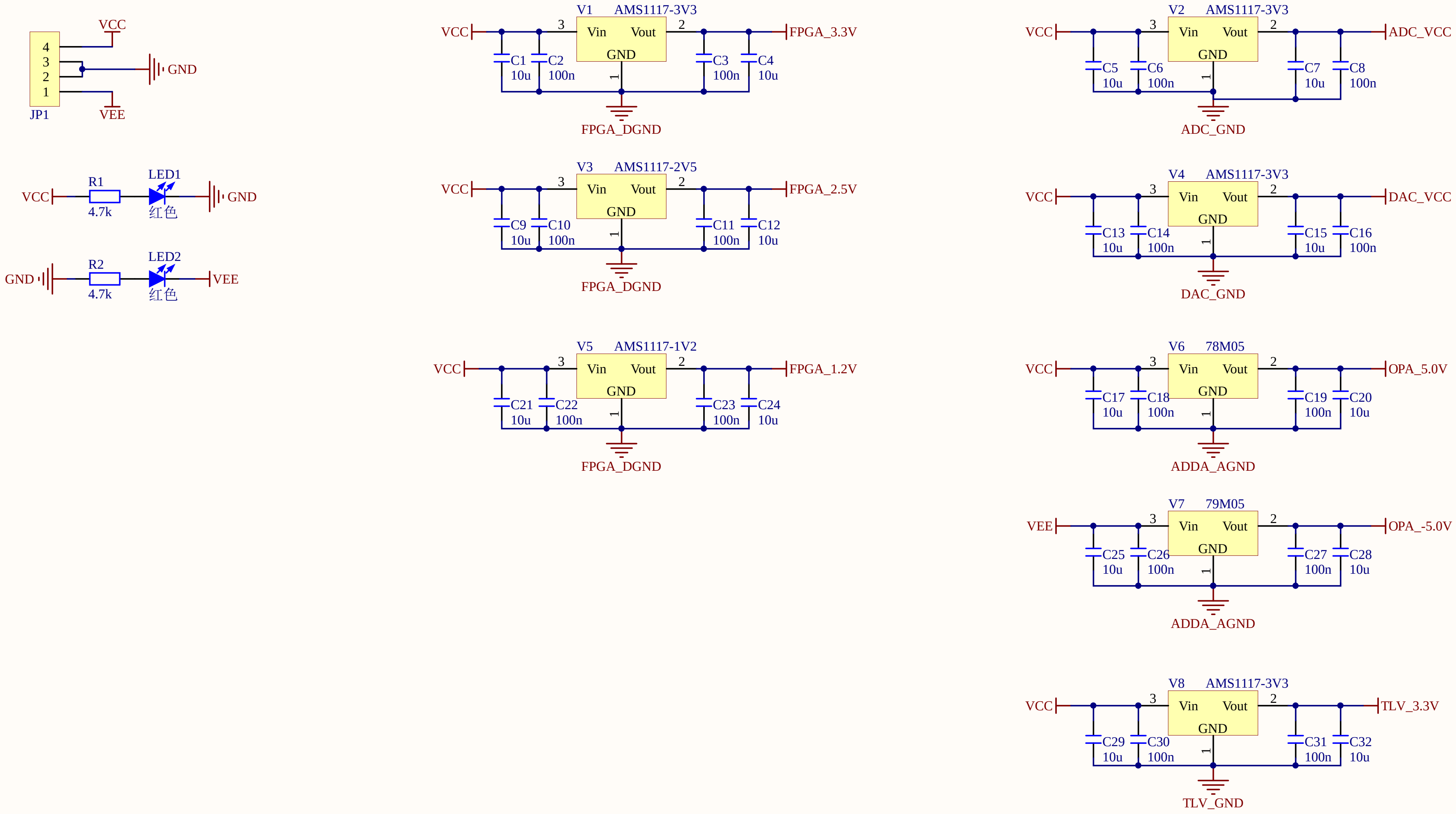

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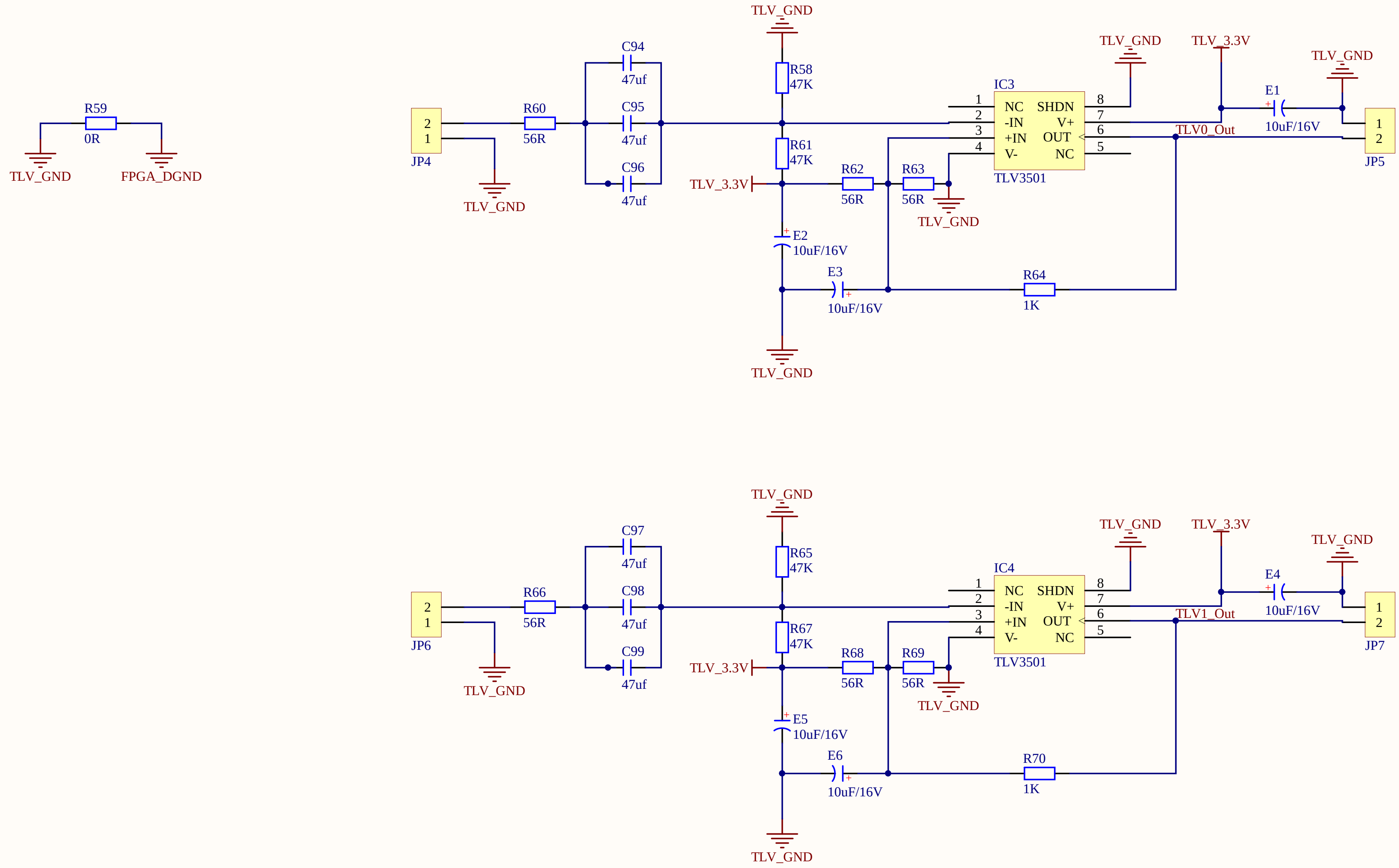

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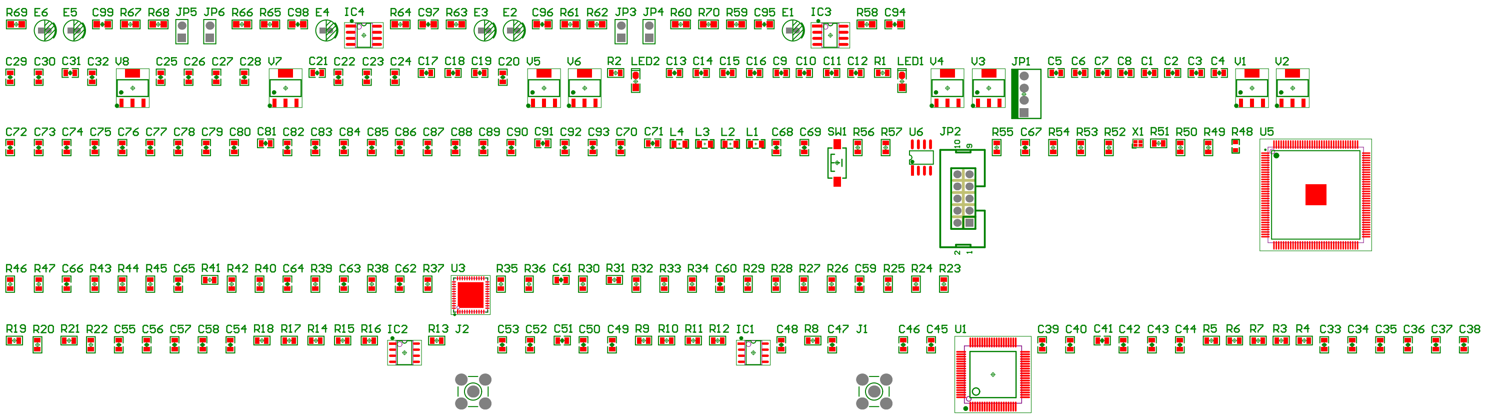
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C29 C30 C31 C32 V8 C25 C26 C27 C28 V7 C21 C22 C23 C24 C17 C18 C19 C20 V5 V6 R2 LED2 C13 C14 C15 C16 C9 C10 C11 C12 R1 LED1 V4 V3 JP1 C5 C6 C7 C8 C1 C2 C3 C4 V1 V2
C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C70 C71 L4 L3 L2 L1 C68 C69 SW1 R56 R57 U6 JP2 R55 C67 R54 R53 R52 X1 R51 R50 R49 R48 U5
10
9
2
1
R46 R47 C66 R43 R44 R45 C65 R41 R42 R40 C64 R39 C63 R38 C62 R37 U3 R35 R36 C61 R30 R31 R32 R33 R34 C60 R29 R28 R27 R26 C59 R25 R24 R23
R19 R20 R21 R22 C55 C56 C57 C58 C54 R18 R17 R14 R15 R16 IC2 R13 J2 C53 C52 C51 C50 C49 R9 R10 R11 R12 IC1 C48 R8 C47 J1 C46 C45 U1 C39 C40 C41 C42 C43 C44 R5 R6 R7 R3 R4 C33 C34 C35 C36 C37 C38