Hi3516A/Hi3516D Professional HD IP Camera SoC

Data Sheet

Issue	**08**
Date	**2016-10-28**

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Contents

Contents i
About This Document 1

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About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of the Hi3516A/Hi3516D. This document also describes the interface timings and related parameter in diagrams. In addition, this document details the pins, pin usages, performance parameters, and package of the Hi3516A/Hi3516D.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.

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Symbol	Description
WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
CAUTION	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
TIP	Indicates a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

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Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

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Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 08 (2016-10-28)

This issue is the eighth official release, which incorporates the following changes:

Chapter 2 Hardware

Section 2.7.6 is modified.

In section 2.9.3, figure 2-21 and table 2-109 are modified.

Chapter 3 System

In section 3.5.4, SC_CTRL is modified.

In section 3.5.5, MISC_CTRL56 is modified.

Section 3.9.3 and section 3.9.4 are modified.

Issue 07 (2016-05-10)

This issue is the seventh official release, which incorporates the following changes:

Chapter 2 Hardware

Section 2.7 is modified.

Section 2.9.1.3, table 2-103 is modified.

Issue 06 (2016-01-28)

This issue is the sixth official release, which incorporates the following changes:

Chapter 2 Hardware

Section 2.7.3 and section 2.7.6 are modified.

Section 2.7.8 "Audio CODEC Electrical Parameters" is added.

Chapter 9 Intelligent Video Engine

Section 9.3.2 is modified.

Chapter 13 Peripherals

Section 13.6.1 is modified.

Issue 05 (2015-12-15)

Chapter 2 Hardware

In section 2.9.9, the description of the SPI Timings is modified.

In section 2.3.2, the descriptions of muxctrl_reg93 is modified.

Chapter 3 System

In section 3.2.7, the descriptions of PERI_CRG51 is modified.

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Issue 04 (2015-10-31)

Chapter 2 Hardware

In section 2.6.2, the description of the [6]bit from PADCTRL_REG4 to PADCTRL_REG19 is modified as reserved, and the description of the[5:4]bit is modified.

In section 2.7.3, Table 2-83 is modified.

Chapter 8 Motion Detect Unit

Section 8.2 is modified.

Chapter 13 Peripherals

In section 13.7, the description of USB2.0 registers are modified.

Issue 03 (2015-06-19)

This issue is the third official release, which incorporates the following changes:

Chapter 2 Hardware

In section 2.9.2.3, figure 2-18, figure 2-19 and table 2-97 are modified.

Chapter 3 System

In section 3.10.4.3, step 7 is added to the RTC initialization process.

Chapter 4 Memory Interfaces

In section 4.3.4, the ECC type used in boot mode is changed from ECC60 to ECC64.

Issue 02 (2015-02-10)

This issue is the second official release, which incorporates the following changes:

Chapter 2 Hardware

In section 2.7.3, Table 2-83 is modified.

Chapter 3 System

In section 3.10.7, RTC_ANA_CTRL is added.

Chapter 4 Memory Interfaces

In section 4.1.7.2, the description of IOCTL is modified.

Sections 4.3.6 and 4.4.6 are added.

In section 4.3.9, the Reset Value of the NANDC register is modified.

Appendix A Ordering Information

The Hi3516D mark is added.

Issue 01 (2014-12-20)

This issue is the first official release, which incorporates the following changes:

The contents related to the Hi3516D are added.

Chapter 2 Hardware

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In Table 2-81, the reference power consumption of the Hi3516A is added.

Chapter 3 System

In section 3.5.5.2, Audio Codec register are modified.

Chapter 4 Memory Interfaces

In section 4.3.5.2, the description related to the 2 KB page size is added.

Chapter 10 Video Interfaces

In section 10.3.3.2, Figure 10-23 is modified.

Chapter 13 Peripherals

In section 13.1.5, the descrption of I2C_SCL_HCNT and I2C_SCL_LCNT is modified.

Issue 00B05 (2014-11-10)

This issue is the fifth draft release, which incorporates the following changes:

Chapter 2 Hardware

In section 2.2.2, the voltages of the UART and IR pins are changed.

Chapter 3 System

In section 3.11.6, Table 3-22 is modified.

Chapter 9 Intelligent Video Engine

In section 9.1, Figure 9-1 is modified.

Chapter 12 Audio Interfaces

In section 12.1.6, the I2S_CRG_CFG1_00 and I2S_CRG_CFG1_08 registers are modified.

Issue 00B04 (2014-10-09)

This issue is the fourth draft release, which incorporates the following changes:

Chapter 1 Product Description

In section 1.2.13, the description of the NAND flash interface is modified.

Chapter 2 Hardware

In section 2.9.11, contents related to the SDIO interface timing are added.

Chapter 3 System

In section 3.6.3, "Connection Between the DMAC and Peripherals" and "DMAC Request Signals" are added.

The description of the MISC_CTRL50 is modified.

Chpter 9 Intelligent Video Engine

Contents related to registers in section 9.5 and all the configuration information in this document are deleted.

Chapter 10 Video Interfaces

In section 10.2.3.3, the description of the APB clock frequency is deleted.

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Chapter 13 Peripherals

In section 13.4.2, contents related to SDIO interface timing and parameters are deleted.

The description in section 13.9.2 and 13.9.3 is modifed.

Issue 00B03 (2014-09-21)

This issue is the third draft release, which incorporates the following changes:

Chapter 2 Hardware

In section 2.2.1, the pin corresponding to RSTN is changed in Table 2-19.

Chapter 4 Memory Interfaces

In section 4.14.3, Step 1 is deleted.

In section 4.1.6.2, a note related to DDRC_CFG_DDRMODE bit[8] is added

Chapter 9 Intelligent Video Engine

In section 9.3.1, a note is added.

Chapter 10 Video Interfaces

In section 10.3, Table 10-8 is modified, and Table 10-9 is added.

Issue 00B02 (2014-09-14)

This issue is the second draft release, which incorporates the following changes:

Chapter 1 Product Description

In section 1.3.4, internal registers such as ARM WDG, timer, and GIC registers are added to Table 1-3.

Chapter 2 Hardware

In section 2.2.2, Table 2-15 and Table 2-16 are modified, the VI pin description is moved below the MIPI pin description, a caution is added, and the voltage of AVDD18_MIPI is changed to 3.3 V/1.8 V in Table 2-16.

Section 2.2.3, 2.7.6, 2.9.10 and 2.9.11 are added.

In section 2.6.1, the base address for pad_ctrl registers is changed to 0x200F_0800.

Chapter 3 System

In section 3.5.3, the description of the normal mode is modified.

In section 3.5.4.2, the description of SYSSTAT bit[2:1] is modified.

In section 3.2.7, the description of PERI_CRG10 bit[10:0] and PERI_CRG11 bit[9] is changed to "reserved", VPLL0 of PERI_CRG4 and PERI_CRG5 is changed to VPLL, and the description of PERI_CRG51 bit[1:0] is modified.

Chapter 9 Intelligent Video Engine

Table 9-2 is added.

In section 9.3.1, two cautions are added.

In section 9.4, the registers from NEXT_NODE_ADDR are deleted.

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Chapter 13 Peripherals

In sections 13.5 and 13.8, the base addresses for IR registers and LSADC registers are changed.

In section 13.8.2, the sampling precision of 6 bits is deleted.

Issue 00B01 (2014-07-25)

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Contents

1 Product Description 1-1
1.1 Application Scenarios 1-1
1.1.1 Hi3516A HD IP Camera Solution 1-2
1.1.2 Hi3516D HD IP Camera Solution 1-2
1.2 Architecture 1-3
1.2.1 Overview 1-3
1.2.2 Processor Core 1-5
1.2.3 Video Encoding Specifications 1-5
1.2.4 Video Encoding Performance 1-5
1.2.5 Intelligent Video Analysis 1-6
1.2.6 Video and Graphics Processing 1-6
1.2.7 ISP 1-6
1.2.8 Audio Encoding and Decoding 1-6
1.2.9 Security Engine 1-7
1.2.10 Video Interfaces 1-7
1.2.11 Audio Interfaces 1-7
1.2.12 Peripheral Interfaces 1-7
1.2.13 External Memory Interfaces 1-8
1.2.14 SDK 1-8
1.2.15 Physical Specifications 1-8
1.3 Boot Modes 1-8
1.3.2 Booting from the BOOTROM 1-9
1.3.3 Booting from the NAND Flash 1-9
1.3.4 Booting from the SPI Flash 1-9
1.4 Address Space Mapping 1-10

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Figures

Figure 1-1 Application block diagram of the Hi3516A 1-2
Figure 1-2 Application block diagram of the Hi3516D 1-3
Figure 1-3 Logic block diagram of the Hi3516A 1-4
Figure 1-4 Logic block diagram of the Hi3516D 1-5

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Tables

Table 1-1 Mapping between signal values and boot modes 1-9

Table 1-2 Mapping between signal values and SPI flash boot modes 1-10

Table 1-3 Address space mapping 1-10

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1 Product Description

CAUTION

Unless otherwise specified, this document applies to the Hi3516A and Hi3516D. The descriptions are provided using the Hi3516A as an example.

Differences Between the Hi3516A and the Hi3516D

Item	Hi3516A	Hi3516D
Memory interface	32-/16-bit DDR3/3L	16-bit DDR3/3L
Maximum encoding performance	5 megapixels@30 fps+VGA@30 fps	3 megapixels@30 fps+VGA@30 fps
Hardware	-	22 I/O pins not supported (for details, see chapter 2 "Hardware.")

1.1 Application Scenarios

As a new-generation system-on-chip (SoC) designed for the high-definition (HD) IP camera, the Hi3516A/Hi3516D integrates a new-generation image signal processor (ISP) and adopts the latest H.265 compressed video encoder, advanced low-power technology, and low-power architecture design. These features help the Hi3516A/Hi3516D keep the leading position in the aspects of low bit rate, high picture quality, and low power consumption. The Hi3516A/Hi3516D supports 90° or 270° rotation and lens distortion correction, which meets requirements in various surveillance applications. It also fully supports 3A algorithms, which allow customers to design different types of IP cameras including the IP automatic focus (AF) zoom module. The Hi3516A/Hi3516D integrates the power-on reset (POR), real-time clock (RTC), and audio coder/decoder (CODEC) and supports various sensor levels and clock outputs, which significantly reduces the EBOM costs for the Hi3516A/Hi3516D HD IP

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camera. Similar to other HiSilicon digital video recorder (DVR) and network video recorder (NVR) software development kits (SDKs), the Hi3516A/Hi3516D SDK features high stability and ease of use, which allows rapid mass production and facilitates system layout of IP cameras, DVRs, and NVRs.

1.1.1 Hi3516A HD IP Camera Solution

Figure 1-1 shows the typical application scenario of the Hi3516A.

Figure 1-1 Application block diagram of the Hi3516A

1.1.2 Hi3516D HD IP Camera Solution

Figure 1-2 shows the typical application scenario of the Hi3516D.

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Figure 1-2 Application block diagram of the Hi3516D

1.2 Architecture

1.2.1 Overview

Figure 1-3 and Figure 1-4 show the logic block diagrams the Hi3516A and Hi3516D respectively.

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Figure 1-3 Logic block diagram of the Hi3516A

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Figure 1-4 Logic block diagram of the Hi3516D

1.2.2 Processor Core

- A7@600 MHz, 32 KB I-cache, 32 KB D-cache/128 KB L2 cache
- Neon acceleration, integrated floating-point unit (FPU)

1.2.3 Video Encoding Specifications

- H.264 BP/MP/HP
- H.265 main profile
- MJPEG/JPEG baseline encoding

1.2.4 Video Encoding Performance

- A maximum of 5-megapixel resolution for H.264/H.265 encoding
- Real-time H.264/H.265 encoding of multiple streams:

  Hi3516A:
  - 1080p@30 fps+720p@30 fps+video graphics array (VGA)@30 fps
  - 1080p@60 fps+VGA@30 fps
  - 5-megapixel@30 fps+VGA@30 fps

  Hi3516D:

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  - 1080p@30 fps+720p@30 fps+video graphics array (VGA)@30 fps
  - 3-megapixel@30 fps+VGA@30 fps
  - 5-megapixel@15 fps
- JPEG snapshot at 5-megapixel@8 fps
- Supporting the constant bit rate (CBR)/variable bit rate (VBR) bit rate control mode, ranging from 16 kbit/s to 40 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 240 fps
- Encoding of eight regions of interest (ROIs)

1.2.5 Intelligent Video Analysis

Integrated intelligent video engine (IVE), supporting various intelligent analysis applications such as motion detection, boundary security and video diagnosis

1.2.6 Video and Graphics Processing

- 3D denoising, image enhancement, and dynamic contrast enhancement
- Anti-flicker for output videos and graphics
- 1/15.99x to 16x video scaling
- 1/2x to 2x graphics scaling
- On-screen display (OSD) overlay pre-processing for eight regions
- Video graphics overlaying of two layers (video layer and graphics layer)

1.2.7 ISP

- Adjustable 3A functions, including automatic exposure (AE), automatic white balance (AWB), and AF
- Noise reduction in fixed pattern noise (FPN) mode
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilizer
- Anti-fog
- Lens distortion correction
- Picture rotation by 90° or 270°
- Mirroring and flipping
- Digital wide dynamic range (WDR), frame base/line base WDR, and tone mapping
- ISP tuning tools for the PC

1.2.8 Audio Encoding and Decoding

- Voice encoding/decoding in compliance with multiple protocols by using software
- G.711, ADPCM, and G.726 protocols
- Audio echo cancellation (AEC), automatic noise reduction (ANR), and auto level control (ALC)

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1.2.9 Security Engine

- Various encryption and decryption algorithms using hardware, such as advanced encryption standard (AES), data encryption standard (DES), and triple data encryption standard (3DES)
- Digital watermark

1.2.10 Video Interfaces

- Input
  - 8-/10-/12-/14-bit RGB Bayer digital camera (DC) timing VI, a maximum of 150 MHz clock frequency
  - BT.601, BT.656, or BT.1120 VI interface
  - Mobile industry processor interface (MIPI), low-voltage differential signaling (LVDS)/sub-LVDS, and high-speed serial pixel interface (HiSPI)
  - Compatibility with mainstream HD complementary metal-oxide semiconductor (CMOS) sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
  - Maximum input resolution of 5 megapixels
- Output
  - One phase alternating line (PAL)/National Television Systems Committee (NTSC) output for automatic load detection
  - One BT.1120/BT.656 video output (VO) interface for connecting to an external high definition multimedia interface (HDMI) or serial digital interface (SDI), up to 1080p@60 fps output

1.2.11 Audio Interfaces

- Integrated audio CODEC, supporting 16-bit audio inputs and outputs
- Inter-IC sound (I^2S) interface for connecting to an external audio CODEC

1.2.12 Peripheral Interfaces

- POR
- One integrated high-precision RTC
- One dual-channel successive approximation register analog-to-digital converter (SAR ADC)
- Four universal asynchronous receiver transmitter (UART) interfaces
- One infrared (IR) interface, three inter-integrated circuit (I^2C) interfaces, four serial peripheral interface (SPI) master interfaces, 14 x 8 + 3 general-purpose input/output (GPIO) interfaces
- Eight pulse-width modulation (PWM) interfaces (four independent interfaces and four multiplexed with other pins)
- Two secure digital input/output 3.0 (SDIO 3.0) interfaces, supporting secure digital extended capacity (SDXC)
- One USB 2.0 host/device port

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- RGMII/RMII/MII in 100/1000 Mbit/s full-duplex or half-duplex mode, physical layer (PHY) clock output, and TCP segmentation offload (TSO) network acceleration

1.2.13 External Memory Interfaces

- DDR3/3L synchronous dynamic random access memory (SDRAM interface)
  - One 32-bit DDR3/3L interface with the maximum frequency of 600 MHz (1.2 Gbit/s) (16-bit DDR3/3L for the Hi3516D)
  - Maximum capacity of 4 Gbits for a 16-bit DDR
  - Maximum capacity of 8 Gbits for two 16-bit DDRs
- SPI NOR flash interface
  - 1-, 2-, or 4-wire mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface

  Maximum capacity of 4 Gbits
- NAND flash interface
  - 8-bit data width
  - Single-level cell (SLC) or multi-level cell (MLC)
  - 4-, 8-, or 24-bit error correcting code (ECC)
  - Components with 8 GB capacity or larger
- Booting from the SPI flash, SPI NAND flash, or NAND flash

1.2.14 SDK

- Linux-3.4-based SDK
- High-performance H.264/H.265 PC decoding library

1.2.15 Physical Specifications

- Power consumption
  - 1.1 typical power consumption@1080p60
  - Multi-level power-saving mode
- Operating voltages
  - 1.1 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
  - 1.35 V or 1.5 V DDR3/3L SDRAM interface voltage
- Package

  Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.), 0.65 mm (0.03 in.) ball pitch, thin & fine-pitch ball grid array (TFBGA), restrictions on the use of certain hazardous substances (RoHS)

1.3 Boot Modes

The Hi3516A can boot from:

- External NAND flash

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- External SPI flash
- BOOTROM

During POR, the boot mode of the Hi3516A depends on the values of the BOOTROM_SEL and BOOT_SEL signals. Table 1-1 describes the mapping between signal values and boot modes.

Table 1-1 Mapping between signal values and boot modes

BOOTROM_SEL	BOOT_SEL	Boot Mode
1	X	Booting from the BOOTROM
0	0	Booting from an external SPI flash
0	1	Booting from an external NAND flash

NOTE

- The BOOTROM_SEL signal is multiplexed with the external pin VO_DAT1.
- The BOOT_SEL signal is multiplexed with the external pin VO_DAT0.

1.3.2 Booting from the BOOTROM

When the Hi3516A boots from the BOOTROM, the serial port communication mechanism starts, the communication between the serial port and the related software running on the PC is set up, and then the boot program is downloaded. For details, see the *Fastboot Application Notes*. If the serial port communication times out, the level of BOOT_SEL is checked. If BOOT_SEL is 0, the Hi3516A boots from the SPI flash; if BOOT_SEL is 1, the Hi3516A boots from the NAND flash.

1.3.3 Booting from the NAND Flash

When the Hi3516A boots from the NAND flash, the external memory is a NAND flash. In this case, you must select the boot memory by configuring the levels of the pins BOOTROM_SEL (multiplexed with the external pin VO_DAT1) and BOOT_SEL (multiplexed with the external pin VO_DAT0). When BOOTROM_SEL is 0 and BOOT_SEL is 1, the Hi3516A can boot from the NAND flash mounted on the NANDC interface.

1.3.4 Booting from the SPI Flash

When the Hi3516A boots from the SPI flash, the external memory is an SPI flash. In this case, you must select the boot memory by configuring the levels of the pins BOOTROM_SEL (multiplexed with the external pin VO_DAT1) and BOOT_SEL (multiplexed with the external pin VO_DAT0). When BOOTROM_SEL is 0 and BOOT_SEL is 0, the Hi3516A can boot from the SPI flash mounted on the SFC interface.

During POR, the SPI flash boot mode of the Hi3516A depends on the values of the SFC_DEVICE_MODE and SFC_BOOT_MODE signals. Table 1-2 describes the mapping between signal values and SPI flash boot modes.

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Table 1-2 Mapping between signal values and SPI flash boot modes

SFC_DEVICE_MOD	SFC_BOOT_MODE	SPI Flash Boot Mode
0	0	SPI NOR flash, 3-byte address mode
0	1	SPI NOR flash, 4-byte address mode
1	0	SPI NAND flash, 1-wire boot mode
1	1	SPI NAND flash, 4-wire boot mode

NOTE

- The SFC_DEVICE_MODE signal is multiplexed with the external pin VO_DAT3.
- The SFC_BOOT_MODE signal is multiplexed with the external pin SFC_CLK.

1.4 Address Space Mapping

Table 1-3 describes the address space mapping.

Table 1-3 Address space mapping

Start Address	End Address	Function	Capacity	Remarks
0xC000_0000	0xFFFF_FFFF	Reserved	-	-
0x8000_0000	0xBFFF_FFFF	Address space of the connected external DDR	1 GB	The Hi3516D supports only the 512 MB DDR.
0x5C00_0000	0x7FFF_FFFF	Reserved	-	-
0x5800_0000	0x5BFF_FFFF	Storage space of the SPI NOR flash	64 MB	-
0x5400_0000	0x57FF_FFFF	Storage space of the SPI NAND flash	64 MB	-
0x5000_0000	0x53FF_FFFF	Storage space of the NAND flash	64 MB	-
0x2070_0000	0x4FFF_FFFF	Reserved	-	-
0x206F_0000	0x206F_FFFF	SDIO1 register	64 KB	-
0x206E_0000	0x206E_FFFF	SDIO0 register	64 KB	-
0x206D_0000	0x206D_FFFF	DDR test module	64 KB	-
0x206C_0000	0x206C_FFFF	MD register	64 KB	-
0x206B_0000	0x206B_FFFF	Reserved	-	-
0x206A_0000	0x206A_FFFF	IVE register	64 KB	-

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Start Address	End Address	Function	Capacity	Remarks
0x2069_0000	0x2069_FFFF	Reserved	64 KB	-
0x2068_0000	0x2068_FFFF	MIPI register	64 KB	-
0x2067_0000	0x2067_FFFF	Reserved	-	-
0x2066_0000	0x2066_FFFF	JPGE register	64 KB	-
0x2065_0000	0x2065_FFFF	AIO register	64 KB	-
0x2064_0000	0x2064_FFFF	VEDU register	64 KB	-
0x2063_0000	0x2063_FFFF	VGS register	64 KB	-
0x2062_0000	0x2062_FFFF	AVC register	64 KB	-
0x2061_0000	0x2061_FFFF	TDE register	64 KB	-
0x2060_0000	0x2060_FFFF	VPSS register	64 KB	-
0x205D_0000	0x205F_FFFF	Reserved	-	-
0x205C_0000	0x205C_FFFF	VDP register	64 KB	-
0x2058_0000	0x205B_FFFF	VICAP register	256 KB	-
0x2030_0000	0x2030_FFFF	GIC internal register	64KB	-
0x2028_0000	0x2057_FFFF	Reserved	-	-
0x2027_0000	0x2027_FFFF	PMC register	64 KB	-
0x2026_0000	0x2026_FFFF	GPIO15 register	64 KB	-
0x2025_0000	0x2025_FFFF	I^2C2 register	64 KB	-
0x2024_0000	0x2024_FFFF	I^2C1 register	64 KB	-
0x2023_0000	0x2023_FFFF	UART3 register	64 KB	-
0x2022_0000	0x2022_FFFF	GPIO14 register	64 KB	-
0x2021_0000	0x2021_FFFF	GPIO13 register	64 KB	-
0x2020_0000	0x2020_FFFF	GPIO12 register	64 KB	-
0x201F_0000	0x201F_FFFF	GPIO11 register	64 KB	-
0x201E_0000	0x201E_FFFF	GPIO10 register	64 KB	-
0x201D_0000	0x201D_FFFF	GPIO9 register	64 KB	-
0x201C_0000	0x201C_FFFF	GPIO8 register	64 KB	-
0x201B_0000	0x201B_FFFF	GPIO7 register	64 KB	-
0x201A_0000	0x201A_FFFF	GPIO6 register	64 KB	-
0x2019_0000	0x2019_FFFF	GPIO5 register	64 KB	-

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Start Address	End Address	Function	Capacity	Remarks
0x2018_0000	0x2018_FFFF	GPIO4 register	64 KB	-
0x2017_0000	0x2017_FFFF	GPIO3 register	64 KB	-
0x2016_0000	0x2016_FFFF	GPIO2 register	64 KB	-
0x2015_0000	0x2015_FFFF	GPIO1 register	64 KB	-
0x2014_0000	0x2014_FFFF	GPIO0 register	64 KB	-
0x2013_2000	0x2013_FFFF	Reserved	-	-
0x2013_1000	0x2013_1FFF	PWM4−7 register	4 KB	-
0x2013_0000	0x2013_0FFF	PWM0−3 register	4 KB	-
0x2012_0000	0x2012_FFFF	MISC register	64 KB	-
0x2011_0000	0x2011_FFFF	DDRC/DDR PHY register	64 KB	-
0x2010_0000	0x2010_FFFF	Reserved	64 KB	-
0x200F_0800	0x200F_FFFF	IO CTR register	62 KB	-
0x200F_0000	0x200F_07FF	IO MUX register	2 KB	-
0x200E_0000	0x200E_FFFF	SPI1 register	64 KB	-
0x200D_0000	0x200D_FFFF	I^2C0 register	64 KB	-
0x200C_0000	0x200C_FFFF	SPI0 register	64 KB	-
0x200B_0000	0x200B_FFFF	SAR_ADC register	64 KB	-
0x200A_0000	0x200A_FFFF	UART2 register	64 KB	-
0x2009_0000	0x2009_FFFF	UART1 register	64 KB	-
0x2008_0000	0x2008_FFFF	UART0 register	64 KB	-
0x2007_0000	0x2007_FFFF	IR register	64 KB	-
0x2006_0000	0x2006_FFFF	RTC register	64 KB	-
0x2005_0000	0x2005_FFFF	SYS_CTRL register	64 KB	-
0x2004_0000	0x2004_FFFF	WDG register	64 KB	-
0x2003_0000	0x2003_FFFF	CRG register	64 KB	-
0x2002_0000	0x2002_FFFF	Reserved	64 KB	-
0x2001_0000	0x2001_FFFF	Timer 2/Timer 3 register	64 KB	-
0x2000_0000	0x2000_FFFF	Timer 0/Timer 1 register	64 KB	-
0x100D_0000	0x1FFF_FFFF	Reserved	-	-
0x100C_0000	0x100C_FFFF	Cipher register	64 KB	-

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Start Address	End Address	Function	Capacity	Remarks
0x100B_0000	0x100B_FFFF	USB EHCI register	64 KB	-
0x100A_0000	0x100A_FFFF	USB OHCI register	64 KB	-
0x1009_0000	0x1009_FFFF	GSF register	64 KB	-
0x1008_0000	0x1008_FFFF	USB device register	64 KB	-
0x1007_0000	0x1007_FFFF	Reserved	64 KB	-
0x1006_0000	0x1006_FFFF	DMAC register	64 KB	-
0x1005_0000	0x1005_FFFF	Reserved	64 KB	-
0x1004_0000	0x1004_FFFF	SPI NAND flash control register	64 KB	-
0x1002_0000	0x1003_FFFF	Reserved	-	-
0x1001_0000	0x1001_FFFF	SPI NOR flash control register	64 KB	-
0x1000_0000	0x1000_FFFF	NAND flash control register	64 KB	-
0x0402_0000	0x0FFF_FFFF	Reserved	-	-
0x0401_0000	0x0401_FFFF	On-chip RAM	64 KB	-
0x0400_0000	0x0400_FFFF	BOOTROM	64 KB	-
0x0000_0000	0x03FF_FFFF	Memory selected after address remapping is cleared. The address points to the on-chip RAM after remapping is cleared.	64 MB	The boot address space varies according to the setting of BOOT_SEL and BOOTROOM_SEL. {BOOT_SEL, BOOTROOM_SEL}: 00: storage space of the SPI flash 01: BOOTROM 10: storage space of the NAND flash 11: BOOTROM

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Contents

2 Hardware 2-1
2.1 Package and Pinout 2-1
2.1.1 Package 2-1
2.1.2 Pinout 2-3
2.2 Pin Description 2-15
2.2.1 Pin Types 2-15
2.2.2 Pin Details 2-16
2.2.3 Default Reset Status of Digital Pins 2-56
2.3 Pin Multiplexing Control Registers 2-63
2.3.1 Register Summary 2-63
2.3.2 Register Description 2-69
2.4 Software Multiplexed Pins 2-131
2.5 Hardware Multiplexed Pins 2-155
2.6 Pin Drive Capability Registers 2-157
2.6.1 Register Summary 2-157
2.6.2 Register Description 2-164
2.7 Electrical Specifications 2-272
2.7.1 Power Consumption Parameters 2-272
2.7.2 Temperature and Thermal Resistance Parameters 2-272
2.7.3 Operating Conditions 2-273
2.7.4 Power-On and Power-Off Sequences 2-274
2.7.5 DC and AC Electrical Parameters 2-275
2.7.6 MIPI/LVDS RX Electrical Parameters 2-278
2.7.7 SDIO Electrical Parameters 2-279
2.7.8 Audio CODEC Electrical Parameters 2-280
2.8 PCB Design Recommendations 2-281
2.9 Interface Timings 2-282
2.9.1 DDR Interface Timings 2-282
2.9.2 Timings of the NANDC Interface 2-284
2.9.3 SFC Interface Timings 2-287
2.9.4 Ethernet MAC Port Timings 2-288
2.9.5 VI Interface Timing 2-294

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2.9.6 VO Interface Timing 2-295
2.9.7 AIO Interface Timings 2-295
2.9.8 I^2C Interface Timing 2-297
2.9.9 SPI Timings 2-298
2.9.10 MIPI RX Timings 2-300
2.9.11 SDIO Timings 2-301

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Figures

Figure 2-1 Top view 2-1
Figure 2-2 Bottom view 2-2
Figure 2-3 Side view 2-2
Figure 2-4 Enlarged view of detail "A" 2-2
Figure 2-5 Package dimensions 2-3
Figure 2-6 Pin map part 1 of the Hi3516A (A1–K11) 2-5
Figure 2-7 Pin map part 1 of the Hi3516D (A1–K11) 2-6
Figure 2-8 Pin map part 2 of the Hi3516A/Hi3516D (A12–K22) 2-7
Figure 2-9 Pin map part 3 of the Hi3516A/Hi3516D (L1–AB11) 2-8
Figure 2-10 Pin map part 4 of the Hi3516A/Hi3516D (L12–AB22) 2-9
Figure 2-11 Video input paths of the MIPI PHY and VI pin 2-33
Figure 2-12 Write timing of dqs_out relative to dq_out for the DDR3 2-282
Figure 2-13 Write timing of dqs_out relative to CK for the DDR3 2-282
Figure 2-14 Write timing of CMD/ADDR relative to CK 2-283
Figure 2-15 Output timing of the DDRn SDRAM 2-283
Figure 2-16 Command cycle timing of the NANDC interface 2-284
Figure 2-17 Address cycle timing of the NANDC interface 2-285
Figure 2-18 Write data timing of the NANDC interface 2-286
Figure 2-19 Read data timing of the NANDC interface 2-287
Figure 2-20 SFC input timing 2-288
Figure 2-21 SFC output timing 2-288
Figure 2-22 100 Mbit/s RX timing of the MII 2-289
Figure 2-23 100 Mbit/s TX timing of the MII 2-289
Figure 2-24 10 Mbit/s RX timing of the MII 2-289
Figure 2-25 10 Mbit/s TX timing of the MII 2-289
Figure 2-26 RX timing parameters of the MII 2-290

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Figure 2-27 TX timing parameters of the MII 2-290
Figure 2-28 100 Mbit/s RX timing of the RMII 2-291
Figure 2-29 100 Mbit/s TX timing of the RMII 2-291
Figure 2-30 10 Mbit/s RX timing of the RMII 2-291
Figure 2-31 10 Mbit/s TX timing of the RMII 2-291
Figure 2-32 Timing parameters of the RMII 2-292
Figure 2-33 1000 Mbit/s RX timing of the RGMII 2-292
Figure 2-34 1000 Mbit/s TX timing of the RGMII 2-293
Figure 2-35 Read timing of the MDIO interface 2-293
Figure 2-36 Write timing of the MDIO interface 2-293
Figure 2-37 RX timing parameters of the MDIO interface 2-294
Figure 2-38 VI interface timing in CMOS mode 2-294
Figure 2-39 Timing of the VO interface 2-295
Figure 2-40 RX timing of the I^2S interface 2-295
Figure 2-41 TX timing of the I^2S interface 2-295
Figure 2-42 RX timing of the PCM interface 2-296
Figure 2-43 TX timing of the PCM interface 2-296
Figure 2-44 I^2C transfer timing 2-297
Figure 2-45 SPICK timing 2-298
Figure 2-46 SPI timing in master mode (sph = 1) 2-298
Figure 2-47 SPI timing in master mode (sph = 0) 2-298
Figure 2-48 Output timing 2-301
Figure 2-49 Input timing 2-301

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Tables

Table 2-1 Pin quantity of the Hi3516A 2-3
Table 2-2 Pin quantity of the Hi3516D 2-4
Table 2-3 Pin arrangement 2-9
Table 2-4 I/O types 2-15
Table 2-5 ACODEC pins 2-16
Table 2-6 DDR pins 2-17
Table 2-7 EPHY pin 2-22
Table 2-8 MDIO pins 2-23
Table 2-9 Functions of RGMII pins in three modes 2-23
Table 2-10 RGMII pins 2-24
Table 2-11 Sensor pins 2-26
Table 2-12 GPIO pins 2-27
Table 2-13 I^2C2 pins 2-28
Table 2-14 IR pin 2-28
Table 2-15 JTAG pins 2-29
Table 2-16 Functions of MIPI pins in two modes 2-30
Table 2-17 MIPI pins 2-31
Table 2-18 VI pins 2-34
Table 2-19 NFC pins 2-36
Table 2-20 SYS pins 2-39
Table 2-21 PWM pins 2-39
Table 2-22 RTC pins 2-40
Table 2-23 SAR_ADC pins 2-41
Table 2-24 SDIO0 pins 2-41
Table 2-25 SDIO1 pins 2-43
Table 2-26 SFC pins 2-45

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Table 2-27 SPI0 pins....2-46
Table 2-28 SPI1 pins....2-47
Table 2-29 UART pins....2-47
Table 2-30 USB pins....2-49
Table 2-31 VDAC pins....2-50
Table 2-32 Functions of VO pins in two modes....2-50
Table 2-33 VO pins....2-51
Table 2-34 OSC pins....2-55
Table 2-35 Power pins and GND pins....2-55
Table 2-36 Default reset status of digital pins....2-56
Table 2-37 Summary of pin multiplexing control registers (base address: 0x200F_0000)....2-63
Table 2-38 Software multiplexed sensor pins....2-131
Table 2-39 Description of software multiplexed sensor signals....2-132
Table 2-40 Software multiplexed VO pins....2-132
Table 2-41 Description of software multiplexed VO signals....2-133
Table 2-42 Software multiplexed SPI0 pins....2-135
Table 2-43 Description of software multiplexed SPI0 signals....2-135
Table 2-44 Software multiplexed SPI1 pins....2-136
Table 2-45 Description of software multiplexed SPI1 signals....2-136
Table 2-46 Software multiplexed I^2C2 pins....2-137
Table 2-47 Description of software multiplexed I^2C2 signals....2-137
Table 2-48 Software multiplexed UART pins....2-137
Table 2-49 Description of software multiplexed UART signals....2-138
Table 2-50 Software multiplexed JTAG pins....2-139
Table 2-51 Description of software multiplexed JTAG signals....2-139
Table 2-52 Software multiplexed IR pin....2-140
Table 2-53 Description of software multiplexed IRsignals....2-140
Table 2-54 Software multiplexed USB pins....2-140
Table 2-55 Description of software multiplexed USB signals....2-141
Table 2-56 Software multiplexed SDIO0 pins....2-141
Table 2-57 Description of software multiplexed SDIO0 signals....2-142
Table 2-58 Software multiplexed GPIO pins....2-143
Table 2-59 Description of software multiplexed GPIO signals....2-143

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Table 2-60 Software multiplexed SDIO1 pins 2-144

Table 2-61 Description of software multiplexed SDIO1 signals 2-144

Table 2-62 Software multiplexed NFC pins 2-146

Table 2-63 Description of software multiplexed NFC signals 2-147

Table 2-64 Software multiplexed PWM pins 2-148

Table 2-65 Description of software multiplexed PWM signals 2-148

Table 2-66 Software multiplexed SAR_ADC pins 2-149

Table 2-67 Description of software multiplexed SAR_ADC signals 2-149

Table 2-68 Software multiplexed FEPHY pin 2-149

Table 2-69 Description of software multiplexed EPHY signals 2-150

Table 2-70 Software multiplexed MDIO pins 2-150

Table 2-71 Description of software multiplexed MDIO signals 2-150

Table 2-72 Software multiplexed RGMII pins 2-151

Table 2-73 Description of software multiplexed RGMII signals 2-151

Table 2-74 Software multiplexed VI pins 2-152

Table 2-75 Description of software multiplexed VI signals 2-153

Table 2-76 Hardware multiplexed SYS pin 2-156

Table 2-77 Description of the hardware multiplexed SYS signal 2-156

Table 2-78 Hardware multiplexed SFC pin 2-156

Table 2-79 Hardware multiplexed SFC signal 2-156

Table 2-80 Summary of pad_ctrl registers (base address: 0x200F_0800) 2-157

Table 2-81 Power consumption parameters 2-272

Table 2-83 Operating conditions for the SVB related power supply 2-273

Table 2-84 Operating conditions for the power supply under normal voltage 2-273

Table 2-85 DC electrical parameters (DVDD33/DVDD3318_VI/DVDD3318_SENSOR/DVDDIO_RGMII = 3.3 V, incompatible with the 5 V input current) 2-275

Table 2-86 DC electrical parameters (DVDD3318*=1.8V/DVDDIO_RGMII=1.8V) 2-275

Table 2-87 DC electrical parameters in DDR3 SSTL15 mode (VDDIO_DDR = 1.5 V) 2-276

Table 2-88 AC electrical parameters in DDR3 SSTL15 mode (VDDIO_DDR = 1.5 V) 2-277

Table 2-89 DC electrical parameters in DDR3L SSTL135 mode (VDDIO_DDR = 1.35 V) 2-277

Table 2-90 AC electrical specifications in DDR3L SSTL135 mode (VDDIO_DDR = 1.35 V) 2-277

Table 2-91 LVDS differential DC electrical parameters 2-278

Table 2-92 MIPI high-speed (HS) DC parameters 2-279

Table 2-93 MIPI HS AC parameters 2-279

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Table 2-94 MIPI low-power (LP) DC parameters 2-279
Table 2-95 SDIO electrical parameters (3.3 V) 2-279
Table 2-96 SDIO electrical parameters (1.8 V) 2-280
Table 2-97 Overall specifications 2-280
Table 2-98 Major DAC specifications 2-281
Table 2-99 Major ADC specifications 2-281
Table 2-100 Major MICBIAS specifications 2-281
Table 2-101 Major MICPGA specifications 2-281
Table 2-102 DDR3 clock parameters 2-284
Table 2-103 Parameters for the DDR3-1600 SDRAM 2-284
Table 2-104 Command cycle timing parameters of the NANDC interface 2-285
Table 2-105 Address cycle timing parameters of the NANDC interface 2-285
Table 2-106 Write data timing parameters of the NANDC interface 2-286
Table 2-107 Read data timing parameters of the NANDC interface 2-287
Table 2-108 SFC input timing parameters 2-288
Table 2-109 SFC output timing parameters 2-288
Table 2-110 MII timing parameters 2-290
Table 2-111 Timing parameters of the RMII 2-292
Table 2-112 Timing parameters of the RGMII 2-293
Table 2-113 Timing parameters of the MDIO interface 2-294
Table 2-114 VI interface timing parameters 2-294
Table 2-115 Timing parameters of the VO interface 2-295
Table 2-116 Timing parameters of the I^2S interface 2-296
Table 2-117 Timing parameters of the PCM interface 2-296
Table 2-118 Timing parameters of the I^2C interface 2-297
Table 2-119 SPI timing parameters 2-299
Table 2-120 MIPI RX timing parameters 2-300
Table 2-121 SDIO timing parameters 2-301

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2 Hardware

2.1 Package and Pinout

2.1.1 Package

The Hi3516A/Hi3516D uses the lead thin-fine pitch ball grid array (LD TFBGA) package. The Hi3516A has 395 pins, whereas the Hi3516D has 373 pins. The body size is 15 mm x 15 mm (0.6 in. x 0.6 in.), and the ball pitch is 0.65 mm (0.03 in.). Figure 2-1 to Figure 2-4 show package views. Figure 2-5 describes the dimensions.

Figure 2-1 Top view

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Figure 2-2 Bottom view

Figure 2-3 Side view

Figure 2-4 Enlarged view of detail "A"

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Figure 2-5 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	13.65	---	---	0.537	---
E1	---	13.65	---	---	0.537	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	22/22					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

2.1.2 Pinout

Table 2-1 lists the pin quantity of the Hi3516A by type.

Table 2-1 Pin quantity of the Hi3516A

Pin Type	Quantity
I/O	249
Digital power	40
Digital GND	73
Others/Analog power	13
Others/Analog GND	20
DDR reference power	0
Total	395

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Table 2-2 lists the pin quantity of the Hi3516D by type.

Table 2-2 Pin quantity of the Hi3516D

Pin Type	Quantity
I/O	227
Digital power	40
Digital GND	73
Others/Analog power	13
Others/Analog GND	20
DDR reference power	0
Total	373

Pin Map

Figure 2-6 to Figure 2-10 show pin maps of the Hi3516A and Hi3516D.

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Figure 2-6 Pin map part 1 of the Hi3516A (A1–K11)

	01	02	03	04	05	06	07	08	09	10	11
A	VSS	DDR3_CAS_N	DDR3_BA0	DDR3_A5	DDR3_A7	DDR3_A9	DDR3_A0	DDR3_CLK1_P	VSS	DDR3_CLK0_N	VSS
B	DDR3_CS1_N	DDR3_ODT_1	DDR3_RAS_N	DDR3_A3	DDR3_A2	DDR3_RESET_N	DDR3_A13	DDR3_CLK1_N	VSS	DDR3_CLK0_P	VSS
C	DDR3_DQ22	DDR3_DQ20	DDR3_A6	DDR3_WE_N	DDR3_A1	DDR3_A10	DDR3_A12	DDR3_CS0_N	DDR3_A4	DDR3_DQ5	DDR3_DQ3
D	DDR3_DQ25	DDR3_DQ23	DDR3_DQ17	DDR3_A8	DDR3_A14	DDR3_A11	DDR3_CKE	DDR3_BA2	DDR3_BA1	DDR3_ODT_0	DDR3_DQ7
E	DDR3_DQS2_P	DDR3_DQS2_N	DDR3_DQ21	DDR3_DQ19	VSS	VDDIO_DDR	VSS	AVDD_DDRPLL2	VDDIO_DDR	VDDIO_CK_DDR	AVDD_DDRPLL3
F	VSS	VSS	DDR3_DQ18	DDR3_DM3	VDDIO_DDR						
G	DDR3_DQS3_N	DDR3_DQS3_P	DDR3_DQ16	DDR3_DQ31	VDDIO_DDR						
H	DDR3_DQ30	DDR3_DQ28	DDR3_DM2	DDR3_DQ27				VDD_DDR	VSS	VDD_DDR	VDD_DDR
J	DDR3_DQ26	DDR3_ZQ	DDR3_DQ24	DDR3_DQ29	AVDD_DDRPLL1			VDD_DDR	VSS	VSS	VSS
K	NF_RDY0	NF_RDY1	NF_DQ3	NF_DQ2	VSS			VSS	VSS	VSS	VSS

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Figure 2-7 Pin map part 1 of the Hi3516D (A1–K11)

	01	02	03	04	05	06	07	08	09	10	11
A	VSS	DDR3_CAS_N	DDR3_BA0	DDR3_A5	DDR3_A7	DDR3_A9	DDR3_A0	DDR3_CLK1_P	VSS	DDR3_CLK0_N	VSS
B	DDR3_CS1_N	DDR3_ODT_1	DDR3_RAS_N	DDR3_A3	DDR3_A2	DDR3_RESET_N	DDR3_A13	DDR3_CLK1_N	VSS	DDR3_CLK0_P	VSS
C	NC	NC	DDR3_A6	DDR3_WE_N	DDR3_A1	DDR3_A10	DDR3_A12	DDR3_CS0_N	DDR3_A4	DDR3_DQ5	DDR3_DQ3
D	NC	NC	NC	DDR3_A8	DDR3_A14	DDR3_A11	DDR3_CKE	DDR3_BA2	DDR3_BA1	DDR3_ODT_0	DDR3_DQ7
E	NC	NC	NC	NC	VSS	VDDIO_DDR	VSS	AVDD_DDRPLL2	VDDIO_DDR	VDDIO_CK_DDR	AVDD_DDRPLL3
F	VSS	VSS	NC	NC	VDDIO_DDR						
G	NC	NC	NC	NC	VDDIO_DDR						
H	NC	NC	NC	NC				VDD_DDR	VSS	VDD_DDR	VDD_DDR
J	NC	DDR3_ZQ	NC	NC	AVDD_DDRPLL1			VDD_DDR	VSS	VSS	VSS
K	NF_RDY0	NF_RDY1	NF_DQ3	NF_DQ2	VSS			VSS	VSS	VSS	VSS

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Figure 2-8 Pin map part 2 of the Hi3516A/Hi3516D (A12–K22)

12	13	14	15	16	17	18	19	20	21	22	
DDR3_DQ10	DDR3_DQS1_N	VSS	DDR3_DQS0_N	DDR3_DQ0	DDR3_DQ6	RGMII_RXD0	RGMII_RXD2	RGMII_RXD3	RGMII_RX_CLK	VSS	A
DDR3_DM0	DDR3_DQS1_P	VSS	DDR3_DQS0_P	DDR3_DQ12	VSS	RGMII_RX_DV	MDCK	VSS	RGMII_TXD0	RGMII_TX_CLK	B
DDR3_DQ8	DDR3_DQ2	DDR3_DQ4	DDR3_DQ9	DDR3_DQ13		RGMII_RXD1	RGMII_TX_EN	RGMII_TXD2	RGMII_TXD1	VO_DAT15	C
DDR3_DQ1	DDR3_DM1	DDR3_DQ14	DDR3_DQ11	DDR3_DQ15	VSS	MDIO	RGMII_TXD3	GPIO0_1	VO_DAT13	VO_DAT12	D
VDDIO_DDR	VDDIO_DDR	VSS			DVDDIO_RGMII	VSS	EPHY_CLK	VO_DAT14	VO_DAT11	VO_DAT9	E
						DVDD33	VO_DAT8	VO_DAT10	VO_DAT7	VO_DAT5	F
						DVDD33	VO_DAT3	VO_DAT6	VO_DAT4	VO_CLK	G
VSS	VDD	VDD	VDD_MEDIA			VSS	VO_DAT1	VO_DAT0	VO_DAT2	VSS	H
VSS	VSS	VSS	VDD_MEDIA				SDIO1_CWPR	SDIO1_CARD_DETECT	SDIO1_CARD_POWER	SDIO1_CDATA1	J
VSS	VSS	VSS	VDD			SDIO1_VOUT	SDIO1_CDATA3	SDIO1_CDATA0	SDIO1_CCMD	SDIO1_CCLK_OUT	K

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Figure 2-9 Pin map part 3 of the Hi3516A/Hi3516D (L1–AB11)

L	NF_CSN0	NF_REN	NF_DQ4	NF_DQ1	DVDD33			VDD	VSS	VSS	VSS
M	NF_CLE	NF_CSN1	NF_DQ5	NF_DQ6	DVDD33			VDD	VSS	VSS	VSS
N	NF_WEN	NF_ALE	NF_DQ0	NF_DQ7	VSS			VDD	VSS	VSS	VSS
P	SFC_CLK	SFC_WP_IO2	SFC_SOI_IO1	RSTN	AVDD_EFUSE			VDD_CPU	VSS	VSS	VSS
R	VSS	SFC_SIO_IO0	SFC_CSN1	SFC_HOLD_IO3	AVDD11_PLL			VDD_CPU	VDD_CPU	VDD	VDD
T	TEST_MODE	JTAG_EN	POR_SEL	WDG_RSTN	AVSS_PLL						
U	XIN	XOUT	AVDD_BAT	AVDD33_RTC	AVDD33_PLL						
V	VSS	VSS	SAR_ADC_CH0	SAR_ADC_CH1	AVSS_RTC	DVDD3318_SENSOR		DVDD3318_VI		AVSS_MIPI	AVDD18_MIPI
W	RTC_XOUT	RTC_XIN	VSS	VI_HS	VI_DAT13	VI_DAT15	VI_DAT7	VI_DAT11	MIPI0_D3M	MIPI0_CKP	AVSS_MIPI
Y	GPIO0_0	SPI0_SDO	SPI0_CSN	VI_DAT10	VI_DAT12	VI_DAT14	VI_DAT9	AVSS_MIPI	MIPI0_D3P	MIPI0_CKM	AVSS_MIPI
AA	SENSOR_CLK	SPI0_SDI	VI_DAT0	VI_DAT2	VI_DAT4	VSS	VI_CLK	AVSS_MIPI	MIPI0_D1P	MIPI0_D0P	MIPI0_D2P
AB	VSS	SPI0_SCLK	VI_VS	VI_DAT1	VI_DAT3	VI_DAT5	VI_DAT6	VI_DAT8	MIPI0_D1M	MIPI0_D0M	MIPI0_D2M
	01	02	03	04	05	06	07	08	09	10	11

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Figure 2-10 Pin map part 4 of the Hi3516A/Hi3516D (L12–AB22)

VSS	VSS	VSS	VSS			DVDD18_SDIO	SDIO1_CDATA2	SDIO0_CDATA2	SDIO0_CDATA1	SDIO0_CCLK_OUT	L
VSS	VSS	VSS	VDD_MEDIA			SDIO0_VOUT	SDIO0_CDATA0	SDIO0_CCMD	SDIO0_CDATA3	SDIO0_CWPR	M
VSS	VSS	VSS	VDD_MEDIA			AVDD33_AC	SDIO0_CARD_DETEC	SDIO0_CARD_POWE	AVSS_AC	AVSS_AC	N
VSS	VSS	VSS	VDD			AVDD33_VDAC	AVSS_AC	AVSS_AC	AC_LINER	AC_LINEL	P
VSS	VDD_MEDIA	VDD_MEDIA	VDD			AVSS_VDAC	AC_OUTL	AC_OUTR	AC_VREF	AC_MICBIAS	R
						AVDD33_USB	VDAC_IREF	VDAC_CVBS	AVSS_USB	AVSS_USB	T
							AVSS_USB	USB_REXT	USB_DM	USB_DP	U
AVDD18_MIPI	AVSS_MIPI		VSS	DVDD33	DVDD33	VSS	USB_PWREN	PWM0	USB_OVRCUR	UART2_TXD	V
MIPI1_D1P	MIPI1_CKM	AVSS_MIPI	SHUTTER_TRIG	SPI1_SDI	VSS	JTAG_TDO	PWM1	UART1_CTSN	UART0_RXD	UART1_TXD	W
MIPI1_D1M	MIPI1_CKP	AVSS_MIPI	FLASH_TRIG	SPI1_SDO	SPI1_CSN0	JTAG_TCK	UART1_RTSN	GPIO0_4	UART0_TXD	UART1_RXD	Y
MIPI1_D3M	MIPI1_D0M	MIPI1_D2M	AVSS_MIPI	SPI1_SCLK	UART2_RXD	VSS	JTAG_TDI	I2C2_SDA	PWM3	PWM2	AA
MIPI1_D3P	MIPI1_D0P	MIPI1_D2P	AVSS_MIPI	GPIO0_3	JTAG_TRSTN	GPIO0_2	JTAG_TMS	IR_IN	I2C2_SCL	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Pin Arrangement

Table 2-3 lists the pins of the Hi3516A based on their positions.

Table 2-3 Pin arrangement

Position	Pin Name	Position	Pin Name	Position	Pin Name
A1	VSS	H9	VSS	R18	AVSS_VDAC
A2	DDR3_CAS_N	H10	VDD_DDR	R19	AC_OUTL
A3	DDR3_BA0	H11	VDD_DDR	R20	AC_OUTR
A4	DDR3_A5	H12	VSS	R21	AC_VREF

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Position	Pin Name	Position	Pin Name	Position	Pin Name
A5	DDR3_A7	H13	VDD	R22	AC_MICBIAS
A6	DDR3_A9	H14	VDD	T1	TEST_MODE
A7	DDR3_A0	H15	VDD_MEDIA	T2	JTAG_EN
A8	DDR3_CLK1_P	H18	VSS	T3	POR_SEL
A9	VSS	H19	VO_DAT1	T4	WDG_RSTN
A10	DDR3_CLK0_N	H20	VO_DAT0	T5	AVSS_PLL
A11	VSS	H21	VO_DAT2	T18	AVDD33_USB
A12	DDR3_DQ10	H22	VSS	T19	VDAC_IREF
A13	DDR3_DQS1_N	J1	DDR3_DQ26 (not supported for the Hi3516D)	T20	VDAC_CVBS
A14	VSS	J2	DDR3_ZQ	T21	AVSS_USB
A15	DDR3_DQS0_N	J3	DDR3_DQ24 (not supported for the Hi3516D)	T22	AVSS_USB
A16	DDR3_DQ0	J4	DDR3_DQ29 (not supported for the Hi3516D)	U1	XIN
A17	DDR3_DQ6	J5	AVDD_DDRPLL1	U2	XOUT
A18	RGMII_RXD0	J8	VDD_DDR	U3	AVDD_BAT
A19	RGMII_RXD2	J9	VSS	U4	AVDD33_RTC
A20	RGMII_RXD3	J10	VSS	U5	AVDD33_PLL
A21	RGMII_RX_CLK	J11	VSS	U19	AVSS_USB
A22	VSS	J12	VSS	U20	USB_REXT
B1	DDR3_CS1_N	J13	VSS	U21	USB_DM
B2	DDR3_ODT_1	J14	VSS	U22	USB_DP
B3	DDR3_RAS_N	J15	VDD_MEDIA	V1	VSS
B4	DDR3_A3	J19	SDIO1_CWPR	V2	VSS
B5	DDR3_A2	J20	SDIO1_CARD_DETECT	V3	SAR_ADC_CH0
B6	DDR3_RESET_N	J21	SDIO1_CARD_POWER_EN	V4	SAR_ADC_CH1
B7	DDR3_A13	J22	SDIO1_CDATA1	V5	AVSS_RTC
B8	DDR3_CLK1_N	K1	NF_RDY0	V6	DVDD3318_SENSOR

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Position	Pin Name	Position	Pin Name	Position	Pin Name
B9	VSS	K2	NF_RDY1	V8	DVDD3318_VI
B10	DDR3_CLK0_P	K3	NF_DQ3	V10	AVSS_MIPI
B11	VSS	K4	NF_DQ2	V11	AVDD18_MIPI
B12	DDR3_DM0	K5	VSS	V12	AVDD18_MIPI
B13	DDR3_DQS1_P	K8	VSS	V13	AVSS_MIPI
B14	VSS	K9	VSS	V15	VSS
B15	DDR3_DQS0_P	K10	VSS	V16	DVDD33
B16	DDR3_DQ12	K11	VSS	V17	DVDD33
B17	VSS	K12	VSS	V18	VSS
B18	RGMII_RX_DV	K13	VSS	V19	USB_PWREN
B19	MDCK	K14	VSS	V20	PWM0
B20	VSS	K15	VDD	V21	USB_OVRCUR
B21	RGMII_TXD0	K18	SDIO1_VOUT	V22	UART2_TXD
B22	RGMII_TX_CLK	K19	SDIO1_CDATA3	W1	RTC_XOUT
C1	DDR3_DQ22 (not supported for the Hi3516D)	K20	SDIO1_CDATA0	W2	RTC_XIN
C2	DDR3_DQ20 (not supported for the Hi3516D)	K21	SDIO1_CCMD	W3	VSS
C3	DDR3_A6	K22	SDIO1_CCLK_OUT	W4	VI_HS
C4	DDR3_WE_N	L1	NF_CSN0	W5	VI_DAT13
C5	DDR3_A1	L2	NF_REN	W6	VI_DAT15
C6	DDR3_A10	L3	NF_DQ4	W7	VI_DAT7
C7	DDR3_A12	L4	NF_DQ1	W8	VI_DAT11
C8	DDR3_CS0_N	L5	DVDD33	W9	MIPI0_D3M
C9	DDR3_A4	L8	VDD	W10	MIPI0_CKP
C10	DDR3_DQ5	L9	VSS	W11	AVSS_MIPI
C11	DDR3_DQ3	L10	VSS	W12	MIPI1_D1P
C12	DDR3_DQ8	L11	VSS	W13	MIPI1_CKM
C13	DDR3_DQ2	L12	VSS	W14	AVSS_MIPI
C14	DDR3_DQ4	L13	VSS	W15	SHUTTER_TRIG

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Position	Pin Name	Position	Pin Name	Position	Pin Name
C15	DDR3_DQ9	L14	VSS	W16	SPI1_SDI
C16	DDR3_DQ13	L15	VSS	W17	VSS
C18	RGMII_RXD1	L18	DVDD18_SDIO	W18	JTAG_TDO
C19	RGMII_TX_EN	L19	SDIO1_CDATA2	W19	PWM1
C20	RGMII_TXD2	L20	SDIO0_CDATA2	W20	UART1_CTSN
C21	RGMII_TXD1	L21	SDIO0_CDATA1	W21	UART0_RXD
C22	VO_DAT15	L22	SDIO0_CCLK_OUT	W22	UART1_TXD
D1	DDR3_DQ25 (not supported for the Hi3516D)	M1	NF_CLE	Y1	GPIO0_0
D2	DDR3_DQ23 (not supported for the Hi3516D)	M2	NF_CSN1	Y2	SPI0_SDO
D3	DDR3_DQ17 (not supported for the Hi3516D)	M3	NF_DQ5	Y3	SPI0_CSN
D4	DDR3_A8	M4	NF_DQ6	Y4	VI_DAT10
D5	DDR3_A14	M5	DVDD33	Y5	VI_DAT12
D6	DDR3_A11	M8	VDD	Y6	VI_DAT14
D7	DDR3_CKE	M9	VSS	Y7	VI_DAT9
D8	DDR3_BA2	M10	VSS	Y8	AVSS_MIPI
D9	DDR3_BA1	M11	VSS	Y9	MIPI0_D3P
D10	DDR3_ODT_0	M12	VSS	Y10	MIPI0_CKM
D11	DDR3_DQ7	M13	VSS	Y11	AVSS_MIPI
D12	DDR3_DQ1	M14	VSS	Y12	MIPI1_D1M
D13	DDR3_DM1	M15	VDD_MEDIA	Y13	MIPI1_CKP
D14	DDR3_DQ14	M18	SDIO0_VOUT	Y14	AVSS_MIPI
D15	DDR3_DQ11	M19	SDIO0_CDATA0	Y15	FLASH_TRIG
D16	DDR3_DQ15	M20	SDIO0_CCMD	Y16	SPI1_SDO
D17	VSS	M21	SDIO0_CDATA3	Y17	SPI1_CSN0
D18	MDIO	M22	SDIO0_CWPR	Y18	JTAG_TCK
D19	RGMII_TXD3	N1	NF_WEN	Y19	UART1_RTSN
D20	GPIO0_1	N2	NF_ALE	Y20	GPIO0_4

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Position	Pin Name	Position	Pin Name	Position	Pin Name
D21	VO_DAT13	N3	NF_DQ0	Y21	UART0_TXD
D22	VO_DAT12	N4	NF_DQ7	Y22	UART1_RXD
E1	DDR3_DQS2_P (not supported for the Hi3516D)	N5	VSS	AA1	SENSOR_CLK
E2	DDR3_DQS2_N (not supported for the Hi3516D)	N8	VDD	AA2	SPI0_SDI
E3	DDR3_DQ21 (not supported for the Hi3516D)	N9	VSS	AA3	VI_DAT0
E4	DDR3_DQ19 (not supported for the Hi3516D)	N10	VSS	AA4	VI_DAT2
E5	VSS	N11	VSS	AA5	VI_DAT4
E6	VDDIO_DDR	N12	VSS	AA6	VSS
E7	VSS	N13	VSS	AA7	VI_CLK
E8	AVDD_DDRPLL2	N14	VSS	AA8	AVSS_MIPI
E9	VDDIO_DDR	N15	VDD_MEDIA	AA9	MIPI0_D1P
E10	VDDIO_CK_DDR	N18	AVDD33_AC	AA10	MIPI0_D0P
E11	AVDD_DDRPLL3	N19	SDIO0_CARD_DETECT	AA11	MIPI0_D2P
E12	VDDIO_DDR	N20	SDIO0_CARD_POWER_EN	AA12	MIPI1_D3M
E13	VDDIO_DDR	N21	AVSS_AC	AA13	MIPI1_D0M
E14	VSS	N22	AVSS_AC	AA14	MIPI1_D2M
E17	DVDDIO_RGMII	P1	SFC_CLK	AA15	AVSS_MIPI
E18	VSS	P2	SFC_WP_IO2	AA16	SPI1_SCLK
E19	EPHY_CLK	P3	SFC_SOI_IO1	AA17	UART2_RXD
E20	VO_DAT14	P4	RSTN	AA18	VSS
E21	VO_DAT11	P5	AVDD_EFUSE	AA19	JTAG_TDI
E22	VO_DAT9	P8	VDD_CPU	AA20	I2C2_SDA
F1	VSS	P9	VSS	AA21	PWM3
F2	VSS	P10	VSS	AA22	PWM2
F3	DDR3_DQ18 (not supported for the	P11	VSS	AB1	VSS

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Position	Pin Name	Position	Pin Name	Position	Pin Name
	Hi3516D)				
F4	DDR3_DM3 (not supported for the Hi3516D)	P12	VSS	AB2	SPI0_SCLK
F5	VDDIO_DDR	P13	VSS	AB3	VI_VS
F18	DVDD33	P14	VSS	AB4	VI_DAT1
F19	VO_DAT8	P15	VDD	AB5	VI_DAT3
F20	VO_DAT10	P18	AVDD33_VDAC	AB6	VI_DAT5
F21	VO_DAT7	P19	AVSS_AC	AB7	VI_DAT6
F22	VO_DAT5	P20	AVSS_AC	AB8	VI_DAT8
G1	DDR3_DQS3_N (not supported for the Hi3516D)	P21	AC_LINER	AB9	MIPI0_D1M
G2	DDR3_DQS3_P (not supported for the Hi3516D)	P22	AC_LINEL	AB10	MIPI0_D0M
G3	DDR3_DQ16 (not supported for the Hi3516D)	R1	VSS	AB11	MIPI0_D2M
G4	DDR3_DQ31 (not supported for the Hi3516D)	R2	SFC_SIO_IO0	AB12	MIPI1_D3P
G5	VDDIO_DDR	R3	SFC_CSN1	AB13	MIPI1_D0P
G18	DVDD33	R4	SFC_HOLD_IO3	AB14	MIPI1_D2P
G19	VO_DAT3	R5	AVDD11_PLL	AB15	AVSS_MIPI
G20	VO_DAT6	R8	VDD_CPU	AB16	GPIO0_3
G21	VO_DAT4	R9	VDD_CPU	AB17	JTAG_TRSTN
G22	VO_CLK	R10	VDD	AB18	GPIO0_2
H1	DDR3_DQ30 (not supported for the Hi3516D)	R11	VDD	AB19	JTAG_TMS
H2	DDR3_DQ28 (not supported for the Hi3516D)	R12	VSS	AB20	IR_IN
H3	DDR3_DM2 (not supported for the Hi3516D)	R13	VDD_MEDIA	AB21	I2C2_SCL
H4	DDR3_DQ27 (not	R14	VDD_MEDIA	AB22	VSS

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Position	Pin Name	Position	Pin Name	Position	Pin Name
	supported for the Hi3516D)				
H8	VDD_DDR	R15	VDD		

2.2 Pin Description

2.2.1 Pin Types

Table 2-4 describes the I/O pin types.

Table 2-4 I/O types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down
I_{SPU}	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{SPD}/O	Bidirectional signal with Schmitt trigger, input pull-down
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply

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I/O	Description
G	Ground (GND)

2.2.2 Pin Details

ACODEC Pins

Table 2-5 describes audio coder/decoder (ACODEC) pins.

Table 2-5 ACODEC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P22	AC_LINE L	I	None	None	Audio-left channel input
P21	AC_LINE R	I	None	None	Audio-right channel input
R22	AC_MICB IAS	I/O	None	2.1	Audio input microphone bias
R19	AC_OUTL	O	None	None	Audio-left channel output
R20	AC_OUT R	O	None	None	Audio-right channel output
R21	AC_VREF	P	None	1.65	Audio reference source. It is recommended that this pin connect to a 10 μF external capacitor and a 100 nF ceramic capacitor with low equivalent series resistance (ESR) in parallel and then connect to GND. The 100 nF capacitor should be placed as close as possible to this pin.
N18	AVDD33_ AC	P	None	3.3	Analog power of the audio interface
N21 N22 P19 P20	AVSS_AC	G	None	None	Analog GND of the audio interface

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DDR Pins

Table 2-6 describes double data rate (DDR) pins.

Table 2-6 DDR pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A7	DDR3_A0	I/O	None	1.5/1.35	Address signal 0 of the DDR (synchronous dynamic random access memory SDRAM)
C5	DDR3_A1	I/O	None	1.5/1.35	Address signal 1 of the DDR SDRAM
B5	DDR3_A2	I/O	None	1.5/1.35	Address signal 2 of the DDR SDRAM
B4	DDR3_A3	I/O	None	1.5/1.35	Address signal 3 of the DDR SDRAM
C9	DDR3_A4	I/O	None	1.5/1.35	Address signal 4 of the DDR SDRAM
A4	DDR3_A5	I/O	None	1.5/1.35	Address signal 5 of the DDR SDRAM
C3	DDR3_A6	I/O	None	1.5/1.35	Address signal 6 of the DDR SDRAM
A5	DDR3_A7	I/O	None	1.5/1.35	Address signal 7 of the DDR SDRAM
D4	DDR3_A8	I/O	None	1.5/1.35	Address signal 8 of the DDR SDRAM
A6	DDR3_A9	I/O	None	1.5/1.35	Address signal 9 of the DDR SDRAM
C6	DDR3_A10	I/O	None	1.5/1.35	Address signal 10 of the DDR SDRAM
D6	DDR3_A11	I/O	None	1.5/1.35	Address signal 11 of the DDR SDRAM
C7	DDR3_A12	I/O	None	1.5/1.35	Address signal 12 of the DDR SDRAM
B7	DDR3_A13	I/O	None	1.5/1.35	Address signal 13 of the DDR SDRAM
D5	DDR3_A14	I/O	None	1.5/1.35	Address signal 14 of the DDR SDRAM
A3	DDR3_BA0	I/O	None	1.5/1.35	Bank address signal 0 of the DDR SDRAM

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D9	DDR3_BA1	I/O	None	1.5/1.35	Bank address signal 1 of the DDR SDRAM
D8	DDR3_BA2	I/O	None	1.5/1.35	Bank address signal 2 of the DDR SDRAM
A2	DDR3_CAS_N	I/O	None	1.5/1.35	Column address select signal of the DDR SDRAM
D7	DDR3_CKE	I/O	None	1.5/1.35	Clock enable signal of the DDR SDRAM
A10	DDR3_CLK0_N	I/O	None	1.5/1.35	Negative differential clock 0 of the DDR SDRAM
B10	DDR3_CLK0_P	I/O	None	1.5/1.35	Positive differential clock 0 of the DDR SDRAM
B8	DDR3_CLK1_N	I/O	None	1.5/1.35	Negative differential clock 1 of the DDR SDRAM
A8	DDR3_CLK1_P	I/O	None	1.5/1.35	Positive differential clock 1 of the DDR SDRAM
C8	DDR3_CS0_N	I/O	None	1.5/1.35	Chip select 0 (CS0) of the DDR SDRAM (corresponding to lower-16-bit DQ[15:0])
B1	DDR3_CS1_N	I/O	None	1.5/1.35	CS1 of the DDR SDRAM (corresponding to upper-16-bit DQ[31:16]). The source of DDR3_CS1_N is the same as that of DDR3_CS0_N.
B12	DDR3_DM0	I/O	None	1.5/1.35	Data mask signal 0 of the DDR SDRAM
D13	DDR3_DM1	I/O	None	1.5/1.35	Data mask signal 1 of the DDR SDRAM
H3	DDR3_DM2	I/O	None	1.5/1.35	Data mask signal 2 of the DDR SDRAM (not supported for the Hi3516D, NC)
F4	DDR3_DM3	I/O	None	1.5/1.35	Data mask signal 3 of the DDR SDRAM (not supported for the Hi3516D, NC)
A16	DDR3_DQ0	I/O	None	1.5/1.35	Data line 0 of the DDR SDRAM

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D12	DDR3_DQ1	I/O	None	1.5/1.35	Data line 1 of the DDR SDRAM
C13	DDR3_DQ2	I/O	None	1.5/1.35	Data line 2 of the DDR SDRAM
C11	DDR3_DQ3	I/O	None	1.5/1.35	Data line 3 of the DDR SDRAM
C14	DDR3_DQ4	I/O	None	1.5/1.35	Data line 4 of the DDR SDRAM
C10	DDR3_DQ5	I/O	None	1.5/1.35	Data line 5 of the DDR SDRAM
A17	DDR3_DQ6	I/O	None	1.5/1.35	Data line 6 of the DDR SDRAM
D11	DDR3_DQ7	I/O	None	1.5/1.35	Data line 7 of the DDR SDRAM
C12	DDR3_DQ8	I/O	None	1.5/1.35	Data line 8 of the DDR SDRAM
C15	DDR3_DQ9	I/O	None	1.5/1.35	Data line 9 of the DDR SDRAM
A12	DDR3_DQ10	I/O	None	1.5/1.35	Data line 10 of the DDR SDRAM
D15	DDR3_DQ11	I/O	None	1.5/1.35	Data line 11 of the DDR SDRAM
B16	DDR3_DQ12	I/O	None	1.5/1.35	Data line 12 of the DDR SDRAM
C16	DDR3_DQ13	I/O	None	1.5/1.35	Data line 13 of the DDR SDRAM
D14	DDR3_DQ14	I/O	None	1.5/1.35	Data line 14 of the DDR SDRAM
D16	DDR3_DQ15	I/O	None	1.5/1.35	Data line 15 of the DDR SDRAM
G3	DDR3_DQ16	I/O	None	1.5/1.35	Data line 16 of the DDR SDRAM (not supported for the Hi3516D, NC)
D3	DDR3_DQ17	I/O	None	1.5/1.35	Data line 17 of the DDR SDRAM (not supported for the Hi3516D, NC)
F3	DDR3_DQ18	I/O	None	1.5/1.35	Data line 18 of the DDR SDRAM (not supported for

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					the Hi3516D, NC)
E4	DDR3_DQ19	I/O	None	1.5/1.35	Data line 19 of the DDR SDRAM (not supported for the Hi3516D, NC)
C2	DDR3_DQ20	I/O	None	1.5/1.35	Data line 20 of the DDR SDRAM (not supported for the Hi3516D, NC)
E3	DDR3_DQ21	I/O	None	1.5/1.35	Data line 21 of the DDR SDRAM (not supported for the Hi3516D, NC)
C1	DDR3_DQ22	I/O	None	1.5/1.35	Data line 22 of the DDR SDRAM (not supported for the Hi3516D, NC)
D2	DDR3_DQ23	I/O	None	1.5/1.35	Data line 23 of the DDR SDRAM (not supported for the Hi3516D, NC)
J3	DDR3_DQ24	I/O	None	1.5/1.35	Data line 24 of the DDR SDRAM (not supported for the Hi3516D, NC)
D1	DDR3_DQ25	I/O	None	1.5/1.35	Data line 25 of the DDR SDRAM (not supported for the Hi3516D, NC)
J1	DDR3_DQ26	I/O	None	1.5/1.35	Data line 26 of the DDR SDRAM (not supported for the Hi3516D, NC)
H4	DDR3_DQ27	I/O	None	1.5/1.35	Data line 27 of the DDR SDRAM (not supported for the Hi3516D, NC)
H2	DDR3_DQ28	I/O	None	1.5/1.35	Data line 28 of the DDR SDRAM (not supported for the Hi3516D, NC)
J4	DDR3_DQ29	I/O	None	1.5/1.35	Data line 29 of the DDR SDRAM (not supported for the Hi3516D, NC)
H1	DDR3_DQ30	I/O	None	1.5/1.35	Data line 30 of the DDR SDRAM (not supported for the Hi3516D, NC)
G4	DDR3_DQ31	I/O	None	1.5/1.35	Data line 31 of the DDR SDRAM (not supported for the Hi3516D, NC)

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A15	DDR3_DQS0_N	I/O	None	1.5/1.35	Negative data strobe signal 0 of the DDR, corresponding to DQ[7:0]
B15	DDR3_DQS0_P	I/O	None	1.5/1.35	Positive data strobe signal 0 of the DDR, corresponding to DQ[7:0]
A13	DDR3_DQS1_N	I/O	None	1.5/1.35	Negative data strobe signal 1 of the DDR, corresponding to DQ[15:8]
B13	DDR3_DQS1_P	I/O	None	1.5/1.35	Positive data strobe signal 1 of the DDR, corresponding to DQ[15:8]
E2	DDR3_DQS2_N	I/O	None	1.5/1.35	Negative data strobe signal 2 of the DDR, corresponding to DQ[23:16] (not supported for the Hi3516D, NC)
E1	DDR3_DQS2_P	I/O	None	1.5/1.35	Positive data strobe signal 2 of the DDR, corresponding to DQ[23:16] (not supported for the Hi3516D, NC)
G1	DDR3_DQS3_N	I/O	None	1.5/1.35	Negative data strobe signal 3 of the DDR, corresponding to DQ[31:24] (not supported for the Hi3516D, NC)
G2	DDR3_DQS3_P	I/O	None	1.5/1.35	Positive data strobe signal 3 of the DDR, corresponding to DQ[31:24] (not supported for the Hi3516D, NC)
D10	DDR3_ODT_0	I/O	None	1.5/1.35	On-die termination (ODT) signal of DDR0 (corresponding to lower-16-bit DQ[15:0])
B2	DDR3_ODT_1	I/O	None	1.5/1.35	ODT signal of DDR1 (corresponding to upper-16-bit DQ[31:16]). The source of DDR3_ODT_1 is the same as that of DDR3_ODT_0.
B3	DDR3_RAS_N	I/O	None	1.5/1.35	Row address select signal of the DDR SDRAM
B6	DDR3_RESET_N	I/O	None	1.5/1.35	Reset signal of the DDR3 SDRAM

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
C4	DDR3_WE_N	I/O	None	1.5/1.35	Write enable signal of the DDR SDRAM
J2	DDR3_ZQ	I/O	None	None	Pin connected to an external reference resistor for calibrating the on-chip DDR I/O ZQ. This pin is different from the ZQ pin of the DDR.
E10	VDDIO_CK_DDR	P	None	1.5/1.35	DDR I/O power
E6 E9 E12 E13 F5 G5	VDDIO_DDR	P	None	1.5/1.35	DDR I/O power
J5	AVDD_DDR PLL1	P	None	3.3	Analog power of the DDR phase-locked loop (PLL)
E8	AVDD_DDR PLL2	P	None	3.3	Analog power of the DDR PLL
E11	AVDD_DDR PLL3	P	None	3.3	Analog power of the DDR PLL

EPHY Pin

Table 2-7 describes the external physical layer (EPHY) pin.

Table 2-7 EPHY pin

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E19	EPHY_CLK	I/O	Configurable (for details, see the PADCTRL_REG102 register)	3.3/2.5/1.8	**Function 0: GPIO14_4** General-purpose input/output (GPIO) **Function 1: EPHY_CLK** Working clock of the EPHY

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MDIO Pins

Table 2-8 describes management data input/output (MDIO) pins.

Table 2-8 MDIO pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
B19	MDCK	I/O	Configurable (for details, see the PADCTRL_REG103 register)	3.3/2.5/1.8	**Function 0: GPIO14_5** GPIO **Function 1: MDCK** MDIO clock
D18	MDIO	I/O	Configurable (for details, see the PADCTRL_REG104 register)	3.3/2.5/1.8	**Function 0: GPIO14_6** GPIO **Function 1: MDIO** MDIO data

RGMII Pins

The Ethernet port supports the reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), and media independent interface (MII) modes. Table 2-9 describes the functions of RGMII pins in each mode.

Table 2-9 Functions of RGMII pins in three modes

Pin Name	Function in RGMII Mode	Function in RMII Mode	Function in MII Mode
RGMII_RX_CLK	Receive (RX) clock	None	RX clock
RGMII_RXD0	RX data 0	RX data 0	RX data 0
RGMII_RXD1	RX data 1	RX data 1	RX data 1
RGMII_RXD2	RX data 2	None	RX data 2
RGMII_RXD3	RX data 3	None	RX data 3
RGMII_RX_DV	RX data validity indicator	RX data validity indicator/carrier detection	RX data validity indicator
RGMII_TX_CLK	Transmit (TX) clock	Reference clock	TX clock
RGMII_TXD0	TX data 0	TX data 0	TX data 0
RGMII_TXD1	TX data 1	TX data 1	TX data 1

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Pin Name	Function in RGMII Mode	Function in RMII Mode	Function in MII Mode
RGMII_TXD2	TX data 2	None	TX data 2
RGMII_TXD3	TX data 3	None	TX data 3
RGMII_TX_EN	TX data enable	TX data enable	TX data enable

Table 2-10 describes RGMII pins.

Table 2-10 RGMII pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A21	RGMII_RX_CLK	I/O	Configurable (for details, see the PADCTRL_REG111 register)	3.3/2.5/1.8	**Function 0: GPIO4_5** GPIO **Function 1: RGMII_RX_CLK** RGMII mode: 125 MHz RX clock, valid at the rising and falling edges MII mode: RX clock
B18	RGMII_RX_DV	I/O	Configurable (for details, see the PADCTRL_REG112 register)	3.3/2.5/1.8	**Function 0: GPIO4_6** GPIO **Function 1: RGMII_RX_DV** RGMII mode: RX data validity MII mode: RX data validity RMII mode: RX data validity or carrier detection signal
A18	RGMII_RXD0	I/O	Configurable (for details, see the PADCTRL_REG113 register)	3.3/2.5/1.8	**Function 0: GPIO4_7** GPIO **Function 1: RGMII_RXD0** RGMII/RMII/MII mode: RX data 0
C18	RGMII_RXD1	I/O	Configurable (for details, see the PADCTRL_REG114 register)	3.3/2.5/1.8	**Function 0: GPIO1_3** GPIO **Function 1: RGMII_RXD1** RGMII/RMII/MII mode: RX data 1
A19	RGMII_R	I/O	Configurable (for details,	3.3/2.5/1.8	**Function 0: GPIO1_4**

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
	XD2		see the PADCTRL_REG115 register)		GPIO **Function 1: RGMII_RXD2** RGMII/MII mode: RX data 2
A20	RGMII_RXD3	I/O	Configurable (for details, see the PADCTRL_REG116 register)	3.3/2.5/1.8	**Function 0: GPIO1_5** GPIO **Function 1: RGMII_RXD3** RGMII/MII mode: RX data 3
B22	RGMII_TX_CLK	I/O	Configurable (for details, see the PADCTRL_REG106 register)	3.3/2.5/1.8	**Function 0: GPIO4_0** GPIO **Function 1: RGMII_TX_CLK** RGMII mode: 125 MHz TX clock, valid at the rising and falling edges **Function 2: RMII_CLK** RMII mode: reference clock MII mode: TX clock
C19	RGMII_TX_EN	I/O	Configurable (for details, see the PADCTRL_REG105 register)	3.3/2.5/1.8	**Function 0: GPIO14_7** GPIO **Function 1: RGMII_TX_EN** RGMII/RMII/MII mode: TX enable
B21	RGMII_TXD0	I/O	Configurable (for details, see the PADCTRL_REG107 register)	3.3/2.5/1.8	**Function 0: GPIO4_1** GPIO **Function 1: RGMII_TXD0** RGMII/RMII/MII mode: TX data 0
C21	RGMII_TXD1	I/O	Configurable (for details, see the PADCTRL_REG108 register)	3.3/2.5/1.8	**Function 0: GPIO4_2** GPIO **Function 1: RGMII_TXD1** RGMII/RMII/MII mode: TX data 1
C20	RGMII_TXD2	I/O	Configurable (for details, see the	3.3/2.5/1.8	**Function 0: GPIO4_3** GPIO

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			PADCTRL_REG109 register)		**Function 1: RGMII_TXD2** RGMII/MII mode: TX data 2
D19	RGMII_TXD3	I/O	Configurable (for details, see the PADCTRL_REG110 register)	3.3/2.5/1.8	**Function 0: GPIO4_4** GPIO **Function 1: RGMII_TXD3** RGMII/MII mode: TX data 3

Sensor Pins

Table 2-11 describes sensor pins.

Table 2-11 Sensor pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA1	SENSOR_CLK	I/O	Configurable (for details, see the PADCTRL_REG0 register)	3.3/1.8	**Function 0: GPIO0_5** GPIO **Function 1: SENSOR_CLK** Sensor working clock
Y15	FLASH_TRIG	I/O	Configurable (for details, see the PADCTRL_REG1 register)	3.3	**Function 0: GPIO0_6** GPIO **Function 1: FLASH_TRIG** Camera flash control **Function 2: SPI1_CSN1** Serial peripheral interface 1 (SPI1) CS1
W15	SHUTTER_TRIG	I/O	Configurable (for details, see the PADCTRL_REG2 register)	3.3	**Function 0: GPIO0_7** GPIO **Function 1: SHUTTER_TRIG** Shutter control **Function 2: SPI1_CSN2** SPI1 CS2

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GPIO Pins

Table 2-12 describes GPIO pins.

Table 2-12 GPIO pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y1	GPIO0_0	I/O	Configurable (for details, see the PADCTRL_REG60 register)	3.3/1.8	**Function 0: SENSOR_RSTN** Sensor reset signal **Function 1: GPIO0_0** GPIO **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
D20	GPIO0_1	I/O	Configurable (for details, see the PADCTRL_REG61 register)	3.3/2.5/1.8	**Function 0: GPIO0_1** GPIO **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
AB18	GPIO0_2	I/O	Configurable (for details, see the PADCTRL_REG62 register)	3.3	**Function 0: GPIO0_2** GPIO **Function 1: PWM5** Pulse width modulation (PWM) output 5 **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
AB16	GPIO0_3	I/O	Configurable (for details, see the PADCTRL_REG63 register)	3.3	**Function 0: GPIO0_3** GPIO **Function 1: PWM6** PWM output 6 **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y20	GPIO0_4	I/O	Configurable (for details, see the PADCTRL_REG64 register)	3.3	**Function 0: GPIO0_4** GPIO **Function 1: PWM7** PWM output 7 **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

I²C2 Pins

Table 2-13 describes inter-integrated circuit 2 (I^2C2) pins.

Table 2-13 I^2C2 pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AB21	I2C2_SCL	I/O	Configurable (for details, see the PADCTRL_REG29 register)	3.3	**Function 0: GPIO9_1** GPIO **Function 1: I2C2_SCL** I^2C2 bus clock
AA20	I2C2_SDA	I/O	Configurable (for details, see the PADCTRL_REG28 register)	3.3	**Function 0: GPIO9_0** GPIO **Function 1: I2C2_SDA** I^2C2 bus data/address

IR Pin

Table 2-14 describes the infrared (IR) pin.

Table 2-14 IR pin

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AB20	IR_IN	I_{PU}/O	Configurable (for details, see the PADCTRL_REG44 register)	3.3	**Function 0: GPIO10_5** GPIO **Function 1: IR_IN** Infrared input **Function 2: PWM4** PWM output 4

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JTAG Pins

Table 2-15 describes Joint Test Action Group (JTAG) pins.

Table 2-15 JTAG pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T2	JTAG_EN	I_{PD}	Configurable (for details, see the PADCTRL_REG38 register)	3.3	JTAG pin enable 0: disabled (other functions for the JTAG pin) 1: enabled
Y18	JTAG_TCK	I_{PD}/O	Configurable (for details, see the PADCTRL_REG40 register)	3.3	**Function 0: GPIO10_1** GPIO (valid only when the input of the JTAG_EN pin is 0) **Function 1: JTAG_TCK** JTAG clock **Function 2: I2S_BCLK_TX** TX clock of the inter-IC sound (I^2S) or pulse code modulation (PCM) interface
AA19	JTAG_TDI	I_{PU}/O	Configurable (for details, see the PADCTRL_REG43 register)	3.3	**Function 0: GPIO10_4** GPIO **Function 1: JTAG_TDI** JTAG data input **Function 2: I2S_SD_TX** TX data output of the I^2S or PCM interface
W18	JTAG_TDO	I/O	Configurable (for details, see the PADCTRL_REG42 register)	3.3	**Function 0: GPIO10_3** GPIO **Function 1: JTAG_TDO** JTAG data output **Function 2: I2S_SD_RX** RX data input of the I^2S or PCM interface
AB19	JTAG_TMS	I_{PU}/O	Configurable (for details, see the PADCTRL_REG41 register)	3.3	**Function 0: GPIO10_2** GPIO **Function 1: JTAG_TMS** JTAG mode select input or data output for software trace. The modes are controlled by using the CPU. **Function 2: I2S_WS_TX** I^2S TX audio channel select signal or

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					PCM TX frame sync signal
AB17	JTAG_TRSTN	I_{PD}/O	Configurable (for details, see the PADCTRL_REG39 register)	3.3	**Function 0: GPIO10_0** GPIO **Function 1: JTAG_TRSTN** JTAG reset signal **Function 2: I2S_MCLK** Main clock of the I^2S or PCM interface. It can act as the main clock of the ACODEC.

NOTE

Functions 0 and 2 are valid only when the input of the JTAG_EN pin is 0, and function 1 is valid only when the input of the JTAG_EN pin is 1.

MIPI Pins

The mobile industry processor interface (MIPI) supports the differential and single-ended modes. Table 2-16 describes the functions of MIPI pins in each mode.

Table 2-16 Functions of MIPI pins in two modes

Pin Name	Function in Differential Mode	Function in Single-Ended Mode
MIPI0_CKM	MIPI0 differential clock	VI_DAT4
MIPI0_CKP	MIPI0 differential clock	VI_DAT5
MIPI0_D0M	MIPI0 differential data 0	VI_DAT0
MIPI0_D0P	MIPI0 differential data 0	VI_DAT1
MIPI0_D1M	MIPI0 differential data 1	VI_HS
MIPI0_D1P	MIPI0 differential data 1	VI_VS
MIPI0_D2M	MIPI0 differential data 2	VI_DAT6
MIPI0_D2P	MIPI0 differential data 2	VI_DAT7
MIPI0_D3M	MIPI0 differential data 3	VI_DAT2
MIPI0_D3P	MIPI0 differential data 3	VI_DAT3
MIPI1_CKM	MIPI1 differential clock	VI_DAT13
MIPI1_CKP	MIPI1 differential clock	VI_DAT12
MIPI1_D0M	MIPI1 differential data 0	VI_DAT15
MIPI1_D0P	MIPI1 differential data 0	VI_DAT14

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Pin Name	Function in Differential Mode	Function in Single-Ended Mode
MIPI1_D1M	MIPI1 differential data 1	VI_DAT11
MIPI1_D1P	MIPI1 differential data 1	VI_DAT10
MIPI1_D2M	MIPI1 differential data 2/	None
MIPI1_D2P	MIPI1 differential data 2	VI_CLK
MIPI1_D3M	MIPI1 differential data 3	VI_DAT9
MIPI1_D3P	MIPI1 differential data 3	VI_DAT8

Table 2-17 describes MIPI pins.

Table 2-17 MIPI pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y10	MIPI0_CKM	I	None	3.3/1.8	VI_DAT4 in single-ended mode or differential clock of MIPI0
W10	MIPI0_CKP	I	None	3.3/1.8	VI_DAT5 in single-ended mode or differential clock of MIPI0
AB10	MIPI0_D0M	I	None	3.3/1.8	VI_DAT0 in single-ended mode or differential data 0 of MIPI0
AA10	MIPI0_D0P	I	None	3.3/1.8	VI_DAT1 in single-ended mode or differential data 0 of MIPI0
AB9	MIPI0_D1M	I	None	3.3/1.8	VI_HS in single-ended mode or differential data 1 of MIPI0
AA9	MIPI0_D1P	I	None	3.3/1.8	VI_VS in single-ended mode or differential data 1 of MIPI0
AB11	MIPI0_D2M	I	None	3.3/1.8	VI_DAT6 in single-ended mode or differential data 2 of MIPI0
AA11	MIPI0_D2P	I	None	3.3/1.8	VI_DAT7 in single-ended mode or

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					differential data 2 of MIPI0
W9	MIPI0_D3M	I	None	3.3/1.8	VI_DAT2 in single-ended mode or differential data 3 of MIPI0
Y9	MIPI0_D3P	I	None	3.3/1.8	VI_DAT3 in single-ended mode or differential data 3 of MIPI0
W13	MIPI1_CKM	I	None	3.3/1.8	VI_DAT13 in single-ended mode or differential clock of MIPI1
Y13	MIPI1_CKP	I	None	3.3/1.8	VI_DAT12 in single-ended mode or differential clock of MIPI1
AA13	MIPI1_D0M	I	None	3.3/1.8	VI_DAT15 in single-ended mode or differential data 0 of MIPI1
AB13	MIPI1_D0P	I	None	3.3/1.8	VI_DAT14 in single-ended mode or differential data 0 of MIPI1
Y12	MIPI1_D1M	I	None	3.3/1.8	VI_DAT11 in single-ended mode or differential data 1 of MIPI1
W12	MIPI1_D1P	I	None	3.3/1.8	VI_DAT10 in single-ended mode or differential data 1 of MIPI1
AA14	MIPI1_D2M	I	None	3.3/1.8	MIPI1 differential data 2
AB14	MIPI1_D2P	I	None	3.3/1.8	VI_CLK in single-ended mode or differential data 2 of MIPI1
AA12	MIPI1_D3M	I	None	3.3/1.8	VI_DAT 9 in single-ended mode or differential data 3 of MIPI1

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AB12	MIPI1_D3P	I	None	3.3/1.8	VI_DAT 8 in single-ended mode or differential data 3 of MIPI1
V11 V12	AVDD18_MIPI	P	None	3.3/1.8	Analog power of the MIPI PHY
V10 V13 W11 W14 Y8 Y11 Y14 AA8 AA15 AB15	AVSS_MIPI	G	None	None	Analog GND of the MIPI PHY

CAUTION

As the VICAP supports only one video input, the video input paths of the MIPI PHY and VI pin are mutually exclusive (Only one sensor input is supported). The mipi_phy_mode register determines the video input path connected to the VICAP. See Figure 2-11.

Figure 2-11 Video input paths of the MIPI PHY and VI pin

VI Pins

Table 2-18describes video input (VI) pins.

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Table 2-18 VI pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA7	VI_CLK	I/O	Configurable (for details, see the PADCTRL_REG117 register)	3.3/1.8	**Function 0: GPIO15_0** GPIO **Function 1: VI_CLK** VI input clock
AA3	VI_DAT0	I/O	Configurable (for details, see the PADCTRL_REG135 register)	3.3/1.8	**Function 0: GPIO13_7** GPIO **Function 1: VI_DAT0** VI input data 0 **Function 3: PWM4** PWM output 4
AB4	VI_DAT1	I/O	Configurable (for details, see the PADCTRL_REG134 register)	3.3/1.8	**Function 0: GPIO13_6** GPIO **Function 1: VI_DAT1** VI input data 1
AA4	VI_DAT2	I/O	Configurable (for details, see the PADCTRL_REG133 register)	3.3/1.8	**Function 0: GPIO13_5** GPIO **Function 1: VI_DAT2** VI input data 2
AB5	VI_DAT3	I/O	Configurable (for details, see the PADCTRL_REG132 register)	3.3/1.8	**Function 0: GPIO13_4** GPIO **Function 1: VI_DAT3** VI input data 3
AA5	VI_DAT4	I/O	Configurable (for details, see the PADCTRL_REG131 register)	3.3/1.8	**Function 0: GPIO13_3** GPIO **Function 1: VI_DAT4** VI input data 4
AB6	VI_DAT5	I/O	Configurable (for details, see the PADCTRL_REG130 register)	3.3/1.8	**Function 0: GPIO13_2** GPIO **Function 1: VI_DAT5** VI input data 5
AB7	VI_DAT6	I/O	Configurable (for details, see the PADCTRL_REG129 register)	3.3/1.8	**Function 0: GPIO13_1** GPIO **Function 1: VI_DAT6** VI input data 6
W7	VI_DAT7	I/O	Configurable (for details, see the PADCTRL_REG128	3.3/1.8	**Function 0: GPIO13_0** GPIO

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			register)		**Function 1: VI_DAT7** VI input data 7
AB8	VI_DAT8	I/O	Configurable (for details, see the PADCTRL_REG127 register)	3.3/1.8	**Function 0: GPIO12_7** GPIO **Function 1: VI_DAT8** VI input data 8
Y7	VI_DAT9	I/O	Configurable (for details, see the PADCTRL_REG126 register)	3.3/1.8	**Function 0: GPIO12_6** GPIO **Function 1: VI_DAT9** VI input data 9 **Function 2: I2S_SD_RX** RX data input of the I^2S or PCM interface
Y4	VI_DAT10	I/O	Configurable (for details, see the PADCTRL_REG125 register)	3.3/1.8	**Function 0: GPIO12_5** GPIO **Function 1: VI_DAT10** VI input data 10 **Function 2: I2S_WS_RX** I^2S RX audio channel select signal or PCM TX frame sync signal
W8	VI_DAT11	I/O	Configurable (for details, see the PADCTRL_REG124 register)	3.3/1.8	**Function 0: GPIO12_4** GPIO **Function 1: VI_DAT11** VI input data 11 **Function 2: I2S_BCLK_RX** RX clock of the I^2S or PCM interface
Y5	VI_DAT12	I/O	Configurable (for details, see the PADCTRL_REG123 register)	3.3/1.8	**Function 0: GPIO12_3** GPIO **Function 1: VI_DAT12** VI input data 12 **Function 2: I2S_SD_TX** TX data output of the I2S or PCM interface
W5	VI_DAT13	I/O	Configurable (for details, see the PADCTRL_REG122 register)	3.3/1.8	**Function 0: GPIO12_2** GPIO **Function 1: VI_DAT13** VI input data 13

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 2: I2S_WS_TX I^2S TX audio channel select signal or PCM TX frame sync signal
Y6	VI_DAT14	I/O	Configurable (for details, see the PADCTRL_REG121 register)	3.3/1.8	**Function 0: GPIO12_1** GPIO **Function 1: VI_DAT14** VI input data 14 **Function 2: I2S_BCLK_TX** TX clock of I^2S or PCM interface
W6	VI_DAT15	I/O	Configurable (for details, see the PADCTRL_REG120 register)	3.3/1.8	**Function 0: GPIO12_0** GPIO **Function 1: VI_DAT15** VI input data 15 **Function 2: I2S_MCLK** Main clock of the I2S or PCM interface. It can act as the main clock of the ACODEC.
W4	VI_HS	I/O	Configurable (for details, see the PADCTRL_REG118 register)	3.3/1.8	**Function 0: GPIO15_1** GPIO **Function 1: VI_HS** VI input horizontal sync signal
AB3	VI_VS	I/O	Configurable (for details, see the PADCTRL_REG119 register)	3.3/1.8	**Function 0: GPIO15_2** GPIO **Function 1: VI_VS** VI input vertical sync signal

NFC Pins

Table 2-19 describes NAND flash controller (NFC) pins.

Table 2-19 NFC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
N2	NF_ALE	I/O	Configurable (for details, see the PADCTRL_REG94 register)	3.3	**Function 0: NF_ALE** Address latch signal of the NAND flash **Function 1: GPIO3_6** GPIO
M1	NF_CLE	I/O	Configurable (for details, see the	3.3	**Function 0: NF_CLE** Command latch signal of the

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			PADCTRL_REG93 register)		NAND flash **Function 1: GPIO3_5** GPIO
L1	NF_CSN0	I/O	Configurable (for details, see the PADCTRL_REG91 register)	3.3	**Function 0: NF_CSN0** CS0 of the NAND flash (active low) for mounting the NAND flash from which the system boots **Function 1: GPIO3_3** GPIO
M2	NF_CSN1	I/O	Configurable (for details, see the PADCTRL_REG92 register)	3.3	**Function 0: NF_CSN1** CS1 of the NAND flash, active low **Function 1: GPIO3_4** GPIO **Function 2: SFC_CSN0** CS0 of the SPI flash, active low
N3	NF_DQ0	I/O	Configurable (for details, see the PADCTRL_REG80 register)	3.3	**Function 0: NF_DQ0** Data bus 0 of the NAND flash **Function 1: GPIO5_0** GPIO
L4	NF_DQ1	I/O	Configurable (for details, see the PADCTRL_REG81 register)	3.3	**Function 0: NF_DQ1** Data bus 1 of the NAND flash **Function 1: GPIO5_1** GPIO
K4	NF_DQ2	I/O	Configurable (for details, see the PADCTRL_REG82 register)	3.3	**Function 0: NF_DQ2** Data bus 2 of the NAND flash **Function 1: GPIO5_2** GPIO
K3	NF_DQ3	I/O	Configurable (for details, see the PADCTRL_REG83 register)	3.3	**Function 0: NF_DQ3** Data bus 3 of the NAND flash **Function 1: GPIO5_3** GPIO
L3	NF_DQ4	I/O	Configurable (for details, see the PADCTRL_REG84 register)	3.3	**Function 0: NF_DQ4** Data bus 4 of the NAND flash **Function 1: GPIO5_4** GPIO
M3	NF_DQ5	I/O	Configurable (for	3.3	**Function 0: NF_DQ5**

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			details, see the PADCTRL_REG85 register)		Data bus 5 of the NAND flash **Function 1: GPIO5_5** GPIO
M4	NF_DQ6	I/O	Configurable (for details, see the PADCTRL_REG86 register)	3.3	**Function 0: NF_DQ6** Data bus 6 of the NAND flash **Function 1: GPIO5_6** GPIO
N4	NF_DQ7	I/O	Configurable (for details, see the PADCTRL_REG87 register)	3.3	**Function 0: NF_DQ7** Data bus 7 of the NAND flash **Function 1: GPIO5_7** GPIO
K1	NF_RDY0	I_{PU}/O	Configurable (for details, see the PADCTRL_REG88 register)	3.3	**Function 0: NF_RDY0** Status indicator signal 0 of the NAND flash 0: busy 1: idle **Function 1: GPIO3_0** GPIO
K2	NF_RDY1	I_{PU}/O	Configurable (for details, see the PADCTRL_REG89 register)	3.3	**Function 0: NF_RDY1** Status indicator signal 1 of the NAND flash 0: busy 1: idle **Function 1: GPIO3_1** GPIO
L2	NF_REN	I/O	Configurable (for details, see the PADCTRL_REG90 register)	3.3	**Function 0: NF_REN** Read enable signal of the NAND flash, active low **Function 1: GPIO3_2** GPIO
N1	NF_WEN	I/O	Configurable (for details, see the PADCTRL_REG95 register)	3.3	**Function 0: NF_WEN** Write enable signal of the NAND flash, active low **Function 1: GPIO3_7** GPIO

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SYS Pins

Table 2-20 describes system (SYS) pins.

Table 2-20 SYS pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T3	POR_SEL	I_{PD}	None	3.3	Reset select (valid only during power-on) 0: reset by the internal power-on-reset (POR) module 1: reset by the external reset pin
P4	RSTN	I_{PU}	None	3.3	System power-on reset input, active low
T1	TEST_MODE	I_{PD}	None	3.3	Mode select 0: functional mode 1: test mode
T4	WDG_RSTN	I/O	Configurable (for details, see the PADCTRL_REG47 register)	3.3	**Function 0: WDG_RSTN** Watchdog reset output, active low **Function 1: SYS_RSTN_OUT** System reset output. The reset valid time is about 130 ms. 0: reset 1: reset deasserted

PWM Pins

Table 2-21 describes PWM pins.

Table 2-21 PWM pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V20	PWM0	I/O	Configurable (for details, see the PADCTRL_REG96 register)	3.3	**Function 0: PWM0** PWM output 0 **Function 1: GPIO14_0** GPIO **Function 2: PMC_I2C_SCL** I^2C bus clock of the PMC for communicating with the external PMU
W19	PWM1	I/O	Configurable (for details, see the PADCTRL_RE	3.3	**Function 0: PWM1** PWM output 1 **Function 1: GPIO14_1**

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			G97 register)		GPIO **Function 2: PMC_I2C_SDA** I^2C bus data/address of the PMC for communicating with the external PMU
AA22	PWM2	I/O	Configurable (for details, see the PADCTRL_REG98 register)	3.3	**Function 0: PWM2** PWM output 2 **Function 1: GPIO14_2** GPIO
AA21	PWM3	I/O	Configurable (for details, see the PADCTRL_REG99 register)	3.3	**Function 0: PWM3** PWM output 3 **Function 1: GPIO14_3** GPIO

RTC Pins

Table 2-22 describes real-time clock (RTC) pins.

Table 2-22 RTC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W2	RTC_XIN	CIN	None	None	RTC crystal input
W1	RTC_XOUT	COUT	None	None	RTC crystal drive output
U3	AVDD_BAT	P	None	3.3	RTC external battery power
U4	AVDD33_RTC	P	None	3.3	RTC analog power
V5	AVSS_RTC	G	None	None	RTC analog GND

SAR_ADC Pins

Table 2-23 describes successive approximation register analog-to-digital converter (SAR_ADC) pins.

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Table 2-23 SAR_ADC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V3	SAR_ADC_CH0	I/O	Configurable (for details, see the PADCTRL_REG100 register)	3.3	**Function 0: SAR_ADC_CH0** LSADC channel 0 **Function 1: GPIO1_6** GPIO
V4	SAR_ADC_CH1	I/O	Configurable (for details, see the PADCTRL_REG101 register)	3.3	**Function 0: SAR_ADC_CH1** LSADC channel 1 **Function 1: GPIO1_7** GPIO

SDIO0 Pins

Table 2-24 describes secure digital input/output 0 (SDIO0) pins.

Table 2-24 SDIO0 pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
N19	SDIO0_CARD_DETECT	I/O	Configurable (for details, see the PADCTRL_REG53 register)	3.3	**Function 0: GPIO2_2** GPIO **Function 1: SDIO0_CARD_DETECT** SDIO0 card detection signal, active low **Function 2: I2S_WS_TX** I^2S TX audio channel select signal or PCM TX frame sync signal
N20	SDIO0_CARD_POWER_EN	I/O	Configurable (for details, see the PADCTRL_REG52 register)	3.3	**Function 0: GPIO2_1** GPIO **Function 1: SDIO0_CARD_POWER_EN** SDIO0 power enable signal. The value 1 indicates power-on. **Function 2: I2S_BCLK_TX** TX clock of I^2S or PCM interface
L22	SDIO0_CCLK_OUT	I/O	Configurable (for details, see the PADCTRL_REG51 register)	3.3/1.8	**Function 0: GPIO2_0** GPIO **Function 1: SDIO0_CCLK_OUT** SDIO0 output working clock for the card

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 2: I2S_MCLK Main clock of the I^2S or PCM interface. It can act as the main clock of the ACODEC.
M20	SDIO0_CCMD	I/O	Configurable (for details, see the PADCTRL_REG55 register)	3.3/1.8	**Function 0: GPIO2_4** GPIO **Function 1: SDIO0_CCMD** SDIO0 command **Function 2: I2S_BCLK_RX** RX clock of the I^2S or PCM interface
M19	SDIO0_CDATA0	I/O	Configurable (for details, see the PADCTRL_REG56 register)	3.3/1.8	**Function 0: GPIO2_5** GPIO **Function 1: SDIO0_CDATA0** SDIO0 data 0 **Function 2: I2S_WS_RX** I^2S RX audio channel select signal or PCM TX frame sync signal
L21	SDIO0_CDATA1	I/O	Configurable (for details, see the PADCTRL_REG57 register)	3.3/1.8	**Function 0: GPIO2_6** GPIO **Function 1: SDIO0_CDATA1** SDIO0 data 1 **Function 2: I2S_SD_RX** RX data input of the I^2S or PCM interface
L20	SDIO0_CDATA2	I/O	Configurable (for details, see the PADCTRL_REG58 register)	3.3/1.8	**Function 0: GPIO2_7** GPIO **Function 1: SDIO0_CDATA2** SDIO0 data 2
M21	SDIO0_CDATA3	I/O	Configurable (for details, see the PADCTRL_REG59 register)	3.3/1.8	**Function 0: GPIO1_1** GPIO **Function 1: SDIO0_CDATA3** SDIO0 data 3
M22	SDIO0_CWPR	I/O	Configurable (for details, see the PADCTRL_REG54 register)	3.3	**Function 0: GPIO2_3** GPIO **Function 1: SDIO0_CWPR** SDIO0 card write protection detection **Function 2: I2S_SD_TX** TX data output of the I^2S or PCM interface

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
M18	SDIO0_VOUT	P	-	3.3/1.8	Power output of the pull-up resistor of SDIO0

SDIO1 Pins

Table 2-25 describes SDIO1 pins.

Table 2-25 SDIO1 pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
J20	SDIO1_CARD_DETECT	I/O	Configurable (for details, see the PADCTRL_REG67 register)	3.3	**Function 0: GPIO11_2** GPIO **Function 1: SDIO1_CARD_DETECT** SDIO1 card detection signal, active low
J21	SDIO1_CARD_POWER_EN	I/O	Configurable (for details, see the PADCTRL_REG66 register)	3.3	**Function 0: GPIO11_1** GPIO **Function 1: SDIO1_CARD_POWER_EN** SDIO1 power enable signal. The value 1 indicates power-on.
K22	SDIO1_CCLK_OUT	I/O	Configurable (for details, see the PADCTRL_REG65 register)	3.3/1.8	**Function 0: GPIO11_0** GPIO **Function 1: SDIO1_CCLK_OUT** SDIO1 output working clock for the card
K21	SDIO1_CCMD	I/O	Configurable (for details, see the PADCTRL_REG69 register)	3.3/1.8	**Function 0: GPIO11_4** GPIO **Function 1: SDIO1_CCMD** SDIO1 command
K20	SDIO1_CDATA0	I/O	Configurable (for details, see the PADCTRL_REG70 register)	3.3/1.8	**Function 0: GPIO11_5** GPIO **Function 1: SDIO1_CDATA0** SDIO1 data 0 **Function 2: CLK_TEST_OUT0** Main test clock 0 **Function 3: CLK_TEST_OUT1** Main test clock 1 **Function 4: CLK_TEST_OUT2** Main test clock 2

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 5: CLK_TEST_OUT3 Main test clock 3 **Function 6: RTC_TEST_CLK** RTC test clock **Function 7: OSC_TEST_CLK** System crystal oscillator test clock
J22	SDIO1_CDATA1	I/O	Configurable (for details, see the PADCTRL_REG71 register)	3.3/1.8	**Function 0: PLL_TEST_OUT0** PLL test clock 0 **Function 1: SDIO1_CDATA1** SDIO1 data 1 **Function 2: PLL_TEST_OUT1** PLL test clock 1 **Function 3: PLL_TEST_OUT2** PLL test clock 2 **Function 4: PLL_TEST_OUT3** PLL test clock 3 **Function 5: GPIO11_6** GPIO
L19	SDIO1_CDATA2	I/O	Configurable (for details, see the PADCTRL_REG72 register)	3.3/1.8	**Function 0: GPIO11_7** GPIO **Function 1: SDIO1_CDATA2** SDIO1 data 2
K19	SDIO1_CDATA3	I/O	Configurable (for details, see the PADCTRL_REG73 register)	3.3/1.8	**Function 0: GPIO1_2** GPIO **Function 1: SDIO1_CDATA3** SDIO1 data 3
J19	SDIO1_CWPR	I/O	Configurable (for details, see the PADCTRL_REG68 register)	3.3	**Function 0: GPIO11_3** GPIO **Function 1: SDIO1_CWPR** SDIO1 card write protection detection
K18	SDIO1_VOUT	P	None	3.3/1.8	Power output of the pull-up resistor of SDIO1

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SFC Pins

Table 2-26 describes SPI flash controller (SFC) pins.

Table 2-26 SFC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P1	SFC_CLK	I_{PD}/O	Configurable (for details, see the PADCTRL_REG76 register)	3.3	**Function 0: SFC_CLK** Clock signal transmitted to the SPI flash. The high level or low level can be selected when the clock is not switched. **Function 1: SFC_BOOT_MODE** This pin works with SFC_DEVICE_MODE. Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode Boot address mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire mode 1: 4-wire mode
R3	SFC_CSN1	O	Configurable (for details, see the PADCTRL_REG79 register)	3.3	CS1 of the SPI flash for mounting the SPI flash from which the system boots, active low
R4	SFC_HOLD_IO3	I_{PU}/O	Configurable (for details, see the PADCTRL_REG78 register)	3.3	Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal 3 in quad-SPI mode
R2	SFC_SIO_IO0	I/O	Configurable (for details, see the PADCTRL_REG74 register)	3.3	Data output signal in standard SPI mode Data I/O signal 0 in dual-SPI mode Data I/O signal 0 in quad-SPI mode
P3	SFC_SOI_IO1	I/O	Configurable (for details, see the PADCTRL_REG77 register)	3.3	Data input signal in standard SPI mode Data I/O signal 1 in dual-SPI mode Data I/O signal 1 in quad-SPI mode

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P2	SFC_WP_IO2	I/O	Configurable (for details, see the PADCTRL_REG75 register)	3.3	Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal 2 in quad-SPI mode

SPI0 Pins

Table 2-27 describes SPI0 pins.

Table 2-27 SPI0 pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y3	SPI0_CSN	I/O	Configurable (for details, see the PADCTRL_REG23 register)	3.3/1.8	**Function 0: GPIO8_3** GPIO **Function 1: SPI0_CSN** SPI0 CS
AB2	SPI0_SCLK	I/O	Configurable (for details, see the PADCTRL_REG24 register)	3.3/1.8	**Function 0: GPIO8_0** GPIO **Function 1: SPI0_SCLK** SPI0 clock **Function 2: I2C0_SCL** I^2C0 bus clock
AA2	SPI0_SDI	I_{PU}/O	Configurable (for details, see the PADCTRL_REG22 register)	3.3/1.8	**Function 0: GPIO8_2** GPIO **Function 1: SPI0_SDI** SPI0 input data
Y2	SPI0_SDO	I/O	Configurable (for details, see the PADCTRL_REG21 register)	3.3/1.8	**Function 0: GPIO8_1** GPIO **Function 1: SPI0_SDO** SPI0 output data **Function 2: I2C0_SDA** I^2C0 bus data/address

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SPI1 Pins

Table 2-28 describes SPI1 pins.

Table 2-28 SPI1 pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y17	SPI1_CSN0	I/O	Configurable (for details, see the PADCTRL_REG27 register)	3.3	**Function 0: GPIO8_7** GPIO **Function 1: SPI1_CSN** SPI1 CS
AA16	SPI1_SCLK	I/O	Configurable (for details, see the PADCTRL_REG24 register)	3.3	**Function 0: GPIO8_4** GPIO **Function 1: SPI1_SCLK 0** SPI1 clock 0 **Function 2: I2C1_SCL** I^2C1 bus clock
W16	SPI1_SDI	I_{PU}/O	Configurable (for details, see the PADCTRL_REG26 register)	3.3	**Function 0: GPIO8_6** GPIO **Function 1: SPI1_SDI** SPI1 input data
Y16	SPI1_SDO	I/O	Configurable (for details, see the PADCTRL_REG25 register)	3.3	**Function 0: GPIO8_5** GPIO **Function 1: SPI1_SDO** SPI1 output data **Function 2: I2C1_SDA** I^2C1 bus data/address

UART Pins

Table 2-29 describes universal asynchronous receiver transmitter (UART) pins.

Table 2-29 UART pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W21	UART0_RXD	I_{PU}	Configurable (for details, see the PADCTRL_REG30 register)	3.3	UART0 RX data
Y21	UART0_TXD	O	Configurable (for details, see the PADCTRL_REG31	3.3	UART0 TX data

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
			register)		
W20	UART1_CTSN	I/O	Configurable (for details, see the PADCTRL_REG34 register)	3.3	**Function 0: GPIO9_4** GPIO **Function 1: UART1_CTSN** UART1 modem status input, active low **Function 2: UART3_TXD** UART3 TX data
Y19	UART1_RTSN	I_{PU} /O	Configurable (for details, see the PADCTRL_REG32 register)	3.3	**Function 0: GPIO9_2** GPIO **Function 1: UART1_RTSN** UART1 modem status output, active low **Function 2: UART3_RXD** UART3 RX data
Y22	UART1_RXD	I_{PU} /O	Configurable (for details, see the PADCTRL_REG33 register)	3.3	**Function 0: GPIO9_3** GPIO **Function 1: UART1_RXD** UART1 RX data
W22	UART1_TXD	I/O	Configurable (for details, see the PADCTRL_REG31 register)	3.3	**Function 0: GPIO9_5** GPIO **Function 1: UART1_TXD** UART1 TX data
AA17	UART2_RXD	I_{PU} /O	Configurable (for details, see the PADCTRL_REG36 register)	3.3	**Function 0: GPIO9_6** GPIO **Function 1: UART2_RXD** UART2 RX data **Function 2: I2S_BCLK_RX** RX clock of the I^2S or PCM interface

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V22	UART2_TXD	I/O	Configurable (for details, see the PADCTRL_REG37 register)	3.3	**Function 0: GPIO9_7** GPIO **Function 1: UART2_TXD** UART2 TX data **Function 2: I2S_WS_RX** I^2S RX audio channel select signal or PCM TX frame sync signal

USB Pins

Table 2-30 describes USB pins.

Table 2-30 USB pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U21	USB_DM	I/O	None	None	USB D− signal. In high-speed mode, the maximum voltage of this port is 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
U22	USB_DP	I/O	None	None	USB D+ signal. In high-speed mode, the maximum voltage of this port is 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
V21	USB_OVRCUR	I/O	Configurable (for details, see the PADCTRL_REG49 register)	3.3	**Function 0: GPIO10_6** GPIO **Function 1: USB_OVRCUR** USB port overcurrent indicator. The level polarity can be specified by configuring the peripheral control register MISC_CTRL30 bit[17].
V19	USB_PWREN	I/O	Configurable (for details, see the PADCTRL_REG50 register)	3.3	**Function 0: GPIO10_7** GPIO **Function 1: USB_PWREN** Power control output pin of the USB port. The level polarity can be specified by configuring the peripheral control register MISC_CTRL30 bit[16].
U20	USB_REXT	I/O	None	None	USB pin for connecting to an external reference resistor. The 135 Ω resistor is recommended.

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T18	AVDD33_USB	P	None	3.3	USB analog power
T21 T22 U19	AVSS_USB	G	None	None	USB analog GND

VDAC Pins

Table 2-31 describes video digital-to-analog converter (VDAC) pins.

Table 2-31 VDAC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T20	VDAC_CVBS	O	None	None	VDAC CVBS channel output
T19	VDAC_IREF	I/O	None	None	Reference current. When an external resistor is connected, the current is output; when an external power supply is connected, the current is input. The 1130 Ω resistor is recommended.
P18	AVDD33_VDAC	P	None	3.3	VDAC analog power
R18	AVSS_VDAC	G	None	None	VDAC analog GND

VO Pins

The Hi3516A video output (VO) interface supports the BT.1120 and BT.656 modes. Table 2-32 describes the functions of VO pins in each mode.

Table 2-32 Functions of VO pins in two modes

Pin Name	BT.1120 Mode		BT.656 Mode	
	VO_MUX [27]==0	VO_MUX [27]==1	VO_MUX [27]==0	VO_MUX [27]==1
VO_CLK	Output clock	Output clock	Output clock	Output clock
VO_DAT0	C0	Y0	DATA0	None
VO_DAT1	C1	Y1	DATA1	None

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Pin Name	BT.1120 Mode		BT.656 Mode	
	VO_MUX [27]==0	VO_MUX [27]==1	VO_MUX [27]==0	VO_MUX [27]==1
VO_DAT2	C2	Y2	DATA2	None
VO_DAT3	C3	Y3	DATA3	None
VO_DAT4	C4	Y4	DATA4	None
VO_DAT5	C5	Y5	DATA5	None
VO_DAT6	C6	Y6	DATA6	None
VO_DAT7	C7	Y7	DATA7	None
VO_DAT8	Y0	C0	None	DATA0
VO_DAT9	Y1	C1	None	DATA1
VO_DAT10	Y2	C2	None	DATA2
VO_DAT11	Y3	C3	None	DATA3
VO_DAT12	Y4	C4	None	DATA4
VO_DAT13	Y5	C5	None	DATA5
VO_DAT14	Y6	C6	None	DATA6
VO_DAT15	Y7	C7	None	DATA7

Table 2-33 describes VO pins.

Table 2-33 VO pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
G22	VO_CLK	I/O	Configurable (for details, see the PADCTRL_REG3 register)	3.3	**Function 0: GPIO1_0** GPIO **Function 1: VO_CLK** VO output clock
H20	VO_DAT0	I_{SPD}/O	Configurable (for details, see the PADCTRL_REG19 register)	3.3	**Function 0: GPIO7_7** GPIO **Function 1: VO_DAT0** VO output data 0 **Function 2: BOOT_SEL** BOOT_SEL (valid only during power-on) 0: booting from the storage space of the SPI flash

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					1: booting from the storage space of the NAND flash
H19	VO_DAT1	I_{SPD}/O	Configurable (for details, see the PADCTRL_REG18 register)	3.3	**Function 0: GPIO7_6** GPIO **Function 1: VO_DAT1** VO output data 1 **Function 2: BOOTROM_SEL** BOOTROM boot enable (valid only during power-on) 0: booting from the other space (determined by BOOT_Sel) 1: booting from the BOOTROM
H21	VO_DAT2	I/O	Configurable (for details, see the PADCTRL_REG17 register)	3.3	**Function 0: GPIO7_5** GPIO **Function 1: VO_DAT2** VO output data 2
G19	VO_DAT3	I_{SPD}/O	Configurable (for details, see the PADCTRL_REG16 register)	3.3	**Function 0: GPIO7_4** GPIO **Function 1: VO_DAT3** VO output data 3 **Function 2: SFC_DEVICE_MODE** SPI flash select (valid only during power-on) 0: SPI NOR flash 1: SPI NAND flash
G21	VO_DAT4	I/O	Configurable (for details, see the PADCTRL_REG15 register)	3.3	**Function 0: GPIO7_3** GPIO **Function 1: VO_DAT4** VO output data 4
F22	VO_DAT5	I/O	Configurable (for details, see the PADCTRL_REG14 register)	3.3	**Function 0: GPIO7_2** GPIO **Function 1: VO_DAT5** VO output data 5
G20	VO_DAT6	I/O	Configurable (for details, see the PADCTRL_REG13 register)	3.3	**Function 0: GPIO7_1** GPIO **Function 1: VO_DAT6** VO output data 6

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
F21	VO_DAT7	I/O	Configurable (for details, see the PADCTRL_REG12 register)	3.3	**Function 0: GPIO7_0** GPIO **Function 1: VO_DAT7** VO output data 7
F19	VO_DAT8	I/O	Configurable (for details, see the PADCTRL_REG11 register)	3.3	**Function 0: GPIO6_7** GPIO **Function 1: VO_DAT8** VO output data 8
E22	VO_DAT9	I_{SPU}/O	Configurable (for details, see the PADCTRL_REG10 register)	3.3	**Function 0: GPIO6_6** GPIO **Function 1: VO_DAT9** VO output data 9 **Function 2: SFC_NAND_BOOT_PIN0** SPI NAND flash configuration. This function is valid only during power-on. {SF_NAND_BOOT_PIN1, SF_NAND_BOOT_PIN0} indicate the error correcting code (ECC) type. 00: reserved 01: 8-bit ECC 10: reserved 11: 24-bit ECC
F20	VO_DAT10	I_{SPD}/O	Configurable (for details, see the PADCTRL_REG9 register)	3.3	**Function 0: GPIO6_5** GPIO **Function 1: VO_DAT10** VO output data 10 **Function 2: SFC_NAND_BOOT_PIN1** SPI NAND flash configuration. This function is valid only during power-on. {SF_NAND_BOOT_PIN1, SF_NAND_BOOT_PIN0} indicate the ECC type. 00: reserved 01: 8-bit ECC 10: reserved 11: 24-bit ECC

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E21	VO_DAT11	I_{SPD}/O	Configurable (for details, see the PADCTRL_REG8 register)	3.3	**Function 0: GPIO6_4** GPIO **Function 1: VO_DAT11** VO output data 11 **Function 2: SFC_NAND_BOOT_PIN2** SPI NAND flash configuration. This function is valid only during power-on. SF_NAND_BOOT_PIN2 indicates the page size. 0: 2 KB page size 1: 4 KB page size
D22	VO_DAT12	I/O	Configurable (for details, see the PADCTRL_REG7 register)	3.3	**Function 0: GPIO6_3** GPIO **Function 1: VO_DAT12** VO output data 12
D21	VO_DAT13	I/O	Configurable (for details, see the PADCTRL_REG6 register)	3.3	**Function 0: GPIO6_2** GPIO **Function 1: VO_DAT13** VO output data 13
E20	VO_DAT14	I/O	Configurable (for details, see the PADCTRL_REG5 register)	3.3	**Function 0: GPIO6_1** GPIO **Function 1: VO_DAT14** VO output data 14
C22	VO_DAT15	I/O	Configurable (for details, see the PADCTRL_REG4 register)	3.3	**Function 0: GPIO6_0** GPIO **Function 1: VO_DAT15** VO output data 15

OSC Pins

Table 2-34 describes oscillator (OSC) pins.

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Table 2-34 OSC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U1	XIN	CIN	None	None	24 MHz system crystal input
U2	XOUT	COUT	None	None	24 MHz system crystal drive output

Power Pins and GND Pins

Table 2-35 describes power pins and GND pins.

Table 2-35 Power pins and GND pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P5	AVDD_EFUSE	P	None	2.5	eFUSE power
R5	AVDD11_PLL	P	None	1.1	1.1 V PLL analog power
U5	AVDD33_PLL	P	None	3.3	3.3 V PLL analog power
T5	AVSS_PLL	G	None	-	PLL analog GND
F18, G18, L5, M5, V16, V17	DVDD33	P	None	3.3	Digital I/O power
L18	DVDD18_SDIO	P	None	1.8	1.8 V input power of the SDIO power switch
V6	DVDD3318_SENSOR	P	None	3.3/1.8	Sensor I/O power
V8	DVDD3318_VI	P	None	3.3/1.8	VI I/O power
E17	DVDDIO_RGMII	P	None	3.3/2.5/1.8	RGMII I/O power
P8, R8, R9	VDD_CPU	P	None	0.9~1.32	CPU working power
H8, H10, H11, J8	VDD_DDR	P	None	0.9~1.32	DDR working power
H15, J15, M15, N15, R13, R14	VDD_MEDIA	P	None	0.9~1.32	Media working power

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Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
H13, H14, K15, L8, M8, N8, P15, R10, R11, R15	VDD	P	None	1.1	Core working power.
A1, A9, A11, A14, A22, B9, B11, B14, B17, B20, D17, E5, E7, E14, E18, F1, F2, H9, H12, H18, H22, J9, J10, J11, J12, J13, J14, K5, K8, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, L15, M9, M10, M11, M12, M13, M14, N5, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R1, R12, V1, V2, V15, V18, W3, W17, AA6, AA18, AB1, AB22	VSS	G	None	-	Digital GND

2.2.3 Default Reset Status of Digital Pins

Table 2-36describes the default reset status of digital pins.

Table 2-36 Default reset status of digital pins

PAD	Default Function	I/O	Level Status	Remarks
SENSOR_CLK	GPIO0_5	I	TBD	-
FLASH_TRIG	GPIO0_6	I	TBD	-

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PAD	Default Function	I/O	Level Status	Remarks
SHUTTER_TRIG	GPIO0_7	I	TBD	-
VO_CLK	GPIO1_0	I	TBD	-
VO_DAT15	GPIO6_0	I	TBD	-
VO_DAT14	GPIO6_1	I	TBD	-
VO_DAT13	GPIO6_2	I	TBD	-
VO_DAT12	GPIO6_3	I	TBD	-
VO_DAT11	GPIO6_4	I	TBD	The level of SFC_NAND_BOOT_PIN2 is controlled by connecting VO_DAT11 to a pull-up or pull-down resistor.
VO_DAT10	GPIO6_5	I	TBD	The level of SFC_NAND_BOOT_PIN1 is controlled by connecting VO_DAT10 to a pull-up or pull-down resistor.
VO_DAT9	GPIO6_6	I	TBD	The level of SFC_NAND_BOOT_PIN0 is controlled by connecting VO_DAT9 to a pull-up or pull-down resistor.
VO_DAT8	GPIO6_7	I	TBD	-
VO_DAT7	GPIO7_0	I	TBD	-
VO_DAT6	GPIO7_1	I	TBD	-
VO_DAT5	GPIO7_2	I	TBD	-
VO_DAT4	GPIO7_3	I	TBD	-
VO_DAT3	GPIO7_4	I	TBD	The level of SFC_DEVICE_MODE is controlled by connecting VO_DAT3 to a pull-up or pull-down resistor.
VO_DAT2	GPIO7_5	I	0	The pin connects to a pull-down resistor.
VO_DAT1	GPIO7_6	I	TBD	The level of BOOTROM_SEL is controlled by connecting

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PAD	Default Function	I/O	Level Status	Remarks
				VO_DAT1 to a pull-up or pull-down resistor.
VO_DAT0	GPIO7_7	I	TBD	The level of BOOT_SEL is controlled by connecting VO_DAT0 to a pull-up or pull-down resistor.
SPI0_SCLK	GPIO8_0	I	TBD	-
SPI0_SDO	GPIO8_1	I	TBD	-
SPI0_SDI	GPIO8_2	I	TBD	-
SPI0_CSN	GPIO8_3	I	TBD	-
SPI1_SCLK	GPIO8_4	I	TBD	-
SPI1_SDO	GPIO8_5	I	TBD	-
SPI1_SDI	GPIO8_6	I	TBD	-
SPI1_CSN0	GPIO8_7	I	TBD	-
I2C2_SDA	GPIO9_0	I	TBD	-
I2C2_SCL	GPIO9_1	I	TBD	-
UART0_RXD	UART0_RXD	I	1	The pin connects to a pull-up resistor.
UART0_TXD	UART0_TXD	O	0	-
UART1_RTSN	GPIO9_2	I	1	The pin connects to a pull-up resistor.
UART1_RXD	GPIO9_3	I	1	The pin connects to a pull-up resistor.
UART1_CTSN	GPIO9_4	I	TBD	-
UART1_TXD	GPIO9_5	I	TBD	-
UART2_RXD	GPIO9_6	I	1	The pin connects to a pull-up resistor.
UART2_TXD	GPIO9_7	I	TBD	-
JTAG_EN	JTAG_EN	I	TBD	-
JTAG_TRSTN	GPIO10_0	I	TBD	-

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PAD	Default Function	I/O	Level Status	Remarks
JTAG_TCK	GPIO10_1	I	TBD	-
JTAG_TMS	GPIO10_2	I	TBD	-
JTAG_TDO	GPIO10_3	I	TBD	-
JTAG_TDI	GPIO10_4	I	TBD	-
IR_IN	GPIO10_5	I	1	The pin connects to a pull-up resistor.
POR_SEL	POR_SEL	I	TBD	-
RSTN	RSTN	I	TBD	-
WDG_RSTN	WDG_RSTN	O		The level depends on POR_SEL. If POR_SEL is 0, the output level is 0 and the level is pulled up after about 130 ms. When POR_SEL is 1, the level is to be determined (TBD).
TEST_MODE	TEST_MODE	I	TBD	-
USB_OVRCUR	GPIO10_6	I	TBD	-
USB_PWREN	GPIO10_7	I	TBD	--
SDIO0_CCLK_OUT	GPIO2_0	I	TBD	-
SDIO0_CARD_POWER_EN	GPIO2_1	I	TBD	-
SDIO0_CARD_DETECT	GPIO2_2	I	TBD	-
SDIO0_CWPR	GPIO2_3	I	TBD	-
SDIO0_CCMD	GPIO2_4	I	TBD	-
SDIO0_CDATA0	GPIO2_5	I	TBD	-
SDIO0_CDATA1	GPIO2_6	I	TBD	-
SDIO0_CDATA2	GPIO2_7	I	TBD	-
SDIO0_CDATA3	GPIO1_1	I	TBD	-
GPIO0_0	SENSOR_RSTN	O	0	The level is pulled up after about 130 ms.

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PAD	Default Function	I/O	Level Status	Remarks
GPIO0_1	GPIO0_1	I	TBD	-
GPIO0_2	GPIO0_2	I	TBD	-
GPIO0_3	GPIO0_3	I	TBD	-
GPIO0_4	GPIO0_4	I	TBD	-
SDIO1_CCLK_OUT	GPIO11_0	I	TBD	-
SDIO1_CARD_POWER_EN	GPIO11_1	I	TBD	-
SDIO1_CARD_DETECT	GPIO11_2	I	TBD	-
SDIO1_CWPR	GPIO11_3	I	TBD	-
SDIO1_CCMD	GPIO11_4	I	TBD	-
SDIO1_CDATA0	GPIO11_5	I	TBD	-
SDIO1_CDATA1	PLL_TEST_OUT0	O		Test clock output
SDIO1_CDATA2	GPIO11_7	I	TBD	-
SDIO1_CDATA3	GPIO1_2	I	TBD	-
SFC_SIO_IO0	SFC_SIO_IO0	I	TBD	-
SFC_WP_IO2	SFC_WP_IO2	I	TBD	-
SFC_CLK	SFC_CLK	I		Clock signal
SFC_SOI_IO1	SFC_SOI_IO1	O	TBD	-
SFC_HOLD_IO3	SFC_HOLD_IO3	I	TBD	-
SFC_CSN1	SFC_CSN1	O	1	-
NF_DQ0	NF_DQ0	I	TBD	-
NF_DQ1	NF_DQ1	I	TBD	-
NF_DQ2	NF_DQ2	I	TBD	-
NF_DQ3	NF_DQ3	I	TBD	-
NF_DQ4	NF_DQ4	I	TBD	-

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PAD	Default Function	I/O	Level Status	Remarks
NF_DQ5	NF_DQ5	I	TBD	-
NF_DQ6	NF_DQ6	I	TBD	-
NF_DQ7	NF_DQ7	I	TBD	-
NF_RDY0	NF_RDY0	I	1	The pin connects to a pull-up resistor.
NF_RDY1	NF_RDY1	I	1	The pin connects to a pull-up resistor.
NF_REN	NF_REN	O	1	-
NF_CSN0	NF_CSN0	O	1	-
NF_CSN1	NF_CSN1	O	1	-
NF_CLE	NF_CLE	O	0	-
NF_ALE	NF_ALE	O	0	-
NF_WEN	NF_WEN	O	0	-
PWM0	PWM0	O	0	-
PWM1	PWM1	O	0	-
PWM2	PWM2	O	0	-
PWM3	PWM3	O	0	-
SAR_ADC_CH0	SAR_ADC_CH0	I	TBD	-
SAR_ADC_CH1	SAR_ADC_CH1	I	TBD	-
EPHY_CLK	GPIO14_4	I	TBD	-
MDCK	GPIO14_5	I	TBD	-
MDIO	GPIO14_6	I	TBD	-
RGMII_TX_EN	GPIO14_7	I	TBD	-
RGMII_TX_CLK	GPIO4_0	I	TBD	-
RGMII_TXD0	GPIO4_1	I	TBD	-

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PAD	Default Function	I/O	Level Status	Remarks
RGMII_TXD1	GPIO4_2	I	TBD	-
RGMII_TXD2	GPIO4_3	I	TBD	-
RGMII_TXD3	GPIO4_4	I	TBD	-
RGMII_RX_CLK	GPIO4_5	I	TBD	-
RGMII_RX_DV	GPIO4_6	I	TBD	-
RGMII_RXD0	GPIO4_7	I	TBD	-
RGMII_RXD1	GPIO1_3	I	TBD	-
RGMII_RXD2	GPIO1_4	I	TBD	-
RGMII_RXD3	GPIO1_5	I	TBD	-
VI_CLK	GPIO15_0	I	TBD	-
VI_HS	GPIO15_1	I	TBD	-
VI_VS	GPIO15_2	I	TBD	-
VI_DAT15	GPIO12_0	I	TBD	-
VI_DAT14	GPIO12_1	I	TBD	-
VI_DAT13	GPIO12_2	I	TBD	-
VI_DAT12	GPIO12_3	I	TBD	-
VI_DAT11	GPIO12_4	I	TBD	-
VI_DAT10	GPIO12_5	I	TBD	-
VI_DAT9	GPIO12_6	I	TBD	-
VI_DAT8	GPIO12_7	I	TBD	-
VI_DAT7	GPIO13_0	I	TBD	-
VI_DAT6	GPIO13_1	I	TBD	-
VI_DAT5	GPIO13_2	I	TBD	-
VI_DAT4	GPIO13_3	I	TBD	-

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PAD	Default Function	I/O	Level Status	Remarks
VI_DAT3	GPIO13_4	I	TBD	-
VI_DAT2	GPIO13_5	I	TBD	-
VI_DAT1	GPIO13_6	I	TBD	-
VI_DAT0	GPIO13_7	I	TBD	-

2.3 Pin Multiplexing Control Registers

2.3.1 Register Summary

Table 2-37 describes pin multiplexing control registers.

Table 2-37 Summary of pin multiplexing control registers (base address: 0x200F_0000)

Offset Address	Register	Description	Page
0x000	muxctrl_reg0	Multiplexing control register for the SENSOR_CLK pin	2-69
0x004	muxctrl_reg1	Multiplexing control register for the FLASH_TRIG pin	2-70
0x008	muxctrl_reg2	Multiplexing control register for the SHUTTER_TRIG pin	2-70
0x00C	muxctrl_reg3	Multiplexing control register for the VO_CLK pin	2-71
0x010	muxctrl_reg4	Multiplexing control register for the VO_DAT15 pin	2-71
0x014	muxctrl_reg5	Multiplexing control register for the VO_DAT14 pin	2-72
0x018	muxctrl_reg6	Multiplexing control register for the VO_DAT13 pin	2-72
0x01C	muxctrl_reg7	Multiplexing control register for the VO_DAT12 pin	2-73
0x020	muxctrl_reg8	Multiplexing control register for the VO_DAT11 pin	2-73
0x024	muxctrl_reg9	Multiplexing control register for the VO_DAT10 pin	2-74
0x028	muxctrl_reg10	Multiplexing control register for the	2-75

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Offset Address	Register	Description	Page
		VO_DAT9 pin	
0x02C	muxctrl_reg11	Multiplexing control register for the VO_DAT8 pin	2-75
0x030	muxctrl_reg12	Multiplexing control register for the VO_DAT7 pin	2-76
0x034	muxctrl_reg13	Multiplexing control register for the VO_DAT6 pin	2-76
0x038	muxctrl_reg14	Multiplexing control register for the VO_DAT5 pin	2-76
0x03C	muxctrl_reg15	Multiplexing control register for the VO_DAT4 pin	2-77
0x040	muxctrl_reg16	Multiplexing control register for the VO_DAT3 pin	2-77
0x044	muxctrl_reg17	Multiplexing control register for the VO_DAT2 pin	2-78
0x048	muxctrl_reg18	Multiplexing control register for the VO_DAT1 pin	2-78
0x04C	muxctrl_reg19	Multiplexing control register for the VO_DAT0 pin	2-79
0x050	muxctrl_reg20	Multiplexing control register for the SPI0_SCLK pin	2-80
0x054	muxctrl_reg21	Multiplexing control register for the SPI0_SDO pin	2-80
0x058	muxctrl_reg22	Multiplexing control register for the SPI0_SDI pin	2-81
0x05C	muxctrl_reg23	Multiplexing control register for the SPI0_CSN pin	2-81
0x060	muxctrl_reg24	Multiplexing control register for the SPI1_SCLK pin	2-82
0x064	muxctrl_reg25	Multiplexing control register for the SPI1_SDO pin	2-82
0x068	muxctrl_reg26	Multiplexing control register for the SPI1_SDI pin	2-83
0x06C	muxctrl_reg27	Multiplexing control register for the SPI1_CSN0 pin	2-83
0x070	muxctrl_reg28	Multiplexing control register for the I2C2_SDA pin	2-83
0x074	muxctrl_reg29	Multiplexing control register for the I2C2_SCL pin	2-84

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Offset Address	Register	Description	Page
0x078	muxctrl_reg30	Multiplexing control register for the UART1_RTSN pin	2-84
0x07C	muxctrl_reg31	Multiplexing control register for the UART1_RXD pin	2-85
0x080	muxctrl_reg32	Multiplexing control register for the UART1_CTSN pin	2-85
0x084	muxctrl_reg33	Multiplexing control register for the UART1_TXD pin	2-86
0x088	muxctrl_reg34	Multiplexing control register for the UART2_RXD pin	2-86
0x08C	muxctrl_reg35	Multiplexing control register for the UART2_TXD pin	2-87
0x090	muxctrl_reg36	Multiplexing control register for the JTAG_TRSTN pin	2-88
0x094	muxctrl_reg37	Multiplexing control register for the JTAG_TCK pin	2-88
0x098	muxctrl_reg38	Multiplexing control register for the JTAG_TMS pin	2-89
0x09C	muxctrl_reg39	Multiplexing control register for the JTAG_TDO pin	2-89
0x0A0	muxctrl_reg40	Multiplexing control register for the JTAG_TDI pin	2-90
0x0A4	muxctrl_reg41	Multiplexing control register for the IR_IN pin	2-90
0x0A8	muxctrl_reg42	Multiplexing control register for the USB_OVRCUR pin	2-91
0x0AC	muxctrl_reg43	Multiplexing control register for the USB_PWREN pin	2-91
0x0B0	muxctrl_reg44	Multiplexing control register for the SDIO0_CCLK_OUT pin	2-92
0x0B4	muxctrl_reg45	Multiplexing control register for the SDIO0_CARD_POWER_EN pin	2-92
0x0B8	muxctrl_reg46	Multiplexing control register for the SDIO0_CARD_DETECT pin	2-93
0x0BC	muxctrl_reg47	Multiplexing control register for the SDIO0_CWPR pin	2-93
0x0C0	muxctrl_reg48	Multiplexing control register for the SDIO0_CCMD pin	2-94
0x0C4	muxctrl_reg49	Multiplexing control register for the	2-94

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Offset Address	Register	Description	Page
		SDIO0_CDATA0 pin	
0x0C8	muxctrl_reg50	Multiplexing control register for the SDIO0_CDATA1 pin	2-95
0x0CC	muxctrl_reg51	Multiplexing control register for the SDIO0_CDATA2 pin	2-95
0x0D0	muxctrl_reg52	Multiplexing control register for the SDIO0_CDATA3 pin	2-96
0x0D4	muxctrl_reg53	Multiplexing control register for the GPIO0_0 pin	2-96
0x0D8	muxctrl_reg54	Multiplexing control register for the GPIO0_1 pin	2-97
0x0DC	muxctrl_reg55	Multiplexing control register for the GPIO0_2 pin	2-97
0x0E0	muxctrl_reg56	Multiplexing control register for the GPIO0_3 pin	2-98
0x0E4	muxctrl_reg57	Multiplexing control register for the GPIO0_4 pin	2-98
0x0E8	muxctrl_reg58	Multiplexing control register for the SDIO1_CCLK_OUT pin	2-99
0x0EC	muxctrl_reg59	Multiplexing control register for the SDIO1_CARD_POWER_EN pin	2-99
0x0F0	muxctrl_reg60	Multiplexing control register for the SDIO1_CARD_DETECT pin	2-99
0x0F4	muxctrl_reg61	Multiplexing control register for the SDIO1_CWPR pin	2-100
0x0F8	muxctrl_reg62	Multiplexing control register for the SDIO1_CCMD pin	2-100
0x0FC	muxctrl_reg63	Multiplexing control register for the SDIO1_CDATA0 pin	2-101
0x100	muxctrl_reg64	Multiplexing control register for the SDIO1_CDATA1 pin	2-102
0x104	muxctrl_reg65	Multiplexing control register for the SDIO1_CDATA2 pin	2-102
0x108	muxctrl_reg66	Multiplexing control register for the SDIO1_CDATA3 pin	2-103
0x10C	muxctrl_reg67	Multiplexing control register for the NF_DQ0 pin	2-103
0x110	muxctrl_reg68	Multiplexing control register for the NF_DQ1 pin	2-104

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Offset Address	Register	Description	Page
0x114	muxctrl_reg69	Multiplexing control register for the NF_DQ2 pin	2-104
0x118	muxctrl_reg70	Multiplexing control register for the NF_DQ3 pin	2-104
0x11C	muxctrl_reg71	Multiplexing control register for the NF_DQ4 pin	2-105
0x120	muxctrl_reg72	Multiplexing control register for the NF_DQ5 pin	2-105
0x124	muxctrl_reg73	Multiplexing control register for the NF_DQ6 pin	2-106
0x128	muxctrl_reg74	Multiplexing control register for the NF_DQ7 pin	2-106
0x12C	muxctrl_reg75	Multiplexing control register for the NF_RDY0 pin	2-107
0x130	muxctrl_reg76	Multiplexing control register for the NF_RDY1 pin	2-107
0x134	muxctrl_reg77	Multiplexing control register for the NF_REN pin	2-108
0x138	muxctrl_reg78	Multiplexing control register for the NF_CSN0 pin	2-108
0x13C	muxctrl_reg79	Multiplexing control register for the NF_CSN1 pin	2-109
0x140	muxctrl_reg80	Multiplexing control register for the NF_CLE pin	2-109
0x144	muxctrl_reg81	Multiplexing control register for the NF_ALE pin	2-110
0x148	muxctrl_reg82	Multiplexing control register for the NF_WEN pin	2-110
0x14C	muxctrl_reg83	Multiplexing control register for the PWM0 pin	2-111
0x150	muxctrl_reg84	Multiplexing control register for the PWM1 pin	2-111
0x154	muxctrl_reg85	Multiplexing control register for the PWM2 pin	2-112
0x158	muxctrl_reg86	Multiplexing control register for the PWM3 pin	2-112
0x15C	muxctrl_reg87	Multiplexing control register for the SAR_ADC_CH0 pin	2-113
0x160	muxctrl_reg88	Multiplexing control register for the	2-113

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Offset Address	Register	Description	Page
		SAR_ADC_CH1 pin	
0x164	muxctrl_reg89	Multiplexing control register for the EPHY_CLK pin	2-114
0x168	muxctrl_reg90	Multiplexing control register for the MDCK pin	2-114
0x16C	muxctrl_reg91	Multiplexing control register for the MDIO pin	2-115
0x170	muxctrl_reg92	Multiplexing control register for the RGMII_TX_EN pin	2-115
0x174	muxctrl_reg93	Multiplexing control register for the RGMII_TX_CLK pin	2-116
0x178	muxctrl_reg94	Multiplexing control register for the RGMII_TXD0 pin	2-116
0x17C	muxctrl_reg95	Multiplexing control register for the RGMII_TXD1 pin	2-117
0x180	muxctrl_reg96	Multiplexing control register for the RGMII_TXD2 pin	2-117
0x184	muxctrl_reg97	Multiplexing control register for the RGMII_TXD3 pin	2-118
0x188	muxctrl_reg98	Multiplexing control register for the RGMII_RX_CLK pin	2-118
0x18C	muxctrl_reg99	Multiplexing control register for the RGMII_RX_DV pin	2-119
0x190	muxctrl_reg100	Multiplexing control register for the RGMII_RXD0 pin	2-119
0x194	muxctrl_reg101	Multiplexing control register for the RGMII_RXD1 pin	2-120
0x198	muxctrl_reg102	Multiplexing control register for the RGMII_RXD2 pin	2-120
0x19C	muxctrl_reg103	Multiplexing control register for the RGMII_RXD3 pin	2-121
0x1A0	muxctrl_reg104	Multiplexing control register for the VI_CLK pin	2-121
0x1A4	muxctrl_reg105	Multiplexing control register for the VI_HS pin	2-122
0x1A8	muxctrl_reg106	Multiplexing control register for the VI_VS pin	2-122
0x1AC	muxctrl_reg107	Multiplexing control register for the VI_DAT15 pin	2-123

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Offset Address	Register	Description	Page
0x1B0	muxctrl_reg108	Multiplexing control register for the VI_DAT14 pin	2-123
0x1B4	muxctrl_reg109	Multiplexing control register for the VI_DAT13 pin	2-124
0x1B8	muxctrl_reg110	Multiplexing control register for the VI_DAT12 pin	2-125
0x1BC	muxctrl_reg111	Multiplexing control register for the VI_DAT11 pin	2-125
0x1C0	muxctrl_reg112	Multiplexing control register for the VI_DAT10 pin	2-126
0x1C4	muxctrl_reg113	Multiplexing control register for the VI_DAT9 pin	2-126
0x1C8	muxctrl_reg114	Multiplexing control register for the VI_DAT8 pin	2-127
0x1CC	muxctrl_reg115	Multiplexing control register for the VI_DAT7 pin	2-127
0x1D0	muxctrl_reg116	Multiplexing control register for the VI_DAT6 pin	2-128
0x1D4	muxctrl_reg117	Multiplexing control register for the VI_DAT5 pin	2-128
0x1D8	muxctrl_reg118	Multiplexing control register for the VI_DAT4 pin	2-129
0x1DC	muxctrl_reg119	Multiplexing control register for the VI_DAT3 pin	2-129
0x1E0	muxctrl_reg120	Multiplexing control register for the VI_DAT2 pin	2-130
0x1E4	muxctrl_reg121	Multiplexing control register for the VI_DAT1 pin	2-130
0x1E8	muxctrl_reg122	Multiplexing control register for the VI_DAT0 pin	2-131

2.3.2 Register Description

muxctrl_reg0

muxctrl_reg0 is a multiplexing control register for the SENSOR_CLK pin.

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Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg0	Multiplexing control for the SENSOR_CLK pin 0: GPIO0_5 1: SENSOR_CLK

muxctrl_reg1

muxctrl_reg1 is a multiplexing control register for the FLASH_TRIG pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg1	Multiplexing control for the FLASH_TRIG pin 00: GPIO0_6 01: FLASH_TRIG 10: SPI1_CSN1 11: reserved

muxctrl_reg2

muxctrl_reg2 is a multiplexing control register for the SHUTTER_TRIG pin.

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Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg2	Multiplexing control for the SHUTTER_TRIG pin 00: GPIO0_7 01: SHUTTER_TRIG 10: SPI1_CSN2 11: reserved

muxctrl_reg3

muxctrl_reg3 is a multiplexing control register for the VO_CLK pin.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg3	VO_CLK pin 0: GPIO1_0 1: VO_CLK

muxctrl_reg4

muxctrl_reg4 is a multiplexing control register for the VO_DAT15 pin.

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Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg4	Multiplexing control for the VO_DAT15 pin 0: GPIO6_0 1: VO_DAT15

muxctrl_reg5

muxctrl_reg5 is a multiplexing control register for the VO_DAT14 pin.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg5	Multiplexing control for the VO_DAT14 pin 0: GPIO6_1 1: VO_DAT14

muxctrl_reg6

muxctrl_reg6 is a multiplexing control register for the VO_DAT13 pin.

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Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg6	Multiplexing control for the VO_DAT13 pin 0: GPIO6_2 1: VO_DAT13

muxctrl_reg7

muxctrl_reg7 is a multiplexing control register for the VO_DAT12 pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg7	Multiplexing control for the VO_DAT12 pin 0: GPIO6_3 1: VO_DAT12

muxctrl_reg8

muxctrl_reg8 is a multiplexing control register for the VO_DAT11 pin.

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Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg8	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg8	Multiplexing control for the VO_DAT11 pin 00: GPIO6_4 01: VO_DAT11 10: SFC_NAND_BOOT_PIN2 Other values: reserved

muxctrl_reg9

muxctrl_reg9 is a multiplexing control register for the VO_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg9	Multiplexing control for the VO_DAT10 pin 00: GPIO6_5 01: VO_DAT10 10: SFC_NAND_BOOT_PIN1 Other values: reserved

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muxctrl_reg10

muxctrl_reg10 is a multiplexing control register for the VO_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg10	Multiplexing control for the VO_DAT9 pin 00: GPIO6_6 01: VO_DAT9 10: SFC_NAND_BOOT_PIN0 Other values: reserved

muxctrl_reg11

muxctrl_reg11 is a multiplexing control register for the VO_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg11
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg11	Multiplexing control for the VO_DAT8 pin 0: GPIO6_7 1: VO_DAT8

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muxctrl_reg12

muxctrl_reg12 is a multiplexing control register for the VO_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg12	Multiplexing control for the VO_DAT7 pin 0: GPIO7_0 1: VO_DAT7

muxctrl_reg13

muxctrl_reg13 is a multiplexing control register for the VO_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg13
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg13	Multiplexing control for the VO_DAT6 pin 0: GPIO7_1 1: VO_DAT6

muxctrl_reg14

muxctrl_reg14 is a multiplexing control register for the VO_DAT5 pin.

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Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg14
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg14	Multiplexing control for the VO_DAT5 pin 0: GPIO7_2 1: VO_DAT5

muxctrl_reg15

muxctrl_reg15 is a multiplexing control register for the VO_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg15
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg15	Multiplexing control for the VO_DAT4 pin 0: GPIO7_3 1: VO_DAT4

muxctrl_reg16

muxctrl_reg16 is a multiplexing control register for the VO_DAT3 pin.

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Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg16	Multiplexing control for the VO_DAT3 pin 00: GPIO7_4 01: VO_DAT3 10: SFC_DEVICE_MODE Other values: reserved

muxctrl_reg17

muxctrl_reg17 is a multiplexing control register for the VO_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg17
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg17	Multiplexing control for the VO_DAT2 pin 0: GPIO7_5 1: VO_DAT2

muxctrl_reg18

muxctrl_reg18 is a multiplexing control register for the VO_DAT1 pin.

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Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg18	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg18	Multiplexing control for the VO_DAT1 pin 00: GPIO7_6 01: VO_DAT1 10: BOOTROM_SEL Other values: reserved

muxctrl_reg19

muxctrl_reg19 is a multiplexing control register for the VO_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg19	Multiplexing control for the VO_DAT0 pin 00: GPIO7_7 01: VO_DAT0 10: BOOT_SEL Other values: reserved

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muxctrl_reg20

muxctrl_reg20 is a multiplexing control register for the SPI0_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg20	Multiplexing control for the SPI0_SCLK pin 00: GPIO8_0 01: SPI0_SCLK 10: I2C0_SCL Other values: reserved

muxctrl_reg21

muxctrl_reg21 is a multiplexing control register for the SPI0_SDO pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg21	Multiplexing control for the SPI0_SDO pin 00: GPIO8_1 01: SPI0_SDO 10: I2C0_SDA Other values: reserved

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muxctrl_reg22

muxctrl_reg22 is a multiplexing control register for the SPI0_SDI pin.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg22
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg22	Multiplexing control for the SPI0_SDI pin 0: GPIO8_2 1: SPI0_SDI

muxctrl_reg23

muxctrl_reg23 is a multiplexing control register for the SPI0_CSN pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg23
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg23	Multiplexing control for the SPI0_CSN pin 0: GPIO8_3 1: SPI0_CSN

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muxctrl_reg24

muxctrl_reg24 is a multiplexing control register for the SPI1_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg24	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg24	Multiplexing control for the SPI1_SCLK pin 00: GPIO8_4 01: SPI1_SCLK 10: I2C1_SCL Other values: reserved

muxctrl_reg25

muxctrl_reg25 is a multiplexing control register for the SPI1_SDO pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg25	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg25	Multiplexing control for the SPI1_SDO pin 00: GPIO8_5 01: SPI1_SDO 10: I2C1_SDA Other values: reserved

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muxctrl_reg26

muxctrl_reg26 is a multiplexing control register for the SPI1_SDI pin.

Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg26
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg26	Multiplexing control for the SPI1_SDI pin 0: GPIO8_6 1: SPI1_SDI

muxctrl_reg27

SPI1_CSN0 is a multiplexing control register for the SPI1_CSN pin.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg27
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg27	Multiplexing control for the SPI1_CSN0 pin 0: GPIO8_7 1: SPI1_CSN0

muxctrl_reg28

muxctrl_reg28 is a multiplexing control register for the I2C2_SDA pin.

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Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg28
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg28	Multiplexing control for the I2C2_SDA pin 0: GPIO9_0 1: I2C2_SDA

muxctrl_reg29

muxctrl_reg29 is a multiplexing control register for the I2C2_SCL pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg29
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg29	Multiplexing control for the I2C2_SCL pin 0: GPIO9_1 1: I2C2_SCL

muxctrl_reg30

muxctrl_reg30 is a multiplexing control register for the UART1_RTSN pin.

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Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg30	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg30	Multiplexing control for the UART1_RTSN pin 00: GPIO9_2 01: UART1_RTSN 10: UART3_RXD Other values: reserved

muxctrl_reg31

muxctrl_reg31 is a multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg31
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg31	Multiplexing control for the UART1_RXD pin 0: GPIO9_3 1: UART1_RXD

muxctrl_reg32

muxctrl_reg32 is a multiplexing control register for the UART1_CTSN pin.

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Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg32	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg32	Multiplexing control for the UART1_CTSN pin 00: GPIO9_4 01: UART1_CTSN 10: UART3_TXD Other values: reserved

muxctrl_reg33

muxctrl_reg33 is a multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg33
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg33	Multiplexing control for the UART1_TXD pin 0: GPIO9_5 1: UART1_TXD

muxctrl_reg34

muxctrl_reg34 is a multiplexing control register for the UART2_RXD pin.

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Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg34	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg34	Multiplexing control for the UART2_RXD pin 00: GPIO9_6 01: UART2_RXD 10: I2S_BCLK_RX Other values: reserved

muxctrl_reg35

muxctrl_reg35 is a multiplexing control register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg35	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg35	Multiplexing control for the UART2_TXD pin 00: GPIO9_7 01: UART2_TXD 10: I2S_WS_RX Other values: reserved

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muxctrl_reg36

muxctrl_reg36 is a multiplexing control register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg36	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg36	Multiplexing control for the JTAG_TRSTN pin 00: GPIO10_0 01: JTAG_TRSTN 10: I2S_MCLK Other values: reserved

muxctrl_reg37

muxctrl_reg37 is a multiplexing control register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg37	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg37	Multiplexing control for the JTAG_TCK pin 00: GPIO10_1 01: JTAG_TCK 10: I2S_BCLK_TX Other values: reserved

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muxctrl_reg38

muxctrl_reg38 is a multiplexing control register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg38	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg38	Multiplexing control for the JTAG_TMS pin 00: GPIO10_2 01: JTAG_TMS 10: I2S_WS_TX Other values: reserved

muxctrl_reg39

muxctrl_reg39 is a multiplexing control register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg39	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg39	Multiplexing control for the JTAG_TDO pin 00: GPIO10_3 01: JTAG_TDO 10: I2S_SD_RX Other values: reserved

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muxctrl_reg40

muxctrl_reg40 is a multiplexing control register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg40	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg40	Multiplexing control for the JTAG_TDI pin 00: GPIO10_4 01: JTAG_TDI 10: I2S_SD_TX Other values: reserved

muxctrl_reg41

muxctrl_reg41 is a multiplexing control register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg41	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg41	Multiplexing control for the IR_IN pin 00: GPIO10_5 01: IR_IN 10: PWM4 Other values: reserved

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muxctrl_reg42

muxctrl_reg42 is a multiplexing control register for the USB_OVRCUR pin.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg42
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg42	Multiplexing control for the USB_OVRCUR pin 0: GPIO10_6 1: USB_OVRCUR

muxctrl_reg43

muxctrl_reg43 is a multiplexing control register for the USB_PWREN pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg43
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg43	Multiplexing control for the USB_PWREN pin 0: GPIO10_7 1: USB_PWREN

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muxctrl_reg44

muxctrl_reg44 is a multiplexing control register for the SDIO0_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg44	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg44	Multiplexing control for the SDIO0_CCLK_OUT pin 00: GPIO2_0 01: SDIO0_CCLK_OUT 10: I2S_MCLK Other values: reserved

muxctrl_reg45

muxctrl_reg45 is a multiplexing control register for the SDIO0_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg45	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg45	Multiplexing control for the SDIO0_CARD_POWER_EN pin 00: GPIO2_1 01: SDIO0_CARD_POWER_EN 10: I2S_BCLK_TX Other values: reserved

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muxctrl_reg46

muxctrl_reg46 is a multiplexing control register for the SDIO0_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg46	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg46	Multiplexing control for the SDIO0_CARD_DETECT pin 00: GPIO2_2 01: SDIO0_CARD_DETECT 10: I2S_WS_TX Other values: reserved

muxctrl_reg47

muxctrl_reg47 is a multiplexing control register for the SDIO0_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg47	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg47	Multiplexing control for the SDIO0_CWPR pin 00: GPIO2_3 01: SDIO0_CWPR 10: I2S_SD_TX Other values: reserved

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muxctrl_reg48

muxctrl_reg48 is a multiplexing control register for the SDIO0_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg48	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg48	Multiplexing control for the SDIO0_CCMD pin 00: GPIO2_4 01: SDIO0_CCMD 10: I2S_BCLK_RX Other values: reserved

muxctrl_reg49

muxctrl_reg49 is a multiplexing control register for the SDIO0_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg49	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg49	Multiplexing control for the SDIO0_CDATA0 pin 00: GPIO2_5 01: SDIO0_CDATA0 10: I2S_WS_RX Other values: reserved

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muxctrl_reg50

muxctrl_reg50 is a multiplexing control register for the SDIO0_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg50	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg50	Multiplexing control for the SDIO0_CDATA1 pin 00: GPIO2_6 01: SDIO0_CDATA1 10: I2S_SD_RX Other values: reserved

muxctrl_reg51

muxctrl_reg51 is a multiplexing control register for the SDIO0_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x0CC	muxctrl_reg51	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg51
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg51	Multiplexing control for the SDIO0_CDATA2 pin 0: GPIO2_7 1: SDIO0_CDATA2

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muxctrl_reg52

muxctrl_reg52 is a multiplexing control register for the SDIO0_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x0D0	muxctrl_reg52	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg52
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg52	Multiplexing control for the SDIO0_CDATA3 pin 0: GPIO1_1 1: SDIO0_CDATA3

muxctrl_reg53

muxctrl_reg53 is a multiplexing control register for the GPIO0_0 pin.

Offset Address	Register Name	Total Reset Value
0x0D4	muxctrl_reg53	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg53
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg53	Multiplexing control for the GPIO0_0 pin 00: SENSOR_RSTN 01: GPIO0_0 10: TEMPER_DQ Other values: reserved

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muxctrl_reg54

muxctrl_reg54 is a multiplexing control register for the GPIO0_1 pin.

Offset Address	Register Name	Total Reset Value
0x0D8	muxctrl_reg54	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg54	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg54	Multiplexing control for the GPIO0_1 pin 00: GPIO0_1 10: TEMPER_DQ Other values: reserved

muxctrl_reg55

muxctrl_reg55 is a multiplexing control register for the GPIO0_2 pin.

Offset Address	Register Name	Total Reset Value
0x0DC	muxctrl_reg55	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg55	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg55	Multiplexing control for the GPIO0_2 pin 00: GPIO0_2 01: PWM5 10: TEMPER_DQ Other values: reserved

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muxctrl_reg56

muxctrl_reg56 is a multiplexing control register for the GPIO0_3 pin.

Offset Address	Register Name	Total Reset Value
0x0E0	muxctrl_reg56	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg56	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg56	Multiplexing control for the GPIO0_3 pin 00: GPIO0_3 01: PWM6 10: TEMPER_DQ Other values: reserved

muxctrl_reg57

muxctrl_reg57 is a multiplexing control register for the GPIO0_4 pin.

Offset Address	Register Name	Total Reset Value
0x0E4	muxctrl_reg57	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg57	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg57	Multiplexing control for the GPIO0_4 pin 00: GPIO0_4 01: PWM7 10: TEMPER_DQ Other values: reserved

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muxctrl_reg58

muxctrl_reg58 is a multiplexing control register for the SDIO1_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x0E8	muxctrl_reg58	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg58
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg58	Multiplexing control for the SDIO1_CCLK_OUT pin 0: GPIO11_0 1: SDIO1_CCLK_OUT

muxctrl_reg59

muxctrl_reg59 is a multiplexing control register for the SDIO1_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x0EC	muxctrl_reg59	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg59
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg59	Multiplexing control for the SDIO1_CARD_POWER_EN pin 0: GPIO11_1 1: SDIO1_CARD_POWER_EN

muxctrl_reg60

muxctrl_reg60 is a multiplexing control register for the SDIO1_CARD_DETECT pin.

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Offset Address	Register Name	Total Reset Value
0x0F0	muxctrl_reg60	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg60
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg60	Multiplexing control for the SDIO1_CARD_DETECT pin 0: GPIO11_2 1: SDIO1_CARD_DETECT

muxctrl_reg61

muxctrl_reg61 is a multiplexing control register for the SDIO1_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x0F4	muxctrl_reg61	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg61
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg61	Multiplexing control for the SDIO1_CWPR pin 0: GPIO11_3 1: SDIO1_CWPR

muxctrl_reg62

muxctrl_reg62 is a multiplexing control register for the SDIO1_CCMD pin.

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Offset Address	Register Name	Total Reset Value
0x0F8	muxctrl_reg62	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg62
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg62	Multiplexing control for the SDIO1_CCMD pin 0: GPIO11_4 1: SDIO1_CCMD

muxctrl_reg63

muxctrl_reg63 is a multiplexing control register for the SDIO1_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x0FC	muxctrl_reg63	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg63
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reseved	Reserved
[2:0]	RW	muxctrl_reg63	Multiplexing control for the SDIO1_CDATA0 pin 000: GPIO11_5 001: SDIO1_CDATA0 010: CLK_TEST_OUT0 011: CLK_TEST_OUT1 100: CLK_TEST_OUT2 101: CLK_TEST_OUT3 110: RTC_TEST_CLK 111: OSC_TEST_CLK

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muxctrl_reg64

muxctrl_reg64 is a multiplexing control register for the SDIO1_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x100	muxctrl_reg64	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg64
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reseved	Reserved
[2:0]	RW	muxctrl_reg64	Multiplexing control for the SDIO1_CDATA1 pin 000: PLL_TEST_OUT0 001: SDIO1_CDATA1 010: PLL_TEST_OUT1 011: PLL_TEST_OUT2 100: PLL_TEST_OUT3 101: GPIO11_6 Other values: reserved

muxctrl_reg65

muxctrl_reg65 is a multiplexing control register for the SDIO1_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x104	muxctrl_reg65	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg65
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg65	Multiplexing control for the SDIO1_CDATA2 pin 0: GPIO11_7 1: SDIO1_CDATA2

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muxctrl_reg66

muxctrl_reg66 is a multiplexing control register for the SDIO1_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x108	muxctrl_reg66	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg66
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg66	Multiplexing control for the SDIO1_CDATA3 pin 0: GPIO1_2 1: SDIO1_CDATA3

muxctrl_reg67

muxctrl_reg67 is a multiplexing control register for the NF_DQ0 pin.

Offset Address	Register Name	Total Reset Value
0x10C	muxctrl_reg67	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg67
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg67	Multiplexing control for the NF_DQ0 pin 0: NF_DQ0 1: GPIO5_0

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muxctrl_reg68

muxctrl_reg68 is a multiplexing control register for the NF_DQ1 pin.

Offset Address	Register Name	Total Reset Value
0x110	muxctrl_reg68	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg68
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg68	Multiplexing control for the NF_DQ1 pin 0: NF_DQ1 1: GPIO5_1

muxctrl_reg69

muxctrl_reg69 is a multiplexing control register for the NF_DQ2 pin.

Offset Address	Register Name	Total Reset Value
0x114	muxctrl_reg69	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg69
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg69	Multiplexing control for the NF_DQ2 pin 0: NF_DQ2 1: GPIO5_2

muxctrl_reg70

muxctrl_reg70 is a multiplexing control register for the NF_DQ3 pin.

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Offset Address	Register Name	Total Reset Value
0x118	muxctrl_reg70	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg70
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg70	Multiplexing control for the NF_DQ3 pin 0: NF_DQ3 1: GPIO5_3

muxctrl_reg71

muxctrl_reg71 is a multiplexing control register for the NF_DQ4 pin.

Offset Address	Register Name	Total Reset Value
0x11C	muxctrl_reg71	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg71
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg71	Multiplexing control for the NF_DQ4 pin 0: NF_DQ4 1: GPIO5_4

muxctrl_reg72

muxctrl_reg72 is a multiplexing control register for the NF_DQ5 pin.

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Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg72
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg72	Multiplexing control for the NF_DQ5 pin 0: NF_DQ5 1: GPIO5_5

muxctrl_reg73

muxctrl_reg73 is a multiplexing control register for the NF_DQ6 pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg73
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg73	Multiplexing control for the NF_DQ6 pin 0: NF_DQ6 1: GPIO5_6

muxctrl_reg74

muxctrl_reg74 is a multiplexing control register for the NF_DQ7 pin.

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Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg74
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg74	Multiplexing control for the NF_DQ7 pin 0: NF_DQ7 1: GPIO5_7

muxctrl_reg75

muxctrl_reg75 is a multiplexing control register for the NF_RDY0 pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg75
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg75	Multiplexing control for the NF_RDY0 pin 0: NF_RDY0 1: GPIO3_0

muxctrl_reg76

muxctrl_reg76 is a multiplexing control register for the NF_RDY1 pin.

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Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg76
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg76	Multiplexing control for the NF_RDY1 pin 0: NF_RDY1 1: GPIO3_1

muxctrl_reg77

muxctrl_reg77 is a multiplexing control register for the NF_REN pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg77
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg77	Multiplexing control for the NF_REN pin 0: NF_REN 1: GPIO3_2

muxctrl_reg78

muxctrl_reg78 is a multiplexing control register for the NF_CSN0 pin.

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Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg78
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg78	Multiplexing control for the NF_CSN0 pin 0: NF_CSN0 1: GPIO3_3

muxctrl_reg79

muxctrl_reg79 is a multiplexing control register for the NF_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg79
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg79	Multiplexing control for the NF_CSN1 pin 00: NF_CSN1 01: GPIO3_4 10: SFC_CSN0 Other values: reserved

muxctrl_reg80

muxctrl_reg80 is a multiplexing control register for the NF_CLE pin.

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Offset Address	Register Name	Total Reset Value
0x140	muxctrl_reg80	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg80	Multiplexing control for the NF_CLE pin 0: NF_CLE 1: GPIO3_5

muxctrl_reg81

muxctrl_reg81 is a multiplexing control register for the NF_ALE pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg81
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg81	Multiplexing control for the NF_ALE pin 0: NF_ALE 1: GPIO3_6

muxctrl_reg82

muxctrl_reg82 is a multiplexing control register for the NF_WEN pin.

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Offset Address	Register Name	Total Reset Value
0x148	muxctrl_reg82	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg82	Multiplexing control for the NF_WEN pin 0: NF_WEN 1: GPIO3_7

muxctrl_reg83

muxctrl_reg83 is a multiplexing control register for the PWM0 pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg83
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg83	Multiplexing control for the PWM0 pin 00: PWM0 01: GPIO14_0 10: PMC_I2C_SCL Other values: reserved

muxctrl_reg84

muxctrl_reg84 is a multiplexing control register for the PWM1 pin.

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Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg84	Multiplexing control for the PWM1 pin 00: PWM1 01: GPIO14_1 10: PMC_I2C_SDA Other values: reserved

muxctrl_reg85

muxctrl_reg85 is a multiplexing control register for the PWM2 pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg85	Multiplexing control for the PWM2 pin 0: PWM2 1: GPIO14_2

muxctrl_reg86

muxctrl_reg86 is a multiplexing control register for the PWM3 pin.

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Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg86	Multiplexing control for the PWM3 pin 0: PWM3 1: GPIO14_3

muxctrl_reg87

muxctrl_reg87 is a multiplexing control register for the SAR_ADC_CH0 pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg87	Multiplexing control for the SAR_ADC_CH0 pin 0: SAR_ADC_CH0 1: GPIO1_6

muxctrl_reg88

muxctrl_reg88 is a multiplexing control register for the SAR_ADC_CH1 pin.

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Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg88	Multiplexing control for the SAR_ADC_CH1 pin 0: SAR_ADC_CH1 1: GPIO1_7

muxctrl_reg89

muxctrl_reg89 is a multiplexing control register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg89	Multiplexing control for the EPHY_CLK pin 0: GPIO14_4 1: EPHY_CLK

muxctrl_reg90

muxctrl_reg90 is a multiplexing control register for the MDCK pin.

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Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg90
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg90	Multiplexing control for the MDCK pin 0: GPIO14_5 1: MDCK

muxctrl_reg91

muxctrl_reg91 is a multiplexing control register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg91
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg91	Multiplexing control for the MDIO pin 0: GPIO14_6 1: MDIO

muxctrl_reg92

muxctrl_reg92 is a multiplexing control register for the RGMII_TX_EN pin.

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Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg92
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg92	Multiplexing control for the RGMII_TX_EN pin 0: GPIO14_7 1: RGMII_TX_EN

muxctrl_reg93

muxctrl_reg93 is a multiplexing control register for the RGMII_TX_CLK pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg93	Multiplexing control for the RGMII_TX_CLK pin 00: GPIO4_0 01: RGMII_TX_CLK 10: RMII_CLK_OUT/MII_TX_CLK Other values: reserved

muxctrl_reg94

muxctrl_reg94 is a multiplexing control register for the RGMII_TXD0 pin.

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Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg94
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg94	Multiplexing control for the RGMII_TXD0 pin 0: GPIO4_1 1: RGMII_TXD0

muxctrl_reg95

muxctrl_reg95 is a multiplexing control register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x17C	muxctrl_reg95	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg95
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg95	Multiplexing control for the RGMII_TXD1 pin 0: GPIO4_2 1: RGMII_TXD1

muxctrl_reg96

muxctrl_reg96 is a multiplexing control register for the RGMII_TXD2 pin.

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Offset Address	Register Name	Total Reset Value
0x180	muxctrl_reg96	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg96
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg96	Multiplexing control for the RGMII_TXD2 pin 0: GPIO4_3 1: RGMII_TXD2

muxctrl_reg97

muxctrl_reg97 is a multiplexing control register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x184	muxctrl_reg97	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg97
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg97	Multiplexing control for the RGMII_TXD3 pin 0: GPIO4_4 1: RGMII_TXD3

muxctrl_reg98

muxctrl_reg98 is a multiplexing control register for the RGMII_RX_CLK pin.

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Offset Address	Register Name	Total Reset Value
0x188	muxctrl_reg98	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg98
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg98	Multiplexing control for the RGMII_RX_CLK pin 0: GPIO4_5 1: RGMII_RX_CLK

muxctrl_reg99

muxctrl_reg99 is a multiplexing control register for the RGMII_RX_DV pin.

Offset Address	Register Name	Total Reset Value
0x18C	muxctrl_reg99	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg99
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg99	Multiplexing control for the RGMII_RX_DV pin 0: GPIO4_6 1: RGMII_RX_DV

muxctrl_reg100

muxctrl_reg100 is a multiplexing control register for the RGMII_RXD0 pin.

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Offset Address	Register Name	Total Reset Value
0x190	muxctrl_reg100	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg100
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg100	Multiplexing control for the RGMII_RXD0 pin 0: GPIO4_7 1: RGMII_RXD0

muxctrl_reg101

muxctrl_reg101 is a multiplexing control register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x194	muxctrl_reg101	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg101
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg101	Multiplexing control for the RGMII_RXD1 pin 0: GPIO1_3 1: RGMII_RXD1

muxctrl_reg102

muxctrl_reg102 is a multiplexing control register for the RGMII_RXD2 pin.

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Offset Address	Register Name	Total Reset Value
0x198	muxctrl_reg102	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg102
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg102	Multiplexing control for the RGMII_RXD2 pin 0: GPIO1_4 1: RGMII_RXD2

muxctrl_reg103

muxctrl_reg103 is a multiplexing control register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x19C	muxctrl_reg103	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg103
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg103	Multiplexing control for the RGMII_RXD3 pin 0: GPIO1_5 1: RGMII_RXD3

muxctrl_reg104

muxctrl_reg104 is a multiplexing control register for the VI_CLK pin.

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Offset Address	Register Name	Total Reset Value
0x1A0	muxctrl_reg104	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg104
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reseved	Reserved
[0]	RW	muxctrl_reg104	Multiplexing control for the VI_CLK pin 0: GPIO15_0 1: VI_CLK

muxctrl_reg105

muxctrl_reg105 is a multiplexing control register for the VI_HS pin.

Offset Address	Register Name	Total Reset Value
0x1A4	muxctrl_reg105	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg105
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg105	Multiplexing control for the VI_HS pin 00: GPIO15_1 01: VI_HS Other values: reserved

muxctrl_reg106

muxctrl_reg106 is a multiplexing control register for the VI_VS pin.

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Offset Address	Register Name	Total Reset Value
0x1A8	muxctrl_reg106	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								muxctrl_reg 106	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg106	Multiplexing control for the VI_VS pin 00: GPIO15_2 01: VI_VS Other values: reserved

muxctrl_reg107

muxctrl_reg107 is a multiplexing control register for the VI_DAT15 pin.

Offset Address	Register Name	Total Reset Value
0x1AC	muxctrl_reg107	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								muxctrl_reg 107	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg107	Multiplexing control for the VI_DAT15 pin 00: GPIO12_0 01: VI_DAT15 10: I2S_MCLK Other values: reserved

muxctrl_reg108

muxctrl_reg108 is a multiplexing control register for the VI_DAT14 pin.

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Offset Address	Register Name	Total Reset Value
0x1B0	muxctrl_reg108	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								muxctrl_reg 108	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg108	Multiplexing control for the VI_DAT14 pin 00: GPIO12_1 01: VI_DAT14 10: I2S_BCLK_TX Other values: reserved

muxctrl_reg109

muxctrl_reg109 is a multiplexing control register for the VI_DAT13 pin.

Offset Address	Register Name	Total Reset Value
0x1B4	muxctrl_reg109	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								muxctrl_reg 109	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg109	Multiplexing control for the VI_DAT13 pin 00: GPIO12_2 01: VI_DAT13 10: I2S_WS_TX Other values: reserved

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muxctrl_reg110

muxctrl_reg110 is a multiplexing control register for the VI_DAT12 pin.

Offset Address	Register Name	Total Reset Value
0x1B8	muxctrl_reg110	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 110	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg110	Multiplexing control for the VI_DAT12 pin 00: GPIO12_3 01: VI_DAT12 10: I2S_SD_TX Other values: reserved

muxctrl_reg111

muxctrl_reg111 is a multiplexing control register for the VI_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x1BC	muxctrl_reg111	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 111	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg111	Multiplexing control for the VI_DAT11 pin 00: GPIO12_4 01: VI_DAT11 10: I2S_BCLK_RX Other values: reserved

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muxctrl_reg112

muxctrl_reg112 is a multiplexing control register for the VI_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x1C0	muxctrl_reg112	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 112	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg112	Multiplexing control for the VI_DAT10 pin 00: GPIO12_5 01: VI_DAT10 10: I2S_WS_RX Other values: reserved

muxctrl_reg113

muxctrl_reg113 is a multiplexing control register for the VI_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x1C4	muxctrl_reg113	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 113	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg113	Multiplexing control for the VI_DAT9 pin 00: GPIO12_6 01: VI_DAT9 10: I2S_SD_RX Other values: reserved

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muxctrl_reg114

muxctrl_reg114 is a multiplexing control register for the VI_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x1C8	muxctrl_reg114	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 114	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg114	Multiplexing control for the VI_DAT8 pin 00: GPIO12_7 01: VI_DAT8 Other values: reserved

muxctrl_reg115

muxctrl_reg115 is a multiplexing control register for the VI_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x1CC	muxctrl_reg115	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 115	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg115	Multiplexing control for the VI_DAT7 pin 00: GPIO13_0 01: VI_DAT7 Other values: reserved

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muxctrl_reg116

muxctrl_reg116 is a multiplexing control register for the VI_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x1D0	muxctrl_reg116	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 116	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg116	Multiplexing control for the VI_DAT6 pin 00: GPIO13_1 01: VI_DAT6 Other values: reserved

muxctrl_reg117

muxctrl_reg117 is a multiplexing control register for the VI_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x1D4	muxctrl_reg117	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 117	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg117	Multiplexing control for the VI_DAT5 pin 00: GPIO13_2 01: VI_DAT5 Other values: reserved

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muxctrl_reg118

muxctrl_reg118 is a multiplexing control register for the VI_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x1D8	muxctrl_reg118	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 118	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg118	Multiplexing control for the VI_DAT4 pin 00: GPIO13_3 01: VI_DAT4 Other values: reserved

muxctrl_reg119

muxctrl_reg119 is a multiplexing control register for the VI_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x1DC	muxctrl_reg119	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 119	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg119	Multiplexing control for the VI_DAT3 pin 00: GPIO13_4 01: VI_DAT3 Other values: reserved

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muxctrl_reg120

muxctrl_reg120 is a multiplexing control register for the VI_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x1E0	muxctrl_reg120	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 120	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg120	Multiplexing control for the VI_DAT2 pin 00: GPIO13_5 01: VI_DAT2 Other values: reserved

muxctrl_reg121

muxctrl_reg121 is a multiplexing control register for the VI_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x1E4	muxctrl_reg121	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 121	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg121	Multiplexing control for the VI_DAT1 pin 00: GPIO13_6 01: VI_DAT1 Other values: reserved

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muxctrl_reg122

muxctrl_reg122 is a multiplexing control register for the VI_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x1E8	muxctrl_reg122	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 122	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reseved	Reserved
[1:0]	RW	muxctrl_reg122	Multiplexing control for the VI_DAT0 pin 00: GPIO13_7 01: VI_DAT0 11: PWM4 Other values: reserved

2.4 Software Multiplexed Pins

Sensor

Table 2-38 lists software multiplexed sensor pins.

Table 2-38 Software multiplexed sensor pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AA1	SENSOR_CLK	muxctrl_reg0	GPIO0_5	SENSOR_CLK	None
Y15	FLASH_TRIG	muxctrl_reg1	GPIO0_6	FLASH_TRIG	SPI1_CSN1
W15	SHUTTER_TRIG	muxctrl_reg2	GPIO0_7	SHUTTER_TRIG	SPI1_CSN2

Table 2-39 describes software multiplexed sensor signals.

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Table 2-39 Description of software multiplexed sensor signals

Signal	Direction	Description
FLASH_TRIG	O	Camera flash control
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
SENSOR_CLK	O	Sensor working clock
SHUTTER_TRIG	O	Shutter control
SPI1_CSN1	O	SPI1 CS1
SPI1_CSN2	O	SPI1 CS2

VO

Table 2-40 lists software multiplexed VO pins.

Table 2-40 Software multiplexed VO pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
G22	VO_CLK	muxctrl_reg3	GPIO1_0	VO_CLK	None
C22	VO_DAT15	muxctrl_reg4	GPIO6_0	VO_DAT15	None
E20	VO_DAT14	muxctrl_reg5	GPIO6_1	VO_DAT14	None
D21	VO_DAT13	muxctrl_reg6	GPIO6_2	VO_DAT13	None
D22	VO_DAT12	muxctrl_reg7	GPIO6_3	VO_DAT12	None
E21	VO_DAT11	muxctrl_reg8	GPIO6_4	VO_DAT11	SFC_NAND_BOOT_PIN2
F20	VO_DAT10	muxctrl_reg9	GPIO6_5	VO_DAT10	SFC_NAND_BOOT_PIN1
E22	VO_DAT9	muxctrl_reg10	GPIO6_6	VO_DAT9	SFC_NAND_BOOT_PIN0
F19	VO_DAT8	muxctrl_reg11	GPIO6_7	VO_DAT8	None
F21	VO_DAT7	muxctrl_reg12	GPIO7_0	VO_DAT7	None
G20	VO_DAT6	muxctrl_reg13	GPIO7_1	VO_DAT6	None
F22	VO_DAT5	muxctrl_reg14	GPIO7_2	VO_DAT5	None
G21	VO_DAT4	muxctrl_reg15	GPIO7_3	VO_DAT4	None
G19	VO_DAT3	muxctrl_reg16	GPIO7_4	VO_DAT3	SFC_DEVICE_MODE
H21	VO_DAT2	muxctrl_reg17	GPIO7_5	VO_DAT2	None

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Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
H19	VO_DAT1	muxctrl_reg18	GPIO7_6	VO_DAT1	BOOTROM_SEL
H20	VO_DAT0	muxctrl_reg19	GPIO7_7	VO_DAT0	BOOT_SEL

Table 2-41 describes software multiplexed VO signals.

Table 2-41 Description of software multiplexed VO signals

Signal	Direction	Description
BOOT_SEL	I	BOOT_SEL 0: booting from the storage space of the SPI flash 1: booting from the storage space of the NAND flash
BOOTROM_SEL	I	BOOTROM boot enable 0: booting from the other space (determined by BOOT_Sel) 1: booting from the BOOTROM
GPIO1_0	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
GPIO6_2	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
GPIO7_5	I/O	GPIO
GPIO7_6	I/O	GPIO
GPIO7_7	I/O	GPIO

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Signal	Direction	Description
SFC_DEVICE_MODE	I	SPI flash select 0: SPI NOR flash 1: SPI NAND flash
SFC_NAND_BOOT_PIN0	I	SPI NAND flash configuration. This function is valid only during power-on. {SF_NAND_BOOT_PIN1, SF_NAND_BOOT_PIN0} indicate the ECC type. 00: reserved 01: 8-bit ECC 10: reserved 11: 24-bit ECC
SFC_NAND_BOOT_PIN1	I	SPI NAND flash configuration. This function is valid only during power-on. {SF_NAND_BOOT_PIN1, SF_NAND_BOOT_PIN0} indicate the ECC type. 00: reserved 01: 8-bit ECC 10: reserved 11: 24-bit ECC
SFC_NAND_BOOT_PIN2	I	SPI NAND flash configuration. This function is valid only during power-on. SF_NAND_BOOT_PIN2 indicates the page size. 0: 2 KB page size 1: 4 KB page size
VO_CLK	O	VO output clock
VO_DAT0	O	VO output data 0
VO_DAT1	O	VO output data 1
VO_DAT2	O	VO output data 2
VO_DAT3	O	VO output data 3
VO_DAT4	O	VO output data 4
VO_DAT5	O	VO output data 5
VO_DAT6	O	VO output data 6
VO_DAT7	O	VO output data 7
VO_DAT8	O	VO output data 8
VO_DAT9	O	VO output data 9
VO_DAT10	O	VO output data 10

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Signal	Direction	Description
VO_DAT11	O	VO output data 11
VO_DAT12	O	VO output data 12
VO_DAT13	O	VO output data 13
VO_DAT14	O	VO output data 14
VO_DAT15	O	VO output data 15

SPI0

Table 2-42 lists software multiplexed SPI0 pins.

Table 2-42 Software multiplexed SPI0 pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AB2	SPI0_SCLK	muxctrl_reg20	GPIO8_0	SPI0_SCLK	I2C0_SCL
Y2	SPI0_SDO	muxctrl_reg21	GPIO8_1	SPI0_SDO	I2C0_SDA
AA2	SPI0_SDI	muxctrl_reg22	GPIO8_2	SPI0_SDI	None
Y3	SPI0_CSN	muxctrl_reg23	GPIO8_3	SPI0_CSN	None

Table 2-43 describes software multiplexed SPI0 signals.

Table 2-43 Description of software multiplexed SPI0 signals

Signal	Direction	Description
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
GPIO8_3	I/O	GPIO
I2C0_SCL	I/O	I^2C0 bus clock
I2C0_SDA	I/O	I^2C0 bus data/address
SPI0_CSN	O	SPI0 CS
SPI0_SCLK	O	SPI0 clock
SPI0_SDI	I	SPI0 input data
SPI0_SDO	O	SPI0 output data

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SPI1

Table 2-44 lists software multiplexed SPI1 pins.

Table 2-44 Software multiplexed SPI1 pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AA16	SPI1_SCLK	muxctrl_reg24	GPIO8_4	SPI1_SCLK	I2C1_SCL
Y16	SPI1_SDO	muxctrl_reg25	GPIO8_5	SPI1_SDO	I2C1_SDA
W16	SPI1_SDI	muxctrl_reg26	GPIO8_6	SPI1_SDI	None
Y17	SPI1_CSN0	muxctrl_reg27	GPIO8_7	SPI1_CSN0	None

Table 2-45 describes software multiplexed SPI1 signals.

Table 2-45 Description of software multiplexed SPI1 signals

Signal	Direction	Description
GPIO8_4	I/O	GPIO
GPIO8_5	I/O	GPIO
GPIO8_6	I/O	GPIO
GPIO8_7	I/O	GPIO
I2C1_SCL	I/O	I^2C1 bus clock
I2C1_SDA	I/O	I^2C1 bus data/address
SPI1_CSN0	O	SPI1 CS0
SPI1_SCLK	O	SPI1 clock
SPI1_SDI	I	SPI1 input data
SPI1_SDO	O	SPI1 output data

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I²C2

Table 2-46 lists the software multiplexed I²C2 pins.

Table 2-46 Software multiplexed I²C2 pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
AA20	I2C2_SDA	muxctrl_reg28	GPIO9_0	I2C2_SDA
AB21	I2C2_SCL	muxctrl_reg29	GPIO9_1	I2C2_SCL

Table 2-47 describes software multiplexed I²C2 signals.

Table 2-47 Description of software multiplexed I²C2 signals

Signal	Direction	Description
GPIO9_0	I/O	GPIO
GPIO9_1	I/O	GPIO
I2C2_SCL	I/O	I²C2 bus clock
I2C2_SDA	I/O	I²C2 bus data/address

UART

Table 2-48 lists software multiplexed UART pins.

Table 2-48 Software multiplexed UART pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
Y19	UART1_RTSN	muxctrl_reg30	GPIO9_2	UART1_RTSN	UART3_RXD
Y22	UART1_RXD	muxctrl_reg31	GPIO9_3	UART1_RXD	None
W20	UART1_CTSN	muxctrl_reg32	GPIO9_4	UART1_CTSN	UART3_TXD
W22	UART1_TXD	muxctrl_reg33	GPIO9_5	UART1_TXD	None

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Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AA17	UART2_RXD	muxctrl_reg34	GPIO9_6	UART2_RXD	I2S_BCLK_RX
V22	UART2_TXD	muxctrl_reg35	GPIO9_7	UART2_TXD	I2S_WS_RX

Table 2-49 describes software multiplexed UART signals.

Table 2-49 Description of software multiplexed UART signals

Signal	Direction	Description
GPIO9_2	I/O	GPIO
GPIO9_3	I/O	GPIO
GPIO9_4	I/O	GPIO
GPIO9_5	I/O	GPIO
GPIO9_6	I/O	GPIO
GPIO9_7	I/O	GPIO
I2S_BCLK_RX	I/O	RX clock of the I^2S or PCM interface
I2S_WS_RX	I/O	I^2S RX audio channel select signal or PCM TX frame sync signal
UART1_CTSN	I	UART1 modem status input, active low
UART1_RTSN	O	UART1 modem status output, active low
UART1_RXD	I	UART1 RX data
UART1_TXD	O	UART1 TX data
UART2_RXD	I	UART2 RX data
UART2_TXD	O	UART2 TX data
UART3_RXD	I	UART3 RX data
UART3_TXD	O	UART3 TX data

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JTAG

Table 2-50 lists software multiplexed JTAG pins.

Table 2-50 Software multiplexed JTAG pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AB17	JTAG_TRSTN	muxctrl_reg36	GPIO10_0	JTAG_TRSTN	I2S_MCLK
Y18	JTAG_TCK	muxctrl_reg37	GPIO10_1	JTAG_TCK	I2S_BCLK_TX
AB19	JTAG_TMS	muxctrl_reg38	GPIO10_2	JTAG_TMS	I2S_WS_TX
W18	JTAG_TDO	muxctrl_reg39	GPIO10_3	JTAG_TDO	I2S_SD_RX
AA19	JTAG_TDI	muxctrl_reg40	GPIO10_4	JTAG_TDI	I2S_SD_TX

Table 2-51 describes software multiplexed JTAG signals.

Table 2-51 Description of software multiplexed JTAG signals

Signal	Direction	Description
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
GPIO10_2	I/O	GPIO
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
I2S_BCLK_TX	I/O	TX clock of I^2S or PCM interface
I2S_MCLK	O	Main clock of the I^2S or PCM interface. It can act as the main clock of the ACODEC.
I2S_SD_RX	I	RX data input of the I^2S or PCM interface
I2S_SD_TX	O	TX data output of the I^2S or PCM interface
I2S_WS_TX	I/O	I^2S TX audio channel select signal or PCM TX frame sync signal
JTAG_TCK	I	JTAG clock
JTAG_TDI	I	JTAG input data
JTAG_TDO	O	JTAG output data

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Signal	Direction	Description
JTAG_TMS	I/O	JTAG mode select input or data output for software trace. The modes are controlled by using the CPU.
JTAG_TRSTN	I	JTAG reset

IR

Table 2-52 lists the software multiplexed IR pin.

Table 2-52 Software multiplexed IR pin

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
AB20	IR_IN	muxctrl_reg41	GPIO10_5	IR_IN	PWM4

Table 2-53 describes software multiplexed IR signals.

Table 2-53 Description of software multiplexed IRsignals

Signal	Direction	Description
GPIO10_5	I/O	GPIO
IR_IN	I	Infrared input
PWM4	O	PWM output 4

USB

Table 2-54 lists the software multiplexed USB pins.

Table 2-54 Software multiplexed USB pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V21	USB_OVRCUR	muxctrl_reg42	GPIO10_6	USB_OVRCUR
V19	USB_PWREN	muxctrl_reg43	GPIO10_7	USB_PWREN

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Table 2-55 describes software multiplexed USB signals.

Table 2-55 Description of software multiplexed USB signals

Signal	Direction	Description
GPIO10_6	I/O	GPIO
GPIO10_7	I/O	GPIO
USB_OVRCUR	I	USB port overcurrent indicator. The level polarity can be specified by configuring the peripheral control register MISC_CTRL30 bit[17].
USB_PWREN	O	Power control output pin of the USB port. The level polarity can be specified by configuring the peripheral control register MISC_CTRL30 bit[16].

SDIO0

Table 2-56 lists the software multiplexed SDIO0 pins.

Table 2-56 Software multiplexed SDIO0 pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
L22	SDIO0_CCLK_OUT	muxctrl_reg44	GPIO2_0	SDIO0_CCLK_OUT	I2S_MCLK
N20	SDIO0_CARD_POWER_EN	muxctrl_reg45	GPIO2_1	SDIO0_CARD_POWER_EN	I2S_BCLK_TX
N19	SDIO0_CARD_DETECT	muxctrl_reg46	GPIO2_2	SDIO0_CARD_DETECT	I2S_WS_TX
M22	SDIO0_CWPR	muxctrl_reg47	GPIO2_3	SDIO0_CWPR	I2S_SD_TX
M20	SDIO0_CCMD	muxctrl_reg48	GPIO2_4	SDIO0_CCMD	I2S_BCLK_RX
M19	SDIO0_CDATA0	muxctrl_reg49	GPIO2_5	SDIO0_CDATA0	I2S_WS_RX
L21	SDIO0_CDATA1	muxctrl_reg50	GPIO2_6	SDIO0_CDATA1	I2S_SD_RX
L20	SDIO0_CDATA2	muxctrl_reg51	GPIO2_7	SDIO0_CDATA2	None
M21	SDIO0_CDATA3	muxctrl_reg52	GPIO1_1	SDIO0_CDATA3	None

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Table 2-57 describes software multiplexed SDIO0 signals.

Table 2-57 Description of software multiplexed SDIO0 signals

Signal	Direction	Description
GPIO1_1	I/O	GPIO
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_4	I/O	GPIO
GPIO2_5	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
I2S_BCLK_RX	I/O	RX clock of the I^2S or PCM interface
I2S_BCLK_TX	I/O	TX clock of the I^2S or PCM interface
I2S_MCLK	O	Main clock of the I^2S or PCM interface. It can act as the main clock of the ACODEC.
I2S_SD_RX	I	RX data input of the I^2S or PCM interface
I2S_SD_TX	O	TX data output of the I^2S or PCM interface
I2S_WS_RX	I/O	I^2S RX audio channel select signal or PCM TX frame sync signal
I2S_WS_TX	I/O	I^2S TX audio channel select signal or PCM TX frame sync signal
SDIO0_CARD_DETECT	I	SDIO0 card detection signal, active low
SDIO0_CARD_POWER_EN	O	SDIO0 power enable signal. The value 1 indicates power-on.
SDIO0_CCLK_OUT	O	SDIO0 output working clock for the card
SDIO0_CCMD	I/O	SDIO0 command
SDIO0_CDATA0	I/O	SDIO0 data 0
SDIO0_CDATA1	I/O	SDIO0 data 1
SDIO0_CDATA2	I/O	SDIO0 data 2
SDIO0_CDATA3	I/O	SDIO0 data 3
SDIO0_CWPR	I	SDIO0 card write protection detection

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GPIO

Table 2-58 lists the software multiplexed GPIO pins.

Table 2-58 Software multiplexed GPIO pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
Y1	GPIO0_0	muxctrl_reg53	SENSOR_RSTN	GPIO0_0	TEMPER_DQ
D20	GPIO0_1	muxctrl_reg54	GPIO0_1	TEMPER_DQ	None
AB18	GPIO0_2	muxctrl_reg55	GPIO0_2	PWM5	TEMPER_DQ
AB16	GPIO0_3	muxctrl_reg56	GPIO0_3	PWM6	TEMPER_DQ
Y20	GPIO0_4	muxctrl_reg57	GPIO0_4	PWM7	TEMPER_DQ

Table 2-59 describes software multiplexed GPIO signals.

Table 2-59 Description of software multiplexed GPIO signals

Signal	Direction	Description
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
GPIO0_3	I/O	GPIO
GPIO0_4	I/O	GPIO
PWM5	O	PWM output 5
PWM6	O	PWM output 6
PWM7	O	PWM output 7
SENSOR_RSTN	O	Sensor reset signal
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.

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SDIO1

Table 2-60 lists the software multiplexed SDIO1 pins.

Table 2-60 Software multiplexed SDIO1 pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1–7
K22	SDIO1_CCLK_OUT	muxctrl_reg58	GPIO11_0	1: SDIO1_CCLK_OUT
J21	SDIO1_CARD_POWER_EN	muxctrl_reg59	GPIO11_1	1: SDIO1_CARD_POWER_EN
J20	SDIO1_CARD_DETECT	muxctrl_reg60	GPIO11_2	1: SDIO1_CARD_DETECT
J19	SDIO1_CWPR	muxctrl_reg61	GPIO11_3	1: SDIO1_CWPR
K21	SDIO1_CCMD	muxctrl_reg62	GPIO11_4	1: SDIO1_CCMD
K20	SDIO1_CDATA0	muxctrl_reg63	GPIO11_5	1: SDIO1_CDATA0 2: CLK_TEST_OUT0 3: CLK_TEST_OUT1 4: CLK_TEST_OUT2 5: CLK_TEST_OUT3 6: RTC_TEST_CLK 7: OSC_TEST_CLK
J22	SDIO1_CDATA1	muxctrl_reg64	PLL_TEST_OUT0	1: SDIO1_CDATA1 2: PLL_TEST_OUT1 3: PLL_TEST_OUT2 4: PLL_TEST_OUT3 5: GPIO11_6
L19	SDIO1_CDATA2	muxctrl_reg65	GPIO11_7	1: SDIO1_CDATA2
K19	SDIO1_CDATA3	muxctrl_reg66	GPIO1_2	1: SDIO1_CDATA3

Table 2-61 describes software multiplexed SDIO1 signals.

Table 2-61 Description of software multiplexed SDIO1 signals

Signal	Direction	Description
CLK_TEST_OUT0	O	Main test clock 0
CLK_TEST_OUT1	O	Main test clock 1
CLK_TEST_OUT2	O	Main test clock 2
CLK_TEST_OUT3	O	Main test clock 3

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Signal	Direction	Description
GPIO1_2	I/O	GPIO
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
GPIO11_2	I/O	GPIO
GPIO11_3	I/O	GPIO
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO11_6	I/O	GPIO
GPIO11_7	I/O	GPIO
OSC_TEST_CLK	O	System crystal oscillator test clock
PLL_TEST_OUT0	O	PLL test clock 0
PLL_TEST_OUT1	O	PLL test clock 1
PLL_TEST_OUT2	O	PLL test clock 2
PLL_TEST_OUT3	O	PLL test clock 3
RTC_TEST_CLK	O	RTC test clock
SDIO1_CARD_DETECT	I	SDIO1 card detection signal, active low
SDIO1_CARD_POWER_EN	O	SDIO1 power enable signal. The value 1 indicates power-on.
SDIO1_CCLK_OUT	O	SDIO1 output working clock for the card
SDIO1_CCMD	I/O	SDIO1 command
SDIO1_CDATA0	I/O	SDIO1 data 0
SDIO1_CDATA1	I/O	SDIO1 data 1
SDIO1_CDATA2	I/O	SDIO1 data 2
SDIO1_CDATA3	I/O	SDIO1 data 3
SDIO1_CWPR	I	SDIO1 card write protection detection

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NFC

Table 2-62 lists the software multiplexed NFC pins.

Table 2-62 Software multiplexed NFC pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
N3	NF_DQ0	muxctrl_reg67	NF_DQ0	GPIO5_0	None
L4	NF_DQ1	muxctrl_reg68	NF_DQ1	GPIO5_1	None
K4	NF_DQ2	muxctrl_reg69	NF_DQ2	GPIO5_2	None
K3	NF_DQ3	muxctrl_reg70	NF_DQ3	GPIO5_3	None
L3	NF_DQ4	muxctrl_reg71	NF_DQ4	GPIO5_4	None
M3	NF_DQ5	muxctrl_reg72	NF_DQ5	GPIO5_5	None
M4	NF_DQ6	muxctrl_reg73	NF_DQ6	GPIO5_6	None
N4	NF_DQ7	muxctrl_reg74	NF_DQ7	GPIO5_7	None
K1	NF_RDY0	muxctrl_reg75	NF_RDY0	GPIO3_0	None
K2	NF_RDY1	muxctrl_reg76	NF_RDY1	GPIO3_1	None
L2	NF_REN	muxctrl_reg77	NF_REN	GPIO3_2	None
L1	NF_CSN0	muxctrl_reg78	NF_CSN0	GPIO3_3	None
M2	NF_CSN1	muxctrl_reg79	NF_CSN1	GPIO3_4	SFC_CSN0
M1	NF_CLE	muxctrl_reg80	NF_CLE	GPIO3_5	None
N2	NF_ALE	muxctrl_reg81	NF_ALE	GPIO3_6	None
N1	NF_WEN	muxctrl_reg82	NF_WEN	GPIO3_7	None

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Table 2-63 describes software multiplexed NFC signals.

Table 2-63 Description of software multiplexed NFC signals

Signal	Direction	Description
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
GPIO5_0	I/O	GPIO
GPIO5_1	I/O	GPIO
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
GPIO5_4	I/O	GPIO
GPIO5_5	I/O	GPIO
GPIO5_6	I/O	GPIO
GPIO5_7	I/O	GPIO
NF_ALE	O	Address latch signal of the NAND flash
NF_CLE	O	Command latch signal of the NAND flash
NF_CSN0	O	CS0 of the NAND flash (active low) for mounting the NAND flash from which the system boots
NF_CSN1	O	CS1 of the NAND flash, active low
NF_DQ0	I/O	Data bus 0 of the NAND flash
NF_DQ1	I/O	Data bus 1 of the NAND flash
NF_DQ2	I/O	Data bus 2 of the NAND flash
NF_DQ3	I/O	Data bus 3 of the NAND flash
NF_DQ4	I/O	Data bus 4 of the NAND flash
NF_DQ5	I/O	Data bus 5 of the NAND flash
NF_DQ6	I/O	Data bus 6 of the NAND flash

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Signal	Direction	Description
NF_DQ7	I/O	Data bus 7 of the NAND flash
NF_RDY0	I	Status indicator signal 0 of the NAND flash 0: busy 1: idle
NF_RDY1	I	Status indicator signal 1 of the NAND flash 0: busy 1: idle
NF_REN	O	Read enable signal of the NAND flash, active low
NF_WEN	O	Write enable signal of the NAND flash, active low
SFC_CSN0	O	CS0 of the SPI flash, active low

PWM

Table 2-64 lists the software multiplexed PWM pins.

Table 2-64 Software multiplexed PWM pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
V20	PWM0	muxctrl_reg83	PWM0	GPIO14_0	PMC_I2C_SCL
W19	PWM1	muxctrl_reg84	PWM1	GPIO14_1	PMC_I2C_SDA
AA22	PWM2	muxctrl_reg85	PWM2	GPIO14_2	None
AA21	PWM3	muxctrl_reg86	PWM3	GPIO14_3	None

Table 2-65 describes software multiplexed PWM signals.

Table 2-65 Description of software multiplexed PWM signals

Signal	Direction	Description
GPIO14_0	I/O	GPIO
GPIO14_1	I/O	GPIO
GPIO14_2	I/O	GPIO
GPIO14_3	I/O	GPIO
PWM0	O	PWM output 0

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Signal	Direction	Description
PWM1	O	PWM output 1
PWM2	O	PWM output 2
PWM3	O	PWM output 3
PMC_I2C_SCL	I/O	I^2C bus clock of the PMC for communicating with the external PMU
PMC_I2C_SDA	I/O	I^2C bus data/address of the PMC for communicating with the external PMU

SAR_ADC

Table 2-66 lists the software multiplexed SAR_ADC pins.

Table 2-66 Software multiplexed SAR_ADC pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V3	SAR_ADC_CH0	muxctrl_reg87	SAR_ADC_CH0	GPIO1_6
V4	SAR_ADC_CH1	muxctrl_reg88	SAR_ADC_CH1	GPIO1_7

Table 2-67 describes software multiplexed SAR_ADC signals.

Table 2-67 Description of software multiplexed SAR_ADC signals

Signal	Direction	Description
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
SAR_ADC_CH0	I	LSADC channel 0
SAR_ADC_CH1	I	LSADC channel 1

EPHY

Table 2-68 lists the software multiplexed EPHY pin.

Table 2-68 Software multiplexed FEPHY pin

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
E19	EPHY_CLK	muxctrl_reg89	GPIO14_4	EPHY_CLK

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Table 2-69 describes software multiplexed EPHY signals.

Table 2-69 Description of software multiplexed EPHY signals

Signal	Direction	Description
EPHY_CLK	O	Working clock of the EPHY
GPIO14_4	I/O	GPIO

MDIO

Table 2-70 lists the software multiplexed MDIO pins.

Table 2-70 Software multiplexed MDIO pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
B19	MDCK	muxctrl_reg90	GPIO14_5	MDCK
D18	MDIO	muxctrl_reg91	GPIO14_6	MDIO

Table 2-71 describes software multiplexed MDIO signals.

Table 2-71 Description of software multiplexed MDIO signals

Signal	Direction	Description
GPIO14_5	I/O	GPIO
GPIO14_6	I/O	GPIO
MDCK	O	MDIO clock
MDIO	I/O	MDIO data

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RGMII

Table 2-72 lists the software multiplexed RGMII pins.

Table 2-72 Software multiplexed RGMII pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
C19	RGMII_TX_EN	muxctrl_reg92	GPIO14_7	RGMII_TX_EN	None
B22	RGMII_TX_CLK	muxctrl_reg93	GPIO4_0	RGMII_TX_CLK	RMII_CLK
B21	RGMII_TXD0	muxctrl_reg94	GPIO4_1	RGMII_TXD0	None
C21	RGMII_TXD1	muxctrl_reg95	GPIO4_2	RGMII_TXD1	None
C20	RGMII_TXD2	muxctrl_reg96	GPIO4_3	RGMII_TXD2	None
D19	RGMII_TXD3	muxctrl_reg97	GPIO4_4	RGMII_TXD3	None
A21	RGMII_RX_CLK	muxctrl_reg98	GPIO4_5	RGMII_RX_CLK	None
B18	RGMII_RX_DV	muxctrl_reg99	GPIO4_6	RGMII_RX_DV	None
A18	RGMII_RXD0	muxctrl_reg100	GPIO4_7	RGMII_RXD0	None
C18	RGMII_RXD1	muxctrl_reg101	GPIO1_3	RGMII_RXD1	None
A19	RGMII_RXD2	muxctrl_reg102	GPIO1_4	RGMII_RXD2	None
A20	RGMII_RXD3	muxctrl_reg103	GPIO1_5	RGMII_RXD3	None

Table 2-73 describes software multiplexed RGMII signals.

Table 2-73 Description of software multiplexed RGMII signals

Signal	Direction	Description
GPIO1_3	I/O	GPIO
GPIO1_4	I/O	GPIO
GPIO1_5	I/O	GPIO
GPIO14_7	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO

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Signal	Direction	Description
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
RGMII_RX_CLK	I	RGMII mode: 125 MHz RX clock, valid at the rising and falling edges MII mode: RX mode
RGMII_RX_DV	I	RGMII mode: RX data validity MII mode: RX data validity RMII mode: RX data validity or carrier detection signal
RGMII_RXD0	I	RGMII/RMII/MII mode: RX data 0
RGMII_RXD1	I	RX data 1 in RGMII/RMII/MII mode
RGMII_RXD2	I	RX data 2 in RGMII/MII mode
RGMII_RXD3	I	RX data 3 in RGMII/MII mode
RGMII_TX_CLK	O	125 MHz TX clock in RGMII mode, valid at the rising and falling edges
RGMII_TX_EN	O	TX enable in RGMII/RMII/MII mode
RGMII_TXD0	O	TX data 0 in RGMII/RMII/MII mode
RGMII_TXD1	O	TX data 1 in RGMII/RMII mode
RGMII_TXD2	O	TX data 2 in RGMII/MII mode
RGMII_TXD3	O	TX data 3 in RGMII/MII mode
RMII_CLK	I/O	RMII mode: reference clock MII mode: TX clock

VI

Table 2-74 lists the software multiplexed VI pins.

Table 2-74 Software multiplexed VI pins

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
AA7	VI_CLK	muxctrl_reg104	GPIO15_0	VI_CLK	None	None
W4	VI_HS	muxctrl_reg105	GPIO15_1	VI_HS	None	None

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Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
AB3	VI_VS	muxctrl_reg106	GPIO15_2	VI_VS	None	None
W6	VI_DAT15	muxctrl_reg107	GPIO12_0	VI_DAT15	I2S_MCLK	None
Y6	VI_DAT14	muxctrl_reg108	GPIO12_1	VI_DAT14	I2S_BCLK_TX	None
W5	VI_DAT13	muxctrl_reg109	GPIO12_2	VI_DAT13	I2S_WS_TX	None
Y5	VI_DAT12	muxctrl_reg110	GPIO12_3	VI_DAT12	I2S_SD_TX	None
W8	VI_DAT11	muxctrl_reg111	GPIO12_4	VI_DAT11	I2S_BCLK_RX	None
Y4	VI_DAT10	muxctrl_reg112	GPIO12_5	VI_DAT10	I2S_WS_RX	None
Y7	VI_DAT9	muxctrl_reg113	GPIO12_6	VI_DAT9	I2S_SD_RX	None
AB8	VI_DAT8	muxctrl_reg114	GPIO12_7	VI_DAT8	None	None
W7	VI_DAT7	muxctrl_reg115	GPIO13_0	VI_DAT7	None	None
AB7	VI_DAT6	muxctrl_reg116	GPIO13_1	VI_DAT6	None	None
AB6	VI_DAT5	muxctrl_reg117	GPIO13_2	VI_DAT5	None	None
AA5	VI_DAT4	muxctrl_reg118	GPIO13_3	VI_DAT4	None	None
AB5	VI_DAT3	muxctrl_reg119	GPIO13_4	VI_DAT3	None	None
AA4	VI_DAT2	muxctrl_reg120	GPIO13_5	VI_DAT2	None	None
AB4	VI_DAT1	muxctrl_reg121	GPIO13_6	VI_DAT1	None	None
AA3	VI_DAT0	muxctrl_reg122	GPIO13_7	VI_DAT0	None	PWM4

Table 2-75 describes software multiplexed VI signals.

Table 2-75 Description of software multiplexed VI signals

Signal	Direction	Description
GPIO12_0	I/O	GPIO
GPIO12_1	I/O	GPIO
GPIO12_2	I/O	GPIO
GPIO12_3	I/O	GPIO

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Signal	Direction	Description
GPIO12_4	I/O	GPIO
GPIO12_5	I/O	GPIO
GPIO12_6	I/O	GPIO
GPIO12_7	I/O	GPIO
GPIO13_0	I/O	GPIO
GPIO13_1	I/O	GPIO
GPIO13_2	I/O	GPIO
GPIO13_3	I/O	GPIO
GPIO13_4	I/O	GPIO
GPIO13_5	I/O	GPIO
GPIO13_6	I/O	GPIO
GPIO13_7	I/O	GPIO
GPIO15_0	I/O	GPIO
GPIO15_1	I/O	GPIO
GPIO15_2	I/O	GPIO
I2S_BCLK_RX	I/O	RX clock of the I^2S or PCM interface
I2S_BCLK_TX	I/O	TX clock of I^2S or PCM interface
I2S_MCLK	O	Main clock of the I^2S or PCM interface. It can act as the main clock of the ACODEC.
I2S_SD_RX	I	RX data input of the I^2S or PCM interface
I2S_SD_TX	O	TX data output of the I^2S or PCM interface
I2S_WS_RX	I/O	I^2S RX audio channel select signal or PCM TX frame sync signal
I2S_WS_TX	I/O	I^2S TX audio channel select signal or PCM TX frame sync signal
PWM4	O	PWM output 4
VI_CLK	I	VI input clock
VI_DAT0	I	VI input data 0
VI_DAT1	I	VI input data 1
VI_DAT2	I	VI input data 2
VI_DAT3	I	VI input data 3
VI_DAT4	I	VI input data 4

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Signal	Direction	Description
VI_DAT5	I	VI input data 5
VI_DAT6	I	VI input data 6
VI_DAT7	I	VI input data 7
VI_DAT8	I	VI input data 8
VI_DAT9	I	VI input data 9
VI_DAT10	I	VI input data 10
VI_DAT11	I	VI input data 11
VI_DAT12	I	VI input data 12
VI_DAT13	I	VI input data 13
VI_DAT14	I	VI input data 14
VI_DAT15	I	VI input data 15
VI_DAT2	I	VI input data 2
VI_DAT3	I	VI input data 3
VI_DAT4	I	VI input data 4
VI_DAT5	I	VI input data 5
VI_DAT6	I	VI input data 6
VI_DAT7	I	VI input data 7
VI_DAT8	I	VI input data 8
VI_DAT9	I	VI input data 9
VI_HS	I	VI input horizontal sync signal
VI_VS	I	VI input vertical sync signal

2.5 Hardware Multiplexed Pins

SYS Pin

Table 2-76 lists the hardware multiplexed SYS pin.

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Table 2-76 Hardware multiplexed SYS pin

Pin	Pad Signal	Multiplexed Signal 1 (por_sel == 1'b0)
T4	WDG_RSTN	SYS_RSTN_OUT

Table 2-77 describes the hardware multiplexed SYS signal.

Table 2-77 Description of the hardware multiplexed SYS signal

Signal	Direction	Description
SYS_RSTN_OUT	O	System reset output 0: reset 1: reset deasserted

SFC Pin

Table 2-78 lists the hardware multiplexed SFC pin.

Table 2-78 Hardware multiplexed SFC pin

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
P1	SFC_CLK	SFC_BOOT_MODE

Table 2-79 lists the hardware multiplexed SFC signal.

Table 2-79 Hardware multiplexed SFC signal

Signal	Direction	Description
SFC_BOOT_MODE	I	This signal works with SFC_DEVICE_MODE. Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode This signal works with SFC_DEVICE_MODE. Boot address mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire mode 1: 4-wire mode

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2.6 Pin Drive Capability Registers

2.6.1 Register Summary

Table 2-80 describes pin drive capability registers.

Table 2-80 Summary of pad_ctrl registers (base address: 0x200F_0800)

Offset Address	Register	Description	Page
0x0000	PADCTRL_REG0	Drive capability register for the SENSOR_CLK pin	2-164
0x0004	PADCTRL_REG1	Drive capability register for the FLASH_TRIG pin	2-165
0x0008	PADCTRL_REG2	Drive capability register for the SHUTTER_TRIG pin	2-165
0x000C	PADCTRL_REG3	Drive capability register for the VO_CLK pin	2-166
0x0010	PADCTRL_REG4	Drive capability register for the VO_DAT15 pin	2-167
0x0014	PADCTRL_REG5	Drive capability register for the VO_DAT14 pin	2-168
0x0018	PADCTRL_REG6	Drive capability register for the VO_DAT13 pin	2-168
0x001C	PADCTRL_REG7	Drive capability register for the VO_DAT12 pin	2-169
0x0020	PADCTRL_REG8	Drive capability register for the VO_DAT11 pin	2-170
0x0024	PADCTRL_REG9	Drive capability register for the VO_DAT10 pin	2-171
0x0028	PADCTRL_REG10	Drive capability register for the VO_DAT9 pin	2-171
0x002C	PADCTRL_REG11	Drive capability register for the VO_DAT8 pin	2-172
0x0030	PADCTRL_REG12	Drive capability register for the VO_DAT7 pin	2-173
0x0034	PADCTRL_REG13	Drive capability register for the VO_DAT6 pin	2-174
0x0038	PADCTRL_REG14	Drive capability register for the VO_DAT5 pin	2-174
0x003C	PADCTRL_REG15	Drive capability register for the VO_DAT4 pin	2-175

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Offset Address	Register	Description	Page
0x0040	PADCTRL_REG16	Drive capability register for the VO_DAT3 pin	2-176
0x0044	PADCTRL_REG17	Drive capability register for the VO_DAT2 pin	2-177
0x0048	PADCTRL_REG18	Drive capability register for the VO_DAT1 pin	2-177
0x004C	PADCTRL_REG19	Drive capability register for the VO_DAT0 pin	2-178
0x0050	PADCTRL_REG20	Drive capability register for the SPI0_SCLK pin	2-179
0x0054	PADCTRL_REG21	Drive capability register for the SPI0_SDO pin	2-180
0x0058	PADCTRL_REG22	Drive capability register for the SPI0_SDI pin	2-180
0x005C	PADCTRL_REG23	Drive capability register for the SPI0_CSN pin	2-181
0x0060	PADCTRL_REG24	Drive capability register for the SPI1_SCLK pin	2-182
0x0064	PADCTRL_REG25	Drive capability register for the SPI1_SDO pin	2-183
0x0068	PADCTRL_REG26	Drive capability register for the SPI1_SDI pin	2-183
0x006C	PADCTRL_REG27	Drive capability register for the SPI1_CSN0 pin	2-184
0x0070	PADCTRL_REG28	Drive capability register for the I2C2_SDA pin	2-185
0x0074	PADCTRL_REG29	Drive capability register for the I2C2_SCL pin	2-186
0x0078	PADCTRL_REG30	Drive capability register for the UART0_RXD pin	2-186
0x007C	PADCTRL_REG31	Drive capability register for the UART0_TXD pin	2-187
0x0080	PADCTRL_REG32	Drive capability register for the UART1_RTSN pin	2-188
0x0084	PADCTRL_REG33	Drive capability register for the UART1_RXD pin	2-189
0x0088	PADCTRL_REG34	Drive capability register for the UART1_CTSN pin	2-189

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Offset Address	Register	Description	Page
0x008C	PADCTRL_REG35	Drive capability register for the UART1_TXD pin	2-190
0x0090	PADCTRL_REG36	Drive capability register for the UART2_RXD pin	2-191
0x0094	PADCTRL_REG37	Drive capability register for the UART2_TXD pin	2-192
0x0098	PADCTRL_REG38	Drive capability register for the JTAG_EN pin	2-192
0x009C	PADCTRL_REG39	Drive capability register for the JTAG_TRSTN pin	2-193
0x00A0	PADCTRL_REG40	Drive capability register for the JTAG_TCK pin	2-194
0x00A4	PADCTRL_REG41	Drive capability register for the JTAG_TMS pin	2-195
0x00A8	PADCTRL_REG42	Drive capability register for the JTAG_TDO pin	2-195
0x00AC	PADCTRL_REG43	Drive capability register for the JTAG_TDI pin	2-196
0x00B0	PADCTRL_REG44	Drive capability register for the IR_IN pin	2-197
0x00B4	PADCTRL_REG45	Drive capability register for the POR_SEL pin	2-198
0x00B8	PADCTRL_REG46	Drive capability register for the RSTN pin	2-198
0x00BC	PADCTRL_REG47	Drive capability register for the WDG_RSTN pin	2-199
0x00C0	PADCTRL_REG48	Drive capability register for the TEST_MODE pin	2-200
0x00C4	PADCTRL_REG49	Drive capability register for the USB_OVRCUR pin	2-201
0x00C8	PADCTRL_REG50	Drive capability register for the USB_PWREN pin	2-201
0x00CC	PADCTRL_REG51	Drive capability register for the SDIO0_CCLK_OUT pin	2-202
0x00D0	PADCTRL_REG52	Drive capability register for the SDIO0_CARD_POWER_EN pin	2-203
0x00D4	PADCTRL_REG53	Drive capability register for the SDIO0_CARD_DETECT pin	2-204
0x00D8	PADCTRL_REG54	Drive capability register for the SDIO0_CWPR pin	2-205

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Offset Address	Register	Description	Page
0x00DC	PADCTRL_REG55	Drive capability register for the SDIO0_CCMD pin	2-206
0x00E0	PADCTRL_REG56	Drive capability register for the SDIO0_CDATA0 pin	2-207
0x00E4	PADCTRL_REG57	Drive capability register for the SDIO0_CDATA1 pin	2-208
0x00E8	PADCTRL_REG58	Drive capability register for the SDIO0_CDATA2 pin	2-209
0x00EC	PADCTRL_REG59	Drive capability register for the SDIO0_CDATA3 pin	2-210
0x00F0	PADCTRL_REG60	Drive capability register for the GPIO0_0 pin	2-211
0x00F4	PADCTRL_REG61	Drive capability register for the GPIO0_1 pin	2-211
0x00F8	PADCTRL_REG62	Drive capability register for the GPIO0_2 pin	2-212
0x00FC	PADCTRL_REG63	Drive capability register for the GPIO0_3 pin	2-213
0x0100	PADCTRL_REG64	Drive capability register for the GPIO0_4 pin	2-214
0x0104	PADCTRL_REG65	Drive capability register for the SDIO1_CCLK_OUT pin	2-214
0x0108	PADCTRL_REG66	Drive capability register for the SDIO1_CARD_POWER_EN pin	2-215
0x010C	PADCTRL_REG67	Drive capability register for the SDIO1_CARD_DETECT pin	2-216
0x0110	PADCTRL_REG68	Drive capability register for the SDIO1_CWPR pin	2-217
0x0114	PADCTRL_REG69	Drive capability register for the SDIO1_CCMD pin	2-218
0x0118	PADCTRL_REG70	Drive capability register for the SDIO1_CDATA0 pin	2-219
0x011C	PADCTRL_REG71	Drive capability register for the SDIO1_CDATA1 pin	2-220
0x0120	PADCTRL_REG72	Drive capability register for the SDIO1_CDATA2 pin	2-221
0x0124	PADCTRL_REG73	Drive capability register for the SDIO1_CDATA3 pin	2-222

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Offset Address	Register	Description	Page
0x0128	PADCTRL_REG74	Drive capability register for the SFC_SIO_IO0 pin	2-223
0x012C	PADCTRL_REG75	Drive capability register for the SFC_WP_IO2 pin	2-223
0x0130	PADCTRL_REG76	Drive capability register for the SFC_CLK pin	2-224
0x0134	PADCTRL_REG77	Drive capability register for the SFC_SOI_IO1 pin	2-225
0x0138	PADCTRL_REG78	Drive capability register for the SFC_HOLD_IO3 pin	2-226
0x013C	PADCTRL_REG79	Drive capability register for the SFC_CSN1 pin	2-226
0x0140	PADCTRL_REG80	Drive capability register for the NF_DQ0 pin	2-227
0x0144	PADCTRL_REG81	Drive capability register for the NF_DQ1 pin	2-228
0x0148	PADCTRL_REG82	Drive capability register for the NF_DQ2 pin	2-228
0x014C	PADCTRL_REG83	Drive capability register for the NF_DQ3 pin	2-229
0x0150	PADCTRL_REG84	Drive capability register for the NF_DQ4 pin	2-230
0x0154	PADCTRL_REG85	Drive capability register for the NF_DQ5 pin	2-230
0x0158	PADCTRL_REG86	Drive capability register for the NF_DQ6 pin	2-231
0x015C	PADCTRL_REG87	Drive capability register for the NF_DQ7 pin	2-232
0x0160	PADCTRL_REG88	Drive capability register for the NF_RDY0 pin	2-233
0x0164	PADCTRL_REG89	Drive capability register for the NF_RDY1 pin	2-233
0x0168	PADCTRL_REG90	Drive capability register for the NF_REN pin	2-234
0x016C	PADCTRL_REG91	Drive capability register for the NF_CSN0 pin	2-235
0x0170	PADCTRL_REG92	Drive capability register for the NF_CSN1 pin	2-236

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Offset Address	Register	Description	Page
0x0174	PADCTRL_REG93	Drive capability register for the NF_CLE pin	2-236
0x0178	PADCTRL_REG94	Drive capability register for the NF_ALE pin	2-237
0x017C	PADCTRL_REG95	Drive capability register for the NF_WEN pin	2-238
0x0180	PADCTRL_REG96	Drive capability register for the PWM0 pin	2-238
0x0184	PADCTRL_REG97	Drive capability register for the PWM1 pin	2-239
0x0188	PADCTRL_REG98	Drive capability register for the PWM2 pin	2-240
0x018C	PADCTRL_REG99	Drive capability register for the PWM3 pin	2-240
0x0190	PADCTRL_REG100	Drive capability register for the SAR_ADC_CH0 pin	2-241
0x0194	PADCTRL_REG101	Drive capability register for the SAR_ADC_CH1 pin	2-242
0x0198	PADCTRL_REG102	Drive capability register for the EPHY_CLK pin	2-243
0x019C	PADCTRL_REG103	Drive capability register for the MDCK pin	2-244
0x01A0	PADCTRL_REG104	Drive capability register for the MDIO pin	2-245
0x01A4	PADCTRL_REG105	Drive capability register for the RGMII_TX_EN pin	2-246
0x01A8	PADCTRL_REG106	Drive capability register for the RGMII_TX_CLK pin	2-247
0x01AC	PADCTRL_REG107	Drive capability register for the RGMII_TXD0 pin	2-248
0x01B0	PADCTRL_REG108	Drive capability register for the RGMII_TXD1 pin	2-249
0x01B4	PADCTRL_REG109	Drive capability register for the RGMII_TXD2 pin	2-250
0x01B8	PADCTRL_REG110	Drive capability register for the RGMII_TXD3 pin	2-251
0x01BC	PADCTRL_REG111	Drive capability register for the RGMII_RX_CLK pin	2-252
0x01C0	PADCTRL_REG112	Drive capability register for the RGMII_RX_DV pin	2-253
0x01C4	PADCTRL_REG113	Drive capability register for the RGMII_RXD0 pin	2-254

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Offset Address	Register	Description	Page
0x01C8	PADCTRL_REG114	Drive capability register for the RGMII_RXD1 pin	2-255
0x01CC	PADCTRL_REG115	Drive capability register for the RGMII_RXD2 pin	2-256
0x01D0	PADCTRL_REG116	Drive capability register for the RGMII_RXD3 pin	2-257
0x01D4	PADCTRL_REG117	Drive capability register for the VI_CLK pin	2-257
0x01D8	PADCTRL_REG118	Drive capability register for the VI_HS pin	2-258
0x01DC	PADCTRL_REG119	Drive capability register for the VI_VS pin	2-259
0x01E0	PADCTRL_REG120	Drive capability register for the VI_DAT15 pin	2-260
0x01E4	PADCTRL_REG121	Drive capability register for the VI_DAT14 pin	2-260
0x01E8	PADCTRL_REG122	Drive capability register for the VI_DAT13 pin	2-261
0x01EC	PADCTRL_REG123	Drive capability register for the VI_DAT12 pin	2-262
0x01F0	PADCTRL_REG124	Drive capability register for the VI_DAT11 pin	2-263
0x01F4	PADCTRL_REG125	Drive capability register for the VI_DAT10 pin	2-263
0x01F8	PADCTRL_REG126	Drive capability register for the VI_DAT9 pin	2-264
0x01FC	PADCTRL_REG127	Drive capability register for the VI_DAT8 pin	2-265
0x0200	PADCTRL_REG128	Drive capability register for the VI_DAT7 pin	2-266
0x0204	PADCTRL_REG129	Drive capability register for the VI_DAT6 pin	2-266
0x0208	PADCTRL_REG130	Drive capability register for the VI_DAT5 pin	2-267
0x020C	PADCTRL_REG131	Drive capability register for the VI_DAT4 pin	2-268
0x0210	PADCTRL_REG132	Drive capability register for the VI_DAT3 pin	2-269
0x0214	PADCTRL_REG133	Drive capability register for the VI_DAT2 pin	2-269

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Offset Address	Register	Description	Page
0x0218	PADCTRL_REG134	Drive capability register for the VI_DAT1 pin	2-270
0x021C	PADCTRL_REG135	Drive capability register for the VI_DAT0 pin	2-271

2.6.2 Register Description

PADCTRL_REG0

PADCTRL_REG0 is a drive capability register for the SENSOR_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0000	PADCTRL_REG0	0x0000_0040

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6 5 4	3 2 1 0
Name	reserved						sensor_clk_sr	sensor_clk_ds	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sensor_clk_sr	Level conversion rate of the SENSOR_CLK pin 0: fast edge 1: slow edge
[6:4]	RW	sensor_clk_ds	Drive current of the SENSOR_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG1

PADCTRL_REG1 is a drive capability register for the FLASH_TRIG pin.

Offset Address	Register Name	Total Reset Value
0x0004	PADCTRL_REG1	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								flash_trig_sr	reserved	flash_trig_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	flash_trig_sr	Level conversion rate of the FLASH_TRIG pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	flash_trig_ds	Drive current of the FLASH_TRIG pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG2

PADCTRL_REG2 is a drive capability register for the SHUTTER_TRIG pin.

Offset Address	Register Name	Total Reset Value
0x0008	PADCTRL_REG2	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								shutter_trig_sr	reserved	shutter_trig_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	shutter_trig_sr	Level conversion rate of the SHUTTER_TRIG pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	shutter_trig_ds	Drive current of the SHUTTER_TRIG pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG3

PADCTRL_REG3 is a drive capability register for the VO_CLK pin.

Offset Address	Register Name	Total Reset Value
0x000C	PADCTRL_REG3	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_clk_sr	vo_clk_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_clk_sr	Level conversion rate of the VO_CLK pin 0: fast edge 1: slow edge

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[6:4]	RW	vo_clk_ds	Drive current of the VO_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG4

PADCTRL_REG4 is a drive capability register for the VO_DAT15 pin.

Offset Address	Register Name	Total Reset Value
0x0010	PADCTRL_REG4	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat15_sr	reserved	vo_dat15_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat15_sr	Level conversion rate of the VO_DAT15 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat15_ds	Drive current of the VO_DAT15 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG5

PADCTRL_REG5 is a drive capability register for the VO_DAT14 pin.

Offset Address	Register Name	Total Reset Value
0x0014	PADCTRL_REG5	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat14_sr	reserved	vo_dat14_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat14_sr	Level conversion rate of the VO_DAT14 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat14_ds	Drive current of the VO_DAT14 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG6

PADCTRL_REG6 is a drive capability register for the VO_DAT13 pin.

Offset Address	Register Name	Total Reset Value
0x0018	PADCTRL_REG6	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat13_sr	reserved	vo_dat13_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat13_sr	Level conversion rate of the VO_DAT13 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat13_ds	Drive current of the VO_DAT13 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG7

PADCTRL_REG7 is a drive capability register for the VO_DAT12 pin.

Offset Address	Register Name	Total Reset Value
0x001C	PADCTRL_REG7	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat12_sr	reserved	vo_dat12_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat12_sr	Level conversion rate of the VO_DAT12 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vo_dat12_ds	Drive current of the VO_DAT12 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG8

PADCTRL_REG8 is a drive capability register for the VO_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x0020	PADCTRL_REG8	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat11_sr	reserved	vo_dat11_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat11_sr	Level conversion rate of the VO_DAT11 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat11_ds	Drive current of the VO_DAT11 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG9

PADCTRL_REG9 is a drive capability register for the VO_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x0024	PADCTRL_REG9	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat10_sr	reserved	vo_dat10_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat10_sr	Level conversion rate of the VO_DAT10 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat10_ds	Drive current of the VO_DAT10 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG10

PADCTRL_REG10 is a drive capability register for the VO_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x0028	PADCTRL_REG10	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat9_sr	reserved	vo_dat9_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat9_sr	Level conversion rate of the VO_DAT9 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat9_ds	Drive current of the VO_DAT9 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG11

PADCTRL_REG11 is a drive capability register for the VO_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x002C	PADCTRL_REG11	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat8_sr	reserved	vo_dat8_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat8_sr	Level conversion rate of the VO_DAT8 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vo_dat8_ds	Drive current of the VO_DAT8 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG12

PADCTRL_REG12 is a drive capability register for the VO_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0030	PADCTRL_REG12	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat7_sr	reserved	vo_dat7_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat7_sr	Level conversion rate of the VO_DAT7 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat7_ds	Drive current of the VO_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG13

PADCTRL_REG13 is a drive capability register for the VO_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0034	PADCTRL_REG13	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat6_sr	reserved	vo_dat6_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat6_sr	Level conversion rate of the VO_DAT6 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat6_ds	Drive current of the VO_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG14

PADCTRL_REG14 is a drive capability register for the VO_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0038	PADCTRL_REG14	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat5_sr	reserved	vo_dat5_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat5_sr	Level conversion rate of the VO_DAT5 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat5_ds	Drive current of the VO_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG15

PADCTRL_REG15 is a drive capability register for the VO_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x003C	PADCTRL_REG15	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat4_sr	reserved	vo_dat4_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat4_sr	Level conversion rate of the VO_DAT4 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vo_dat4_ds	Drive current of the VO_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG16

PADCTRL_REG16 is a drive capability register for the VO_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0040	PADCTRL_REG16	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat3_sr	reserved	vo_dat3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat3_sr	Level conversion rate of the VO_DAT3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat3_ds	Drive current of the VO_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG17

PADCTRL_REG17 is a drive capability register for the VO_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0044	PADCTRL_REG17	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat2_sr	reserved	vo_dat2_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat2_sr	Level conversion rate of the VO_DAT2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat2_ds	Drive current of the VO_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG18

PADCTRL_REG18 is a drive capability register for the VO_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0048	PADCTRL_REG18	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat1_sr	reserved	vo_dat1_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat1_sr	Level conversion rate of the VO_DAT1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vo_dat1_ds	Drive current of the VO_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG19

PADCTRL_REG19 is a drive capability register for the VO_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x004C	PADCTRL_REG19	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vo_dat0_sr	reserved	vo_dat0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vo_dat0_sr	Level conversion rate of the VO_DAT0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vo_dat0_ds	Drive current of the VO_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG20

PADCTRL_REG20 is a drive capability register for the SPI0_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x0050	PADCTRL_REG20	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi0_sclk_sr	spi0_sclk_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi0_sclk_sr	Level conversion rate of the SPI0_SCLK pin 0: fast edge 1: slow edge
[6:4]	RW	spi0_sclk_ds	Drive current of the SPI0_SCLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG21

PADCTRL_REG21 is a drive capability register for the SPI0_SDO pin.

Offset Address	Register Name	Total Reset Value
0x0054	PADCTRL_REG21	0x0000_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi0_sdo_sr	reserved	sip0_sdo_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi0_sdo_sr	Level conversion rate of the SPI0_SDO pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sip0_sdo_ds	Drive current of the SPI0_SDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG22

PADCTRL_REG22 is a drive capability register for the SPI0_SDI pin.

Offset Address	Register Name	Total Reset Value
0x0058	PADCTRL_REG22	0x0000_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi0_sdi_sr	reserved	spi0_sdi_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi0_sdi_sr	Level conversion rate of the SPI0_SDI pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	spi0_sdi_ds	Drive current of the SPI0_SDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG23

PADCTRL_REG23 is a drive capability register for the SPI0_CSN pin.

Offset Address	Register Name	Total Reset Value
0x005C	PADCTRL_REG23	0x0000_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi0_csn_sr	reserved	sip0_csn_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi0_csn_sr	Level conversion rate of the SPI0_CSN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	sip0_csn_ds	Drive current of the SPI0_CSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG24

PADCTRL_REG24 is a drive capability register for the SPI1_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x0060	PADCTRL_REG24	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi1_sclk_sr	reserved	spi1_sclk_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi1_sclk_sr	Level conversion rate of the SPI1_SCLK pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	spi1_sclk_ds	Drive current of the SPI1_SCLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG25

PADCTRL_REG25 is a drive capability register for the SPI1_SDO pin.

Offset Address	Register Name	Total Reset Value
0x0064	PADCTRL_REG25	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi1_sdo_sr	reserved	spi1_sdo_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi1_sdo_sr	Level conversion rate of the SPI1_SDO pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	spi1_sdo_ds	Drive current of the SPI1_SDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG26

PADCTRL_REG26 is a drive capability register for the SPI1_SDI pin.

Offset Address	Register Name	Total Reset Value
0x0068	PADCTRL_REG26	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi1_sdi_sr	reserved	spi1_sdi_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi1_sdi_sr	Level conversion rate of the SPI1_SDI pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	spi1_sdi_ds	Drive current of the SPI1_SDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG27

PADCTRL_REG27 is a drive capability register for the SPI1_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x006C	PADCTRL_REG27	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi1_csn_sr	reserved	spi1_csn_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	spi1_csn_sr	Level conversion rate of the SPI1_CSN0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	spi1_csn_ds	Drive current of the SPI1_CSN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG28

PADCTRL_REG28 is a drive capability register for the I2C2_SDA pin.

Offset Address	Register Name	Total Reset Value
0x0070	PADCTRL_REG28	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c2_sda_sr	reserved	i2c2_sda_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	i2c2_sda_sr	Level conversion rate of the I2C2_SDA pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	i2c2_sda_ds	Drive current of the I2C2_SDA pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG29

PADCTRL_REG29 is a drive capability register for the I2C2_SCL pin.

Offset Address	Register Name	Total Reset Value
0x0074	PADCTRL_REG29	0x0000_00A0

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5 4	3 2 1 0
Name	reserved						i2c2_scl_sr	reserved	i2c2_scl_ds	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1	0	1 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	i2c2_scl_sr	Level conversion rate of the I2C2_SCL pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	i2c2_scl_ds	Drive current of the I2C2_SCL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG30

PADCTRL_REG30 is a drive capability register for the UART0_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0078	PADCTRL_REG30	0x0000_00A0

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5 4	3 2 1 0
Name	reserved						uart0_rxd_sr	reserved	uart0_rxd_ds	reserved

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart0_rxd_sr	Level conversion rate of the UART0_RXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart0_rxd_ds	Drive current of the UART0_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG31

PADCTRL_REG31 is a drive capability register for the UART0_TXD pin.

Offset Address	Register Name	Total Reset Value
0x007C	PADCTRL_REG31	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart0_txd_sr	reserved	uart0_txd_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart0_txd_sr	Level conversion rate of the UART0_TXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	uart0_txd_ds	Drive current of the UART0_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG32

PADCTRL_REG32 is a drive capability register for the UART1_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x0080	PADCTRL_REG32	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart1_rtsn_sr	reserved	uart1_rtsn_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart1_rtsn_sr	Level conversion rate of the UART1_RTSN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart1_rtsn_ds	Drive current of the UART1_RTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG33

PADCTRL_REG33 is a drive capability register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0084	PADCTRL_REG33	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart1_rxd_sr	reserved	uart1_rxd_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart1_rxd_sr	Level conversion rate of the UART1_RXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart1_rxd_ds	Drive current of the UART1_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG34

PADCTRL_REG34 is a drive capability register for the UART1_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x0088	PADCTRL_REG34	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart1_ctsn_sr	reserved	uart1_ctsn_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart1_ctsn_sr	Level conversion rate of the UART1_CTSN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart1_ctsn_ds	Drive current of the UART1_CTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG35

PADCTRL_REG35 is a drive capability register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x008C	PADCTRL_REG35	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart1_txd_sr	reserved	uart1_txd_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart1_txd_sr	Level conversion rate of the UART1_TXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	uart1_txd_ds	Drive current of the UART1_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG36

PADCTRL_REG36 is a drive capability register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0090	PADCTRL_REG36	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart2_rxd_sr	reserved	uart2_rxd_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart2_rxd_sr	Level conversion rate of the UART2_RXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart2_rxd_ds	Drive current of the UART2_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG37

PADCTRL_REG37 is a drive capability register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0094	PADCTRL_REG37	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uart2_txd_sr	reserved	uart2_txd_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	uart2_txd_sr	Level conversion rate of the UART2_TXD pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	uart2_txd_ds	Drive current of the UART2_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG38

PADCTRL_REG38 is a drive capability register for the JTAG_EN pin.

Offset Address	Register Name	Total Reset Value
0x0098	PADCTRL_REG38	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_en_sr	reserved	jtag_en_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_en_sr	Level conversion rate of the JTAG_EN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	jtag_en_ds	Drive current of the JTAG_EN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG39

PADCTRL_REG39 is a drive capability register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x009C	PADCTRL_REG39	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_trstn_sr	reserved	jtag_trstn_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_trstn_sr	Level conversion rate of the JTAG_TRSTN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	jtag_trstn_ds	Drive current of the JTAG_TRSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG40

PADCTRL_REG40 is a drive capability register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x00A0	PADCTRL_REG40	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_tck_sr	reserved	jtag_tck_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_tck_sr	Level conversion rate of the JTAG_TCK pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	jtag_tck_ds	Drive current of the JTAG_TCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG41

PADCTRL_REG41 is a drive capability register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x00A4	PADCTRL_REG41	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_tms_sr	reserved	jtag_tms_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_tms_sr	Level conversion rate of the JTAG_TMS pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	jtag_tms_ds	Drive current of the JTAG_TMS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG42

PADCTRL_REG42 is a drive capability register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x00A8	PADCTRL_REG42	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_tdo_sr	reserved	jtag_tdo_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_tdo_sr	Level conversion rate of the JTAG_TDO pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	jtag_tdo_ds	Drive current of the JTAG_TDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG43

PADCTRL_REG43 is a drive capability register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x00AC	PADCTRL_REG43	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								jtag_tdi_sr	reserved	jtag_tdi_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	jtag_tdi_sr	Level conversion rate of the JTAG_TDI pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	jtag_tdi_ds	Drive current of the JTAG_TDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG44

PADCTRL_REG44 is a drive capability register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x00B0	PADCTRL_REG44	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ir_in_sr	reserved	ir_in_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ir_in_sr	Level conversion rate of the IR_IN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	ir_in_ds	Drive current of the IR_IN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG45

PADCTRL_REG45 is a drive capability register for the POR_SEL pin.

Offset Address	Register Name	Total Reset Value
0x00B4	PADCTRL_REG45	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								por_sel_sr	reserved	por_sel_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	por_sel_sr	Level conversion rate of the POR_SEL pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	por_sel_ds	Drive current of the POR_SEL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG46

PADCTRL_REG46 is a drive capability register for the RSTN pin.

Offset Address	Register Name	Total Reset Value
0x00B8	PADCTRL_REG46	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rstn_sr	reserved	rstn_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rstn_sr	Level conversion rate of the RSTN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rstn_ds	Drive current of the RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG47

PADCTRL_REG47 is a drive capability register for the WDG_RSTN pin.

Offset Address	Register Name	Total Reset Value
0x00BC	PADCTRL_REG47	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								wdg_rstn_sr	reserved	wdg_rstn_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	wdg_rstn_sr	Level conversion rate of the WDG_RSTN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	wdg_rstn_ds	Drive current of the WDG_RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG48

PADCTRL_REG48 is a drive capability register for the TEST_MODE pin.

Offset Address	Register Name	Total Reset Value
0x00C0	PADCTRL_REG48	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								test_mode_sr	reserved	test_mode_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	test_mode_sr	Level conversion rate of the TEST_MODE pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	test_mode_ds	Drive current of the TEST_MODE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG49

PADCTRL_REG49 is a drive capability register for the USB_OVRCUR pin.

Offset Address	Register Name	Total Reset Value
0x00C4	PADCTRL_REG49	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usb_ovrcur_sr	reserved	usb_ovrcur_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	usb_ovrcur_sr	Level conversion rate of the USB_OVRCUR pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	usb_ovrcur_ds	Drive current of the USB_OVRCUR pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG50

PADCTRL_REG50 is a drive capability register for the USB_PWREN pin.

Offset Address	Register Name	Total Reset Value
0x00C8	PADCTRL_REG50	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usb_pwren_sr	reserved	usb_pwren_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	usb_pwren_sr	Level conversion rate of the USB_PWREN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	usb_pwren_ds	Drive current of the USB_PWREN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG51

PADCTRL_REG51 is a drive capability register for the SDIO0_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x00CC	PADCTRL_REG51	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cclk_out_sr	sdio0_cclk_out_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cclk_out_sr	Level conversion rate of the SDIO0_CCLK_OUT pin 0: fast edge 1: slow edge

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[6:4]	RW	sdio0_cclk_out_ds	Drive current of the SDIO0_CCLK_OUT pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG52

PADCTRL_REG52 is a drive capability register for the SDIO0_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x00D0	PADCTRL_REG52	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_card_power_en_sr	reserved	sdio0_card_power_en_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_card_power_en_sr	Level conversion rate of the SDIO0_CARD_POWER_EN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sdio0_card_power_en_ds	Drive current of the SDIO0_CARD_POWER_EN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG53

PADCTRL_REG53 is a drive capability register for the SDIO0_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x00D4	PADCTRL_REG53	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_card_detect_en_sr	reserved	sdio0_card_detect_en_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_card_detect_en_sr	Level conversion rate of the SDIO0_CARD_DETECT pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sdio0_card_detect_en_ds	Drive current of the SDIO0_CARD_DETECT pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG54

PADCTRL_REG54 is a drive capability register for the SDIO0_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x00D8	PADCTRL_REG54	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cwpr_sr	reserved	sdio0_cwpr_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cwpr_sr	Level conversion rate of the SDIO0_CWPR pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sdio0_cwpr_ds	Drive current of the SDIO0_CWPR pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG55

PADCTRL_REG55 is a drive capability register for the SDIO0_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x00DC	PADCTRL_REG55	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_ccmd_sr	sdio0_ccmd_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_ccmd_sr	Level conversion rate of the SDIO0_CCMD pin 0: fast edge 1: slow edge
[6:4]	RW	sdio0_ccmd_ds	Drive current of the SDIO0_CCMD pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG56

PADCTRL_REG56 is a drive capability register for the SDIO0_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x00E0	PADCTRL_REG56	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cdata0_sr	sdio0_cdata0_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cdata0_sr	Level conversion rate of the SDIO0_CDATA0 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio0_cdata0_ds	Drive current of the SDIO0_CDATA0 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG57

PADCTRL_REG57 is a drive capability register for the SDIO0_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x00E4	PADCTRL_REG57	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cdata1_sr	sdio0_cdata1_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cdata1_sr	Level conversion rate of the SDIO0_CDATA1 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio0_cdata1_ds	Drive current of the SDIO0_CDATA1 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG58

PADCTRL_REG58 is a drive capability register for the SDIO0_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x00E8	PADCTRL_REG58	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cdata2_sr	sdio0_cdata2_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cdata2_sr	Level conversion rate of the SDIO0_CDATA2 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio0_cdata2_ds	Drive current of the SDIO0_CDATA2 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG59

PADCTRL_REG59 is a drive capability register for the SDIO0_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x00EC	PADCTRL_REG59	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio0_cdata3_sr	sdio0_cdata3_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio0_cdata3_sr	Level conversion rate of the SDIO0_CDATA3 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio0_cdata3_ds	Drive current of the SDIO0_CDATA3 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG60

PADCTRL_REG60 is a drive capability register for the GPIO0_0 pin.

Offset Address	Register Name	Total Reset Value
0x00F0	PADCTRL_REG60	0x0000_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gpio0_0_sr	reserved	gpio0_0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gpio0_0_sr	Level conversion rate of the GPIO0_0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	gpio0_0_ds	Drive current of the GPIO0_0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG61

PADCTRL_REG61 is a drive capability register for the GPIO0_1 pin.

Offset Address	Register Name	Total Reset Value
0x00F4	PADCTRL_REG61	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gpio0_1_sr	gpio0_1_ds			reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gpio0_1_sr	Level conversion rate of the GPIO0_1 pin 0: fast edge 1: slow edge
[6:4]	RW	gpio0_1_ds	Drive current of the GPIO0_1 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG62

PADCTRL_REG62 is a drive capability register for the GPIO0_2 pin.

Offset Address	Register Name	Total Reset Value
0x00F8	PADCTRL_REG62	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gpio0_2_sr	reserved	gpio0_2_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gpio0_2_sr	Level conversion rate of the GPIO0_2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	gpio0_2_ds	Drive current of the GPIO0_2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG63

PADCTRL_REG63 is a drive capability register for the GPIO0_3 pin.

Offset Address	Register Name	Total Reset Value
0x00FC	PADCTRL_REG63	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gpio0_3_sr	reserved	gpio0_3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gpio0_3_sr	Level conversion rate of the GPIO0_3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	gpio0_3_ds	Drive current of the GPIO0_3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG64

PADCTRL_REG64 is a drive capability register for the GPIO0_4 pin.

Offset Address	Register Name	Total Reset Value
0x0100	PADCTRL_REG64	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gpio0_4_sr	reserved	gpio0_4_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gpio0_4_sr	Level conversion rate of the GPIO0_4 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	gpio0_4_ds	Drive current of the GPIO0_4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG65

PADCTRL_REG65 is a drive capability register for the SDIO1_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x0104	PADCTRL_REG65	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cclk_out_sr	sdio1_cclk_out_ds			reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cclk_out_sr	Level conversion rate of the SDIO1_CCLK_OUT pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_cclk_out_ds	Drive current of the SDIO1_CCLK_OUT pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG66

PADCTRL_REG66 is a drive capability register for the SDIO1_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x0108	PADCTRL_REG66	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_card_power_en_sr	reserved	sdio1_card_power_en_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

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[7]	RW	sdio1_card_power_en_sr	Level conversion rate of the SDIO1_CARD_POWER_EN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sdio1_card_power_en_ds	Drive current of the SDIO1_CARD_POWER_EN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG67

PADCTRL_REG67 is a drive capability register for the SDIO1_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x010C	PADCTRL_REG67	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_card_detect_en_sr	reserved	sdio1_card_detect_en_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_card_detect_en_sr	Level conversion rate of the SDIO1_CARD_DETECT pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	sdio1_card_detect_en_ds	Drive current of the SDIO1_CARD_DETECT pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG68

PADCTRL_REG68 is a drive capability register for the SDIO1_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x0110	PADCTRL_REG68	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cwpr_sr	reserved	sdio1_cwpr_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cwpr_sr	Level conversion rate of the SDIO1_CWPR pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sdio1_cwpr_ds	Drive current of the SDIO1_CWPR pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG69

PADCTRL_REG69 is a drive capability register for the SDIO1_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x0114	PADCTRL_REG69	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_ccmd_sr	sdio1_ccmd_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_ccmd_sr	Level conversion rate of the SDIO1_CCMD pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_ccmd_ds	Drive current of the SDIO1_CCMD pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG70

PADCTRL_REG70 is a drive capability register for the SDIO1_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x0118	PADCTRL_REG70	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cdata0_sr	sdio1_cdata0_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cdata0_sr	Level conversion rate of the SDIO1_CDATA0 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_cdata0_ds	Drive current of the SDIO1_CDATA0 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG71

PADCTRL_REG71 is a drive capability register for the SDIO1_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x011C	PADCTRL_REG71	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cdata1_sr	sdio1_cdata1_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cdata1_sr	Level conversion rate of the SDIO1_CDATA1 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_cdata1_ds	Drive current of the SDIO1_CDATA1 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG72

PADCTRL_REG72 is a drive capability register for the SDIO1_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x0120	PADCTRL_REG72	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cdata2_sr	sdio1_cdata2_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cdata2_sr	Level conversion rate of the SDIO1_CDATA2 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_cdata2_ds	Drive current of the SDIO1_CDATA2 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG73

PADCTRL_REG73 is a drive capability register for the SDIO1_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x0124	PADCTRL_REG73	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sdio1_cdata3_sr	sdio1_cdata3_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sdio1_cdata3_sr	Level conversion rate of the SDIO1_CDATA3 pin 0: fast edge 1: slow edge
[6:4]	RW	sdio1_cdata3_ds	Drive current of the SDIO1_CDATA3 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG74

PADCTRL_REG74 is a drive capability register for the SFC_SIO_IO0 pin.

Offset Address	Register Name	Total Reset Value
0x0128	PADCTRL_REG74	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_sio_io0_sr	reserved	sfc_sio_io0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_sio_io0_sr	Level conversion rate of the SFC_SIO_IO0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_sio_io0_ds	Drive current of the SFC_SIO_IO0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG75

PADCTRL_REG75 is a drive capability register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x012C	PADCTRL_REG75	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_wp_io1_sr	reserved	sfc_wp_io1_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_wp_io1_sr	Level conversion rate of the SFC_WP_IO2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_wp_io1_ds	Drive current of the SFC_WP_IO2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG76

PADCTRL_REG76 is a drive capability register for the SFC_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0130	PADCTRL_REG76	0x0000_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_clk_sr	reserved	sfc_clk_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_clk_sr	Level conversion rate of the SFC_CLK pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_clk_ds	Drive current of the SFC_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG77

PADCTRL_REG77 is a drive capability register for the SFC_SOI_IO1 pin.

Offset Address	Register Name	Total Reset Value
0x0134	PADCTRL_REG77	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_soi_io1_sr	reserved	sfc_soi_io1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_soi_io1_sr	Level conversion rate of the SFC_SOI_IO1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_soi_io1_ds	Drive current of the SFC_SOI_IO1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG78

PADCTRL_REG78 is a drive capability register for the SFC_HOLD_IO3 pin.

Offset Address	Register Name	Total Reset Value
0x0138	PADCTRL_REG78	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_hold_io3_sr	reserved	sfc_hold_io3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_hold_io3_sr	Level conversion rate of the SFC_HOLD_IO3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_hold_io3_ds	Drive current of the SFC_HOLD_IO3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG79

PADCTRL_REG79 is a drive capability register for the SFC_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x013C	PADCTRL_REG79	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_csn1_sr	reserved	sfc_csn1_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	sfc_csn1_sr	Level conversion rate of the SFC_CSN1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	sfc_csn1_ds	Drive current of the SFC_CSN1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG80

PADCTRL_REG80 is a drive capability register for the NF_DQ0 pin.

Offset Address	Register Name	Total Reset Value
0x0140	PADCTRL_REG80	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq0_sr	reserved	nf_dq0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq0_sr	Level conversion rate of the NF_DQ0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq0_ds	Drive current of the NF_DQ0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG81

PADCTRL_REG81 is a drive capability register for the NF_DQ1 pin.

Offset Address	Register Name	Total Reset Value
0x0144	PADCTRL_REG81	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq1_sr	reserved	nf_dq1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq1_sr	Level conversion rate of the NF_DQ1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq1_ds	Drive current of the NF_DQ1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG82

PADCTRL_REG82 is a drive capability register for the NF_DQ2 pin.

Offset Address	Register Name	Total Reset Value
0x0148	PADCTRL_REG82	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq2_sr	reserved	nf_dq2_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq2_sr	Level conversion rate of the NF_DQ2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq2_ds	Drive current of the NF_DQ2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG83

PADCTRL_REG83 is a drive capability register for the NF_DQ3 pin.

Offset Address	Register Name	Total Reset Value
0x014C	PADCTRL_REG83	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq3_sr	reserved	nf_dq3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq3_sr	Level conversion rate of the NF_DQ3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq3_ds	Drive current of the NF_DQ3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG84

PADCTRL_REG84 is a drive capability register for the NF_DQ4 pin.

Offset Address	Register Name	Total Reset Value
0x0150	PADCTRL_REG84	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq4_sr	reserved	nf_dq4_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq4_sr	Level conversion rate of the NF_DQ4 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq4_ds	Drive current of the NF_DQ4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG85

PADCTRL_REG85 is a drive capability register for the NF_DQ5 pin.

Offset Address	Register Name	Total Reset Value
0x0154	PADCTRL_REG85	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq5_sr	reserved	nf_dq5_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq5_sr	Level conversion rate of the NF_DQ5 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq5_ds	Drive current of the NF_DQ5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG86

PADCTRL_REG86 is a drive capability register for the NF_DQ6 pin.

Offset Address	Register Name	Total Reset Value
0x0158	PADCTRL_REG86	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq6_sr	reserved	nf_dq6_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq6_sr	Level conversion rate of the NF_DQ6 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq6_ds	Drive current of the NF_DQ6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG87

PADCTRL_REG87 is a drive capability register for the NF_DQ7 pin.

Offset Address	Register Name	Total Reset Value
0x015C	PADCTRL_REG87	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_dq7_sr	reserved	nf_dq7_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_dq7_sr	Level conversion rate of the NF_DQ7 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_dq7_ds	Drive current of the NF_DQ7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG88

PADCTRL_REG88 is a drive capability register for the NF_RDY0 pin.

Offset Address	Register Name	Total Reset Value
0x0160	PADCTRL_REG88	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_rdy0_sr	reserved	nf_rdy0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_rdy0_sr	Level conversion rate of the NF_RDY0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_rdy0_ds	Drive current of the NF_RDY0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG89

PADCTRL_REG89 is a drive capability register for the NF_RDY1 pin.

Offset Address	Register Name	Total Reset Value
0x0164	PADCTRL_REG89	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_rdy1_sr	reserved	nf_rdy1_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_rdy1_sr	Level conversion rate of the NF_RDY1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_rdy1_ds	Drive current of the NF_RDY1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG90

PADCTRL_REG90 is a drive capability register for the NF_REN pin.

Offset Address	Register Name	Total Reset Value
0x0168	PADCTRL_REG90	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_ren_sr	reserved	nf_ren_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_ren_sr	Level conversion rate of the NF_REN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_ren_ds	Drive current of the NF_REN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG91

PADCTRL_REG91 is a drive capability register for the NF_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x016C	PADCTRL_REG91	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_csn0_sr	reserved	nf_csn0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_csn0_sr	Level conversion rate of the NF_CSN0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_csn0_ds	Drive current of the NF_CSN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG92

PADCTRL_REG92 is a drive capability register for the NF_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x0170	PADCTRL_REG92	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_csn1_sr	reserved	nf_csn1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_csn1_sr	Level conversion rate of the NF_CSN1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_csn1_ds	Drive current of the NF_CSN1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG93

PADCTRL_REG93 is a drive capability register for the NF_CLE pin.

Offset Address	Register Name	Total Reset Value
0x0174	PADCTRL_REG93	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_cle_sr	reserved	nf_cle_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_cle_sr	Level conversion rate of the NF_CLE pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_cle_ds	Drive current of the NF_CLE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG94

PADCTRL_REG94 is a drive capability register for the NF_ALE pin.

Offset Address	Register Name	Total Reset Value
0x0178	PADCTRL_REG94	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_ale_sr	reserved	nf_ale_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_ale_sr	Level conversion rate of the NF_ALE pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_ale_ds	Drive current of the NF_ALE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG95

PADCTRL_REG95 is a drive capability register for the NF_WEN pin.

Offset Address	Register Name	Total Reset Value
0x017C	PADCTRL_REG95	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								nf_wen_sr	reserved	nf_wen_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	nf_wen_sr	Level conversion rate of the NF_WEN pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	nf_wen_ds	Drive current of the NF_WEN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG96

PADCTRL_REG96 is a drive capability register for the PWM0 pin.

Offset Address	Register Name	Total Reset Value
0x0180	PADCTRL_REG96	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pwm0_sr	reserved	pwm0_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pwm0_sr	Level conversion rate of the PWM0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	pwm0_ds	Drive current of the PWM0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG97

PADCTRL_REG97 is a drive capability register for the PWM1 pin.

Offset Address	Register Name	Total Reset Value
0x0184	PADCTRL_REG97	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pwm1_sr	reserved	pwm1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pwm1_sr	Level conversion rate of the PWM1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	pwm1_ds	Drive current of the PWM1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG98

PADCTRL_REG98 is a drive capability register for the PWM2 pin.

Offset Address	Register Name	Total Reset Value
0x0188	PADCTRL_REG98	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pwm2_sr	reserved	pwm2_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pwm2_sr	Level conversion rate of the PWM2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	pwm2_ds	Drive current of the PWM2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG99

PADCTRL_REG99 is a drive capability register for the PWM3 pin.

Offset Address	Register Name	Total Reset Value
0x018C	PADCTRL_REG99	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pwm3_sr	reserved	pwm3_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pwm3_sr	Level conversion rate of the PWM3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	pwm3_ds	Drive current of the PWM3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG100

PADCTRL_REG100 is a drive capability register for the SAR_ADC_CH0 pin.

Offset Address	Register Name	Total Reset Value
0x0190	PADCTRL_REG100	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					sar_adc_ch0_st	sar_adc_ch0_pd	sar_adc_ch0_pu	sar_adc_ch0_sl	reserved	sar_adc_ch0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RW	sar_adc_ch0_st	Input Schmitt control for the SAR_ADC_CH0 pin 0: no Schmitt input 1: Schmitt input
[9]	RW	sar_adc_ch0_pd	Input pull-down control for the SAR_ADC_CH0 pin 0: no pull-down 1: pull-down

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[8]	RW	sar_adc_ch0_pu	Input pull-up control for the SAR_ADC_CH0 pin 0: no pull-up 1: pull-up
[7]	RW	sar_adc_ch0_sl	Level conversion rate of the SAR_ADC_CH0 pin 0: slow edge 1: fast edge
[6]	RO	reserved	Reserved
[5:4]	RW	sar_adc_ch0_ds	Drive current of the SAR_ADC_CH0 pin 00: 1.9 mA 01: 3.7 mA 10: 5.7 mA 11: 7.5 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG101

PADCTRL_REG101 is a drive capability register for the SAR_ADC_CH1 pin.

Offset Address	Register Name	Total Reset Value
0x0194	PADCTRL_REG101	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					sar_adc_ch1_st	sar_adc_ch1_pd	sar_adc_ch1_pu	sar_adc_ch1_sl	reserved	sar_adc_ch1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RW	sar_adc_ch1_st	Input Schmitt control for the SAR_ADC_CH1 pin 0: no Schmitt input 1: Schmitt input
[9]	RW	sar_adc_ch1_pd	Input pull-down control for the SAR_ADC_CH1 pin 0: no pull-down 1: pull-down

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[8]	RW	sar_adc_ch1_pu	Input pull-up control for the SAR_ADC_CH1 pin 0: no pull-up 1: pull-up
[7]	RW	sar_adc_ch1_sl	Level conversion rate of the SAR_ADC_CH1 pin 0: slow edge 1: fast edge
[6]	RO	reserved	Reserved
[5:4]	RW	sar_adc_ch1_ds	Drive current of the SAR_ADC_CH1 pin 00: 1.9 mA 01: 3.7 mA 10: 5.7 mA 11: 7.5 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG102

PADCTRL_REG102 is a drive capability register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0198	PADCTRL_REG102	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ephy_clk_sr	ephy_clk_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ephy_clk_sr	Level conversion rate of the EPHY_CLK pin 0: fast edge 1: slow edge

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[6:4]	RW	ephy_clk_ds	Drive current of the EPHY_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG103

PADCTRL_REG103 is a drive capability register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x019C	PADCTRL_REG103	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mdck_sr	mdck_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	mdck_sr	Level conversion rate of the MDCK pin 0: fast edge 1: slow edge
[6:4]	RW	mdck_ds	Drive current of the MDCK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG104

PADCTRL_REG104 is a drive capability register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x01A0	PADCTRL_REG104	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mdio_sr	mdio_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	mdio_sr	Level conversion rate of the MDIO pin 0: fast edge 1: slow edge
[6:4]	RW	mdio_ds	Drive current of the MDIO pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG105

PADCTRL_REG105 is a drive capability register for the RGMII_TX_EN pin.

Offset Address	Register Name	Total Reset Value
0x01A4	PADCTRL_REG105	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_tx_en_sr	rgmii_tx_en_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_tx_en_sr	Level conversion rate of the RGMII_TX_EN pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_tx_en_ds	Drive current of the RGMII_TX_EN pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG106

PADCTRL_REG106 is a drive capability register for the RGMII_TX_CLK pin.

Offset Address	Register Name	Total Reset Value
0x01A8	PADCTRL_REG106	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_tx_clk_sr	rgmii_tx_clk_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_tx_clk_sr	Level conversion rate of the RGMII_TX_CLK pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_tx_clk_ds	Drive current of the RGMII_TX_CLK pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG107

PADCTRL_REG107 is a drive capability register for the RGMII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x01AC	PADCTRL_REG107	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_txd0_sr	rgmii_txd0_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_txd0_sr	Level conversion rate of the RGMII_TXD0 pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_txd0_ds	Drive current of the RGMII_TXD0 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG108

PADCTRL_REG108 is a drive capability register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x01B0	PADCTRL_REG108	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_txd1_sr	rgmii_txd1_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_txd1_sr	Level conversion rate of the RGMII_TXD1 pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_txd1_ds	Drive current of the RGMII_TXD1 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG109

PADCTRL_REG109 is a drive capability register for the RGMII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x01B4	PADCTRL_REG109	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_txd2_sr	rgmii_txd2_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_txd2_sr	Level conversion rate of the RGMII_TXD2 pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_txd2_ds	Drive current of the RGMII_TXD2 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG110

PADCTRL_REG110 is a drive capability register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x01B8	PADCTRL_REG110	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_txd3_sr	rgmii_txd3_ds			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_txd3_sr	Level conversion rate of the RGMII_TXD3 pin 0: fast edge 1: slow edge
[6:4]	RW	rgmii_txd3_ds	Drive current of the RGMII_TXD3 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG111

PADCTRL_REG111 is a drive capability register for the RGMII_RX_CLK pin.

Offset Address	Register Name	Total Reset Value
0x01BC	PADCTRL_REG111	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rx_clk_sr	reserved	rgmii_rx_clk_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rx_clk_sr	Level conversion rate of the RGMII_RX_CLK pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rx_clk_ds	Drive current of the RGMII_RX_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG112

PADCTRL_REG112 is a drive capability register for the RGMII_RX_DV pin.

Offset Address	Register Name	Total Reset Value
0x01C0	PADCTRL_REG112	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rx_dv_sr	reserved	rgmii_rx_dv_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rx_dv_sr	Level conversion rate of the RGMII_RX_DV pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rx_dv_ds	Drive current of the RGMII_RX_DV pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG113

PADCTRL_REG113 is a drive capability register for the RGMII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x01C4	PADCTRL_REG113	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rxd0_sr	reserved	rgmii_rxd0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rxd0_sr	Level conversion rate of the RGMII_RXD0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rxd0_ds	Drive current of the RGMII_RXD0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG114

PADCTRL_REG114 is a drive capability register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x01C8	PADCTRL_REG114	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rxd1_sr	reserved	rgmii_rxd1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rxd1_sr	Level conversion rate of the RGMII_RXD1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rxd1_ds	Drive current of the RGMII_RXD1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG115

PADCTRL_REG115 is a drive capability register for the RGMII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x01CC	PADCTRL_REG115	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rxd2_sr	reserved	rgmii_rxd2_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rxd2_sr	Level conversion rate of the RGMII_RXD2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rxd2_ds	Drive current of the RGMII_RXD2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG116

PADCTRL_REG116 is a drive capability register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x01D0	PADCTRL_REG116	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgmii_rxd3_sr	reserved	rgmii_rxd3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rgmii_rxd3_sr	Level conversion rate of the RGMII_RXD3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	rgmii_rxd3_ds	Drive current of the RGMII_RXD3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG117

PADCTRL_REG117 is a drive capability register for the VI_CLK pin.

Offset Address	Register Name	Total Reset Value
0x01D4	PADCTRL_REG117	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_clk_sr	reserved	vi_clk_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_clk_sr	Level conversion rate of the VI_CLK pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_clk_ds	Drive current of the VI_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG118

PADCTRL_REG118 is a drive capability register for the VI_HS pin.

Offset Address	Register Name	Total Reset Value
0x01D8	PADCTRL_REG118	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_hs_sr	reserved	vi_hs_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_hs_sr	Level conversion rate of the VI_HS pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_hs_ds	Drive current of the VI_HS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

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[3:0]	RO	reserved	Reserved

PADCTRL_REG119

PADCTRL_REG119 is a drive capability register for the VI_VS pin.

Offset Address	Register Name	Total Reset Value
0x01DC	PADCTRL_REG119	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_vs_sr	reserved	vi_vs_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_vs_sr	Level conversion rate of the VI_VS pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_vs_ds	Drive current of the VI_VS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG120

PADCTRL_REG120 is a drive capability register for the VI_DAT15 pin.

Offset Address	Register Name	Total Reset Value
0x01E0	PADCTRL_REG120	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat15_sr	reserved	vi_dat15_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat15_sr	Level conversion rate of the VI_DAT15 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat15_ds	Drive current of the VI_DAT15 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG121

PADCTRL_REG121 is a drive capability register for the VI_DAT14 pin.

Offset Address	Register Name	Total Reset Value
0x01E4	PADCTRL_REG121	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat14_sr	reserved	vi_dat14_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat14_sr	Level conversion rate of the VI_DAT14 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat14_ds	Drive current of the VI_DAT14 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG122

PADCTRL_REG122 is a drive capability register for the VI_DAT13 pin.

Offset Address	Register Name	Total Reset Value
0x01E8	PADCTRL_REG122	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat13_sr	reserved	vi_dat13_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat13_sr	Level conversion rate of the VI_DAT13 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vi_dat13_ds	Drive current of the VI_DAT13 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG123

PADCTRL_REG123 is a drive capability register for the VI_DAT12 pin.

Offset Address	Register Name	Total Reset Value
0x01EC	PADCTRL_REG123	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat12_sr	reserved	vi_dat12_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat12_sr	Level conversion rate of the VI_DAT12 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat12_ds	Drive current of the VI_DAT12 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG124

PADCTRL_REG124 is a drive capability register for the VI_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x01F0	PADCTRL_REG124	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat11_sr	reserved	vi_dat11_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat11_sr	Level conversion rate of the VI_DAT11 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat11_ds	Drive current of the VI_DAT11 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG125

PADCTRL_REG125 is a drive capability register for the VI_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x01F4	PADCTRL_REG125	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat10_sr	reserved	vi_dat10_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat10_sr	Level conversion rate of the VI_DAT10 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat10_ds	Drive current of the VI_DAT10 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG126

PADCTRL_REG126 is a drive capability register for the VI_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x01F8	PADCTRL_REG126	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat9_sr	reserved	vi_dat9_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat9_sr	Level conversion rate of the VI_DAT9 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vi_dat9_ds	Drive current of the VI_DAT9 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG127

PADCTRL_REG127 is a drive capability register for the VI_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x01FC	PADCTRL_REG127	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat8_sr	reserved	vi_dat8_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat8_sr	Level conversion rate of the VI_DAT8 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat8_ds	Drive current of the VI_DAT8 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG128

PADCTRL_REG128 is a drive capability register for the VI_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0200	PADCTRL_REG128	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat7_sr	reserved	vi_dat7_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat7_sr	Level conversion rate of the VI_DAT7 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat7_ds	Drive current of the VI_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG129

PADCTRL_REG129 is a drive capability register for the VI_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0204	PADCTRL_REG129	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat6_sr	reserved	vi_dat6_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat6_sr	Level conversion rate of the VI_DAT6 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat6_ds	Drive current of the VI_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG130

PADCTRL_REG130 is a drive capability register for the VI_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0208	PADCTRL_REG130	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat5_sr	reserved	vi_dat5_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat5_sr	Level conversion rate of the VI_DAT5 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vi_dat5_ds	Drive current of the VI_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG131

PADCTRL_REG131 is a drive capability register for the VI_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x020C	PADCTRL_REG131	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat4_sr	reserved	vi_dat4_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat4_sr	Level conversion rate of the VI_DAT4 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat4_ds	Drive current of the VI_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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PADCTRL_REG132

PADCTRL_REG132 is a drive capability register for the VI_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0210	PADCTRL_REG132	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat3_sr	reserved	vi_dat3_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat3_sr	Level conversion rate of the VI_DAT3 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat3_ds	Drive current of the VI_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG133

PADCTRL_REG133 is a drive capability register for the VI_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0214	PADCTRL_REG133	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat2_sr	reserved	vi_dat2_ds		reserved			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat2_sr	Level conversion rate of the VI_DAT2 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat2_ds	Drive current of the VI_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG134

PADCTRL_REG134 is a drive capability register for the VI_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0218	PADCTRL_REG134	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat1_sr	reserved	vi_dat1_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat1_sr	Level conversion rate of the VI_DAT1 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved

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[5:4]	RW	vi_dat1_ds	Drive current of the VI_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

PADCTRL_REG135

PADCTRL_REG135 is a drive capability register for the VI_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x021C	PADCTRL_REG135	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vi_dat0_sr	reserved	vi_dat0_ds		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	vi_dat0_sr	Level conversion rate of the VI_DAT0 pin 0: fast edge 1: slow edge
[6]	RO	reserved	Reserved
[5:4]	RW	vi_dat0_ds	Drive current of the VI_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3:0]	RO	reserved	Reserved

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2.7 Electrical Specifications

2.7.1 Power Consumption Parameters

Table 2-81 describes power consumption parameters.

CAUTION

- The values of power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3516A Hardware Design User Guide*.

Table 2-81 Power consumption parameters

Parameter	Description	Typ	Max	Unit
VDD core power	Power consumption of the VDD core power domain	56	107	mW
CPU power	Power consumption of the CPU power domain	36	119	mW
MEDIA power	Power consumption of the MEDIA power domain	682	808	mW
DDR power	Power consumption of the DDR power domain	71	103	mW
MIPI 1.8V power	Power consumption of the 1.8 V power	26	26	mW
3.3 V power	Power consumption of the 3.3 V I/O power	200	200	mW
1.5 V power	Power consumption of the DDR interface	120	120	mW

2.7.2 Temperature and Thermal Resistance Parameters

Table 2-82 describes temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3516A Hardware Design User Guide*.

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Table 2-82 Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	0	None	70	℃
Rated temperature	T_{JMAX}	–20	None	105	℃
Junction-to-ambient thermal resistance	θ_{JA}	None	24	None	℃/W
Junction-to-board thermal resistance	θ_{JB}	None	12.26	None	℃/W
Junction-to-case thermal resistance	θ_{JC}	None	6.25	None	℃/W

2.7.3 Operating Conditions

Table 2-83 and Table 2-84 describes operating conditions.

CAUTION

The prerequisite for using the VDD voltage range (when SVB is used) listed in Table 2-83 is as follows: the customer's board must use the SVB circuit, and the impedance and capacitance parameters of the SVB circuit must completely copy the related RC parameters of Hi3518EV20XDMEB VER.A.

Table 2-83 Operating conditions for the SVB related power supply

Symbol	Description	SVB voltage range			Unit
		Min	Typ	Max	
VDD	Internal core power	1.01	1.05	1.1	V
VDD_CPU	CPU power	0.99	1.1	1.3	V
VDD_MEDIA	Media power	0.95	1.04	1.1	V
VDD_DDR	DDR core power	1.01	1.05	1.1	V
AVDD11_PLL	PLL core analog power	0.99	1.1	1.21	V

Table 2-84 Operating conditions for the power supply under normal voltage

Symbol	Description	Min	Typ	Max	Unit
DVDD33	I/O power	2.97	3.3	3.63	V
DVDD3318_VI	VI I/O power	1.62	1.8	1.98	V

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Symbol	Description	Min	Typ	Max	Unit
	VI I/O power	2.97	3.3	3.63	V
DVDD3318_SENSOR	SENSOR, SPI0 I/O power	1.62	1.8	1.98	V
	SENSOR, SPI0 I/O power	2.97	3.3	3.63	V
DVDD3318_RGMII	RGMII I/O power	1.62	1.8	1.98	V
	RGMII I/O power	2.25	2.5	2.75	V
	RGMII I/O power	2.97	3.3	3.63	V
DVDD18_SDIO	SDIO1.8V I/O power	1.62	1.8	1.98	V
VDDIO_DDR	DDR3L interface power	1.282	1.35	1.418	V
	DDR3 interface power	1.425	1.5	1.575	V
AVDD_DDRPLL 1/2/3	DDR3/3L PLL3.3V analog power	2.97	3.3	3.63	V
AVDD33_PLL	PLL 3.3V analog power	2.97	3.3	3.63	V
AVDD33_VDAC	VDAC 3.3V analog power	2.97	3.3	3.63	V
AVDD33_AC	ACODEC 3.3V analog power	3	3.3	3.6	V
AVDD33_USB	USB 3.3V analog power	3	3.3	3.6	V
AVDD18_MIPI	MIPI analog power	1.71	1.8	1.89	V
	3.3 V power when the MIPI signal is multiplexed as a single-ended signal	2.97	3.3	3.63	V
AVDD_BAT	RTC battery power	1.6	3.3	3.6	V
AVDD33_RTC	RTC analog power	2.97	3.3	3.63	V

2.7.4 Power-On and Power-Off Sequences

For details about power-on and power-off sequences, see section 1.2.5 "requirements on the power-on and power-off timing" in the *Hi3516A/Hi3516D Hardware Design User Guide*.

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2.7.5 DC and AC Electrical Parameters

Table 2-85 and Table 2-86 describes DC parameters.

Table 2-85 DC electrical parameters (DVDD33/DVDD3318_VI/DVDD3318_SENSOR/DVDDIO_RGMII = 3.3 V, incompatible with the 5 V input current)

Symbol	Description	Min	Type	Max	Unit	Remarks
DVDD33	Interface voltage	2.97	3.3	3.63	V	The interface is incompatible with the 5 V input current.
V_{IH}	High-level input voltage	2.0	None	DVDD33 + 0.3 V	V	None
V_{IL}	Low-level input voltage	–0.3	None	0.8	V	None
I_L	Input leakage current	None	None	±10	μA	None
I_{OZ}	Tristate output leakage current	None	None	±10	μA	None
V_{OH}	High-level output voltage	2.4	None	None	V	None
V_{OL}	Low-level output voltage	None	None	0.4	V	None
R_{PU}	Internal pull-up impedance	33	80	100	kΩ	None
R_{PD}	Internal pull-down impedance	33	80	100	kΩ	None

Table 2-86 DC electrical parameters (DVDD3318*=1.8V/DVDDIO_RGMII=1.8V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD18	Interface voltage	1.62	1.8	1.98	V	None
V_{IH}	High-level input voltage	1.17	None	DVDD18 + 0.3 V	V	None
V_{IL}	Low-level input voltage	–0.3	None	0.63	V	None
I_L	Input leakage current	None	None	±10	μA	None
I_{OZ}	Tristate output leakage current	None	None	±10	μA	None
V_{OH}	High-level output voltage	1.35	None	None	V	None

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Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OL}	Low-level output voltage	None	None	0.45	V	None
R_{PU}	Internal pull-up impedance	80	None	100	kΩ	None
R_{PD}	Internal pull-down impedance	80	None	100	kΩ	None

Table 2-87 describes DC electrical parameters in DDR3 SSTL15 mode.

Table 2-87 DC electrical parameters in DDR3 SSTL15 mode (VDDIO_DDR = 1.5 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V	None
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	V	(0.49~0.51) x VDDIO_DDR
$V_{IH(DC)}$	High-level input voltage	Vref+0.1	None	VDDIO_DDR +0.3	V	None
$V_{IL(DC)}$	Low-level input voltage	–0.3	None	Vref–0.1	V	None
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	None	(1+0.1) x VDDIO_DDR	V	The driver is configurable.
V_{OL}	Low-level output voltage	0	None	0.2 x VDDIO_DDR	V	The driver is configurable.
I_{OH}	High-level output current	None	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
I_{OL}	Low-level output current	None	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
Output impedance	None	34	None	80	Ω	None

Table 2-88 describes AC electrical parameters in DDR3 SSTL15 mode.

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Table 2-88 AC electrical parameters in DDR3 SSTL15 mode (VDDIO_DDR = 1.5 V)

Symbol	Parameter	Min	Max	Unit	Remarks
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR+0.3	V	None
$V_{IL(AC)}$	Low-level input voltage	None	Vref–0.15	V	None

Table 2-89 describes DC electrical parameters in DDR3L SSTL135 mode.

Table 2-89 DC electrical parameters in DDR3L SSTL135 mode (VDDIO_DDR = 1.35 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.283	1.35	1.45	V	None
VREF	Reference voltage of the DDR interface	0.49 x VDDIO_DDR	0.5 x VDDIO _DDR	0.51 x VDDIO_DDR	V	None
$V_{IH(DC)}$	High-level input voltage	0.49 x VDDIO_DDR +0.125	None	VDDIO_DDR +0.3	V	None
$V_{IL(DC)}$	Low-level input voltage	–0.3	None	0.51 x VDDIO_DDR -0.125	V	None
V_{OH}	High-level output voltage	VDDIO_DDR -0.28	None	None	V	None
V_{OL}	Low-level output voltage	None	None	VDDIO_DDR +0.28	V	None
I_{OH}	High-level output current	None	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
I_{OL}	Low-level output current	None	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.

Table 2-90 describes the AC electrical specifications in DDR3L SSTL135 mode.

Table 2-90 AC electrical specifications in DDR3L SSTL135 mode (VDDIO_DDR = 1.35 V)

Symbol	Description	533−1600 Mbit/s		Unit	Remarks
		Min	Max		
$V_{IH(AC)}$	AC high-level input voltage	0.49 x VDDIO_DDR + 0.25	None	V	None

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Symbol	Description	533−1600 Mbit/s		Unit	Remarks
		Min	Max		
$V_{IL(AC)}$	AC low-level input voltage	None	0.51 x VDDIO_DDR – 0.25	V	None

2.7.6 MIPI/LVDS RX Electrical Parameters

Table 2-91 describes low-voltage differential signaling (LVDS) differential DC electrical parameters.

Table 2-91 LVDS differential DC electrical parameters

Symbol	Description		Min	Typ	Max	Unit
VIDTH(SL)	Differential Input Threshold Voltage |(VP−VM)|	Sub-LVDS	70	-	-	mV
VIDTH(HS)		HiSPi(SLVS)	70	-	-	
VIDTH(HiVCM)		HiSPi(HiVCM)	100	-	-	
VIDTH(DP)		D-PHY HS	70	-	-	
VIDTH(LV)		LVDS	100	-	-	
VIDTH(ML)		Mini-LVDS	100	-	-	
VCM(SL)	Common Mode Voltage Range (VP+VM)/2	Sub-LVDS	0.5	0.9	1.3	V
VCM(HS)		HiSPi(SLVS)	0.07	0.2	0.35	
VCM(HiVCM)		HiSPi(HiVCM)	0.66	0.90	1.17	
VCM(DP)		D-PHY HS	0.07	0.2	0.33	
VCM(LV)		LVDS	0.925	1.2	1.475	
VCM(ML)		Mini-LVDS	1.025	1.2	1.375	
VISVR (SL)	Single-ended Input Voltage Range VP,VM	Sub-LVDS	0.4		1.4	V
VCM(HS)		HiSPi(SLVS)	-0.04		0.49	
VCM(HiVCM)		HiSPi(HiVCM)	0.55		1.35	
VCM(DP)		D-PHY HS	-0.04		0.46	
VCM(LV)		LVDS	0		1.8	
VCM(ML)		Mini-LVDS	0.825		1.575	
ZID(SL)	Internal Termination Resister Value	Sub-LVDS	80	100	120	Ω
ZID(HS)		HiSPi(SLVS)			125	
ZID(HiVCM)		HiSPi(HiVCM)			125	

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Symbol	Description		Min	Typ	Max	Unit
ZID(LV)		LVDS			120	
ZID(ML)		Mini-LVDS			120	
ZID(DP)		D-PHY HS			125	

Table 2-92 to Table 2-94 describe the MIPI parameters.

Table 2-92 MIPI high-speed (HS) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VTERM-EN	Single-ended threshold for HS termination enable	-	-	450	mV

Table 2-93 MIPI HS AC parameters

Symbol	Description	Min	Typ	Max	Unit
ΔVCMRX (HF)	Common-mode interface beyond 450 MHz	-	-	100	-
ΔVCMRX (LF)	Common-mode interface 50 MHz–450 MHz	-50	-	50	mV
CCM	Common-mode termination	-	-	60	pF

Table 2-94 MIPI low-power (LP) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VIHLP	Logic 1 input voltage	880	-	-	mV
VILLP	Logic 0 input voltage	-	-	550	
VHYST	Input hysteresis	25	-	-	

2.7.7 SDIO Electrical Parameters

Table 2-95 describes the SDIO electrical parameters (3.3 V).

Table 2-95 SDIO electrical parameters (3.3 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO	Power supply voltage	2.97	3.3	3.6	V	-

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Symbol	Description	Min	Typ	Max	Unit	Remarks
VOH	Output high level	2.4	-		V	
VOL	Output low level	-	-	0.4	V	
VIH	Input high level	2.0	-	VDD IO + 0.3	V	
VIL	Input low level	– 0.3	-	0.8	V	
-	Power-on duration	-	-	250	Ms	0 V to VDDIO

Table 2-96 describes the SDIO electrical parameters (1.8 V).

Table 2-96 SDIO electrical parameters (1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO	Power supply voltage	1.62	1.8	1.98	V	-
VOH	Output high level	1.35	-	-	V	
VOL	Output low level	-	-	0.45	V	
VIH	Input high level	1.17	-	VDDIO+0.3	V	
VIL	Input low level	– 0.3	-	0.63	V	
-	Power-on duration	-	-	250	ms	0 V to VDDIO

2.7.8 Audio CODEC Electrical Parameters

Table 2-97 to Table 2-101 describe the electrical parameters of the audio CODEC.

Table 2-97 Overall specifications

Description	Min	Typ	Max	Unit	Remarks
Analog circuit power AVDD	3	3.3	3.6	V	Relative to AGND
VREF	-	AVDD/2		V	Relative to AGND

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Table 2-98 Major DAC specifications

Description	Min	Typ	Max	Unit	Remarks
Output amplitude at full scale	-	0.875	-	Vrms	Maximum output signal swing

Table 2-99 Major ADC specifications

Description	Min	Typ	Max	Unit	Remarks
Maximum input amplitude	-	1	-	Vrms	Maximum input signal swing of the ADC

Table 2-100 Major MICBIAS specifications

Description	Min	Typ	Max	Unit	Remarks
Bias voltage	-	2.1 x AVDD/3.3	-	V	MIC bias voltage
Maximum output current	-	-	3	mA	-

Table 2-101 Major MICPGA specifications

Description	Min	Typ	Max	Unit	Remarks
Input voltage range	-	1	-	Vrms	Maximum input signal swing
Input impedance	5	-	12	kΩ	MICPGA input impedance

2.8 PCB Design Recommendations

For details about printed circuit board (PCB) design recommendations, see the *Hi3516A/Hi3516D Hardware Design User Guide*.

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2.9 Interface Timings

2.9.1 DDR Interface Timings

2.9.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH.

Figure 2-12 Write timing of dqs_out relative to dq_out for the DDR3

Write Timings of dqs_out Relative to CK

Figure 2-13 shows the write timing of dqs_out relative to CK for the DDR3.

Figure 2-13 Write timing of dqs_out relative to CK for the DDR3

Write Timing of CMD/ADDR Relative to CK

Figure 2-14 shows the write timing of CMD/ADDR relative to CK.

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Figure 2-14 Write timing of CMD/ADDR relative to CK

2.9.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-15 shows the output timing of the DDRn SDRAM.

Figure 2-15 Output timing of the DDRn SDRAM

2.9.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3516A is based on the timing parameters of the DDR3-1600 SDRAMs.

Table 2-102 and Table 2-103 describe the clock parameters of the DDR3-1600 SDRAM.

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Table 2-102 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	800.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-103 Parameters for the DDR3-1600 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.18	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.18	tCK
Setup time, DQ/DM to DQS	tDS	0.010	ns
Hold time, DQ/DM to DQS	tDH	0.045	ns
Skew between DQS and DQ	tDQSQ	0.100	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.170	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.120	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.225	ns

2.9.2 Timings of the NANDC Interface

2.9.2.1 Command Cycle Timing

Figure 2-16 shows the command cycle timing of the NANDC) interface.

Figure 2-16 Command cycle timing of the NANDC interface

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NOTE

The level widths of NAND_WE_N and NAND_RE_N can be set by configuring the NF_PULSE_WIDTH register of the NANDC. Therefore, some parameters in the timing diagrams of the NANDC interface vary according to the settings of NF_PULSE_WIDTH. In the following tables, these parameters are marked with "Configurable."

Table 2-104 describes the command cycle timing parameters of the NANDC interface.

Table 2-104 Command cycle timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CLE	tCLS	15	None	ns	None
Hold time of NAND_CLE	tCLH	10	None	ns	None
Setup time of NAND_CE_N	tCS	15	None	ns	Configurable
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

2.9.2.2 Address Cycle Timing

Figure 2-17 shows the address cycle timing of the NANDC interface.

Figure 2-17 Address cycle timing of the NANDC interface

Table 2-105 describes the address cycle timing parameters of the NANDC interface.

Table 2-105 Address cycle timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CE_N	tCS	15	None	ns	None

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Parameter	Symbol	Min	Max	Unit	Remarks
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	15	None	ns	None
Hold time of NAND_ALE	tALH	10	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

2.9.2.3 Write Data Timing

Figure 2-18 shows the write data timing of the NANDC interface.

Figure 2-18 Write data timing of the NANDC interface

Table 2-106 describes the write data timing parameters of the NANDC interface.

Table 2-106 Write data timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Hold time of NAND_CLE	tCLH	10	None	ns	Configurable
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	15	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

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Parameter	Symbol	Min	Max	Unit	Remarks
High-level hold time of NAND_WE_N	tWH	15	None	ns	Configurable

2.9.2.4 Read Data Timing

Figure 2-19 shows the read data timing of the NANDC interface.

Figure 2-19 Read data timing of the NANDC interface

Table 2-107 describes the read data timing parameters of the NANDC interface.

Table 2-107 Read data timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Low-level wait time of NAND_RE_N	tRR	15	None	ns	Configurable
Pulse width of NAND_RE_N	tRP	15	None	ns	Configurable
High-level width of NAND_RE_N	tREH	15	None	ns	Configurable

NOTE

The tRR delay is configurable.

2.9.3 SFC Interface Timings

Figure 2-20 shows the SFC input timing.

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Figure 2-20 SFC input timing

Table 2-108 describes the SFC input timing parameters.

Table 2-108 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	16	None	83.2	ns
Input signal setup time	T_{su}	8	None	None	ns
Input signal hold time	T_{hd}	1.2	None	None	ns

Figure 2-21 shows the SFC output timing.

Figure 2-21 SFC output timing

Table 2-109 describes the SFC output timing parameters.

Table 2-109 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	16	None	83.2	ns
Output data signal delay	T_{ov}	-3	None	3	ns
Output CS signal delay	T_{ov}	-3	None	3	ns

2.9.4 Ethernet MAC Port Timings

2.9.4.1 MII Timings

The Hi3516A provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-22 shows the 100 Mbit/s RX timing of the MII.

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Figure 2-22 100 Mbit/s RX timing of the MII

Figure 2-23 shows the 100 Mbit/s TX timing of the MII.

Figure 2-23 100 Mbit/s TX timing of the MII

Figure 2-24 shows the 10 Mbit/s RX timing of the MII.

Figure 2-24 10 Mbit/s RX timing of the MII

Figure 2-25 shows the 10 Mbit/s TX timing of the MII.

Figure 2-25 10 Mbit/s TX timing of the MII

Figure 2-26 shows the RX timing parameters of the MII.

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Figure 2-26 RX timing parameters of the MII

Figure 2-27 shows the TX timing parameters of the MII.

Figure 2-27 TX timing parameters of the MII

Table 2-110 describes the MII timing parameters.

Table 2-110 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	RXCK, TXCK	400 (10 Mbit/s)	400	ns
			40 (100 Mbit/s)	40	
MII signal setup time	Tsu (RX)	RXER, RXDV, RXD[3:0]	10	None	ns
MII signal hold time	Thd (RX)	RXER, RXDV, RXD[3:0]	10	None	ns
MII output signal delay	Tov (MIITX)	TXD[3:0],TX EN	0	25	ns

2.9.4.2 RMII Timings

Figure 2-28 shows the 100 Mbit/s RX timing of the RMII.

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Figure 2-28 100 Mbit/s RX timing of the RMII

Figure 2-29 shows the 100 Mbit/s TX timing of the RMII interface.

Figure 2-29 100 Mbit/s TX timing of the RMII

Figure 2-30 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-30 10 Mbit/s RX timing of the RMII

Figure 2-31 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-31 10 Mbit/s TX timing of the RMII

Figure 2-32 shows the timing parameters of the RMII.

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Figure 2-32 Timing parameters of the RMII

Table 2-111 describes the RMII timing parameters of the RMII.

Table 2-111 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	REF_CLK	20	20	ns
Setup time of RMII signal	Tsu (RX)	CRS_DV/RXD[1:0]	4	None	ns
Hold time of RMII signal	Thd (RX)	CRS_DV/RXD[1:0]	2	None	ns
RMII output signal delay	Tov (TX)	TXEN/TXD[1:0]	3	16	ns

2.9.4.3 RGMII Timings

Figure 2-33 shows the 1000 Mbit/s RX timing of the RGMII.

Figure 2-33 1000 Mbit/s RX timing of the RGMII

Figure 2-34 shows the 1000 Mbit/s TX timing of the RGMII.

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Figure 2-34 1000 Mbit/s TX timing of the RGMII

Table 2-112 describes the timing parameters of the RGMII.

Table 2-112 Timing parameters of the RGMII

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	RXCK, TXCK	8	8	ns
RGMII signal setup time	Tsu(RX)	RXER, RXDV, RXD[3:0]	1	None	ns
RGMII signal hold time	Thd(RX)	RXER, RXDV, RXD[3:0]	1	None	ns
RGMII output signal delay	Tov(TX)	TXD[3:0], TXEN	-0.5	0.5	ns

2.9.4.4 MDIO Interface Timings

Figure 2-35 shows the read timing of the MDIO interface.

Figure 2-35 Read timing of the MDIO interface

Figure 2-36 shows the write timing of the MDIO interface.

Figure 2-36 Write timing of the MDIO interface

Figure 2-37 shows the RX timing parameters of the MDIO interface.

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Figure 2-37 RX timing parameters of the MDIO interface

Table 2-113 describes the timing parameters of the MDIO interface.

Table 2-113 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDCK	400	400	ns
MDIO data TX setup time	Tsu	MDIO	10	None	ns
MDIO data TX hold time	Thd	MDIO	10	None	ns

2.9.5 VI Interface Timing

Figure 2-38 shows the VI interface timing in CMOS mode.

Figure 2-38 VI interface timing in CMOS mode

Table 2-114 describes the VI interface timing parameters.

Table 2-114 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	None	None	ns
Input signal setup time	T_{su}	2.5	None	None	ns
Input signal hold time	T_{hd}	2.0	None	None	ns

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2.9.6 VO Interface Timing

Figure 2-39 shows the timing of the VO interface.

Figure 2-39 Timing of the VO interface

Table 2-115 describes the timing parameters of the VO interface.

Table 2-115 Timing parameters of the VO interface

Parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock cycle	T	6.74	13.48	37	ns
Output signal delay	T_{ov}	T/2-1.5	None	T/2+1.5	ns

2.9.7 AIO Interface Timings

2.9.7.1 I²S Interface Timing

Figure 2-40 shows the RX timing of the I^2S interface.

Figure 2-40 RX timing of the I^2S interface

Figure 2-41 shows the TX timing of the I^2S interface.

Figure 2-41 TX timing of the I^2S interface

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Table 2-116 describes the timing parameters of the I^2S interface.

Table 2-116 Timing parameters of the I^2S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.9.7.2 PCM Interface Timings

Figure 2-42 shows the RX timing of the PCM interface.

Figure 2-42 RX timing of the PCM interface

Figure 2-43 shows the TX timing of the PCM interface

Figure 2-43 TX timing of the PCM interface

Table 2-117 describes the timing parameters of the PCM interface.

Table 2-117 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

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2.9.8 I²C Interface Timing

Figure 2-44 shows the I²C transfer timing.

Figure 2-44 I²C transfer timing

Table 2-118 describes the timing parameters of the I²C interface.

Table 2-118 Timing parameters of the I²C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	μs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	μs
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	μs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	μs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	None	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	μs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	μs
Bus load	C_b	None	400	None	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	None	$0.1V_{DD}$	None	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	None	$0.2V_{DD}$	None	V

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2.9.9 SPI Timings

NOTE

In Figure Figure 2-45 to Figure 2-47, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-45 shows the SPI clock (SPICK) timing.

Figure 2-45 SPICK timing

Figure 2-46 and Figure 2-47 show the SPI timings in master mode.

Figure 2-46 SPI timing in master mode (sph = 1)

Figure 2-47 SPI timing in master mode (sph = 0)

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Table 2-119 describes the SPI timing parameters.

Table 2-119 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit	Remark
1	Cycle time, SPI_CK	tc	2000/Fsspclk	N/A	65024000/Fsspclk	ns	Fsspclk unit: MHz
2	Pulse duration, SPI_CK high (all master modes)	tw1	N/A	1/2 tc	N/A	ns	
3	Pulse duration. SPI_CK low (all master modes)	tw2	N/A	1/2 tc	N/A	ns	
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	N/A	1/2 tc	N/A	ns	
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	N/A	1/2 tc	N/A	ns	
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	N/A	1/2 tc	N/A	ns	
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	N/A	1/2 tc	N/A	ns	
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	0	N/A	N/A	ns	
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	0	N/A	N/A	ns	
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	N/A	tc	N/A	ns	
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	N/A	1/2 tc	N/A	ns	
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	N/A	1/2 tc	N/A	ns	
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	N/A	1/2 tc	N/A	ns	
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising	th3	N/A	1/2 tc	N/A	ns	

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No.	Parameter	Symbol	Min	Typ	Max	Unit	Remark
	edge						
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	N/A	1/2 tc	N/A	ns	
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	0	N/A	N/A	ns	
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	0	N/A	N/A	ns	
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	N/A	1/2 tc	N/A	ns	
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	N/A	tc	N/A	ns	

2.9.10 MIPI RX Timings

Table 2-120 describes the MIPI RX timing parameters.

Table 2-120 MIPI RX timing parameters

Symbol	Description	Min	Tye	Max	Unit
F_{MAX}	Data rate	-	-	1G	bit/s
T_{PERIOD}	Differential clock cycle	2	T	-	ns
T_{DUTY}	Differential clock duty cycle	0.45T	-	0.55T	ns
T_{SET}	Differential clock setup time	0.15 x UI	-	-	ns
T_{HD}	Differential clock hold time	0.15 x UI	-	-	ns
T_{RISE}	Differential clock rising time (20%−80%)	150	-	-	ps
		-	-	0.3	UI
T_{FALL}	Differential clock falling time (20%−80%)	150	-	-	ps
		-	-	0.3	UI

NOTE

UI = T/2

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2.9.11 SDIO Timings

Output Timing

Figure 2-48 Output timing

Input Timing

Figure 2-49 Input timing

Table 2-121 describes the SDIO timing parameters.

Table 2-121 SDIO timing parameters

Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time (T_{IH})	Minimum Setup Time (T_{IS})	Maximum Output Delay of the Card	High Level Duration of the Card Clock
SDR50	100 MHz	10 ns	0.8 ns	3.0 ns	7.5 ns	(0.45−0.55) tCYC
DDR50 (CMD line)	50 MHz	20 ns	0.8 ns	6.0 ns	13.7 ns	
DDR50 (DAT line)	50 MHz	20 ns	0.8 ns	3.0 ns	7.0 ns	
SDR25	50 MHz	20 ns	2.0 ns	6.0 ns	14.0 ns	
SDR12	25 MHz	40 ns	5.0 ns	5.0 ns	14.0 ns	

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Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time (T_{IH})	Minimum Setup Time (T_{IS})	Maximum Output Delay of the Card	High Level Duration of the Card Clock
HS	50 MHz	20 ns	2.0 ns	6.0 ns	14 ns	
DS	25 MHz	40 ns	5.0 ns	5.0 ns	14 ns	
Identification mode	400 kHz	2.5us	5.0 ns	5.0 ns	50 ns	

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Contents

3 System 3-1
3.1 Reset 3-1
3.1.1 Overview 3-1
3.1.2 Reset Control 3-1
3.1.3 Reset Configuration 3-2
3.2 Clock 3-3
3.2.1 Overview 3-3
3.2.2 Clock Control Block Diagram 3-3
3.2.3 Clock Distribution 3-4
3.2.4 PLL Configuration 3-6
3.2.5 Frequency Configurations 3-7
3.2.6 CRG Register Summary 3-10
3.2.7 Register Description 3-11
3.3 Processor Subsystem 3-50
3.4 Interrupt System 3-50
3.5 System Controller 3-52
3.5.1 Overview 3-52
3.5.2 Features 3-52
3.5.3 Function Description 3-52
3.5.4 System Controller Registers 3-55
3.5.5 Peripheral Control Registers 3-76
3.6 DMA Controller 3-113
3.6.1 Overview 3-113
3.6.2 Features 3-113
3.6.3 Function Description 3-113
3.6.4 Operating Mode 3-118
3.6.5 Register Summary 3-122
3.6.6 Register Description 3-124
3.7 Cipher 3-142
3.7.1 Overview 3-142
3.7.2 Features 3-142
3.7.3 Function Description 3-143

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3.7.4 Operating Mode 3-153
3.7.5 Register Summary 3-155
3.7.6 Register Description 3-157
3.8 Timer 3-176
3.8.1 Overview 3-176
3.8.2 Features 3-176
3.8.3 Function Description 3-176
3.8.4 Operating Mode 3-177
3.8.5 Register Summary 3-178
3.8.6 Register Description 3-178
3.9 Watchdog 3-183
3.9.1 Overview 3-183
3.9.2 Features 3-183
3.9.3 Function Description 3-183
3.9.4 Operating Mode 3-184
3.9.5 Register Summary 3-185
3.9.6 Register Description 3-186
3.10 RTC 3-189
3.10.1 Overview 3-189
3.10.2 Features 3-189
3.10.3 Function Description 3-190
3.10.4 Operating Mode 3-190
3.10.5 Register Summary 3-193
3.10.6 RTC Register Description 3-198
3.10.7 Internal Register Description 3-204
3.11 Power Management and Low-Power Mode Control 3-241
3.11.1 Overview 3-241
3.11.2 System Operating Modes 3-241
3.11.3 Clock Gating and Clock Frequency Adjustment 3-242
3.11.4 Module Low-Power Control 3-242
3.11.5 DDR Low-Power Control 3-243
3.11.6 CPU DVFS 3-243
3.11.7 AVS of the CPU/CORE/MDDRC/MDA0 Power Supplies 3-245
3.11.8 Powering on and Powering off the VEDU and AVC 3-247
3.11.9 PMC Register Summary 3-248
3.11.10 PMC Register Description 3-251

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Figures

Figure 3-1 Diagram of controlling reset signals 3-1
Figure 3-2 Functional block diagram of the CRG 3-3
Figure 3-3 Clock distribution diagram 3-5
Figure 3-4 Process of switching the system mode 3-53
Figure 3-5 Bit allocation of chip ID registers 3-55
Figure 3-6 Functional block diagram of the DMAC 3-114
Figure 3-7 Updating channel registers through the LLI 3-115
Figure 3-8 Structure of DMAC LLIs 3-117
Figure 3-9 3DES encryption of a 3-key operation and a 2-key operation 3-143
Figure 3-10 3DES decryption of a 3-key operation and a 2-key operation 3-144
Figure 3-11 ECB mode of the AES and DES algorithms 3-144
Figure 3-12 ECB mode of the 3DES algorithm 3-145
Figure 3-13 CBC mode of the AES and DES algorithms 3-146
Figure 3-14 CBC mode of the 3DES algorithm 3-147
Figure 3-15 S-bit CFB mode of the AES and DES algorithms 3-148
Figure 3-16 S-bit CFB mode of the 3DES algorithm 3-149
Figure 3-17 OFB mode of the AES algorithm 3-150
Figure 3-18 S-bit OFB mode of the DES algorithm 3-151
Figure 3-19 S-bit OFB mode of the 3DES algorithm 3-152
Figure 3-20 CTR mode of the AES algorithm 3-153
Figure 3-21 Structure of the linked list header of a multi-block encryption/decryption channel 3-154
Figure 3-22 Bits of cas 3-155
Figure 3-23 Application block diagram of the watchdog 3-183

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Tables

Table 3-1 Types of reset signals 3-2
Table 3-2 Configuration registers corresponding to PLLs 3-6
Table 3-3 Methods of calculating PLL output frequencies 3-6
Table 3-4 Frequency configurations of A7/DDR/bus clocks 3-7
Table 3-5 Mapping between system controller modes and clock states 3-7
Table 3-6 Frequency configurations of VDP clocks 3-8
Table 3-7 Summary of CRG registers (base address: 0x2003_0000) 3-10
Table 3-8 A7 interrupt sources 3-50
Table 3-9 Summary of system controller registers (base address: 0x2005_0000) 3-55
Table 3-10 Summary of peripheral control registers (base address: 0x2012_0000) 3-76
Table 3-11 DMAC hardware request signals and corresponding peripheral requests 3-116
Table 3-12 Mapping between the value of dbsize or sbsize and the burst length 3-119
Table 3-13 Mapping between the value of dwidth or swidth and the transfer bit width 3-120
Table 3-14 Definitions of the prot_stat field of DMAC_Cn_CONTROL 3-121
Table 3-15 Flow controllers and transfer types corresponding to the flow_cntrl field 3-121
Table 3-16 Summary of the DMAC registers (base address: 0x1006_0000) 3-123
Table 3-17 Summary of cipher registers (base address: 0x100c_0000) 3-155
Table 3-18 Summary of timer registers 3-178
Table 3-19 Summary of watchdog registers (base address: 0x2004_0000) 3-185
Table 3-20 Summary of RTC registers (base address: 0x2006_0000) 3-193
Table 3-21 Summary of internal RTC registers (base address: 0x00) 3-194
Table 3-22 Four CPU profiles 3-243
Table 3-23 Summary of PMC registers (base address: 0x2027_0000) 3-248

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3 System

3.1 Reset

3.1.1 Overview

The reset management module resets the entire chip and all functional modules in a unified manner as follows:

- Manages and controls power-on reset.
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.
- Generates reset signals for each internal functional module.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals

NOTE

- RSTN: pin reset input
- POR: internal power-on reset (POR) module

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- POR_SEL: POR selection
- sys_rst_req: global soft reset request signal. This signal is derived from the system controller.
- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_n, and npor: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from RSTN or the internal POR module	Globally resets the entire Hi3516A.
Global soft reset signal (syn_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3516A, excluding the clock reset circuits, test circuits, and registers that do not support soft reset
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3516A.

3.1.3 Reset Configuration

Power-On Reset

To implement power-on reset, the following conditions must be met:

- The POR input pin or internal POR module generates a low-level pulse, and the low pulse duration is greater than 12 XIN crystal clock cycles.
- The clock input by the XIN pin of the crystal oscillator clock works properly.

System Reset

The system is reset in either of the following ways:

- Power-on reset
- Global soft reset, controlled by the system controller

Soft Reset

Soft reset control is implemented by configuring the corresponding CRG controller. For details about configurations, see the description of the reset register for each module.

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CAUTION

- After a system soft reset request is sent, the circuit reset is deasserted after at least 360 system clock cycles.
- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

The clock and reset generator (CRG) manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the CRG.

Figure 3-2 Functional block diagram of the CRG

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NOTE

XIN is the PLL input clock and is always connected to a 24 MHz crystal, whereas RTC_XIN is the RTC input clock and is always connected to a 32.768 kHz crystal.

3.2.3 Clock Distribution

The CRG configures, controls, and manages the internal PLLs and the input clocks from pins. It also generates the clocks required by each module. Figure 3-3 shows the clock distribution diagram.

NOTE

The APLL in gray can be configured by programming, the BPLL is powered down by default, and the configurations of other PLLs are fixed. If a module has multiple clock sources, the default clock source is specified.

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Figure 3-3 Clock distribution diagram

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3.2.4 PLL Configuration

The Hi3516A has four internal PLLs. Each PLL uses two configuration registers. See Table 3-2.

Table 3-2 Configuration registers corresponding to PLLs

PLL	Configuration Register 0	Configuration Register 1
APLL	PERI_CRG0	PERI_CRG1
BPLL	PERI_CRG2	PERI_CRG3
VPLL	PERI_CRG4	PERI_CRG5
EPLL	PERI_CRG8	PERI_CRG9

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-3.

Table 3-3 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	PLL working frequency. It must be greater than 600 MHz but less than or equal to 2.4 GHz.
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	None
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	None
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	None
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	None
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	None

NOTE

- fbdiv: integral frequency multiplier
- frac: decimal frequency multiplier
- refdiv: frequency divider of the reference clock
- pstdiv1: level-1 output frequency divider
- pstdiv2: level-2 output frequency divider

For details about the frequency multiplier and divider of each PLL, see Table 3-2.

The following uses APLL as an example. If APLL outputs the 600 MHz FOUTPOSTDIV clock to the CPU module, the configured values of the register are calculated as follows:

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- If postdiv2 is 2 and postdiv1 is 1, the value of FOUTVCO is 1200 MHz based on the following formula:

  FOUTOISTDIV = FOUTVCO/(pstdiv1 x pstdiv2)

- If refdiv is 1, fbdiv and frac can be calculated based on the following formula:

  FOUTVCO = FREF x (fbdiv + frac/2^24)/refdiv = 24 x (fbdiv + frac/2^24)/1 = 1200 MHz

  That is, fbdiv = 50 and frac = 000000

3.2.5 Frequency Configurations

Frequency Configurations of A7/DDR/Bus Clocks

Table 3-4 describes the frequency configurations of A7/DDR/bus clocks.

Table 3-4 Frequency configurations of A7/DDR/bus clocks

Signal	Configuration Register
cpu_sc_sel	You can control this signal by configuring PERI_CRG12 bit[8:7].
a7clk_loaden	You can control this signal by configuring PERI_CRG10 bit[17].
a7clk_skipcfg	You can control this signal by configuring PERI_CRG10 bit[16:12].
ddr_sc_sel	You can control this signal by configuring PERI_CRG12 bit[5:4].
bus_sc_sel	You can control this signal by configuring PERI_CRG12 bit[3:0].

Table 3-5 shows the mapping between system controller modes and clock states.

Table 3-5 Mapping between system controller modes and clock states

System Controller Mode	Enable State of the 46.875 kHz Clock	Enable State of the 24 MHz Crystal Oscillator	Enable State of the APLL	System Clock State
Normal	Enabled	Enabled	Enabled	The working clocks of the ARM subsystem are derived from the PLL.
Slow	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 24 MHz crystal oscillator.
Doze	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 46.875 kHz clock. The 46.875 kHz clock is generated by dividing the 24 MHz crystal oscillator.

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Frequency Configurations of Module Clocks

Table 3-6 describes the frequency configurations of VDP clocks.

Table 3-6 Frequency configurations of VDP clocks

Signal	Configuration Register
VDP clock configurations	
vdp_cksel	PERI_CRG13 bit[16]
vo_out_cksel	PERI_CRG13 bit[15:14]
hd_cksel	PERI_CRG13 bit[13:12]
dac_pctrl	PERI_CRG13 bit[3]
vohd_out_pctrl	PERI_CRG13 bit[2]
VI_MIPI clock configurations	
sensor_cksel	PERI_CRG11 bit[18:16]
vi_sc_sel	PERI_CRG11 bit[3:2]
phy_cmos_lat	PERI_CRG11 bit[7:6]
phy_hs_lat	PERI_CRG11 bit[5:4]
vi_pctrl	PERI_CRG11 bit[1]
Video encoding/decoding unit (VEDU)/Advanced video coding (AVC) clock configurations	
mda_sc_sel	PERI_CRG12 bit[19:18], PERI_CRG12 bit[13:12]
avcclk_loaden	PERI_CRG16 bit[21]
avcclk_skipcfg	PERI_CRG16 bit[20:16]
veduclk_loaden	PERI_CRG16 bit[9]
veduclk_skipcfg	PERI_CRG16 bit[8:4]
VPSS clock configurations	
mda_sc_sel	PERI_CRG12 bit[15:14] Note: The VPSS working clocks must be the same as the VI-MIPI working clock in online mode.
vpssclk_loaden	PERI_CRG18 bit[9]
vpssclk_skipcfg	PERI_CRG18 bit[8:4]
TDE clock configurations	
tdeclk_loaden	PERI_CRG22 bit[9]
tdeclk_skipcfg	PERI_CRG22 bit[8:4]

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Signal	Configuration Register
VGS clock configurations	
mda_sc_sel	PERI_CRG12 bit[17:16]
vgsclk_loaden	PERI_CRG23 bit[9]
vgsclk_skipcfg	PERI_CRG23 bit[8:4]
JPGE clock configurations	
jpgeclk_loaden	PERI_CRG24 bit[9]
tdeclk_skipcfg	PERI_CRG24 bit[8:4]
MDU clock configurations	
mduclk_loaden	PERI_CRG26 bit[9]
mduclk_skipcfg	PERI_CRG26 bit[8:4]
IVE clock configurations	
ive_cksel	PERI_CRG27 bit[2]
SFC clock configurations	
sfc_cksel	PERI_CRG48 bit[3:2]
sfc_nand_cksel	PERI_CRG48 bit[7:6]
Secure digital input/output (SDIO) clock configurations	
sdxc1_cksel	PERI_CRG49 bit[11:10]
sdxc0_cksel	PERI_CRG49 bit[3:2]
NFC clock configurations	
nfc_cksel	PERI_CRG52 bit[2]
PWM/UART clock configurations	
pwm_cksel	PERI_CRG14 bit[2]
uart_cksel	PERI_CRG57 bit[19]
GSF/GMAC clock configurations	
mac_speed	PERI_CRG59 bit[1]
port_select	PERI_CRG59 bit[0]
ext_fephy_cksel	PERI_CRG51 bit[6]
rmii_cksel	PERI_CRG51 bit[4]
AIO clock configurations	
ai0_cksel	PERI_CRG35 bit[3:2]

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Precautions

Take the following precautions when configuring clocks:

- By default, the A7 working clock is in crystal oscillator mode after power-on. That is, the crystal oscillator clock input by the XIN pin is selected.
- If the frequency of the PLL is changed, the PLL can output a stable clock 0.1 ms later. The frequency of the PLL can be changed only when the system runs in slow mode.
- If the PLL output clock is not stable, the system mode cannot be switched to PLL mode. You can view the PLL lock bit to check whether the PLL is locked. The status of the PLL lock bit can be obtained by reading PERI_CRG58 bit[3:0].

3.2.6 CRG Register Summary

Table 3-7 describes CRG registers.

Table 3-7 Summary of CRG registers (base address: 0x2003_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG0	APLL configuration register 0	3-11
0x0004	PERI_CRG1	APLL configuration register 1	3-12
0x0008	PERI_CRG2	BPLL configuration register 0	3-13
0x000C	PERI_CRG3	BPLL configuration register 1	3-14
0x0010	PERI_CRG4	VPLL configuration register 0	3-15
0x0014	PERI_CRG5	VPLL configuration register 1	3-16
0x0020	PERI_CRG8	EPLL configuration register 0	3-17
0x0024	PERI_CRG9	EPLL configuration register 1	3-18
0x0028	PERI_CRG10	A7 frequency mode and reset configuration register	3-19
0x002C	PERI_CRG11	VICAP&MIPI CTRL clock and reset configuration register	3-20
0x0030	PERI_CRG12	SoC clock selection register	3-22
0x0034	PERI_CRG13	VOU clock and reset control register	3-24
0x0038	PERI_CRG14	PWM clock and reset control register	3-25
0x0040	PERI_CRG16	VEDU clock and soft reset control register	3-26
0x0048	PERI_CRG18	VPSS clock and reset control register	3-28
0x0058	PERI_CRG22	TDE clock and soft reset control register	3-29
0x005C	PERI_CRG23	VGS clock and soft reset control register	3-30
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-31
0x0068	PERI_CRG26	MDU clock and soft reset control register	3-32

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Offset Address	Register	Description	Page
0x006C	PERI_CRG27	IVE clock and soft reset control register	3-33
0x007C	PERI_CRG31	SAR_ADC & cipher clock and soft reset control register	3-34
0x008C	PERI_CRG35	AIO clock and soft reset control register	3-34
0x00B8	PERI_CRG46	USB clock and soft reset control register	3-35
0x00C0	PERI_CRG48	SFC clock and soft reset control register	3-37
0x00C4	PERI_CRG49	SDIO0/SDIO1 clock and soft reset control register	3-37
0x00CC	PERI_CRG51	GSF/GMAC/FE PHY clock and soft reset control register	3-39
0x00D0	PERI_CRG52	NANDC clock and soft reset control register	3-40
0x00D8	PERI_CRG54	DMA/DDRTEST/eFUSE clock and soft reset control register	3-40
0x00E4	PERI_CRG57	Soft reset control register for other CRG interface modules	3-41
0x00E8	PERI_CRG58	CRG status register	3-43
0x00EC	PERI_CRG59	GMAC interface control register	3-44
0x0104	PERI_CRG65	PWM clock select register1	3-45
0x010C	PERI_CRG67	BPLL spread spectrum configuration register	3-45
0x0110	PERI_CRG68	VPLL spread spectrum configuration register	3-47
0x0118	PERI_CRG70	EPLL spread spectrum configuration register	3-48
0x012C	PERI_CRG75	Core high performance monitor (HPM) control register 1	3-49

3.2.7 Register Description

PERI_CRG0

PERI_CRG0 is APLL configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG0	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	apll_postdiv2			reserved	apll_postdiv1			apll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:28]	RW	apll_postdiv2	Level-2 output divider of the APLL.
[27]	RO	reserved	Reserved.
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL.
[23:0]	RW	apll_frac	Decimal divider of the APLL.

PERI_CRG1

PERI_CRG1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG1	0x0150_1032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					apll_bypass	apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	reserved		apll_refdiv						apll_fbdiv											
Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26]	RW	apll_bypass	APLL clock frequency division bypass. 0: not bypassed 1: bypassed

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[25]	RW	apll_dacpd	APLL test signal control. 0: normal operating mode 1: power-down mode
[24]	RW	apll_dsmpd	APLL decimal division control. 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	apll_pd	APLL power-down control. 0: normal operating mode 1: power-down mode
[22]	RW	apll_foutvcopd	APLL VCO output power-down control. 0: normal output clock 1: no output clock
[21]	RW	apll_postdivpd	APLL POSTDIV output power-down control. 0: normal clock output 1: no output clock
[20]	RW	apll_fout4phasepd	APLL FOUT output power-down control. 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved.
[17:12]	RW	apll_refdiv	Frequency divider of the APLL reference clock.
[11:0]	RW	apll_fbdiv	Integral frequency multiplier of the APLL.

PERI_CRG2

PERI_CRG2 is BPLL configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0008	PERI_CRG2	0x1300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	bpll_postdiv2			reserved	bpll_postdiv1			bpll_frac																							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved.
[30:28]	RW	bpll_postdiv2	Level-2 output divider of the BPLL.
[27]	RW	reserved	Reserved.
[26:24]	RW	bpll_postdiv1	Level-1 output divider of the BPLL.
[23:0]	RW	bpll_frac	Decimal divider of the BPLL.

PERI_CRG3

PERI_CRG3 is BPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x000C	PERI_CRG3	0x01F0_1036

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					bpll_bypass	bpll_dacpd	bpll_dsmpd	bpll_pd	bpll_foutvcopd	bpll_postdivpd	bpll_fout4phasepd	reserved				bpll_refdiv				bpll_fbdiv											
Reset	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26]	RW	bpll_bypass	BPLL clock frequency division bypass. 0: not bypassed 1: bypassed

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[25]	RW	bpll_dacpd	BPLL test signal control. 0: normal operating mode 1: power-down mode
[24]	RW	bpll_dsmpd	BPLL decimal division control. 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	bpll_pd	BPLL power-down control. 0: normal operating mode 1: power-down mode
[22]	RW	bpll_foutvcopd	BPLL VCO output power-down control. 0: normal output clock 1: no output clock
[21]	RW	bpll_postdivpd	BPLL POSTDIV output power-down control. 0: normal output clock 1: no output clock
[20]	RW	bpll_fout4phasepd	BPLL FOUT output power-down control. 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved.
[17:12]	RW	bpll_refdiv	Frequency divider of the BPLL reference clock.
[11:0]	RW	bpll_fbdiv	Integral frequency multiplier of the BPLL.

PERI_CRG4

PERI_CRG4 is VPLL configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG4	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll_postdiv2			reserved	vpll_postdiv1			vpll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved.
[30:28]	RW	vpll_postdiv2	Level-2 output divider of VPLL.
[27]	RW	reserved	Reserved.
[26:24]	RW	vpll_postdiv1	Level-1 output divider of VPLL.
[23:0]	RW	vpll_frac	Decimal divider of VPLL.

PERI_CRG5

PERI_CRG5 is VPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG5	0x0100_2063

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					vpll0_bypass	vpll0_dacpd	vpll0_dsmpd	vpll0_pd	vpll0_foutvcopd	vpll0_postdivpd	vpll0_fout4phasepd	reserved				vpll0_refdiv				vpll0_fbdiv											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.

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[26]	RW	vpll_bypass	VPLL clock frequency division bypass. 0: not bypassed 1: bypassed
[25]	RW	vpll_dacpd	VPLL test signal control. 0: normal operating mode 1: power-down mode
[24]	RW	vpll_dsmpd	VPLL decimal division control. 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	vpll_pd	VPLL power-down control. 0: normal operating mode 1: power-down mode
[22]	RW	vpll_foutvcopd	VPLL VCO output power-down control. 0: normal output clock 1: no output clock
[21]	RW	vpll_postdivpd	VPLL POSTDIV output power-down control. 0: normal output clock 1: no output clock
[20]	RW	vpll_fout4phasepd	VPLL FOUT output power-down control. 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved.
[17:12]	RW	vpll_refdiv	Frequency divider of the VPLL reference clock.
[11:0]	RW	vpll_fbdiv	Integral frequency multiplier of VPLL.

PERI_CRG8

PERI_CRG8 is EPLL configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG8	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	epll_postdiv2			reserved	epll_postdiv1			epll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved.
[30:28]	RW	epll_postdiv2	Level-2 output divider of the EPLL.
[27]	RW	reserved	Reserved.
[26:24]	RW	epll_postdiv1	Level-1 output divider of the EPLL.
[23:0]	RW	epll_frac	Decimal divider of the EPLL.

PERI_CRG9

PERI_CRG9 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG9	0x0100_307D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					epll_bypass	epll_dacpd	epll_dsmpd	epll_pd	epll_foutvcopd	epll_postdivpd	epll_fout4phasepd	reserved		epll_refdiv						epll_fbdiv											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26]	RW	epll_bypass	EPLL clock frequency division bypass. 0: not bypassed 1: bypassed

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[25]	RW	epll_dacpd	EPLL test signal control. 0: normal operating mode 1: power-down mode
[24]	RW	epll_dsmpd	EPLL decimal division control. 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	epll_pd	EPLL power-down control. 0: normal operating mode 1: power-down mode
[22]	RW	epll_foutvcopd	EPLL VCO output power-down control. 0: normal output clock 1: no output clock
[21]	RW	epll_postdivpd	EPLL POSTDIV output power-down control. 0: normal output clock 1: no output clock
[20]	RW	epll_fout4phasepd	EPLL FOUT output power-down control. 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved.
[17:12]	RW	epll_refdiv	Frequency divider of the EPLL reference clock.
[11:0]	RW	epll_fbdiv	Integral frequency multiplier of the EPLL.

PERI_CRG10

PERI_CRG10 is an A7 frequency mode and reset configuration register.

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Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved		cpuclk_loaden		cpuclk_skipcfg				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:18]	RO	reserved	Reserved.
[17]	RW	cpuclk_loaden	Skip configuration enable for the CPU clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[16:12]	RW	cpuclk_skipcfg	Skip configuration of the CPU clock. N: *N*-beat clocks are disabled every 32-beat CPU clocks. The following example assumes that the CPU source clock is 750 MHz. If a7clk_skipcfg is set to 00, the CPU works in full-speed mode; if a7clk_skipcfg is set to 01, the CPU works in speed-down mode. The actual working frequency is calculated as follows: 750 x 31/32 = 726.25 MHz This rule applies to other configurations. The default mode is full-speed mode.
[11:0]	RO	reserved	Reserved.

PERI_CRG11

PERI_CRG11 is a VICAP&MIPI CTRL clock and reset configuration register.

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Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											sensor_srst_req	sensor_cken	sensor_cksel			reserved		isp_cfg_srst_req	isp_core_srst_req	mipi_hrst_req	mipi_srst_req	vi_hrst_req	vi_srst_req	phy_cmos_lat		phy_hs_lat		vi_sc_sel		vi_pctrl	vi_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20]	RW	sensor_srst_req	Sensor soft reset request. 0: reset deasserted 1: reset
[19]	RW	sensor_cken	Sensor CLKOUT clock gating. 0: disabled 1: enabled
[18:16]	RW	sensor_cksel	Sensor output clock 000: 74.25 MHz 001: 37.125 MHz 010: 54 MHz 011: 27 MHz 1X0: 24 MHz 1X1: 25 MHz
[15:14]	RO	reserved	Reserved.
[13]	RW	isp_cfg_srst_req	ISP CFG soft reset request. 0: reset deasserted 1: reset
[12]	RW	isp_core_srst_req	ISP core soft reset request. 0: reset deasserted 1: reset
[11]	RO	reserved	Reserved.
[10]	RW	mipi_srst_req	MIPI Ctrl soft reset request. 0: reset deasserted 1: reset

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[9]	RW	vi_hrst_req	VI bus soft reset request. 0: reset deasserted 1: reset
[8]	RW	vi_srst_req	VI CH soft reset request. 0: reset deasserted 1: reset
[7:6]	RW	phy_cmos_lat	Interface clock latency in MIPI PHY CMOS mode. N: *N* steps are added based on the default value (500 ps per step).
[5:4]	RW	phy_hs_lat	Interface clock latency in MIPI PHY HS mode. N: *N* steps are added based on the default value (500 ps per step).
[3:2]	RW	vi_sc_sel	VI working clock select. 00: reserved 01: 250 MHz 10: 148.5 MHz 11: 99 MHz
[1]	RW	vi_pctrl	Phase of the VI interface clock. 0: positive phase clock 1: inverted clock
[0]	RW	vi_cken	VI CH clock gating. 0: disabled 1: enabled

PERI_CRG12

PERI_CRG12 is an SoC clock selection register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6	5 4	3 2 1 0
Name	reserved			mda_sc_sel		reserved	cpu_sc_sel	reserved	ddr_sc_sel	bus_sc_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0	0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.

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[19:12]	RW	mda_sc_sel	[19:18]: AVC source clock select. 00: 297 MHz 01: 250 MHz 10: 198 MHz 11: reserved [17:16]: VGS source clock select. 00: 300 MHz 01: 237 MHz 10: 200 MHz 11: reserved [15:14]: VPSS source clock select. 00: reserved 01: 250 MHz 10: 148.5 MHz 11: 99 MHz [13:12]: VEDU source clock select. 00: 297 MHz 01: 250 MHz 10: 198 MHz 11: reserved
[11:10]	RO	reserved	Reserved.
[9:8]	RW	cpu_sc_sel	CPU clock select. 00: APLL_FOUTPOSTDIV 01: 500 MHz 10: 400 MHz 11: BPLL_FOUTPOSTDIV
[7:6]	RO	reserved	Reserved.
[5:4]	RW	ddr_sc_sel	DDR clock select. 00: 297 MHz 01: reserved 10: 250 MHz 11: 198 MHz

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[3:0]	RW	bus_sc_sel	[3]: sysaxi clock select. 0: 198 MHz 1: 148.5 MHz [2]: mda1axi clock select. 0: 198 MHz 1: 250 MHz [1:0]: mda0axi clock select. 00: 237 MHz 01: 297 MHz 10: 200 MHz 11: 250 MHz

PERI_CRG13

PERI_CRG13 is a VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															vdp_cksel	vo_out_cksel		hd_cksel		dac_cken	vou_sd_cken	vou_hd_cken	vou_acken	vo_out_cken	vo_pcken	vo_ppc_cken	vo_cfg_cken	dac_pctrl	vohd_out_pctrl	reserved	vo_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RW	vdp_cksel	VDP working clock select. 0: 198 MHz 1: 99 MHz
[15:14]	RW	vo_out_cksel	Associated clock select for the VOU digital interface. 00: 148.5 MHz 01: 74.25 MHz 1X: 27 MHz
[13:12]	RW	hd_cksel	DHD frequency. 00: 148.5 MHz 01: 74.25 MHz 10: 13.5 MHz 11: 27 MHz

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[11]	RW	dac_cken	VOU DAC clock gating. 0: disabled 1: enabled
[10]	RW	vou_sd_cken	VOU SD DATE clock gating. 0: disabled 1: enabled
[9]	RW	vou_hd_cken	VOU HD clock gating. 0: disabled 1: enabled
[8]	RW	vou_acken	VOU AXI bus clock gating. 0: disabled 1: enabled
[7]	RW	vo_out_cken	VO_CLKOUT clock gating. 0: disabled 1: enabled
[6]	RW	vo_pcken	VO APB clock gating. 0: disabled 1: enabled
[5]	RW	vo_ppc_cken	VO PPC clock gating. 0: disabled 1: enabled
[4]	RW	vo_cfg_cken	VOU CFG clock gating (internally configured). 0: disabled 1: enabled
[3]	RW	dac_pctrl	VDAC clock phase. 0: positive phase clock 1: inverted clock
[2]	RW	vohd_out_pctrl	Phase of the output associated clock of the VOU digital interface. 0: positive phase clock 1: inverted clock
[1]	RO	reserved	Reserved.
[0]	RW	vo_srst_req	VOU soft reset request. 0: reset deasserted 1: reset

PERI_CRG14

PERI_CRG14 is a PWM clock and reset control register.

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Offset Address	Register Name	Total Reset Value
0x0038	PERI_CRG14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													pwm_cksel	pwm_cken	pwm_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	pwm_cksel0	PWM clock select by working with PERI_CRG65 bit[10]. [pwm_cksel1, pwm_cksel0] 00:3M 01:50M 1x:24M
[1]	RW	pwm_cken	PWM clock gating. 0: disabled 1: enabled
[0]	RW	pwm_srst_req	PWM soft reset request. 0: reset deasserted 1: reset

PERI_CRG16

PERI_CRG16 is a VEDU clock and reset control register.

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Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_3003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										avcclk_loaden	avcclk_skipcfg					reserved		avc_cken	avc_srst_req	reserved		veudclk_loaden	veduclk_skipcfg					reserved		vedu_cken	vedu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	avcclk_loaden	Skip configuration enable for the AVC clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[20:16]	RW	avcclk_skipcfg	Skip configuration of the AVC clock. N: *N*-beat clocks are disabled every 32-beat AVC clocks. The following example assumes that the AVC working source clock is 250 MHz. If avcclk_skipcfg is set to 00, the AVC works in full-speed mode; if avcclk_skipcfg is set to 01, the AVC works in speed-down mode. The actual working frequency is calculated as follows: 250 x 31/32 = 242 MHz This rule applies to other configurations.
[15:14]	RO	reserved	Reserved.
[13]	RW	avc_cken	AVC clock gating. 0: disabled 1: enabled
[12]	RW	avc_srst_req	AVC soft reset request. 0: reset deasserted. 1: reset
[11:10]	RO	reserved	Reserved.

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[9]	RW	veudclk_loaden	Skip configuration enable for the VEDU clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	veduclk_skipcfg	Skip configuration of the VEDU clock. N: *N*-beat clocks are disabled every 32-beat VEDU clocks. The following example assumes that the VEDU working source clock is 250 MHz. If veduclk_skipcfg is set to 00, the VEDU works in full-speed mode; if veduclk_skipcfg is set to 01, the VEDU works in speed-down mode. The actual working frequency is calculated as follows: 250 x 31/32 = 242 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	vedu_cken	VEDU clock gating. 0: disabled 1: enabled
[0]	RW	vedu_srst_req	VEDU soft reset request. 0: reset deasserted. 1: reset

PERI_CRG18

PERI_CRG18 is a VPSS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vpsclk_loaden	vpsclk_skipcfg					reserved		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9]	RW	vpsclk_loaden	Skip configuration enable for the VPSS clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	vpsclk_skipcfg	Skip configuration of the VPSS clock. N: *N*-beat clocks are disabled every 32-beat VPSS clocks. The following example assumes that the VPSS working source clock is 250 MHz. If vpssclk_skipcfg is set to 00, the VPSS works in full-speed mode; if vpssclk_skipcfg is set to 01, the VPSS works in speed-down mode. The actual working frequency is calculated as follows: 250 x 31/32 = 242 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	vps_cken	VPSS clock gating. 0: disabled 1: enabled
[0]	RW	vps_srst_req	VPSS soft reset request. 0: reset deasserted. 1: reset

PERI_CRG22

PERI_CRG22 is a TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tdeclk_loaden	tdeclk_skipcfg					reserved			tde_cken	tde_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9]	RW	tdeclk_loaden	Skip configuration enable for the TDE clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	tdeclk_skipcfg	Skip configuration of the TDE clock. N: *N*-beat clocks are disabled every 32-beat TDE clocks. The following example assumes that the TDE working source clock is 150 MHz. If tdeclk_skipcfg is set to 00, the TDE works in full-speed mode; if tdeclk_skipcfg is set to 01, the TDE works in speed-down mode. The actual working frequency is calculated as follows: 150 x 31/32 = 145 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	tde_cken	TDE clock gating. 0: disabled 1: enabled
[0]	RW	tde_srst_req	TDE soft reset request. 0: reset deasserted. 1: reset

PERI_CRG23

PERI_CRG23 is a VGS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_CRG23	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vgsclk_loaden	vgsclk_skipcfg					reserved		vgs_cken	vgs_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9]	RW	vgsclk_loaden	Skip configuration enable for the VGS clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	vgsclk_skipcfg	Skip configuration of the VGS clock. N: *N*-beat clocks are disabled every 32-beat VGS clocks. The following example assumes that the VGS working source clock is 237 MHz. If vgsclk_skipcfg is set to 00, the VGS works in full-speed mode; if vgsclk_skipcfg is set to 01, the VGS works in speed-down mode. The actual working frequency is calculated as follows: 237 x 31/32 = 229 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	vgs_cken	VGS clock gating. 0: disabled 1: enabled
[0]	RW	vgs_srst_req	VGS soft reset request. 0: reset deasserted. 1: reset

PERI_CRG24

PERI_CRG24 is a JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						jpgeclk_loaden	jpgeclk_skipcfg					reserved		jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9]	RW	jpgeclk_loaden	Skip configuration enable for the JPGE clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	jpgeclk_skipcfg	Skip configuration of the JPGE clock. N: *N*-beat clocks are disabled every 32-beat JPGE clocks. The following example assumes that the JPGE working source clock is 200 MHz. If jpgeclk_skipcfg is set to 00, the JPGE works in full-speed mode; if jpgeclk_skipcfg is set to 01, the JPGE works in speed-down mode. The actual working frequency is calculated as follows: 200 x 31/32 = 194 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	jpge_cken	JPGE clock gating. 0: disabled 1: enabled
[0]	RW	jpge_srst_req	JPGE soft reset request. 0: reset deasserted. 1: reset

PERI_CRG26

PERI_CRG26 is an MDU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						mduclk_loaden	mduclk_skipcfg					reserved		mdu_cken	mdu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9]	RW	mduclk_loaden	Skip configuration enable for the MDU clock. To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	mduclk_skipcfg	Skip configuration of the MDU clock. N: *N*-beat clocks are disabled every 32-beat MDU clocks. The following example assumes that the MDU working source clock is 150 MHz. If mduclk_skipcfg is set to 00, the MDU works in full-speed mode; if mduclk_skipcfg is set to 01, the MDU works in speed-down mode. The actual working frequency is calculated as follows: 150 x 31/32 = 145 MHz This rule applies to other configurations.
[3:2]	RO	reserved	Reserved.
[1]	RW	mdu_cken	MDU clock gating. 0: disabled 1: enabled
[0]	RW	mdu_srst_req	MDU soft reset request. 0: reset deasserted. 1: reset

PERI_CRG27

PERI_CRG27 is an IVE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												reserved	ive_cksel	ive_cken	ive_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	reserved	Reserved.

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[2]	RW	ive_cksel	IVE clock select. 0: 300 MHz 1: 200 MHz
[1]	RW	ive_cken	IVE clock gating. 0: disabled 1: enabled
[0]	RW	ive_srst_req	IVE soft reset request. 0: reset deasserted 1: reset

PERI_CRG31

PERI_CRG31 is an SAR_ADC & cipher clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													sar_adc_srst_req	cipher_cken	cipher_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	sar_adc_srst_req	SAR ADC soft reset request. 0: reset deasserted 1: reset
[1]	RW	cipher_cken	Cipher clock gating. 0: disabled 1: enabled
[0]	RW	cipher_srst_req	Cipher soft reset request. 0: reset deasserted 1: reset

PERI_CRG35

PERI_CRG35 is an AIO clock and reset control register.

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Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												aio_cksel		aiao_cken	aio_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:2]	RW	aio_cksel	AIO MCLK PLL clock source select. 00: 500 MHz 01: BPLL_FOUTVCO 1x: VPLL_FOUTVCO
[1]	RW	aiao_cken	AIO clock gating. 0: disabled 1: enabled
[0]	RW	aio_srst_req	AIO soft reset request. 0: reset deasserted. 1: reset

PERI_CRG46

PERI_CRG46 is a USB2.0 clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							usb_device_ctrl_srst_req	usb_cken	reserved	usb_ctrl_utmi0_req	usb_ctrl_hub_req	reserved	usbphy_port0_treq	usbphy_req	usb_ahb_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	usb_device_ctrl_srst_req	USB2.0 device controller soft reset request. 0: reset deasserted 1: reset
[7]	RW	usb_cken	Clock gating of the USB2.0 PHY reference clock. 0: disabled 1: enabled
[6]	RO	reserved	Reserved.
[5]	RW	usb_ctrl_utmi0_req	USB2.0 controller port 0 soft reset request. 0: reset deasserted 1: reset
[4]	RW	usb_ctrl_hub_req	USB2.0 controller hub soft reset request. 0: reset deasserted 1: reset
[3]	RO	reserved	Reserved.
[2]	RW	usbphy_port0_treq	USB2.0 PHY port 0 soft reset request. 0: reset deasserted 1: reset
[1]	RW	usbphy_req	USB2.0 PHY soft reset request. 0: reset deasserted 1: reset
[0]	RW	usb_ahb_srst_req	USB2.0 controller bus soft reset request. 0: reset deasserted 1: reset

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PERI_CRG48

PERI_CRG48 is an SFC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0022

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sfc_nand_cksel		sfc_nand_cken	sfc_nand_srst_req		sfc_cksel		sfc_cken	sfc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:6]	RW	sfc_nand_cksel	SFC NAND 2X clock source select. 00: 24 MHz 01: 75 MHz 1X: 125 MHz
[5]	RW	sfc_nand_cken	SFC NAND clock gating. 0: disabled 1: enabled
[4]	RW	sfc_nand_srst_req	SFC NAND soft reset request. 0: reset deasserted 1: reset
[3:2]	RW	sfc_cksel	SFC NOR 2X clock source select. 00: 24 MHz 01: 75 MHz 1X: 125 MHz
[1]	RW	sfc_cken	SFC NOR clock gating. 0: disabled 1: enabled
[0]	RW	sfc_srst_req	SFC NOR soft reset request. 0: reset deasserted 1: reset

PERI_CRG49

PERI_CRG49 is an SDIO0/SDIO1 clock and soft reset control register.

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Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0000_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sdxc1_cksel		sdxc1_cken	sdxc1_srst_req	reserved				sdxc0_cksel		sdxc0_cken	sdxc0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:10]	RW	sdio1_cksel	SDIO1 working clock select. 00: 50 MHz 01: 100 MHz 10: 25 MHz 11: 75 MHz
[9]	RW	sdio1_cken	SDIO1 clock gating. 0: disabled 1: enabled
[8]	RW	sdio1_srst_req	SDIO1 soft reset request. 0: reset deasserted 1: reset
[7:4]	RO	reserved	Reserved.
[3:2]	RW	sdio0_cksel	SDIO0 working clock select. 00: 50 MHz 01: 100 MHz 10: 25 MHz 11: 75 MHz
[1]	RW	sdio0_cken	SDIO0 clock gating. 0: disabled 1: enabled
[0]	RW	sdio0_srst_req	SDIO0 soft reset request. 0: reset deasserted 1: reset

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PERI_CRG51

PERI_CRG51 is a GSF/GMAC/FE PHY clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ext_fephy_cksel	reserved	rmii_cksel	gmac_if_cken	gmac_if_srst_req	gsf_cken	gsf_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6]	RW	ext_fephy_cksel	External FE PHY clock select. 0: 50 MHz 1: 25 MHz
[5]	RO	reserved	Reserved.
[4]	RW	rmii_cksel	RMII clock select. 0: CRG clock 1: PAD input Note: In MII mode, set this bit to 1, indicating that MII_TX_CLK is used as the input clock. In RGMII/RMII mode, set this bit to 0, indicating that RGMII_TX_CLK is used as the output clock.
[3]	RW	gmac_if_cken	GMAC clock gating. 0: disabled 1: enabled
[2]	RW	gmac_if_srst_req	GMAC soft reset request. 0: reset deasserted 1: reset
[1]	RW	gsf_cken	GSF clock gating. 0: disabled 1: enabled
[0]	RW	gsf_srst_req	GSF soft reset request. 0: reset deasserted 1: reset

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PERI_CRG52

PERI_CRG52 is a NANDC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D0	PERI_CRG52	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													nfc_cksel	nfc_cken	nfc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	nfc_cksel	NFC clock source select. 0: 24 MHz clock 1: 198 MHz clock
[1]	RW	nfc_cken	NFC clock gating. 0: disabled 1: enabled
[0]	RW	nfc_srst_req	NFC soft reset request. 0: reset deasserted 1: reset

PERI_CRG54

PERI_CRG54 is a DMA/DDRTEST/eFUSE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dma_cken	dma_srst_req	ddrtest_cken	ddrtest_srst_req	efuse_cken	efuse_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.

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[5]	RW	dma_cken	DMA clock gating. 0: disabled 1: enabled
[4]	RW	dma_srst_req	DMA soft reset request. 0: reset deasserted 1: reset
[3]	RW	ddrtest_cken	DDRTEST clock gating. 0: disabled 1: enabled
[2]	RW	ddrtest_srst_req	DDRTEST soft reset request. 0: reset deasserted 1: reset
[1]	RW	efuse_cken	eFUSE clock gating. 0: disabled 1: enabled
[0]	RW	efuse_srst_req	eFUSE soft reset request. 0: reset deasserted 1: reset

PERI_CRG57

PERI_CRG57 is a soft reset control register for other CRG interface modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x000F_F001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												uart_cksel	uart3_cken	uart2_cken	uart1_cken	uart0_cken	ssp1_cken	ssp0_cken	ir_cken	reserved	uart3_srst_req	uart2_srst_req	uart1_srst_req	uart0_srst_req	ssp1_srst_req	ssp0_srst_req	ir_srst_req	reserved	tcap_srst_req	i2c_srst_req	test_clk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RW	uart_cksel	UART clock select. 0: APB clock 1: 6 MHz clock

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[18]	RW	uart3_cken	UART3 clock gating. 0: disabled 1: enabled
[17]	RW	uart2_cken	UART2 clock gating. 0: disabled 1: enabled
[16]	RW	uart1_cken	UART1 clock gating. 0: disabled 1: enabled
[15]	RW	uart0_cken	UART0 clock gating. 0: disabled 1: enabled
[14]	RW	ssp1_cken	SSP1 clock gating. 0: disabled 1: enabled
[13]	RW	ssp0_cken	SSP0 clock gating. 0: disabled 1: enabled
[12]	RW	ir_cken	IR clock gating. 0: disabled 1: enabled
[11]	RO	reserved	Reserved.
[10]	RW	uart3_srst_req	UART3 soft reset request. 0: reset deasserted 1: reset
[9]	RW	uart2_srst_req	UART2 soft reset request. 0: reset deasserted 1: reset
[8]	RW	uart1_srst_req	UART1 soft reset request. 0: reset deasserted 1: reset
[7]	RW	uart0_srst_req	UART0 soft reset request. 0: reset deasserted 1: reset
[6]	RW	ssp1_srst_req	SSP1 soft reset request. 0: reset deasserted 1: reset

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[5]	RW	ssp0_srst_req	SSP0 soft reset request. 0: reset deasserted 1: reset
[4]	RW	ir_srst_req	IR soft reset request. 0: reset deasserted 1: reset
[3]	RO	reserved	Reserved.
[2]	RW	tcap_srst_req	t_cap soft reset request. 0: reset deasserted 1: reset
[1]	RW	i2c_srst_req	I^2C soft reset request. 0: reset deasserted 1: reset
[0]	RW	test_clk_en	Test clock enable. 0: All test clocks are disabled. 1: All test clocks are enabled.

PERI_CRG58

PERI_CRG58 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												epll_lock	vpll_lock	bpll_lock	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	epll_lock	EPLL lock status. 0: unlocked 1: locked
[2]	RO	vpll_lock	VPLL lock status. 0: unlocked 1: locked

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[1]	RO	bpll_lock	BPLL lock status. 0: unlocked 1: locked
[0]	RO	apll_lock	APLL lock status. 0: unlocked 1: locked

PERI_CRG59

PERI_CRG59 is a GMAC interface control register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_CRG59	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							loopback_mode	phy_select			duplex_mode	tx_config	link_status	mac_speed	port_select
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	loopback_mode	Loopback mode enable. 0: disabled 1: enabled
[7:5]	RW	phy_select	PHY interface mode. 000: GMII/MII mode 001: RGMII mode 100: RMII mode Other values: reserved
[4]	RW	duplex_mode	PHY duplex mode. 0: half-duplex mode 1: full-duplex mode
[3]	RW	tx_config	TX configuration enable. 0: disabled 1: enabled

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[2]	RW	link_status	PHY link status. 0: link down 1: link up
[1]	RW	mac_speed	10/100 Mbit/s mode. 0: 10 Mbit/s 1: 100 Mbit/s
[0]	RW	port_select	Gigabit mode select. 0: 1000 Mbit/s 1: 10/100 Mbit/s

PERI_CRG65

PERI_CRG65 is PWM clock select register1.

Offset Address	Register Name	Total Reset Value
0x0104	PERI_CRG65	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pwm_cksel0	reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	pwm_cksel0	PWM clock select by working with PERI_CRG14 bit[2]. For details, see the description of PERI_CRG14 bit[2].
[9:0]	RW	reserved	Reserved.

PERI_CRG67

PERI_CRG67 is a BPLL spread spectrum configuration register.

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Offset Address	Register Name	Total Reset Value
0x010C	PERI_CRG67	0x0000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				bpll_ssmod_ctrl											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:0]	RW	bpll_ssmod_ctrl	ssmod divval[11:8]: SSMOD divval control. ssmod spread[6:4]: SSMOD spread control. 000: 0 001: 0.049% 010: 0.098% 011: 0.195% 100: 0.391% 101: 0.781% 110: 1.563% 111: 3.125% ssmod downspread[3]: SSMOD downspread control. 0: central spread spectrum 1: down spread spectrum ssmod_disable[2]: SSMOD disable control. 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control. 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating. 0: disabled (default) 1: enabled

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PERI_CRG68

PERI_CRG68 is a VPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0110	PERI_CRG68	0x0000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vpll_ssmod_ctrl											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	vpll_ssmod_ctrl	ssmod divval[11:8]: SSMOD divval control. ssmod spread[6:4]: SSMOD spread control. 000: 0 001: 0.049% 010: 0.098% 011: 0.195% 100: 0.391% 101: 0.781% 110: 1.563% 111: 3.125% ssmod downspread[3]: SSMOD downspread control. 0: central spread spectrum 1: down spread spectrum ssmod_disable[2]: SSMOD disable control. 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control. 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating. 0: disabled 1: enabled

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PERI_CRG70

PERI_CRG70 is an EPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0118	PERI_CRG70	0x0000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				epll_ssmod_ctrl											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	epll_ssmod_ctrl	ssmod divval[11:8]: SSMOD divval control. ssmod spread[6:4]: SSMOD spread control. 000: 0 001: 0.049% 010: 0.098% 011: 0.195% 100: 0.391% 101: 0.781% 110: 1.563% 111: 3.125% ssmod downspread[3]: SSMOD downspread control. 0: central spread spectrum 1: down spread spectrum ssmod_disable[2]: SSMOD disable control. 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control. 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating. 0: disabled (default) 1: enabled

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PERI_CRG75

PERI_CRG75 is core HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x012C	PERI_CRG75	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_srst_req	core_hpm_monitor_en	core_hpm_bypass	core_hpm_en	reserved				core_hpm_offset								reserved		core_hpm_shift		reserved				core_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27]	RW	core_hpm_srst_req	Core HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	core_hpm_monitor_en	Core HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	core_hpm_bypass	Core HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	core_hpm_en	Core HPM measurement enable. 0: The value is retained 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RW	reserved	Reserved.
[21:12]	RW	core_hpm_offset	Core HPM offset.
[11:10]	RW	reserved	Reserved.
[9:8]	RW	core_hpm_shift	Core HPM shift.
[7:6]	RW	reserved	Reserved.
[5:0]	RW	core_hpm_div	Core HPM clock divider. N: frequency divided by *N*

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3.3 Processor Subsystem

The Hi3516A uses the ARM Cortex-A7MPCore single-core processor. This processor has the following features:

- 600 MHz dominant working frequency
- 32 KB I-cache and 32 KB D-cache for the L1 cache
- Integrated 128 KB 8-way set-associative L2 cache. The L2 cache and processor have the same frequency. The cache line is fixed at 64 bytes. The L2 cache is based on the physical address and physical tag and supports the pseudo random cache replacement policy.
- 128-bit ACE bus interface that is compatible with the AXI interface, and asynchronous system bus and processor (including L2)
- Integrated generic interrupt controller (GIC), which supports 96 interrupt sources (including 64 external interrupts)
- Single-thread, out-of-order, dual-issue structure that supports 1.9 DMIPs/MHz
- 8-stage sequential pipelines
- Integrated memory management unit (MMU)
- Compatibility with multiple operating systems such as Vxworks and Linux
- Branch prediction with up to 95% precision
- JTAG debugging interface
- Integrated NEON with the floating-point unit (FPU) coprocessor

NOTE

For details about the principles of the lockdown function in C format, see the *ARM Architecture Reference Manual*.

3.4 Interrupt System

The Hi3516A has an integrated generic interrupt controller (GIC) of Cortex-A7 and supports a maximum of 96 interrupt sources. Table 3-8 describes the A7 interrupt sources.

Table 3-8 A7 interrupt sources

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
0–31	For A7 internal use	64	A7_PMU_INT0
32	COMMTX[0]	65	VDP
33	COMMRX[0]	66	MIPI
34	Watchdog	67	VICAP
35	Timer01	68	VPSS
36	Timer23	69	TDE
37	DMAC	70	VGS
38	Reserved	71	AIO

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Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
39	RTC	72	AVC (264)
40	UART0	73	JPGE
41	UART1	74	Reserved
42	UART2	75	VEDU (265)
43	UART3	76	MD
44	SSP0	77	IVE
45	SSP1	78	Reserved
46	I2C	79	GPIO0
47	IR	80	GPIO1
48	SAR_ADC	81	GPIO2/ GPIO15
49	SFC_NOR	82	GPIO3/ GPIO14
50	NFC	83	GPIO4/ GPIO13
51	SDIO0	84	GPIO5/ GPIO12
52	SDIO1	85	GPIO6/ GPIO11
53	USB_EHCI	86	GPIO7/ GPIO10
54	USB_OHCI	87	GPIO8/ GPIO9
55	USB_DEV	88	tem_cap_int
56	SFC_NAND	89	I2C1
57	GSF	90	I2C2
58	Cipher	91	Reserved
59	Reserved	92	Reserved
60	Software int	93	Reserved
61	Reserved	94	Reserved
62	Reserved	95	Reserved
63	Reserved		

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3.5 System Controller

3.5.1 Overview

The system controller controls the operating mode from several aspects. To be specific, it controls the operating mode of the system, monitors the system status, manages the key functions of the system, and configures some functions of peripherals.

3.5.2 Features

The system controller has the following features:

- Controls and monitors the operating mode of the system.
- Controls the system clock and queries its status.
- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.5.3 Function Description

Controlling the System Operating Mode

The system can work in any of the following modes:

- Normal mode

  The system typically works in normal mode. In this mode, the system is driven by the output clock of the on-chip PLL, and all modules work properly.
- Slow mode

  The slow mode is a low-speed mode. In this mode, the system is driven by the external crystal oscillator clock. Only part of on-chip peripherals (such as the system controller, timer, NANDC, and SFC) work properly. Modules (such as the DDRC) that require high-speed clock cannot work under the crystal oscillator clock.
- Doze mode

  The doze mode is also a slow-speed mode, but its speed is lower than the speed of the slow mode. Only a few on-chip peripherals can work in doze mode. In this mode, the system is driven by a 46.875 kHz low-frequency clock. This clock is generated by dividing the external crystal oscillator. Except the CPU and a few modules (such as the system controller, timer, and IR), most on-chip peripherals and the memory interface cannot work in this mode.

The system controller provides a mode switching mechanism to switch the system clock source. The mode is switched by configuring three bits of the mode control register SC_CTRL [modectrl]. These bits define the operating mode to which the system is switched.

- 000: reserved
- 001: doze mode
- 010: slow mode
- 100: normal mode
- Other values: reserved

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When the required system operating mode is specified by configuring the system mode control register, the system operating mode is switched to the target mode. In this case, no software intervention or command intervention is required.

The current system status can be queried by reading SC_CTRL [modestatus]. SC_CTRL [modestatus] shows not only the preceding three main modes (normal, slow, and doze modes), but also the following intermediate status between the main modes: SWfromPLL, SWtoPLL, PLLCTL, SWfromXTAL, SWtoXTAL, and XTALCTL.

NOTE

The normal, slow, and doze modes can be switched directly. For example, if the system is in normal mode, you can switch the system to doze mode by setting ***SC_CTRL*** [modectrl] to 001. The system mode is switched to SWfromPLL, slow, and then SWfromXTAL modes before being switched to the doze mode.

Figure 3-4 shows the process of switching the system mode.

Figure 3-4 Process of switching the system mode

The operations involved in mode switching are as follows:

- When the most significant bit (MSB) of SC_CTRL [modectrl] is set to 0, the system exits the normal mode and is switched to the slow mode.
- Before being switched from the normal mode to the slow mode, the system is switched to the SWfromPLL status. This indicates that the system clock source is switched from

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the PLL to the crystal oscillator. After the clock switching is done, the system enters the slow mode.

- After power-on reset, the system is in slow mode. When the MSB of SC_CTRL[modectrl] is set to 1, the system enters the normal mode. During the switching to normal mode, the system is switched to the PLLCTL status to enable the ARMPLL. After a fixed wait time (the wait time depends on SC_XTALCTRL[plltime]), the system enters the SWtoPLL status to switch the clock source. After the switching is done, the system enters the normal mode.
- When the upper two bits of SC_CTRL [modectrl] are set to 0, the system is switched to the doze mode. In this case, the system is first switched to the SWfromXTAL status. This indicates that the system clock source is switched from the crystal oscillator clock to a 46.875 kHz low-frequency clock. The 46.875 kHz clock is generated by dividing the crystal oscillator clock. After the clock switching is done, the system enters the doze mode.
- When either of the upper two bits of SC_CTRL [modectrl] is set to 1, the system is switched to the slow mode. During the switching to the slow mode, the system is switched to the XTALCTL status to initialize the clock module. After a fixed wait time (the wait time depends on SC_XTALCTRL[xtaltime]), the system enters the SWtoXTAL status to switch the clock source. After the switching is done, the system enters the slow mode.

For details about the mapping between the status of the system controller and system clocks, see Table 3-5.

Soft Reset

The system controller can soft-reset the entire chip or some modules.

After the global soft reset register SC_SYSRST is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3516A.

System Address Remap Control

For details, see section 1.3 "Boot Modes."

Write Protection for Key Registers

To avoid the entire system being severely affected by the misoperation on the system controller, the system controller provides write protection for key configuration registers. The key configuration registers are as follows:

- Mode switching control register: SC_CTRL
- Control register for system global soft reset: SC_SYSRST
- PLL control register: SC_PLLCTRL
- PLL frequency control register: SC_PLLCTRL

Before writing to these key registers, you must disable the write protection function by configuring SC_LOCKEN. After write operations, you need to enable the write protection function by configuring SC_LOCKEN, ensuring that these key registers are not mistakenly written by the software.

NOTE

By default, write protection is not enabled for key registers after reset. It is recommended that you enable write protection by configuring SC_LOCKEN when the system starts.

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System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SCSYSID3, SCSYSID2, SCSYSID1, and SCSYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0x3516_A100, is obtained. Figure 3-5 shows the bit allocation of chip ID registers.

Figure 3-5 Bit allocation of chip ID registers

3.5.4 System Controller Registers

3.5.4.1 Register Summary

Table 3-9 describes system controller registers.

Table 3-9 Summary of system controller registers (base address: 0x2005_0000)

Offset Address	Register	Description	Page
0x000	SC_CTRL	System control register	3-56
0x004	SC_SYSRST	System soft reset register	3-58
0x008	SC_IMCTRL	Interrupt mode control register	3-59
0x00C	SC_IMSTAT	Interrupt mode status register	3-60
0x010	SC_XTALCTRL	Crystal oscillator control register	3-61
0x014	SC_PLLCTRL	PLL control register	3-62
0x001C	SOLFINT	Software interrupt register	3-64
0x0020	SOLFTYPE	Software interrupt vector register	3-64
0x0044	SC_LOCKEN	Key register lock register	3-65
0x008C	SYSSTAT	System status register	3-65
0x0090	DDRT0	DDR training register 0	3-67
0x0094	DDRT1	DDR training register 1	3-67
0x0098	DDRT2	DDR training register 2	3-68
0x009C	DDRT3	DDR training register 3	3-68

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Offset Address	Register	Description	Page
0x00A0	DDRT4	DDR training register 4	3-69
0x00A4	DDRT5	DDR training register 5	3-69
0x00A8	DDRT6	DDR training register 6	3-70
0x00AC	DDRT7	DDR training register 7	3-70
0x0130	SYSBOOT0	System boot register 0	3-71
0x0134	SYSBOOT1	System boot register 1	3-71
0x0138	SYSBOOT2	System boot register 2	3-71
0x013C	SYSBOOT3	System boot register 3	3-72
0x0140	SYSBOOT4	System boot register 4	3-72
0x0144	SYSBOOT5	System boot register 5	3-72
0x0148	SYSBOOT6	System boot register 6	3-73
0x014C	SYSBOOT7	System boot register 7	3-73
0x0150	SYSBOOT8	System boot register 8	3-73
0x0154	SYSBOOT9	System boot register 9	3-74
0x0158	SYSBOOT10	System boot register 10	3-74
0x015C	SYSBOOT11	System boot register 11	3-74
0xEE0	SCSYSID0	Chip ID register 0	3-75
0xEE4	SCSYSID1	Chip ID register 1	3-75
0xEE8	SCSYSID2	Chip ID register 2	3-75
0xEEC	SCSYSID3	Chip ID register 3	3-76

3.5.4.2 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations to be performed by the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

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Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0212

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									timeren3ov	reserved	timeren2ov	reserved	timeren1ov	reserved	timeren0ov	reserved	reserved					remapstat	remapclear	reserved	modestatus				modectrl		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22]	RW	timeren3ov	Timer 3 count clock select. 0: 3 MHz clock 1: bus clock
[21]	RO	reserved	Reserved.
[20]	RW	timeren2ov	Timer 2 count clock select. 0: 3 MHz clock 1: bus clock
[19]	RW	reserved	Reserved.
[18]	RW	timeren1ov	Timer 1 count clock select. 0: 3 MHz clock 1: bus clock
[17]	RW	reserved	Reserved.
[16]	RW	timeren0ov	Timer 0 count clock select. 0: 3 MHz clock 1: bus clock
[15]	RW	reserved	Reserved.
[14:10]	RO	reserved	Reserved. Reading this field returns 0, and writing to this field has no effect.
[9]	RO	remapstat	Address remap status. 0: The address is not remapped. 1: The address is remapped. The BOOTROM, NANDC CS 0, or SFC CS 1 is remapped to address 0.

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[8]	RW	remapclear	Address remap clear. 0: The remap status is retained. 1: The remap status is cleared. For details about the address mappings before and after remapping is cleared, see Table 1-2 "Address space mapping" in chapter 1 "Product Description."
[7]	RO	reserved	Reserved. Reading this field returns 0, and writing to this field has no effect.
[6:3]	RW	modestatus	Mode status. Reading this field returns the current operating mode of the system. 0x0: reserved 0x1: doze 0x2: slow 0x3: XTAL CTL 0x4: normal 0x6: PLL CTL 0x9: SW from XTAL 0xA: SW from PLL 0xB: SW to XTAL 0xE: SW to PLL Other values: reserved
[2:0]	RW	modectrl	Mode control. This field defines the operating mode to which the system controller is switched. 001: doze 010: slow 100: normal Other values: reserved

SC_SYSRST

SC_SYSRST is a system soft reset register. When a value is written to this register, the system controller sends a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

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Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRST	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	Writing any value to this register soft-resets the system.

SC_IMCTRL

SC_IMCTRL is an interrupt mode control register. It is used to control the system mode when an interrupt is generated.

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Offset Address	Register Name	Total Reset Value
0x008	SC_IMCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								inmdtype	reserved			itmdctrl			itmden
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved. Reading this field returns 0x000000, and writing to this field has no effect.
[7]	RW	inmdtype	Type of the interrupt for triggering the interrupt mode of the system. 0: FIQ interrupt only 1: FIQ interrupt and IRQ interrupt
[6:4]	RO	reserved	Reserved.
[3:1]	RW	itmdctrl	Operating mode of the system with the lowest speed in interrupt mode. The value obtained after the values of this register and SC_CTRL[modectrl] are ORed indicates the operating mode of the system after an interrupt is generated. The definition of this field is as follows: 000: sleep 001: doze 01X: slow 1XX: normal
[0]	RW	itmden	Interrupt mode enable. 0: disabled 1: enabled. When an interrupt is generated, the system enters the interrupt mode.

SC_IMSTAT

SC_IMSTAT is an interrupt mode control register. It is used to check whether the system is in interrupt mode. The system can be forcibly set to the interrupt mode by configuring this register.

CAUTION

When the interrupt service routine (ISR) ends, the interrupt mode must be manually cleared.

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Offset Address	Register Name	Total Reset Value
0x00C	SC_IMSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															itmdstat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved. Reading this field returns 0x00000000, and writing to this field has no effect.
[0]	RW	itmdstat	Interrupt mode status. The bit is used by software for controlling whether the system enters the interrupt mode. When the register is read: 0: The system is not in interrupt mode. 1: The system is in interrupt mode. When the register is written: 0: Software does not control whether the system enters the interrupt mode. 1: Software controls whether the system enters the interrupt mode.

SC_XTALCTRL

SC_XTALCTRL is a crystal oscillator control register. It is used to specify the stable wait time after the clock module is initialized. The stable wait time is the period for switching the system from the XTAL CTL mode to the SW-to-XTAL mode.

Offset Address	Register Name	Total Reset Value
0x010	SC_XTALCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												xtaltime																	reserved	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved. Reading this field returns 0x0000, and writing to this field has no effect.

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[18:3]	RW	xtaltime	Wait time for crystal oscillator switching. The value of this field is used to specify the time spent on switching the system mode from XTAL CTL to SW-to-XTAL. The wait cycle can be calculated as follows: (65536 – xtaltime) x T46.8 K. T46.8 K indicates the clock cycle of the 46.8 kHz low-frequency clock.
[2]	RO	reserved	Reserved. Reading this field returns 0x0, and writing to this field has no effect.
[1:0]	RO	reserved	Reserved. Reading this field returns the written value, and writing to this field has no effect.

SC_PLLCTRL

SC_PLLCTRL is a PLL control register. It is used to enable or disable the on-chip ARM PLL through software or system mode switching. It can be also used to the set the stable time of the ARM PLL.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

When the ARM PLL is enabled by controlling the system mode (implemented by configuring SC_PLLCTRL[pllover]), the ARM PLL is automatically disabled if the system is in non-normal mode.

When the ARM PLL is enabled by controlling the software (implemented by configuring SC_PLLCTRL[pllen]), whether the ARMPLL is enabled is controlled by the software but not system mode switching.

The clock frequency of the ARM PLL is controlled by PERI_CRG0 and PERI_CRG1. When the PLL frequency is changed, a stable clock can be output only after 0.5 ms. Therefore, the plltime of this register must meet this requirement.

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Offset Address	Register Name	Total Reset Value
0x014	SC_PLLCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plltime																									reserved	reserved	pllover
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved. Reading this field returns 0x0, and writing to this field has no effect.
[27:3]	RW	plltime	Stable time of the ARM PLL. This time refers to the period from the start of the PLL to the output of a stable PLL clock, that is, the wait time for switching the system mode from PLL CTL to SW-to-PLL. The timeout period is calculated as follows: (33554432 – plltime) x TXIN TXIN indicates the clock cycle of the external crystal oscillator of the Hi3516A.
[2]	RO	reserved	Reserved. Reading this field returns 0x0, and writing to this field has no effect.
[1]	RO	reserved	Reserved.
[0]	RW	pllover	Whether the ARM PLL is enabled is controlled by the software but not system mode switching. This bit must be set to 0. The ARM PLL is enabled by switching the system mode. 1: reserved

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SOLFINT

SOLFINT is a software interrupt register.

Offset Address	Register Name	Total Reset Value
0x001C	SOLFINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															software_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	software_int	Software interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

SOLFTYPE

SOLFTYPE is a software interrupt vector register.

Offset Address	Register Name	Total Reset Value
0x0020	SOLFTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	software_int_vector																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	software_int_vector	Software interrupt vector.

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SC_LOCKEN

SC_LOCKEN is a key register lock registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL, SYSSTAT and SC_PLLCTRL. When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status but not the written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

SYSSTAT

SYSSTAT is a system status register.

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bootrom_sel_in	reserved		a7_standbywfe	reserved	a7_standbywfi	reserved		reserved		reserved	a7_smpnamp	reserved												sfc_addr_mode	a7_standbywfil2	boot_mode	reserved	sfc_device_mode		sfc_nand_ecc_type	sfc_nand_page_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	bootrom_sel_in	Whether the system boots from the BOOTROM. 0: no 1: yes
[30:29]	RO	reserved	Reserved.

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[28]	RO	a7_standbywfe	Whether the A7 processor is in wait for event (WFE) status. 0: non-WFE status 1: WFE status
[27]	RO	reserved	Reserved.
[26]	RO	a7_standbywfi	Whether the A7 processor is in wait for interrupt (WFI) status. 0: non-WFI status 1: WFI status
[25:24]	RO	reserved	Reserved.
[23:22]	RO	reserved	Reserved.
[21]	RO	reserved	Reserved.
[20]	RO	a7_smpnamp	Equalization mode of the A7 processor. 0: non-equalization mode 1: equalization mode
[19:8]	RO	reserved	Reserved.
[7]	RO	sfc_boot_mode	Boot address mode of the SPI NOR flash when Ssfc_device_mode is 0. 0: 3-byte mode 1: 4-byte mode Boot address mode of the SPI NAND flash when sfc_device_mode is 1. 0: 1-wire boot mode 1: 4-wire boot mode
[6]	RO	a7_standbywfil2	Whether L2 is in WFI status. 0: non-WFI status 1: WFI status
[5]	RO	boot_mode	Boot mode. 0: booting from the SPI flash 1: booting from the NAND flash
[4]	RO	reserved	Reserved.
[3]	RO	sfc_device_mode	SPI flash select. 0: SPI NOR flash 1: SPI NAND flash
[2:1]	RO	sfc_nand_ecc_type	ECC type of the SPI NAND flash. 01: 8-bit ECC 11: 24-bit ECC Others: reserved

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[0]	RO	sfc_nand_page_size	SPI NAND flash page size. 0: 2 KB 1: 4 KB

DDRT0

DDRT0 is DDR training register 0.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0090	DDRT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt0	DDR training register 0.

DDRT1

DDRT1 is DDR training register 1.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0094	DDRT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt1	DDR training register 1.

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DDRT2

DDRT2 is DDR training register 2.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0098	DDRT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt2	DDR training register 2.

DDRT3

DDRT3 is DDR training register 3.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x009C	DDRT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt3	DDR training register 3.

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DDRT4

DDRT4 is DDR training register 4.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x00A0	DDRT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt4	DDR training register 4.

DDRT5

DDRT5 is DDR training register 5.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x00A4	DDRT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt5	DDR training register 5.

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DDRT6

DDRT6 is DDR training register 6.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x00A8	DDRT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt6	DDR training register 6.

DDRT7

DDRT7 is DDR training register 7.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x00AC	DDRT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddrt7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ddrt7	DDR training register 7.

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SYSBOOT0

SYSBOOT0 is system boot register 0.

Offset Address	Register Name	Total Reset Value
0x0130	SYSBOOT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot0	System boot register 0.

SYSBOOT1

SYSBOOT1 is system boot register 1.

Offset Address	Register Name	Total Reset Value
0x0134	SYSBOOT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot1	System boot register 1.

SYSBOOT2

SYSBOOT2 is system boot register 2.

Offset Address	Register Name	Total Reset Value
0x0138	SYSBOOT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot2	System boot register 2.

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SYSBOOT3

SYSBOOT3 is system boot register 3.

Offset Address	Register Name	Total Reset Value
0x013C	SYSBOOT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot3	System boot register 3.

SYSBOOT4

SYSBOOT4 is system boot register 4.

Offset Address	Register Name	Total Reset Value
0x0140	SYSBOOT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot4	System boot register 4.

SYSBOOT5

SYSBOOT5 is system boot register 5.

Offset Address	Register Name	Total Reset Value
0x0144	SYSBOOT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot5	System boot register 5.

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SYSBOOT6

SYSBOOT6 is system boot register 6.

Offset Address	Register Name	Total Reset Value
0x0148	SYSBOOT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot6	System boot register 6.

SYSBOOT7

SYSBOOT7 is system boot register 7.

Offset Address	Register Name	Total Reset Value
0x014C	SYSBOOT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot7	System boot register 7.

SYSBOOT8

SYSBOOT8 is system boot register 8.

Offset Address	Register Name	Total Reset Value
0x0150	SYSBOOT8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot8																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot8	System boot register 8.

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SYSBOOT9

SYSBOOT9 is system boot register 9.

Offset Address	Register Name	Total Reset Value
0x0154	SYSBOOT9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot9																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot9	System boot register 9.

SYSBOOT10

SYSBOOT10 is system boot register 10.

Offset Address	Register Name	Total Reset Value
0x0158	SYSBOOT10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot10																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot10	System boot register 10.

SYSBOOT11

SYSBOOT11 is system boot register 11.

Offset Address	Register Name	Total Reset Value
0x015C	SYSBOOT11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysboot11																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sysboot11	System boot register 11.

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SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	chipid		reserved				sysid0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	chipid	Version 0x01: Hi3516A 0x02: Hi3516D Others values: reserved
[23:8]	RO	reserved	Reserved.
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0xA1

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	1	0	1	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0xA1.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x16

Bit	7	6	5	4	3	2	1	0
Name	sysid2							

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Reset	0	0	0	1	0	1	1	0

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x16.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5.5 Peripheral Control Registers

3.5.5.1 Register Summary

Table 3-10 describes peripheral control registers.

Table 3-10 Summary of peripheral control registers (base address: 0x2012_0000)

Offset Address	Register	Description	Page
0x0000	MISC_CTRL0	MISC register 0	3-78
0x0004	MISC_CTRL1	MISC register 1	3-79
0x0008	MISC_CTRL2	MISC register 2	3-81
0x000C	MISC_CTRL3	MISC register 3	3-82
0x0010	MISC_CTRL4	MISC register 4	3-83
0x0014	MISC_CTRL5	MISC register 5	3-84
0x0018	MISC_CTRL6	MISC register 6	3-86
0x001C	MISC_CTRL7	MISC register 7	3-87
0x0020	MISC_CTRL8	MISC register 8	3-87
0x0024	MISC_CTRL9	MISC register 9	3-88
0x0028	MISC_CTRL10	MISC register 10	3-89
0x002C	MISC_CTRL11	MISC register 11	3-89

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Offset Address	Register	Description	Page
0x0030	MISC_CTRL12	MISC register 12	3-90
0x0034	MISC_CTRL13	MISC register 13	3-91
0x0038	MISC_CTRL14	MISC register 14	3-91
0x003C	MISC_CTRL15	MISC register 15	3-92
0x0040	MISC_CTRL16	MISC register 16	3-93
0x0044	MISC_CTRL17	MISC register 17	3-94
0x0048	MISC_CTRL18	MISC register 18	3-95
0x004C	MISC_CTRL19	MISC register 19	3-96
0x0050	MISC_CTRL20	MISC register 20	3-96
0x0054	MISC_CTRL21	MISC register 21	3-96
0x0058	MISC_CTRL22	MISC register 22	3-97
0x005C	MISC_CTRL23	MISC register 23	3-97
0x0060	MISC_CTRL24	MISC register 24	3-98
0x0064	MISC_CTRL25	MISC register 25	3-98
0x0068	MISC_CTRL26	MISC register 26	3-99
0x006C	MISC_CTRL27	MISC register 27	3-100
0x0070	MISC_CTRL28	MISC register 28	3-100
0x0074	MISC_CTRL29	MISC register 29	3-101
0x0078	MISC_CTRL30	MISC register 30	3-101
0x00C8	MISC_CTRL50	Audio CODEC control register 0	3-103
0x00CC	MISC_CTRL51	Audio CODEC control register 1	3-107
0x00D0	MISC_CTRL52	Audio CODEC control register 2	3-108
0x00D4	MISC_CTRL53	Audio CODEC control register 3	3-110
0x00D8	MISC_CTRL54	Audio CODEC control register 4	3-110
0x00E0	MISC_CTRL56	MISC register 56	3-112

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3.5.5.2 Register Description

MISC_CTRL0

MISC_CTRL0 is MISC register 0.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0000	MISC_CTRL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		l2rstdisable	l1rstdisable	reserved																							a7_cfgsdisable	reserved	a7_cfgte	reserved	a7_cp15sdiable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29]	RW	l2rstdisable	Automatic L2 cache invalidate disable at reset. Tie this signal high to disable L2 cache invalidate at reset (soft reset). Tie this signal low to enable L2 cache invalidate at reset. Only change this signal when the processor is in the reset state.
[28]	RW	l1rstdisable	Automatic data cache, instruction cache, and TLB invalidate disable at reset. Tie this signal high to disable data cache invalidate, instruction cache invalidate, and TLB invalidate at reset (soft reset). Tie this signal low to enable data cache invalidate, instruction cache invalidate, and TLB invalidate at reset. Only change these signals when the processor is in the reset state.
[27:5]	RW	reserved	Reserved.
[4]	RW	a7_cfgsdisable	Disable for write access to some secure registers. Connect to system security control logic to control access to GIC registers. If the system does not include this functionality, tie this signal low.
[3]	RW	reserved	Reserved.

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[2]	RW	a7_cfgte	Processor state control for exception handling (TE bit) at reset. Tie this signal low for ARM instruction set for exception handling, or high for Thumb instruction set for exception handling. Only change this signal when the processor is in the reset state.
[1]	RW	reserved	Reserved.
[0]	RW	a7_cp15sdiable	CP15 security extension registers disable.

MISC_CTRL1

MISC_CTRL1 is MISC register 1.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0004	MISC_CTRL1	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vicap_vpss_online	reserved	reserved	ssp1_cs_sel		i2c1_dma_ch_sel		mipi_phy_mode				reserved		reserved		reserved								uart1_rts_ctrl	bootrom_pgen	bootram2_ck_gt_en	bootram1_ck_gt_en	bootram0_ck_gt_en	mdu_ddrt_mst_sel	sdio0_card_det_mode	sdio1_card_det_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	vicap_vpss_online	VICAP and VPSS mode. 0: offline mode 1: online mode
[29]	RW	reserved	Reserved.
[28]	RO	reserved	Reserved.

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[27:26]	RW	ssp1_cs_sel	SSP1 CS select. 00: CS0 01: CS1 10: CS2 11: reserved
[25:23]	RW	i2c1_dma_ch_sel	Connection between I^2C1 and DMA hardware request line. 0xx: I^2C1 does not connect to any DMA hardware request line. In this case, I^2C1 cannot work in DMA mode. 100: I^2C1 connects to DMA hardware request lines 0 and 1. In this case, I^2C0 cannot work in DMA mode. 101: I^2C1 connects to DMA hardware request lines 2 and 3. In this case, I^2C2 cannot work in DMA mode. 110: I^2C1 connects to DMA hardware request lines 12 and 13. In this case, SSP1 cannot work in DMA mode. 111: I^2C1 connects to DMA hardware request lines 14 and 15. In this case, SSP0 cannot work in DMA mode.
[22:20]	RW	mipi_phy_mode	MIPI PHY mode. 000: MIPI mode 001: LVDS mode 01x: CMOS mode 1xx: bypass mode (VI data is derived from the chip I/O)
[19:18]	RO	reserved	Reserved.
[17:16]	RO	reserved	Reserved.
[15:8]	RW	reserved	Reserved.
[7]	RW	uart1_rts_ctrl	uart1_rts signal reverse control. 0: not reversed 1: reversed
[6]	RW	bootrom_pgen	BOOTROM power supply control. 0: powered on 1: powered off
[5]	RW	bootram2_ck_gt_en	BOOTRAM2 clock enable. 0: enabled 1: disabled
[4]	RW	bootram1_ck_gt_en	BOOTRAM1 clock enable. 0: enabled 1: disabled
[3]	RW	bootram0_ck_gt_en	BOOTRAM0 clock enable. 0: enabled 1: disabled

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[2]	RW	mdu_ddrt_mst_sel	MDU/DDRT access select through media1 AXI. 0: MDU 1: DDRT
[1]	RW	sdio0_card_det_mode	Reverse control for the SDIO0 card detection signal. 0: not reversed 1: reversed
[0]	RW	sdio1_card_det_mode	Reverse control for the SDIO1 card detection signal. 0: not reversed 1: reversed

MISC_CTRL2

MISC_CTRL2 is MISC register 2.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0008	MISC_CTRL2	0x0052_5101

Bit	31 30 29 28	27	26	25 24	23 22 21 20	19	18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Name	reserved		reserved	reserved		reserved	l2_data_ram_ema	tlb_ram_adjust	l2_tag_ram_adjust	l2_data_ram_emaw	l1_itag_ram_adjust	l1_idata_ram_adjust	l1_dtag_ram_adjust	l1_ddirty_ram_adjust	l1_ddata_ram_adjust
Reset	0 0 0 0	0	0	0 0	0 1 0 1	0	0 1 0	0 1	0 1	0 0	0 1	0 0	0 0	0 0	0 1

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26]	RO	reserved	Reserved.
[25:20]	RO	reserved	Reserved.
[19]	RW	reserved	Reserved.
[18:16]	RW	l2_data_ram_ema	l2_data_ram ema control signal.
[15:14]	RW	tlb_ram_adjust	tlb_ram mem speed adjustment control.
[13:12]	RW	l2_tag_ram_adjust	l2_tag_ram mem speed adjustment control.

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[11:10]	RW	l2_data_ram_emaw	l2_data_ram emaw control signal.
[9:8]	RW	l1_itag_ram_adjust	l1_itag_ram mem speed adjustment control.
[7:6]	RW	l1_idata_ram_adjust	l1_idata_ram mem speed adjustment control.
[5:4]	RW	l1_dtag_ram_adjust	l1_dtag_ram mem speed adjustment control.
[3:2]	RW	l1_ddirty_ram_adjust	l1_ddirty_ram mem speed adjustment control.
[1:0]	RW	l1_ddata_ram_adjust	l1_ddata_ram mem speed adjustment control.

MISC_CTRL3

MISC_CTRL3 is MISC register 3.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x000C	MISC_CTRL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										powerswitch1_sel_mux	powerswitch1_sel	reserved		powerswitch0_sel_mux	powerswitch0_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved.
[5]	RW	powerswitch1_sel_mux	Power switch 1 source select. 0: SDIO1 controller 1: powerswitch1_sel register

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[4]	RW	powerswitch1_sel	Power switch 1 output voltage select (valid only when powerswitch1_sel_mux is 1). 0: 3.3 V 1: 1.8 V
[3:2]	RW	reserved	Reserved.
[1]	RW	powerswitch0_sel_mux	Power switch 0 source select. 0: SDIO0 controller 1: powerswitch0_sel register
[0]	RW	powerswitch0_sel	Power switch 0 select (valid only when powerswitch0_sel_mux is 1). 0: 3.3 V 1: 1.8 V

MISC_CTRL4

MISC_CTRL4 is MISC register 4.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0010	MISC_CTRL4	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	avc_ret1n_bypass	reserved																								sfc_nor_ret1n	sfc_nand_ret1n	gsf_ret1n	usb_ret1n	nandc_ret1n	cipher_ret1n	bootram_ret1n
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	avc_ret1n_bypass	AVC automatic mem ret1n function bypass. 0: enabled 1: bypassed
[30:7]	RW	reserved	Reserved.

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[6]	RW	sfc_nor_ret1n	mem ret1n signal in sfc_nor ctrl. Set this signal to 1 when sfc_nor ctrl is enabled or set this signal to 0 when sfc_nor ctrl is disabled to reduce mem power consumption.
[5]	RW	sfc_nand_ret1n	mem ret1n signal in sfc_nand ctrl. Set this signal to 1 when sfc_nand ctrl is enabled or set this signal to 0 when sfc_nand ctrl is disabled to reduce mem power consumption.
[4]	RW	gsf_ret1n	mem ret1n signal in gsf ctrl. Set this signal to 1 whengsf ctrl is enabled or set this signal to 0 when gsf ctrl is disabled to reduce mem power consumption.
[3]	RW	usb_ret1n	mem ret1n signal in usb ctrl. Set this signal to 1 when usb ctrl is enabled or set this signal to 0 when usb ctrl is disabled to reduce mem power consumption.
[2]	RW	nandc_ret1n	mem ret1n signal in nandc ctrl. Set this signal to 1 when nandc ctrl is enabled or set this signal to 0 when nandc ctrl is disabled to reduce mem power consumption.
[1]	RW	cipher_ret1n	mem ret1n signal in the cipher. Set this signal to 1 when the cipher is enabled or set this signal to 0 when the cipher is disabled to reduce mem power consumption.
[0]	RW	bootram_ret1n	mem ret1n signal in the BOOTROM. Set this signal to 1 when the BOOTROM is enabled or set this signal to 0 when the BOOTROM is disabled to reduce mem power consumption.

MISC_CTRL5

MISC_CTRL5 is MISC register 5.

CAUTION

This register is not reset when the system is soft-reset.

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Offset Address	Register Name	Total Reset Value
0x0014	MISC_CTRL5	0x0000_0066

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm3_mux_sel	pwm2_mux_sel	pwm1_mux_sel	pwm0_mux_sel	reserved									vedu_pwrdn_stat	vedu_pwrdn_req	vedu_pwrdn_iso	reserved	avc_pwrdn_stat	avc_pwrdn_req	avc_pwrdn_iso
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.
[19]	RW	pwm3_mux_sel	PWM3 output source select. 0: normal PWM3 output 1: PWM3 output of the PMC module
[18]	RW	pwm2_mux_sel	PWM2 output source select. 0: normal PWM2 output 1: PWM2 output of the PMC module
[17]	RW	pwm1_mux_sel	PWM1 output source select. 0: normal PWM1 output 1: PWM1 output of the PMC module
[16]	RW	pwm0_mux_sel	PWM0 output source select. 0: normal PWM0 output 1: PWM0 output of the PMC module
[15:7]	RW	reserved	Reserved.
[6]	RO	vedu_pwrdn_stat	VEDU power-off status. 0: powered off 1: powered on
[5]	RW	vedu_pwrdn_req	VEDU power-off request. 0: powered off 1: powered on
[4]	RW	vedu_pwrdn_iso	VEDU signal isolation control. The VEDU signal must be isolated before power-off, and the bus must be idle when isolation is started. 0: not isolated 1: isolated
[3]	RW	reserved	Reserved.

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[2]	RO	avc_pwrdn_stat	AVC power-off status. 0: powered off 1: powered on
[1]	RW	avc_pwrdn_req	AVC power-off request. 0: powered off 1: powered on
[0]	RW	avc_pwrdn_iso	AVC signal isolation control. The AVC signal must be isolated before power-off, and the bus must be idle when isolation is started. 0: not isolated 1: isolated

MISC_CTRL6

MISC_CTRL6 is MISC register 6.

Offset Address	Register Name	Total Reset Value
0x0018	MISC_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysaxi_count_en_port1	sysaxi_over_value_port1															sysaxi_count_en_port0	sysaxi_over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_count_en_port1	Timeout count enable for the SYS AXI bus port M1 (AHB1). 0: disabled 1: enabled
[30:16]	RW	sysaxi_over_value_port1	Timeout count value of the SYS AXI bus port M1 (AHB1). Count value = sysaxi_over_value_port1 x 2
[15]	RW	sysaxi_count_en_port0	Timeout count enable for the SYS AXI bus port M0 (AHB0). 0: disabled 1: enabled
[14:0]	RW	sysaxi_over_value_port0	Timeout count value of the SYS AXI bus port M0 (AHB0). Count value = sysaxi_over_value_port0 x 2

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MISC_CTRL7

MISC_CTRL7 is MISC register 7.

Offset Address	Register Name	Total Reset Value
0x001C	MISC_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sysaxi_count_en_port2	sysaxi_over_value_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15]	RW	sysaxi_count_en_port2	Timeout count enable for the SYS AXI bus port M2 (A7). 0: disabled 1: enabled
[14:0]	RW	sysaxi_over_value_port2	Timeout count value of the SYS AXI bus port M2 (A7). Count value = sysaxi_over_value_port2 x 2

MISC_CTRL8

MISC_CTRL8 is MISC register 8.

Offset Address	Register Name	Total Reset Value
0x0020	MISC_CTRL8	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					sysaxi_port2_pri			reserved	sysaxi_port1_pri			reserved	sysaxi_port0_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved.

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[10:8]	RW	sysaxi_port2_pri	Priority of the SYS AXI bus port M2 (A7). The value 3 indicates the highest priority.
[7]	RW	reserved	Reserved.
[6:4]	RW	sysaxi_port1_pri	Priority of the SYS AXI bus port M1 (AHB1). The value 3 indicates the highest priority.
[3]	RW	reserved	Reserved.
[2:0]	RW	sysaxi_port0_pri	Priority of the SYS AXI bus port M0 (AHB0). The value 3 indicates the highest priority.

MISC_CTRL9

MISC_CTRL9 is MISC register 9.

Offset Address	Register Name	Total Reset Value
0x0024	MISC_CTRL9	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													sysaxi_slave_priority_s5			reserved	sysaxi_slave_priority_s4			reserved	sysaxi_slave_priority_s3			reserved	sysaxi_slave_priority_s2			reserved	sysaxi_slave_priority_s1		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved.
[18:16]	RW	sysaxi_slave_priority_s5	Priority for accessing the SYS AXI s5 (cfgahb1) port bus. The value 7 indicates the highest priority.
[15]	RW	reserved	Reserved.
[14:12]	RW	sysaxi_slave_priority_s4	Priority for accessing the SYS AXI s4 (mddrc) port bus. The value 7 indicates the highest priority.
[11]	RW	reserved	Reserved.
[10:8]	RW	sysaxi_slave_priority_s3	Priority for accessing the SYS AXI s3 (mediaapb) port bus. The value 7 indicates the highest priority.
[7]	RW	reserved	Reserved.

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[6:4]	RW	sysaxi_slave_priority_s2	Priority for accessing the SYS AXI s2 (sysapb) port bus. The value 7 indicates the highest priority.
[3]	RW	reserved	Reserved.
[2:0]	RW	sysaxi_slave_priority_s1	Priority for accessing the SYS AXI s1 (cfgahb0) port bus. The value 7 indicates the highest priority.

MISC_CTRL10

MISC_CTRL10 is MISC register 10.

Offset Address	Register Name	Total Reset Value
0x0028	MISC_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

MISC_CTRL11

MISC_CTRL11 is MISC register 11.

Offset Address	Register Name	Total Reset Value
0x002C	MISC_CTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0axi0_count_en_port1	mda0axi0_over_value_port1															mda0axi0_count_en_port0	mda0axi0_over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mda0axi0_count_en_port1	Timeout count enable for the MDA0 AXI0 bus port M1 (AVC). 0: disabled 1: enabled

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[30:16]	RW	mda0axi0_over_value_port1	Timeout count value of the MDA0 AXI0 bus port M1 (AVC). Count value = mda0axi_over_value_port1 x 2
[15]	RW	mda0axi0_count_en_port0	Timeout count enable for the MDA0 AXI0 bus port M0 (VEDU). 0: disabled 1: enabled
[14:0]	RW	mda0axi0_over_value_port0	Timeout count value of the MDA0 AXI0 bus port M0 (VEDU). Count value = mda0axi_over_value_port0 x 2

MISC_CTRL12

MISC_CTRL12 is MISC register 12.

Offset Address	Register Name	Total Reset Value
0x0030	MISC_CTRL12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0axi0_count_en_port2	mda0axi0_over_value_port2															mda0axi0_count_en_port3	mda0axi0_over_value_port3														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mda0axi0_count_en_port2	Timeout count enable for the MDA0 AXI0 bus port M2 (VGS). 0: disabled 1: enabled
[30:16]	RW	mda0axi0_over_value_port2	Timeout count value of the MDA0 AXI0 bus port M2 (VGS). Count value = mda0axi_over_value_port1 x 2
[15]	RW	mda0axi0_count_en_port3	Timeout count enable for the MDA0 AXI0 bus port M3 (SDIO). 0: disabled 1: enabled
[14:0]	RW	mda0axi0_over_value_port3	Timeout count value of the MDA0 AXI0 bus port M3 (SDIO). Count value = mda0axi_over_value_port0 x 2

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MISC_CTRL13

MISC_CTRL13 is MISC register 13.

Offset Address	Register Name	Total Reset Value
0x0034	MISC_CTRL13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

MISC_CTRL14

MISC_CTRL14 is MISC register 14.

Offset Address	Register Name	Total Reset Value
0x0038	MISC_CTRL14	0x0000_0123

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	mda0axi0_port3_pri			reserved	mda0axi0_port2_pri			reserved	mda0axi0_port1_pri			reserved	mda0axi0_port0_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved.
[14:12]	RW	mda0axi0_port3_pri	Priority of the MDA0 AXI0 bus port M3 (SDIO). The value 3 indicates the highest priority.
[11]	RW	reserved	Reserved.
[10:8]	RW	mda0axi0_port2_pri	Priority of the MDA0 AXI0 bus port M2 (VGS). The value 3 indicates the highest priority.
[7]	RW	reserved	Reserved.
[6:4]	RW	mda0axi0_port1_pri	Priority of the MDA0 AXI0 bus port M1 (AVC). The value 3 indicates the highest priority.
[3]	RW	reserved	Reserved.

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[2:0]	RW	mda0axi0_port0_pri	Priority of the MDA0 AXI0 bus port M0 (VEDU). The value 3 indicates the highest priority.

MISC_CTRL15

MISC_CTRL15 is MISC register 15.

Offset Address	Register Name	Total Reset Value
0x003C	MISC_CTRL15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda1axi_count_en_port1	mda1axi_over_value_port1															mda1axi_count_en_port0	mda1axi_over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mda1axi_count_en_port1	Timeout count enable for the MDA1 AXI bus port M1 (JPGE). 0: disabled 1: enabled
[30:16]	RW	mda1axi_over_value_port1	Timeout count value of the MDA1 AXI bus port M1 (JPGE). Count value = mda1axi_over_value_port1 x 2
[15]	RW	mda1axi_count_en_port0	Timeout count enable for the MDA1 AXI bus port M0 (TDE). 0: disabled 1: enabled
[14:0]	RW	mda1axi_over_value_port0	Timeout count value of the MDA1 AXI bus port M0 (TDE). Count value = mda1axi_over_value_port0 x 2

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MISC_CTRL16

MISC_CTRL16 is MISC register 16.

Offset Address	Register Name	Total Reset Value
0x0040	MISC_CTRL16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda1axi_count_en_port3	mda1axi_over_value_port3															mda1axi_count_en_port2	mda1axi_over_value_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mda1axi_count_en_port3	Timeout count enable for the MDA1 AXI bus port M3 (IVE). 0: disabled 1: enabled
[30:16]	RW	mda1axi_over_value_port3	Timeout count value of the MDA1 AXI bus port M3 (IVE). Count value = mda1axi_over_value_port3 x 2
[15]	RW	mda1axi_count_en_port2	Timeout count enable for the MDA1 AXI bus port M2 (AIO). 0: disabled 1: enabled
[14:0]	RW	mda1axi_over_value_port2	Timeout count value of the MDA1 AXI bus port M2 (AIO). Count value = mda1axi_over_value_port2 x 2

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MISC_CTRL17

MISC_CTRL17 is MISC register 17.

Offset Address	Register Name	Total Reset Value
0x0044	MISC_CTRL17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mda1axi_count_en_port4	mda1axi_over_value_port4														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15]	RW	mda1axi_count_en_port4	Timeout count enable for the MDA1 AXI bus port M4 (MD_DDRT). 0: disabled 1: enabled
[14:0]	RW	mda1axi_over_value_port4	Timeout count value of the MDA1 AXI bus port M4 (MD_DDRT). Count value = mda1axi_over_value_port4 x 2

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MISC_CTRL18

MISC_CTRL18 is MISC register 18.

Offset Address	Register Name	Total Reset Value
0x0048	MISC_CTRL18	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													mda1axi_port4_pri			reserved	mda1axi_port3_pri			reserved	mda1axi_port2_pri			reserved	mda1axi_port1_pri			reserved	mda1axi_port0_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved.
[18:16]	RW	mda1axi_port4_pri	Priority of the MDA1 AXI bus port M4 (MD_DDRT). The value 7 indicates the highest priority.
[15]	RW	reserved	Reserved.
[14:12]	RW	mda1axi_port3_pri	Priority of the MDA1 AXI bus port M3 (IVE). The value 7 indicates the highest priority.
[11]	RW	reserved	Reserved.
[10:8]	RW	mda1axi_port2_pri	Priority of the MDA1 AXI bus port M2 (AIO). The value 7 indicates the highest priority.
[7]	RW	reserved	Reserved.
[6:4]	RW	mda1axi_port1_pri	Priority of the MDA1 AXI bus port M1 (JPGE). The value 7 indicates the highest priority.
[3]	RW	reserved	Reserved.
[2:0]	RW	mda1axi_port0_pri	Priority of the MDA1 AXI bus port M0 (TDE). The value 7 indicates the highest priority.

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MISC_CTRL19

MISC_CTRL19 is MISC register 19.

Offset Address	Register Name	Total Reset Value
0x004C	MISC_CTRL19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

MISC_CTRL20

MISC_CTRL20 is MISC register 20.

Offset Address	Register Name	Total Reset Value
0x0050	MISC_CTRL20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

MISC_CTRL21

MISC_CTRL21 is MISC register 21.

Offset Address	Register Name	Total Reset Value
0x0054	MISC_CTRL21	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

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MISC_CTRL22

MISC_CTRL22 is MISC register 22.

Offset Address	Register Name	Total Reset Value
0x0058	MISC_CTRL22	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	vedu_qosmap	md_ddrt_qosmap	ive_qosmap	aio_qosmap	jpge_qosmap	tde_qosmap	vicap_qosmap	vdp_qosmap
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	vedu_qosmap	QoS value of the VEDU in the MDDRC.
[27:24]	RW	md_ddrt_qosmap	QoS value of the MD_DDRT in the MDDRC.
[23:20]	RW	ive_qosmap	QoS value of the IVE in the MDDRC.
[19:16]	RW	aio_qosmap	QoS value of the AIO in the MDDRC.
[15:12]	RW	jpge_qosmap	QoS value of the JPGE in the MDDRC.
[11:8]	RW	tde_qosmap	QoS value of the TDE in the MDDRC.
[7:4]	RW	vicap_qosmap	QoS value of the VICAP in the MDDRC.
[3:0]	RW	vdp_qosmap	QoS value of the VDP in the MDDRC.

MISC_CTRL23

MISC_CTRL23 is MISC register 23.

Offset Address	Register Name	Total Reset Value
0x005C	MISC_CTRL23	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	sfc_nand_qosmap	sfc_nor_qosmap	nfc_qosmap	sdio1_qosmap	sdio0_qosmap	a7_qosmap	vpss_qosmap	vgs_qosmap
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	sfc_nand_qosmap	QoS value of sfc_nand in the MDDRC.
[27:24]	RW	sfc_nor_qosmap	QoS value of sfc_nor in the MDDRC.
[23:20]	RW	nfc_qosmap	QoS value of the NFC in the MDDRC.
[19:16]	RW	sdio1_qosmap	QoS value of SDIO1 in the MDDRC.
[15:12]	RW	sdio0_qosmap	QoS value of SDIO0 in the MDDRC.

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[11:8]	RW	a7_qosmap	QoS value of A7 in the MDDRC.
[7:4]	RW	vpss_qosmap	QoS value of the VPSS in the MDDRC.
[3:0]	RW	vgs_qosmap	QoS value of the VGS in the MDDRC.

MISC_CTRL24

MISC_CTRL24 is MISC register 24.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		avc_qosmap	usb_qosmap	cipher_qosmap	dma2_qosmap	dma1_qosmap	gsf_qosmap
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:20]	RW	avc_qosmap	QoS value of the AVC in the MDDRC.
[19:16]	RW	usb_qosmap	QoS value of the USB in the MDDRC.
[15:12]	RW	cipher_qosmap	QoS value of the cipher in the MDDRC.
[11:8]	RW	dma2_qosmap	QoS value of DMA2 in the MDDRC.
[7:4]	RW	dma1_qosmap	QoS value of DMA1 in the MDDRC.
[3:0]	RW	gsf_qosmap	QoS value of GSF in the MDDRC.

MISC_CTRL25

MISC_CTRL25 is MISC register 25.

Offset Address	Register Name	Total Reset Value
0x0064	MISC_CTRL25	0x3210_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	vedu_to	md_ddrt_to	ive_to	aio_to	jpge_to	tde_to	vicap_to	vdp_to
Reset	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	vedu_to	Timeout select for the VEDU in the MDDRC.
[27:24]	RW	md_ddrt_to	Timeout select for MD_DDRT in the MDDRC.
[23:20]	RW	ive_to	Timeout select for the IVE in the MDDRC.

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[19:16]	RW	aio_to	Timeout select for the AIO in the MDDRC.
[15:12]	RW	jpge_to	Timeout select for the JPGE in the MDDRC.
[11:8]	RW	tde_to	Timeout select for the TDE in the MDDRC.
[7:4]	RW	vicap_to	Timeout select for the VICAP in the MDDRC.
[3:0]	RW	vdp_to	Timeout select for the VDP in the MDDRC.

MISC_CTRL26

MISC_CTRL26 is MISC register 26.

Offset Address	Register Name	Total Reset Value
0x0068	MISC_CTRL26	0x3210_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	sfc_nand_to	sfc_nor_to	nfc_to	sdio1_to	sdio0_to	a7_to	vpss_to	vgs_to
Reset	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	sfc_nand_to	Timeout select for sfc_nand in the MDDRC.
[27:24]	RW	sfc_nor_to	Timeout select for sfc_nor in the MDDRC.
[23:20]	RW	nfc_to	Timeout select for the NFC in the MDDRC.
[19:16]	RW	sdio1_to	Timeout select for SDIO1 in the MDDRC.
[15:12]	RW	sdio0_to	Timeout select for SDIO0 in the MDDRC.
[11:8]	RW	a7_to	Timeout select for A7 in the MDDRC.
[7:4]	RW	vpss_to	Timeout select for the VPSS in the MDDRC.
[3:0]	RW	vgs_to	Timeout select for the VGS in the MDDRC.

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MISC_CTRL27

MISC_CTRL27 is MISC register 27.

Offset Address	Register Name	Total Reset Value
0x006C	MISC_CTRL27	0x3210_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		avc_to	usb_to	cipher_to	dma2_to	dma1_to	gsf_to
Reset	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:20]	RW	avc_to	Timeout select for the AVC in the MDDRC.
[19:16]	RW	usb_to	Timeout select for the USB in the MDDRC.
[15:12]	RW	cipher_to	Timeout select for the cipher in the MDDRC.
[11:8]	RW	dma2_to	Timeout select for DMA2 in the MDDRC.
[7:4]	RW	dma1_to	Timeout select for DMA1 in the MDDRC.
[3:0]	RW	gsf_to	Timeout select for the GSF in the MDDRC.

MISC_CTRL28

MISC_CTRL28 is MISC register 28.

Offset Address	Register Name	Total Reset Value
0x0070	MISC_CTRL28	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

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MISC_CTRL29

MISC_CTRL29 is MISC register 29.

Offset Address	Register Name	Total Reset Value
0x0074	MISC_CTRL29	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

MISC_CTRL30

MISC_CTRL30 is MISC register 30.

Offset Address	Register Name	Total Reset Value
0x0078	MISC_CTRL30	0x0C03_13A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb_chipid	reserved			usb2_phy_dmpulldown	usb2_phy_dppulldown	ss_scaledown_mode		reserved	ss_hubsetup_min_i	reserved				usbovr_p_ctrl	usbpwr_pctrl	reserved	port_ovr_en	reserved	port_pwr_en	reserved		ss_ena_incr16_i	ss_ena_incr8_i	ss_ena_incr4_i	ss_ena_incr_align_i	ss_autoppd_on_overcur_en_i	reserved		app_start_clk_i	ohci_susp_lgcy_i	ss_word_if_i
Reset	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	usb_chipid	Host and device switching control. 0: host 1: device
[30:28]	RW	reserved	Reserved.
[27]	RW	usb2_phy_dmpulldown	D− pull-down resistor enable. 1: enabled 0: disabled

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[26]	RW	usb2_phy_dppulldown	D+ pull-down resistor enable. 1: enabled 0: disabled
[25:24]	RW	ss_scaledown_mode	Scale-down mode. 00: Scale-down is disabled for all timings, and the actual timings are used. 01: Scale-down is enabled for all timings except the suspended and resumed timings in device mode. 10: Scale-down is enabled only for the suspended and resumed timings in device mode. 11: Scale-down timings of bit 0 and bit 1 are enabled.
[23]	RW	reserved	Reserved.
[22]	RW	ss_hubsetup_min_i	Number of idle cycles after the full-speed preamble packet. 0: 5 idle full-speed cycles 1: 4 full-speed idle cycles
[21:18]	-	reserved	Reserved.
[17]	RW	usbovr_p_ctrl	Over-current protection polarity. 0: active low 1: active high
[16]	RW	usbpwr_pctrl	USB PHY power shutdown polarity. 0: active low 1: active high
[15]	-	reserved	Reserved.
[14]	RW	port_ovr_en	Over-current protection enable for the USB PHY. 0: disabled 1: enabled
[13]	-	reserved	Reserved.
[12]	RW	port_pwr_en	USB PHY power shutdown control. 0: The power is shut down. 1: The controller power output is enabled.
[11:10]	-	reserved	Reserved.
[9]	RW	ss_ena_incr16_i	AHB burst 16 enable. 0: disabled 1: enabled (default)
[8]	RW	ss_ena_incr8_i	AHB burst 8 enable. 0: disabled 1: enabled (default)

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[7]	RW	ss_ena_incr4_i	AHB burst 4 enable. 0: disabled 1: enabled (default)
[6]	RW	ss_ena_incr_align_i	Burst alignment enable. 0: disabled (default) 1: enabled
[5]	RW	ss_autoppd_on_overcur_en_i	Automatic port power shutdown enable during over-current. 0: disabled 1: enabled (default)
[4:3]	-	reserved	Reserved.
[2]	RW	app_start_clk_i	Open host controller interface (OHCI) clock control. 0: The OHCI works normally (default value). 1: The OHCI clock is enabled in suspend mode.
[1]	RW	ohci_susp_lgcy_i	Strap input signal when the OHCI is suspended.
[0]	RW	ss_word_if_i	Data bit width select for the UTMI interface. 0: 8 bits (default) 1: 16 bits

MISC_CTRL50

MISC_CTRL50 is audio CODEC control register 0.

Offset Address	Register Name	Total Reset Value
0x00C8	MISC_CTRL50	0xFCCC_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd_adcl	pd_adcr	pd_dacl	pd_dacr	pd_micbias	pd_vref	reserved	ana_loop	mute_dacl	mute_dacr	reserved		mute_adcl	mute_adcr	reserved	reserved	gain_micl						gainboostl	reserved	gain_micr				gainboostr	reserved		
Reset	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pd_adcl	ADCL power-off control. 0: normal mode 1: powered off

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[30]	RW	pd_adcr	ADCR power-off control. 0: normal mode 1: powered off
[29]	RW	pd_dacl	DACL power-off control. 0: normal mode 1: powered off
[28]	RW	pd_dacr	DACR power-off control. 0: normal mode 1: powered off
[27]	RW	pd_micbias	Microphone bias circuit power-off control. 0: normal mode 1: powered off
[26]	RW	pd_vref	Reference voltage power-off control. 0: normal mode 1: powered off
[25]	RO	reserved	Reserved
[24]	RW	ana_loop	Analog loopback control. 0: normal mode 1: analog loopback mode
[23]	RW	mute_dacl	DACL analog mute. 0: normal mode 1: muted
[22]	RW	mute_dacr	DACR analog mute. 0: normal mode 1: muted
[21:20]	RO	reserved	Reserved
[19]	RW	mute_adcl	ADCL analog mute. 0: normal mode 1: muted
[18]	RW	mute_adcr	ADCR analog mute. 0: normal mode 1: muted
[17]	RO	reserved	Reserved. This bit is fixed at 1.
[16:15]	RO	reserved	Reserved. This bit is fixed at 0.

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[14:10]	RW	gain_micl	LINEINL input gain control. The gain is calculated as follows: [(gain_micl) x 1.5 − 16.5] dB 00000: -16.5db 00001: -15db 00010: -13.5db 00011: -12db 00100: -10.5db 00101: -9db 00110: -7.5 00111: -6db 01000: -4.5db 01001: -3db 01010: -1.5db 01011: 0db 01100: 1.5db 01101: 3db 01110: 4.5db 01111: 6db 10000: 7.5db 10001: 9db 10010: 10.5db 10011: 12db 10100: 13.5db 10101: 15db 10110: 16.5db 10111: 18db 11000: 19.5db 11001: 21db 11010: 22.5db 11011: 24db 11100: 25.5db 11101: 27db 11110: 28.5db 11111: 30db
[9]	RW	gainboostl	LINEINL gain BOOST control. 0: 0 dB 1: 26 dB
[8:7]	RO	reserved	Reserved. This bit is fixed at 0.

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[6:2]	RW	gain_micr	LINEINR input gain control. The gain is calculated as follows: [(gain_micr) x 1.5 − 16.5] dB 00000: -16.5db 00001: -15db 00010: -13.5db 00011: -12db 00100: -10.5db 00101: -9db 00110: -7.5 00111: -6db 01000: -4.5db 01001: -3db 01010: -1.5db 01011: 0db 01100: 1.5db 01101: 3db 01110: 4.5db 01111: 6db 10000: 7.5db 10001: 9db 10010: 10.5db 10011: 12db 10100: 13.5db 10101: 15db 10110: 16.5db 10111: 18db 11000: 19.5db 11001: 21db 11010: 22.5db 11011: 24db 11100: 25.5db 11101: 27db 11110: 28.5db 11111: 30db
[1]	RW	gainboostr	LINEINR gain boost control. 0: 0 dB 1: 26 dB
[0]	RO	reserved	Reserved. This bit is fixed at 0.

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MISC_CTRL51

MISC_CTRL51 is audio CODEC control register 1.

Offset Address	Register Name	Total Reset Value
0x00CC	MISC_CTRL51	0x00F3_5A4A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_rst_n	dacr_rst_n	adcl_rst_n	adcr_rst_n	dacl_en	dacr_en	adcl_en	adcr_en	reserved						i2s_fs_sel					reserved												rst
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[31]	RW	dacl_rst_n	DACL reset. 0: valid 1: invalid
[30]	RW	dacr_rst_n	DACR reset. 0: valid 1: invalid
[29]	RW	adcl_rst_n	ADCL reset. 0: valid 1: invalid
[28]	RW	adcr_rst_n	ADCR reset. 0: valid 1: invalid
[27]	RW	dacl_en	DACL enable. 0: disabled 1: enabled
[26]	RW	dacr_en	DACR enable. 0: disabled 1: enabled
[25]	RW	adcl_en	ADCL enable. 0: disabled 1: enabled
[24]	RW	adcr_en	ADCR enable. 0: disabled 1: enabled
[23:18]	RO	reserved	Reserved.

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[17:13]	RW	i2s_fs_sel	Sampling rate of I^2S channel. 00000: 8 kHz, 16.896 MHz mclk 00001: 16 kHz, 16.896 MHz mclk 00010: 32 kHz, 16.896 MHz mclk 00011: 64 kHz, 16.896 MHz mclk 001xx: 128 kHz, 16.896 MHz mclk 01000: 11 kHz, 16.896 MHz mclk 01001: 22 kHz, 16.896 MHz mclk 01010: 44 kHz, 16.896 MHz mclk 01011: 88 kHz, 16.896 MHz mclk 011xx: 176 kHz, 16.896 MHz mclk 10000: 12 kHz, 16.896 MHz mclk 10001: 24 kHz, 16.896 MHz mclk 10010: 48 kHz, 16.896 MHz mclk 10011: 96 kHz, 16.896 MHz mclk 101xx: 192 kHz, 16.896 MHz mclk 11000: mclk/512/2 11001: mclk/256/2 11010: mclk/128/2 11011: mclk/64/2 111xx: mclk/32/2
[12:1]	RO	reserved	Reserved.
[0]	RW	rst	Analog circuit reset. 0: normal mode 1: reset

MISC_CTRL52

MISC_CTRL52 is audio CODEC control register 2.

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Offset Address	Register Name	Total Reset Value
0x00D0	MISC_CTRL52	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smutel	smuter	sunmutel	sunmuter	dacvu	mutel_rate			muter_rate				reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	smutel	DACL soft mute control. 0: disabled 1: enabled
[30]	RW	smuter	DACR soft mute control. 0: disabled 1: enabled
[29]	RW	sunmutel	DACL soft mute control. 0: disabled 1: enabled
[28]	RW	sunmuter	DACR soft mute control. 0: disabled 1: enabled
[27]	RW	dacvu	DAC volume update control. 0: not updated 1: updated
[26:25]	RW	mutel_rate	DACL soft mute rate control. 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[24:23]	RW	muter_rate	DACR soft mute rate control. 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[22:0]	RO	reserved	Reserved.

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MISC_CTRL53

MISC_CTRL53 is audio CODEC control register 3.

Offset Address	Register Name	Total Reset Value
0x00D4	MISC_CTRL53	0x0606_2424

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_mute	dacl_vol							dacr_mute	dacr_vol							reserved															
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	dacl_mute	DACL digital mute control. 0: normal mode 1: muted
[30:24]	RW	dacl_vol	DACL digital volume control. The volume is calculated as follows: (6 − dacl_vol x 1) dB 0x00: 6dB 0x01: 5dB 0x02: 4dB … 0x7E: -120dB; When dacl_vol is 0x7F, the DACL is muted.
[23]	RW	dacr_mute	DACR digital mute control. 0: normal mode 1: muted
[22:16]	RW	dacr_vol	DACR digital volume control. The volume is calculated as follows: (6 − dacr_vol x 1) dB 0x00: 6dB 0x01: 5dB 0x02: 4dB … 0x7E: -120dB; When dacr_vol is 0x7F, the DACR is muted.
[15:0]	RO	reserved	Reserved.

MISC_CTRL54

MISC_CTRL54 is audio CODEC control register 4.

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Offset Address	Register Name	Total Reset Value
0x00D8	MISC_CTRL54	0x1E1E_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adcl_mute	adcl_vol							adcr_mute	adcr_vol							adcl_hpf_en	adcr_hpf_en	reserved													
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	adcl_mute	ADCL digital mute control. 0: unmuted 1: muted
[30:24]	RW	adcl_vol	ADCL volume control. The volume is calculated as follows: (30 − adcl_vol x 1) dB 00: 30dB 01: 29dB 02: 28dB … 7E: -96dB 7F: -97dB
[23]	RW	adcr_mute	ADCR digital mute control. 0: unmuted 1: muted
[22:16]	RW	adcr_vol	ADCR volume control. The volume is calculated as follows: (30 − adcr_vol x 1) dB 00: 30dB 01: 29dB 02: 28dB … 7E: -96dB 7F: -97dB
[15]	RW	adcl_hpf_en	ADCL high-pass filter enable. 0: disabled 1: enabled
[14]	RW	adcr_hpf_en	ADCR high-pass filter enable. 0: disabled 1: enabled
[13:0]	RO	reserved	Reserved.

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MISC_CTRL56

MISC_CTRL56 is MISC register 56.

Offset Address	Register Name	Total Reset Value
0x00E0	MISC_CTRL56	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														i2s_pad_enable	audio_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RW	i2s_pad_mclk_sel	mclk selection control for the chip I^2S interface. 0: aio_i2s_rx_mclk 1: aio_i2s_tx_mclk
[2]	RO	reserved	Reserved.
[1]	RW	i2s_pad_enable	Enable for the channel between the I^2S interface of the chip and AIO. 0: The channel between the I^2S interface of the chip and AIO is disabled, and the I^2S interface of the chip has no output. 1: The channel between the I^2S interface of the chip and AIO is enabled, and the I^2S interface of the chip connects to the I^2S interface of the AIO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.
[0]	RW	audio_enable	Enable for the channel between the I^2S interface of the internal audio CODEC and AIO. 0: The channel between the I^2S interface of the internal audio CODEC and AIO is disabled, and the I^2S interface of the internal audio CODEC has no output. 1: The channel between the I^2S interface of the internal audio CODEC and AIO is enabled, and the I^2S interface of internal audio CODEC connects to the I^2S interface of the AIO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.

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3.6 DMA Controller

3.6.1 Overview

The direction memory access (DMA) operation is a high-speed data transfer operation. It supports data read/write between peripherals and memories without using the CPU. The direction memory access controller (DMAC) directly transfers data between a memory and a peripheral, between peripherals, or between memories. This avoids the CPU intervention and reduces the interrupt handling overhead of the CPU.

3.6.2 Features

The DMAC has the following features:

- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides four DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports the DMA requests controlled through software.
- Programs the DMA burst size.
- Configures the source address and the destination address as automatic incremental or decremented addresses during DMA transfer.
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.

3.6.3 Function Description

Functional Block Diagram

Figure 3-6 shows the functional block diagram of the DMAC.

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Figure 3-6 Functional block diagram of the DMAC

NOTE

- The priorities of DMAC channels are fixed. DMA channel 0 has the highest priority; whereas channel 3 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- DMA channel 0 and DMA channel 1 have one 4 x 32-bit FIFO each, and DMA channel 2 and DMA channel 3 have one 16 x 32-bit FIFO each.

Each DMA channel has a group of transfer control logic and one FIFO. The transfer control logic automatically performs the following operations:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer data in the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

----End

Workflow

The workflow of the DMAC is as follows:

Step 1 The software selects one DMA channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Header pointer of the linked list
- Amount of the transferred data
- Source and destination peripheral request signal numbers

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- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request lines of the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then the DAMC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 5 The DMA channel responds to the DMA request of the destination device. Then the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

Step 6 The steps 2 and step 3 as well as step 4 and 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, step 2 to step 5 are performed repeatedly until the specified data is completely transferred and a maskable transfer terminal interrupt is sent. If the value of DMAC_Cn_LLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the read values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_Cn_LLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-6), and then go to step 2. If the value of DMAC_Cn_LLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

----End

Figure 3-7 illustrates how to update channel registers through the LLI.

Figure 3-7 Updating channel registers through the LLI

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Connection Between the DMA and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides the following two DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preconfigured.
- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC provides a request clear signal DMACLR.

This signal is sent to each peripheral by the DMAC as a response to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-11 describes the mapping between DMAC hardware request signals and devices.

Table 3-11 DMAC hardware request signals and corresponding peripheral requests

DMAC Hardware Request Signal No.	Device Request
0	DMA request of the I^2C1/I^2C0 RX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
1	DMA request of the I^2C1/I^2C0 TX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
2	DMA request of the I^2C1/I^2C2 RX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
3	DMA request of the I^2C1/I^2C2 TX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
4	DMA request of the UART0 RX channel
5	DMA request of the UART0 TX channel
6	DMA request of the UART1 RX channel
7	DMA request of the UART1 TX channel
8	DMA request of the UART2 RX channel
9	DMA request of the UART2 TX channel
10	DMA request of the UART3 RX channel
11	DMA request of the UART3 TX channel
12	DMA request of the I^2C1/SSP1 RX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])

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DMAC Hardware Request Signal No.	Device Request
13	DMA request of the I^2C1/SSP1 TX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
14	DMA request of the I^2C1/SSP0 RX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])
15	DMA request of the I^2C1/SSP0 TX channel (for details about the configuration, see MISC_CTRL1[i2c1_dma_ch_sel])

The source and destination requests of each DMA channel are configured by software. For example, DMA request 4 is the request of the UART0 RX channel. To transmit the UART0 RX data by using channel 3, you must configure DMA request 4 as the source request of channel 3.

As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 2 or channel 3. In this way, the master with a higher priority channel can transfer data on the bus first. Therefore, to prevent other channels from waiting for the bus for a long time, you are advised to transmit data from memory to memory using channel 2 or channel 3.

DMA Linked List

The data structure of the DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address for the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address for the destination device
- Channel register DMAC_Cn_LLI, for setting the address for the next node
- Channel register DMAC_Cn_CONTROL, for setting the master, data width, burst size, address increment, and transfer size of the source device and destination device

Figure 3-8 Structure of DMAC LLIs

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CAUTION

The LLI field value must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a consecutive address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after data blocks corresponding to the current node are transferred.

3.6.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMA channels are idle and there is no DMA transfer request.
- DMAC_Cn_CONFIG[ch_en] is set to 0 and all the DMA channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG[ch_en] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG [dmac_enable] to disable the DMAC.

Step 3 Write 0 to PERI_CRG54 [dma_cken] to disable DMAC bus clock gating. Then the DMAC clock is disabled.

Step 4 Enable the clock and the DMAC again when the DMAC is required for data transfer.

----End

Initialization

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endianness of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[dmac_enable] to enable the DMAC.

Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupts.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable channels in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG[ch_en] of each channel.

----End

Enabling a Channel

After the DMAC is initialized, the DMAC can transmit data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

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Step 1 Read DMAC_ENABLED_CHNS to search for idle channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Write to DMAC_Cn_SRC_ADDR to set the access start address for the source device.

Step 4 Write to DMAC_Cn_DEST_ADDR to set the access start address for the destination device.

Step 5 Write to DMAC_Cn_LLI to set the linked list information. If the channel is used for single-block data transfer, set DMAC_Cn_LLI to 0. If the channel is used for linked list data transfer, set DMAC_Cn_LLI to the linked list header pointer.

Step 6 Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.

Step 7 Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel.

Step 8 Write 1 to DMAC_Cn_CONFIG[ch_en] to enable this channel.

----End

Usage of DMAC_Cn_CONTROL

The DMAC_Cn_CONTROL register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register value is updated when being loaded from an LLI node after a complete data block is transferred.

If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. As a result, the register can be read after the channel stops data transfer.

Table 3-12 lists the mapping between the value of dbsize or sbsize of DMAC_Cn_CONTROL and the burst length.

Table 3-12 Mapping between the value of dbsize or sbsize and the burst length

Value of bsize or sbSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

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Table 3-13 describes mapping between the value of dwidth or swidth of DMAC_Cn_CONTROL and the transfer data width.

Table 3-13 Mapping between the value of dwidth or swidth and the transfer bit width

Value of swidth or dwidth	Transfer Bit Width
000	Byte (8 bits)
001	Halfword (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- swidth and dwidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Never conduct common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and read value may be the same. During the write operation, this field serves as a control register, because it determines the number of data segments transferred by the DMAC. During the read operation, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.
- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO but not the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-incremental mode. Otherwise, the peripheral FIFO may overflow.

The bus access information is provided for the source device or destination device over the master interface signals during data transfer. Such information is related to the bits DMAC_Cn_CONTROL[prot_stat] and DMAC_Cn_CONFIG[ch_lock] that are configured by programming channel registers. Table 3-14 describes the three protection bits of the prot field of DMAC_Cn_CONTROL.

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Table 3-14 Definitions of the prot_stat field of DMAC_Cn_CONTROL

Bits	Description	Purpose
[2]	Cacheable or noncacheable	Indicates whether the access is cacheable. 0: noncacheable 1: cacheable For example, this bit can notify an advanced microcontroller bus architecture (AMBA) bridge of the following information: When finding the first read operation of the 8-digit burst, this bridge can originate one 8-digit burst read operation on the destination bus directly instead of transmitting the read operations on the source bus to the destination bus one by one. This bit controls the output of the bus signal HPROT[3].
[1]	Bufferable or nonbufferable	Indicates whether the access is bufferable. 0: nonbufferable 1: bufferable For example, this bit is used to notify an AMBA bridge that the write operation on the source bus can be complete without waiting. That is, the operation can be performed even when the bridge does not arbitrate the operation to the destination bus and the slave device does not receive data completely. This bit controls the output of the bus signal HPROT[2].
[0]	Privileged or User	Access mode. 0: user mode 1: privileged mode This bit controls the output of the bus signal HPROT[1].

NOTE

AMBA: Advanced Microcontroller Bus Architecture

Usage of DMAC_Cn_CONFIG

Table 3-15 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-15 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC

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100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Interrupt Handling

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is handled as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels initiate interrupt requests at the same time, the interrupt request with the highest priority is handled first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a transfer terminal interrupt. If the value is 1, the interrupt is a transfer terminal interrupt. In this case, go to step 4; otherwise, go to step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to step 5; otherwise, end the operation.

Step 4 Handle the transfer terminal interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.
2. Fetch or use up the data buffered in the memory. If necessary (for example, you need to create a buffer in the memory), configure and enable the channel again.
3. End interrupt handling.

Step 5 Handle the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.
2. Provide the error information. If necessary, configure and enable the channel again.
3. End interrupt handling.

----End

3.6.5 Register Summary

NOTE

The *n* in the offset addresses for DMA registers indicates the DMA channel and its value range is 0−3.

Table 3-16 describes the DMAC registers.

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Table 3-16 Summary of the DMAC registers (base address: 0x1006_0000)

Offset Address	Register	Description	Page
0x0000	DMAC_INT_STAT	DMAC interrupt status register	3-124
0x0004	DMAC_INT_TC_STAT	DMAC transfer terminal interrupt status register	3-124
0x0008	DMAC_INT_TC_CLR	DMAC transfer terminal interrupt clear register	3-125
0x000C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-127
0x0010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-128
0x0014	DMAC_RAW_INT_TC_STAT	DMAC raw transfer terminal interrupt status register	3-129
0x0018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-130
0x001C	DMAC_ENABLED_CHNS	DMAC channel enable status register	3-131
0x0020	DMAC_SOFT_BREQ	DMAC software burst transfer request register	3-131
0x0024	DMAC_SOFT_SREQ	DMAC software single transfer request register	3-132
0x0028	DMAC_SOFT_LBREQ	DMAC software last burst request register	3-133
0x002C	DMAC_SOFT_LSREQ	DMAC software last single request register	3-133
0x0030	DMAC_CONFIG	DMAC configuration register	3-134
0x0034	DMAC_SYNC	DMAC request line sync enable register	3-135
0x0100 + *n* x 0x20	DMAC_Cn_SRC_ADDR	Source address register of DMA channel *n* (*n* = 0−3)	3-135
0x0104 + *n* x 0x20	DMAC_Cn_DEST_ADDR	Destination address register of DMA channel *n* (*n* = 0−3)	3-136
0x0108 + *n* x 0x20	DMAC_Cn_LLI	LLI information register of DMA channel *n* (*n* = 0−3)	3-136
0x010C + *n* x 0x20	DMAC_Cn_CONTROL	Control register of DMA channel *n* (*n* = 0−3)	3-137
0x110 + *n* x 0x20	DMAC_Cn_CONFIG	Configuration register of DMA channel *n* (*n* = 0−3)	3-140

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3.6.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	DMAC_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_stat	ch2_int_stat	ch1_int_stat	ch0_int_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_int_stat	Masked interrupt status of channel 3. 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[2]	RO	ch2_int_stat	Masked interrupt status of channel 2. 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[1]	RO	ch1_int_stat	Masked interrupt status of channel 1. 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[0]	RO	ch0_int_stat	Masked interrupt status of channel 0. 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is a DMAC transfer terminal interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x0004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_stat	ch2_int_tc_stat	ch1_int_tc_stat	ch0_int_tc_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_int_tc_stat	Status of the masked transfer terminal interrupt of channel 3. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_tc_stat	Status of the masked transfer terminal interrupt of channel 2. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_tc_stat	Status of the masked transfer terminal interrupt of channel 1. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_tc_stat	Status of the masked transfer terminal interrupt of channel 0. 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a DMAC transfer terminal interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x0008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_clr	ch2_int_tc_clr	ch1_int_tc_clr	ch0_int_tc_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	WO	ch3_int_tc_clr	Transfer terminal interrupt clear for channel 3. 0: not cleared 1: cleared
[2]	WO	ch2_int_tc_clr	Transfer terminal interrupt clear for channel 2. 0: not cleared 1: cleared
[1]	WO	ch1_int_tc_clr	Transfer terminal interrupt clear for channel 1. 0: not cleared 1: cleared
[0]	WO	ch0_int_tc_clr	Transfer terminal interrupt clear for channel 0. 0: not cleared 1: cleared

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DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is a DMAC error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_stat	ch2_int_err_stat	ch1_int_err_stat	ch0_int_err_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_int_err_stat	Status of the masked error interrupt of channel 3. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_err_stat	Status of the masked error interrupt of channel 2. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_err_stat	Status of the masked error interrupt of channel 1. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_err_stat	Status of the masked error interrupt of channel 0. 0: No interrupt is generated. 1: An interrupt is generated.

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DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is a DMAC transfer error interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_clr	ch2_int_err_clr	ch1_int_err_clr	ch0_int_err_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	WO	ch3_int_err_clr	Error interrupt clear for channel 3. 0: not cleared 1: cleared
[2]	WO	ch2_int_err_clr	Error interrupt clear for channel 2. 0: not cleared 1: cleared
[1]	WO	ch1_int_err_clr	Error interrupt clear for channel 1. 0: not cleared 1: cleared
[0]	WO	ch0_int_err_clr	Error interrupt clear for channel 0. 0: not cleared 1: cleared

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DMAC_RAW_INT_TC_STAT

DMAC_RAW_INT_TC_STAT is a DMAC raw transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	DMAC_RAW_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_tc	ch2_raw_int_tc	ch1_raw_int_tc	ch0_raw_int_tc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_raw_int_tc	Status of the raw transfer terminal interrupt of channel 3. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_tc	Status of the raw transfer terminal interrupt of channel 2. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_tc	Status of the raw transfer terminal interrupt of channel 1. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_tc	Status of the raw transfer terminal interrupt of channel 0. 0: No interrupt is generated. 1: An interrupt is generated.

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DMAC_RAW_INT_ERR_STAT

DMAC_RAW_INT_ERR_STAT is a DMAC raw error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	DMAC_RAW_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_err	ch2_raw_int_err	ch1_raw_int_err	ch0_raw_int_err
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_raw_int_err	Status of the raw error interrupt of channel 3. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_err	Status of the raw error interrupt of channel 2. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_err	Status of the raw error interrupt of channel 1. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_err	Status of the raw error interrupt of channel 0. 0: No interrupt is generated. 1: An interrupt is generated.

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DMAC_ENABLED_CHNS

DMAC_ENABLED_CHNS is a DMAC channel enable status register.

Offset Address	Register Name	Total Reset Value
0x001C	DMAC_ENABLED_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_enabled	ch2_enabled	ch1_enabled	ch0_enabled
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	ch3_enabled	Channel 3 enable. 0: disabled 1: enabled
[2]	RO	ch2_enabled	Channel 2 enable. 0: disabled 1: enabled
[1]	RO	ch1_enabled	Channel 1 enable. 0: disabled 1: enabled
[0]	RO	ch0_enabled	Channel 0 enable. 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMAC software burst transfer request register.

Software controls the generation of a DMA burst transfer request by using this register.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral can generate a DMA request each.

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Offset Address	Register Name	Total Reset Value
0x0020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	soft_breq	Controls whether to generate a DMA burst transfer request. When this register is written: 0: No effect. 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not send any DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting the DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMAC software single transfer request register.

Software controls the generation of DMA single transfer requests by using this register.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	soft_sreq	Controls whether to generate a DMA single transfer request. When this register is written: 0: No effect. 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

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			When this register is read: 0: The peripheral corresponding to the request signal DMACSREQ[15:0] does not send a DMA single request. 1: The peripheral corresponding to the request signal DMACSREQ[15:0] is requesting the DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMAC software last burst request register.

Software controls the generation of the DMA last burst transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x0028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	soft_lbreq	Last burst request issued by the software. 0: No effect. 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMAC software last single transfer request register.

Software controls the generation of the DMA last single transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x002C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	soft_lsreq	Last single transfer request issued by the software. 0: No effect. 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2_endianness	m1_endianness	dmac_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	m2_endianness	Byte endianness of master 2. 0: little endian 1: big endian
[1]	RW	m1_endianness	Byte endianness of master 1. 0: little endian 1: big endian
[0]	RW	dmac_enable	DMA enable. 0: disabled 1: enabled

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DMAC_SYNC

DMAC_SYNC is a DMAC request line sync enable register.

Offset Address	Register Name	Total Reset Value
0x0034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	dmac_sync	Controls whether to synchronize the request signals. 0: The sync logic provided for the DMA request signals of the corresponding peripheral is enabled. 1: The sync logic provided for the DMA request signals of the corresponding peripheral is disabled.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a source address register of DMA channel *n* (*n* = 0–3).

Its offset address is 0x100 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0100 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address.

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DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x104 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register contains the destination address for the data to be transferred. Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- Destination address increment.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0104 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address.

DMAC_Cn_LLI

DMAC_Cn_LLI is an LLI information register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x108 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3. For details, see section "DMA Linked List."

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Offset Address	Register Name	Total Reset Value
0x0108 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_LLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ll_item																														reserved	ll_master
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	ll_item	The bit[31:2] in the next LLI node address and the address bit[1:0] are set to 0. A linked list address must be 4-byte aligned.
[1]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[0]	RW	ll_master	Master for loading the next LLI node. 0: master 1 1: master 2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a control register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x10C + n x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

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Offset Address	Register Name	Total Reset Value
0x010C + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_tc_enable	prot_stat			dest_incr	src_incr	dest_select	src_select	dwidth				swidth				dbsize				sbsize				trans_size							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_tc_enable	Transfer terminal interrupt enable. This bit determines whether the current LLI node triggers a transfer terminal interrupt. 0: do not trigger 1: trigger
[30:28]	RW	prot_stat	HPROT[2:0] access protection signal transmitted by the master.
[27]	RW	dest_incr	Destination address increment. 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	src_incr	Source address increment. 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	dest_select	Master for accessing the destination device. 0: master 1 1: master 2
[24]	RW	src_select	Master for accessing the source device. 0: master 1 1: master 2

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[23:21]	RW	dwidth	Transfer bit width of the destination device. The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of dwidth and the bit width, see Table 3-13.
[20:18]	RW	swidth	Transfer bit width of the source device. The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of swidth and the bit width, see Table 3-13.
[17:15]	RW	dbsize	Burst size of the destination device. It indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCxBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of dbsize and the transfer length, see Table 3-12.
[14:12]	RW	sbsize	Burst size of the source device. It indicates the amount of data to be transferred by the source device in a burst transfer, that is, the amount of transferred data when DMACCxBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of sbsize and the transfer length, see Table 3-12.
[11:0]	RW	trans_size	The DMA transfer size can be configured by writing to this register only when the DMAC is a flow controller. The field indicates the amount of data to be transferred by the source device. When this register is read, the amount of data transferred through the bus connected to the destination device is obtained. If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer stops.

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DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a configuration register of channel *n* (*n* = 0−3).

Its offset address is 0x110 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													ch_halt	ch_active	ch_lock	tc_int_msk	err_int_msk	flow_ctrl			reserved	dest_periph				reserved	src_periph				ch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[18]	RW	ch_halt	Halt bit. 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transmitted. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RW	ch_active	Active bit. 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	ch_lock	Lock bit. 0: Lock transfer on the bus is disabled. 1: Lock transfer on the bus is enabled.
[15]	RW	tc_int_msk	Transfer terminal interrupt mask. 0: The transfer terminal interrupts of the channel are masked. 1: The transfer terminal interrupts of the channel are not masked.

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[14]	RW	err_int_msk	Transfer error interrupt mask. 0: The error interrupts of the channel are masked. 1: The error interrupts of the channel are not masked.
[13:11]	RW	flow_ctrl	Flow control and transfer type. This field specifies the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-15.
[10]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[9:6]	RW	dest_periph	Destination device. The field is used to select a peripheral request signal as the request signal for the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[4:1]	RW	src_periph	Source device. This field is used to select a peripheral request signal as the request signal for the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	ch_en	Channel enable. The current status of the channel can be queried by reading this field or DMAC_ENABLED_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI node is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0, indicating that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. Before enabling a channel by setting this bit to 1, you must reinitialize the channel; otherwise, unexpected results may occur. When a channel is disabled by writing DMAC_Cn_CONFIG [ch_en], DMAC_Cn_CONFIG [ch_en] can be reset again only after the corresponding bit of DMAC_ENABLED_CHNS is 0. This is because the channel is not disabled immediately after the Channel Enable bit is cleared. The running delay during a bus burst operation also needs to be considered.

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3.7 Cipher

3.7.1 Overview

The cipher module supports data encryption and decryption by following the data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The cipher module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

3.7.2 Features

The cipher module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.
- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes respectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of electronic codebook (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST special 800-38a standard.
- Supports the operating modes of ECB, CBC, 1-/8-/64-CFB, and 1-/8-/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.
- Provides eight keys (fixed at 128 bits) configured by the key management module. The master CPU supports the write operation but not the read operation.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.
- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.

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- Supports data combination for multi-block channels. To be specific, if the remaining data in a linked list data block is insufficient to form an encryption/decryption block and the data block is not the last one to be processed, the remaining data is combined with the data in the next data block for encryption or decryption. This avoids data stuffing.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

3.7.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 3-9 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 3-9 3DES encryption of a 3-key operation and a 2-key operation

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Figure 3-10 shows the 3DES decryption of a 3-key operation and a 2-key operation.

Figure 3-10 3DES decryption of a 3-key operation and a 2-key operation

ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 3-11 shows the ECB mode of the AES and DES algorithms, and Figure 3-12 shows the ECB mode of the 3DES algorithm.

Figure 3-11 ECB mode of the AES and DES algorithms

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Figure 3-12 ECB mode of the 3DES algorithm

CBC Mode

In CBC mode, the encrypted input plain text block must be exclusively ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text. Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 3-13 shows the CBC mode of the AES and DES algorithms, and Figure 3-14 shows the CBC mode of the 3DES algorithm.

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Figure 3-13 CBC mode of the AES and DES algorithms

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Figure 3-14 CBC mode of the 3DES algorithm

CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 3-15 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 3-16 shows the s-bit CFB mode of the 3DES algorithm.

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Figure 3-15 S-bit CFB mode of the AES and DES algorithms

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Figure 3-16 S-bit CFB mode of the 3DES algorithm

OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

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Figure 3-17 shows the OFB mode of the AES algorithm.

Figure 3-17 OFB mode of the AES algorithm

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Figure 3-18 shows the s-bit OFB mode of the DES algorithm.

Figure 3-18 S-bit OFB mode of the DES algorithm

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Figure 3-19 shows the s-bit OFB mode of the 3DES algorithm.

Figure 3-19 S-bit OFB mode of the 3DES algorithm

CTR Mode

In CTR mode, different data segments are input to the cipher module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE

CTRn is obtained by using the accumulation count mode.

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Figure 3-20 shows the CTR mode of the AES algorithm.

Figure 3-20 CTR mode of the AES algorithm

3.7.4 Operating Mode

Single-Block Operation Process of the Cipher Module

The cipher module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

Step 3 Check whether encryption and decryption of channel 0 are complete in either of following ways:

- Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.
- Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete.

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Step 4 Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

---End

Multi-Block Operation Process of the Cipher Module

The cipher module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

---End

Figure 3-21 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 3-21 Structure of the linked list header of a multi-block encryption/decryption channel

The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is cipher control information.

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Figure 3-22 shows the bits of cas.

Figure 3-22 Bits of cas

- iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
- last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the cipher module is idle, the cipher clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The cipher module can be soft-reset by configuring the registers of the system controller.

3.7.5 Register Summary

Table 3-17 describes cipher registers.

NOTE

The variable *n* in the offset addresses indicates the channel ID and ranges from 1 to 7.

Table 3-17 Summary of cipher registers (base address: 0x100c_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	Cipher output register for channel 0 (for single-block encryption/decryption)	3-157
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the cipher module	3-158
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	3-158
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the cipher module	3-159

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Offset Address	Register	Description	Page
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	3-160
0x1004–0x1010	CHAN0_CIPHER_IVIN	Cipher VI block input register for channel 0	3-162
0x1014–0x1020	CHAN0_CIPHER_DIN	128-bit block input register of the cipher module	3-163
0x1000 + *n* x 0x80	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	3-164
0x1000 + *n* x 0x80 + 0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	3-164
0x1000 + *n* x 0x80 + 0x8	CHANn_IEMPTY_CNT	Processed data buffer count register for channel n in the input queue	3-165
0x1000 + *n* x 0x80+ 0xC	CHANn_INT_ICNTCFG	Input queue multi-packet interrupt threshold register for channel n	3-165
0x1000 + *n* x 0x80 + 0x10	CHANn_CIPHER_CTRL	Encryption/decryption control register for channel n	3-166
0x1000 + *n* x 0x80 + 0x14	CHANn_SRC_LST_SADDR	Input queue start address register for channel n	3-168
0x1000 + *n* x 0x80 + 0x18	CHANn_IAGE_TIMER	Input queue interrupt aging time configuration register for channel n	3-168
0x1000 + *n* x 0x80 + 0x3C	CHANn_OBUF_NUM	Output queue total depth register for channel n (linked list header count register)	3-169
0x1000 + *n* x 0x80 + 0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	3-169
0x1000 + *n* x 0x80 + 0x44	CHANn_OFULL_CNT	Processed data buffer count register for channel n in the output queue	3-170
0x1000 + *n* x 0x80 + 0x48	CHANn_INT_OCNTCFG	Output queue multi-packet interrupt threshold register for channel n	3-170
0x1000 + *n* x 0x80 + 0x4C	CHANn_DEST_LST_SADDR	Output queue start address register for channel n	3-170
0x1000 + *n* x 0x80 + 0x50	CHANn_OAGE_TIMER	Output queue interrupt aging time configuration register for channel n	3-171
0x1400	INT_STATUS	Interrupt status register	3-172
0x1404	INT_EN	Interrupt enable register	3-173
0x1408	INT_RAW	Raw interrupt status register	3-174
0x140C	RST_STATUS	Reset status indicator register	3-175

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Offset Address	Register	Description	Page
0x1410	CHAN0_CFG	Channel 0 configuration register	3-175

3.7.6 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is a cipher output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the cipher module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

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CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the cipher module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the cipher module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is an IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the cipher module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
  - CIPHER_KEY bit[191:128] indicates key 3.

  If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The cipher module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

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Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	Key input of the cipher module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is an encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the cipher module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

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Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder				key_sel			byte_seq	reserved				key_length				ivin_sel				width				alg_sel				mode				decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select. 0: keys configured by the CPU 1: keys generated by the key management module
[12]	RO	reserved	Reserved.
[11]	RO	reserved	Reserved.
[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN. 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

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[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is a cipher VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

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- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the cipher module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the cipher module.

Note the following points when configuring this register:

If channel 0 is selected for the single-block operation, this register needs to be configured.

- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

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Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the cipher module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is an input queue total depth register for channel *n* (*n* = 1–7). This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is a pending data buffer count register for channel *n* in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

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Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue.

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is a processed buffer count register for channel *n* in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue.

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is an input queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

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Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_icnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold.

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is an encryption/decryption control register for channel *n*.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight										reserved						key_adder			key_sel	byte_seq	ts_vld	key_length		reserved	width		alg_sel		mode		decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	weight	Weighted value of the current channel, in the unit of 64 bytes.
[21:17]	RO	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12:11]	RO	reserved	Reserved.

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[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RO	reserved	Reserved.
[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

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[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is an input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address for the input queue.

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is an input queue interrupt aging time configuration register for channel *n*. If an overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

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Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	iage_timer	Aging interrupt timer.

CHANn_OBUF_NUM

CHANn_OBUF_NUM is an output queue total depth register for channel *n*. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	obuf_num	Total depth of the output queue.

CHANn_OBUF_CNT

CHANn_OBUF_CNT is a pending data buffer count register for channel *n* in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue.

CHANn_OFULL_CNT

CHANn_OFULL_CNT is a processed buffer count register for channel *n* in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue.

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is an output queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold.

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is an output queue start address register for channel *n*. The address must be aligned by word.

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Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address for the output queue.

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is an output queue interrupt aging time configuration register for channel *n*. If an overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	oage_timer	Aging interrupt timer.

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INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7.
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6.
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5.
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4.
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3.
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2.
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1.
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0.
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7.
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6.
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5.
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4.
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3.
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2.
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1.
[0]	RO	reserved	Reserved.

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INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the cipher module.
[30:16]	RO	reserved	Reserved.
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7.
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6.
[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5.
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4.
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3.
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2.
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1.
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0.
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7.
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6.
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5.
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4.
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3.
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2.
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1.
[0]	RO	reserved	Reserved.

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INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	ch0_ibuf_raw	ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7.
[14]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6.
[13]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5.
[12]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4.
[11]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3.
[10]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2.
[9]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1.
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0.
[7]	RWC	ch7_ibuf_raw	Raw intput queue data interrupt for channel 7.
[6]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6.
[5]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5.
[4]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4.
[3]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3.
[2]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2.
[1]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1.
[0]	RO	reserved	Reserved.

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RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rst_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	rst_status	Reset status indicator of the cipher module. 0: The cipher module is being reset. 1: The cipher module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	ch0_busy	Status signal of channel 0.
[0]	RW	ch0_start	Encryption/Decryption start signal of channel 0.

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3.8 Timer

3.8.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The Hi3516A has four timers.

3.8.2 Features

Timer has the following features:

- Provides 16-bit or 32-bit down counter that has a programmable 8-bit prescaler.
- Provides a configurable count clock, that is, the clock can serve as the 50 MHz bus clock or 3 MHz crystal oscillator clock.
- Supports three count modes: free-running mode, periodic mode, and one-shot mode.
- Loads the initial value through either of the following registers: TIMERx_LOAD and TIMERx_BGLOAD.
- Reads the current count value at any time.
- Generates an interrupt when the count value is decreased to 0.

3.8.3 Function Description

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

  The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF. When the count length is 16 bits, the maximum value is 0xFFFF. In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.
- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from TIMERx_BGLOAD again and then continues to count.
- One-shot mode

  The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256. In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.

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- The count cycle in periodic mode can be set by writing TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of TIMERx_BGLOAD and starts to count.

3.8.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timer*X* (*X* ranges from 0 to 3), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the bus clock as the count clock, do as follows:

Step 1 Set **SC_CTRL** [timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 1 Set **SC_CTRL** [timeren0sel] to 0.

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Step 2 Initialize the timer and start to count.

----End

3.8.5 Register Summary

The timer module consists of four timers and each timer involves a group of registers. The four groups of registers have the same features except that their base addresses are different. The details about their base addresses are as follows:

- The base address of timer 0: 0x2000_0000.
- The base address of timer 1: 0x2000_0020.
- The base address of timer 2: 0x2001_0000.
- The base address of timer 3: 0x2001_0020.

NOTE

The value of *X* in timerX ranges from 0 to 3. The registers for timer 0 to timer 3 are the same. In this section, timer 0 registers are described as an example.

Table 3-18 Summary of timer registers

Offset Address	Register	Description	Page
0x000	TIMERx_LOAD	Initial count value register	3-178
0x004	TIMERx_VALUE	Current count value register	3-179
0x008	TIMERx_CONTROL	Control register	3-179
0x00C	TIMERx_INTCLR	Interrupt clear register	3-181
0x010	TIMERx_RIS	Raw interrupt status register	3-181
0x014	TIMERx_MIS	Masked interrupt status register	3-182
0x018	TIMERx_BGLOAD	Initial count value register in periodic mode	3-182

3.8.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is an initial count value register. It is used to set the initial count value of each timer. Each timer (timers 0–7) has one such register.

NOTE

- The minimum valid value written to TIMERx_LOAD is 1.
- When the value 0 is written to TIMERx_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOAD before the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of

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TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and T TIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer 0.

TIMERx_VALUE

TIMERx_VALUE is a current count value register. It shows the current value of the counter that is decremented. Each timer (timers 0–3) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer 0 that is decremented.

TIMERx_CONTROL

TIMERx_CONTROL is a control register. Each timer (timers 0–3) has one such register.

NOTE

When the periodic mode is selected, TIMERx_CONTROL[timermode] must be set to 1 and TIMERx_CONTROL[oneshot] must be set to 0.

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Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	timeren	Timer enable. 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode. 0: free-running mode 1: periodic mode
[5]	RW	intenable	TIMERx_RIS interrupt mask. 0: masked 1: not masked
[4]	RO	reserved	Reserved.
[3:2]	RW	timerpre	Prescaling factor configuration. 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select. 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select. 0: periodic mode or free-running mode 1: one-shot mode

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TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timers 0–3) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer 0.

TIMERx_RIS

TIMERx_RIS is a raw interrupt status register. Each timer (timers 0–3) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer0. 0: No interrupt is generated. 1: An interrupt is generated.

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TIMERx_MIS

TIMERx_MIS is a masked interrupt status register. Each timer (timers 0–3) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	timer0mis	Masked interrupt status of timer 0. 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is an initial count value register in periodic mode. Each timer (timers 0–3) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer 0. Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

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3.9 Watchdog

3.9.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.9.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.
- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

3.9.3 Function Description

Application Block Diagram

The system configures the parameter values of watchdog registers by using the system bus. The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the WDG_RSTN reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-23 shows the application block diagram of the watchdog.

Figure 3-23 Application block diagram of the watchdog

Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on

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the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal WDG_RSTN and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.
- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.9.4 Operating Mode

Configuring the Frequency of the Count Clock

The watchdog counting clock is a 3 MHz.

The count time T_{WDG} of the watchdog is calculated as follows: $T_{WDG} = Value_{WDG_LOAD} \times (1/f_{clk})$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The counting time of the watchdog counting clock ranges from 0s to 1400s.

Initializing the System

The watchdog counter stops counting after the system power-on reset. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

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Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

---End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

---End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.9.5 Register Summary

Table 3-19 describes watchdog registers.

Table 3-19 Summary of watchdog registers (base address: 0x2004_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-186
0x0004	WDG_VALUE	Current count value register	3-186
0x0008	WDG_CONTROL	Control register	3-186
0x000C	WDG_INTCLR	Interrupt clear register	3-187
0x0010	WDG_RIS	Raw interrupt register	3-187
0x0014	WDG_MIS	Masked interrupt status register	3-188
0x0C00	WDG_LOCK	Lock register	3-189

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3.9.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter.

WDG_VALUE

WDG_VALUE is a current count value register It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter.

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	resen	Output enable of the watchdog reset signal. 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal. 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog. 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write

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			permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.10 RTC

3.10.1 Overview

The RTC is used to display the time in real time and periodically generate alarms.

3.10.2 Features

The RTC has the following features:

- Provides a 40-bit counter. Of the 40 bits, 16 bits are for counting days, five bits are for counting hours, six bits are for counting minutes, six bits are for counting seconds, and the other seven bits are for counting 10 ms.
- Provides a 100 Hz count clock.
- Allows you to configure the initial count value.
- Allows you to configure the match value.
- Supports the timeout interrupt.
- Supports soft reset.
- Supports the fixed frequency-division mode.
- Automatically corrects the counting frequency based on the measured temperature.
- Provides the junction temperature of the position where the RTC is located.
- Stores user data in a 64-bit user register.

3.10.3 Function Description

The RTC has a 40-bit up counter for counting days, hours, minutes, seconds, and 10 ms. The initial values are loaded from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, and RTC_LR_D_H. This section assumes that the counter is divided into the day counter, hour counter, minute counter, second counter, and 10 ms counter. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt. Then, the counter continues to count in incremental mode on the rising edge of the next count clock.

By configuring RTC_IMSC, you can allow or forbid the RTC to generate interrupts. Note the following two cases:

- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MSC_INT shows the status of masked interrupts and RTC_RAW_INT shows the status of raw interrupts.

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- When the function of generating interrupts is enabled, the RTC counter still counts in incremental mode. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt.

The RTC uses a 100 Hz count clock and a 16-bit day counter. The value of the day counter can be used to reckon the specific year, month, and day.

3.10.4 Operating Mode

3.10.4.1 Count Clock Frequency

The RTC uses a 100 Hz count clock. The maximum RTC count time (T_{RTC}) is calculated as follows:

$T_{RTC} = 2^{16} = 65536$ days

NOTE

T_{RTC} is the RTC count time.

3.10.4.2 Soft Reset

The RTC can be separately soft-reset by configuring RTC_POR_N. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To soft-reset the RTC, perform the following steps:

Step 1 Write 0 to RTC_POR_N.

Step 2 Wait 30 ms.

----End

3.10.4.3 Initializing the RTC

The system needs to initialize the RTC when the RTC is powered on for the first time. The initialization process is as follows:

Step 1 Configure RTC_POR_N to reset the RTC.

Step 2 Wait 30 ms.

Step 3 Configure RTC_IMSC to set the interrupt mask bit of the RTC.

Step 4 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the RTC match value.

Step 5 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the initial count value of the RTC.

Step 6 Wait 5 ms.

Step 7 Set RTC_LORD to 1 to load the initial count value to the RTC counter.

Step 8 Based on the 100 Hz count clock, the RTC counts starting from the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H. When the count value is equal to the values of RTC_MR_10MS,

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RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC determines whether to generate an interrupt based on the settings of RTC_IMSC.

----End

3.10.4.4 Handling Interrupts

If the system receives an interrupt from the RTC, the configured time is reached. Then user-defined operations can be performed. The RTC counter, however, still counts in incremental mode. To clear an RTC interrupt, set RTC_INT_CLR to 1. To continue to configure time, write a new match value to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H.

3.10.4.5 Accessing RTC Registers

Internal RTC registers are located in the RTC module, not on the bus. The RTC registers on the bus are used only for accessing internal RTC registers.

To write to internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This example assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to write 0x10 to RTC_MR_10MS, write 0x01060010 to SPI_RW. That is, spi_start is 1, spi_rw is 0, spi_add is 0x06, and spi_wdata is 0x10.

----End

To read internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This step assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to read SPI_RW, write 0x01860000 to SPI_RW. That is, spi_start is 1, spi_rw is 0, and spi_add is 0x06.

Step 4 Read SPI_RW bit[31] until it is 0. SPI_RW [15:8] is the value that is returned after RTC_MR_10MS is read.

----End

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3.10.4.6 Automatically Correcting the Counting Frequency Based on the Temperature

The crystal output frequency changes when the temperature changes. The relationship between the temperature and the output frequency of a specific crystal is defined by configuring registers during RTC initialization. The temperature is measured and the temperature calculated by using the correction algorithm is written at intervals (such as 1 minute). This ensures that the RTC generates a 100 Hz clock for counting. When the RTC correction algorithm is used, the temperature can be the value of the internal t_sensor or the externally measured temperature. When the temperature obtained by the internal t_sensor is selected, the system reads the internal chip temperature from the internal t_sensor at an interval of 1 minute, 4 minutes, 8 minutes, or 16 minutes. The ambient temperature that is equal to the read temperature minus the experience deviation is written to the OUTSIDE_TEMP register. When the externally measured temperature is selected, you can use the successive approximation register analog-to-digital converter (SAR ADC) and temperature-sensitive resistors or you can use only the external temperature sensor DS1820 or DS18B20. In this case, the system must measure the temperature and write the value to the external temperature register in a period. As the temperature update period allowed by the RTC is 1 minute, 4 minute, 8 minutes, or 16 minutes, you are advised to set the temperature measurement period to 1 minute, 4 minute, 8 minutes, or 16 minutes.

CAUTION

When the chip is powered off, the chip temperature obtained by the internal t_sensor is the same as the ambient temperature. Therefore, you are advised to use the chip temperature obtained by the internal t_sensor as the input of the correction circuit. For details about how to select the temperature source, see the description of the register TEMP_SEL.

The following takes the external temperature sensor DS1820 as an example. To correct the counting frequency based on the temperature, perform the following steps:

Step 1 Set TEMP_SEL bit[1] to 0 and TEMP_SEL bit[0] to 1 to select an external temperature mode.

Step 2 Set RTC_SAR_CTRL[1:0] to 0 to set the temperature update period to 1 minute.

Step 3 Set INT_MASK to 0 to enable the temperature sensor measurement interrupt.

Step 4 Set CONVER_T to 1 to start the temperature measurement sensor.

Step 5 Wait until the temperature sensor measurement completion interrupt is generated.

Step 6 Set INT_CLEAR to 1 to clear the interrupt.

Step 7 Read T_VALUE and convert the temperature code words into the temperature code words supported by the t_sensor, and write the converted code words to

Step 8 OUTSIDE_TEMP.

Step 9 Wait 1 minute and repeat Step 4 to Step 9.

----End

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3.10.5 Register Summary

Table 3-20 describes RTC registers.

Table 3-20 Summary of RTC registers (base address: 0x2006_0000)

Offset Address	Register	Description	Page
0x0000	SPI_CLK_DIV	SPI clock divider register	3-198
0x0004	SPI_RW	SPI read/write register	3-199
0x0080	CONVER_T	External temperature sensor DS1820 (DS18B20) measurement control register	3-200
0x0084	CRC_EN	External temperature sensor DS1820 (DS18B20) measurement CRC check enable register	3-200
0x0088	INT_MASK	External temperature sensor DS1820 (DS18B20) measurement interrupt mask register	3-201
0x008C	INT_CLEAR	External temperature sensor DS1820 (DS18B20) measurement interrupt clear register	3-201
0x0090	BUSY	External temperature sensor DS1820 (DS18B20) measurement status register	3-202
0x0094	INT_RAW	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-202
0x0098	INT_TCAP	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-203
0x009C	T_VALUE	External temperature sensor DS1820 (DS18B20) measurement value register	3-203
0x00A0	FILTER_NUM	Filter glitch width configuration register	3-204

Table 3-21 describes the internal RTC registers.

Table 3-21 Summary of internal RTC registers (base address: 0x00)

Offset Address	Register	Description	Page
0x00	RTC_10MS_COUNT	Count value register for the RTC 10 ms counter	3-204
0x01	RTC_S_COUNT	Count value register for the RTC second counter	3-205

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Offset Address	Register	Description	Page
0x02	RTC_M_COUNT	Count value register for the RTC minute counter	3-205
0x03	RTC_H_COUNT	Count value register for the RTC hour counter	3-205
0x04	RTC_D_COUNT_L	Lower-8-bit count value register for the RTC day counter	3-206
0x05	RTC_D_COUNT_H	Upper-8-bit count value register for the RTC day counter	3-206
0x06	RTC_MR_10MS	Match value register for the RTC 10 ms counter	3-207
0x07	RTC_MR_S	Match value register for the RTC second counter	3-207
0x08	RTC_MR_M	Match value register for the RTC minute counter	3-208
0x09	RTC_MR_H	Match value register for the RTC hour counter	3-208
0x0A	RTC_MR_D_L	Lower-8-bit match value register for the RTC day counter	3-209
0x0B	RTC_MR_D_H	Upper-8-bit match value register for the RTC day counter	3-209
0x0C	RTC_LR_10MS	Configured value register for the RTC 10 ms counter	3-210
0x0D	RTC_LR_S	Configured value register for the RTC second counter	3-210
0x0E	RTC_LR_M	Configured value register for the RTC minute counter	3-211
0x0F	RTC_LR_H	Configured value register for the RTC hour counter	3-211
0x10	RTC_LR_D_L	Lower-8-bit configured value register for the RTC day counter	3-212
0x11	RTC_LR_D_H	Upper-8-bit configured value register for the RTC day counter	3-212
0x12	RTC_LORD	RTC configured value loading enable register	3-213
0x13	RTC_IMSC	RTC interrupt enable register	3-214
0x14	RTC_INT_CLR	RTC interrupt clear register	3-214
0x15	RTC_MSC_INT	RTC mask interrupt status register.	3-215
0x16	RTC_RAW_INT	RTC raw interrupt status register	3-215
0x17	RTC_CLK	RTC output clock select register	3-216
0x18	RTC_POR_N	RTC reset control register	3-216

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Offset Address	Register	Description	Page
0x1A	RTC_SAR_CTRL	RTC internal t_sensor control register	3-217
0x1B	RTC_ANA_CTRL	RTC_ANA_CTRL is an RTC analog startup circuit control register.	3-217
0x1C	TOT_OFFSET_L	Lower-8-bit corrected tot_offset register when the correction algorithm is used	3-218
0x1D	TOT_OFFSET_H	Upper-1-bit corrected tot_offset register when the correction algorithm is used	3-218
0x1E	TEMP_OFFSET	Temperature code word offset register corresponding to the correction input lookup table (LUT)	3-219
0x1F	OUTSIDE_TEMP	External ambient temperature register	3-219
0x20	DIE_TEMP	RTC internal t_sensor temperature register	3-219
0x21	TEMP_SEL	Correction algorithm input temperature source select register	3-220
0x22	LUT1	Temperature correction algorithm LUT1 register	3-222
0x23	LUT2	Temperature correction algorithm LUT2 register	3-222
0x24	LUT3	Temperature correction algorithm LUT3 register	3-222
0x25	LUT4	Temperature correction algorithm LUT4 register	3-223
0x26	LUT5	Temperature correction algorithm LUT5 register	3-223
0x27	LUT6	Temperature correction algorithm LUT6 register	3-223
0x28	LUT7	Temperature correction algorithm LUT7 register	3-224
0x29	LUT8	Temperature correction algorithm LUT8 register	3-224
0x2A	LUT9	Temperature correction algorithm LUT9 register	3-224
0x2B	LUT10	Temperature correction algorithm LUT10 register	3-225
0x2C	LUT11	Temperature correction algorithm LUT11 register	3-225
0x2D	LUT12	Temperature correction algorithm LUT12 register	3-225

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Offset Address	Register	Description	Page
0x2E	LUT13	Temperature correction algorithm LUT13 register	3-226
0x2F	LUT14	Temperature correction algorithm LUT14 register	3-226
0x30	LUT15	Temperature correction algorithm LUT15 register	3-226
0x31	LUT16	Temperature correction algorithm LUT16 register	3-227
0x32	LUT17	Temperature correction algorithm LUT17 register	3-227
0x33	LUT18	Temperature correction algorithm LUT18 register	3-227
0x34	LUT19	Temperature correction algorithm LUT19 register	3-228
0x35	LUT20	Temperature correction algorithm LUT20 register	3-228
0x36	LUT21	Temperature correction algorithm LUT21 register	3-228
0x37	LUT22	Temperature correction algorithm LUT22 register	3-229
0x38	LUT23	Temperature correction algorithm LUT23 register	3-229
0x39	LUT24	Temperature correction algorithm LUT24 register	3-229
0x3A	LUT25	Temperature correction algorithm LUT25 register	3-230
0x3B	LUT26	Temperature correction algorithm LUT26 register	3-230
0x3C	LUT27	Temperature correction algorithm LUT27 register	3-230
0x3D	LUT28	Temperature correction algorithm LUT28 register	3-231
0x3E	LUT29	Temperature correction algorithm LUT29 register	3-231
0x3F	LUT30	Temperature correction algorithm LUT30 register	3-231
0x40	LUT31	Temperature correction algorithm LUT31 register	3-232

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Offset Address	Register	Description	Page
0x41	LUT32	Temperature correction algorithm LUT32 register	3-232
0x42	LUT33	Temperature correction algorithm LUT33 register	3-232
0x43	LUT34	Temperature correction algorithm LUT34 register	3-233
0x44	LUT35	Temperature correction algorithm LUT35 register	3-233
0x45	LUT36	Temperature correction algorithm LUT36 register	3-233
0x46	LUT37	Temperature correction algorithm LUT37 register	3-234
0x47	LUT38	Temperature correction algorithm LUT38 register	3-234
0x48	LUT39	Temperature correction algorithm LUT39 register	3-234
0x49	LUT40	Temperature correction algorithm LUT40 register	3-235
0x4A	LUT41	Temperature correction algorithm LUT41 register	3-235
0x4B	LUT42	Temperature correction algorithm LUT42 register	3-235
0x4C	LUT43	Temperature correction algorithm LUT43 register	3-236
0x4D	LUT44	Temperature correction algorithm LUT44 register	3-236
0x4E	LUT45	Temperature correction algorithm LUT45 register	3-236
0x4F	LUT46	Temperature correction algorithm LUT46 register	3-237
0x50	LUT47	Temperature correction algorithm LUT47 register	3-237
0x51	SDM_COEF_OUSIDE_H	Upper-4-bit clock divider register in fixed frequency-division mode	3-237
0x52	SDM_COEF_OUSIDE_L	Lower-8-bit register clock divider register in fixed frequency-division mode	3-238
0x53	USER_REGISTER1	64-bit user register 1	3-238

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Offset Address	Register	Description	Page
0x54	USER_REGISTER2	64-bit user register 2	3-239
0x55	USER_REGISTER3	64-bit user register 3	3-239
0x56	USER_REGISTER4	64-bit user register 4	3-239
0x57	USER_REGISTER5	64-bit user register 5	3-240
0x58	USER_REGISTER6	64-bit user register 6	3-240
0x59	USER_REGISTER7	64-bit user register 7	3-240
0x5A	USER_REGISTER8	64-bit user register 8	3-241

3.10.6 RTC Register Description

SPI_CLK_DIV

SPI_CLK_DIV is an SPI clock divider register.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	spi_clk_div	SPI clock divider. The SPI clock frequency cannot be higher than 20 MHz. The value 12 MHz is recommended. The field value ranges from 1 to 255. The value of spi_clk_div is used to define the SPI RX and RX bit rates. The formula is as follows: FSPICLK = FAPBCLK/[2 x (spi_clk_div + 1)]. FAPBCLK is the clock frequency. If the clock is 120 MHz and the expected SPI clock is 12 MHz, the configured value of spi_clk_div is calculated as follows: (120/12)/2 – 1 = 4

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SPI_RW

SPI_RW is an SPI read/write register.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_busy	reserved							spi_start	spi_rw	spi_add						spi_rdata								spi_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	spi_busy	SPI read/write status indicator. 0: The SPI is idle, and a new read/write operation can be initiated over the SPI. 1: A read/write operation is being performed over the SPI, and no new operation is allowed.
[30:25]	RO	reserved	Reserved.
[24]	W1_PULSE	spi_start	SPI read/write start. Writing 1 automatically clears this field. Writing has no effect when spi_busy is 1. That is, no new SPI operation is started before the previous read/write operation is complete. If a start request is sent, hardware ignores this request.
[23]	RW	spi_rw	SPI operation type. 0: write 1: read
[22:16]	RW	spi_add	SPI operation address. The address range is 0–127.
[15:8]	RO	spi_rdata	Data read from the SPI.
[7:0]	RW	spi_wdata	Data to be written to the SPI.

CONVER_T

CONVER_T is an external temperature sensor DS1820 (DS18B20) measurement control register.

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Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															conver_t
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	conver_t	External temperature sensor DS1820 (DS18B20) measurement start. This field must be set to 1. 1: start. Hardware automatically sets this field to 0 when the interrupt is cleared.

CRC_EN

CRC_EN is an external temperature sensor DS1820 (DS18B20) measurement CRC check enable register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	crc_en	External temperature sensor DS1820 (DS18B20) measurement CRC check enable. 0: disabled 1: enabled

INT_MASK

INT_MASK is an external temperature sensor DS1820 (DS18B20) measurement interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	int_mask	External temperature sensor DS1820 (DS18B20) measurement interrupt mask. 0: not masked 1: masked

INT_CLEAR

INT_CLEAR is an external temperature sensor DS1820 (DS18B20) measurement interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	int_clear	External temperature sensor DS1820 (DS18B20) measurement interrupt clear. Writing 1 clears the interrupt. Hardware automatically sets this field to 0 after the interrupt is cleared.

BUSY

BUSY is an external temperature sensor DS1820 (DS18B20) measurement status register.

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Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	busy	External temperature sensor DS1820 (DS18B20) measurement status. 0: ready 1: busy

INT_RAW

INT_RAW is an external temperature sensor DS1820 (DS18B20) raw measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														int_err	get_tmprt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	int_err	Error interrupt.
[0]	RO	get_tmprt_int	External temperature sensor DS1820 (DS18B20) measurement completion interrupt.

INT_TCAP

INT_TCAP is an external temperature sensor DS1820 (DS18B20) measurement interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								int_tcap
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	int_tcap	Masked interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.

T_VALUE

T_VALUE is an external temperature sensor DS1820 (DS18B20) measurement value register.

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved					t_value			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	t_value	Temperature measured by the external temperature sensor DS1820 (DS18B20).

FILTER_NUM

FILTER_NUM is a filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								filter_num

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	filter_num	Filter glitch width for inputs. The glitch with the width of (N + 1) APB clocks is filtered.

3.10.7 Internal Register Description

RTC_10MS_COUNT

RTC_10MS_COUNT is a count value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved.
[6:0]	RO	rtc_10ms_count	RTC 10 ms counter value. It indicates the currently counted time. Its unit is 10 ms. The value range is 0–99.

RTC_S_COUNT

RTC_S_COUNT is a count value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_s_count					

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved.
[5:0]	RO	rtc_s_count	RTC second counter value. It indicates the currently counted seconds. The value range is 0–59.

RTC_M_COUNT

RTC_M_COUNT is a count value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_m_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved.
[5:0]	RO	rtc_m_count	RTC minute counter value. It indicates the currently counted minutes. The value range is 0–59.

RTC_H_COUNT

RTC_H_COUNT is a count value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved.

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[4:0]	RO	rtc_h_count	RTC hour counter value. It indicates the currently counted hours. The value range is 0–23.

RTC_D_COUNT_L

RTC_D_COUNT_L is a lower-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	Lower eight bits of the RTC day counter value. This field works with RTC_D_COUNT_H to indicate the currently counted days. The day range is 0–65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is an upper-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	Upper eight bits of the RTC day counter value. This field works with RTC_D_COUNT_L to indicate the currently counted day. The day range is 0–65535.

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RTC_MR_10MS

RTC_MR_10MS is a match value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RW	reserved	Reserved.
[6:0]	RW	rtc_mr_10ms	Match value of the RTC 10 ms counter. The value range is 0–99.

RTC_MR_S

RTC_MR_S is a match value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_mr_s	Match value of the RTC second counter. The value range is 0–59.

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RTC_MR_M

RTC_MR_M is a match value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_mr_m	Match value of the RTC minute counter. The value range is 0–59.

RTC_MR_H

RTC_MR_H is a match value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RW	reserved	Reserved.
[4:0]	RW	rtc_mr_h	Match value of the RTC hour counter. The value range is 0–23.

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RTC_MR_D_L

RTC_MR_D_L is a lower-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	Lower eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_H to indicate the matched day. The day range is 0–65535.

RTC_MR_D_H

RTC_MR_D_H is an upper-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	Upper eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_L to indicate the matched day. The day range is 0–65535.

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RTC_LR_10MS

RTC_LR_10MS is a configured value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	reserved	Reserved.
[6:0]	RW	rtc_lr_10ms	Configured value of the RTC 10 ms counter. The value range is 0–99.

RTC_LR_S

RTC_LR_S is a configured value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_s					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_lr_s	Configured value of the RTC second counter. The value range is 0–59.

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RTC_LR_M

RTC_LR_M is a configured value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_m					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_lr_m	Configured value of the RTC minute counter. The value range is 0–59.

RTC_LR_H

RTC_LR_H is a configured value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RW	reserved	Reserved.
[4:0]	RW	rtc_lr_h	Configured value of the RTC hour counter. The value range is 0–23.

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RTC_LR_D_L

RTC_LR_D_L is a lower-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_l	Lower eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_H to indicate the configured day. The day range is 0–65535.

RTC_LR_D_H

RTC_LR_D_H is an upper-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_h	Upper eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_L to indicate the configured day. The day range is 0–65535.

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RTC_LORD

RTC_LORD is an RTC configured value loading enable register.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_lock_bypass	rtc_lock	rtc_load
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	-	reserved	Reserved.
[2]	RW	rtc_lock_bypass	RTC lock enable. 0: enabled. The RTC count value (0x00−0x05) is updated only after the RTC is successfully locked. 1: disabled. The RTC count value (0x00−0x05) is updated in real time.
[1]	RW	rtc_lock	RTC lock. If software writes 1, hardware is automatically cleared after the RTC is successfully locked. Note: This field is valid only when rtc_lock_bypass is 0.
[0]	RW	rtc_load	RTC configured value loading enable. When the field is enabled, the RTC configured value will be loaded to the RTC accumulator. If software writes 1 to load the configured value, hardware will automatically set this field to 0 after successful loading.

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RTC_IMSC

RTC_IMSC is an RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_imsc
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RW	rtc_imsc	RTC timing interrupt enable. 0: disabled 1: enabled

RTC_INT_CLR

RTC_INT_CLR is an RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_int_clr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RW	rtc_int_clr	RTC timing interrupt clear. If software writes 1 to clear the interrupt, hardware will automatically set this field to 0 after the interrupt is successfully cleared.

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RTC_MSC_INT

RTC_MSC_INT is an RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							mask_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RO	mask_int	Mask interrupt status.

RTC_RAW_INT

RTC_RAW_INT is an RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							raw_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RO	raw_int	Raw interrupt status.

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RTC_CLK

RTC_CLK is an RTC output clock select register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						clk_out_sel	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved.
[1:0]	RW	clk_out_sel	Output test clock of the RTC. 00: output crystal oscillator clock 01: output corrected 100 Hz clock 1X: output 1 Hz clock

RTC_POR_N

RTC_POR_N is an RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_por_n
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RW	rtc_por_n	RTC reset. This field is automatically set to 1 after the RTC is successfully reset. 0: reset

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RTC_SAR_CTRL

RTC_SAR_CTRL is an RTC internal t_sensor control register.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_SAR_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						sample_time	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RW	reserved	Reserved.
[1:0]	RW	sample_time	Temperature update period 00: 1 minute 01: 4 minutes 10: 8 minutes 11: 16 minutes

RTC_ANA_CTRL

RTC_ANA_CTRL is an RTC analog startup circuit control register.

Offset Address	Register Name	Total Reset Value
0x1B	RTC_ANA_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						ana_ctrl	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved.
[1:0]	RW	ana_ctrl	Adjustment of the bias current of the RTC analog startup circuit.

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TOT_OFFSET_L

TOT_OFFSET_L is a lower-8-bit corrected tot_offset register when the correction algorithm is used.

Offset Address	Register Name	Total Reset Value
0x1C	TOT_OFFSET_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	tot_offset_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	tot_offset_l	Corrected tot_offset by using the correction algorithm. The value is expressed by complement codes –256 to +255. That is, tot_offset is 1990 + (–256 to +255) in the correction algorithm. This field value is the lower seven bits of tot_offset.

TOT_OFFSET_H

TOT_OFFSET_H is an upper-1-bit corrected tot_offset register when the correction algorithm is used.

Offset Address	Register Name	Total Reset Value
0x1D	TOT_OFFSET_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							tot_offset_h
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved.
[0]	RW	tot_offset_h	Corrected tot_offset by using the correction algorithm. The value is expressed by complement codes –256 to +255. That is, tot_offset is 1990 + (–256 to +255) in the correction algorithm. This field value is the upper one bit of tot_offset.

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TEMP_OFFSET

TEMP_OFFSET is a temperature code word offset register corresponding to the correction input LUT.

Offset Address	Register Name	Total Reset Value
0x1E	TEMP_OFFSET	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		temp_offset					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved.
[5:0]	RW	temp_offset	Offset of the temperature code words that are input to the correction LUT. The value is expressed by the complement code and the value ranges from –32 to +31.

OUTSIDE_TEMP

OUTSIDE_TEMP is an external ambient temperature register.

Offset Address	Register Name	Total Reset Value
0x1F	OUTSIDE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	outside_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	outside_temp	Ambient temperature. The code word indicates –40°C to +140°C.

DIE_TEMP

DIE_TEMP is an RTC internal t_sensor temperature register.

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Offset Address	Register Name	Total Reset Value
0x20	DIE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	die_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	die_temp	Internal chip temperature provided by the t_sensor in the RTC. The code word indicates –40°C to +140°C.

TEMP_SEL

TEMP_SEL is a correction algorithm input temperature source select register.

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Offset Address	Register Name	Total Reset Value
0x21	TEMP_SEL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					sdm_sel	fix_mode	temp_sel
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved.
[2]	RW	sdm_sel	Whether to perform temperature compensation. This field works with fix_model and temp_sel. When the chip is powered on or off: {sdm_sel, fix_mode, temp_sel} 0xx: temperature compensation enabled. The mode depends on {fix_mode, temp_sel}. 110: temperature compensation disabled. The RTC clock is obtained after decimal frequency division. For details about the frequency dividers, see the frequency divider registers with the offset addresses of 0x51 and 0x52. Other values: reserved
[1]	RW	fix_mode	Correction algorithm input temperature source select. This field works with temp_sel. For details, see descriptions of the temp_sel field.
[0]	RW	temp_sel	Correction algorithm input temperature source select. This field parameter works with fix_mode. When the chip is powered on, the value meanings for {fix_mode, temp_sel} are as follows: 00: The correction circuit temperature is read from the DIE_TEMP register. 01: The correction circuit temperature is read from the OUTSIDE_TEMP register. 1X: The correction circuit temperature is read from the OUTSIDE_TEMP register. When the chip is powered off, the value meanings for {fix_mode, temp_sel} are as follows: 0X: The correction circuit temperature is read from the DIE_TEMP register. 1X: The correction circuit temperature is read from the OUTSIDE_TEMP register.

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LUT1

LUT1 is a temperature correction algorithm LUT1 register.

Offset Address	Register Name	Total Reset Value
0x22	LUT1	0xAC

Bit	7	6	5	4	3	2	1	0
Name	lut1							
Reset	1	0	1	0	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut1	Temperature correction algorithm LUT1.

LUT2

LUT2 is a temperature correction algorithm LUT2 register.

Offset Address	Register Name	Total Reset Value
0x23	LUT2	0xB4

Bit	7	6	5	4	3	2	1	0
Name	lut2							
Reset	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut2	Temperature correction algorithm LUT2.

LUT3

LUT3 is a temperature correction algorithm LUT3 register.

Offset Address	Register Name	Total Reset Value
0x24	LUT3	0xBB

Bit	7	6	5	4	3	2	1	0
Name	lut3							
Reset	1	0	1	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut3	Temperature correction algorithm LUT3.

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LUT4

LUT4 is a temperature correction algorithm LUT4 register.

Offset Address	Register Name	Total Reset Value
0x25	LUT4	0xC2

Bit	7	6	5	4	3	2	1	0
Name	lut4							
Reset	1	1	0	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut4	Temperature correction algorithm LUT4.

LUT5

LUT5 is a temperature correction algorithm LUT5 register.

Offset Address	Register Name	Total Reset Value
0x26	LUT5	0xC8

Bit	7	6	5	4	3	2	1	0
Name	lut5							
Reset	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut5	Temperature correction algorithm LUT5.

LUT6

LUT6 is a temperature correction algorithm LUT6 register.

Offset Address	Register Name	Total Reset Value
0x27	LUT6	0xCF

Bit	7	6	5	4	3	2	1	0
Name	lut6							
Reset	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut6	Temperature correction algorithm LUT6.

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LUT7

LUT7 is a temperature correction algorithm LUT7 register.

Offset Address	Register Name	Total Reset Value
0x28	LUT7	0xD5

Bit	7	6	5	4	3	2	1	0
Name	lut7							
Reset	1	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut7	Temperature correction algorithm LUT7.

LUT8

LUT8 is a temperature correction algorithm LUT8 register.

Offset Address	Register Name	Total Reset Value
0x29	LUT8	0xDC

Bit	7	6	5	4	3	2	1	0
Name	lut8							
Reset	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut8	Temperature correction algorithm LUT8.

LUT9

LUT9 is a temperature correction algorithm LUT9 register.

Offset Address	Register Name	Total Reset Value
0x2A	LUT9	0xE2

Bit	7	6	5	4	3	2	1	0
Name	lut9							
Reset	1	1	1	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut9	Temperature correction algorithm LUT9.

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LUT10

LUT10 is a temperature correction algorithm LUT10 register.

Offset Address	Register Name	Total Reset Value
0x2B	LUT10	0xE8

Bit	7	6	5	4	3	2	1	0
Name	lut10							
Reset	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut10	Temperature correction algorithm LUT10.

LUT11

LUT11 is a temperature correction algorithm LUT11 register.

Offset Address	Register Name	Total Reset Value
0x2C	LUT11	0xEE

Bit	7	6	5	4	3	2	1	0
Name	lut11							
Reset	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut11	Temperature correction algorithm LUT11.

LUT12

LUT12 is a temperature correction algorithm LUT12 register.

Offset Address	Register Name	Total Reset Value
0x2D	LUT12	0xF3

Bit	7	6	5	4	3	2	1	0
Name	lut12							
Reset	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut12	Temperature correction algorithm LUT12.

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LUT13

LUT13 is a temperature correction algorithm LUT13 register.

Offset Address	Register Name	Total Reset Value
0x2E	LUT13	0xF9

Bit	7	6	5	4	3	2	1	0
Name	lut13							
Reset	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut13	Temperature correction algorithm LUT13.

LUT14

LUT14 is a temperature correction algorithm LUT14 register.

Offset Address	Register Name	Total Reset Value
0x2F	LUT14	0xFE

Bit	7	6	5	4	3	2	1	0
Name	lut14							
Reset	1	1	1	1	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut14	Temperature correction algorithm LUT14.

LUT15

LUT15 is a temperature correction algorithm LUT15 register.

Offset Address	Register Name	Total Reset Value
0x30	LUT15	0x03

Bit	7	6	5	4	3	2	1	0
Name	lut15							
Reset	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut15	Temperature correction algorithm LUT15.

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LUT16

LUT16 is a temperature correction algorithm LUT16 register.

Offset Address	Register Name	Total Reset Value
0x31	LUT16	0x08

Bit	7	6	5	4	3	2	1	0
Name	lut16							
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut16	Temperature correction algorithm LUT16.

LUT17

LUT17 is a temperature correction algorithm LUT17 register.

Offset Address	Register Name	Total Reset Value
0x32	LUT17	0x0D

Bit	7	6	5	4	3	2	1	0
Name	lut17							
Reset	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut17	Temperature correction algorithm LUT17.

LUT18

LUT18 is a temperature correction algorithm LUT18 register.

Offset Address	Register Name	Total Reset Value
0x33	LUT18	0x12

Bit	7	6	5	4	3	2	1	0
Name	lut18							
Reset	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut18	Temperature correction algorithm LUT18.

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LUT19

LUT19 is a temperature correction algorithm LUT19 register.

Offset Address	Register Name	Total Reset Value
0x34	LUT19	0x17

Bit	7	6	5	4	3	2	1	0
Name	lut19							
Reset	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut19	Temperature correction algorithm LUT19.

LUT20

LUT20 is a temperature correction algorithm LUT20 register.

Offset Address	Register Name	Total Reset Value
0x35	LUT20	0x1B

Bit	7	6	5	4	3	2	1	0
Name	lut20							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut20	Temperature correction algorithm LUT20.

LUT21

LUT21 is a temperature correction algorithm LUT21 register.

Offset Address	Register Name	Total Reset Value
0x36	LUT21	0x1F

Bit	7	6	5	4	3	2	1	0
Name	lut21							
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut21	Temperature correction algorithm LUT21.

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LUT22

LUT22 is a temperature correction algorithm LUT22 register.

Offset Address	Register Name	Total Reset Value
0x37	LUT22	0x23

Bit	7	6	5	4	3	2	1	0
Name	lut22							
Reset	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut22	Temperature correction algorithm LUT22.

LUT23

LUT23 is a temperature correction algorithm LUT23 register.

Offset Address	Register Name	Total Reset Value
0x38	LUT23	0x27

Bit	7	6	5	4	3	2	1	0
Name	lut23							
Reset	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut23	Temperature correction algorithm LUT23.

LUT24

LUT24 is a temperature correction algorithm LUT24 register.

Offset Address	Register Name	Total Reset Value
0x39	LUT24	0x2B

Bit	7	6	5	4	3	2	1	0
Name	lut24							
Reset	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut24	Temperature correction algorithm LUT24.

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LUT25

LUT25 is a temperature correction algorithm LUT25 register.

Offset Address	Register Name	Total Reset Value
0x3A	LUT25	0x2E

Bit	7	6	5	4	3	2	1	0
Name	lut25							
Reset	0	0	1	0	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut25	Temperature correction algorithm LUT25.

LUT26

LUT26 is a temperature correction algorithm LUT26 register.

Offset Address	Register Name	Total Reset Value
0x3B	LUT26	0x32

Bit	7	6	5	4	3	2	1	0
Name	lut26							
Reset	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut26	Temperature correction algorithm LUT26.

LUT27

LUT27 is a temperature correction algorithm LUT27 register.

Offset Address	Register Name	Total Reset Value
0x3C	LUT27	0x35

Bit	7	6	5	4	3	2	1	0
Name	lut27							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut27	Temperature correction algorithm LUT27.

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LUT28

LUT28 is a temperature correction algorithm LUT28 register.

Offset Address	Register Name	Total Reset Value
0x3D	LUT28	0x38

Bit	7	6	5	4	3	2	1	0
Name	lut28							
Reset	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut28	Temperature correction algorithm LUT28.

LUT29

LUT29 is a temperature correction algorithm LUT29 register.

Offset Address	Register Name	Total Reset Value
0x3E	LUT29	0x3B

Bit	7	6	5	4	3	2	1	0
Name	lut29							
Reset	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut29	Temperature correction algorithm LUT29.

LUT30

LUT30 is a temperature correction algorithm LUT30 register.

Offset Address	Register Name	Total Reset Value
0x3F	LUT30	0x3E

Bit	7	6	5	4	3	2	1	0
Name	lut30							
Reset	0	0	1	1	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut30	Temperature correction algorithm LUT30.

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LUT31

LUT31 is a temperature correction algorithm LUT31 register.

Offset Address	Register Name	Total Reset Value
0x40	LUT31	0x41

Bit	7	6	5	4	3	2	1	0
Name	lut31							
Reset	0	1	0	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut31	Temperature correction algorithm LUT31.

LUT32

LUT32 is a temperature correction algorithm LUT32 register.

Offset Address	Register Name	Total Reset Value
0x41	LUT32	0x43

Bit	7	6	5	4	3	2	1	0
Name	lut32							
Reset	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut32	Temperature correction algorithm LUT32.

LUT33

LUT33 is a temperature correction algorithm LUT33 register.

Offset Address	Register Name	Total Reset Value
0x42	LUT33	0x45

Bit	7	6	5	4	3	2	1	0
Name	lut33							
Reset	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut33	Temperature correction algorithm LUT33.

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LUT34

LUT34 is a temperature correction algorithm LUT34 register.

Offset Address	Register Name	Total Reset Value
0x43	LUT34	0x48

Bit	7	6	5	4	3	2	1	0
Name	lut34							
Reset	0	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut34	Temperature correction algorithm LUT34.

LUT35

LUT35 is a temperature correction algorithm LUT35 register.

Offset Address	Register Name	Total Reset Value
0x44	LUT35	0x4A

Bit	7	6	5	4	3	2	1	0
Name	lut35							
Reset	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut35	Temperature correction algorithm LUT35.

LUT36

LUT36 is a temperature correction algorithm LUT36 register.

Offset Address	Register Name	Total Reset Value
0x45	LUT36	0x4B

Bit	7	6	5	4	3	2	1	0
Name	lut36							
Reset	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut36	Temperature correction algorithm LUT36.

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LUT37

LUT37 is a temperature correction algorithm LUT37 register.

Offset Address	Register Name	Total Reset Value
0x46	LUT37	0x4D

Bit	7	6	5	4	3	2	1	0
Name	lut37							
Reset	0	1	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut37	Temperature correction algorithm LUT37.

LUT38

LUT38 is a temperature correction algorithm LUT38 register.

Offset Address	Register Name	Total Reset Value
0x47	LUT38	0x4F

Bit	7	6	5	4	3	2	1	0
Name	lut38							
Reset	0	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut38	Temperature correction algorithm LUT38.

LUT39

LUT39 is a temperature correction algorithm LUT39 register.

Offset Address	Register Name	Total Reset Value
0x48	LUT39	0x50

Bit	7	6	5	4	3	2	1	0
Name	lut39							
Reset	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut39	Temperature correction algorithm LUT39.

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LUT40

LUT40 is a temperature correction algorithm LUT40 register.

Offset Address	Register Name	Total Reset Value
0x49	LUT40	0x51

Bit	7	6	5	4	3	2	1	0
Name	lut40							
Reset	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut40	Temperature correction algorithm LUT40.

LUT41

LUT41 is a temperature correction algorithm LUT41 register.

Offset Address	Register Name	Total Reset Value
0x4A	LUT41	0x52

Bit	7	6	5	4	3	2	1	0
Name	lut41							
Reset	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut41	Temperature correction algorithm LUT41.

LUT42

LUT42 is a temperature correction algorithm LUT42 register.

Offset Address	Register Name	Total Reset Value
0x4B	LUT42	0x53

Bit	7	6	5	4	3	2	1	0
Name	lut42							
Reset	0	1	0	1	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut42	Temperature correction algorithm LUT42.

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LUT43

LUT43 is a temperature correction algorithm LUT43 register.

Offset Address	Register Name	Total Reset Value
0x4C	LUT43	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut43							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut43	Temperature correction algorithm LUT43.

LUT44

LUT44 is a temperature correction algorithm LUT44 register.

Offset Address	Register Name	Total Reset Value
0x4D	LUT44	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut44							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut44	Temperature correction algorithm LUT44.

LUT45

LUT45 is a temperature correction algorithm LUT45 register.

Offset Address	Register Name	Total Reset Value
0x4E	LUT45	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut45							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut45	Temperature correction algorithm LUT45.

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LUT46

LUT46 is a temperature correction algorithm LUT46 register.

Offset Address	Register Name	Total Reset Value
0x4F	LUT46	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut46							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut46	Temperature correction algorithm LUT46.

LUT47

LUT47 is a temperature correction algorithm LUT47 register.

Offset Address	Register Name	Total Reset Value
0x50	LUT47	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut47							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut47	Temperature correction algorithm LUT47.

SDM_COEF_OUSIDE_H

SDM_COEF_OUSIDE_H is an external upper-4-bit clock divider register.

Offset Address	Register Name	Total Reset Value
0x51	SDM_COEF_OUSIDE_H	0x8

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Sdm_coef_ouside_h			
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved.
[3:0]	RW	Sdm_coef_ousi de_h	Upper four bits of the clock divider in fixed frequency-division mode

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SDM_COEF_OUSIDE_L

SDM_COEF_OUSIDE_L is an external lower-8-bit clock divider register.

Offset Address	Register Name	Total Reset Value
0x52	SDM_COEF_OUSIDE_L	0x1B

Bit	7	6	5	4	3	2	1	0
Name	Sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	Sdm_coef_ouside_l	Lower eight bits of the clock divider in fixed frequency-division mode Note: When clock divider registers (addresses of 0x51 and 0x52) are read or written, you need to read or write to the upper four bits and then the lower eight bits continuously. The clock divider is calculated as follows: (f − 32700) x 30.52. f indicates the oscillation frequency of the external crystal and ranges from 32700 to 32799.

USER_REGISTER1

USER_REGISTER1 is 64-bit user register 1.

Offset Address	Register Name	Total Reset Value
0x53	USER_REGISTER1	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register1	64-bit user register 1 corresponding to bit[7:0].

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USER_REGISTER2

USER_REGISTER2 is 64-bit user register 2.

Offset Address	Register Name	Total Reset Value
0x54	USER_REGISTER2	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register2	64-bit user register 2 corresponding to bit[15:8].

USER_REGISTER3

USER_REGISTER3 is 64-bit user register 3.

Offset Address	Register Name	Total Reset Value
0x55	USER_REGISTER3	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register3	64-bit user register 3 corresponding to bit[23:16].

USER_REGISTER4

USER_REGISTER4 is 64-bit user register 4.

Offset Address	Register Name	Total Reset Value
0x56	USER_REGISTER4	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register4	64-bit user register 4 corresponding to bit[31:24].

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USER_REGISTER5

USER_REGISTER5 is 64-bit user register 5.

Offset Address	Register Name	Total Reset Value
0x57	USER_REGISTER5	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register5	64-bit user register 5 corresponding to bit[39:32].

USER_REGISTER6

USER_REGISTER6 is 64-bit user register 6.

Offset Address	Register Name	Total Reset Value
0x58	USER_REGISTER6	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register6	64-bit user register 6 corresponding to bit[47:40].

USER_REGISTER7

USER_REGISTER7 is 64-bit user register 7.

Offset Address	Register Name	Total Reset Value
0x59	USER_REGISTER7	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register7	64-bit user register 7 corresponding to bit[55:48].

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USER_REGISTER8

USER_REGISTER8 is 64-bit user register 8.

Offset Address	Register Name	Total Reset Value
0x5A	USER_REGISTER8	0x0

Bit	7	6	5	4	3	2	1	0
Name	2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register8	64-bit user register 8 corresponding to bit[63:56].

3.11 Power Management and Low-Power Mode Control

3.11.1 Overview

In low-power mode, the power consumption of the chip is reduced effectively. The Hi3516A reduces its power consumption in the following low-power control modes:

- System operating mode control

  In all operating modes except the normal mode, the power consumption is reduced to some extent. You can select different operating modes according to the actual power consumption and function requirements.
- Clock gating and clock frequency adjustment

  The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.
- Module low-power control

  When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.
- DDR low-power control

  The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.
- Dynamic voltage and frequency scaling (DVFS) based on CPU load monitoring
- Adaptive voltage scaling (AVS) based on CPU/core/MDDRC/MDA0 timing monitoring
- VEDU/AVC power-off

3.11.2 System Operating Modes

The system provides two operating modes.

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- Normal operating mode: This mode maps to the normal running mode of the system.

  When the system works in normal mode, you can control the clock frequency and set the modules and DDR to low-power mode to reduce the power consumption.
- Standby operating mode: This mode maps to the slow and doze running modes of the system.
  - In standby mode, the system works at the clock with low frequency, and the clocks of most idle modules are disabled. Therefore, the power consumption is low.
  - When the system works in slow or doze mode, you can power off the power supplies of idle modules to reduce the power consumption.

  The mode can be switched by configuring the system controller. For details, see section 3.5 "System Controller."

3.11.3 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce chip power consumption. For details about the process, see the description in section "clock gating" of each module.

In normal mode, the system can adjust its working frequency to reduce chip power consumption. To adjust the system working frequency, perform the following steps:

- Disable the service module to prevent it from accessing the DDR.
- Enable the system to run in the off-chip memory.

When DDRC_SREFCTRL[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode.

Step 1 Set SC_PLLCTRL bit[27:3] to the stable time of the PLL.

Step 2 Configure PERI_CRG12 bit[3:0] to select the clock sources of sysaxi, mda0axi, and mda1axi.

Step 3 Wait and configure DDRC_SREF_CTRL to enable the DDRC to exit the self-refresh mode based on the configuration requirements of the DDRC.

Step 4 The program starts to run in the DDR.

---End

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.4 "PLL Configuration."

3.11.4 Module Low-Power Control

Most modules including USB 2.0 host/Device, Video DAC (VDAC), and PLL modules support low-power operating modes. For details, see the descriptions of the system controller, VDP, and clocks.

- Low-power control for the USB 2.0 host/Device module:

  If the USB 2.0 host is not used, it can be disabled to switch the USB 2.0 host clock by setting PERI_CRG46 bit[7] to 0.
- Low-power control for the VDAC

  Unused VDAC channels can be disabled to reduce power consumption. For details, see section 11.5 "Registers Description."

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- The PLL also supports the low-power mode. If the PLL is not used, it can be disabled to switch the system to low-power mode.
  - If the APLL is not used, you can set PERI_CRG1 bit[23] to 1 to disable it. Then the APLL enters the low-power mode.
  - If the BPLL is not used, you can set PERI_CRG3 bit[23] to 1 to disable it. Then the BPLL enters the low-power mode
  - If VPLL is not used, you can set PERI_CRG5 bit[23] to 1 to disable it. Then VPLL enters the low-power mode.
  - If the EPLL is not used, you can set PERI_CRG9 bit[23] to 1 to disable it. Then the EPLL enters the low-power mode.

3.11.5 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

3.11.6 CPU DVFS

Table 3-22 describes the four profiles supported by the CPU.

Table 3-22 Four CPU profiles

Profile	Frequency	Voltage	Clock Source
Profile 1	438 MHz	0.99 V	APLL_FOUTPOSTDIV
Profile 2	600 MHz	1.1 V	APLL_FOUTPOSTDIV
Profile 3	732 MHz	1.21 V	APLL_FOUTPOSTDIV
Profile 4	850 MHz	1.32 V	APLL_FOUTPOSTDIV

Power Supply Mode

The core power supplies are provided by the DC-DC (controlled by the PWM) and PMU over the I^2C interface. The power supply mode can be configured based on board conditions:

- Mode 1: Four core power supplies are provided by the DC-DC controlled by the PWM.

  The PWM signals from the PMC need to be output to the PWMx pins by setting MISC_CTRL5 bit[19:16] to 0xF.
- Mode 2: Four core power supplies are provided by the PMU over the I^2C interface.

  The I^2C signals from the PMC need to be output to the PWM0 and PWM1 pins by setting muxctrl_reg83 and muxctrl_reg84 to 0x2.
- Mode 3: Four core power supplies are provided by the DC-DC (controlled by the PWM) and PMU over the I^2C interface respectively.

  The PWM2 and PWM3 signals from the PMC need to be output to the PWM2 and PWM3 pins by setting MISC_CTRL5 bit[19:16] to 0xC, and the I^2C signals from the PMC need to be output to the PWM0 and PWM1 pins by setting muxctrl_reg83 and muxctrl_reg84 to 0x2.

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Initializing the PWM

When the core power supplies of the CPU are provided by the DC-DC controlled by the PWM, the PMW in the PMC needs to be initialized

as follows:

Step 1 Configure the PWM period.

If the PWM period is N ($N \neq 0$), the PWM output frequency is 24 MHz/(N + 1).

The maximum PWM output frequency is 12 MHz.

If the PWM output frequency is 200 kHz, set PERI_PMC1 bit[15:0] to 0x77.

Step 2 Select the PWM for controlling the voltage of the CPU power domain.

PWM1 is selected by default.

The PWM control pin of the CPU DCDC on the board needs to be determined. The CPU PWM control pin is mapped to the PWMx pin by configuring PERI_PMC4 bit[15:8].

CAUTION

pwm3_reuse_cfg, pwm2_reuse_cfg, pwm1_reuse_cfg, and pwm0_reuse_cfg in PERI_PMC4 bit[15:8] must be set to different values among 24 values such as 0x0123, 0x1023, 0x2013, and 0x3012.

Step 3 Configure the PWM duty cycle.

If the PWM duty cycle is M, the PWM period is N, and M is less than N, the PWM output high-level duty cycle is (M + 1)/(N + 1).

For details, see the description of PERI_PMC1.

Step 4 Enable the PWM

by setting PERI_PMC4 bit[2] to 1.

----End

Increasing the Voltage to the Target Voltage

If the profile is switched to a low-level one, this operation can be skipped.

If the profile is switched to a high-level one, the CPU voltage needs to be increased by configuring the PMU or PWM. The CPU DCDC voltage can be set to the target voltage by adjusting the duty cycle. Wait 20 ms to ensure that the voltage is stable.

Switching the CPU Working Frequency

Perform the following steps:

Step 1 Switch the CPU working frequency to 500 MHz or 400 MHz by setting PERI_CRG12 bit[9:8] to 0x1 or 0x2 respectively.

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Step 2 Enable the APLL_FOUTPOSTDIV to output the target working frequency by configuring PERI_CRG0 and PERI_CRG1.

Step 3 Wait until PERI_CRG58 bit[0] is 1, indicating that the APLL is locked.

Step 4 Switch the CPU working frequency to APLL_FOUTPOSTDIV by setting PERI_CRG12 bit[9:8] to 0x0.

----End

Decreasing the Voltage to the Target Voltage

If the profile is switched to a high-level one, this operation can be skipped.

If the profile is switched to a low-level one, the CPU voltage needs to be decreased by configuring the PMU or PWM. The CPU DCDC voltage can be set to the target voltage by adjusting the duty cycle. Wait 20 ms to ensure that the voltage is stable.

3.11.7 AVS of the CPU/CORE/MDDRC/MDA0 Power Supplies

AVS is supported for the four core power supplies: CPU, CORE, MDDRC, and MDA0.

Selecting the Timing Monitoring Module and Voltage Regulation Output Interface

The Hi3516A monitors timings by using the HPM or timing sensor (TS), and the voltage can be adjusted by using the DCDC controlled by the PWM or the PMU over the I^2C interface. The voltages of all core power supplies need to be configured before AVS is enabled.

The timing monitoring module is selected as follows:

- Select the AVS control source of the CORE power domain by configuring PERI_PMC64 bit[18].
- Select the AVS control source of the CPU power domain by configuring PERI_PMC65 bit[18].
- Select the AVS control source of the MDDRC power domain by configuring PERI_PMC66 bit[18].
- Select the AVS control source of the MDA0 power domain by configuring PERI_PMC67 bit[18]. Because the timing monitoring module of MDA0 may be derived from mda0_top and VEDU, PERI_PMC67 bit[21:20] also need to be configured.

CAUTION

When the VEDU (H.265) encoder is powered off, PERI_PMC67 bit[21:20] must be set to 0x3.

The voltage regulation output interface of each power domain is selected as follows:

- Select the voltage regulation output interface of the CORE power domain by configuring PERI_PMC64 bit[19]. If the PWM mode is selected, the voltage regulation step of the PWM needs to be set by configuring PERI_PMC5 bit[31:16]. The recommended step is 10 mV.

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- Select the voltage regulation output interface of the CPU power domain by configuring PERI_PMC65 bit[19]. If the PWM mode is selected, the voltage regulation step of the PWM needs to be set by configuring PERI_PMC6 bit[31:16]. The recommended step is 10 mV.
- Select the voltage regulation output interface of the MDDRC power domain by configuring PERI_PMC66 bit[19]. If the PWM mode is selected, the voltage regulation step of the PWM needs to be set by configuring PERI_PMC7 bit[31:16]. The recommended step is 10 mV.
- Select the voltage regulation output interface of the MDA0 power domain by configuring PERI_PMC67 bit[19]. If the PWM mode is selected, the voltage regulation step of the PWM needs to be set by configuring PERI_PMC8 bit[31:16]. The recommended step is 10 mV.

Initializing the Timing Monitoring Module HPM

The HPM must be initialized before AVS is enabled. If the TS is the timing monitoring source, this operation can be skipped. The following example describes how to initialize the CPU HPM:

Step 1 Specify the monitoring cycle of the CPU HPM by configuring PERI_PMC17 bit[31:24] and PERI_PMC30 bit[31:24].

The monitoring cycle (T) is calculated as follows: $T = (N \times 2048 + M \times 16)/1000$ ms. N is specified by configuring PERI_PMC17 bit[31:24], and M is specified by configuring PERI_PMC30 bit[31:24].

Step 2 Enable CPU HPM cyclic monitoring and specify the HPM operating mode by configuring PERI_PMC14.

Step 3 Specify the upper limit and lower limit of the CPU HPM by configuring PERI_PMC17 bit[9:0] and PERI_PMC17 bit[21:12] respectively.

----End

Initializing the Timing Monitoring Module TS

The TS must be initialized before AVS is enabled. If the HPM is the timing monitoring source, this operation can be skipped. For example, to initialize the CPU TS, enable the CPU TS and perform related configurations by configuring PERI_PMC32.

Initializing HPM AVS CTRL

The Hi3516A supports HPM hardware AVS for the CPU/CORE/MDDRC/MDA0. HPM AVS CTRL must be initialized before HPM hardware AVS is enabled. If the TS is the timing monitoring source, this operation can be skipped. The following example describes how to initialize CPU HPM AVS CTRL:

Step 1 Specify the hardware AVS calculation mode by configuring PERI_PMC6 bit[2:1].

Step 2 Enable hardware AVS by setting PERI_PMC6 bit[0] to 1.

----End

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Initializing TS AVS CTRL

The Hi3516A supports TS hardware AVS for the CPU/CORE/MDDRC/MDA0. TS AVS CTRL must be initialized before TS hardware AVS is enabled. If the HPM is the timing monitoring source, this operation can be skipped. The following example describes how to initialize CPU TS AVS CTRL:

Step 1 Specify the hardware AVS monitoring cycle by configuring PERI_PMC65 bit[15:0]. The monitoring cycle (*T*) is calculated as follows: $T = (M \times 16)/1000$ ms. *M* is specified by configuring PERI_PMC65 bit[15:0].

Step 2 Specify the hardware AVS calculation mode by configuring PERI_PMC65 bit[22] and PERI_PMC65 bit[17].

Step 3 Enable hardware AVS by setting PERI_PMC65 bit[16] to 1.

----End

Configuring the PWM Power Output

If the PMU is the voltage regulation interface, this operation can be skipped. The following example assumes that the CORE, CPU, MDDRC, and MDA0 power domains connect to PWM0, PWM1, PWM2, and PWM3 respectively:

Configure the PWM power output by setting PERI_PMC4 to 0xE455.

Configuring the PMU Power Output

If the PWM is the voltage regulation interface, this operation can be skipped. The following example assumes that the CORE, CPU, MDDRC, and MDA0 power domains are controlled by pmu_reg6, pmu_reg5, pmu_reg4, and pmu_reg3 respectively:

Step 1 Enable the PMC I^2C master by setting PERI_PMC58 bit[31] to 1.

Step 2 Specify the I^2C slave address to be written to the PMU by configuring PERI_PMC58 bit[6:0].

Step 3 Set the I^2C clock frequency to 400 kHz by setting PERI_PMC62 to 0x003E.

Step 4 Configure the PWM power output by setting PERI_PMC63 to 0x7806C0.

----End

3.11.8 Powering on and Powering off the VEDU and AVC

The Hi3516A supports H.265 (VEDU) and H.264 (AVC) encoding. If the VEDU and AVC are not used, they can be powered off to reduce power consumption.

The VEDU and AVC are powered off as follows:

Step 1 Disable the VEDU and AVC. Then the VEDU and AVC do not access DDRs after the current access.

Step 2 Reset the VEDU and AVC by setting PERI_CRG16 bit[0] (VEDU) and PERI_CRG16 bit[12] (AVC) to 1.

Step 3 Disable the working clocks of the VEDU and AVC by setting PERI_CRG16 bit[1] (VEDU) and PERI_CRG16 bit[13] (AVC) to 0.

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Step 4 Enable signal isolation for the VEDU and AVC by setting MISC_CTRL5 bit[4] (VEDU) and MISC_CTRL5 bit[0] (AVC) to 1.

Step 5 Validate the power-off requests of the VEDU and AVC by setting MISC_CTRL5 bit[5] (VEDU) and MISC_CTRL5 bit[1] (AVC) to 0.

Step 6 Wait until MISC_CTRL5 bit[6] (VEDU) and MISC_CTRL5 bit[12] (AVC) are 0, indicating that the VEDU and AVC are powered off.

----End

The VEDU and AVC are powered on as follows:

Step 1 Validate the power-on requests of the VEDU and AVC by setting MISC_CTRL5 bit[5] (VEDU) and MISC_CTRL5 bit[1] (AVC) to 1.

Step 2 Wait until MISC_CTRL5 bit[6] (VEDU) and MISC_CTRL5 bit[12] (AVC) are 1, indicating that the VEDU and AVC are powered on.

Step 3 Enable the working clocks of the VEDU and AVC by setting PERI_CRG16 bit[1] (VEDU) and PERI_CRG16 bit[13] (AVC) to 1.

Step 4 Deassert the reset on the VEDU and AVC by setting PERI_CRG16 bit[0] (VEDU) and PERI_CRG16 bit[12] (AVC) to 0.

Step 5 Disable signal isolation for the VEDU and AVC by setting MISC_CTRL5 bit[4] (VEDU) and MISC_CTRL5 bit[0] (AVC) to 0.

----End

3.11.9 PMC Register Summary

Table 3-23 describes PMC registers.

Table 3-23 Summary of PMC registers (base address: 0x2027_0000)

Offset Address	Register	Description	Page
0x0000	PERI_PMC0	PMC register 0	3-251
0x0004	PERI_PMC1	PMC register 1	3-251
0x0008	PERI_PMC2	PMC register 2	3-251
0x000c	PERI_PMC3	PMC register 3	3-252
0x0010	PERI_PMC4	PMC register 4	3-252
0x0014	PERI_PMC5	PMC register 5	3-254
0x0018	PERI_PMC6	PMC register 6	3-255
0x001c	PERI_PMC7	PMC register 7	3-256
0x0020	PERI_PMC8	PMC register 8	3-257
0x0024	PERI_PMC9	PMC register 9	3-258

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Offset Address	Register	Description	Page
0x0028	PERI_PMC10	Core high performance monitor (HPM) control register 1	3-259
0x002C	PERI_PMC11	Core HPM status register 1	3-260
0x0030	PERI_PMC12	Core HPM status register 2	3-261
0x0034	PERI_PMC13	Core HPM control register 2	3-262
0x0038	PERI_PMC14	CPU HPM control register 1	3-263
0x003C	PERI_PMC15	CPU HPM status register 1	3-264
0x0040	PERI_PMC16	CPU HPM status register 2	3-265
0x0044	PERI_PMC17	CPU HPM control register 2	3-265
0x0048	PERI_PMC18	DDR HPM control register 1	3-266
0x004C	PERI_PMC19	DDR HPM status register 1	3-267
0x0050	PERI_PMC20	DDR HPM status register 2	3-268
0x0054	PERI_PMC21	DDR HPM control register 2	3-269
0x0058	PERI_PMC22	MDA TOP HPM control register 1	3-270
0x005C	PERI_PMC23	MDA TOP HPM status register 1	3-271
0x0060	PERI_PMC24	MDA TOP HPM status register 2	3-272
0x0064	PERI_PMC25	MDA TOP HPM control register 2	3-272
0x0068	PERI_PMC26	VEDU HPM control register 1	3-273
0x006C	PERI_PMC27	VEDU HPM status register 1	3-274
0x0070	PERI_PMC28	VEDU HPM status register 2	3-275
0x0074	PERI_PMC29	VEDU HPM control register 2	3-276
0x0078	PERI_PMC30	HPM control register (fine 1)	3-277
0x007C	PERI_PMC31	HPM control register (fine 2)	3-277
0x0080	PERI_PMC32	CPU TS control register	3-278
0x0084	PERI_PMC33	DDR TS control register	3-279
0x0088	PERI_PMC34	Core TS control register	3-280
0x008C	PERI_PMC35	MDA TOP TS control register	3-282
0x0090	PERI_PMC36	VEDU TS control register	3-283
0x0094	PERI_PMC37	CPU TS status register 0	3-284
0x0098	PERI_PMC38	CPU TS status register 1	3-285
0x009C	PERI_PMC39	CPU TS status register 2	3-285

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Offset Address	Register	Description	Page
0x0A0	PERI_PMC40	CPU TS status register 3	3-286
0x00A4	PERI_PMC41	DDR TS status register 0	3-286
0x00A8	PERI_PMC42	DDR TS status register 1	3-286
0x00AC	PERI_PMC43	DDR TS status register 2	3-287
0x0B0	PERI_PMC44	DDR TS status register 3	3-287
0x00B4	PERI_PMC45	CORE TS status register 0	3-288
0x00B8	PERI_PMC46	CORE TS status register 1	3-288
0x00BC	PERI_PMC47	CORE TS status register 2	3-289
0x0C0	PERI_PMC48	CORE TS status register 3	3-289
0x00C4	PERI_PMC49	MDA TOP TS status register 0	3-290
0x00C8	PERI_PMC50	MDA TOP TS status register 1	3-290
0x00CC	PERI_PMC51	MDA TOP TS status register 2	3-291
0x0D0	PERI_PMC52	MDA TOP TS status register 3	3-291
0x00D4	PERI_PMC53	VEDU TS status register 0	3-292
0x00D8	PERI_PMC54	VEDU TS status register 1	3-292
0x00DC	PERI_PMC55	VEDU TS status register 2	3-293
0x0E0	PERI_PMC56	VEDU TS status register 3	3-293
0x00E4	PERI_PMC57	PMC register 57	3-294
0x00E8	PERI_PMC58	PMC_I2C_CFG1 register	3-294
0x00EC	PERI_PMC59	PMC_I2C_CFG2 register	3-296
0x00F0	PERI_PMC60	PMC_I2C_CFG3 register	3-296
0x00F4	PERI_PMC61	PMC_I2C_STAT register	3-296
0x00F8	PERI_PMC62	PMC_I2C_CFG4 register	3-297
0x00FC	PERI_PMC63	PMC_I2C_CFG5 register	3-298
0x0100	PERI_PMC64	PMC register 64	3-299
0x0104	PERI_PMC65	PMC register 65	3-300
0x0108	PERI_PMC66	PMC register 66	3-301
0x010C	PERI_PMC67	PMC register 67	3-302

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3.11.10 PMC Register Description

PERI_PMC0

PERI_PMC0 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_PMC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_pwm_duty																core_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	core_pwm_duty	Number of PWM high-level beats for the core AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	core_pwm_period	Number of PWM cycles for the core AVS output.

PERI_PMC1

PERI_PMC1 is PMC register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_PMC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cpu_pwm_duty																cpu_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cpu_pwm_duty	Number of PWM high-level beats for the CPU AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	cpu_pwm_period	Number of PWM cycles for the CPU AVS output.

PERI_PMC2

PERI_PMC2 is PMC register 2.

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Offset Address	Register Name	Total Reset Value
0x0008	PERI_PMC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddr_pwm_duty																ddr_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ddr_pwm_duty	Number of PWM high-level beats for the DDR AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	ddr_pwm_period	Number of PWM cycles for the DDR AVS output.

PERI_PMC3

PERI_PMC3 is PMC register 3.

Offset Address	Register Name	Total Reset Value
0x000c	PERI_PMC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda_pwm_duty																mda_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mda_pwm_duty	Number of PWM high-level beats for the MDA AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	mda_pwm_period	Number of PWM cycles for the MDA AVS output.

PERI_PMC4

PERI_PMC4 is PMC register 4.

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Offset Address	Register Name	Total Reset Value
0x0010	PERI_PMC4	0x0000_E400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pwm3_reuse_cfg		pwm2_reuse_cfg		pwm1_reuse_cfg		pwm0_reuse_cfg		mda_pwm_inv	mda_pwm_enable	ddr_pwm_inv	ddr_pwm_enable	cpu_pwm_inv	cpu_pwm_enable	core_pwm_inv	core_pwm_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:14]	RW	pwm3_reuse_cfg	PWM3 source select for the AVS output. 00: core 01: CPU 10: DDR 11: MDA
[13:12]	RW	pwm2_reuse_cfg	PWM2 source select for the AVS output. 00: core 01: CPU 10: DDR 11: MDA
[11:10]	RW	pwm1_reuse_cfg	PWM1 source select for the AVS output. 00: core 01: CPU 10: DDR 11: MDA
[9:8]	RW	pwm0_reuse_cfg	PWM0 source select for the AVS output. 00: core 01: CPU 10: DDR 11: MDA
[7]	RW	mda_pwm_inv	PWM phase control for the MDA AVS output. 0: normal output 1: inverted output

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[6]	RW	mda_pwm_enable	PWM enable for the MDA AVS output. 0: disabled 1: enabled
[5]	RW	ddr_pwm_inv	PWM phase control for the DDR AVS output. 0: normal output 1: inverted output
[4]	RW	ddr_pwm_enable	PWM enable for the DDR AVS output. 0: disabled 1: enabled
[3]	RW	cpu_pwm_inv	PWM phase control for the CPU AVS output. 0: normal output 1: inverted output
[2]	RW	cpu_pwm_enable	PWM enable for the CPU AVS output. 0: disabled 1: enabled
[1]	RW	core_pwm_inv	PWM phase control for the core AVS output. 0: normal output 1: inverted output
[0]	RW	core_pwm_enable	PWM enable for the core AVS output. 0: disabled 1: enabled

PERI_PMC5

PERI_PMC5 is PMC register 5.

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Offset Address	Register Name	Total Reset Value
0x0014	PERI_PMC5	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	core_avs_fsm_inc_pwm_step		core_avs_fsm_dec_pwm_step		reserved					core_avs_hpm_fsm_calc_mode	core_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	core_avs_fsm_inc_pwm_step	Automatic increase step of the core AVS FSM PWM.
[23:16]	RW	core_avs_fsm_dec_pwm_step	Automatic decrease step of the core AVS FSM PWM.
[15:3]	RO	reserved	Reserved.
[2:1]	RW	core_avs_hpm_fsm_calc_mode	Calculation mode of the core AVS HPM FSM. 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	core_hpm_fsm_en	Core AVS HPM FSM enable. 0: disabled 1: enabled

PERI_PMC6

PERI_PMC6 is PMC register 6.

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Offset Address	Register Name	Total Reset Value
0x0018	PERI_PMC6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	cpu_avs_fsm_inc_pwm_step		cpu_avs_fsm_dec_pwm_step		reserved				cpu_avs_hpm_fsm_calc_mode		cpu_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	cpu_avs_fsm_inc_pwm_step	Automatic increase step of the CPU AVS FSM PWM.
[23:16]	RW	cpu_avs_fsm_dec_pwm_step	Automatic decrease step of the CPU AVS FSM PWM.
[15:3]	RO	reserved	Reserved.
[2:1]	RW	cpu_avs_hpm_fsm_calc_mode	Calculation mode of the CPU AVS HPM FSM. 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	cpu_hpm_fsm_en	CPU AVS HPM FSM enable. 0: disabled 1: enabled

PERI_PMC7

PERI_PMC7 is PMC register 7.

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Offset Address	Register Name	Total Reset Value
0x001c	PERI_PMC7	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	ddr_avs_fsm_inc_pwm_step		ddr_avs_fsm_dec_pwm_step		reserved				ddr_avs_hpm_fsm_calc_mode		ddr_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ddr_avs_fsm_inc_pwm_step	Automatic increase step of the DDR AVS FSM PWM.
[23:16]	RW	ddr_avs_fsm_dec_pwm_step	Automatic decrease step of the DDR AVS FSM PWM.
[15:3]	RO	reserved	Reserved.
[2:1]	RW	ddr_avs_hpm_fsm_calc_mode	Calculation mode of the core DDR AVS HPM FSM. 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	ddr_hpm_fsm_en	DDR AVS HPM FSM enable. 0: disabled 1: enabled

PERI_PMC8

PERI_PMC8 is PMC register 8.

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Offset Address	Register Name	Total Reset Value
0x0020	PERI_PMC8	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	mda_avs_fsm_inc_pwm_step		mda_avs_fsm_dec_pwm_step		reserved				mda_avs_hpm_fsm_calc_mode		mda_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	mda_avs_fsm_inc_pwm_step	Automatic increase step of the MDA AVS FSM PWM.
[23:16]	RW	mda_avs_fsm_dec_pwm_step	Automatic decrease step of the MDA AVS FSM PWM.
[15:3]	RO	reserved	Reserved.
[2:1]	RW	mda_avs_hpm_fsm_calc_mode	Calculation mode of the MDA AVS HPM FSM. 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	mda_hpm_fsm_en	MDA AVS HPM FSM enable. 0: disabled 1: enabled

PERI_PMC9

PERI_PMC9 is PMC register 9.

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Offset Address	Register Name	Total Reset Value
0x0024	PERI_PMC9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	mda_avs_state_machine			reserved	ddr_avs_state_machine			reserved	cpu_avs_state_machine			reserved	core_avs_state_machine		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RO	mda_avs_state_machine	MDA AVS HPM FSM status.
[11]	RO	reserved	Reserved.
[10:8]	RO	ddr_avs_state_machine	DDR AVS HPM FSM status.
[7]	RO	reserved	Reserved.
[6:4]	RO	cpu_avs_state_machine	CPU AVS HPM FSM status.
[3]	RO	reserved	Reserved.
[2:0]	RO	core_avs_state_machine	Core AVS HPM FSM status.

PERI_PMC10

PERI_PMC10 is core HPM control register 1.

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Offset Address	Register Name	Total Reset Value
0x0028	PERI_PMC10	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_srst_req	core_hpm_monitor_en	core_hpm_bypass	core_hpm_en	reserved				core_hpm_offset								reserved		core_hpm_shift		reserved				core_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27]	RW	core_hpm_srst_req	Core HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	core_hpm_monitor_en	Core HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	core_hpm_bypass	Core HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	core_hpm_en	Core HPM measurement enable. 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	WO	reserved	Reserved.
[21:12]	RW	core_hpm_offset	Core HPM offset.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	core_hpm_shift	Core HPM shift.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	core_hpm_div	Core HPM clock divider. n: divn

PERI_PMC11

PERI_PMC11 is core HPM status register 1.

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Offset Address	Register Name	Total Reset Value
0x002C	PERI_PMC11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						core_hpm_up_warning	core_hpm_low_warning	reserved				core_hpm_pc_record1								reserved	core_hpm_pc_valid	core_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	core_hpm_up_warning	Upper limit for the core HPM warning.
[24]	RO	core_hpm_low_warning	Lower limit for the core HPM warning.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	core_hpm_pc_record1	Core HPM original code pattern 1.
[11]	RO	reserved	Reserved.
[10]	RO	core_hpm_pc_valid	Core HPM output validity indicator. 0: invalid 1: valid
[9:0]	RO	core_hpm_pc_record0	Core HPM original code pattern 0.

PERI_PMC12

PERI_PMC12 is core HPM status register 2.

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Offset Address	Register Name	Total Reset Value
0x0030	PERI_PMC12	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	core_hpm_rcc	reserved	core_hpm_pc_record3		reserved	core_hpm_pc_record2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	core_hpm_rcc	Core HPM output with the RCC code.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	core_hpm_pc_record3	Core HPM original code pattern 3.
[11:10]	RO	reserved	Reserved.
[9:0]	RO	core_hpm_pc_record2	Core HPM original code pattern 2.

PERI_PMC13

PERI_PMC13 is core HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_PMC13	0x0100_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	core_hpm_monitor_period		reserved	core_hpm_lowlimit		reserved	core_hpm_uplimit	
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	core_hpm_monitor_period	Core HPM cyclic monitoring period. If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved.

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[21:12]	RW	core_hpm_lowlimit	Core HPM lower limit.
[11:10]	RO	reserved	Reserved.
[9:0]	RW	core_hpm_uplimit	Core HPM upper limit.

PERI_PMC14

PERI_PMC14 is CPU HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_PMC14	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_hpm_srst_req	cpu_hpm_monitor_en	cpu_hpm_bypass	cpu_hpm_en	reserved				cpu_hpm_offset								reserved		cpu_hpm_shift		reserved				cpu_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27]	RW	cpu_hpm_srst_req	CPU HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	cpu_hpm_monitor_en	CPU HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	cpu_hpm_bypass	CPU HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	cpu_hpm_en	CPU HPM measurement enable. 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	cpu_hpm_offset	CPU HPM offset.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	cpu_hpm_shift	CPU HPM shift.

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[7:6]	RW	reserved	Reserved.
[5:0]	RW	cpu_hpm_div	CPU HPM clock divider. n: divn

PERI_PMC15

PERI_PMC15 is CPU HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_PMC15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						cpu_hpm_up_warning	cpu_hpm_low_warning	reserved				cpu_hpm_pc_record1								reserved	cpu_hpm_pc_valid	cpu_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	cpu_hpm_up_warning	Upper limit for the CPU HPM warning.
[24]	RO	cpu_hpm_low_warning	Lower limit for the CPU HPM warning.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	cpu_hpm_pc_record1	CPU HPM original code pattern 1.
[11]	RO	reserved	Reserved.
[10]	RO	cpu_hpm_pc_valid	CPU HPM output validity indicator. 0: invalid 1: valid
[9:0]	RO	cpu_hpm_pc_record0	CPU HPM original code pattern 0.

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PERI_PMC16

PERI_PMC16 is CPU HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_PMC16	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cpu_hpm_rcc	reserved	cpu_hpm_pc_record3		reserved	cpu_hpm_pc_record2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	cpu_hpm_rcc	CPU HPM output with the RCC code.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	cpu_hpm_pc_record3	CPU HPM original code pattern 3.
[11:10]	RO	reserved	Reserved.
[9:0]	RO	cpu_hpm_pc_record2	CPU HPM original code pattern 2.

PERI_PMC17

PERI_PMC17 is CPU HPM control register 2.

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Offset Address	Register Name	Total Reset Value
0x0044	PERI_PMC17	0x0100_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	cpu_hpm_monitor_period		reserved	cpu_hpm_lowlimit		reserved	cpu_hpm_uplimit		
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	cpu_hpm_monitor_period	CPU HPM cyclic monitoring period. If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	cpu_hpm_lowlimit	CPU HPM lower limit.
[11:10]	RO	reserved	Reserved.
[9:0]	RW	cpu_hpm_uplimit	CPU HPM upper limit.

PERI_PMC18

PERI_PMC18 is DDR HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_PMC18	0x0000_000A

Bit	31 30 29 28	27	26	25	24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved	ddr_hpm_srst_req	ddr_hpm_monitor_en	ddr_hpm_bypass	ddr_hpm_en	reserved	ddr_hpm_offset		reserved	ddr_hpm_shift	reserved	ddr_hpm_div
Reset	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	1 0 1 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.

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[27]	RW	ddr_hpm_srst_req	DDR HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	ddr_hpm_monitor_en	DDR HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	ddr_hpm_bypass	DDR HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	ddr_hpm_en	DDR HPM measurement enable. 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	ddr_hpm_offset	DDR HPM offset.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	ddr_hpm_shift	DDR HPM shift.
[7:6]	RW	reserved	Reserved.
[5:0]	RW	ddr_hpm_div	DDR HPM clock divider. n: divn

PERI_PMC19

PERI_PMC19 is DDR HPM status register 1.

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Offset Address	Register Name	Total Reset Value
0x004C	PERI_PMC19	0x0000_0000

Bit	31 30 29 28	27 26	25	24	23 22	21 20	19 18 17 16	15 14 13 12	11	10	9 8	7 6 5 4	3 2 1 0
Name	reserved		ddr_hpm_up_warning	ddr_hpm_low_warning	reserved	ddr_hpm_pc_record1			reserved	ddr_hpm_pc_valid	ddr_hpm_pc_record0		
Reset	0 0 0 0	0 0	0	0	0 0	0 0	0 0 0 0	0 0 0 0	0	0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	ddr_hpm_up_warning	Upper limit for the DDR HPM warning.
[24]	RO	ddr_hpm_low_warning	Lower limit for the DDR HPM warning.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	ddr_hpm_pc_record1	DDR HPM original code pattern 1.
[11]	RO	reserved	Reserved.
[10]	RO	ddr_hpm_pc_valid	DDR HPM output validity indicator. 0: invalid 1: valid
[9:0]	RO	ddr_hpm_pc_record0	DDR HPM original code pattern 0.

PERI_PMC20

PERI_PMC20 is DDR HPM status register 2.

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Offset Address	Register Name	Total Reset Value
0x0050	PERI_PMC20	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ddr_hpm_rcc	reserved	ddr_hpm_pc_record3		reserved	ddr_hpm_pc_record2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	ddr_hpm_rcc	DDR HPM output with the RCC code.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	ddr_hpm_pc_record3	DDR HPM original code pattern 3.
[11:10]	RO	reserved	Reserved.
[9:0]	RO	ddr_hpm_pc_record2	DDR HPM original code pattern 2.

PERI_PMC21

PERI_PMC21 is DDR HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0054	PERI_PMC21	0x0100_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ddr_hpm_monitor_period		reserved	ddr_hpm_lowlimit		reserved	ddr_hpm_uplimit	
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	ddr_hpm_monitor_period	DDR HPM cyclic monitoring period. If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved.

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[21:12]	RW	ddr_hpm_lowlimit	DDR HPM lower limit.
[11:10]	RO	reserved	Reserved.
[9:0]	RW	ddr_hpm_uplimit	DDR HPM upper limit.

PERI_PMC22

PERI_PMC22 is MDA TOP HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_PMC22	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mda_top_hpm_srst_req	mda_top_hpm_monitor_en	mda_top_hpm_bypass	mda_top_hpm_en	reserved				mda_top_hpm_offset								reserved		mda_top_hpm_shift		reserved				mda_top_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27]	RW	mda_top_hpm_srst_req	MDA TOP HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	mda_top_hpm_monitor_en	MDA TOP HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	mda_top_hpm_bypass	MDA TOP HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	mda_top_hpm_en	MDA TOP HPM measurement enable. 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	mda_top_hpm_offset	MDA TOP HPM offset.

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[11:10]	RO	reserved	Reserved.
[9:8]	RW	mda_top_hpm_shift	MDA TOP HPM shift.
[7:6]	RW	reserved	Reserved.
[5:0]	RW	mda_top_hpm_div	MDA TOP HPM clock divider. n: divn

PERI_PMC23

PERI_PMC23 is MDA TOP HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_PMC23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						mda_top_hpm_up_warning	mda_top_hpm_low_warning	reserved				mda_top_hpm_pc_record1								reserved	mda_top_hpm_pc_valid	mda_top_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	mda_top_hpm_up_warning	Upper limit for the MDA TOP HPM warning.
[24]	RO	mda_top_hpm_low_warning	Lower limit for the MDA TOP HPM warning.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	mda_top_hpm_pc_record1	MDA TOP HPM original code pattern 1.
[11]	RO	reserved	Reserved.
[10]	RO	mda_top_hpm_pc_valid	MDA TOP HPM output validity indicator. 0: invalid 1: valid

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[9:0]	RO	mda_top_hpm_pc_record0	MDA TOP HPM original code pattern 0.

PERI_PMC24

PERI_PMC24 is MDA TOP HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_PMC24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mda_top_hpm_rcc				reserved				mda_top_hpm_pc_record3								reserved				mda_top_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	mda_top_hpm_rcc	MDA TOP HPM output with the RCC code.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	mda_top_hpm_pc_record3	MDA TOP HPM original code pattern 3.
[11:10]	RO	reserved	Reserved.
[9:0]	RO	mda_top_hpm_pc_record2	MDA TOP HPM original code pattern 2.

PERI_PMC25

PERI_PMC25 is MDA TOP HPM control register 2.

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Offset Address	Register Name	Total Reset Value
0x0064	PERI_PMC25	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda_top_hpm_monitor_period								reserved				mda_top_hpm_lowlimit								reserved		mda_top_hpm_uplimit									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	mda_top_hpm_monitor_period	MDA TOP HPM cyclic monitoring period. If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	mda_top_hpm_lowlimit	MDA TOP HPM lower limit
[11:10]	RO	reserved	Reserved.
[9:0]	RW	mda_top_hpm_uplimit	MDA TOP HPM upper limit

PERI_PMC26

PERI_PMC26 is VEDU HPM control register 1.

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Offset Address	Register Name	Total Reset Value
0x0068	PERI_PMC26	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vedu_hpm_srst_req	vedu_hpm_monitor_en	vedu_hpm_bypass	vedu_hpm_en	reserved				vedu_hpm_offset								reserved		vedu_hpm_shift		reserved				vedu_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27]	RW	vedu_hpm_srst_req	VEDU HPM reset request, active high. 0: reset deasserted 1: reset
[26]	RW	vedu_hpm_monitor_en	VEDU HPM cyclic monitoring enable. 0: disabled 1: enabled
[25]	RW	vedu_hpm_bypass	VEDU HPM cyclic monitoring bypass. 0: not bypassed 1: bypassed
[24]	RW	vedu_hpm_en	VEDU HPM measurement enable. 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved.
[21:12]	RW	vedu_hpm_offset	VEDU HPM offset.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	vedu_hpm_shift	VEDU HPM shift.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	vedu_hpm_div	VEDU HPM clock divider. n: divn

PERI_PMC27

PERI_PMC27 is VEDU HPM status register 1.

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Offset Address	Register Name	Total Reset Value
0x006C	PERI_PMC27	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						vedu_hpm_up_warning	vedu_hpm_low_warning	reserved				vedu_hpm_pc_record1								reserved	vedu_hpm_pc_valid	vedu_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	vedu_hpm_up_warning	Upper limit for the VEDU HPM warning.
[24]	RO	vedu_hpm_low_warning	Lower limit for the VEDU HPM warning.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	vedu_hpm_pc_record1	VEDU HPM original code pattern 1.
[11]	RO	reserved	Reserved.
[10]	RO	vedu_hpm_pc_valid	VEDU HPM output validity indicator. 0: invalid 1: valid
[9:0]	RO	vedu_hpm_pc_record0	VEDU HPM original code pattern 0.

PERI_PMC28

PERI_PMC28 is VEDU HPM status register 2.

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Offset Address	Register Name	Total Reset Value
0x0070	PERI_PMC28	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vedu_hpm_rcc	reserved	vedu_hpm_pc_record3		reserved	vedu_hpm_pc_record2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	vedu_hpm_rcc	VEDU HPM output with the RCC code.
[23:22]	RO	reserved	Reserved.
[21:12]	RO	vedu_hpm_pc_record3	VEDU HPM original code pattern 3.
[11:10]	RO	reserved	Reserved.
[9:0]	RO	vedu_hpm_pc_record2	VEDU HPM original code pattern 2.

PERI_PMC29

PERI_PMC29 is VEDU HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_PMC29	0x0100_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	vedu_hpm_monitor_period		reserved	vedu_hpm_lowlimit		reserved	vedu_hpm_uplimit	
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	vedu_hpm_monitor_period	VEDU HPM cyclic monitoring period. If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved.

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[21:12]	RW	vedu_hpm_lowlimit	VEDU HPM lower limit.
[11:10]	RO	reserved	Reserved.
[9:0]	RW	vedu_hpm_uplimit	VEDU HPM upper limit.

PERI_PMC30

PERI_PMC30 is an HPM control register (fine 1).

Offset Address	Register Name	Total Reset Value
0x0078	PERI_PMC30	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cpu_hpm_monitor_period								ddr_hpm_monitor_period								mda_top_hpm_monitor_period								vedu_hpm_monitor_period							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	cpu_hpm_monitor_period	CPU HPM cyclic monitoring period fine.
[23:16]	RW	ddr_hpm_monitor_period	DDR HPM cyclic monitoring period fine.
[15:8]	RW	mda_top_hpm_monitor_period	MDA TOP HPM cyclic monitoring period fine.
[7:0]	RW	vedu_hpm_monitor_period	VEDU HPM cyclic monitoring period fine.

PERI_PMC31

PERI_PMC31 is an HPM control register (fine 2).

Offset Address	Register Name	Total Reset Value
0x007C	PERI_PMC31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								core_hpm_monitor_period							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	core_hpm_monitor_period	Core HPM cyclic monitoring period fine.

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PERI_PMC32

PERI_PMC32 is a CPU TS control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_PMC32	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved			cpu_ts_en	reserved	cpu_ts_step			cpu_ts_dly_adjust			cpu_ts_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:9]	RW	reserved	Reserved.
[8]	RW	cpu_ts_en	CPU TS module enable for controlling the internal ICG.
[7]	RW	reserved	Reserved.
[6:5]	RW	cpu_ts_step	CPU TS code step. 00: step = 1 01: step = 2 1x: step = 3

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[4:1]	RW	cpu_ts_dly_adjust	CPU TS crazy path delay. 0x0: −4 0x1: −4 0x2: −4 0x3: −4 0x4: −3 0x5: −2 0x6: −1 0x7: 0 (default) 0x8: +1 0x9: +2 0xA: +3 0xB: +4 0xC: +5 0xD: +6 0xE: +7 0xF: +8
[0]	RW	cpu_ts_sel	CPU TS crazy path select. 0: path A 1: path B

PERI_PMC33

PERI_PMC33 is a DDR TS control register.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_PMC33	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved			ddr_ts_en	reserved	ddr_ts_step			ddr_ts_dly_adjust			ddr_ts_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:9]	RW	reserved	Reserved.
[8]	RW	ddr_ts_en	DDR TS module enable for controlling the internal ICG.

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[7]	RW	reserved	Reserved.
[6:5]	RW	ddr_ts_step	DDR TS code step. 00: step = 1 01: step = 2 1x: step = 3
[4:1]	RW	ddr_ts_dly_adjust	DDR TS crazy path delay. 0x0: −4 0x1: −4 0x2: −4 0x3: −4 0x4: −3 0x5: −2 0x6: −1 0x7: 0 (default) 0x8: +1 0x9: +2 0xA: +3 0xB: +4 0xC: +5 0xD: +6 0xE: +7 0xF: +8
[0]	RW	ddr_ts_sel	DDR TS crazy path select. 0: path A 1: path B

PERI_PMC34

PERI_PMC34 is a core TS control register.

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Offset Address	Register Name	Total Reset Value
0x0088	PERI_PMC34	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved			core_ts_en	reserved	core_ts_step			core_ts_dly_adjust			core_ts_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:9]	RW	reserved	Reserved.
[8]	RW	core_ts_en	Core TS module enable for controlling the internal ICG.
[7]	RW	reserved	Reserved.
[6:5]	RW	core_ts_step	Core TS code step. 00: step = 1 01: step = 2 1x: step = 3
[4:1]	RW	core_ts_dly_adjust	Core TS crazy path delay. 0x0: −4 0x1: −4 0x2: −4 0x3: −4 0x4: −3 0x5: −2 0x6: −1 0x7: 0 (default) 0x8: +1 0x9: +2 0xA: +3 0xB: +4 0xC: +5 0xD: +6 0xE: +7 0xF: +8
[0]	RW	core_ts_sel	Core TS crazy path select. 0: path A 1: path B

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PERI_PMC35

PERI_PMC35 is an MDA TOP TS control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_PMC35	0x0000_000E

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7	6 5	4	3 2 1	0
Name	reserved					reserved	mda_top_ts_en	reserved	mda_top_ts_step	mda_top_ts_dly_adjust		mda_top_ts_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0	0 0	0	1 1 1	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:9]	RW	reserved	Reserved.
[8]	RW	mda_top_ts_en	MDA TOP TS module enable for controlling the internal ICG.
[7]	RW	reserved	Reserved.
[6:5]	RW	mda_top_ts_step	MDA TOP TS code step. 00: step = 1 01: step = 2 1x: step = 3

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[4:1]	RW	mda_top_ts_dly_adjust	MDA TOP TS crazy path delay. 0x0: −4 0x1: −4 0x2: −4 0x3: −4 0x4: −3 0x5: −2 0x6: −1 0x7: 0 (default) 0x8: +1 0x9: +2 0xA: +3 0xB: +4 0xC: +5 0xD: +6 0xE: +7 0xF: +8
[0]	RW	mda_top_ts_sel	MDA TOP TS crazy path select. 0: path A 1: path B

PERI_PMC36

PERI_PMC36 is a VEDU TS control register.

Offset Address	Register Name	Total Reset Value
0x0090	PERI_PMC36	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved			vedu_ts_en	reserved	vedu_ts_step			vedu_ts_dly_adjust			vedu_ts_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:9]	RW	reserved	Reserved.
[8]	RW	vedu_ts_en	VEDU TS module enable for controlling the internal ICG.

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[7]	RW	reserved	Reserved.
[6:5]	RW	vedu_ts_step	VEDU TS code step. 00: step = 1 01: step = 2 1x: step = 3
[4:1]	RW	vedu_ts_dly_adjust	VEDU TS crazy path delay. 0x0: −4 0x1: −4 0x2: −4 0x3: −4 0x4: −3 0x5: −2 0x6: −1 0x7: 0 (default) 0x8: +1 0x9: +2 0xA: +3 0xB: +4 0xC: +5 0xD: +6 0xE: +7 0xF: +8
[0]	RW	vedu_ts_sel	VEDU TS crazy path select. 0: path A 1: path B

PERI_PMC37

PERI_PMC37 is CPU TS status register 0.

Offset Address	Register Name	Total Reset Value
0x0094	PERI_PMC37	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record1												reserved				cpu_ts_stat											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	cpu_ts_record1	CPU TS record 1.

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[15:11]	RO	reserved	Reserved.
[10:0]	RO	cpu_ts_stat	CPU TS record.

PERI_PMC38

PERI_PMC38 is CPU TS status register 1.

Offset Address	Register Name	Total Reset Value
0x0098	PERI_PMC38	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record3												reserved				cpu_ts_record2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	cpu_ts_record3	CPU TS record 3.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	cpu_ts_record2	CPU TS record 2.

PERI_PMC39

PERI_PMC39 is CPU TS status register 2.

Offset Address	Register Name	Total Reset Value
0x009C	PERI_PMC39	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record5												reserved				cpu_ts_record4											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	cpu_ts_record5	CPU TS record 5.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	cpu_ts_record4	CPU TS record 4.

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PERI_PMC40

PERI_PMC40 is CPU TS status register 3.

Offset Address	Register Name	Total Reset Value
0x0A0	PERI_PMC40	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cpu_ts_record7				reserved								cpu_ts_record6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	cpu_ts_record7	CPU TS record 7.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	cpu_ts_record6	CPU TS record 6.

PERI_PMC41

PERI_PMC41 is DDR TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00A4	PERI_PMC41	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ddr_ts_record1				reserved								ddr_ts_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	ddr_ts_record1	DDR TS record 1.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	ddr_ts_stat	DDR TS record.

PERI_PMC42

PERI_PMC42 is DDR TS status register 1.

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Offset Address	Register Name	Total Reset Value
0x00A8	PERI_PMC42	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ddr_ts_record3			reserved	ddr_ts_record2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	ddr_ts_record3	DDR TS record 3.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	ddr_ts_record2	DDR TS record 2.

PERI_PMC43

PERI_PMC43 is DDR TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00AC	PERI_PMC43	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ddr_ts_record5			reserved	ddr_ts_record4		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	ddr_ts_record5	DDR TS record 5.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	ddr_ts_record4	DDR TS record 4.

PERI_PMC44

PERI_PMC44 is DDR TS status register 3.

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Offset Address	Register Name	Total Reset Value
0x0B0	PERI_PMC44	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ddr_ts_record7			reserved	ddr_ts_record6		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	ddr_ts_record7	DDR TS record 7.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	ddr_ts_record6	DDR TS record 6.

PERI_PMC45

PERI_PMC45 is core TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_PMC45	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	core_ts_record1			reserved	core_ts_stat		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	core_ts_record1	Core TS record 1.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	core_ts_stat	Core TS record.

PERI_PMC46

PERI_PMC46 is core TS status register 1.

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Offset Address	Register Name	Total Reset Value
0x00B8	PERI_PMC46	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		core_ts_record3		reserved		core_ts_record2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	core_ts_record3	Core TS record 3.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	core_ts_record2	Core TS record 2.

PERI_PMC47

PERI_PMC47 is core TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00BC	PERI_PMC47	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		core_ts_record5		reserved		core_ts_record4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	core_ts_record5	Core TS record 5.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	core_ts_record4	Core TS record 4.

PERI_PMC48

PERI_PMC48 is core TS status register 3.

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Offset Address	Register Name	Total Reset Value
0x0C0	PERI_PMC48	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	core_ts_record7			reserved	core_ts_record6		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	core_ts_record7	Core TS record 7.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	core_ts_record6	Core TS record 6.

PERI_PMC49

PERI_PMC49 is MDA TOP TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_PMC49	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	mda_top_ts_record1			reserved	mda_top_ts_stat		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	mda_top_ts_record1	MDA TOP TS record 1.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	mda_top_ts_stat	MDA TOP TS record.

PERI_PMC50

PERI_PMC50 is MDA TOP TS status register 1.

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Offset Address	Register Name	Total Reset Value
0x00C8	PERI_PMC50	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	mda_top_ts_record3			reserved	mda_top_ts_record2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	mda_top_ts_record 3	MDA TOP TS record 3.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	mda_top_ts_record 2	MDA TOP TS record 2.

PERI_PMC51

PERI_PMC51 is MDA TOP TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_PMC51	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	mda_top_ts_record5			reserved	mda_top_ts_record4		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	mda_top_ts_record 5	MDA TOP TS record 5.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	mda_top_ts_record 4	MDA TOP TS record 4.

PERI_PMC52

PERI_PMC52 is MDA TOP TS status register 3.

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Offset Address	Register Name	Total Reset Value
0x0D0	PERI_PMC52	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	mda_top_ts_record7			reserved	mda_top_ts_record6		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	mda_top_ts_record 7	MDA TOP TS record 7.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	mda_top_ts_record 6	MDA TOP TS record 6.

PERI_PMC53

PERI_PMC53 is VEDU TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00D4	PERI_PMC53	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vedu_ts_record1			reserved	vedu_ts_stat		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	vedu_ts_record1	VEDU TS record 1.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	vedu_ts_stat	VEDU TS record.

PERI_PMC54

PERI_PMC54 is VEDU TS status register 1.

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Offset Address	Register Name	Total Reset Value
0x00D8	PERI_PMC54	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vedu_ts_record3			reserved	vedu_ts_record2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	vedu_ts_record3	VEDU TS record 3.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	vedu_ts_record2	VEDU TS record 2.

PERI_PMC55

PERI_PMC55 is VEDU TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00DC	PERI_PMC55	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vedu_ts_record5			reserved	vedu_ts_record4		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	vedu_ts_record5	VEDU TS record 5.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	vedu_ts_record4	VEDU TS record 4.

PERI_PMC56

PERI_PMC56 is VEDU TS status register 3.

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Offset Address	Register Name	Total Reset Value
0x0E0	PERI_PMC56	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vedu_ts_record7			reserved	vedu_ts_record6		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RO	vedu_ts_record7	VEDU TS record 7.
[15:11]	RO	reserved	Reserved.
[10:0]	RO	vedu_ts_record6	VEDU TS record 6.

PERI_PMC57

PERI_PMC57 is PMC register 57.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_PMC57	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved.

PERI_PMC58

PERI_PMC58 is a PMC_I2C_CFG1 register.

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Offset Address	Register Name	Total Reset Value
0x00E8	PERI_PMC58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pmc_i2c_enable	i2c_int_clear	reserved										pmu_reg7_wt_req	pmu_reg6_wt_req	pmu_reg5_wt_req	pmu_reg4_wt_req	pmu_reg3_wt_req	pmu_reg2_wt_req	pmu_reg1_wt_req	pmu_reg0_wt_req	reserved			pmu_reg_rd_all	reserved	pmu_addr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pmc_i2c_enable	I^2C enable. 0: disabled 1: enabled
[30]	RW	i2c_int_clear	I^2C interrupt status clear.
[29:20]	RW	reserved	Reserved.
[19]	RW	pmu_reg7_wt_req	PMU reg7 write request. If the read value is 0, the operation is complete.
[18]	RW	pmu_reg6_wt_req	PMU reg6 write request. If the read value is 0, the operation is complete.
[17]	RW	pmu_reg5_wt_req	PMU reg5 write request. If the read value is 0, the operation is complete.
[16]	RW	pmu_reg4_wt_req	PMU reg4 write request. If the read value is 0, the operation is complete.
[15]	RW	pmu_reg3_wt_req	PMU reg3 write request. If the read value is 0, the operation is complete.
[14]	RW	pmu_reg2_wt_req	PMU reg2 write request. If the read value is 0, the operation is complete.
[13]	RW	pmu_reg1_wt_req	PMU reg1 write request. If the read value is 0, the operation is complete.
[12]	RW	pmu_reg0_wt_req	PMU reg0 write request. If the read value is 0, the operation is complete.
[11:9]	RW	reserved	Reserved.
[8]	RW	pmu_reg_rd_all	PMU reg0−7 read request. If the read value is 0, the operation is complete.
[7]	RW	reserved	Reserved.
[6:0]	RW	pmu_addr	Address for the I^2C slave of the PMU.

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PERI_PMC59

PERI_PMC59 is a PMC_I2C_CFG2 register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_PMC59	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	pmu_reg3		pmu_reg2		pmu_reg1		pmu_reg0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	pmu_reg3	Shadow of PMU reg3.
[23:16]	RW	pmu_reg2	Shadow of PMU reg2.
[15:8]	RW	pmu_reg1	Shadow of PMU reg1.
[7:0]	RW	pmu_reg0	Shadow of PMU reg0.

PERI_PMC60

PERI_PMC60 is a PMC_I2C_CFG3 register.

Offset Address	Register Name	Total Reset Value
0x00F0	PERI_PMC60	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	pmu_reg7		pmu_reg6		pmu_reg5		pmu_reg4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	pmu_reg7	Shadow of PMU reg7.
[23:16]	RW	pmu_reg6	Shadow of PMU reg6.
[15:8]	RW	pmu_reg5	Shadow of PMU reg5.
[7:0]	RW	pmu_reg4	Shadow of PMU reg4.

PERI_PMC61

PERI_PMC61 is a PMC_I2C_STAT register.

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Offset Address	Register Name	Total Reset Value
0x00F4	PERI_PMC61	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_mst_active	i2c_busy	i2c_abrt_7addr_nack	i2c_abrt_data_nack	i2c_mst_tx_abrt	i2c_arb_lost	i2c_start_det	i2c_stop_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	i2c_mst_active	I^2C operating status.
[6]	RO	i2c_busy	I^2C busy status.
[5]	RO	i2c_abrt_7addr_nack	I^2C slave component address no-acknowledgment interrupt.
[4]	RO	i2c_abrt_data_nack	I^2C write data no-acknowledgment interrupt.
[3]	RO	i2c_mst_tx_abrt	I^2C TX failure interrupt.
[2]	RO	i2c_arb_lost	I^2C bus lost interrupt.
[1]	RO	i2c_start_det	I^2C start bit detection interrupt.
[0]	RO	i2c_stop_det	I^2C stop bit detection interrupt.

PERI_PMC62

PERI_PMC62 is a PMC_I2C_CFG4 register.

Offset Address	Register Name	Total Reset Value
0x00F8	PERI_PMC62	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pmc_i2c_hcnt																pmc_i2c_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	pmc_i2c_hcnt	Number of SCL high-level beats for the PMC I^2C.
[15:0]	RW	pmc_i2c_lcnt	Number of SCL low-level beats for the PMC I^2C.

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PERI_PMC63

PERI_PMC63 is a PMC_I2C_CFG5 register.

Offset Address	Register Name	Total Reset Value
0x00FC	PERI_PMC63	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pmu_avs_reg7_en	pmu_avs_reg6_en	pmu_avs_reg5_en	pmu_avs_reg4_en	pmu_avs_reg3_en	pmu_avs_reg2_en	pmu_avs_reg1_en	pmu_avs_reg0_en	pmu_avs_reg7_mux		pmu_avs_reg6_mux		pmu_avs_reg5_mux		pmu_avs_reg4_mux		pmu_avs_reg3_mux		pmu_avs_reg2_mux		pmu_avs_reg1_mux		pmu_avs_reg0_mux	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23]	RW	pmu_avs_reg7_en	PMU reg7 AVS automatic update enable.
[22]	RW	pmu_avs_reg6_en	PMU reg6 AVS automatic update enable.
[21]	RW	pmu_avs_reg5_en	PMU reg5 AVS automatic update enable.
[20]	RW	pmu_avs_reg4_en	PMU reg4 AVS automatic update enable.
[19]	RW	pmu_avs_reg3_en	PMU reg3 AVS automatic update enable.
[18]	RW	pmu_avs_reg2_en	PMU reg2 AVS automatic update enable.
[17]	RW	pmu_avs_reg1_en	PMU reg1 AVS automatic update enable.
[16]	RW	pmu_avs_reg0_en	PMU reg0 AVS automatic update enable.
[15:14]	RW	pmu_avs_reg7_mux	PMU reg7 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[13:12]	RW	pmu_avs_reg6_mux	PMU reg6 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA

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[11:10]	RW	pmu_avs_reg5_mux	PMU reg5 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[9:8]	RW	pmu_avs_reg4_mux	PMU reg4 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[7:6]	RW	pmu_avs_reg3_mux	PMU reg3 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[5:4]	RW	pmu_avs_reg2_mux	PMU reg2 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[3:2]	RW	pmu_avs_reg1_mux	PMU reg1 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA
[1:0]	RW	pmu_avs_reg0_mux	PMU reg0 AVS automatic update control source. 00: core 01: CPU 10: DDR 11: MDA

PERI_PMC64

PERI_PMC64 is PMC register 64.

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Offset Address	Register Name	Total Reset Value
0x0100	PERI_PMC64	0x0004_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									core_ts_inc_case_sel	reserved		core_avs_ctrl_mux	core_avs_ctrl_sel	core_ts_en_must_inc	core_ts_monitor_en	core_ts_monitor_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved.
[22]	RW	core_ts_inc_case_sel	Voltage increase mode of the core TS AVS. 0: mode 0 1: mode 1
[21:20]	RW	reserved	Reserved.
[19]	RW	core_avs_ctrl_mux	AVS control output mode for the core power domain. 0: PWM DC-DC 1: PMU of the I^2C interface
[18]	RW	core_avs_ctrl_sel	AVS control source of the core power domain. 0: TS 1: HPM
[17]	RW	core_ts_en_must_inc	Core TS AVS mode. 0: normal mode 1: The window voltage must be increased next time if the voltage increases in the monitoring period.
[16]	RW	core_ts_monitor_en	Core TS AVS monitoring enable.
[15:0]	RW	core_ts_monitor_period	Core TS AVS monitoring period.

PERI_PMC65

PERI_PMC65 is PMC register 65.

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Offset Address	Register Name	Total Reset Value
0x0104	PERI_PMC65	0x0004_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									cpu_ts_inc_case_sel	reserved		cpu_avs_ctrl_mux	cpu_avs_ctrl_sel	cpu_ts_en_must_inc	cpu_ts_monitor_en	cpu_ts_monitor_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved.
[22]	RW	cpu_ts_inc_case_sel	Voltage increase mode of the CPU TS AVS. 0: mode 0 1: mode 1
[21:20]	RW	reserved	Reserved.
[19]	RW	cpu_avs_ctrl_mux	AVS control output mode for the CPU power domain. 0: PWM DC-DC 1: PMU of the I^2C interface
[18]	RW	cpu_avs_ctrl_sel	AVS control source of the CPU power domain. 0: TS 1: HPM
[17]	RW	cpu_ts_en_must_inc	CPU TS AVS mode. 0: normal mode 1: The window voltage must be increased next time if the voltage increases in the monitoring period.
[16]	RW	cpu_ts_monitor_en	CPU TS AVS monitoring enable.
[15:0]	RW	cpu_ts_monitor_period	CPU TS AVS monitoring period.

PERI_PMC66

PERI_PMC66 is PMC register 66.

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Offset Address	Register Name	Total Reset Value
0x0108	PERI_PMC66	0x0004_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									ddr_ts_inc_case_sel	reserved		ddr_avs_ctrl_mux	ddr_avs_ctrl_sel	ddr_ts_en_must_inc	ddr_ts_monitor_en	ddr_ts_monitor_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved.
[22]	RW	ddr_ts_inc_case_sel	Voltage increase mode of the DDR TS AVS. 0: mode 0 1: mode 1
[21:20]	RW	reserved	Reserved.
[19]	RW	ddr_avs_ctrl_mux	AVS control output mode for the DDR power domain. 0: PWM DC-DC 1: PMU of the I^2C interface
[18]	RW	ddr_avs_ctrl_sel	AVS control source of the DDR power domain. 0: TS 1: HPM
[17]	RW	ddr_ts_en_must_inc	DDR TS AVS mode. 0: normal mode 1: The window voltage must be increased next time if the voltage increases in the monitoring period.
[16]	RW	ddr_ts_monitor_en	DDR TS AVS monitoring enable.
[15:0]	RW	ddr_ts_monitor_period	DDR TS AVS monitoring period.

PERI_PMC67

PERI_PMC67 is PMC register 67.

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Offset Address	Register Name	Total Reset Value
0x010C	PERI_PMC67	0x0004_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									mda_ts_inc_case_sel	mda_avs_ts_sel	mda_avs_hpm_sel	mda_avs_ctrl_mux	mda_avs_ctrl_sel	mda_ts_en_must_inc	mda_ts_monitor_en	mda_ts_monitor_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved.
[22]	RW	mda_ts_inc_case_sel	Voltage increase mode of the MDA TS AVS. 0: mode 0 1: mode 1
[21]	RW	mda_avs_ts_sel	AVS TS control source of the MDA power domain. 0: VEDU 1: MDA TOP
[20]	RW	mda_avs_hpm_sel	AVS HPM control source of the MDA power domain. 0: VEDU 1: MDA TOP
[19]	RW	mda_avs_ctrl_mux	AVS control output mode for the MDA power domain. 0: PWM DC-DC 1: PMU of the I^2C interface
[18]	RW	mda_avs_ctrl_sel	AVS control source of the MDA power domain. 0: TS 1: HPM
[17]	RW	mda_ts_en_must_inc	MDA TS AVS mode. 0: normal mode 1: The window voltage must be increased next time if the voltage increases in the monitoring period.
[16]	RW	mda_ts_monitor_en	MDA TS AVS monitoring enable.
[15:0]	RW	mda_ts_monitor_period	MDA TS AVS monitoring period.

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Contents

4 Memory Interfaces 4-1
4.1 DDRC 4-1
4.1.1 Overview 4-1
4.1.2 Features 4-1
4.1.3 Function Description 4-2
4.1.4 Operating Mode 4-13
4.1.5 AXI Registers of the DDRC 4-16
4.1.6 DMC Registers of the DDRC 4-43
4.1.7 DDR PHY Registers 4-93
4.2 SPI Flash Controller 4-191
4.2.1 Overview 4-191
4.2.2 Features 4-192
4.2.3 Function Description 4-193
4.2.4 Working Process 4-198
4.2.5 Register Summary 4-202
4.2.6 Register Description 4-203
4.3 NAND Flash Controller 4-218
4.3.1 Overview 4-218
4.3.2 Features 4-218
4.3.3 Function Description 4-219
4.3.4 Operating Modes 4-221
4.3.5 Data Storage Structure 4-223
4.3.6 ECC Mode Selection 4-228
4.3.7 Software Operations 4-228
4.3.8 Notes 4-230
4.3.9 Register Summary 4-230
4.3.10 Register Description 4-233
4.4 SPI NAND Flash Controller 4-261
4.4.1 Overview 4-261
4.4.2 Features 4-262
4.4.3 Function Description 4-263
4.4.4 Working Process 4-267

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4.4.6 ECC Mode Selection....4-273
4.4.7 Register Summary....4-273
4.4.8 Register Description....4-274

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Figures

Figure 4-1 DDRC structure 4-1
Figure 4-2 Connecting the DDRC to two 16-bit DDR3 SDRAMs in 32-bit mode for the Hi3516A 4-3
Figure 4-3 Connecting the DDRC to four 8-bit DDR3 SDRAMs in 32-bit mode for the Hi3516A 4-4
Figure 4-4 Connecting the DDRC to a 16-bit DDR3 SDRAM in 16-bit mode for the Hi3516A 4-5
Figure 4-5 Connecting the DDRC to two 8-bit DDR3 SDRAMs in 16-bit mode for the Hi3516A 4-6
Figure 4-6 Connecting the DDRC to one 16-bit DDR3 SDRAM for the Hi3516D 4-7
Figure 4-7 Connecting the DDRC to two 8-bit DDR3 SDRAMs for the Hi3516D 4-8
Figure 4-8 SFC application block diagram 4-192
Figure 4-9 Timing of the standard SPI interface (write) 4-193
Figure 4-10 Timing of the standard SPI interface (read) 4-193
Figure 4-11 Timing of the dual input/dual output SPI interface 4-194
Figure 4-12 Timing of the dual I/O SPI interface 4-194
Figure 4-13 Timing of the full dual-I/O SPI interface 4-195
Figure 4-14 Timing of the quad input/quad output SPI interface 4-195
Figure 4-15 Timing of the quad I/O SPI interface 4-196
Figure 4-16 Timing of the full quad SPI interface 4-196
Figure 4-17 SPI output timing 4-198
Figure 4-18 Process of reading the flash memory by using related registers in query mode 4-199
Figure 4-19 Process of writing to the flash memory by using related registers in interrupt mode 4-200
Figure 4-20 Process of other operations 4-201
Figure 4-21 Block diagram of NANDC interfaces 4-219
Figure 4-22 Typical timing when the NANDC reads a page of data from the NAND flash 4-220
Figure 4-23 Typical timing when the NANDC programs the NAND flash 4-220
Figure 4-24 Data structure of the driver in 8-bit ECC mode (2 KB page size) 4-223
Figure 4-25 Data structure of the NAND flash in 8-bit ECC mode (2 KB page size) 4-224
Figure 4-26 Data structure of the driver in 8-bit ECC mode (4 KB page size) 4-224

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Figure 4-27 Data structure of the NAND flash in 8-bit ECC mode (4 KB page size).....4-224
Figure 4-28 Data structure of the driver in 24-bit ECC mode (2 KB page size) 4-224
Figure 4-29 Data structure of the NAND flash in 24-bit ECC mode (2 KB page size).....4-224
Figure 4-30 Data structure of the driver in 24-bit ECC mode (4 KB page size) 4-225
Figure 4-31 Data structure of the NAND flash in 24-bit ECC mode (4 KB page size).....4-225
Figure 4-32 Data structure of the driver in 24-bit ECC mode (8 KB page size) 4-225
Figure 4-33 Data structure of the NAND flash in 24-bit ECC mode (8 KB page size).....4-225
Figure 4-34 Data structure of the driver in 40-bit ECC mode (8 KB page size) 4-226
Figure 4-35 Data structure of the NAND flash in 40-bit ECC mode (8 KB page size).....4-226
Figure 4-36 Data structure of the driver in 40-bit ECC mode (16 KB page size) 4-226
Figure 4-37 Data structure of the NAND flash in 40-bit ECC mode (16 KB page size).....4-226
Figure 4-38 Data structure of the driver in 64-bit ECC mode (8 KB page size) 4-227
Figure 4-39 Data structure of the NAND flash in 64-bit ECC mode (8 KB page size).....4-227
Figure 4-40 Data structure of the driver in 64-bit ECC mode (16 KB page size) 4-227
Figure 4-41 Data structure of the NAND flash in 64-bit ECC mode (16 KB page size).....4-228
Figure 4-42 SFC_NAND application block diagram 4-261
Figure 4-43 Write timing of the standard SPI.....4-263
Figure 4-44 Read timing of the standard SPI 4-264
Figure 4-45 Timing in dual-input/dual-output SPI mode 4-264
Figure 4-46 Timing in dual-I/O SPI mode.....4-265
Figure 4-47 Timing in quad-input/quad-output SPI mode.....4-265
Figure 4-48 Timing in quad-I/O SPI mode.....4-266
Figure 4-49 SPI output timing.....4-267
Figure 4-50 (2048+32)-byte data structure of the driver software in 4-bit ECC mode 4-271
Figure 4-51 Data structure of the NAND flash in 4-bit ECC mode 4-271
Figure 4-52 (4096+32)-byte data structure of the driver software in 4-bit ECC mode 4-271
Figure 4-53 (4096+128)- byte data structure of the NAND flash in 4-bit ECC mode 4-271
Figure 4-54 (2048+32)-byte data structure of the driver software in 24-bit ECC mode 4-272
Figure 4-55 (2048+116)-byte data structure of the NAND flash in 24-bit ECC mode 4-272
Figure 4-56 (4096+32)-byte data structure of the driver software in 24-bit ECC mode 4-272
Figure 4-57 (4096+200)-byte data structure of the NAND flash in 24-bit ECC mode 4-273

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Tables

Table 4-1 DDR3 SDRAMs supported by the DDRC 4-2
Table 4-2 Command truth values of the DDRC 4-9
Table 4-3 DDRC address mapping in 32–bit mode 4-12
Table 4-4 DDRC address mapping in 16–bit mode 4-12
Table 4-5 Summary of EMI registers (base address: 0x2011_0000) 4-16
Table 4-6 DMC registers (base address: 0x2011_1000) 4-43
Table 4-7 Summary of DDR PHY registers (base address: 0x2011_8000) 4-93
Table 4-8 Summary of SFC registers (base address: 0x1001_0000) 4-202
Table 4-9 Addresses for the K9F2G08U0M 4-222
Table 4-10 Addresses for the K9GAG08X0M 4-222
Table 4-11 Common commands for operating NAND flash memories 4-223
Table 4-12 Summary of NANDC registers (base address: 0x1000_0000) 4-230
Table 4-13 Boot configuration pins 4-267
Table 4-14 Summary of SPI NAND flash registers (base address: 0x1004_0000) 4-273

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4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR3 SDRAM controller (DDRC) controls access to the DDR3 SDRAM. Figure 4-1 shows the DDRC structure.

Figure 4-1 DDRC structure

4.1.2 Features

The DDRC has the following features:

- One DDR3 SDRAM chip select (CS)
- Configurable DDR3 SDRAM data bus bit width (32 bits or 16 bits) for the Hi3516A, and 16-bit DDR3 SDRAM data bus for the Hi3516D
- A maximum of 1 GB storage capacity for the Hi3516A, and a maximum of 512 MB storage capacity for the Hi3516D
- A maximum of 600 MHz DDR3 SDRAM working frequency and 1200 Mbit/s data rate

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- Various DDR3 SDRAM low-power modes, such as the power-down and self-refresh modes
- Burst8 transfer mode for the DDR3 SDRAM

4.1.3 Function Description

4.1.3.1 Application Block Diagram

The DDRC enables the master devices of the SoC such as the CPU to access the external DDR3 SDRAM. It supports the DDR3 SDRAM that complies with the JEDEC (JESD79) standard after the timing parameter registers of the DDRC are configured by using the CPU. Table 4-1 lists the mainstream DDR3 SDRAMs supported by the DDRC. The descriptions in Table 4-1 are based on the working frequencies of DDR3 SDRAMs. The restrictions such as the capacity are not taken into account.

Table 4-1 DDR3 SDRAMs supported by the DDRC

Vendor	400 MHz	533 MHz	667 MHz
JESD79 (DDR3 standard)	DDR3-800 DDR3-1066 DDR3-1333 DDR3-1600	DDR3-1066 DDR3-1333 DDR3-1600	DDR3-1333 DDR3-1600

NOTE

The maximum working frequency of the DDR3 SDRAM supported by the DDRC is 600 MHz.

For details about the supported component types, see the JEDEC standard and the component data sheet.

The Hi3516A DDRC supports the 32-bit or 16-bit DDR. In 32-bit mode, the DDRC connects to two 16-bit DDR3 SDRAMs or four 4-bit DDR3 SDRAMs; in 16-bit mode, the DDRC connects to one 16-bit DDR3 SDRAM or two 8-bit DDR3 SDRAMs.

Figure 4-2 and Figure 4-3 show the connection between the DDRC and DDR3 SDRAMs in 32-bit mode for the Hi3516A.

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Figure 4-2 Connecting the DDRC to two 16-bit DDR3 SDRAMs in 32-bit mode for the Hi3516A

NOTE

The DDR3 SDRAMx is a 16-bit memory.

The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0], and DDR_ODT) connect to the DDR3 SDRAMx command control signals.
The DDRC command control bus uses the one-drive-two mode.

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Figure 4-3 Connecting the DDRC to four 8-bit DDR3 SDRAMs in 32-bit mode for the Hi3516A

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NOTE

The DDR3 SDRAM*x* is an 8-bit memory.

The DDRC command control signals (DDR_CS, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0], and DDR_ODT) connect to the DDR3 SDRAM*x* command control signals. The DDRC command control bus uses the one-drive-four mode.

Figure 4-4 and Figure 4-5 show the connection between the DDRC and DDR3 SDRAMs in 16-bit mode for the Hi3516A.

Figure 4-4 Connecting the DDRC to a 16-bit DDR3 SDRAM in 16-bit mode for the Hi3516A

NOTE

The DDR3 SDRAM is a 16-bit memory.

The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0]) connect to the DDR3 SDRAM command control signals. The DDRC command control bus uses the one-drive-one mode.

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Figure 4-5 Connecting the DDRC to two 8-bit DDR3 SDRAMs in 16-bit mode for the Hi3516A

NOTE

The DDR3 SDRAM*x* is an 8-bit memory.

The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0]) connect to the DDR3 SDRAM command control signals. The DDRC command control bus uses the one-drive-two mode.

The Hi3516D DDRC supports the 16-bit DDR. The DDRC connects to one 16-bit DDR3 SDRAM or two 8-bit DDR3 SDRAMs.

Figure 4-6 and Figure 4-7 show the connection between the DDRC and DDR3 SDRAMs in 16-bit mode for the Hi3516D.

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Figure 4-6 Connecting the DDRC to one 16-bit DDR3 SDRAM for the Hi3516D

NOTE

The DDR3 SDRAM*x* is a 16-bit memory.

The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0]) connect to the DDR3 SDRAM command control signals. The DDRC command control bus uses the one-drive-one mode.

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Figure 4-7 Connecting the DDRC to two 8-bit DDR3 SDRAMs for the Hi3516D

NOTE

The DDR3 SDRAM*x* is an 8-bit memory.

The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0]) connect to the DDR3 SDRAM command control signals. The DDRC command control bus uses the one-drive-two mode.

4.1.3.2 Function Implementation

As the timings of the DDRC interface comply with the JESD79 standard, the DDRC can access (read or write) data in the DDR3 SDRAM and control the status of the DDR3 SDRAM (including automatic refresh and low power control) by sending the command words of the DDR3 SDRAM.

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Command Truth Value Table

The DDRC can read and write to the DDR3 SDRAM and control command words. Table 4-2 lists the command truth values of the DDRC. For details, see the JEDEC standard and component data sheet.

Table 4-2 Command truth values of the DDRC

Function	DDR3_CKE	DDR3_CSN	DDR3_RASN	DDR3_CASN	DDR3_WEN	DDR3_ADR			DDR3_BA
						15:11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	V	L	V	BA
PRECHARGE ALL	H	L	L	H	L	V	H	V	V
AUTO REFRESH	H	L	L	L	H	V	V	V	V
SELF REFRESH ENTRY	H->L	L	L	L	H	V	V	V	V
SELF REFRESH EXIT	L->H	L	H	H	H	V	V	V	V
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

H: high level; L: low level; V: valid; X: ignored.
ZQ calibration long (ZQCL): starts ZQ calibration on the DDR3 SDRAM when it is initialized during power-on.
ZQ calibration short (ZQCS): starts ZQ calibration on the DDR3 SDRAM when its ambient environment is changed.

Auto Refresh

When DDRC_CFG_TIMING2 [taref] is set to a non-zero value, the DDRC refreshes the DDR3 SDRAM by automatically generating a periodical auto refresh command. At ambient temperature, the DDR3 SDRAM is required to implement 8,192 auto-refresh operations within 64 ms. That is, the auto-refresh cycle is 7.8 μs. The relationship between the value of DDRC_CFG_TIMING2 [taref] (taref) and the auto-refresh cycle T (T = 7.8 μs) is as follows:

$T \geq taref \times (16 \times DDR\ clock\ cycle)$

When DDRC_CFG_TIMING2 [taref] is configured, the internal counter of the DDRC automatically loads the taref value and then counts in decremented mode. When the count

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value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two modes of low-power management: common low-power mode and auto-refresh low-power mode.

When DDRC_CFG_PD [pd_en] is set to 1 to enable the SDRAM low-power mode, and the system is idle (the DDR is not read or written through the DDRC bus interface for a period), the DDR3 SDRAM enters the common low-power mode automatically.

To switch the system mode to standby mode, you can force the DDR3 SDRAM to enter the auto-refresh mode by setting DDRC_CTRL_SREF [sref_req] to 1. In this mode, the power consumption of the DDR3 SDRAM is minimized, data in the DDR3 SDRAM is retained, but the system cannot access the DDR3 SDRAM.

Arbitration Mechanism

The DDRC uses the priority scheduling algorithm and flow control algorithm.

The priority mapping mode can be selected by configuring AXI_QOSCFG0n[pri_map_mode]. If AXI_QOSCFG0n[pri_map_mode] is set to 1, the system bus signal is used as the QoS priority. If AXI_QOSCFG0n[pri_map_mode] is set to 0, AXI_QOSCFG0n[id_map] needs to be configured to select some bits of the ID for QoS configuration. The DDRC adds priority attributes to the read/write commands sent to the bus by configuring AXI_WRPRIn and AXI_RDPRI, and then schedules the commands based on the priority attributes to implement highly effective access to the DDR3 SDRAM.

The DDRC adds response timeout attributes to commands sent to the bus by setting AXI_WRTOUT and AXI_RDTOUT to non-zero values. The mapping mode of the timeout value can be selected by configuring AXI_QOSCFG0n[tout_map_mode]. If AXI_QOSCFG0n[tout_map_mode] is set to 1, the 2 bit select signals of the system bus are used the address to search for one of the four preset timeout values. If AXI_QOSCFG0n[tout_map_mode] is set to 0, AXI_QOSCFG0n[tout_id_map] needs to be configured to select 2 bit signals of the ID as the address to search for one of the four preset timeout values. Then the bus command response timeout is ensured based on the response timeout priority scheduling algorithm.

The DDRC adds the flow control attributes to bus interfaces by configuring DDRC_CFG_PERF [flux_en] and AXI_FLUX0n [flux_cfg0]. The DDRC allocates traffic to each bus interface to ensure sufficient bandwidth of each interface when the traffic is heavy. The commands with the response timeout attributes are not controlled after the timeout period elapse.

Traffic Statistics and Command Latency Statistics

The DDRC supports traffic statistics. The interface read and write traffic statistics can be collected to determine whether dynamic frequency scaling (DFS) is required, that is, whether to increase or reduce the DDRC frequency. The DDRC can collect the read and write traffic statistics of a specific ID, or the overall read and write traffic statistics. The DDRC can also collect DDR interface usage statistics. The statistic counter supports the continuous counts and one-time count. When counting continuously, the counter is a non-saturating counter, and it is wrapped when the maximum count is reached to facilitate the continuous count. Therefore, the system needs to read the count value before the counter is wrapped. When

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counting for only one time, the counter stops counting when the statistic time elapses. The system can obtain the instantaneous traffic and latency by using this function.

The DDRC can collect command latency statistics, including the maximum latency of the read and write access to a specific ID and the accumulative latency statistics.

The process for collecting statistics is as follows:

Step 1 Set the statistic mode to continuous triggering or one-time triggering by configuring DDRC_CFG_PERF.perf_mode. If the one-time triggering is selected, set the perf_prd field to configure the statistic cycle.

Step 2 Set the ID for which statistics are to be collected by configuring DDRC_CFG_STAID.

Step 3 Set the mask value of the ID by configuring DDRC_CFG_STAIDMSK. The DDRC determines whether to collect statistics of the current access based on sta_idmask and the accessed ID. Statistics of multiple IDs can be collected by using this method.

Step 4 Enable the statistic function by configuring DDRC_CTRL_PERF[perf_en]. For the one-time count, counting is complete when DDRC_CTRL_PERF[perf_en] restores to 0. For the continuous count, the software needs to write 0 to DDRC_CTRL_PERF[perf_en] to stop counting.

Step 5 Observe the collected statistics by using DDRC_HIS_FLUX_WR, DDRC_HIS_FLUX_RD, DDRC_HIS_FLUX_WCMD, DDRC_HIS_FLUX_RCMD, DDRC_HIS_FLUXID_WR, DDRC_HIS_FLUXID_RD, DDRC_HIS_FLUXID_WCMD, DDRC_HIS_FLUXID_RCMD, DDRC_HIS_WLATCNT0, DDRC_HIS_WLATCNT1, DDRC_HIS_RLATCNT0, DDRC_HIS_RLATCNT1, and DDRC_HIS_INHERE_RLAT_CNT.

----End

Address Mapping

The DDRC can convert the access address for the system bus into that for the DDR3 SDRAM. You can set the address mapping mode to row-bank-column (RBC) by configuring DDRC_CFG_RNKVOL[mem_map]. Currently only the RBC mode is supported. Then you can set the SDRAM row and column address bit width by configuring DDRC_CFG_RNKVOL[mem_row] and DDRC_CFG_RNKVOL[mem_col]. The DDRC then converts the system bus address into the DDR3 SDRAM address based on the address mapping algorithm.

The following describes the mapping algorithms for the system bus address and the address for the DDR3 SDRAM by using the RBC mode as an example. Assume that the system bus address is BUSADR[31:0], the valid address is BUSADR[m – 1:0], and the address for the DDR3 SDRAM is DDRADR[14:0]. When DDRADR[14:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when DDRADR[13:0] serves as the column address, its valid address is DDRCOL[y – 1:0]. In addition, the bank address for the DDR is DDRBA[z – 1:0] and the width of the storage data bus of the DDRC is DW. In this case, the address mappings are as follows:

- When DDRC_CFG_RNKVOL[mem_map] is set to 2b00, the RBC mapping mode is as follows:

  BUSADR[m − 1:0] = {DDRROW[x − 1:0], DDRBA[z − 1:0], DDRCOL[y − 1:0], DW{b0}}

  In the preceding expressions, the following condition is met: m = x + y + z + DW

  - When the DDRC is in 32-bit mode, the value of DW is 2.

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– When the DDRC is in 16-bit mode, the value of DW is 1.

- When DDRC_CFG_RNKVOL[mem_map] is set to 2'b00 and A10 acts as the AP function bit of the DDR, the mapping between the system bus addresses and the DDR3 SDRAM addresses is shown in Table 4-4.

  Table 4-3 and Table 4-4 describe the address mappings in the RBC mode.

Table 4-3 DDRC address mapping in 32–bit mode

Memory Type	Row address Width	Column address Width	DDR BA			Row Address or Column Address	DDR ADR								
Mbit x bw			2	1	0		15	14	13	12	11	10/AP	9	8	7:0
1 Gbit 8 banks															
64 x 16	13	10	14	13	12	Row address	-	-	-	27	26	25	24	23	22:15
						Column address	-	-	-	-	-	AP	11	10	9:2
2 Gbits 8 banks															
128 x 16	14	10	14	13	12	Row address	-	-	28	27	26	25	24	23	22:15
						Column address	-	-	-	-	-	AP	11	10	9:2
4 Gbits 8 banks															
256 x 16	15	10	14	13	12	Row address	-	29	28	27	26	25	24	23	22:15
						Column address	-	-	-	-	-	AP	11	10	9:2
8 Gbits 8 banks															
512 x 16	16	10	13	12	11	Row address	30	29	28	27	26	25	24	23	22:15
						Column address	-	-	-	-	-	AP	11	10	9:2

Table 4-4 DDRC address mapping in 16–bit mode

Memory Type	Row address Width	Column address Width	DDR BA			Row Address or Column Address	DDR ADR								
Mbit x bw			2	1	0		15	14	13	12	11	10/AP	9	8	7:0
1 Gbits 8 banks															

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Memory Type	Row address Width	Column address Width	DDR BA			Row Address or Column Address	DDR ADR								
Mbit x bw			2	1	0		15	14	13	12	11	10/AP	9	8	7:0
64 x16	13	10	13	12	11	Row address	-	-	-	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1
2 Gbits 8 banks															
128 x16	14	10	13	12	11	Row address	-	-	27	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1
4 Gbits 8 banks															
256 x16	15	10	13	12	11	Row address	-	28	27	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1

4.1.4 Operating Mode

4.1.4.1 Clock Gating

After the system enters the low-power mode, the working clock of the DDRC can be disabled. Before the system restores to the normal mode, the working clock of the DDRC must be enabled.

To disable the working clock after the DDRC enters the low-power mode, perform the following steps:

Step 1 Set DDRC_CTRL_SREF[sref_req] to 1 to request to enter the self-refresh mode.

Step 2 Query DDRC_CURR_FUNC[in_sref] until its value is 1. It indicates that the DDRC enters the low-power mode.

Step 3 Disable the DDRC clock.

Step 4 Enter the low-power mode.

----End

To enable the working clock after the DDRC exits the low-power mode, perform the following steps:

Step 1 Enable the DDRC clock when the system runs in normal mode.

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Step 2 Set PLLCTRL[31:0] to 0x2 to power down the PLL.

Step 3 Wait 1 μs, and set PLLCTRL[31:0] to 0x0 to enable the PLL to exit the power-down mode.

Step 4 Set PHYCTRL1 to 0x780078 to reset the PLL.

Step 5 Wait 1 μs and set PHYCTRL1 to 0x700070 to deassert the reset on the PLL.

Step 6 Set PHYINITCTRL to 0x0000_000B.

Step 7 Query PHYINITCTRL[init_en] until its value is 0, which indicates that PLL initialization and impedance calibration are complete.

Step 8 Set DDRC_CTRL_SREF[sref_req] to 0 to request to exit the self-refresh mode.

Step 9 Query DDRC_CURR_FUNC[in_sref] until its value is 0, which indicates that the DDRC exits the low-power mode.

Step 10 Set DDRC_CTRL_SREF[sref_done] to 1.

Step 11 The system accesses the DDR properly.

----End

4.1.4.2 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDR3 DRAM must be reinitialized according to the following initialization processes.

4.1.4.3 Initializing the DDR3 SDRAM

After power-on, the system can access the DDR3 SDRAM only when the DDR3 SDRAM is initialized. Before initializing the DDR3 SDRAM, note the following:

- Power on the DDR3 SDRAM by following the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR3 SDRAM after the system runs in normal mode.

In DDRC 32-bits, the total capacity of DDR3 SDRAMs is 2 Gbits. The DDRC SDRAMs can be two 16-bit DDR3 SDRAMs (capacity of 1 Gbit for each) or four 8-bit DDR3 SDRAMs (capacity of 512 Mbits for each). The following describes the procedure for initializing the DDRC when the ratio of the working frequency of the DDRC to that of the DDR3 is 1:2 (400 MHz for the DDRC, 800 MHz (1.6 Gbit/s) for the DDR3):

Step 1 Set DDRC_CFG_SREF to 0x8100 to back-press the DDRC back-pressure commands when the DDRC enters the auto-refresh mode.

Step 2 Set DDRC_CFG_AREF to 0x0 to disable auto-refresh during initialization.

Step 3 Set DDRC_CFG_PD to disable the power-down function during initialization.

Step 4 Set DDRC_CFG_WORKMODE to 0x11002011.

Step 5 Set DDRC_CFG_DDRMODE to 0x26 to set the DDR bit width to 32 bits, DDR type to DDR3, and DDRC burst length to BL4.

NOTE

The bit width varies according to DDRs. You can change the value of DDRC_CFG_DDRMODE to configure the bit width based on the used DDR.

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Step 6 Set DDRC_CFG_RNKVOL to 0x132.

NOTE

The row and column bit widths vary according to DDRs. Change the value of DDRC_CFG_RNKVOL based on the used DDR.

Step 7 Set DDRC_CFG_TIMING0−DDRC_CFG_TIMING5 to 0x47421818, 0x3F4AE0A0, 0x4601C000, 0x9C6, 0x820F18 and 0x2707 respectively to set DDR timing parameters.

Step 8 Set DDRC_CFG_ODT to 0x1 to enable ODT on write or disable ODT on read.

Step 9 Set PHYTIMER0, to 0x80FFFF respectively to configure the PHY timing.

Step 10 Set PLLTIMER to 0x80000080, respectively to configure the PHY timing.

Step 11 Set DLYMEASCTRL to 0x465, respectively to configure the PHY timing.

Step 12 Set DRAMCFG to 0x22 to set the DDR type to DDR3.

NOTE

Set DRAMCFG[ma2t] to 1 only when the frequency ratio is 1:2.

Step 13 Set ACPHYCTL4 to 0xFFFF0770.

NOTE

ACPHYCTL4 is a register related to 2T timing. It needs to be configured only when the frequency ratio is 1:2.

Step 14 Set DRAMTIMER0−DRAMTIMER4 to 0xC3B0EECC, 0x11407108, 0x24084140, 0xEA100240 and 0x6430 respectively to set DDR timing parameters.

Step 15 Set ODTCR to 0x1 to ensure consistency with the DDRC.

Step 16 Set MISC to 0x40609.

NOTE

- MISC[cfg_rl] = CL − 2
- MISC[cfg_wl] = CWL − 1

Step 17 Set MODEREG01 to 0x61F24.

Step 18 Set MODEREG23 to 0x28.

Step 19 Set PHYINITCTRL to 0x17FF to start the PHY for initialization.

Step 20 Software queries PHYINITCTRL[init_en] until its value is 0, which indicates that initialization is complete.

Step 21 Set DDRC_CFG_TIMING2 to 0x4601C0C0 to enable auto-refresh.

Step 22 Set DDRC_CTRL_SREF to 0x2 to enable the DDRC to exit the self-refresh mode.

Step 23 Software queries DDRC_CURR_FUNC[in_sref] until its value is 0, which indicates that the DDRC exits self-refresh.

Step 24 Set DDRC_CTRL_SREF[sref_done] to 1.

----End

After the preceding steps are complete, the DDR3 SDRAM works properly.

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NOTE

The initialization procedure applies to the Hi3516A and the Hi3516D. However, the register values vary according to the DDR type and clock frequency.

4.1.4.4 Low-Power Configuration

The DDRC supports two types of low-power modes for the DDR3 SDRAM: DDR3 SDRAM power-down mode and DDR3 SDRAM self-refresh mode.

When DDRC_CFG_PD[pd_en] and DDRC_CFG_PD[pd_prd] are set to valid values, the DDRC automatically forces the DDR3 SDRAM to enter the low-power mode if the system is idle. When DDRC_CFG_PD[pd_en] is set to 1 and the DDRC does not access the DDRn SDRAM within DDRC_CFG_PD[pd_prd] bus clock cycles, the DDRC forces the DDRn SDRAM to enter the low-power mode.

When DDRC_CTRL_SREF[sr_req] is set to 1, the DDRC forces the DDR3 SDRAM to enter the self-refresh mode without responding to the bus requests after completing the current access operation.

4.1.5 AXI Registers of the DDRC

4.1.5.1 Register Summary

Table 4-5 describes AXI registers.

NOTE

The variable **ports** in the offset addresses indicates the number of AXI ports and ranges from 0 to 6.

Table 4-5 Summary of EMI registers (base address: 0x2011_0000)

Offset Address	Register	Description	Page
0x000	AXI_CONFIG	DDRC function configuration register	4-17
0x004	AXI_CKGCFG	DDRC clock gating configuration register	4-19
0x01C	AXI_STATUS	DDRC interface status register	4-20
0x020	AXI_CHCFG0	MDDRC channel configuration register 0	4-21
0x024	AXI_CHCFG1	MDDRC channel configuration register 1	4-22
0x028	AXI_CHCFG2	MDDRC channel configuration register 2	4-24
0x02C	AXI_CHCFG3	MDDRC channel configuration register 3	4-26
0x030	AXI_CHCFG4	MDDRC channel configuration register 4	4-28
0x034	AXI_CHCFG5	MDDRC channel configuration register 5	4-29

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Offset Address	Register	Description	Page
0x038	AXI_LPCFG	MDDRC low-power zone configuration register	4-30
0x040 + 0x4 x *ports*	AXI_QOSCFG0	DDRC QoS configuration register 0	4-31
0x080 + 0x4 x *ports*	AXI_QOSCFG1	DDRC QoS configuration register 1	4-32
0x0C0 + 0x4 x *ports*	AXI_WRPRI	DDRC write command priority configuration register	4-33
0x100 + 0x4 x *ports*	AXI_RDPRI	DDRC read command priority configuration register	4-34
0x140 + 0x4 x *ports*	AXI_WRTOUT	DDRC write command timeout configuration register	4-36
0x180 + 0x4 x *ports*	AXI_RDTOUT	DDRC read command timeout configuration register	4-36
0x200 + 0x4 x *ports*	AXI_OSTDCFG0	DDRC port command outstanding configuration register 0	4-37
0x240	AXI_OSTDCFG1	DDRC port command outstanding configuration register 1	4-38
0x244	AXI_OSTDCFG2	DDRC port command outstanding configuration register 2	4-38
0x248	AXI_OSTDSTATUS	DDRC channel command outstanding status register	4-41
0x280 + 0x4 x *ports*	AXI_FLUX0	DDRC port bandwidth traffic control configuration register for channel 0	4-41

4.1.5.2 Register Description

AXI_CONFIG

AXI_CONFIG is a DDRC function configuration register.

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Offset Address	Register Name	Total Reset Value
0x000	AXI_CONFIG	0x0006_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													wr_rcv_mode	exclusive_en	rd_wrap_split_en	reserved												bank_width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RW	wr_rcv_mode	Mode of receiving the write command over the DDRC AXI port. 0: The write command is received directly. 1: The write command is received only after the expected written data arrives.
[17]	RW	exclusive_en	Exclusive command enable. 0: disabled 1: enabled
[16]	RW	rd_wrap_split_en	WRAP read command split enable. 0: not split 1: split
[15:4]	RO	reserved	Reserved.
[3:0]	RW	bank_width	Bank bit width. 1000: 256 bits 1001: 512 bits 1010: 1 KB 1011: 2 KB 1100: 4 KB 1101: 8 KB 1110: 16 KB 1111: 32 KB Other values: reserved For example, if the column is 10 for a 32-bit DDR, the bank width is calculated as follows: bank_width = (32/8) x (2^10) = 4 KB

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AXI_CKGCFG

AXI_CKGCFG is a DDRC clock gating configuration register.

Offset Address	Register Name	Total Reset Value
0x004	AXI_CKGCFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			sta_ckg_pub0	reserved			sta_ckg_dmc0	reserved			sta_ckg_apb	reserved			dyn_ckg_rdr	reserved								dyn_ckg_axi6	dyn_ckg_axi5	dyn_ckg_axi4	dyn_ckg_axi3	dyn_ckg_axi2	dyn_ckg_axi1	dyn_ckg_axi0
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved.
[28]	RW	sta_ckg_pub0	Static clock gating for PUB0. 0: disabled 1: enabled
[27:25]	RW	reserved	Reserved
[24]	RW	sta_ckg_dmc0	Dynamic clock gating for DMC0. 0: disabled 1: enabled
[23:21]	RO	reserved	Reserved.
[20]	RW	sta_ckg_apb	Static clock gating for the register configuration module. 0: disabled 1: enabled
[19:17]	RO	reserved	Reserved.
[16]	RW	dyn_ckg_rdr	Dynamic clock gating for the REORDER module. 0: The clock is always enabled. 1: Clock gating is automatic when the module is idle.
[15:7]	RW	reserved	Reserved
[6]	RW	dyn_ckg_axi6	Dynamic clock gating for AXI port 6. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[5]	RW	dyn_ckg_axi5	Dynamic clock gating for AXI port 5. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.

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[4]	RW	dyn_ckg_axi4	Dynamic clock gating for AXI port 4. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[3]	RW	dyn_ckg_axi3	Dynamic clock gating for AXI port 3. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[2]	RW	dyn_ckg_axi2	Dynamic clock gating for AXI port 2. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[1]	RW	dyn_ckg_axi1	Dynamic clock gating for AXI port 1. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[0]	RW	dyn_ckg_axi0	Dynamic clock gating for AXI port 0. 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.

AXI_STATUS

AXI_STATUS is a DDRC interface status register.

Offset Address	Register Name	Total Reset Value
0x01C	AXI_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									axist6	axist5	axist4	axist3	axist2	axist1	axist0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6]	RO	axist6	Status of controller bus interface 6. 0: The interface is idle. 1: A command is being executed.
[5]	RO	axist5	Status of controller bus interface 5. 0: The interface is idle. 1: A command is being executed.
[4]	RO	axist4	Status of controller bus interface 4. 0: The interface is idle. 1: A command is being executed.

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[3]	RO	axist3	Status of controller bus interface 3. 0: The interface is idle. 1: A command is being executed.
[2]	RO	axist2	Status of controller bus interface 2. 0: The interface is idle. 1: A command is being executed.
[1]	RO	axist1	Status of controller bus interface 1. 0: The interface is idle. 1: A command is being executed.
[0]	RO	axist0	Status of controller bus interface 0. 0: The interface is idle. 1: A command is being executed.

AXI_CHCFG0

AXI_CHCCFG0 is MDDRC channel configuration register 0.

Offset Address	Register Name	Total Reset Value
0x020	AXI_CHCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ch_addr_msk_idx
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved

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[2:0]	RW	ch_addr_msk_idx	Sequence number of mask for the address space index. Four consecutive bits in the address are obtained for searching the channel configuration table. 000: addr[ADDR_WIDTH − 1: ADDR_WIDTH − 4] 001: addr[ADDR_WIDTH − 2: ADDR_WIDTH − 5] 010: addr[ADDR_WIDTH − 3: ADDR_WIDTH − 6] 011: addr[ADDR_WIDTH − 4: ADDR_WIDTH − 7] 100: addr[ADDR_WIDTH − 5: ADDR_WIDTH − 8] 101: addr[ADDR_WIDTH − 6: ADDR_WIDTH − 9] 110: addr[ADDR_WIDTH − 7: ADDR_WIDTH − 10] 111: addr[ADDR_WIDTH − 8: ADDR_WIDTH − 11] ADDR_WIDTH: bit width of the system address (32 bits to 40 bits) Prevent upper-bit addresses from being wrapped. For example, when the address bit width is 32 bits, if it is set to 3, addr[31:29] must be fixed.

AXI_CHCFG1

AXI_CHCCFG1 is MDDRC channel configuration register 1.

Offset Address	Register Name	Total Reset Value
0x024	AXI_CHCFG1	0x0000_0000

Bit	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Name	ch_start15	ch_start14	ch_start13	ch_start12	ch_start11	ch_start10	ch_start9	ch_start8	ch_start7	ch_start6	ch_start5	ch_start4	ch_start3	ch_start2	ch_start1	ch_start0
Reset	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

Bits	Access	Name	Description
[31:30]	RW	ch_start15	Channel configuration table, start channel of address space 15. 0−3 correspond to channels 0−3.
[29:28]	RW	ch_start14	Channel configuration table, start channel of address space 14. 0−3 correspond to channels 0−3.
[27:26]	RW	ch_start13	Channel configuration table, start channel of address space 13. 0−3 correspond to channels 0−3.
[25:24]	RW	ch_start12	Channel configuration table, start channel of address space 12. 0−3 correspond to channels 0−3.
[23:22]	RW	ch_start11	Channel configuration table, start channel of address space 11. 0−3 correspond to channels 0−3.

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[21:20]	RW	ch_start10	Channel configuration table, start channel of address space 10. 0−3 correspond to channels 0−3.
[19:18]	RW	ch_start9	Channel configuration table, start channel of address space 9. 0−3 correspond to channels 0−3.
[17:16]	RW	ch_start8	Channel configuration table, start channel of address space 8. 0−3 correspond to channels 0−3.
[15:14]	RW	ch_start7	Channel configuration table, start channel of address space 7. 0−3 correspond to channels 0−3.
[13:12]	RW	ch_start6	Channel configuration table, start channel of address space 6. 0−3 correspond to channels 0−3.
[11:10]	RW	ch_start5	Channel configuration table, start channel of address space 5. 0−3 correspond to channels 0−3.
[9:8]	RW	ch_start4	Channel configuration table, start channel of address space 4. 0−3 correspond to channels 0−3.
[7:6]	RW	ch_start3	Channel configuration table, start channel of address space 3. 0−3 correspond to channels 0−3.
[5:4]	RW	ch_start2	Channel configuration table, start channel of address space 2. 0−3 correspond to channels 0−3.
[3:2]	RW	ch_start1	Channel configuration table, start channel of address space 1. 0−3 correspond to channels 0−3.
[1:0]	RW	ch_start0	Channel configuration table, start channel of address space 0. 0−3 correspond to channels 0−3.

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AXI_CHCFG2

AXI_CHCCFG2 is MDDRC channel configuration register 2.

Offset Address	Register Name	Total Reset Value
0x028	AXI_CHCFG2	0x0000_0000

Bit	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Name	ch_mode15	ch_mode14	ch_mode13	ch_mode12	ch_mode11	ch_mode10	ch_mode9	ch_mode8	ch_mode7	ch_mode6	ch_mode5	ch_mode4	ch_mode3	ch_mode2	ch_mode1	ch_mode0
Reset	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

Bits	Access	Name	Description
[31:30]	RW	ch_mode15	Channel configuration table, channel mode of address space 15. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[29:28]	RW	ch_mode14	Channel configuration table, channel mode of address space 14. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[27:26]	RW	ch_mode13	Channel configuration table, channel mode of address space 13. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[25:24]	RW	ch_mode12	Channel configuration table, channel mode of address space 12. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[23:22]	RW	ch_mode11	Channel configuration table, channel mode of address space 11. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

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[21:20]	RW	ch_mode10	Channel configuration table, channel mode of address space 10. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[19:18]	RW	ch_mode9	Channel configuration table, channel mode of address space 9. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[17:16]	RW	ch_mode8	Channel configuration table, channel mode of address space 8. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[15:14]	RW	ch_mode7	Channel configuration table, channel mode of address space 7. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[13:12]	RW	ch_mode6	Channel configuration table, channel mode of address space 6. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[11:10]	RW	ch_mode5	Channel configuration table, channel mode of address space 5. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[9:8]	RW	ch_mode4	Channel configuration table, channel mode of address space 4. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

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[7:6]	RW	ch_mode3	Channel configuration table, channel mode of address space 3. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[5:4]	RW	ch_mode2	Channel configuration table, channel mode of address space 2. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[3:2]	RW	ch_mode1	Channel configuration table, channel mode of address space 1. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[1:0]	RW	ch_mode0	Channel configuration table, channel mode of address space 0. 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

AXI_CHCFG3

AXI_CHCCFG3 is MDDRC channel configuration register 3.

Offset Address	Register Name	Total Reset Value
0x02C	AXI_CHCFG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch_invld15	ch_invld14	ch_invld13	ch_invld12	ch_invld11	ch_invld10	ch_invld9	ch_invld8	ch_invld7	ch_invld6	ch_invld5	ch_invld4	ch_invld3	ch_invld2	ch_invld1	ch_invld0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15]	RW	ch_invld15	Channel configuration table, address space 15 mask enable. 0: The current address space is valid. 1: The current address space is invalid.

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[14]	RW	ch_invld14	Channel configuration table, address space 14 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[13]	RW	ch_invld13	Channel configuration table, address space 13 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[12]	RW	ch_invld12	Channel configuration table, address space 12 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[11]	RW	ch_invld11	Channel configuration table, address space 11 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[10]	RW	ch_invld10	Channel configuration table, address space 10 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[9]	RW	ch_invld9	Channel configuration table, address space 9 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[8]	RW	ch_invld8	Channel configuration table, address space 8 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[7]	RW	ch_invld7	Channel configuration table, address space 7 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[6]	RW	ch_invld6	Channel configuration table, address space 6 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[5]	RW	ch_invld5	Channel configuration table, address space 5 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[4]	RW	ch_invld4	Channel configuration table, address space 4 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[3]	RW	ch_invld3	Channel configuration table, address space 3 mask enable. 0: The current address space is valid. 1: The current address space is invalid.

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[2]	RW	ch_invld2	Channel configuration table, address space 2 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[1]	RW	ch_invld1	Channel configuration table, address space 1 mask enable. 0: The current address space is valid. 1: The current address space is invalid.
[0]	RW	ch_invld0	Channel configuration table, address space 0 mask enable. 0: The current address space is valid. 1: The current address space is invalid.

AXI_CHCFG4

AXI_CHCCFG4 is MDDRC channel configuration register 4.

Offset Address	Register Name	Total Reset Value
0x030	AXI_CHCFG4	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ch_sect7	ch_sect6	ch_sect5	ch_sect4	ch_sect3	ch_sect2	ch_sect1	ch_sect0
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	ch_sect7	Channel configuration table, position of the channel section to which address space 7 is mapped.
[27:24]	RW	ch_sect6	Channel configuration table, position of the channel section to which address space 6 is mapped.
[23:20]	RW	ch_sect5	Channel configuration table, position of the channel section to which address space 5 is mapped.
[19:16]	RW	ch_sect4	Channel configuration table, position of the channel section to which address space 4 is mapped.
[15:12]	RW	ch_sect3	Channel configuration table, position of the channel section to which address space 3 is mapped.
[11:8]	RW	ch_sect2	Channel configuration table, position of the channel section to which address space 2 is mapped.
[7:4]	RW	ch_sect1	Channel configuration table, position of the channel section to which address space 1 is mapped.
[3:0]	RW	ch_sect0	Channel configuration table, position of the channel section to which address space 0 is mapped.

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AXI_CHCFG5

AXI_CHCCFG5 is MDDRC channel configuration register 5.

Offset Address	Register Name	Total Reset Value
0x034	AXI_CHCFG5	0xFEDC_BA98

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ch_sect15	ch_sect14	ch_sect13	ch_sect12	ch_sect11	ch_sect10	ch_sect9	ch_sect8
Reset	1 1 1 1	1 1 1 0	1 1 0 1	1 1 0 0	1 0 1 1	1 0 1 0	1 0 0 1	1 0 0 0

Bits	Access	Name	Description
[31:28]	RW	ch_sect15	Channel configuration table, position of the channel section to which address space 15 is mapped.
[27:24]	RW	ch_sect14	Channel configuration table, position of the channel section to which address space 14 is mapped.
[23:20]	RW	ch_sect13	Channel configuration table, position of the channel section to which address space 13 is mapped.
[19:16]	RW	ch_sect12	Channel configuration table, position of the channel section to which address space 12 is mapped.
[15:12]	RW	ch_sect11	Channel configuration table, position of the channel section to which address space 11 is mapped.
[11:8]	RW	ch_sect10	Channel configuration table, position of the channel section to which address space 10 is mapped.
[7:4]	RW	ch_sect9	Channel configuration table, position of the channel section to which address space 9 is mapped.
[3:0]	RW	ch_sect8	Channel configuration table, position of the channel section to which address space 8 is mapped.

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AXI_LPCFG

AXI_LPCFG is a low-power zone configuration register of the MDDRC.

Offset Address	Register Name	Total Reset Value
0x038	AXI_LPCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lp_zone_size																reserved															lp_zone_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lp_zone_size	Size of the low-power zone. The zone size (in MB) equals lp_zone_size plus 1 and increases by the multiple of 2. 0x0000: 1 MB 0x0001: 2 MB 0x0003: 4 MB 0x0007: 8 MB ... If the address space where the low-power zone is located is dual-/quad-channel interleaved, the size of the low-power zone cannot exceed half or a quarter of the address space.
[15:1]	RW	reserved	Reserved
[0]	RW	lp_zone_en	Low-power zone enable. 0: disabled 1: enabled

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AXI_QOSCFG0

AXI_QOSCFG0 is DDRC QoS configuration register 0.

Offset Address	Register Name	Total Reset Value
0x040 + 0x4 x *ports* (*ports* = 0–6)	AXI_QOSCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pri_deliver_en	push_deliver_en	reserved					tout_map_mode	tout_id_map								reserved			pri_map_mode	pri_id_map											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pri_deliver_en	Port priority deliver enable. 0: disabled 1: enabled
[30]	RW	push_deliver_en	Push priority deliver enable. 0: disabled 1: enabled
[29:25]	RO	reserved	Reserved.
[24]	RW	tout_map_mode	Timeout mapping mode of the read/write command. 0: mapping mode specified by tout_id_map 1: mapping mode specified by the command associated signal wr(rd)_tout_sel
[23:16]	RW	tout_id_map	Two bits of the read/write command ID for timeout configuration. id_map[7:4]: bit[1] for ID mapping id_map[3:0]: bit[0] for ID mapping For example, if ID_MAP is set to 0x32, {ID[3], ID[2]} of the read/write command ID is used for ID mapping and priority configuration. Note that the lower four bits of the read/write command ID indicate the AXI port ID. That is, read/write command ID = {Bus ID, 4-bit AXI port ID}.

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[15:13]	RO	reserved	Reserved.
[12]	RW	pri_map_mode	Priority mapping mode of the read/write command. 0: mapping mode specified by pri_id_map 1: QoS mapping mode specified by using the AxQOS[2:0] signal of the AXI4 read/write command
[11:0]	RW	pri_id_map	Three bits of the read/write command ID for QoS configuration. pri_id_map[11:8]: bit[2] for ID mapping pri_id_map[7:4]: bit[1] for IP mapping pri_id_map[3:0]: bit[0] for ID mapping For example, if ID_MAP is set to 0x320, {ID[3], ID[2], ID[0]} of the read/write command ID is used for ID mapping and priority configuration. Note that the lower four bits of the read/write command ID indicate the AXI port ID. That is, read/write command ID = {Bus ID, 4-bit AXI port ID}.

AXI_QOSCFG1

AXI_QOSCFG1 is a DDRC QoS configuration register 1.

Offset Address	Register Name	Total Reset Value
0x080 + 0x4 x *ports* (*ports* = 0–6)	AXI_QOSCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								wr_pri_apt				wr_age_prd				reserved								rd_pri_apt				rd_age_prd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:20]	RW	wr_pri_apt	Write command priority adaptation cycle. 0x0: disabled 0x1-0xF: (*n* x 16) clock cycles
[19:16]	RW	wr_age_prd	Write command aging cycle. 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles
[15:8]	RO	reserved	Reserved.
[7:4]	RW	rd_pri_apt	Read command priority adaptation cycle. 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles

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[3:0]	RW	rd_age_prd	Read command aging cycle. 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles

AXI_WRPRI

AXI_WRPRI is a DDRC write command priority configuration register.

Offset Address	Register Name	Total Reset Value
0x0C0 + 0x4 x *ports* (*ports* = 0–6)	AXI_WRPRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	wr_pri7			reserved	wr_pri6			reserved	wr_pri5			reserved	wr_pri4			reserved	wr_pri3			reserved	wr_pri2			reserved	wr_pri1			reserved	wr_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:28]	RW	wr_pri7	Priority when the write command ID mapping is 7. 000: highest priority ... 111: lowest priority
[27]	RO	reserved	Reserved.
[26:24]	RW	wr_pri6	Priority when the write command ID mapping is 6. 000: highest priority ... 111: lowest priority
[23]	RO	reserved	Reserved.
[22:20]	RW	wr_pri5	Priority when the write command ID mapping is 5. 000: highest priority ... 111: lowest priority
[19]	RO	reserved	Reserved.
[18:16]	RW	wr_pri4	Priority when the write command ID mapping is 4. 000: highest priority ... 111: lowest priority

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[15]	RO	reserved	Reserved.
[14:12]	RW	wr_pri3	Priority when the write command ID mapping is 3. 000: highest priority ... 111: lowest priority
[11]	RO	reserved	Reserved.
[10:8]	RW	wr_pri2	Priority when the write command ID mapping is 2. 000: highest priority ... 111: lowest priority
[7]	RO	reserved	Reserved.
[6:4]	RW	wr_pri1	Priority when the write command ID mapping is 1. 000: highest priority ... 111: lowest priority
[3]	RO	reserved	Reserved.
[2:0]	RW	wr_pri0	Priority when the write command ID mapping is 0. 000: highest priority ... 111: lowest priority

AXI_RDPRI

AXI_RDPRI is a DDRC read command priority configuration register.

Offset Address	Register Name	Total Reset Value
0x100 + 0x4 x *ports* (*ports* = 0–6)	AXI_RDPRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rd_pri7			reserved	rd_pri6			reserved	rd_pri5			reserved	rd_pri4			reserved	rd_pri3			reserved	rd_pri2			reserved	rd_pri1			reserved	rd_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

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[30:28]	RW	rd_pri7	Priority when the read command ID mapping is 7. 000: highest priority ... 111: lowest priority
[27]	RO	reserved	Reserved.
[26:24]	RW	rd_pri6	Priority when the read command ID mapping is 6. 000: highest priority ... 111: lowest priority
[23]	RO	reserved	Reserved.
[22:20]	RW	rd_pri5	Priority when the read command ID mapping is 5. 000: highest priority ... 111: lowest priority
[19]	RO	reserved	Reserved.
[18:16]	RW	rd_pri4	Priority when the read command ID mapping is 4. 000: highest priority ... 111: lowest priority
[15]	RO	reserved	Reserved.
[14:12]	RW	rd_pri3	Priority when the read command ID mapping is 3. 000: highest priority ... 111: lowest priority
[11]	RO	reserved	Reserved.
[10:8]	RW	rd_pri2	Priority when the read command ID mapping is 2. 000: highest priority ... 111: lowest priority
[7]	RO	reserved	Reserved.
[6:4]	RW	rd_pri1	Priority when the read command ID mapping is 1. 000: highest priority ... 111: lowest priority
[3]	RO	reserved	Reserved.

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[2:0]	RW	rd_pri0	Priority when the read command ID mapping is 0. 000: highest priority ... 111: lowest priority

AXI_WRTOUT

AXI_WRTOUT is a DDRC write command timeout configuration register.

Offset Address	Register Name	Total Reset Value
0x140 + 0x4 x *ports* (*ports* = 0–6)	AXI_WRTOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout3								wr_tout2								wr_tout1								wr_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout3	Write command timeout period (level 3). The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout2	Write command timeout period (level 2). The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout1	Write command timeout period (level 1). The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout0	Write command timeout period (level 0). 0x0: disabled 0x01–0xFF: (*n* x 4) clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bit. That is, the lower two bits are fixed at 0.

AXI_RDTOUT

AXI_RDTOUT is a DDRC read command timeout configuration register.

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Offset Address	Register Name	Total Reset Value
0x180 + 0x4 x *ports* (*ports* = 0–6)	AXI_RDTOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout3								rd_tout2								rd_tout1								rd_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout3	Read command timeout period (level 3). The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout2	Read command timeout period (level 2). The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout1	Read command timeout period (level 1). The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout0	Read command timeout period (level 0). 0x0: disabled 0x01–0xFF: (*n* x 4) clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bit. That is, the lower two bits are fixed at 0.

AXI_OSTDCFG0

AXI_OSTDCFG0 is DDRC port command outstanding configuration register 0.

Offset Address	Register Name	Total Reset Value
0x200 + 0x4 x *ports* (*ports* = 0–6)	AXI_OSTDCFG0	0x1F1F_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												port_ostd_lvl0			
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	port_ostd_lvl0	OSTD threshold of the command transmitted from the port to channel 0 (used with the AXI_OSTDCFG2 register).

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AXI_OSTDCFG1

AXI_OSTDCFG1 is DDRC port command outstanding configuration register 1.

Offset Address	Register Name	Total Reset Value
0x240	AXI_OSTDCFG1	0x1F1F_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dmc_ostd_lvl0			
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	dmc_ostd_lvl0	Accumulated OSTD threshold of commands transmitted from all ports to channel 0 (used with the AXI_OSTDCFG2 register).

AXI_OSTDCFG2

AXI_OSTDCFG2 is DDRC port command outstanding configuration register 2.

Offset Address	Register Name	Total Reset Value
0x244	AXI_OSTDCFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		ostd_mode6		ostd_mode5		ostd_mode4		ostd_mode3		ostd_mode2		ostd_mode1		ostd_mode0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.

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[13:12]	RW	ostd_mode6	OSTD mode of port 6. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[11:10]	RW	ostd_mode5	OSTD mode of port 5. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[9:8]	RW	ostd_mode4	OSTD mode of port 4. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

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[7:6]	RW	ostd_mode3	OSTD mode of port 3. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[5:4]	RW	ostd_mode2	OSTD mode of port 2. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[3:2]	RW	ostd_mode1	OSTD mode of port 1. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

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[1:0]	RW	ostd_mode0	OSTD mode of port 0. 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

AXI_OSTDSTATUS

AXI_OSTDSTATUS is a DDRC channel command outstanding status register.

Offset Address	Register Name	Total Reset Value
0x248	AXI_OSTDSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ostd_st0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RO	ostd_st0	Command OSTD status of channel 0. The statistics are valid when at least a port is in non-green port mode.

AXI_FLUX0

AXI_FLUX0 is a DDRC port bandwidth traffic control configuration register for channel 0.

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Offset Address	Register Name	Total Reset Value
0x280 + 0x4 x *ports* (*ports* = 0–6)	AXI_FLUX0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22	21	20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved			flux_port_en0	flux_ovfl_en0	reserved	flux_ovfl_lvl0	reserved	flux_cfg0		
Reset	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	flux_port_en0	AXI interface DDRC traffic statistics enable. 0: disabled 1: enabled
[20]	RW	flux_ovfl_en0	AXI interface traffic overflow allow enable 0: disabled 1: enabled When this field is set to 1, the bandwidth of the AXI interface can exceed the configured traffic if the AXI interface traffic exceeds the bandwidth limit, there is no AXI interface with traffic overflow, and a command request is initiated.
[19:17]	RO	reserved	Reserved.
[16:12]	RW	flux_ovfl_lvl0	AXI interface traffic overflow threshold. 0x0–0x10: DMC threshold for allowing traffic overflow Other values: reserved When the AXI interface traffic exceeds the configured bandwidth of flux, flux_ovfl is 1, and the number of commands to be processed in the DMC is less than the configured threshold, transmission is allowed. Otherwise, no arbitration is performed.
[11:10]	RO	reserved	Reserved.
[9:0]	RW	flux_cfg0	Allowed bandwidth of the AXI interface. 0x0–0x3FF: ratio of the maximum DDR bandwidth to the total bandwidth accessed by the AXI interface. The total bandwidth is 1024. The configured value is a ratio of the allowed bandwidth to the total bandwidth. Other values: reserved

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4.1.6 DMC Registers of the DDRC

4.1.6.1 Register Summary

Table 4-6 describes DMC registers.

Table 4-6 DMC registers (base address: 0x2011_1000)

Offset Address	Register	Description	Page
0x000	DDRC_CTRL_SREF	DDRC self-refresh control register	4-47
0x004	DDRC_CTRL_INIT	DDRC initialization control register	4-47
0x00C	DDRC_CTRL_SFC	DDRC software configuration command start register	4-48
0x010	DDRC_CTRL_PERF	DDRC performance statistics control register	4-48
0x020	DDRC_CFG_SREF	DDR self-refresh configuration register	4-49
0x028	DDRC_CFG_PD	DDR power-down status register	4-50
0x02C	DDRC_CFG_AREF	DDRC auto-refresh mode register	4-51
0x040	DDRC_CFG_WORKMODE	DDRC operating mode register	4-52
0x050	DDRC_CFG_DDRMODE	DDR operating mode register	4-53
0x060	DDRC_CFG_RNKVOL	DDRC-controlled DDR capacity configuration register	4-55
0x070	DDRC_CFG_EMRS01	DDR mode register 0 and mode register 1	4-57
0x074	DDRC_CFG_EMRS23	DDR mode register 2 and mode register 3	4-57
0x080	DDRC_CFG_TIMING0	DDRC timing parameter register 0	4-57
0x084	DDRC_CFG_TIMING1	DDRC timing parameter register 1	4-58
0x88	DDRC_CFG_TIMING2	DDRC timing parameter register 2	4-60
0x8C	DDRC_CFG_TIMING3	DDRC timing parameter register 3	4-61

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Offset Address	Register	Description	Page
0x090	DDRC_CFG_TIMING4	DDRC timing parameter register 4	4-62
0x094	DDRC_CFG_TIMING5	DDRC timing parameter register 5	4-63
0x098	DDRC_CFG_TIMING6	DDRC timing parameter register 6	4-64
0x0A0	DDRC_CFG_NXT_TIMING 0	DDRC timing parameter register 0 for switching the frequency	4-65
0x0A4	DDRC_CFG_NXT_TIMING 1	DDRC timing parameter register 1 for switching the frequency	4-66
0x0A8	DDRC_CFG_NXT_TIMING 2	DDRC timing parameter register 2 for switching the frequency	4-67
0x0AC	DDRC_CFG_NXT_TIMING 3	DDRC timing parameter register 3 for switching the frequency	4-68
0x0B0	DDRC_CFG_NXT_TIMING 4	DDRC timing parameter register 4 for switching the frequency	4-69
0x0B4	DDRC_CFG_NXT_TIMING 5	DDRC timing parameter register 5 for switching the frequency	4-70
0x0B8	DDRC_CFG_NXT_TIMING 6	DDRC timing parameter register 6 for switching the frequency	4-71
0x0BC	DDRC_CFG_BLDATA	DDRC pre-received write data configuration register	4-71
0x0C0	DDRC_CFG_ODT	DDR ODT feature configuration register	4-72
0x0C4	DDRC_CFG_DMCLVL	DDRC command queue depth threshold configuration register	4-73
0x200	DDRC_CFG_DDRPHY	DDR I/O configuration register	4-73
0x210	DDRC_CFG_SFC	DDRC software DDR command attribute register	4-74
0x214	DDRC_CFG_SFC_ADDR0	Read/Write memory address register 0 for the software configuration module	4-75

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Offset Address	Register	Description	Page
0x218	DDRC_CFG_SFC_ADDR1	Read/Write memory address register 1 for the software configuration module	4-75
0x21C	DDRC_CFG_SFC_WDATA 0	Write data register 0 for the software configuration module	4-76
0x220	DDRC_CFG_SFC_WDATA 1	Write data register 1 for the software configuration module	4-76
0x224	DDRC_CFG_SFC_WDATA 2	Write data register 2 for the software configuration module	4-76
0x228	DDRC_CFG_SFC_WDATA 3	Write data register 3 for the software configuration module	4-77
0x270	DDRC_CFG_PERF	DDRC performance statistics mode register	4-77
0x274	DDRC_CFG_STAID	DDRC performance statistics command ID register	4-78
0x278	DDRC_CFG_STAIDMSK	DDR performance statistics command ID mask register	4-79
0x280	DDRC_INTMSK	DDRC interrupt mask register	4-79
0x284	DDRC_RINT	DDRC raw interrupt register	4-80
0x288	DDRC_INTSTS	DDRC interrupt status register	4-81
0x290	DDRC_CURR_STATUS	DDRC status register	4-81
0x294	DDRC_CURR_FUNC	DDRC FUNC module status register	4-82
0x2A0	DDRC_CURR_EXECST	DDRC command state machine status register	4-83
0x2A4	DDRC_CURR_WGFIFOST	DDRC write data FIFO status register	4-84
0x380	DDRC_HIS_FLUX_WR	DDRC all write command traffic statistics register	4-84
0x384	DDRC_HIS_FLUX_RD	DDRC all read command traffic statistics register	4-85
0x388	DDRC_HIS_FLUX_WCMD	DDRC all write command count register	4-85
0x38C	DDRC_HIS_FLUX_RCMD	DDRC all read command	4-86

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Offset Address	Register	Description	Page
		count register	
0x390	DDRC_HIS_FLUXID_WR	DDRC specified ID write traffic statistics registers	4-86
0x394	DDRC_HIS_FLUXID_RD	DDRC specified ID read traffic statistics registers	4-87
0x0398	DDRC_HIS_FLUXID_WCMD	DDRC all ID write command count register	4-87
0x039C	DDRC_HIS_FLUXID_RCMD	DDRC all ID read command count register	4-88
0x3A0	DDRC_HIS_WLATCNT0	DDRC specified ID write command latency statistics register 0	4-88
0x3A4	DDRC_HIS_WLATCNT1	DDRC specified ID write command latency statistics register 1	4-89
0x3A8	DDRC_HIS_RLATCNT0	DDRC specified ID read command latency statistics register 0	4-89
0x3AC	DDRC_HIS_RLATCNT1	DDRC specified ID read command latency statistics register 1	4-90
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	Read channel inherent latency register	4-90
0x3BC	DDRC_HIS_CMD_SUM	DMC accumulated command count register	4-91
0x4B4	DDRC_HIS_SFC_RDATA3	Software configuration read data register 3	4-91
0x4B8	DDRC_HIS_SFC_RDATA4	SFC read data register	4-91
0x4BC	DDRC_HIS_SFC_RDATA5	SFC read data register	4-92
0x4C0	DDRC_HIS_SFC_RDATA6	SFC read data register	4-92
0x4C4	DDRC_HIS_SFC_RDATA7	SFC read data register	4-92
0x4C8	DDRC_HIS_SFC_RDATA_ECC	SFC read data error correcting code (ECC) register	4-93

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4.1.6.2 Register Description

DDRC_CTRL_SREF

DDRC_CTRL_SREF is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_CTRL_SREF	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sref_done	sref_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	sref_done	DDR PHY self-refresh done. 1: The transition from 0 to 1 indicates that the DDR PHY completes all required operations after exiting the self-refresh status and the DMC can accept new requests.
[0]	RW	sref_req	SDRAM self-refresh request. 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_CTRL_INIT

DDRC_CTRL_INIT is a DDRC initialization control register.

Offset Address	Register Name	Total Reset Value
0x004	DDRC_CTRL_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dfi_init_start	init_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.

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[1]	RW	dfi_init_start	DFI initialization start. 0: normal state 1: DFI interface initialization is started, and the PHY implements related control processes. This bit is automatically cleared by hardware after initialization is complete.
[0]	RW	init_req	Initialization enable. 0: Initialization is complete or initialization is performed properly. 1: The SDRAM starts to be initialized.

DDRC_CTRL_SFC

DDRC_CTRL_SFC is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x00C	DDRC_CTRL_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC. 0: The command is not executed or the parameter is automatically cleared after the command is executed. 1: The command is requested to be executed.

DDRC_CTRL_PERF

DDRC_CTRL_PERF is a DDRC performance statistics enable register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL_PERF	0x0014_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															perf_en

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Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	perf_en	Performance statistics mode. 0: disabled 1: enabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When perf_mode is 1, this bit is automatically cleared after counting is complete.

DDRC_CFG_SREF

DDRC_CFG_SREF is a DDRC self-refresh configuration register.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CFG_SREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sref_arefnum				reserved			clk_switch	reserved			sref_odis	reserved			sref_cc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:12]	RW	sref_arefnum	Number of self-refresh operations initiated after DDRn SDRAM exits the self-refresh status during the DFS process. 0x0: No self-refresh operation is initiated. 0x1–0xF: *n*
[11:9]	RO	reserved	Reserved.
[8]	RW	clk_switch	DDRC low-power clock switch. Whether to back press AXI interface command when the DDRC enters the low-power status (DDR self-refresh). 0: The interface commands are not back pressed, and an error is returned directly. 1: The interface commands are back pressed, and the original command is executed after the clock is switched.
[7:5]	RO	reserved	Reserved.

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[4]	RW	sref_odis	Output disable for the DDR command and data I/O in self-refresh mode. 0: enabled 1: disabled **NOTE** The configuration is a static configuration. It is recommended that this bit be set to 1 to disable the output of the DDR command and data I/O after the DDR enters the self-refresh status. It is recommended that this bit be set to 0 to enable the output of the DDR command and data I/O before the DDR exits the self-refresh status.
[3:1]	RO	reserved	Reserved.
[0]	RW	sref_cc	SDRAM clock control in self-refresh mode. 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled.

DDRC_CFG_PD

DDRC_CFG_PD is a DDR power-down status register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CFG_PD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								t_clk_cke				reserved			pd_ac	reserved			pd_cc	pd_prd								reserved			pd_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:20]	RW	t_clk_cke	Relationship between CKL and CKE. 0x0–0x7: The delay relative to CKE when the PHY disables the clock is related to the DDR PHY. For example, it is set to 5 for SNPS G2 MULTIPHY or 0 for SNPS 32PHY.
[19:17]	RW	reserved	Reserved.
[16]	RW	pd_ac	SDRAM address command dynamic disable in power-down mode. 0: enabled 1: disabled **NOTE** This field is valid when pd_en is enabled. The control pins exclude CKE, ODT, CSN, and RESET_N.

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[15:13]	RO	reserved	Reserved.
[12]	RW	pd_cc	SDRAM clock control in power-down mode. 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled. Note: This field is valid only when the LPDDR SDRAM or LPDDR2 SDRAM is used.
[11:4]	RW	pd_prd	SDRAM power-down cycle. When the DDRC does not receive any command in consecutive pd_prd cycles, it forces the SDRAM to enter the power-down status. When a command is received, the DDRC forces the SDRAM to exit the power-down status. 0x00: not to enter the power-down status 0x01−0xFF: *n* clock cycles **NOTE** This field is valid only when pd_en is 1.
[3:1]	RO	reserved	Reserved.
[0]	RW	pd_en	Automatic power-down enable for the SDRAM. 0: disabled 1: enabled

DDRC_CFG_AREF

DDRC_CFG_AREF is a DDRC auto-refresh mode register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_CFG_AREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aref_alarm_num								reserved			aref_alarm_en	reserved			aref_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:8]	RW	aref_alarm_num	The auto-refresh command is forced to be transmitted if a specific number of auto-refresh commands cannot be transmitted. 0x0–0xFF: lack of (*n* + 1) auto-refresh commands Note that only one auto-refresh command is considered when *n* is 255 because the upper bits are lost after the bits of the 8-bit counter are carried.
[7:5]	RO	reserved	Reserved.
[4]	RW	aref_alarm_en	Auto-refresh loss alarm enable (AREF function). 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved.
[1:0]	RW	aref_mode	Auto-refresh mode. 0: An auto-refresh operation is performed every one tREFI cycle. 0: Three auto-refresh operations are performed every three tREFI cycles. 10: Four auto-refresh operations are performed every five tREFI cycles. 11: Eight auto-refresh operations are performed every nine tREFI cycles.

DDRC_CFG_WORKMODE

DDRC_CFG_WORKMODE is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_CFG_WORKMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		hdr_mode	read_mode	reserved			wrap_en	reserved			apre_en	func_clkon	data_clkon	cmd_clkon	clk_ratio
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13]	RW	hdr_mode	DFI interface mode select. 0: SDR mode 1: HDR mode The Hi3516A supports only the HDR mode.

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[12]	RW	read_mode	DDRC read mode. 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC. **NOTE** This field must be set to 0 when DDRC_DTRCTRL[train_mode] is set to 0.
[11:9]	RO	reserved	Reserved.
[8]	RW	wrap_en	Wrap command optimization enable. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.
[4]	RW	apre_en	Auto-precharge enable. 0: disabled 1: enabled
[3]	RW	func_clkon	Functional module clock enable. 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[2]	RW	data_clkon	Data channel clock enable. 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[1]	RW	cmd_clkon	Command channel clock enable. 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[0]	RW	clk_ratio	Operating mode of the DDRC. 0: The ratio of the DDRC frequency to the PHY frequency is 1:1. 1: The ratio of the frequency of the DDRC to the frequency of the PHY is 1:2.

DDRC_CFG_DDRMODE

DDRC_CFG_DDRMODE is a DDR operating mode register.

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Offset Address	Register Name	Total Reset Value
0x050	DDRC_CFG_DDRMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rank		reserved		odt_on	zqc_en	reserved			bc_en	reserved			brstlen	reserved		mem_width		reserved		dram_type	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:20]	RW	rank	DDRC rank. 00: 1 rank 01: 2 ranks 10: 3 ranks 11: 4 ranks
[19:18]	RO	reserved	Reserved.
[17]	RW	odt_on	Whether the ODT signal output to the SDRAM is fixed. 0: The signal is controlled by the DDRC. 1: The output is fixed at the wodt configuration of rank 0.
[16]	RW	zqc_en	DDR3 SDRAM ZQ enable. 0: disabled 1: enabled **NOTE** This field is valid only for the DDR3 SDRAM or LPDDR2 SDRAM and its default value is 0.
[15:13]	RO	reserved	Reserved.
[12]	RW	bc_en	DDR3 burst chop mode. 0: disabled 1: enabled **NOTE** This field is valid only for the DDR3 SDRAM.
[11:9]	RO	reserved	Reserved.

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[8]	RW	brstlen	Burst length of the DDRC. 0: BL4 1: BL8 The burst mode of the DDR2 SDRAM can be set to burst4 or burst8 mode. The burst mode of the DDR3 SDRAM must be burst8 mode. **NOTE** When DDRC_CFG_WORKMODE[clk_ratio] is 1, this bit must be set to 0 (BL4) for the DDR3 SDRAM, which indicates the burst8 mode.
[7:6]	RO	reserved	Reserved.
[5:4]	RW	mem_width	Bit width of the storage data bus. 00: 8 bits 01: 16 bits 10: 32 bits 11: 64 bits
[3]	RO	reserved	Reserved.
[2:0]	RW	dram_type	External memory type. 000: reserved 001: LPDDR 010: LPDDR2 011: LPDDR3 100: DDR 101: DDR2 110: DDR3 111: DDR4

DDRC_CFG_RNKVOL

DDRC_CFG_RNKVOL is a DDRC-controlled DDR capacity configuration register.

Offset Address	Register Name	Total Reset Value
0x060	DDRC_CFG_RNKVOL	0x0000_0022

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14	13 12	11 10 9	8	7	6 5 4	3	2 1 0
Name	reserved					mem_map	reserved	mem_bank	reserved	mem_row	reserved	mem_col

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:12]	RW	mem_map	Address translation mode of the SDRAM. 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW}= AXI_Address 10: {Rank, Row, Ba, Col, cs, Col, DW}= AXI_Address 11: {Rank, Ba, Row, Col, cs, Col, DW}= AXI_Address This parameter can be set to 10 or 11 only when DDRC_CONFIG1[dual_ch] is valid. When there are multiple ranks, the configuration must be the same for each rank.
[11:9]	RO	reserved	Reserved.
[8]	RW	mem_bank	Number of banks of a single SDRAM. 0: 4 banks 1: 8 banks
[7]	RO	reserved	Reserved.
[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM. 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits 101: 16 bits Other values: reserved
[3]	RO	reserved	Reserved.
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM. 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits Other values: reserved **NOTE** The DDRC does not support the DDR whose col address is less than 8. That is, the 32-bit LPDDR2 with the capacity of 64 Mbits is not supported.

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DDRC_CFG_EMRS01

DDRC_CFG_EMRS01 is a configuration register for DDR mode register 0 and mode register 1.

Offset Address	Register Name	Total Reset Value
0x070	DDRC_CFG_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDRn SDRAM extended mode register 1.
[15:0]	RW	mrs	DDRn SDRAM mode register.

DDRC_CFG_EMRS23

DDRC_CFG_EMRS23 is a configuration register for DDR mode register 2 and mode register 3.

Offset Address	Register Name	Total Reset Value
0x074	DDRC_CFG_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDRn SDRAM extended mode register 3.
[15:0]	RW	emrs2	DDRn SDRAM extended mode register 2.

DDRC_CFG_TIMING0

DDRC_CFG_TIMING0 is DDRC timing parameter register 0.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

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Offset Address	Register Name	Total Reset Value
0x080	DDRC_CFG_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved	tras	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the load mode register (LMR) command. The value is the larger value between tMOD and tMRD for the DDR2 or LPDDR2 and is tMRD for the DDR3. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period). 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command. 0x0–0x3: 3 clock cycles 0x4–0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command. 0x00–0x01: 1 clock cycle 0x02–0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved.
[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE). 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_TIMING1

DDRC_CFG_TIMING1 is DDRC timing parameter register 1.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

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Offset Address	Register Name	Total Reset Value
0x084	DDRC_CFG_TIMING1	0xFF24_51FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tsre		trtw	twl	tcl	reserved	trfc	
Reset	1 1 1 1	1 1 1 1	0 0 1 0	0 1 0 0	0 1 0 1	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command. 0x0: reserved 0x01–0xFF: (*n* x 4) clock cycles This field is set to the larger value between tXSDLL and tXS for the DDR3 SDRAM.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command. 0x0–0x1: 1 clock cycle 0x2–0xF: (*n* + 1) clock cycles **NOTE** In DDR2/DDR3 mode, the field value depends on the latency of the board, package, and I/O; in LPDDR/LPDDR2/LPDDR3 mode, the field value depends on the latency of the board, package, and I/O and tdqsckmax.
[19:16]	RW	twl	Number of wait cycles from the write command to the write data command. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles. The clock cycles are obtained from DDR user manuals. You can directly configure this field based on the clock cycles.
[15:12]	RW	tcl	Column address strobe latency (CL) from the read command to the read data operation. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles The clock cycles are obtained from DDR user manuals. You can directly configure this field based on the clock cycles.
[11:9]	RO	reserved	Reserved.
[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00: reserved 0x01–0x1FF: *n* clock cycles

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DDRC_CFG_TIMING2

DDRC_CFG_TIMING2 is DDRC timing parameter register 2.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x88	DDRC_CFG_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved						tfaw						reserved	taref										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the self-refresh mode. 0x0: reserved 0x1–0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last write data to the write-to-read command. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved.
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands. 0x00–0x3F: *n* clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved.

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[10:0]	RW	taref	Number of auto-refresh cycles. 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x *n*) clock cycles. For example, 0x008 indicates 128 (16 x 8) clock cycles. The interval tREFI is 7800/16/tclk. Tclk is the running cycle of the SDRAM. When DDRC_CONFIG1[aref_mode] is 1, the interval must be set to 8 x tREFI.

DDRC_CFG_TIMING3

DDRC_CFG_TIMING3 is DDRC timing parameter register 3.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x8C	DDRC_CFG_TIMING3	0xFFDF_F0F2

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tzq_prd			tzqinit		taond	txard	trtp
Reset	1 1 1 1	1 1 1 1	1 1 0 1	1 1 1 1	1 1 1 1	0 0 0 0	1 1 1 1	0 0 1 0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles. 0x000: The ZQCS command is forbidden. 0x001–0x3FF: (*n* x 128) AREF cycles The number of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:12]	RW	tzqinit	Number of ZQ initialization delay cycles. 0x0–0x1FF: (*n* + 1) clock cycles The field value must be the larger value between tZQINIT and tDLLK.
[11:8]	RW	taond	Number of ODT enable/disable cycles. In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5 0x3: 5/5.5 Other values: reserved

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			In DDR3 mode, this value is set to tWL − 1. In 1:2 mode, this value needs to be set to tWL − 2. However, if the PHY has been separately processed, the value tWL − 1 is used. In LPDDR3 mode, the value is set to tODTon(max)/tCK.
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode. 0x0–0xF: n clock cycles (in decimal) For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, the field value is the larger value between tXP and tCKE.
[3:0]	RW	trtp	Wait delay from the read command to the disable command. 000–010: 2 clock cycles 011–111: *n* clock cycles Trtp is calculated as follows: Trtp = AL + BL/2 + Max (trtp, 2) – 2 **NOTE** For DDR2, Trtp is greater than or equal to 2; for DDR3, Trtp is greater than or equal to 4.

DDRC_CFG_TIMING4

DDRC_CFG_TIMING4 is DDRC timing parameter register 4.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x090	DDRC_CFG_TIMING4	0x01FF_2000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tmod	twlo	reserved	twldqsen	reserved	twlmrd
Reset	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1	0 1 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.

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[24:20]	RW	tmod	Delay from the MRS command to ODT and ZQCL validity. 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles The clock cycles are obtained from DDR user manuals. If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.
[19:16]	RW	twlo	DDR3 write level status delay. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles The parameter is equal to twlo + twloe.
[15:14]	RO	reserved	Reserved.
[13:8]	RW	twldqsen	DDR3 write level start delay. 0x0 and 0x1: one clock cycle 0x2−0x3F: n clock cycles
[7:6]	RO	reserved	Reserved
[5:0]	RW	twlmrd	Delay of the initial valid DDR3 write level DQS. 0x0 and 0x1: one clock cycle 0x2−0x3F: n clock cycles

DDRC_CFG_TIMING5

DDRC_CFG_TIMING5 is DDRC timing parameter register 5.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x094	DDRC_CFG_TIMING5	0x1113_FF1F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			trnk2rnk	tzqcs		reserved	twr

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Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.
[19:16]	RW	trnk2rnk	Rank-to-rank delay. 0000–1111: *n* clock cycles Note: In DDR2/DDR3 mode, the field value depends on the latency of the board, package, and I/O; in LPDDR/LPDDR2/LPDDR3 mode, the field value depends on the latency of the board, package, and I/O, and tdqsckmax.
[15:8]	RW	tzqcs	ZQCS calibration delay period. 0x0–0xFF: (*n* + 1) clock cycles The field value must be greater than or equal to 10 due to the DMC design.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	twr	Number of wait cycles of write recovery. 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles **NOTE** When DFS is required, tWR must be set based on the maximum chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_TIMING6

DDRC_CFG_TIMING6 is DDRC timing parameter register 6.

Timing parameters in the register are obtained from DDR user manuals.
If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x098	DDRC_CFG_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:4]	RW	tcksrx	tCKSRX for the DDR3 or DDR4. Number of advanced valid beats after before the DDR exits the self-refresh status.

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			0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[3:0]	RW	tcksre	tCKSRE for the DDR3 or DDR4. Number of beats to be retained after the DDR enters the self-refresh status. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_NXT_TIMING0

DDRC_CFG_NXT_TIMING0 is DDRC timing parameter register 0 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_CFG_NXT_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved	tras	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the loading command of the loading mode register (LMR). 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B. 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period). 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command. 0x0−0x3: three clock cycles 0x4−0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command. 0x00–0x01: one clock cycle 0x02−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved

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[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE). 0x00 – 0x01: one clock cycle 0x02−0x3F: *n* clock cycles

DDRC_CFG_NXT_TIMING1

DDRC_CFG_NXT_TIMING1 is DDRC timing parameter register 1 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A4	DDRC_CFG_NXT_TIMING1	0xFF24_51FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tsre		trtw	twl	tcl	reserved	trfc	
Reset	1 1 1 1	1 1 1 1	0 0 1 0	0 1 0 0	0 1 0 1	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command. 0x0: one clock cycle 0x01–0xFF: n x 4 clock cycles When the DDR3 SDRAM is used, the value is set to tXSDLL.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command. 0x0 and 0x1: one clock cycle 0x2−0xF: n + 1 clock cycles
[19:16]	RW	twl	Number of wait cycles from the write command to the data write operation. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles For example, 0x3 indicates three clock cycles. Note: In DDR2 mode, tw1 is set to tcl − 1 and the condition (twl − taond ≥ 1) must be met.
[15:12]	RW	tcl	Column address strobe latency (CL) from the read command to the data read operation. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles
[11:9]	RO	reserved	Reserved

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[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00 – 0x01: one clock cycle 0x02-0xFF: n clock cycles

DDRC_CFG_NXT_TIMING2

DDRC_CFG_NXT_TIMING2 is DDRC timing parameter register 2 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A8	DDRC_CFG_NXT_TIMING2	0xF303_F000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11	10 9 8	7 6 5 4	3 2 1 0
Name	tcke	twtr	reserved		tfaw	reserved	taref		
Reset	1 1 1 1	0 0 1 1	0 0 0 0	0 0 1 1	1 1 1 1	0	0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the low-power mode. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last data write operation to the write-to-read command. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles For example, 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands. 0x00−0x3F: n clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved

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[10:0]	RW	taref	Number of auto-refresh cycles. 0x000: auto-refresh disabled 0x001–0x7FF: The auto-refresh cycle of the SDRAM is 16 x n clock cycles. For example, 0x008 indicates 128 (16 x 8) clock cycles. The interval tREF is 7800/16/tclk. Tclk is the running cycle of the SDRAM.

DDRC_CFG_NXT_TIMING3

DDRC_CFG_NXT_TIMING3 is DDRC timing parameter register 3 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0AC	DDRC_CFG_NXT_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd										tzqinit										taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles. 0x000: The ZQCS command is disabled. 0x001−0x3FF: n x 128 AREF cycles The time of ZQCS command cycles is equal to n x 128 taref clock cycles.
[21:12]	RW	tzqinit	Number of ZQ initialization delay cycles. 0x0–0x3ff: n + 1 clock cycles The value needs to be set to the larger one between tZQINIT and tDLLK.
[11:8]	RW	taond	Number of ODT enable/disable cycles. In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5 0x3: 5/5.5 Other values: reserved In DDR3 mode, the value is set to tWL − 1. In 1:2 mode, the value needs to be set to tWL – 2. However, if the PHY has been separately processed, the value tWL − 1 is used. In LPDDR3 mode, the value is set to tODTon(max)/tCK.
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode.

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			0x0–0xF: n clock cycles. n indicates a decimal value. For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, when the register is set to tXS, txard only needs to be set to an equivalent clock cycle of 10 ns.
[3:0]	RW	trtp	Wait delay from the read command to the disable command. 0000−0010: two clock cycles 0011–1111: n clock cycles Trtp = AL + BL/2 + Max (trtp, 2) – 2

DDRC_CFG_NXT_TIMING4

DDRC_CFG_NXT_TIMING4 is DDRC timing parameter register 4 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B0	DDRC_CFG_NXT_TIMING4	0x01FF_2000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tmod	twlo	reserved	twldqsen	reserved	twlmrd
Reset	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved
[24:20]	RW	tmod	Delay from the MRS command to ODT valid. 0x0 and 0x1: one clock cycle 0x02−0x1F: n clock cycles
[19:16]	RW	twlo	DDR3 write level status delay parameter. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles The parameter is equal to twlo + twloe.
[15:14]	RO	reserved	Reserved
[13:8]	RW	twldqsen	DDR3 write level start delay. 0x0 and 0x1: one clock cycle 0x2−0x3F: n clock cycles
[7:6]	RO	reserved	Reserved

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[5:0]	RW	twlmrd	Delay of the initial valid DDR3 write level DQS. 0x0 and 0x1: one clock cycle 0x2−0x3F: n clock cycles

DDRC_CFG_NXT_TIMING5

DDRC_CFG_NXT_TIMING5 is DDRC timing parameter register 5 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B4	DDRC_CFG_NXT_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												trnk2rnk				tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.
[19:16]	RW	trnk2rnk	Rank-to-rank delay. 0000–1111: n clock cycles
[15:8]	RW	tzqcs	ZQCS calibration delay period. 0x0−0xFF: n + 1 clock cycles
[7:5]	RW	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery. 0x0 and 0x1: one clock cycle 0x2−0x1F: n clock cycles **NOTE** When DFS is required, tWR must be set based on the maximum chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

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DDRC_CFG_NXT_TIMING6

DDRC_CFG_NXT_TIMING6 is DDRC timing parameter register 6 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B8	DDRC_CFG_NXT_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				todt_sft				tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:8]	RW	todt_sft	ODT delay control in LPDDR3 mode, for compensating the delay of the DDR PHY for ODT IO of POP LPDDR3. 0x0−0xF: n clock cycles ODT delay = tWL − taond + todt_sft. Note that the maximum ODT delay cannot exceed 0xF.
[7:4]	RW	tcksrx	tCKSRX for the DDR3 or DDR4. Number of advanced valid beats before the DDR exits the self-refresh status. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles
[3:0]	RW	tcksre	tCKSRE for the DDR3 or DDR4. Number of beats to be retained after the DDR enters the self-refresh status. 0x0 and 0x1: one clock cycle 0x2−0xF: n clock cycles

DDRC_CFG_BLDATA

DDRC_CFG_BLDATA is a DDRC pre-received write data configuration register.

Offset Address	Register Name	Total Reset Value
0x0BC	DDRC_CFG_BLDATA	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bl_data			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	bl_data	Number of DMC data segments corresponding to each DDR command in the current mode. 0x0–0xF: *n* data segments

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DDRC_CFG_ODT

DDRC_CFG_ODT is a DDR ODT feature configuration register.

Offset Address	Register Name	Total Reset Value
0x0C0	DDRC_CFG_ODT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rodt3	rodt2	rodt1	rodt0	wodt3	wodt2	wodt1	wodt0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rodt3	Read ODT enable for rank 3. 0: disabled 1: enabled
[27:24]	RW	rodt2	Read ODT enable for rank 2. 0: disabled 1: enabled
[23:20]	RW	rodt1	Read ODT enable for rank 1. 0: disabled 1: enabled
[19:16]	RW	rodt0	Read ODT enable for rank 0. 0: disabled 1: enabled
[15:12]	RW	wodt3	Write ODT enable for rank 3. 0: disabled 1: enabled
[11:8]	RW	wodt2	Write ODT enable for rank 2. 0: disabled 1: enabled
[7:4]	RW	wodt1	Write ODT enable for rank 1. 0: disabled 1: enabled
[3:0]	RW	wodt0	Write ODT enable for rank 0. 0: disabled 1: enabled

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DDRC_CFG_DMCLVL

DDRC_CFG_DMCLVL is a DDRC command queue depth threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x0C4	DDRC_CFG_DMCLVL	0x0000_010C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												que_level			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	que_level	Depth of the command register FIFO in the DMC. 0x1−0x10: depth of *n* commands Other values: reserved

DDRC_CFG_DDRPHY

DDRC_CFG_DDRPHY is a DDR IO configuration register.

Offset Address	Register Name	Total Reset Value
0x200	DDRC_CFG_DDRPHY	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			phy_upden	trdlat				reserved			phy_zqen	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	phy_upden	dfi_phyupd_en enable in response to the DDR PHY. 0: disabled 1: enabled
[11:8]	RW	trdlat	Inherent delay of the DDRPHY. 0x0–0xF: n + 1 clock cycles The value needs to be set to 8 when synopsys3/2phy is used.
[7:5]	RW	reserved	Reserved

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[4]	RW	phy_zqen	DDRPHY dfi_ctrlupd_req enable. 0: disabled 1: enabled
[3:0]	RO	reserved	Reserved

DDRC_CFG_SFC

DDRC_CFG_SFC is a DDRC software DDR command attribute register.

Offset Address	Register Name	Total Reset Value
0x210	DDRC_CFG_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_mrs																cmd_ma								cmd_rank				reserved	cmd_type		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cmd_mrs	Value of the DDR mode register when the LMR command is configured. This field is valid for the lower eight bits of the LPDDR2.
[15:8]	RW	cmd_ma	Address for the mode register to be configured when the LMR command is configured in LPDDR mode.
[7:4]	RW	cmd_rank	DDR rank for executing commands. 0: The configuration command is not executed. 1: The configuration command is executed. **NOTE** Each bit controls a rank. For example, cmd_rank[0] control DDR rank 0.
[3]	RO	reserved	Reserved.
[2:0]	RW	cmd_type	DDR command configuration. 000: enter the deep power-down status 001: exit the deep power-down status 010: LMR command 011: ZQCL 100: WRITE command 101: read command 110: precharge all command 111: read MRS command

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DDRC_CFG_SFC_ADDR0

DDRC_CFG_SFC_ADDR0 is read/write memory address register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x214	DDRC_CFG_SFC_ADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfc_row																sfc_col															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sfc_row	Row address for the memory that is read or written by the software configuration module.
[15:0]	RW	sfc_col	Column address for the memory that is read or written by the software configuration module. **NOTE** The DDRC access address must be aligned based on the current DMC bit width. For example, if the current DMC bit width is 128 bits: When the 64-/72-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:1], 1'b0}. When the 32-/36-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:2]0.2'b0}.

DDRC_CFG_SFC_ADDR1

DDRC_CFG_SFC_ADDR1 is read/write memory address register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x218	DDRC_CFG_SFC_ADDR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													sfc_bank		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	sfc_bank	Bank address for the memory that is read or written by the software configuration module.

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DDRC_CFG_SFC_WDATA0

DDRC_CFG_SFC_WDATA0 is write data configuration register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x21C	DDRC_CFG_SFC_WDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata0	Bits 127−96 of the written data of the software configuration module.

DDRC_CFG_SFC_WDATA1

DDRC_CFG_SFC_WDATA1 is write data configuration register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x220	DDRC_CFG_SFC_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata1	Bits 95−64 of the written data of the software configuration module.

DDRC_CFG_SFC_WDATA2

DDRC_CFG_SFC_WDATA2 is write data configuration register 2 for the software configuration module.

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Offset Address	Register Name	Total Reset Value
0x224	DDRC_CFG_SFC_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata2	Bits 63−32 of the written data of the software configuration module.

DDRC_CFG_SFC_WDATA3

DDRC_CFG_SFC_WDATA3 is write data configuration register 3 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x228	DDRC_CFG_SFC_WDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata3	Bits 31−0 of the written data of the software configuration module.

DDRC_CFG_PERF

DDRC_CFG_PERF is a DDRC performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x270	DDRC_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		flux_en	perf_mode	perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.

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[29]	RW	flux_en	DMC traffic monitoring enable. 0: disabled 1: enabled When traffic monitoring is enabled, the statistics module provides the number of cycles occupied by the DDR interface by ID to each request port. The traffic can be controlled by using this field and the port traffic setting function.
[28]	RW	perf_mode	Performance statistical mode. 0: continuous trigger mode. The performance counter continues to count. This ensures no overflow within 1s in continuous count mode. 1: single trigger mode. When the performance statistics time reaches perf_prd, the count value is retained and counting stops. **NOTE** After the count value overflows, the value is retained.
[27:0]	RW	perf_prd	Performance statistics cycle. 0x0–0x1: invalid 0x2–0xFFFFFFF: statistics cycles The actual statistics cycle is perf_prd x 16 x tclk (tclk is the bus clock cycle of the DDRC) **NOTE** This field is valid only when perf_mode is 1. When perf_mode is 0, the performance counter keeps on counting.

DDRC_CFG_STAID

DDRC_CFG_STAID is a DDRC performance statistics command ID register.

Offset Address	Register Name	Total Reset Value
0x274	DDRC_CFG_STAID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												sta_id																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:0]	RW	sta_id	Performance statistics by a specified ID. This field works with sta_idmask.

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DDRC_CFG_STAIDMSK

DDRC_CFG_STAIDMSK is a DDR performance statistics command ID mask register.

Offset Address	Register Name	Total Reset Value
0x278	DDRC_CFG_STAIDMSK	0x0000_1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sta_idmask											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved. NOTE This field must be set to 0.
[12:0]	RW	sta_idmask	Specified ID mask. The DDRC performance statistics register collects statistics only for specified ID commands. Cmd_id&sta_idmask = sta_id

DDRC_INTMSK

DDRC_INTMSK is a DDRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_int_mask	reserved			rdtimeout_int_mask	reserved						sref_err_int_mask	reserved			flux_int_mask	serr_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RW	aref_alarm_int_mask	DDR AREF command error interrupt mask enable. 0: enabled 1: disabled
[15:13]	RO	reserved	Reserved.

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[12]	RW	rdtimeout_int_mask	DDR PHY read data timeout interrupt mask enable. 0: enabled 1: disabled
[11:6]	RO	reserved	Reserved.
[5]	RW	sref_err_int_mask	Interface command error interrupt enable in DDR self-refresh mode. 0: enabled 1: disabled
[4:2]	RO	reserved	Reserved.
[1]	RW	flux_int_mask	DDR FLUX statistics period reach interrupt mask enable. 0: enabled 1: disabled
[0]	RW	serr_int_mask	DDR ECC single-bit error interrupt mask enable. 0: enabled 1: disabled

DDRC_RINT

DDRC_RINT is a DDRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_rint	reserved			rdtimeout_rint	reserved				sref_err_rint	reserved			flux_rint	serr_rint		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	INT_WC	aref_alarm_rint	DDR AREF command error raw interrupt. Writing 1 clears the interrupt.
[15:13]	RO	reserved	Reserved.
[12]	INT_WC	rdtimeout_rint	DDR PHY read data timeout raw interrupt. Writing 1 clears the interrupt.
[11:6]	RO	reserved	Reserved.

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[5]	INT_WC	sref_err_rint	Self-refresh interface command access interrupt. Writing 1 clears the interrupt.
[4:2]	RO	reserved	Reserved.
[1]	RW	flux_rint	DDR FLUX statistics period reach interrupt. Writing 1 clears the interrupt.
[0]	INT_WC	serr_rint	DDR ECC single-bit error raw interrupt. Writing 1 clears the interrupt.

DDRC_INTSTS

DDRC_INTSTS is a DDRC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_intsts	reserved			rdtimeout_intsts	reserved						sref_err_intsts	reserved			flux_intsts	serr_intsts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	INT	aref_alarm_intsts	DDR AREF command error interrupt.
[15:13]	RO	reserved	Reserved.
[12]	INT	rdtimeout_intsts	DDR PHY read data timeout interrupt.
[11:6]	RO	reserved	Reserved.
[5]	INT	sref_err_intsts	Self-refresh interface command access interrupt.
[4:2]	RO	reserved	Reserved.
[1]	RW	flux_intsts	DDR FLUX statistics period reach interrupt.
[0]	INT	serr_intsts	DDR ECC single-bit error interrupt.

DDRC_CURR_STATUS

DDRC_CURR_STATUS is a DDRC status register.

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Offset Address	Register Name	Total Reset Value
0x290	DDRC_CURR_STATUS	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							busy_func	reserved			busy_dmc	reserved			busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RO	busy_func	Status of the DDRC FUNC module. This field is in the SREF status during reset. 0: idle 1: A command is being processed.
[7:5]	RO	reserved	Reserved.
[4]	RO	busy_dmc	Status of the DDRC DMC. 0: idle 1: A command is being processed.
[3:1]	RO	reserved	Reserved.
[0]	RO	busy	Overall status of the DDRC. 0: idle 1: A command is being processed.

DDRC_CURR_FUNC

DDRC_CURR_FUNC is a DDRC FUNC module status register.

Offset Address	Register Name	Total Reset Value
0x294	DDRC_CURR_FUNC	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			in_phyupd	reserved															in_sfc	in_pd				reserved		dfi_init_complete	in_init	reserved			in_sref

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RO	in_phyupd	DDRC PHY update status. 0: idle 1: The PHY is being updated.
[27:13]	RO	reserved	Reserved.
[12]	RO	in_sfc	DDRC SFC status. 0: idle 1: An SFC command is being processed.
[11:8]	RO	in_pd	DDRC power-down status. 0: normal 0: power-down status Each bit represents a rank.
[7:6]	RO	reserved	Reserved.
[5]	RO	dfi_init_complete	DFI initialization status. 0: initializing 1: normal operating mode
[4]	RO	in_init	DDRC initialization status. 0: normal 1: initializing
[3:1]	RO	reserved	Reserved.
[0]	RO	in_sref	DDR self-refresh status. 0: normal 1: self-refresh.

DDRC_CURR_EXECST

DDRC_CURR_EXECST is a DDRC command state machine status register.

Offset Address	Register Name	Total Reset Value
0x2A0	DDRC_CURR_EXECST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	Controller command type. 0: read command 1: write command
[15:0]	RO	dmc_cv	Controller command validity flag. 0: invalid 1: valid

DDRC_CURR_WGFIFOST

DDRC_CURR_WGFIFOST is a DDRC write data FIFO status register.

Offset Address	Register Name	Total Reset Value
0x2A4	DDRC_CURR_WGFIFOST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wgntfifo_e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	wgntfifo_e	WGNT_FIFO empty or full status. The empty status indicates that all written data is received, and the non-empty status indicates that the written data is not completely received. 0: not empty 1: empty

DDRC_HIS_FLUX_WR

DDRC_HIS_FLUX_WR is a DDRC all write command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x380	DDRC_HIS_FLUX_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr	Write traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RD

DDRC_HIS_FLUX_RD is a DDRC all read command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x384	DDRC_HIS_FLUX_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd	Read traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_WCMD

DDRC_HIS_FLUX_WCMD is a DDRC all write command count register.

Offset Address	Register Name	Total Reset Value
0x388	DDRC_HIS_FLUX_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr_cmd																															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr_cmd	Write command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RCMD

DDRC_HIS_FLUX_RCMD is a DDRC all read command count register.

Offset Address	Register Name	Total Reset Value
0x38C	DDRC_HIS_FLUX_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd_cmd	Read command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WR

DDRC_HIS_FLUXID_WR is a DDRC specified ID write traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x390	DDRC_HIS_FLUXID_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr	Write traffic statistics of the master with the specified ID of

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			the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RD

DDRC_HIS_FLUXID_RD is a DDRC specified ID read traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x394	DDRC_HIS_FLUXID_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd	Read traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WCMD

DDRC_HIS_FLUXID_WCMD is a DDRC all ID write command count register.

Offset Address	Register Name	Total Reset Value
0x0398	DDRC_HIS_FLUXID_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr_cmd	Read traffic statistics of the master based on specified IDs. The counting is performed in the valid statistics cycle. The unit is the DMC bit width.

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			When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RCMD

DDRC_HIS_FLUXID_RCMD is a DDRC all ID read command count register.

Offset Address	Register Name	Total Reset Value
0x039C	DDRC_HIS_FLUXID_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd_cmd	Read command count of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT0

DDRC_HIS_WLATCNT0 is DDRC specified ID write command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A0	DDRC_HIS_WLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_max																wlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wlatcnt_max	Maximum latency of the write command with the specified ID of the DDRC. This field is cleared when the next statistics start.
[15:0]	RO	wlatcnt_min	Minimum latency of the write command with the specified ID of the DDRC. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

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DDRC_HIS_WLATCNT1

DDRC_HIS_WLATCNT1 is DDRC specified ID write command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3A4	DDRC_HIS_WLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	wlatcnt_all	Accumulated latency of the write command with the specified ID in the statistics cycle (the results of the lower four bits are ignored). When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the write command with the specified ID by dividing wlatcnt_all by fluxid_wr_cmd.

DDRC_HIS_RLATCNT0

DDRC_HIS_RLATCNT0 is a DDRC specified ID read command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A8	DDRC_HIS_RLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_max																rlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	rlatcnt_max	Maximum latency of the read command with the specified ID of the DDRC. The actual maximum read latency is rlatcnt_max plus inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.
[15:0]	RO	rlatcnt_min	Minimum latency of the read command with the specified ID of the DDRC.

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			Note that the actual minimum read latency is rlatcnt_min plus inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_RLATCNT1

DDRC_HIS_RLATCNT1 is DDRC specified ID read command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3AC	DDRC_HIS_RLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rlatcnt_all	Accumulated latency of the read command with the specified ID in the statistics cycle (the results of the lower four bits are ignored). When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the read command with the specified ID by using rlatcnt_all/fluxid_rd_cmd+inhere_rlatcnt.

DDRC_HIS_INHERE_RLAT_CNT

DDRC_HIS_INHERE_RLAT_CNT is a read channel inherent latency register.

Offset Address	Register Name	Total Reset Value
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																inhere_rlatcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	inhere_rlatcnt	Inherent latency of the read data channel for the DDRC and PHY. The actual latency can be obtained only by using this register and rlatcnt_min, rlatcnt_max, rlatcnt_all, and fluxid_rd_cmd.

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DDRC_HIS_CMD_SUM

DDRC_HIS_CMD_SUM is a DDRC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3BC	DDRC_HIS_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dmc_cmd_sum	Accumulated value of the commands that are temporarily stored in the DMC in the cycle. The value is wrapped if an overflow occurs.

DDRC_HIS_SFC_RDATA3

DDRC_HIS_SFC_RDATA3 is software configuration read data register 3.

Offset Address	Register Name	Total Reset Value
0x4B4	DDRC_HIS_SFC_RDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata3	Bits 159−128 of the data read by the SFC.

DDRC_HIS_SFC_RDATA4

DDRC_HIS_SFC_RDATA4 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B8	DDRC_HIS_SFC_RDATA4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata4	Bits 127−96 of the data read by the SFC.

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DDRC_HIS_SFC_RDATA5

DDRC_HIS_SFC_RDATA5 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4BC	DDRC_HIS_SFC_RDATA5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata5	Bits 95−64 of the data read by the SFC.

DDRC_HIS_SFC_RDATA6

DDRC_HIS_SFC_RDATA6 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4C0	DDRC_HIS_SFC_RDATA6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata6	Bits 63−32 of the data read by the SFC.

DDRC_HIS_SFC_RDATA7

DDRC_HIS_SFC_RDATA7 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4C4	DDRC_HIS_SFC_RDATA7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata7	Bits 31−0 of the data read by the SFC. The value of bits 7−0 is the readback value of the LPDDR2 MRS register in RD_MRS mode.

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DDRC_HIS_SFC_RDATA_ECC

DDRC_HIS_SFC_RDATA_ECC is an SFC read data ECC register.

Offset Address	Register Name	Total Reset Value
0x4C8	DDRC_HIS_SFC_RDATA_ECC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rdata_ecc3		rdata_ecc2		rdata_ecc1		rdata_ecc0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rdata_ecc3	8-bit ECC for bits 255−192 of the data read by the SFC.
[23:16]	RW	rdata_ecc2	8-bit ECC for bits 191−128 of the data read by the SFC.
[15:8]	RW	rdata_ecc1	8-bit ECC for bits 127−64 of the data read by the SFC.
[7:0]	RW	rdata_ecc0	8-bit ECC for bits 63−0 of the data read by the SFC.

4.1.7 DDR PHY Registers

4.1.7.1 Register Summary

NOTE

The variable *n* in the offset addresses for DDR PHY registers indicates the data block ID and ranges from 0 to 3.

Table 4-7 describes DDR PHY registers.

Table 4-7 Summary of DDR PHY registers (base address: 0x2011_8000)

Offset Address	Register	Description	Page
0x000	REVISION	PHY control block version register	4-99
0x004	PHYINITCTRL	PHY initialization control register	4-99
0x008	PHYINITSTATUS	PHY status register	4-102
0x00C	PHYCLKGATED	PHY clock gating control register	4-103
0x010	PHYTIMER0	PHY timing parameter register	4-104
0x014	PHYTIMER1	DRAM CKE low initialization register	4-105
0x018	PLLCTRL	Timing parameter register for the PLL in both address/command and data block	4-105
0x01C	PLLTIMER	PLL address/command and data block control register	4-106

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Offset Address	Register	Description	Page
0x020	DLYMEASCTRL	Read delay line delay measurement control register	4-107
0x024	IMPCTRL	ZQ calibration control register	4-108
0x028	IMPSTATUS	ZQ calibration result register	4-108
0x02C	DRAMCFG	DRAM system configuration register	4-110
0x030	DRAMTIMER0	DRAM timing parameter register 0	4-111
0x034	DRAMTIMER1	DRAM timing parameter register 1	4-112
0x038	DRAMTIMER2	DRAM timing parameter register 2	4-113
0x03C	DRAMTIMER3	DRAM timing parameter register 3	4-113
0x040	DRAMTIMER4	DRAM write leveling timing parameter register	4-114
0x044	ODTCR	Rank ODT control register while reading or writing to particular ranks	4-114
0x048	TRAINCTRL0	Training control register	4-115
0x04C	RANKEN	Training rank control register	4-117
0x0050	TRAINMADDR	Data training memory start address register	4-118
0x0054	BISTCTRL	Built-in self test (BIST) behavior register	4-118
0x0058	BISTDATA0	DRAM loopback test BIST data register 0	4-120
0x005C	BISTDATA1	DRAM loopback test BIST data register 1	4-120
0x0060	BISTSTATUS	BIST test result and status register	4-121
0x0064	MODEREG01	Mode register content register 1	4-122
0x0068	MODEREG23	Mode register content register 2	4-122
0x006C	DETPATTERN	Write/Read DET pattern register	4-123
0x0070	MISC	Miscellaneous control register	4-124
0x0074	RNK2RNK	Rank-to-rank delay control register	4-126
0x0078	PHYCTRL0	PHY control register 0	4-126
0x007C	PHYDBG	PHY debug register	4-127
0x0080	RETCTRL0	Retraining control register	4-127
0x0084	DMSEL	DM swap selection register	4-128
0x0088	IOCTL	I/O control register	4-129
0x008C	DQSSEL	PHY DQ swap register	4-130

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Offset Address	Register	Description	Page
0x0090	PHYCTRL1	AC PHY control register	4-130
0x0094	DXNCKCTRL	PLL phase selection register	4-131
0x0098	PHYPLLCTRL_AC	PHY PLL control register 1	4-132
0x009C	PHYPLLCTRL_DX	PHY PLL control register 2	4-133
0x00A0	SWTMODE	S/W training mode register	4-133
0x00A4	SWTWLDQS	Write DQS issue register during S/W write leveling training	4-134
0x00A8	SWTRLT	S/W training result register	4-134
0x00AC	PHYCTRL2	PHY control register 2	4-135
0x00B0	IOCTL1	PHY I/O control register 1	4-135
0x00B4	IOCTL2	PHY I/O control register 2	4-136
0x00B8	BISTTIMER	Code update period register during BIST running	4-137
0x00D0	TRAINCTRL1	Data training control register 1	4-137
0x00D4	TRAINCTRL2	Data training control register 2	4-138
0x00D8	REGBANKCTRL	Register bank control register	4-139
0x00DC	TRAINCTRL3	Data training control register 3	4-140
0x100	ACBISTCTRL0	Comparison control register 0 while BIST activated	4-141
0x104	ACBISTCTRL1	Comparison control register 1 while BIST activated	4-143
0x108	ACBISTSTS0	BIST test result and status register 0	4-143
0x10C	ACBISTSTS1	BIST test result and status register 1	4-144
0x120	ACCMDBDL0	AC command bit delay line configuration register 0	4-145
0x124	ACCMDBDL1	AC command bit delay line configuration register 1	4-145
0x128	ACCMDBDL2	AC command bit delay line configuration register 2	4-145
0x12C	ACCMDBDL3	AC command bit delay line configuration register 3	4-146
0x130	ACCMDBDL4	AC command bit delay line configuration register 4	4-146

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Offset Address	Register	Description	Page
0x134	ACCMDBDL5	AC command bit delay line configuration register 5	4-147
0x138	ACCMDBDL6	AC command bit delay line configuration register 6	4-147
0x13C	ACCMDBDL7	AC command bit delay line configuration register 7	4-148
0x140	ACADDRBDL0	AC address bit delay line configuration register 0	4-148
0x144	ACADDRBDL1	AC address bit delay line configuration register 1	4-149
0x148	ACADDRBDL2	AC address bit delay line configuration register 2	4-149
0x14C	ACADDRBDL3	AC address bit delay line configuration register 3	4-150
0x150	ACADDRBDL4	AC address bit delay line configuration register 4	4-150
0x154	ACADDRBDL5	AC address bit delay line configuration register 5	4-151
0x158	ACADDRBDL6	AC address bit delay line configuration register 6	4-151
0x15C	ACADDRBDL7	AC address bit delay line configuration register 7	4-152
0x160	ACADDRBDL8	AC address bit delay line configuration register 8	4-152
0x164	ACADDRBDL9	AC address bit delay line configuration register 9	4-153
0x168	ACCLKBDL	AC clock bit delay line configuration register	4-153
0x170	ACPHYCTL0	AC block PHY control register 0	4-154
0x174	ACPHYCTL1	AC block PHY control register 1	4-155
0x178	ACPHYCTL2	AC block PHY control register 2	4-156
0x17C	ACPHYCTL3	AC block PHY control register 3	4-156
0x180	ACPHYCTL4	AC block PHY control register 4	4-157
0x184	ACPHYCTL5	AC block PHY control register 5	4-158
0x188	ACPHYCTL6	AC block PHY control register 6	4-159
0x018C	ACPHYCTL7	AC block PHY control register 7	4-159

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Offset Address	Register	Description	Page
0x0190	ACDEBUG	PHY debugging register	4-160
0x0194	ACPHYRSVDC	AC block PHY reserved control pin register 1	4-161
0x0198	ACPHYRSVDS	AC block PHY reserved control pin register 2	4-161
0x019C	ACPHYCTL8	AC block PHY control register 8	4-162
0x1A0	ACCMDBDL8	AC command bit delay line configuration register 8	4-162
0x1A4	ACCMDBDL9	AC command bit delay line configuration register 9	4-163
0x1A8	ACCMDBDL10	AC command bit delay line configuration register 10	4-163
0x1AC	ACCMDBDL11	AC command bit delay line configuration register 11	4-164
0x01B0	ACPHYDCC	AC block PHY DCC control register	4-164
0x01B4	ACPHYCTL9	AC block PHY control register 9	4-165
0x01C0	CATTIMER0	CA training timer 0 register	4-166
0x01C4	CATTIMER1	CA training timer 1 register	4-167
0x01C8	CATCONFIG	CA training configuration register	4-167
0x01CC	CATRESULT	CA training result register (for debugging)	4-169
0x01D0	PHYDQRESULT	SW CA training DQ result (from PHY) register	4-169
0x01D4	ADDRPHBOUND	CA training address phase boundary register	4-169
0x01D8	SWCATPATTERN_P	SW CA training pattern register for the positive CK edge	4-171
0x01DC	SWCATPATTERN_N	SW CA training pattern register for the negative CK edge	4-171
0x01E4	LPCTRL	Low-power control register	4-171
0x200 + *n* x 0x80	DXNBISTCTRL	Loopback data comparison control register during BIST of data blocks	4-173
0x204 + *n* x 0x80	DXNBISTSTS	BIST test result and status register	4-174
0x208 + *n* x 0x80	DXNCTRL	Data block control register	4-175

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Offset Address	Register	Description	Page
0x210 + *n* x 0x80	DXNWDQNBDL0	Data block bit delay configuration register 0	4-175
0x214 + *n* x 0x80	DXNWDQNBDL1	Data block bit delay configuration register 1	4-176
0x218 + *n* x 0x80	DXNWDQNBDL2	Data block bit delay configuration register 2	4-177
0x21C + *n* x 0x80	DXNRDQNBDL0	Data block bit delay configuration register 3	4-177
0x220 + *n* x 0x80	DXNRDQNBDL1	Data block bit delay configuration register 4	4-178
0x224 + *n* x 0x80	DXNRDQNBDL2	Data block bit delay configuration register 5	4-179
0x22C + *n* x 0x80	DXNRDQSDLY	Local delay line control register	4-179
0x230 + *n* x 0x80	DXNWDQSDLY	Write leveling DQS delay control register	4-180
0x234 + *n* x 0x80	DXNWDQDLY	Write leveling delay line control register	4-180
0x238 + *n* x 0x80	DXNWLSL	Extra system latency addition control register	4-181
0x23C + *n* x 0x80 + *m* x 0x400	DXNRDQSGDLY	Local delay line control register	4-181
0x240 + *n* x 0x80	DXPHYCTRL	DX PHY control register	4-182
0x248 + *n* x 0x80	DXNGDS	Latch enable register	4-183
0x24C + *n* x 0x80	DXNCLKBDL	Data block clock bit delay line configuration register	4-183
0x250 + *n* x 0x80	DXNRDBOUND	Read data eye boundary register	4-184
0x254 + *n* x 0x80	DXNWRBOUND	Write data eye boundary register	4-184
0x258 + *n* x 0x80	DXNOEBDL	Output enable delay line control register	4-185
0x260 + *n* x 0x80	DXNMISCCTRL0	Data block PHY miscellaneous control register 0	4-185

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Offset Address	Register	Description	Page
0x264 + *n* x 0x80	DXNMISCCTRL1	Data block PHY miscellaneous control register 1	4-186
0x268 + *n* x 0x80	DXDEBUG0	Data block PHY debug signal register 0	4-187
0x26C + *n* x 0x80	DXDEBUG1	Data block PHY debug signal register 1	4-188
0x270 + *n* x 0x80	DXPHYRSVD	Data block PHY reserved control pin register	4-188
0x274 + *n* x 0x80	DXNMISCCTRL2	Data block PHY miscellaneous control register 2	4-189
0x278 + *n* x 0x80	DXDEBUGCONFIG	Data block PHY debugging control register	4-190
0x27C + *n* x 0x80	DXNDCC	Data block PHY DCC control register	4-190

4.1.7.2 Register Description

REVISION

REVISION is a PHY control block version register.

Offset Address	Register Name	Total Reset Value
0x000	REVISION	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																major								minor							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RO	major	Major version of the PHY control block.
[7:0]	RO	minor	Minor version of the PHY control block.

PHYINITCTRL

PHYINITCTRL is a PHY initialization control register.

NOTE

Writing to this register has no effect if init_en is 1.

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Offset Address	Register Name	Total Reset Value
0x004	PHYINITCTRL	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctl_cke_bypass	reserved															phyconn_rst	pack_rst	phy_rst	dram_rst	cat_en	dram_init_en	wdet_en	rdet_en	wl2_en	gdst_en	gt_en	wl_en	zcal_en	dlymeas_en	pll_init_en	init_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31]	RW	ctl_cke_bypass	PACK CKE bypass function enable. 1'b1: CKE is controlled by MC even when PACK controls the DFI interface. 1'b0: CKE is controlled by PACK when PACK controls the DFI interface.
[30:16]	RO	reserved	Reserved.
[15]	RW	phyconn_rst	PHY counter reset. This field is used to set the PHY counter reset signal. To issue a reset signal to PHY counter, this field should be set to 1. To end the reset signal to PHY counter, this field should be cleared. Note that the reset signal connects to the A/C block counter and the counter of all of the data blocks.
[14]	RW	pack_rst	PACK reset. This field is used to issue reset to all the digital circuits of the PACK including the register file. If this field is set to 1, all of the digital parts (including control registers) of the PHY will be set to default value. The reset will be automatically executed, and this bit will be cleared after reset is complete.
[13]	RW	phy_rst	PHY reset. This field is used to set PHY reset signal. To issue a reset signal to the PHY, this field should be set to 1. To end the reset signal to the PHY, this field should be cleared. Note that the reset signal connects to the A/C block and all of the data blocks.
[12]	RW	dram_rst	DRAM reset. This field is used to initiate the DRAM reset sequence. If this field is set to 1, RESET# and CKE will be pulled low for t_dram_rst. After t_dram_rst, the CKE RESET# is pulled to high while keeping CKE at low for t_cke_low. After t_cke_low, CKE is pulled to high, and after t_cke_high, this field is cleared automatically. For LPDDR2/LPDDR3, only CKE will be active during DRAM reset sequence.

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[11]	RW	cat_en	HW CA training enable. Writing 1 to this field starts the HW CA training sequence. This field will be cleared after CA training is complete. Note that the CA training applies only to LPDDR3.
[10]	RW	dram_init_en	DRAM initialization enable. This field is used to control whether the internal DRAM initialization sequence is executed after PHY initialization is complete. For LPDDR2/LPDDR3, this field will complete the initial sequence including tINIT3−tINIT5 & tZQC.
[9]	RW	wdet_en	Write data eye training enable. Writing 1 to this field starts the write data eye training sequence. This field will be cleared after the write data eye training is complete.
[8]	RW	rdet_en	Read data eye training enable. Writing 1 to this field starts the read data eye training sequence. This field will be cleared after the read data eye training is complete.
[7]	RW	wl2_en	Second write leveling enable. Writing 1 to this field starts write latency adjustment. This field will be cleared after adjustment is complete. Note that write leveling adjustment applies only to DDR3.
[6]	RW	gdst_en	PHY read data latch train enable. Writing 1 to this field starts the read data latch position training. This field will be cleared after write leveling is complete.
[5]	RW	gt_en	Gate training enable. Writing 1 to this field starts the gate training sequence. This field will be cleared after the gate training is complete.
[4]	RW	wl_en	Write leveling enable. Writing 1 to this field starts the write leveling sequence. This field will be cleared after write leveling is complete. Note that write leveling applies only to DDR3.
[3]	RW	zcal_en	Impedance calibration enable. This field is used to specify whether impedance calibration is executed. This bit will be cleared after impedance calibration is complete.
[2]	RW	dlymeas_en	Delay measurement enable. This field is used to enable initial delay measurement of the activated read delay line. If it is set to 1, delay measurement is enabled.
[1]	RW	pll_init_en	PLL initialization enable. If this field is used to activate the PLL initialization. If it is set to 1, the PLL is reset and waiting for a period of time for PLL to be locked.

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[0]	RW	init_en	PHY initialization enable. Writing 1 to this field triggers the PHY initialization sequence. The exact initialization executed is specified in bits 1−15 of this register. If PHY initialization is complete, this bit will be cleared. Note that writing 0 to this field has no effect.

PHYINITSTATUS

PHYINITSTATUS is a PHY status register.

Offset Address	Register Name	Total Reset Value
0x008	PHYINITSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					cat_err	wdet_err	rdet_err	wl2_err	gdst_err	gt_err	wl_err	zcal_err	dlymeas_err	pll_lock_err	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RWC	cat_err	CA training error. This field indicates whether an error occurs during CA training. Writing 1 to this field clears the error status.
[9]	RWC	wdet_err	Write data eye calibration error. This field indicates whether an error occurs during write data eye calibration. Writing 1 to this field clears the error status.
[8]	RWC	rdet_err	Read data eye calibration error. This field indicates whether an error occurs during read data eye calibration. Writing 1 to this field clears the error status.
[7]	RWC	wl2_err	Write leveling adjustment error. This field indicates whether an error occurs during write leveling adjustment. Writing 1 to this field clears the error status.
[6]	RWC	gdst_err	PHY read data latch train error. This field indicates whether an error occurs during read data latch training. Writing 1 to this field clears the error status.
[5]	RWC	gt_err	Gate training error. This field indicates whether an error occurs during gate training. Writing 1 to this field clears the error status.

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[4]	RWC	wl_err	Write leveling error. This field indicates whether an error occurs during write leveling. Writing 1 to this field clears the error status.
[3]	RWC	zcal_err	Impedance calibration error. This field indicates whether an error occurs during impedance calibration. Writing 1 to this field clears the error status.
[2]	RWC	dlymeas_err	Delay measurement fail. This field indicates whether one of the initial delay measurements fails. Writing 1 to this field clears the error status.
[1]	RWC	pll_lock_err	PLL locked fail. This field indicates whether one of the PLLs within the PHY fails to assert locked flag after t_pll_lock timer. Writing 1 to this field clears the error status.
[0]	RO	reserved	Reserved.

PHYCLKGATED

PHYCLKGATED is a PHY clock gating control register.

Offset Address	Register Name	Total Reset Value
0x000C	PHYCLKGATED	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	byp_pll_lock	reserved																		dx_phgated_men	dx_phclkgated	dx_phgated_en	ck_phy_clkgated	ac_phy_clkgated	reserved				dx_phy_clkgated			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	byp_pll_lock	PLL lock bypass. The user can assert this field to bypass the PLL lock signal when re-locking the PLL in the bypass mode (DFS) or when the PLL lock signal cannot be used. 0: use the PLL lock to gate the PHY clocks to prevent clock glitch 1: bypass the PLL lock (do not use the PLL lock signal to gate the PHY clocks)
[30:13]	RO	reserved	Reserved.

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[12]	RW	dx_phgated_men	PHY phase clock gated manual control enable. This field takes effect only when dx_phgated_en is 1'b0. If dx_phgated_en is high and this field is high, the user can use dx_phclkgated to manually control the clock gating of the PHY phase clock. 0: disabled 1: enabled
[11]	RW	dx_phclkgated	PHY phase clock gated control. This field takes effect only when dx_phgated_en is 1'b0. If dx_phgated_en is '1b1, this field is used, and the gated function is automatically controlled by PACK FSM. 0: The clock is disabled. 1: The clock is enabled.
[10]	RW	dx_phgated_en	PHY phase clock gated function (automatically controlled by PACK FSM) enable. 0: disabled 1: enabled
[9]	RW	ck_phy_clkgated	Dedicated clock gated control for the output CK and related circuits. 0: The clock is gated. 1: The clock is enabled. NOTE This field is automatically set to 1 when the PLL is locked without error.
[8]	RW	ac_phy_clkgated	Clock gated for the circuits in AC block except CK and CK related circuits. 0: The clock is gated. 1: The clock is enabled. NOTE This field is automatically set to 1 when the PLL is locked without error.
[7:4]	RO	reserved	Reserved.
[3:0]	RW	dx_phy_clkgated	Clock gated for circuits in data blocks. 0: The clock is gated. 1: The clock is enabled. NOTE This field is automatically set to 1 when the PLL is locked without error.

PHYTIMER0

PHYTIMER0 is a PHY timing parameter register. The timing parameters are required by the PHY.

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Offset Address	Register Name	Total Reset Value
0x010	PHYTIMER0	0x2710_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_dram_cke_high																				reserved				t_dram_reset							
Reset	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RW	t_dram_cke_high	DRAM CKE high initialization. This field specifies the number of PCLK clock cycles of the first DRAM command from CKE pulled to high (LPDDR2/LPDDR3 tINIT3).
[11:8]	RO	reserved	Reserved.
[7:0]	RW	t_dram_reset	DDR3 DRAM reset. This field is used to specify the time issuing reset signaling to the DRAM (number of PCLK clock cycles).

PHYTIMER1

PHYTIMER1 is a DRAM CKE low initialization register.

Offset Address	Register Name	Total Reset Value
0x014	PHYTIMER1	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																t_dram_cke_low															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	t_dram_cke_low	DRAM CKE low initialization. This field specifies the number of PCLK clock cycles during which CKE should be kept low after power is reset and the clock is stable.

PLLCTRL

PLLCTRL is a timing parameter register for the PLL in both address/command and data block.

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Offset Address	Register Name	Total Reset Value
0x018	PLLCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										pll_freq_range		reserved	pll_pwdn		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5:4]	RW	pll_freq_range	PLL frequency range select. This field specifies the frequency input range of the PLLs.
[3]	RO	reserved	Reserved.
[2:0]	RW	pll_pwdn	PLL power down. This field is used to set the power-down status of the PLL input. If this field is set to 1, the PLL power-down pin is activated. Writing 0 to this field will remove the deactivated PLL power down pin. Bit[2] for AC PLL Bit[1] for DX1 (DATA1) PLL Bit[0] for DX0 (DATA0) PLL

PLLTIMER

PLLTIMER is a PLL address/command and data block control register.

Offset Address	Register Name	Total Reset Value
0x01C	PLLTIMER	0x4E20_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_pll_lock																reserved								t_pll_rst							
Reset	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	t_pll_lock	PLL lock time. This field specifies the number of PCLK clock cycles waiting for the PLL to be locked.
[15:8]	RO	reserved	Reserved.

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[7:0]	RW	t_pll_rst	PLL reset time. This field specifies the number of PCLK clock cycles to issue reset to the PLL.

DLYMEASCTRL

DLYMEASCTRL is a read delay line delay measurement control register.

Offset Address	Register Name	Total Reset Value
0x020	DLYMEASCTRL	0x0000_0471

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	dly_track_limit							reserved	phy_autoref_en	dynamic_dqsen	dynamic_dqsgen	dynamic_dqsgth		dly_track_type	dly_meas_type
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:8]	RW	dly_track_limit	Delay tracking limit. This field specifies the maximum number of accumulated taps allowed while dynamic tracking.
[7]	RO	reserved	Reserved.
[6]	RW	phy_autoref_en	PHY auto-refresh tracking enable.
[5]	RW	dynamic_dqsen	Dynamic DQS tracking enable. This field should be set to high during delay measurement.
[4]	RW	dynamic_dqsgen	Dynamic DQSG tracking enable.
[3:2]	RW	dynamic_dqsgth	Dynamic DQSG update threshold. This field specifies the number of taps accumulated before the RDQSG delay line is updated. 0: update every 4 times 1: update every 2 times 2 or 3: update each time
[1]	RW	dly_track_type	Delay tracking type. This field specifies whether priority updated from the PHY is used during dynamic tracking. If this field is set to 1, the priority updated from the PHY is used.

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[0]	RW	dly_meas_type	Delay measurement type. This field specifies whether the delay measurement is for one clock cycle or half a clock cycle. If this field is set to 1, a full clock cycle is measured.

IMPCTRL

IMPCTRL is a ZQ calibration control register.

Offset Address	Register Name	Total Reset Value
0x024	IMPCTRL	0x8000_8020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	zcfuzzy_en	reserved															zcomp_num				reserved						zcomp_rsp_dly					
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	zcfuzzy_en	ZQ comparator result selection by weighted method. When this function is disabled, the precision is improved but ZQ comparison may fail. When this function is enabled, ZQ comparison is successful. 0: disabled 1: enabled (default)
[30:16]	RO	reserved	Reserved.
[15:12]	RW	zcomp_num	ZQ comparator iteration time. This field specifies the iteration time of zcomp changing detection.
[11:6]	RO	reserved	Reserved.
[5:0]	RW	zcomp_rsp_dly	ZQ comparator response time. This field specifies the delay of the zcomp result after zctrl is used.

IMPSTATUS

IMPSTATUS is a ZQ calibration status register.

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Offset Address	Register Name	Total Reset Value
0x028	IMPSTATUS	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	zcode_pdrv_cal							pdrv_cal_result	reserved	zcode_pdrv						reserved	zcode_ndrv_cal							ndrv_cal_result	reserved	zcode_ndrv					
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:24]	RO	zcode_pdrv_cal	P-drive impedance calibration code. This field shows the p-drive calibration code during impedance calibration.
[23]	RO	pdrv_cal_result	P-drive calibration result. This field specifies the ZQ calibration result. The valid values are as follows: 0: calibration done with OK. 1: calibration done with error. Writing 1 to this field clears this field.
[22]	RO	reserved	Reserved.
[21:16]	RW	zcode_pdrv	P-drive impedance control code. This field is used to specify the p-drive impedance control code. This register is updated by the user or is updated each time the ZQ calibration is complete.
[15]	RO	reserved	Reserved.
[14:8]	RO	zcode_ndrv_cal	N-drive impedance calibration code. This field shows the n-driver calibration code during impedance calibration.
[7]	RO	ndrv_cal_result	N-drive calibration result. This field specifies the ZQ calibration result. The valid values are as follows: 0: calibration done with OK. 1: calibration done with error Writing 1 to this field clears this field.
[6]	RO	reserved	Reserved.

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[5:0]	RW	zcode_ndrv	N-drive impedance control code. This field is used to specify the n-drive impedance control code. This register is updated by the user or is updated each time the ZQ calibration is complete.

DRAMCFG

DRAMCFG is a DRAM system configuration register.

Offset Address	Register Name	Total Reset Value
0x02C	DRAMCFG	0x0000_0405

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					lpddr23_zqc_en	lpddr23_mrw1617_en	lpddr23_pre_en	reserved	maddr_mir	ma2t	nosra	reserved		dcfg_type	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	lpddr23_zqc_en	LPDDR2/LPDDR3 initialization ZQC (init) enable. 0: disabled 1: issue ZQC(init) commands during initialization sequence rank by rank (default).
[9]	RW	lpddr23_mrw1617_en	LPDDR2/LPDDR3 initialization MRW16/17 enable. 0: disabled (default) 1: issue MRW16 then MRW17 commands during initialization sequence
[8]	RW	lpddr23_pre_en	LPDDR2/LPDDR3 initialization precharge all enable. 0: disabled (default) 1: issue the precharge all command before the reset command during initialization sequence
[7]	RO	reserved	Address mirroring. This bit should be set to 0 in single rank configuration
[6]	RW	maddr_mir	Address mirroring. This bit should be set to 0 in single rank configuration

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[5]	RW	ma2t	Two cycles on address/command. This field specifies whether the 2T timing should be used by the PHY controller that internally generates the DRAM command.
[4]	RW	nosra	No simultaneous rank access. This field specifies whether simultaneously rank access in the same clock cycle is allowed. If it set to 1, the rank access will be taken in turn. Note that this field can be enabled only when the number of ranks is 2 or 4. This field should be set to 0 in single rank configuration
[3]	RO	reserved	Reserved.
[2:0]	RW	dcfg_type	DRAM type selection. This field specifies the DDR RAM type. The valid values are as follows: 010: DDR3 101: LPDDR2/LPDDR3 Other values: reserved

DRAMTIMER0

DRAMTIMER0 is a DRAM timing parameter register.

NOTE

The command delay specified in this register applies only to the command issued by the PHY controller internally.

Offset Address	Register Name	Total Reset Value
0x030	DRAMTIMER0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_rc						t_rrd				t_ras						t_rcd				t_rp				t_wtr				t_rtp			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	t_rc	Activated to activated on same bank command delay.
[25:22]	RW	t_rrd	Activated to activated on different bank command delay.
[21:16]	RW	t_ras	Activated to precharge command delay.
[15:12]	RW	t_rcd	Activated to read/write delay.
[11:8]	RW	t_rp	Precharge command period. The unit is two clock cycles.
[7:4]	RW	t_wtr	Write to read command delay.

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[3:0]	RW	t_rtp	Read to precharge command delay.

DRAMTIMER1

Offset Address	Register Name	Total Reset Value
0x034	DRAMTIMER1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		t_rtw						t_rfc								reserved	t_faw							t_mod				t_mrd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:25]	RW	t_rtw	Read to write command delay. This field specifies whether to insert extra cycles between read and write commands to compensate tdqsck. This value should be 3 for the common condition when DDR3 is used. This value should be 6 for the common condition when LPDDR2/LPDDR3 is used.
[24:16]	RW	t_rfc	Refresh to refresh command delay.
[15]	RO	reserved	Reserved.
[14:9]	RW	t_faw	Four-bank activated period. This field applies only to the 8-bank device.
[8:4]	RW	t_mod	Load mode register to non load mode register command delay. This field is used as max (t_mod, t_mrd) in DDR3, max (t_mrw, tmrd) in LPDDR3, and t_mrw in LPDDR2.
[3:0]	RW	t_mrd	Load mode register to load mode register command delay. Not used.

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DRAMTIMER2

Offset Address	Register Name	Total Reset Value
0x038	DRAMTIMER2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_ccd	reserved	t_dllk										t_cke				reserved	t_xp					t_xs									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	t_ccd	Read to read and write to write command delay. 0 = BL/2 (for DDR3, this value should be 4) 1 = BL/2 + 1 (for DDR3, this value should be 5)
[30]	RO	reserved	Reserved.
[29:20]	RW	t_dllk	DLL lock time.
[19:16]	RW	t_cke	CKE minimum pulse width.
[15]	RO	reserved	Reserved.
[14:10]	RW	t_xp	Power down exit delay.
[9:0]	RW	t_xs	Self refresh exit delay.

DRAMTIMER3

Offset Address	Register Name	Total Reset Value
0x03C	DRAMTIMER3	0x0010_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_wr				t_wl				t_init5														t_zcal									
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	t_wr	Write recovery cycle.
[27:24]	RW	t_wl	Write latency (AL + CWL).
[23:10]	RW	t_init5	LPDDR device initialization time. This field specifies the time during which the LPDDR sets the DAI bit to 1.

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[9:0]	RW	t_zcal	ZQ calibration to command delay. This field specifies the number of clock cycles to wait after initial ZQ calibration. For DDR3 ZQ normal operation full calibration, this value is divided by 2. For DDR3 ZQ initialization calibration, this value is divided by 4. For LPDDR2/3, this field specifies the value of tZQINIT during initialization.

DRAMTIMER4

DRAMTIMER4 is a DRAM write leveling timing parameter register. This register applies only to the DDR3/LPDDR3 SDRAM.

Offset Address	Register Name	Total Reset Value
0x040	DRAMTIMER4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5 4	3 2 1 0
Name	reserved	t_odton	reserved		t_odt	t_wlo		reserved	t_wlmrd	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0		0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	t_odton	ODT turn-on latency (number of cycles from write command to assert of ODT).
[23:16]	RO	reserved	Reserved.
[15:12]	RW	t_odt	ODT turn-on cycles.
[11:7]	RW	t_wlo	Write leveling output delay. This field specifies the write leveling output delay in cycles (dficlk cycle).
[6]	RO	reserved	Reserved.
[5:0]	RW	t_wlmrd	Write leveling mode programmed (load mode register) to first DQS/DQS# rising edge delay (dficlk cycle).

ODTCR

ODTCR is a rank ODT control register while reading or writing to particular ranks.

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Offset Address	Register Name	Total Reset Value
0x044	ODTCR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wodt_rank3				wodt_rank2				wodt_rank1				wodt_rank0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:12]	RW	wodt_rank3	Write rank 3 ODT control. This field specifies the ODT issued while write on rank 3. The valid bit width is the number of ranks.
[11:8]	RW	wodt_rank2	Write rank 2 ODT control. This field specifies the ODT issued while write on rank 2. The valid bit width is the number of ranks.
[7:4]	RW	wodt_rank1	Write rank 1 ODT control. This field specifies the ODT issued while write on rank 1. The valid bit width is the number of ranks.
[3:0]	RW	wodt_rank0	Write rank 0 ODT control. This field specifies the ODT issued while write on rank 0. The valid bit width is the number of ranks.

TRAINCTRL0

TRAINCTRL0 is a training control register.

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Offset Address	Register Name	Total Reset Value
0x048	TRAINCTRL0	0xD044_1080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_eye_opening	dtrerrstop	gtds_rspdly						dqsg_cstep		dqsgrt_chk						dqsgrt_shft				dqsgsl_mrgn								dtr_rank			
Reset	1	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	skip_eye_opening	Skip eye opening of data eye training. This field specifies whether the eye opening should be skipped. If this field is set to 1, the eye opening before data eye training is skipped. If this field is set to 0, the eye opening is executed before data eye training.
[30]	RW	dtrerrstop	Data training error stop. This field controls whether the data training is terminated if an error occurs. The data training is stopped if this bit is set to 1. If this bit set to 0, the training will continue even an error occurs. The error status is recorded no matter when this field is set to 0 or 1.
[29:24]	RW	gtds_rspdly	Gate/Read latch training response delay. This field specifies the waiting time to check the response from PHY while gate and read latch training is performed (dficlk cycle).
[23:22]	RW	dqsg_cstep	Gate training coarse tuning step (the unit is phase). The recommended values are 0x0−0x2. 2'd0: step = 1 2'd1: step = 2 (default) 2'd2: step = 3 2'd3: step = 4
[21:16]	RW	dqsgrt_chk	Gate retraining check window. This field specifies the delta value to be checked during gate retraining check. The delta is added/subtracted to/from the read DQS gate. This position is checked to determine whether gating phase adjustment is required. The phase movement is the configured value multiple by 2. Note that 3'b000 is reserved and should not be used. The recommended values are 0x1−0x3.

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[15:10]	RW	dqsgrt_shft	Gate retraining shift window. This field specifies the value to be shifted if gate phase adjustment is required after gate retraining checks. The phase movement is the configured value multiple by 2. Note that 3'b000 is reserved and should not be used. The recommended value is dqsgrt_chk.
[9:4]	RW	dqsgsl_mrgn	Read DQS gate margin. This field specifies the margin to be reserved after the DQS gate training. The number of phases specified in this field is decreased to create DQS gating margin. The valid values are as follows: 6'b00100: 1/4 cycle 6'b01000: 1/2 cycle (recommended) 6'b01100: 3/4 cycle 6'b10000: 1 cycle Other values: reserved
[3:0]	RW	dtr_rank	Training rank. This field specifies the rank used for training. After the training, this field is used to select the source of rank specific settings.

RANKEN

RANKEN is a training rank control register.

Offset Address	Register Name	Total Reset Value
0x04C	RANKEN	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rank_en															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rank_en	Training rank enable. This field specifies whether the dtr_rank is enabled. 0: disabled 1: enabled (default) Bit 0 indicates rank 0. Bit 1 indicates rank 1. ... Bit 15 indicates rank 15. The maximum number of ranks is specified by the system.

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TRAINMADDR

TRAINMADDR is a data training memory start address register. The minimum space required for the data training is 64 bytes, and the allocated memory must be 64-byte-aligned.

Offset Address	Register Name	Total Reset Value
0x0050	TRAINMADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtrow																dtcol												reserved	dtbank		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	dtrow	Data training row address. This field is used to configure the memory row address required for the data training.
[15:4]	RW	dtcol	Data training column address. This field is used to configure the column address required for the data training. The field should be 0.
[3]	RO	reserved	Reserved.
[2:0]	RW	dtbank	Data training bank address. This field is used to configure the memory bank address required for the data training.

BISTCTRL

BISTCTRL is a BIST behavior register.

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Offset Address	Register Name	Total Reset Value
0x0054	BISTCTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7	6 5 4	3 2	1 0
Name	reserved		bist_fail_stop		reserved		bist_pat	reserved	bist_mode	reserved	bist_op
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0	0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	bist_fail_stop	BIST stop error count. This field specifies the number of failures at which the BIST should be stopped. If this field is set to 0x00, the BIST will run infinite until the BIST operation is stopped or reset. If a non-zero value is specified, the BIST is stopped while the accumulated errors reach the count specified in this field.
[15:10]	RO	reserved	Reserved.
[9:8]	RW	bist_pat	BIST pattern generation. This field specifies the BIST pattern generated for test. Note that bist_pat can be changed only when bist_done is 1. 00: walking 0 01: walking 1 10: LFSR-based random generation 11: user programmed
[7]	RO	reserved	Reserved.
[6:4]	RW	bist_mode	BIST mode select. This field specifies the BIST mode. The valid values are as follows: 000: pattern generated only 100: loopback before output buffer 101: loopback after output buffer 110: DRAM read/write mode Other values: reserved Note that bist_mode can be changed only when bist_done is 1. When the data loopback mode is selected, swapwl_en/swap_en must be set to all zeros (no swap).
[3:2]	RO	reserved	Reserved.

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[1:0]	RW	bist_op	During Reg write, this field is used for selecting the BIST operation. The valid values are as follows: 00: BIST stop 01: BIST run 10: BIST reset 11: reserved Writing the Reset clears all the status registers, and this field is cleared to BIST Stop. During Reg read, this field is for BIST active status (only bit 0 is valid, and bit1 is read as 1'b0). 0: BIST inactive 1: BIST active

BISTDATA0

BISTDATA0 is DRAM loopback test BIST data register 0.

NOTE

This register is valid only when bist_pat is set to "User Defined."

Offset Address	Register Name	Total Reset Value
0x0058	BISTDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bist_data_b3								bist_data_b2								bist_data_b1								bist_data_b0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	bist_data_b3	BIST data byte 3. This field is used as the fourth beat of burst during BIST test
[23:16]	RW	bist_data_b2	BIST data byte 2. This field is used as the third beat of burst during BIST test.
[15:8]	RW	bist_data_b1	BIST data byte 1. This field is used as the second beat of burst during BIST test.
[7:0]	RW	bist_data_b0	BIST data byte 0. This field is used as the first beat of burst during BIST test.

BISTDATA1

BISTDATA1 is DRAM loopback test BIST data register 1.

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Offset Address	Register Name	Total Reset Value
0x005C	BISTDATA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bist_data_b7		bist_data_b6		bist_data_b5		bist_data_b4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	bist_data_b7	BIST data byte 7. This field is used as the eighth beat of burst during BIST test
[23:16]	RW	bist_data_b6	BIST data byte 6. This field is used as the sixth beat of burst during BIST test.
[15:8]	RW	bist_data_b5	BIST data byte 5. This field is used as the fifth beat of burst during BIST test.
[7:0]	RW	bist_data_b4	BIST data byte 4. This field is used as the fourth beat of burst during BIST test.

BISTSTATUS

BISTSTATUS is a BIST test result and status register.

Offset Address	Register Name	Total Reset Value
0x0060	BISTSTATUS	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								bist_dxerr	bist_acerr	bist_done
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	bist_dxerr	BIST error on DX blocks. This bit shows whether any error occurs on the DXn during BIST test.
[1]	RO	bist_acerr	BIST error on AC block. This bit shows whether any error occurs on the AC during BIST test.

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[0]	RO	bist_done	BIST done. This field shows whether the BIST is complete. Note that if the BIST Stop Error Count field (bist_fail_stop) is set to 0, this field is never asserted.

MODEREG01

MODEREG01 is mode register content register 1.

Offset Address	Register Name	Total Reset Value
0x0064	MODEREG01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mr1																mr0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mr1	Mode register 1. For DDR/DDR2/DDR3/LPDDR, this field specifies the content of extend mode register 1. For LPDDR2/LPDDR3, this field defines the content of MR3/MR9 (mode register). bit[31:24]: MR9 OP bit[23:16]: MR3 OP
[15:0]	RW	mr0	Mode register 0. For DDR/DDR2/DDR3/LPDDR, this field specifies the content of mode register 0. For LPDDR2/LPDDR3, this field defines the mode registers MR1/MR2. bit[15:8]: MR2 OP bit[7:0]: MR1 OP

MODEREG23

MODEREG23 is mode register content register 2.

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Offset Address	Register Name	Total Reset Value
0x0068	MODEREG23	0xFF0A_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mr3																mr2															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mr3	Mode register 3. For DDR/DDR2/DDR3, this field specifies extend mode register 3. For LPDDR2/LPDDR3, this field is for the ZQ commands. bit[31:24]: OP bit[23:16]: MA The ZQ commands are issued rank by rank after tINIT5. bit[31:24]: MR10 OP bit[23:16]: MR10 MA
[15:0]	RW	mr2	Mode register 2. For DDR/DDR2/DDR3, this field specifies extend mode register 2. For LPDDR2/LPDDR3, this field specifies MR16/MR17. bit[15:8]: MR17 OP bit[7:0]: MR16 OP

DETPATTERN

DETPATTERN is a write/read DET pattern register.

NOTE

These fields are used to fine-tune the training procedure. You are advised not to modify them.

Offset Address	Register Name	Total Reset Value
0x006C	DETPATTERN	0x00FF_AA55

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_patFF								det_patAA								det_pat55							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	det_patFF	DET pattern 2.
[15:8]	RW	det_patAA	DET pattern 1.

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[7:0]	RW	det_pat55	DET pattern 0.

MISC

MISC is a miscellaneous control register.

Offset Address	Register Name	Total Reset Value
0x0070	MISC	0x0008_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	swapdfibyte_en		swapwl_en			swapdm_en		swapaddr_en		swap_en		cfg_dlyupd	addr_delay	swap_en_msb	addr_toggle	scramb_en	reserved				cfg_rl				reserved				cfg_wl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	swapdfibyte_en	Swap DFI byte lane. 00: no swap 01: swap
[29:27]	RW	swapwl_en	Swap WL/CA result. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 Note: When the data BIST loopback mode is selected, this field must be set to 0x0.
[26:25]	RW	swapdm_en	Swap DM bus. 00: no swap 01: 16-bit T2 swap
[24:23]	RW	swapaddr_en	Swap address bus. 00: no swap 01: 32-bit flyby-4, flyby-2 swap 10: 16-bit T-2 swap

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[22:21]	RW	swap_en	Swap DQ bus bit[1:0]. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 NOTE When the data BIST loopback mode is selected, this field must be set to 0x0.
[20]	RW	cfg_dlyupd	Transparent mode for the delay update module. When this bit is set to 1, the delay setting in registers are applied to the PHY immediately.
[19]	RW	addr_delay	Add 1-T delay on address/command. This bit must be set to 1 when CWL is 5.
[18]	RW	swap_en_msb	Swap DQ bus bit[2]. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 NOTE When the data BIST loopback mode is selected, this field must be set to 0x0.
[17]	RW	addr_toggle	Toggle address bus every clock cycle. This bit is set to 1 only for the burn-in test.
[16]	RW	scramb_en	Data scrambler enable. Set this field to 1 to enable data scramble function
[15:12]	RO	reserved	Reserved.
[11:7]	RW	cfg_rl	PHY read latency. It defines the number of cycles from read command to assert of rddata_en and is equal to CL + AL − 2 (for LPDDR2/3, the field should be RL-2).
[6:5]	RO	reserved	Reserved.
[4:0]	RW	cfg_wl	PHY write latency. It defines the number of cycles from write command to assert of wrdata_en and is equal to CWL + AL − 1 (for LPDDR2/3, the field should be WL + 1). If the DFI clock ratio is 1:2, cfg_wl must be greater than or equal to 2.

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RNK2RNK

RNK2RNK is a rank-to-rank delay control register.

Offset Address	Register Name	Total Reset Value
0x0074	RNK2RNK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			trnkwtr	trnkrtw	trnkrtr		trnkwtw
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	trnkwtr	Delay from write to read command targeted to different ranks.
[14:10]	RW	trnkrtw	Delay from read to write command targeted to different ranks.
[9:5]	RW	trnkrtr	Delay from read to read command targeted to different ranks.
[4:0]	RW	trnkwtw	Delay from write to write command targeted to different ranks.

PHYCTRL0

PHYCTRL0 is PHY control register 0.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x0078	PHYCTRL0	0x0000_3980

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14	13	12	11	10 9 8	7	6 5 4	3 2	1 0
Name	reserved					resetoen	csoen	ckeoen	ckoen	cmdoen	reserved	lp_ck_sel	sel_pos_rx	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1	1	1	0 0 1	1	0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13]	RW	resetoen	Set this field to default value.
[12]	RW	csoen	Set this field to default value.
[11]	RW	ckeoen	Set this field to default value.
[10:8]	RW	ckoen	Set this field to default value.
[7]	RW	cmdoen	Set this field to default value.

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[6:5]	RO	reserved	Set this field to default value.
[4:3]	RW	lp_ck_sel	Set this field to default value.
[2]	RW	sel_pos_rx	PHY output trigger edge select. 0: falling edge 1: rising edge
[1:0]	RO	reserved	Reserved.

PHYDBG

PHYDBG is a PHY debug register.

Offset Address	Register Name	Total Reset Value
0x007C	PHYDBG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dqsb_gated_error								reserved								dqs_gated_error							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	dqsb_gated_error	DQSN gated error flag. This error flag can be cleared only by issuing PHY reset.
[15:8]	RO	reserved	Reserved.
[7:0]	RO	dqs_gated_error	DQS gated error flag. This error flag can be cleared only by issuing PHY reset.

RETCTRL0

RETCTRL0 is a retraining control register.

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Offset Address	Register Name	Total Reset Value
0x0080	RETCTRL0	0x0001_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	retrain_thrd																reserved	gtrten	retrain_en		phyupd_resp											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	retrain_thrd	Retraining threshold. The PHY counts the number of AREFs issued by MC. When the number reaches the threshold, the retraining operation is triggered to be started. Only a non-zero value is valid.
[15]	RO	reserved	Reserved.
[14]	RW	gtrten	Gate retraining active. This field controls whether the gate retraining is executed during retraining on-going. This field should be asserted only after the initial gate training is complete.
[13]	RW	retrain_en	PHY retraining enable. This field controls whether the PHY is enabled to request memory controller for retraining.
[12:0]	RW	phyupd_resp	PHY update response latency. When the PHY asserts dfi_phyupd_req to MC, MC should assert dfi_phyupd_ack no later than the number of cycles configured by the response latency.

DMSEL

DMSEL is a DM swap selection register.

Offset Address	Register Name	Total Reset Value
0x0084	DMSEL	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dxctl_dmswap_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	dxctl_dmswap_sel	bit[3:2]: DM1 swap select bit[1:0]: DM0 swap select

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IOCTL

IOCTL is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x0088	IOCTL	0x4BFF_F801

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	odtsel_dqs				odtsel				ronsel_ck				ronsel_ac2t				ronsel_ac1t				ronsel_dqs				ronsel				reserved								aciopldn	dxiopldn	diff_dqs_en
Reset	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:29]	RW	odtsel_dqs	Matched ODT impedance of the RX terminal for the DQS signal. The configurations are the same as those of odtsel.
[28:26]	RW	odtsel	Matched ODT impedance of the RX terminal for the DQ signal 000: 0 Ω 001: 120 Ω 010: 60 Ω 011: 40 Ω 100: 40 Ω 101: 30 Ω 110: N/A 111: 20 Ω
[25:23]	RW	ronsel_ck	Driver impedance of the differential clock signal The configurations are the same as those of ronsel.
[22:20]	RW	ronsel_ac2t	Driver impedance of the 2T address and command signals (RAS, CAS, WEN, ADDR, and BA) The configurations are the same as those of ronsel.
[19:17]	RW	ronsel_ac1t	Driver impedance of the 1T signals (CKE, ODT, CS, and RESET) The configurations are the same as those of ronsel.
[16:14]	RW	ronsel_dqs	Driver impedance of the DQS signal The configurations are the same as those of ronsel.

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[13:11]	RW	ronsel	Driver impedance of the DQ signal 110: RON = 40 Ω 111: RON = 34 Ω 000: RON = 240 Ω 001: RON = 120 Ω 010: RON = 80 Ω 011: RON = 60 Ω 100: RON = 60 Ω 101: RON = 48 Ω
[10:3]	RO	reserved	Reserved.
[2]	RW	aciopldn	Set this field to default value.
[1]	RW	dxiopldn	Set this field to default value.
[0]	RW	diff_dqs_en	Differential DQS enable.

DQSSEL

DQSSEL is a PHY DQ swap register.

Offset Address	Register Name	Total Reset Value
0x008C	DQSSEL	0xFF00_FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqswap_sel																															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dqswap_sel	DQ swap in PHY. Each bit determines the relative DQS with DQ. 0: relative to DQS0 1: relative to DQS1

PHYCTRL1

PHYCTRL1 is an AC PHY control register.

NOTE

Register in this field are connected to PHY interface directly

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Offset Address	Register Name	Total Reset Value
0x0090	PHYCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ac_pll_cal	ac_pll_calm	ac_pll_calt	ac_pll_lt		ac_pll_sp		ac_pll_cpi				ac_pll_init	ac_pll_testen	ac_pll_testpem	ac_pll_thrm	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	ac_pll_cal	The value 0x0 is recommended.
[29]	RW	ac_pll_calm	The value 0x0 is recommended.
[28]	RW	ac_pll_calt	The value 0x0 is recommended.
[27:26]	RW	ac_pll_lt	The value 0x0 is recommended.
[25:23]	RW	ac_pll_sp	The value 0x2 is recommended.
[22:20]	RW	ac_pll_cpi	The value 0x4 is recommended.
[19]	RW	ac_pll_init	The value 0x0 is recommended.
[18]	RW	ac_pll_testen	The value 0x0 is recommended.
[17]	RW	ac_pll_testpem	The value 0x0 is recommended.
[16]	RW	ac_pll_thrm	The value 0x0 is recommended.
[15:0]	RO	reserved	Reserved.

DXNCKCTRL

DXNCKCTRL is a PLL phase selection (within the PHY) register. You are advised not to modify this register.

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Offset Address	Register Name	Total Reset Value
0x0094	DXNCKCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dx_ckd2			dx_ck0p_mclk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5:3]	RW	dx_ckd2	Set this field to default value.
[2:0]	RW	dx_ck0p_mclk	Set this field to default value.

PHYPLLCTRL_AC

PHYPLLCTRL_AC is PHY PLL control register 1.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x0098	PHYPLLCTRL_AC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_pll_lock	reserved																							ac_pll_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ac_pll_lock	AC PLL lock signal. 0: not locked 1: locked
[30:8]	RO	reserved	Reserved.
[7:0]	RW	ac_pll_test	AC PLL test mode. 0: normal mode 1: test mode

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PHYPLLCTRL_DX

PHYPLLCTRL_DX is PHY PLL control register 2.

Offset Address	Register Name	Total Reset Value
0x009C	PHYPLLCTRL_DX	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dx_pll_lock	reserved			dx_pll_test			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	dx_pll_lock	ND: number of data PHY blocks DX PLL lock signals for each byte lane 0: not locked 1: locked
[27:16]	RO	reserved	Reserved.
[15:0]	RW	dx_pll_test	PLL test for 16-bit data block bit[7:0]: 16-bit block 0 bit[15:8]: 16-bit block 1

SWTMODE

SWTMODE is an S/W training mode register.

Offset Address	Register Name	Total Reset Value
0x00A0	SWTMODE	0x0000_0000

Bit	31	30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	wl_wdqs_gated	reserved								sw_gtmode	sw_wlmode
Reset	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31]	RW	wl_wdqs_gated	Write leveling WDQS strobe disable when the related PH/BDL is tuned to prevent glitch. 0: not gated 1: gated (disable WDQS strobe)

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[30:2]	RO	reserved	Reserved.
[1]	RW	sw_gtmode	Set this bit to 1 when performing S/W gate training or GDS training.
[0]	RW	sw_wlmode	Set this bit to 1 when performing S/W write leveling training.

SWTWLDQS

SWTWLDQS is a write DQS issue register during S/W write leveling training.

Offset Address	Register Name	Total Reset Value
0x00A4	SWTWLDQS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sw_wl_dqs
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	sw_wl_dqs	Writing 1 to this bit once issues one DQS pulse from the PHY to DRAM.

SWTRLT

SWTRLT is an S/W training result register.

Offset Address	Register Name	Total Reset Value
0x00A8	SWTRLT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gds_result								gt_result								wl_dq_result							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	gds_result	Each bit corresponds to one byte lane.
[15:8]	RO	gt_result	Each bit corresponds to one byte lane.
[7:0]	RO	wl_dq_result	Each bit corresponds to one byte lane.

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PHYCTRL2

PHYCTRL2 is PHY control register 2.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x00AC	PHYCTRL2	0x0000_000B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											phy_dyn_pupden	phy_dummypad_use	phy_odten_gated	phy_gatetdc	phy_dqsgerror
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	phy_dyn_pupden	DATA16BIT_blk.reg_dynamic_PUPDEN_16b control.
[3]	RW	phy_dummypad_use	DATA16BIT_blk.reg_dummypad_use control.
[2]	RW	phy_odten_gated	DATA16BIT_blk.reg_ODTEN_Gated control.
[1]	RW	phy_gatetdc	DATA16BIT_blk.BUFRESETCONTN_gated_TDC control.
[0]	RW	phy_dqsgerror	DATA16BIT_blk.BUFRESETCONTN_gated_DQSGERROR control.

IOCTL1

IOCTL1 is I/O PHY control register 1.

NOTE

Register in this field are connected to PHY interface directly

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Offset Address	Register Name	Total Reset Value
0x00B0	IOCTL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ioctl_squeach_pd	reserved	ioctl_genvref_pd		ioctl_genvref_ie		ioctl_popmode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	ioctl_squeach_pd	Set this field to default value.
[23:18]	RO	reserved	Reserved.
[17:12]	RW	ioctl_genvref_pd	Set this field to default value.
[11:6]	RW	ioctl_genvref_ie	Set this field to default value.
[5:0]	RW	ioctl_popmode	Set this field to default value.

IOCTL2

IOCTL2 is I/O PHY control register 2.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x00B4	IOCTL2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ioctl_genvref_refsel_2	ioctl_genvref_refsel_1	ioctl_genvref_refsel_0		ioctl_genvref_rangel_1		ioctl_genvref_rangel_0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:24]	RW	ioctl_genvref_refsel_2	Set this field to default value.
[23:18]	RW	ioctl_genvref_refsel_1	Set this field to default value.
[17:12]	RW	ioctl_genvref_refsel_0	Set this field to default value.

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[11:6]	RW	ioctl_genvref_range1_1	Set this field to default value.
[5:0]	RW	ioctl_genvref_range1_0	Set this field to default value.

BISTTIMER

BISTTIMER is a code update period register during BIST running.

Offset Address	Register Name	Total Reset Value
0x00B8	BISTTIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bstupdt_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	bstupdt_timer	BIST update code timer. This field controls the code update period. If this field is programmed to a non-zero value, the BIST is temporarily stopped, and the internal delay code is updated to the PHY when the timer reaches the configured value. The BIST will continue if the code update is complete. If this field is programmed to zero, the update code mechanism is disabled.

TRAINCTRL1

TRAINCTRL1 is data training control register 1.

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Offset Address	Register Name	Total Reset Value
0x00D0	TRAINCTRL1	0xF036_F026

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdet_lbs_en	rdet_ds_en	rdet_rbs_en	rdet_av_en	reserved	rdet_rb_backtap							rdet_samp_num				wdet_lbs_en	wdet_ds_en	wdet_rbs_en	wrdet_av_en	reserved				wdet_rb_backtap				wdet_samp_num			
Reset	1	1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	1	0	0	1	1	0

Bits	Access	Name	Description
[31]	RW	rdet_lbs_en	Read DET left boundary search enable.
[30]	RW	rdet_ds_en	Read DET deskew enable.
[29]	RW	rdet_rbs_en	Read DET right boundary search enable.
[28]	RW	rdet_av_en	Read DET average stage enable
[27]	RO	reserved	Reserved.
[26:20]	RW	rdet_rb_backtap	Read DET right boundary back tap. This field is used to offset (+) the rdqsbdl before the right boundary search is started to overcome meta-sable zone.
[19:16]	RW	rdet_samp_num	Read DET sample number control. The multiple sample is used to overcome the meta situations. Valid value: 1−15
[15]	RW	wdet_lbs_en	Write DET left boundary search enable.
[14]	RW	wdet_ds_en	Write DET deskew enable.
[13]	RW	wdet_rbs_en	Write DET right boundary search enable.
[12]	RW	wrdet_av_en	Write DET average stage enable.
[11:8]	RO	reserved	Reserved.
[7:4]	RW	wdet_rb_backtap	Write DET right boundary back tap. This field is used to offset (−) the wdqphase before the right boundary search is started to overcome meta-sable zone.
[3:0]	RW	wdet_samp_num	Write DET sample number control. The multiple sample is used to overcome the meta situations. Valid value: 1−15

TRAINCTRL2

TRAINCTRL2 is data training control register 2.

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Offset Address	Register Name	Total Reset Value
0x00D4	TRAINCTRL2	0x0000_CC55

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdet_method_sel	mrr_pat_order			mrr_bl4	reserved		gds_automrg_en	mrr_pat_mask								mrr_pat_B								mrr_pat_A							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31]	RW	rdet_method_sel	Read DET method select. 0: write-then-read 1: MRR32/40 (only for LPDDR3)
[30:28]	RW	mrr_pat_order	MRR pattern order. If MRR is used in the read DET, PACK will issue three MRR commands. The order is indicated by bit 2 -> bit 1 -> bit 0. 0: MRR32 1: MRR40
[27]	RW	mrr_bl4	MRR burst 4 indicator. If MRR is used in the read DET, PACK needs to know whether MRR burst is 4 (LPDDR2) or 8 (LPDDR3). 0: MRR32/40 burst length = 8 (default) 1: MRR32/40 burst length = 4
[26:25]	RO	reserved	Reserved.
[24]	RW	gds_automrg_en	GDS training/retraining auto tuning enable. 0: disable GDS auto margin tuning (will increase GDS when GDS training/retraining is complete) 1: enable GDS auto margin tuning (default)
[23:16]	RW	mrr_pat_mask	MRR pattern mask. 0: not masked 1: masked (does not compare data)
[15:8]	RW	mrr_pat_B	MRR40 pattern. This field should comply with the LPDDR2/LPDDR3 specifications.
[7:0]	RW	mrr_pat_A	MRR32 pattern. This field should comply with the LPDDR2/LPDDR3 specifications.

REGBANKCTRL

REGBANKCTRL is register bank control register.

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Offset Address	Register Name	Total Reset Value
0x00D8	REGBANKCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														op_sel	wr_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	op_sel	Register bank select related to DFS. 0: bank 0 for PHY operating 1: bank 1 for PHY operating
[0]	RW	wr_sel	Register bank select related to DFS. 0: bank 0 while APB read/write 1: bank 1 while APB read/write

TRAINCTRL3

TRAINCTRL3 is data training control register 3.

Offset Address	Register Name	Total Reset Value
0x00DC	TRAINCTRL3	0x8002_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exd_gtres_en	reserved											gdsrt_backtap				reserved				rpat_cnt_num_open				reserved				rpat_cnt_num			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	exd_gtres_en	Extended gate result enable. When this field is set as high, the PACK will use additional information (EN_DQSx_regread) to help extend the gate result in the "fine tune stage of gate training" and "gate retraining." 0: disabled 1: enabled (default)
[30:19]	RO	reserved	Reserved.

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[18:16]	RW	gdsrt_backtap	GDS retraining back tap. This field controls the number of back taps during GDS retraining. The value range is 1−7. The recommended value range is 1−2.
[15:12]	RO	reserved	Reserved.
[11:8]	RW	rpat_cnt_num_open	RDET pattern length control for eye open. This field is used to set the pattern length for eye open. The same RDET pattern will be extended as the following settings (field value + 1): 0x0: pattern length = 1 0x1: pattern length = 2 ... 0xF: pattern length = 16
[7:4]	RO	reserved	Reserved.
[3:0]	RW	rpat_cnt_num	RDET pattern length control. This field is used to set the pattern length. The same RDET pattern will be extended as the following settings (field value + 1): 0x0: pattern length = 1 0x1: pattern length = 2 ... 0xF: pattern length = 16

ACBISTCTRL0

ACBISTCTRL0 is comparison control register 0 while BIST activated.

Offset Address	Register Name	Total Reset Value
0x100	ACBISTCTRL0	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_rdffsel			aclpbk_tg	acbist_en	rst_cmp_mask	cs_cmp_mask				ras_cmp_mask	cas_cmp_mask	we_cmp_mask	ba_cmp_mask			addr_cmp_mask															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	ac_rdffsel	AC loopback read latch select.
[28]	RW	aclpbk_tg	AC loopback toggle control. The user should not modify this bit. It is related to the analog PHY design. 0: 28LPP PHY (default) 1: 40PHY

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[27]	RW	acbist_en	BIST enable. This field specifies whether the AC block is included for loopback test while bist_op is set to BIST Enable.
[26]	RW	rst_cmp_mask	RST loopback compare mask. This field controls whether the comparison of the loopback data on the RST bit is disabled. 0: not compared 1: compared
[25:22]	RW	cs_cmp_mask	CS loopback compare mask. This field controls whether the comparison of the loopback data on the CS bits is disabled. 0: not compared 1: compared
[21]	RW	ras_cmp_mask	RAS loopback compare mask. This field controls whether the comparison of the loopback data on RAS is disabled. 0: not compared 1: compared
[20]	RW	cas_cmp_mask	CAS loopback compare mask. This field controls whether the comparison of the loopback data on CAS is disabled. 0: not compared 1: compared
[19]	RW	we_cmp_mask	Write enable loopback compare mask. This field controls whether the comparison of the loopback data on WE is disabled. 0: not compared 1: compared
[18:16]	RW	ba_cmp_mask	Bank address loopback compare mask. This field controls whether the comparison of the loopback data on bank address bits is disabled. 0: not compared 1: compared
[15:0]	RW	addr_cmp_mask	Memory address loopback compare mask. This field controls whether the comparison of the loopback data on address bits is disabled. 0: not compared 1: compared

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ACBISTCTRL1

ACBISTCTRL1 is comparison control register 1 while BIST activated.

Offset Address	Register Name	Total Reset Value
0x104	ACBISTCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ac_lfsr_seed								cke_cmp_mask				odt_cmp_mask			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	ac_lfsr_seed	LFSR seed value. This field specifies the initial seed value of the LFSR generator to this byte lane.
[7:4]	RW	cke_cmp_mask	CKE loopback compare mask. This field controls whether the comparison of the loopback data on CKE bits is disabled. 0: not compared 1: compared
[3:0]	RW	odt_cmp_mask	ODT loopback compare mask. This field controls whether the comparison of the loopback data on ODT bits is disabled. 0: not compared 1: compared

ACBISTSTS0

ACBISTSTS0 is BIST test result and status register 0.

NOTE

This register is read-only, and can only be reset by setting bist_op to BIST Reset.

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Offset Address	Register Name	Total Reset Value
0x108	ACBISTSTS0	0x0000_0000

Bit	31 30 29 28	27	26	25 24	23 22	21	20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		rst_bist_err	cs_bist_err		ras_bist_err	cas_bist_err	we_bist_err	ba_bist_err	addr_bist_err			
Reset	0 0 0 0	0	0	0 0	0 0	0	0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26]	RO	rst_bist_err	BIST error on RST.
[25:22]	RO	cs_bist_err	BIST error on CS.
[21]	RO	ras_bist_err	BIST error on RAS.
[20]	RO	cas_bist_err	BIST error on CAS.
[19]	RO	we_bist_err	BIST error on write enable.
[18:16]	RO	ba_bist_err	BIST error on bank address.
[15:0]	RO	addr_bist_err	BIST error on address bus.

ACBISTSTS1

ACBISTSTS1 is BIST test result and status register 1.

NOTE

This register is read-only, and can only be reset by setting bist_op to BIST Reset.

Offset Address	Register Name	Total Reset Value
0x10C	ACBISTSTS1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						cke_bist_err	odt_bist_err
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:4]	RO	cke_bist_err	BIST error on CKE.
[3:0]	RO	odt_bist_err	BIST error on ODT.

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ACCMDBDL0

ACCMDBDL0 is AC command bit delay line configuration register 0.

Offset Address	Register Name	Total Reset Value
0x120	ACCMDBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												odt1_bdl				reserved												odt0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt1_bdl	Bit delay line of ODT1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	odt0_bdl	Bit delay line of ODT0.

ACCMDBDL1

ACCMDBDL1 is AC command bit delay line configuration register 1.

Offset Address	Register Name	Total Reset Value
0x124	ACCMDBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												odt3_bdl				reserved												odt2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt3_bdl	Bit delay line of ODT3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	odt2_bdl	Bit delay line of ODT2.

ACCMDBDL2

ACCMDBDL2 is AC command bit delay line configuration register 2.

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Offset Address	Register Name	Total Reset Value
0x128	ACCMDBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cs1_bdl				reserved												cs0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs1_bdl	Bit delay line of CS1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs0_bdl	Bit delay line of CS0.

ACCMDBDL3

ACCMDBDL3 is AC command bit delay line configuration register 3.

Offset Address	Register Name	Total Reset Value
0x12C	ACCMDBDL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cs3_bdl				reserved												cs2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs3_bdl	Bit delay line of CS3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs2_bdl	Bit delay line of CS2.

ACCMDBDL4

ACCMDBDL4 is AC command bit delay line configuration register 4.

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Offset Address	Register Name	Total Reset Value
0x130	ACCMDBDL4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cke1_bdl	reserved			cke0_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cke1_bdl	Bit delay line of CKE1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cke0_bdl	Bit delay line of CKE0.

ACCMDBDL5

ACCMDBDL5 is AC command bit delay line configuration register 5.

Offset Address	Register Name	Total Reset Value
0x134	ACCMDBDL5	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cke3_bdl	reserved			cke2_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cke3_bdl	Bit delay line of CKE3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cke2_bdl	Bit delay line of CKE2.

ACCMDBDL6

ACCMDBDL6 is AC command bit delay line configuration register 6.

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Offset Address	Register Name	Total Reset Value
0x138	ACCMDBDL6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cas_bdl	reserved			we_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cas_bdl	Bit delay line of CAS.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	we_bdl	Bit delay line of WE.

ACCMDBDL7

ACCMDBDL7 is AC command bit delay line configuration register 7.

Offset Address	Register Name	Total Reset Value
0x13C	ACCMDBDL7	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			resetn_bdl	reserved			ras_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	resetn_bdl	Bit delay line of RESETN.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	ras_bdl	Bit delay line of RAS.

ACADDRBDL0

ACADDRBDL0 is AC address bit delay line configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x140	ACADDRBDL0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr1_bdl	reserved			addr0_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr1_bdl	Bit delay line of ADDR1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr0_bdl	Bit delay line of ADDR0.

ACADDRBDL1

ACADDRBDL1 is AC address bit delay line configuration register 1.

Offset Address	Register Name	Total Reset Value
0x144	ACADDRBDL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr3_bdl	reserved			addr2_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr3_bdl	Bit delay line of ADDR3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr2_bdl	Bit delay line of ADDR2.

ACADDRBDL2

ACADDRBDL2 is AC address bit delay line configuration register 2.

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Offset Address	Register Name	Total Reset Value
0x148	ACADDRBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr5_bdl				reserved												addr4_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr5_bdl	Bit delay line of ADDR5.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr4_bdl	Bit delay line of ADDR4.

ACADDRBDL3

ACADDRBDL3 is AC address bit delay line configuration register 3.

Offset Address	Register Name	Total Reset Value
0x14C	ACADDRBDL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr7_bdl				reserved												addr6_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr7_bdl	Bit delay line of ADDR7.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr6_bdl	Bit delay line of ADDR6.

ACADDRBDL4

ACADDRBDL4 is AC address bit delay line configuration register 4.

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Offset Address	Register Name	Total Reset Value
0x150	ACADDRBDL4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr9_bdl	reserved			addr8_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr9_bdl	Bit delay line of ADDR9.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr8_bdl	Bit delay line of ADDR8.

ACADDRBDL5

ACADDRBDL5 is AC address bit delay line configuration register 5.

Offset Address	Register Name	Total Reset Value
0x154	ACADDRBDL5	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr11_bdl	reserved			addr10_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr11_bdl	Bit delay line of ADDR11.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr10_bdl	Bit delay line of ADDR10.

ACADDRBDL6

ACADDRBDL6 is AC address bit delay line configuration register 6.

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Offset Address	Register Name	Total Reset Value
0x158	ACADDRBDL6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr13_bdl	reserved			addr12_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr13_bdl	Bit delay line of ADDR13.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr12_bdl	Bit delay line of ADDR12.

ACADDRBDL7

ACADDRBDL7 is AC address bit delay line configuration register 7.

Offset Address	Register Name	Total Reset Value
0x15C	ACADDRBDL7	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			addr15_bdl	reserved			addr14_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr15_bdl	Bit delay line of ADDR15.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr14_bdl	Bit delay line of ADDR14.

ACADDRBDL8

ACADDRBDL8 is AC address bit delay line configuration register 8.

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Offset Address	Register Name	Total Reset Value
0x160	ACADDRBDL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ba1_bdl				reserved												ba0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	ba1_bdl	Bit delay line of BA1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	ba0_bdl	Bit delay line of BA0.

ACADDRBDL9

ACADDRBDL9 is AC address bit delay line configuration register 9.

Offset Address	Register Name	Total Reset Value
0x164	ACADDRBDL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ba2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	ba2_bdl	Bit delay line of BA2.

ACCLKBDL

ACCLKBDL is an AC clock bit delay line configuration register.

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Offset Address	Register Name	Total Reset Value
0x168	ACCLKBDL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	fbclk_bdl	reserved	refclk_bdl	reserved	dramclk1_bdl	reserved	dramclk0_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	fbclk_bdl	Bit delay line of FBCLK.
[23:21]	RO	reserved	Reserved.
[20:16]	RW	refclk_bdl	Bit delay line of REFCLK.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	dramclk1_bdl	Set this field to default value.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	dramclk0_bdl	Set this field to default value.

ACPHYCTL0

ACPHYCTL0 is AC block PHY control register 0. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x170	ACPHYCTL0	0x0000_0010

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved							bufphyclk_div2	lvdqclkdiv2	dramclk_l	dramclk_h	margin_a1	margin_a0	enshift_a0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6]	RW	bufphyclk_div2	PHY control.

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[5]	RW	lvdqclkdiv2	PHY control.
[4]	RW	dramclk_l	PHY control.
[3]	RW	dramclk_h	PHY control.
[2]	RW	margin_a1	PHY control.
[1]	RW	margin_a0	PHY control.
[0]	RW	enshift_a0	PHY control.

ACPHYCTL1

ACPHYCTL1 is AC block PHY control register 1. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x174	ACPHYCTL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dram1sel_addr																reserved					dram1sel_ba			reserved	dram1sel_we	dram1sel_cas	dram1sel_ras	dram1sel_odt	dram1sel_cke	dram1sel_cs	dram1sel_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	dram1sel_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	dram1sel_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	dram1sel_we	PHY control.
[5]	RW	dram1sel_cas	PHY control.
[4]	RW	dram1sel_ras	PHY control.
[3]	RW	dram1sel_odt	PHY control.
[2]	RW	dram1sel_cke	PHY control.
[1]	RW	dram1sel_cs	PHY control.
[0]	RW	dram1sel_reset	PHY control.

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ACPHYCTL2

ACPHYCTL2 is AC block PHY control register 2. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x178	ACPHYCTL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdrsel_addr																Reserved.					sdrsel_ba			Reserved.	sdrsel_we	sdrsel_cas	sdrsel_ras	sdrsel_odt	sdrsel_cke	sdrsel_cs	sdrsel_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sdrsel_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	sdrsel_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	sdrsel_we	PHY control.
[5]	RW	sdrsel_cas	PHY control.
[4]	RW	sdrsel_ras	PHY control.
[3]	RW	sdrsel_odt	PHY control.
[2]	RW	sdrsel_cke	PHY control.
[1]	RW	sdrsel_cs	PHY control.
[0]	RW	sdrsel_reset	PHY control.

ACPHYCTL3

ACPHYCTL3 is AC block PHY control register 3. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x17C	ACPHYCTL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	posedge_addr																reserved.					posedge_ba			reserved.	posedge_we	posedge_cas	posedge_ras	posedge_odt	posedge_cke	posedge_cs	posedge_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	posedge_addr	PHY control.
[15:11]	RO	reserved	Reserved.
[10:8]	RW	posedge_ba	PHY control.
[7]	RO	reserved	Reserved.
[6]	RW	posedge_we	PHY control.
[5]	RW	posedge_cas	PHY control.
[4]	RW	posedge_ras	PHY control.
[3]	RW	posedge_odt	PHY control.
[2]	RW	posedge_cke	PHY control.
[1]	RW	posedge_cs	PHY control.
[0]	RW	posedge_reset	PHY control.

ACPHYCTL4

ACPHYCTL4 is AC block PHY control register 4. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x180	ACPHYCTL4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	timing2T_addr				reserved.	timing2T_ba	reserved.	timing2T_we	timing2T_cas	timing2T_ras	timing2T_odt	timing2T_cke	timing2T_cs	timing2T_reset
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	timing2T_addr	PHY control.
[15:11]	RO	reserved	Reserved.
[10:8]	RW	timing2T_ba	PHY control.
[7]	RO	reserved	Reserved.
[6]	RW	timing2T_we	PHY control.
[5]	RW	timing2T_cas	PHY control.
[4]	RW	timing2T_ras	PHY control.
[3]	RW	timing2T_odt	PHY control.
[2]	RW	timing2T_cke	PHY control.
[1]	RW	timing2T_cs	PHY control.
[0]	RW	timing2T_reset	PHY control.

ACPHYCTL5

ACPHYCTL5 is AC block PHY control register 5. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x184	ACPHYCTL5	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	clk1x_cmd2t_ctl2	clk1x_mclk	clk1x_cmd1t	clk1x_cmd2t	clk1x_cmd2t_ctl	clk1x_dramclk1	clk1x_dramclk0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	clk1x_cmd2t_ctl2	PHY control.

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[23:20]	RW	clk1x_mclk	PHY control.
[19:16]	RW	clk1x_cmd1t	PHY control.
[15:12]	RW	clk1x_cmd2t	PHY control.
[11:8]	RW	clk1x_cmd2t_ctl	PHY control.
[7:4]	RW	clk1x_dramclk1	PHY control.
[3:0]	RW	clk1x_dramclk0	PHY control.

ACPHYCTL6

ACPHYCTL6 is AC block PHY control register 6. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x188	ACPHYCTL6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	clk2x_cmd2t_ctl2	clk2x_mclk	clk2x_cmd1t	clk2x_cmd2t	clk2x_cmd2t_ctl	clk2x_dramclk1	clk2x_dramclk0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	clk2x_cmd2t_ctl2	PHY control.
[23:20]	RW	clk2x_mclk	PHY control.
[19:16]	RW	clk2x_cmd1t	PHY control.
[15:12]	RW	clk2x_cmd2t	PHY control.
[11:8]	RW	clk2x_cmd2t_ctl	PHY control.
[7:4]	RW	clk2x_dramclk1	PHY control.
[3:0]	RW	clk2x_dramclk0	PHY control.

ACPHYCTL7

ACPHYCTL7 is AC block PHY control register 7. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x018C	ACPHYCTL7	0x0080_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					halft_cmd2tctl2	halft_dramclk0	halft_dramclk1	halft_cmd1t	reserved	halft_cmd2tctl	ck5p_cmd2tc			reserved		ck3p_cmd1t				ck2p_dclk1				ck1p_dclk0				ck0p_mclk				ckd2_mclk			
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26]	RW	halft_cmd2tctl2	Set this field to default value.
[25]	RW	halft_dramclk0	Set this field to default value.
[24]	RW	halft_dramclk1	Set this field to default value.
[23]	RW	halft_cmd1t	Set this field to default value.
[22]	RO	reserved	Reserved.
[21]	RW	halft_cmd2tctl	Set this field to default value.
[20:18]	RW	ck5p_cmd2tc	Set this field to default value.
[17:15]	RO	reserved	Reserved.
[14:12]	RW	ck3p_cmd1t	Set this field to default value.
[11:9]	RW	ck2p_dclk1	Configure DRAM CK1 clock phase from PLL1 tap: 1/16 T
[8:6]	RW	ck1p_dclk0	Configure DRAM CK0 clock phase from PLL1 tap: 1/16 T
[5:3]	RW	ck0p_mclk	Set this field to default value.
[2:0]	RW	ckd2_mclk	Set this field to default value.

ACDEBUG

ACDEBUG is a PHY debugging register.

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Offset Address	Register Name	Total Reset Value
0x0190	ACDEBUG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5 4	3 2 1 0
Name	reserved			acdbg_config	reserved		DESKEW_regread	reserved	ac_rdcnt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:16]	RW	acdbg_config	Set this field to default value.
[15:9]	RO	reserved	Reserved.
[8]	RO	DESKEW_regread	Set this field to default value.
[7:3]	RO	reserved	Reserved.
[2:0]	RO	ac_rdcnt	Set this field to default value.

ACPHYRSVDC

ACPHYRSVDC is AC block PHY reserved control pin register 1. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x0194	ACPHYRSVDC	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ac_rsv_control							
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ac_rsv_control	Reserved.

ACPHYRSVDS

ACPHYRSVDS is AC block PHY reserved control pin register 2. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x0198	ACPHYRSVDS	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_rsv_status																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ac_rsv_status	Reserved.

ACPHYCTL8

ACPHYCTL8 is AC block PHY control register 8. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x019C	ACPHYCTL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ac_ck12p_reserve				ac_ck11p_reserve				ac_ck10p_reserve				ac_ck9p_reserve				ac_ck8p_reserve				ac_ck7p_reserve				ac_ck6p_reserve			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:18]	RW	ac_ck12p_reserve	Set this field to default value.
[17:15]	RW	ac_ck11p_reserve	Set this field to default value.
[14:12]	RW	ac_ck10p_reserve	Set this field to default value.
[11:9]	RW	ac_ck9p_reserve	Set this field to default value.
[8:6]	RW	ac_ck8p_reserve	Set this field to default value.
[5:3]	RW	ac_ck7p_reserve	Set this field to default value.
[2:0]	RW	ac_ck6p_reserve	Set this field to default value.

ACCMDBDL8

ACCMDBDL8 is AC command bit delay line configuration register 8.

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Offset Address	Register Name	Total Reset Value
0x1A0	ACCMDBDL8	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			odt1_bdl1	Reserved.			odt1_bdl0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt1_bdl1	Set this field to default value.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	odt1_bdl0	Set this field to default value.

ACCMDBDL9

ACCMDBDL9 is AC command bit delay line configuration register 9.

Offset Address	Register Name	Total Reset Value
0x1A4	ACCMDBDL9	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			odt1_bdl3	reserved			odt1_bdl2
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt1_bdl3	Set this field to default value.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	odt1_bdl2	Set this field to default value.

ACCMDBDL10

ACCMDBDL10 is AC command bit delay line configuration register 10.

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Offset Address	Register Name	Total Reset Value
0x1A8	ACCMDBDL10	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cs1_bdl1	reserved			cs1_bdl0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs1_bdl1	Set this field to default value.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs1_bdl0	Set this field to default value.

ACCMDBDL11

ACCMDBDL11 is AC command bit delay line configuration register 11.

Offset Address	Register Name	Total Reset Value
0x1AC	ACCMDBDL11	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cs1_bdl3	reserved			cs1_bdl2
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs1_bdl3	Set this field to default value.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs1_bdl2	Set this field to default value.

ACPHYDCC

ACPHYDCC is an AC block PHY DCC control register. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x01B0	ACPHYDCC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													acdcc_mclk			reserved	acdcc_dqs0			reserved	acdcc_dqs1			reserved	acdcc_dq0			reserved	acdcc_dq1		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18:16]	RW	acdcc_mclk	Set this field to default value.
[15]	RO	reserved	Reserved.
[14:12]	RW	acdcc_dqs0	Set this field to default value.
[11]	RO	reserved	Reserved.
[10:8]	RW	acdcc_dqs1	Set this field to default value.
[7]	RO	reserved	Reserved.
[6:4]	RW	acdcc_dq0	Set this field to default value.
[3]	RO	reserved	Reserved.
[2:0]	RW	acdcc_dq1	Set this field to default value.

ACPHYCTL9

ACPHYCTL9 is AC block PHY control register 9. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x01B4	ACPHYCTL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				actiming2t_odt1	actiming2t_cke1	actiming2t_cs1	acdram1sel_odt1	acdram1sel_cke1	acdram1sel_cs1	acposedge_odt1	acposedge_cke1	acposedge_cs1	acsdrsel_odt1	acsdrsel_cke1	acsdrsel_cs1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11]	RW	actiming2t_odt1	Set this field to default value.
[10]	RW	actiming2t_cke1	Set this field to default value.
[9]	RW	actiming2t_cs1	Set this field to default value.
[8]	RW	acdram1sel_odt1	Set this field to default value.
[7]	RW	acdram1sel_cke1	Set this field to default value.
[6]	RW	acdram1sel_cs1	Set this field to default value.
[5]	RW	acposedge_odt1	Set this field to default value.
[4]	RW	acposedge_cke1	Set this field to default value.
[3]	RW	acposedge_cs1	Set this field to default value.
[2]	RW	acsdrsel_odt1	Set this field to default value.
[1]	RW	acsdrsel_cke1	Set this field to default value.
[0]	RW	acsdrsel_cs1	Set this field to default value.

CATTIMER0

CATTIMER0 is a CA training timer 0 register.

Offset Address	Register Name	Total Reset Value
0x01C0	CATTIMER0	0x0B17_0B0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tcackeh				reserved				tcacd				reserved				tcaent				reserved				tcackel			
Reset	0	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:24]	RW	tcackeh	tCACKEH (dficlk cycle).
[23:22]	RO	reserved	Reserved.
[21:16]	RW	tcacd	tCACD (dficlk cycle).
[15:14]	RO	reserved	Reserved.
[13:8]	RW	tcaent	tCAENT (dficlk cycle).
[7:6]	RO	reserved	Reserved.
[5:0]	RW	tcackel	tCACKEL (dficlk cycle).

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CATTIMER1

CATTIMER1 is CA training timer 1 register.

Offset Address	Register Name	Total Reset Value
0x01C4	CATTIMER1	0x0000_040B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		tmrz						reserved				tcaext			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:8]	RW	tmrz	tMRZ (dficlk cycle).
[7:6]	RO	reserved	Reserved.
[5:0]	RW	tcaext	tCAEXT (dficlk cycle).

CATCONFIG

CATCONFIG is a CA training configuration register.

Offset Address	Register Name	Total Reset Value
0x01C8	CATCONFIG	0x0008_2606

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cat_en	sw_cat_dqvalid	sw_cat_cke_low	sw_cat_cke_high	sw_cat_strobe	sw_cat_mrw41	sw_cat_mrw48	sw_cat_mrw42	reserved			cat_openeye_en	cat_restore_en	cat_cat_phydq_sel	reserved		cat_rb_backtap				ca_samp_num_ph				reserved				ca_samp_num_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31]	RW	sw_cat_en	SW CA training enable. When this field is asserted, PACK will enter the SW CA training state. After the SW CA training is complete, this bit should be deasserted by firmware. 0: disabled (default) 1: enabled

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[30]	RW	sw_cat_dqvalid	SW CA training. This field indicates whether the CA result is ready. This bit is cleared when sw_cat_strobe is asserted. Then after the timing tCACD, this bit is asserted. 0: not valid 1: valid
[29]	RW	sw_cat_cke_low	SW CA training. This field is used to request the CKE to be low and it cleared by HW.
[28]	RW	sw_cat_cke_high	SW CA training. This field is used to request the CKE to be high and is cleared by HW.
[27]	RW	sw_cat_strobe	SW CA training. This field is used to issue the predefined SW CA pattern and is cleared by HW.
[26]	RW	sw_cat_mrw41	SW CA training. This field is used to issue the MRW41 command and is cleared by HW.
[25]	RW	sw_cat_mrw48	SW CA training. This field is used to issue the MRW48 command and is cleared by HW.
[24]	RW	sw_cat_mrw42	SW CA training. This field is used to issue the MRW42 command and is cleared by HW.
[23:21]	RO	reserved	Reserved.
[20]	RW	cat_openeye_en	HW CA training open eye enable. 0: disabled (default) 1: enabled
[19]	RW	cat_restore_en	HW CA training restore enable. If this field is set to high, the CA training will restore the CA phase before the second CA training (mapping stage) starts. This field is recommended to set to high. 0: disabled 1: enabled (default)
[18]	RW	cat_cat_phydq_sel	HW CA training PHY DQ CA result select. 0: LSB (default) 1: MSB
[17:16]	RO	reserved	Reserved.
[15:12]	RW	cat_rb_backtap	HW CA training right boundary back tap. This field is used to offset the addrph_a before the right boundary search is started to overcome meta-sable zone.
[11:8]	RW	ca_samp_num_ph	HW CA training sample count for CA phase. Value range: 1−15
[7:4]	RO	reserved	Reserved.
[3:0]	RW	ca_samp_num_bdl	HW CA training sample count for CA BDL. Value range: 1−15

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CATRESULT

CATRESULT is a CA training result register (for debugging).

Offset Address	Register Name	Total Reset Value
0x01CC	CATRESULT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						cat_reault									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RO	cat_reault	CA training. HW CA training result for each address bit during each HW CA training state. This field is meaningful only after the HW CA training is complete and is only for debugging. 0: Failed 1: OK

PHYDQRESULT

PHYDQRESULT is a SW CA training DQ result (from PHY) register.

Offset Address	Register Name	Total Reset Value
0x01D0	PHYDQRESULT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy_dq_result																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	phy_dq_result	SW CA training. SW CA training latched results from the DRAM device. For the LPDDR3 CA training, the meaningful bits are [15:0] (mapped to DQ[15:0]). PACK and PHY will not latch these bits, so these bits are those you obtained on DQ of the DRAM device.

ADDRPHBOUND

ADDRPHBOUND is a CA training address phase boundary register.

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Offset Address	Register Name	Total Reset Value
0x01D4	ADDRPHBOUND	0x0008_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	addrph_a_ori	reserved	addrph_a	reserved	addrph_a_left	reserved	addrph_a_right
Reset	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	addrph_a_ori	HW CA training. This field records the address phase before the HW CA training (for debugging).
[23:21]	RO	reserved	Reserved.
[20:16]	RW	addrph_a	HW CA training. This field records the left boundary of the address phase after the HW CA training (for debugging).
[15:13]	RO	reserved	Reserved.
[12:8]	RO	addrph_a_left	HW CA training. This field records the left boundary of the address phase after the HW CA training (for debugging).
[7:5]	RO	reserved	Reserved.
[4:0]	RO	addrph_a_right	HW CA training. This field records the right boundary of the address phase after the HW CA training (for debugging).

SWCATPATTERN_P

SWCATPATTERN_P is an SW CA training pattern register for the positive CK edge.

Offset Address	Register Name	Total Reset Value
0x01D8	SWCATPATTERN_P	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						sw_cat_pat_p	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	sw_cat_pat_p	SW CA training pattern for the positive CK edge. You can fill any pattern.

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SWCATPATTERN_N

SWCATPATTERN_N is an SW CA training pattern register for the negative CK edge.

Offset Address	Register Name	Total Reset Value
0x01DC	SWCATPATTERN_N	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						sw_cat_pat_n										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	sw_cat_pat_n	SW CA training pattern for the negative CK edge. You can fill any pattern.

LPCTRL

LPCTRL is a low-power control register.

Offset Address	Register Name	Total Reset Value
0x01E4	LPCTRL	0xFE80_8688

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcken_auto_en	gcken_dfi_main	gcken_dinit	gcken_dtrain	gcken_retrain	gcken_acbist	gcken_dxbist	t_wakeup_thrd_lv2				lp_cmdoen_disable	lp_ac_phy_clkgated_disable	lp_dx_phy_clkgated_disable	lp_dx_phy_phgated_disable	lp_pll_powerdown_disable	t_resp				t_wakeup_thrd_lv3				t_dram_clk_disable				t_dram_clk_enable			
Reset	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31]	RW	gcken_auto_en	Auto gated clock control enable. If this field is set to high, HW automatically/dynamically controls the PACK high-level clock gating. 0: off 1: on (default)

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[30]	RW	gcken_dfi_main	Manual gating control, main DFI clock gating switch. 0: clock off 1: clock on (default) When this field is set to low (clock off), some control registers that use the dfi_main clock are affected.
[29]	RW	gcken_dinit	Manual gating control, DRAM initialization clock gating. 0: clock off 1: clock on (default)
[28]	RW	gcken_dtrain	Manual gating control, data training clock gating. 0: clock off 1: clock on (default)
[27]	RW	gcken_retrain	Manual gating control, retraining clock gating. 0: clock off 1: clock on (default)
[26]	RW	gcken_acbist	Manual gating control, AC BIST clock gating. 0: clock off 1: clock on (default)
[25]	RW	gcken_dxbist	Manual gating control, data BIST clock gating. 0: clock off 1: clock on (default)
[24:21]	RW	t_wakeup_thrd_lv2	DFI low-power control interface timing threshold. ≥ wakeup_thrd_lv2: PHY clock gating, disable AC output enable ≥ wakeup_thrd_lv3: PHY clock gating, disable AC output enable, PHY PLL disable **NOTE** wakeup_thrd_lv3 should ≥ wakeup_thrd_lv2
[20]	RW	lp_cmdoen_disable	LP CMDOEN function disable when low-power assert. If this function is enabled, the I/O output of CA is floating to reduce I/O power. 0: LP-related function enabled (default) 1: LP-related function disabled
[19]	RW	lp_ac_phy_clkgated_disable	LP AC PHY clock gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[18]	RW	lp_dx_phy_clkgated_disable	LP DX PHY clock gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled

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[17]	RW	lp_dx_phy_phgated_disable	DX PHY clock phase gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[16]	RW	lp_pll_powerdown_disable	LP PLL disable function disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[15:12]	RW	t_resp	DFI low-power control interface timing parameter. The field value must be smaller than DFI tlp_resp.
[11:8]	RW	t_wakeup_thrd_lv3	DFI low-power control interface timing threshold. ≥ wakeup_thrd_lv2: PHY clock gating, disable AC output enable ≥ wakeup_thrd_lv3: PHY clock gating, disable AC output enable, PHY PLL power down Note: wakeup_thrd_lv3 should ≥ wakeup_thrd_lv2
[7:4]	RW	t_dram_clk_disable	DFI DRAM clock disable timing parameter. This field is used to count down before DRAM CK is disabled.
[3:0]	RW	t_dram_clk_enable	DFI DRAM clock enable timing parameter. This field is used to count down before DRAM CK is enabled.

DXNBISTCTRL

DXNBISTCTRL is a loopback data comparison control register during BIST of data blocks.

Offset Address	Register Name	Total Reset Value
0x200 + *n* x 0x80 (*n* = 0–3)	DXNBISTCTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	lfsr_seed		reserved		dqm_cmp_mask	dq_cmp_mask	reserved		bist_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RW	lfsr_seed	LFSR seed value. This field specifies the initial seed value of the LFSR generator to this byte lane.
[23:17]	RO	reserved	Reserved.

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[16]	RW	dqm_cmp_mask	DQM loopback compare mask. This field controls whether the comparison of the loopback data on DQM bits is disabled. 0: not compared 1: compared
[15:8]	RW	dq_cmp_mask	DQ loopback compare mask. This field controls whether the comparison of the loopback data on DQ bits is disabled. 0: not compared 1: compared
[7:1]	RO	reserved	Reserved.
[0]	RW	bist_en	BIST enable. This field specifies whether the data block is included for the loopback test while bist_op is set to BIST Enable.

DXNBISTSTS

DXNBISTSTS is a BIST test result and status register. Note that this register is read-only, and can be reset only by setting bist_op to BIST Reset.

Offset Address	Register Name	Total Reset Value
0x204 + *n* x 0x80 (*n* = 0–3)	DXNBISTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dqm_cmp_err	dq_cmp_ferr								dq_cmp_rerr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RO	dqm_cmp_err	BIST error on DQM.
[15:8]	RO	dq_cmp_ferr	BIST error on DQ at the falling edge of DQS.
[7:0]	RO	dq_cmp_rerr	BIST error on DQ at the rising edge of DQS

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DXNCTRL

DXNCTRL is a data block control register.

Offset Address	Register Name	Total Reset Value
0x208 + *n* x 0x80 (*n* = 0–3)	DXNCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dm_dis	bl_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	dm_dis	Data mask disable. This field specifies whether the corresponding write data mask (DM) is enabled. When this field is set to 1, the corresponding DM is not used and calibrated during training.
[0]	RW	bl_dis	Byte lane disable. This field specifies whether the corresponding byte lane is in use. If the corresponding byte lane is not used, the PLL/DDL is powered down, and the output driver is turned off.

DXNWDQNBDL0

DXNWDQNBDL0 is data block bit delay configuration register 0.

Offset Address	Register Name	Total Reset Value
0x210 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wdq3bdl				reserved				wdq2bdl				reserved				wdq1bdl				reserved				wdq0bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	wdq3bdl	Delay select of WDQ3. This field specifies the delay value of the bit delay line on the write path of DQ3.

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[23:21]	RO	reserved	Reserved.
[20:16]	RW	wdq2bdl	Delay select of WDQ2. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	wdq1bdl	Delay select of WDQ1. This field specifies the delay value of the bit delay line on the write path of DQ1.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	wdq0bdl	Delay select of WDQ0. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNWDQNBDL1

DXNWDQNBDL1 is data block bit delay configuration register 1.

Offset Address	Register Name	Total Reset Value
0x214 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	wdq7bdl	reserved	wdq6bdl	reserved	wdq5bdl	reserved	wdq4bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	wdq7bdl	Delay select of WDQ7. This field specifies the delay value of the bit delay line on the write path of DQ3.
[23:21]	RO	reserved	Reserved.
[20:16]	RW	wdq6bdl	Delay select of WDQ6. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	wdq5bdl	Delay select of WDQ5. This field specifies the delay value of the bit delay line on the write path of DQ1.

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[7:5]	RO	reserved	Reserved.
[4:0]	RW	wdq4bdl	Delay select of WDQ4. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNWDQNBDL2

DXNWDQNBDL2 is data block bit delay configuration register 2.

Offset Address	Register Name	Total Reset Value
0x218 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												wdmbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	wdmbdl	Delay select of WDQM. This field specifies the delay value of the bit delay line on DQM.

DXNRDQNBDL0

DXNRDQNBDL0 is data block bit delay configuration register 4.

Offset Address	Register Name	Total Reset Value
0x21C + *n* x 0x80 (*n* = 0–3)	DXNRDQNBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rdq3bdl				reserved				rdq2bdl				reserved				rdq1bdl				reserved				rdq0bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	rdq3bdl	Delay select of RDQ3. This field specifies the delay value of the bit delay line on the write path of DQ3.

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[23:21]	RO	reserved	Reserved.
[20:16]	RW	rdq2bdl	Delay select of RDQ2. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	rdq1bdl	Delay select of RDQ1. This field specifies the delay value of the bit delay line on the write path of DQ1.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	rdq0bdl	Delay select of RDQ0. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNRDQNBDL1

DXNRDQNBDL1 is data block bit delay configuration register 5.

Offset Address	Register Name	Total Reset Value
0x220 + *n* x 0x80 (*n* = 0−3)	DXNRDQNBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rdq7bdl				reserved				rdq6bdl				reserved				rdq5bdl				reserved				rdq4bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	rdq7bdl	Delay select of RDQ7. This field specifies the delay value of the bit delay line on the write path of DQ3.
[23:21]	RO	reserved	Reserved.
[20:16]	RW	rdq6bdl	Delay select of RDQ6. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	rdq5bdl	Delay select of RDQ5. This field specifies the delay value of the bit delay line on the write path of DQ1.

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[7:5]	RO	reserved	Reserved.
[4:0]	RW	rdq4bdl	Delay select of RDQ4. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNRDQNBDL2

DXNRDQNBDL2 is data block bit delay configuration register 6.

Offset Address	Register Name	Total Reset Value
0x224 + *n* x 0x80 (*n* = 0–3)	DXNRDQNBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rdmbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	rdmbdl	Delay select of RDQM. This field specifies the delay value of the bit delay line on loopback read path of DQM.

DXNRDQSDLY

DXNRDQSDLY is a local delay line control register.

Offset Address	Register Name	Total Reset Value
0x22C + *n* x 0x80 (*n* = 0–3)	DXNRDQSDLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rdqscyc								reserved												rdqsbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:16]	RW	rdqscyc	Read DQS clock phase select. This field specifies the number of taps in one clock cycle for the 1-T delay measurement type or the number of taps in half of clock cycle for the half-T delay measurement type. This field is used to create 90 degree delays for RDQS.

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[15:7]	RO	reserved	Reserved.
[6:0]	RW	rdqsbdl	Read DQS delay select. This field specifies the phase shift of the read DQS to create 90 degree delays.

DXNWDQSDLY

DXNWDQSDLY is a write leveling DQS delay control register.

Offset Address	Register Name	Total Reset Value
0x230 + *n* x 0x80 (*n* = 0–3)	DXNWDQSDLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wdqsphase				reserved				wdqsbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RW	wdqsphase	Write DQS clock phase select.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	wdqsbdl	Write leveling DQS delay select. This field specifies the delay value of delay applied on WDQS for write leveling.

DXNWDQDLY

DXNWDQDLY is a write leveling delay line control register.

Offset Address	Register Name	Total Reset Value
0x234 + *n* x 0x80 (*n* = 0–3)	DXNWDQDLY	0x0000_0C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wdqphase				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.

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[12:8]	RW	wdqphase	Write data eye clock phase select.
[7:0]	RO	reserved	Reserved.

DXNWLSL

DXNWLSL is an extra system latency addition control register.

Offset Address	Register Name	Total Reset Value
0x238 + *n* x 0x80 (*n* = 0–3)	DXNWLSL	0x0001_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														wlsl		reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17:16]	RW	wlsl	Write leveling system latency. This field is used to adjust the write latency after write leveling.
[15:0]	RO	reserved	Reserved.

DXNRDQSGDLY

DXNRDQSGDLY is a local delay line control register.

Offset Address	Register Name	Total Reset Value
0x23C + *n* x 0x80 + *m* x 0x400 (*n* = 0–3) (*m* = 0–1)	DXNRDQSGDLY	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				org_rdqsgph				reserved				rdqsgtxbdl				reserved				rdqsgphase				reserved				rdqsgbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.

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[29:24]	RO	org_rdqsgph	Original read DQS gate phase before HW gate training post-update stage (for debugging).
[23:21]	RO	reserved	Reserved.
[20:16]	RW	rdqsgtxbdl	Read DQS gate delay select. This field specifies the delay value of the read gating delay before DQS dummy PAD.
[15:14]	RO	reserved	Reserved.
[13:8]	RW	rdqsgphase	Read DQS gating clock phase select.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	rdqsgbdl	Read DQS gating delay select. This field specifies the delay value of the read gating delay after DQS dummy PAD.

DXPHYCTRL

DXPHYCTRL is a DX PHY control register.

Offset Address	Register Name	Total Reset Value
0x240 + *n* x 0x80 (*n* = 0–3)	DXPHYCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	dx_pll_cal	dx_pll_calm	dx_pll_calt	dx_pll_lt		dx_pll_sp		dx_pll_cpi				dx_pll_init	dx_pll_testen	dx_pll_testpem	dx_pll_thrm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RW	dx_pll_cal	The value 0x0 is recommended.
[13]	RW	dx_pll_calm	The value 0x0 is recommended.
[12]	RW	dx_pll_calt	The value 0x0 is recommended.
[11:10]	RW	dx_pll_lt	The value 0x0 is recommended.
[9:7]	RW	dx_pll_sp	The value 0x2 is recommended.
[6:4]	RW	dx_pll_cpi	The value 0x4 is recommended.

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[3]	RW	dx_pll_init	The value 0x0 is recommended.
[2]	RW	dx_pll_testen	The value 0x0 is recommended.
[1]	RW	dx_pll_testpem	The value 0x0 is recommended.
[0]	RW	dx_pll_thrm	The value 0x0 is recommended.

DXNGDS

DXNGDS is a latch enable register. It is used to control the latch enable within the PHY to obtain stable data.

Offset Address	Register Name	Total Reset Value
0x248 + *n* x 0x80 (*n* = 0–3)	DXNGDS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													gds		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	gds	Rank 0 read data latch delay. This field is used as a reference stable region for the PHY to latch the read data.

DXNCLKBDL

DXNCLKBDL is a data block clock bit delay line configuration register.

Offset Address	Register Name	Total Reset Value
0x24C + *n* x 0x80 (*n* = 0–3)	DXNCLKBDL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												dx_refclk_bdl				reserved												dx_fbclk_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	dx_refclk_bdl	Bit delay line of REFCLK.
[15:5]	RO	reserved	Reserved.

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[4:0]	RW	dx_fbclk_bdl	Bit delay line of FBCLK.

DXNRDBOUND

DXNRDBOUND is a read data eye boundary register. This register indicates the left and right boundaries of RDQSQDL of the data eye.

Offset Address	Register Name	Total Reset Value
0x250 + *n* x 0x80 (*n* = 0–3)	DXNRDBOUND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									rdqsbdl_left							reserved								rdqsbdl_right							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:16]	RO	rdqsbdl_left	Left boundary of read data eye.
[15:7]	RO	reserved	Reserved.
[6:0]	RO	rdqsbdl_right	Right boundary of read data eye.

DXNWRBOUND

DXNWRBOUND is a write data eye boundary register. This register indicates the left and right boundaries of WDQSQDL of the data eye.

Offset Address	Register Name	Total Reset Value
0x254 + *n* x 0x80 (*n* = 0–3)	DXNWRBOUND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wdqphase_left				reserved												wdqphase_right			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RO	wdqphase_left	Left boundary of the write data eye.
[15:5]	RO	reserved	Reserved.
[4:0]	RO	wdqphase_right	Right boundary of the write data eye.

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DXNOEBDL

DXNOEBDL is an output enable delay line control register. This register specifies the delay line value of the output enable delay line within the PHY data block.

Offset Address	Register Name	Total Reset Value
0x258 + *n* x 0x80 (*n* = 0–3)	DXNOEBDL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wdqsoe_bdl				reserved												oen_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	wdqsoe_bdl	Write DQS output enable delay control.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	oen_bdl	DQ output enable delay control.

DXNMISCCTRL0

DXNMISCCTRL0 is data block PHY miscellaneous control register 0. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x260 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL0	0x0002_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					ptrgated_en	enshift_a0	margin_a0	bufphyclkdiv2	lvdqclkdiv2	dqsgatedla	dx_rxp_2nd_dm	dx_rxn_2nd_dm	dx_dqs_h	dx_dqs_l	dx_margin_a1	rxp_2nd_dq								rxn_2nd_dq							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26]	RW	ptrgated_en	Set this field to default value.
[25]	RW	enshift_a0	Set this field to default value.

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[24]	RW	margin_a0	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[23]	RW	bufphyclkdiv2	Set this field to default value.
[22]	RW	lvdqclkdiv2	Set this field to default value.
[21]	RW	dqsgatedla	Set this field to default value.
[20]	RW	dx_rxp_2nd_dm	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[19]	RW	dx_rxn_2nd_dm	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[18]	RW	dx_dqs_h	Set this field to default value.
[17]	RW	dx_dqs_l	Set this field to default value.
[16]	RW	dx_margin_a1	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[15:8]	RW	rxp_2nd_dq	After this field is modified, "phyconn_rst" is required to update the latest setting. When the dly_track_type=1 tracking type is required, this field should be set to 0xFF before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[7:0]	RW	rxn_2nd_dq	After this field is modified, "phyconn_rst" is required to update the latest setting. When the dly_track_type=1 tracking type is required, this field should be set to 0xFF before initial trainings and dly_track_type should be set to 0x1 after initial trainings.

DXNMISCCTRL1

DXNMISCCTRL1 is data block PHY miscellaneous control register 1. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x264 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dqclk1x	dqclk2x	dqsgclk1x	dqsgclk2x	dqsclk1x	dqsclk2x	mclk1x	mclk2x
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dqclk1x	Set this field to default value.
[27:24]	RW	dqclk2x	Set this field to default value.
[23:20]	RW	dqsgclk1x	Set this field to default value.
[19:16]	RW	dqsgclk2x	Set this field to default value.
[15:12]	RW	dqsclk1x	Set this field to default value.
[11:8]	RW	dqsclk2x	Set this field to default value.
[7:4]	RW	mclk1x	Set this field to default value.
[3:0]	RW	mclk2x	Set this field to default value.

DXDEBUG0

DXDEBUG0 is data block PHY debug signal register 0.

Offset Address	Register Name	Total Reset Value
0x268 + *n* x 0x80 (*n* = 0–3)	DXDEBUG0	0x0000_5415

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15	14	13	12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					s0a	s0b	s1a	reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	0	1	0 1 0 0	0 0 0 1	0 1 0 1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RO	s0a	Set this field to default value.
[13]	RO	s0b	Set this field to default value.
[12]	RO	s1a	Set this field to default value.
[11:0]	RO	reserved	Reserved.

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DXDEBUG1

DXDEBUG1 is data block PHY debug signal register 1.

Offset Address	Register Name	Total Reset Value
0x26C + *n* x 0x80 (*n* = 0–3)	DXDEBUG1	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dqs0								dqs0b								dqs0_gold							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Debug signal. Note that the field may have unknown values in the simulation.
[23:0]	RO	dqs0	Reserved.
[15:8]	RO	dqs0b	Reserved.
[7:0]	RO	dqs0_gold	Reserved.

DXPHYRSVD

DXPHYRSVD is a data block PHY reserved control pin register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x270 + *n* x 0x80 (*n* = 0–3)	DXPHYRSVD	0x0000_FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dx_rsv_status																dx_rsv_control															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dx_rsv_status	Reserved.
[15:0]	RW	dx_rsv_control	Reserved. The followings are for (n = 0, 2): Bit 1 (reg_DQSG_extend_2T): 0/1: extend DQSG 1T/2T dfi_clk, when reg_DQSG_extend_en is 1 Bit 0 (reg_DQSG_extend_en): 0/1: disable/enable the DQSG extend function

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DXNMISCCTRL2

DXNMISCCTRL2 is data block PHY miscellaneous control register 2. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x274 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL2	0x0000_026F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					reg_OE_extend1T_en	reg_dqsg_TX_2path	reg_squeach_en	reg_dqsglat1T_en	reg_sel_halfT_gated_16b	reg_dynamic_PUPDEN_16b	reg_dummypad_use	reg_ODTEN_gated	reg_GDS_r1T_sel_16b	BUFRESETCONTN_gated_TDC	BUFRESETCONTN_gated_DQSGERROR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	reg_OE_extend1T_en	Set this field to default value.
[9]	RW	reg_dqsg_TX_2path	Set this field to default value.
[8]	RW	reg_squeach_en	Set this field to default value.
[7]	RW	reg_dqsglat1T_en	Set this field to default value.
[6]	RW	reg_sel_halfT_gated_16b	Set this field to default value.
[5]	RW	reg_dynamic_PUPDEN_16b	Set this field to default value.
[4]	RW	reg_dummypad_use	Set this field to default value.
[3]	RW	reg_ODTEN_gated	Set this field to default value.
[2]	RW	reg_GDS_r1T_sel_16b	Set this field to default value.
[1]	RW	BUFRESETCONTN_gated_TDC	Set this field to default value.

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[0]	RW	BUFRESETCONTN_gated_DQSGERROR	Set this field to default value.

DXDEBUGCONFIG

DXDEBUGCONFIG is a data block PHY debugging control register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x278 + *n* x 0x80 (*n* = 0–3)	DXDEBUGCONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											DESKEW_regread	reg_dbg_prepost_sel	reg_dbg_pllclk_sel	reg_dbg_REFFB_predly	reg_dbg_REFFB_postdly
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RO	DESKEW_regread	Reserved. registers for the future.
[3]	RW	reg_dbg_prepost_sel	Set this field to default value.
[2]	RW	reg_dbg_pllclk_sel	Set this field to default value.
[1]	RW	reg_dbg_REFFB_predly	Set this field to default value.
[0]	RW	reg_dbg_REFFB_postdly	Set this field to default value.

DXNDCC

DXNDCC is a data block PHY DCC control register. This register is used to control the PHY and should not be modified.

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Offset Address	Register Name	Total Reset Value
0x27C + *n* x 0x80 (*n* = 0–3)	DXNDCC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dxctl_mclk_dcc				dxctl_dqs_dcc				dxctl_dqsg_dcc				dxctl_dq_dcc			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:9]	RW	dxctl_mclk_dcc	bit[11]: dly_sel_xxx_DCC_16b bit[10]: ctrlC_xxx_DCC_16b bit[9]: ctrl2_xxx_DCC_16b
[8:6]	RW	dxctl_dqs_dcc	bit[8]: dly_sel_xxx_DCC_16b bit[7]: ctrlC_xxx_DCC_16b bit[6]: ctrl2_xxx_DCC_16b
[5:3]	RW	dxctl_dqsg_dcc	bit[5]: dly_sel_xxx_DCC_16b bit[4]: ctrlC_xxx_DCC_16b bit[3]: ctrl2_xxx_DCC_16b
[2:0]	RW	dxctl_dq_dcc	bit[2]: dly_sel_xxx_DCC_16b bit[1]: ctrlC_xxx_DCC_16b bit[0]: ctrl2_xxx_DCC_16b

4.2 SPI Flash Controller

4.2.1 Overview

The serial peripheral interface flash controller (SFC) is a SPI flash controller. The SFC provides an AHB slave interface on the service side to control access to the SPI flash through the AHB channel and provides an AHB master interface to read and write to the SPI flash in direct memory access (DMA) mode.

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Figure 4-8 SFC application block diagram

CAUTION

Because the SPI NAND flash and SPI NOR flash share a set of pins, the two types of flash memories cannot be used at the same time.

4.2.2 Features

4.2.2.1 AHB Slave Interface

The AHB slave interface has the following features:

- Provides an AHB slave interface to allow users to access an internal configuration register or the SPI flash memory based on the selected signal.
- Supports the advanced micro-controller bus architecture 2.0 (AMBA 2.0) protocol.
- Supports the little endian mode.

4.2.2.2 AHB Master Interface

The AHB master interface has the following features:

- Provides an AHB master interface for transferring data between the memory and flash memory in DMA mode.
- Supports the AMBA2.0 protocol.
- Supports only the little endian mode.
- Provides the transfer modes such as Single, INCR4, INCR8, and INCR16.
- Does not support early termination.
- Supports lock transfer.

4.2.2.3 Memory Interface

The memory interface has the following features:

- Supports two CSs. Supports a maximum of 128 Mbits (in 3-byte address mode) or 8 Gbits (in 4-byte address mode) storage space. In addition, the SPI flash can be mapped to the system address space. The mapping base address can be configured. The mapping system space must be within the space of 0x58000000–0x5BFFFFFF.

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- Supports address aliasing. Address 0 can be mapped to the CS1 by address aliasing after power-on to boot the chip from the CS1.
- Supports the standard SPI, dual input/dual-output SPI, quad-output/quad-input SPI, dual I/O SPI, quad-I/O SPI, full DIO SPI, and full QIO SPI. After power-on, the standard SPI is selected by default. You can change the interface type by configuring the corresponding registers.
- Supports two flash address modes: 3-byte address mode and 4-byte address mode. The 3-byte address mode supports a maximum capacity of 128 Mbits. The 4-byte address mode supports a maximum capacity of 8 Gbits.
- Supports read/write operations by means of bus, register programming, or DMA.
- Supports various write protection operations.

4.2.3 Function Description

4.2.3.1 Interface Mode Timing

Standard SPI

In standard SPI interface mode, a 1-bit data input line and a 1-bit data output line are supported. Figure 4-9 and Figure 4-10 show the timings of the standard SPI interface.

Figure 4-9 Timing of the standard SPI interface (write)

NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output in unit of a single bit in serial mode through the sfc_soi0 line.

Figure 4-10 Timing of the standard SPI interface (read)

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NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output in unit of a single bit in serial mode through the sfc_soi1 line.

Dual Input/Dual Output SPI

In dual input/dual output SPI mode, 2-bit bidirectional data lines are supported. Figure 4-11 shows the timing in dual input/dual output SPI mode.

Figure 4-11 Timing of the dual input/dual output SPI interface

NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output (write) and input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Dual I/O SPI

In dual I/O SPI interface mode, 2-bit bidirectional data lines are supported. Figure 4-12 shows the timing in dual I/O SPI interface mode.

Figure 4-12 Timing of the dual I/O SPI interface

NOTE

- The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of dual bits through the sfc_sio0 or sfc_soi1 line.
- The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

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Full Dual I/O SPI

In full dual I/O SPI mode, 2-bit bidirectional data lines are supported. Figure 4-13 shows the timing in full dual I/O SPI mode.

Figure 4-13 Timing of the full dual-I/O SPI interface

NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of dual bits through thesfc_sio0 or sfc_soi1 line.
- The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Quad Input/Quad Output SPI

In quad input/quad output SPI mode, 4-bit bidirectional data lines are used. Figure 4-14 shows the timing in quad input/quad output SPI mode.

Figure 4-14 Timing of the quad input/quad output SPI interface

NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

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Quad I/O SPI

In quad I/O SPI interface mode, 4-bit bidirectional data lines are used. Figure 4-15 shows the timing in quad I/O SPI interface mode.

Figure 4-15 Timing of the quad I/O SPI interface

NOTE

- The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, or sfc_wp, or sfc_hold line.
- The data bytes are output (write) or input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Full Quad SPI

In full quad SPI interface mode, 4-bit bidirectional data lines are supported. Figure 4-16 shows the timing in full quad SPI interface mode.

Figure 4-16 Timing of the full quad SPI interface

NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.
- The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

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4.2.3.2 Reading or Writing to the SPI Flash

The SPI flash can be read and written in the following ways:

- Send commands such as **SPI Flash Program** and **Read** based on register configurations to write to and read the SPI flash.

  This method requires the CPU to directly control the SPI flash commands and parameters to be sent.
- The CPU reads and writes to the SPI flash over the AHB slave interface in a similar way as the CPU reads and writes to a common memory.

  The SFC automatically maps the AHB bus read/write timing to an SPI flash read/write command.
- Data is transferred between the SPI flash and the memory in DMA mode.

4.2.3.3 Other Operations

Other operations on the SPI flash such as erase and device ID read can be implemented only by using registers.

4.2.3.4 Switching the Flash Address Mode

The SFC module supports 3-byte and 4-byte flash address modes. You can set the default address mode by pulling up or down the SFC_ADDR_MODE, and dynamically switch the address mode by configuring registers after the chip boots.
To set the default address mode when the chip boots, do as follows:

- Pull down the SFC_ADDR_MODE pin (multiplexed with the SFC_CLK pin) to set the default address mode to 3-byte address mode.
- Pull up the SFC_ADDR_MODE pin (multiplexed with the SFC_CLK pin) to set the default address mode to 4-byte address mode.

To switch the SPI flash address mode, perform the following steps:

Step 1 Before switching between flash address modes, ensure that the operations on the SPI flash are complete.

Step 2 Send specific commands to configure the SPI flash to enter the 4-byte mode by using registers based on SPI flash requirements.

Step 3 Set the SFC flash address mode to 4-byte (GLOBAL_CONFIG[flash_addr_mode]).

----End

For details about the commands for switching between SPI flash address modes, see the SPI flash manual.

4.2.3.5 Timing Description

Figure 4-17 describes timings and related parameters.

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Figure 4-17 SPI output timing

NOTE

- tcsh: CS setup time
- tcss: CS hold time
- tshsl: CS deselect time

4.2.4 Working Process

4.2.4.1 Initialization

The initialization is implemented as follows:

Step 1 Configure the timing register if the timing parameter needs to be configured.

Step 2 For details about the flash 4-bye address mode, see section 4.2.3.4 "Switching the Flash Address Mode."

Step 3 Configure the bus operation direction register.

1. Configure BUS_FLASH_SIZE based on the size of the flash memory. You can obtain the size by sending the **Read ID** command to the flash memory to get the device models.
2. Configure CS1_BUS_BASE_ADDR and BUS_ALIAS_ADDR based on the situation the flash memory is mapped to the system address space. The mapping address space must be within the address space that the system bus allocates to SFC_MEM.
3. For some devices, the Hi3516A needs to send special instructions before reading and writing devices (flash memory) in non-standard SPI timing mode.
4. Configure the instructions and parameters of the bus read and write operations.

   Configure BUS_CONFIG1 or BUS_CONFIG2.
5. Enable the bus write function if necessary. The bus write function is disabled by default.

   Configure BUS_CONFIG1[wr_enable] as 1.

NOTE

- The SPI flash does not need to be initialized for operations on the SPI flash by using registers. Registers must be reconfigured before each operation.
- This initialization process is only for reference. You are advised to adjust the initialization process based on device difference.

----End

4.2.4.2 Process of Reading the Flash Memory

Figure 4-18 shows the process of reading the flash memory by using related registers in query mode.

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Figure 4-18 Process of reading the flash memory by using related registers in query mode

4.2.4.3 Process of Writing to the Flash Memory

Figure 4-19 shows the process of writing to the flash memory by using related registers in interrupt mode.

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Figure 4-19 Process of writing to the flash memory by using related registers in interrupt mode

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4.2.4.4 Other Operations in Register Mode

Figure 4-20 Process of other operations

4.2.4.5 Process of Reading and Writing the Flash Memory Directly over the AHB Bus

After the SFC module is power-on reset, it is set to standard SPI timing mode by default. The flash memory can be directly read and written without additional configurations.

By default, writing to the flash memory over the AHB bus is forbidden. To enable the bus write operation, set BUS_CONFIG1[wr_enable] to 1.

For details about the read and write configuration of the bus, see section 4.2.4.1 "Initialization."

4.2.4.6 Process of Reading and Writing the Flash Memory in DMA Mode

The process of reading and writing the flash memory in DMA mode is as follows:

Step 1 If you need to adjust the timing configurations of the bus operation mode, see section 4.2.4.1 "Initialization."

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Step 2 Configure the memory start address, flash memory start address (flash memory offset address), and data length.

Step 3 Configure the read and write directions.

Step 4 Enabled the DMA operation (set BUS_DMA_CTRL [start] to 1).

Step 5 Wait for the dma_done interrupt or poll BUS_DMA_CTRL [start] until it is changed to 0.

NOTE

- The DMA operation and flash memory register command operation can be performed simultaneously.
- The flash memory can be directly accessed over the AHB slave interface during the DMA operation, but the configurations related to bus operation cannot be changed.

----End

4.2.5 Register Summary

Table 4-8 describes SFC registers.

Table 4-8 Summary of SFC registers (base address: 0x1001_0000)

Offset Address	Register	Description	Page
0x0100	GLOBAL_CONFIG	Global configuration register	4-203
0x0110	TIMING	Timing configuration register	4-204
0x0120	INT_RAW_STATUS	Interrupt raw status register	4-205
0x0124	INT_STATUS	Masked interrupt status register	4-205
0x0128	INT_MASK	Interrupt mask register	4-206
0x012C	INT_CLEAR	Interrupt clear register	4-207
0x01F8	VERSION	Version register	4-207
0x01FC	VERSION_SEL	Version selection register	4-208
0x0200	BUS_CONFIG1	Bus operation configuration register 1	4-208
0x0204	BUS_CONFIG2	Bus configuration register 2	4-210
0x0210	BUS_FLASH_SIZE	Bus operation mapping size register	4-210
0x0214	CS0_BUS_BASE_ADDR	CS0 bus mapping base address register	4-211
0x0218	CS1_BUS_BASE_ADDR	CS1 bus mapping base address register	4-211
0x021C	BUS_ALIAS_ADDR	Bus mapping alias mapping base address register	4-212
0x0240	BUS_DMA_CTRL	DMA operation control register	4-212

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Offset Address	Register	Description	Page
0x0244	BUS_DMA_MEM_SADDR	DMA DDR start address register	4-213
0x0248	BUS_DMA_FLASH_SADDR	DMA operation Flash start address register	4-213
0x024C	BUS_DMA_LEN	DMA operation transfer data length register	4-214
0x0250	BUS_DMA_AHB_CTRL	DMA operation AHB burst control register	4-214
0x0300	CMD_CONFIG	Command operation configuration register	4-215
0x0308	CMD_INS	Command operation instruction register	4-216
0x030C	CMD_ADDR	Command operation address register	4-217
0x0400 + 4 x *N*	CMD_DATABUF_N	Command operation data buffer register N (*N* = 0−15)	4-217

4.2.6 Register Description

GLOBAL_CONFIG

GLOBAL_CONFIG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0100	GLOBAL_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											reserved		flash_addr_mode	wp_en	mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:3]	RW	reserved	Reserved. This bit must be set to 0.

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[2]	RW	flash_addr_mode	SPI address mode 0: 3-byte address mode (default) 1: 4-byte address mode The write operation is invalid when CMD.start is 1.
[1]	RW	wp_en	Enable hardware write protection. The WP pin is forcibly pulled down when the bit is set to 1. 0: disabled 1: enabled
[0]	RW	mode	SPI mode configuration 0: mode 0 1: mode 3

TIMING

TIMNG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0110	TIMING	0x0000_660F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	tcsh			reserved	tcss			reserved				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	tcsh	Set the CS hold time 000–111: $n + 1$ clock cycles ($n = 0–7$)
[11]	RW	reserved	Reserved.
[10:8]	RW	tcss	Set the setup time of the CS. 000–111: $n + 1$ clock cycles ($n = 0–7$)
[7:4]	RO	reserved	Reserved
[3:0]	RW	tshsl	Indicates the deselect time of the CS. It is equal to the interval between two flash operations. 0000–1111: $n + 2$ clock cycles. ($n = 0–15$)

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INT_RAW_STATUS

INT_RAW_STATUS is an interrupt raw status register.

Offset Address	Register Name	Total Reset Value
0x0120	INT_RAW_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_raw_status	cmd_op_end_raw_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	dma_done_int_raw_status	Raw status of DMA operation done interrupt (not masked) 0: The operation is not complete. 1: The operation is complete.
[0]	RO	cmd_op_end_raw_status	Raw interrupt status of instruction operation end (not masked). 0: The operation is not complete. 1: The operation is complete.

INT_STATUS

INT_STATUS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0124	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_status	cmd_op_end_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.

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[1]	RO	dma_done_int_status	Raw status of DMA operation done interrupt (masked) 0: The operation is not complete. 1: The operation is complete.
[0]	RO	cmd_op_end_status	Interrupt status of instruction operation end (masked) 0: The operation is not complete. 1: The operation is complete.

INT_MASK

INT_MASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0128	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_mask	cmd_op_end_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	dma_done_int_mask	DMA operation done interrupt mask bit 0: masked 1: not masked
[0]	RW	cmd_op_end_int_mask	Instruction operation end interrupt mask bit 0: masked 1: not masked

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INT_CLEAR

INT_CLEAR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x012C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_clr	cmd_op_end_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	WO	dma_done_int_clr	DMA done interrupt clear bit. Writing 1 to this bit clears dma_done_status and dma_done_raw_status. 0: not cleared 1: cleared After a clear operation is complete, this bit returns 0 automatically.
[0]	WO	cmd_op_end_int_clr	Instruction operation end interrupt clear bit. Writing 1 to this bit clears cmd_op_end_status and cmd_op_end_raw_status. 0: not cleared 1: cleared After a clear operation is complete, this bit returns 0 automatically.

VERSION

VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x01F8	VERSION	0x0000_0350

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	VERSION	SFC version number

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VERSION_SEL

VERSION_SEL is a version selection register.

Offset Address	Register Name	Total Reset Value
0x01FC	VERSION_SEL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															version_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	version_sel	New and earlier version register group indication signal 0: earlier version register group 1: new version register group

BUS_CONFIG1

BUS_CONFIG1 is bus operation configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0200	BUS_CONFIG1	0x8080_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_enable	wr_enable	wr_ins						wr_dummy_bytes				wr_mem_if_type				rd_ins								rd_prefetch_cnt				rd_dummy_bytes			rd_mem_if_type
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	rd_enable	Bus read control. The value 0 is returned when the bus reads data. 0: disabled 1: enabled
[30]	RW	wr_enable	Bus write control. Ignore the bus write operation. 0: disabled 1: enabled

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[29:22]	RW	wr_ins	Write instruction
[21:19]	RW	wr_dummy_bytes	Dummy byte of the bus write operation 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[18:16]	RW	wr_mem_if_type	Bus write operation specifies the type of the connected SPI flash interface. 000: standard SPI interface type 001: dual-input/dual-output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-input/dual-output SPI 110: quad-I/O SPI 111: full QIO SPI
[15:8]	RW	rd_ins	Read instruction
[7:6]	RW	rd_prefetch_cnt	Clock cycle for prefetching data when the flash memory is accessed at a variable data length through the bus. 00: not prefetched (default) 01: prefetch the data in one clock cycle 10: prefetch the data in two clock cycles 11: prefetch the data in three clock cycles
[5:3]	RW	rd_dummy_bytes	Dummy byte of the bus read operation 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[2:0]	RW	rd_mem_if_type	Bus read operation specifies the type of the connected SPI flash interface. 000: standard SPI interface type 001: dual-Input/dual-output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-input/dual-output SPI 110: quad-I/O SPI 111: full QIO SPI

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BUS_CONFIG2

BUS_CONFIG2 is bus configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0204	BUS_CONFIG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	reserved	Reserved. The value 0 must be written to this bit.

BUS_FLASH_SIZE

BUS_FLASH_SIZE is a bus mapping size register.

Offset Address	Register Name	Total Reset Value
0x0210	BUS_FLASH_SIZE	0x0000_0909

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				flash_size_cs1				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RW	flash_size_cs1	Capacity of the SPI flash connected to CS1. 0000: 0000: No SPI flash is connected. 0001: 512 kbits 0010: 1 Mbit 0011: 2 Mbits 0100: 4 Mbits 0101: 8 Mbits 0110: 16 Mbits 0111: 32 Mbits 1000: 64 Mbits 1001: 128 Mbits (default) 1010: 256 Mbits

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			1011: 512 Mbits 1100: 1 Gbit 1101: 2 Gbits 1110: 4 Gbits 1111: 8 Gbits
[7:0]	RW	reserved	Reserved

CS0_BUS_BASE_ADDR

CS0 bus mapping base address register is a bus mapping base address register.

Offset Address	Register Name	Total Reset Value
0x0214	CS0_BUS_BASE_ADDR	0x5A00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cs0_bus_base_addr_high																reserved															
Reset	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cs0_bus_base_addr_high	The CS0 flash memory is mapped to the system space address.
[15:0]	RO	reserved	Reserved.

CS1_BUS_BASE_ADDR

CS1 bus mapping base address register is a bus mapping base address register.

Offset Address	Register Name	Total Reset Value
0x0218	CS1_BUS_BASE_ADDR	0x5800_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cs1_bus_base_addr_high																reserved															
Reset	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cs1_bus_base_addr_high	The CS1 flash memory is mapped to the system space address.
[15:0]	RO	reserved	Reserved.

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BUS_ALIAS_ADDR

BUS_ALIAS_ADDR is a bus alias base address register.

Offset Address	Register Name	Total Reset Value
0x021C	BUS_ALIAS_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flash_alias_addr																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	flash_alias_addr	The flash memory is mapped to the second base address of the system space.
[15:0]	RO	reserved	Reserved.

BUS_DMA_CTRL

BUS_DMA_CTRL is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x0240	BUS_DMA_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rw	start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	reserved	CS specified for the DMA operation. 0: CS0 1: CS1
[3:2]	RO	reserved	Reserved.
[1]	RW	rw	DMA read and write indication. 0: write operation (write data to the flash memory) 1: read operation (read data from the flash memory)

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[0]	RW	start	DMA transfer enable control 0: no operation or the operation is complete. 1: Writing 1 to this bit to enable the DMA operation. Read 1 from this bit indicates the DMA is operating. The value 0 is automatically returned after the DMA operation is complete.

BUS_DMA_MEM_SADDR

BUS_DMA_MEM_SADDR is DMA DDR start address register.

Offset Address	Register Name	Total Reset Value
0x0244	BUS_DMA_MEM_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr	DMA DDR start address. The start address must be 4-byte aligned.

BUS_DMA_FLASH_SADDR

BUS_DMA_MEM_SADDR is a DMA flash start address register.

Offset Address	Register Name	Total Reset Value
0x0248	BUS_DMA_FLASH_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_flash_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_flash_saddr	DMA flash start address.

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BUS_DMA_LEN

BUS_DMA_LEN is a DMA transfer data length register.

Offset Address	Register Name	Total Reset Value
0x024C	BUS_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dma_len																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29:0]	RW	dma_len	DMA data transfer length. The maximum value is 256 MB.

BUS_DMA_AHB_CTRL

BUS_DMA_AHB_CTRL is a DMA AHB burst control register.

Offset Address	Register Name	Total Reset Value
0x0250	BUS_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													incr16_en	incr8_en	incr4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved.
[2]	RW	incr16_en	INC16 burst type enable. 0: disabled 1: enabled
[1]	RW	incr8_en	INC8 burst type enable. 0: disabled. 1: enabled
[0]	RW	incr4_en	INC4 burst type enable. 0: disabled. 1: enabled

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CMD_CONFIG

CMD_CONFIG is a command configuration register.

Offset Address	Register Name	Total Reset Value
0x0300	CMD_CONFIG	0x0000_7E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mem_if_type			reserved	data_cnt							rw	data_en	dummy_byte_cnt				addr_en	reserved	start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:17]	RW	mem_if_type	Specifies the type of the SPI flash interface in register command operation mode. 000: standard SPI interface type 001: dual-Input/Dual-Output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-input/dual-output SPI 110: quad-I/O SPI 111: full QIO SPI
[16:15]	RW	reserved	Reserved. The value 0 must be written to this bit.
[14:9]	RW	data_cnt	The length of the read and written data is N+1 bytes.
[8]	RW	rw	Indicates that the data is read or written when that data_en is 1. 0: write. Data is written to the flash memory. 1: read. Data is read from the flash memory.
[7]	RW	data_en	Indicates whether there is data in this operation. 0: no data 1: there is data.
[6:4]	RW	dummy_byte_cnt	Dummy byte in register command operation mode. 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes

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[3]	RW	addr_en	Indicates whether there is an address for the current operation. 0: There is no address 1: There is an address.
[2]	RO	reserved	Reserved.
[1]	RW	reserved	CS select. 0: CS0 1: CS1
[0]	RW	start	Instruction operation start. 0: The operation is complete. 1: The operation starts. After the operation is complete, the bit returns 0 automatically.

CMD_INS

CMD_INS is a command instruction register.

Offset Address	Register Name	Total Reset Value
0x0308	CMD_INS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								REG_INS							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	REG_INS	Instruction code in the mode that the register accesses the flash memory.

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CMD_ADDR

CMD_ADDR is a command address register.

Offset Address	Register Name	Total Reset Value
0x030C	CMD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cmd_addr																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:0]	RW	cmd_addr	Operation address in the mode that the register accesses the flash memory.

CMD_DATABUF_N

CMD_DATABUF_N is a command data buffer register.

Offset Address	Register Name	Total Reset Value
0x0400 + 4xN (*N* = 0−15)	CMD_DATABUF_N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_databuf_n																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_databuf_n	Data buffer N in the mode that the register accesses the flash memory. Register offset address 0x400 + 4 x *N*. The variable *N* can be set to 0 to 15.

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4.3 NAND Flash Controller

4.3.1 Overview

The NANDC provides memory controller interfaces that connect to external NAND flash memories to store and access data.

4.3.2 Features

The NANDC has the following features:

- Provides a 9 KB (8192 bytes+1024 bytes) on-chip buffer for improving the read speed.
- Supports two CSs, two independent read_busy signals, and two external read_busy signals.
- Supports the CS don't care mode for reducing power consumption of the NAND flash.
- Supports bad block skipping and a maximum of 1 MB boot space.
- Supports boot without pin configuration. The component configuration information is automatically detected and adapted, including the page size, block size, and required ECC capability.
- Supports the low-power mode.
- Provides 8-bit data bus NAND flash interfaces.
- Allows the chip to boot from the NAND flash (with the page size of 2 KB, 4 KB, 8 KB, 16 KB) corresponding to CS0.
- Allows the ECC check and error correction to be enabled/disabled.
  - 8 bits/1 KB, 24 bits/1 KB BCH code ECC check and error correction for the NAND flash memory with the 2 KB or 4 KB page size
  - 24 bits/1 KB, 40 bits/1 KB, 64 bits/1 KB BCH code ECC check and error correction for the NAND flash memory with the 8 KB page size, 8 bits/1 KB ECC check and error correction for the 1 bit/512 bytes component
  - 40 bits/1 KB, 64 bits/1 KB BCH code ECC check and error correction for the NAND flash memory with the 16 KB page size
- Reports the read/write interrupt, erase interrupt, programming completion interrupt, and ECC check error interrupt.
- Supports read and write operations on data with variable length in ECC0 mode; write operations on the entire page in non-ECC0 mode; and direct memory access (DMA) read operations on only the out-of-band (OOB) or the entire page in non-ECC0 mode
- Flexibly configures the commands and addresses issued by the controller to support various NAND flash command operations (including cache read and write)
- Provides write protection for the NAND flash and allows write-protection addresses to be configured.
- Supports the lock and lock-down modes and allows the flash lock and flash global lock to be enabled and disabled. By default, the flash lock and flash global lock are disabled.
- Allows the randomizer function to be enabled for the NAND flash with the 8 KB, 16 KB page size.

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4.3.3 Function Description

4.3.3.1 Interface Block Diagram

Hi3516A provides two CSs and two ready/busy signals. Figure 4-21 shows the block diagram of NANDC interfaces.

Figure 4-21 Block diagram of NANDC interfaces

4.3.3.2 Function Implementation

Data in the NAND flash memory is stored by block and page. Each block consists of several pages. Before writing data to the NAND flash, you must erase the NAND flash by block, and then read/write to the NAND flash by page.

The commands for operating the NAND flash vary according to vendors. For details, see the appropriate NAND flash manuals.

Figure 4-22 shows the typical timing when the NANDC reads a page of data from the NAND flash.

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Figure 4-22 Typical timing when the NANDC reads a page of data from the NAND flash

A typical read operation is performed as follows:

Step 1 Send the read command **0x00** to the NAND flash.

Step 2 Send the read start address. The start address consists of the internal page address, page address, and block address. For details, see the appropriate NAND flash manuals.

Step 3 Send the read confirmation command **0x30**. The NAND flash pulls the RB signal low, indicating that the NAND flash is being read. About 25 μs later, the RB signal becomes high, indicating that data of the NAND flash has been prepared.

Step 4 Output the NF_RD_N signal, and obtain the NAND flash data by sampling at the rising edge of the NF_RD_N signal.

----End

Figure 4-23 shows the typical timing when the NANDC programs the NAND flash.

Figure 4-23 Typical timing when the NANDC programs the NAND flash

A typical program (write) operation is performed as follows:

Step 1 Send the programming command **0x80** to the NAND flash.

Step 2 Send the start address from which data is written. The start address consists of the internal page address, page address, and block address. For details, see the appropriate NAND flash manuals.

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Step 3 Write data to the internal buffer of the NAND flash.

Step 4 Send the program confirmation command **0x10**. The NAND flash pulls the RB signal low, indicating that the NAND flash is being programmed. About 200 ms later, the RB signal becomes high, indicating that the program operation is complete.

Step 5 Send the command **0x70** to read the NAND flash status to check whether the program operation is successful.

----End

4.3.4 Operating Modes

Boot Mode

- The NANDC is in boot mode by default. The system can boot from only the NAND flash corresponding to CS0, even when the randomizer is enabled.
- In boot mode, the CPU can directly read data stored in a 1 MB address space in loop mode.
- When the NANDC boots from the NAND flash, the NANDC automatically sends a command to read the corresponding page of the NAND flash based on the addresses read by the CPU and then returns the corresponding data.
- In boot mode, the CPU cannot write data to the internal buffer of the NAND flash.
- In boot mode, bad blocks can be automatically identified and skipped. If seven consecutive bad blocks are identified, the boot fails.
- In the boot mode which is automatically configured based on the type of the connected component, ECC8 2 KB/4 KB, ECC24 2 KB/4 KB/8 KB, ECC40 8 KB/16 KB, and ECC64 8 KB/16 KB are supported. ECC24/ECC40 8 KB supports the boot modes when the randomizer is enabled or disabled. The randomizer is disabled in ECC 2 KB/4 KB but enabled in other modes by default.
- The boot mode supports the following flash specifications:
  - 8 bits/1 KB ECC, 2 KB page size
  - 24 bits/1 KB ECC, 2 KB page size
  - 8 bits/1 KB ECC, 4 KB page size
  - 24 bits/1 KB ECC, 4 KB page size
  - 24 bits/1 KB ECC, 8 KB page size
  - 40 bits/1 KB ECC, 8 KB page size
  - 40 bits/1 KB ECC, 16 KB page size
  - 64 bits/1 KB ECC, 16 KB page size
  - 64 bits/1 KB ECC, 8 KB page size

Normal Mode

The NANDC is switched to the normal mode when NFC_CON[op_mode] is set to 1. In this mode, the CPU can erase, program, and read the NAND flash.

NAND Flash Address Configuration

The NANDC does not translate addresses. It directly sends the values of low and high address registers to the NAND flash according to the number of addresses configured in the command

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configuration register. Therefore, the software needs to translate the address for the CPU into the address for the NAND flash and then write the translated address to the address register. For details about the address configuration requirements for each flash memory, see the user manual of the corresponding NAND flash.

Table 4-9 lists the requirements for setting the addresses for the Samsung K9F2G08U0M memory. Its capacity is 256 MB x 8 bits and its page size is 2 KB. A0 to A11 indicate the internal page addresses (column addresses) and A12 to A27 indicate the page addresses (row addresses).

Table 4-9 Addresses for the K9F2G08U0M

Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd cycle	A8	A9	A10	A11	0	0	0	0
3rd cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 4-10 lists the requirements for setting the addresses for the Samsung K9GAG08X0M memory. Its capacity is 2 GB x 8 bits and its page size is 4 KB. A0 to A12 indicate the internal page addresses (column addresses) and A13 to A31 indicate the page addresses (row addresses).

Table 4-10 Addresses for the K9GAG08X0M

Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd cycle	A8	A9	A10	A11	A12	0	0	0
3rd cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th cycle	A29	A30	A31	0	0	0	0	0

Address Mapping

In normal mode, NANDC address mapping is as follows:

- The base address for the internal buffer of the NANDC is 0x5000_0000.
- The base address for the internal register area of the NANDC is 0x1000_0000.

Operation Commands

The NAND flash manufacturers may provide certain advanced commands. Table 4-11 shows the common commands for operating the NAND flash.

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Table 4-11 Common commands for operating NAND flash memories

Operation	1st Cycle	2nd Cycle	Remarks
Read	00H	30H	None
Program	80H	10H	None
Block erase	60H	D0H	None
Read ID	90H	None	None
Read status	70H	None	None
Reset	FFH	None	None

4.3.5 Data Storage Structure

The size of the NANDC internal buffer is (8192 +1024) bytes. This section describes the storage structures of the data read from or written to the NAND flash in the NANDC buffer.

4.3.5.1 Non-ECC Mode

When the NANDC does not need to perform the ECC:

- The NANDC transparently writes the data in buffers to the NAND flash without processing.
- The NANDC writes data read from the NAND flash to the internal buffers without processing.
- The number of bytes of the read and written data is set by the NFC_DATA_NUM register. The NAND flash with the 2 KB, 4 KB, 8 KB, 16 KB page size is supported.
- The non-ECC mode is used when the read ID, set feature, and get feature operations are performed.

4.3.5.2 8-Bit/1024 ECC Mode

2 KB Page Size

Figure 4-24 shows the data structure of the driver in 8-bit ECC mode (2 KB page size).

Figure 4-24 Data structure of the driver in 8-bit ECC mode (2 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

Figure 4-25 shows the data structure of the data written to the NAND flash. The software valid data is divided into two 1040-byte data segments, and the ECC is calculated for each data segment. When being written to the NAND flash, the data is automatically stored in two groups in the alternate form of 1040-byte data+14-byte ECC code. The BB information is stored in the first two bytes of the NAND flash spare area.

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Figure 4-25 Data structure of the NAND flash in 8-bit ECC mode (2 KB page size)

4 KB Page Size

Figure 4-26 shows the data structure of the driver in 8-bit ECC mode (4 KB page size).

Figure 4-26 Data structure of the driver in 8-bit ECC mode (4 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

Figure 4-27 shows the data structure of the data written to the NAND flash. The software valid data is divided into four 1032-byte data segments, and the ECC is calculated for each data segment.

Data written to the NAND flash is automatically stored in three segments in the alternate form of 1032-byte data+14-byte ECC code. For the last data segment (1032-byte data+14-byte ECC code), the bad block flag is inserted in byte 4096 of the NAND flash.

Figure 4-27 Data structure of the NAND flash in 8-bit ECC mode (4 KB page size)

4.3.5.3 24-Bit ECC Mode

2 KB Page Size

Figure 4-28 shows the data structure of the driver in 24-bit ECC mode (2 KB page size).

Figure 4-28 Data structure of the driver in 24-bit ECC mode (2 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

Figure 4-29 shows the data structure of the data written to the NAND flash. The BB is inserted in byte 2048 of the NAND flash.

Figure 4-29 Data structure of the NAND flash in 24-bit ECC mode (2 KB page size)

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4 KB Page Size

Figure 4-30 shows the data structure of the driver in 24-bit ECC mode (4 KB page size).

Figure 4-30 Data structure of the driver in 24-bit ECC mode (4 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into four 1024 bytes+8 bytes data segments, and a 42-byte ECC is calculated for each data segment.

When being written to the NAND flash, the data and ECC code in the first three data segments are stored in alternate form. For the last data segment (1024 bytes+8 bytes+42 bytes), the bad block flag is inserted in byte 4096 of the NAND flash.

Figure 4-31 Data structure of the NAND flash in 24-bit ECC mode (4 KB page size)

8 KB Page Size

Figure 4-32 shows the data structure of the driver in 24-bit ECC mode (8 KB page size).

Figure 4-32 Data structure of the driver in 24-bit ECC mode (8 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into eight 1024 bytes+4 bytes data segments, and a 42-byte ECC is calculated for each data segment. When being written to the NAND flash, the first seven data segments and ECC codes are stored in alternate form. For the last data segment (1024 bytes+4 bytes+42 bytes), the bad block flag is inserted in byte 8192 of the NAND flash.

Figure 4-33 Data structure of the NAND flash in 24-bit ECC mode (8 KB page size)

4.3.5.4 40-Bit/1024 ECC Mode

8 KB Page Size

Figure 4-34 shows the data structure of the driver in 40-bit ECC mode (8 KB page size).

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Figure 4-34 Data structure of the driver in 40-bit ECC mode (8 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into eight 1024 bytes+4 bytes data segments, and a 70-byte ECC is calculated for each data segment. When being written to the NAND flash, the first seven data segments and ECC codes are stored in alternate form. For the last data segment (1024 bytes+4 bytes+70 bytes), the bad block flag is inserted in byte 8192 of the NAND flash.

Figure 4-35 Data structure of the NAND flash in 40-bit ECC mode (8 KB page size)

16 KB Page Size

Figure 4-36 shows the data structure of the driver in 40-bit ECC mode (16 KB page size).

Figure 4-36 Data structure of the driver in 40-bit ECC mode (16 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into sixteen 1024 bytes+2 bytes data segments, and a 70-byte ECC is calculated for each data segment. When being written to the NAND flash, the first seven data segments and ECC codes are stored in alternate form. For the last data segment (1024 bytes+2 bytes+70 bytes), the bad block flag is inserted in byte 16384 of the NAND flash.

Figure 4-37 Data structure of the NAND flash in 40-bit ECC mode (16 KB page size)

Two NANDC operations are required to write to each page. Write the 8192 bytes+16 bytes valid data to the start position of address 0 in the NANDC buffer, and then start the write-only

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mode of the NANDC. The ECC code generated by the NANDC for each operation is stored in the start position of the 8192 bytes+128 bytes in the internal buffer.

Reading each page also requires two NANDC operations, which are similar to writing to the page.

4.3.5.5 64-Bit/1024 ECC Mode

8 KB Page Size

Figure 4-38 shows the data structure of the driver in 64-bit ECC mode (8 KB page size).

Figure 4-38 Data structure of the driver in 64-bit ECC mode (8 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into eight 1024 bytes+4 bytes data segments, and a 112-byte ECC is calculated for each data segment. When being written to the NAND flash, the first seven data segments and ECC codes are stored in alternate form. For the last data segment (1024 bytes+4 bytes+112 bytes), the bad block flag is inserted in byte 8192 of the NAND flash.

Figure 4-39 Data structure of the NAND flash in 64-bit ECC mode (8 KB page size)

16 KB Page Size

Figure 4-40 shows the data structure of the driver in 64-bit ECC mode (16 KB page size).

Figure 4-40 Data structure of the driver in 64-bit ECC mode (16 KB page size)

BB: bad block, 2 bytes CTRL: control area for software, 30 bytes

The software valid data is divided into sixteen 1024 bytes+2 bytes data segments, and a 112-byte ECC is calculated for each data segment. When being written to the NAND flash, the first 14 data segments and ECC codes are stored in alternate form. For the fifteenth data segment (1024 bytes+2 bytes+112 bytes), the bad block flag is inserted in byte 16384 of the NAND flash.

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Figure 4-41 Data structure of the NAND flash in 64-bit ECC mode (16 KB page size)

Two NANDC operations are required to write to each page. Write the 8192 bytes+16 bytes valid data to the start position of address 0 in the NANDC buffer, and then start the write-only mode of the NANDC. The ECC code generated by the NANDC for each operation is stored in the start position of the 8192 bytes+128 bytes in the internal buffer.

Reading each page also requires two NANDC operations, which are similar to writing to the page.

4.3.6 ECC Mode Selection

The ECC IP used by the controller processes data based on 1 KB data block. Therefore, the ECC performance of the controller is described in the format of *n* bits/1 KB, for example, 8 bits/1 KB or 24 bits/1 KB. To ensure component reliability, the recommended ECC performance of 1 bit/512 bytes, 4 bits/512 bytes, or 8 bits/512 bytes is provided in the component data sheet. The ECC performance of 8 bits/1 KB is equivalent to that of 4 bits/512 bytes. When you select the ECC mode for the controller, note the following:

- The priority of the ECC performance of the controller is higher than or equal to that of the recommended ECC performance.

  For example, if the recommended ECC performance is 1 bit/512 bytes or 4 bits/512 bytes, the controller can select the ECC mode with the performance of 8 bits/1 KB.
- The component page size must be greater than or equal to the required storage size of the ECC mode for the controller.

  For example, if the component page size is (2 KB + 64 bytes), the controller cannot select the ECC mode with the performance of 24 bits/1 KB because the required storage size of this ECC mode is (2 KB + 116 bytes). For details about the required storage size for the ECC mode, see section 4.3.5 "Data Storage Structure."

4.3.7 Software Operations

4.3.7.1 Initializing the NAND Flash

The NAND flash is initialized as follows:

Step 1 Write 1 to NFC_CON[op_mode] to enter the normal mode, set NFC_CON[bus_width] and NFC_CON[page_size] based on the page size and bit width of the interconnected flash memory, and set NFC_CON[ecc_type] to configure the check and error correction modes.

Step 2 Set NFC_PWIDTH based on the timing requirements for the connected memory.

Step 3 In query mode, set the interrupt enable register NFC_INTEN to mask all interrupts; in interrupt mode, enable only the op_done interrupt and mask other interrupts.

----End

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4.3.7.2 Erasing the NAND Flash

The NAND flash is erased as follows:

Step 1 Write the address of the block to be erased in NFC_ADDRL and the erase command 0x0070_D060 in NFC_CMD.

Step 2 Write 0x66d to NFC_OP to enable the NANDC to erase the NAND flash. (Assume that the NAND flash needs three addresses and the operation is performed on the first NAND flash.)

Step 3 In query mode, check whether NFC_STATUS[nfc_ready] is 1. If yes, go to step 4. If no, continue the query. In interrupt mode, check whether NFC_INTS[op_done] is 1. If yes, go to step 4.

Step 4 Read NFC_STATUS[nf_status] to check whether the erase operation is successful.

----End

4.3.7.3 Writing to the NAND Flash in DMA Mode

- Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the interconnected flash memory.
- Configure the base addresses for storing data in the DDR by setting NFC_BADDR_D0, NFC_BADDR_D1, NFC_BADDR_D2, NFC_BADDR_D3, and NFC_BADDR_OOB. Each base address stores 4 KB data (4-KB-aligned).
  - Set the base address register NFC_BADDR_D0 for the NAND flash with the page size of 2 KB.
  - Set the base address register NFC_BADDR_D0 for the NAND flash with the page size of 4 KB.
  - Set the base addresses registers NFC_BADDR_D0 and NFC_BADDR_D1 for the NAND flash with the page size of 8 KB. Each base address stores 4 KB data.
  - Set the base address registers NFC_BADDR_D0, NFC_BADDR_D1, NFC_BADDR_D2, and NFC_BADDR_D3 for the NAND flash with the page size of 16 KB. Each base address stores 4 KB data.
  - Set the base address register NFC_BADDR_OOB that specifies the storage address for the OOB data in the DDR for the NAND flash memory with the page size of 2 KB, 4 KB, 8 KB, or 16 KB.
  - In ECC0 mode, configure NFC_DMA_LEN[len_oob] to set the size of the OOB area.
- Set NFC_DMA_CTRL to 0x73 to enable the NANDC to write to the NAND flash.
- The CPU waits until the NANDC sends the DMA transfer completion interrupt or queries NFC_DMA_CTRL[dma_start] until it is 0.

4.3.7.4 Reading the NAND Flash in DMA Mode

- Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the interconnected flash memory.
- Configure the base addresses for storing data in the DDR by setting NFC_BADDR_D0, NFC_BADDR_D1, NFC_BADDR_D2, NFC_BADDR_D3, and NFC_BADDR_OOB. Each base address stores 4 KB data (4-KB-aligned).
  - Set the base address register NFC_BADDR_D0 for the NAND flash with the page size of 2 KB.

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  - Set the base address register NFC_BADDR_D0 for the NAND flash with the page size of 4 KB.
  - Set the base addresses registers NFC_BADDR_D0 and NFC_BADDR_D1 for the NAND flash with the page size of 8 KB. Each base address stores 4 KB data.
  - Set the base address registers NFC_BADDR_D0, NFC_BADDR_D1, NFC_BADDR_D2, and NFC_BADDR_D3 for the NAND flash with the page size of 16 KB. Each base address stores 4 KB data.
- Set the base address register NFC_BADDR_OOB that specifies the storage address for the OOB data in the DDR for the NAND flash memory with the page size of 2 KB, 4 KB, 8 KB, or 16 KB.
- Set NFC_DMA_CTRL to 0x71 to enable the NANDC to read the NAND flash.
- If only the OOB is read in DMA mode, set NFC_DMA_CTRL to 0x1071 to enable the NANDC to read the NAND flash.
- The CPU waits until the NANDC sends the DMA transfer completion interrupt or queries NFC_DMA_CTRL[dma_start] until it is 0.

4.3.8 Notes

Note the following:

- Reset the MLC NAND flash memory before using based on memory manuals.
- The operation commands supported by the NAND flash memories vary according to vendors. Therefore, the command register NFC_CMD must be properly configured based on memory manuals. In addition, the number of address cycles required by the NAND flash memories vary according to the NAND flash capacity. You need to configure the address_cycles field of NFC_OP based on memory manuals. Furthermore, the supported timings vary according to memories. Hence, the read/write pulse width register NFC_PWIDTH and operation interval register NFC_OPIDLE must be properly configured according to memory manuals.
- After configuring related registers and buffers, write the NFC_OP register to enable the NANDC to read and write to the NAND flash memory. After that, do not write to relevant registers; otherwise, the NANDC or NAND flash memory may be abnormal.
- After starting to read or write the NAND flash by writing to NFC_OP, do not read or write to the buffer of the NANDC when NFC_STATUS[nfc_ready] is 0. Otherwise, error data may be returned.

4.3.9 Register Summary

Table 4-12 lists NANDC registers.

Table 4-12 Summary of NANDC registers (base address: 0x1000_0000)

Offset Address	Register Name	Description	Page
0x0000	NFC_CON	NANDC configuration register	4-233
0x0004	NFC_PWIDTH	Read/Write pulse width configuration register	4-234
0x0008	NFC_OPIDLE	Operation interval configuration register	4-235
0x000C	NFC_CMD	Command word configuration register	4-235

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Offset Address	Register Name	Description	Page
0x0010	NFC_ADDRL	Lower-bit address configuration register	4-236
0x0014	NFC_ADDRH	High address configuration register	4-236
0x0018	NFC_DATA_NUM	Read/Written data count configuration register	4-237
0x001C	NFC_OP	Operation register	4-237
0x0020	NFC_STATUS	Status register	4-238
0x0024	NFC_INTEN	Interrupt enable register	4-239
0x0028	NFC_INTS	Interrupt status register	4-241
0x002C	NFC_INTCLR	Interrupt clear register	4-243
0x0030	NFC_LOCK	Lock address configuration register	4-243
0x0034	NFC_LOCK_SA0	Lock start address 0 configuration register	4-244
0x0038	NFC_LOCK_SA1	Lock start address 1 configuration register	4-245
0x003C	NFC_LOCK_SA2	Lock start address 2 configuration register	4-245
0x0040	NFC_LOCK_SA3	Lock start address 3 configuration register	4-246
0x0044	NFC_LOCK_EA0	Lock end address 0 configuration register	4-246
0x0048	NFC_LOCK_EA1	Lock end address 1 configuration register	4-247
0x004C	NFC_LOCK_EA2	Lock end address 2 configuration register	4-248
0x0050	NFC_LOCK_EA3	Lock end address 3 configuration register	4-248
0x0054	NFC_EXPCMD	Extended page command register	4-249
0x0058	NFC_EXBCMD	Extended block command register	4-249
0x005C	NFC_ECC_TEST	ECC test register	4-249
0x0060	NFC_DMA_CTRL	DMA control register	4-251
0x0064	NFC_BADDR_D0	Base address register for the data transfer area	4-252
0x0068	NFC_BADDR_OOB	Base address register for the OOB transfer area	4-253
0x006C	NFC_DMA_LEN	Transfer length register	4-253

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Offset Address	Register Name	Description	Page
0x0070	NFC_OP_PARA	Operation parameter register	4-254
0x0074	NFC_VERSION	NANDC version register	4-254
0x0084	NFC_SEGMENT_ID	Data segment ID register for reading/writing to the NAND flash in DMA mode	4-255
0x0090	NFC_FIFO_EMPTY	Internal FIFO status register	4-256
0x0094	NFC_BOOT_SET	Boot parameter configuration register	4-256
0x009C	NF_LP_CTRL	NANDC low-power control register	4-257
0x00A0	NFC_ERR_NUM0_BUF0	NAND flash error bit count register 0 for the first buffer operation	4-257
0x00A4	NFC_ERR_NUM1_BUF0	NAND flash error bit count register 1 for the first buffer operation	4-258
0x00A8	NFC_ERR_NUM0_BUF1	NAND flash error bit count register 0 for the second buffer operation	4-258
0x00AC	NFC_ERR_NUM1_BUF1	NAND flash error bit count register 1 for the second buffer operation	4-258
0x00B0	NF_RB_MODE	NAND flash ready_busy mode register	4-259
0x00B4	NFC_BASE_ADDR_D1	Base address register 1 for the data area of the DDR to be read or written	4-259
0x00B8	NFC_BASE_ADDR_D2	Base address register 2 for the data area of the DDR to be read or written	4-260
0x00BC	NFC_BASE_ADDR_D3	Base address register 3 for the data area of the DDR to be read or written	4-260
0x00CC	NFC_MEM_CTRL	Instantiated memory management register	4-261

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4.3.10 Register Description

NFC_CON

NFC_CON is a NANDC configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	NFC_CON	0x0000_4886

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	randomizer_en	reserved		ecc_type				rb_sel	cs_ctrl	reserved		bus_width	page_size		op_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	randomizer_en	Randomizer enable 0: disabled 1: enabled
[13]	RO	reserved	Reserved
[12:9]	RW	ecc_type	ECC mode 0000: non-ECC 0001: reserved 0010: 8bit 0100: 24bits 0101: 40bits 0110: 64bits Others: reserved
[8]	RW	rb_sel	Ready/busy signal select. It is valid when multiple external NAND flash memories (multiple CSs) are connected. 0: The NAND flash memories share a ready/busy signal. 1: The NAND flash memory each has its own ready/busy signal. When only one NAND flash is connected, only cs0 and ready_busy 0 are used.
[7]	RW	cs_ctrl	CS control 0: When the NAND flash is busy, the CS signal is fixed at 0. 1: When the NAND flash is busy, the CS signal is set to 1. This mode maps to the "cs don't care" mode of the NAND flash.

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[6:5]	RO	reserved	Reserved
[4]	RW	bus_width	Data line width of the NAND flash 0: 8 bits 1: reserved
[3:1]	RW	page_size	Page size of the NAND flash 000: reserved 001: 2 KB 010: 4 KB 011: 8 KB 100: 16 KB 101~111: reserved
[0]	RW	op_mode	Operating mode of the NANDC 0: boot mode 1: normal mode

NFC_PWIDTH

NFC_PWIDTH is a read/write pulse width configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	NFC_PWIDTH	0x0000_0222

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rw_hcnt				r_lcnt				w_lcnt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	rw_hcnt	High-level width of the read/write signal of the NAND flash 0x1–0xF: 2 to 16 clock cycles
[7:4]	RW	r_lcnt	Low-level width of the read signal of the NAND flash 0x2–0xF: 3 to 16 clock cycles
[3:0]	RW	w_lcnt	Low-level width of the write signal of the NAND flash 0x1–0xF: 2 to 16 clock cycles

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NFC_OPIDLE

NFC_OPIDLE is an operation interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	NFC_OPIDLE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								frb_wait				cmd1_wait				addr_wait				reserved				cmd2_wait				wait_ready_wait			
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	frb_wait	Several delay cycles later after a read/write command is sent, the ready signal is detected to check whether it becomes high. Number of delay cycles = frb_wait x 8
[19:16]	RW	cmd1_wait	Number of wait cycles after command 1 is sent 0000–1111: 1 to 16 clock cycles
[15:12]	RW	addr_wait	Number of wait cycles after addresses are sent 0000–1111: configured values Number of delay cycles = addr_wait x 8
[11:8]	RO	reserved	Reserved
[7:4]	RW	cmd2_wait	Number of wait cycles after command 2 is sent 0000–1111: 1 to 16 clock cycles
[3:0]	RW	wait_ready_wait	When a number of cycles are delayed after the ready signal of the NAND flash becomes high, a read signal is sent to read data. Number of delay cycles = frb_idle x 8

NFC_CMD

NFC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	NFC_CMD	0x0070_3000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								read_status_cmd								cmd2								cmd1							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

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[23:16]	RW	read_status_cmd	Read status command word
[15:8]	RW	cmd2	Second command sent to the NAND flash by the NANDC
[7:0]	RW	cmd1	First command sent to the NAND flash by the NANDC

NFC_ADDRL

NFC_ADDRL is a low address configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	NFC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addr_l	Lower 32-bit address of the NAND flash

NFC_ADDRH

NFC_ADDRH is a high address configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	NFC_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								addr_h							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	addr_h	Upper 8-bit address of the NAND flash

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NFC_DATA_NUM

NFC_DATA_NUM is a read/written data count configuration register.

Offset Address	Register Name	Total Reset Value
0x0018	NFC_DATA_NUM	0x0000_2480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nfc_data_num													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	nfc_data_num	Number of data segments that are read or written randomly by the NANDC. The maximum value is 9344 bytes. This field is valid only when ecc_type is set to 00.

NFC_OP

NFC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x001C	NFC_OP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				address_cycles			nf_cs		cmd1_en	addr_en	write_data_en	cmd2_en	wait_ready_en	read_data_en	read_status_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:9]	RW	address_cycles	Number of address cycles sent to the NAND flash
[8:7]	RW	nf_cs	NAND flash CS signal select 00: CS0 01: CS1 Others: reserved
[6]	RW	cmd1_en	Command 1 TX enable 0: disabled 1: enabled

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[5]	RW	addr_en	NAND flash address write enable 0: disabled 1: enabled
[4]	RW	write_data_en	NAND flash data write enable Note: read_data_en and write_data_en cannot be 1 at the same time. 0: disabled 1: enabled
[3]	RW	cmd2_en	Command 2 TX enable 0: disabled 1: enabled
[2]	RW	wait_ready_en	Wait ready/busy high enable 0: disabled 1: enabled
[1]	RW	read_data_en	Start read state machine, NAND flash data read enable Note: read_data_en and write_data_en cannot be 1 at the same time. 0: disabled 1: enabled
[0]	RW	read_status_en	When this bit is 1, the command **0x70** for reading the status is sent to the NAND flash and the status data is read from the NAND flash. After that, the returned status data is written to the nfc_status field of the NANDC status register but not the internal buffer. 0: disabled 1: enabled

NFC_STATUS

NFC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0020	NFC_STATUS	0x0000_001F

Bit	31 30 29 28	27 26 25 24	23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved			nfc_randomizer_en	nfc_ecc_type	nf_status		reserved		nf1_ready	nf0_ready	nfc_ready

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Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 1

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RO	nfc_randomizer_en	Randomizer enable of the NANDC 0: disabled 1: enabled
[19:16]	RO	nfc_ecc_type	ECC information of the NANDC The read value indicates the same as the value of ecc_type in the NFC_CON register.
[15:8]	RO	nf_status	NAND flash status data read from the NAND flash
[7:5]	RO	reserved	Reserved
[4:3]	RO	reserved	Reserved
[2]	RO	nf1_ready	Status of the ready/busy signal of the NAND flash corresponding to CS1 This bit is valid when multiple external flash memories are connected and they use independent ready_busy signals. The reset value of this bit is 0 because multiple NAND flash memories share a ready/busy signal by default.
[1]	RO	nf0_ready	Status of the ready/busy signal of the NAND flash corresponding to CS0 This bit is valid when multiple external flash memories are connected and they use independent ready_busy signals. The reset value of this bit is 0 because multiple NAND flash memories share a ready/busy signal by default.
[0]	RO	nfc_ready	Current NANDC status 0: The controller is performing an operation. 1: The operation is complete and the controller is ready to receive the next command. This bit is automatically cleared when the operation register is written to start the NANDC.

NFC_INTEN

NFC_INTEN is an interrupt enable register.

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Offset Address	Register Name	Total Reset Value
0x0024	NFC_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					dma_err_en	dma_done_en	wr_lock_en	ahb_op_en	err_invalid_en	err_valid_en	reserved		cs1_done_en	cs0_done_en	op_done_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RW	dma_err_en	DMA transfer bus error interrupt enable 0: disabled 1: enabled
[9]	RW	dma_done_en	DMA transfer completion interrupt enable 0: disabled 1: enabled
[8]	RW	wr_lock_en	Lock address write error interrupt enable 0: disabled 1: enabled
[7]	RW	ahb_op_en	NANDC buffer read/write error interrupt enable when the NANDC reads/writes data from/to the flash memory 0: disabled 1: enabled
[6]	RW	err_invalid_en	Uncorrectable error interrupt enable 0: disabled 1: enabled
[5]	RW	err_valid_en	Correctable error interrupt enable 0: disabled 1: enabled
[4:3]	RO	reserved	Reserved
[2]	RW	cs1_done_en	Interrupt generated when the ready/busy signal corresponding to CS1 changes from low to high 0: disabled 1: enabled
[1]	RW	cs0_done_en	Interrupt generated when the ready/busy signal corresponding to CS0 changes from low to high 0: disabled 1: enabled

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[0]	RW	op_done_en	Current operation completion interrupt enable of the NANDC 0: disabled 1: enabled

NFC_INTS

NFC_INTS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0028	NFC_INTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					dma_err	dma_done	wr_lock_err	ahb_op_err	err_invalid	err_valid	reserved		cs1_done	cs0_done	op_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RO	dma_err	DMA transfer bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	dma_done	DMA transfer completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	wr_lock_err	Locked address write interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	ahb_op_err	Interrupt generated when the CPU reads and writes to the NANDC buffer in the process of reading/writing data from/to the flash by the NANDC 0: No interrupt is generated. 1: An interrupt is generated.

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[6]	RO	err_invalid	Uncorrectable error interrupt An interrupt is generated if errors occur in eight or more bits of the checked 1 KB data in 8-bit ECC mode. An interrupt is generated if errors occur in 24 or more bits of the checked 1 KB data in 24-bit ECC mode. An interrupt is generated if errors occur in 40 or more bits of the checked 1 KB data in 40-bit ECC mode. An interrupt is generated if errors occur in 64 or more bits of the checked 1 KB data in 64-bit ECC mode. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	err_valid	Correctable error interrupt. An interrupt is generated if errors occur in 1 to 8 bits of the checked 1 KB data in 8-bit ECC mode. An interrupt is generated if errors occur in 1 to 24 bits of the checked 1 KB data in 24-bit ECC mode. An interrupt is generated if errors occur in 1 to 40 bits of the checked 1 KB data in 40-bit ECC mode. An interrupt is generated if errors occur in 1 to 64 bits of the checked 1 KB data in 64-bit ECC mode. 0: No interrupt is generated. 1: An interrupt is generated.
[4:3]	RO	reserved	Reserved
[2]	RO	cs1_done	Interrupt generated when the ready/busy signal corresponding to CS1 changes from low to high This bit is valid when two flash memories are connected and the two memories use separate ready_busy signals. Otherwise, this bit is fixed at 0. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	cs0_done	Interrupt generated when the ready/busy signal corresponding to CS0 changes from low to high This bit is valid when two flash memories are connected and the two memories use separate ready_busy signals. Otherwise, this bit is fixed at 0. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	op_done	Current NANDC operation completion interrupt This bit is automatically cleared when the NFC_OP register is written. 0: No interrupt is generated. 1: An interrupt is generated.

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NFC_INTCLR

NFC_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x002C	NFC_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					dma_err_clr	dma_done_clr	wr_lock_err_clr	ahb_op_err_clr	err_invalid_clr	err_valid_clr	reserved		cs1_done_clr	cs0_done_clr	op_done_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	WO	dma_err_clr	Writing 1 clears the DMA transfer bus error interrupt.
[9]	WO	dma_done_clr	Writing 1 clears the dma_done interrupt.
[8]	WO	wr_lock_err_clr	Writing 1 clears the wr_lock_err interrupt.
[7]	WO	ahb_op_err_clr	Writing 1 clears the ahb_op_err interrupt.
[6]	WO	err_invalid_clr	Writing 1 clears the err_invalid interrupt.
[5]	WO	err_valid_clr	Writing 1 clears the err_valid interrupt.
[4:3]	RO	reserved	Reserved
[2]	WO	cs1_done_clr	Writing 1 clears the cs1_done interrupt.
[1]	WO	cs0_done_clr	Writing 1 clears the cs0_done interrupt.
[0]	WO	op_done_clr	Writing 1 clear the op_done interrupt.

NFC_LOCK

NFC_LOCK is a lock address configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	NFC_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lock_excmd_en	lock_en	global_lock_en	lock_down

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	lock_excmd_en	Address write-protection enable for the extended write command (new command added for new memories) 0: disabled 1: enabled
[2]	RW	lock_en	Flash lock enable 0: disabled 1: enabled
[1]	RW	global_lock_en	Flash global lock enable 0: disabled 1: enabled
[0]	RW	lock_down	Flash lock mode 0: lock mode 1: lock-down mode. If this bit is set to 1, it can be set to 0 only after hardware reset.

NFC_LOCK_SA0

NFC_LOCK_SA0 is lock start address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	NFC_LOCK_SA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_addr0																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock start address 0 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_addr0	Lock start address 0. The least significant bit (LSB) corresponds to flash_row_addr[5].

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NFC_LOCK_SA1

NFC_LOCK_SA1 is lock start address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x0038	NFC_LOCK_SA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Flash_lock_cs	Flash_lock_addr1				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock start address 1 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_addr1	Lock start address 1. The LSB corresponds to flash_row_addr[5].

NFC_LOCK_SA2

NFC_LOCK_SA2 is lock start address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x003C	NFC_LOCK_SA2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Flash_lock_cs	Flash_lock_addr2				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved

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[20:19]	RW	Flash_lock_cs	CS corresponding to lock start address 2 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_addr2	Lock start address 2. The LSB corresponds to flash_row_addr[5].

NFC_LOCK_SA3

NFC_LOCK_SA3 is lock start address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x0040	NFC_LOCK_SA3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Flash_lock_cs	Flash_lock_addr3			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock start address 3 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_addr3	Lock start address 3. The LSB corresponds to flash_row_addr[5].

NFC_LOCK_EA0

NFC_LOCK_EA0 is lock end address 0 configuration register.

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Offset Address	Register Name	Total Reset Value
0x0044	NFC_LOCK_EA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												Flash_lock_cs	Flash_lock_eaddr0																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock end address 0 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_eaddr0	Lock end address 0. The LSB corresponds to flash_row_addr[5].

NFC_LOCK_EA1

NFC_LOCK_EA1 is lock end address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x0048	NFC_LOCK_EA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												Flash_lock_cs	Flash_lock_eaddr1																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock end address 1 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_eaddr1	Lock end address 1. The LSB corresponds to flash_row_addr[5].

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NFC_LOCK_EA2

NFC_LOCK_EA2 is lock end address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x004C	NFC_LOCK_EA2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Flash_lock_cs	Flash_lock_eaddr2				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock end address 2 00: CS0 01: CS1 Others: reserved
[18:0]	RW	Flash_lock_eaddr2	Lock end address 2. The LSB corresponds to flash_row_addr[5].

NFC_LOCK_EA3

NFC_LOCK_EA3 is lock end address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x0050	NFC_LOCK_EA3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Flash_lock_cs	Flash_lock_eaddr3				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	Flash_lock_cs	CS corresponding to lock end address 3 00: CS0 01: CS1 Others: reserved

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[18:0]	RW	Flash_lock_eaddr3	Lock end address 3. The LSB corresponds to flash_row_addr[5].

NFC_EXPCMD

NFC_EXPCMD is an extended page command register.

Offset Address	Register Name	Total Reset Value
0x0054	NFC_EXPCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ex_pcmd3								ex_pcmd2								ex_pcmd1								ex_pcmd0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ex_pcmd3	Write command 3 for the flash extended page
[23:16]	RW	ex_pcmd2	Write command 2 for the flash extended page
[15:8]	RW	ex_pcmd1	Write command 1 for the flash extended page
[7:0]	RW	ex_pcmd0	Write command 0 for the flash extended page

NFC_EXBCMD

NFC_EXBCMD is an extended block command register.

Offset Address	Register Name	Total Reset Value
0x0058	NFC_EXBCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ex_bcmd1								ex_bcmd0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	ex_bcmd1	Write command 1 for the flash extended block
[7:0]	RW	ex_bcmd0	Write command 0 for the flash extended block

NFC_ECC_TEST

NFC_ECC_TEST is an ECC test register.

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Offset Address	Register Name	Total Reset Value
0x005C	NFC_ECC_TEST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											bb_err	reserved	ecc_mask	dec_only	enc_only
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	bb_err	Boot failure due to bad blocks. 0: no bad block 1: boot failure due to bad blocks
[3]	RO	reserved	Reserved
[2]	RW	ecc_mask	ECC function mask. 0: Whether to perform ECC check and correction depends on the value of ecc_type. 1: The ECC check and correction are disabled. The structure of the data read from or written to the NAND flash is still converted based on the ecc_type format.
[1]	RW	dec_only	Decoding only enable. Writing 1 to this bit enables ECC decoding, but the NAND flash cannot be read or written. Reading this bit returns 0.
[0]	RW	enc_only	Encoding only enable. Writing 1 to this bit enables ECC encoding, but the NAND flash cannot be read or written. When this bit is read, the following values may be returned: 0: Encoding and decoding are being performed. 1: ECC encoding and decoding are complete.

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NFC_DMA_CTRL

NFC_DMA_CTRL is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x0060	NFC_DMA_CTRL	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			dma_rd_oob	wr_cmd_disable	reserved	dma_nf_cs		dma_addr_num	burst16_en	burst8_en	burst4_en	reserved		dma_wr_en	dma_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	dma_rd_oob	Whether to read only the OOB or the entire page (data area+OOB) during the DMA read operation 0: read the entire page 1: read only the OOB
[11]	RW	wr_cmd_disable	Whether the write command is sent when the DMA write operation is selected 0: The NANDC initiates a complete NAND flash write timing. 1: The NANDC initiates a write data timing but not a write command timing. This bit is valid only when the NAND flash is written in DMA mode.
[10]	RO	reserved	Reserved
[9:8]	RW	dma_nf_cs	CS corresponding to the NAND flash that is selected for the DMA operation 00: CS0 01: CS1 Others: reserved
[7]	RW	dma_addr_num	Number of addresses 0: 5 1: 4
[6]	RW	burst16_en	Burst 16 enable 0: disabled 1: enabled

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[5]	RW	burst8_en	Burst 8 enable 0: disabled 1: enabled
[4]	RW	burst4_en	Burst 4 enable 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved
[1]	RW	dma_wr_en	DMA read/write enable 0: read 1: write
[0]	RW	dma_start	DMA operation start Writing 1 to this bit starts the DMA operation. The bit retains 1 until the DMA operation is complete. Writing 0 to this bit has no effect. After the DMA operation is started, if 0 is returned when this bit is read, the DMA operation is complete.

NFC_BADDR_D0

NFC_BADDR_D0 is a base address register for the data transfer area.

Offset Address	Register Name	Total Reset Value
0x0064	NFC_BADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d0	Base address for the DDR data area that stores the data to be read or written

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NFC_BADDR_OOB

NFC_BADDR_OOB is a base address register for the OOB transfer area.

Offset Address	Register Name	Total Reset Value
0x0068	NFC_BADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_oob	DDR base address for the OOB area that stores the data to be read

NFC_DMA_LEN

NFC_DMA_LEN is a transfer length register.

Offset Address	Register Name	Total Reset Value
0x006C	NFC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				len_oob												reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	len_oob	Length of the OOB area when the NAND flash is written in DMA mode (4-byte aligned). This field is valid only in ECC0 DMA write mode. In other modes, the OOB length is fixed.
[15:0]	RW	reserved	Reserved

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NFC_OP_PARA

NFC_OP_PARA is an operation parameter register.

Offset Address	Register Name	Total Reset Value
0x0070	NFC_OP_PARA	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												oob_edc_en	data_edc_en	oob_rw_en	data_rw_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	oob_edc_en	OOB area check enable. 0: disabled 1: enabled In programming mode, an ECC code for the OOB area is generated. In data read mode, the OOB area is checked.
[2]	RW	data_edc_en	Check enable. 0: disabled 1: enabled In programming mode, an ECC code is generated. In data read mode, the check function is enabled.
[1]	RW	oob_rw_en	Read/Write enable for the OOB area in the NAND flash. 0: disabled 1: enabled
[0]	RW	data_rw_en	Read/Write enable for the data area of the NAND flash. 0: disabled 1: enabled

NFC_VERSION

NFC_VERSION is a NANDC version register.

Offset Address	Register Name	Total Reset Value
0x0074	NFC_VERSION	0x0000_0620

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				version											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	version	Version number

NFC_SEGMENT_ID

NFC_SEGMENT_ID is a data segment ID register for reading and writing to the NAND flash in DMA mode.

Offset Address	Register Name	Total Reset Value
0x0084	NFC_SEGMENT_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														segment_id	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	segment_id	As the internal buffer stores only 8 KB data at a time, this bit indicates the 8 KB data segment that is being read or written when the flash memory page size is 16 KB. 00: The first 8 KB data segment is being read/written. 01: The second 8 KB data segment is being read/written. 10: The third 8 KB data segment is being read/written. 11: The fourth 8 KB data segment is being read/written.

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NFC_FIFO_EMPTY

NFC_FIFO_EMPTY is an internal FIFO status register.

Offset Address	Register Name	Total Reset Value
0x0090	NFC_FIFO_EMPTY	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								empty_dbg																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RO	empty_dbg	Empty status of the internal FIFO, only for debugging.

NFC_BOOT_SET

NFC_BOOT_SET is a boot parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	NFC_BOOT_SET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												boot_page0_cfg	addr_num	block_size	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	boot_page0_cfg	This bit is fixed at 1.
[2]	RW	addr_num	Number of addresses sent to the NAND flash by the NANDC during booting. 0: 4 address cycles 1: 5 address cycles
[1:0]	RW	block_size	Bus width of the NAND flash during booting 00: 64 pages 01: 128 pages 10: 256 pages 11: 512 pages

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NF_LP_CTRL

NF_LP_CTRL is a NANDC low-power control register.

Offset Address	Register Name	Total Reset Value
0x009C	NF_LP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clk_gate_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	clk_gate_en	Clock gating select. 0: All clocks are enabled. 1: Unused clocks are disabled based on the value of ecc_type.

NFC_ERR_NUM0_BUF0

NFC_ERR_NUM0_BUF0 is NAND flash error bit count register 0 for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00A0	NFC_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf0	Error bit count for the first 4 KB data during the first buffer operation of the NAND flash with the page size of 2 KB, 4 KB, 8 KB, or 16 KB bit[31:24]: number of error bits in the fourth 1 KB data bit[23:16]: number of error bits in the third 1 KB data bit[15:8]: number of error bits in the second 1 KB data bit[7:0]: number of error bits in the first 1 KB data

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NFC_ERR_NUM1_BUF0

NFC_ERR_NUM1_BUF0 is NAND flash error bit count register 1 for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00A4	NFC_ERR_NUM1_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num1_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf0	Error bit count for the last 4 KB data during the first buffer operation of the NAND flash with the page size of 8 KB or 16 KB bit[31:24]: number of error bits in the eighth 1 KB data bit[23:16]: number of error bits in the seventh 1 KB data bit[15:8]: number of error bits in the sixth 1 KB data bit[7:0]: number of error bits in the fifth 1 KB data

NFC_ERR_NUM0_BUF1

NFC_ERR_NUM0_BUF1 is NAND flash error bit count register 0 for the second buffer operation.

Offset Address	Register Name	Total Reset Value
0x00A8	NFC_ERR_NUM0_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf1	Error bit count for the first 4 KB data during the second buffer operation of the NAND flash with the page size of 16 KB bit[31:24]: number of error bits in the fourth 1 KB data bit[23:16]: number of error bits in the third 1 KB data bit[15:8]: number of error bits in the second 1 KB data bit[7:0]: number of error bits in the first 1 KB data

NFC_ERR_NUM1_BUF1

NFC_ERR_NUM1_BUF1 is NAND flash error bit count register 1 for the second buffer operation.

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Offset Address	Register Name	Total Reset Value
0x00AC	NFC_ERR_NUM1_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num1_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf1	Error bit count for the last 4 KB data during the second buffer operation of the NAND flash with the page size of 16 KB bit[31:24]: number of error bits in the eighth 1 KB data bit[23:16]: number of error bits in the seventh 1 KB data bit[15:8]: number of error bits in the sixth 1 KB data bit[7:0]: number of error bits in the fifth 1 KB data

NF_RB_MODE

NF_RB_MODE is a ready_busy mode register of the NAND flash.

Offset Address	Register Name	Total Reset Value
0x00B0	NF_RB_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	status	Ready_busy mode 0: normal ready signal 1: enhanced clear NAND signal of Micron

NFC_BADDR_D1

NFC_BADDR_D1 is base address register 1 of the data transfer area.

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Offset Address	Register Name	Total Reset Value
0x00B4	NFC_BADDR_D1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d1	Base address 1 of the DDR data area that stores the data to be read or written.

NFC_BADDR_D2

NFC_BADDR_D2 is base address register 2 of the data transfer area.

Offset Address	Register Name	Total Reset Value
0x00B8	NFC_BADDR_D2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d2	Base address 2 of the DDR data area that stores the data to be read or written.

NFC_BADDR_D3

NFC_BADDR_D3 is base address register 3 of the data transfer area.

Offset Address	Register Name	Total Reset Value
0x00BC	NFC_BADDR_D3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d3	Base address 3 of the DDR data area that stores the data to be read or written.

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NFC_MEM_CTRL

NFC_MEM_CTRL is an instantiated memory management register.

Offset Address	Register Name	Total Reset Value
0x00CC	NFC_MEM_CTRL	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												mem_ctrl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	mem_ctrl	EMA and EMAW pin value control. [4:1]: The value of the EMA pin is controlled. [0]: The value of the EMAW pin is controlled.

4.4 SPI NAND Flash Controller

4.4.1 Overview

The SPI NAND flash controller provides two AHB slave interfaces on the service side: one is used for accessing controller registers, and the other is used for accessing the SPI NAND flash. It also provides an AHB master interface for reading or writing to the flash in DMA mode. The SPI NAND flash controller integrates the ECC check module for protecting data in the SPI NAND flash.

Figure 4-42 SFC_NAND application block diagram

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CAUTION

Because the SPI NAND flash and SPI NOR flash share a set of pins, the two types of flash memories cannot be used at the same time.

4.4.2 Features

4.4.2.1 AHB Slave Interfaces

The AHB slave interface has the following features:

- Provides AHB slave 0 for accessing the SPI NAND flash by accessing the buffer.
- Provides AHB slave 1 for accessing the internal configuration registers based on selected signals.
- Supports the AMBA 2.0 protocol.
- Supports only the little endian mode.
- Supports OK and ERROR responses but not retry and split responses; supports the 8-/16-/32-bit width; supports busy transmission.

4.4.2.2 AHB Master Interface

The AHB master interface has the following features:

- Enables data transfer between the memory and SPI flash in DMA mode.
- Supports the AMBA 2.0 protocol.
- Supports only the little endian mode.
- Supports the transfer modes including Single, INCR4, INCR8, and INCR16.
- Does not support early termination.
- Supports bus lock.

4.4.2.3 Memory Interfaces

The memory interfaces have the following features:

- Support two CSs. The system can boot from CS1, and CS1 is used by default.
- Support components with 2 KB or 4 KB page size.
- Support components with 64 pages in each block.
- Support address aliasing. Address 0 can be mapped to the SPI NAND flash by using address aliasing after power-on to boot the chip from the SPI NAND flash.
- Support the following interface types: standard SPI, dual-O/dual-I SPI, quad-O/quad-I SPI, dual-I/O SPI, and quad-I/O SPI. The standard SPI is supported by default after power-on. You can change the interface type by configuring a specific register.
- Support the standard SPI and quad-O/quad-I SPI when the chip boots from the SPI NAND flash.
- Support three modes for reading/writing to the SPI NAND flash: single-step register read/write, consecutive register read/write, and DMA read/write. You can read an entire page, only the data, or only the OOB, and you can write to only entire pages.
- Flexibly configure the flash commands issued by the controller to support various SPI NAND flash operations including cache read and write.

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- Support read and write operations on data with variable lengths in transparent transmission mode. The controller does not adjust the sequence of data, that is, data in the SPI NAND flash can be viewed and modified.
- Support two write-protection operations (hardware write protection for the WP pin and software write protection for the BP bit of internal registers of the component).

4.4.2.4 Others

- 8-bit/1024-byte and 24-bit/1024-byte ECC check and error correction
- 2 KB (2048 bytes + 256 bytes) on-chip buffer for improving the read speed
- 1 MB space for boot
- Maximum three consecutive bad blocks allowed during boot. The boot fails if four consecutive bad blocks are detected. The bad block flag is in the default position specified in factory settings.

4.4.3 Function Description

4.4.3.1 Interface Mode Timings

Standard SPI

The standard SPI interface is connected to a 1-bit data input line and a 1-bit data output line. Figure 4-43 and Figure 4-44 show the timings of the standard SPI interface.

Figure 4-43 Write timing of the standard SPI

NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

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Figure 4-44 Read timing of the standard SPI

NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are input in unit of a single bit in serial mode through the sfc_soi1 line.

Dual-Input/Dual-Output SPI

In dual-input/dual-output SPI mode, a 2-bit bidirectional data line is used. Figure 4-45 shows the timing in dual-input/dual-output SPI mode.

Figure 4-45 Timing in dual-input/dual-output SPI mode

NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Dual-I/O SPI

In dual-I/O SPI mode, a 2-bit bidirectional data line is used. Figure 4-46 shows the timing in dual-I/O SPI mode.

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Figure 4-46 Timing in dual-I/O SPI mode

NOTE

The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of dual bits through the sfc_sio0 or sfc_soi1 line. The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Quad-Input/Quad-Output SPI

In quad-input/quad-output SPI mode, a 4-bit bidirectional data line is used. Figure 4-47 shows the timing in quad-input/quad-output SPI mode.

Figure 4-47 Timing in quad-input/quad-output SPI mode

NOTE

The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.

The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Quad-I/O SPI

In quad-I/O SPI mode, a 4-bit bidirectional data line is used. Figure 4-48 shows the timing in quad-I/O SPI mode.

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Figure 4-48 Timing in quad-I/O SPI mode

NOTE

The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line. The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

4.4.3.2 Reading/Writing to the Flash

According to the data sheet of the flash component, a group of command timings needs to be initiated to read or write to the flash. The SPI NAND flash can be read or written in the following modes:

- Single-step register mode. Each command in the command sequence needs to be sent by configuring registers. Take the flash read operation as an example. The command sequences include page read, get feature, and read from cache. In this mode, commands need to be issued for at least three times to read data back to the buffer. This method requires that the CPU directly control the SPI flash commands and parameters to be sent.
- Consecutive register mode. In this mode, only parameters of a key command in the command sequence need to be configured. After the command is sent, data is read or written. Take the flash read operation as an example. The command sequences include page read, get feature, and read from cache. You need to configure only parameters of the read from cache command. After that, data is read back to the buffer.
- DMA mode. This mode is similar to the consecutive register mode. The only difference is that data is transferred to the corresponding DDR address after being read back to the buffer in DMA mode.

NOTE

The preceding modes are restricted by the buffer size (2048 + 256). Components with the 2 KB page size support all the three modes, while components with the 4 KB page size support only the single-step register mode and DMA mode.

4.4.3.3 Other Operations

Other operations on the SPI flash such as erasing and reading the device ID can be implemented only in single-step register mode.

4.4.3.4 Timing Description

Figure 4-49 shows the SPI output timing.

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Figure 4-49 SPI output timing

tcsh: CS setup time
tcss: CS hold time
tshsl: CS deselect time

4.4.4 Working Process

The SPI NAND flash controller supports the boot mode and normal mode. In boot mode, the CPU is allowed only to read data over AHB slave 0; in normal mode, the CPU can perform operations on the flash memory by configuring controller registers.

4.4.4.1 Boot Mode

Boot Configuration Pins

The SPI NAND flash controller supports the following features:

- Booting from the SPI NAND flash
- Components with 2 KB or 4 KB page size
- Components with 64 pages in each block
- Standard SPI and quad-output/quad-input SPI
- Booting from the flash memory corresponding to CS1

After reset, the boot mode depends on the level of the SFC_NAND boot configuration pins. SFC_NAND samples the level values of the boot configuration pins once after the reset is complete, and then the level values of these pins do not affect SFC_NAND any more. Table 4-13 describes the boot configuration pins.

Table 4-13 Boot configuration pins

Pin Name	Register	I/O	Description
SFC_CLK	boot_4_wire_cr	I	Type of the interface for booting 0: standard SPI, one line 1: quad-input/dual-output SPI, four lines
VO_DATA[11]	page_size	I	NAND flash page size 0: 2 KB page size 1: 4 KB page size
VO_DATA[10:9]	ecc_type[1:0]	I	ECC type of the controller 00: reserved

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Pin Name	Register	I/O	Description
			01: 4-bit ECC (8-bit/1024-byte ECC) 10: reserved 11: 24-bit ECC (24-bit/1024-byte ECC)

Notes

In boot mode, the CPU is allowed only to read at most 1 MB data from AHB slave 0. If the read data exceeds 1 MB, the space is wrapped. When the CPU is reading data from AHB slave 0, the controller automatically determines whether data to be read is in the buffer based on the AHB address. If yes, data is directly returned; if not, the controller reads data from the flash to the buffer and then returns the data.

4.4.4.2 Normal Mode

In normal mode, the CPU issues commands on the flash memory by configuring controller registers. Commands can be issued in three modes: single-step register mode, consecutive register mode, and DMA mode.

Initialization

The SPI NAND flash is initialized as follows:

Step 1 Write 1 to SFC_CFG[op_mode] to enter the normal mode, and set SFC_CFG[ecc_type] to configure the check and error correction mode.

Step 2 Write 0 to GLOBAL_CFG[wp_en].

Step 3 Write to TIMING_CFG based on the timing requirements on the connected memory.

In query mode, set the interrupt enable register NFC_INTEN to mask all interrupts; in interrupt mode, enable only the op_done interrupt and mask other interrupts.

----End

Single-Step Register Mode

In single-step register mode, the CPU can issue all commands supported by the flash memory by configuring controller registers. The process is as follows:

Step 1 To transparently transmit data on a specific page of the flash memory (reading or writing to internal registers of the component does not count), write 1 to SFC_CFG[dev_internal_ecc_cr]; otherwise, write 0 to SFC_CFG[dev_internal_ecc_cr].

Step 2 If the interrupt mode is used, clear the op_done interrupt.

Step 3 Configure SFC_OPCODE to set the command to be sent to the flash memory from the controller.

Step 4 Configure SFC_OP_ADDR to set the address of the flash memory to be operated.

Step 5 Configure SFC_DATA_NUM to set the length of data to be operated (in byte).

Step 6 If data is to be written to the flash memory, write data to the buffer.

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Step 7 Configure SFC_OP_CFG to set the interface type, number of dummy bytes, and whether transparent transmission is used.

Step 8 Set SFC_OP[op_start] to 1 to start issuing the command.

Step 9 In interrupt mode, wait until the op_done interrupt is triggered; in query mode, query SFC_OP[op_start] until it is 0.

Step 10 If data on a specific page of the flash memory is transparently transmitted, write 0 to SFC_CFG [dev_internal_ecc_cr].

If data is read from the flash memory, read the data to the buffer. However, if the values of internal status registers of the flash memory are read, the read data is in SF_STATUS.

----End

Consecutive Register Mode

In consecutive register mode, the controller automatically implements two groups of command sequences (one group at a time). One group is required for the read operation (page read, get feature, and read from cache), and the other group is required for the write operation (write enable, program load, program execute, and get feature). The process is as follows:

Step 1 To transparently transmit data on a specific page of the flash memory, write 1 to SFC_CFG[dev_internal_ecc_cr]; otherwise, write 0 to SFC_CFG[dev_internal_ecc_cr].

Step 2 If the interrupt mode is used, clear the op_done interrupt.

Step 3 If data is to be written to the flash memory, write data to the buffer.

Step 4 Configure SFC_OP_CFG to set the interface type, number of dummy bytes, and whether transparent transmission is used.

Step 5 Configure SFC_ADDRH and SFC_ADDRL to set the address of the page to be operated.

Step 6 Configure SFC_OP_CTRL to start issuing the command. SFC_OP_CTRL[rd_opcode] is the operation code for the read from cache command, and SFC_OP_CTRL[wr_opcode] is the operation code for the program load command. Only SFC_OP_CTRL[rd_opcode] needs to be configured for the read operation, and only SFC_OP_CTRL[wr_opcode] needs to be configured for the write operation.

Step 7 In interrupt mode, wait until the op_done interrupt is triggered; in query mode, query SFC_OP_CTRL[op_ready] until it is 0.

Step 8 If data on a specific page of the flash memory is transparently transmitted, write 0 to SFC_CFG [dev_internal_ecc_cr].

Step 9 If data is read from the flash memory, read the data to the buffer.

----End

DMA Mode

In DMA mode, the controller automatically implements two groups of command sequences (one group at a time). One group is required for the read operation (page read, get feature, and read from cache), and the other group is required for the write operation (write enable, program load, program execute, and get feature). The process is as follows:

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Step 1 To transparently transmit data on a specific page of the flash memory, write 1 to SFC_CFG[dev_internal_ecc_cr]; otherwise, write 0 to SFC_CFG[dev_internal_ecc_cr].

Step 2 If the interrupt mode is used, clear the op_done interrupt.

Step 3 Configure SFC_DMA_SADDR_D to set the base address for the data in the DDR.

Step 4 Configure SFC_DMA_SADDR_OOB to set the base address for the OOB in the DDR.

Step 5 If data is to be written to the flash memory, write the data to the position specified by SFC_DMA_SADDR_D in the DDR, and write the OOB to the position specified by SFC_DMA_SADDR_OOB in the DDR.

Step 6 If data on a specific page of the flash memory is to be transparently transmitted, configure SFC_DMA_LEN to set the number of OOB bytes to be transmitted.

Step 7 Configure SFC_OP_CFG to set the interface type, number of dummy bytes, and whether transparent transmission is used.

Step 8 Configure SFC_ADDRH and SFC_ADDRL to set the address of the page to be operated.

Step 9 Configure SFC_OP_CTRL to start issuing the command. SFC_OP_CTRL[rd_opcode] is the operation code for the read from cache command, and SFC_OP_CTRL[wr_opcode] is the operation code for the program load command. Only SFC_OP_CTRL[rd_opcode] needs to be configured for the read operation, and only SFC_OP_CTRL[wr_opcode] needs to be configured for the write operation.

Step 10 In the interrupt mode, wait until the op_done interrupt is triggered; in query mode, query SFC_OP_CTRL[op_ready] until it is 0.

Step 11 If data on a specific page of the flash memory is passed through, write 0 to SFC_CFG [dev_internal_ecc_cr].

Step 12 If data is read from the flash memory, read the data to the DDR.

----End

Notes

For details about the parameters related to flash instructions, see the data sheet of the connected component.

4.4.5 Data Storage Structure

The size of the SFC_NAND buffer is 2048 bytes+256 bytes. This section describes the storage structures of the data in the SFC_NAND buffer read from or written to the SPI NAND flash.

4.4.5.1 Non-ECC Mode

If no ECC check is required for the SFC_NAND:

- The SFC_NAND transparently writes the data in buffers to the SPI NAND flash without processing.
- The SFC_NAND writes data read from the SPI NAND flash to the internal buffers without processing.
- The SPI NAND flash with 2 KB or 4 KB page size is supported.

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NOTE

To enter the non-ECC mode, set SFC_CFG[dev_internal_ecc_cr] and SFC_OP_CFG[dir_trans_en] to 1. To enter any other ECC mode, set SFC_CFG[dev_internal_ecc_cr] to 0.

4.4.5.2 4-Bit ECC Mode (8-Bit/1024-Byte ECC)

2 KB (2048+64) Page Size

For the SPI NAND flash with the 2 KB page size, the available spare area for the software is 30 bytes. Figure 4-50 shows the (2048+32)-byte data structure of the driver software.

Figure 4-50 (2048+32)-byte data structure of the driver software in 4-bit ECC mode

DATA(2048B)	BB	CTRL	RSV

BB: bad block, 2 bytes
CTRL: control area for software, 30 bytes

Figure 4-51 shows the data structure of the data written to the NAND flash. The software valid data is divided into two 1040-byte data segments, and the ECC is calculated for each data segment. When being written to the NAND flash, the data is automatically stored in two groups in the alternate form of 1040-byte data+14-byte ECC code. The BB information is stored in the first two bytes of the NAND flash spare area.

Figure 4-51 Data structure of the NAND flash in 4-bit ECC mode

DATA(1040)+ECC(14)+DATA(994)+BB(2) +DATA(14)+ECC(14)+CTRL(30)

4 KB (4096+128) Page Size

For the SPI NAND flash with the 4 KB page size, the available spare area for the software is 30 bytes. Figure 4-52 shows the (4096+32)-byte data structure of the driver software.

Figure 4-52 (4096+32)-byte data structure of the driver software in 4-bit ECC mode

DATA(4096)	BB	CTRL	RSV

BB: bad block, 2 bytes
CTRL: control area for software, 30 bytes

Figure 4-53 shows the data structure of the data written to the NAND flash. The software valid data is divided into four 1032-byte data segments, and the ECC is calculated for each data segment. When being written to the NAND flash, the data is automatically stored in four groups in the alternate form of 1032-byte data+14-byte ECC code. The BB information is stored in the first two bytes of the NAND flash spare area.

Figure 4-53 (4096+128)- byte data structure of the NAND flash in 4-bit ECC mode

DATA(1032)+ECC(14)+DATA(1032)+ECC(14)+DATA(1032)+ECC(14)+DATA(958)+BB(2) +DATA(42)+ECC(14)+CTRL(30)

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4.4.5.3 24-Bit ECC Mode (24-Bit/10240-Byte ECC)

The 24-bit ECC mode requires larger spare area than that required for the 4-bit ECC mode (because there are more ECC bytes). Therefore, ensure that there is sufficient spare area before choosing the 24-bit ECC mode. The spare area must be greater than to equal to 116 bytes if the component page size is 2 KB, and it must greater than or equal to 200 bytes if the component page size is 4 KB.

2 KB Page Size

Figure 4-54 shows the (2048+32)-byte data structure of the driver software when the page size is 2 KB.

Figure 4-54 (2048+32)-byte data structure of the driver software in 24-bit ECC mode

DATA(2048B)	BB	CTRL	RSV

BB: bad block, 2 bytes
CTRL: control area for software, 30 bytes

Figure 4-55 shows the data structure of the data written to the NAND flash. The BB information is stored in byte 2048.

The software valid data is divided into two 1024 bytes+16 bytes data segments, and a 42-byte ECC is calculated for each data segment. When being written to the NAND flash, the data segments and ECC code are alternatively stored, totally (2048+116) bytes. The BB flag is stored in byte 2048 of the NAND flash.

Figure 4-55 (2048+116)-byte data structure of the NAND flash in 24-bit ECC mode

DATA(1040)	ECC(42)	DATA(966)	BB(2)	DATA(42)	ECC(42)	CTRL(30)

4 KB Page Size

Figure 4-56 shows the (4096+32)-byte data structure of the driver software when the page size is 4 KB.

Figure 4-56 (4096+32)-byte data structure of the driver software in 24-bit ECC mode

DATA(4096)	BB	CTRL	RSV

BB: bad block, 2 bytes
CTRL: control area for software, 30 bytes

Figure 4-57 shows the structure of the data written to the NAND flash. The software valid data is divided into four 1024 bytes+8 bytes data segments, and a 42-byte ECC is calculated for each data segment.

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When being written to the NAND flash, data and ECC code in the first three data segments are stored in the alternative form. For the last data segment (1024 bytes+8 bytes+42 bytes), the bad block flag is inserted in byte 4096 of the NAND flash.

Figure 4-57 (4096+200)-byte data structure of the NAND flash in 24-bit ECC mode

DATA(1032)+ECC(42)+DATA(1032)+ECC(42)+DATA(1032)+ECC(42)+DATA(874)+BB(2)+DATA(126)+ECC(42)+CTRL(30)

4.4.6 ECC Mode Selection

The ECC IP used by the controller processes data based on 1 KB data block. Therefore, the ECC performance of the controller is described in the format of *n* bits/1 KB, for example, 8 bits/1 KB or 24 bits/1 KB. To ensure component reliability, the recommended ECC performance of 1 bit/512 bytes, 4 bits/512 bytes, or 8 bits/512 bytes is provided in the component data sheet. The ECC performance of 8 bits/1 KB is equivalent to that of 4 bits/512 bytes. When you select the ECC mode for the controller, note the following:

- The priority of the ECC performance of the controller is higher than or equal to that of the recommended ECC performance.

  For example, if the recommended ECC performance is 1 bit/512 bytes or 4 bits/512 bytes, the controller can select the ECC mode with the performance of 8 bits/1 KB.
- The component page size must be greater than or equal to the required storage size of the ECC mode for the controller.

  For example, if the component page size is (2 KB + 64 bytes), the controller cannot select the ECC mode with the performance of 24 bits/1 KB because the required storage size of this ECC mode is (2 KB + 116 bytes). For details about the required storage size for the ECC mode, see section 4.3.5 "Data Storage Structure."

4.4.7 Register Summary

Table 4-14 describes SPI NAND flash registers.

Table 4-14 Summary of SPI NAND flash registers (base address: 0x1004_0000)

Offset Address	Register	Description	Page
0x0000	SFC_CFG	SFC configuration register	4-274
0x0004	GLOBAL_CFG	Global configuration register	4-276
0x0008	TIMING_CFG	Timing configuration register	4-277
0x000C	SFC_INT	Interrupt status register	4-277
0x0010	SFC_INT_EN	Interrupt enable register	4-279
0x0014	SFC_INT_CLR	Interrupt clear register	4-279
0x0018	SFC_OPCODE	Command word configuration register	4-280
0x001C	SFC_OP_ADDR	Operation address configuration register	4-281
0x0020	SFC_OP	Operation register	4-281

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Offset Address	Register	Description	Page
0x0024	SFC_DATA_NUM	Data length register	4-282
0x0028	SFC_OP_CFG	Operation configuration register	4-283
0x002C	SFC_ADDRH	Upper-bit component address configuration register	4-284
0x0030	SFC_ADDRL	Lower-bit component address configuration register	4-284
0x0034	SFC_OP_CTRL	Operation control register	4-285
0x003C	SFC_DMA_CTRL	DMA operation control register	4-286
0x0040	SFC_DMA_SADDR_D	DDR start address register for the DMA operation mode	4-286
0x0044	SFC_DMA_SADDR_OOB	DDR start address register for the DMA operation mode	4-287
0x0048	SFC_DMA_LEN	Data transfer length register for the DMA operation mode	4-287
0x004C	SFC_TIMEOUT_WR	Write operation timeout register	4-288
0x0050	SFC_SEGMENT_ID	Data segment ID register for reading/writing to the NAND flash in DMA mode	4-288
0x0054	SF_STATUS	Flash memory status register	4-289
0x0058	SFC_OP_CNT	SFC command issuing count register	4-289
0x005C	SFC_OP_CNT_CLR	SFC command issuing count clear register	4-290
0x0060	AFIFO_DEBUG	Clock domain convert AFIFO debug register	4-290
0x0064	BB_ERR	Boot status indicator register	4-291
0x0068	VERSION	Version register	4-291
0x006C	SFC_ERR_NUM	Error correction count register	4-292

4.4.8 Register Description

SFC_CFG

SFC_CFG is an SFC configuration register.

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Offset Address	Register Name	Total Reset Value
0x0000	SFC_CFG	0x0000_1DC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														boot_4_wire_cr	dev_internal_ecc_cr	spi_nand_sel		reserved				reserved				reserved		ecc_type		page_size	flash_sel	op_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	1	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	boot_4_wire_cr	Type of the interface for booting. 0: standard SPI, one line 1: quad-input/dual-output SPI, four lines
[16]	RW	dev_internal_ecc_cr	ECC management solution. 0: The ECC is managed by the controller. 1: The internal ECC of the component is used.
[15:14]	RW	spi_nand_sel	Vendor of the SPI NAND flash. 01: Winbond 10: ESMT Other values: other vendors
[13:10]	RO	reserved	Reserved
[9:6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4:3]	RW	ecc_type	ECC type of the controller. 00: reserved 01: 4-bit ECC (8-bit/1024-byte ECC) 10: reserved 11: 24-bit ECC(24-bit/1024-byte ECC) The reset value is determined by the corresponding pin.
[2]	RW	page_size	Page size of the NAND flash. 0: 2 KB page size 1: 4 KB page size The reset value is determined by the corresponding pin.

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[1]	RW	flash_sel	Flash type 0: reserved 1: SPI NAND flash
[0]	RW	op_mode	SFC operation mode. 0: boot mode 1: normal mode

GLOBAL_CFG

GLOBAL_CFG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	GLOBAL_CFG	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									force_cs_en	wp_en	wip_locate				rd_delay
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	force_cs_en	CS forcible enable. 0: disabled 1: enabled
[5]	RW	wp_en	Write protection enable for the WP pin. When it is enabled, the chip outputs 0 to the WP pin. 0: disabled 1: enabled
[4:2]	RW	wip_locate	Position of the write in progress (WIP) bit in the status register.
[1:0]	RW	rd_delay	Number of delayed clock cycles for reading data from the SPI NAND flash. 00: no delay (default) 01: one clock cycle 10: two clock cycles 11: three clock cycles

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TIMING_CFG

TIMNG_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	TIMING_CFG	0x0000_066F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				tcsh				tcss				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	tcsh	CS hold time 0000–1111: (n + 1) clock cycles. Note: n represents 0, 1, 2, ..., or 15.
[7:4]	RW	tcss	CS setup time 0000–1111: (n + 1) clock cycles. Note: n represents 0, 1, 2, ..., or 15.
[3:0]	RW	tshsl	CS deselect time. It is equal to the interval between two flash operations. 0000–1111: (n + 1) clock cycles. Note: n represents 0, 1, 2, ..., or 15.

SFC_INT

SFC_INT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	SFC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ahb_op_err_int	dma_err_int	err_inval_int	err_val_int	op_fail_int	reserved	op_done_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

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[6]	RO	ahb_op_err_int	AHB operation error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	dma_err_int	DMA transfer bus error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	err_inval_int	Uncorrectable error interrupt. In 4-bit ECC mode, if there are eight or more error bits in the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if there are 24 or more error bits in the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err_val_int	Correctable error interrupt. In 4-bit ECC mode, if there are 1−8 error bits in the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if there are 1−24 error bits in the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	op_fail_int	Program operation failure interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	reserved	Reserved
[0]	RO	op_done_int	Current controller operation completion interrupt. This bit is automatically cleared when SFC_OP[op_start] is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

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SFC_INT_EN

SFC_INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0010	SFC_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ahb_op_err_int_en	dma_err_int_en	err_inval_int_en	err_val_int_en	op_fail_int_en	reserved	op_done_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	ahb_op_err_int_en	AHB operation error interrupt enable. 0: disabled 1: enabled
[5]	RW	dma_err_int_en	DMA transfer bus error interrupt enable. 0: disabled 1: enabled
[4]	RW	err_inval_int_en	Uncorrectable error interrupt enable. 0: disabled 1: enabled
[3]	RW	err_val_int_en	Correctable error interrupt enable. 0: disabled 1: enabled
[2]	RW	op_fail_int_en	Program operation failure interrupt enable. 0: disabled 1: enabled
[1]	RO	reserved	Reserved
[0]	RW	op_done_int_en	Current operation completion interrupt enable. 0: disabled 1: enabled

SFC_INT_CLR

SFC_INT_CLR is an interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x0014	SFC_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ahb_op_err_int_clr	dma_err_int_clr	err_inval_int_clr	err_val_int_clr	op_fail_int_clr	reserved	op_done_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RWS	ahb_op_err_int_clr	AHB operation error interrupt clear. Writing 1 clears the interrupt.
[5]	RWS	dma_err_int_clr	DMA transfer bus error interrupt clear. Writing 1 clears the interrupt.
[4]	RWS	err_inval_int_clr	err_invalid interrupt clear. Writing 1 clears the interrupt.
[3]	RWS	err_val_int_clr	err_valid interrupt clear. Writing 1 clears the interrupt.
[2]	RWS	op_fail_int_clr	op_fail interrupt clear. Writing 1 clears the interrupt.
[1]	RO	reserved	Reserved
[0]	RWS	op_done_int_clr	op_done interrupt clear. Writing 1 clears the interrupt.

SFC_OPCODE

SFC_OPCODE is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0018	SFC_OPCODE	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								opcode							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	opcode	Command issued to the flash from the controller.

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SFC_OP_ADDR

SFC_OP_ADDRL is an operation address configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	SFC_OP_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	op_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	op_addr	Operation address of the flash.

SFC_OP

SFC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x0020	SFC_OP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sf_cs	addr_num			dummy1_en	dummy0_en	opcode_en	addr_en	write_data_en	read_data_en	read_status_en	op_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	sf_cs	CS corresponding to the flash memory to be operated. 0: CS0 1: CS1
[10:8]	RW	addr_num	Number of bytes of the address sent to the flash.
[7]	RW	dummy1_en	Dummy byte transfer enable after the command operation is enabled. 0: disabled 1: enabled
[6]	RW	dummy0_en	Dummy byte transfer enable after the address operation is enabled. 0: disabled 1: enabled

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[5]	RW	opcode_en	Opcode command transfer enable. 0: disabled 1: enabled
[4]	RW	addr_en	Flash write address enable. 0: disabled 1: enabled
[3]	RW	write_data_en	Flash data write enable. Note: read_data_en and write_data_en cannot be 1 at the same time. 0: disabled 1: enabled
[2]	RW	read_data_en	Flash data read enable. Note: read_data_en and write_data_en cannot be 1 at the same time. 0: disabled 1: enabled
[1]	RW	read_status_en	When this flag is 1, the SPI NAND flash status is read, and the returned data is written to the sf_status register (but not the internal buffer). 0: disabled 1: enabled
[0]	RW	op_start	Start operation indicator. This bit is pulled down when the completion of the corresponding operation is detected.

SFC_DATA_NUM

SFC_DATA_NUM is a data length register.

Offset Address	Register Name	Total Reset Value
0x0024	SFC_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				data_num											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	data_num	Length of data to be processed during one operation. This register needs to be configured when there is data transmission and does not need to be configured for the DMA operations.

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SFC_OP_CFG

SFC_OP_CFG is an operation configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	SFC_OP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dir_trans_en	rd_op_sel			mem_if_type			dummy1_num		dummy0_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	dir_trans_en	Whether to use the data structure of the controller when accessing the SPI flash. The value 1 indicates transparent transmission, and the controller only transfers data. It must be set to 1 when registers need to be accessed. 0: disabled 1: enabled
[10:9]	RW	rd_op_sel	Area of data to be read. 00: entire page 01: data area only 10: OOB only 11: reserved
[8:6]	RW	mem_if_type	SPI flash interface type. 000: standard SPI 101: dual-input/dual-output SPI 010: dual-I/O SPI 011: quad-input/dual-output SPI 100: quad-I/O SPI 101−111: reserved
[5:3]	RW	dummy1_num	In single-step mode, this field specifies the number of bytes to be operated for dummy1_en. In consecutive mode, this field is configured based on the timing parameters of the rd_opcode/wr_opcode command words.
[2:0]	RW	dummy0_num	In single-step mode, this field specifies the number of bytes to be operated for dummy0_en. In consecutive mode, this field is configured based on the timing parameters of the rd_opcode/wr_opcode command words.

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SFC_ADDRH

SFC_ADDRH is an upper-bit component address configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	SFC_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								page_addr_h							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	page_addr_h	Page address, upper 1 byte.

SFC_ADDRL

SFC_ADDRL is a lower-bit component address configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	SFC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	page_addr_l																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	page_addr_l	Page address, lower 2 bytes.
[15:0]	RO	reserved	Reserved

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SFC_OP_CTRL

SFC_OP_CTRL is an operation control register.

Offset Address	Register Name	Total Reset Value
0x0034	SFC_OP_CTRL	0x0003_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rd_opcode								wr_opcode								reserved				cs_op	dma_op	rw_op	op_ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	rd_opcode	Non-bus mode, read operation command.
[15:8]	RW	wr_opcode	Non-bus mode, write operation command.
[7:4]	RO	reserved	Reserved
[3]	RW	cs_op	CS corresponding to the flash to be operated. 0: CS0 1: CS1
[2]	RW	dma_op	Operation mode select. 0: register access mode 1: DMA access mode
[1]	RW	rw_op	Operation type. 0: read 1: write
[0]	RW	op_ready	Start operation indicator. This bit is pulled down when the completion of the corresponding operation is detected.

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SFC_DMA_CTRL

SFC_DMA_CTRL is a DMA operation control register.

Offset Address	Register Name	Total Reset Value
0x003C	SFC_DMA_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													burst16_en	burst8_en	burst4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	burst16_en	Burst16 enable. 0: disabled 1: enabled
[1]	RW	burst8_en	Burst8 enable. 0: disabled 1: enabled
[0]	RW	burst4_en	Burst4 enable. 0: disabled 1: enabled

SFC_DMA_SADDR_D

SFC_DMA_SADDR_D is a DDR start address register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0040	SFC_DMA_SADDR_D	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr	DMA operation indicator, base address for data to be operated in the DDR.

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SFC_DMA_SADDR_OOB

SFC_DMA_SADDR_OOB is a DDR start address register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0044	SFC_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_oob	DMA operation indicator, base address for OOB data to be operated in the DDR.

SFC_DMA_LEN

SFC_DMA_LEN is a data transfer length register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0048	SFC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dma_len																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dma_len	Length of data to be transferred for DMA operations. It indicates the length of the spare area to be transferred. This field is valid only during transparent transmission (dev_internal_ecc_cr and dir_trans_en are 1).

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SFC_TIMEOUT_WR

SFC_TIMEOUT_WR is a write operation timeout register.

Offset Address	Register Name	Total Reset Value
0x004C	SFC_TIMEOUT_WR	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sfc_timeout_wr																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	sfc_timeout_wr	Program operation busy wait time, timeout period.

SFC_SEGMENT_ID

SFC_SEGMENT_ID is a data segment ID register for reading/writing to the NAND flash in DMA mode.

Offset Address	Register Name	Total Reset Value
0x0050	SFC_SEGMENT_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															last_segment
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	last_segment	As the internal buffer stores only 2 KB data at a time, this bit indicates whether the 2 KB data segment being read or written is the last data segment for the component whose page size is 4 KB. 0: The 2 KB data segment being read or written is not the last data segment. 1: The 2 KB data segment being read or written is the last data segment. This bit needs to be configured only for components with the 4 KB page size in single-step mode.

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SF_STATUS

SF_STATUS is a flash memory status register.

Offset Address	Register Name	Total Reset Value
0x0054	SF_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sf_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	sf_status	Reading the flash status register returns the value to this register.

SFC_OP_CNT

SFC_OP_CNT is an SFC command issuing count register.

Offset Address	Register Name	Total Reset Value
0x0058	SFC_OP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																op_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	op_cnt	Count of op operations issued by the SFC, for debugging only.

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SFC_OP_CNT_CLR

SFC_OP_CNT_CLR is an SFC command issuing count clear register.

Offset Address	Register Name	Total Reset Value
0x005C	SFC_OP_CNT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															op_cnt_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RWS	op_cnt_clr	SFC command issuing count clear.

AFIFO_DEBUG

AFIFO_DEBUG is a clock domain convert AFIFO debug register.

Offset Address	Register Name	Total Reset Value
0x0060	AFIFO_DEBUG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rx_fifo_empty	tx_fifo_empty
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	rx_fifo_empty	RX FIFO read empty.
[0]	RO	tx_fifo_empty	TX FIFO read empty.

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BB_ERR

BB_ERR is a boot status indicator register.

Offset Address	Register Name	Total Reset Value
0x0064	BB_ERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															bb_err
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	bb_err	Boot status indicator. 0: success 1: failure

VERSION

VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x0068	VERSION	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	SFC version V400.

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SFC_ERR_NUM

SFC_ERR_NUM is an error correction count register.

Offset Address	Register Name	Total Reset Value
0x006C	SFC_ERR_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ecc_err_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ecc_err_num	Error count. bit[31:24]: number of error bits in the fourth 1 KB data for components with the 4 KB page size bit[23:16]: number of error bits in the third 1 KB data for components with the 4 KB page size bit[15:8]: number of error bits in the second 1 KB data for components with the 4 KB or 2 KB page size bit[7:0]: number of error bits in the first 1 KB data for components with the 4 KB or 2 KB page size

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Contents

5 GSF.....5-1
5.1 Overview.....5-1
5.2 Function Description.....5-1
5.3 General Data Flow.....5-2
5.4 Port Function Configuration Description.....5-2
5.4.1 Managing RX and TX Frames.....5-2
5.4.2 Configuring Descriptor Queues in RX and TX DDR Buffer Areas.....5-2
5.4.3 Managing RX Interrupts.....5-5
5.4.4 Managing TX Interrupts.....5-5
5.4.5 Configuring the Working Status of the PHY Chip.....5-6
5.4.6 Switching Operating Modes.....5-6
5.5 Typical Applications.....5-7
5.5.1 Ethernet Flow Control.....5-7
5.5.2 WoL.....5-8
5.6 Register Summary.....5-9
5.7 Register Description.....5-17

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Figures

Figure 5-1 GSF general data flow 5-2

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5 GSF

5.1 Overview

The gigabit switch fabric (GSF) receives and transmits data over two Ethernet ports at 10/100/1000 Mbit/s in full-duplex or half-duplex mode. The Ethernet port exchanges data with the CPU port, and supports the energy efficient Ethernet (EEE) and wake on LAN (WoL) functions.

5.2 Function Description

The GSF has the following features:

- Supports 10/100/1000 Mbit/s rate.
- Supports the full-duplex or half-duplex mode.
- Supports the reduced media independent interface (RMII), Medium Independent Interface (MII), and reduced gigabit media independent interface (RGMII) interfaces.
- Provides the management data input/output (MDIO) interface.
- Supports frame length effectiveness detection and discards long and short frames.
- Supports the cyclic redundancy check (CRC) on receive (RX) frames and discards frames with CRC errors.
- Supports the CRC on transmit (TX) frames.
- Supports short frame filling.
- Supports outloop (that is, line-side loopback) in full-duplex mode.
- Supports count of RX and TX frames.
- Supports filtering of broadcast, multicast, and unicast frames.
- Supports configurable speed control processing of the control packets, IP packets, and broadcast or multicast packets.
- Supports packet filtering.
- Supports the enqueue interrupt and timeout interrupt modes.
- Supports buffer of RX and TX packets.
- Supports EEE.
- Supports WoL.
- Supports scatter gather (SG).

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- Supports the checksum offload engine (COE).
- Supports TCP segment offload (TSO).
- Supports UDP fragment offload (UFO).

5.3 General Data Flow

Figure 5-1 shows the overall data flow of the GSF GE ports.

Figure 5-1 GSF general data flow

5.4 Port Function Configuration Description

5.4.1 Managing RX and TX Frames

The CPU manages addresses for storing RX and TX frames by configuring the descriptor queue buffer area.

- During reception, the Ethernet module checks whether data packets received from external networks are valid, and then stores the valid packets to the device description repository (DDR) over the bus based on the packet buffer information, including the start address for the packet buffer and packet buffer depth, configured by the CPU.
- During transmission, the Ethernet module obtains the corresponding packets in the DDR over the bus based on the packet buffer information, including the start address for the packet buffer and packet length, configured by the CPU, then packages and transmits the packets to external networks.

5.4.2 Configuring Descriptor Queues in RX and TX DDR Buffer Areas

During transmission, the CPU configures the two buffer queues stored in the DDR. During reception, the CPU configures another two buffer queues. The start addresses for the buffer

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queues are word addresses. A descriptor contains eight words and specifies the information about a packet buffer. Table 5-1 describes the data structure of the first two descriptors in the RX and TX buffers.

Table 5-1 Data structure of the first two descriptors in the RX and TX buffers

Name	Width (Bit)	Description
DataBudSAddr	32	Start address of the packet buffer. The byte address format is supported.
DescVld	1	Whether the flag of the descriptor is valid 0: invalid 1: valid
DataLen	11	Valid data volume in the packet buffer (unit: byte)
BufLen	11	Packet buffer depth (unit: byte)

NOTE

The maximum frame length in the RX direction is 1.6 KB, and therefore the space allocated for storing each frame must be greater than 1.6 KB. It is recommended that the space for storing each frame be (1600 + 128) bytes to ensure sufficient space for storing network packet data.

Table 5-2 Data structure of the first two descriptors in the TX buffer

Name	Bit	Bit Name	Description
desc_word1	[31:0]	DataBufSAddr	If the current descriptor is a non-SG descriptor, this bit indicates the start address of the packet buffer. If the current descriptor is an SG descriptor, this bit indicates the start address of the Level-2 linked list.
desc_word2	[31]	hw_own	Ownership of the current descriptor 0: software 1: logic
	[30]	sg_flag	Whether the SG is supported 0: not supported 1: supported Note: When sg_flag is set to 0, tso_flag must be set to 0.
	[29]	coe_flag	Whether checksum offload is executed. 0: no 1: yes

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Name	Bit	Bit Name	Description
	[28]	tso_flag	Whether TSO is executed 0: no 1: yes
	[27]	reserved	Reserved
	[26:16]	data_len	When sg_flag is set to 1, this bit indicates the size of the mss in the fragmented packet. When sg_flag is set to 0, this bit indicates the size of the whole packet.
	[15:11]	nfrags_num	Number of nfrags in the SK buffer specified by the current descriptor. The maximum number is 17.
	[10]	vlan_flag	Whether the current packet has a VLAN flag 0: no 1: yes
	[9]	ip_version	IP protocol version of the current packet 0: IPv4 1: IPv6
	[8]	protocol_type	Type of the transmission layer protocol of the current packet 0: TCP 1: UDP
	[7:4]	ip_hdr_len	Length of the IP header of the current packet, in the unit of word (four bytes) If the current packet is an IPv4 packet, the length of the IP header is 5 to 15 words. If the current packet is an IPv6 packet, the length of the IP header is 10 words.
	[3:0]	protocol_hdr_len	If the current packet is a TCP packet, this bit indicates the length of the TCP header, in the unit of word (four bytes). The length ranges from 5 to 15 words. If the current packet is a UDP packet, this bit indicates the length of the UDP header, in the unit of word (four bytes). The length is two words.

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5.4.3 Managing RX Interrupts

Generating Interrupts

If the RX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, an RX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the rx_bq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[17].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[7:0].

  Enable the RX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, an RX timeout interrupt is generated. If the requirements for triggering the RX enqueue and timeout interrupts are met, only the RX enqueue interrupt is generated.
- Enable the rx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[28].
- Configure the rx_bq enqueue timeout raw interrupt threshold register RX_BQ_IN_TIMEOUT_TH.

Clearing Interrupts

After the CPU receives an RX enqueue interrupt or RX timeout interrupt, it writes 1 to clear the RX enqueue interrupt and RX timeout interrupt.

5.4.4 Managing TX Interrupts

Generating Interrupts

If the TX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, a TX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the tx_rq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[19].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[23:16].
- Enable the TX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, a TX timeout interrupt is generated. If the requirements for triggering the TX enqueue and timeout interrupts are met, only the TX enqueue interrupt is generated.
- Enable the tx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[29].
- Configure the tx_rq enqueue timeout raw interrupt threshold register TX_RQ_IN_TIMEOUT_TH.

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Clearing Interrupts

After the CPU receives a TX enqueue interrupt or TX timeout interrupt, it writes 1 to clear the TX enqueue interrupt and TX timeout interrupt.

5.4.5 Configuring the Working Status of the PHY Chip

The GSF provides the MDIO interface to manage the physical layer entity sublayer (PHY) chip. The PHY chip can be written or read through the MDIO interface.

The procedure for reading the PHY chip is as follows:

- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[12:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 2'b10 to start the MDIO read operation.
- The MDIO writes the data read from the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0.
- The CPU queries the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] to obtain the data read by the MDIO from the external PHY chip.

The procedure for writing the PHY chip is as follows:

- The CPU writes the data to be transmitted to the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0].
- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[9:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 1 to start the MDIO write operation.
- The MDIO writes the value of the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0] to the corresponding PHY internal registers and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0x0.

5.4.6 Switching Operating Modes

The GSF supports the following operating modes and switches between the modes: RMII (10/100 Mbit/s) and RGMII (10/100/1000 Mbit/s). The operating mode is switched as follows:

Step 1 Set the corresponding GSF CRG control register 0x200300cc PERI_CRG51 to 0xe to implement the reset, configure bit[8:0] of the MAC_IF status control register PERI_CRG59, and set PERI_CRG51 to 0xa to clear the reset so that the configured operating mode takes effect.

Step 2 Enable the MODE_CHANGE_EN register, configure the MAC port rate mode register PORT_MODE, and then disable the MODE_CHANGE_EN register.

NOTE

Do not perform the configuration when the chip is working properly. You are advised to perform the configuration when the chip is initialized.

----End

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5.5 Typical Applications

5.5.1 Ethernet Flow Control

The GSF can control the RX packet flow. That is, the GSF discards the subsequent packets when the number of RX packets exceeds the preset maximum quantity.

The GSF controls the flow of the following three types of packets:

- Control packets
- Service packets
- Multicast or broadcast packets

Flow Control of the Control Packets

The flow of control packets is controlled in the following scenarios:

- Within a specified time segment (indicated by T), a limited number of control packets are allowed to pass through. When the count exceeds the configured upper threshold, the subsequent packets are discarded. The time limit T is measured by 125 μs, which is equal to the configured upper threshold.
- If the number of RX addresses of the RX configuration FIFO is less than the number of limited addresses, all RX control packets pass through preferentially. IP packets are filtered out and discarded no matter whether the IP packet flow is controlled or the number of IP packets reaches the configured upper threshold for flow control.

To control the flow of control packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[20] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[15:0].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].
- Configure the flow control RX address count register CRF_RX_LEFT_NUM.

Flow Control of Service Packets

The flow control of service packets is the same as that of control packets in the first scenario. In the second scenario, all IP packets will be discarded.

To control the flow of service packets (for example, IP packets), the following configurations are required:

- Set the control register CONTROL_WORD bit[21] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[31:16].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].

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Flow Control of Broadcast or Multicast Packets

The time limit for flow control of broadcast or multicast packets is 1 μs. Within the time limit, if the count of packets passing through exceeds the upper threshold, the subsequent broadcast or multicast packets are discarded.

To control the flow of broadcast or multicast packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[16] to 1.
- Configure the flow control packet count register for broadcast or multicast packets CRF_BM_PKT_THRSLD.
- Configure the flow control time threshold register for broadcast and multicast packets CRF_BM_TIME_THRSLD.

5.5.2 WoL

The WoL supports wake-up using wake-up frames and magic packets.

Wake_up Frame

The following describes how to configure the filter template by using template 1 as an example (four templates in total):

- Configure valid byte selection register 1 FILTER_0_BYTE_MASK.
- Configure filter template enable register 1 FILTER_COMMAND.
- Configure the CRC position offset register FILTER_OFFSET.
- Configure the software-expected CRC value register FILTER0_1_CRC.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[2] to 1 to enable wake_up frame reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a wake-up frame is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

Magic Packet

To receive magic packets, the following configurations are required:

- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode, and set PMT_CTRL_STAUTS bit[1] to 1 to enable the magic packet reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a magic packet is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

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5.6 Register Summary

Table 5-3 describes GSF registers.

Table 5-3 Summary of GSF registers (base address: 0x1009_0000)

Offset Address	Register	Description	Page
0x00000000	STATION_ADDR_LOW	Local MAC address register	5-17
0x00000004	STATION_ADDR_HIGH	Local MAC address register	5-17
0x00000008	DUPLEX_SEL_RGMII	Half-duplex selection register	5-18
0x0000000C	FD_FC_TYPE	Flow control frame type domain register	5-18
0x00000014	COL_DISTANCE	Single retransmission packet length threshold register	5-19
0x0000001C	FC_TX_TIMER	Flow control time parameter register	5-19
0x00000020	FD_FC_ADDR_LOW	Flow control frame destination address register	5-19
0x00000024	FD_FC_ADDR_HIGH	Flow control frame destination address register	5-20
0x00000030	IPG_TX_TIMER	TX frame inter-packet gap (IPG) register	5-20
0x00000038	PAUSE_THR	TX flow control frame IPG register	5-21
0x0000003C	MAX_FRM_SIZE	Maximum frame length register	5-21
0x00000040	PORT_MODE	Port status register	5-22
0x00000044	PORT_EN	Channel enable register	5-22
0x00000048	PAUSE_EN	Flow control enable register	5-23
0x00000050	SHORT_RUNTS_THR	Short frame threshold register	5-23
0x00000054	DROP_UNK_CTL_FRM	Drop enable register for unknown control frames	5-24
0x00000060	TRANSMIT_CONTROL	Common configuration register	5-24
0x00000064	REC_FILT_CONTROL	RX frame filter control register	5-25
0x00000068	PORT_MC_ADDR_LOW	Multicast address register	5-26
0x0000006C	PORT_MC_ADDR_HIGH	Multicast address register	5-26
0x00000070	MAC_CLR	MAC clear register	5-27
0x00000080	RX_OCTETS_OK_CNT	Byte count register for valid RX frames	5-27

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Offset Address	Register	Description	Page
0x00000084	RX_OCTETS_BAD_CNT	Byte count register for error RX frames	5-28
0x00000088	RX_UC_PKTS	MAC frame count register for RX unicast frames	5-28
0x0000008C	RX_MC_PKTS	Frame count register for RX multicast frames	5-28
0x00000090	RX_BC_PKTS	Frame count register for RX broadcast frames	5-29
0x00000094	RX_PKTS_64OCTETS	Frame count register for RX 64-byte frames	5-29
0x00000098	RX_PKTS_65TO127OCTETS	Frame count register for RX frames ranging from 65 bytes to 127 bytes in length	5-29
0x0000009C	RX_PKTS_128TO255OCTETS	Frame count register for RX frames ranging from 128 bytes to 255 bytes in length	5-30
0x000000A0	RX_PKTS_255TO511OCTETS	Frame count register for RX frames ranging from 256 bytes to 511 bytes in length	5-30
0x000000A4	RX_PKTS_512TO1023OCTETS	Frame count register for RX frames ranging from 512 bytes to 1023 bytes in length	5-30
0x000000A8	RX_PKTS_1024TO1518OCTETS	Frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length	5-31
0x000000AC	RX_PKTS_1519TOMAXOCTETS	Frame count register for RX frames ranging from 1519 bytes to the maximum in length	5-31
0x000000B0	RX_FCS_ERRORS	Frame count register for RX frames with CRC errors	5-32
0x000000B4	RX_TAGGED	Frame count register for RX frames with tags	5-32
0x000000B8	RX_DATA_ERR	Frame count register for RX frames with data errors	5-32
0x000000BC	RX_ALIGN_ERRORS	Frame count register for RX frames with byte-alignment errors	5-33
0x000000C0	RX_LONG_ERRORS	Frame count register for RX oversized frames	5-33
0x000000C4	RX_JABBER_ERRORS	Frame count register for RX oversized frames	5-33

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Offset Address	Register	Description	Page
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	Frame count register for RX flow control frames	5-34
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	Frame count register for RX non-flow-control frames	5-34
0x000000D0	RX_VERY_LONG_ERR_CNT	Frame count register for RX long frames	5-35
0x000000D4	RX_RUNT_ERR_CNT	Frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length	5-35
0x000000D8	RX_SHORT_ERR_CNT	Frame count register for RX frames less than 96 bits in length	5-36
0x00000100	OCTETS_TRANSMITTED_OK	Byte count register for TX normal packets	5-36
0x00000104	OCTETS_TRANSMITTED_BAD	Byte count register for TX bad packets	5-36
0x00000108	TX_UC_PKTS	Frame count register for TX unicast frames	5-37
0x0000010C	TX_MC_PKTS	Frame count register for TX multicast frames	5-37
0x00000110	TX_BC_PKTS	Frame count register for TX broadcast frames	5-37
0x00000114	TX_PKTS_64OCTETS	Frame count register for TX 64-byte frames	5-38
0x00000118	TX_PKTS_65TO127OCTETS	Frame count register for TX frames ranging from 65 bytes to 127 bytes in length	5-38
0x0000011C	TX_PKTS_128TO255OCTETS	Frame count register for TX frames ranging from 128 bytes to 255 bytes in length	5-39
0x00000120	TX_PKTS_255TO511OCTETS	Frame count register for TX frames ranging from 256 bytes to 511 bytes in length	5-39
0x00000124	TX_PKTS_512TO1023OCTETS	Frame count register for TX frames ranging from 512 bytes to 1023 bytes in length	5-40
0x00000128	TX_PKTS_1024TO1518OCTETS	Frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length	5-40

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Offset Address	Register	Description	Page
0x0000012C	TX_PKTS_1519TOMAXOCTETS	Frame count register for TX frames greater than 1519 bytes in length	5-41
0x00000144	TX_EXC_COL_ERR_CNT	Count register for packets whose number reaches the maximum retransmission number threshold	5-41
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	Count register for transmission failures caused by oversized frames	5-42
0x00000150	TX_UNDERRUN	Count register for transmission failures caused by internal errors	5-42
0x00000154	TX_TAGGED	Frame count register for TX VLAN frames	5-43
0x00000158	TX_CRC_ERROR	Frame count register for TX frames with valid lengths and CRC errors	5-43
0x0000015C	TX_PAUSE_FRAMES	Frame count register for TX PAUSE frames	5-43
0x000001A8	LINE_LOOP_BACK	Loopback register on the MAC line side	5-44
0x000001B0	CF_CRC_STRIP	CRC strip enable register	5-44
0x000001B4	MODE_CHANGE_EN	Port mode change enable register	5-45
0x000001C0	COL_SLOT_TIME	Count register for half-duplex collision retransmission intervals	5-45
0x000001DC	LOOP_REG	Loopback supplement register	5-46
0x000001E0	RECV_CONTROL	RX control register	5-46
0x000001E8	VLAN_CODE	VLAN code register	5-47
0x000001EC	RX_OVERRUN_CNT	FIFO overrun count register	5-47
0x000001F4	RX_LENGTHFIELD_ERR_CNT	Frame count register for RX frames containing PADs	5-47
0x000001F8	RX_FAIL_COMMA_CNT	COMMA count register for byte delimitation	5-48
0x00000200	MAC_SA_ADDR_L	Source MAC address register	5-48
0x00000204	MAC_SA_ADDR_H	Source MAC address register	5-49
0x00000208	MAC_DA_ADDR_L	Destination MAC address register	5-49
0x0000020C	MAC_DA_ADDR_H	Destination MAC address register	5-49
0x00000210	CRF_MIN_PACKET	Minimum filter packet length register	5-50
0x00000214	CONTROL_WORD	Control register	5-50

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Offset Address	Register	Description	Page
0x00000218	FLOW_CTRL_PKG_THRSLD	Flow control packet count register	5-52
0x0000021C	CRF_FLOW_TIME_THRSLD	Flow control time register	5-52
0x00000220+4*m	FILTER_LISTm (m ranging from 0 to 15)	Filter list register	5-53
0x00000260	CRF_UDP_NO	UDP port number register	5-53
0x00000264	CRF_TX_FIFO_THRSLD	TX FIFO threshold register	5-54
0x00000268	CRF_RX_FIFO_THRSLD	RX FIFO threshold register	5-54
0x00000280	ERR_GIVEN_PKG_CNT	Count register for dropped packets caused by the frame tailors marked as errors	5-55
0x00000284	SHORT_ERR_PKT_CNT	Short error packet count register	5-55
0x00000288	ERR_FRM_TYPE_CNT	Count register for dropped packets caused by the frame types not listed in the filter list	5-56
0x0000028C	ERR_IP_TYPE_CNT	Count register for dropped packets caused by the IP types not listed in the filter list	5-56
0x00000290	ERR_UDP_CNT	Count register for filtered packets caused by UDP port numbers beyond the specified range	5-57
0x00000294	OVER_FLOW_CNT	Count register for dropped packets caused by the full RX FIFO	5-57
0x00000298	OVER_LENGTH_CNT	Count register for dropped packets whose sizes exceed the upper threshold of the PMU	5-57
0x000002A4	RX_PAUSE_EN	Flow control frame enable register in the RX direction	5-58
0x000002A8	CRF_CFF_DATA_NUM	Configuration FIFO data count register	5-58
0x000002AC	FLOW_OUT_IP_CNT	Count register for dropped IP packets caused by flow control	5-59
0x000002B0	FLOW_OUT_CTRL_CNT	Count register for dropped control packets caused by flow control	5-59
0x00000340	CRF_TX_PAUSE	TX flow control frame control register	5-60

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Offset Address	Register	Description	Page
0x00000344	CRF_RX_LEFT_NUM	Flow control RX address count register	5-60
0x00000348	CRF_CTRL_0_TYPE	Control packet type 0 register	5-61
0x0000034C	CRF_CTRL_1_TYPE	Control packet type 1 register	5-61
0x00000350	CRF_CTRL_2_TYPE	Control packet type 2 register	5-61
0x00000354	CRF_CTRL_3_TYPE	Control packet type 3 register	5-62
0x00000358	CRF_BM_PKT_THRSLD	Count threshold register for broadcast/multicast packets under flow control	5-62
0x0000035C	CRF_BM_TIME_THRSLD	Flow control time threshold register for broadcast and multicast packets	5-63
0x000003C0	MDIO_SINGLE_CMD	MDIO single operation register	5-63
0x000003C4	MDIO_SINGLE_DATA	MDIO read/write data register	5-64
0x000003CC	MDIO_CTL	MDIO control register	5-64
0x000003D0	MDIO_RDATA_STATUS	MDIO read data status register	5-66
0x00000500	RX_FQ_START_ADDR	Start address register for the idle descriptor queue	5-66
0x00000504	RX_FQ_DEPTH	Depth register for the idle descriptor queue	5-66
0x00000508	RX_FQ_WR_ADDR	Write address register for the idle descriptor queue	5-67
0x0000050C	RX_FQ_RD_ADDR	Read address register for the idle descriptor queue	5-68
0x00000510	RX_FQ_VLDDESC_CNT	Valid descriptor number register for the idle descriptor queue	5-68
0x00000514	RX_FQ_ALRMPTY_TH	Almost-empty threshold register for the idle descriptor queue	5-69
0x00000518	RX_FQ_REG_EN	Enable register related to idle descriptor queue in the RX direction	5-69
0x0000051C	RX_FQ_ALFULL_TH	Almost-full threshold register for the idle descriptor queue	5-70
0x00000520	RX_BQ_START_ADDR	Start address register for the rx_buff descriptor queue	5-70
0x00000524	RX_BQ_DEPTH	Depth register for the rx_buff descriptor queue	5-71

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Offset Address	Register	Description	Page
0x00000528	RX_BQ_WR_ADDR	Write address register for the rx_buff descriptor queue	5-72
0x0000052C	RX_BQ_RD_ADDR	Read address register for the rx_buff descriptor queue	5-72
0x00000530	RX_BQ_FREE_DESC_CNT	Writable descriptor count register for the rx_buff descriptor queue	5-73
0x00000534	RX_BQ_ALEMPTY_TH	Almost-empty threshold register for the rx_buff descriptor queue	5-73
0x00000538	RX_BQ_REG_EN	Enable register related to rx_buff descriptor queue	5-74
0x0000053C	RX_BQ_ALFULL_TH	Almost-full threshold register for the rx_buff descriptor queue	5-75
0x00000580	TX_BQ_START_ADDR	Start address register for the tx_buff descriptor queue	5-75
0x00000584	TX_BQ_DEPTH	Depth register for the tx_buff descriptor queue	5-76
0x00000588	TX_BQ_WR_ADDR	Write address register for the tx_buff descriptor queue	5-76
0x0000058C	TX_BQ_RD_ADDR	Read address register for the tx_buff descriptor queue	5-77
0x00000590	TX_BQ_VLDDESC_CNT	Valid descriptor number register for the tx_buff descriptor queue	5-77
0x00000594	TX_BQ_ALEMPTY_TH	Almost-empty threshold register for the tx_buff descriptor queue	5-78
0x00000598	TX_BQ_REG_EN	Enable register related to tx_buff descriptor queue	5-78
0x0000059C	BQ1_ALFULL_TH	Almost-full threshold register for the tx_buff descriptor queue	5-79
0x000005A0	TX_RQ_START_ADDR	Start address register for the tx_rq descriptor queue	5-79
0x000005A4	TX_RQ_DEPTH	Depth register for the tx_rq descriptor queue	5-80
0x000005A8	TX_RQ_WR_ADDR	Write address register for the tx_rq descriptor queue	5-80
0x000005AC	TX_RQ_RD_ADDR	Read address register for the tx_rq descriptor queue	5-80
0x000005B0	TX_RQ_FREE_DESC_CNT	Writable descriptor count register for the tx_rq descriptor queue	5-81

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Offset Address	Register	Description	Page
0x000005B4	TX_RQ_ALEMPTY_TH	Almost-empty threshold register for the tx_rq descriptor queue	5-81
0x000005B8	TX_RQ_REG_EN	Enable register related to the tx_rq descriptor queue	5-82
0x000005BC	TX_RQ_ALFULL_TH	Almost-full threshold register for the tx_rq descriptor queue	5-83
0x000005C0	RAW_PMU_INT	PMU raw interrupt register	5-83
0x000005C4	ENA_PMU_INT	PMU raw interrupt register	5-86
0x000005C8	STATUS_PMU_INT	PMU interrupt status register	5-90
0x000005CC	DESC_WR_RD_ENA	cff read/write descriptor enable register	5-93
0x000005D8	IN_QUEUE_TH	rx_bq or tx_rq enqueue interrupt threshold register	5-94
0x000005DC	OUT_QUEUE_TH	rx_fq or tx_bq dequeue interrupt threshold register	5-94
0x000005E0	RX_BQ_IN_TIMEOUT_TH	rx_bq enqueue timeout raw interrupt threshold register	5-95
0x000005E4	TX_RQ_IN_TIMEOUT_TH	tx_rq enqueue timeout raw interrupt threshold register	5-95
0x000005E8	STOP_CMD	RX and TX packet control stop register	5-96
0x000005EC	FLUSH_CMD	Recycle descriptor enable register	5-96
0x00000800	U_EEE_INTR_SRC	LPI status register in the RX and TX directions	5-97
0x00000804	U_EEE_INTR_EN	Interrupt mask and enable register in the RX and TX directions	5-98
0x00000808	U_EEE_ENABLE	EEE enable signal register	5-100
0x0000080C	U_EEE_TIMER	LPI time threshold register	5-101
0x00000810	U_EEE_LINK_STATUS	EEE status register	5-101
0x00000814	U_EEE_TIME_CLK_CNT	Timing pulse count register	5-102
0x00000A00	PMT_CTRL_STAUTS	PMT control and status register	5-102
0x00000A04	FILTER_0_BYTE_MASK	PMT valid byte selection register 0	5-104
0x00000A08	FILTER_1_BYTE_MASK	PMT valid byte selection register 1	5-104
0x00000A0C	FILTER_2_BYTE_MASK	PMT valid byte selection register 2	5-105
0x00000A10	FILTER_3_BYTE_MASK	PMT valid byte selection register 3	5-105

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Offset Address	Register	Description	Page
0x00000A14	FILTER_COMMAND	PMT template selection and multicast enable register	5-106
0x00000A18	FILTER_OFFSET	CRC position offset register	5-107
0x00000A1C	FILTER0_1_CRC	Software-expected CRC value 0 and 1 register	5-108
0x00000A20	FILTER2_3_CRC	Software-expected CRC value 2 and 3 register	5-108

5.7 Register Description

STATION_ADDR_LOW

STATION_ADDR_LOW is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000000	STATION_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	station_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	station_addr_low	Lower 32 bits for the source MAC address of MAC_CORE

STATION_ADDR_HIGH

STATION_ADDR_HIGH is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000004	STATION_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																station_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

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[15:0]	RW	station_addr_high	Upper 16 bits of the source MAC address of MAC_CORE. The default configurations can be used.

DUPLEX_SEL_RGMII

DUPLEX_SEL_RGMII is a half-duplex selection register.

Offset Address	Register Name	Total Reset Value
0x00000008	DUPLEX_SEL_RGMII	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															duplex_sel_rgmii
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	duplex_sel_rgmii	Half-duplex selection signal 0: half duplex 1: full duplex

FD_FC_TYPE

FD_FC_TYPE is a flow control frame type domain register.

Offset Address	Register Name	Total Reset Value
0x0000000C	FD_FC_TYPE	0x0000_8808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_fc_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_type	Flow control frame type domain in full-duplex mode

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COL_DISTANCE

COL_DISTANCE is a single retransmission packet length threshold register.

Offset Address	Register Name	Total Reset Value
0x00000014	COL_DISTANCE	0x0000_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						col_distance									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	col_distance	Single retransmission packet length threshold

FC_TX_TIMER

FC_TX_TIMER is a flow control time parameter register.

Offset Address	Register Name	Total Reset Value
0x0000001C	FC_TX_TIMER	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fc_tx_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fc_tx_timer	Parameter of the time period during which flow control frames are transmitted. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

FD_FC_ADDR_LOW

FD_FC_ADDR_LOW is a flow control frame destination address register.

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Offset Address	Register Name	Total Reset Value
0x00000020	FD_FC_ADDR_LOW	0xC200_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fd_fc_addr_low																															
Reset	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:0]	RW	fd_fc_addr_low	Lower 32 bits of the destination address of the flow control frame

FD_FC_ADDR_HIGH

FD_FC_ADDR_HIGH is a flow control frame destination address register.

Offset Address	Register Name	Total Reset Value
0x00000024	FD_FC_ADDR_HIGH	0x0000_0180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_fc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_addr_high	Upper 16 bits of the destination address of the flow control frame

IPG_TX_TIMER

IPG_TX_TIMER is a TX frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000030	IPG_TX_TIMER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ipg_tx_timer							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ipg_tx_timer	TX frame IPG, in the unit of byte

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PAUSE_THR

PAUSE_THR is a TX flow control frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000038	PAUSE_THR	0x0000_002F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pause_thr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	pause_thr	IPG of the flow control frame. If the flow control time is longer than the IPG, the MAC transmits the flow control frame automatically. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

MAX_FRM_SIZE

MAX_FRM_SIZE is a maximum frame length register.

Offset Address	Register Name	Total Reset Value
0x0000003C	MAX_FRM_SIZE	0x0000_05EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_frm_size											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	max_frm_size	Maximum frame length on the MAC side If the length of an RX frame is greater than the maximum length, the RX frame is regarded as an oversized frame. When the length of a frame to be transmitted is greater than the maximum length, the frame is broken up and then transmitted as an error frame.

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PORT_MODE

PORT_MODE is a port status register.

Offset Address	Register Name	Total Reset Value
0x00000040	PORT_MODE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													port_mode		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	port_mode	Current MAC port mode 000: 10 Mbit/s 001: 100 Mbit/s 101: 1000 Mbit/s Other values: reserved

PORT_EN

PORT_EN is a channel enable register.

Offset Address	Register Name	Total Reset Value
0x00000044	PORT_EN	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx en	rx en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_en	TX channel enable 0: disabled 1: enabled
[1]	RW	rx_en	RX channel enable 0: disabled 1: enabled

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[0]	RO	reserved	Reserved

PAUSE_EN

PAUSE_EN is a flow control enable register.

Offset Address	Register Name	Total Reset Value
0x00000048	PAUSE_EN	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx fdfc	rx fdfc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_fdfc	Flow control frame transmit enable in full-duplex mode 0: disabled 1: enabled
[0]	RW	rx_fdfc	Flow control frame response enable in full-duplex mode 0: disabled 1: enabled

SHORT_RUNTS_THR

SHORT_RUNTS_THR is a short frame threshold register.

Offset Address	Register Name	Total Reset Value
0x00000050	SHORT_RUNTS_THR	0x0000_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												short_runts_thr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	short_runts_thr	Short frame threshold (for statistics only)

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DROP_UNK_CTL_FRM

DROP_UNK_CTL_FRM is a drop enable register for unknown control frames.

Offset Address	Register Name	Total Reset Value
0x00000054	DROP_UNK_CTL_FRM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															drop_unk_ctl_frm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	drop_unk_ctl_frm	Processing method of the unknown control frames 0: The unknown control frames are forwarded normally. 1: The unknown control frames are dropped.

TRANSMIT_CONTROL

TRANSMIT_CONTROL is a common configuration register.

Offset Address	Register Name	Total Reset Value
0x00000060	TRANSMIT_CONTROL	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pad_enable	crc_add	reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pad_enable	PAD addition enable 0: disabled 1: enabled
[6]	RW	crc_add	FCS addition enable 0: enabled 1: disabled

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[5:0]	RO	reserved	Reserved

REC_FILT_CONTROL

REC_FILT_CONTROL is an RX frame filter control register.

Offset Address	Register Name	Total Reset Value
0x00000064	REC_FILT_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										crc_err_pass	pause_frm_pass	vlan_drop_en	bc_drop_en	mc_match_en	uc_match_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	crc_err_pass	CRC error frame filter enable 0: disabled 1: enabled
[4]	RW	pause_frm_pass	Flow control frame filter enable 0: disabled. This bit takes effect only when flow control is enabled, which is transmitted to the software. 1: enabled. This bit takes effect only when flow control is enabled, which is not transmitted to the software.
[3]	RW	vlan_drop_en	VLAN frame filter enable 0: disabled 1: enabled
[2]	RW	bc_drop_en	Broadcast frame filter enable 0: disabled 1: enabled
[1]	RW	mc_match_en	Multicast frame enable with unmatched DA filter 0: disabled 1: enabled
[0]	RW	uc_match_en	Unicast frame enable with unmatched DA filter 0: disabled 1: enabled

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PORT_MC_ADDR_LOW

PORT_MC_ADDR_LOW is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x00000068	PORT_MC_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_mc_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_mc_addr_low	Lower 32 bits of the multicast address, used to check whether the multicast frames match

PORT_MC_ADDR_HIGH

PORT_MC_ADDR_HIGH is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x0000006C	PORT_MC_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																port_mc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	port_mc_addr_high	Upper 16 bits of the multicast address, used to check whether the multicast frames match

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MAC_CLR

MAC_CLR is a MAC clear register.

Offset Address	Register Name	Total Reset Value
0x00000070	MAC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												soft_rst_mdio	soft_rst_mii	soft_rst_rx	soft_rst_tx
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	soft_rst_mdio	MDIO clear signal 0: invalid 1: valid
[2]	RW	soft_rst_mii	MII clear signal 0: invalid 1: valid
[1]	RW	soft_rst_rx	RX clear signal 0: invalid 1: valid
[0]	RW	soft_rst_tx	TX clear signal 0: invalid 1: valid

RX_OCTETS_OK_CNT

RX_OCTETS_OK_CNT is a byte count register for valid RX frames.

Offset Address	Register Name	Total Reset Value
0x00000080	RX_OCTETS_OK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_ok_cnt	Count of bytes of the valid RX frames, ranging from DA to FCS

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RX_OCTETS_BAD_CNT

RX_OCTETS_BAD_CNT is a byte count register for error RX frames.

Offset Address	Register Name	Total Reset Value
0x00000084	RX_OCTETS_BAD_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_bad_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_bad_cnt	Count of bytes of the frames with CRC errors and alignment errors

RX_UC_PKTS

RX_UC_PKTS is a MAC frame count register for RX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000088	RX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_uc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_uc_pkts_cnt	Count of RX unicast frames, excluding bad frames

RX_MC_PKTS

RX_MC_PKTS is a frame count register for RX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000008C	RX_MC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_mc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_mc_pkts_cnt	Count of RX multicast frames, excluding bad frames

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RX_BC_PKTS

RX_BC_PKTS is a frame count register for RX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000090	RX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_bc_pkts_cnt	Count of RX broadcast frames, excluding bad frames

RX_PKTS_64OCTETS

RX_PKTS_64OCTETS is a frame count register for RX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000094	RX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_64oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_64oct_cnt	Count of RX 64-byte frames, including bad frames

RX_PKTS_65TO127OCTETS

RX_PKTS_65TO127OCTETS is a frame count register for RX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000098	RX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_65to127_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_65to127_oct_cnt	Count of RX frames ranging from 65 bytes to 127 bytes in length, including bad frames

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RX_PKTS_128TO255OCTETS

RX_PKTS_128TO255OCTETS is a frame count register for RX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000009C	RX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_128to255_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_128to255_oct_cnt	Count of RX frames ranging from 128 bytes to 255 bytes in length, including bad frames

RX_PKTS_255TO511OCTETS

RX_PKTS_255TO511OCTETS is a frame count register for RX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A0	RX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_256to511_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_256to511_oct_cnt	Count of RX frames ranging from 256 bytes to 511 bytes in length, including bad frames

RX_PKTS_512TO1023OCTETS

RX_PKTS_512TO1023OCTETS is a frame count register for RX frames ranging from 512 bytes to 1023 bytes in length.

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Offset Address	Register Name	Total Reset Value
0x000000A4	RX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_512to1023_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_512to1023_oct_cnt	Count of RX frames ranging from 512 bytes to 1023 bytes in length, including bad frames

RX_PKTS_1024TO1518OCTETS

RX_PKTS_1024TO1518OCTETS is a frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A8	RX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1024to1518_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1024to1518_oct_cnt	Count of RX frames ranging from 1024 bytes to 1518 bytes in length, including bad frames

RX_PKTS_1519TOMAXOCTETS

RX_PKTS_1519TOMAXOCTETS is a frame count register for RX frames ranging from 1519 bytes to the maximum in length.

Offset Address	Register Name	Total Reset Value
0x000000AC	RX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1519tomax_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1519tomax_oct_cnt	Count of RX frames ranging from 1519 bytes to the maximum in length, including bad frames

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RX_FCS_ERRORS

RX_FCS_ERRORS is a frame count register for RX frames with CRC errors.

Offset Address	Register Name	Total Reset Value
0x000000B0	RX_FCS_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fcs_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fcs_errors	Count of RX frames with CRC errors, excluding short frames

RX_TAGGED

RX_TAGGED is a frame count register for RX frames with tags.

Offset Address	Register Name	Total Reset Value
0x000000B4	RX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_tagged	Count of RX frames with tags

RX_DATA_ERR

RX_DATA_ERR is a frame count register for RX frames with data errors.

Offset Address	Register Name	Total Reset Value
0x000000B8	RX_DATA_ERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_data_err																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_data_err	Count of RX frames with data errors

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RX_ALIGN_ERRORS

RX_ALIGN_ERRORS is a frame count register for RX frames with byte-alignment errors.

Offset Address	Register Name	Total Reset Value
0x000000BC	RX_ALIGN_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_align_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_align_errors	Count of RX frames with byte-alignment errors

RX_LONG_ERRORS

RX_LONG_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C0	RX_LONG_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_long_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_long_errors	Count of RX oversized frames (without CRC errors)

RX_JABBER_ERRORS

RX_JABBER_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C4	RX_JABBER_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_jabber_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_jabber_errors	Count of RX oversized frames with CRC errors or non-integer byte count

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RX_PAUSE_MACCONTROL_FRAMCOUNTER

RX_PAUSE_MACCONTROL_FRAMCOUNTER is a frame count register for RX flow control frames.

Offset Address	Register Name	Total Reset Value
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pause_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pause_maccontrol_framecounter	Count of RX flow control frames. The CRC must be correct when it is valid.

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER is a frame count register for RX non-flow-control frames.

Offset Address	Register Name	Total Reset Value
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_unknown_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_unknown_maccontrol_framecounter	Count of RX non-flow control frames

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RX_VERY_LONG_ERR_CNT

RX_VERY_LONG_ERR_CNT is a frame count register for RX long frames.

Offset Address	Register Name	Total Reset Value
0x000000D0	RX_VERY_LONG_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_very_long_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_very_long_err_cnt	Count of RX long frames (with the length more than twice the maximum frame length)

RX_RUNT_ERR_CNT

RX_RUNT_ERR_CNT is a frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D4	RX_RUNT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_runt_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_runt_err_cnt	Count of RX frames less than 64 bytes but greater than or equal to 12 bytes in length

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RX_SHORT_ERR_CNT

RX_SHORT_ERR_CNT is a frame count register for RX frames less than 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D8	RX_SHORT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_short_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_short_err_cnt	Count of RX frames less than 12 bytes in length.

OCTETS_TRANSMITTED_OK

OCTETS_TRANSMITTED_OK is a byte count register for TX normal packets.

Offset Address	Register Name	Total Reset Value
0x00000100	OCTETS_TRANSMITTED_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_ok	Count of bytes of the transmitted normal packets, excluding the preambles and SFDs

OCTETS_TRANSMITTED_BAD

OCTETS_TRANSMITTED_BAD is a byte count register for TX bad packets.

Offset Address	Register Name	Total Reset Value
0x00000104	OCTETS_TRANSMITTED_BAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_bad																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_bad	Count of bytes of the TX bad packets

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TX_UC_PKTS

TX_UC_PKTS is a frame count register for TX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000108	TX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_uc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_uc_pkts	Count of TX unicast frames, excluding bad packets

TX_MC_PKTS

TX_MC_PKTS is a frame count register for TX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000010C	TX_MC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_mc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_mc_pkts	Count of TX multicast frames, excluding bad packets

TX_BC_PKTS

TX_BC_PKTS is a frame count register for TX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000110	TX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_bc_pkts	Count of TX broadcast frames, excluding bad packets

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TX_PKTS_64OCTETS

TX_PKTS_64OCTETS is a frame count register for TX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000114	TX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_64octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_64octets	Count of TX 64-byte frames, including bad packets

TX_PKTS_65TO127OCTETS

TX_PKTS_65TO127OCTETS is a frame count register for TX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000118	TX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_65to127octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_65to127octets	Count of TX frames ranging from 65 bytes to 127 bytes in length, including bad packets

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TX_PKTS_128TO255OCTETS

TX_PKTS_128TO255OCTETS is a frame count register for TX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000011C	TX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_128to255octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_128to255octets	Count of TX frames ranging from 128 bytes to 255 bytes in length, including bad packets

TX_PKTS_255TO511OCTETS

TX_PKTS_255TO511OCTETS is a frame count register for TX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000120	TX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_256to511octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_256to511octets	Count of TX frames ranging from 256 bytes to 511 bytes in length, including bad packets

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TX_PKTS_512TO1023OCTETS

TX_PKTS_512TO1023OCTETS is a frame count register for TX frames ranging from 512 bytes to 1023 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000124	TX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_512to1023octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_512to1023octets	Count of TX frames ranging from 512 bytes to 1023 bytes in length, including bad packets

TX_PKTS_1024TO1518OCTETS

TX_PKTS_1024TO1518OCTETS is a frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000128	TX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1024to1518octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1024to1518octets	Count of TX frames ranging from 1024 bytes to 1518 bytes in length, including bad packets

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TX_PKTS_1519TOMAXOCTETS

TX_PKTS_1519TOMAXOCTETS is a frame count register for TX frames greater than 1519 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000012C	TX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1519tomaxoctes																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1519tomaxoctes	Count of TX frames greater than 1519 bytes in length, including bad packets

TX_EXC_COL_ERR_CNT

TX_EXC_COL_ERR_CNT is a count register for packets whose number reaches the maximum retransmission number threshold.

Offset Address	Register Name	Total Reset Value
0x00000144	TX_EXC_COL_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_exc_col_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_exc_col_err_cnt	Count of packets whose number reaches the maximum retransmission number threshold

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TX_EXCESSIVE_LENGTH_DROP

TX_EXCESSIVE_LENGTH_DROP is a count register for transmission failures caused by oversized frames.

Offset Address	Register Name	Total Reset Value
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_excessive_length_drop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_excessive_length_drop	Count of transmission failures caused by oversized frames

TX_UNDERRUN

TX_UNDERRUN is a count register for transmission failures caused by internal errors.

Offset Address	Register Name	Total Reset Value
0x00000150	TX_UNDERRUN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_underrun																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_underrun	Count of transmission failures caused by internal errors

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TX_TAGGED

TX_TAGGED is a frame count register for TX VLAN frames.

Offset Address	Register Name	Total Reset Value
0x00000154	TX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_tagged	Count of TX VLAN frames The value of the Type field equals to that of the 0x8100 packet.

TX_CRC_ERROR

TX_CRC_ERROR is a frame count register for TX frames with valid lengths and CRC errors.

Offset Address	Register Name	Total Reset Value
0x00000158	TX_CRC_ERROR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_crc_error																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_crc_error	Count of TX frames with valid lengths and CRC errors

TX_PAUSE_FRAMES

TX_PAUSE_FRAMES is a frame count register for TX PAUSE frames.

Offset Address	Register Name	Total Reset Value
0x0000015C	TX_PAUSE_FRAMES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pause_frames																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pause_frames	Count of TX PAUSE frames

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LINE_LOOP_BACK

LINE_LOOP_BACK is a loopback register on the MAC line side.

Offset Address	Register Name	Total Reset Value
0x000001A8	LINE_LOOP_BACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															line_loop_back
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	line_loop_back	MAC line-side loopback enable 0: disabled 1: enabled

CF_CRC_STRIP

CF_CRC_STRIP is a CRC strip enable register.

Offset Address	Register Name	Total Reset Value
0x000001B0	CF_CRC_STRIP	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cf_crc_strip
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cf_crc_strip	RX CRC strip enable on the MAC side 0: disabled. The four bytes of the CRC are regarded as part of the packet. 1: enabled. The four bytes of the CRC are stripped from the packet.

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MODE_CHANGE_EN

MODE_CHANGE_EN is a port mode change enable register.

Offset Address	Register Name	Total Reset Value
0x000001B4	MODE_CHANGE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mode_change_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mode_change_en	port_mode change enable 0: disabled 1: enabled

COL_SLOT_TIME

COL_SLOT_TIME is a count register for half-duplex collision retransmission intervals.

Offset Address	Register Name	Total Reset Value
0x000001C0	COL_SLOT_TIME	0x0000_40FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cf2bc_slottime																cf2bc_random_seed							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RW	cf2bc_slottime	Interval for half-duplex collision retransmission
[7:0]	RW	cf2bc_random_seed	Random multiple radix for half-duplex collision retransmission

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LOOP_REG

LOOP_REG is a loopback supplement register.

Offset Address	Register Name	Total Reset Value
0x000001DC	LOOP_REG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cf_ext_drive_lp	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	cf_ext_drive_lp	Generation of the read/write enable signals of the MAC data during loopback on the line side 0: The read/write enable signals are generated in the MAC. 1: The read/write enable signals are generated based on the MAC enable signals read by the downlink FIFO.
[0]	RO	reserved	Reserved

RECV_CONTROL

RECV_CONTROL is an RX control register.

Offset Address	Register Name	Total Reset Value
0x000001E0	RECV_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											runt_pkt_en	strip_pad_en	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

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[4]	RW	runt_pkt_en	Transparent transmission enable of the RX short frames 0: discarded and not transmitted to the software 1: transmitted to the software
[3]	RW	strip_pad_en	PAD for stripping RX frames enable 0: disabled 1: enabled
[2:0]	RO	reserved	Reserved

VLAN_CODE

VLAN_CODE is a VLAN code register.

Offset Address	Register Name	Total Reset Value
0x000001E8	VLAN_CODE	0x0000_8100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cf_vlan_code															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	cf_vlan_code	Ethernet Type field configuration

RX_OVERRUN_CNT

RX_OVERRUN_CNT is a FIFO overrun count register.

Offset Address	Register Name	Total Reset Value
0x000001EC	RX_OVERRUN_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_overrun_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_overrun_cnt	Count of FIFO overruns on the MAC application side

RX_LENGTHFIELD_ERR_CNT

RX_LENGTHFIELD_ERR_CNT is a frame count register for RX frames containing PADs.

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Offset Address	Register Name	Total Reset Value
0x000001F4	RX_LENGTHFIELD_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_lengthfield_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_lengthfield_err_cnt	Count of RX frames containing PADs and with the length of not 64 bytes when the PAD strip enable is valid

RX_FAIL_COMMA_CNT

RX_FAIL_COMMA_CNT is a COMMA count register for byte delimitation.

Offset Address	Register Name	Total Reset Value
0x000001F8	RX_FAIL_COMMA_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fail_comma_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fail_comma_cnt	Count of COMMA codes when two or more COMMA codes exist during byte delimitation

MAC_SA_ADDR_L

MAC_SA_ADDR_L is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000200	MAC_SA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_sa_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_sa_addr_l	Lower 32 bits of the source MAC address used by the PMU, which are inserted into the lower 32 bits of the source address (SA) field

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MAC_SA_ADDR_H

MAC_SA_ADDR_H is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000204	MAC_SA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mac_sa_addr_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	mac_sa_addr_h	Upper 16 bits of the source MAC address used by the PMU

MAC_DA_ADDR_L

MAC_DA_ADDR_L is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000208	MAC_DA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_da_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_da_addr_l	Lower 32 bits of the destination MAC address used by the PMU, which are inserted into the lower 32 bits of the destination address field

MAC_DA_ADDR_H

MAC_DA_ADDR_H is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x0000020C	MAC_DA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_tx_max_packet												mac_da_addr_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

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[26:16]	RW	crf_tx_max_packet	Maximum length of the normal and SG packets allowed by the PMU
[15:0]	RW	mac_da_addr_h	Upper 16 bits of the destination MAC address used by the PMU

CRF_MIN_PACKET

CRF_MIN_PACKET is a minimum filter packet length register.

Offset Address	Register Name	Total Reset Value
0x00000210	CRF_MIN_PACKET	0x0000_0F2A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tso_version												reserved						crf_tx_min_packet						reserved		crf_rx_min_packet					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:20]	RO	tso_version	TSO version 100: single-byte combination version 200: SG or COE version 300: TSO version
[19:14]	RO	reserved	Reserved
[13:8]	RW	crf_tx_min_packet	Minimum length of the TX packet. The default length is 15 bytes.
[7:6]	RO	reserved	Reserved
[5:0]	RW	crf_rx_min_packet	Minimum length of the RX packet. The default length is 42 bytes.

CONTROL_WORD

CONTROL_WORD is a control register.

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Offset Address	Register Name	Total Reset Value
0x00000214	CONTROL_WORD	0x00C0_0640

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						crf_tx_standard	reserved			crf_ip_flow_ctrl	crf_ctrl_flow_ctrl	reserved		crf_filt_unused_pkg	crf_bm_flow_ctrl	crf_peel_dsa	crf_add_da_sa	crf_large_packet													
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	crf_tx_standard	Configuration standard for the transmit waterline of the TX FIFO 0: The standard is set based on the packet and empty threshold. If the TX FIFO contains a complete packet or the number of valid data items in the TX FIFO is equal to or greater than the threshold multiplied by 4, a read request is sent to the MAC. 1: The standard is set based on the packet. If the TX FIFO contains a complete packet, a read request is sent to the MAC.
[24:22]	RO	reserved	Reserved
[21]	RW	crf_ip_flow_ctrl	IP packet flow control enable 0: disabled 1: enabled
[20]	RW	crf_ctrl_flow_ctrl	Control packet flow control enable 0: disabled 1: enabled
[19:18]	RO	reserved	Reserved
[17]	RW	crf_filt_unused_pkg	Invalid packets filter enable 0: disabled 1: enabled
[16]	RW	crf_bm_flow_ctrl	Multicast/broadcast packet flow control enable 0: disabled 1: enabled
[15]	RW	crf_peel_dsa	DA/SA stripping control enable 0: disabled 1: enabled

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[14]	RW	crf_add_da_sa	DA/SA addition control enable 0: disabled 1: enable
[13:0]	RW	crf_large_packet	Maximum length configured for packets. The default length is 1600 bytes (maximum length of packets used by the PMU).

FLOW_CTRL_PKG_THRSLD

FLOW_CTRL_PKG_THRSLD is a flow control packet number threshold register.

Offset Address	Register Name	Total Reset Value
0x00000218	FLOW_CTRL_PKG_THRSLD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_ip_pkg_thrsld																crf_ctrl_pkg_thrsld															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	crf_ip_pkg_thrsld	Upper threshold of the number of IP packets. When the number of IP packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.
[15:0]	RW	crf_ctrl_pkg_thrsld	Upper threshold of the number of control packets. When the number of control packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.

CRF_FLOW_TIME_THRSLD

CRF_FLOW_TIME_THRSLD is a flow control time register.

Offset Address	Register Name	Total Reset Value
0x0000021C	CRF_FLOW_TIME_THRSLD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_flow_time_thrsld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_flow_time_thrsld	Flow control time, measured by 125 μs Flow control time T = (crf_flow_time_thrsld + 1) x 125 μs

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FILTER_LISTm

FILTER_LISTm (*m* ranging from 0 to 15) is a filter list register.

Offset Address	Register Name	Total Reset Value
0x00000220 + 4 x m	FILTER_LISTm	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														crf_filt_cfg0	crf_filt_id0	crf_filt_frm_type0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	crf_filt_cfg0	Configured row or not 0: not configured 1: configured The content of this list needs to be parsed only when crf_filt_cfg is set to 1. Otherwise, the content of this list can be ignored.
[16]	RW	crf_filt_id0	Type of the list 0: MAC frame 1: IP
[15:0]	RW	crf_filt_frm_type0	Configured filter type When the ID is 0, 16 bits of crf_filt_frm_type are valid. When the ID is 1, the lower 8 bits of crf_filt_frm_type are valid, and the upper 8 bits are ignored.

CRF_UDP_NO

CRF_UDP_NO is a UDP port number register.

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Offset Address	Register Name	Total Reset Value
0x00000260	CRF_UDP_NO	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_udp_max_no																reserved															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_udp_max_no	Maximum number of the UDP ports
[15:0]	RO	reserved	Reserved

CRF_TX_FIFO_THRSLD

CRF_TX_FIFO_THRSLD is a TX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x00000264	CRF_TX_FIFO_THRSLD	0x0271_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								crf_tx_p_full_th								reserved				crf_tx_p_empty_th											
Reset	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	crf_tx_p_full_th	Upper threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, packets are not transferred from the SDRAM. After the threshold is set, the TX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD bit[13:0] < 8192 – 4(crf_tx_p_full_th)
[15:11]	RO	reserved	Reserved
[10:0]	RW	crf_tx_p_empty_th	Lower threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, data can be read from the FX FIFO. It is recommended that this threshold be set to 0x14.

CRF_RX_FIFO_THRSLD

CRF_RX_FIFO_THRSLD is an RX FIFO threshold register.

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Offset Address	Register Name	Total Reset Value
0x00000268	CRF_RX_FIFO_THRSLD	0x0E10_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_rx_p_full_th												reserved				crf_rx_p_empty_th											
Reset	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	crf_rx_p_full_th	Upper threshold of the RX FIFO When the number of valid data packets in the RX FIFO quadruples crf_rx_p_full_th, new packets are not written to the RX FIFO. After the threshold is set, the RX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD[13:0] < (8192 – 4(crf_rx_p_full_th)
[15:12]	RO	reserved	Reserved
[11:0]	RW	crf_rx_p_empty_th	Lower threshold of the RX FIFO. When the number of valid data packets in the RX FIFO quadruples crf_rx_p_empty_th, data can be read from the RX FIFO. This threshold must be set to 0x200 at least.

ERR_GIVEN_PKG_CNT

ERR_GIVEN_PKG_CNT is a count register for dropped packets caused by the frame tailors marked as errors.

Offset Address	Register Name	Total Reset Value
0x00000280	ERR_GIVEN_PKG_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_given_pkg_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_given_pkg_cnt	Count of dropped packets caused by the frame tailors marked as errors

SHORT_ERR_PKT_CNT

SHORT_ERR_PKT_CNT is a short error packet count register.

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Offset Address	Register Name	Total Reset Value
0x00000284	SHORT_ERR_PKT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	short_err_pkt_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	short_err_pkt_cnt	Count of short error packets

ERR_FRM_TYPE_CNT

ERR_FRM_TYPE_CNT is a count register for dropped packets caused by the frame types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x00000288	ERR_FRM_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_frm_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_frm_type_cnt	Count of dropped packets caused by the frame types not listed in the filter list

ERR_IP_TYPE_CNT

ERR_IP_TYPE_CNT is a count register for dropped packets caused by the IP types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x0000028C	ERR_IP_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_ip_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_ip_type_cnt	Count of the dropped packets caused by the IP types not listed in the filter list

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ERR_UDP_CNT

ERR_UDP_CNT is a count register for filtered packets caused by UDP port numbers beyond the specified range.

Offset Address	Register Name	Total Reset Value
0x00000290	ERR_UDP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_udp_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_udp_cnt	Count of filtered packets caused by UDP port numbers beyond the specified range

OVER_FLOW_CNT

OVER_FLOW_CNT is a count register for dropped packets caused by the full RX FIFO.

Offset Address	Register Name	Total Reset Value
0x00000294	OVER_FLOW_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	over_flow_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	over_flow_cnt	Count of dropped packets caused by the full RX FIFO

OVER_LENGTH_CNT

OVER_LENGTH_CNT is a count register for dropped packets whose size exceeds the upper threshold of the PMU.

Offset Address	Register Name	Total Reset Value
0x00000298	OVER_LENGTH_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	over_length_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	over_length_cnt	Count of dropped packets whose size exceeds the upper threshold of the PMU

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RX_PAUSE_EN

RX_PAUSE_EN is a flow control frame enable register in the RX direction.

Offset Address	Register Name	Total Reset Value
0x000002A4	RX_PAUSE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_fifo_pause_en	rx_bq_pause_en	rx_fq_pause_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fifo_pause_en	rx_fifo flow control frame enable 0: disabled 1: enabled
[1]	RW	rx_bq_pause_en	rx_bq flow control frame enable 0: disabled 1: enabled
[0]	RW	rx_fq_pause_en	rx_fq flow control frame enable 0: disabled 1: enabled

CRF_CFF_DATA_NUM

CRF_CFF_DATA_NUM is a configuration FIFO data count register.

Offset Address	Register Name	Total Reset Value
0x000002A8	CRF_CFF_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_rx_cfg_num																crf_tx_cfg_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_rx_cfg_num	Count of valid descriptors remained in the rx_fq FIFO
[15:0]	RW	crf_tx_cfg_num	Count of valid descriptors remained in the tx_bq FIFO

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FLOW_OUT_IP_CNT

FLOW_OUT_IP_CNT is a count register for dropped IP packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002AC	FLOW_OUT_IP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ip_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ip_cnt	Count of dropped IP packets caused by flow control

FLOW_OUT_CTRL_CNT

FLOW_OUT_CTRL_CNT is a count register for dropped control packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002B0	FLOW_OUT_CTRL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ctrl_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ctrl_cnt	Count of dropped control packets caused by flow control

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CRF_TX_PAUSE

CRF_TX_PAUSE is a TX flow control frame control register.

Offset Address	Register Name	Total Reset Value
0x00000340	CRF_TX_PAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crf_tx_pause_auto
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	crf_tx_pause_auto	Flow control frame control register, specifying the way in which the MAC transmits flow control frames 0: The MAC determines whether to transmit flow control frames according to the actual traffic. When the RX FIFO of the PMU is full or to be full, the MAC transmits flow control frames automatically. 1: The MAC is forced to transmit flow control frames.

CRF_RX_LEFT_NUM

CRF_RX_LEFT_NUM is a flow control RX address count register.

Offset Address	Register Name	Total Reset Value
0x00000344	CRF_RX_LEFT_NUM	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_rx_left_num							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_rx_left_num	When the remaining count of addresses in the RX configuration FIFO is less than the configured value, the control packets are allowed to pass only. The data packets are filtered out.

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CRF_CTRL_0_TYPE

CRF_CTRL_0_TYPE is a control packet type 0 register.

Offset Address	Register Name	Total Reset Value
0x00000348	CRF_CTRL_0_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_0_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_0_type	Control packet type 0. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_1_TYPE

CRF_CTRL_1_TYPE is a control packet type 1 register.

Offset Address	Register Name	Total Reset Value
0x0000034C	CRF_CTRL_1_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_1_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_1_type	Control packet type 1. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_2_TYPE

CRF_CTRL_2_TYPE is a control packet type 2 register.

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Offset Address	Register Name	Total Reset Value
0x00000350	CRF_CTRL_2_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_2_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_2_type	Control packet type 2. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_3_TYPE

CRF_CTRL_3_TYPE is a control packet type 3 register.

Offset Address	Register Name	Total Reset Value
0x00000354	CRF_CTRL_3_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_3_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	crf_ctrl_3_type	Control packet type 3. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_BM_PKT_THRSLD

CRF_BM_PKT_THRSLD is a count threshold register for broadcast/multicast packets under flow control.

Offset Address	Register Name	Total Reset Value
0x00000358	CRF_BM_PKT_THRSLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_bm_pkt_thrsld															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

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[15:0]	RW	crf_bm_pkt_thrsld	Upper threshold of the number of broadcast/multicast packets under flow control. When the number of broadcast/multicast packets that are received during the flow control time exceeds the configured value, the flow is controlled; otherwise, the flow is not controlled.

CRF_BM_TIME_THRSLD

CRF_BM_TIME_THRSLD is a flow control time threshold register for broadcast and multicast packets.

Offset Address	Register Name	Total Reset Value
0x0000035C	CRF_BM_TIME_THRSLD	0x0000_2710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												crf_bm_time_thrsld																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	crf_bm_time_thrsld	Flow control time threshold for broadcast and multicast packets, measured by 1 μs. When the count equals the configured threshold, a time limit is reached.

MDIO_SINGLE_CMD

MDIO_SINGLE_CMD is an MDIO single operation register.

Offset Address	Register Name	Total Reset Value
0x000003C0	MDIO_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											mdio_cmd	reserved				op_code				reserved				phy_addr				reserved				reg_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RW	mdio_cmd	Operation completion through the MDIO indicator 0: The operation through the MDIO is complete. 1: The operation through the MDIO starts.

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[19:18]	RO	reserved	Reserved
[17:16]	RW	op_code	MDIO operation type 00: Reserved 01: Write 10: Read 11: Reserved
[15:13]	RO	reserved	Reserved
[12:8]	RW	phy_addr	5 bits of the external PHY address
[7:5]	RO	reserved	Reserved
[4:0]	RW	reg_addr	Internal address of the PHY component

MDIO_SINGLE_DATA

MDIO_SINGLE_DATA is an MDIO read/write data register.

Offset Address	Register Name	Total Reset Value
0x000003C4	MDIO_SINGLE_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdio_rd_data																mdio_wr_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	mdio_rd_data	Data that is read back from the external PHY through the MDIO
[15:0]	RW	mdio_wr_data	Data that is written through the MDIO

MDIO_CTL

MDIO_CTL is an MDIO control register.

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Offset Address	Register Name	Total Reset Value
0x000003CC	MDIO_CTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												mdio_in_work	mdio_in_work_en	autoscan_en	mdc_speed
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	mdio_in_work	Single operation through the MDIO indicator 0: The single operation is not performed. 1: The single operation is performed.
[2]	RW	mdio_in_work_en	MDIO_IN_WORK bit validity indicator 0: The MDIO_IN_WORK bit is invalid. 1: The MDIO_IN_WORK bit is valid.
[1]	RW	autoscan_en	Automatic detection enable 0: disabled 1: enabled (It controls the automatic scanning enable for all the PHY addresses. The value can be set to 1 because there is only one PHY currently.)
[0]	RW	mdc_speed	Frequency of the MDIO interface clock 0: The frequency of the MDIO interface clock is 2.5 MHz. 1: The frequency of the MDIO interface clock is 18 MHz.

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MDIO_RDATA_STATUS

MDIO_RDATA_STATUS is an MDIO read data status register.

Offset Address	Register Name	Total Reset Value
0x000003D0	MDIO_RDATA_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdio_rdata_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RC	mdio_rdata_status	Whether the data read by the MDIO is valid 0: valid 1: invalid

RX_FQ_START_ADDR

RX_FQ_START_ADDR is a start address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000500	RX_FQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fq_start_addr	Start address of the idle descriptor queue. When rx_fq_start_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_FQ_DEPTH

RX_FQ_DEPTH is a depth register for the idle descriptor queue.

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Offset Address	Register Name	Total Reset Value
0x00000504	RX_FQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	fq_depth	Depth of the idle descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_fq_depth_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

RX_FQ_WR_ADDR

RX_FQ_WR_ADDR is a write address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000508	RX_FQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_wr_addr	Write address of the idle descriptor queue in the RX direction.

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RX_FQ_RD_ADDR

RX_FQ_WR_ADDR is a read address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000050C	RX_FQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_rd_addr	Read address of the idle descriptor queue in the RX direction. When rx_fq_rd_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_rd_addr_en is set to 0, the register is read-only.

RX_FQ_VLDDESC_CNT

RX_FQ_VLDDESC_CNT is a valid descriptor number register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000510	RX_FQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	fq_vlddesc_cnt	Count of valid descriptors in the idle descriptor queue in the RX direction

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RX_FQ_ALRMPTY_TH

RX_FQ_ALRMPTY_TH is an almost-empty threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000514	RX_FQ_ALRMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_low_th																fq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_low_th	Lower flow control threshold of the rx_fq queue. If the count of valid descriptors is less than or equal to the value of fq_pause_low_th, a signal for sending flow control frames is generated.
[15:0]	RW	fq_alempty_th	Almost-empty threshold of the idle descriptor queue in the RX direction

RX_FQ_REG_EN

RX_FQ_REG_EN is an enable register related to the idle descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000518	RX_FQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_fq_start_addr_en	rx_fq_depth_en	rx_fq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fq_start_addr_en	Software write enable for the RX_FQ_START_ADDR register 0: The RX_FQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_FQ_START_ADDR register can be written.

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[1]	RW	rx_fq_depth_en	Software write enable for the RX_FQ_DEPTH register 0: The RX_FQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_FQ_DEPTH register can be written.
[0]	RW	rx_fq_rd_addr_en	Software write enable for the RX_FQ read address register 0: The RX_FQ read address register is protected, and software cannot be written. 1: Software of the RX_FQ read address register can be written.

RX_FQ_ALFULL_TH

RX_FQ_ALFULL_TH is an almost-full threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000051C	RX_FQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_hi_th																fq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_hi_th	Upper flow control threshold for the rx_fq queue. If the count of valid descriptors is greater than or equal to the value of fq_pause_hi_th, a signal for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	fq_alfull_th	Almost-full threshold of the idle descriptor queue in the RX direction

RX_BQ_START_ADDR

RX_BQ_START_ADDR is a start address register for the rx_buff descriptor queue.

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Offset Address	Register Name	Total Reset Value
0x00000520	RX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_bq_start_addr	Start address of the buff descriptor queue in the RX direction. When rx_bq_start_addr_en in the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_BQ_DEPTH

RX_BQ_DEPTH is a depth register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000524	RX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	rx_bq_depth	Depth of the buff descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_bq_depth_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

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RX_BQ_WR_ADDR

RX_BQ_WR_ADDR is a write address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000528	RX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_wr_addr	Write address of the buff descriptor queue in the RX direction. When rx_bq_wr_addr_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_wr_addr_en is set to 0, the register is read-only.

RX_BQ_RD_ADDR

RX_BQ_RD_ADDR is a read address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000052C	RX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_rd_addr	Read address of the buff descriptor queue in the RX direction

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RX_BQ_FREE_DESC_CNT

RX_BQ_FREE_DESC_CNT is a writable descriptor count register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000530	RX_BQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rx_bq_free_desc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rx_bq_free_desc_cnt	Count of writable descriptors in the buff descriptor queue in the RX direction

RX_BQ_ALEMPTY_TH

RX_BQ_ALEMPTY_TH is an almost-empty threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000534	RX_BQ_ALEMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_low_th																rx_bq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_low_th	Flow control threshold of the rx_bq queue. If the count of writable descriptors is less than or equal to the value of bq_pause_low_th, an indicator for sending flow control frames is generated.
[15:0]	RW	rx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the RX direction

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RX_BQ_REG_EN

RX_BQ_REG_EN is an enable register related to the buff descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000538	RX_BQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_bq_start_addr_en	rx_bq_depth_en	rx_bq_wr_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_bq_start_addr_en	Software write enable for the RX_BQ_START_ADDR register 0: The RX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_BQ_START_ADDR register can be written.
[1]	RW	rx_bq_depth_en	Software write enable for the RX_BQ_DEPTH register 0: The RX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_BQ_DEPTH register can be written.
[0]	RW	rx_bq_wr_addr_en	Software write enable for the RX_BQ write address register 0: The RX_BQ write address register is protected, and software cannot be written. 1: Software of the RX_BQ write address register can be written.

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RX_BQ_ALFULL_TH

RX_BQ_ALFULL_TH is an almost-full threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000053C	RX_BQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_hi_th																rx_bq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_hi_th	Upper flow control threshold for the rx_bq queue. If the count of writable descriptors is greater than or equal to the value of bq_pause_hi_th, the indicator for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	rx_bq_alfull_th	Almost-full threshold of the buff descriptor queue in the RX direction

TX_BQ_START_ADDR

TX_BQ_START_ADDR is a start address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000580	TX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_bq_start_addr	Start address of the buff descriptor queue in the TX direction. When tx_bq_start_addr_en in the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

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TX_BQ_DEPTH

TX_BQ_DEPTH is a depth register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000584	TX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_bq_depth	Depth of the buff descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_bq_depth_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_BQ_WR_ADDR

TX_BQ_WR_ADDR is a write address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000588	TX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_wr_addr	Write address of the buff descriptor queue in the TX direction

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TX_BQ_RD_ADDR

TX_BQ_RD_ADDR is a read address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000058C	TX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_rd_addr	Read address of the buff descriptor queue in the TX direction. When rx_bq_rd_addr_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_rd_addr_en is set to 0, the register is read-only.

TX_BQ_VLDDESC_CNT

TX_BQ_VLDDESC_CNT is a valid descriptor number register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000590	TX_BQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_vlddesc_cnt	Count of valid descriptors in the buff descriptor queue in the TX direction

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TX_BQ_ALEMPTY_TH

TX_BQ_ALEMPTY_TH is an almost-empty threshold register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000594	TX_BQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the TX direction

TX_BQ_REG_EN

TX_BQ_REG_EN is an enable register related to the buff descriptor queue in the TX direction.

Offset Address	Register Name	Total Reset Value
0x00000598	TX_BQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx_bq_start_addr_en	tx_bq_depth_en	tx_bq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_bq_start_addr_en	Software write enable for the TX_BQ_START_ADDR register 0: The TX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_BQ_START_ADDR register can be written.

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[1]	RW	tx_bq_depth_en	Software write enable for the TX_BQ_DEPTH register 0: The TX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_BQ_DEPTH register can be written.
[0]	RW	tx_bq_rd_addr_en	Software write enable for the TX_BQ read address register 0: The TX_BQ read address register is protected, and software cannot be written. 1: Software of the TX_BQ read address register can be written.

BQ1_ALFULL_TH

BQ1_ALFULL_TH is an almost-full threshold register for the buff1 descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000059C	BQ1_ALFULL_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bq1_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bq1_alfull_th	Almost-full threshold of the buff1 descriptor queue in the TX direction

TX_RQ_START_ADDR

TX_RQ_START_ADDR is a start address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A0	TX_RQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_rq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_rq_start_addr	Start address of the recycle descriptor queue in the TX direction. When tx_rq_start_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

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TX_RQ_DEPTH

TX_RQ_DEPTH is a depth register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A4	TX_RQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_rq_depth	Depth of the recycle descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_rq_depth_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_RQ_WR_ADDR

TX_RQ_WR_ADDR is a write address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A8	TX_RQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_wr_addr	Write address of the recycle descriptor queue in the TX direction. When tx_rq_wr_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_wr_addr_en is set to 0, the register is read-only.

TX_RQ_RD_ADDR

TX_RQ_RD_ADDR is a read address register for the tx_rq descriptor queue.

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Offset Address	Register Name	Total Reset Value
0x000005AC	TX_RQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_rd_addr	Read address of the recycle descriptor queue in the TX direction.

TX_RQ_FREE_DESC_CNT

TX_RQ_FREE_DESC_CNT is a writable descriptor count register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B0	TX_RQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_free_desc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_free_desc_cnt	Count of writable descriptors in the recycle descriptor queue in the TX direction

TX_RQ_ALEMPTY_TH

TX_RQ_ALEMPTY_TH is an almost-empty threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B4	TX_RQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

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[15:0]	RW	tx_rq_alempty_th	Almost-empty threshold of the recycle descriptor queue in the TX direction

TX_RQ_REG_EN

TX_RQ_REG_EN is an enable register related to the tx_rq descriptor queue

Offset Address	Register Name	Total Reset Value
0x000005B8	TX_RQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx_rq_start_addr_en	tx_rq_depth_en	tx_rq_wr_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_rq_start_addr_en	Software write enable for the TX_RQ_START_ADDR register 0: The TX_RQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_RQ_START_ADDR register can be written.
[1]	RW	tx_rq_depth_en	Software write enable for the TX_RQ_DEPTH register 0: The TX_RQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_RQ_DEPTH register can be written.
[0]	RW	tx_rq_wr_addr_en	Software write enable for the TX_RQ write address register 0: The TX_RQ write address register is protected, and software cannot be written. 1: Software of the TX_RQ write address register can be written.

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TX_RQ_ALFULL_TH

TX_RQ_ALFULL_TH is an almost-full threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005BC	TX_RQ_ALFULL_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_alfull_th	Almost-full threshold of the recycle descriptor queue in the TX direction

RAW_PMU_INT

RAW_PMU_INT is a PMU raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x000005C0	RAW_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	raw_mac_fifo_err_int	raw_tx_rq_in_timeout_int	raw_rx_bq_in_timeout_int	raw_txoutcff_full_int	raw_txoutcff_empty_int	raw_txcff_full_int	raw_txcff_empty_int	raw_rxoutcff_full_int	raw_rxoutcff_empty_int	raw_rxcff_full_int	raw_rxcff_empty_int	raw_tx_rq_in_int	raw_tx_bq_out_int	raw_rx_bq_in_int	raw_rx_fq_out_int	raw_tx_rq_empty_int	raw_tx_rq_full_int	raw_tx_rq_alempty_int	raw_tx_rq_alfull_int	raw_tx_bq_empty_int	raw_tx_bq_full_int	raw_tx_bq_alempty_int	raw_tx_bq_alfull_int	raw_rx_bq_empty_int	raw_rx_bq_full_int	raw_rx_bq_alempty_int	raw_rx_bq_alfull_int	raw_rx_fq_empty_int	raw_rx_fq_full_int	raw_rx_fq_alempty_int	raw_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	raw_mac_fifo_err_int	Raw interrupt of FIFO empty and full errors in the MAC address, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[29]	RW	raw_tx_rq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the RQ queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

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[28]	RW	raw_rx_bq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the BQ queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[27]	RW	raw_txoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[26]	RW	raw_txoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[25]	RW	raw_txcff_full_int	Raw interrupt of full DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[24]	RW	raw_txcff_empty_int	Raw interrupt of empty DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[23]	RW	raw_rxoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[22]	RW	raw_rxoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[21]	RW	raw_rxcff_full_int	Raw interrupt of full DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[20]	RW	raw_rxcff_empty_int	Raw interrupt of empty DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[19]	RW	raw_tx_rq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the tx_rq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

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[18]	RW	raw_tx_bq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the tx_bq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	RW	raw_rx_bq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the rx_bq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RW	raw_rx_fq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the rx_fq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15]	RW	raw_tx_rq_empty_int	Raw interrupt of the empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[14]	RW	raw_tx_rq_full_int	Raw interrupt of the full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[13]	RW	raw_tx_rq_alempty_int	Raw interrupt of the almost-empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[12]	RW	raw_tx_rq_alfull_int	Raw interrupt of the almost-full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	RW	raw_tx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	RW	raw_tx_bq_full_int	Raw interrupt of the full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	RW	raw_tx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

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[8]	RW	raw_tx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7]	RW	raw_rx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	raw_rx_bq_full_int	Raw interrupt of the full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RW	raw_rx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RW	raw_rx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RW	raw_rx_fq_empty_int	Raw interrupt of the empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RW	raw_rx_fq_full_int	Raw interrupt of the full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RW	raw_rx_fq_alempty_int	Raw interrupt of the almost-empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RW	raw_rx_fq_alfull_int	Raw interrupt of the almost-full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

ENA_PMU_INT

ENA_PMU_INT is a PMU raw interrupt register.

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Offset Address	Register Name	Total Reset Value
0x000005C4	ENA_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ena_mac_fifo_err_int	ena_tx_rq_in_timeout_int	ena_rx_bq_in_timeout_int	ena_txoutcff_full_int	ena_txoutcff_empty_int	ena_txcff_full_int	ena_txcff_empty_int	ena_rxoutcff_full_int	ena_rxoutcff_empty_int	ena_rxcff_full_int	ena_rxcff_empty_int	ena_tx_rq_in_int	ena_tx_bq_out_int	ena_rx_bq_in_int	ena_rx_fq_out_int	ena_tx_rq_empty_int	ena_tx_rq_full_int	ena_tx_rq_alempty_int	ena_tx_rq_alfull_int	ena_tx_bq_empty_int	ena_tx_bq_full_int	ena_tx_bq_alempty_int	ena_tx_bq_alfull_int	ena_rx_bq_empty_int	ena_rx_bq_full_int	ena_rx_bq_alempty_int	ena_rx_bq_alfull_int	ena_rx_fq_empty_int	ena_rx_fq_full_int	ena_rx_fq_alempty_int	ena_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	ena_mac_fifo_err_int	Internal FIFO empty and full error interrupt enable in the MAC address 0: disabled 1: enabled
[29]	RW	ena_tx_rq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the RQ queue in the TX direction 0: disabled 1: enabled
[28]	RW	ena_rx_bq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the BQ queue in the RX direction 0: disabled 1: enabled
[27]	RW	ena_txoutcff_full_int	Full DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[26]	RW	ena_txoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[25]	RW	ena_txcff_full_int	Full DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled
[24]	RW	ena_txcff_empty_int	Empty DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled

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[23]	RW	ena_rxoutcff_full_int	Full DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[22]	RW	ena_rxoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[21]	RW	ena_rxcff_full_int	Full DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[20]	RW	ena_rxcff_empty_int	Empty DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[19]	RW	ena_tx_rq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the tx_rq queue in the TX direction 0: disabled 1: enabled
[18]	RW	ena_tx_bq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the tx_bq queue in the TX direction 0: disabled 1: enabled
[17]	RW	ena_rx_bq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the rx_bq queue in the RX direction 0: disabled 1: enabled
[16]	RW	ena_rx_fq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the rx_fq queue in the RX direction 0: disabled 1: enabled
[15]	RW	ena_tx_rq_empty_int	Empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[14]	RW	ena_tx_rq_full_int	Full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[13]	RW	ena_tx_rq_alempty_int	Almost-empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled

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[12]	RW	ena_tx_rq_alfull_int	Almost-full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[11]	RW	ena_tx_bq_empty_int	Empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[10]	RW	ena_tx_bq_full_int	Full buff descriptor queue interrupt enable in the TX direction 1: enabled 0: disabled
[9]	RW	ena_tx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[8]	RW	ena_tx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[7]	RW	ena_rx_bq_empty_int	Empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[6]	RW	ena_rx_bq_full_int	Full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[5]	RW	ena_rx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[4]	RW	ena_rx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[3]	RW	ena_rx_fq_empty_int	Empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[2]	RW	ena_rx_fq_full_int	Full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

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[1]	RW	ena_rx_fq_alempty_int	Almost-empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[0]	RW	ena_rx_fq_alfull_int	Almost-full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

STATUS_PMU_INT

STATUS_PMU_INT is a PMU interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000005C8	STATUS_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	status_mac_fifo_err_int	status_tx_rq_in_timeout_int	status_rx_bq_in_timeout_int	status_txoutcff_full_int	status_txoutcff_empty_int	status_txcff_full_int	status_txcff_empty_int	status_rxoutcff_full_int	status_rxoutcff_empty_int	status_rxcff_full_int	status_rxcff_empty_int	status_tx_rq_in_int	status_tx_bq_out_int	status_rx_bq_in_int	status_rx_fq_out_int	status_tx_rq_empty_int	status_tx_rq_full_int	status_tx_rq_alempty_int	status_tx_rq_alfull_int	status_tx_bq_empty_int	status_tx_bq_full_int	status_tx_bq_alempty_int	status_tx_bq_alfull_int	status_rx_bq_empty_int	status_rx_bq_full_int	status_rx_bq_alempty_int	status_rx_bq_alfull_int	status_rx_fq_empty_int	status_rx_fq_full_int	status_rx_fq_alempty_int	status_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	status_mac_fifo_err_int	Status of the MAC internal FIFO empty and full error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[29]	RW	status_tx_rq_in_timeout_int	Status of the TX RQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[28]	RW	status_rx_bq_in_timeout_int	Status of the RX BQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[27]	RW	status_txoutcff_full_int	Status of the TX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

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[26]	RW	status_txoutcff_empty_int	Status of the TX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RW	status_txcff_full_int	Status of the TX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RW	status_txcff_empty_int	Status of the TX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[23]	RW	status_rxoutcff_full_int	Status of the RX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[22]	RW	status_rxoutcff_empty_int	Status of the RX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[21]	RW	status_rxcff_full_int	Status of the RX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RW	status_rxcff_empty_int	Status of the RX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RW	status_tx_rq_in_int	Status of the tx_rq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RW	status_tx_bq_out_int	Status of the tx_bq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	status_rx_bq_in_int	Status of the rx_bq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	status_rx_fq_out_int	Status of the rx_fq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.

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[15]	RW	status_tx_rq_empty_int	Status of the TX recycle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	status_tx_rq_full_int	Status of the TX recycle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	status_tx_rq_alempty_int	Status of the TX recycle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RW	status_tx_rq_alfull_int	Status of the TX recycle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RW	status_tx_bq_empty_int	Status of the TX buff descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RW	status_tx_bq_full_int	Status of the TX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RW	status_tx_bq_alempty_int	Status of the TX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RW	status_tx_bq_alfull_int	Status of the TX buff descriptor queue almost-full interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[7]	RW	status_rx_bq_empty_int	Status of the RX buff descriptor queue empty interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[6]	RW	status_rx_bq_full_int	Status of the RX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RW	status_rx_bq_alempty_int	Status of the RX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	status_rx_bq_alfull_int	Status of the RX buff descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

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[3]	RW	status_rx_fq_empty_int	Status of the RX idle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RW	status_rx_fq_full_int	Status of the RX idle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RW	status_rx_fq_alempty_int	Status of the RX idle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	status_rx_fq_alfull_int	Status of the RX idle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

DESC_WR_RD_ENA

DESC_WR_RD_ENA is a cff read/write descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x000005CC	DESC_WR_RD_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_outcff_wr_desc_ena	rx_cff_rd_desc_ena	tx_outcff_wr_desc_ena	tx_cff_rd_desc_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	rx_outcff_wr_desc_ena	RX_OUTCFF write descriptor to RX_BQ enable in the RX direction 0: disabled 1: enabled
[2]	RW	rx_cff_rd_desc_ena	RX_CFF read descriptor from the idle descriptor queue enable in the RX direction 0: disabled 1: enabled

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[1]	RW	tx_outcff_wr_desc_ena	TX_OUTCFF write descriptor to TX_RQ enable in the TX direction 0: disabled 1: enabled
[0]	RW	tx_cff_rd_desc_ena	TX_CFF read descriptor from TX_BQ enable in the TX direction 0: disabled 1: enabled

IN_QUEUE_TH

IN_QUEUE_TH is an rx_bq or tx_rq enqueue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05D8	IN_QUEUE_TH	0x0001_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_rq_in_th		reserved		rx_bq_in_th	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	tx_rq_in_th	Threshold for reporting descriptor enqueue interrupts in the TX direction. The threshold must be greater than or equal to 1.
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_bq_in_th	Threshold for reporting descriptor enqueue interrupts in the RX direction. The threshold must be greater than or equal to 1.

OUT_QUEUE_TH

OUT_QUEUE_TH is an rx_fq or tx_bq dequeue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05DC	OUT_QUEUE_TH	0x0001_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_bq_out_th		reserved		rx_fq_out_th	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

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[23:16]	RW	tx_bq_out_th	Threshold for reporting descriptor dequeue interrupts in the TX direction
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_fq_out_th	Threshold for reporting descriptor dequeue interrupts in the RX direction

RX_BQ_IN_TIMEOUT_TH

RX_BQ_IN_TIMEOUT_TH is an rx_bq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E0	RX_BQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_bq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_bq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the BQ queue in the RX direction

TX_RQ_IN_TIMEOUT_TH

TX_RQ_IN_TIMEOUT_TH is a tx_rq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E4	TX_RQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_rq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the RQ queue in the TX direction

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STOP_CMD

STOP_CMD is an RX and TX packet control stop register.

Offset Address	Register Name	Total Reset Value
0x05E8	STOP_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx_stop_en	rx_stop_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_stop_en	Packet TX stop enable 0: disabled 1: enabled
[0]	RW	rx_stop_en	Packet RX stop enable 0: disabled 1: enabled

FLUSH_CMD

FLUSH_CMD is a recycle descriptor enable register.

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Offset Address	Register Name	Total Reset Value
0x05EC	FLUSH_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_flush_cmd	rx_flush_cmd	tx_flush_flag_down	tx_flush_flag_up	rx_flush_flag_down	rx_flush_flag_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	tx_flush_cmd	Recycle descriptor command in the TX direction, instructing the descriptors to enter the tx_rq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[4]	RW	rx_flush_cmd	Recycle descriptor command in the RX direction, instructing the descriptors to enter the rx_bq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[3]	RW	tx_flush_flag_down	Recycle descriptor stop indicator in the TX direction. After descriptors are recycled, the logic sets tx_flush_flag to 1, and the software writes 1 to clear the register.
[2]	RW	tx_flush_flag_up	Recycle descriptor stop indicator in the TX direction. After RX and TX packets are stopped, the logic sets tx_flush_flag to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.
[1]	RW	rx_flush_flag_down	Recycle descriptor stop indicator in the RX direction. After descriptors are recycled, the logic sets rx_flush_flag_down to 1, and the software writes 1 to clear the register.
[0]	RW	rx_flush_flag_up	Recycle descriptor indicator in the RX direction. After RX packets are stopped, the logic sets rx_flush_flag_up to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.

U_EEE_INTR_SRC

U_EEE_INTR_SRC is an LPI status register in the RX and TX directions.

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Offset Address	Register Name	Total Reset Value
0x0800	U_EEE_INTR_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_lpi_cond	rx_leave_lpi	rx_entry_lpi	tx_leave_lpi	tx_entry_lpi
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	tx_lpi_cond	LPI status in the TX direction 0: The TX FIFO and TX descriptors cannot be empty simultaneously. 1: The TX FIFO and TX descriptors are empty simultaneously.
[3]	RW	rx_leave_lpi	LPI exit in the RX direction 0: not exited 1: exited
[2]	RW	rx_entry_lpi	LPI enter in the RX direction 0: not entered 1: entered
[1]	RW	tx_leave_lpi	LPI exit in the TX direction 0: not exited 1: exited
[0]	RW	tx_entry_lpi	LPI enter in the TX direction 0: not entered 1: entered

U_EEE_INTR_EN

U_EEE_INTR_EN is an interrupt mask and enable register in the RX and TX directions.

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Offset Address	Register Name	Total Reset Value
0x0804	U_EEE_INTR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_lpi_cond_msk	rx_leave_lpi_msk	rx_entry_lpi_msk	tx_leave_lpi_msk	tx_entry_lpi_msk	tx_lpi_cond_en	rx_leave_lpi_en	rx_entry_lpi_en	tx_leave_lpi_en	tx_entry_lpi_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	tx_lpi_cond_msk	LPI status interrupt mask in the TX direction 0: not masked 1: masked
[8]	RW	rx_leave_lpi_msk	LPI status exit interrupt mask in the RX direction 0: not masked 1: masked
[7]	RW	rx_entry_lpi_msk	LPI status enter interrupt mask in the RX direction 0: not masked 1: masked
[6]	RW	tx_leave_lpi_msk	LPI status exit interrupt mask in the TX direction 0: not masked 1: masked
[5]	RW	tx_entry_lpi_msk	LPI status enter interrupt mask in the TX direction 0: not masked 1: masked
[4]	RW	tx_lpi_cond_en	LPI status interrupt enable in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[3]	RW	rx_leave_lpi_en	LPI status interrupt enable exit in the RX direction 0: Disable interrupts. 1: Enable interrupts.
[2]	RW	rx_entry_lpi_en	LPI status interrupt enable enter in the RX direction 0: Disable interrupts. 1: Enable interrupts.

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[1]	RW	tx_leave_lpi_en	LPI status interrupt enable exit in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[0]	RW	tx_entry_lpi_en	LPI status interrupt enable enter in the TX direction 0: Disable interrupts. 1: Enable interrupts.

U_EEE_ENABLE

U_EEE_ENABLE is an EEE enable signal register.

Offset Address	Register Name	Total Reset Value
0x0808	U_EEE_ENABLE	0x00F4_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eee_ls_timer																												gmii_mode	cond_intr_keep	tx_lpi_assert	eee_enable
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	Buffer time for the buffer software to enable the hardware to enter the LPI when phy_link_sts is set to 1. The default time is 1s.
[3]	RW	gmii_mode	GMII mode select 0: MII mode 1: GMII mode
[2]	RW	cond_intr_keep	Interrupt signal TX frequency 0: The hardware sends only one tx_lpi_cond interrupt. 1: The interrupt is enabled on the rising edge of each clock in LPI mode in the TX direction.
[1]	RW	tx_lpi_assert	Software configuring the hardware to enter the LPI state 0: The hardware does not enter the LPI state. 1: The hardware enters the LPI state.
[0]	RW	eee_enable	EEE module enable 0: disabled 1: enabled

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U_EEE_TIMER

U_EEE_TIMER is an LPI time threshold register.

Offset Address	Register Name	Total Reset Value
0x080C	U_EEE_TIMER	0x001E_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lpi_tw_timer																lpi_cond_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	lpi_tw_timer	Wake-up time of the register from the LPI mode to normal mode. The default time is 30 μs.
[15:0]	RW	lpi_cond_timer	Duration when the TX FIFO and EX_DESC are empty at the same time. When the duration is equal to the value of lpi_cond_timer, the register enters the LPI mode.

U_EEE_LINK_STATUS

U_EEE_LINK_STATUS is an EEE status register.

Offset Address	Register Name	Total Reset Value
0x0810	U_EEE_LINK_STATUS	0x0000_3F20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_cnt																eee_tx_lpi_stay	eee_rx_lpi_stay_ff3	version										reserved	eee_auto	eee_hold_txdesc_read	phy_link_sts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	intr_cnt	EEE interrupt count
[15]	RO	eee_tx_lpi_stay	Whether the TX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.
[14]	RO	eee_rx_lpi_stay_ff3	Whether the RX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.

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[13:4]	RO	version	Logical version number
[3]	RO	reserved	Reserved
[2]	RW	eee_auto	Automatic EEE entry and exit 0: The logic enters or exits the EEE mode by using the software and logic interrupt. 1: The logic automatically enters or exits the EEE without the intervention of software.
[1]	RW	eee_hold_txdesc_read	Whether the MAC can obtain packets from the TX FIFO in LPI status 0: yes 1: no
[0]	RW	phy_link_sts	PHY connection state 0: link_down 1: link_up

U_EEE_TIME_CLK_CNT

U_EEE_TIME_CLK_CNT is a timing pulse count register.

Offset Address	Register Name	Total Reset Value
0x0814	U_EEE_TIME_CLK_CNT	0x0000_007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_period_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:0]	RW	clk_period_cnt	Count register used to generate a 1 μs timing pulse in the hardware. The clock cycle is 8 ns when the clock frequency is 125 MHz.

PMT_CTRL_STAUTS

PMT_CTRL_STAUTS is a PMT control and status register.

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Offset Address	Register Name	Total Reset Value
0x0A00	PMT_CTRL_STAUTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						scr_wkupfrm_glbucast	reserved		rcvd_wkup_frm	rcvd_mgk_pkt	reserved	scr_intr_en	scr_wkupfrm_en	scr_mgkpkt_en	scr_power_down
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	scr_wkupfrm_glbucast	Whether the unicast frame used to configure the MAC address is the wake-up frame 0: The unicast frame is not regarded as the wake-up frame. 1: The unicast frame used to configure the MAC address is regarded as the valid wake-up frame.
[8:7]	RO	reserved	Reserved
[6]	RW	rcvd_wkup_frm	Whether a wake_up frame is received 0: no 1: yes
[5]	RW	rcvd_mgk_pkt	Whether the magic packet is received. 0: no 1: yes
[4]	RO	reserved	Reserved
[3]	RW	scr_intr_en	PMT interrupt enable 0: disabled 1: enabled
[2]	RW	scr_wkupfrm_en	wake_up frame receive enable 0: disabled 1: enabled
[1]	RW	scr_mgkpkt_en	Magic packet receive enable 0: disabled 1: enabled
[0]	RW	scr_power_down	Power-down mode enable 0: Exit the power-down mode. 1: Enter the power-down mode.

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FILTER_0_BYTE_MASK

FILTER_0_BYTE_MASK is PMT valid byte selection register 1.

Offset Address	Register Name	Total Reset Value
0x0A04	FILTER_0_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter0bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter0bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask. If a bit is 1, the corresponding byte is valid.

FILTER_1_BYTE_MASK

FILTER_1_BYTE_MASK is PMT valid byte selection register 2.

Offset Address	Register Name	Total Reset Value
0x0A08	FILTER_1_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter1bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

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FILTER_2_BYTE_MASK

FILTER_2_BYTE_MASK is PMT valid byte selection register 3.

Offset Address	Register Name	Total Reset Value
0x0A0C	FILTER_2_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter2bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter2bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_3_BYTE_MASK

FILTER_3_BYTE_MASK is PMT valid byte selection register 4.

Offset Address	Register Name	Total Reset Value
0x0A10	FILTER_3_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter3bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

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FILTER_COMMAND

FILTER_COMMAND is a PMT template selection and multicast enable register.

Offset Address	Register Name	Total Reset Value
0x0A14	FILTER_COMMAND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wkupfrm_filter3mcast	reserved		wkupfrm_filter3en	reserved				wkupfrm_filter2mcast	reserved		wkupfrm_filter2en	reserved				wkupfrm_filter1mcast	reserved		wkupfrm_filter1en	reserved				wkupfrm_filter0mcast	reserved		wkupfrm_filter0en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	wkupfrm_filter3mcast	Address type specified by template 3 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[26:25]	RO	reserved	Reserved.
[24]	RW	wkupfrm_filter3en	Filter template 3 enable 0: disabled 1: enabled
[23:20]	RO	reserved	Reserved
[19]	RW	wkupfrm_filter2mcast	Address type specified by template 2 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[18:17]	RO	reserved	Reserved
[16]	RW	wkupfrm_filter2en	Filter template 2 enable 0: disabled 1: enabled
[15:12]	RO	reserved	Reserved

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[11]	RW	wkupfrm_filter1mcast	Address type specified by template 1 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[10:9]	RO	reserved	Reserved.
[8]	RW	wkupfrm_filter1en	Filter template 1 enable 0: disabled 1: enabled
[7:4]	RO	reserved	Reserved
[3]	RW	wkupfrm_filter0mcast	Address type specified by template 0 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[2:1]	RO	reserved	Reserved.
[0]	RW	wkupfrm_filter0en	Filter template 0 enable 0: disabled 1: enabled

FILTER_OFFSET

FILTER_OFFSET is a CRC position offset register.

Offset Address	Register Name	Total Reset Value
0x0A18	FILTER_OFFSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wkupfrm_filter3offset		wkupfrm_filter2offset		wkupfrm_filter1offset		wkupfrm_filter0offset	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wkupfrm_filter3offset	Template 3 of the four templates, used to calculate the CRC position offset
[23:16]	RW	wkupfrm_filter2offset	Template 2 of the four templates, used to calculate the CRC position offset
[15:8]	RW	wkupfrm_filter1offset	Template 1 of the four templates, used to calculate the CRC position offset
[7:0]	RW	wkupfrm_filter0offset	Template 0 of the four templates, used to calculate the CRC position offset

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FILTER0_1_CRC

FILTER0_1_CRC is a software-expected CRC value 0 and 1 register.

Offset Address	Register Name	Total Reset Value
0x0A1C	FILTER0_1_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1crc																wkupfrm_filter0crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter1crc	CRC value expected by software of template 1 in the four templates
[15:0]	RW	wkupfrm_filter0crc	CRC value expected by software of template 1

FILTER2_3_CRC

FILTER2_3_CRC is a software-expected CRC value 2 and 3 register.

Offset Address	Register Name	Total Reset Value
0x0A20	FILTER2_3_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3crc																wkupfrm_filter2crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter3crc	CRC value expected by software of template 3
[15:0]	RW	wkupfrm_filter2crc	CRC value expected by software of template 2

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Contents

6 Video Encoder 6-1
6.1 Introduction 6-1
6.2 AVC 6-1
6.2.1 Overview 6-1
6.2.2 Features 6-1
6.2.3 Function Description 6-2
6.3 VEDU 6-3
6.3.1 Overview 6-3
6.3.2 Features 6-3
6.3.3 Function Description 6-4
6.4 JPGE 6-6
6.4.1 Overview 6-6
6.4.2 Features 6-6
6.4.3 Function Description 6-6

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Figures

Figure 6-1 Encoding functional block diagram of the AVC 6-3

Figure 6-2 Encoding functional block diagram of the VEDU 6-5

Figure 6-3 Encoding functional block diagram of the JPGE 6-7

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6 Video Encoder

6.1 Introduction

The encoding unit consists of the video encoding units (AVC/VEDU) and JPEG encoder (JPGE). The AVC supports H.264 encoding. The VEDU supports H.265 encoding, and the JPGE supports JPEG encoding.

6.2 AVC

6.2.1 Overview

The AVC is a CODEC that supports H.264 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, short delay, and low power consumption.

6.2.2 Features

The VENC has the following features:

- Supports ITU-T H.264 high profile/main profile/baseline profile@level 5.1 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four subblock types of 16x16, 16x8, 8x16, and 8x8 for inter-prediction
  - Prediction modes of intra4x4, intra8x8, and intra16x16
  - Trans4x4 and Trans8x8

    Context-based adaptive binary arithmetic coding (CABAC) and context-based adaptive variable-length coding (CAVLC) entropy encoding
  - De-blocking filtering
  - IPCM encoding
- Supports SVC time-domain layering (SVC-T).
- Supports the input picture format of semi-planar YCbCr4:2:0.
- Supports H.264 video encoding:
  - 1080P@30 fps
  - 5-megapixel@30 fps+VGA@30 fps
  - 5-megapixel@30 fps

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  - 2*1080p@30 fps + VGA@30 fps
  - 1080p@30 fps+720p@30 fps+VGA@30 fps
- Supports configurable picture resolutions.
  - Minimum picture resolution: 160 x 64
  - Maximum picture resolution: 2592 x 2592
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding.
  - A maximum of eight ROIs
  - ROI encoding control (enabled or disabled)
- Supports on-screen display (OSD) encoding protection.

  OSD encoding protection control (enabled or disabled)
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlaying anywhere (the maximum OSD size is the picture size)
  - 129-level alpha blending
  - OSD overlaying control
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP.
- Supports color-to-gray encoding.
- Supports the output bit rate ranging from 2 kbit/s to 40 Mbit/s.

CAUTION

The AVC encoding protection function applies only to the OSD overlaid on the AVC.

6.2.3 Function Description

Figure 6-1 shows the encoding functional block diagram of the AVC.

Based on related protocols and algorithms, the AVC supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, variable length code (VLC) encoding, stream generation, and de-blocking filtering. The video firmware (FMW) controls the bit rate and handles interrupts.

Before the AVC is enabled for video encoding, the software allocates three types of buffers for the AVC in the external DDR SDRAM:

- Input picture buffer

  The AVC reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.
- Reconstruction/reference picture buffer

  The AVC writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.
- Stream buffer

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This buffer stores encoded streams. The AVC writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-1 Encoding functional block diagram of the AVC

6.3 VEDU

6.3.1 Overview

The video encoding/decoding unit (VEDU) is a video encoder that supports the H.265 protocol and implements encoding by using hardware. It features low CPU usage, low bus bandwidth, short delay, and low power consumption.

6.3.2 Features

The VEDU has the following features:

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- Supports ITU-T H.265 main profile @level 5.1 main-tier encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four prediction unit (PU) types of 64x64, 32x32, 16x16, and 8x8 for inter-prediction
  - Four PU types of 32x32, 16x16, 8x8, and 4x4 for intra-prediction
  - Skip mode and merge mode with a maximum of two candidate points to be merged
  - Four transform unit (TU) types of 32x32, 16x16, 8x8, and 4x4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
  - IPCM encoding
- Supports the input picture format of semi-planar YCbCr4:2:0.
- Supports H.265 encoding of multiple streams:

  Hi3516A:
  - 5-megapixel@30 fps+VGA@30 fps
  - 2*1080p@30 fps + VGA@30 fps
  - 1080p@30 fps+720p@30 fps+VGA@30 fps

  Hi3516D:
  - 1080p@30 fps+720p@30 fps+VGA@30 fps
  - 3-megapixel@30 fps+VGA@30 fps
  - 5-megapixel@15 fps
- Supports configurable picture resolutions.
  - Minimum picture resolution: 128 x 128
  - Maximum picture resolution: 2592 x 2592
  - Picture width or height step: 2
- Supports ROI encoding.
  - A maximum of eight ROIs
  - ROI encoding control (enabled or disabled)
- Supports OSD encoding protection.

  OSD encoding protection control (enabled or disabled)
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlaying anywhere (the maximum OSD size is the picture size)
  - 129-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports color-to-gray encoding.
- Supports three bit rate control modes: CBR, VBR and FIXQP.
- Provides the output bit rate ranging from 2 kbit/s to 40 Mbit/s.

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CAUTION

The VEDU encoding protection function applies only to the OSD overlaid on the VEDU.

6.3.3 Function Description

Figure 6-2 shows the functional block diagram of the VEDU.

Based on related protocols and algorithms, the VEDU supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding, stream generation, de-blocking filtering, and SAO. The ARM software controls the bit rate and handles interrupts.

Before the VEDU is enabled for video encoding, software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Input picture buffer

  The VEDU reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.

- Reconstruction/Reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.

- Stream buffer

  This buffer stores encoded streams. The VEDU writes streams to this buffer during encoding. This buffer is read by software.

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Figure 6-2 Encoding functional block diagram of the VEDU

6.4 JPGE

6.4.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports 67.1-megapixel snapshot or HD MJPEG encoding.

6.4.2 Features

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding.
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2, or YCbCr4:4:4.
- Supports the microprogrammed control unit (MCU) using the interleaved sequence.

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- Supports multiple input picture formats:
  - Planar YCbCr4:2:0
  - Planar YCbCr4:2:2
  - Planar YCbCr4:4:4
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Package YUYV
- Supports JPEG encoding:
  - 1080p@15 fps
  - 5-megapixel@8 fps
- Supports configurable picture resolutions.
  - Minimum picture resolution: 32 x 32
  - Maximum picture resolution: 8192 x 8192
- Supports the picture width or height step of 4.
- Supports configurable quantization tables.

  An independent quantization table for the Y component, Cb component, and Cr component respectively
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlapping with the maximum size of the source picture and within the picture position range
  - 129-level alpha blending
  - OSD overlaying control

6.4.3 Function Description

Figure 6-3 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports OSD, level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-3 Encoding functional block diagram of the JPGE

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Contents

7 Video and Graphics Processing 7-1
7.1 TDE 7-1
7.1.1 Overview 7-1
7.1.2 Function Description 7-1
7.2 VPSS 7-2
7.2.1 Overview 7-2
7.2.2 Features 7-2
7.3 VGS 7-3
7.3.1 Overview 7-3
7.3.2 Features 7-3

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7 Video and Graphics Processing

7.1 TDE

7.1.1 Overview

The two-dimensional engine (TDE) draws graphics using hardware. This significantly reduces the CPU usage and improves the utilization of the memory bandwidth. The TDE reads and writes the information about the bitmap data, filtering/scaling coefficients, parameters of linked list nodes, and linked list over the advanced eXtensible bus (AXI) master interface. By using the advanced peripheral bus (AHB) interface, the TDE obtains the CPU register configuration information.

The graphics data interface includes two channels, Their functions are as follows:

- Channel 1 implements direct copy and direct filling during a single-source operation.
- Channel 2 implements complicated functions such as scaling during a single-source operation.
- Channel 1 works with channel 2 to implement color blending and process the images in macroblock format.

7.1.2 Function Description

The TDE has the following features:

- Channel 1 supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, halfword.
- Channel 2 supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8.
- The output image supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, byte, halfword.
- Supports only the little-endian system.
- Allows the formats of source bitmap 1, source bitmap 2, and output bitmaps to be configured separately.
- Supports gamma correction and adjustable contrast and luminance.
- Supports direct copy.
- Supports direct filling.

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- Supports 2D resize.
- Supports clip.
- Supports alpha blending.
- Supports colorkey.
- Supports clip mask.
- Supports inverse scanning.
- Provides status interrupts.

7.2 VPSS

7.2.1 Overview

The video processing subsystem (VPSS) implements video processing. It supports Gaussian 3D adaptive noise reduction (NR) as well as video covering, cropping, scaling, and processing.

The VPSS has the following features:

- Processing of video sources with 2592-pixel width using a single frame in online or offline mode
- A maximum of four video output channels including three encoding channels and one display channel
- Eight video regions covered by any filled quadrilaterals for each of the three output encoding channels. Eight sets of covering coordinates are fixed. The display channel does not support video covering.
- Video cropping four three output channels (two encoding channels and one display channel)
- Video data compression
- Register configuration using the linked list in offline mode and register configuration using the APB in online mode
- Span of 4 KB boundary
- Input or output data format of semi-planar 420/422
- Outstanding configuration
- Memory low-power mode by using clock gating
- Low delay

7.2.2 Features

The following describes the major features:

- Gaussian NR: The NR module removes the Gaussian noises from pictures by configuring parameters. Then pictures become smooth and the encoding bit rate is reduced.
- Scaling: Low-frequency filtering is supported when the input and output resolution are different. At most 15 times zoom out are supported.

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7.3 VGS

7.3.1 Overview

The video graphics system (VGS) implements video and graphics processing. The functions include OSD overlaying, luminance region statistics, video cropping, video covering, rotation, and distortion correction.

The VGS has the following features:

- Processing of video sources with the 2592-pixel width by using a single frame in offline mode
- One video output channel
- Overlaying of one regions of OSDs and videos
- OSD input format of ARGB1555, ARGB4444, or ARGB8888
- Configuration of register linked lists
- Span of 4 KB boundary
- Linear storage for input data
- Linear storage for output data
- Video data compression
- Rotation by 90º or 270º
- One video region covered by any filled or hollow quadrilateral
- Video cropping
- Outstanding configuration
- Memory low-power mode by using clock gating
- Statistics of the region luminance sum

7.3.2 Features

The following describes the major features:

- Video covering: A video region is covered by any filled or hollow quadrilateral.
- Scaling: Low-frequency filtering is supported when the input and output resolution are different. At most 15.5 times zoom out and 16 times zoom in are supported.

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Contents

8 Motion Detect Unit 8-1
8.1 Overview 8-1
8.2 Function Description 8-1
8.3 Operating Mode 8-1
8.3.1 Software and Hardware for Motion Detection 8-1
8.3.2 Software and Hardware for Video Occlusion Detection 8-2
8.4 Register Summary 8-2
8.5 Register Description 8-3

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Tables

Table 8-1 Summary of the MDU registers (base address: 0x206C_0000) 8-2

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8 Motion Detect Unit

8.1 Overview

As a high-performance hardware acceleration intellectual property (IP), the motion detect unit (MDU) is used to detect the motion status and video occlusion, implement modeling on the video background, and calculate the information about the object (OBJ) region. The OBJ region is a rectangular motion part of the current frame. By using the advanced eXtensible interface (AXI) master bus, the MDU reads picture information, and writes the updated information about the background, sum of absolute differences (SADs), and OBJ regions. By using the slave advanced high-performance bus (APB), the MDU obtains register configurations.

8.2 Function Description

The MDU provides the following features:

- Calculates and outputs the SAD in the unit of 8x8 or 16x16.
- Detects OBJ regions and outputs the information about the OBJ regions.
- Refreshes the background.
- Supports the input of uncompressed data but not the input of compressed data.

8.3 Operating Mode

8.3.1 Software and Hardware for Motion Detection

The software performs the following operations for the pictures to be encoded:

- Allocates the storage space in the double-data rate (DDR).
- Calls the hardware to capture videos or perform scaling.
- Schedules multiple motion detection operations, specifies and divides the regions to be detected, and generates addresses.

The hardware calculates the SADs of input pictures. The details are as follows:

- Detects OBJ regions based on the SAD and threshold, and refreshes the background.

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- Outputs the information about OBJ regions, background, and SADs based on the settings of the software.

8.3.2 Software and Hardware for Video Occlusion Detection

Based on the size of OBJ regions output by the hardware, the software checks whether the occlusion threshold is reached. If the threshold is reached, the background is forbidden to refresh, but motion detection is still performed. When the size of OBJ regions is greater than the occlusion threshold, an occlusion alarm is generated.

8.4 Register Summary

Table 8-1 describes the MDU registers.

Table 8-1 Summary of the MDU registers (base address: 0x206C_0000)

Offset Address	Register	Description	Page
0x0000	MDU_INTSTAT	Interrupt status register	8-3
0x0004	MDU_INTEN	Interrupt enable register	8-4
0x0008	MDU_RAWINT	Raw interrupt register	8-5
0x000C	MDU_INTCLR	Interrupt clear register	8-5
0x0020	MDU_VEDIMGSIZE	Picture size configuration register	8-6
0x0024	MDU_MODE	Mode configuration register	8-7
0x0028	MDU_START	MDU start register	8-8
0x002C	MDU_AXI_OUTSTD_NUM	AXI outstanding configuration register	8-8
0x0040	MDU_REF_YADDR	Luminance storage address register of the reference picture	8-9
0x0044	MDU_REF_YSTRIDE	Luminance stride register of the reference picture	8-9
0x0048	MDU_CUR_YADDR	Luminance storage address register of the current picture	8-10
0x004C	MDU_CUR_YSTRIDE	Luminance stride register of the current picture	8-10
0x0060	MDU_MBSAD_ADDR	Macroblock SAD storage address register	8-11
0x0064	MDU_MBSAD_STRIDE	Macroblock SAD storage stride register	8-11
0x0070	MDU_BACKGROUND_ADDR	Luminance storage address register of the background	8-12

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Offset Address	Register	Description	Page
0x0074	MDU_BACKGROUND_STRIDE	Luminance stride register of the background	8-12
0x0078	MDU_OBJ_ADDR	OBJ region storage address register	8-12
0x007C	MDU_BG_UP_WEIGHT	Background refresh weight register	8-13
0x0080	MDU_MBSAD_TH	Macroblock motion detection threshold register	8-14
0x0084	MDU_TIMEOUT	Timeout upper limit register	8-14
0x0090	MDU_WND_SIZE	SAD output window configuration register	8-14
0x0094	MDU_MIN_OBJ_SIZE	Minimum window configuration register for boundary search	8-15
0x0098	MDU_MAX_OBJ_CNT	Maximum window configuration register for boundary search	8-16
0x009C	MDU_OBJ_CNT	OBJ region information readback register	8-16
0x00A0	MDU_MAX_OBJ_SIZE	Maximum OBJ region readback register	8-16
0x00A4	MDU_TOTAL_OBJ_SIZE	All OBJ region information readback register	8-17
0x00A8	MDU_MOVE_PIX_CNT	Motion pixel statistics register for an entire frame	8-18
0x00AC	MDU_OBJ_CNT1	OBJ region information readback register based on the background	8-18
0x00B0	MDU_MAX_OBJ_SIZE1	Maximum OBJ region readback register based on the background	8-18
0x00B4	MDU_TOTAL_OBJ_SIZE1	All OBJ region information readback register based on the background	8-19
0x00B8	MDU_MOVE_PIX_CNT1	Motion pixel statistics register for an entire frame based on the background	8-19

8.5 Register Description

MDU_INTSTAT

MDU_INTSTAT is an interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x0000	MDU_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err	mdu_cfg_err	reserved																												mdu_timeout	mdu_endofpic
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err	Bus read/write error.
[30]	RO	mdu_cfg_err	Register configuration error.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout	MDU timeout interrupt. This interrupt is valid when the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT.
[0]	RO	mdu_endofpic	End of picture indicator of the MDU, active high.

MDU_INTEN

MDU_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	MDU_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_en	mdu_cfg_err_en	reserved																												mdu_timeout_en	mdu_endofpic_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_en	BUS read/write error interrupt enable. 0: disabled 1: enabled

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[30]	RW	mdu_cfg_err_en	Register configuration error interrupt enable. 0: disabled 1: enabled
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_en	MDU timeout interrupt enable. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid. 0: disabled 1: enabled
[0]	RW	mdu_endofpic_en	End of picture interrupt enable of the MDU 0: disabled 1: enabled

MDU_RAWINT

MDU_RAWINT is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	MDU_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_raw	mdu_cfg_err_raw	reserved																												mdu_timeout_raw	mdu_endofpic_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err_raw	Raw bus read/write error interrupt, active high.
[30]	RO	mdu_cfg_err_raw	Raw register configuration error interrupt, active high.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout_raw	Raw MDU timeout interrupt, active high.
[0]	RO	mdu_endofpic_raw	Raw end of picture interrupt of the MDU, active high.

MDU_INTCLR

MDU_INTCLR is an interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x000C	MDU_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_clr	mdu_cfg_err_clr	reserved																												mdu_timeout_clr	mdu_endofpic_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_clr	Bus read/write error clear, active high.
[30]	RW	mdu_cfg_err_clr	Register configuration error clear, active high.
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_clr	MDU timeout interrupt clear. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid.
[0]	RW	mdu_endofpic_clr	End of picture indicator clear of the MDU, active high.

MDU_VEDIMGSIZE

MDU_VEDIMGSIZE is a picture size configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	MDU_VEDIMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				imgheightinpixelsminus1												reserved				imgwidthinpixelsminus1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	imgheightinpixelsminus1	Picture height. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual height. For example, if the picture height is 352 pixels, this field must be set to 351 pixels. The maximum picture height is 960 pixels.
[15:13]	RO	reserved	Reserved.

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[12:0]	RW	imgwidthinpixelsminus1	Picture width. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual width. For example, if the picture width is 288 pixels, this field must be set to 287 pixels. The maximum picture width is 960 pixels.

MDU_MODE

MDU_MODE is a mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	MDU_MODE	0x0000_019C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							mcpi_clkgate_en	mcpi_wrlock_en	timeout_en	md_mod	bg_update_en	eg_find_en	obj_out_en	sad_out_en	sad_mad_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	mcpi_clkgate_en	Clock gating enable.
[7]	RW	mcpi_wrlock_en	Register configuration lock enable. If this field is enabled, registers cannot be configured even if the MDU is started until the detection ends. This avoids modifications made to registers.
[6]	RW	timeout_en	MDU timeout detection enable. If this field is enabled, the upper limits of the working cycle that is configured using MDU_TIMEOUT by the software can be automatically queried. 0: disabled 1: enabled
[5]	RW	md_mod	Motion detection mode. 0: background algorithm 1: frame reference algorithm
[4]	RW	bg_update_en	Background refresh enable. 0: disabled 1: enabled This field is valid only when md_mod is set to 0 (background algorithm).

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[3]	RW	eg_find_en	Joint detection enable for OBJ regions. 0: disabled 1: enabled If the background algorithm is selected, only the last joint detection based on the background is disabled.
[2]	RW	obj_out_en	OBJ region output enable. If this field is enabled, MDU_OBJ_ADDR must be configured. 0: disabled 1: enabled
[1]	RW	sad_out_en	SAD output enable. If this field is enabled, MDU_MBSAD_ADDR and MDU_MBSAD_STRIDE must be configured. 0: disabled 1: enabled
[0]	RW	sad_mad_sel	Number of SAD output bits. 0: 8 bits 1: 16 bits

MDU_START

MDU_START is an MDU start register.

Offset Address	Register Name	Total Reset Value
0x0028	MDU_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdu_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	mdu_start	MDU start control. 0: The MDU does not work. 1: The MDU is started.

MDU_AXI_OUTSTD_NUM

MDU_AXI_OUTSTD_NUM is an AXI outstanding configuration register.

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Offset Address	Register Name	Total Reset Value
0x002C	MDU_AXI_OUTSTD_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													axi_outstd_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	axi_outstd_num	AXI outstanding configuration. The count value is numbered from 0 and the actual value is obtained by adding 1 to the count value.

MDU_REF_YADDR

MDU_REF_YADDR is a luminance storage address register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0040	MDU_REF_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_ref_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_ref_yaddr	Storage address of the Y component of the reference picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_REF_YSTRIDE

MDU_REF_YSTRIDE is a luminance stride register of the reference picture.

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Offset Address	Register Name	Total Reset Value
0x0044	MDU_REF_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_ref_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_ref_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_CUR_YADDR

MDU_CUR_YADDR is a luminance storage address register of the current picture.

Offset Address	Register Name	Total Reset Value
0x0048	MDU_CUR_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_cur_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_cur_yaddr	Storage address of the Y component of the raw picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_CUR_YSTRIDE

MDU_CUR_YSTRIDE is a luminance stride register of the current picture.

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Offset Address	Register Name	Total Reset Value
0x004C	MDU_CUR_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_cur_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_cur_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_MBSAD_ADDR

MDU_MBSAD_ADDR is a macroblock SAD storage address register.

Offset Address	Register Name	Total Reset Value
0x0060	MDU_MBSAD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_mbsad_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_mbsad_addr	Address for storing the macroblock SAD. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_MBSAD_STRIDE

MDU_MBSAD_STRIDE is a macroblock SAD storage stride register.

Offset Address	Register Name	Total Reset Value
0x0064	MDU_MBSAD_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	mdu_mbsad_stride	Macroblock SAD stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_ADDR

MDU_BACKGROUND_ADDR is a luminance storage address register of the background.

Offset Address	Register Name	Total Reset Value
0x0070	MDU_BACKGROUND_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	bg_yaddr	Background address. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_STRIDE

MDU_BACKGROUND_STRIDE is a luminance stride register of the background.

Offset Address	Register Name	Total Reset Value
0x0074	MDU_BACKGROUND_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bg_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	bg_ystride	Background stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_OBJ_ADDR

MDU_OBJ_ADDR is an OBJ region storage address register.

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Offset Address	Register Name	Total Reset Value
0x0078	MDU_OBJ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obj_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	obj_addr	Address for storing OBJ regions. The address must be Qword-aligned. Therefore, the lower four bits must be 0. An OBJ region is stored as follows: The coordinates of the left, top, right, and bottom points of the OBJ region are stored in sequence in four 16-bit spaces. Therefore, two 32-bit DDRs are used to store an OBJ region. When the DDR is allocated by using the software, the minimum DDR size is calculated as follows: 2 x 32 bits x Maximum number of OBJ regions

MDU_BG_UP_WEIGHT

MDU_BG_UP_WEIGHT is a background refresh weight register.

Offset Address	Register Name	Total Reset Value
0x007C	MDU_BG_UP_WEIGHT	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																src_weight								weight_sum_exp_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	src_weight	New picture weight.
[7:0]	RW	weight_sum_exp_2	Exponent of 2 to the weighted sum. When the MDU generates a new background by overlaying the source picture with the existing background, the following formula is used: (Background pixel x ((1<<weight_sum_exp_2) – src_weight) + Pixel of source picture x bg_weight) >> weight_sum_exp_2) The background weight bg_weight is calculated as follows: ((1<<weight_sum_exp_2) – src_weight) The greater the value obtained from background weight bg_weight minus source weight src_weight, the more slowly the background is refreshed. The default value is 0x1, and the maximum value is 0x8.

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MDU_MBSAD_TH

MDU_MBSAD_TH is a macroblock motion detection threshold register.

Offset Address	Register Name	Total Reset Value
0x0080	MDU_MBSAD_TH	0x0000_001E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_mbsad_th	Threshold for detecting the motion status of the 4x4 macroblock. All calculations of the MDU are based on the 4x4 macroblock.

MDU_TIMEOUT

MDU_TIMEOUT is a timeout upper limit register.

Offset Address	Register Name	Total Reset Value
0x0084	MDU_TIMEOUT	0x0360_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_timeout																															
Reset	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_timeout	Maximum number of working cycles.

MDU_WND_SIZE

MDU_WND_SIZE is a SAD output window configuration register.

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Offset Address	Register Name	Total Reset Value
0x0090	MDU_WND_SIZE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sad_wnd_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sad_wnd_size	Size of the SAD output window. The calculations of the MDU are based on the 4x4 macroblock. After the sad_out_en bit of the mode register is enabled, the MDU adds the values of multiple 4x4 macroblocks based on the settings of sad_wnd_size, and outputs the value to the DDR. 0: 8x8 1: 16x16 (default)

MDU_MIN_OBJ_SIZE

MDU_MIN_OBJ_SIZE is the minimum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0094	MDU_MIN_OBJ_SIZE	0x0300_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	egsearch_timeout																min_obj_size_h								min_obj_size_w							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	egsearch_timeout	Boundary search timeout. If the number of points of an OBJ region is greater than the value, the boundary search of the OBJ region stops, and the search for the next region starts.
[15:8]	RW	min_obj_size_h	Minimum height of the OBJ region. The OBJ region whose height is smaller than this value is not reported. The value 1 of min_obj_size_h indicates a 4x4 macroblock.
[7:0]	RW	min_obj_size_w	Minimum width of the OBJ region. The OBJ region whose width is smaller than this value is not reported. The value 1 of min_obj_size_w indicates a 4x4 macroblock.

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MDU_MAX_OBJ_CNT

MDU_MAX_OBJ_CNT is the maximum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0098	MDU_MAX_OBJ_CNT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	max_obj_cnt	Maximum value for detecting the OBJ regions.

MDU_OBJ_CNT

MDU_OBJ_CNT is an OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x009C	MDU_OBJ_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index																obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index	Maximum OBJ region index. For the statistics register whose name does not contain the digital suffix, the statistics are obtained when the SAD is calculated and the OBJ region is searched for the first time based on the frame reference algorithm or background algorithm.
[15:0]	RO	obj_cnt	Number of detected OBJ regions.

MDU_MAX_OBJ_SIZE

MDU_MAX_OBJ_SIZE is a maximum OBJ region readback register.

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Offset Address	Register Name	Total Reset Value
0x00A0	MDU_MAX_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size	Maximum size of the OBJ region. This value is used to detect video occlusion. The value is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE

MDU_TOTAL_OBJ_SIZE is an all OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x00A4	MDU_TOTAL_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size	Total size of all OBJ regions. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field. The MDU adds the sizes of all OBJ regions. The size is in the unit of pixel. The size of each OBJ region is calculated as follows: number of 4x4 macroblocks x 16 **NOTE** • In some cases, the OBJ regions may overlap, and the total size of OBJ regions may be greater than the size of the original picture. • Based on the 4x4 macroblock, the height and width of each OBJ region are calculated as follows: Width = (Horizontal coordinate of the right point – Horizontal coordinate of the left point) + 1 Height = (Vertical coordinate of the bottom point – Vertical coordinate of the top point) + 1

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MDU_MOVE_PIX_CNT

MDU_MOVE_PIX_CNT is a motion pixel statistics register for an entire frame.

Offset Address	Register Name	Total Reset Value
0x00A8	MDU_MOVE_PIX_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt	Number of motion pixels of an entire frame. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field. Note: The value of this register is based on pixels. Therefore, the register value may be different from the value of total_obj_size.

MDU_OBJ_CNT1

MDU_OBJ_CNT1 is an OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00AC	MDU_OBJ_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index1																obj_cnt1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index1	Index of the maximum OBJ region based on the background. The registers with the suffix 1 indicate statistics registers. The statistics are obtained when the background algorithm is used and the SAD is calculated and the OBJ region is searched for the second time.
[15:0]	RO	obj_cnt1	Number of detected OBJ regions based on the background.

MDU_MAX_OBJ_SIZE1

MDU_MAX_OBJ_SIZE1 is a maximum OBJ region readback register based on the background.

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Offset Address	Register Name	Total Reset Value
0x00B0	MDU_MAX_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size1	Maximum size of the OBJ region based on the background. This value is used to detect video occlusion, and is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE1

MDU_TOTAL_OBJ_SIZE1 is a all OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B4	MDU_TOTAL_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size1	Sum of the sizes of all OBJ regions based on the background. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field.

MDU_MOVE_PIX_CNT1

MDU_MOVE_PIX_CNT1 is a motion pixel statistics register for an entire frame based on the background.

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Offset Address	Register Name	Total Reset Value
0x00B8	MDU_MOVE_PIX_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt1	Number of motion pixels of an entire frame based on the background. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field.

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Contents

9 IVE.....9-1
9.1 Overview.....9-1
9.2 Function Description.....9-1
9.3 Operating Mode.....9-3
9.3.1 Input and Output Data Formats.....9-3
9.3.2 Supported Functions.....9-7
9.4 Register Summary.....9-16

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Figures

Figure 9-1 Position of the IVE in the system 9-1
Figure 9-2 SP422 storage format 9-3
Figure 9-3 SP420 storage format 9-3
Figure 9-4 Storage format of the 8-bit single component data in the memory 9-4
Figure 9-5 Package storage format 9-4
Figure 9-6 Planar storage format 9-5
Figure 9-7 Storage format of the 16-bit single component data in the memory 9-5
Figure 9-8 Storage format of the 32-bit single component data in the memory 9-6
Figure 9-9 Storage format of the 64-bit single component data in the memory 9-6
Figure 9-10 Storage format of NCC output data in the memory 9-6
Figure 9-11 Storage format of CCL statistics in the memory (in sequence) 9-6
Figure 9-12 Storage format of 16-bit interleaving data (in the horizontal and vertical directions) in the memory 9-7

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Tables

Table 9-1 Summary of IVE registers (base address: 0x206A_0000).....9-16

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9 IVE

9.1 Overview

The intelligent video engine (IVE) module is used to accelerate hardware processing. It provides a series of basic calculation functions and some time-consuming functions used in the intelligent analysis algorithm.

Figure 9-1 Position of the IVE in the system

9.2 Function Description

The IVE has the following features:

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- DMA: Supports direct copying, alternative copying, and memory filling.
- Filter: Supports 5x5 template filtering.
- Color space conversion (CSC): Supports the color space conversion of YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV.
- FilterAndCSC: Combines 5x5 template filtering and CSC.
- Sobel: Supports the Sobel-like gradient calculation of 5x5 template.
- MagAndAng/Canny: Supports 5x5 template calculation and Canny edge extraction.
- Erode: Supports 5x5 template erode.
- Dilate: Supports 5x5 template dilate.
- Thresh\Thresh_S16\Thresh_U16: Supports image thresh processing.
- And\Or\Xor: Supports the AND, OR, or XOR operation on two images.
- Add\Sub: Deals with the weighted plus and minus of two images.
- Integ: Supports the integral calculation.
- Hist: Supports the histogram statistics.
- Map: Assigns values to images by using 256-level mapping.
- 16BitTo8Bit: Performs linear conversion from 16-bit data to 8-bit data.
- OrdStatFilter: Supports the sequence statistic filtering, including the median filtering, maximum filtering, and minimum filtering.
- Bernsen: Supports Bernsen thresh.
- NCC: Calculates the correlation coefficients of two images with the same size.
- CCL: Marks connected regions.
- GMM: Creates the GMM for a gray image and RGB image.
- LBP: Supports the calculation in simple partial thresh mode.
- NormGrad: Performs a normalized gradient calculation.
- LKOpticalFlow: Tracks the LK optical flow.
- STCorner: Detects the ShiTomasi point.
- GradFg: Supports the gradient foreground calculation.
- MatchBgModel\UpdateBgModel: Supports background match and background refresh.
- ANN_MLP_Predict: Predicts ANN_MLP.
- SVM_Predict: Predicts SVS_MLP.
- Supports separate soft reset.
- Supports 128-bit AXI bus and 32-bit APB.
- Supports linked-list interrupt, node interrupt, and timeout interrupt.
- Supports input formats includingSP 400, semi-planar 420 (SP420), semi-planar 422 (SP422), package, and planar.
- Supports output formats including SP400, SP420, SP422, package, and planar.
- Supports non-16-byte-aligned read and write addresses for some operators.

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9.3 Operating Mode

9.3.1 Input and Output Data Formats

The w and h in Figure 9-2 to Figure 9-12 indicate the width and height of images in pixels. Unless otherwise specified, the sequence for storing data is the same as that in the little endian system. The following sections use word as the storage unit. In actual applications, the data alignment format varies with operators. The input and output format for operators described in section 9.3.2 "Supported Functions" are also different.

Figure 9-2 SP422 storage format

Figure 9-3 SP420 storage format

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Figure 9-4 Storage format of the 8-bit single component data in the memory

Figure 9-5 Package storage format

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Figure 9-6 Planar storage format

Figure 9-7 Storage format of the 16-bit single component data in the memory

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Figure 9-8 Storage format of the 32-bit single component data in the memory

Figure 9-9 Storage format of the 64-bit single component data in the memory

Figure 9-10 Storage format of NCC output data in the memory

Figure 9-11 Storage format of CCL statistics in the memory (in sequence)

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Figure 9-12 Storage format of 16-bit interleaving data (in the horizontal and vertical directions) in the memory

9.3.2 Supported Functions

NOTE

For details about the resolutions supported by operators described in this section, see the *HiIVE API Reference*.

DMA

1. Direct copy mode

This mode allows you to quickly transfer the data of rectangle regions. In this mode, the source data is transferred to the destination region through the internal fast channel, and directly overwrites the data of the destination region.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 9-4.

2. Alternative copy mode

This mode allows you to transfer the data of rectangle regions indirectly. In this mode, the source data with a specified size is transferred to the destination region at a specified distance in horizontal and vertical directions.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 9-4.
- Others: The width of the source data must be an integral multiple of the distance.

3. Memset mode (3 bytes)

This mode allows you to set the memory in rectangle regions, and fill the destination region by three bytes.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.

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- Input and output formats: No input data is available. The output is 8-bit single component data, as shown in Figure 9-4.

4. Memset mode (8 bytes)

This mode allows you to set the memory in rectangle regions, with 8 byte as the unit for filling the target region.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: No input data is available. The output is 8-bit single component data, as shown in Figure 9-4.

Filter

The filter function allows the output of the source image after filtering it based on the 5x5 template.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- The following lists the three input and output formats:
  - Both the input and output are 8-bit single component data, as shown in Figure 9-4.
  - Both the input and output are SP420 data, as shown in Figure 9-3.
  - Both the input and output are SP422 data, as shown in Figure 9-2.

CSC

The CSC among YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV is supported.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar
  - Package > SP420; package > SP422
  - planar > SP420; planar > SP422

  Figure 9-3 and Figure 9-2 show the SP420 format and SP422 format respectively.

  Figure 9-5 shows the package format.

  Figure 9-6 shows the planar format.

FilterAndCSC

The FilterAndCSC function indicates that the YUV SP420/SP422 images are filtered based on the 5x5 template and then the color space is converted into YUV2RGB for output.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar

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Figure 9-3 and Figure 9-2 show the SP420 format and SP422 format respectively. Figure 9-5 shows the package format. Figure 9-6 shows the planar format.

Sobel

This function implements vertical and horizontal Sobel filtering based on the 5x5 template.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single component image, as shown in Figure 9-4.
  - Only H or V is outputted, as shown in Figure 9-7.
  - Both H and V are outputted, as shown in Figure 9-7.

MagAndAng

The MagAndAng indicates that gradient magnitude and angle are calculated. It supports the thresh operation for TO_ZERO.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 9-5.
  - The output is the 16-bit single component amplitude image, as shown in Figure 9-7.
  - The output is the 8-bit single component angle image, as shown in Figure 9-4.

Dilate

This function implements dilation of a binary image based on the 5x5 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 9-4.

Erode

This function implements erosion of a binary image based on the 5x5 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 9-4.

Thresh

This function performs thresh processing for an image using specified thresh. Eight modes are available.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 9-4.

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And

This function implements the calculation for source data 2 and 1, and outputs the data to the destination region.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single component data of source 1.
  - The input is an 8-bit single component data of source 2.
  - The output is the 8-bit single component destination data, as shown in Figure 9-4.

Sub

This function performs the subtraction of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - An 8-bit single component minuend.
  - An 8-bit single component subtrahend.
  - The 8-bit single component destination data, as shown in Figure 9-4

Or

This function performs the Or calculation of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The two input images are 8-bit single component images.
  - The output is the 8-bit single component image, as shown in Figure 9-4.

Integral

This function performs the calculation of integrogram and square sum integrogram, and supports the output of sum integrogram, square sum integrogram, and the combination of the sum integrogram and square sum integrogram (the accumulated component sum occupied the lower 28-bit, and the accumulated component square sum occupied the upper 36-bit).

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 9-4.
  - As shown in Figure 9-8, if a sum integrogram is outputted, the output is a 32-bit single component image. As shown in Figure 9-9, if a square sum integrogram is

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outputted or is outputted by combining with a sum integrogram, the output is a 64-bit single component image.

Histogram

This function performs the 256-segment histogram statistics. The input is a single component, and the output is the statistics of a 32 bit wide 256-segment histogram.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 9-4.
  - The output is the 32-bit single component data of the statistic result, as shown in Figure 9-8.

Thresh_S16

This function implements thresh processing of signed 16-bit data to signed 8-bit data. It supports four comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 9-7.
  - The output is the converted 8-bit single component data, as shown in Figure 9-4.

Thresh_U16

This function implements thresh processing of unsigned 16-bit data to unsigned 8-bit data. It supports two comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 9-7.
  - The output is the converted 8-bit single component data, as shown in Figure 9-4.

16BitTo8Bit

This function implements linear conversion of 16-bit data to 8-bit data. It supports four comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit data, as shown in Figure 9-7.
  - The output is the converted 8-bit data, as shown in Figure 9-4.

OrdStatFilter

Supports median filtering, maximum value filtering, and minimum filtering in sequence based on a 3x3 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats: Both the input and output are 8-bit single component images, as shown in Figure 9-4.

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Map

This function outputs new data by mapping the source data to the 256-segment unsigned 8-bit mapping configured by the user.

- Address alignment mode: Both the input and output must be byte-aligned, and the mapping and all the strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 9-4.
  - The input is the 8-bit wide mapping with a fixed entry length of 256.
  - The output is the 8-bit single component after mapping, as shown Figure 9-4.

Add

This function implements the sum of the weighted values of two gray images. The weight of the two images can be configured independently.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 9-4.
  - The output is the sum of data of 8-bit single component image, as shown Figure 9-4.

Xor

This function performs the Xor operation for two binary image data.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 9-4.
  - The output is the 8-bit single component data after performing the Xor operation, as shown in Figure 9-4.

NCC

This function calculates the cross correlation coefficient of two gray scale images of the same resolution.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 9-4.
  - The output contains three types of data, namely the accumulative product of two images, accumulative product of square sum of image 1, and the accumulative product of square sum of image 2 (in sequence), as shown in Figure 9-10.

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CCL

This function marks eight connected regions.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image, as shown in Figure 9-4.
  - The 16-bit output data indicates the minimum area of the output valid connected components.
  - The 8-bit output data indicates whether the area of the detected connected components is greater than the threshold.
  - The output is the coordinate and area of the circumscribed rectangle for each connected component, as shown in Figure 9-11. The original image is changed to an 8-bit single component image after the labeling of the connected components, as shown in Figure 9-4.

GMM

The GMM performs the inputted GMM background modeling for the gray images and RGB package images. Three or five Gauss models are supported.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image or RGB package image, as shown in Figure 9-4 and Figure 9-5.
  - The input is the model data.
  - The output is the 8-bit single component foreground data, as shown in Figure 9-4.
  - The output is the updated model data.
  - The output is the background data and the corresponding input is an 8-bit single component image or RGB package image, as shown in Figure 9-4 and Figure 9-5.

CannyHysEdge

- This function performs the threshold processing for the magnetic hysteresis, limited non-maximum values, outputted strong and weak edge image and the strong edge coordinate detected by the Canny edge.
- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component angle image, as shown in Figure 9-4.
  - The input is a 16-bit single component amplitude image, as shown in Figure 9-7.
  - The output is an 8-bit single edge mark image, as shown in Figure 9-4.
  - The output is a 32-bit single component data stack, as shown in Figure 9-8.
  - The output is the number of the 32-bit stack.

LBP

This function performs the partial thresh processing. It extracts the texture of partial images.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input data format:

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- The input is the 8-bit single component data.
- The output is the 8-bit single component destination data, as shown in Figure 9-4.

NormGrad

This function performs the normalized gradient calculation. The gradient components are all normalized to eight bits.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 9-4.
  - When out_fmt is set to 0x00, 0x01, or 0x02, the output is the 8-bit single component data, as shown in Figure 9-4. When out_fmt is set to 0x03, the output is the 16-bit interleaving data of H and V, as shown in Figure 9-12.

LKOpticalFlow

This function performs the optical flow estimation. A maximum of 200 points are supported.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image of the previous frame.
  - The input is an 8-bit single component image of the current frame, as shown in Figure 9-4.
  - The input is the angular coordinate, as shown in Figure 9-9. Lower 32 bits indicate the horizontal coordinate, and upper 32 bits indicate the vertical coordinate.
  - The angular motion vector is both the input and the output, as shown in Figure 9-9. Lower 32 bits indicate the status of success and failure of the tracing. Upper 32 bits indicate the angle displacement vector.

STBoxFltAndEigCalc

This function performs the box filtering during the point calculation, and calculates the response value and maximum response value of the points.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input data format:
  - The input is the vertical and horizontal 16-bit interleaving data, as shown in Figure 9-12.
  - The output is the 16-bit single component data, as shown in Figure 9-7.
  - The output is a 16-bit maxEig.

STCandiCorner

This function filters the points from Shi-Tomasi-like candidate points.

- Resolution: The resolution of the inputted two images should be the same.
- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:

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- The input is an 8-bit single component image.
- The output is the 8-bit single component image, as shown in Figure 9-4.

GradFg

This function calculates the gradient foreground based on the gradient of the background images and current frame images.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the background differential foreground images, as shown in Figure 9-4.
  - The input is the current gradient interleaving images.
  - The input is the background gradient interleaving images, as shown in Figure 9-12.
  - The output is gradient foreground images, as shown in Figure 9-4.

MatchBgModel

This function performs the background model matching based on CodeBook.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component current gray image.
  - The input is the foreground status flag (8-bit single component), as shown in Figure 9-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is the frame differential images (8-bit single component)
  - The output is the forehead status flag (8-bit single component), as shown in Figure 9-4.
  - The output is the 24-byte model data.
  - The output is a 64-bit statistic value.

UpdateBgModel

This function performs the background model refresh based on CodeBook.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the foreground status flag (8-bit single component), as shown in Figure 9-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is a background gray image (8-bit single component)
  - The output is a gray image in the change state (8-bit single component)
  - The output is a foreground image in the change state (8-bit single component), as shown in Figure 9-4.

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- The output is the pixel life period in the change state (16-bit single component), as shown in Figure 9-7.
- The output is the 24-byte model data.
- The output is a 64-bit statistic value.

ANN_MLP_Predict

This function performs the ANN_MLP prediction of a single feature sample, supporting a maximum of six hidden layers with 256 nerve cells at each layer.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 32-bit eigenvector data for the input layer, as shown in Figure 9-8.
  - The input is the 8-bit model data, as shown in Figure 9-4.
  - The input is the 16-bit lookup table data, as shown in Figure 9-7.
  - The output is the 32-bit output layer data, as shown in Figure 9-8.

SVM_Predict

This function performs the prediction of a single feature sample SVM.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 32-bit eigenvector data, as shown in Figure 9-8.
  - The input is the 8-bit supporting component, as shown in Figure 9-4.
  - The input is the 16-bit lookup table data, as shown in Figure 9-7.
  - The input is the 8-bit decision function, as shown in Figure 9-4.
  - The output is the 16-bit prediction vote result component, as shown in Figure 9-7.

9.4 Register Summary

Table 9-1 describes IVE registers.

Table 9-1 Summary of IVE registers (base address: 0x206A_0000)

Offset Address	Register	Description
0x0000	IVE_START	IVE start configuration register
0x0004	INT_EN	IVE interrupt enable register
0x0008	INT_RW	IVE clear interrupt register
0x000C	INT_STATUS	IVE interrupt status register
0x0010	LIST_POINTER	Linked list start address register
0x0014	IVE_STATUS	IVE working status register

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Offset Address	Register	Description
0x0018	IVE_TASK_ID	ID register for the tasks processed by the IVE at the previous time
0x0030	NODE_CLK_VALUE	Register for the number of cycles consumed by the preceding node
0x0034	CLK_GT_EN	Clock gating of the IVE internal module
0x0040	NODE_DONE_CNT	Register for the number of processed nodes
0x0044	LIST_DONE_CNT	Register for the number of processed linked lists
0x0054	AXI_INFO	Read and write outstanding number register
0x0060	IVE_OVER_TIME_THR	Overtime interrupt threshold register
0x0064	IVE_OVER_TIME_CNT	Register for the dynamic counting number of the operator working cycle
0x0068	CHAIN_STAT_CLK_VALUE	Register for the number of cycles consumed by the preceding linked list
0x006C	CHAIN_CYCLE_CNT	Register for the counting number of the current linked list cycles

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Contents

10 Video Interface 10-1
10.1 VICAP 10-1
10.1.1 Overview 10-1
10.1.2 Features 10-1
10.1.3 Function Description 10-2
10.1.4 Operating Mode 10-12
10.1.5 Register Summary 10-14
10.1.6 Register Description 10-27
10.2 VDP 10-163
10.2.1 Overview 10-163
10.2.2 Architecture 10-163
10.2.3 Operating Mode 10-164
10.2.4 Function Description 10-166
10.2.5 Register Summary 10-169
10.2.6 Register Description 10-176
10.3 MIPI RX 10-269
10.3.1 Overview 10-269
10.3.2 Features 10-269
10.3.3 Function Description 10-270
10.3.4 Operating Mode of the MIPI RX Controller 10-276
10.3.5 MIPI RX Register Summary 10-278
10.3.6 MIPI RX Register Description 10-281

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Figures

Figure 10-1 Functional block diagram of the VICAP module 10-1
Figure 10-2 Vertical timing of the 525-line 60 field/s video system 10-4
Figure 10-3 Vertical timing of the 625-line 50 field/s video system 10-5
Figure 10-4 Horizontal input timing of the HD interface 10-5
Figure 10-5 Vertical input timing of the HD interface 10-6
Figure 10-6 ITU-R BT.601 horizontal timing 10-6
Figure 10-7 Vertical sync timings in the NTSC standard 10-7
Figure 10-8 Vertical sync timings in the PAL standard 10-7
Figure 10-9 DC horizontal timing 10-8
Figure 10-10 DC vertical pulse timing 10-8
Figure 10-11 DC vertical line active timing 10-9
Figure 10-12 Relationship between the active video area and the horizontal/vertical blanking regions 10-9
Figure 10-13 YCbCr4:2:2 storage mode 10-11
Figure 10-14 Big endian and little endian storage modes 10-11
Figure 10-15 VICAP hardware workflow 10-13
Figure 10-16 Software Configuration 10-14
Figure 10-17 Block diagram of the VDP 10-163
Figure 10-18 MIPI RX workflow and its position in the system 10-269
Figure 10-19 CSI-2 data packet transmission mechanism 10-271
Figure 10-20 CSI-2 long packet format 10-272
Figure 10-21 CSI-2 short packet format 10-272
Figure 10-22 LVDS data transmission mode 10-273
Figure 10-23 LVDS synchronization mode 1 10-274
Figure 10-24 LVDS synchronization mode 2 10-275
Figure 10-25 HiSPI Packetized-SP data format 10-276
Figure 10-26 MIPI RX configuration process in MIPI mode 10-277

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Figure 10-27 MIPI RX configuration process in LVDS and HiSPI modes 10-278

Figure 10-17 Block diagram of the VDP 10-163

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Tables

Table 10-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data 10-3

Table 10-2 Formats of the SAV and EAV 10-3

Table 10-3 Valid SAV and EAV values 10-3

Table 10-4 ITU-R BT.656 error-correcting codes 10-3

Table 10-5 Summary of VICAP registers (base address: 0x2058_0000) 10-14

Table 10-6 Summary of VDP registers (base address: 0x205C_0000) 10-169

Table 10-7 Interfaces supported by the MIPI RX 10-270

Table 10-8 LVDS synchronization code format 10-272

Table 10-9 Summary of MIPI RX registers (base address: 0x2068_0000) 10-278

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10 Video Interfaces

10.1 VICAP

10.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface, BT.601 interface, BT.1120 interface, digital camera (DC) interface, or mobile industry processor interface receiver (MIPI RX), and stores the data in the specified addresses of the memory or transmits the data to the video processing subsystem (VPSS). Note that the MIPI RX includes the MIPI, low-voltage differential signal (LVDS), and high-speed serial pixel interface (HiSPI). The VICAP module has a built-in image signal processor (ISP) that can directly receive external raw data (bayer RGB data). Figure 10-1 shows the functional block diagram of the VICAP module.

Figure 10-1 Functional block diagram of the VICAP module

10.1.2 Features

The VICAP module has the following features:

- Maximum input resolution of 2592 x 1944
- One external interface with maximum 16-bit width
- One internal interface and 1-channel video processing in interlaced or progressive input mode
- BT.656, BT.601, BT.1120, DC, MIPI, LVDS, and HiSPI timings
- SMPTE293M or ITU-R BT.1358 timing (480p/576p)
- Flash trigger

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- Shuttle trigger
- Built-in ISP
- Noise reduction in fixed pattern noise (FPN) mode
- Anti-fog
- Automatic focus (AF), weighted 17x15 zones
- Digital image stabilizer (DIS)
- Adaptive color management (ACM)
- Dynamic contrast improvement (DCI)
- Horizontal chrominance down sampling (YUV444 to YUV422)
- Vertical chrominance down sampling (YUV422 to YUV420)
- Data obtained in a specified window
- Data output to the DDR in offline mode or to the VPSS in online mode
- Output storage modes
  - SPYCbCr 4:2:2 mode
  - SPYCbCr 4:2:0 mode

10.1.3 Function Description

10.1.3.1 Typical Applications

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR or transmits data to the VPSS online. By using different function modes configured by the system, the VICAP module can be connected to different external VI interfaces, supporting multiple external input devices.

The VICAP module has 21 pins, one clock, two external sync signals (multiplexed with other pins), 16 data lines, one shutter trigger signal, and one camera flash trigger signal.

It has one port and one channel. The port parses the timings of an interconnected chip, and the channel processes one video signal.

The VICAP module supports the following typical inputs:

- 1-channel 1080p
- 1-channel 5-megapixel

10.1.3.2 Function Implementation

ITU-R BT.656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of the active line data respectively. In video data streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 10-1 shows the format of the ITU-R BT.656 line data.

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Table 10-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				Line Blanking Region					Timing Reference Code				YCbCr 4:2:2 with 720 Active Pixels						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between the SAV and EAV depends on the special bit H. Both the SAV and EAV include the vertical blanking bit V and field indicator bit F. For details about the SAV and EAV, see Table 10-2.

Table 10-2 Formats of the SAV and EAV

Bit[7]	Bit[6] (F)	Bit[5] (V)	Bit[4] (H)	Bit[3:0] (P3−P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits can be used to correct 1-bit error and detect 2-bit errors. Table 10-3 describes the valid SAV and EAV values.

Table 10-3 Valid SAV and EAV values

Encoding	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	None
EAV	10011101	1	None
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	None
EAV	11011010	2	None
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits (P0, P1, P2, and P3) provide the error correction function. They are determined by the F, V, and H bits. See Table 10-4.

Table 10-4 ITU-R BT.656 error-correcting codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0

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F	V	H	P3	P2	P1	P0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

where

P0 = F^V^H

P1 = F^V

P2 = F^H

P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 10-2 shows the vertical timing of the 525-line 60 field/s video system, and Figure 10-3 shows the vertical timing of the 625-line 50 field/s video system.

Figure 10-2 Vertical timing of the 525-line 60 field/s video system

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Figure 10-3 Vertical timing of the 625-line 50 field/s video system

NOTE

The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

BT.1120 (HD) Interface Timings

The VICAP module supports the HD interface timings with separated Y/C inputs. In this case, two data ports are required. One is used to transfer luminance and the other one is used to transfer chrominance, as shown in Figure 10-4 and Figure 10-5.

Figure 10-4 Horizontal input timing of the HD interface

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Figure 10-5 Vertical input timing of the HD interface

ITU-R BT.601 YCbCr4:2:2

1. Horizontal timing

The horizontal pulse indicates the start of a new line, as shown in Figure 10-6. After hoff clock cycles, an input signal passes the line front blanking region and enters the line active data region. The value of hoff is 244 in the NTSC 525-line system or 264 in the PAL 625-line system. After act_width clock cycles, the input signal passes the line active data region and enters the line back blanking region. The value of act_width can be configured, and the typical value is 720 or 704. In addition, the horizontal sync polarity is configurable.

Figure 10-6 ITU-R BT.601 horizontal timing

2. Vertical timings

Based on the ITU-R BT.601 recommendation, the signals VSYNC and FIELD are vertical sync signals. The VSYNC pulse or FIELD transition indicates the start of the odd field or even field. The VICAP module supports two types of vertical sync.

Figure 10-7 shows VI vertical sync timings in the NTSC standard (525 lines), and Figure 10-8 shows VI vertical sync timings in the PAL standard (625 lines). VI_HSYNC_VD indicates the

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horizontal sync pulse, and VI_VSYNC_FIELD indicates the vertical sync pulse when VSYNC is 1 or field sync signal when VSYNC is 0.

Figure 10-7 Vertical sync timings in the NTSC standard

In NTSC interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low in the start position of line 4, retains low for three consecutive lines, and then becomes high in the start position of line 7. The VICAP module receives 240-line data from line 22 to line 261. The level of the vertical sync signal in field 2 becomes low in the middle of line 266, retains low for three consecutive lines, and then becomes high in the middle of line 269. The VICAP module receives 240-line data from line 285 to line 524.

Figure 10-8 Vertical sync timings in the PAL standard

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In PAL interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low in the start position of line 1, retains low for 2.5 consecutive lines, and then becomes high in the middle of line 3. The VICAP module receives 288-line data from line 24 to line 310. The level of the vertical sync signal in field 2 becomes low in the middle of line 313, retains low for 2.5 consecutive lines, and then becomes high in the start position of line 316. The VICAP module receives 288-line data from line 336 to line 623.

The preceding timings are typical BT.601 vertical timings. The number of lines from the start of the field to the active line, the number of field active lines, and vertical sync polarity can be configured.

DC Interface Timings

1. Horizontal timing

When a DC is connected to the VICAP module, VI_HSYNC_VD is the data valid signal. The polarity of this signal is configurable. Figure 10-9 shows the DC horizontal timing.

Figure 10-9 DC horizontal timing

2. Vertical timing

The VICAP module supports the vertical pulse timing and vertical line active timing, as shown in Figure 10-10 and Figure 10-11. The vertical sync polarity is configurable.

Figure 10-10 DC vertical pulse timing

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Figure 10-11 DC vertical line active timing

The preceding two timings are the same from the aspect of internal processing of the VICAP module. To be specific, the VICAP module considers the start of a frame after it detects a rising edge or a falling edge, and then detects the data active signal to check whether the current data is active.

10.1.3.3 Image Cropping

As shown in Figure 10-12, an active video starts from the end of the horizontal blanking region and vertical blanking region. The actual view range, however, is within the active video range. That is, compared with the boundary of the active video, the boundary of the actual view is shrunk, which avoids the boundary effect.

Figure 10-12 Relationship between the active video area and the horizontal/vertical blanking regions

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10.1.3.4 Internal Image Processing

AF Module

The AF implements AF statistics. Software adjusts the sensor based on statistics to implement AF. An image is divided into 17x15 zones (17 rows and 15 columns). The focus accuracy of each zone is separately measured. The weighted statistics or the statistics of each zone can be read.

DIS Module

The DIS module implements digital stabilization and DIS statistics. It calculates the final offset based on the horizontal offset (−128 to +128) and vertical offset (−128 to +128).

Anti-fog Module

The anti-fog strength of each zone can be configured, and a maximum of 16x16 zones are supported.

FPN Noise Reduction Module

The FPN noise reduction module supports line calibration mode and frame calibration mode. The number of frames to be calibrated can be configured.

ACM Module

The ACM implements automatic color management, corrects the hue offset and saturation loss caused during video transferring, compensates the differences between color gamuts (for the same display effect on various screens), and shows colors based on user preferences and styles.

DCI Module

The DCI module automatically adjusts the image luminance and contrast based on luminance statistics. No matter whether an image is too dark, too bright, or monotonic or has a too large contrast, its display effect is satisfied after it is adjusted by the DCI module.

10.1.3.5 Image Storage Modes

The supported image storage modes include:

- Semi-planar YCbCr storage mode

  After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.
- For one line, the luminance component and chrominance component are stored separately and consecutively.
- For two consecutive lines, the components are stored based on the offset parameter. This parameter defines the storage stride between the starts of two lines. The storage positions in the DDR of the luminance component and chrominance component are specified by the start address base_addr. Figure 10-13 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

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Figure 10-13 YCbCr4:2:2 storage mode

In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word in big endian mode or little endian mode. Figure 10-14 shows the big endian and little endian storage modes of the luminance and chrominance components.

Figure 10-14 Big endian and little endian storage modes

The VICAP module supports only the DDR that stores data in little endian mode.

10.1.4 Operating Mode

10.1.4.1 reg_newer Function

- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configures the VICAP attribute register.

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  - Writes 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts receiving data, generates the register update interrupt (reg_update_int), and sets the hardware to busy state.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:
  - If reg_newer is 0, the VICAP module does not receive the data of the next field or frame.
  - If reg_newer is 1, the VICAP module receives the data of the next field or frame.

10.1.4.2 VICAP Hardware Workflow

Figure 10-15 shows the VICAP hardware workflow.

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Figure 10-15 VICAP hardware workflow

Each time after the VICAP module receives the data of a field or frame, it checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, software has updated or checked corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer is 1 and a new field or frame arrives.

10.1.4.3 Software Configuration Workflow

Figure 10-16 shows the software configuration process in interrupt mode.

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Figure 10-16 Software Configuration

When the BT.656, BT.1120, MIPI Rx, or DC interface is used, timing registers do not need to be configured. If the BT.601 interface is used, timing registers including vertical sync registers and horizontal sync registers need to be configured.

10.1.5 Register Summary

Table 10-5 describes VICAP registers.

Table 10-5 Summary of VICAP registers (base address: 0x2058_0000)

Offset Address	Register	Description	Page
0x0010	AXI_CFG	Bus configuration register	10-27
0x0014	MAC_CFG	MAC configuration register	10-27

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Offset Address	Register	Description	Page
0x0030	CH_SEL	Channel input data selection register	10-28
0x0040	DES_SEL	DES input data selection register	10-29
0x0050	ISP_SEL	ISP input data selection register	10-29
0x00E0	APB_TIMEOUT	APB timeout register	10-30
0x00F0	VICAP_INT	Interrupt status register	10-30
0x00F8	VICAP_INT_MASK	Interrupt mask register	10-31
0x0100	PT_INTF_MOD	Port mode register	10-32
0x0110	PT_OFFSET0	Component 0 offset register	10-33
0x0114	PT_OFFSET1	Component 1 offset register	10-33
0x0118	PT_OFFSET2	Component 2 offset register	10-34
0x0120	PT_BT656_CFG	BT.656 configuration register	10-35
0x0130	PT_UNIFY_TIMING_CFG	Timing configuration register	10-36
0x0134	PT_GEN_TIMING_CFG	Timing recovery module configuration register	10-38
0x0140	PT_UNIFY_DATA_CFG	Data configuration register	10-38
0x0150	PT_YUV444_CFG	YUV444 configuration register	10-39
0x0180	PT_INTF_HFB	Horizontal front blanking width register	10-40
0x0184	PT_INTF_HACT	Horizontal active width register	10-40
0x0188	PT_INTF_HBB	Horizontal back blanking width register	10-41
0x018C	PT_INTF_VFB	Vertical front blanking width register	10-41
0x0190	PT_INTF_VACT	Vertical active width register	10-42
0x0194	PT_INTF_VBB	Vertical back blanking width register	10-42
0x0198	PT_INTF_VBFB	Vertical bottom front blanking width register	10-42
0x019C	PT_INTF_VBACT	Vertical bottom active width register	10-43
0x01A0	PT_INTF_VBBB	Vertical bottom back blanking width register	10-43
0x01A4	PT_ID_CFG	ID configuration register	10-44
0x01B0	PT_FLASH_CFG	Flash configuration register	10-44
0x01C0	PT_FLASH_CYC0	Flash timing 0 width register	10-45

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Offset Address	Register	Description	Page
0x01C4	PT_FLASH_CYC1	Flash timing 1 width register	10-46
0x01D0	PT_SHUTTER_CYC0	Shutter timing 0 width register	10-46
0x01D4	PT_SHUTTER_CYC1	Shutter timing 1 width register	10-47
0x01D8	PT_SHUTTER_CYC2	Shutter timing 2 width register	10-47
0x01DC	PT_SHUTTER_CYC3	Shutter timing 3 width register	10-47
0x01E0	PT_STATUS	Port status register	10-48
0x01E4	PT_BT656_STATUS	BT656 status register	10-48
0x01EC	PT_SIZE	Input picture size register	10-49
0x01F0	PT_INT	Port interrupt status register	10-49
0x01F8	PT_INT_MASK	Port interrupt mask register	10-50
0x0200	DES_CTRL	DES control register	10-51
0x0204	DES_REG_NEWER	Capture control register	10-52
0x0210	DES_ID_CFG	DES RX ID selection register	10-52
0x0220	DES_CROP_CFG	Crop enable register	10-53
0x0230	DES_CROP0_START	Crop start position register for region 0	10-53
0x0234	DES_CROP0_SIZE	Crop size configuration register for region 0	10-54
0x0270	DES_CFG	DES configuration register	10-54
0x0274	DES_CMP_FRM_LEN	DES compressed data length register	10-55
0x0284	DES_SIZE	DES storage size register	10-55
0x0290	DES_FADDR	DES storage base address register	10-56
0x029C	DES_BUF_CFG	DES bus buffer control register	10-56
0x02F0	DES_INT	DES raw interrupt register	10-57
0x02F8	DES_MASK	DES interrupt mask register	10-58
0x0500	LINE_BUF_CFG	LINE_BUF control register	10-59
0x0504	LINE_BUF_REG_NEWER	LINE_BUF updating register	10-60
0x0510	LINE_BUF_ID_CFG	LINE_BUF RX ID selection register	10-60
0x0520	LINE_BUF_CROP_CFG	Crop enable register	10-60
0x0530	LINE_BUF_CROP0_START	Crop start position register for region 0	10-61

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Offset Address	Register	Description	Page
0x0534	LINE_BUF_CROP0_SIZE	Crop size configuration register for region 0	10-61
0x0550	LINE_BUF_WIDTH	LINE_BUF picture width register	10-62
0x0554	LINE_BUF_HEIGHT	LINE_BUF picture height register	10-62
0x05F0	LINE_BUF_INT	LINE_BUF raw interrupt register	10-63
0x05F8	LINE_BUF_MASK	LINE_BUF interrupt mask register	10-64
0x0600	SRC_CTRL	SRC control register	10-65
0x0604	SRC_REG_NEWER	Capture control register	10-66
0x0670	SRC_CFG	SRC configuration register	10-66
0x0674	SRC_DCMP_FRM_LEN	Read compressed data length configuration register for the SRC channel	10-67
0x0684	SRC_SIZE	SRC storage size register	10-68
0x0690	SRC_FADDR	SRC storage base address register	10-68
0x069C	SRC_BUF_CFG	SRC bus buffer control register	10-68
0x06F0	SRC_INT	SRC raw interrupt register	10-69
0x06F8	SRC_MASK	SRC interrupt mask register	10-70
0x1000	CH_CTRL	Channel control register	10-71
0x1004	CH_REG_NEWER	Capture control register	10-72
0x1020	CH_SUM_Y	Input picture luminance statistics register	10-72
0x1034	CH_DLY_CFG	Channel input picture start interrupt delay configuration register	10-73
0x1080	CH_WCH_Y_CFG	Y component configuration register for the WCH module	10-73
0x1084	CH_WCH_Y_SIZE	Y component storage size register for the WCH module	10-74
0x1090	CH_WCH_Y_FADDR	Y component storage base address register for the WCH module	10-75
0x1094	CH_WCH_Y_HADDR	Y component header information storage base address register for the WCH module	10-75
0x1098	CH_WCH_Y_STRIDE	Y component line offset register for the WCH module	10-76

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Offset Address	Register	Description	Page
0x10A0	CH_WCH_C_CFG	C component configuration register for the WCH module	10-76
0x10A4	CH_WCH_C_SIZE	C component storage size register for the WCH module	10-77
0x10B0	CH_WCH_C_FADDR	C component storage base address register for the WCH module	10-78
0x10B4	CH_WCH_C_HADDR	C component header information storage base address register for the WCH module	10-78
0x10B8	CH_WCH_C_STRIDE	C component line offset register for the WCH module	10-79
0x10F0	CH_INT	Channel raw interrupt register	10-79
0x10F8	CH_INT_MASK	Channel interrupt mask register	10-81
0x1100	CH_CROP_CFG	Crop enable register	10-82
0x1110	CH_CROP0_START	Crop start position register for region 0	10-83
0x1114	CH_CROP0_SIZE	Crop size configuration register for region 0	10-83
0x1200	CH_CSC_CFG	Color space conversion (CSC) configuration register	10-84
0x1210	CH_CSC_COEF0	CSC coefficient register 0	10-84
0x1214	CH_CSC_COEF1	CSC coefficient register 1	10-85
0x1218	CH_CSC_COEF2	CSC coefficient register 2	10-86
0x121C	CH_CSC_COEF3	CSC coefficient register 3	10-86
0x1220	CH_CSC_COEF4	CSC coefficient register 4	10-87
0x1230	CH_CSC_IN_DC0	CSC input DC component register 0	10-87
0x1234	CH_CSC_IN_DC1	CSC input DC component register 1	10-88
0x1238	CH_CSC_OUT_DC0	CSC output DC component register 0	10-88
0x123C	CH_CSC_OUT_DC1	CSC output DC component register 1	10-89
0x1300	CH_DITHER_CFG	Dither configuration register	10-89
0x1400	CH_ACM_CTRL	ACM control register	10-90
0x1404	CH_ACM_ADJ	ACM processed pixel change register	10-91
0x1410	CH_ACM_SIZE	ACM processed picture size register	10-92
0x1414	CH_ACM_PARA_ADDR	ACM coefficient loading address configuration register	10-92

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Offset Address	Register	Description	Page
0x1420	CH_ACM_PARA_UP	ACM parameter update register	10-92
0x1500	CH_SKIP_Y_CFG	Y skip configuration register	10-93
0x1510	CH_SKIP_C_CFG	C skip configuration register	10-93
0x1600	CH_HCDS_CFG	Horizontal chrominance down sampling configuration register	10-94
0x1604	CH_HCDS_OFFSET	Horizontal chrominance down sampling offset register	10-94
0x1610	CH_HCDS_IN_SIZE	Horizontal chrominance down sampling input size configuration register	10-94
0x1614	CH_HCDS_OUT_SIZE	Horizontal chrominance down sampling output size configuration register	10-95
0x1620	CH_HCDS_COEF0	Horizontal chrominance down sampling coefficient register 0	10-96
0x1624	CH_HCDS_COEF1	Horizontal chrominance down sampling coefficient register 1	10-96
0x1628	CH_HCDS_COEF2	Horizontal chrominance down sampling coefficient register 2	10-97
0x1700	CH_VCDS_CFG	Vertical chrominance down sampling configuration register for large streams	10-97
0x1704	CH_VCDS_COEF	Vertical chrominance down sampling coefficient register for large streams	10-97
0x1800	CH_CLIP_Y_CFG	Luminance clamp configuration register	10-98
0x1804	CH_CLIP_C_CFG	Chrominance clamp configuration register	10-98
0x01900	CH_UV2C_CFG	UV2C_CFG configuration register	10-99
0x1A00	CH_DIS_CFG	CH_DIS enable register	10-99
0x1A04	CH_DIS_BLK	CH_DIS block configuration register	10-100
0x1A10	CH_DIS_V0POS	CH_DIS vertical PRJ0 block address register	10-101
0x1A14	CH_DIS_V4POS	CH_DIS vertical PRJ4 block address register	10-101
0x1A18	CH_DIS_V8POS	CH_DIS vertical PRJ8 block address register	10-101

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Offset Address	Register	Description	Page
0x1A20	CH_DIS_V0POSE	CH_DIS vertical PRJ0 block address register	10-102
0x1A24	CH_DIS_V4POSE	CH_DIS vertical PRJ4 block address register	10-102
0x1A28	CH_DIS_V8POSE	CH_DIS vertical PRJ8 block address register	10-103
0x1A30	CH_DIS_H0POS	CH_DIS horizontal PRJ0 block address register	10-103
0x1A34	CH_DIS_H4POS	CH_DIS horizontal PRJ4 block address register	10-104
0x1A38	CH_DIS_H8POS	CH_DIS horizontal PRJ8 block address register	10-104
0x1A40	CH_DIS_H0POSE	CH_DIS horizontal PRJ0 block address register	10-105
0x1A44	CH_DIS_H4POSE	CH_DIS horizontal PRJ4 block address register	10-105
0x1A48	CH_DIS_H8POSE	CH_DIS horizontal PRJ8 block address register	10-106
0x1B00~0x1B68	CH_DIS_VSTAT	Vertical DIS statistics register for all CH_DIS blocks	10-106
0x1B80~0x1Be8	CH_DIS_HSTAT	Horizontal DIS statistics register for all CH_DIS blocks	10-107
0x1C00	CH_VPDCICTRL	DCI control register	10-107
0x1C04	CH_VPDCIHPOS	DCI algorithm horizontal adjustment region register	10-109
0x1C08	CH_VPDCIVPOS	DCI algorithm vertical adjustment region register	10-110
0x1C0C	CH_VPDCIHISBLD	DCI histogram statistics weighted coefficient register	10-111
0x1C10	CH_VPDCIHISOFT	DCI histogram statistics offset register	10-111
0x1C14	CH_VPDCIHISCOR	DCI histogram coring register	10-111
0x1C18	CH_VPDCIMERBLD	Blend value register for the DCI adjustment unit	10-112
0x1C1C	CH_VPDCIADJWGT	DCI manually configured curve weight register	10-112
0x1C20	CH_VPDCICLIP0	DCI curve 0 weight range register	10-113
0x1C24	CH_VPDCICLIP1	DCI curve 1 weight range register	10-113

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Offset Address	Register	Description	Page
0x1C28	CH_VPDCICLIP2	DCI curve 2 weight range register	10-114
0x1C2C	CH_VPDCIGLBGAIN	Global gain register for the DCI luminance adjustment unit	10-114
0x1C30	CH_VPDCIPOSTHR0	Positive adjustment threshold register 0 for the DCI adjustment unit	10-115
0x1C34	CH_VPDCIPOSTHR1	Positive adjustment threshold register 1 for the DCI adjustment unit	10-115
0x1C38	CH_VPDCIPOSGAIN0	Positive adjustment gain register 0 for the DCI adjustment unit	10-116
0x1C3C	CH_VPDCIPOSGAIN1	Positive adjustment gain register 1 for the DCI adjustment unit	10-117
0x1C40	CH_VPDCIPOSSLP0	Positive adjustment slope register 0 for the DCI adjustment unit	10-117
0x1C44	CH_VPDCIPOSSLP1	Positive adjustment slope register 1 for the DCI adjustment unit	10-118
0x1C48	CH_VPDCIPOSSLP2	Positive adjustment slope register 2 for the DCI adjustment unit	10-119
0x1C4C	CH_VPDCINEGTHR0	Negative adjustment threshold register 0 for the DCI adjustment unit	10-119
0x1C50	CH_VPDCINEGTHR1	Negative adjustment threshold register 1 for the DCI adjustment unit	10-119
0x1C54	CH_VPDCINEGGAIN0	Negative adjustment gain register 0 for the DCI adjustment unit	10-120
0x1C58	CH_VPDCINEGGAIN1	Negative adjustment gain register 1 for the DCI adjustment unit	10-121
0x1C5C	CH_VPDCINEGSLP0	Negative adjustment slope register 0 for the DCI adjustment unit	10-121
0x1C60	CH_VPDCINEGSLP1	Negative adjustment slope register 1 for the DCI adjustment unit	10-122
0x1C64	CH_VPDCINEGSLP2	Negative adjustment slope register 2 for the DCI adjustment unit	10-123
0x1E00	CH_SPLIT_CFG	Split enable register	10-123
0x1E0C	CH_SPLIT_VERSION	Split version register	10-123
0x1E10	CH_SPLIT_DATA_CFG	Split configuration register	10-124
0x1E14	CH_SPLIT_DATA_VERSION	Split data version register	10-126

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Offset Address	Register	Description	Page
0x1E18	CH_SPLIT_DATA_BIT WIDTH	Split data bit width register	10-126
0x1EE4	CH_SPLIT_CTRL_I	Split register update control register	10-127
0x1EEC	CH_SPLIT_UPDATE	Split register update register	10-127
0x2000	CH_AF_CFG	AF control register	10-128
0x2010	CH_AF_ZONE	AF block configuration register	10-129
0x2014	CH_AF_CROP_START	AF crop start coordinate configuration register	10-130
0x2018	CH_AF_CROP_SIZE	AF crop picture size configuration register	10-130
0x2020	CH_AF_IIRG0	AF IIR filtering parameter 0 register	10-131
0x2024	CH_AF_IIRG1	AF IIR filtering parameter 1 register	10-131
0x2028	CH_AF_IIRG2	AF IIR filtering parameter 2 register	10-132
0x202C	CH_AF_IIRG3	AF IIR filtering parameter 3 register	10-132
0x2030	CH_AF_IIRG4	AF IIR filtering parameter 4 register	10-133
0x2034	CH_AF_IIRG5	AF IIR filtering parameter 5 register	10-133
0x2038	CH_AF_IIRG6	AF IIR filtering parameter 6 register	10-134
0x2040	CH_AF_SHIFT	AF IIR filtering shift parameter register	10-134
0x2050	CH_AF_FIRH0	AF FIR filtering parameter 0 register	10-135
0x2054	CH_AF_FIRH1	AF FIR filtering coefficient 1 register	10-136
0x2058	CH_AF_FIRH2	AF FIR filtering coefficient 2 register	10-136
0x205C	CH_AF_FIRH3	AF FIR filtering coefficient 3 register	10-137
0x2060	CH_AF_FIRH4	AF FIR filtering coefficient 4 register	10-137
0x2070	CH_AF_IIRTHRE	AF IIR filtering threshold register	10-138
0x2074	CH_AF_FIRTHRE	AF FIR filtering threshold register	10-138
0x2078	CH_AF_ACC_SHIFT	AF statistics shift register	10-139
0x207C	CH_AF_CNT_SHIFT	AF count value shift register	10-139
0x20E0	CH_AF_SIZE	AF picture size register	10-140
0x2100–0x2CF0	CH_AF_STAT_RDATA	Read statistics register for AF blocks	10-140
0x10000	ISP_MAX_ADDR	ISP buffer maximum address register	10-141

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Offset Address	Register	Description	Page
0x10004	ISP_MAX_ADDR_DIS_Y	DIS Y depth maximum address register	10-142
0x10008	ISP_MAX_ADDR_SINTER1	ISP sinter buffer 1 maximum address register	10-142
0x1000C	ISP_MAX_ADDR_SINTER2	ISP sinter buffer 2 maximum address register	10-143
0x10010	ISP_TIMING	ISP timing configuration register	10-143
0x10020	ISP_BYTE_EN	ISP byte enable register	10-143
0x10024	ISP_MAX_ADDR_FSTITCH	ISP FSTITCH maximum address register	10-144
0x10028	ISP_CH_SWITCH	ISP input switch register	10-144
0x10030	ISP_CROP_CFG	Crop enable register	10-145
0x10034	ISP_CROP_WIN	Crop window register	10-146
0x10038	ISP_CROP0_START	Crop start position register for region 0	10-146
0x1003C	ISP_CROP0_SIZE	Crop size configuration register for region 0	10-147
0x10040	ISP_CROP1_START	Crop start position register for region 1	10-147
0x10044	ISP_CROP1_SIZE	Crop size configuration register for region 1	10-148
0x100F0	ISP_INT	ISP interrupt indicator register	10-148
0x100F8	ISP_INT_MASK	ISP interrupt mask register	10-149
0x10100	ISP_FPN_CFG	FPN configuration register	10-150
0x10104	ISP_FPN_CALIB_START	FPN calibration start signal register	10-151
0x10108	ISP_FPN_CORR_CFG	FPN correction enable register	10-152
0x1010C	ISP_FPN_STAT	FPN calibration status register	10-152
0x10110	ISP_FPN_WHITE_LEVEL	FPN calibration white point configuration register	10-153
0x10118	ISP_FPN_DIVCOEF	FPN calibration division coefficient register	10-153
0x1011C	ISP_FPN_FRAMELOG2	FPN calibrated frame number register	10-154
0x10120	ISP_FPN_SUM0	FPN calibration accumulated sum low register	10-154
0x10124	ISP_FPN_SUM1	FPN calibration accumulated sum high register	10-155

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Offset Address	Register	Description	Page
0x10130	ISP_FPN_CORR0	FPN correction configuration register 0	10-155
0x10134	ISP_FPN_CORR1	FPN correction configuration register 1	10-156
0x10140	ISP_FPN_SHIFT	FPN shift configuration register	10-156
0x10150	ISP_FPN_MAX_O	FPN maximum output value register	10-157
0x101D0	ISP_FPN_PIC_SIZE	FPN picture size register	10-157
0x101D4	ISP_FPN_REG_UPDATE	Register update register	10-157
0x101D8	ISP_FPN_UPDATE_MODE	Register update mode register	10-158
0x10200	ISP_DITHER_CFG	Dither configuration register	10-158
0x10300	ISP_VB_CFG0	Vertical blanking clock gating configuration register 0	10-159
0x10304	ISP_VB_CFG1	Vertical blanking clock gating configuration register 1	10-159
0x10310	ISP_VB_CLKNUM	Wait clock number configuration register for vertical blanking clock gating	10-160
0x10314	ISP_VB_DLYN	Wait clock number configuration register for disabling the clock after the vertical blanking clock gating indicator is valid	10-160
0x10318	ISP_VB_TRIG	Vertical blanking clock count reset trigger configuration register	10-161
0x1031C	ISP_VB_GT_STAT	Vertical blanking clock gating status register	10-161
0x103F0	ISP_VB_SIZE	Picture size register	10-162
0x12000–0x1343C	ISP_FPN_MEM	FPN line mode memory register	10-162
0x19000	ISP_DEHAZE_CFG	Dehaze enable register	10-163
0x1900C	ISP_DEHAZE_VERSION	Dehaze version register	10-163
0x19010	ISP_DEHAZE_PRE_UPDATE	Dehaze statistics result update register	10-164
0x19014	ISP_DEHAZE_BLK_SIZE	Dehaze block size configuration register	10-164
0x19018	ISP_DEHAZE_BLK_NUM	Dehaze block number configuration register	10-165

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Offset Address	Register	Description	Page
0x1901C	ISP_DEHAZE_DC_SIZE	Bilinear interpolation point number configuration register	10-165
0x19020	ISP_DEHAZE_X	Configuration register for the horizontal phase difference between the pixels of the dehaze enlarged picture	10-166
0x19024	ISP_DEHAZE_Y	Configuration register for the vertical phase difference between the pixels of the dehaze enlarged picture	10-166
0x19028	ISP_DEHAZE_STAT_MODE	Dehaze statistics mode control register	10-167
0x1902C	ISP_DEHAZE_NEG_MODE	Dehaze inversion enable register	10-168
0x19030	ISP_DEHAZE_AIR	Dehaze airglow configuration register	10-169
0x19034	ISP_DEHAZE_THLD	T threshold coefficient configuration register	10-169
0x19038	ISP_DEHAZE_GSTRTH	T calculation coefficient configuration register	10-169
0x1903C	ISP_DEHAZE_BLTHLD	Minimum value filtering threshold coefficient configuration register	10-170
0x190E4	ISP_DEHAZE_CTRL_I	Dehaze register update control register	10-170
0x190EC	ISP_DEHAZE_UPDATE	Dehaze register update register	10-171
0x190F0	ISP_DEHAZE_SIZE	Dehaze picture size register	10-171
0x19100~0x191FC	ISP_DEHAZE_MINSTAT	Dehaze minimum value statistics register	10-172
0x19200~0x192FC	ISP_DEHAZE_PRESTAT	Dehaze processed minimum value statistics register after processing	10-172
0x19400~0x197FC	ISP_DEHAZE_MAXSTAT	Dehaze maximum value statistics register	10-173
0x19800~0x19BFC	ISP_DEHAZE_LUT	Dehaze strength lookup table (LUT) configuration register	10-173

10.1.6 Register Description

AXI_CFG

AXI_CFG is a bus configuration register.

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Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x1010_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				r_outstanding	reserved	w_outstanding	reserved
Reset	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	r_outstanding	Number of read request outstandings. The value range is [1, 8].
[11:8]	RO	reserved	Reserved
[7:4]	RW	w_outstanding	Number of write request outstandings. The value range is [1, 8].
[3:0]	RO	reserved	Reserved

MAC_CFG

MAC_CFG is an MAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				r_req_prio		w_req_prio	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	r_req_prio	Read request arbitration priority. 0: low priority 1: high priority bit 0: SRC0 read request priority bit 1: SRC1 read request priority bit 2: reserved bit 3: reserved bit 4: reserved bit 5: reserved bit 6: reserved bit 7: reserved

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Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																r_req_prio								w_req_prio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	w_req_prio	Write request arbitration priority. 0: low priority 1: high priority bit 0: DES0 write request priority bit 1: reserved bit 2: reserved bit 3: reserved bit 4: reserved bit 5: reserved bit 6: reserved bit 7: reserved

CH_SEL

CH_SEL is a channel input data selection register.

Offset Address	Register Name	Total Reset Value
0x0030	CH_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	ch_sel	Channel input data select. 000: The channel connects to the port. 001: The channel connects to the ISP. Other values: reserved

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DES_SEL

DES_SEL is a DES input data selection register.

Offset Address	Register Name	Total Reset Value
0x0040	DES_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														des_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1:0]	RW	des_sel	DES input data select. 00: The DES connects to the port. 01: The DES connects to LINE_BUF. 10: The DES connects to the FPN. 11: reserved

ISP_SEL

ISP_SEL is an ISP input data selection register.

Offset Address	Register Name	Total Reset Value
0x0050	ISP_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														isp_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	isp_sel	ISP input data select. 00: The ISP connects to LINE_BUF. 01: The ISP connects to SRC0. 10: The ISP connects to SRC1. 11: reserved

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APB_TIMEOUT

APB_TIMEOUT is an APB timeout register.

Offset Address	Register Name	Total Reset Value
0x00E0	APB_TIMEOUT	0x8000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved															timeout															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timeout enable. 0: disabled 1: enabled
[30:16]	RO	reserved	Reserved
[15:0]	RW	timeout	Timeout threshold (in APB clock).

VICAP_INT

VICAP_INT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															int_isp	reserved										int_buf	int_src1	int_src0	int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	int_isp	ISP interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[15:6]	RO	reserved	Reserved
[5]	RO	int_buf	LINE_BUF interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.

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[4]	RO	int_src1	SRC1 interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_src0	SRC0 interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_des0	DES0 interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_ch	Channel interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_pt	Port interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.

VICAP_INT_MASK

VICAP_INT_MASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															int_isp	reserved										int_buf	int_src1	int_src0	int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	int_isp	ISP interrupt enable. 0: masked 1: enabled
[15:6]	RO	reserved	Reserved
[5]	RW	int_buf	LINE_BUF interrupt enable. 0: masked 1: enabled

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[4]	RW	int_src1	SRC1 interrupt enable. 0: masked 1: enabled
[3]	RW	int_src0	SRC0 interrupt enable. 0: masked 1: enabled
[2]	RW	int_des0	DES0 interrupt enable. 0: masked 1: enabled
[1]	RW	int_ch	Channel interrupt enable. 0: masked 1: enabled
[0]	RW	int_pt	Port interrupt enable. 0: masked 1: enabled

PT_INTF_MOD

PT_INTF_MOD is a port mode register.

Offset Address	Register Name	Total Reset Value
0x0100	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Port enable. 0: disabled 1: enabled
[30:1]	RO	reserved	Reserved
[0]	RW	mode	Timing mode. 0: external sync 1: BT.656

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PT_OFFSET0

PT_OFFSET0 is a component 0 offset register.

Offset Address	Register Name	Total Reset Value
0x0110	PT_OFFSET0	0xFFF0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 0 offset.

PT_OFFSET1

PT_OFFSET1 is a component 1 offset register.

Offset Address	Register Name	Total Reset Value
0x0114	PT_OFFSET1	0xFFF0_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 1 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 1 offset.

PT_OFFSET2

PT_OFFSET2 is a component 2 offset register.

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Offset Address	Register Name	Total Reset Value
0x0118	PT_OFFSET2	0xFFF0_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved									offset					
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 2 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 2 offset.

PT_BT656_CFG

PT_BT656_CFG is a BT.656 configuration register.

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31]	RW	enable	BT.656 enable. 0: disabled 1: enabled
[30:11]	RO	reserved	Reserved.
[10]	RW	field_inv	Reverse control. 0: not reversed 1: reversed
[9]	RW	vsync_inv	Reverse control. 0: not reversed 1: reversed

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[8]	RW	hsync_inv	Reverse control. 0: not reversed 1: reversed
[7:4]	RO	reserved	Reserved
[3:0]	RW	mode	Mode select. mode[0] 0: hsync is not an active signal. 1: hsync is an active signal. mode[1] 0: The hsync output is active low. 1: The hsync output is active high. mode[3:2] 00: Component 0 is parsed. 01: Component 1 is parsed. 10: Component 2 is parsed. 11: reserved

PT_UNIFY_TIMING_CFG

PT_UNIFY_TIMING_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					field_inv	field_sel		reserved				vsync_mode		vsync_inv		vsync_sel	reserved	hsync_mode		hsync_and		hsync_inv		hsync_sel	reserved					de_inv	de_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	field_inv	Field inverse (level-1 field processing). 0: not inverted 1: inverted
[25:24]	RW	field_sel	Field source select (level-0 field processing). 00: input field 01: input vsync 10: detected based on the relationship between vsync and hsync 11: fixed at 0

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[23:21]	RO	reserved	Reserved
[20:19]	RW	vsync_mode	vsync processing mode (level-2 vsync processing). 00: not processed 01: detect the rising edge 10: detect the rising edge and falling edge 11: reserved
[18]	RW	vsync_inv	vsync inversion (level-1 vsync processing). 0: not inverted 1: inverted
[17:16]	RW	vsync_sel	vsync source select (level-0 vsync processing). 00: input vsync 01: input field 10: fixed at 0 11: reserved
[15]	RO	reserved	Reserved
[14:13]	RW	hsync_mode	hsync processing mode (level-3 hsync processing). 0: not processed 1: detect the rising edge
[12:11]	RW	hsync_and	Whether hsync is operated with the result of level-1 vsync processing (level-2 hsync processing). 00: not processed 01: ANDed 10: exclusive ORed 11: reserved
[10]	RW	hsync_inv	hsync inversion (level-1 hsync processing). 0: not inverted 1: inverted
[9:8]	RW	hsync_sel	hsync source select (level-0 hsync processing). 00: input hsync 01: input de 10: fixed at 0 11: reserved
[7:3]	RO	reserved	Reserved
[2]	RW	de_inv	de inversion (level-1 de processing). 0: not inverted 1: inverted

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[1:0]	RW	de_sel	de source select (level-0 de processing). 00: input de 01: result of level-2 hsync processing 10: fixed at 1 11: fixed at 0

PT_GEN_TIMING_CFG

PT_GEN_TIMING_CFG is a timing recovery module configuration register.

Offset Address	Register Name	Total Reset Value
0x0134	PT_GEN_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reserved																											vsync_mode	hsync_mode	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timing recovery enable (timings are recovered based on timing parameters). 0: disabled 1: enabled
[30]	RW	mode	Timing recovery mode (timings are recovered based on timing parameters). 0: Timings are generated based on the input valid signal of PT. 1: Timings are internally calculated and generated.
[29:3]	RO	reserved	Reserved
[2]	RW	vsync_mode	vsync recovery. 0: not recovered 1: recovered
[1]	RW	hsync_mode	hsync recovery. 0: not recovered 1: recovered
[0]	RO	reserved	Reserved.

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PT_UNIFY_DATA_CFG

PT_UNIFY_DATA_CFG is a data configuration register.

Offset Address	Register Name	Total Reset Value
0x0140	PT_UNIFY_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											uv_seq	yc_seq	comp_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Data separation enable. 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3]	RW	uv_seq	CbCr sequence. 0: CbCr 1: CrCb
[2]	RW	yc_seq	YC sequence. 0: CY 1: YC
[1:0]	RW	comp_num	Data component select. 00: component 1 01: component 2 10: component 3 11: reserved

PT_YUV444_CFG

PT_YUV444_CFG is a YUV444 configuration register.

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Offset Address	Register Name	Total Reset Value
0x0150	PT_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable for converting YUV422 signals into YUV444 signals. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

PT_INTF_HFB

PT_INTF_HFB is a horizontal front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0180	PT_INTF_HFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hfb	Horizontal front blanking width.

PT_INTF_HACT

PT_INTF_HACT is a horizontal active width register.

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Offset Address	Register Name	Total Reset Value
0x0184	PT_INTF_HACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hact	Horizontal active width (in clock cycle).

PT_INTF_HBB

PT_INTF_HBB is a horizontal back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0188	PT_INTF_HBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	hbb	Horizontal back blanking width.

PT_INTF_VFB

PT_INTF_VFB is a vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x018C	PT_INTF_VFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vfb	Vertical front blanking width.

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PT_INTF_VACT

PT_INTF_VACT is a vertical active width register.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vact	Vertical active width.

PT_INTF_VBB

PT_INTF_VBB is a vertical back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0194	PT_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbb	Vertical back blanking width.

PT_INTF_VBFB

PT_INTF_VBFB is a vertical bottom front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0198	PT_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

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[15:0]	RW	vbfb	Vertical bottom front blanking width.

PT_INTF_VBACT

PT_INTF_VBACT is a vertical bottom active width register.

Offset Address	Register Name	Total Reset Value
0x019C	PT_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbact	Vertical bottom active width.

PT_INTF_VBBB

PT_INTF_VBBB is a vertical bottom back blanking width register.

Offset Address	Register Name	Total Reset Value
0x01A0	PT_INTF_VBBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbbb	Vertical bottom back blanking width.

PT_ID_CFG

PT_ID_CFG is an ID configuration register.

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Offset Address	Register Name	Total Reset Value
0x01A4	PT_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reset	reserved																							id_det		id_max		id	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	ID generation enable. 0: disabled 1: enabled
[30]	RW	mode	ID generation mode. 0: automatic mode (the ID automatically increases for each frame) 1: non-automatic mode (the ID depends on the configured value)
[29]	WO	reset	In automatic mode, setting this field to 1 restores the ID of the next frame to the initial value. This field is automatically cleared after restoration.
[28:6]	RO	reserved	Reserved
[5:4]	RW	id_det	ID of the frame whose width and height are detected.
[3:2]	RW	id_max	Maximum ID in automatic mode.
[1:0]	RW	id	Initial ID in automatic mode or generated ID in non-automatic mode.

PT_FLASH_CFG

PT_FLASH_CFG is a flash configuration register.

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Offset Address	Register Name	Total Reset Value
0x01B0	PT_FLASH_CFG	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_sel				reserved									shutter_times	shutter_phase	shutter_en	reserved														flash_phase	flash_en
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	id_sel	Trigger frame ID. 0001: triggered by using the start interrupt of the frame whose ID is 0 0010: triggered by using the start interrupt of the frame whose ID is 1 0100: triggered by using the start interrupt of the frame whose ID is 2 1000: triggered by using the start interrupt of the frame whose ID is 3
[27:19]	RO	reserved	Reserved
[18]	RW	shutter_times	Shutter pulse times. 0: twice 1: once
[17]	RW	shutter_phase	Shutter signal reverse. 0: not reversed 1: reversed
[16]	WO	shutter_en	Shutter trigger enable. This field is automatically cleared.
[15:2]	RO	reserved	Reserved
[1]	RW	flash_phase	Flash signal reverse. 0: not reversed 1: reversed
[0]	WO	flash_en	Flash trigger enable. This field is automatically cleared.

PT_FLASH_CYC0

PT_FLASH_CYC0 is a flash timing 0 width register.

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Offset Address	Register Name	Total Reset Value
0x01C0	PT_FLASH_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 0 (in PT clock). The configured value is the actual value minus 1.

PT_FLASH_CYC1

PT_FLASH_CYC1 is a flash timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01C4	PT_FLASH_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 1 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC0

PT_SHUTTER_CYC0 is a shutter timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01D0	PT_SHUTTER_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 0 (in PT clock). The configured value is the actual value minus 1.

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PT_SHUTTER_CYC1

PT_SHUTTER_CYC1 is a shutter timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01D4	PT_SHUTTER_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 1 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC2

PT_SHUTTER_CYC2 is a shutter timing 2 width register.

Offset Address	Register Name	Total Reset Value
0x01D8	PT_SHUTTER_CYC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 2 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC3

PT_SHUTTER_CYC3 is a shutter timing 3 width register.

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Offset Address	Register Name	Total Reset Value
0x01DC	PT_SHUTTER_CYC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 3 (in PT clock). The configured value is the actual value minus 1.

PT_STATUS

PT_STATUS is a port status register.

Offset Address	Register Name	Total Reset Value
0x01E0	PT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										id		field	vysync	hsync	de
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RO	id	Port output ID.
[3]	RO	field	Field output over the port.
[2]	RO	vysync	vysync signal output over the port.
[1]	RO	hsync	hsync signal over the port.
[0]	RO	de	de signal output over the port.

PT_BT656_STATUS

PT_BT656_STATUS is a BT.656 status register.

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Offset Address	Register Name	Total Reset Value
0x01E4	PT_BT656_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																seav								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	seav	Sync code.
[7:0]	RO	reserved	Reserved.

PT_SIZE

PT_SIZE is an input picture size register.

Offset Address	Register Name	Total Reset Value
0x01EC	PT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Picture height.
[15:0]	RO	width	Picture width.

PT_INT

PT_INT is a channel interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x01F0	PT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	WC	height_err	Status of the picture height change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	width_err	Status of the picture width change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

PT_INT_MASK

PT_INT_MASK is a port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	PT_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved

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[2]	RW	height_err	Picture height change interrupt enable. 0: masked 1: enabled
[1]	RW	width_err	Picture width change interrupt enable. 0: masked 1: enabled
[0]	RW	fstart	Frame/Field start interrupt enable. 0: masked 1: enabled

DES_CTRL

DES_CTRL is a DES control register.

Offset Address	Register Name	Total Reset Value
0x0200	DES_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																									bit_width					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	DES enable. 0: disabled 1: enabled
[30:6]	RO	reserved	Reserved
[5:0]	RW	bit_width	Data width. 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

DES_REG_NEWER

DES_REG_NEWER is a capture control register.

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Offset Address	Register Name	Total Reset Value
0x0204	DES_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_newer	DES update. This bit is automatically cleared for each frame.

DES_ID_CFG

DES_ID_CFG is a DES RX ID selection register (instant register).

Offset Address	Register Name	Total Reset Value
0x0210	DES_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	id_sel	ID of the data received by the DES. XXX1: 0 XX1X: 1 X1XX: 2 1XXX: 3

DES_CROP_CFG

DES_CROP_CFG is a crop enable register.

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Offset Address	Register Name	Total Reset Value
0x0220	DES_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable. 0: disabled 1: enabled

DES_CROP0_START

DES_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x0230	DES_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which pictures start to be captured.
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which pictures start to be captured.

DES_CROP0_SIZE

DES_CROP0_SIZE is a crop size configuration register for region 0.

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Offset Address	Register Name	Total Reset Value
0x0234	DES_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	height			reserved	width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

DES_CFG

DES_CFG is a DES configuration register.

Offset Address	Register Name	Total Reset Value
0x0270	DES_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	cmp_en	k_coef_range	reserved					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RW	cmp_en	DES channel frame compress enable. 0: disabled 1: enabled
[30:27]	RO	k_coef_range	Frame compression rate of the DES channel. The value range is [7:12]. The typical value is the data bit width minus 1. The configured value is 12 when the data bit width is 14 bits.
[26:0]	RO	reserved	Reserved

DES_CMP_FRM_LEN

DES_CMP_FRM_LEN is a DES compressed data length register.

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Offset Address	Register Name	Total Reset Value
0x0274	DES_CMP_FRM_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmp_frm_len																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	cmp_frm_len	Length of the compressed DES frame data (a multiple of 128 bits).

DES_SIZE

DES_SIZE is a DES storage size register.

Offset Address	Register Name	Total Reset Value
0x0284	DES_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

DES_FADDR

DES_FADDR is a DES storage base address register.

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Offset Address	Register Name	Total Reset Value
0x0290	DES_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	DES storage base address.

DES_BUF_CFG

DES_BUF_CFG is a DES bus buffer control register.

Offset Address	Register Name	Total Reset Value
0x029C	DES_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	buf_thd	Depth of the bus buffer.

DES_INT

DES_INT is a DES raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x02F0	DES_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

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[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

DES_MASK

DES_MASK is a DES interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x02F8	DES_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.

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[3]	RW	field_throw	Field/Frame loss interrupt enable. 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable. 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable. 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable. 0: masked 1: enabled

LINE_BUF_CFG

LINE_BUF_CFG is a LINE_BUF control register.

Offset Address	Register Name	Total Reset Value
0x0500	LINE_BUF_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	LINE_BUF enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

LINE_BUF_REG_NEWER

LINE_BUF_REG_NEWER is a LINE_BUF update register.

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Offset Address	Register Name	Total Reset Value
0x0504	LINE_BUF_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	reg_newer	LINE_BUF update. This bit is automatically cleared for each frame.

LINE_BUF_ID_CFG

LINE_BUF_ID_CFG is a LINE_BUF RX ID selection register (instant register).

Offset Address	Register Name	Total Reset Value
0x0510	LINE_BUF_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	id_sel	ID of the data received by the LINE_BUF. XXX1: 0 XX1X: 1 X1XX: 2 1XXX: 3

LINE_BUF_CROP_CFG

LINE_BUF_CROP_CFG is a crop register.

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Offset Address	Register Name	Total Reset Value
0x0520	LINE_BUF_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	n0_en	Region 0 enable. 0: disabled 1: enabled

LINE_BUF_CROP0_START

LINE_BUF_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x0530	LINE_BUF_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	y_start	ID of the line from which pictures start to be captured.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	x_start	ID of the pixel from which pictures start to be captured.

LINE_BUF_CROP0_SIZE

LINE_BUF_CROP0_SIZE is a crop size configuration register for region 0.

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Offset Address	Register Name	Total Reset Value
0x0534	LINE_BUF_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	height			reserved	width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

LINE_BUF_WIDTH

LINE_BUF_WIDTH is a LINE_BUF picture width register.

Offset Address	Register Name	Total Reset Value
0x0550	LINE_BUF_WIDTH	0x077F_077F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	line_buf_thd			reserved	line_buf_width		
Reset	0 0 0 0	0 1 1 1	0 1 1 1	1 1 1 1	0 0 0 0	0 1 1 1	0 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	line_buf_thd	Threshold for starting the LINE_BUF RAM read operation.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	line_buf_width	LINE_BUF picture width.

LINE_BUF_HEIGHT

LINE_BUF_HEIGHT is a LINE_BUF picture height register.

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Offset Address	Register Name	Total Reset Value
0x0554	LINE_BUF_HEIGHT	0x0000_0437

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_buf_height											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	line_buf_height	LINE_BUF picture height.

LINE_BUF_INT

LINE_BUF_INT is a LINE_BUF raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x05F0	LINE_BUF_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	reserved	reserved	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.

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[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

LINE_BUF_MASK

LINE_BUF_MASK is a LINE_BUF interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x05F8	LINE_BUF_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	reserved	reserved	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	update_cfg	Register update interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable. 0: masked 1: enabled
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RW	fstart	Field/Frame start interrupt enable. 0: masked 1: enabled

SRC_CTRL

SRC_CTRL is an SRC control register.

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Offset Address	Register Name	Total Reset Value
0x0600	SRC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											bit_width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	SRC enable. 0: disabled 1: enabled 0x600−0x6FF: address space of the SRC0 register 0x700−0x7FF: address space of the SRC1 register
[30:6]	RO	reserved	Reserved.
[5:0]	RW	bit_width	Data bit width. 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

SRC_REG_NEWER

SRC_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x0604	SRC_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	reg_newer	SRC update. This bit is automatically cleared for each frame.

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SRC_CFG

SRC_CFG is an SRC configuration register.

Offset Address	Register Name	Total Reset Value
0x0670	SRC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_en	k_coef_range				dcmp_mode	reserved																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dcmp_en	SRC read channel frame compress enable. 0: disabled 1: enabled
[30:27]	RW	k_coef_range	Frame compression rate of the SRC channel. The value range is [7:12]. The configuration during decompression must be the same as the that during data compression. The typical value is the bit width minus 1. The configured value is 12 when the bit width is 14 bits.
[26]	RW	dcmp_mode	Frame compression mode of the SRC read channel. 0: The length of the read compressed data is determined by the internal DES channel of the logic. 1: The length of the read compressed data is specified by configuring the related register.
[25:0]	RO	reserved	Reserved.

SRC_DCMP_FRM_LEN

SRC_DCMP_FRM_LEN is a read compressed data length configuration register for the SRC channel.

Offset Address	Register Name	Total Reset Value
0x0674	SRC_DCMP_FRM_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_frm_len																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dcmp_frm_len	Length of the compressed frame data read by the SRC read channel (a multiple of 128 bits).

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SRC_SIZE

SRC_SIZE is an SRC storage size register.

Offset Address	Register Name	Total Reset Value
0x0684	SRC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

SRC_FADDR

SRC_FADDR is an SRC storage base address register.

Offset Address	Register Name	Total Reset Value
0x0690	SRC_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	SRC storage base address.

SRC_BUF_CFG

SRC_BUF_CFG is an SRC bus buffer control register.

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Offset Address	Register Name	Total Reset Value
0x069C	SRC_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	buf_thd	Depth of the bus buffer.

SRC_INT

SRC_INT is an SRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x06F0	SRC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	WC	dcmp_wrong	Status of the decompress error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

SRC_MASK

SRC_MASK is an SRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x06F8	SRC_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5]	RW	dcmp_wrong	Decompress error interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	update_cfg	Register update interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable. 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable. 0: masked 1: enabled

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[1]	RW	cc_int	Capture completion interrupt enable. 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable. 0: masked 1: enabled

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x1000	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x1004	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	RW	reg_newer	Channel update. This bit is automatically cleared for each frame.

CH_SUM_Y

CH_SUM_Y is an input picture luminance statistics register.

Offset Address	Register Name	Total Reset Value
0x1020	CH_SUM_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum_y																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum_y	Luminance statistics.

CH_DLY_CFG

CH_DLY_CFG is a channel input picture start interrupt delay configuration register.

Offset Address	Register Name	Total Reset Value
0x1034	CH_DLY_CFG	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_dly_cfg																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	v_dly_cfg	Vertical line number delay.
[15:0]	RO	reserved	Reserved.

CH_WCH_Y_CFG

CH_WCH_Y_CFG is a Y component configuration register for the WCH module.

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Offset Address	Register Name	Total Reset Value
0x1080	CH_WCH_Y_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	reserved		reserved													head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable. 0: disabled 1: enabled
[30:20]	RO	reserved	Reserved.
[19]	RW	interleave	Progressive/Interlaced flag. 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storing. 1: The output data interlaced and needs to be interleaved as frames for storing.
[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data interlaced and needs to be interleaved as frames for storing. 0: top field 1: bottom field
[17:16]	RO	reserved	Reserved.
[15:3]	RO	reserved	Reserved.
[2]	RW	head_tword	Header information stride. 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)
[1]	RW	cmp_mode	Compressed segment length. 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable. 0: disabled 1: enabled

CH_WCH_Y_SIZE

CH_WCH_Y_SIZE is a Y component storage size register for the WCH module.

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Offset Address	Register Name	Total Reset Value
0x1084	CH_WCH_Y_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

CH_WCH_Y_FADDR

CH_WCH_Y_FADDR is a Y component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1090	CH_WCH_Y_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the Y component.

CH_WCH_Y_HADDR

CH_WCH_Y_HADDR is a Y component header information storage base address register for the WCH module.

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Offset Address	Register Name	Total Reset Value
0x1094	CH_WCH_Y_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the Y component header information.

CH_WCH_Y_STRIDE

CH_WCH_Y_STRIDE is a Y component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1098	CH_WCH_Y_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the Y component.

CH_WCH_C_CFG

CH_WCH_C_CFG is a C component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A0	CH_WCH_C_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	reserved		reserved													head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable. 0: disabled 1: enabled

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[30:20]	RO	reserved	Reserved.
[19]	RW	interleave	Progressive/Interlaced flag. 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storing. 1: The output data interlaced and needs to be interleaved as frames for storing.
[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data interlaced and needs to be interleaved as frames for storing. 0: top field 1: bottom field
[17:16]	RO	reserved	Reserved.
[15:3]	RO	reserved	Reserved.
[2]	RW	head_tword	Header information stride. 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)
[1]	RW	cmp_mode	Compressed segment length. 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable. 0: disabled 1: enabled

CH_WCH_C_SIZE

CH_WCH_C_SIZE is a C component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A4	CH_WCH_C_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.

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[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

CH_WCH_C_FADDR

CH_WCH_C_FADDR is a C component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B0	CH_WCH_C_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the C component.

CH_WCH_C_HADDR

CH_WCH_C_HADDR is a C component header information storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B4	CH_WCH_C_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the C component header information.

CH_WCH_C_STRIDE

CH_WCH_C_STRIDE is a C component line offset register for the WCH module.

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Offset Address	Register Name	Total Reset Value
0x10B8	CH_WCH_C_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the C component.

CH_INT

CH_INT is a channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10F0	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																acm_para_finish	fstart_dly	reserved									update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	WC	acm_para_finish	Status of the ACM LUT loading completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	WC	fstart_dly	Status of the delayed field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14:5]	RO	reserved	Reserved.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

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[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10F8	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															acm_para_finish	fstart_dly	reserved										update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RW	acm_para_finish	ACM LUT loading completion interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RW	fstart_dly	Delayed field/frame start interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[14:5]	RO	reserved	Reserved.

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[4]	RW	update_cfg	Register update interrupt enable. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable. 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable. 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable. 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable. 0: masked 1: enabled

CH_CROP_CFG

CH_CROP_CFG is a crop register.

Offset Address	Register Name	Total Reset Value
0x1100	CH_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	n0_en	Region 0 enable. 0: disabled 1: enabled

CH_CROP0_START

CH_CROP0_START is a crop start position register for region 0.

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Offset Address	Register Name	Total Reset Value
0x1110	CH_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	y_start	ID of the line from which pictures start to be captured.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	x_start	ID of the pixel from which pictures start to be captured.

CH_CROP0_SIZE

CH_CROP0_SIZE is a crop size configuration register for region 0.

Offset Address	Register Name	Total Reset Value
0x1114	CH_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

CH_CSC_CFG

CH_CSC_CFG is a CSC configuration register.

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Offset Address	Register Name	Total Reset Value
0x1200	CH_CSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	CSC enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

CH_CSC_COEF0

CH_CSC_COEF0 is CSC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1210	CH_CSC_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01															reserved	coef00															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef01	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved.
[15:1]	RW	coef00	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved.

CH_CSC_COEF1

CH_CSC_COEF1 is CSC coefficient register 1.

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Offset Address	Register Name	Total Reset Value
0x1214	CH_CSC_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10															reserved	coef02															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef10	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved.
[15:1]	RW	coef02	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved.

CH_CSC_COEF2

CH_CSC_COEF2 is CSC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x1218	CH_CSC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12															reserved	coef11															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef12	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved.
[15:1]	RW	coef11	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved.

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CH_CSC_COEF3

CH_CSC_COEF3 is CSC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x121C	CH_CSC_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21															reserved	coef20															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef21	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved.
[15:1]	RW	coef20	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved.

CH_CSC_COEF4

CH_CSC_COEF4 is CSC coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x1220	CH_CSC_COEF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															reserved	coef22															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RO	reserved	Reserved.
[15:1]	RW	coef22	CSC coefficient. Its format is (s, 4, 10). The value consists of a 1-bit signed part, a 4-bit integer part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved.

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CH_CSC_IN_DC0

CH_CSC_IN_DC0 is CSC input DC component register 0.

Offset Address	Register Name	Total Reset Value
0x1230	CH_CSC_IN_DC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	in_dc1												reserved				in_dc0												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RW	in_dc1	DC offset of the input G component, signed integer.
[20:16]	RO	reserved	Reserved.
[15:5]	RW	in_dc0	DC offset of the input R component, signed integer.
[4:0]	RO	reserved	Reserved.

CH_CSC_IN_DC1

CH_CSC_IN_DC1 is CSC input DC component register 1.

Offset Address	Register Name	Total Reset Value
0x1234	CH_CSC_IN_DC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved				in_dc2												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RO	reserved	Reserved.
[15:5]	RW	in_dc2	DC offset of the input B component, signed integer.
[4:0]	RO	reserved	Reserved.

CH_CSC_OUT_DC0

CH_CSC_OUT_DC0 is CSC output DC component register 0.

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Offset Address	Register Name	Total Reset Value
0x1238	CH_CSC_OUT_DC0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	out_dc1			reserved	out_dc0			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	out_dc1	DC offset of the output U component, signed integer.
[20:16]	RO	reserved	Reserved.
[15:5]	RW	out_dc0	DC offset of the output Y component, signed integer.
[4:0]	RO	reserved	Reserved.

CH_CSC_OUT_DC1

CH_CSC_OUT_DC1 is CSC output DC component register 1.

Offset Address	Register Name	Total Reset Value
0x123C	CH_CSC_OUT_DC1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			reserved	out_dc2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RO	reserved	Reserved.
[15:5]	RW	out_dc2	DC offset of the output V component, signed integer.
[4:0]	RO	reserved	Reserved.

CH_DITHER_CFG

CH_DITHER_CFG is a dither configuration register.

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Offset Address	Register Name	Total Reset Value
0x1300	CH_DITHER_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Dither enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

CH_ACM_CTRL

CH_ACM_CTRL is an ACM control register.

Offset Address	Register Name	Total Reset Value
0x1400	CH_ACM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm_en	acm_dbg_en	acm_stretch	acm_cliprange	acm_cliporwrap	reserved																			acm_cbcrthr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	acm_en	ACM enable. 0: disabled (data output bypassed) 1: enabled (implementing luminance and contrast adjustment)
[30]	RW	acm_dbg_en	ACM debug enable. When acm_dbg_en is valid, the original picture is displayed on the left part of the screen, and the picture processed by the ACM is displayed on the right part of the screen.
[29]	RW	acm_stretch	Input pixel range. 0: Y 64−940, C 64−960 1: Y 0−1023, C 0−1023
[28]	RW	acm_cliprange	Output pixel range. 0: Y 64−940, C 64−960 1: Y 0−1023, C 0−1023

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[27]	RW	acm_cliporwrap	Hue component limit after ACM. 0: The hue component is wrapped around to fall within [0, 1023]. 1: The hue component is clipped to fall within [0, 1023].
[26:8]	RO	reserved	Reserved.
[7:0]	RW	acm_cbcrthr	ACM algorithm enable threshold. It is a 9-bit unsigned number and ranges from 0 to 255.

CH_ACM_ADJ

CH_ACM_ADJ is an ACM processed pixel change register.

Offset Address	Register Name	Total Reset Value
0x1404	CH_ACM_ADJ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_gain0								acm_gain1										acm_gain2									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	acm_gain0	Control coefficient of the luminance adjustment range. The range is 0−512.
[19:10]	RW	acm_gain1	Control coefficient of the hue adjustment range. The range is 0−512.
[9:0]	RW	acm_gain2	Control coefficient of the saturation adjustment range. The range is 0−512.

CH_ACM_SIZE

CH_ACM_SIZE is an ACM processed picture size register.

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Offset Address	Register Name	Total Reset Value
0x1410	CH_ACM_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	height			reserved	width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Picture height (in pixel). The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1.

CH_ACM_PARA_ADDR

CH_ACM_PARA_ADDR is an ACM coefficient loading address configuration register.

Offset Address	Register Name	Total Reset Value
0x1414	CH_ACM_PARA_ADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	acm_para_addr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	acm_para_addr	Address for loading ACM coefficients.

CH_ACM_PARA_UP

CH_ACM_PARA_UP is an ACM parameter update register.

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Offset Address	Register Name	Total Reset Value
0x1420	CH_ACM_PARA_UP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															para_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	para_up	Parameter update. This bit is automatically cleared for each frame.

CH_SKIP_Y_CFG

CH_SKIP_Y_CFG is a Y skip configuration register.

Offset Address	Register Name	Total Reset Value
0x1500	CH_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration.

CH_SKIP_C_CFG

CH_SKIP_C_CFG is a C component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x1510	CH_SKIP_C_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration.

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CH_HCDS_CFG

CH_HCDS_CFG is a horizontal chrominance down sampling configuration register.

Offset Address	Register Name	Total Reset Value
0x1600	CH_HCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cds_en	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cds_en	Down sampling enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

CH_HCDS_OFFSET

CH_HCDS_OFFSET is a horizontal chrominance down sampling offset register.

Offset Address	Register Name	Total Reset Value
0x1604	CH_HCDS_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hcds_offset																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	hcds_offset	Horizontal chrominance start position offset in the format of (s, 7, 20). That is, the offset value consists of a 1-bit signed part, 7-bit integer part, and 20-bit decimal part. The value is expressed as a two's complement and ranges from –6 to +15.

CH_HCDS_IN_SIZE

CH_HCDS_IN_SIZE is a horizontal chrominance down sampling input size configuration register.

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Offset Address	Register Name	Total Reset Value
0x1610	CH_HCDS_IN_SIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of a picture chrominance line. The configured value is the actual value minus 1.

CH_HCDS_OUT_SIZE

CH_HCDS_OUT_SIZE is a horizontal chrominance down sampling output size configuration register.

Offset Address	Register Name	Total Reset Value
0x1614	CH_HCDS_OUT_SIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12:0]	RW	width	Width (in pixel) of a picture chrominance line. The configured value is the actual value minus 1.

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CH_HCDS_COEF0

CH_HCDS_COEF0 is horizontal chrominance down sampling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1620	CH_HCDS_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef2								coef1										coef0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	coef2	Horizontal chrominance scaling and filtering coefficient 2
[19:10]	RW	coef1	Horizontal chrominance scaling and filtering coefficient 1.
[9:0]	RW	coef0	Horizontal chrominance scaling and filtering coefficient 0. Horizontal scaling contains eight taps, and the sum of the eight coefficients is 512.

CH_HCDS_COEF1

CH_HCDS_COEF1 horizontal chrominance down sampling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x1624	CH_HCDS_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4										coef3									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	coef5	Horizontal chrominance scaling and filtering coefficient 5.
[19:10]	RW	coef4	Horizontal chrominance scaling and filtering coefficient 4.
[9:0]	RW	coef3	Horizontal chrominance scaling and filtering coefficient 3.

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CH_HCDS_COEF2

CH_HCDS_COEF2 horizontal chrominance down sampling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x1628	CH_HCDS_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7										coef6									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:10]	RW	coef7	Horizontal chrominance scaling and filtering coefficient 7.
[9:0]	RW	coef6	Horizontal chrominance scaling and filtering coefficient 6.

CH_VCDS_CFG

CH_VCDS_CFG is a vertical chrominance down sampling configuration register for large streams.

Offset Address	Register Name	Total Reset Value
0x1700	CH_VCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	enable	Down scaling enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

CH_VCDS_COEF

CH_VCDS_COEF is a vertical chrominance down sampling coefficient register for large streams.

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Offset Address	Register Name	Total Reset Value
0x1704	CH_VCDS_COEF	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef1				reserved												coef0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	coef1	Down sampling coefficient 1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	coef0	Down sampling coefficient 0.

CH_CLIP_Y_CFG

CH_CLIP_Y_CFG is a luminance clamp configuration register.

Offset Address	Register Name	Total Reset Value
0x1800	CH_CLIP_Y_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum luminance value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum luminance value. When the data bit width is less than 16 bits, the upper bits are valid.

CH_CLIP_C_CFG

CH_CLIP_C_CFG is a chrominance clamp configuration register.

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Offset Address	Register Name	Total Reset Value
0x1804	CH_CLIP_C_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum chrominance value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum chrominance value. When the data bit width is less than 16 bits, the upper bits are valid.

CH_UV2C_CFG

CH_UV2C_CFG is a UV2C_CFG configuration register.

Offset Address	Register Name	Total Reset Value
0x01900	CH_UV2C_CFG	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved	reserved																													
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	UV2C enable for converting the internal UV components into the single C component. 0: disabled 1: enabled
[30]	RO	reserved	Reserved.
[29:0]	RO	reserved	Reserved.

CH_DIS_CFG

CH_DIS_CFG is a CH_DIS enable register.

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Offset Address	Register Name	Total Reset Value
0x1A00	CH_DIS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	close_clk	reserved																														work_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	close_clk	Clock disable. 0: normal 1: DIS core clock disabled (excluding the CPI)
[30:1]	RO	reserved	Reserved.
[0]	RW	work_en	DIS enable. 0: disabled 1: enabled

CH_DIS_BLK

CH_DIS_BLK is a CH_DIS block configuration register.

Offset Address	Register Name	Total Reset Value
0x1A04	CH_DIS_BLK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								srch_range								reserved								blk_size							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	srch_range	Search range. The value is an even number ranging from 8 to 128.
[15:9]	RO	reserved	Reserved.
[8:0]	RW	blk_size	Side length of the square block. The value is an even number ranging from 16 to 256.

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CH_DIS_V0POS

CH_DIS_V0POS is a CH_DIS vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x1A10	CH_DIS_V0POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ0 block. The least significant bit (LSB) of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_V4POS

CH_DIS_V4POS is a CH_DIS vertical PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x1A14	CH_DIS_V4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_V8POS

CH_DIS_V8POS is a CH_DIS vertical PRJ8 block address register.

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Offset Address	Register Name	Total Reset Value
0x1A18	CH_DIS_V8POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_V0POSE

CH_DIS_V0POSE is a CH_DIS vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x1A20	CH_DIS_V0POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_V4POSE

CH_DIS_V4POSE is a CH_DIS vertical PRJ4 block address register.

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Offset Address	Register Name	Total Reset Value
0x1A24	CH_DIS_V4POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_V8POSE

CH_DIS_V8POSE is a CH_DIS vertical PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x1A28	CH_DIS_V8POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H0POS

CH_DIS_H0POS is a CH_DIS horizontal PRJ0 block address register.

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Offset Address	Register Name	Total Reset Value
0x1A30	CH_DIS_H0POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H4POS

CH_DIS_H4POS is a CH_DIS horizontal PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x1A34	CH_DIS_H4POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H8POS

CH_DIS_H8POS is a CH_DIS horizontal PRJ8 block address register.

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Offset Address	Register Name	Total Reset Value
0x1A38	CH_DIS_H8POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H0POSE

CH_DIS_H0POSE is a CH_DIS horizontal PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x1A40	CH_DIS_H0POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H4POSE

CH_DIS_H4POSE is a CH_DIS horizontal PRJ4 block address register.

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Offset Address	Register Name	Total Reset Value
0x1A44	CH_DIS_H4POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_H8POSE

CH_DIS_H8POSE is a CH_DIS horizontal PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x1A48	CH_DIS_H8POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

CH_DIS_VSTAT

CH_DIS_VSTAT is a vertical DIS statistics register for all CH_DIS blocks.

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Offset Address	Register Name	Total Reset Value
0x1B00~0x1B68	CH_DIS_VSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dis_vstat																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dis_vstat	v_delta, v_sad, and v_mv information about each block. Each address contains only one piece of information. For example: 0x1900: v_delta[15:0] of block 1 0x1904: v_sad[23:0] of block 1 0x1908: v_mv[8:0] of block 1 The same rule applies to other addresses.

CH_DIS_HSTAT

CH_DIS_HSTAT is a horizontal DIS statistics register for all CH_DIS blocks.

Offset Address	Register Name	Total Reset Value
0x1B80~0x1Be8	CH_DIS_HSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dis_hstat																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dis_hstat	h_delta, h_sad, and h_mv information about each block. Each address contains only one piece of information. For example: 0x1980: h_delta[15:0] of block 1 0x1984: h_sad[23:0] of block 1 0x1988: h_mv[8:0] of block 1 The same rule applies to other addresses.

CH_VPDCICTRL

CH_VPDCICTRL is a DCI control register.

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Offset Address	Register Name	Total Reset Value
0x1C00	CH_VPDCICTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_en	dci_dbg_en	dci_scene_flg	dci_man_adj0	dci_man_adj1	dci_man_adj2	dci_cbcrcmp_en	dci_cbcrsta_en	dci_in_range	dci_out_range	dci_shift_ctrl		dci_histlpf_en	reserved																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dci_en	DCI enable. 0: disabled (data output bypassed) 1: enabled (implementing luminance and contrast adjustment)
[30]	RW	dci_dbg_en	DCI demo mode enable. 0: disabled 1: The original picture is displayed on the left part of the screen, and the picture processed by the DCI is displayed on the right part of the screen.
[29]	RW	dci_scene_flg	DCI scenario switch enable. 0: disabled 1: enabled
[28]	RW	dci_man_adj0	Adjustment mode of curve 0. 0: automatic mode (the results calculated by hardware are used) 1: manual mode (the results calculated by software are used)
[27]	RW	dci_man_adj1	Adjustment mode of curve 1. 0: automatic mode (the results calculated by hardware are used) 1: manual mode (the results calculated by software are used)
[26]	RW	dci_man_adj2	Adjustment mode of curve 2. 0: automatic mode (the results calculated by hardware are used) 1: manual mode (the results calculated by software are used)
[25]	RW	dci_cbcrcmp_en	DCI chrominance compensation enable. 0: The DCI algorithm does not adjust the chrominance component. 1: The DCI algorithm adjusts the chrominance component.
[24]	RW	dci_cbcrsta_en	Histogram statistics select. 0: Histogram statistics are collected only on the luminance component. 1: Histogram statistics are collected on weighted YCbCr components.

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[23]	RW	dci_in_range	Input range. 0: limit range (Y 64−940 and C 64−960 for the input 10-bit pixel data) 1: full range (Y 0−1023 and C 0−1023 for the input 10-bit pixel data)
[22]	RW	dci_out_range	Output range. 0: limit range (Y 64−940 and C 64−960 for the output 10-bit pixel data) 1: full range (Y 0−1023 and C 0−1023 for the output 10-bit pixel data)
[21:20]	RW	dci_shift_ctrl	DCI histogram statistics shift control. 00: shifted rightwards by 6 bits 01: shifted rightwards by 7 bits 10: shifted rightwards by 8 bits 11: shifted rightwards by 9 bits
[19]	RW	dci_histlpf_en	Histogram low-pass filter enable. 0: disabled 1: enabled
[18:0]	RO	reserved	Reserved.

CH_VPDCIHPOS

CH_VPDCIHPOS is a DCI algorithm horizontal adjustment region register.

Offset Address	Register Name	Total Reset Value
0x1C04	CH_VPDCIHPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_hstart												dci_hend												reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	dci_hstart	Start value of the DCI algorithm horizontal active region.
[19:8]	RW	dci_hend	End value of the DCI algorithm horizontal active region.
[7:0]	RO	reserved	Reserved.

CH_VPDCIVPOS

CH_VPDCIVPOS is a DCI algorithm vertical adjustment region register.

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Offset Address	Register Name	Total Reset Value
0x1C08	CH_VPDCIVPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_vstart			dci_vend			reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RW	dci_vstart	Start value of the DCI algorithm vertical active region.
[19:8]	RW	dci_vend	End value of the DCI algorithm vertical active region.
[7:0]	RO	reserved	Reserved.

CH_VPDCIHISBLD

CH_VPDCIHISBLD is a DCI histogram statistics weighted coefficient register.

Offset Address	Register Name	Total Reset Value
0x1C0C	CH_VPDCIHISBLD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_cbcrsta_y			dci_cbcrsta_cb			dci_cbcrsta_cr	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_cbcrsta_y	Weighted coefficient of the Y component when histogram statistics are added. It is an 8-bit signed number and the MSB is the signed bit.
[23:16]	RW	dci_cbcrsta_cb	Weighted coefficient of the Cb component when histogram statistics are added. It is an 8-bit signed number and the MSB is the signed bit.
[15:8]	RW	dci_cbcrsta_cr	Weighted coefficient of the Cr component when histogram statistics are added. It is an 8-bit signed number and the MSB is the signed bit.
[7:0]	RO	reserved	Reserved.

CH_VPDCIHISOFT

CH_VPDCIHISOFT is a DCI histogram statistics offset register.

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Offset Address	Register Name	Total Reset Value
0x1C10	CH_VPDCIHISOFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_cbcrsta_oft								reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	dci_cbcrsta_oft	Offset when histogram statistics are added. It is a 9-bit signed number and the MSB is the signed bit.
[22:0]	RO	reserved	Reserved.

CH_VPDCIHISCOR

CH_VPDCIHISCOR is a DCI histogram coring register.

Offset Address	Register Name	Total Reset Value
0x1C14	CH_VPDCIHISCOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_histcor_thr0								dci_histcor_thr1								dci_histcor_thr2								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_histcor_thr0	Coring threshold for histogram 0.
[23:16]	RW	dci_histcor_thr1	Coring threshold for histogram 1.
[15:8]	RW	dci_histcor_thr2	Coring threshold for histogram 2.
[7:0]	RO	reserved	Reserved.

CH_VPDCIMERBLD

CH_VPDCIMERBLD is a blend value register for the DCI adjustment unit.

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Offset Address	Register Name	Total Reset Value
0x1C18	CH_VPDCIMERBLD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_metrc_abld0	dci_metrc_abld1		dci_metrc_abld2		dci_hist_abld	dci_org_abld	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RW	dci_metrc_abld0	Weighted alpha blend value of the current frame for metric 0.
[25:20]	RW	dci_metrc_abld1	Weighted alpha blend value of the current frame for metric 1.
[19:14]	RW	dci_metrc_abld2	Weighted alpha blend value of the current frame for metric 2.
[13:8]	RW	dci_hist_abld	Weighted alpha blend value of the current histogram and the previous histogram.
[7:2]	RW	dci_org_abld	Alpha blend value when the luminance component is adjusted.
[1:0]	RO	reserved	Reserved.

CH_VPDCIADJWGT

CH_VPDCIADJWGT is a DCI manually configured curve weight register.

Offset Address	Register Name	Total Reset Value
0x1C1C	CH_VPDCIADJWGT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_man_adjwgt0		dci_man_adjwgt1		dci_man_adjwgt2		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_man_adjwgt0	Weighted value of curve 0 in manual mode.
[23:16]	RW	dci_man_adjwgt1	Weighted value of curve 1 in manual mode.
[15:8]	RW	dci_man_adjwgt2	Weighted value of curve 2 in manual mode.
[7:0]	RO	reserved	Reserved.

CH_VPDCICLIP0

CH_VPDCICLIP0 is a DCI curve 0 weight range register.

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Offset Address	Register Name	Total Reset Value
0x1C20	CH_VPDCICLIP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_wgt_cliplow0		dci_wgt_cliphigh0		reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow0	Lower limit of the weighted value of curve 0.
[23:16]	RW	dci_wgt_cliphigh0	Upper limit of the weighted value of curve 0.
[15:0]	RO	reserved	Reserved.

CH_VPDCICLIP1

CH_VPDCICLIP1 is a DCI curve 1 weight range register.

Offset Address	Register Name	Total Reset Value
0x1C24	CH_VPDCICLIP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_wgt_cliplow1		dci_wgt_cliphigh1		reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow1	Lower limit of the weighted value of curve 1.
[23:16]	RW	dci_wgt_cliphigh1	Upper limit of the weighted value of curve 1.
[15:0]	RO	reserved	Reserved.

CH_VPDCICLIP2

CH_VPDCICLIP2 is a DCI curve 2 weight range register.

Offset Address	Register Name	Total Reset Value
0x1C28	CH_VPDCICLIP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_wgt_cliplow2		dci_wgt_cliphigh2		reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow2	Lower limit of the weighted value of curve 2.

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[23:16]	RW	dci_wgt_cliphigh2	Upper limit of the weighted value of curve 2.
[15:0]	RO	reserved	Reserved.

CH_VPDCIGLBGAIN

CH_VPDCIGLBGAIN is a global gain register for the DCI luminance adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C2C	CH_VPDCIGLBGAIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_glb_gain0	dci_glb_gain1		dci_glb_gain2		reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RW	dci_glb_gain0	Global gain 0 when the luminance component is adjusted.
[25:20]	RW	dci_glb_gain1	Global gain 1 when the luminance component is adjusted.
[19:14]	RW	dci_glb_gain2	Global gain 2 when the luminance component is adjusted.
[13:0]	RO	reserved	Reserved.

CH_VPDCIPOSTHR0

CH_VPDCIPOSTHR0 is positive adjustment threshold register 0 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C30	CH_VPDCIPOSTHR0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_thr1		dci_gainpos_thr2		dci_gainpos_thr3		dci_gainpos_thr4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr1	Threshold 1 for luminance Y when the picture is adjusted from dark to bright.
[23:16]	RW	dci_gainpos_thr2	Threshold 2 for luminance Y when the picture is adjusted from dark to bright.
[15:8]	RW	dci_gainpos_thr3	Threshold 3 for luminance Y when the picture is adjusted from dark to bright.
[7:0]	RW	dci_gainpos_thr4	Threshold 4 for luminance Y when the picture is adjusted from dark to bright.

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CH_VPDCIPOSTHR1

CH_VPDCIPOSTHR1 is positive adjustment threshold register 1 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C34	CH_VPDCIPOSTHR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_thr5		dci_gainpos_thr6		dci_gainpos_thr7		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr5	Threshold 5 for luminance Y when the picture is adjusted from dark to bright.
[23:16]	RW	dci_gainpos_thr6	Threshold 6 for luminance Y when the picture is adjusted from dark to bright.
[15:8]	RW	dci_gainpos_thr7	Threshold 7 for luminance Y when the picture is adjusted from dark to bright.
[7:0]	RO	reserved	Reserved.

CH_VPDCIPOSGAIN0

CH_VPDCIPOSGAIN0 is positive adjustment gain register 0 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C38	CH_VPDCIPOSGAIN0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_cbcr0	dci_gainpos_cbcr1	dci_gainpos_cbcr2	dci_gainpos_cbcr3	dci_gainpos_cbcr4	dci_gainpos_cbcr5	dci_gainpos_cbcr6	dci_gainpos_cbcr7
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from dark to bright.
[27:24]	RW	dci_gainpos_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from dark to bright.
[23:20]	RW	dci_gainpos_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from dark to bright.
[19:16]	RW	dci_gainpos_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from dark to bright.
[15:12]	RW	dci_gainpos_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from dark to bright.

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[11:8]	RW	dci_gainpos_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from dark to bright.
[7:4]	RW	dci_gainpos_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from dark to bright.
[3:0]	RW	dci_gainpos_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from dark to bright.

CH_VPDCIPOSGAIN1

CH_VPDCIPOSGAIN1 is positive adjustment gain register 1 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C3C	CH_VPDCIPOSGAIN1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_cbcr8	reserved						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from dark to bright.
[27:0]	RO	reserved	Reserved.

CH_VPDCIPOSSLP0

CH_VPDCIPOSSLP0 is positive adjustment slope register 0 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C40	CH_VPDCIPOSSLP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp0			dci_gainpos_slp1			dci_gainpos_slp2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp0	Slope of region 1 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[21:12]	RW	dci_gainpos_slp1	Slope of region 2 when the picture is adjusted from dark to bright. It is a 10-bit signed number.

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[11:2]	RW	dci_gainpos_slp2	Slope of region 3 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[1:0]	RO	reserved	Reserved.

CH_VPDCIPOSSLP1

CH_VPDCIPOSSLP1 is positive adjustment slope register 1 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C44	CH_VPDCIPOSSLP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp3			dci_gainpos_slp4		dci_gainpos_slp5		reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp3	Slope of region 4 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[21:12]	RW	dci_gainpos_slp4	Slope of region 5 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[11:2]	RW	dci_gainpos_slp5	Slope of region 6 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[1:0]	RO	reserved	Reserved.

CH_VPDCIPOSSLP2

CH_VPDCIPOSSLP2 is positive adjustment slope register 2 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C48	CH_VPDCIPOSSLP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp6			dci_gainpos_slp7		reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp6	Slope of region 7 when the picture is adjusted from dark to bright. It is a 10-bit signed number.
[21:12]	RW	dci_gainpos_slp7	Slope of region 8 when the picture is adjusted from dark to bright.

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			It is a 10-bit signed number.
[11:0]	RO	reserved	Reserved.

CH_VPDCINEGTHR0

CH_VPDCINEGTHR0 is negative adjustment threshold register 0 of the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C4C	CH_VPDCINEGTHR0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_thr1		dci_gainneg_thr2		dci_gainneg_thr3		dci_gainneg_thr4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr1	Threshold 1 for luminance Y when the picture is adjusted from bright to dark.
[23:16]	RW	dci_gainneg_thr2	Threshold 2 for luminance Y when the picture is adjusted from bright to dark.
[15:8]	RW	dci_gainneg_thr3	Threshold 3 for luminance Y when the picture is adjusted from bright to dark.
[7:0]	RW	dci_gainneg_thr4	Threshold 4 for luminance Y when the picture is adjusted from bright to dark.

CH_VPDCINEGTHR1

CH_VPDCINEGTHR1 is negative adjustment threshold register 1 of the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C50	CH_VPDCINEGTHR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_thr5		dci_gainneg_thr6		dci_gainneg_thr7		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr5	Threshold 5 for luminance Y when the picture is adjusted from bright to dark.
[23:16]	RW	dci_gainneg_thr6	Threshold 6 for luminance Y when the picture is adjusted from bright to dark.
[15:8]	RW	dci_gainneg_thr7	Threshold 7 for luminance Y when the picture is adjusted from bright to dark.

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[7:0]	RO	reserved	Reserved.

CH_VPDCINEGGAIN0

CH_VPDCINEGGAIN0 is negative adjustment gain register 0 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C54	CH_VPDCINEGGAIN0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_cbcr0	dci_gainneg_cbcr1	dci_gainneg_cbcr2	dci_gainneg_cbcr3	dci_gainneg_cbcr4	dci_gainneg_cbcr5	dci_gainneg_cbcr6	dci_gainneg_cbcr7
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from bright to dark.
[27:24]	RW	dci_gainneg_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from bright to dark.
[23:20]	RW	dci_gainneg_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from bright to dark.
[19:16]	RW	dci_gainneg_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from bright to dark.
[15:12]	RW	dci_gainneg_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from bright to dark.
[11:8]	RW	dci_gainneg_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from bright to dark.
[7:4]	RW	dci_gainneg_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from bright to dark.
[3:0]	RW	dci_gainneg_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from bright to dark.

CH_VPDCINEGGAIN1

CH_VPDCINEGGAIN1 is negative adjustment gain register 1 for the DCI adjustment unit.

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Offset Address	Register Name	Total Reset Value
0x1C58	CH_VPDCINEGGAIN1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_cbcr8	reserved						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from bright to dark.
[27:0]	RO	reserved	Reserved.

CH_VPDCINEGSLP0

CH_VPDCINEGSLP0 is negative adjustment slope register 0 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C5C	CH_VPDCINEGSLP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp0			dci_gainneg_slp1			dci_gainneg_slp2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp0	Slope of region 1 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[21:12]	RW	dci_gainneg_slp1	Slope of region 2 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[11:2]	RW	dci_gainneg_slp2	Slope of region 3 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[1:0]	RO	reserved	Reserved.

CH_VPDCINEGSLP1

CH_VPDCINEGSLP1 is negative adjustment slope register 1 for the DCI adjustment unit.

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Offset Address	Register Name	Total Reset Value
0x1C60	CH_VPDCINEGSLP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp3			dci_gainneg_slp4		dci_gainneg_slp5		reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp3	Slope of region 4 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[21:12]	RW	dci_gainneg_slp4	Slope of region 5 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[11:2]	RW	dci_gainneg_slp5	Slope of region 6 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[1:0]	RO	reserved	Reserved.

CH_VPDCINEGSLP2

CH_VPDCINEGSLP2 is negative adjustment slope register 2 for the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x1C64	CH_VPDCINEGSLP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp6			dci_gainneg_slp7		reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp6	Slope of region 7 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[21:12]	RW	dci_gainneg_slp7	Slope of region 8 when the picture is adjusted from bright to dark. It is a 10-bit signed number.
[11:0]	RO	reserved	Reserved.

CH_SPLIT_CFG

CH_SPLIT_CFG is a split enable register.

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Offset Address	Register Name	Total Reset Value
0x1E00	CH_SPLIT_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	en	Split enable. 0: disabled 1: enabled

CH_SPLIT_VERSION

CH_SPLIT_VERSION is a split version register.

Offset Address	Register Name	Total Reset Value
0x1E0C	CH_SPLIT_VERSION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	Split version.

CH_SPLIT_DATA_CFG

CH_SPLIT_DATA_CFG is a split configuration register.

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Offset Address	Register Name	Total Reset Value
0x1E10	CH_SPLIT_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dc_data							reserved				data_sel		split_en		ex_yuv_en				ex_v_en	ex_u_en	ex_y_en	replace_v_en	replace_u_en	replace_y_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:16]	RW	dc_data	Split data DC component.
[15:12]	RO	reserved	Reserved
[11:10]	RW	data_sel	Data component to be split. 00: data 0 01: data 1 10: data 2 11: data 0
[9]	RW	split_en	Data split enable.
[8:6]	RW	ex_yuv_en	YUV sequence of split data. 000: YUV output 001: YVU output 010: UYV output 011: UVY output 100: VYU output 101: VUY output Other values: YUV output
[5]	RW	ex_v_en	Exchange with the adjacent data of the split V channel (data cannot be repeatedly exchanged, and data is exchanged every two data segments). 0: disabled 1: enabled
[4]	RW	ex_u_en	Exchange with the adjacent data of the split U channel (data cannot be repeatedly exchanged, and data is exchanged every two data segments). 0: disabled 1: enabled

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[3]	RW	ex_y_en	Exchange with the adjacent data of the split Y channel (data cannot be repeatedly exchanged, and data is exchanged every two data segments). 0: disabled 1: enabled
[2]	RW	replace_v_en	Split data storage enable (stored in the V channel) 0: disabled 1: enabled
[1]	RW	replace_u_en	Split data storage enable (stored in the U channel) 0: disabled 1: enabled
[0]	RW	replace_y_en	Split data storage enable (stored in the Y channel) 0: disabled 1: enabled

CH_SPLIT_DATA_VERSION

CH_SPLIT_DATA_VERSION is a split data version register.

Offset Address	Register Name	Total Reset Value
0x1E14	CH_SPLIT_DATA_VERSION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data_version															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	data_version	Split data version.

CH_SPLIT_DATA_BITWIDTH

CH_SPLIT_DATA_BITWIDTH is a split data bit width register.

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Offset Address	Register Name	Total Reset Value
0x1E18	CH_SPLIT_DATA_BITWIDTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data_bitw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	data_bitw	Bit width of split data.

CH_SPLIT_CTRL_I

CH_SPLIT_CTRL_I is a split register update control register.

Offset Address	Register Name	Total Reset Value
0x1EE4	CH_SPLIT_CTRL_I	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	Split register update mode. 0: update by update register 1: update by frame

CH_SPLIT_UPDATE

CH_SPLIT_UPDATE is a split register update register.

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Offset Address	Register Name	Total Reset Value
0x1EEC	CH_SPLIT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	newer	Split register update. This bit is automatically cleared for each frame.

CH_AF_CFG

CH_AF_CFG is an AF control register.

Offset Address	Register Name	Total Reset Value
0x2000	CH_AF_CFG	0x0000_01DB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ck_gt_en	reserved																				crop_en	data_mode	squ_mode	peak_mode	iir1_en2	iir1_en1	iir1_en0	iir0_en2	iir0_en1	iir0_en0	en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1	1

Bits	Access	Name	Description
[31]	RW	ck_gt_en	AF clock gating enable.
[30:10]	RO	reserved	Reserved.
[11]	RW	crop_en	Crop enable. 0: disabled 1: enabled
[9]	RW	data_mode	Statistics mode. 0: five groups of values 1: nine groups of values
[8]	RW	squ_mode	AF statistics square mod.e 0: Statistics are directly added. 1: Statistics are added after the square calculation.

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[7]	RW	peak_mode	AF statistics peak value mode. 0: All values of a block are selected for statistics. 1: The maximum value in each line of a block is selected for statistics.
[6]	RW	iir1_en2	Enable for cascaded IIR2 among the three IIRs in group 2. 0: disabled 1: enabled
[5]	RW	iir1_en1	Enable for cascaded IIR1 among the three IIRs in group 2. 0: disabled 1: enabled
[4]	RW	iir1_en0	Enable for cascaded IIR0 among the three IIRs in group 2. 0: disabled 1: enabled
[3]	RW	iir0_en2	Enable for cascaded IIR2 among the three IIRs in group 1. 0: disabled 1: enabled
[2]	RW	iir0_en1	Enable for cascaded IIR1 among the three IIRs in group 1. 0: disabled 1: enabled
[1]	RW	iir0_en0	Enable for cascaded IIR0 among the three IIRs in group 1. 0: disabled 1: enabled
[0]	RW	en	AF enable. 0: disabled 1: enabled

CH_AF_ZONE

CH_AF_ZONE is an AF block configuration register.

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Offset Address	Register Name	Total Reset Value
0x2010	CH_AF_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	vnum	Number of vertical AF blocks (15 blocks at most).
[7:5]	RO	reserved	Reserved
[4:0]	RW	hnum	Number of horizontal AF blocks (17 blocks at most and at least eight horizontal pixels for each block).

CH_AF_CROP_START

CH_AF_CROP_START is an AF crop start coordinate configuration register.

Offset Address	Register Name	Total Reset Value
0x2014	CH_AF_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				y_pos				reserved				x_pos			
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	y_pos	Start vertical coordinate of the AF picture to be cropped.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	x_pos	Start horizontal coordinate of the AF picture to be cropped.

CH_AF_CROP_SIZE

CH_AF_CROP_SIZE is an AF crop picture size configuration register.

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Offset Address	Register Name	Total Reset Value
0x2018	CH_AF_CROP_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					vsize	reserved	hsize
Reset	0 0 0 0	0 1 0 0	0 0 1 1	0 1 1 1	0 0 0 0	0 1 1 1	0 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	vsize	Height of the cropped AF picture. The configured value is the actual value minus 1.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	hsize	Width of the cropped AF picture. The configured value is the actual value minus 1.

CH_AF_IIRG0

CH_AF_IIRG0 is an AF IIR filtering parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x2020	CH_AF_IIRG0	0x00A1_00A0

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		iirg0_1		reserved		iirg0_0	
Reset	0 0 0 0	0 0 0 0	1 0 1 0	0 0 0 1	0 0 0 0	0 0 0 0	1 0 1 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	iirg0_1	G0 gain of AF IIR filtering group 2 (the configured value of 0x640 ISP_AF_SHIFT is affected).
[15:8]	RO	reserved	Reserved.
[7:0]	RW	iirg0_0	G0 gain of AF IIR filtering group 1 (the configured value of 0x640 ISP_AF_SHIFT is affected).

CH_AF_IIRG1

CH_AF_IIRG1 is an AF IIR filtering parameter 1 register.

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Offset Address	Register Name	Total Reset Value
0x2024	CH_AF_IIRG1	0x0244_01BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						iirg1_1										reserved						iirg1_0									
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg1_1	G1 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg1_0	G1 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_IIRG2

CH_AF_IIRG2 is an AF IIR filtering parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x2028	CH_AF_IIRG2	0x0328_0328

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						iirg2_1										reserved						iirg2_0									
Reset	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg2_1	G2 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg2_0	G2 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_IIRG3

CH_AF_IIRG3 is an AF IIR filtering parameter 3 register.

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Offset Address	Register Name	Total Reset Value
0x202C	CH_AF_IIRG3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		iirg3_1		reserved		iirg3_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg3_1	G3 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg3_0	G3 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_IIRG4

CH_AF_IIRG4 is an AF IIR filtering parameter 4 register.

Offset Address	Register Name	Total Reset Value
0x2030	CH_AF_IIRG4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		iirg4_1		reserved		iirg4_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg4_1	G4 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg4_0	G4 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_IIRG5

CH_AF_IIRG5 is an AF IIR filtering parameter 5 register.

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Offset Address	Register Name	Total Reset Value
0x2034	CH_AF_IIRG5	0x0284_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						iirg5_1										reserved						iirg5_0									
Reset	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg5_1	G5 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg5_0	G5 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_IIRG6

CH_AF_IIRG6 is an AF IIR filtering parameter 6 register.

Offset Address	Register Name	Total Reset Value
0x2038	CH_AF_IIRG6	0x033C_033C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						iirg6_1										reserved						iirg6_0									
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	iirg6_1	G6 gain of AF IIR filtering group 2. It is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	iirg6_0	G6 gain of AF IIR filtering group 1. It is a signed number and cannot be the negative boundary value −512.

CH_AF_SHIFT

CH_AF_SHIFT is an AF IIR filtering shift parameter register.

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Offset Address	Register Name	Total Reset Value
0x2040	CH_AF_SHIFT	0x0027_1027

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	iirshift1_3	iirshift1_2	iirshift1_1	iirshift1_0	iirshift0_3	iirshift0_2	iirshift0_1	iirshift0_0
Reset	0 0 0 0	0 0 0 0	0 0 1 0	0 1 1 1	0 0 0 1	0 0 0 0	0 0 1 0	0 1 1 1

Bits	Access	Name	Description
[31:28]	RW	iirshift1_3	Shift adjustment for IIR2 in AF IIR filtering group 2.
[27:24]	RW	iirshift1_2	Shift adjustment for IIR1 in AF IIR filtering group 2.
[23:20]	RW	iirshift1_1	Shift adjustment for IIR0 in AF IIR filtering group 2.
[19:16]	RW	iirshift1_0	Input shift adjustment for AF IIR filtering group 2. iirg0_0 ≥ 128, iirshift0_0 ≥ 4 iirg0_0 ≥ 64, iirshift0_0 ≥ 3 iirg0_0 ≥ 32, iirshift0_0 ≥ 2 iirg0_0 ≥ 16, iirshift0_0 ≥ 1)
[15:12]	RW	iirshift0_3	Shift adjustment for IIR2 in AF IIR filtering group 1.
[11:8]	RW	iirshift0_2	Shift adjustment for IIR1 in AF IIR filtering group 1.
[7:4]	RW	iirshift0_1	Shift adjustment for IIR0 in AF IIR filtering group 1.
[3:0]	RW	iirshift0_0	Input shift adjustment for AF IIR filtering group 1. iirg0_0 ≥ 128, iirshift0_0 ≥ 4 iirg0_0 ≥ 64, iirshift0_0 ≥ 3 iirg0_0 ≥ 32, iirshift0_0 ≥ 2 iirg0_0 ≥ 16, iirshift0_0 ≥ 1)

CH_AF_FIRH0

CH_AF_FIRH0 is an AF FIR filtering parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x2050	CH_AF_FIRH0	0x0030_0030

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			firh0_1	reserved			firh0_0
Reset	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:16]	RW	firh0_1	H0 gain of AF FIR filtering group 2. It is a signed number and cannot be the negative boundary value −32.

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[15:6]	RO	reserved	Reserved.
[5:0]	RW	firh0_0	H0 gain of AF FIR filtering group 1. It is a signed number and cannot be the negative boundary value −32.

CH_AF_FIRH1

CH_AF_FIRH1 is an AF FIR filtering parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x2054	CH_AF_FIRH1	0x0015_002B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh1_1				reserved												firh1_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:16]	RW	firh1_1	H1 gain of AF FIR filtering group 2. It is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved.
[5:0]	RW	firh1_0	H1 gain of AF FIR filtering group 1. It is a signed number and cannot be the negative boundary value −32.

CH_AF_FIRH2

CH_AF_FIRH2 is an AF FIR filtering parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x2058	CH_AF_FIRH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh2_1				reserved												firh2_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:16]	RW	firh2_1	H2 gain of AF FIR filtering group 2. It is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved.
[5:0]	RW	firh2_0	H2 gain of AF FIR filtering group 1. It is a signed number and cannot be the negative boundary value −32.

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CH_AF_FIRH3

CH_AF_FIRH3 is an AF FIR filtering parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x205C	CH_AF_FIRH3	0x002B_0015

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh3_1				reserved												firh3_0			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:16]	RW	firh3_1	H3 gain of AF FIR filtering group 2. It is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved.
[5:0]	RW	firh3_0	H3 gain of AF FIR filtering group 1. It is a signed number and cannot be the negative boundary value −32.

CH_AF_FIRH4

CH_AF_FIRH4 is an AF FIR filtering parameter 4 register.

Offset Address	Register Name	Total Reset Value
0x2060	CH_AF_FIRH4	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh4_1				reserved												firh4_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:16]	RW	firh4_1	H4 gain of AF FIR filtering group 2. It is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved.
[5:0]	RW	firh4_0	H4 gain of AF FIR filtering group 1. It is a signed number and cannot be the negative boundary value −32.

CH_AF_IIRTHRE

CH_AF_IIRTHRE is an AF IIR filtering threshold register.

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Offset Address	Register Name	Total Reset Value
0x2070	CH_AF_IIRTHRE	0x0014_0064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				thre2_x												reserved				thre1_x											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	thre2_x	Statistics threshold of AF IIR filtering group 2
[15:11]	RO	reserved	Reserved.
[10:0]	RW	thre1_x	Statistics threshold of AF IIR filtering group 1

CH_AF_FIRTHRE

CH_AF_FIRTHRE is an AF FIR filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x2074	CH_AF_FIRTHRE	0x000A_0032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				thre2_y												reserved				thre1_y											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	thre2_y	Statistics threshold of AF FIR filtering group 2
[15:11]	RO	reserved	Reserved.
[10:0]	RW	thre1_y	Statistics threshold of AF FIR filtering group 1

CH_AF_ACC_SHIFT

CH_AF_ACC_SHIFT is an AF statistics shift register.

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Offset Address	Register Name	Total Reset Value
0x2078	CH_AF_ACC_SHIFT	0x0002_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			acc_shift_y	acc_shift2_v	acc_shift1_v	acc_shift2_h	acc_shift1_h
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:16]	RW	acc_shift_y	Luminance Y statistics shift (0−15). Y in CH_AF_STAT_RDATA is shifted.
[15:12]	RW	acc_shift2_v	Shift of vertical FIR filtering statistics in group 2 (0−15). V2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	acc_shift1_v	Shift of vertical FIR filtering statistics in group 1 (0−15). V1 in CH_AF_STAT_RDATA is shifted.
[7:4]	RW	acc_shift2_h	Shift of horizontal IIR filtering statistics in group 2 (0−15). H2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	acc_shift1_h	Shift of horizontal IIR filtering statistics in group 1 (0−15). H1 in CH_AF_STAT_RDATA is shifted.

CH_AF_CNT_SHIFT

CH_AF_CNT_SHIFT is an AF count value shift register.

Offset Address	Register Name	Total Reset Value
0x207C	CH_AF_CNT_SHIFT	0x0000_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				cnt_shift2_v	cnt_shift1_v	cnt_shift2_h	cnt_shift1_h
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:12]	RW	cnt_shift2_v	Shift of the vertical FIR filtering count value in group 2 (0−15). vcnt2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	cnt_shift1_v	Shift of the vertical FIR filtering count value in group 1 (0−15). vcnt1 in CH_AF_STAT_RDATA is shifted.
[7:4]	RW	cnt_shift2_h	Shift of the horizontal IIR filtering count value in group 2 (0−15). hcnt2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	cnt_shift1_h	Shift of the horizontal FIR filtering count value in group 1 (0−15). hcnt1 in CH_AF_STAT_RDATA is shifted.

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CH_AF_SIZE

CH_AF_SIZE is an AF picture size register.

Offset Address	Register Name	Total Reset Value
0x20E0	CH_AF_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	vsize	AF picture height. The configured value is the actual value minus 1.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	hsize	AF picture width. The configured value is the actual value minus 1.

CH_AF_STAT_RDATA

CH_AF_STAT_RDATA is a read statistics register for AF blocks.

Offset Address	Register Name	Total Reset Value
0x2100~0x2CF0	CH_AF_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	af_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	af_stat_rdata	V1[16], H1[16], V2[16], H2[16], Y[16], hcnt1, hcnt2, vcnt1, and vcnt2 information about each block. The following is the information for each address: When data_mode is 0: 0x00: {V1 (16 bits), H1 (16 bits)} of block 1 0x04: {V2 (16 bits), H2 (16 bits)} of block 1 0x08: Y (16 bits) of block 1 The same rule applies to other addresses. When data_mode is 1: 0x00: {Y_h (6 bits), V1 (13 bits), H1 (13 bits)} of block 1 0x04: {Y_l (6 bits), V2 (13 bits), H2 (13 bits)} of block 1

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			0x08: {vcnt2 (8 bits), vcnt1 (8 bits), hcnt2 (8 bit), hcnt1 (8 bits)} of block 1 The same rule applies to other addresses. Note: V1 is the vertical FIR filtering statistics of group 1. V2 is the vertical FIR filtering statistics of group 2. H1 is the horizontal IIR filtering statistics of group 1. H2 is the horizontal IIR filtering statistics of group 2. Y is luminance statistics. vcnt1 is the number of times that the FIR filtering value is above the threshold. vcnt2 is the number of times that the FIR filtering value is above the threshold. hcnt1 is the number of times that the IIR filtering value is above the threshold. hcnt2 is the number of times that the IIR filtering value is above the threshold.

ISP_MAX_ADDR

ISP_MAX_ADDR is an ISP buffer maximum address register.

Offset Address	Register Name	Total Reset Value
0x10000	ISP_MAX_ADDR	0x0000_051F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr	Maximum address for the ISP buffer.

ISP_MAX_ADDR_DIS_Y

ISP_MAX_ADDR_DIS_Y is a DIS Y depth maximum address register.

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Offset Address	Register Name	Total Reset Value
0x10004	ISP_MAX_ADDR_DIS_Y	0x0000_03DB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_y											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr_y	Maximum address for the DIS Y depth.

ISP_MAX_ADDR_SINTER1

ISP_MAX_ADDR_SINTER1 is an ISP sinter buffer 1 maximum address register.

Offset Address	Register Name	Total Reset Value
0x10008	ISP_MAX_ADDR_SINTER1	0x0000_03CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_sinter1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr_sinter1	Maximum address for sinter buffer 1.

ISP_MAX_ADDR_SINTER2

ISP_MAX_ADDR_SINTER2 is an ISP sinter buffer 2 maximum address register.

Offset Address	Register Name	Total Reset Value
0x1000C	ISP_MAX_ADDR_SINTER2	0x0000_01EF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_sinter2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr_sinter2	Maximum address for sinter buffer 2.

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ISP_TIMING

ISP_TIMING is an ISP timing configuration register.

Offset Address	Register Name	Total Reset Value
0x10010	ISP_TIMING	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vsync_sel	hsync_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vsync_sel	Toggle processing control from vsync. 0: not processed 1: processed
[0]	RW	hsync_sel	hsync select. 0: input hsync 1: input de

ISP_BYTE_EN

ISP_BYTE_EN is an ISP byte enable register.

Offset Address	Register Name	Total Reset Value
0x10020	ISP_BYTE_EN	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												byte_en			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	byte_en	Byte enable. 0: disabled 1: enabled

ISP_MAX_ADDR_FSTITCH

ISP_MAX_ADDR_FSTITCH is an ISP FSTITCH maximum address register.

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Offset Address	Register Name	Total Reset Value
0x10024	ISP_MAX_ADDR_FSTITCH	0x0000_051F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_fstitch											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	max_addr_fstitch	Maximum address for the ISP FSTITCH.

ISP_CH_SWITCH

ISP_CH_SWITCH is an ISP input switch register.

Offset Address	Register Name	Total Reset Value
0x10028	ISP_CH_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									isp_ch_switch_4			reserved	isp_ch_switch_3			reserved	isp_ch_switch_2			reserved	isp_ch_switch_1			reserved	isp_ch_switch_0			reserved			isp_ch_switch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:20]	RW	isp_ch_switch_4	ISP FPN black frame input data select. 0 indicates channel 0, 1 indicates channel 1, 2 indicates channel 2, 3 indicates channel 3, and 4 indicates the FPN black frame input.
[19]	RO	reserved	Reserved.
[18:16]	RW	isp_ch_switch_3	Input data select for ISP channel 3.0 indicates channel 0, 1 indicates channel 1, 2 indicates channel 2, 3 indicates channel 3, and 4 indicates the FPN black frame input.
[15]	RO	reserved	Reserved.
[14:12]	RW	isp_ch_switch_2	Input data select for ISP channel 2. 0 indicates channel 0, 1 indicates channel 1, 2 indicates channel 2, 3 indicates channel 3, and 4 indicates the FPN black frame input.
[11]	RO	reserved	Reserved.

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[10:8]	RW	isp_ch_switch_1	Input data select for ISP channel 1. 0 indicates channel 0, 1 indicates channel 1, 2 indicates channel 2, 3 indicates channel 3, and 4 indicates the FPN black frame input.
[7]	RO	reserved	Reserved.
[6:4]	RW	isp_ch_switch_0	Input data select for ISP channel 0. 0 indicates channel 0, 1 indicates channel 1, 2 indicates channel 2, 3 indicates channel 3, and 4 indicates the FPN black frame input.
[3:1]	RO	reserved	Reserved.
[0]	RW	isp_ch_switch_en	ISP input switch enable. 0: disabled 1: enabled

ISP_CROP_CFG

ISP_CROP_CFG is a crop register.

Offset Address	Register Name	Total Reset Value
0x10030	ISP_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														n1_en	n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	n1_en	Region 1 enable. 0: disabled 1: enabled
[0]	RW	n0_en	Region 0 enable. 0: disabled 1: enabled

ISP_CROP_WIN

ISP_CROP_WIN is a crop window register.

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Offset Address	Register Name	Total Reset Value
0x10034	ISP_CROP_WIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Window height (in line). The configured value is the actual value minus 1.
[15:0]	RW	width	Window width (in pixel). The configured value is the actual value minus 1.

ISP_CROP0_START

ISP_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x10038	ISP_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	y_start																x_start															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	y_start	ID of the line from which pictures start to be captured.
[15:0]	RW	x_start	ID of the pixel from which pictures start to be captured.

ISP_CROP0_SIZE

ISP_CROP0_SIZE is a crop size configuration register for region 0.

Offset Address	Register Name	Total Reset Value
0x1003C	ISP_CROP0_SIZE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.

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[15:0]	RW	width	Width (in pixel) of a line in the obtained picture. The configured value is the actual value minus 1.

ISP_CROP1_START

ISP_CROP1_START is a crop start position register for region 1.

Offset Address	Register Name	Total Reset Value
0x10040	ISP_CROP1_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	y_start																x_start															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	y_start	ID of the line from which pictures start to be captured.
[15:0]	RW	x_start	ID of the pixel from which pictures start to be captured.

ISP_CROP1_SIZE

ISP_CROP1_SIZE is a crop size configuration register for region 1.

Offset Address	Register Name	Total Reset Value
0x10044	ISP_CROP1_SIZE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:0]	RW	width	Width (in pixel) of a line in the obtained picture. The configured value is the actual value minus 1.

ISP_INT

ISP_INT is an ISP interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x100F0	ISP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7	int6	int5	int4	int3	int2	int1	int0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	int7	Status of ISP interrupt 7. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	int6	Status of ISP interrupt 6. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	int5	Status of ISP interrupt 5. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	int4	Status of ISP interrupt 4. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	int3	Status of ISP interrupt 3. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	int2	Status of ISP interrupt 2. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	int1	Status of ISP interrupt 1. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	int0	Status of ISP interrupt 0. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_INT_MASK

ISP_INT_MASK is an ISP interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0x100F8	ISP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7_en	int6_en	int5_en	int4_en	int3_en	int2_en	int1_en	int0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	int7_en	ISP interrupt 7 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RW	int6_en	ISP interrupt 6 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RW	int5_en	ISP interrupt 5 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	int4_en	ISP interrupt 4 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	int3_en	ISP interrupt 3 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RW	int2_en	ISP interrupt 2 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RW	int1_en	ISP interrupt 1 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	int0_en	ISP interrupt 0 mask. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_FPN_CFG

ISP_FPN_CFG is an FPN configuration register.

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Offset Address	Register Name	Total Reset Value
0x10100	ISP_FPN_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gt_en	reserved																					line_frame	calib_corr	reserved							enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	gt_en	FPN clock gating enable. 0: disabled (the clock is normal) 1: enabled (the clock is disabled)
[30:10]	RO	reserved	Reserved
[9]	RW	line_frame	FPN frame/line mode. 0: frame mode 1: line mode
[8]	RW	calib_corr	FPN correction/calibration mode. 0: correction mode 1: calibration mode
[7:1]	RO	reserved	Reserved.
[0]	RW	enable	FPN enable. 1: enabled 0: disabled

ISP_FPN_CALIB_START

ISP_FPN_CALIB_START is an FPN calibration start signal register.

Offset Address	Register Name	Total Reset Value
0x10104	ISP_FPN_CALIB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															calib_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	RW	calib_start	FPN calibration start. This bit is automatically cleared.

ISP_FPN_CORR_CFG

ISP_FPN_CORR_CFG is an FPN correction enable register.

Offset Address	Register Name	Total Reset Value
0x10108	ISP_FPN_CORR_CFG	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														correct1_en	correct0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	correct1_en	FPN correction enable for channel 1. 0: disabled 1: enabled
[0]	RW	correct0_en	FPN correction enable for channel 0. 0: disabled 1: enabled

ISP_FPN_STAT

ISP_FPN_STAT is an FPN calibration status register.

Offset Address	Register Name	Total Reset Value
0x1010C	ISP_FPN_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hcnt												reserved				vcnt				reserved							busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RO	hcnt	Number of lines

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[15:14]	RO	reserved	Reserved.
[13:8]	RO	vcnt	Number of calibrated frames.
[7:1]	RO	reserved	Reserved.
[0]	RO	busy	FPN calibration status 0: idle 1: being calibrated

ISP_FPN_WHITE_LEVEL

ISP_FPN_WHITE_LEVEL is an FPN calibration white point configuration register.

Offset Address	Register Name	Total Reset Value
0x10110	ISP_FPN_WHITE_LEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				white_level											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:0]	RW	white_level	FPN calibration white point configuration.

ISP_FPN_DIVCOEF

ISP_FPN_DIVCOEF is an FPN calibration division coefficient register.

Offset Address	Register Name	Total Reset Value
0x10118	ISP_FPN_DIVCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				divcoef											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	divcoef	FPN calibration division coefficient.

ISP_FPN_FRAMELOG2

ISP_FPN_FRAMELOG2 is an FPN calibrated frame number register.

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Offset Address	Register Name	Total Reset Value
0x1011C	ISP_FPN_FRAMELOG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													cpi_fpn_framelog2		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	cpi_fpn_framelog2	Number of FPN calibrated frames. The configured value is obtained by taking the logarithm of the number of frames to 2.

ISP_FPN_SUM0

ISP_FPN_SUM0 is an FPN calibration accumulated sum low register.

Offset Address	Register Name	Total Reset Value
0x10120	ISP_FPN_SUM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Lower bits of the FPN calibration accumulated sum.

ISP_FPN_SUM1

ISP_FPN_SUM1 is an FPN calibration accumulated sum high register.

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Offset Address	Register Name	Total Reset Value
0x10124	ISP_FPN_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Upper bits of the FPN calibration accumulated sum.

ISP_FPN_CORR0

ISP_FPN_CORR0 is FPN correction configuration register 0.

Offset Address	Register Name	Total Reset Value
0x10130	ISP_FPN_CORR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	offset	FPN correction bias.

ISP_FPN_CORR1

ISP_FPN_CORR1 is FPN correction configuration register 1.

Offset Address	Register Name	Total Reset Value
0x10134	ISP_FPN_CORR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	offset	FPN correction bias.

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ISP_FPN_SHIFT

ISP_FPN_SHIFT is an FPN shift configuration register.

Offset Address	Register Name	Total Reset Value
0x10140	ISP_FPN_SHIFT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	frame_calib_shift	reserved	out_shift	reserved	in_shift	reserved	fpn_shift
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	frame_calib_shift	Number of left shift bits for the last output frame during frame calibration.
[23:20]	RO	reserved	Reserved.
[19:16]	RW	out_shift	Number of left shift bits for the output.
[15:12]	RO	reserved	Reserved.
[11:8]	RW	in_shift	Number of right shift bits for the input.
[7:4]	RO	reserved	Reserved.
[3:0]	RW	fpn_shift	Number of right shift bits for the input FPN.

ISP_FPN_MAX_O

ISP_FPN_MAX_O is an FPN maximum output value register.

Offset Address	Register Name	Total Reset Value
0x10150	ISP_FPN_MAX_O	0x0000_3FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				max_o			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	max_o	Maximum value of the FPN output.

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ISP_FPN_PIC_SIZE

ISP_FPN_PIC_SIZE is an FPN picture size register.

Offset Address	Register Name	Total Reset Value
0x101D0	ISP_FPN_PIC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, the configured value is 1919 if the actual picture height is 1920.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, the configured value is 1079 if the actual picture width is 1080.

ISP_FPN_REG_UPDATE

ISP_FPN_REG_UPDATE is a register update register.

Offset Address	Register Name	Total Reset Value
0x101D4	ISP_FPN_REG_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															isp_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	isp_newer	FPN update. This bit is automatically cleared for each frame.

ISP_FPN_UPDATE_MODE

ISP_FPN_UPDATE_MODE is a register update mode register.

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Offset Address	Register Name	Total Reset Value
0x101D8	ISP_FPN_UPDATE_MODE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_update_mode	FPN update mode. 0: reg_newer update 1: update by frame

ISP_DITHER_CFG

ISP_DITHER_CFG is a dither configuration register.

Offset Address	Register Name	Total Reset Value
0x10200	ISP_DITHER_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Dither enable. 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved.

ISP_VB_CFG0

ISP_VB_CFG0 is vertical blanking clock gating configuration register 0.

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Offset Address	Register Name	Total Reset Value
0x10300	ISP_VB_CFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											mem_pf_en	reserved			gt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	mem_pf_en	Vertical blanking mem power-off enable. 0: disabled 1: enabled
[3:1]	RO	reserved	Reserved.
[0]	RW	gt_en	Vertical blanking clock gating enable. 0: disabled 1: enabled

ISP_VB_CFG1

ISP_VB_CFG1 is vertical blanking clock gating configuration register 1.

Offset Address	Register Name	Total Reset Value
0x10304	ISP_VB_CFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															vb_hb_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	vb_hb_en	Data set-to-0 enable for vertical blanking and horizontal blanking. 0: disabled 1: enabled

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ISP_VB_CLKNUM

ISP_VB_CLKNUM is a wait clock number configuration register for vertical blanking clock gating

Offset Address	Register Name	Total Reset Value
0x10310	ISP_VB_CLKNUM	0x0000_FC60

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clknum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	clknum	Number of wait clocks for vertical blanking clock gating.

ISP_VB_DLYN

ISP_VB_DLYN is a wait clock number configuration register for disabling the clock after the vertical blanking clock gating indicator is valid.

Offset Address	Register Name	Total Reset Value
0x10314	ISP_VB_DLYN	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dlyn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	RW	dlyn	Number of wait clocks for disabling the clock after the vertical blanking clock gating indicator is valid.

ISP_VB_TRIG

ISP_VB_TRIG is a vertical blanking clock count reset trigger configuration register.

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Offset Address	Register Name	Total Reset Value
0x10318	ISP_VB_TRIG	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													vld_rst_en	hs_rst_en	vs_rst_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	vld_rst_en	Valid count reset enable. 0: disabled 1: enabled
[1]	RW	hs_rst_en	hsync count reset enable. 0: disabled 1: enabled
[0]	RW	vs_rst_en	vsync count reset enable. 0: disabled 1: enabled

ISP_VB_GT_STAT

ISP_VB_GT_STAT is a vertical blanking clock gating status register.

Offset Address	Register Name	Total Reset Value
0x1031C	ISP_VB_GT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gt_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	gt_stat	Vertical blanking clock gating status.

ISP_VB_SIZE

ISP_VB_SIZE is a picture size register.

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Offset Address	Register Name	Total Reset Value
0x103F0	ISP_VB_SIZE	0x0797_0A1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Picture height (in line). The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1.

ISP_FPN_MEM

ISP_FPN_MEM is an FPN line mode memory register.

Offset Address	Register Name	Total Reset Value
0x12000~0x1343C	ISP_FPN_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem1																mem0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mem1	Line mode FPN. There are 1296 registers in total.
[15:0]	RW	mem0	Line mode FPN.

ISP_DEHAZE_CFG

ISP_DEHAZE_CFG is a dehaze enable register.

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Offset Address	Register Name	Total Reset Value
0x19000	ISP_DEHAZE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clken	reserved																														en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clken	Dehaze clock gating enable. 0: The dehaze clock is normal. 1: The dehaze clock is disabled (low power consumption).
[30:1]	RO	reserved	Reserved.
[0]	RW	en	Dehaze enable. 0: disabled 1: enabled

ISP_DEHAZE_VERSION

ISP_DEHAZE_VERSION is a dehaze version register.

Offset Address	Register Name	Total Reset Value
0x1900C	ISP_DEHAZE_VERSION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	Dehaze version.

ISP_DEHAZE_PRE_UPDATE

ISP_DEHAZE_PRE_UPDATE is a dehaze statistics update register.

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Offset Address	Register Name	Total Reset Value
0x19010	ISP_DEHAZE_PRE_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															pre_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	pre_update	Dehaze statistics update. This bit is automatically cleared for each frame.

ISP_DEHAZE_BLK_SIZE

ISP_DEHAZE_BLK_SIZE is a dehaze block size configuration register.

Offset Address	Register Name	Total Reset Value
0x19014	ISP_DEHAZE_BLK_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								block_sizeh								reserved								block_sizev							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24:16]	RW	block_sizeh	Horizontal block size. The configured value is the actual value minus 1.
[15:9]	RO	reserved	Reserved.
[8:0]	RW	block_sizev	Vertical block size. The configured value is the actual value minus 1.

ISP_DEHAZE_BLK_NUM

ISP_DEHAZE_BLK_NUM is a dehaze block number configuration register.

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Offset Address	Register Name	Total Reset Value
0x19018	ISP_DEHAZE_BLK_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												block_numh				reserved												block_numv			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	block_numh	Number of horizontal blocks. The configured value is the actual value minus 1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	block_numv	Number of vertical blocks. The configured value is the actual value minus 1.

ISP_DEHAZE_DC_SIZE

ISP_DEHAZE_DC_SIZE is a bilinear interpolation point number configuration register.

Offset Address	Register Name	Total Reset Value
0x1901C	ISP_DEHAZE_DC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						dc_numh						dc_numv			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:5]	RW	dc_numh	Number of bilinear interpolation horizontal points. The configured value is the actual value minus 1.
[4:0]	RW	dc_numv	Number of bilinear interpolation vertical points. The configured value is the actual value minus 1.

ISP_DEHAZE_X

ISP_DEHAZE_X is a configuration register for the horizontal phase difference between the pixels of the dehaze enlarged picture.

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Offset Address	Register Name	Total Reset Value
0x19020	ISP_DEHAZE_X	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phase_x																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:0]	RW	phase_x	Horizontal phase difference between the pixels of the enlarged picture. It is an unsigned integer.

ISP_DEHAZE_Y

ISP_DEHAZE_Y is a configuration register for the vertical phase difference between the pixels of the dehaze enlarged picture.

Offset Address	Register Name	Total Reset Value
0x19024	ISP_DEHAZE_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phase_y																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:0]	RW	phase_y	Vertical phase difference between the pixels of the enlarged picture. It is an unsigned integer.

ISP_DEHAZE_STAT_MODE

ISP_DEHAZE_STAT_MODE is a dehaze statistics mode control register.

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Offset Address	Register Name	Total Reset Value
0x19028	ISP_DEHAZE_STAT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													max_mode	min_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	max_mode	Maximum value statistics control. 0: Mean filtering is performed on RGB components, and then the RGB components corresponding to the maximum RGB sum of each window are counted. 1: The RGB components corresponding to the maximum RGB sum of each window are counted.
[1:0]	RW	min_mode	Minimum value statistics control. 00: The minimum value among RGB components is selected for mean filtering, and the minimum value of each window is counted. 01: The minimum value among RGB components is selected, and the minimum value of each window is counted. 10: The minimum value of the RGB mean filtering results is selected for mean filtering, and the minimum value of each window is counted. Other values: not processed

ISP_DEHAZE_NEG_MODE

ISP_DEHAZE_NEG_MODE is a dehaze inversion enable register.

Offset Address	Register Name	Total Reset Value
0x1902C	ISP_DEHAZE_NEG_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															neg_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

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[0]	RW	neg_mode	Inversion mode control. 0: normal mode 1: inversion mode

ISP_DEHAZE_AIR

ISP_DEHAZE_AIR is a dehaze airglow configuration register.

Offset Address	Register Name	Total Reset Value
0x19030	ISP_DEHAZE_AIR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								air_r								air_g								air_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	air_r	Airglow A corresponding to the R channel.
[15:8]	RW	air_g	Airglow A corresponding to the G channel.
[7:0]	RW	air_b	Airglow A corresponding to the B channel.

ISP_DEHAZE_THLD

ISP_DEHAZE_THLD is a T threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x19034	ISP_DEHAZE_THLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								thld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	thld	T threshold coefficient. It is an unsigned integer.

ISP_DEHAZE_GSTRTH

ISP_DEHAZE_GSTRTH is a T calculation coefficient configuration register.

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Offset Address	Register Name	Total Reset Value
0x19038	ISP_DEHAZE_GSTRTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gstrth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	gstrth	T calculation coefficient. It is an unsigned integer.

ISP_DEHAZE_BLTHLD

ISP_DEHAZE_BLTHLD is a minimum value filtering threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x1903C	ISP_DEHAZE_BLTHLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								blthld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	blthld	Minimum value filtering threshold coefficient. It is an unsigned integer.

ISP_DEHAZE_CTRL_I

ISP_DEHAZE_CTRL_I is a dehaze register update control register.

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Offset Address	Register Name	Total Reset Value
0x190E4	ISP_DEHAZE_CTRL_I	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	Dehaze register update mode. 0: update by update register 1: update by frame

ISP_DEHAZE_UPDATE

ISP_DEHAZE_UPDATE is a dehaze register update register.

Offset Address	Register Name	Total Reset Value
0x190EC	ISP_DEHAZE_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	newer	Dehaze register update. This bit is automatically cleared for each frame.

ISP_DEHAZE_SIZE

ISP_DEHAZE_SIZE is a DEHAZE picture size register.

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Offset Address	Register Name	Total Reset Value
0x190F0	ISP_DEHAZE_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	height	Window height (in line). The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	width	Window width (in pixel). The configured value is the actual value minus 1.

ISP_DEHAZE_MINSTAT

ISP_DEHAZE_MINSTAT is a dehaze minimum value statistics register.

Offset Address	Register Name	Total Reset Value
0x19100–0x191FC	ISP_DEHAZE_MINSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	minstat																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	minstat	Dehaze minimum value statistics write address. There are 64 minimum values in total.

ISP_DEHAZE_PRESTAT

ISP_DEHAZE_PRESTAT is a dehaze processed minimum value statistics register.

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Offset Address	Register Name	Total Reset Value
0x19200–0x192FC	ISP_DEHAZE_PRESTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	prestat																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	prestat	Processed minimum value statistics to be written. There are 64 minimum values in total.

ISP_DEHAZE_MAXSTAT

ISP_DEHAZE_MAXSTAT is a dehaze maximum value statistics register.

Offset Address	Register Name	Total Reset Value
0x19400–0x197FC	ISP_DEHAZE_MAXSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								maxstat																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	maxstat	Dehaze maximum value statistics. There are 256 maximum values in total.

ISP_DEHAZE_LUT

ISP_DEHAZE_LUT is a dehaze strength LUT configuration register.

Offset Address	Register Name	Total Reset Value
0x19800–0x19BFC	ISP_DEHAZE_LUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lutdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	lutdata	Dehaze strength LUT. The LUT has 256 entries.

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10.2 VDP

10.2.1 Overview

The video display processor (VDP) reads video and graphics data from the memory, overlays the data at the video and graphics layers, and transmits the data through the display channel.

10.2.2 Architecture

Figure 10-17 shows the block diagram of the VDP.

Figure 10-17 Block diagram of the VDP

The following describes the major concepts:

- Surface: data path of bus inputs. The surface reads and processes the bus data of a layer. The surfaces include the video layer V1 and graphics layer G2.
- Display channel: It includes the HD display channel DHD1.
- Crossbar mixer (CBM): It supports overlapping of the video layer and graphics layer.
- Memory access controller (MAC): Each module reads data from the memory over the AXI bus. The MAC arbitrates the requests from all surfaces.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers

  Include the bus configuration registers, interrupt registers, and version register.
- Surface registers

  Include the video layer configuration registers and graphics layer configuration registers.
- Display channel registers

  Include the DHD1 configuration registers.

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The VDP has the following features:

- Digital output interfaces. The HD output interfaces support ITU-R BT.1120 outputs, whereas the SD output interfaces support ITU-R BT.656 outputs.
- Analog output interfaces. The HD channel DHD1 supports the CVBS output.
- Video layer (V1)
- Graphics layer (G2)
- Overlay
- One video channel. It has a separate vertical timing interrupt (indicating the end of a field/frame) and a low bandwidth interrupt.

10.2.3 Operating Mode

10.2.3.1 Clock Configurations

The VDP clock source can be set to either of the following clocks:

- Interface output clock source 1: BPLL
- Interface output clock source 2: VPLL

For details, see the description of the PERI_CRG13 for 3.2.7 section.

10.2.3.2 Reset

The VDP supports a hard reset signal and a soft reset signal.

CAUTION

Before soft-resetting the AXI bus, do as follows:

- Disable all layers.
- Configure the bus reset request after the next field/frame interrupt is detected.

10.2.3.3 Bus Configurations

AXI Master

The VDP provides one master interface to improve bus access efficiency.

The VDP supports the AXI master. The data read/write requests of V1 and G2 can be implemented by using the master.

APB Register Configuration

The VDP registers are read and written over the APB interface. The base address for VDP registers is 0x205C_0000, the register addressing space is 64 KB, and the address offset range is 0x0000–0xFFFF.

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Outstanding Configuration

The depth of the AXI master outstanding ranges from 0 to 7. When the outstanding depth is set to 0, the AXI master does not operate the bus.

10.2.3.4 Analog Output Interface

The VDP SD channel supports a CVBS output interface. It supports two output standards: PAL, NTSC.

10.2.3.5 Digital Output Interfaces

The VDP supports two digital interface output modes: ITU-R BT.1120 and ITU-R BT.656.

10.2.3.6 Interrupts

VDP interrupts are classified into:

- Vertical timing interrupt
- Low bandwidth interrupt
- VDAC offload interrupt

Vertical Timing Interrupt

The position of generating the vertical timing interrupt can be configured.

- The VDP supports one vertical timing interrupt, indicating the end of a frame or field.
- The interrupt can be generated by frame or field.
- In progressive display mode, the vertical timing interrupt must be generated by frame.
- In interlaced display mode, the vertical timing interrupt can be generated by frame or field. You are advised to set the interrupt generation mode to generation by field for HD and generation by frame for SD.
- Interrupt mask can be configured.
- The threshold for the vertical timing interrupt can be configured.
- Each interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP allows the low bandwidth status to be reported by using an interrupt.

- The VDP supports one low bandwidth interrupt, indicating low bandwidth of a frame or field.
- The interrupt can be masked.
- Each interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

VDAC Offload Interrupt

The VDP allows the VDAC connection status to be reported by using an interrupt.

- The VDP supports a VDAC offload interrupt, indicating no load connected currently.
- The interrupt can be masked.
- Each interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

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10.2.4 Function Description

10.2.4.1 Video Layer

Features

The video layer has the following features:

- Input pixel formats of semi-planar420 and semi-planar422
- Uncompressed and lossless compressed data sources
- Minimum input resolution of 32 x 32 and maximum input resolution of 2176 x 1080
- Minimum output resolution of 32 x 32 and maximum output resolution of 1920 x 1080
- A multiple of 2 for the input horizontal resolution
- A multiplier of 4 for the interlaced 420 input vertical resolution and a multiple of 2 for the other input vertical resolutions
- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, uncompressed data source (2-byte-aligned), and compressed data source (16-byte-aligned)
- User-defined source luminance and chrominance stride, 16-byte-aligned
- Vertical chrominance up sampling, replication mode
- Horizontal chrominance up scaling (IFIR), replication mode, bilinear interpolation, and 16-order half-band filtering
- Color space conversion (CSC) and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255

DCMP

The data resource to be read by the VDP may be compressed data, which reduces the bandwidth. V1 decompresses the compressed data to restore it to original YCbCr pixel points.

Horizontal Cropping

The input width can be cropped horizontally.

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422. V1 converts the data format in replication mode.

IFIR (Horizontal Chrominance Up Sampling)

Horizontal chrominance up sampling converts the YUV422 data format into YUV444.

This function can be implemented in three ways:

- Replication
- Bilinear interpolation
- 16-order half-band filtering

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CSC

- CSC between YCbCr BT601 and BT709
- Adjustment of luminance, hue, and saturation

10.2.4.2 Graphics Layer

Features

The graphics layer has the following features:

- Input pixel formats of ARGB1555, ARGB4444, and ARGB8888
- Minimum input resolution of 32 x 32 and maximum input resolution of 1920 x 1080
- Minimum output resolution of 32 x 32 and maximum output resolution of 1920 x 1080
- A multiple of 2 for the input horizontal or vertical resolution
- Interlaced mode and progressive mode
- Frame update and field update
- User-defined source start address, 128-bit-aligned (16-byte-aligned)
- User-defined source stride, 128-bit-aligned (16-byte-aligned)
- CSC
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255
- Enabling or disabling of the pixel alpha, and alpha0 or alpha1 for the picture in ARGB1555 format with pixel alpha
- Colorkey processing
- Premultiplication

CSC

CSC between RGB2YCbCr601 and RGB2YCbCr709 is supported.

Alpha Processing

The alpha value sources of the graphics layer are as follows:

- Pixel alpha value: overlay attribute of a pixel
- Global alpha value: overlay attributes of a layer

There is a special pixel alpha value. In RGB1555 format, the alpha value is only one bit. This bit is the index of the alpha value but not the actual alpha value. The index value is used to select the actual alpha value from the alpha register. When the index value is 0, alpha0 is selected; when the index value is other values, alpha1 is selected.

Colorkey

- The key mode is configurable. The pixels inside or outside the range can be selected for key processing.
- The key bit can be masked.

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Premultiplication

Input data can be premultiplied data. In this case, the colorkey function must be disabled.

10.2.4.3 Overlaying

The VDP supports overlaying of V1 and G2.

Features

- Bottom-to-top overlaying
- User-defined overlaying background color
- User-defined priority of the overlaid surface

10.2.4.4 Display Channel

Video Channel Features

- DHD1 can function as an HD or SD output channel.
- Only one output timing is supported in an application scenario. HD and SD timings cannot be output at the same time.
- The following typical output timings are supported: 720p, 1080p, 1080i, PAL, NTSC.

Timing Configuration

The VDP output interfaces support typical and non-typical timings to connect to different interfaces.

CAUTION

Interfaces must be disabled before timing parameters are configured and be enabled after configuration.

10.2.4.5 HD Output Interface BT.1120

Features

- 10 bits to 8 bits dither
- YCbCr444-to-YCbCr422 horizontal chrominance down sampling (DFIR)
- Clipping for data clamp (Y 16−235 and C 16−240 according to the interface protocol)
- Typical output timings of 720p, 1080p, and 1080i
- Bypass mode and truncation and point discarding for dither and DFIR
- 16-bit data (Y for upper bits and C for lower bits)
- Exchange of the output sequence of output YC components

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10.2.4.6 SD Output Interface BT.656

Features

- 10 bits to 8 bits dither
- YCbCr444-to-YCbCr422 horizontal chrominance down sampling (DFIR)
- Clipping for data clamp (Y 16−235 and C 16−240 according to the interface protocol)
- Typical output timings of NTSC and PAL
- 13.5 MHz clk_vo_hd clock and 27 MHz clk_vo_bt clock required for the CRG

10.2.4.7 SD Output Interface CVBS

Features

- Clipping for data clamp (Y 64−960 and C 64−960)
- Digital simulation for the digitalized analog TV encoder (DATE)
- VDAC automatic detection for the DATE
- Typical output timings of NTSC, PAL

10.2.5 Register Summary

Table 10-6 describes VDP registers.

Table 10-6 Summary of VDP registers (base address: 0x205C_0000)

Offset Address	Register	Description	Page
0x0000	VOCTRL	VO control register	10-185
0x0004	VOINTSTA	VO interrupt status register (read-only)	10-186
0x0008	VOMSKINTSTA	VO masked interrupt status register	10-188
0x000C	VOINTMSK	VDP interrupt mask register	10-190
0x0010	VDPVERSION1	VDP version register 1	10-193
0x0014	VDPVERSION2	VDP version register 2	10-193
0x0034	VOAXICTRL	VO AXI bus configuration register	10-193
0x0100	VO_MUX	VO interface multiplexing register	10-194
0x0104	VO_MUX_DAC	VO DAC interface multiplexing register	10-194
0x0108	VO_MUX_TESTSYNC	VO interface test register	10-195
0x010C	VO_MUX_TESTDATA	VO interface test data register	10-196
0x0120	VO_DAC_CTRL	VO DAC control register	10-197
0x0134	VO_DAC_R_CTRL	VO DAC R channel control register	10-198

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Offset Address	Register	Description	Page
0x0140	VO_DAC_STAT0	VO DAC status 0 register	10-198
0x0400	COEF_DATA	Virtual coefficient register	10-199
0x1000	V1_CTRL	V1 configuration register (non-instant register)	10-199
0x1004	V1_UPD	V1 channel update enable register	10-201
0x1028	V1_IRESO	V1 input resolution register (non-instant register)	10-202
0x102C	V1_ORESO	V1 output resolution register (non-instant register)	10-202
0x1038	V1_CBMPARA	V1 overlay parameter register (non-instant register)	10-203
0x1044	V1_CPOS	Horizontal crop coordinate register for the source picture	10-203
0x1060	V1_DFPOS	V1 surface start position (in the display window) register (non-instant register)	10-204
0x1064	V1_DLPOS	V1 surface end position (in the display window) register (non-instant register)	10-204
0x1068	V1_VFPOS	V1 surface content start position (in the display window) register (non-instant register)	10-205
0x106C	V1_VLPOS	V1 surface content end position (in the display window) register (non-instant register)	10-205
0x1070	V1_BK	V1 background color register	10-206
0x1074	V1_ALPHA	V1 background filling color alpha register	10-206
0x1080	V1_CSC_IDC	V1 CSC input DC component register (instant register)	10-207
0x1084	V1_CSC_ODC	V1 CSC output DC component register (instant register)	10-207
0x1088	V1_CSC_IODC	V1 CSC input/output DC component register (instant register)	10-208
0x108C	V1_CSC_P0	V1 CSC parameter 0 register (instant register)	10-208
0x1090	V1_CSC_P1	V1 CSC parameter 1 register (instant register)	10-209
0x1094	V1_CSC_P2	V1 CSC parameter 2 register (instant register)	10-210

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Offset Address	Register	Description	Page
0x1098	V1_CSC_P3	V1 CSC parameter 3 register (instant register)	10-210
0x109C	V1_CSC_P4	V1 CSC parameter 4 register (instant register)	10-211
0x1180	V1_IFIRCOEF01	IFIR filtering coefficient 0/1 register	10-211
0x1184	V1_IFIRCOEF23	IFIR filtering coefficient 2/3 register	10-212
0x1188	V1_IFIRCOEF45	IFIR filtering coefficient 4/5 register	10-212
0x118C	V1_IFIRCOEF67	IFIR filtering coefficient 6/7 register	10-213
0x1204	V1_P0LADDR	V1 luminance address register	10-213
0x1208	V1_P0CADDR	V1 chrominance address register	10-214
0x120C	V1_P0STRIDE	V1 stride register	10-214
0x7000	G2_CTRL	G2 configuration register	10-215
0x7004	G2_UPD	G2 update enable register	10-216
0x7010	G2_ADDR	G2 address register	10-217
0x701C	G2_STRIDE	G2 stride register	10-217
0x7020	G2_IRESO	G2 input resolution register (non-instant register)	10-218
0x7024	G2_SFPOS	G2 surface read data start position (in the source bitmap) register (non-instant register)	10-218
0x7030	G2_CBMPARA	Overlaying parameter register (non-instant register)	10-219
0x7034	G2_CKEYMAX	Maximum colorkey value register (non-instant register)	10-220
0x7038	G2_CKEYMIN	Minimum colorkey value register (non-instant register)	10-220
0x703C	G2_CMASK	Colorkey mask value register (non-instant register)	10-221
0x7040	G2_PARAADDR	G2 LUT coefficient address register	10-221
0x7044	G2_PARAUP	G2 LUT coefficient update register	10-222
0x7080	G2_DFPOS	G2 surface start position (in the display window) register (non-instant register)	10-222
0x7084	G2_DLPOS	G2 surface end position (in the display window) register (non-instant register)	10-223

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Offset Address	Register	Description	Page
0x7088	G2_VFPOS	G2 surface content start position (in the display window) register (non-instant register)	10-223
0x708C	G2_VLPOS	G2 surface content end position (in the display window) register (non-instant register)	10-224
0x7090	G2_BK	G2 background color register	10-224
0x7094	G2_ALPHA	G2 background filling color alpha register	10-225
0x70C0	G2_CSC_IDC	G2 CSC input DC component register (instant register)	10-225
0x70C4	G2_CSC_ODC	G2 CSC output DC component register (instant register)	10-226
0x70C8	G2_CSC_IODC	G2 CSC input/output DC component register (instant register)	10-227
0x70CC	G2_CSC_P0	G2 CSC parameter 0 register (instant register)	10-227
0x70D0	G2_CSC_P1	G2 CSC parameter 1 register (instant register)	10-228
0x70D4	G2_CSC_P2	G2 CSC parameter 2 register (instant register)	10-229
0x70D8	G2_CSC_P3	G2 CSC parameter 3 register (instant register)	10-229
0x70DC	G2_CSC_P4	G2 CSC parameter 4 register (instant register)	10-230
0xB420	CBM_BKG2	CBM mixer 2 overlay background color register	10-230
0xB428	CBM_MIX2	CBM mixer 2 priority configuration register	10-231
0xC400	DHD1_CTRL	DSD1 global control register	10-232
0xC404	DHD1_VSYNC	Top field vertical sync timing register in interlaced output mode or frame vertical sync timing register in progressive output mode	10-234
0xC408	DHD1_HSYNC1	Horizontal sync configuration register in interlaced or progressive output mode	10-235
0xC40C	DHD1_HSYNC2	Horizontal sync configuration register in interlaced or progressive output mode (non-instant register)	10-235

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Offset Address	Register	Description	Page
0xC410	DHD1_VPLUS	Bottom field vertical sync timing register in interlaced output mode (non-instant register)	10-235
0xC414	DHD1_PWR	Sync signal pulse width register (non-instant register)	10-236
0xC418	DHD1_VTTHD3	Vertical timing threshold register (instant register)	10-236
0xC41C	DHD1_VTTHD	Vertical timing threshold register (instant register)	10-237
0xC4B0	DHD1_PARATHD	PARA coefficient update pointer threshold register	10-238
0xC4C0	DHD1_START_POS	DHD1 start signal start position register	10-239
0xC4F0	DHD1_STATE	DHD1 status register	10-239
0xD200	BT_CTRL	BT.656/BT.1120 control register	10-240
0xD210	BT_CLIP0_L	BT.656/BT.1120 clip lowest threshold register (instant register)	10-241
0xD214	BT_CLIP0_H	BT.656/BT.1120 clip highest threshold register (instant register)	10-242
0xD280	BT_DITHER0_CTRL	BT.656/BT.1120 dither control register	10-242
0xD284	BT_DITHER0_COEF0	BT.656/BT.1120 dither coefficient 0 register	10-243
0xD288	BT_DITHER0_COEF1	BT.656/BT.1120 dither coefficient 1 register	10-244
0xD308	DATE_SYNC_INV	Sync signal polarity configuration register in DATE external sync timing input mode	10-244
0xD310	DATE_CLIP0_L	DATE clip lowest threshold register (instant register)	10-245
0xD314	DATE_CLIP0_H	DATE clip highest threshold register (instant register)	10-246
0xF200	DATE_COEFF0	Standard parameter configuration register	10-246
0xF204	DATE_COEFF1	Amplitude configuration register	10-251
0xF208	DATE_COEFF2	DATE coefficient 2 register	10-253
0xF20C	DATE_COEFF3	DATE coefficient 3 register	10-253
0xF210	DATE_COEFF4	DATE coefficient 4 register	10-253
0xF214	DATE_COEFF5	DATE coefficient 5 register	10-254

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Offset Address	Register	Description	Page
0xF218	DATE_COEFF6	DATE coefficient 6 register	10-254
0xF254	DATE_COEFF21	Output matrix control register	10-255
0xF258	DATE_COEFF22	Discrete time oscillator (DTO) initial phase configuration register	10-258
0xF25C	DATE_COEFF23	Video output delay configuration register	10-259
0xF260	DATE_COEFF24	ColorBurst start position register	10-260
0xF264	DATE_COEFF25	SECAM preemphasis curve input coefficient register	10-260
0xF268	DATE_COEFF26	Preemphasis curve input coefficient register	10-261
0xF26C	DATE_COEFF27	SECAM preemphasis curve output coefficient register	10-261
0xF270	DATE_COEFF28	SECAM color sync start coordinate register	10-262
0xF274	DATE_COEFF29	SECAM color sync end coordinate register	10-262
0xF278	DATE_COEFF30	SECAM peak video signal level width coefficient register	10-263
0xF280	DATE_ISRMASK	Interrupt mask register	10-263
0xF284	DATE_ISRSTATE	Interrupt status register	10-264
0xF288	DATE_ISR	Interrupt register	10-264
0xF290	DATE_VERSION	Version register	10-265
0xF294	DATE_COEFF37	Up-sampling filtering coefficient register 1	10-265
0xF298	DATE_COEFF38	Up-sampling filtering coefficient register 2	10-266
0xF29C	DATE_COEFF39	Up-sampling filtering coefficient register 3	10-266
0xF2A0	DATE_COEFF40	Up-sampling filtering coefficient register 4	10-267
0xF2A4	DATE_COEFF41	Up-sampling filtering coefficient register 5	10-267
0xF2A8	DATE_COEFF42	Up-sampling filtering coefficient register 6	10-267
0xF2C0	DATE_DACDET1	DAC automatic detection register 1	10-268
0xF2C4	DATE_DACDET2	DAC automatic detection register 2	10-268
0xF2C8	DATE_COEFF50	Over-sampling filtering coefficient register 1	10-269
0xF2CC	DATE_COEFF51	Over-sampling filtering coefficient register 2	10-270

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Offset Address	Register	Description	Page
0xF2D0	DATE_COEFF52	Over-sampling filtering coefficient register 3	10-270
0xF2D4	DATE_COEFF53	Over-sampling filtering coefficient register 4	10-270
0xF2D8	DATE_COEFF54	Over-sampling filtering coefficient register 5	10-271
0xF2DC	DATE_COEFF55	Over-sampling filtering coefficient register 6	10-271
0xF2E0	DATE_COEFF56	Over-sampling round-off register	10-272
0xF2E4	DATE_COEFF57	CVBS gain control register	10-272
0xF2E8	DATE_COEFF58	Component gain control register	10-273
0xF2EC	DATE_COEFF59	Clip control register	10-274
0xF2F4	DATE_COEFF61	Timing global control register	10-277
0xF2F8	DATE_COEFF62	Chrominance subcarrier duration control register	10-277
0xF2FC	DATE_COEFF63	Chrominance subcarrier boundary control register	10-278
0xF300	DATE_COEFF64	PAL half-line control register	10-278
0xF304	DATE_COEFF65	RGB active region control register	10-278
0xF308	DATE_COEFF66	Sync timing global control register	10-279
0xF30C	DATE_COEFF67	Line point quantity configuration register	10-280
0xF310	DATE_COEFF68	Sync width configuration register	10-280
0xF314	DATE_COEFF69	Horizontal front blanking (HFB) configuration register	10-280
0xF318	DATE_COEFF70	Line active configuration register	10-281
0xF31C	DATE_COEFF71	Phase shift global control register	10-281
0xF320	DATE_COEFF72	Phase shift register	10-282
0xF324	DATE_COEFF73	Luminance notch coefficient global control register	10-282
0xF328	DATE_COEFF74	Luminance notch coefficient register 1	10-283
0xF32C	DATE_COEFF75	Luminance notch coefficient register 2	10-283
0xF330	DATE_COEFF76	Luminance notch coefficient register 3	10-284
0xF334	DATE_COEFF77	Luminance notch coefficient register 4	10-284

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Offset Address	Register	Description	Page
0xF338	DATE_COEFF78	Luminance notch coefficient register 5	10-285
0xF33C	DATE_COEFF79	Luminance notch coefficient register 6	10-285
0xF340	DATE_COEFF80	Chrominance low-pass coefficient global control register	10-286
0xF344	DATE_COEFF81	Chrominance low-pass coefficient register 1	10-286
0xF348	DATE_COEFF82	Chrominance low-pass coefficient register 2	10-287
0xF34C	DATE_COEFF83	Chrominance low-pass coefficient register 3	10-287
0xF350	DATE_COEFF84	Chrominance low-pass coefficient register 4	10-288

10.2.6 Register Description

VOCTRL

VOCTRL is a VO control register. It is used to configure the arbitration mode of surface bus requests.

Offset Address	Register Name	Total Reset Value
0x0000	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	reserved																											m0_arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_ck_gt_en	VDP clock gating enable. 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved.

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[3:0]	RW	m0_arb_mode	Arbitration mode of data requests of internal surface buses of VO MAC0. 0000: polling 0001: graphics layer first Other values: reserved

VOINTSTA

VOINTSTA is a VO interrupt status register (read-only).

Offset Address	Register Name	Total Reset Value
0x0004	VOINTSTA	0x0000_0044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												v1_dc_err_int	v1_dl_err_int	reserved					vdac0_unload_int	reserved	reserved	reserved	reserved	dhd1uf_int	reserved	reserved	dhd1vrthd1_int	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RO	v1_dc_err_int	V1 chrominance decompression error interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[18]	RO	v1_dl_err_int	V1 luminance decompression error interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[17:13]	RO	reserved	Reserved.
[12]	RO	vdac0_unload_int	DAC0 offload interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[11]	RO	reserved	Reserved.
[10]	RO	reserved	Reserved.
[9]	RO	reserved	Reserved.
[8]	RO	reserved	Reserved.

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[7]	RO	dhd1uf_int	DHD1 low-bandwidth alarm interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RO	dhd1vtthd1_int	DHD1 vertical timing interrupt 1. 0: An interrupt is reported. 1: No interrupt is reported.
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												v1_dc_err_int	v1_dl_err_int	reserved					vdac0_unload_int	reserved	reserved	reserved	reserved	dhd1uf_clr	reserved	reserved	dhd1vtthd1_clr	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	WC	v1_dc_err_int	V1 chrominance decompression error interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[18]	WC	v1_dl_err_int	V1 luminance decompression error interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[17:13]	RO	reserved	Reserved.

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[12]	WC	vdac0_unload_int	DAC0 offload interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[11]	RO	reserved	Reserved.
[10]	RO	reserved	Reserved.
[9]	RO	reserved	Reserved.
[8]	RO	reserved	Reserved.
[7]	WC	dhd1uf_clr	DHD1 low-bandwidth alarm interrupt. 0: An interrupt is reported. 1: No interrupt is reported.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	WC	dhd1vtthd1_clr	DHD1 vertical timing interrupt 1. 0: An interrupt is reported. 1: No interrupt is reported.
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

VOINTMSK

VOINTMSK is a VDP interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0x000C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												v1_dc_err_int	v1_dl_err_int	reserved					vdac0_unload_intmsk	reserved	reserved	reserved	reserved	dhd1uf_intmsk	reserved	reserved	dhd1vtthd1_intmsk	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RW	v1_dc_err_int	Mask for the V1 chrominance decompression error interrupt. 0: masked 1: enabled
[18]	RW	v1_dl_err_int	Mask for the V1 luminance decompression error interrupt. 0: masked 1: enabled
[17:13]	RO	reserved	Reserved.
[12]	RW	vdac0_unload_intmsk	Mask for the DAC0 offload interrupt. 0: masked 1: enabled
[11]	RO	reserved	Reserved.
[10]	RO	reserved	Reserved.
[9]	RO	reserved	Reserved.
[8]	RO	reserved	Reserved.
[7]	RW	dhd1uf_intmsk	Mask for the DHD1 low-bandwidth alarm interrupt. 0: masked 1: enabled
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RW	dhd1vtthd1_intmsk	Mask for DHD1 vertical timing interrupt 1. 0: masked 1: enabled
[3]	RO	reserved	Reserved.

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[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

VDPVERSION1

VDPVERSION1 is VDP version register 1.

Offset Address	Register Name	Total Reset Value
0x0010	VDPVERSION1	0x7675_6F76

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion1																															
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion1	VDP version 1.

VDPVERSION2

VDPVERSION2 is VDP version register 2.

Offset Address	Register Name	Total Reset Value
0x0014	VDPVERSION2	0x3031_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion2																															
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion2	VDP version 2.

VOAXICTRL

VOAXICTRL is a VO AXI bus configuration register.

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Offset Address	Register Name	Total Reset Value
0x0034	VOAXICTRL	0x0111_0111

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							m0_outstd_rid0
Reset	0 0 0 0	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 1	0 0 0 1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	m0_outstd_rid0	Read ID0 outstanding of AXI master 0. The value ranges from 0 to 7.

VO_MUX

VO_MUX is a VO interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0x0100	VO_MUX	0x0000_0000

Bit	31 30 29 28	27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	digital_sel	yc_sel	reserved						
Reset	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	digital_sel	Digital interface data select. 0: BT.1120 (default) 1: BT.656
[27]	RW	yc_sel	BT.1120 Y/C position select. 0: The upper eight bits are used to transmit the Y component, and the lower eight bits are used to transmit the C component. 1: The upper eight bits are used to transmit the C component, and the lower eight bits are used to transmit the Y component.
[26:0]	RO	reserved	Reserved.

VO_MUX_DAC

VO_MUX_DAC is a VO DAC interface multiplexing register.

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Offset Address	Register Name	Total Reset Value
0x0104	VO_MUX_DAC	0x0000_6540

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dac0_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	dac0_sel	DAC0 output select. The default value is 0x0. 0x0: CVBS video (SDATE) 0x1: SD analog video Y/R component (SDATE) 0x2: SD analog video Cb/G component (SDATE) 0x3: SD analog video Cr/B component (SDATE) 0x4: HD analog video Y/R component (HDATE) 0x5: HD analog video Cb/G component (HDATE) 0x6: HD analog video Cr/B component (HDATE) 0x7: VGA video R component 0x8: VGA video G component 0x9: VGA video B component Other values: reserved

VO_MUX_TESTSYNC

VO_MUX_TESTSYNC is a VO interface test register.

Offset Address	Register Name	Total Reset Value
0x0108	VO_MUX_TESTSYNC	0x0110_0104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_test_en	reserved																											test_field	test_vsync	test_hsync	test_dv
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	vo_test_en	VDP output interface test enable. 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved.

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[3]	RW	test_field	Test value of the field signal.
[2]	RW	test_vsync	Test value of the vsync signal.
[1]	RW	test_hsync	Test value of the hsync signal.
[0]	RW	test_dv	Test value of the dv signal.

VO_MUX_TESTDATA

VO_MUX_TESTDATA is a VO interface test data register.

Offset Address	Register Name	Total Reset Value
0x010C	VO_MUX_TESTDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				test_data																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:0]	RW	test_data	Output data in test mode. The output of DAC0−3 channels is the lower 10 bits of the register value, the output of the BT.1120 channel is the lower 16 bits of the register value, the output of the LCD channel is bits 29−22, 19−12, and 9−2, and the output of other channels is the register value. The output is from upper bits to lower bits in RGB or YUV format.

VO_DAC_CTRL

VO_DAC_CTRL is a VO DAC control register.

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Offset Address	Register Name	Total Reset Value
0x0120	VO_DAC_CTRL	0x2000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	envbg	enextref	reserved											enctr			reserved															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	envbg	Power up enable for the internal band gap of the DAC. 0: disabled 1: enabled
[30]	RW	enextref	VBG output test enable. 0: The internal signal is used, and the VBG pin does not output a signal to the test pin. 1: The VBG pin outputs a signal externally for tests.
[29:19]	RO	reserved	Reserved.
[18:16]	RW	enctr	DAC0 analog biasing enable. The value 3'b000 indicates the normal working mode.
[15:0]	RO	reserved	Reserved.

VO_DAC_R_CTRL

VO_DAC_R_CTRL is a VO DAC R channel control register.

Offset Address	Register Name	Total Reset Value
0x0134	VO_DAC_R_CTRL	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	endac	reserved											dacgc				reserved															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	endac	DAC enable. 0: disabled 1: enabled
[30:21]	RO	reserved	Reserved.
[20:15]	RW	dacgc	DAC gain.

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[14:0]	RO	reserved	Reserved.

VO_DAC_STAT0

VO_DAC_STAT0 is a VO DAC status 0 register.

Offset Address	Register Name	Total Reset Value
0x0140	VO_DAC_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved	reserved	reserved	cableout0	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RO	reserved	Reserved.
[18]	RO	reserved	Reserved.
[17]	RO	reserved	Reserved.
[16]	RO	cableout0	Cableout3 feedback signal.
[15:0]	RO	reserved	Reserved.

COEF_DATA

COEF_DATA is a virtual coefficient register. All VDP coefficients are read from this register. The coefficients are distinguished from each other by using the PARARD read enable register.

Offset Address	Register Name	Total Reset Value
0x0400	COEF_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	coef_data	Coefficient.

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V1_CTRL

V1_CTRL is a V1 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1000	V1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			reserved				crop_en	reserved	precharge_en	precharge_mode	ifir_mode		vup_mode	reserved	lm_rmode		chm_rmode		reserved			demp_en	time_out			reserved	ifmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant). 0: disabled 1: enabled
[30:28]	RO	reserved	Reserved.
[27]	RO	reserved	Reserved.
[26:24]	RO	reserved	Reserved.
[23]	RW	crop_en	Crop enable (non-instant). 0: disabled 1: enabled
[22]	RO	reserved	Reserved.
[21]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[20]	RW	precharge_mode	Pre-charge mode of the FDR FIFO. 0: hardware mode. Hardware automatically enters the pre-charge status on the frame trailer. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode. 00: reserved 01: chrominance IFIR replication mode 10: bilinear interpolation 11: 16-order half-band filtering

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[17]	RW	vup_mode	Surface coefficient update mode. 0: update by frame 1: update by field
[16]	RO	reserved	Reserved.
[15:14]	RW	lm_rmode	Luminance read mode. 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[13:12]	RW	chm_rmode	Chrominance read mode. 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[11:9]	RO	reserved	Reserved.
[8]	RW	dcmp_en	Decompression enable.
[7:5]	RW	time_out	Timeout period.
[4]	RO	reserved	Reserved.
[3:0]	RW	ifmt	Format of the input data. 0x1: SPYCbCr400 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

V1_UPD

V1_UPD is a V1 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x1004	V1_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

V1_IRESO

V1_IRESO is a V1 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1028	V1_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	iw	Width (in pixel). The configured value is the actual width minus 1.

V1_ORESO

V1_ORESO is a V1 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x102C	V1_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	ow	Width (in pixel). The configured value is the actual width minus 1.

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V1_CBMPARA

V1_CBMPARA is a V1 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1038	V1_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates completely transparent.

V1_CPOS

V1_CPOS is a horizontal crop coordinate register for the source picture.

Offset Address	Register Name	Total Reset Value
0x1044	V1_CPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								src_xlpos												src_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	src_xlpos	End coordinates for horizontally cropping the source picture.
[11:0]	RW	src_xfpos	Start coordinates for horizontally cropping the source picture.

V1_DFPOS

V1_DFPOS is a V1 surface start position (in the display window) register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x1060	V1_DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	disp_yfpos	Start coordinates of the display column. The frame height is referenced and its unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row.

V1_DLPOS

V1_DLPOS is a V1 surface end position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1064	V1_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	disp_ylpos	End coordinates of the display column. The frame height is referenced and its unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row.

V1_VFPOS

V1_VFPOS is a V1 surface content start position (in the display window) register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x1068	V1_VFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_yfpos	Start coordinates of the video column. The frame height is referenced and its unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the video row.

V1_VLPOS

V1_VLPOS is a V1 surface content end position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x106C	V1_VLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_ylpos	End coordinates of the video column. The frame height is referenced and its unit is line.
[11:0]	RW	video_xlpos	End coordinates of the video row.

V1_BK

V1_BK is a V1 background color register.

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Offset Address	Register Name	Total Reset Value
0x1070	V1_BK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vbk_y								vbk_cb										vbk_cr									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	vbk_y	Y component.
[19:10]	RW	vbk_cb	Cb component.
[9:0]	RW	vbk_cr	Cr component.

V1_ALPHA

V1_ALPHA is a V1 background filling color alpha register.

Offset Address	Register Name	Total Reset Value
0x1074	V1_ALPHA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vbk_alpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	vbk_alpha	Level 0–255 of the background filling color of the video layer.

V1_CSC_IDC

V1_CSC_IDC is a V1 CSC input DC component register (instant register).

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Offset Address	Register Name	Total Reset Value
0x1080	V1_CSC_IDC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22	21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_en	cscidc1			cscidc0		
Reset	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of the input U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc0	DC parameter of the input V/B component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_ODC

V1_CSC_ODC is a V1 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1084	V1_CSC_ODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22	21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_sign_mode	cscodc1			cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22]	RW	csc_sign_mode	CSC output mode. 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of the output U/G component. The MSB is the signed bit. The value is expressed as a two's complement.

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[10:0]	RW	cscodc0	DC parameter of the output Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_IODC

V1_CSC_IODC is a V1 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1088	V1_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2			cscidc2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:11]	RW	cscodc2	DC parameter of the output V/B component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc2	DC parameter of the input Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_P0

V1_CSC_P0 is a V1 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x108C	V1_CSC_P0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscp01			reserved	cscp00		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp01	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.

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[14:0]	RW	cscp00	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P1

V1_CSC_P1 is a V1 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1090	V1_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp10															reserved	cscp02														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp10	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp02	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P2

V1_CSC_P2 is a V1 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1094	V1_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp12															reserved	cscp11														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

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[30:16]	RW	cscp12	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp11	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P3

V1_CSC_P3 is a V1 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1098	V1_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp21															reserved	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp21	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp20	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P4

V1_CSC_P4 is a V1 CSC parameter 4 register (instant register).

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Offset Address	Register Name	Total Reset Value
0x109C	V1_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscp22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:0]	RW	cscp22	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_IFIRCOEF01

V1_IFIRCOEF01 is an IFIR filtering coefficient 0/1 register.

Offset Address	Register Name	Total Reset Value
0x1180	V1_IFIRCOEF01	0x000F_03F5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef1								reserved						coef0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef1	IFIR filtering coefficient 1.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef0	IFIR filtering coefficient 0.

V1_IFIRCOEF23

V1_IFIRCOEF23 is an IFIR filtering coefficient 2/3 register.

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Offset Address	Register Name	Total Reset Value
0x1184	V1_IFIRCOEF23	0x001C_03EC

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		coef3		reserved		coef2	
Reset	0 0 0 0	0 0 0 0	0 0 0 1	1 1 0 0	0 0 0 0	0 0 1 1	1 1 1 0	1 1 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef3	IFIR filtering coefficient 3.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef2	IFIR filtering coefficient 2.

V1_IFIRCOEF45

V1_IFIRCOEF45 is an IFIR filtering coefficient 4/5 register.

Offset Address	Register Name	Total Reset Value
0x1188	V1_IFIRCOEF45	0x003D_03D8

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		coef5		reserved		coef4	
Reset	0 0 0 0	0 0 0 0	0 0 1 1	1 1 0 1	0 0 0 0	0 0 1 1	1 1 0 1	1 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef5	IFIR filtering coefficient 5.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef4	IFIR filtering coefficient 4.

V1_IFIRCOEF67

V1_IFIRCOEF67 is an IFIR filtering coefficient 6/7 register.

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Offset Address	Register Name	Total Reset Value
0x118C	V1_IFIRCOEF67	0x014A_0395

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	coef7			reserved	coef6		
Reset	0 0 0 0	0 0 0 1	0 1 0 0	1 0 1 0	0 0 0 0	0 0 1 1	1 0 0 1	0 1 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef7	IFIR filtering coefficient 7.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef6	IFIR filtering coefficient 6.

V1_P0LADDR

V1_P0LADDR is a V1 luminance address register.

Offset Address	Register Name	Total Reset Value
0x1204	V1_P0LADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	surface_addr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Luminance start address for the video layer.

V1_P0CADDR

V1_P0CADDR is a V1 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x1208	V1_P0CADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	surface_addr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address for the video layer.

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V1_P0STRIDE

V1_P0STRIDE is a V1 stride register.

Offset Address	Register Name	Total Reset Value
0x120C	V1_P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of the video layer (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the video layer buffer (luminance stride in semi-planar format), 128-bit alignment.

G2_CTRL

G2_CTR is a G2 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7000	G2_CTRL	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	reserved				precharge_en	precharge_mode	reserved										bitext		ifmt							
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant). 0: disabled 1: enabled
[30:28]	RO	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by fame 1: update by field

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[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25:22]	RO	reserved	Reserved.
[21]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[20]	RW	precharge_mode	Pre-charge mode of the FDR FIFO. 0: hardware mode. Hardware automatically enters the pre-charge status on the frame trailer. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[19:10]	RO	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 00: extend 0s to lower bits 10: extend the value of the MSB to a lower bit 11: extend the values of upper bits to lower bits Other values: reserved
[7:0]	RW	ifmt	Format of the input data. 0x48: ARGB4444 0x49: ARGB1555 0x69: AYCbCr8888 Other values: reserved

G2_UPD

G2_UPD is a G2 update enable register.

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Offset Address	Register Name	Total Reset Value
0x7004	G2_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

G2_ADDR

G2_ADDR is a G2 address register. When the horizontal pixel offsets, the address is calculated by following the description of G2_SFPOS.

Offset Address	Register Name	Total Reset Value
0x7010	G2_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address for the surface frame buffer.

G2_STRIDE

G2_STRIDE is a G2 stride register.

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Offset Address	Register Name	Total Reset Value
0x701C	G2_STRIDE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				surface_stride			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	surface_stride	Frame buffer stride.

G2_IRESO

G2_IRESO is a G2 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7020	G2_IRESO	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		ih			iw		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The configured value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The configured value is the actual width minus 1. Note: The actual layer width must be an even number.

G2_SFPOS

G2_SFPOS is a G2 surface read data start position (in the source bitmap) register (non-instant register)

If the read position is not 128-bit-word-aligned, this register indicates the number of pixels required for completing a 128-bit word. Note: The start position offset must be less than or equal to a 128-bit word. The exceeded part is expressed by an address.

The details are as follows:

The following assumes that the start address for the graphics layer of the source picture is addr_ori, the address configured for the logical physical layer is addr_offset, the graphics

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layer offset is offsetp pixels, and the data format of the graphics layer is bpp (for example, the bpp for ARGB8888 is 32). The offset is calculated as follows:

G2ADDR = addr_offset = addr_ori + int (offsetp x bpp/128)

G2SFPOS = offset%128

where int means the rounding operation, and % means the modulo operation.

Offset Address	Register Name	Total Reset Value
0x7024	G2_SFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												src_xfpos			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6:0]	RW	src_xfpos	Start horizontal coordinate of the source picture. The value 0 indicates the first pixel of a line.

G2_CBMPARA

G2_CBMPARA is a G2 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7030	G2_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_mode	key_en	premult_en	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RW	key_mode	Colorkey mode. 0: The color is regarded as the colorkey when the following condition is met: Keymin ≤ Pixel ≤ Keymax 1: The color is regarded as the colorkey when either of the following conditions is met: Pixel ≤ Keymin or Pixel ≥ Keymax
[14]	RW	key_en	Colorkey enable. 0: disabled 1: enabled

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[13]	RW	premult_en	Whether the input bitmap is a premultiplied bitmap. 0: non-premultiplied bitmap 1: premultiplied bitmap
[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:8]	RO	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates completely transparent.

G2_CKEYMAX

G2_CKEYMAX is a maximum colorkey value register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7034	G2_CKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of the colorkey R component.
[15:8]	RW	keyg_max	Maximum value of the colorkey G component.
[7:0]	RW	keyb_max	Maximum value of the colorkey B component.

G2_CKEYMIN

G2_CKEYMIN is a minimum colorkey value register (non-instant register).

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Offset Address	Register Name	Total Reset Value
0x7038	G2_CKEYMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va1		keyr_min		keyg_min		keyb_min	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of the colorkey R component.
[15:8]	RW	keyg_min	Minimum value of the colorkey G component.
[7:0]	RW	keyb_min	Minimum value of the colorkey B component.

G2_CMASK

G2_CMASK is a colorkey mask register (non-instant register).

The value 1 indicates that a pixel bit is retained during colorkey comparison; the value 0 indicates that a pixel bit is forcibly set to 0 during color comparison no matter whether the bit is 0 or 1.

Offset Address	Register Name	Total Reset Value
0x703C	G2_CMASK	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		kmsk_r		kmsk_g		kmsk_b	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of the masked colorkey.
[15:8]	RW	kmsk_g	G component of the masked colorkey.
[7:0]	RW	kmsk_b	B component of the masked colorkey.

G2_PARAADDR

G2_PARAADDR is a G2 LUT coefficient address register.

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Offset Address	Register Name	Total Reset Value
0x7040	G2_PARAADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Surface LUT coefficient address.

G2_PARAUP

G2_PARAUP is a G2 LUT coefficient update register.

Offset Address	Register Name	Total Reset Value
0x7044	G2_PARAUP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gdc_paraup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	gdc_paraup	LUT coefficient update. 0: not updated 1: updated

G2_DFPOS

G2_DFPOS is a G2 surface start position (in the display window) register (non-instant register). The position unit is pixel.

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Offset Address	Register Name	Total Reset Value
0x7080	G2_DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G2_DLPOS

G2_DLPOS is a G2 surface end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x7084	G2_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Row end coordinates.

G2_VFPOS

G2_VFPOS is a G2 surface content start position (in the display window) register (non-instant register). The position unit is pixel.

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Offset Address	Register Name	Total Reset Value
0x7088	G2_VFPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		video_yfpos			video_xfpos		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_yfpos	Start coordinates of the graphics column. The frame height is referenced and its unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the graphics row.

G2_VLPOS

G2_VLPOS is a G2 surface content end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x708C	G2_VLPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		video_ylpos			video_xlpos		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_ylpos	End coordinates of the graphics column. The frame height is referenced and its unit is line.
[11:0]	RW	video_xlpos	End coordinates of the graphics row.

G2_BK

G2_BK is a G2 background color register.

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Offset Address	Register Name	Total Reset Value
0x7090	G2_BK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vbk_y		vbk_cb		vbk_cr		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	vbk_y	Y component.
[19:10]	RW	vbk_cb	Cb component.
[9:0]	RW	vbk_cr	Cr component.

G2_ALPHA

G2_ALPHA is a G2 background filling color alpha register.

Offset Address	Register Name	Total Reset Value
0x7094	G2_ALPHA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						vbk_alpha	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	vbk_alpha	Level 0–128 of the background filling color of the graphics layer.

G2_CSC_IDC

G2_CSC_IDC is a G2 CSC input DC register (instant register).

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Offset Address	Register Name	Total Reset Value
0x70C0	G2_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						csc_mode			csc_en			cscidc1									cscidc0										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:23]	RW	csc_mode	This field is valid only when the G2 CSC coefficients are fixed. 000: reserved 001: YUV2YUV 010: YUV601_RGB 011: YUV709_RGB 100: YUV2YUV_709_601 101: YUV2YUV_601_709 110: RGB2YUV_601 111: RGB2YUV_709
[22]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of the input U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc0	DC parameter of the input V/B component. The MSB is the signed bit. The value is expressed as a two's complement.

G2_CSC_ODC

G2_CSC_ODC is a G2 CSC output DC component register (instant register).

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Offset Address	Register Name	Total Reset Value
0x70C4	G2_CSC_ODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22	21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_sign_mode	cscodc1			cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22]	RW	csc_sign_mode	CSC output mode. 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of the output U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscodc0	DC parameter of the output Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

G2_CSC_IODC

G2_CSC_IODC is a G2 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x70C8	G2_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22	21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2			cscidc2		
Reset	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:11]	RW	cscodc2	DC parameter of the output V/B component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc2	DC parameter of the input Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

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G2_CSC_P0

G2_CSC_P0 is a G2 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70CC	G2_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp01															reserved	cscp00														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp01	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp00	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P1

G2_CSC_P1 is a G2 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D0	G2_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp10															reserved	cscp02														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp10	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.

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[14:0]	RW	cscp02	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P2

G2_CSC_P2 is a G2 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D4	G2_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp12															reserved	cscp11														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:16]	RW	cscp12	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp11	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P3

G2_CSC_P3 is a G2 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D8	G2_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp21															reserved	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

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[30:16]	RW	cscp21	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved.
[14:0]	RW	cscp20	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P4

G2_CSC_P4 is a G2 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70DC	G2_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscp22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:0]	RW	cscp22	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

CBM_BKG2

CBM_BKG2 is a CBM mixer 2 overlay background color register.

Offset Address	Register Name	Total Reset Value
0xB420	CBM_BKG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cbm_bkgy2								cbm_bkgcb2										cbm_bkgcr2									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	cbm_bkgy2	Overlay background color of CBM mixer 2, Y component.

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[19:10]	RW	cbm_bkgcb2	Overlay background color of CBM mixer 2, Cb component.
[9:0]	RW	cbm_bkgcr2	Overlay background color of CBM mixer 2, Cr component.

CBM_MIX2

CBM_MIX2 is a CBM mixer 2 priority configuration register (instant register). The register configuration takes effect only when the vsync signal is valid. mixer_prio_x is overly layer priority *x*.

Offset Address	Register Name	Total Reset Value
0xB428	CBM_MIX2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:4]	RW	mixer_prio1	Drive layer of CBM mixer 2 with priority 1. 0000: no drive layer 1001: V1 1010: G2 Other values: reserved
[3:0]	RW	mixer_prio0	Drive layer of CBM mixer 2 with priority 0. 0000: no drive layer 1001: V1 1010: G2 Other values: reserved

DHD1_CTRL

DHD1_CTRL is a DHD1 global control register.

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Offset Address	Register Name	Total Reset Value
0xC400	DHD1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	cbar_en	cbar_sel	reserved	fpga_lmt_en	fpga_lmt_width							reserved									precharge_en	precharge_mode	reserved				iop	reserved			regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant). Data is output over the interface only when this field is enabled. 0: disabled 1: enabled
[30]	RW	cbar_en	Color bar enable. The color bar is output over the interface when this field is enabled. 0: disabled 1: enabled
[29]	RW	cbar_sel	Color space select for the output color bar (instant). 0: VGA 1: YPbPr
[28]	RO	reserved	Reserved.
[27]	RW	fpga_lmt_en	Debug field. As the frequency of the FPGA clock bus is limited, the 1080i picture cannot be displayed. After this bit is enabled, the picture with 1280-pixel width can be displayed over the 1080i interface. 0: disabled 1: enabled
[26:20]	RW	fpga_lmt_width	Debug field. When fpga_lmt_en is enabled, the active region width of the VDP interface depends on this field. The actual width of the active region is calculated as follows: Actual width of the active region = fpga_lmt_width x 16
[19:11]	RO	reserved	Reserved.
[10]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled

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[9]	RW	precharge_mode	Pre-charge mode of AFIFO. 0: hardware mode. Hardware automatically enters the pre-charge status in the vertical blanking region. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[8:5]	RO	reserved	Reserved.
[4]	RW	iop	Display mode (non-instant). 0: interlaced display 1: progressive display
[3:1]	RO	reserved	Reserved.
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

DHD1_VSYNC

DHD1_VSYNC is a top field vertical sync timing register in interlaced output mode or frame vertical sync timing register in progressive output mode. This register is a non-instant register.

Offset Address	Register Name	Total Reset Value
0xC404	DHD1_VSYNC	0x0011_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:20]	RW	vfb	In interlaced output mode: top vertical front blanking (TVFB) In progressive output mode: vertical front blanking (VFB)
[19:12]	RW	vbb	In interlaced output mode: top vertical back blanking (TVBB) In progressive output mode: vertical back blanking (VBB)+vertical pulse width (VPW)
[11:0]	RW	vact	In interlaced output mode: height of an active picture on the top field In progressive output mode: height of an active picture in a frame. The configured value is the actual value minus 1.

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DHD1_HSYNC1

DHD1_HSYNC1 is a horizontal sync configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC408	DHD1_HSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal back blanking (HBB), in pixel.
[15:0]	RW	hact	Number of horizontal pixels in an active region.

DHD1_HSYNC2

DHD1_HSYNC2 is a horizontal sync configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC40C	DHD1_HSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hmid	Bottom vertical sync active pixel (active region).
[15:0]	RW	hfb	HFB, in pixel.

DHD1_VPLUS

DHD1_VPLUS is a bottom field vertical sync timing in interlaced output mode (non-instant register).

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Offset Address	Register Name	Total Reset Value
0xC410	DHD1_VPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:20]	RW	bvfb	Bottom vertical front blanking (BVFB) in interlaced output mode.
[19:12]	RW	bvbb	Bottom vertical back blanking (BVBB)+VPW in interlaced output mode.
[11:0]	RW	bvact	Height of an active picture in the bottom field in interlaced output mode. The configured value is the actual value minus 1.

DHD1_PWR

DHD1_PWR is a sync signal pulse width register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC414	DHD1_PWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	vpw	VPW. The configured value is the actual value minus 1.
[15:0]	RW	hpw	Horizontal pulse width (HPW). The configured value is the actual value minus 1.

DHD1_VTTHD3

DHD1_VTTHD3 is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

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Offset Address	Register Name	Total Reset Value
0xC418	DHD1_VTTHD3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd4_mode	reserved			vtmgthd4												thd3_mode	reserved			vtmgthd3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	thd4_mode	Mode of generating threshold 4. 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[30:29]	RO	reserved	Reserved.
[28:16]	RW	vtmgthd4	Vertical timing threshold 4 for simultaneously triggering DHD and DSD. The start time of the DSD interface timing is later than that of the DHD interface timing and is equal to the number of lines configured in vtmgthd4.
[15]	RW	thd3_mode	Mode of generating threshold 3. 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[14:13]	RO	reserved	Reserved.
[12:0]	RW	vtmgthd3	Vertical timing threshold 3. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd3_int] interrupt is triggered.

DHD1_VTTHD

DHD1_VTTHD is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

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Offset Address	Register Name	Total Reset Value
0xC41C	DHD1_VTTHD	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd2_mode	reserved			vtmgthd2												thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	thd2_mode	Mode of generating threshold 2. 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[30:29]	RO	reserved	Reserved.
[28:16]	RW	vtmgthd2	Vertical timing threshold 2. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd2_int] interrupt is triggered.
[15]	RW	thd1_mode	Mode of generating threshold 1. 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[14:13]	RO	reserved	Reserved.
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHD1_PARATHD

DHD1_PARATHDis a PARA coefficient update point threshold register.

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Offset Address	Register Name	Total Reset Value
0xC4B0	DHD1_PARATHD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_en	reserved																									para_thd					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dfs_en	DFS enable. 0: disabled 1: enabled
[30:6]	RW	reserved	Reserved.
[5:0]	RW	para_thd	PARA coefficient update point threshold. It indicates the line after the vertical back blanking where the update point occurs. This field is valid only after DFS is enabled.

DHD1_START_POS

DHD1_START_POS is a DHD1 start signal start position register.

Offset Address	Register Name	Total Reset Value
0xC4C0	DHD1_START_POS	0x0000_0805

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																timing_start_pos								start_pos							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:8]	RW	timing_start_pos	Number of lines before the active region where the timing_gen state machine starts to work.
[7:0]	RW	start_pos	Number of lines before the active region where the start signal is generated in online mode.

DHD1_STATE

DHD1_STATE is a DHD1 status register.

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Offset Address	Register Name	Total Reset Value
0xC4F0	DHD1_STATE	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								count_int								vcnt													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	count_int	DHD1 interrupt count. The count value is increased by 1 each time a vertical timing interrupt is reported.
[15:3]	RO	vcnt	Active display line count of DHD1.
[2]	RO	bottom_field	DHD1 top/bottom field indicator 0: top field 1: bottom field
[1]	RO	vblank	DHD1 blanking region indicator. 0: active region 1: blanking region
[0]	RO	vback_blank	DHD1 back blanking region indicator. 0: non-back blanking region 1: blanking region

BT_CTRL

BT_CTRL is a BT.656/BT.1120 control register.

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Offset Address	Register Name	Total Reset Value
0xD200	BT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	bt1120_bypass	reserved																													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	bt1120_bypass	BT.1120 bypass enable (valid only for the BT.1120 interface). 0: disabled 1: enabled
[29:0]	RO	reserved	Reserved.

BT_CLIP0_L

BT_CLIP0_L is a BT.656/BT.1120 clip lowest threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xD210	BT_CLIP0_L	0x0100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		clip_cl2										clip_cl1										clip_cl0									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	clip_cl2	Lowest threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clip_cl1	Lowest threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clip_cl0	Lowest threshold Cr/B of component 0, unsigned integer.

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BT_CLIP0_H

BT_CLIP0_H is a BT.656/BT.1120 clip highest threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xD214	BT_CLIP0_H	0x0EB3_C0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_ch2								clip_ch1										clip_ch0									
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	clip_ch2	Highest threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clip_ch1	Highest threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clip_ch0	Highest threshold Cr/B of component 0, unsigned integer.

BT_DITHER0_CTRL

BT_DITHER0_CTRL is a BT.656/BT.1120 dither control register.

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Offset Address	Register Name	Total Reset Value
0xD280	BT_DITHER0_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md			reserved																												
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select. 000: 12-bit inputs, 10-bit outputs, no dithering, and direct bit truncation 001: 12-bit inputs, 10-bit outputs, and time-domain dithering 010: 12-bit inputs, 10-bit outputs, and spatial-domain dithering 011: 12-bit inputs, 8-bit outputs, and time-domain and spatial-domain dithering 100: 12-bit inputs, 10-bit outputs, and round off 101: 12-bit inputs, 8-bit outputs, and round off Other values: reserved
[28:0]	RO	reserved	Reserved.

BT_DITHER0_COEF0

BT_DITHER0_COEF0 is BT.656/BT.1120 dither coefficient register 0.

Offset Address	Register Name	Total Reset Value
0xD284	BT_DITHER0_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 for time-domain dithering.
[23:16]	RW	dither_coef2	Coefficient 2 for time-domain dithering.
[15:8]	RW	dither_coef1	Coefficient 1 for time-domain dithering.
[7:0]	RW	dither_coef0	Coefficient 0 for time-domain dithering.

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BT_DITHER0_COEF1

BT_DITHER0_COEF1 is BT.656/BT.1120 dither coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xD288	BT_DITHER0_COEF1	0xDD66_4400

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dither_coef7		dither_coef6		dither_coef5		dither_coef4	
Reset	1 1 0 1	1 1 0 1	0 1 1 0	0 1 1 0	0 1 0 0	0 1 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 for time-domain dithering.
[23:16]	RW	dither_coef6	Coefficient 6 for time-domain dithering.
[15:8]	RW	dither_coef5	Coefficient 5 for time-domain dithering.
[7:0]	RW	dither_coef4	Coefficient 4 for time-domain dithering.

DATE_SYNC_INV

DATE_SYNC_INV is a sync signal polarity configuration register in DATE external sync timing input mode. The setting of this register takes effect immediately after configuration, that is, the polarity of the corresponding sync signal is immediately affected.

Offset Address	Register Name	Total Reset Value
0xD308	DATE_SYNC_INV	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							f_inv	vs_inv	hs_inv	dv_inv
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RW	f_inv	Output phase inversion enable for the odd/even field indicator signal (instant). 0: disabled 1: enabled
[2]	RW	vs_inv	Output phase inversion enable for the vertical sync pulse (instant). 0: disabled 1: enabled

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[1]	RW	hs_inv	Output phase inversion enable for the horizontal sync pulse (instant). 0: disabled 1: enabled
[0]	RW	dv_inv	Output phase inversion enable for the data valid signal (instant). 0: disabled 1: enabled

DATE_CLIP0_L

DATE_CLIP0_L is a DATE clip lowest threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xD310	DATE_CLIP0_L	0x0100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_cl2								clip_cl1										clip_cl0									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	clip_cl2	Lowest threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clip_cl1	Lowest threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clip_cl0	Lowest threshold Cr/B of component 0, unsigned integer.

DATE_CLIP0_H

DATE_CLIP0_H is a DATE clip highest threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

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Offset Address	Register Name	Total Reset Value
0xD314	DATE_CLIP0_H	0x0EB3_C0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_ch2								clip_ch1										clip_ch0									
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:20]	RW	clip_ch2	Highest threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clip_ch1	Highest threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clip_ch0	Highest threshold Cr/B of component 0, unsigned integer.

DATE_COEFF0

DATE_COEFF0 is a standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xF200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved	pal_half_en	pbpr_lpf_en	scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel				sync_mode_sel		sync_mode_scart	length_sel	agc_amp_sel		luma_dl			reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth of the chrominance low-pass filter. 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved

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[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL standards, the black level is 7.5 IRE higher than the blanking level; for other standards, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28]	RO	reserved	Reserved.
[27]	RW	pal_half_en	PAL half line reduction enable. 0: disabled 1: enabled
[26]	RW	pbpr_lpf_en	Component chrominance low-pass filtering enable. 0: disabled 1: enabled
[25]	RW	scanline	Number of scanned lines in each frame based on standards. For the (M) NTSC, NTSC-J, and (M) PAL standards, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL standards, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame
[24]	RW	rgb_en	Whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable. 0: disabled 1: enabled
[22]	RW	fm_sel	FMSECAM frequency modulation select. 0: SIN mode 1: COS mode

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[21:18]	RW	style_sel	CVBS/S-Video output signal standard when this bit works with the scanline bit. When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0001: (M) NTSC standard 0010: NTSC-J standard 0100: (M) PAL standard Other values: reserved When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0001: (B, D, G, H, I) PAL standard 0010: (N) PAL standard 0100: (Nc) PAL standard 1000: SECAM standard Other values: reserved
[17:16]	RW	sync_mode_sel	bit[17]: Whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. 0: Only one channel contains sync signals during component output. 1: Three channels contain sync signals during component output. When bit 17 is set to 0, the sync channel must be the Y channel for YPbPr output or G channel for RGB output. bit[16]: Whether there are blanking radixes during RGB output. 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control for the components of three channels. 0: Component sync output is configured based on sync_mode_sel bit[1]. sync_mode_sel bit[1] is bit 17 of sync_mode_sel 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.
[14]	RW	length_sel	Active width of each video line (in pixel). 0: output according to the line active pixel width in BT.601 mode 1: output according to the line active pixel width in BT.470 mode When this bit is set to 0, the active line width is 720 pixels. When this bit is set to 1, the active line width is 704 pixels for the 625-line standard or 712 pixels for the 525-line standard. Currently, the BT.601 mode and BT.470 mode cannot be dynamically switched. You can change the mode only after reset. The BT.601 mode is recommended, and this mode is the default mode after power-on reset.

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[13]	RW	agc_amp_sel	0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on DATE_COEFF1[amp_outside].
[12:9]	RW	luma_dl	Lead or lag-behind offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width. bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luminance signal. 1: The chrominance signal leads the luminance signal. bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001−111: The chrominance signal leads or lags behind the luminance signal by one to seven units.
[8]	RO	reserved	Reserved.
[7:6]	RW	oversam_en	Level-1 over-sampling enable. Both luminance over-sampling and chrominance over-sampling are controlled. bit[7]: luminance over-sampling enable. 0: disabled 1: enabled bit[6]: chrominance over-sampling enable. 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable. 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 over-sampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable. 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable. 0: disabled 1: enabled

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[1]	RW	chgain_en	Chrominance gain enable. 0: disabled 1: enabled
[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data. 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE_COEFF1

DATE_COEFF1 is an amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xF204	DATE_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode				dac_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude.
[28]	RW	cvbs_limit_en	CVBS amplitude limit. 0: not limited 1: limited
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the video programming system (VPS) data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the copy generation management system (CGMS) data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data. 0: from upper bits to lower bits 1: from lower bits to upper bits

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[23]	RW	c_limit_en	Chrominance amplitude limit. 0: not limited 1: limited
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC.
[12]	RW	date_test_en	Test valid signal.
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE_COEFF2

DATE_COEFF2 is a DATE coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF208	DATE_COEFF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef02																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef02	DATE coefficient 2.

DATE_COEFF3

DATE_COEFF3 is a DATE coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF20C	DATE_COEFF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						coef03																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:0]	RW	coef03	DATE coefficient 3.

DATE_COEFF4

DATE_COEFF4 is a DATE coefficient 4 register.

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Offset Address	Register Name	Total Reset Value
0xF210	DATE_COEFF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef04																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:0]	RW	coef04	DATE coefficient 4.

DATE_COEFF5

DATE_COEFF5 is a DATE coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF214	DATE_COEFF5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef05																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:0]	RW	coef05	DATE coefficient 5.

DATE_COEFF6

DATE_COEFF6 is a DATE coefficient 6 register.

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Offset Address	Register Name	Total Reset Value
0xF218	DATE_COEFF6	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef06_0	reserved											coef06_1																			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	coef06_0	DATE coefficient 6 register 0.
[30:23]	RO	reserved	Reserved.
[22:0]	RW	coef06_1	DATE coefficient 6 register 1.

DATE_COEFF21

DATE_COEFF21 is an output matrix control register.

Offset Address	Register Name	Total Reset Value
0xF254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_in_sel			reserved	dac4_in_sel			reserved	dac3_in_sel			reserved	dac2_in_sel			reserved	dac1_in_sel			reserved	dac0_in_sel		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:20]	RW	dac5_in_sel	DAC5 output mode. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[19]	RO	reserved	Reserved.

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[18:16]	RW	dac4_in_sel	DAC4 output mode. 000: 0 001: cvbs 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[15]	RO	reserved	Reserved.
[14:12]	RW	dac3_in_sel	DAC3 output mode. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[11]	RO	reserved	Reserved.
[10:8]	RW	dac2_in_sel	DAC2 output mode. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[7]	RO	reserved	Reserved.
[6:4]	RW	dac1_in_sel	DAC1 output mode. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

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[3]	RO	reserved	Reserved.
[2:0]	RW	dac0_in_sel	DAC0 output mode. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100 R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE_COEFF22

DATE_COEFF22 is a DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xF258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					video_phase_delta										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	video_phase_delta	DTO initial phase.

DATE_COEFF23

DATE_COEFF23 is a video output delay configuration register.

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Offset Address	Register Name	Total Reset Value
0xF25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_out_dly			reserved	dac4_out_dly			reserved	dac3_out_dly			reserved	dac2_out_dly			reserved	dac1_out_dly			reserved	dac0_out_dly		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved.
[22:20]	RW	dac5_out_dly	DAC5 output delay cycle. The unit is 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[19]	RO	reserved	Reserved.
[18:16]	RW	dac4_out_dly	DAC4 output delay cycle. The unit is 54 MHz clock cycle, and the value n indicates n delay cycles.
[15]	RO	reserved	Reserved.
[14:12]	RW	dac3_out_dly	DAC3 output delay cycle. The unit is 54 MHz clock cycle, and the value n indicates n delay cycles.
[11]	RO	reserved	Reserved.
[10:8]	RW	dac2_out_dly	DAC2 output delay cycle. The unit is 54 MHz clock cycle, and the value n indicates n delay cycles.
[7]	RO	reserved	Reserved.
[6:4]	RW	dac1_out_dly	DAC1 output delay cycle. The unit is 54 MHz clock cycle, and the value n indicates n delay cycles.
[3]	RO	reserved	Reserved.
[2:0]	RW	dac0_out_dly	DAC0 output delay cycle. The unit is 54 MHz clock cycle, and the value n indicates n delay cycles.

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DATE_COEFF24

DATE_COEFF24 is a ColorBurst start position register.

Offset Address	Register Name	Total Reset Value
0xF260	DATE_COEFF24	0x0001_2C99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:0]	RW	burst_start	ColorBurst start position.

DATE_COEFF25

DATE_COEFF25 is a SECAM preemphasis curve input coefficient register.

Offset Address	Register Name	Total Reset Value
0xF264	DATE_COEFF25	0x15B5_09C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			x_n_1_coef													reserved			x_n_coef												
Reset	0	0	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	x_n_1_coef	Input coefficient 2 of the SECAM preemphasis curve.
[15:13]	RO	reserved	Reserved.
[12:0]	RW	x_n_coef	Input coefficient 1 of the SECAM preemphasis curve.

DATE_COEFF26

DATE_COEFF26 is a preemphasis curve input coefficient register.

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Offset Address	Register Name	Total Reset Value
0xF268	DATE_COEFF26	0x0000_0945

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				x_n_1_coef											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12:0]	RW	x_n_1_coef	Input coefficient 3 of the SECAM preemphasis curve.

DATE_COEFF27

DATE_COEFF27 is a SECAM preemphasis curve output coefficient register.

Offset Address	Register Name	Total Reset Value
0xF26C	DATE_COEFF27	0x0780_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_n_1_coef												reserved				y_n_coef											
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	y_n_1_coef	Output coefficient 2 of the SECAM preemphasis curve.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	y_n_coef	Output coefficient 1 of the SECAM preemphasis curve.

DATE_COEFF28

DATE_COEFF28 is a SECAM color sync start coordinate register.

Offset Address	Register Name	Total Reset Value
0xF270	DATE_COEFF28	0x06B0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				pixel_begin2												reserved				pixel_begin1											
Reset	0	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.

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[26:16]	RW	pixel_begin2	Start position 2 for SECAM color sync.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	pixel_begin1	Start position 1 for SECAM color sync.

DATE_COEFF29

DATE_COEFF29 is a SECAM color sync end coordinate register.

Offset Address	Register Name	Total Reset Value
0xF274	DATE_COEFF29	0x0000_00A2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pixel_end										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	pixel_end	End position for SECAM color sync.

DATE_COEFF30

DATE_COEFF30 is a SECAM peak video signal level width coefficient register.

Offset Address	Register Name	Total Reset Value
0xF278	DATE_COEFF30	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									g_secam						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6:0]	RW	g_secam	Level width coefficient of the SECAM peak video signal.

DATE_ISRMASK

DATE_ISRMASK is an interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0xF280	DATE_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	tt_mask	Teletext interrupt mask. 0: enabled 1: masked

DATE_ISRSTATE

DATE_ISRSTATE is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0xF284	DATE_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WC	tt_status	Teletext interrupt status. After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears the interrupt.

DATE_ISR

DATE_ISR is an interrupt register.

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Offset Address	Register Name	Total Reset Value
0xF288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	tt_int	Teletext interrupt. It shows the interrupt status after tt_status is masked by tt_mask.

DATE_VERSION

DATE_VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0xF290	DATE_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	reserved	Reserved.

DATE_COEFF37

DATE_COEFF37 is up-sampling filtering coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xF294	DATE_COEFF37	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y1_coeff3								fir_y1_coeff2								fir_y1_coeff1								fir_y1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_y1_coeff3	Coefficient 13 for luminance up-sampling filtering.
[23:16]	RW	fir_y1_coeff2	Coefficient 12 for luminance up-sampling filtering.

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[15:8]	RW	fir_y1_coeff1	Coefficient 11 for luminance up-sampling filtering.
[7:0]	RW	fir_y1_coeff0	Coefficient 10 for luminance up-sampling filtering.

DATE_COEFF38

DATE_COEFF38 is up-sampling filtering coefficient register 2.

Offset Address	Register Name	Total Reset Value
0xF298	DATE_COEFF38	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff1																fir_y2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff1	Coefficient 21 for luminance up-sampling filtering.
[15:0]	RW	fir_y2_coeff0	Coefficient 20 for luminance up-sampling filtering.

DATE_COEFF39

DATE_COEFF39 is up-sampling filtering coefficient register 3.

Offset Address	Register Name	Total Reset Value
0xF29C	DATE_COEFF39	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff3																fir_y2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff3	Coefficient 23 for luminance up-sampling filtering.
[15:0]	RW	fir_y2_coeff2	Coefficient 22 for luminance up-sampling filtering.

DATE_COEFF40

DATE_COEFF40 is up-sampling filtering coefficient register 4.

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Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_c1_coeff3		fir_c1_coeff2		fir_c1_coeff1		fir_c1_coeff0	
Reset	0 0 0 1	1 0 0 1	1 1 1 0	1 1 1 1	0 0 0 0	1 1 0 0	1 1 1 1	1 0 0 1

Bits	Access	Name	Description
[31:24]	RW	fir_c1_coeff3	Coefficient 13 for chrominance up-sampling filtering.
[23:16]	RW	fir_c1_coeff2	Coefficient 12 for chrominance up-sampling filtering.
[15:8]	RW	fir_c1_coeff1	Coefficient 11 for chrominance up-sampling filtering.
[7:0]	RW	fir_c1_coeff0	Coefficient 10 for chrominance up-sampling filtering.

DATE_COEFF41

DATE_COEFF41 is up-sampling filtering coefficient register 5.

Offset Address	Register Name	Total Reset Value
0xF2A4	DATE_COEFF41	0x003A_FFDA

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_c2_coeff1				fir_c2_coeff0			
Reset	0 0 0 0	0 0 0 0	0 0 1 1	1 0 1 0	1 1 1 1	1 1 1 1	1 1 0 1	1 0 1 0

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff1	Coefficient 21 for chrominance up-sampling filtering.
[15:0]	RW	fir_c2_coeff0	Coefficient 20 for chrominance up-sampling filtering.

DATE_COEFF42

DATE_COEFF42 is up-sampling filtering coefficient register 6.

Offset Address	Register Name	Total Reset Value
0xF2A8	DATE_COEFF42	0x0148_FF97

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_c2_coeff3				fir_c2_coeff2			
Reset	0 0 0 0	0 0 0 1	0 1 0 0	1 0 0 0	1 1 1 1	1 1 1 1	1 0 0 1	0 1 1 1

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff3	Coefficient 23 for chrominance up-sampling filtering.

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[15:0]	RW	fir_c2_coeff2	Coefficient 22 for chrominance up-sampling filtering.

DATE_DACDET1

DATE_DACDET1 is DAC automatic detection register 1.

Offset Address	Register Name	Total Reset Value
0xF2C0	DATE_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						det_line										reserved						vdac_det_high									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	det_line	Line of the detected level.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	vdac_det_high	Detected level.

DATE_DACDET2

DATE_DACDET2 is DAC automatic detection register 2.

Offset Address	Register Name	Total Reset Value
0xF2C4	DATE_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved							det_pixel_wid								reserved				det_pixel_sta											
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC automatic detection enable. 0: disabled 1: enabled
[30:27]	RO	reserved	Reserved.
[26:16]	RW	det_pixel_wid	Level width.
[15:11]	RO	reserved	Reserved.

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[10:0]	RW	det_pixel_sta	Start position of a line.

DATE_COEFF50

DATE_COEFF50 is over-sampling filtering coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xF2C8	DATE_COEFF50	0x07FF_07FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 11 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 10 for luminance over-sampling filtering.

DATE_COEFF51

DATE_COEFF51 is over-sampling filtering coefficient register 2.

Offset Address	Register Name	Total Reset Value
0xF2CC	DATE_COEFF51	0x07FF_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 21 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 20 for luminance over-sampling filtering.

DATE_COEFF52

DATE_COEFF52 is over-sampling filtering coefficient register 3.

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Offset Address	Register Name	Total Reset Value
0xF2D0	DATE_COEFF52	0x0000_07FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ovs_coeff1			reserved	ovs_coeff0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 31 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 30 for luminance over-sampling filtering.

DATE_COEFF53

DATE_COEFF53 is over-sampling filtering coefficient register 4.

Offset Address	Register Name	Total Reset Value
0xF2D4	DATE_COEFF53	0x07BF_000C

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ovs_coeff1			reserved	ovs_coeff0		
Reset	0 0 0 0	0 1 1 1	1 0 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 41 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 40 for luminance over-sampling filtering.

DATE_COEFF54

DATE_COEFF54 is over-sampling filtering coefficient register 5.

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Offset Address	Register Name	Total Reset Value
0xF2D8	DATE_COEFF54	0x0135_0135

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ovs_coeff1			reserved	ovs_coeff0		
Reset	0 0 0 0	0 0 0 1	0 0 1 1	0 1 0 1	0 0 0 0	0 0 0 1	0 0 1 1	0 1 0 1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 51 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 50 for luminance over-sampling filtering.

DATE_COEFF55

DATE_COEFF55 is over-sampling filtering coefficient register 6.

Offset Address	Register Name	Total Reset Value
0xF2DC	DATE_COEFF55	0x000C_07BF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ovs_coeff1			reserved	ovs_coeff0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	0 1 1 1	1 0 1 1	1 1 1 1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:16]	RW	ovs_coeff1	Coefficient 61 for luminance over-sampling filtering.
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 60 for luminance over-sampling filtering.

DATE_COEFF56

DATE_COEFF56 is an over-sampling round-off register.

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Offset Address	Register Name	Total Reset Value
0xF2E0	DATE_COEFF56	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															oversam2_round_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	oversam2_round_en	Round-off enable during 2x over-sampling. 0: disabled 1: enabled

DATE_COEFF57

DATE_COEFF57 is a CVBS gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E4	DATE_COEFF57	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cvbs_gain_en	reserved							ycvbs_gain								u_gain								v_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cvbs_gain_en	CVBS gain enable. 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved.
[23:16]	RW	ycvbs_gain	Gain of the luminance component Y.
[15:8]	RW	u_gain	Gain of the chrominance component U.
[7:0]	RW	v_gain	Gain of the chrominance component V.

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DATE_COEFF58

DATE_COEFF58 is a component gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E8	DATE_COEFF58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	comp_gain_en	reserved							ycomp_gain								pb_gain								pr_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	comp_gain_en	Component gain enable. 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved.
[23:16]	RW	ycomp_gain	Gain of the luminance component Y.
[15:8]	RW	pb_gain	Gain of the chrominance component U.
[7:0]	RW	pr_gain	Gain of the chrominance component V.

DATE_COEFF59

DATE_COEFF59 is a clip control register.

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Offset Address	Register Name	Total Reset Value
0xF2EC	DATE_COEFF59	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															cb_gain_polar	reserved		cr_os_clip_fullrange	cb_os_clip_fullrange	reserved		v_os_clip_fullrange	u_os_clip_fullrange	reserved				y_os_clip_fullrange	reserved		clpf_clip_fullrange	ynotch_clip_fullrange
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RW	cb_gain_polar	Chrominance subcarrier polarity.
[15:14]	RO	reserved	Reserved.
[13]	RW	cr_os_clip_fullrange	Cr component clip enable on the up-sampling module. 0: disabled 1: enabled
[12]	RW	cb_os_clip_fullrange	Cb component clip enable on the up-sampling module. 0: disabled 1: enabled
[11:10]	RO	reserved	Reserved.
[9]	RW	v_os_clip_fullrange	V component clip enable on the up-sampling module. 0: disabled 1: enabled
[8]	RW	u_os_clip_fullrange	U component clip enable on the up-sampling module. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.
[4]	RW	y_os_clip_fullrange	Y component clip enable on the up-sampling module. 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved.
[1]	RW	clpf_clip_fullrange	Chrominance low-pass module clip enable. 0: disabled 1: enabled

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[0]	RW	ynotch_clip_fullrange	Luminance notch module clip enable. 0: disabled 1: enabled

DATE_COEFF61

DATE_COEFF61 is a timing global control register.

Offset Address	Register Name	Total Reset Value
0xF2F4	DATE_COEFF61	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											rgb_acrive_ovrd	pal_half_ovrd	cb_bound_ovrd	burst_dura_ovrd	burst_start_ovrd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	rgb_acrive_ovrd	Global control for the RGB active region coefficient configuration register. 0: The configured RGB active region does not take effect. 1: The configured RGB active region takes effect.
[3]	RW	pal_half_ovrd	Global control for the PAL half-line coefficient configuration register. 0: The configured PAL half line does not take effect. 1: The configured PAL half line takes effect.
[2]	RW	cb_bound_ovrd	Global control for the chrominance subcarrier boundary coefficient configuration register. 0: The configured chrominance subcarrier boundary does not take effect. 1: The configured chrominance subcarrier boundary takes effect.
[1]	RW	burst_dura_ovrd	Global control for the chrominance carrier duration coefficient configuration register. 0: The configured chrominance carrier duration does not take effect. 1: The configured chrominance carrier duration takes effect.

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[0]	RW	burst_start_ovrd	Global control for the chrominance carrier start position coefficient configuration register. 0: The configured chrominance carrier start position does not take effect. 1: The configured chrominance carrier start position takes effect.

DATE_COEFF62

DATE_COEFF62 is a chrominance subcarrier duration control register.

Offset Address	Register Name	Total Reset Value
0xF2F8	DATE_COEFF62	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_dura_coeff																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	burst_dura_coeff	Chrominance carrier duration.

DATE_COEFF63

DATE_COEFF63 is a chrominance subcarrier boundary control register.

Offset Address	Register Name	Total Reset Value
0xF2FC	DATE_COEFF63	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cb_bound_coeff																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cb_bound_coeff	Chrominance subcarrier boundary.

DATE_COEFF64

DATE_COEFF64 is a PAL half-line control register.

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Offset Address	Register Name	Total Reset Value
0xF300	DATE_COEFF64	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pal_half_coeff																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	pal_half_coeff	PAL half line.

DATE_COEFF65

DATE_COEFF65 is an RGB active region control register.

Offset Address	Register Name	Total Reset Value
0xF304	DATE_COEFF65	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgb_active_coeff																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rgb_active_coeff	RGB active region.

DATE_COEFF66

DATE_COEFF66 is a sync timing global control register.

Offset Address	Register Name	Total Reset Value
0xF308	DATE_COEFF66	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												wid_act_ovrd	wid_hfb_ovrd	wid_sync_ovrd	htotal_ovrd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

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[3]	RW	wid_act_ovrd	Timing global control. 0: The configured timing active region does not take effect. 1: The configured timing active region takes effect.
[2]	RW	wid_hfb_ovrd	Timing global control. 0: The HFB configuration does not take effect. 1: The HFB configuration takes effect.
[1]	RW	wid_sync_ovrd	Timing global control. 0: The configured sync header width does not take effect. 1: The configured sync header width takes effect.
[0]	RW	htotal_ovrd	Timing global control. 0: The configured total line point number does not take effect. 1: The configured total line point number takes effect.

DATE_COEFF67

DATE_COEFF67 is a line point quantity configuration register.

Offset Address	Register Name	Total Reset Value
0xF30C	DATE_COEFF67	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				htotal_sw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	htotal_sw	Total number of line points.

DATE_COEFF68

DATE_COEFF68 is a sync width configuration register.

Offset Address	Register Name	Total Reset Value
0xF310	DATE_COEFF68	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wid_sync_sw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:0]	RW	wid_sync_sw	Sync width.

DATE_COEFF69

DATE_COEFF69 is an HFB configuration register.

Offset Address	Register Name	Total Reset Value
0xF314	DATE_COEFF69	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wid_hfb_sw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	wid_hfb_sw	HFB.

DATE_COEFF70

DATE_COEFF70 is a line active configuration register.

Offset Address	Register Name	Total Reset Value
0xF318	DATE_COEFF70	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wid_act_sw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	wid_act_sw	Line active region.

DATE_COEFF71

DATE_COEFF71 is a phase shift global control register.

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Offset Address	Register Name	Total Reset Value
0xF31C	DATE_COEFF71	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															phase_shift_ovrd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	phase_shift_ovrd	Phase shift global control. 0: The phase shift register does not take effect. 1: The phase shift register takes effect.

DATE_COEFF72

DATE_COEFF72 is a phase shift register.

Offset Address	Register Name	Total Reset Value
0xF320	DATE_COEFF72	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phase_shift_coeff																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	phase_shift_coeff	Phase shift.

DATE_COEFF73

DATE_COEFF73 is a luminance notch coefficient global control register.

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Offset Address	Register Name	Total Reset Value
0xF324	DATE_COEFF73	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															coef_notch_ovrd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	coef_notch_ovrd	Luminance notch coefficient validate.

DATE_COEFF74

DATE_COEFF74 is luminance notch coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xF328	DATE_COEFF74	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						coef_notch_2										reserved						coef_notch_1									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_2	Luminance notch coefficient 2.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_1	Luminance notch coefficient 1.

DATE_COEFF75

DATE_COEFF75 is luminance notch coefficient register 2.

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Offset Address	Register Name	Total Reset Value
0xF32C	DATE_COEFF75	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	coef_notch_4			reserved	coef_notch_3		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_4	Luminance notch coefficient 4.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_3	Luminance notch coefficient 3.

DATE_COEFF76

DATE_COEFF76 is luminance notch coefficient register 3.

Offset Address	Register Name	Total Reset Value
0xF330	DATE_COEFF76	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	coef_notch_6			reserved	coef_notch_5		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_6	Luminance notch coefficient 6.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_5	Luminance notch coefficient 5.

DATE_COEFF77

DATE_COEFF77 is luminance notch coefficient register 4.

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Offset Address	Register Name	Total Reset Value
0xF334	DATE_COEFF77	0x0000_0000

Bit	31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved		coef_notch_8			reserved		coef_notch_7		
Reset	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_8	Luminance notch coefficient 8.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_7	Luminance notch coefficient 7.

DATE_COEFF78

DATE_COEFF78 is luminance notch coefficient register 5.

Offset Address	Register Name	Total Reset Value
0xF338	DATE_COEFF78	0x0000_0000

Bit	31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	reserved		coef_notch_10			reserved		coef_notch_9		
Reset	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_10	Luminance notch coefficient 10.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_9	Luminance notch coefficient 9.

DATE_COEFF79

DATE_COEFF79 is luminance notch coefficient register 6.

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Offset Address	Register Name	Total Reset Value
0xF33C	DATE_COEFF79	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	coef_notch_12			reserved	coef_notch_11		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	coef_notch_12	Luminance notch coefficient 12.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	coef_notch_11	Luminance notch coefficient 11.

DATE_COEFF80

DATE_COEFF80 is a chrominance low-pass coefficient global control register.

Offset Address	Register Name	Total Reset Value
0xF340	DATE_COEFF80	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								coef_chra_lpf_ovrd
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	coef_chra_lpf_ovrd	Chrominance low-pass coefficient global control. 0: The chrominance low-pass coefficient does not take effect. 1: The chrominance low-pass coefficient takes effect.

DATE_COEFF81

DATE_COEFF81 is chrominance low-pass coefficient register 1.

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Offset Address	Register Name	Total Reset Value
0xF344	DATE_COEFF81	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		coef_chra_lpf_2		reserved		coef_chra_lpf_1	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24:16]	RW	coef_chra_lpf_2	Chrominance low-pass coefficient 2.
[15:9]	RO	reserved	Reserved.
[8:0]	RW	coef_chra_lpf_1	Chrominance low-pass coefficient 1.

DATE_COEFF82

DATE_COEFF82 is chrominance low-pass coefficient register 2.

Offset Address	Register Name	Total Reset Value
0xF348	DATE_COEFF82	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		coef_chra_lpf_4		reserved		coef_chra_lpf_3	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24:16]	RW	coef_chra_lpf_4	Chrominance low-pass coefficient 4.
[15:9]	RO	reserved	Reserved.
[8:0]	RW	coef_chra_lpf_3	Chrominance low-pass coefficient 3.

DATE_COEFF83

DATE_COEFF83 is chrominance low-pass coefficient register 3.

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Offset Address	Register Name	Total Reset Value
0xF34C	DATE_COEFF83	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		coef_chra_lpf_6		reserved		coef_chra_lpf_5	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24:16]	RW	coef_chra_lpf_6	Chrominance low-pass coefficient 6.
[15:9]	RO	reserved	Reserved.
[8:0]	RW	coef_chra_lpf_5	Chrominance low-pass coefficient 5.

DATE_COEFF84

DATE_COEFF84 is chrominance low-pass coefficient register 4.

Offset Address	Register Name	Total Reset Value
0xF350	DATE_COEFF84	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						coef_chra_lpf_7	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8:0]	RW	coef_chra_lpf_7	Chrominance low-pass coefficient 7.

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10.3 MIPI RX

10.3.1 Overview

The mobile industry processor interface receiver (MIPI RX) receives low-voltage differential signals (LVDSs) that carry raw video data (Bayer RGB data), converts the serial differential signals into the digital camera (DC) timing, and transfers it to the downstream video capture (VICAP) module.

The MIPI RX supports serial video signal inputs such as the MIPI D-PHY, LVDS, and high-speed serial pixel interface (HiSPI). The serial video interfaces provide more bandwidth to enhance transmission stability. The MIPI RX is also compatible with the DC video interface, supports the 3.3 V/1.8 V DC parallel input, and requires a less number of chip pins while providing better compatibility.

The MIPI RX consists of the combo-PHY and controller. Figure 10-18 shows the MIPI RX workflow and its position in the system.

Figure 10-18 MIPI RX workflow and its position in the system

10.3.2 Features

The MIPI RX has the following features:

- 1/2/4-lane MIPI D-PHY interface, up to 1 Gbit/s per lane
- 1/2/4/6/8-lane LVDS. sub-LVDS, or HiSPI interface, up to 1 Gbit/s per lane
- CMOS parallel 1.8 V/3.3 V input
- RAW10, RAW12, or RAW14 data type parsing
- 2-frame WDR
- Endian mode configuration for LVDS or HiSPI mode pixel or synchronization code
- Configuration of channel quantity and sequence

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10.3.3 Function Description

10.3.3.1 Typical Applications

The MIPI RX is a collection unit that supports multiple differential video input interfaces. It uses the combo-PHY to receive data through the MIPI, LVDS, sub-LVDS, HiSPI, or DC interface. Depending on the functional mode configuration, the MIPI RX allows data transmission at different speeds and resolutions and supports multiple external input devices.

The MIPI RX supports a maximum of one link with four lanes for MIPI input and a maximum of one link with four lanes or two links with eight lanes for LVDS input. The input pins can be multiplexed to provide single-end DC or BT.1120 channel input, thereby providing better compatibility with less chip pins.

Table 10-7 lists the interfaces supported by the MIPI RX.

Table 10-7 Interfaces supported by the MIPI RX

Interface Type	Common Mode Voltage	Differential Mode Voltage	Maximum Clock Frequency	Maximum Data Rate per Lane
D-PHY	200 mV	200 mV	500 MHz	1 Gbit/s
Sub-LVDS	900 mV	150 mV	500 MHz	1 Gbit/s
LVDS	1.25 V	350 mV	500 MHz	1 Gbit/s
HiSPI (HiVCM)	900 mV	280 mV	500 MHz	1 Gbit/s
HiSPI (SLVS)	200 mV	200 mV	500 MHz	1 Gbit/s
CMOS Parallel	1.8 V	1.8 V	150 MHz	150 Mbit/s
CMOS Parallel	3.3 V	3.3 V	150 MHz	150 Mbit/s

The MIPI RX supports the following typical input modes:

- 1080p (1920 x 1080) @30 fps
- 1080p (1920 x 1080) @60 fps
- 3M (2048 x 1536) @30 fps
- 5M (2592 x 1944) @30 fps

10.3.3.2 Function Implementation

MIPI Video Data Input

MIPI specifications are developed and maintained by different working groups and cover diverse application requirements for use in different fields. The MIPI RX supports the D-PHY and CSI-2. D-PHY stipulates the rules of transmission at the physical layer, and CSI-2 stipulates the format and protocol of camera output data packets.

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(1) D-PHY

D-PHY is a high-speed physical layer standard released by the MIPI Alliance. The standard stipulates the physical specifications and transmission protocols at the physical layer for hosts and peripherals. D-PHY uses the LVDS technology with 200 mV source synchronization, and each channel has a frequency from 80 MHz to 1 GHz. Typically, each clock supports a maximum of four data channels, which provide a total transmission rate of 4 Gbit/s. D-PHY can work either in low-power (LP) or high-speed (HS) mode.

(2) CSI-2

CSI-2 is a camera data protocol that stipulates the data packet format used for communication between hosts and peripherals.

CSI-2 supports image application in different pixel formats, and the smallest unit for data transmission is byte. An appropriate number of data channels can be selected to attain enhanced CSI-2 performance. CSI-2 specifies how the TX end packetizes pixel data into bytes and how multiple data channels are allocated and managed. Byte data is organized in data packets, which are transmitted between the start of transmission (SoT) and the end of transmission (EoT). The RX end parses the data packets based on the applicable protocol and restores the pixel data.

The MIPI RX can parse pixel data in RAW10, RAW12, or RAW14 format.

CSI-2 data packets can be long or short and contain parity codes for parity check and error correction.

Both long and short packets are transmitted between the SoT and EoT. D-PHY works in LP mode in gaps of data transmission. Figure 10-19 shows the mechanism for transmitting CSI-2 data packets. PH and PF mean packet header and packet footer, respectively.

Figure 10-19 CSI-2 data packet transmission mechanism

Long packets are used to transmit effective pixel data in five parts: Data ID, Word Count, ECC, Payload, and Checksum.

Data ID comprises Virtual Channel and Data Type. Virtual Channel controls the channel used for transmission and can specify channel multiplexing so that different channels will transmit different data. Data Type specifies the type of data.

Word Count indicates the amount of data to be received by the RX end.

ECC is 8-bit error correction code that can be used to detect and correct errors in Data Type and Word Count.

Payload is the pixel data to be transmitted.

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Checksum is generated by a linear feedback shift register and is used to check payload data.

Figure 10-20 shows the format of a long packet.

Figure 10-20 CSI-2 long packet format

Short packets are used to transmit synchronization information in three parts: Data ID, Word Count, and ECC. Figure 10-21 shows its format.

Figure 10-21 CSI-2 short packet format

LVDS Video Data Input

The LVDS is widely used in front-end cameras. It identifies data of the blanking region and active region by synchronization code.

The MIPI RX controller receives parallel data from the HiSPI, PHY, splits and combines the data, and extracts the synchronization code to obtain the pixel data.

In LVDS transmission mode, frame or line synchronization signals are integrated into data streams. In data streams, SOF and EOF indicate the start and end of a frame, whereas SOL and EOL indicate the start and end of a line. In a data stream, each of SOF, EOF, SOL, and EOL consists of four fields, and the bit width and pixel data of each field are consistent. The first three fields are fixed reference codes, and the fourth field is used to identify the start of end of a frame or line. Table 10-8 illustrates the LVDS synchronization code format.

Table 10-8 LVDS synchronization code format

Field	Bit Width	Sync Code			
		SOL/SAV (Valid Line)	EOL/EAV (Valid Line)	SOF/SAV (Invalid Line)	EOF/EAV (Invalid Line)
1st	10-bit	3FFh	3FFh	3FFh	3FFh

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Field	Bit Width	Sync Code			
		SOL/SAV (Valid Line)	EOL/EAV (Valid Line)	SOF/SAV (Invalid Line)	EOF/EAV (Invalid Line)
code	12-bit	FFFh	FFFh	FFFh	FFFh
	14-bit	3FFFh	3FFFh	3FFFh	3FFFh
2nd code	10-bit	000h	000h	000h	000h
	12-bit	000h	000h	000h	000h
	14-bit	0000h	0000h	0000h	0000h
3rd code	10-bit	000h	000h	000h	000h
	12-bit	000h	000h	000h	000h
	14-bit	0000h	0000h	0000h	0000h
4th code	10-bit	XXXh	XXXh	XXXh	XXXh
	12-bit	XXXh	XXXh	XXXh	XXXh
	14-bit	XXXXh	XXXXh	XXXXh	XXXXh

NOTE

The first three fields of the synchronization code are fixed, and the fourth field identifies the start or end of a frame or line. The value of the fourth field is specified by image sensor vendors and therefore it varies according to vendors. Table 10-9 describes an implementation mode. Table 10-9describes an implementation mode.

Table 10-9 Sample of the fourth field of the LVDS synchronization code

Field	Bit Width	Sync code			
		SAV(Valid line)	EAV(Valid line)	SAV(Invalid line)	EAV(Invalid line)
4th code	10bit	200h	274h	2ACh	2D8h
	12bit	800h	9D0h	AB0h	B60h
	14bit	2000h	2740h	2AC0h	2D80h

Figure 10-22 shows how LVDS synchronization information and pixel data are transmitted on each channel. H indicates the synchronization code, and P indicates pixel. The bit widths of H and P are consistent with that of a single output pixel of the image sensor.On each data channel, the synchronization code with four-pixel bit width is transmitted before pixel data. The distribution of pixel data is related to the number of channels. Data is transmitted in series, and the endian mode is configurable in the MIPI RX.

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Figure 10-22 LVDS data transmission mode

Two LVDS synchronization modes are available. In one mode, SAV (Invalid) and EAV (Invalid) identify invalid data of the blanking region whereas SAV (Valid) and EAV (Valid) identify pixel data of the active region. Figure 10-23 shows this synchronization mode.

Figure 10-23 LVDS synchronization mode 1

In the other mode, SOF identifies the start of the first line in the active region, EOF identifies the end of the last line in the active region, and SOL and EOL identify the start and end of the other lines in the active region. Figure 10-24 shows this synchronization mode.

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Figure 10-24 LVDS synchronization mode 2

<table>
<tr><td colspan="5">V.BLK</td></tr>
<tr><td>H.BLK</td><td>SOF</td><td>Effective Pixel</td><td rowspan="12">EOL</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td rowspan="11">SOL</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective Pixel</td><td>EOF</td><td>H.BLK</td></tr>
<tr><td colspan="5">V.BLK</td></tr>
</table>

The sub-LVDS is a differential signal technology with ultra-low voltage swing, whose common or differential mode voltage is lower than the LVDS. The sub-LVDS uses the same format for data transmission as the LVDS and can be considered as one type of LVDS.

HiSPI Video Data Input

HiSPI, formulated by Aptina, includes the HiSPI physical layer protocol and HiSPI specification. The HiSPI physical layer protocol stipulates the electrical specifications and timing parameters, whereas the HiSPI specification defines the data packetizing modes.

The HiSPI specification stipulates two physical layer electric standards (HiVCM and SLVS) and four data transmission modes (Packetized-SP, Streaming-SP, Streaming-S, and ActiveStart-SP8). The Packetized-SP mode is similar to the LVDS in data packetizing mode, except that the checksum (CRC) and filler code (FLR) can be added to data packets in Packetized-SP mode. Figure 10-25 shows the data format in HiSPI Packetized-SP mode.

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Figure 10-25 HiSPI Packetized-SP data format

<table>
<tr><td>SOF</td><td rowspan="13">FLR</td><td>Effective pixel</td><td rowspan="12">EOL</td><td rowspan="13">CRC</td><td rowspan="13">H.BLK</td></tr>
<tr><td rowspan="12">SOL</td><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>⋮</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td></tr>
<tr><td>Effective pixel</td><td>EOF</td></tr>
<tr><td colspan="6">V.BLK</td></tr>
</table>

The MIPI RX supports the HiVCM and SLVS electric standards and supports the Packetized-SP mode (does not process the CRC and FLR data), meaning that the MIPI RX parses data in the same way for the HiSPI and LVDS.

WDR Video Data Input

For video data input through the MIPI, a virtual channel (VC) identifies data streams of different exposure length. The VC is 2-bit wide and supports interleaved data transmission of a maximum of four-frame wide dynamic range (WDR) data. The MIPI RX parses the VC information in a data packet and outputs the VC information with DC timing to the VICAP, where demultiplexing is implemented.

For video data input through the LVDS and HiSPI, the fourth field in a synchronization code is used to identify data of different exposure lengths. The MIPI RX compares the received synchronization code with the preset value in a register to identify data of different exposure lengths. The MIPI RX uses the VC to identify data streams of different exposure lengths and sends them to the VICAP, where demultiplexing is implemented.

10.3.4 Operating Mode of the MIPI RX Controller

The MIPI RX controller supports the MIPI, LVDS, and HiSPI modes. The software configuration in each mode contains two parts: controller and PHY. All register configurations simultaneously take effect when MIPI_START has been set to 1.

10.3.4.1 MIPI Mode Configuration Process

In MIPI mode, configure the channel quantity, data type, and WDR mode for data transmission. Frame or line synchronization information in MIPI mode is included in a short packet. The controller parses the short packet and restores the pixel data. Figure 10-26 shows the software configuration process in MIPI mode.

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Figure 10-26 MIPI RX configuration process in MIPI mode

10.3.4.2 LVDS and HiSPI Mode Configuration Process

In LVDS mode, configure the type of raw data, endian mode, synchronization mode, WDR mode, and image size registers. In LVDS mode, a synchronization code is used to identify frame or line synchronization information. Depending on the type of raw data, the synchronization code can be 10, 12, or 14 bits. Configuration methods are the same for HiSPI and LVDS modes.

Figure 10-27 shows the software configuration process in LVDS and HiSPI modes.

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Figure 10-27 MIPI RX configuration process in LVDS and HiSPI modes

10.3.5 MIPI RX Register Summary

Table 10-10 describes the MIPI RX registers.

Table 10-10 Summary of MIPI RX registers (base address: 0x2068_0000)

Offset Address	Register	Description	Page
0x0000	MIPI_START	MIPI configuration enable register	10-281
0x0004	MIPI_CTRL_MODE	MIPI controller configuration register	10-282
0x000C	LVDS_IMGSIZE	MIPI image size register	10-283
0x0010	LVDS_WDR_MODE	Sensor WDR mode configuration register	10-283
0x0014	LVDS_CTRL_MODE	LVDS operating mode configuration register	10-284
0x1000	INT_STAT_LINK0	Link 0 interrupt status register	10-285

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Offset Address	Register	Description	Page
0x1004	INT_MASK_LINK0	Link 0 interrupt mask register	10-288
0x1008	INT_RAW_LINK0	Link 0 raw interrupt status register	10-289
0x100C	INT_CLR_LINK0	Link 0 interrupt clear register	10-291
0x1010	LANE_EN_LINK0	Link 0 lane enable configuration register	10-293
0x1014	LANE_ID_LINK0	Link 0 lane priority configuration register	10-294
0x1024	PHY_EN_LINK0	Link 0 PHY channel enable register	10-294
0x1028	PHY_CFG_LINK0	Link 0 PHY mode configuration register	10-296
0x1030	MIPI_LANES_NUM	MIPI data channel quantity register	10-297
0x1034	MIPI_RSTN	MIPI controller reset control register	10-298
0x1038	MIPI_DI_1	MIPI controller data ID 1 register	10-298
0x103C	MIPI_DI_2	MIPI controller data ID 2 register	10-299
0x1040	MIPI_INTR1_RAW	MIPI raw interrupt 1 register	10-300
0x1044	MIPI_INTR2_RAW	MIPI raw interrupt 2 register	10-302
0x1048	MIPI_INTR1_MASK	MIPI interrupt 1 mask register	10-303
0x104C	MIPI_INTR2_MASK	MIPI interrupt 2 mask register	10-306
0x1060	MIPI_TIMEOUT	Link 0 MIPI timeout register	10-308
0x1064	MIPI_FSM_PARAM	Link 0 MIPI time parameter register	10-309
0x1068	MIPI_FSM_CKEN	MIPI FSM clock gating register	10-310
0x1080	LINK0_LANE0_SOF_01	SOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-311
0x1088	LINK0_LANE0_EOF_01	EOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-311
0x1090	LINK0_LANE0_SOL_01	SOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.	10-312
0x1098	LINK0_LANE0_EOL_01	EOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-312
0x10A0	LINK0_LANE1_SOF_01	SOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-313
0x10A8	LINK0_LANE1_EOF_01	EOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-313
0x10B0	LINK0_LANE1_SOL_01	SOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.	10-314

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Offset Address	Register	Description	Page
0x10B8	LINK0_LANE1_EOL_01	EOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-314
0x10C0	LINK0_LANE2_SOF_01	SOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-315
0x10C8	LINK0_LANE2_EOF_01	EOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-315
0x10D0	LINK0_LANE2_SOL_01	SOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.	10-316
0x10D8	LINK0_LANE2_EOL_01	EOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-316
0x10E0	LINK0_LANE3_SOF_01	SOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-317
0x10E8	LINK0_LANE3_EOF_01	EOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-317
0x10F0	LINK0_LANE3_SOL_01	SOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.	10-318
0x10F8	LINK0_LANE3_EOL_01	EOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-318
0x1400	INT_STAT_LINK1	Link 1 interrupt status register	10-319
0x1404	INT_MASK_LINK1	Link 1 interrupt mask register	10-320
0x1408	INT_RAW_LINK1	Link 1 raw interrupt status register	10-321
0x140C	INT_CLR_LINK1	Link 1 interrupt clear register	10-322
0x1410	LANE_EN_LINK1	Link 1 lane enable configuration register	10-323
0x1414	LANE_ID_LINK1	Link 1 lane priority configuration register	10-324
0x1424	PHY_EN_LINK1	Link 1 PHY channel enable register	10-325
0x1428	PHY_CFG_LINK1	Link 1 PHY mode configuration register	10-326
0x1480	LINK1_LANE0_SOF_01	SOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-327
0x1488	LINK1_LANE0_EOF_01	EOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-328
0x1490	LINK1_LANE0_SOL_01	SOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.	10-328
0x1498	LINK1_LANE0_EOL_01	EOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode	10-329
0x14A0	LINK1_LANE1_SOF_01	SOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-329

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Offset Address	Register	Description	Page
0x14A8	LINK1_LANE1_EOF_01	EOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-330
0x14B0	LINK1_LANE1_SOL_01	SOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.	10-330
0x14B8	LINK1_LANE1_EOL_01	EOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode	10-331
0x14C0	LINK1_LANE2_SOF_01	SOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-331
0x14C8	LINK1_LANE2_EOF_01	EOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-332
0x14D0	LINK1_LANE2_SOL_01	SOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.	10-332
0x14D8	LINK1_LANE2_EOL_01	EOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode	10-333
0x14E0	LINK1_LANE3_SOF_01	SOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-333
0x14E8	LINK1_LANE3_EOF_01	EOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-334
0x14F0	LINK1_LANE3_SOL_01	SOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.	10-334
0x14F8	LINK1_LANE3_EOL_01	EOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode	10-335

10.3.6 MIPI RX Register Description

MIPI_START

MIPI_START is an MIPI configuration enable register.

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Offset Address	Register Name	Total Reset Value
0x0000	MIPI_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mipi_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	mipi_start	Configuration enable. 0: disabled 1: enabled the APB clock domain configuration signal and convert it into the MIPI working clock domain output.

MIPI_CTRL_MODE

MIPI_CTRL_MODE is an MIPI controller configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	MIPI_CTRL_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mipi_mem_ck_gt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	mipi_mem_ck_gt	MIPI memory clock gating enable. 0: disabled 1: enabled

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LVDS_IMGSIZE

LVDS_IMGSIZE is an MIPI image size register.

Offset Address	Register Name	Total Reset Value
0x000C	LVDS_IMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				lvds_imgheight												reserved				lvds_imgwidth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	lvds_imgheight	Image height. The value is the actual image height minus 1, and the value range is [0, 8191].
[15:13]	RO	reserved	Reserved.
[12:0]	RW	lvds_imgwidth	Image width. The value is the actual image width minus 1, and the value range is [0, 8191].

LVDS_WDR_MODE

LVDS_WDR_MODE is a sensor WDR mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	LVDS_WDR_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wdr_mode	reserved		lvds_wdr_num		reserved			lvds_wdr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.

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[8]	RO	wdr_mode	WDR mode configuration. This signal is valid only if lvds_wdr_en is enabled and lvds_sync_mode is set to 1. 0: normal WDR mode 1: SONY DOL WDR mode. For images of the same exposure length, the current frame has a different synchronization code from the next frame.
[7:6]	RO	reserved	Reserved.
[5:4]	RW	lvds_wdr_num	WDR mode configuration. 01: two-frame WDR Other: reserved
[3:1]	RO	reserved	Reserved.
[0]	RW	lvds_wdr_en	WDR enable. 0: linear mode 1: WDR mode

LVDS_CTRL_MODE

LVDS_CTRL_MODE is an LVDS operating mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	LVDS_CTRL_MODE	0x0000_0310

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			lvds_link_seq	reserved		lvds_code_big_endian	lvds_pix_big_endian	reserved		lvds_raw_type		reserved			lvds_sync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	RW	lvds_link_seq	Sequence of two links in LVDS mode. 0: synchronous transmission mode for two links of the normal sensor 1: asynchronous transmission mode for two links of the Panasonic sensor
[11:10]	RW	reserved	Reserved.

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[9]	RW	lvds_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of raw data to be transmitted in LVDS or HiSPI mode. 0: LSB. Least significant bits are transmitted first. Use RAW12 as an example. The serial data sequence of the synchronization code (sync_code) received is bit 0, bit 1, …, bit 11. 1: MSB. Most significant bits are transmitted first. Use RAW12 as an example. The serial data sequence of the synchronization code (sync_code) received is bit 11, bit 10, …, bit 0.
[8]	RW	lvds_pix_big_endian	Serial bit transmission sequence for the valid pixels of raw data to be transmitted in LVDS or HiSPI mode. 0: LSB. Least significant bits are transmitted first. Use RAW12 as an example. The serial data sequence of the valid pixels received is bit 0, bit 1, …, bit 11. 1: MSB. Most significant bits are transmitted first. Use RAW12 as an example. The serial data sequence of the valid pixels received is bit 11, bit 10, …, bit 0.
[7:6]	RO	reserved	Reserved.
[5:4]	RW	lvds_raw_type	Type of raw data to be transmitted in LVDS or HiSPI mode. 00: reserved 01: raw 10 bit 10: raw 12 bits 11: raw 14 bits
[3:1]	RO	reserved	Reserved.
[0]	RW	lvds_sync_mode	Frame or line synchronization mode in LVDS mode. 0: SOF, EOF, SOL, or EOL mode 1: SAV-EAV mode SAV-EAV mode is widely applied in SONY/OmniVision sensors. In this mode, set InValid SAV/EAV in LINKm_LANEn_SOF_xx or LINKm_LANEn_EOF_xx, and set Valid SAV/EAV in LINKm_LANEn_SOL_xx or LINKm_LANEn_SOL_xx. Here, *m* is 0 or 1, and *n* is 0, 1, 2, or 3. In HiSPI mode, this field must be set to 0.

INT_STAT_LINK0

INT_STAT_LINK0 is a link 0 interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x1000	INT_STAT_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_stat	hsync_err_stat	lane3_sync_err_stat	lane2_sync_err_stat	lane1_sync_err_stat	lane0_sync_err_stat	reserved			timeout_d3_stat	timeout_d2_stat	timeout_d1_stat	timeout_d0_stat	timeout_ck_stat	reserved			escape_d3_stat	escape_d2_stat	escape_d1_stat	escape_d0_stat	escape_ck_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RO	vsync_err_stat	SOF or EOF signal async interrupt status for each lane on link 0. 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RO	hsync_err_stat	SOL or EOL signal async interrupt status for each lane on link 0. 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RO	lane3_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 3 on link 0 in LVDS mode. 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	lane2_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 2 on link 0 in LVDS mode. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	lane1_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 1 on link 0 in LVDS mode. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	lane0_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 0 on link 0 in LVDS mode. 0: No interrupt is generated. 1: An interrupt is generated.
[15:13]	RO	reserved	Reserved.
[12]	RO	timeout_d3_stat	FSM timeout interrupt status for data lane 3 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.

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[11]	RO	timeout_d2_stat	FSM timeout interrupt status for data lane 2 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	timeout_d1_stat	FSM timeout interrupt status for data lane 1 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	timeout_d0_stat	FSM timeout interrupt status for data lane 0 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	timeout_ck_stat	FSM timeout interrupt status for the clock lane on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[7:5]	RO	reserved	Reserved.
[4]	RO	escape_d3_stat	Escape sequence interrupt status for data lane 3 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	escape_d2_stat	Escape sequence interrupt status for data lane 2 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	escape_d1_stat	Escape sequence interrupt status for data lane 1 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	escape_d0_stat	Escape sequence interrupt status for data lane 0 on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	escape_ck_stat	Escape sequence interrupt status for the clock lane on link 0 in MIPI mode. 0: No interrupt is generated. 1: An interrupt is generated.

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INT_MASK_LINK0

INT_MASK_LINK0 is a link 0 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1004	INT_MASK_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_mask	hsync_err_mask	lane3_sync_err_mask	lane2_sync_err_mask	lane1_sync_err_mask	lane0_sync_err_mask	reserved			timeout_d3_mask	timeout_d2_mask	timeout_d1_mask	timeout_d0_mask	timeout_ck_mask	reserved			escape_d3_mask	escape_d2_mask	escape_d1_mask	escape_d0_mask	escape_ck_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	vsync_err_mask	SOF or EOF signal async interrupt mask for each lane on link 0. 0: not masked 1: masked
[20]	RW	hsync_err_mask	SOL or EOL signal async interrupt mask for each lane on link 0. 0: not masked 1: masked
[19]	RW	lane3_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 3 on link 0. 0: not masked 1: masked
[18]	RW	lane2_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 2 on link 0. 0: not masked 1: masked
[17]	RW	lane1_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 1 on link 0. 0: not masked 1: masked
[16]	RW	lane0_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 0 on link 0. 0: not masked 1: masked
[15:13]	RO	reserved	Reserved.

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[12]	RW	timeout_d3_mask	FSM timeout interrupt mask for data lane 3 on link 0. 0: not masked 1: masked
[11]	RW	timeout_d2_mask	FSM timeout interrupt mask for data lane 2 on link 0. 0: not masked 1: masked
[10]	RW	timeout_d1_mask	FSM timeout interrupt mash for data lane 1 on link 0. 0: not masked 1: masked
[9]	RW	timeout_d0_mask	FSM timeout interrupt mask for data lane 0 on link 0. 0: not masked 1: masked
[8]	RW	timeout_ck_mask	FSM timeout interrupt mask for the clock lane on link 0. 0: not masked 1: masked
[7:5]	RO	reserved	Reserved.
[4]	RW	escape_d3_mask	Escape interrupt mask for data lane 3 on link 0. 0: not masked 1: masked
[3]	RW	escape_d2_mask	Escape interrupt mask for data lane 2 on link 0. 0: not masked 1: masked
[2]	RW	escape_d1_mask	Escape interrupt mask for data lane 1 on link 0. 0: not masked 1: masked
[1]	RW	escape_d0_mask	Escape interrupt mask for data lane 0 on link 0. 0: not masked 1: masked
[0]	RW	escape_ck_mask	Escape interrupt mask for the clock lane on link 0. 0: not masked 1: masked

INT_RAW_LINK0

INT_RAW_LINK0 is a link 0 raw interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x1008	INT_RAW_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_raw	hsync_err_raw	lane3_sync_err_raw	lane2_sync_err_raw	lane1_sync_err_raw	lane0_sync_err_raw	reserved			timeout_d3_raw	timeout_d2_raw	timeout_d1_raw	timeout_d0_raw	timeout_ck_raw	reserved			escape_d3_raw	escape_d2_raw	escape_d1_raw	escape_d0_raw	escape_ck_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RO	vsync_err_raw	Raw SOF or EOF signal async interrupt status for each lane on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[20]	RO	hsync_err_raw	Raw SOL or EOL signal async interrupt status for each lane on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[19]	RO	lane3_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 3 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[18]	RO	lane2_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 2 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	RO	lane1_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 1 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RO	lane0_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 0 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:13]	RO	reserved	Reserved.

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[12]	RO	timeout_d3_raw	Raw FSM timeout interrupt status for data lane 3 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	RO	timeout_d2_raw	Raw FSM timeout interrupt status for data lane 2 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	RO	timeout_d1_raw	Raw FSM timeout interrupt status for data lane 1 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	RO	timeout_d0_raw	Raw FSM timeout interrupt status for data lane 0 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	RO	timeout_ck_raw	Raw FSM timeout interrupt status for the clock lane on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:5]	RO	reserved	Reserved.
[4]	RO	escape_d3_raw	Raw escape sequence interrupt status for data lane 3 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RO	escape_d2_raw	Raw escape sequence interrupt status for data lane 2 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	escape_d1_raw	Raw escape sequence interrupt status for data lane 1 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	escape_d0_raw	Raw escape sequence interrupt status for data lane 0 on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	escape_ck_raw	Raw escape sequence interrupt status for the clock lane on link 0. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

INT_CLR_LINK0

INT_CLR_LINK0 is a link 0 interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x100C	INT_CLR_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_clr	hsync_err_clr	lane3_sync_err_clr	lane2_sync_err_clr	lane1_sync_err_clr	lane0_sync_err_clr	reserved			timeout_d3_clr	timeout_d2_clr	timeout_d1_clr	timeout_d0_clr	timeout_ck_clr	reserved			escape_d3_clr	escape_d2_clr	escape_d1_clr	escape_d0_clr	escape_ck_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	vsync_err_clr	SOF or EOF signal async interrupt clear for each lane on link 0. Writing 1 clears this interrupt.
[20]	RW	hsync_err_clr	SOL or EOL signal async interrupt clear for each lane on link 0. Writing 1 clears this interrupt.
[19]	RW	lane3_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 3 on link 0. Writing 1 clears this interrupt.
[18]	RW	lane2_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 2 on link 0. Writing 1 clears this interrupt.
[17]	RW	lane1_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 1 on link 0. Writing 1 clears this interrupt.
[16]	RW	lane0_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 0 on link 0. Writing 1 clears this interrupt.
[15:13]	RO	reserved	Reserved.
[12]	RW	timeout_d3_clr	FSM timeout interrupt clear for data lane 3 on link 0. Writing 1 clears this interrupt.
[11]	RW	timeout_d2_clr	FSM timeout interrupt clear for data lane 2 on link 0. Writing 1 clears this interrupt.
[10]	RW	timeout_d1_clr	FSM timeout interrupt clear for data lane 1 on link 0. Writing 1 clears this interrupt.
[9]	RW	timeout_d0_clr	FSM timeout interrupt clear for data lane 0 on link 0. Writing 1 clears this interrupt.

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[8]	RW	timeout_ck_clr	FSM timeout interrupt clear for the clock lane on link 0. Writing 1 clears this interrupt.
[7:5]	RO	reserved	Reserved.
[4]	RW	escape_d3_clr	Escape interrupt clear for data lane 3 on link 0. Writing 1 clears this interrupt.
[3]	RW	escape_d2_clr	Escape interrupt clear for data lane 2 on link 0. Writing 1 clears this interrupt.
[2]	RW	escape_d1_clr	Escape interrupt clear for data lane 1 on link 0. Writing 1 clears this interrupt.
[1]	RW	escape_d0_clr	Escape interrupt clear for data lane 0 on link 0. Writing 1 clears this interrupt.
[0]	RW	escape_ck_clr	Escape interrupt clear for the clock lane on link 0. Writing 1 clears this interrupt.

LANE_EN_LINK0

LANE_EN_LINK0 is a link 0 lane enable configuration register.

Offset Address	Register Name	Total Reset Value
0x1010	LANE_EN_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			lane3_en	reserved			lane2_en	reserved			lane1_en	reserved			lane0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	RW	lane3_en	Lane 3 enable for link 0. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.
[8]	RW	lane2_en	Lane 2 enable for link 0. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.

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[4]	RW	lane1_en	Lane 1 enable for link 0. 0: disabled 1: enabled
[3:1]	RO	reserved	Reserved.
[0]	RW	lane0_en	Lane 0 enable for link 0. 0: disabled 1: enabled

LANE_ID_LINK0

LANE_ID_LINK0 is a link 0 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1014	LANE_ID_LINK0	0x0000_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		lane3_id		reserved		lane2_id		reserved		lane1_id		reserved		lane0_id	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:12]	RW	lane3_id	Lane 3 priority for link 0. The value ranges from 0 to 3.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	lane2_id	Lane 2 priority for link 0. The value ranges from 0 to 3.
[7:6]	RO	reserved	Reserved.
[5:4]	RW	lane1_id	Lane 1 priority for link 0. The value ranges from 0 to 3.
[3:2]	RO	reserved	Reserved.
[1:0]	RW	lane0_id	Lane 0 priority for link 0. The value ranges from 0 to 3.

PHY_EN_LINK0

PHY_EN_LINK0 is a link 0 PHY channel enable register.

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Offset Address	Register Name	Total Reset Value
0x1024	PHY_EN_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phy_te_d3en	phy_te_d2en	phy_te_d1en	phy_te_d0en	reserved			phy_te_cken	phy_hs_d3en	phy_hs_d2en	phy_hs_d1en	phy_hs_d0en	reserved			phy_hs_cken	reserved	reserved	reserved	reserved	reserved			reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	phy_te_d3en	Termination enable for data lane 3 on link 0. 0: disabled 1: enabled
[22]	RW	phy_te_d2en	Termination enable for data lane 2 on link 0. 0: disabled 1: enabled
[21]	RW	phy_te_d1en	Termination enable for data lane 1 on link 0. 0: disabled 1: enabled
[20]	RW	phy_te_d0en	Termination enable for data lane 0 on link 0. 0: disabled 1: enabled
[19:17]	RO	reserved	Reserved.
[16]	RW	phy_te_cken	Termination enable for the clock lane on link 0. 0: disabled 1: enabled
[15]	RW	phy_hs_d3en	High-speed mode enable for data lane 3 on link 0. 0: disabled 1: enabled
[14]	RW	phy_hs_d2en	High-speed mode enable for data lane 2 on link 0. 0: disabled 1: enabled
[13]	RW	phy_hs_d1en	High-speed mode enable for data lane 1 on link 0. 0: disabled 1: enabled

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[12]	RW	phy_hs_d0en	High-speed mode enable for data lane 0 on link 0. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.
[8]	RW	phy_hs_cken	High-speed mode enable for the clock lane on link 0. 0: disabled 1: enabled
[7]	RO	reserved	Reserved.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RO	reserved	Reserved.
[3:1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

PHY_CFG_LINK0

PHY_CFG_LINK0 is a link 0 PHY mode configuration register.

Offset Address	Register Name	Total Reset Value
0x1028	PHY_CFG_LINK0	0x6A1F_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	phy_rg_sa_en	phy_rg_it_dt		phy_rg_it_ck		phy_rg_it_lp		reserved			phy_da_ulpb_ck	phy_da_ulpb				reserved			phy_rg_en_lp	reserved			phy_rg_en_cmos	reserved			phy_rg_en_clk	phy_rg_en_d			
Reset	0	1	1	0	1	0	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	phy_rg_sa_en	SA enable (function tuning).
[29:28]	RW	phy_rg_it_dt	High-speed mode current adjustment for data channels.
[27:26]	RW	phy_rg_it_ck	High-speed mode current adjustment for the clock channel.
[25:24]	RW	phy_rg_it_lp	Low-power mode current adjustment.
[23:21]	RO	reserved	Reserved.

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[20]	RW	phy_da_ulpb_ck	Ultra-low-power mode enable for the clock lane. 0: enable 1: disable
[19:16]	RW	phy_da_ulpb	Ultra-low-power mode enable for data lanes. Each bit corresponds to one data lane. Bit[16] corresponds to data lane 0. Bit[17] corresponds to data lane 1. Bit[18] corresponds to data lane 2. Bit[19] corresponds to data lane 3 0: enable 1: disable
[15:13]	RO	reserved	Reserved.
[12]	RW	phy_rg_en_lp	LP mode enable. In LVDS mode, the common mode voltage may trigger an internal LP-related circuit. Therefore, this signal must be disabled in LVDS mode. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.
[8]	RW	phy_rg_en_cmos	CMOS mode enable. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.
[4]	RW	phy_rg_en_clk	Clock lane enable. 0: disabled 1: enabled
[3:0]	RW	phy_rg_en_d	Data lane enable. 0: disabled 1: enabled

MIPI_LANES_NUM

MIPI_LANES_NUM is an MIPI data channel quantity register.

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Offset Address	Register Name	Total Reset Value
0x1030	MIPI_LANES_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mipi_lane_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1:0]	RW	1	Number of enabled data channels. 00: one data channel 01: two data channels 10: three data channels 11: four data channels

MIPI_RSTN

MIPI_RSTN is an MIPI controller reset control register.

Offset Address	Register Name	Total Reset Value
0x1034	MIPI_RSTN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															csi2_rstn
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	csi2_rstn	CSI2 controller reset control. 0: reset 1: deassert the reset

MIPI_DI_1

MIPI_DI_1 is an MIPI controller data ID 1 register.

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Offset Address	Register Name	Total Reset Value
0x1038	MIPI_DI_1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	di3_vc	di3_dt	di2_vc	di2_dt	di1_vc	di1_dt	di0_vc	di0_dt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RW	di3_vc	Virtual channel of data ID 3.
[29:24]	RW	di3_dt	Data type of data ID 3. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[23:22]	RW	di2_vc	Virtual channel of data ID 2.
[21:16]	RW	di2_dt	Data type of data ID 2. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[15:14]	RW	di1_vc	Virtual channel of data ID 1.
[13:8]	RW	di1_dt	Data type of data ID 1. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[7:6]	RW	di0_vc	Virtual channel of data ID 0.
[5:0]	RW	di0_dt	Data type of data ID 0. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved

MIPI_DI_2

MIPI_DI_2 is an MIPI controller data ID 2 register.

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Offset Address	Register Name	Total Reset Value
0x103C	MIPI_DI_2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	di7_vc	di7_dt	di6_vc	di6_dt	di5_vc	di5_dt	di4_vc	di4_dt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RW	di7_vc	Virtual channel of data ID 7.
[29:24]	RW	di7_dt	Data type of data ID 7. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[23:22]	RW	di6_vc	Virtual channel of data ID 6.
[21:16]	RW	di6_dt	Data type of data ID 6. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[15:14]	RW	di5_vc	Virtual channel of data ID 5.
[13:8]	RW	di5_dt	Data type of data type 5. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved
[7:6]	RW	di4_vc	Virtual channel of data ID 4.
[5:0]	RW	di4_dt	Data type of data type 4. 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 Other values: reserved

MIPI_INTR1_RAW

MIPI_INTR1_RAW is an MIPI raw interrupt 1 register.

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Offset Address	Register Name	Total Reset Value
0x1040	MIPI_INTR1_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			intr_ecc_double	intr_crc_vc3	intr_crc_vc2	intr_crc_vc1	intr_crc_vc0	intr_l_seq_di3	intr_l_seq_di2	intr_l_seq_di1	intr_l_seq_di0	intr_l_bndy_di3	intr_l_bndy_di2	intr_l_bndy_di1	intr_l_bndy_di0	intr_f_crc_vc3	intr_f_crc_vc2	intr_f_crc_vc1	intr_f_crc_vc0	intr_f_seq_vc3	intr_f_seq_vc2	intr_f_seq_vc1	intr_f_seq_vc0	intr_f_bndry_vc3	intr_f_bndry_vc2	intr_f_bndry_vc1	intr_f_bndry_vc0	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RC	intr_ecc_double	The header has at least two errors, which cannot be fixed by ECC. This field is cleared on a read.
[27]	RC	intr_crc_vc3	VC3 data CRC error. This field is cleared on a read.
[26]	RC	intr_crc_vc2	VC2 data CRC error. This field is cleared on a read.
[25]	RC	intr_crc_vc1	VC1 data CRC error. This field is cleared on a read.
[24]	RC	intr_crc_vc0	VC0 data CRC error. This field is cleared on a read.
[23]	RC	intr_l_seq_di3	VC3 and DT3 line sequence error. This field is cleared on a read.
[22]	RC	intr_l_seq_di2	VC2 and DT2 line sequence error. This field is cleared on a read.
[21]	RC	intr_l_seq_di1	VC1 and DT1 line sequence error. This field is cleared on a read.
[20]	RC	intr_l_seq_di0	VC0 and DT0 line sequence error. This field is cleared on a read.
[19]	RC	intr_l_bndy_di3	SOL and EOL mismatch for VC3 and DT3. This field is cleared on a read.
[18]	RC	intr_l_bndy_di2	SOL and EOL mismatch for VC2 and DT2. This field is cleared on a read.
[17]	RC	intr_l_bndy_di1	SOL and EOL mismatch for VC1 and DT1. This field is cleared on a read.
[16]	RC	intr_l_bndy_di0	SOL and EOL mismatch for VC0 and DT0. This field is cleared on a read.
[15]	RC	intr_f_crc_vc3	In the last frame of data, VC3 channel data has at least one CRC error. This field is cleared on a read.
[14]	RC	intr_f_crc_vc2	In the last frame of data, VC2 channel data has at least one CRC error. This field is cleared on a read.
[13]	RC	intr_f_crc_vc1	In the last frame of data, VC1 channel data has at least one CRC error. This field is cleared on a read.

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[12]	RC	intr_f_crc_vc0	In the last frame of data, VC0 channel data has at least one CRC error. This field is cleared on a read.
[11]	RC	intr_f_seq_vc3	VC3 frame sequence error. This field is cleared on a read.
[10]	RC	intr_f_seq_vc2	VC2 frame sequence error. This field is cleared on a read.
[9]	RC	intr_f_seq_vc1	VC1 frame sequence error. This field is cleared on a read.
[8]	RC	intr_f_seq_vc0	VC0 frame sequence error. This field is cleared on a read.
[7]	RC	intr_f_bndry_vc3	SOF and EOF mismatch for VC3. This field is cleared on a read.
[6]	RC	intr_f_bndry_vc2	SOF and EOF mismatch for VC2. This field is cleared on a read.
[5]	RC	intr_f_bndry_vc1	SOF and EOF mismatch for VC1. This field is cleared on a read.
[4]	RC	intr_f_bndry_vc0	SOF and EOF mismatch for VC0. This field is cleared on a read.
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

MIPI_INTR2_RAW

MIPI_INTR2_RAW is an MIPI raw interrupt 2 register.

Offset Address	Register Name	Total Reset Value
0x1044	MIPI_INTR2_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								intr_l_seq_di7	intr_l_seq_di6	intr_l_seq_di5	intr_l_seq_di4	intr_l_bndry_di7	intr_l_bndry_di6	intr_l_bndry_di5	intr_l_bndry_di4	intr_err_id_vc3	intr_err_id_vc2	intr_err_id_vc1	intr_err_id_vc0	intr_vc3_ecc_corrected	intr_vc2_ecc_corrected	intr_vc1_ecc_corrected	intr_vc0_ecc_corrected	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RC	intr_l_seq_di7	VC 7 and DT 7 line sequence error. This field is cleared on a read.
[22]	RC	intr_l_seq_di6	VC 6 and DT 6 line sequence error. This field is cleared on a read.
[21]	RC	intr_l_seq_di5	VC 5 and DT 5 line sequence error. This field is cleared on a read.

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[20]	RC	intr_l_seq_di4	VC 4 and DT 4 line sequence error. This field is cleared on a read.
[19]	RC	intr_l_bndry_di7	SOL and EOL mismatch for VC 7 and DT 7. This field is cleared on a read.
[18]	RC	intr_l_bndry_di6	SOL and EOL mismatch for VC 6 and DT 6. This field is cleared on a read.
[17]	RC	intr_l_bndry_di5	SOL and EOL mismatch for VC 5 and DT 5. This field is cleared on a read.
[16]	RC	intr_l_bndry_di4	SOL and EOL mismatch for VC 4 and DT 4. This field is cleared on a read.
[15]	RC	intr_err_id_vc3	VC3 channel data type is not supported. This field is cleared on a read.
[14]	RC	intr_err_id_vc2	VC2 channel data type is not supported. This field is cleared on a read.
[13]	RC	intr_err_id_vc1	VC1 channel data type is not supported. This field is cleared on a read.
[12]	RC	intr_err_id_vc0	VC0 channel data type is not supported. This field is cleared on a read.
[11]	RC	intr_vc3_ecc_corrected	VC3 channel header error, fixed by ECC. This field is cleared on a read.
[10]	RC	intr_vc2_ecc_corrected	VC2 channel header error, fixed by ECC. This field is cleared on a read.
[9]	RC	intr_vc1_ecc_corrected	VC1 channel header error, fixed by ECC. This field is cleared on a read.
[8]	RC	intr_vc0_ecc_corrected	VC0 channel header error, fixed by ECC. This field is cleared on a read.
[7]	RO	reserved	Reserved.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RO	reserved	Reserved.
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

MIPI_INTR1_MASK

MIPI_INTR1_MASK is an MIPI interrupt 1 mask register.

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Offset Address	Register Name	Total Reset Value
0x1048	MIPI_INTR1_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			mask_ecc_double	mask_crc_vc3	mask_crc_vc2	mask_crc_vc1	mask_crc_vc0	mask_l_seq_di3	mask_l_seq_di2	mask_l_seq_di1	mask_l_seq_di0	mask_l_bndy_di3	mask_l_bndy_di2	mask_l_bndy_di1	mask_l_bndy_di0	mask_f_crc_vc3	mask_f_crc_vc2	mask_f_crc_vc1	mask_f_crc_vc0	mask_f_seq_vc3	mask_f_seq_vc2	mask_f_seq_vc1	mask_f_seq_vc0	mask_f_bndry_vc3	mask_f_bndry_vc2	mask_f_bndry_vc1	mask_f_bndry_vc0	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28]	RW	mask_ecc_double	Ecc_double interrupt mask, corresponding to the relevant bit in the MIPI_INTR1_RAW register. 0: not masked 1: masked
[27]	RW	mask_crc_vc3	Crc_vc3 interrupt mask. 0: not masked 1: masked
[26]	RW	mask_crc_vc2	Crc_vc2 interrupt mask. 0: not masked 1: masked
[25]	RW	mask_crc_vc1	Crc_vc1 interrupt mask. 0: not masked 1: masked
[24]	RW	mask_crc_vc0	Crc_vc0 interrupt mask. 0: not masked 1: masked
[23]	RW	mask_l_seq_di3	L_seq_di3 interrupt mask. 0: not masked 1: masked
[22]	RW	mask_l_seq_di2	L_seq_di2 interrupt mask. 0: not masked 1: masked
[21]	RW	mask_l_seq_di1	L_seq_di1 interrupt mask. 0: not masked 1: masked

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[20]	RW	mask_l_seq_di0	L_seq_di0 interrupt mask. 0: not masked 1: masked
[19]	RW	mask_l_bndy_di3	L_bndy_di3 interrupt mask. 0: not masked 1: masked
[18]	RW	mask_l_bndy_di2	L_bndy_di2 interrupt mask. 0: not masked 1: masked
[17]	RW	mask_l_bndy_di1	L_bndy_di1 interrupt mask. 0: not masked 1: masked
[16]	RW	mask_l_bndy_di0	L_bndy_di0 interrupt mask. 0: not masked 1: masked
[15]	RW	mask_f_crc_vc3	F_crc_vc3 interrupt mask. 0: not masked 1: masked
[14]	RW	mask_f_crc_vc2	F_crc_vc2 interrupt mask. 0: not masked 1: masked
[13]	RW	mask_f_crc_vc1	F_crc_vc1 interrupt mask. 0: not masked 1: masked
[12]	RW	mask_f_crc_vc0	F_crc_vc0 interrupt mask. 0: not masked 1: masked
[11]	RW	mask_f_seq_vc3	F_seq_vc3 interrupt mask. 0: not masked 1: masked
[10]	RW	mask_f_seq_vc2	F_seq_vc2 interrupt mask. 0: not masked 1: masked
[9]	RW	mask_f_seq_vc1	F_seq_vc1 interrupt mask. 0: not masked 1: masked

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[8]	RW	mask_f_seq_vc0	F_seq_vc0 interrupt mask. 0: not masked 1: masked
[7]	RW	mask_f_bndry_vc3	F_bndry_vc3 interrupt mask. 0: not masked 1: masked
[6]	RW	mask_f_bndry_vc2	F_bndry_vc2 interrupt mask. 0: not masked 1: masked
[5]	RW	mask_f_bndry_vc1	F_bndry_vc1 interrupt mask. 0: not masked 1: masked
[4]	RW	mask_f_bndry_vc0	F_bndry_vc0 interrupt mask. 0: not masked 1: masked
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

MIPI_INTR2_MASK

MIPI_INTR2_MASK is an MIPI interrupt 2 mask register.

Offset Address	Register Name	Total Reset Value
0x104C	MIPI_INTR2_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								intr_1_seq_di7	intr_1_seq_di6	intr_1_seq_di5	intr_1_seq_di4	intr_1_bndry_di7	intr_1_bndry_di6	intr_1_bndry_di5	intr_1_bndry_di4	intr_err_id_vc3	intr_err_id_vc2	intr_err_id_vc1	intr_err_id_vc0	intr_vc3_ecc_corrected	intr_vc2_ecc_corrected	intr_vc1_ecc_corrected	intr_vc0_ecc_corrected	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

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[23]	RW	intr_l_seq_di7	L_seq_di7 interrupt mask, corresponding to the relevant bit in the MIPI_INTR2_RAW register. 0: not masked 1: masked
[22]	RW	intr_l_seq_di6	L_seq_di6 interrupt mask. 0: not masked 1: masked
[21]	RW	intr_l_seq_di5	L_seq_di5 interrupt mask. 0: not masked 1: masked
[20]	RW	intr_l_seq_di4	L_seq_di4 interrupt mask. 0: not masked 1: masked
[19]	RW	intr_l_bndry_di7	L_bndry_di7 interrupt mask. 0: not masked 1: masked
[18]	RW	intr_l_bndry_di6	L_bndry_di6 interrupt mask. 0: not masked 1: masked
[17]	RW	intr_l_bndry_di5	L_bndry_di5 interrupt mask. 0: not masked 1: masked
[16]	RW	intr_l_bndry_di4	L_bndry_di4 interrupt mask. 0: not masked 1: masked
[15]	RW	intr_err_id_vc3	Err_id_vc3 interrupt mask. 0: enable 1: masked
[14]	RW	intr_err_id_vc2	Err_id_vc2 interrupt mask. 0: not masked 1: masked
[13]	RW	intr_err_id_vc1	Err_id_vc1 interrupt mask. 0: not masked 1: masked
[12]	RW	intr_err_id_vc0	Err_id_vc0 interrupt mask. 0: not masked 1: masked

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[11]	RW	intr_vc3_ecc_corrected	Vc3_ecc_corrected interrupt mask. 0: not masked 1: masked
[10]	RW	intr_vc2_ecc_corrected	Vc2_ecc_corrected interrupt mask. 0: not masked 1: masked
[9]	RW	intr_vc1_ecc_corrected	Vc1_ecc_corrected interrupt mask. 0: not masked 1: masked
[8]	RW	intr_vc0_ecc_corrected	Vc0_ecc_corrected interrupt mask. 0: not masked 1: masked
[7]	RO	reserved	Reserved.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RO	reserved	Reserved.
[3]	RO	reserved	Reserved.
[2]	RO	reserved	Reserved.
[1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

MIPI_TIMEOUT

MIPI_TIMEOUT is a link 0 MIPI timeout register.

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Offset Address	Register Name	Total Reset Value
0x1060	MIPI_TIMEOUT	0x004C_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timeout_en_d	timeout_en_ck	reserved						timeout_param																							
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	timeout_en_d	FSM timeout detection enable for data lanes on link 0. 0: disabled 1: enabled
[30]	RW	timeout_en_ck	FSM timeout detection enable for the clock lane on link 0. When in the blanking region, the sensor's clock lane may be still in HS mode or enters the LP mode, depending on the features and configuration of the sensor. If the clock lane is still in HS mode, the clock lane timeout detection must be disabled. 0: disabled 1: enabled
[29:24]	RO	reserved	Reserved.
[23:0]	RW	timeout_param	FSM timeout threshold for the link 0 PHYCIL module.

MIPI_FSM_PARAM

MIPI_FSM_PARAM is a link 0 MIPI time parameter register.

Offset Address	Register Name	Total Reset Value
0x1064	MIPI_FSM_PARAM	0x1D0C_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		cyc_clk_hs0						reserved		cyc_clk_lp00						reserved		cyc_data_hs_trail						reserved		cyc_data_lp00					
Reset	0	0	0	1	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.

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[29:24]	RW	cyc_clk_hs0	FSM HS-0 status duration for the clock lane on link 0. The configured value is the actual value minus 1. 0 indicates that the status lasts for one cycle.
[23:22]	RO	reserved	Reserved.
[21:16]	RW	cyc_clk_lp00	FSM LP-00 status duration for the clock lane on link 0. The configured value is the actual value minus 1. 0 indicates that the status lasts for one cycle.
[15:14]	RO	reserved	Reserved.
[13:8]	RW	cyc_data_hs_trail	FSM HS-TRAIL status duration for data lanes on link 0. The configured value is the actual value minus 1. 0 indicates that the status lasts for one cycle.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	cyc_data_lp00	FSM LP-00 status duration for data lanes on link 0. The configured value is the actual value minus 1. 0 indicates that the status lasts for one cycle.

MIPI_FSM_CKEN

MIPI_FSM_CKEN is an MIPI FSM clock gating register.

Offset Address	Register Name	Total Reset Value
0x1068	MIPI_FSM_CKEN	0x0000_00F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mipi_d3_cken	mipi_d2_cken	mipi_d1_cken	mipi_d0_cken	reserved			mipi_ck_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7]	RW	mipi_d3_cken	FSM clock enable for data lane 3 on link 0. 0: disabled 1: enabled
[6]	RW	mipi_d2_cken	FSM clock enable for data lane 2 on link 0. 0: disabled 1: enabled

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[5]	RW	mipi_d1_cken	FSM clock enable for data lane 1 on link 0. 0: disabled 1: enabled
[4]	RW	mipi_d0_cken	FSM clock enable for data lane 0 on link 0. 0: disabled 1: enabled
[3:1]	RO	reserved	Reserved.
[0]	RW	mipi_ck_cken	FSM clock enable for the clock lane on link 0. 0: disabled 1: enabled

LINK0_LANE0_SOF_01

LINK0_LANE0_SOF_01 is an SOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1080	LINK0_LANE0_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_1																lane0_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_1	SOF synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_0	SOF synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK0_LANE0_EOF_01

LINK0_LANE0_EOF_01 is an EOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x1088	LINK0_LANE0_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_1																lane0_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_1	EOF synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_0	EOF synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK0_LANE0_SOL_01

LINK0_LANE0_SOL_01 is an SOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1090	LINK0_LANE0_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sol_1																lane0_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_1	SOL synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_0	SOL synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK0_LANE0_EOL_01

LINK0_LANE0_EOL_01 is an EOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x1098	LINK0_LANE0_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane0_eol_1				lane0_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_1	EOL synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_0	EOL synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK0_LANE1_SOF_01

LINK0_LANE1_SOF_01 is an SOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10A0	LINK0_LANE1_SOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane1_sof_1				lane1_sof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_1	SOF synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_0	SOF synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK0_LANE1_EOF_01

LINK0_LANE1_EOF_01 is an EOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10A8	LINK0_LANE1_EOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane1_eof_1				lane1_eof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_1	EOF synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_0	EOF synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK0_LANE1_SOL_01

LINK0_LANE1_SOL_01 is an SOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10B0	LINK0_LANE1_SOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane1_sol_1				lane1_sol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_1	SOL synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_0	SOL synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK0_LANE1_EOL_01

LINK0_LANE1_EOL_01 is an EOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10B8	LINK0_LANE1_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eol_1																lane1_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_1	EOL synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_0	EOL synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK0_LANE2_SOF_01

LINK0_LANE2_SOF_01 is an SOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10C0	LINK0_LANE2_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_1																lane2_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_1	SOF synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_0	SOF synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK0_LANE2_EOF_01

LINK0_LANE2_EOF_01 is an EOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10C8	LINK0_LANE2_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_1																lane2_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_1	EOF synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_0	EOF synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK0_LANE2_SOL_01

LINK0_LANE2_SOL_01 is an SOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10D0	LINK0_LANE2_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_1																lane2_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_1	SOL synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_0	SOL synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK0_LANE2_EOL_01

LINK0_LANE2_EOL_01 is an EOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10D8	LINK0_LANE2_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane2_eol_1				lane2_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_1	EOL synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_0	EOL synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK0_LANE3_SOF_01

LINK0_LANE3_SOF_01 is an SOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10E0	LINK0_LANE3_SOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane3_sof_1				lane3_sof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_1	SOF synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_0	SOF synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK0_LANE3_EOF_01

LINK0_LANE3_EOF_01 is an EOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10E8	LINK0_LANE3_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eof_1																lane3_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_1	EOF synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_0	EOF synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK0_LANE3_SOL_01

LINK0_LANE3_SOL_01 is an SOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x10F0	LINK0_LANE3_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sol_1																lane3_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_1	SOL synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_0	SOL synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK0_LANE3_EOL_01

LINK0_LANE3_EOL_01 is an EOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x10F8	LINK0_LANE3_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eol_1																lane3_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_1	EOL synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_0	EOL synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

INT_STAT_LINK1

INT_STAT_LINK1 is a link 1 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STAT_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_stat	hsync_err_stat	lane3_sync_err_stat	lane2_sync_err_stat	lane1_sync_err_stat	lane0_sync_err_stat	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RO	vsync_err_stat	SOF or EOF signal async interrupt status for each lane on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RO	hsync_err_stat	SOL or EOL signal async interrupt status for each lane on link 1. 0: No interrupt is generated. 1: An interrupt is generated.

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[19]	RO	lane3_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 3 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	lane2_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 2 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	lane1_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 1 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	lane0_sync_err_stat	EOL or EOF signal detection failure interrupt status for lane 0 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[15:0]	RO	reserved	Reserved.

INT_MASK_LINK1

INT_MASK_LINK1 is a link 1 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_MASK_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_mask	hsync_err_mask	lane3_sync_err_mask	lane2_sync_err_mask	lane1_sync_err_mask	lane0_sync_err_mask	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	vsync_err_mask	SOF or EOF signal async interrupt mask for each lane on link 1. 0: not masked 1: masked

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[20]	RW	hsync_err_mask	SOL or EOL signal async interrupt mask for each lane on link 1. 0: not masked 1: masked
[19]	RW	lane3_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 3 on link 1. 0: not masked 1: masked
[18]	RW	lane2_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 2. 0: not masked 1: masked
[17]	RW	lane1_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 1. 0: not masked 1: masked
[16]	RW	lane0_sync_err_mask	EOL or EOF signal detection failure interrupt mask for lane 0. 0: not masked 1: masked
[15:0]	RO	reserved	Reserved.

INT_RAW_LINK1

INT_RAW_LINK1 is a link 1 raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_raw	hsync_err_raw	lane3_sync_err_raw	lane2_sync_err_raw	lane1_sync_err_raw	lane0_sync_err_raw	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RO	vsync_err_raw	Raw SOF or EOF signal async interrupt status for each lane on link 1. 0: No interrupt is generated. 1: An interrupt is generated.

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[20]	RO	hsync_err_raw	Raw SOL or EOL signal async interrupt status for each lane on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RO	lane3_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 3 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	lane2_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 2 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	lane1_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 1 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	lane0_sync_err_raw	Raw EOL or EOF signal detection failure interrupt status for lane 0 on link 1. 0: No interrupt is generated. 1: An interrupt is generated.
[15:0]	RO	reserved	Reserved.

INT_CLR_LINK1

INT_CLR_LINK1 is a link 1 interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x140C	INT_CLR_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vsync_err_clr	hsync_err_clr	lane3_sync_err_clr	lane2_sync_err_clr	lane1_sync_err_clr	lane0_sync_err_clr	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.

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[21]	RW	vsync_err_clr	SOF or EOF signal async interrupt clear for each lane on link 1. Writing 1 clears this interrupt.
[20]	RW	hsync_err_clr	SOL or EOL signal async interrupt clear for each lane on link 1. Writing 1 clears this interrupt.
[19]	RW	lane3_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 3 on link 1. Writing 1 clears this interrupt.
[18]	RW	lane2_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 2 on link 1. Writing 1 clears this interrupt.
[17]	RW	lane1_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 1 on link 1. Writing 1 clears this interrupt.
[16]	RW	lane0_sync_err_clr	EOL or EOF signal detection failure interrupt clear for lane 0 on link 1. Writing 1 clears this interrupt.
[15:0]	RO	reserved	Reserved.

LANE_EN_LINK1

LANE_EN_LINK1 is a link 1 lane enable configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	LANE_EN_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			lane3_en	reserved			lane2_en	reserved			lane1_en	reserved			lane0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	RW	lane3_en	Lane 3 enable for link 1. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.

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[8]	RW	lane2_en	Lane 2 enable for link 1. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.
[4]	RW	lane1_en	Lane 1 enable for link 1. 0: disabled 1: enabled
[3:1]	RO	reserved	Reserved.
[0]	RW	lane0_en	Lane 0 enable for link 1. 0: disabled 1: enabled

LANE_ID_LINK1

LANE_ID_LINK1 is a link 1 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1414	LANE_ID_LINK1	0x0000_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		lane3_id		reserved		lane2_id		reserved		lane1_id		reserved		lane0_id	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:12]	RW	lane3_id	Lane 3 priority for link 1. The value ranges from 0 to 3.
[11:10]	RO	reserved	Reserved.
[9:8]	RW	lane2_id	Lane 2 priority for link 1. The value ranges from 0 to 3.
[7:6]	RO	reserved	Reserved.
[5:4]	RW	lane1_id	Lane 1 priority for link 1. The value ranges from 0 to 3.
[3:2]	RO	reserved	Reserved.
[1:0]	RW	lane0_id	Lane 0 priority for link 1. The value ranges from 0 to 3.

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PHY_EN_LINK1

PHY_EN_LINK1 is a link 1 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x1424	PHY_EN_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phy_te_d3en	phy_te_d2en	phy_te_d1en	phy_te_d0en	reserved			phy_te_cken	phy_hs_d3en	phy_hs_d2en	phy_hs_d1en	phy_hs_d0en	reserved			phy_hs_cken	reserved	reserved	reserved	reserved	reserved			reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	phy_te_d3en	Termination enable for data lane 3 on link 1. 0: disabled 1: enabled
[22]	RW	phy_te_d2en	Termination enable for data lane 2 on link 1. 0: disabled 1: enabled
[21]	RW	phy_te_d1en	Termination enable for data lane 1 on link 1. 0: disabled 1: enabled
[20]	RW	phy_te_d0en	Termination enable for data lane 0 on link 1. 0: disabled 1: enabled
[19:17]	RO	reserved	Reserved.
[16]	RW	phy_te_cken	Termination enable for the clock lane on link 1. 0: disabled 1: enabled
[15]	RW	phy_hs_d3en	High-speed mode enable for data lane 3 on link 1. 0: disabled 1: enabled
[14]	RW	phy_hs_d2en	High-speed mode enable for data lane 2 on link 1. 0: disabled 1: enabled

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[13]	RW	phy_hs_d1en	High-speed mode enable for data lane 1 on link 1. 0: disabled 1: enabled
[12]	RW	phy_hs_d0en	High-speed mode enable for data lane 0 on link 1. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.
[8]	RW	phy_hs_cken	High-speed mode enable for the clock lane on link 1. 0: disabled 1: enabled
[7]	RO	reserved	Reserved.
[6]	RO	reserved	Reserved.
[5]	RO	reserved	Reserved.
[4]	RO	reserved	Reserved.
[3:1]	RO	reserved	Reserved.
[0]	RO	reserved	Reserved.

PHY_CFG_LINK1

PHY_CFG_LINK1 is a link 1 PHY mode configuration register.

Offset Address	Register Name	Total Reset Value
0x1428	PHY_CFG_LINK1	0x6A1F_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rg_sa_en	rg_it_dt		rg_it_ck		rg_it_lp		reserved			da_ulpb_ck	da_ulpb				reserved			rg_en_lp	reserved			rg_en_cmos	reserved			rg_en_clk	rg_en_d			
Reset	0	1	1	0	1	0	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	rg_sa_en	SA enable (function tuning).
[29:28]	RW	rg_it_dt	High-speed mode current adjustment for data channels.
[27:26]	RW	rg_it_ck	High-speed mode current adjustment for the clock channel.
[25:24]	RW	rg_it_lp	Low-power mode current adjustment.

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[23:21]	RO	reserved	Reserved.
[20]	RW	da_ulpb_ck	Ultra-low-power mode enable for the clock lane. 0: enable 1: disable
[19:16]	RW	da_ulpb	Ultra-low-power mode enable for data lanes. Each bit corresponds to one data lane. Bit[16] corresponds to data lane 0. Bit[17] corresponds to data lane 1. Bit[18] corresponds to data lane 2. Bit[19] corresponds to data lane 3 0: enable 1: disable
[15:13]	RO	reserved	Reserved.
[12]	RW	rg_en_lp	Low-power mode enable. In LVDS mode, the common mode voltage may trigger an internal LP-related circuit. Therefore, this signal must be disabled in LVDS mode. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved.
[8]	RW	rg_en_cmos	CMOS mode enable. 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved.
[4]	RW	rg_en_clk	Clock lane enable. 0: disabled 1: enabled
[3:0]	RW	rg_en_d	Data lane enable. 0: disabled 1: enabled

LINK1_LANE0_SOF_01

LINK1_LANE0_SOF_01 is an SOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x1480	LINK1_LANE0_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_1																lane0_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_1	SOF synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_0	SOF synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK1_LANE0_EOF_01

LINK1_LANE0_EOF_01 is an EOF synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1488	LINK1_LANE0_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_1																lane0_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_1	EOF synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_0	EOF synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK1_LANE0_SOL_01

LINK1_LANE0_SOL_01 is an SOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x1490	LINK1_LANE0_SOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane0_sol_1				lane0_sol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_1	SOL synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_0	SOL synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK1_LANE0_EOL_01

LINK1_LANE0_EOL_01 is an EOL synchronization code configuration register for lane 0 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1498	LINK1_LANE0_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane0_eol_1				lane0_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_1	EOL synchronization code of frame 1 for lane 0 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_0	EOL synchronization code of frame 0 for lane 0 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK1_LANE1_SOF_01

LINK1_LANE1_SOF_01 is an SOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14A0	LINK1_LANE1_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sof_1																lane1_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_1	SOF synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_0	SOF synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK1_LANE1_EOF_01

LINK1_LANE1_EOF_01 is an EOF synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14A8	LINK1_LANE1_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eof_1																lane1_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_1	EOF synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_0	EOF synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK1_LANE1_SOL_01

LINK1_LANE1_SOL_01 is an SOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14B0	LINK1_LANE1_SOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane1_sol_1				lane1_sol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_1	SOL synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_0	SOL synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK1_LANE1_EOL_01

LINK1_LANE1_EOL_01 is an EOL synchronization code configuration register for lane 1 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14B8	LINK1_LANE1_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane1_eol_1				lane1_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_1	EOL synchronization code of frame 1 for lane 1 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_0	EOL synchronization code of frame 0 for lane 1 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK1_LANE2_SOF_01

LINK1_LANE2_SOF_01 is an SOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14C0	LINK1_LANE2_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_1																lane2_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_1	SOF synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_0	SOF synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK1_LANE2_EOF_01

LINK1_LANE2_EOF_01 is an EOF synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14C8	LINK1_LANE2_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_1																lane2_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_1	EOF synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_0	EOF synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK1_LANE2_SOL_01

LINK1_LANE2_SOL_01 is an SOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14D0	LINK1_LANE2_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_1																lane2_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_1	SOL synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_0	SOL synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK1_LANE2_EOL_01

LINK1_LANE2_EOL_01 is an EOL synchronization code configuration register for lane 2 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14D8	LINK1_LANE2_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eol_1																lane2_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_1	EOL synchronization code of frame 1 for lane 2 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_0	EOL synchronization code of frame 0 for lane 2 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LINK1_LANE3_SOF_01

LINK1_LANE3_SOF_01 is an SOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14E0	LINK1_LANE3_SOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane3_sof_1				lane3_sof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_1	SOF synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_0	SOF synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LINK1_LANE3_EOF_01

LINK1_LANE3_EOF_01 is an EOF synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14E8	LINK1_LANE3_EOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane3_eof_1				lane3_eof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_1	EOF synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_0	EOF synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LINK1_LANE3_SOL_01

LINK1_LANE3_SOL_01 is an SOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

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Offset Address	Register Name	Total Reset Value
0x14F0	LINK1_LANE3_SOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane3_sol_1				lane3_sol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_1	SOL synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_0	SOL synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LINK1_LANE3_EOL_01

LINK1_LANE3_EOL_01 is an EOL synchronization code configuration register for lane 3 in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14F8	LINK1_LANE3_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane3_eol_1				lane3_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_1	EOL synchronization code of frame 1 for lane 3 in LVDS or HiSPI mode. The field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_0	EOL synchronization code of frame 0 for lane 3 in LVDS or HiSPI mode. In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

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Contents

11 ISP 11-1
11.1 Features 11-1
11.2 Function Description 11-1
11.2.1 Function Block Diagram 11-1
11.2.2 Function Description 11-2
11.3 Register Summary 11-5
11.4 Register Description 11-15

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Figures

Figure 11-1 ISP architecture 11-2

Figure 11-2 Matrix manipulation of the color_matrix module 11-4

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Tables

Table 11-1 Summary of ISP registers (base address: 0x205A_0000) 11-5

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11 ISP

11.1 Features

The image signal processor (ISP) has the following features:

- Supports black level correction.
- Supports defect pixel correction.
- Supports domain noise reduction (DNR).
- Supports gamma correction.
- Supports dynamic range compression (DRC).
- Supports sensor data synthesis using the wide dynamic range (WDR) module.
- Supports multi-frame synthesis using the WDR module.
- Supports automatic white balance.
- Supports automatic exposure (AE).
- Supports digital anti-shake function.
- Supports the output of statistics.
- Supports lens shading correction.
- Supports image edge sharpening.
- Supports the maximum image resolution of 2592x1944.
- Supports the minimum image resolution of 480x240.
- Supports the minimum horizontal blanking zone of 32 pixels.
- Supports the minimum vertical blanking zone of 24 lines.

11.2 Function Description

11.2.1 Function Block Diagram

Figure 11-1 shows the function block diagram of the ISP.

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Figure 11-1 ISP architecture

11.2.2 Function Description

Sensor Offset Module

This module provides the sensor-related black-level correction function and supports the offset setting of four components (R, Gr, Gb, and B).

Front-end LUT Module

This module provides the Gamma_FE function that synthesizes sensor data using the WDR module and compresses the data in the wide dynamic range. The gamma curve is composed of 129 points with each point represented by a 12-bit data segment. The points between the

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given data points are obtained through interpolation. The gamma curve requires that gamma[0] is 0x000 and gamma[128] is 0xFFF.

Green Equalization Module

This module equalizes Gb and Gr when imbalance occurs and improves the image quality of some scenarios.

Defect Pixel Module

This module corrects defect pixels for the sensor. The defect pixels can be classified into dynamic defect pixels and static defect pixels. A maximum of 4096 static defect pixels can be corrected after detection. The number of dynamic defect pixels that can be corrected is not limited, and detection is not required before correction. The detection of static defect pixels, however, is more accurate than the detection of dynamic pixels.

WDR Module

This module provides the details in the bright region and dark region even in WDR scenarios.

DNR Module

This module provides the DNR function.

White Balance Module

This module provides the white balance function and supports the gain and offset setting of four components (R, Gr, Gb, and B).

Shading Module

This module corrects the lens shading. It supports the gain setting of three components (R, G, and B) for the pixels. Each pixel gain is represented by an 8-bit data segment. You can set the pixel gain for a maximum of 1296 points and obtain the other points through interpolation.

DRC Module

This module provides the vision-based DRC function. It restrains the brightness in the bright regions of an image to prevent overexposure and increases the brightness of the dark regions to record more details.

Demosaic Module

This module performs the conversion from Bayer to RGB color space and embeds sharpen_demosaic.

Color_matrix Module

This module provides matrix manipulation function, as shown in Figure 11-2. The R, G, and B are the input data, and the R', G', and B' are the output data. The color_matrix module dynamically adjusts the matrix coefficients and saturation, and corrects the color.

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Figure 11-2 Matrix manipulation of the color_matrix module

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} m_{RR} & m_{RG} & m_{RB} \\ m_{GR} & m_{GG} & m_{GB} \\ m_{BR} & m_{BG} & m_{BB} \end{pmatrix} \cdot \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

Gamma_rgb Module

This module applies to the three color channels (R, G, and B), and outputs gamma adjustment result. The gamma curve is composed of 257 points with each point represented by a 16-bit data segment. The points between the provided data points are obtained through interpolation. The gamma curve requires that gamma[0] is 0x0000 and gamma[256] is 0xFFFF.

AE Module

This module collects the AE statistics. The software can adjust the sensor based on the AE statistics to implement the AE function. The AE module divides an image into 17x15 regions (17 rows and 15 columns) and sets the weight for each region. Each region is further divided into five segments for histogram statistics collection. The histogram statistics are normalized to 0xFFFF. Therefore, only the statistics on segments 0, 1, 3, and 4 are stored. The software can read the final weighted statistics or the statistics on each region.

AWB Module

This module collects statistics on automatic white balance (AWB). The software can adjust Rgain, Ggain, and Bgain of the R, G, and B channels based on the AWB statistics to implement the AWB function. The AWB module divides an image into 17x15 regions (17 rows and 15 columns). The module then collects the G/R and G/B values of each region and the number of pixels involved in the value collection. This module collects statistics on the average values of R, G, and B and white points in the region.

AWB Sum Module

This module collects the AWB statistics. The AWB module divides an image into 17x15 regions (17 rows and 15 columns) and collects the average statistics of R, G, and B and the number of white points in each region.

Sharpen

This module sharpens the image edges of the RGB. The sharpening strength can be adjusted.

Fixed-Point Number Format

The format of a fixed-point number is represented by a.b, in which a indicates the width of integer part and b indicates the width of fractional part.

For example, the number 4.8 indicates that the upper 4 bits are used for the integer part and the lower 8 bits are used for the fractional part.

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11.3 Register Summary

Table 11-1 describes the ISP registers.

Table 11-1 Summary of ISP registers (base address: 0x205A_0000)

Offset Address	Register	Description	Page
0x0010	ACTIVE_WIDTH	Picture width register	11-15
0x0014	ACTIVE_HEIGHT	Picture height register	11-15
0x0018	RGGB_START	RGGB mode register	11-16
0x0024	DELAY_LINE_JITTER_CORRECTION	Line blanking jitter register	11-16
0x0028	DELAY_LINE_BLANKING	Blanking timing configuration register	11-17
0x002C	DELAY_LINE_MEMORY_CONFIGURATION	DNR line cache configuration register	11-17
0x0030	CONFIG_BUFFER_MODE	Update mode configuration register	11-18
0x0040	BYPASS	Bypass register	11-18
0x0044	AE_SWITCH	AE region statistics position control register	11-20
0x0048	AWB_SWITCH	AWB statistics position control register	11-21
0x0054	HISTOGRAM_SWITCH	AE global statistics position control register	11-21
0x007C	FIELDSTATUS	Frame status register	11-22
0x0078	GLOBALFSMRESET	State machine reset register	11-22
0x0080	INTERRUPT0	Interrupt 0 register	11-23
0x0084	INTERRUPT1	Interrupt 1 register	11-23
0x0088	INTERRUPT2	Interrupt 2 register	11-24
0x008C	INTERRUPT3	Interrupt 3 register	11-24
0x0090	INTERRUPT4	Interrupt 4 register	11-25
0x0094	INTERRUPT5	Interrupt 5 register	11-25
0x0098	INTERRUPT6	Interrupt 6 register	11-25
0x009C	INTERRUPT7	Interrupt 7 register	11-26
0x0130	INPUTPORT_CTRL	Input port control register	11-26

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Offset Address	Register	Description	Page
0x0134	INPUTPORT_STATUS	Input port status register	11-27
0x0140	SENSOR_R_BLACK	R component black level register for the sensor offset module	11-27
0x0144	SENSOR_GR_BLACK	Gr component black level register for the sensor offset module	11-28
0x0148	SENSOR_GB_BLACK	Gb component black level register for the sensor offset module	11-28
0x014C	SENSOR_B_BLACK	B component black level register for the sensor offset module	11-29
0x01A0	DIGITALGAIN	Sensor digital gain register	11-29
0x01A4	OFFSET	Black level compensation register	11-29
0x0188	FRONTEND_LUT_STATUS	Front-end LUT status register	11-30
0x01C0	GE_CTRL1	Green equalization module control register 1	11-30
0x01C4	GE_CTRL2	Green equalization module control register 2	11-31
0x01C8	GE_CTRL3	Green equalization module control register 3	11-32
0x01CC	GE_CTRL4	Green equalization module control register 4	11-32
0x01D0	GE_CTRL5	Green equalization module control register 5	11-33
0x01D4	GE_CTRL6	Green equalization module control register 6	11-33
0x01D8	GE_CTRL7	Green equalization module control register 7	11-33
0x01DC	GE_CTRL8	Green equalization module control register 8	11-34
0x01B0	GE_CTRL9	Green equalization module control register 9	11-34
0x01B4	GE_CTRL10	Green equalization module control register 10	11-35
0x01B8	SIGMA_IN	Manual override of noise estimation register	11-35
0x01E0	GE_CTRL11	Green equalization module control register 11	11-35

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Offset Address	Register	Description	Page
0x01E8	HP_DEFECT_PIXEL_CTRL	Defect pixel module control register	11-36
0x01EC	HP_COUNT	Defect pixel count register for the defect pixel module	11-37
0x01F0	HP_TABLE_START	Defect pixel start address register for the defect pixel module	11-37
0x01F4	HP_COUNT_IN	Written defect pixel count register for the defect pixel module	11-37
0x0850	HP_TABLE_LUT_ADDR	Lookup table (LUT) address register for the defect pixel module	11-38
0x0854	HP_TABLE_LUT_WRITE_DATA	LUT write data register for the defect pixel module	11-38
0x0858	HP_TABLE_LUT_READ_DATA	LUT read data register for the defect pixel module	11-39
0x0880–0x08FC	NP_WEIGHT_LUT	NP_WEIGHT_LUT is a noise profile lookup table register	11-39
0x0260	NP_EXP_THRESH	Noise profile threshold register	11-39
0x0264	NP_SHORT_RATIO	Noise profile short exposure ratio register	11-40
0x0268	NP_LONG_RATIO	Noise profile long exposure ratio register	11-40
0x0150	WDR_CTRL1	WDR control register 1	11-41
0x0154	WDR_CTRL2	WDR control register 2	11-41
0x0158	WDR_CTRL3	WDR control register 3	11-42
0x0160	WDR_CTRL4	WDR control register 4	11-42
0x015C	WDR_CTRL5	WDR control register 5	11-43
0x016C	WDR_CTRL6	WDR control register 6	11-43
0x0170	WDR_CTRL7	WDR control register 7	11-43
0x0174	WDR_CTRL8	WDR control register 8	11-44
0x0178	WDR_CTRL9	WDR control register 9	11-44
0x0200	DNR_CTRL1	DNR module control register 1	11-45
0x0210	DNR_CTRL2	DNR module control register 2	11-45
0x0214	DNR_CTRL3	DNR module control register 3	11-46
0x0218	DNR_CTRL4	DNR module control register 4	11-46

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Offset Address	Register	Description	Page
0x021C	DNR_THRESH_H	Horizontal noise threshold register for the DNR module	11-46
0x0220	DNR_THRESH_V	Vertical noise threshold register for the DNR module	11-47
0x0224	DNR_THRESH_SHORT	Short exposure noise threshold register for the DNR module	11-47
0x0228	DNR_THRESH_LONG	Long exposure noise threshold register for the DNR module	11-48
0x022C	DNR_STRENGTH0	High-frequency component denoise strength register for the DNR module	11-48
0x0230	DNR_STRENGTH1	Green component denoise strength register for the DNR module	11-49
0x0234	DNR_STRENGTH2	Intermediate-frequency denoise strength register for the DNR module	11-49
0x0238	DNR_STRENGTH4	Low-frequency denoise strength register for the DNR module	11-49
0x0900–0x097C	DNR_NOISE_PROFILE_LUT	Noise profile lookup table write data register for the DNR module	11-50
0x0270	DNR_EXP_THRESH	Long/short exposure threshold register for the DNR module	11-50
0x0274	DNR_RATIO_SHORT	Short exposure noise profile LUT multiplier register for the DNR module	11-51
0x0278	DNR_RATIO_LONG	Long exposure noise profile LUT multiplier register for the DNR module	11-51
0x02C0	WB_GAIN00	R component gain register for the white balance module	11-51
0x02C4	WB_GAIN01	Gr component gain register for the white balance module	11-52
0x02C8	WB_GAIN10	Gb component gain register for the white balance module	11-52
0x02CC	WB_GAIN11	B component gain register for the white balance module	11-53
0x02D0	WB_BLACK00	R component black level register for the white balance module	11-53
0x02D4	WB_BLACK01	Gr component black level register for the white balance module	11-53

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Offset Address	Register	Description	Page
0x02D8	WB_BLACK10	Gb component black level register for the white balance module	11-54
0x02DC	WB_BLACK11	B component black level register for the white balance module	11-54
0x0304	SHADING_RX	R component center horizontal coordinate register for the lens shading module	11-55
0x0308	SHADING_RY	R component center vertical coordinate register for the lens shading module	11-55
0x030C	SHADING_GX	G component center horizontal coordinate register for the lens shading module	11-55
0x0310	SHADING_GY	G component center vertical coordinate register for the lens shading module	11-56
0x0314	SHADING_BX	B component center horizontal coordinate register for the lens shading module	11-56
0x0318	SHADING_BY	B component center vertical coordinate register for the lens shading module	11-57
0x031C	SHADING_MULTR	R component shading factor for the lens shading module	11-57
0x0320	SHADING_MULTG	G component shading factor for the lens shading module	11-57
0x0324	SHADING_MULTB	B component shading factor for the lens shading module	11-58
0x0380	DRC_ENABLE	DRC enable register	11-58
0x0384	DRC_STRENGTH	DRC strength register	11-59
0x0388	DRC_CTRL	DRC module control register	11-59
0x03C8	DRC_LOOKUP1_ENABLE	DRC LUT1 enable register	11-60
0x0820	DRC_LUT1_ADDR	DRC LUT1 address register	11-60
0x0824	DRC_LUT1_DATA	DRC LUT1 data register	11-61
0x03E8	DRC_LOOKUP2_ENABLE	DRC LUT2 enable register	11-61
0x0830	DRC_LUT2_ADDR	DRC LUT2 address register	11-61

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Offset Address	Register	Description	Page
0x0834	DRC_LUT2_DATA	DRC LUT2 data register	11-62
0x0400	DEMOSAIC_VH_SLOPE	Maximum vertical/horizontal slope register for the demosaic module	11-62
0x0404	DEMOSAIC_AA_SLOPE	AA slope register	11-63
0x0408	DEMOSAIC_VA_SLOPE	VA slope register	11-63
0x040C	DEMOSAIC_UU_SLOPE	UU slope register	11-63
0x0410	DEMOSAIC_SAT_SLOPE	SAT slope register	11-64
0x0414	DEMOSAIC_VH_THRESH	VH threshold register	11-64
0x0418	DEMOSAIC_AA_THRESH	AA threshold register	11-65
0x041C	DEMOSAIC_VA_THRESH	VA threshold register	11-65
0x0420	DEMOSAIC_UU_THRESH	UU threshold register	11-65
0x0424	DEMOSAIC_SAT_THRESH	AA threshold register	11-66
0x0428	DEMOSAIC_VH_OFFSET	Vertical/horizontal offset register for the demosaic module	11-66
0x042C	DEMOSAIC_AA_OFFSET	AA offset register	11-66
0x0430	DEMOSAIC_VA_OFFSET	VA offset register	11-67
0x0434	DEMOSAIC_UU_OFFSET	UU offset register	11-67
0x0438	DEMOSAIC_SAT_OFFSET	SAT offset register	11-68
0x043C	DEMOSAIC_SHARP_ALT_D	Edge sharpen strength register	11-68
0x0440	DEMOSAIC_SHARP_ALT_UD	Flat area sharpen strength register	11-68
0x0444	DEMOSAIC_LUM_THRESH	LUM threshold register	11-69

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Offset Address	Register	Description	Page
0x0448	DEMOSAIC_NP_OFFSET	NP offset register	11-69
0x044C	DEMOSAIC_DMSC_CONFIG	Demosaic debugging configuration register	11-69
0x0450	DEMOSAIC_AC_THRESH	AC threshold register	11-70
0x0454	DEMOSAIC_AC_SLOPE	AC slope register	11-70
0x0458	DEMOSAIC_AC_OFFSET	AC offset register	11-71
0x045C	DEMOSAIC_FC_SLPOE	Anti-false color strength register	11-71
0x0460	DEMOSAIC_FC_ALIAS_SLPOE	Anti-false color strength register when the saturation value is in U2.6 format	11-71
0x0464	DEMOSAIC_FC_ALIAS_THRESH	Anti-false color strength register when the saturation value is in U0.8 format	11-72
0x0C00–0x0C7C	NP_LUT_WEIGHT	Noise profile LUT weight register	11-72
0x04A4	CCM_CTRL	Color matrix module control register	11-73
0x0480	CCM_COEFFT_RR	RR position coefficient register for the color matrix module	11-73
0x0484	CCM_COEFFT_RG	RG position coefficient register for the color matrix module	11-73
0x0488	CCM_COEFFT_RB	RB position coefficient register for the color matrix module	11-74
0x048C	CCM_COEFFT_GR	GR position coefficient register for the color matrix module	11-74
0x0490	CCM_COEFFT_GG	GG position coefficient register for the color matrix module	11-75
0x0494	CCM_COEFFT_GB	GB position coefficient register for the color matrix module	11-75
0x0498	CCM_COEFFT_BR	BR position coefficient register for the color matrix module	11-75
0x049C	CCM_COEFFT_BG	BG position coefficient register for the color matrix module	11-76
0x04A0	CCM_COEFFT_BB	BB position coefficient register for the color matrix module	11-76

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Offset Address	Register	Description	Page
0x04A8	CCM_COEFFT_WBR	R component white balance gain register for the color matrix module	11-77
0x04AC	CCM_COEFFT_WBG	G component white balance gain register for the color matrix module	11-77
0x04B0	CCM_COEFFT_WBB	B component white balance gain register for the color matrix module	11-77
0x04D0	SHARPEN_CTRL	Sharpen control register	11-78
0x04D4	SHARPEN_STRENGTH	Sharpen strength control register	11-78
0x0600	METERING_HIST_THRESH01	Segment 0 and segment 1 boundary point register for histogram statistics	11-79
0x0604	METERING_HIST_THRESH12	Segment 1 and segment 2 boundary point register for histogram statistics	11-79
0x0608	METERING_HIST_THRESH34	Segment 3 and segment 4 boundary point register for histogram statistics	11-80
0x060C	METERING_HIST_THRESH45	Segment 4 and segment 5 boundary point register for histogram statistics	11-80
0x0620	METERING_HIST0	Histogram statistics register for segment 0	11-80
0x0624	METERING_HIST1	Histogram statistics register for segment 1	11-81
0x0628	METERING_HIST3	Histogram statistics register for segment 3	11-81
0x062C	METERING_HIST4	Histogram statistics register for segment 4	11-82
0x0630	AE_NODES_USED	AE active region register	11-82
0x0640	METERING_AWB_WHITE_LEVEL	AWB brightest point register	11-82
0x0644	METERING_AWB_BLACK_LEVEL	AWB darkest point register	11-83
0x0648	METERING_AWB_CR_REF_MAX	Maximum Cr value register for the AWB reference white point	11-83
0x064C	METERING_AWB_CR_REF_MIN	Minimum Cr value register for the AWB reference white point	11-84
0x0650	METERING_AWB_CB_REF_MAX	Maximum Cb value register for the AWB reference white point	11-84
0x0654	METERING_AWB_CB_REF_MIN	Minimum Cb value register for the AWB reference white point	11-84

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Offset Address	Register	Description	Page
0x0658	METERING_AWB_RG	AWB output G/R register	11-85
0x065C	METERING_AWB_BG	AWB output G/B register	11-85
0x0660	METERING_AWB_SUM	AWB reference white point count register	11-86
0x066C	AWB_NODES_USED	AWB active region register	11-86
0x0670	CR_REF_HIGH_AWB	Maximum R/G value register for the white area register	11-86
0x0674	CR_REF_LOW_AWB	Minimum R/G value register for the white area	11-87
0x0678	CB_REF_HIGH_AWB	Maximum B/G value register for the white area	11-87
0x067C	CB_REF_LOW_AWB	Minimum B/G value register for the white area	11-88
0x06C0	HISTOGRAM_CTRL	Histogram control register	11-88
0x06C4	SCALE_CTRL	Scale control register	11-89
0x06C8	TOTAL_PIXELS	Total pixel number register	11-89
0x06CC	COUNTED_PIXEL	Involved pixel count register for statistics	11-90
0x0700	SUM_R	R pixel point sum register	11-90
0x0704	SUM_RG	RG pixel point sum register	11-91
0x0708	SUM_BG	BG pixel point sum register	11-91
0x070C	SUM_B	B pixel point sum register	11-91
0x0710	AE_SUM_NODES_USED	AE_SUM active region register	11-92
0x0740	AVG_R	AWB R component normalization sum register	11-92
0x0744	AVG_G	AWB G component normalization sum register	11-92
0x0748	AVG_B	AWB B component normalization sum register	11-93
0x074C	COUNT_ALL	Average normalization register for AVG_R, AVG_G, and AVG_B	11-93
0x0750	COUNT_MIN	Normalization count register for the pixels below the lower threshold	11-94
0x0754	COUNT_MAX	Normalization count register for the pixels above the upper threshold	11-94

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Offset Address	Register	Description	Page
0x0760	AWB_SUM_NODES_USED	AWB_SUM active region register	11-94
0x0764	MIN_THRESHOLD	AWB SUM lower threshold register	11-95
0x0768	MAX_THRESHOLD	AWB SUM upper threshold register	11-95
0x076C	AWB_SUM_CLIP	AWB SUM maximum and minimum clip register	11-95
0x0770	CR_REF	AWB SUM maximum and minimum R/G value register	11-96
0x0774	CB_REF	AWB SUM maximum and minimum B/G value register	11-96
0x0778	CR_HL_REF	AWB SUM maximum and minimum R/G value register	11-97
0x077C	CB_HL_REF	AWB SUM maximum and minimum B/G value register	11-97
0x0A00–0x0AF8	AEXP_WEIGHT	AE block weight register	11-98
0x0AFC	AEXP_WEIGHT_LAST3	Last three block weight register for the AE	11-98
0x04C0	GAMMA_STATUS	Gamma module status register	11-99
0x0530	CSC_CTRL	CSC module control register	11-100
0x0500	CSC_COEFF11	CSC module coefficient register	11-100
0x0504	CSC_COEFF12	CSC module coefficient register	11-101
0x0508	CSC_COEFF13	CSC module coefficient register	11-101
0x050C	CSC_COEFF21	CSC module coefficient register	11-101
0x0510	CSC_COEFF22	CSC module coefficient register	11-102
0x0514	CSC_COEFF23	CSC module coefficient register	11-102
0x0518	CSC_COEFF31	CSC module coefficient register	11-103
0x051C	CSC_COEFF32	CSC module coefficient register	11-103
0x0520	CSC_COEFF33	CSC module coefficient register	11-103
0x0524	CSC_COEFFO1	CSC module coefficient register	11-104
0x0528	CSC_COEFFO2	CSC module coefficient register	11-104
0x052C	CSC_COEFFO3	CSC module coefficient register	11-104
0x0538	CSC_CLIPY	CSC module Y limit register	11-105

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Offset Address	Register	Description	Page
0x053C	CSC_CLIPUV	CSC module UV limit register	11-105
0x0540	CSC_DATA_MASK_RY	Channel 1 mask register for the CSC module	11-106
0x0544	CSC_DATA_MASK_GU	Channel 2 mask register for the CSC module	11-106
0x0548	CSC_DATA_MASK_BV	Channel 3 mask register for the CSC module	11-106

11.4 Register Description

ACTIVE_WIDTH

ACTIVE_WIDTH is a picture width register.

Offset Address	Register Name	Total Reset Value
0x0010	ACTIVE_WIDTH	0x0000_0780

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ActiveWidth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	ActiveWidth	Active video width (in pixel).

ACTIVE_HEIGHT

ACTIVE_HEIGHT is a picture height register.

Offset Address	Register Name	Total Reset Value
0x0014	ACTIVE_HEIGHT	0x0000_0438

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ActiveHeight															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	ActiveHeight	Active video height (in line).

RGGB_START

RGGB_START is an RGGB mode register.

Offset Address	Register Name	Total Reset Value
0x0018	RGGB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														RGGBstart	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1:0]	RW	RGGBstart	Start color of the RGGB pattern. 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

DELAY_LINE_JITTER_CORRECTION

DELAY_LINE_JITTER_CORRECTION is a line blanking jitter register.

Offset Address	Register Name	Total Reset Value
0x0024	DELAY_LINE_JITTER_CORRECTION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																delaylinejittercorrection															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	delaylinejittercorrection	Difference between the maximum line blanking and the minimum line blanking.

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DELAY_LINE_BLANKING

DELAY_LINE_BLANKING is a blanking timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	DELAY_LINE_BLANKING	0x0018_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								delaylineextralines								delaylineregenhblank															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	delaylineextralines	Extra lines to generate at the end of the frame to flush the pipeline.
[15:0]	RW	delaylineregenhblank	Horizontal blanking interval during regeneration (0=measured input interval).

DELAY_LINE_MEMORY_CONFIGURATION

DELAY_LINE_MEMORY_CONFIGURATION is a DNR line cache configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	DELAY_LINE_MEMORY_CONFIGURATION	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														delaylinememoryconfiguration	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1:0]	RW	delaylinememoryconfiguration	Denoise line memory configuration. 00: maximum number of lines, shortest line length 01: 3/4 of maximum lines, 4/3 x shortest line 1x: 1/2 of maximum lines, 2 x shortest line

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CONFIG_BUFFER_MODE

CONFIG_BUFFER_MODE is an update mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	CONFIG_BUFFER_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ConfigBufferMode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1:0]	RW	ConfigBufferMode	Double-buffer mode select. 00: disabled (configuration are updated immediately) 01: blocked (configuration are not updated) 10: local (module configurations are updated during local vertical blanking) 11: global (all module configurations are updated during ISP vertical blanking)

BYPASS

BYPASS is a bypass register.

Offset Address	Register Name	Total Reset Value
0x0040	BYPASS	0x0000_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					ispfullbypassenable	ispprocessingbypassmode		channelswitch	bypasssharpen	reserved		bypassesc	reserved	reserved	gammafeposition	bypassframeswitchwdr	bypassgammargb	bypasscolormatrix	bypassdemosaic	bypasdrc	reserved	bypassradialshading	bypassgain	reserved	bypasssinter	bypassdefectpixel	bypassraw_frontend	bypassgammafe	bypassdigitalgain	bypassbalancefe	bypassvideotestgen
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.

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[26]	RW	ispfullbypassenable	Output is connected directly to input.
[25:24]	RW	ispprocessingbypassmode	00: full processing 01: bypass entire ISP processing (video input and output ports are still connected) and output raw sensor data 10: bypass entire ISP processing (video input and output ports are still connected) and output raw sensor data in most significant bits of channels 1 and 2 11: connect output to ground
[23]	RW	channelswitch	Switch input channels 1 and 2
[22]	RW	bypasssharpen	Bypass sharpen.
[21:20]	RO	reserved	Reserved.
[19]	RW	bypasscsc	Bypass CSC.
[18]	RO	reserved	Reserved.
[17]	RO	reserved	Reserved.
[16]	RW	gammafeposition	Gammafe position adjustment.
[15]	RW	bypassframeswitchwdr	Bypass multi-frame synthesis WDR.
[14]	RW	bypassgammargb	Bypass gamma table.
[13]	RW	bypasscolormatrix	Bypass color matrix.
[12]	RW	bypassdemosaic	Bypass demosaic module (output raw data).
[11]	RW	bypasdrc	Bypass DRC.
[10]	RO	reserved	Reserved.
[9]	RW	bypassradialshading	Bypass shading.
[8]	RW	bypassgain	Bypass black level/gain.
[7]	RW	reserved	Reserved.
[6]	RW	bypasssinter	Bypass denoise.
[5]	RW	bypassdefectpixel	Bypass defect pixel.
[4]	RW	bypassraw_frontend	Bypass raw.
[3]	RW	bypassgammafe	Bypass WDR compression expander lookup table.
[2]	RW	bypassdigitalgain	Bypass digital gain module.
[1]	RW	bypassbalancefe	Bypass front-end black level adjustment.
[0]	RW	bypassvideotestgen	Bypass video test generator.

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AE_SWITCH

AE_SWITCH is an AE region statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0044	AE_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													AEswitch		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	AEswitch	AE tap in the pipeline. 000: after static WB 001: immediately from sensor (for WDR compression modes) 010: after shading 011: after front-end LUT (for WDR compression modes) 100: after Iridix 101: immediately from sensor, channel 2 (for WDR modes) 110: after WDR stitch 111: after frontend LUT, channel 2 (for WDR modes)

AWB_SWITCH

AWB_SWITCH is an AWB statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0048	AWB_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															AWBswitch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[0]	RW	AWBswitch	AWB tap in the pipeline. 0: immediately before color matrix 1: immediately after color matrix (for sensors with strong color channel crosstalk)

HISTOGRAM_SWITCH

HISTOGRAM_SWITCH is an AE global statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0054	HISTOGRAM_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													Histogramswitch		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	Histogramswitch	AE tap in the pipeline. 000: same as AE 001: immediately from sensor, channel 1 (for WDR modes) 010: after shading 011: after frontend LUT, channel 1 (for WDR modes) 100: after Iridix 101: immediately from sensor, channel 2 (for WDR modes) 110: after WDR stitch 111: after frontend LUT, channel 2 (for WDR modes)

FIELDSTATUS

FIELDSTATUS is a frame status register.

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Offset Address	Register Name	Total Reset Value
0x007C	FIELDSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															field_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	field_status	Status of field signal.

GLOBALFSMRESET

GLOBALFSMRESET is a state machine reset register.

Offset Address	Register Name	Total Reset Value
0x0078	GLOBALFSMRESET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															global_fsm_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	global_fsm_reset	FSM synchronous reset signal.

INTERRUPT0

INTERRUPT0 is interrupt 0 register.

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Offset Address	Register Name	Total Reset Value
0x0080	INTERRUPT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt0source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt0source	Interrupt source select.

INTERRUPT1

INTERRUPT1 is interrupt 1 register.

Offset Address	Register Name	Total Reset Value
0x0084	INTERRUPT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt1source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt1source	Interrupt source select.

INTERRUPT2

INTERRUPT2 is interrupt 2 register.

Offset Address	Register Name	Total Reset Value
0x0088	INTERRUPT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt2source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt2source	Interrupt source select.

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INTERRUPT3

INTERRUPT3 is interrupt 3 register.

Offset Address	Register Name	Total Reset Value
0x008C	INTERRUPT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt3source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt3source	Interrupt source select.

INTERRUPT4

INTERRUPT4 is interrupt 4 register.

Offset Address	Register Name	Total Reset Value
0x0090	INTERRUPT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt4source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt4source	Interrupt source select.

INTERRUPT5

INTERRUPT5 is interrupt 5 register.

Offset Address	Register Name	Total Reset Value
0x0094	INTERRUPT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt5source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.

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[4:0]	RW	Interrupt5source	Interrupt source select.

INTERRUPT6

INTERRUPT6 is interrupt 6 register.

Offset Address	Register Name	Total Reset Value
0x0098	INTERRUPT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt6source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt6source	Interrupt source select.

INTERRUPT7

INTERRUPT7 is interrupt 7 register.

Offset Address	Register Name	Total Reset Value
0x009C	INTERRUPT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt7source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	Interrupt7source	Interrupt source select.

INPUTPORT_CTRL

INPUTPORT_CTRL is an input port control register.

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Offset Address	Register Name	Total Reset Value
0x0130	INPUTPORT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								freezeconfig	reserved				moderequest		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	freezeconfig	Configuration status reserved register 0: normal operation 1: retain the previous configuration state
[6:3]	RW	reserved	Reserved.
[2:0]	RW	moderequest	Request mode register 000: safe stop 001: safe start 010: urgent stop 011: urgent start 100: reserved 101: safer start 110: reserved 111: reserved

INPUTPORT_STATUS

INPUTPORT_STATUS is an input port status register.

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Offset Address	Register Name	Total Reset Value
0x0134	INPUTPORT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															modestatus
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	modestatus	For bit 0: 1: started 0: stopped For bits 1 and 2: reserved

SENSOR_R_BLACK

SENSOR_R_BLACK is an R component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x0140	SENSOR_R_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black00															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	Black00	Black offset for color channel 00 (R).

SENSOR_GR_BLACK

SENSOR_GR_BLACK is a Gr component black level register for the sensor offset module.

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Offset Address	Register Name	Total Reset Value
0x0144	SENSOR_GR_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		Black01													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:0]	RW	Black01	Black offset for color channel 01 (Gr).

SENSOR_GB_BLACK

SENSOR_GB_BLACK is a Gb component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x0148	SENSOR_GB_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		Black10													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RW	reserved	Reserved.
[13:0]	RW	Black10	Black offset for color channel 10 (Gb).

SENSOR_B_BLACK

SENSOR_B_BLACK is a B component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x014C	SENSOR_B_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		Black11													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RW	reserved	Reserved.
[13:0]	RW	Black11	Black offset for color channel 11 (B).

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DIGITALGAIN

DIGITALGAIN is a sensor digital gain register.

Offset Address	Register Name	Total Reset Value
0x01A0	DIGITALGAIN	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gain											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	gain	Sensor digital gain.

OFFSET

OFFSET is a black level compensation register.

Offset Address	Register Name	Total Reset Value
0x01A4	OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	offset	Black level compensation.

FRONTEND_LUT_STATUS

FRONTEND_LUT_STATUS is a front-end LUT status register.

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Offset Address	Register Name	Total Reset Value
0x0188	FRONTEND_LUT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										mcuready1	mcuready0	mcupriority	reserved	enable1	enable0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5]	RO	mcuready1	LUT1 is ready to receive the data from the CPU.
[4]	RO	mcuready0	LUT0 is ready to receive the data from the CPU.
[3]	RW	mcupriority	Priority of CPU port. 0: low 1: high
[2]	RO	reserved	Reserved.
[1]	RW	enable1	Front end lookup enable 1. 0: disabled 1: enabled
[0]	RW	enable0	Front end lookup enable 0. 0: disabled 1: enabled

GE_CTRL1

GE_CTRL1 is green equalization module control register 1.

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Offset Address	Register Name	Total Reset Value
0x01C0	GE_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bright_disable	dark_disable	reserved		showdynamicdefectpixel	dpenable	reserved	geenable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	bright_disable	Bright spot check disable.
[6]	RW	dark_disable	Dark spot check disable.
[5:4]	RO	reserved	Reserved.
[3]	RW	showdynamicdefect pixel	Show defect pixel. 0: off 1: on
[2]	RW	dpenable	Defect pixel enable. 0: disabled 1: enabled
[1]	RO	reserved	Reserved.
[0]	RW	geenable	Green equalization enable. 0: disabled 1: enabled

GE_CTRL2

GE_CTRL2 is green equalization module control register 2.

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Offset Address	Register Name	Total Reset Value
0x01C4	GE_CTRL2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						gestrength	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	gestrength	Green equalization strength.

GE_CTRL3

GE_CTRL3 is green equalization module control register 3.

Offset Address	Register Name	Total Reset Value
0x01C8	GE_CTRL3	0x0040_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	dpthreshold			debugsel			
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	dpthreshold	Green equalization configuration.
[15:0]	RW	debugsel	Debug port select.

GE_CTRL4

GE_CTRL4 is green equalization module control register 4.

Offset Address	Register Name	Total Reset Value
0x01CC	GE_CTRL4	0x0000_0400

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					gethreshold		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	gethreshold	Green equalization configuration.

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GE_CTRL5

GE_CTRL5 is green equalization module control register 5.

Offset Address	Register Name	Total Reset Value
0x01D0	GE_CTRL5	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dpslope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	dpslope	Slope for the HP mask function.

GE_CTRL6

GE_CTRL6 is green equalization module control register 6.

Offset Address	Register Name	Total Reset Value
0x01D4	GE_CTRL6	0x0000_00AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				geslope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	geslope	Slope for the GE mask function.

GE_CTRL7

GE_CTRL7 is green equalization module control register 7.

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Offset Address	Register Name	Total Reset Value
0x01D8	GE_CTRL7	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gesens							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[7:0]	RW	gesens	STD-DEV sensitivity.

GE_CTRL8

GE_CTRL8 is green equalization module control register 8.

Offset Address	Register Name	Total Reset Value
0x01DC	GE_CTRL8	0x0000_0266

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				hpdevthreshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	hpdevthreshold	Threshold for Deviation of other colors for HP.

GE_CTRL9

GE_CTRL9 is green equalization module control register 9.

Offset Address	Register Name	Total Reset Value
0x01B0	GE_CTRL9	0x0000_0150

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				linethresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	linethresh	Line Threshold.

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GE_CTRL10

GE_CTRL10 is green equalization module control register 10.

Offset Address	Register Name	Total Reset Value
0x01B4	GE_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hpblend							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	hpblend	HP Blend.

SIGMA_IN

SIGMA_IN is manual override of noise estimation register.

Offset Address	Register Name	Total Reset Value
0x01B8	SIGMA_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sigmain											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	sigmain	Manual override of noise estimation.

GE_CTRL11

GE_CTRL11 is green equalization module control register 11.

Offset Address	Register Name	Total Reset Value
0x01E0	GE_CTRL11	0x0030_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								threshlong								reserved								threshshort							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

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[23:16]	RW	threshlong	Noise threshold for long exposure data. Format: unsigned 4.4-bit floating-point.
[15:8]	RO	reserved	Reserved.
[7:0]	RW	threshshort	Noise threshold for short exposure data. Format: unsigned 4.4-bit floating-point.

HP_DEFECT_PIXEL_CTRL

HP_DEFECT_PIXEL_CTRL is a defect pixel module control register.

Offset Address	Register Name	Total Reset Value
0x01E8	HP_DEFECT_PIXEL_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									overflow	reserved	DetectionTrigger	ShowStaticDefect_Pixels	Enable	ShowReference	PointerReset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6]	RO	overflow	Table overflow flag. 0: not overflow 1:overflow
[5]	RO	reserved	Reserved.
[4]	RW	DetectionTrigger	Start detection on 0-1 transition.
[3]	RW	ShowStaticDefect_Pixels	Show the pixels that have been detected as defect pixels.
[2]	RW	Enable	Correction enable. 0: disabled 1: enabled
[1]	RW	ShowReference	Show reference values that are compared with actual values to detect defect pixels.
[0]	RW	PointerReset	Reset defect-pixel table pointer each frame. This field is set when the defect-pixel table has been written from the MCU.

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HP_COUNT

HP_COUNT is a defect pixel count register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01EC	HP_COUNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						DefectPixelCount									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	DefectPixelCount	Number of defect pixels detected.

HP_TABLE_START

HP_TABLE_START is a defect pixel start address register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01F0	HP_TABLE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						TableStart									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	TableStart	Address of the first defect pixel in stored defect pixels.

HP_COUNT_IN

HP_COUNT_IN is a written defect pixel count register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01F4	HP_COUNT_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						DefectPixelCountIn									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:0]	RW	DefectPixelCountIn	Number of defect pixels in the written table.

HP_TABLE_LUT_ADDR

HP_TABLE_LUT_ADDR is a lookup table (LUT) address register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x0850	HP_TABLE_LUT_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						TableLUTAddr										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	TableLUTAddr	LUT address register (valid range 0 to 1023)

HP_TABLE_LUT_WRITE_DATA

HP_TABLE_LUT_WRITE_DATA is an LUT write data register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x0854	HP_TABLE_LUT_WRITE_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								TableLUTWriteData																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	TableLUTWriteData	LUT write data register.

HP_TABLE_LUT_READ_DATA

HP_TABLE_LUT_READ_DATA is an LUT read data register for the defect pixel module.

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Offset Address	Register Name	Total Reset Value
0x0858	HP_TABLE_LUT_READ_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TableLUTReadData																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RO	TableLUTReadData	LUT read data register.

NP_WEIGHT_LUT

NP_WEIGHT_LUT is a noise profile lookup table register.

Offset Address	Register Name	Total Reset Value
0x0880–0x08FC	NP_WEIGHT_LUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weightlut_3_								weightlut_2_								weightlut_1_								weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3_	Noise profile LUT (128 8-bit registers in total).
[23:16]	RW	weightlut_2_	Noise profile LUT (128 8-bit registers in total).
[15:8]	RW	weightlut_1_	Noise profile LUT (128 8-bit registers in total).
[7:0]	RW	weightlut_0_	Noise profile LUT (128 8-bit registers in total).

NP_EXP_THRESH

NP_EXP_THRESH is a noise profile threshold register.

Offset Address	Register Name	Total Reset Value
0x0260	NP_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																expthresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	expthresh	Threshold for determining long/short exposure data.

NP_SHORT_RATIO

NP_SHORT_RATIO is a noise profile short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x0264	NP_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								shortratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	shortratio	Multiplier applied to short exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point.

NP_LONG_RATIO

NP_LONG_RATIO is a noise profile long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x0268	NP_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								longratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	longratio	Multiplier applied to long exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point.

WDR_CTRL1

WDR_CTRL1 is WDR control register 1.

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Offset Address	Register Name	Total Reset Value
0x0150	WDR_CTRL1	0x0F00_C001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				shortthresh												reserved				reserved					wdrmode	reserved		reserved			reserved
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	shortthresh	Data above this threshold will be taken from short exposure only
[15:13]	RO	reserved	Reserved.
[12:7]	RO	reserved	Reserved.
[6]	RW	wdrmode	Selects WDR mode. 0: WDR disabled 1: Frame-switching
[5]	RO	reserved	Reserved.
[4:2]	RO	reserved	Reserved.
[1:0]	RO	reserved	Reserved.

WDR_CTRL2

WDR_CTRL2 is WDR control register 2.

Offset Address	Register Name	Total Reset Value
0x0154	WDR_CTRL2	0x0000_0C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				longthresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	longthresh	Data below this threshold will be taken from long exposure only.

WDR_CTRL3

WDR_CTRL3 is WDR control register 3.

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Offset Address	Register Name	Total Reset Value
0x0158	WDR_CTRL3	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				exposureratio												reserved															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	exposureratio	Sets ratio between long and short exposures - this must match the actual exposure ratio on the sensor Format: unsigned 6.6-bit fixed-point
[15:0]	RO	reserved	Reserved.

WDR_CTRL4

WDR_CTRL4 is WDR control register 4.

Offset Address	Register Name	Total Reset Value
0x0160	WDR_CTRL4	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								stitchcorrect							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	stitchcorrect	Allows adjustment for error in sensor exposure ratio for stitching area Format: unsigned 1.7-bit fixed-point

WDR_CTRL5

WDR_CTRL5 is WDR control register 5.

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Offset Address	Register Name	Total Reset Value
0x015C	WDR_CTRL5	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stitcherrorthresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	stitcherrorthresh	Sets level for detection of stitching errors due to motion.

WDR_CTRL6

WDR_CTRL6 is WDR control register 6.

Offset Address	Register Name	Total Reset Value
0x016C	WDR_CTRL6	0x0200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	stitcherrorlimit																reserved															
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	stitcherrorlimit	Sets intensity level for long exposure below which stitching error detection is disabled.
[15:0]	RO	reserved	Reserved.

WDR_CTRL7

WDR_CTRL7 is WDR control register 7.

Offset Address	Register Name	Total Reset Value
0x0170	WDR_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				blacklevellong											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	blacklevellong	Long exposure input black level.

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WDR_CTRL8

WDR_CTRL8 is WDR control register 8.

Offset Address	Register Name	Total Reset Value
0x0174	WDR_CTRL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				blacklevelshort											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	blacklevelshort	Short exposure input black level.

WDR_CTRL9

WDR_CTRL9 is WDR control register 9.

Offset Address	Register Name	Total Reset Value
0x0178	WDR_CTRL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																blacklevelout															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	blacklevelout	Module output black level.

DNR_CTRL1

DNR_CTRL1 is DNR module control register 1.

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Offset Address	Register Name	Total Reset Value
0x0200	DNR_CTRL1	0x0000_041C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				intconfig				rmenable	Intselect	Filterselect	Enable	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RW	intconfig	Intensity blending with mosaic raw.
[7]	RW	rmenable	Lens shading correction enable. 0: disabled 1: enabled
[6]	RW	intselect	Intensity filter select.
[5]	RW	filterselect	Denoise filter fine tuning.
[4]	RW	enable	Denoise enable. 0: disabled 1: enabled
[3:0]	RW	reserved	Reserved.

DNR_CTRL2

DNR_CTRL2 is DNR module control register 2.

Offset Address	Register Name	Total Reset Value
0x0210	DNR_CTRL2	0x0000_0280

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rmcenterx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rmcenterx	Horizontal coordinates of the shading map.

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DNR_CTRL3

DNR_CTRL3 is DNR module control register 3.

Offset Address	Register Name	Total Reset Value
0x0214	DNR_CTRL3	0x0000_0168

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rmcentery															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rmcentery	Vertical coordinates of the shading map.

DNR_CTRL4

DNR_CTRL4 is DNR module control register 4.

Offset Address	Register Name	Total Reset Value
0x20218	DNR_CTRL4	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rmoffcentermult															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rmoffcentermult	Normalizing factor for sum of squares.

DNR_THRESH_H

DNR_THRESH_H a horizontal intermediate-frequency noise threshold register for the DNR module.

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Offset Address	Register Name	Total Reset Value
0x021C	DNR_THRESH_H	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	thresh4h		thresh2h		thresh1h		thresh0h	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	thresh4h	Noise threshold for low horizontal spatial frequencies.
[23:16]	RW	thresh2h	Noise threshold for medium horizontal spatial frequencies.
[15:8]	RW	thresh1h	Noise threshold for the horizontal green-only filter.
[7:0]	RW	thresh0h	Noise threshold for high horizontal spatial frequencies.

DNR_THRESH_V

DNR_THRESH_V a vertical high-frequency noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0220	DNR_THRESH_V	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	thresh4v		thresh2v		thresh1v		thresh0v	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	thresh4v	Noise threshold for low vertical spatial frequencies.
[23:16]	RW	thresh2v	Noise threshold for medium vertical spatial frequencies.
[15:8]	RW	thresh1v	Noise threshold for the vertical green-only filter.
[7:0]	RW	thresh0v	Noise threshold for high vertical spatial frequencies.

DNR_THRESH_SHORT

DNR_THRESH_SHORT is a short exposure noise threshold register for the DNR module.

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Offset Address	Register Name	Total Reset Value
0x0224	DNR_THRESH_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ThreshShort							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	ThreshShort	Noise threshold adjustment for short exposure data.

DNR_THRESH_LONG

DNR_THRESH_LONG is a long exposure noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0228	DNR_THRESH_LONG	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ThreshLong							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	ThreshLong	Noise threshold adjustment for long exposure data.

DNR_STRENGTH0

DNR_STRENGTH0 is a high-frequency component denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x022C	DNR_STRENGTH0	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	Strength0	Noise reduction effect for high spatial frequencies.

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DNR_STRENGTH1

DNR_STRENGTH1 is a green component denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0230	DNR_STRENGTH1	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	Strength1	Noise reduction effect for the green-only filter.

DNR_STRENGTH2

DNR_STRENGTH2 is an intermediate-frequency denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0234	DNR_STRENGTH2	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	Strength2	Noise reduction effect for medium spatial frequencies.

DNR_STRENGTH4

DNR_STRENGTH4 is a low-frequency denoise strength register for the DNR module.

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Offset Address	Register Name	Total Reset Value
0x0238	DNR_STRENGTH4	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	Strength4	Noise reduction effect for low spatial frequencies.

DNR_NOISE_PROFILE_LUT

DNR_NOISE_PROFILE_LUT a noise profile LUT write data register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0900–0x097C	DNR_NOISE_PROFILE_LUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weightlut_3_								weightlut_2_								weightlut_1_								weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3_	Noise profile LUT (128 registers in total).
[23:16]	RW	weightlut_2_	Noise profile LUT (128 registers in total).
[15:8]	RW	weightlut_1_	Noise profile LUT (128 registers in total).
[7:0]	RW	weightlut_0_	Noise profile LUT (128 registers in total).

DNR_EXP_THRESH

DNR_EXP_THRESH is a long/short exposure threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0270	DNR_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ExpThresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	ExpThresh	Threshold for determining long/short exposure data.

DNR_RATIO_SHORT

DNR_RATIO_SHORT is a short exposure noise profile LUT multiplier register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0274	DNR_RATIO_SHORT	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ShortRatio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	ShortRatio	Multiplier that applies to short exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point

DNR_RATIO_LONG

DNR_RATIO_LONG is a long exposure noise profile LUT multiplier register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0278	DNR_RATIO_LONG	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								LongRatio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	LongRatio	Multiplier that applies to long exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point

WB_GAIN00

WB_GAIN00 is an R component gain register for the white balance module.

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Offset Address	Register Name	Total Reset Value
0x02C0	WB_GAIN00	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Gain00	Multiplier for color channel 00 (R). Format: unsigned 4.8-bit fixed-point

WB_GAIN01

WB_GAIN01 is a Gr component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02C4	WB_GAIN01	0x0000_000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Gain01	Multiplier for color channel 01 (Gr). Format: unsigned 4.8-bit fixed-point

WB_GAIN10

WB_GAIN10 is a Gb component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02C8	WB_GAIN10	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:0]	RW	Gain10	Multiplier for color channel 10 (Gb). Format: unsigned 4.8-bit fixed-point

WB_GAIN11

WB_GAIN11 is a B component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02CC	WB_GAIN11	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Gain11	Multiplier for color channel 11 (B). Format: unsigned 4.8-bit fixed-point

WB_BLACK00

WB_BLACK00 is an R component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02D0	WB_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black00															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	Black00	Black offset for color channel 00(R).

WB_BLACK01

WB_BLACK01 is a Gr component black level register for the white balance module.

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Offset Address	Register Name	Total Reset Value
0x02D4	WB_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Black01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Black01	Black offset for color channel 01 (Gr).

WB_BLACK10

WB_BLACK10 is a Gb component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02D8	WB_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Black10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Black10	Black offset for color channel 10 (Gb).

WB_BLACK11

WB_BLACK11 is a B component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02DC	WB_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Black11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	Black11	Black offset for color channel 11 (B).

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SHADING_RX

SHADING_RX is an R component center horizontal coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0304	SHADING_RX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerRx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerRx	Rx coordinates of the shading map.

SHADING_RY

SHADING_RY is an R component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0308	SHADING_RY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerRy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerRy	Ry coordinates of the shading map.

SHADING_GX

SHADING_GX is a G component center horizontal coordinate register for the lens shading module.

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Offset Address	Register Name	Total Reset Value
0x030C	SHADING_GX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerGx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerGx	Gx coordinates of the shading map.

SHADING_GY

SHADING_GY is a G component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0310	SHADING_GY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerGy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerGy	Gy coordinates of the shading map.

SHADING_BX

SHADING_BX is a B component center horizontal coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0314	SHADING_BX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerBx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerBx	Bx coordinates of the shading map.

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SHADING_BY

SHADING_BY is a B component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0318	SHADING_BY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerBy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	centerBy	By coordinates of the shading map.

SHADING_MULTR

SHADING_MULTR is an R component shading factor for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x031C	SHADING_MULTR	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	offcentermultR	Normalizing factor for sum of squares.

SHADING_MULTG

SHADING_MULTG is a G component shading factor for the lens shading module.

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Offset Address	Register Name	Total Reset Value
0x0320	SHADING_MULTG	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultG															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	offcentermultG	Normalizing factor for sum of squares.

SHADING_MULTB

SHADING_MULTB is a B component shading factor for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0324	SHADING_MULTB	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	offcentermultB	Normalizing factor for sum of squares.

DRC_ENABLE

DRC_ENABLE is a DRC enable register.

Offset Address	Register Name	Total Reset Value
0x0380	DRC_ENABLE	0x0000_4629

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

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[0]	RW	Enable	DRC enable. 0: disabled 1: enabled

DRC_STRENGTH

DRC_STRENGTH is a DRC strength register.

Offset Address	Register Name	Total Reset Value
0x0384	DRC_STRENGTH	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	Strength	Strength of dynamic range compression. When other parameters are default values, increase the visibility of shadows.

DRC_CTRL

DRC_CTRL is a DRC module control register.

Offset Address	Register Name	Total Reset Value
0x0388	DRC_CTRL	0x0040_8012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								slopemin								slopemax								varianceintensity				VarianceSpace			
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	slopemin	Restrict the minimum slope (gain) that can be generated by the adaptive algorithm.
[15:8]	RW	slopemax	Restrict the maximum slope (gain) which can be generated by the adaptive algorithm.
[7:4]	RW	varianceintensity	Degree of luminance sensitivity of the algorithm.
[3:0]	RW	VarianceSpace	Degree of spatial sensitivity of the algorithm.

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DRC_LOOKUP1_ENABLE

DRC_LOOKUP1_ENABLE is a DRC LUT1 enable register.

Offset Address	Register Name	Total Reset Value
0x03C8	DRC_LOOKUP1_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														RevPerceptEnable	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	RevPerceptEnable	DRC look-up 1 enable. 0: disabled 1: enabled
[0]	RW	reserved	Reserved.

DRC_LUT1_ADDR

DRC_LOOKUP1_ENABLE is a DRC LUT1 address register.

Offset Address	Register Name	Total Reset Value
0x0820	DRC_LUT1_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									revperceptlutaddr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6:0]	RW	revperceptlutaddr	LUT address register (valid range 0 to 64).

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DRC_LUT1_DATA

DRC_LOOKUP1_ENABLE is a DRC LUT1 data register.

Offset Address	Register Name	Total Reset Value
0x0824	DRC_LUT1_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																RevPerceptLUTWriteData															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	RevPerceptLUTWriteData	LUT write data register.

DRC_LOOKUP2_ENABLE

DRC_LOOKUP1_ENABLE is a DRC LUT2 enable register.

Offset Address	Register Name	Total Reset Value
0x03E8	DRC_LOOKUP2_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														FwdPerceptEnable	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	FwdPerceptEnable	DRC look-up 2 enable. 0: disabled 1: enabled
[0]	RO	reserved	Reserved.

DRC_LUT2_ADDR

DRC_LOOKUP1_ENABLE is a DRC LUT2 address register.

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Offset Address	Register Name	Total Reset Value
0x0830	DRC_LUT2_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								FwdPerceptLUTAddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6:0]	RW	FwdPerceptLUTAddr	LUT address register (valid range 0 to 64).

DRC_LUT2_DATA

DRC_LOOKUP1_ENABLE is a DRC LUT2 data register.

Offset Address	Register Name	Total Reset Value
0x0834	DRC_LUT2_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				FwdPerceptLUTWriteData											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	FwdPerceptLUTWriteData	LUT write data register.

DEMOSAIC_VH_SLOPE

DEMOSAIC_VH_SLOPE is a maximum vertical/horizontal slope register for the demosaic module.

Offset Address	Register Name	Total Reset Value
0x0400	DEMOSAIC_VH_SLOPE	0x0000_00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								VHSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.

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[7:0]	RW	VHSlope	Slope of vertical/horizontal blending threshold in 4.4 logarithmic format.

DEMOSAIC_AA_SLOPE

DEMOSAIC_AA_SLOPE is an AA slope register.

Offset Address	Register Name	Total Reset Value
0x0404	DEMOSAIC_AA_SLOPE	0x0000_00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								AASlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	AASlope	Slope of angular blending threshold in 4.4 logarithmic format.

DEMOSAIC_VA_SLOPE

DEMOSAIC_VA_SLOPE is a VA slope register.

Offset Address	Register Name	Total Reset Value
0x0408	DEMOSAIC_VA_SLOPE	0x0000_00AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								VASlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	VASlope	Slope of VH-AA (VA) blending threshold in 4.4 logarithmic format.

DEMOSAIC_UU_SLOPE

DEMOSAIC_UU_SLOPE is a UU slope register.

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Offset Address	Register Name	Total Reset Value
0x040C	DEMOSAIC_UU_SLOPE	0x0000_00AD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								UUSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	UUSlope	Slope of undefined blending threshold in 4.4 logarithmic format.

DEMOSAIC_SAT_SLOPE

DEMOSAIC_SAT_SLOPE is an SAT slope register.

Offset Address	Register Name	Total Reset Value
0x0410	DEMOSAIC_SAT_SLOPE	0x0000_005D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								SatSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	SatSlope	Slope of saturation blending threshold in linear format 2.6.

DEMOSAIC_VH_THRESH

DEMOSAIC_VH_THRESH is a VH threshold register.

Offset Address	Register Name	Total Reset Value
0x0414	DEMOSAIC_VH_THRESH	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VHThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	VHThresh	Threshold for the range of vertical/horizontal blending in 0.12 format.

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DEMOSAIC_AA_THRESH

DEMOSAIC_AA_THRESH is an AA threshold register.

Offset Address	Register Name	Total Reset Value
0x0418	DEMOSAIC_AA_THRESH	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AAThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	AAThresh	Threshold for the range of angular blending in 0.12 format.

DEMOSAIC_VA_THRESH

DEMOSAIC_VA_THRESH is a VA threshold register.

Offset Address	Register Name	Total Reset Value
0x041C	DEMOSAIC_VA_THRESH	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VAThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	VAThresh	Threshold for the range of VA blending in 0.12 format.

DEMOSAIC_UU_THRESH

DEMOSAIC_UU_THRESH is a UU threshold register.

Offset Address	Register Name	Total Reset Value
0x0420	DEMOSAIC_UU_THRESH	0x0000_0171

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				UUThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:0]	RW	UUThresh	Threshold for the range of undefined blending in 0.12 format.

DEMOSAIC_SAT_THRESH

DEMOSAIC_AA_OFFSET is an AA threshold register.

Offset Address	Register Name	Total Reset Value
0x0424	DEMOSAIC_SAT_THRESH	0x0000_0171

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				SatThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	SatThresh	Threshold for the range of saturation blending in signed 2.9 format.

DEMOSAIC_VH_OFFSET

DEMOSAIC_VH_OFFSET is a vertical/horizontal offset register for the demosaic module.

Offset Address	Register Name	Total Reset Value
0x0428	DEMOSAIC_VH_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VHOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	VHOffset	Offset for vertical/horizontal blending threshold in 0.12 format.

DEMOSAIC_AA_OFFSET

DEMOSAIC_AA_OFFSET is an AA offset register.

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Offset Address	Register Name	Total Reset Value
0x042C	DEMOSAIC_AA_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AAOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	AAOffset	Offset for angular blending threshold in 0.12 format.

DEMOSAIC_VA_OFFSET

DEMOSAIC_VA_OFFSET is a VA offset register.

Offset Address	Register Name	Total Reset Value
0x0430	DEMOSAIC_VA_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VAOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	VAOffset	Offset for VA blending threshold in 0.12 format.

DEMOSAIC_UU_OFFSET

DEMOSAIC_UU_OFFSET is a UU offset register.

Offset Address	Register Name	Total Reset Value
0x0434	DEMOSAIC_UU_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				UUOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	UUOffset	Offset for undefined blending threshold in 0.12 format.

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DEMOSAIC_SAT_OFFSET

DEMOSAIC_SAT_OFFSET is an SAT offset register.

Offset Address	Register Name	Total Reset Value
0x0438	DEMOSAIC_SAT_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				SatOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	SatOffset	Offset for saturation blending threshold in signed 2.9 format.

DEMOSAIC_SHARP_ALT_D

DEMOSAIC_SHARP_ALT_D is an edge sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x043C	DEMOSAIC_SHARP_ALT_D	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharpaltd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	sharpaltd	Directional sharp mask strength in signed 4.4 format.

DEMOSAIC_SHARP_ALT_UD

DEMOSAIC_SHARP_ALT_UD is a flat area sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x0440	DEMOSAIC_SHARP_ALT_UD	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharpaltud							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.

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[7:0]	RW	sharpaltud	Non-directional sharp mask strength in signed 4.4 format.

DEMOSAIC_LUM_THRESH

DEMOSAIC_LUM_THRESH is an LUM threshold register.

Offset Address	Register Name	Total Reset Value
0x0444	DEMOSAIC_LUM_THRESH	0x0000_0060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lumthresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	lumthresh	Luminance threshold for directional sharpening.

DEMOSAIC_NP_OFFSET

DEMOSAIC_NP_OFFSET is an NP offset register.

Offset Address	Register Name	Total Reset Value
0x0448	DEMOSAIC_NP_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								npoffset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	npoffset	Noise profile offset in logarithmic 4.4 format.

DEMOSAIC_DMSC_CONFIG

DEMOSAIC_DMSC_CONFIG is a demosaic debugging configuration register.

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Offset Address	Register Name	Total Reset Value
0x044C	DEMOSAIC_DMSC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dmscconfig							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	dmscconfig	Debug output select. Set to 0x00 for normal operation.

DEMOSAIC_AC_THRESH

DEMOSAIC_AC_THRESH is an AC threshold register.

Offset Address	Register Name	Total Reset Value
0x0450	DEMOSAIC_AC_THRESH	0x0000_01B3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ACThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	ACThresh	Threshold for the range of AC blending in signed 2.9 format.

DEMOSAIC_AC_SLOPE

DEMOSAIC_AC_SLOPE is an AC slope register.

Offset Address	Register Name	Total Reset Value
0x0454	DEMOSAIC_AC_SLOPE	0x0000_00CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ACSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	ACSlope	Slope of AC blending threshold in linear 2.6 format.

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DEMOSAIC_AC_OFFSET

DEMOSAIC_AC_OFFSET is an AC offset register.

Offset Address	Register Name	Total Reset Value
0x0458	DEMOSAIC_AC_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ACOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	ACOffset	Offset for AC blending threshold in signed 2.9 format.

DEMOSAIC_FC_SLPOE

DEMOSAIC_FC_SLPOE is an anti-false color strength register.

Offset Address	Register Name	Total Reset Value
0x045C	DEMOSAIC_FC_SLPOE	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								FCSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	FCSlope	Slope (strength) of false color correction.

DEMOSAIC_FC_ALIAS_SLPOE

DEMOSAIC_FC_ALIAS_SLPOE is an anti-false color strength register when the saturation value is in U2.6 format.

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Offset Address	Register Name	Total Reset Value
0x0460	DEMOSAIC_FC_ALIAS_SLPOE	0x0000_0055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fcaliasslope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	fcaliasslope	Anti-false color correction strength when the saturation value is in U2.6 format.

DEMOSAIC_FC_ALIAS_THRESH

DEMOSAIC_FC_ALIAS_THRESH is an anti-false color strength register when the saturation value is in U0.8 format.

Offset Address	Register Name	Total Reset Value
0x0464	DEMOSAIC_FC_ALIAS_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fcaliasthresh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	fcaliasthresh	Anti-false color strength when the saturation value is in U0.8 format.

NP_LUT_WEIGHT

NP_LUT_WEIGHT is noise profile LUT weight register.

Offset Address	Register Name	Total Reset Value
0x0C00–0x0C7C	NP_LUT_WEIGHT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weightlut_3_								weightlut_2_								weightlut_1_								weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3_	Noise profile LUT (128 registers in total).
[23:16]	RW	weightlut_2_	Noise profile LUT (128 registers in total).

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[15:8]	RW	weightlut_1_	Noise profile LUT (128 registers in total).
[7:0]	RW	weightlut_0_	Noise profile LUT (128 registers in total).

CCM_CTRL

CCM_CTRL is a color matrix module control register.

Offset Address	Register Name	Total Reset Value
0x04A4	CCM_CTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	Enable	Color matrix enable. 0: disabled 1: enabled

CCM_COEFFT_RR

CCM_COEFFT_RR is an RR position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0480	CCM_COEFFT_RR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftR_R	Matrix coefficient for red-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_RG

CCM_COEFFT_RG is an RG position coefficient register for the color matrix module.

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Offset Address	Register Name	Total Reset Value
0x0484	CCM_COEFFT_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftR_G	Matrix coefficient for red-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_RB

CCM_COEFFT_RB is an RB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0488	CCM_COEFFT_RB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftR_B	Matrix coefficient for red-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GR

CCM_COEFFT_GR is a GR position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x048C	CCM_COEFFT_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	CoefftG_R	Matrix coefficient for green-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GG

CCM_COEFFT_GG is a GG position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0490	CCM_COEFFT_GG	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftG_G	Matrix coefficient for green-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GB

CCM_COEFFT_GB is a GB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0494	CCM_COEFFT_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftG_B	Matrix coefficient for green-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BR

CCM_COEFFT_BR is a BR position coefficient register for the color matrix module.

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Offset Address	Register Name	Total Reset Value
0x0498	CCM_COEFFT_BR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftB_R	Matrix coefficient for blue-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BG

CCM_COEFFT_BG is a BG position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x049C	CCM_COEFFT_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftB_G	Matrix coefficient for blue-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BB

CCM_COEFFT_BB is a BB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04A0	CCM_COEFFT_BB	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	CoefftB_B	Matrix coefficient for blue-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBR

CCM_COEFFT_WBR is an R component white balance gain register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04A8	CCM_COEFFT_WBR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftWBR	White balance gain for red. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBG

CCM_COEFFT_WBG is a G component white balance gain register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04AC	CCM_COEFFT_WBG	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBG															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	CoefftWBG	White balance gain for green. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBB

CCM_COEFFT_WBB is a B component white balance gain register for the color matrix module.

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Offset Address	Register Name	Total Reset Value
0x04B0	CCM_COEFFT_WBB	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftWBB	White balance gain for blue. Format: sign/magnitude 8.8-bit fixed-point

SHARPEN_CTRL

SHARPEN_CTRL is a sharpen control register.

Offset Address	Register Name	Total Reset Value
0x04D0	SHARPEN_CTRL	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												coring		reserved	enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:2]	RW	coring	Selects LUT memory bank, value 00 connects bank 0 to sharpening and bank 1 to programming, value 01 swap banks
[1]	RO	reserved	Reserved
[0]	RW	enable	Sharpen enable: 0: disabled 1: enabled

SHARPEN_STRENGTH

SHARPEN_STRENGTH is a sharpen strength control register.

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Offset Address	Register Name	Total Reset Value
0x04D4	SHARPEN_STRENGTH	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	strength	Sharpen strength control.

METERING_HIST_THRESH01

METERING_HIST_THRESH01 is segment 0 and segment 1 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0600	METERING_HIST_THRESH01	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh01							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	HistThresh01	Histogram threshold for bin 0/1 boundary.

METERING_HIST_THRESH12

METERING_HIST_THRESH12 is segment 1 and segment 2 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0604	METERING_HIST_THRESH12	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	HistThresh12	Histogram threshold for bin 1/2 boundary.

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METERING_HIST_THRESH34

METERING_HIST_THRESH34 is segment 3 and segment 4 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0608	METERING_HIST_THRESH34	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh34							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	HistThresh34	Histogram threshold for bin 2/3 boundary.

METERING_HIST_THRESH45

METERING_HIST_THRESH45 is segment 4 and segment 5 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x060C	METERING_HIST_THRESH45	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh45							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	HistThresh45	Histogram threshold for bin 3/4 boundary.

METERING_HIST0

METERING_HIST0 is histogram statistics register for segment 0.

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Offset Address	Register Name	Total Reset Value
0x0620	METERING_HIST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist0	Normalized histogram results for bin 0.

METERING_HIST1

METERING_HIST1 is histogram statistics register for segment 1.

Offset Address	Register Name	Total Reset Value
0x0624	METERING_HIST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist1	Normalized histogram results for bin 1.

METERING_HIST3

METERING_HIST3 is histogram statistics register for segment 3.

Offset Address	Register Name	Total Reset Value
0x0628	METERING_HIST3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist3	Normalized histogram results for bin 3.

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METERING_HIST4

METERING_HIST4 is histogram statistics register for segment 4.

Offset Address	Register Name	Total Reset Value
0x062C	METERING_HIST4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist4	Normalized histogram results for bin 4.

AE_NODES_USED

AE_NODES_USED is an AE active region register.

Offset Address	Register Name	Total Reset Value
0x0630	AE_NODES_USED	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AEXPNodesUsedVert								AEXPNodesUsedHoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:8]	RW	AEXPNodesUsedVert	Number of vertical active zones.
[7:0]	RW	AEXPNodesUsedHoriz	Number of horizontal active zones.

METERING_AWB_WHITE_LEVEL

METERING_AWB_WHITE_LEVEL is an AWB brightest point register.

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Offset Address	Register Name	Total Reset Value
0x0640	METERING_AWB_WHITE_LEVEL	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						WhiteLevelAWB										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	WhiteLevelAWB	Upper limit of valid data for AWB.

METERING_AWB_BLACK_LEVEL

METERING_AWB_BLACK_LEVEL is an AWB darkest point register.

Offset Address	Register Name	Total Reset Value
0x0644	METERING_AWB_BLACK_LEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				BlackLevelAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	BlackLevelAWB	Lower limit of valid data for AWB.

METERING_AWB_CR_REF_MAX

METERING_AWB_CR_REF_MAX is the maximum Cr value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x0648	METERING_AWB_CR_REF_MAX	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CrRefMaxAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	CrRefMaxAWB	Maximum value of R/G for white region. Format: unsigned 4.8-bit fixed-point

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METERING_AWB_CR_REF_MIN

METERING_AWB_CR_REF_MIN is the minimum Cr value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x064C	METERING_AWB_CR_REF_MIN	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CrRefMinAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	CrRefMinAWB	Minimum value of R/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_CB_REF_MAX

METERING_AWB_CB_REF_MAX is the maximum Cb value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x0650	METERING_AWB_CB_REF_MAX	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CbRefMaxAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	CbRefMaxAWB	Maximum value of B/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_CB_REF_MIN

METERING_AWB_CB_REF_MIN is the minimum Cb value register for the AWB reference white point.

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Offset Address	Register Name	Total Reset Value
0x0654	METERING_AWB_CB_REF_MIN	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CbRefMinAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	CbRefMinAWB	Minimum value of B/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_RG

METERING_AWB_RG is an AWB output G/R register.

Offset Address	Register Name	Total Reset Value
0x0658	METERING_AWB_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AWBRG											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	AWBRG	AWB output R/G. Format: unsigned 4.8-bit fixed-point

METERING_AWB_BG

METERING_AWB_BG is an AWB output G/B register.

Offset Address	Register Name	Total Reset Value
0x065C	METERING_AWB_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AWBBG											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.

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[11:0]	RO	AWBBG	AWB output B/G. Format: unsigned 4.8-bit fixed-point

METERING_AWB_SUM

METERING_AWB_SUM is an AWB reference white point count register.

Offset Address	Register Name	Total Reset Value
0x0660	METERING_AWB_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWBSUM																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	AWBSUM	Format: unsigned 4.8-bit fixed-point

AWB_NODES_USED

AWB_NODES_USED is an AWB active region register.

Offset Address	Register Name	Total Reset Value
0x066C	AWB_NODES_USED	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Vert								Horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	Vert	Number of AWB vertical regions.
[7:0]	RW	Horiz	Number of AWB horizontal regions.

CR_REF_HIGH_AWB

CR_REF_HIGH_AWB is the maximum R/G value of white area register.

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Offset Address	Register Name	Total Reset Value
0x0670	CR_REF_HIGH_AWB	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	cr_ref_high	Maximum R/G threshold in the white area. Format: U4.8

CR_REF_LOW_AWB

CR_REF_LOW_AWB is the minimum R/G value of white area register.

Offset Address	Register Name	Total Reset Value
0x0674	CR_REF_LOW_AWB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_low											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	cr_ref_low	Minimum R/G threshold in the white area.

CB_REF_HIGH_AWB

CR_REF_HIGH_AWB is the maximum B/G value of white area register.

Offset Address	Register Name	Total Reset Value
0x0678	CB_REF_HIGH_AWB	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	cb_ref_high	Maximum B/G threshold in the white area. Format: U4.8

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CB_REF_LOW_AWB

CB_REF_LOW_AWB is the minimum B/G value of white area register.

Offset Address	Register Name	Total Reset Value
0x067C	CB_REF_LOW_AWB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_low											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	cb_ref_low	Minimum B/G threshold in the white area. Format: U4.8

HISTOGRAM_CTRL

HISTOGRAM_CTRL is a histogram control register.

Offset Address	Register Name	Total Reset Value
0x06C0	HISTOGRAM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								offsety	skipy			offsetx	skipx		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	offsety	Histogram statistics control register. 0: start from the first row 1: start from the second row
[6:4]	RW	skipy	Histogram decimation in vertical direction. 000: every pixel 001: every second pixel 010: every third pixel 011: every fourth pixel 100: every fifth pixel 101: every eighth pixel Others: every nineth pixel

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[3]	RW	offsetx	0: start from the first column 1: start from the second column
[2:0]	RW	skipx	Histogram decimation in horizontal direction. 000: Reserved. 001: every third pixel 010: every fourth pixel 011: every fifth pixel 100: every eighth pixel Others: every nineth pixel

SCALE_CTRL

SCALE_CTRL is a scale control register.

Offset Address	Register Name	Total Reset Value
0x06C4	SCALE_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								scaletop				scalebottom			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:4]	RW	scaletop	Scale of top half of the range. 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved
[3:0]	RW	scalebottom	Scale of bottom half of the range. 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved

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TOTAL_PIXELS

TOTAL_PIXELS is a total pixel number register.

Offset Address	Register Name	Total Reset Value
0x06C8	TOTAL_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TotalPixels																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	TotalPixels	Total number of pixels processed (skip x and skip y are taken into account).

COUNTED_PIXEL

COUNTED_PIXEL is an involved pixel count register for statistics.

Offset Address	Register Name	Total Reset Value
0x06CC	COUNTED_PIXEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CountedPixels																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	CountedPixels	Number of pixels accumulated (with non-zero weight).

SUM_R

SUM_R is an R pixel point sum register.

Offset Address	Register Name	Total Reset Value
0x0700	SUM_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sumr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	sumr	Sum of the R pixel points.

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SUM_RG

SUM_RG is an RG pixel point sum register.

Offset Address	Register Name	Total Reset Value
0x0704	SUM_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sumrg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	sumrg	Sum of the RG pixel points.

SUM_BG

SUM_BG is a BG pixel point sum register.

Offset Address	Register Name	Total Reset Value
0x0708	SUM_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sumbg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	sumbg	Sum of the BG pixel points.

SUM_B

SUM_B is a B pixel point sum register.

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Offset Address	Register Name	Total Reset Value
0x070C	SUM_B	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				sumb			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	sumb	Sum of the B pixel points.

AE_SUM_NODES_USED

AE_SUM_NODES_USED is an AE_SUM active region register.

Offset Address	Register Name	Total Reset Value
0x0710	AE_SUM_NODES_USED	0x0000_0F11

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				aesumnodesusedvert		aesumnodesusedhoriz	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 1	0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	aesumnodesusedvert	Number of vertical active regions.
[7:0]	RW	aesumnodesusedhoriz	Number of horizontal active regions.

AVG_R

AVG_R is an AWB R component normalization sum register.

Offset Address	Register Name	Total Reset Value
0x0740	AVG_R	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				avgr			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

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[15:0]	RO	avgr	AWB R component normalization sum.

AVG_G

AVG_G is an AWB G component normalization sum register.

Offset Address	Register Name	Total Reset Value
0x0744	AVG_G	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avgg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	avgg	AWB G component normalization sum.

AVG_B

AVG_B is an AWB B component normalization sum register.

Offset Address	Register Name	Total Reset Value
0x0748	AVG_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avgb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	avgb	AWB B component normalization sum.

COUNT_ALL

COUNT_ALL is an average normalization register for AVG_R, AVG_G, and AVG_B.

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Offset Address	Register Name	Total Reset Value
0x074C	COUNT_ALL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																countall															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	countall	Average normalization value for AVG_R, AVG_G, and AVG_B.

COUNT_MIN

COUNT_MIN is a normalization count register for the pixels below the lower threshold.

Offset Address	Register Name	Total Reset Value
0x0750	COUNT_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																countmin															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	countmin	Normalization count for the pixels below the lower threshold.

COUNT_MAX

COUNT_MAX is a normalization count register for the pixels above the upper threshold.

Offset Address	Register Name	Total Reset Value
0x0754	COUNT_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																countmax															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	countmax	Normalization count for the pixels above the upper threshold.

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AWB_SUM_NODES_USED

AWB_SUM_NODES_USED is an AWB_SUM active region register.

Offset Address	Register Name	Total Reset Value
0x0760	AWB_SUM_NODES_USED	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																awbsumnodesusedvert								awbsumnodesusedhoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	awbsumnodesusedvert	Number of vertical active regions.
[7:0]	RW	awbsumnodesusedhoriz	Number of horizontal active regions.

MIN_THRESHOLD

MIN_THRESHOLD is an AWB SUM lower threshold register.

Offset Address	Register Name	Total Reset Value
0x0764	MIN_THRESHOLD	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				minthreshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	minthreshold	AWB SUM lower threshold.

MAX_THRESHOLD

MAX_THRESHOLD is an AWB SUM upper threshold register.

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Offset Address	Register Name	Total Reset Value
0x0768	MAX_THRESHOLD	0x0000_0FF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				maxthreshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RW	maxthreshold	AWB SUM upper threshold.

AWB_SUM_CLIP

AWB_SUM_CLIP is an AWB SUM maximum and minimum clip register.

Offset Address	Register Name	Total Reset Value
0x076C	AWB_SUM_CLIP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														maxclip	minclip
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	maxclip	AWB SUM upper threshold clip.
[0]	RW	minclip	AWB SUM lower threshold clip.

CR_REF

CR_REF is an AWB SUM R/G maximum and minimum value register.

Offset Address	Register Name	Total Reset Value
0x0770	CR_REF	0x0040_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crrefmin												reserved				crrefmax											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.

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[27:16]	RW	crrefmin	Minimum R/G value of the AWB SUM.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	crrefmax	Maximum R/G value of the AWB SUM.

CB_REF

CB_REF is an AWB SUM B/G maximum and minimum value register.

Offset Address	Register Name	Total Reset Value
0x0774	CB_REF	0x0040_01FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cbrefmin			reserved	cbrefmax		
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	cbrefmin	Minimum B/G value of the AWB SUM.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	cbrefmax	Maximum B/G value of the AWB SUM.

CR_HL_REF

CR_HL_REF is an AWB SUM R/G maximum and minimum value register.

Offset Address	Register Name	Total Reset Value
0x0778	CR_HL_REF	0x0000_0FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	crreflow			reserved	crrefhigh		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	crreflow	Minimum R/G value of the AWB SUM.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	crrefhigh	Maximum R/G value of the AWB SUM.

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CB_HL_REF

CB_HL_REF is an AWB SUM B/G maximum and minimum value register.

Offset Address	Register Name	Total Reset Value
0x077C	CB_HL_REF	0x0000_0FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cbreflow			reserved	cbrefhigh		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:16]	RW	cbreflow	Minimum B/G value of the AWB SUM.
[15:12]	RO	reserved	Reserved.
[11:0]	RW	cbrefhigh	Maximum B/G value of the AWB SUM.

AEXP_WEIGHT

AEXP_WEIGHT is an AE block weight register.

Offset Address	Register Name	Total Reset Value
0x0A00–0x0AF8	AEXP_WEIGHT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	aexp_weight0_3	reserved	aexp_weight0_2	reserved	aexp_weight0_1	reserved	aexp_weight0_0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	aexp_weight0_3	AE block weight, 255 4-bit registers in total.
[23:20]	RO	reserved	Reserved.
[19:16]	RW	aexp_weight0_2	AE block weight, 255 4-bit registers in total.
[15:12]	RO	reserved	Reserved.
[11:8]	RW	aexp_weight0_1	AE block weight, 255 4-bit registers in total.
[7:4]	RO	reserved	Reserved.
[3:0]	RW	aexp_weight0_0	AE block weight, 255 4-bit registers in total.

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AEXP_WEIGHT_LAST3

AEXP_WEIGHT_LAST3 is a last three block weight register for the AE.

Offset Address	Register Name	Total Reset Value
0x0AFC	AEXP_WEIGHT_LAST3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			aexp_weight16_14	reserved	aexp_weight16_13	reserved	aexp_weight16_12
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:16]	RW	aexp_weight16_14	AE block weight, one of the last three in 255 4-bit registers.
[15:12]	RO	reserved	Reserved.
[11:8]	RW	aexp_weight16_13	AE block weight, one of the last three in 255 4-bit registers.
[7:4]	RO	reserved	Reserved.
[3:0]	RW	aexp_weight16_12	AE block weight, one of the last three in 255 4-bit registers.

GAMMA_STATUS

GAMMA_STATUS is a GAMMA module status register.

Offset Address	Register Name	Total Reset Value
0x04C0	GAMMA_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								mcuready	mcupriority	enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	mcuready	LUT is ready to receive data from the CPU.
[1]	RW	mcupriority	CPU port priority. 0: low 1: high

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[0]	RW	enable	Gamma enable 0: disabled 1: enabled

CSC_CTRL

CSC_CTRL is a CSC module control register.

Offset Address	Register Name	Total Reset Value
0x0530	CSC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													enabledownsample	enablefilter	enablematrix
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	enabledownsample	Downsample enable 0: disabled 1: enabled
[1]	RW	enablefilter	Filter enable 0: disabled 1: enabled
[0]	RW	enablematrix	Color matrix enable 0: disabled 1: enabled

CSC_COEFF11

CSC_COEFF11 is a CSC module coefficient register.

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Offset Address	Register Name	Total Reset Value
0x0500	CSC_COEFF11	0x0000_002F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft11															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft11	Matrix coefficient for R-Y multiplier

CSC_COEFF12

CSC_COEFF12 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0504	CSC_COEFF12	0x0000_009D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft12															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft12	Matrix coefficient for G-Y multiplier.

CSC_COEFF13

CSC_COEFF13 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0508	CSC_COEFF13	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft13															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft13	Matrix coefficient for B-Y multiplier.

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CSC_COEFF21

CSC_COEFF21 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x050C	CSC_COEFF21	0x0000_801A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft21															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft21	Matrix coefficient for R-Cb multiplier.

CSC_COEFF22

CSC_COEFF22 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0510	CSC_COEFF22	0x0000_8057

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft22	Matrix coefficient for G-Cb multiplier.

CSC_COEFF23

CSC_COEFF23 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0514	CSC_COEFF23	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft23															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

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[15:0]	RW	coefft23	Matrix coefficient for B-Cb multiplier.

CSC_COEFF31

CSC_COEFF31 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0518	CSC_COEFF31	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft31															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft31	Matrix coefficient for R-Cr multiplier.

CSC_COEFF32

CSC_COEFF32 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x051C	CSC_COEFF32	0x0000_8066

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft32															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft32	Matrix coefficient for G-Cr multiplier.

CSC_COEFF33

CSC_COEFF33 is a CSC module coefficient register.

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Offset Address	Register Name	Total Reset Value
0x0520	CSC_COEFF33	0x0000_800A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft33															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	coefft33	Matrix coefficient for B-Cr multiplier.

CSC_COEFFO1

CSC_COEFFO1 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0524	CSC_COEFFO1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						coeffto1									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	coeffto1	Offset for Y.

CSC_COEFFO2

CSC_COEFFO2 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0528	CSC_COEFFO2	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						coeffto2									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	coeffto2	Offset for Cb

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CSC_COEFFO3

CSC_COEFFO3 is a CSC module coefficient register.

Offset Address	Register Name	Total Reset Value
0x052C	CSC_COEFFO3	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						coeffto3									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	coeffto3	Offset for Cr.

CSC_CLIPY

CSC_CLIPY is a CSC module Y limit register.

Offset Address	Register Name	Total Reset Value
0x0538	CSC_CLIPY	0x03FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						clipmaxy										reserved						clipminy									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	clipmaxy	Maximum value of Y.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	clipminy	Minimum value of Y.

CSC_CLIPUV

CSC_CLIPUV is a CSC module UV limit register.

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Offset Address	Register Name	Total Reset Value
0x053C	CSC_CLIPUV	0x03FF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	clipmaxuv			reserved	clipminuv		
Reset	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:16]	RW	clipmaxuv	Maximum value of UV.
[15:10]	RO	reserved	Reserved.
[9:0]	RW	clipminuv	Minimum value of UV.

CSC_DATA_MASK_RY

CSC_DATA_MASK_RY is a channel 1 mask register for the CSC module.

Offset Address	Register Name	Total Reset Value
0x0540	CSC_DATA_MASK_RY	0x0000_03FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						datamaskry	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	datamaskry	Data mask for channel 1 (R or Y).

CSC_DATA_MASK_GU

CSC_DATA_MASK_GU is a channel 2 mask register for the CSC module.

Offset Address	Register Name	Total Reset Value
0x0544	CSC_DATA_MASK_GU	0x0000_03FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						datamaskgu	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

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[9:0]	RW	datamaskgu	Data mask for channel 2 (G or U).

CSC_DATA_MASK_BV

CSC_DATA_MASK_BV is a channel 3 mask register for the CSC module.

Offset Address	Register Name	Total Reset Value
0x0548	CSC_DATA_MASK_BV	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						datamaskbv									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	datamaskbv	Data mask for channel 3 (B or V).

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Contents

12 Audio Interfaces 12-1
12.1 AIAO 12-1
12.1.1 Overview 12-1
12.1.2 Features 12-1
12.1.3 Function Description 12-2
12.1.4 Operating Mode 12-6
12.1.5 Register Summary 12-8
12.1.6 Register Description 12-10
12.2 Audio CODEC 12-46
12.2.1 Overview 12-46
12.2.2 Features 12-47
12.2.3 Function Description 12-47
12.2.4 Register Summary 12-48
12.2.5 Register Description 12-48

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Figures

Figure 12-1 Connection diagram over the 6-line I^2S/PCM interface in master mode 12-2
Figure 12-2 Connection diagram over the 4-line I^2S/PCM interface in master mode 12-3
Figure 12-3 Connection diagram over the 6-line I^2S/PCM interface in slave mode 12-3
Figure 12-4 Connection diagram over the 4-line I^2S/PCM interface in slave mode 12-4
Figure 12-5 I^2S interface timing 12-4
Figure 12-6 Timing of the PCM interface in standard mode 12-5
Figure 12-7 Timing of the PCM interface in customized mode 12-5
Figure 12-8 Receiving 2-/4-/8-/16-channel data over the I^2S interface 12-5
Figure 12-9 Receiving 2-/4-/8-/16-channel data over the PCM interface 12-6

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Tables

Table 12-1 Summary of AIAO registers (base address: 0x2068_0000).....12-8

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12 Audio Interfaces

12.1 AIAO

12.1.1 Overview

The audio input/audio output (AIAO) interface is used to connect to the off-chip audio CODEC to input and output audio data, implementing the recording, talkback, and playback functions. The Hi3516A has an integrated AIAO interface that includes one audio input port (AIP) and one audio output ports (AOPs). The AIP supports two, four, eight, or 16 audio inputs. The AOP supports one or two audio outputs, and implements internal interconnection over the inter-IC sound (I^2S) interface.

12.1.2 Features

The AIAO interface supports the pulse code modulation (PCM) mode and I^2S mode. The AIAO interface reads data from or writes data to the memory in DMA mode.

PCM Interfaces

The PCM interfaces have the following features:

- Support the master/slave mode.
- Transmit/receive the 8- or 16-bit linear PCM code from a channel.
- Receive 8- or 16-bit data from two, four, eight or sixteen channels.
- Support the bit stream clocks and frame sync signals internally generated and external clocks and sync signals.
- Support only short pulse sync signals in frame sync signals (the duration of those sync signals is one clock cycle). The PCM interfaces can work in both the standard mode and customized mode.
- Separately enable or disable input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

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I²S Interfaces

The I²S interfaces have the following features:

- Support the master/slave mode.
- Transmit or receive left-/right-channel 8-, 16-, 24-, or 32-bit data.
- Receive 8- or 16-bit data from two, four, eight, or 16 channels.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Separately enables or disables input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

12.1.3 Function Description

Typical Application

The Hi3516A provides one AIP and one AOP. Their functions are as follows:

- The AIP is used for receiving 8- or 16-bit data from two, four, eight, or 16 channels.
- AOP is used for playing 16-bit audio data from two channels.

AIP and AOP support both the master and slave modes. The following describes the typical connections over the I²S/PCM interface in master or slave mode.

Figure 12-1 and Figure 12-2 show the typical connections over the I²S/PCM interface in master mode.

NOTE

- In Figure 12-1, AIP and AOP connect to the I2S interface of the audio CODEC in 6-line mode. The 6-line mode means that the TX and RX have independent bit stream clock (BCLK) and audio channel select signal (WS).
- In Figure 12-2, AIP and AOP connect to the I2S interface of the audio CODEC in 4-line mode. The 4-line mode means that the TX and RX share the BCLK and WS.
- In master mode, the BCLK and WS (sync signal in PCM mode) are sent to the audio CODEC by the AIAO module.

Figure 12-1 Connection diagram over the 6-line I²S/PCM interface in master mode

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Figure 12-2 Connection diagram over the 4-line I^2S/PCM interface in master mode

Figure 12-3 and Figure 12-4 show the typical connections over the I^2S/PCM interface in slave mode.

NOTE

- In Figure 12-3, AIP and AOP connect to the I2S interface of the audio CODEC in 6-line mode. The 6-line mode means that the TX and RX have independent BCLK and WS.
- In Figure 12-4, AIP and AOP connect to the I2S interface of the audio CODEC in 4-line mode. The 4-line mode means that the TX and RX share the BCLK and WS.
- In slave mode, the BCLK and WS (sync signal in PCM mode) are sent to the audio CODEC by the AIAO module. The main working clock of the audio CODEC is provided by the Hi3516A over the AIAO_MCLK pin or provided by the external crystal oscillator.

Figure 12-3 Connection diagram over the 6-line I^2S/PCM interface in slave mode

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Figure 12-4 Connection diagram over the 4-line I^{2}S/PCM interface in slave mode

Function Principle

The AIP receives the audio data after the analog-to-digital (AD) conversion performed by the audio CODEC over the I^{2}S or PCM interface and stores the data into the cyclic FIFO created for the AIP. Then, the CPU fetches the data and stores it. In this way, audio recording is complete.

AOP reads audio data from the cyclic buffer and sends the audio data to the interconnected audio CODEC over the I^{2}S or PCM interface at a specified sampling rate. The audio CODEC performs digital-to-analog (DA) conversion on the audio data and plays the audio.

The data transferred over the I^{2}S interface consists of the right-channel data and left-channel data, which are distinguished by the levels of the WS_TX/WS_RX signal, as shown in Figure 12-5. Data is sampled on the rising edge of the BCLK_TX/BCLK_RX clock according to the protocol. The MSB is valid in the next clock cycle of WS_TX/WS_RX. The data is transferred from the MSB to the LSB.

Figure 12-5 shows the timing of the I^{2}S interface.

Figure 12-5 I^{2}S interface timing

The data transferred over the PCM interface is the single-channel data. WS_TX/WS_RX identifies the start position of the data. The MSB is transmitted or received first, and data is sampled on the falling edge. In standard timing mode, the MSB is valid in the next cycle after the high-level pulse of WS_TX/WS_RX; in customized timing mode, the MSB is aligned with the high-level pulse of WS_TX/WS_RX.

Figure 12-6 shows the timing of the PCM interface in standard mode.

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Figure 12-6 Timing of the PCM interface in standard mode

Figure 12-7 shows the timing of the PCM interface in customized mode.

Figure 12-7 Timing of the PCM interface in customized mode

When receiving 2-/4-/8-/16-channel 8-/16-bit data, the I^2S interface stores the data into the left and right channels respectively, as shown in Figure 12-8.

Figure 12-8 Receiving 2-/4-/8-/16-channel data over the I^2S interface

Figure 12-9 shows how data from multiple channels is received in PCM mode. Both the standard and customized PCM modes are supported. The AIAO interface can receive data on the rising edge or falling edging. Figure 12-9 shows how the AIAO interface receives data on the rising edge in PCM mode.

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Figure 12-9 Receiving 2-/4-/8-/16-channel data over the PCM interface

12.1.4 Operating Mode

Clock Gating and Configuration

Before enabling the AIAO interface for audio recording or playback, you must enable clock gating of the related channels (AIP/AOP). To enable clock gating, perform the following steps:

Step 1 Check whether the component connected to the AIAO interface is an independent audio CODEC or a video AD chip with an integrated audio CODEC.

- If the inherent audio CODEC of the Hi3516A is used, configure I2S_CRG_CFG0_08, I2S_CRG_CFG0_08, I2S_CRG_CFG1_08, and I2S_CRG_CFG1_00.
- If an external audio CODEC is used, configure I2S_CRG_CFG0_08 and I2S_CRG_CFG1_08.

Step 2 Enable the AIAO clock.

----End

Soft Reset

The two internal channels (AIP and AOP) of the AIAO module support separate soft reset. When the AIAO module is reset, the two channels are reset at the same time.

Recording Process

The following example assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 307 MHz clock, and the AIAO clock of the system controller is enabled. To record data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x0051eb85 to set the channel-8 MCLK to 12.288 MHz.

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Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the channel-8 clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set AIAO_SWITCH_RX_BCLK to 0x00000008 to set the working clock of the RX channel to channel-8 clock.

Step 4 Set RX_IF_ATTRI to 0xE4800014 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 5 Set RX_BUFF_SADDR to the start address of the allocated DDR (for example, 0x00000100), set RX_BUFF_SIZE to the size of the allocated DDR buffer (for example, 0x0000f000), set RX_BUFF_WPTR and RX_BUFF_RPTR to 0x0 to initialize the write and read pointers, and set RX_TRANS_SIZE to the data transfer length (for example, 0x00000f00).

Step 6 Configure RX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set RX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 7 Set RX_DSP_CTRL to 0x10000000 to enable the RX channel. Then the RX channel starts recording.

Step 8 Read RX_BUFF_WPTR and RX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that data is fetched before the cyclic buffer is full and the updated read address for the cyclic buffer is written to RX_BUFF_RPTR. Otherwise, an overflow occurs in the cyclic buffer and the audio is discontinuous.

Step 9 After recording, write 0x00000000 to RX_DSP_CTRL and query RX_DSP_CTRL until its value is 0x20000000, which indicates that the RX channel stops working.

----End

CAUTION

Configure the AIP clock before starting the AIP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.

Playback Process

The following assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 307 MHz clock, and the AIAO clock of the system controller is enabled. To play data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x0051eb85 to set the channel-8 MCLK to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the channel-8 clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set AIAO_SWITCH_TX_BCLK to 0x00000008 to set the working clock of the RX channel to channel-8 clock.

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Step 4 Set TX_IF_ATTRI to 0xE4000014 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 5 Set TX_BUFF_SADDR to the start address for the allocated buffer (for example, 0x00000100), set TX_BUFF_SIZE to the size of the allocated buffer, set TX_BUFF_WPTR and TX_BUFF_RPTR to 0x0, and set TX_TRANS_SIZE to the data transfer length. For details, see step 5 in the "Recording Process" section.

Step 6 Configure TX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set TX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 7 Set TX_DSP_CTRL to 0x10000000 to enable the playback channel.

Step 8 Read RX_BUFF_WPTR and RX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that new audio data is stuffed before the cyclic buffer is empty and the updated write address for the cyclic buffer is written to TX_BUFF_WPTR. Otherwise, an underflow occurs in the cyclic buffer and the audio is discontinuous.

Step 9 After playback, write 0x00000000 to TX_DSP_CTRL to stop the playback channel and query TX_DSP_CTRL until its value is 0x20000000, which indicates that the playback channel stops working.

----End

CAUTION

- Configure AOP clock before starting AOP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.
- Ensure that the minimum available space of the AOP cyclic buffer is 32 bytes when writing data to the cyclic buffer and updating TX_BUFF_WPTR.

12.1.5 Register Summary

Table 12-1 describes AIAO registers.

Table 12-1 Summary of AIAO registers (base address: 0x2068_0000)

Offset Address	Register	Description	Page
0x0000	AIAO_INT_ENA	AIAO interrupt enable register.	12-10
0x0004	AIAO_INT_STATUS	AIAO interrupt status register	12-11
0x0008	AIAO_INT_RAW	AIAO raw interrupt register	12-12
0x0028	AIAO_SWITCH_RX_BCLK	AIAO I^2S RX BCLK switch configuration register	12-12
0x002C	AIAO_SWITCH_TX_BCLK	AIAO I^2S TX BCLK switch configuration register	12-13

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Offset Address	Register	Description	Page
0x0030	AIAO_STATUS	AIAO status register	12-13
0x0100	I2S_CRG_CFG0_00	I^2S0 CRG configuration register 0	12-14
0x0104	I2S_CRG_CFG1_00	I^2S000 CRG configuration register 1	12-14
0x0140	I2S_CRG_CFG0_08	I^2S08 CRG configuration register 0	12-16
0x0144	I2S_CRG_CFG1_08	I^2S08 CRG configuration register 1	12-17
0x1000	RX_IF_ATTRI	Interface attribute configuration register for the RX channel	12-18
0x1004	RX_DSP_CTRL	RX channel control register	12-21
0x1080	RX_BUFF_SADDR	DDR buffer start address register for the RX channel	12-22
0x1084	RX_BUFF_SIZE	DDR buffer size register for the RX channel	12-23
0x1088	RX_BUFF_WPTR	DDR buffer write address register for the RX channel	12-23
0x108C	RX_BUFF_RPTR	DDR buffer read address register for the RX channel	12-23
0x1090	RX_BUFF_ALFULL_TH	DDR buffer almost full threshold register for the RX channel	12-24
0x1094	RX_TRANS_SIZE	Data transfer length register for the RX channel	12-24
0x1098	RX_WPTR_TMP	Write address storage register for the RX channel upon reporting of the transfer completion interrupt	12-25
0x10A0	RX_INT_ENA	Interrupt enable register for the RX channel	12-25
0x10A4	RX_INT_RAW	Raw interrupt register for the RX channel	12-26
0x10A8	RX_INT_STATUS	Interrupt status register for the RX channel	12-27
0x10AC	RX_INT_CLR	Interrupt clear register for the RX channel	12-28
0x2000	TX_IF_ATTRI	Interface attribute configuration register for the TX channel	12-30
0x2004	TX_DSP_CTRL	TX channel control register	12-32
0x2008	TX_DSP_STATUS	TX channel status register.	12-34
0x200C	TX_IF_STATUS	TX control interface status register	12-36
0x2010	TX_DMAR_STATUS	TX DMAW status register	12-37

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Offset Address	Register	Description	Page
0x2020	TX_WS_CNT	WS cyclic count status register for the TX channel	12-38
0x2024	TX_BCLK_CNT	BCLK cyclic count status register for the TX channel	12-38
0x2080	TX_BUFF_SADDR	DDR buffer start address register for the TX channel	12-38
0x2084	TX_BUFF_SIZE	DDR buffer size register for the TX channel	12-39
0x2088	TX_BUFF_WPTR	DDR buffer write address register for the TX channel	12-39
0x208C	TX_BUFF_RPTR	DDR buffer read address register for the TX channel	12-40
0x2090	TX_BUFF_ALEMPTY_TH	DDR buffer almost empty threshold register for the TX channel	12-40
0x2094	TX_TRANS_SIZE	Data transfer length register for the TX channel	12-41
0x2098	TX_RPTR_TMP	Read address storage register for the TX channel upon reporting of the transfer completion interrupt	12-41
0x20A0	TX_INT_ENA	Interrupt enable register for the TX channel	12-42
0x20A4	TX_INT_RAW	Raw interrupt register for the TX channel	12-43
0x20A8	TX_INT_STATUS	Interrupt status register for the TX channel	12-44
0x20AC	TX_INT_CLR	Interrupt clear register for the TX channel	12-45

12.1.6 Register Description

AIAO_INT_ENA

AIAO_INT_ENA is an AIAO interrupt enable register.

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Offset Address	Register Name	Total Reset Value
0x0000	AIAO_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_ena	reserved															rx_ch0_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved.
[16]	RW	tx_ch0_int_ena	TX channel interrupt enable. 0: disabled 1: enabled
[15:1]	RW	reserved	Reserved.
[0]	RW	rx_ch0_int_ena	RX channel interrupt enable. 0: disabled 1: enabled

AIAO_INT_STATUS

AIAO_INT_STATUS is an AIAO interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	AIAO_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_status	reserved															rx_ch0_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RO	tx_ch0_int_status	Interrupt status of TX channel . 0: No interrupt is generated. 1: An interrupt is generated.

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[15:1]	RO	reserved	Reserved.
[0]	RO	rx_ch0_int_status	Interrupt status of RX channel. 0: No interrupt is generated. 1: An interrupt is generated.

AIAO_INT_RAW

AIAO_INT_RAW is an AIAO raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	AIAO_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_raw	reserved															rx_ch0_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved.
[16]	RO	tx_ch0_int_raw	Raw interrupt of TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:1]	RO	reserved	Reserved.
[0]	RO	rx_ch0_int_raw	Raw interrupt of RX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

AIAO_SWITCH_RX_BCLK

AIAO_SWITCH_RX_BCLK is an AIAO I^2S RX BCLK switch configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	AIAO_SWITCH_RX_BCLK	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												inner_bclk_ws_sel_rx_00			

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Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved.
[3:0]	RW	inner_bclk_ws_sel_rx_00	Internal BCLK select for the RX channel. 0000: BCLK0 1000: BCLK8 Other values: reserved

AIAO_SWITCH_TX_BCLK

AIAO_SWITCH_TX_BCLK is an AIAO I^2S TX BCLK switch configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	AIAO_SWITCH_TX_BCLK	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							inner_bclk_ws_sel_tx_00
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved.
[3:0]	RW	inner_bclk_ws_sel_tx_00	Internal BCLK select for TX channel . 0000: BCLK0 1000: BCLK8 Other values: reserved

AIAO_STATUS

AIAO_STATUS is an AIAO status register.

Offset Address	Register Name	Total Reset Value
0x0030	AIAO_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								srst_rdy

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	srst_rdy	Soft reset status. 0: resetting 1: reset completed

I2S_CRG_CFG0_00

I2S_CRG_CFG0_00 is I^{2}S00 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0100	I2S_CRG_CFG0_00	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aiao_mclk_div																							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the AIAO clock source) x 2^27. For details about the clock source frequency of MCLK0, see section 3.2 "Clock."

I2S_CRG_CFG1_00

I2S_CRG_CFG1_00 is I^{2}S00 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0104	I2S_CRG_CFG1_00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aiao_rx_ws_en	aiao_rx_bclk_en	aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15]	RW	aiao_rx_ws_en	rx bclk gating select. 0: disabled 1: enabled
[14]	RW	aiao_rx_bclk_en	rx bclk gating select. 0: disabled 1: enabled
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity. 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity. 0: positive 1: negative
[11]	RW	aiao_bclk_sel	BCLK/FCLK select. 0: Clocks are internally generated. 1: Clocks are input from the external ADAC.
[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control. 0: The BCLK/FCLK I/O is output. 1: The BCLK/FCLK I/O is input. **NOTE** This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^2S interface.
[9]	RW	aiao_srst_req	Soft reset request. 0: reset deasserted 1: reset
[8]	RW	aiao_cken	Clock status. 0: disabled 1: enabled
[7]	RW	reserved	Reserved for extension.

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[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS. 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK. 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

I2S_CRG_CFG0_08

I2S_CRG_CFG0_08 is I^2S08 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0140	I2S_CRG_CFG0_08	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				aiao_mclk_div																											
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (MCLK0/Frequency of the AIAO clock source) x 2^27. For details about the clock source frequency of MCLK0, see section 3.2 "Clock."

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I2S_CRG_CFG1_08

I2S_CRG_CFG1_08 is I^2S08 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0144	I2S_CRG_CFG1_08	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aiao_tx_ws_en	aiao_tx_bclk_en	aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15]	RW	aiao_tx_ws_en	tx ws gating select. 0: disabled 1: enabled
[14]	RW	aiao_tx_bclk_en	tx bclk gating select. 0: disabled 1: enabled
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity. 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity. 0: positive 1: negative
[11]	RW	aiao_bclk_sel	BCLK/FCLK select. 0: Clocks are internally generated. 1: Clocks are input from the external ADAC.
[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control. 0: The BCLK/FCLK I/O is output (the AIAO works in master mode). 1: The BCLK/FCLK I/O is input (the AIAO works in slave mode). **NOTE** This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^2S interface.

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[9]	RW	aiao_srst_req	Soft reset request. 0: reset deasserted 1: reset
[8]	RW	aiao_cken	Clock status. 0: disabled 1: enabled
[7]	RW	reserved	Reserved.
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS. 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK. 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

RX_IF_ATTRI

RX_IF_ATTRI is an interface attribute configuration register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x1000	RX_IF_ATTRI	0xE400_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_sd3_sel		rx_sd2_sel		rx_sd1_sel		rx_sd0_sel		rx_sd_source_sel				reserved	rx_trackmode			rx_sd_offset								rx_multislot_en	reserved	rx_ch_num		rx_i2s_precision		rx_mode	
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:30]	RW	rx_sd3_sel	SD3 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[29:28]	RW	rx_sd2_sel	SD2 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[27:26]	RW	rx_sd1_sel	SD1 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[25:24]	RW	rx_sd0_sel	SD0 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.

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[23:20]	RW	rx_sd_source_sel	Source select for SD0, SD1, SD2, and SD3. 0000: I^2S TX0 1000: I^2S RX0 Other values: reserved
[19]	RW	reserved	Reserved.
[18:16]	RW	rx_trackmode	Audio-left and audio-right channel mode in I^2S mode. 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** Rackmode is still valid in 1-channel RX mode.
[15:8]	RW	rx_sd_offset	Number of BCLK clocks delayed for data relative to the frame sync signal in PCM mode. 0x00: 0 bit clocks 0x01: 1 bit clock 0x02: 2 bit clocks … 0xFE: 254 bit clocks 0xFF: 255 bit clocks
[7]	RW	rx_multislot_en	Time-division multiplexing validity indicator. 0: invalid (normal mode) 1: valid
[6]	RW	reserved	Reserved.

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[5:4]	RW	rx_ch_num	Number of RX channels. rx_multislot_en = 0 00: 1-channel RX (SD0 data line) 01: 2-channel RX (SD0 data line) 10: reserved 11: 8-channel RX (data lines of SD0, SD1, SD2, and SD3) Other values: reserved rx_multislot_en = 1 Number of RX channels in time-division multiplexing mode. 00: 2-channel RX (SD0 data line) 01: 4-channel RX (SD0 data line) 10: 8-channel RX (SD0 data line) 11: 16-channel RX (SD0 data line) **NOTE** The data line must be SD0 for multi-channel RX.
[3:2]	RW	rx_i2s_precision	Data sampling precision. rx_multislot_en = 0 I^2S normal mode: 00: reserved 01: 16 bits 10: 24 bits 11: reserved PCM normal mode: 00: 8 bits 01: 16 bits Other values: reserved rx_multislot_en = 1 I^2S/PCM mode: 00: 8 bits 01: 16 bits Other values: reserved
[1:0]	RW	rx_mode	Interface mode of the RX channel. 00: I^2S mode 01: PCM mode Other values: reserved

RX_DSP_CTRL

RX_DSP_CTRL is an RX channel control register.

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Offset Address	Register Name	Total Reset Value
0x1004	RX_DSP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		disable_done	rx_enable	bypass_en	reserved																										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29]	RW	disable_done	RX channel stop/complete indicator. 0: The RX channel stops but the operation is not complete. 1: The RX channel stops and the operation is complete.
[28]	RW	rx_enable	RX channel start/stop indicator. 0: stop 1: start
[27]	RW	bypass_en	Operation bypass enable (the control function still takes effect). 0: disabled 1: enabled (trackmode is bypassed)
[26:0]	RW	reserved	Reserved.

RX_BUFF_SADDR

RX_BUFF_SADDR is a DDR buffer start address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1080	RX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_buff_saddr	Start address for the DDR buffer of RX channel 0. Its unit is byte. **NOTE** The start address must be 128x2-bit-aligned.

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RX_BUFF_SIZE

RX_BUFF_SIZE is a DDR buffer size register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1084	RX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	rx_buff_size	DDR buffer size of the RX channel. Its unit is byte. **NOTE** The buffer size must be an integral multiple of 32 bytes.

RX_BUFF_WPTR

RX_BUFF_WPTR is a DDR buffer write address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1088	RX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	rx_buff_wptr	Write address for the DDR buffer of the RX channel. Its unit is byte. **NOTE** • The write address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The write address must be 128x2-bit-aligned.

RX_BUFF_RPTR

RX_BUFF_RPTR is a DDR buffer read address register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x108C	RX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	rx_buff_rptr	Read address for the DDR buffer of the RX channel. Its unit is byte. **NOTE** • The read address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The software operation is performed by byte, and the hardware operation is performed by 32 bytes.

RX_BUFF_ALFULL_TH

RX_BUFF_ALFULL_TH is a DDR buffer almost full threshold register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1090	RX_BUFF_ALFULL_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_alfull_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	rx_buff_alfull_th	Almost full threshold for the DDR buffer of the RX channel. Its unit is byte. If the available space of the DDR buffer is below the almost full threshold, the almost full raw interrupt is generated. **NOTE** If the rx_alfull_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x40.

RX_TRANS_SIZE

RX_TRANS_SIZE is data transfer length register for the RX interrupt.

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Offset Address	Register Name	Total Reset Value
0x1094	RX_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_trans_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	rx_trans_size	After the RX channel receives the audio data with the length of rx_trans_size (in byte), a transfer completion interrupt is generated.

RX_WPTR_TMP

RX_WPTR_TMP is a write address storage register for the RX channel upon reporting of the transfer completion interrupt.

Offset Address	Register Name	Total Reset Value
0x1098	RX_WPTR_TMP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_wptr_tmp																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RO	rx_wptr_tmp	This field is used to save the write address for the RX channel when the transfer completion interrupt is reported.

RX_INT_ENA

RX_INT_ENA is an interrupt enable register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x10A0	RX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo_lost_int_ena	reserved	rx_stop_int_ena	reserved	rx_bfifo_full_int_ena	rx_alfull_int_ena	rx_full_int_ena	rx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7]	RO	rx_fifo_lost_int_ena	Frame loss interrupt enable for the RX channel. 0: disabled 1: enabled
[6]	RO	reserved	Reserved.
[5]	RW	rx_stop_int_ena	Stop interrupt enable for the RX channel. 0: disabled 1: enabled
[4]	RW	reserved	Reserved.
[3]	RW	rx_bfifo_full_int_ena	Bus FIFO overflow interrupt enable for the RX channel. 0: disabled 1: enabled
[2]	RW	rx_alfull_int_ena	DDR buffer almost full interrupt enable for the RX channel. 0: disabled 1: enabled
[1]	RW	rx_full_int_ena	DDR buffer full interrupt for the RX channel. 0: disabled 1: enabled
[0]	RW	rx_trans_int_ena	Transfer completion interrupt enable for the RX channel. 0: disabled 1: enabled

RX_INT_RAW

RX_INT_RAW is a raw interrupt register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x10A4	RX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo_lost_int_raw	reserved	rx_stop_int_raw	reserved	rx_fifo_full_int_raw	rx_alfull_int_raw	rx_full_int_raw	rx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	rx_fifo_lost_int_raw	Data full lost raw interrupt of the RX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	reserved	Reserved.
[5]	RO	rx_stop_int_raw	Stop raw interrupt of the RX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	reserved	Reserved.
[3]	RO	rx_fifo_full_int_raw	Bus FIFO overflow raw interrupt of the RX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	rx_alfull_int_raw	DDR buffer almost full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	rx_full_int_raw	DDR buffer full raw interrupt of the RX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	rx_trans_int_raw	Transfer completion raw interrupt of the RX interrupt. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

RX_INT_STATUS

RX_INT_STATUS is an interrupt status register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x10A8	RX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo_lost_int_raw	reserved	rx_stop_int_status	reserved	rx_bfifo_full_int_status	rx_alfull_int_status	rx_full_int_status	rx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	rx_fifo_lost_int_raw	Status of the data full loss interrupt of the RX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	reserved	Reserved.
[5]	RO	rx_stop_int_status	Status of the stop interrupt of the RX interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	reserved	Reserved.
[3]	RO	rx_bfifo_full_int_status	Status of the bus FIFO overflow interrupt of the RC channel. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_alfull_int_status	Status of the DDR buffer almost full interrupt of the RX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_full_int_status	Status of the DDR buffer full interrupt of the RX interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_trans_int_status	Status of the transfer completion interrupt of the RX channel. 0: No interrupt is generated. 1: An interrupt is generated.

RX_INT_CLR

RX_INT_CLR is an interrupt clear register for the RX channel.

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Offset Address	Register Name	Total Reset Value
0x10AC	RX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo_lost_int_clear	reserved	rx_stop_int_clear	rx_ififo_full_int_clear	rx_bfifo_full_int_clear	rx_alfull_int_clear	rx_full_int_clear	rx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	WC	reserved	Reserved.
[7]	WC	rx_fifo_lost_int_clear	Data full loss interrupt clear for the RX channel. 0: not cleared 1: cleared
[6]	WC	reserved	Reserved.
[5]	WC	rx_stop_int_clear	Stop interrupt clear for the RX channel. 0: not cleared 1: cleared
[4]	WC	rx_ififo_full_int_clear	Interface FIFO overflow interrupt clear for the RX channel. 0: not cleared 1: cleared
[3]	WC	rx_bfifo_full_int_clear	Bus FIFO overflow interrupt clear for the RX channel. 0: not cleared 1: cleared
[2]	WC	rx_alfull_int_clear	DDR buffer almost full interrupt clear for the RX channel 0: not cleared 1: cleared
[1]	WC	rx_full_int_clear	DDR buffer full interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WO	rx_trans_int_clear	Transfer completion interrupt clear for the RX interrupt. 0: not cleared 1: cleared

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TX_IF_ATTRI

TX_IF_ATTRI is an interface attribute configuration register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2000	TX_IF_ATTRI	0xE400_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_sd3_sel		tx_sd2_sel		tx_sd1_sel		tx_sd0_sel		tx_sd_source_sel				reserved	tx_trackmode			tx_sd_offset								reserved	tx_underflow_ctrl	tx_ch_num		tx_i2s_precision		tx_mode	
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:30]	RW	tx_sd3_sel	SD3 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[29:28]	RW	tx_sd2_sel	SD2 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[27:26]	RW	tx_sd1_sel	SD1 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.

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[25:24]	RW	tx_sd0_sel	SD0 select. 00: SD0 01: SD1 10: SD2 11: SD3 **NOTE** Select the channel and data line in sequence.
[23:20]	RW	tx_sd_source_sel	Source select for SD0, SD1, SD2, and SD3. 0000: I^2S TX0 1000: I^2S RX0 Other values: reserved
[19]	RW	reserved	Reserved.
[18:16]	RW	tx_trackmode	Audio-left and audio-right channel mode in I^2S mode. 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** Trackmode is still valid in 1-channel TX mode.
[15:8]	RW	tx_sd_offset	Number of BCLK clocks delayed for data relative to the frame sync signal in PCM mode. 0x00: 0 bit clocks 0x01: 1 bit clock 0x02: 2 bit clocks … 0xFE: 254 bit clocks 0xFF: 255 bit clocks
[7]	RW	reserved	Reserved.
[6]	RW	tx_underflow_ctrl	Output control when an underflow occurs in the TX channel. 0: 0 is output. 1: The data at the last sampling point is output.

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[5:4]	RW	tx_ch_num	Number of TX channels. tx_multislot_en = 0 00: 1-channel TX 01: 2-channel TX 10: 6-channel TX 11: 8-channel TX Other values: reserved tx_multislot_en = 1 Number of TX channels in time-division multiplexing mode. 00: 2-channel TX 01: 4-channel TX 10: 8-channel TX 11: 16-channel TX **NOTE** • The data line must be SD0 for multi-channel TX. • The time-division multiplexing mode is not supported during transmission.
[3:2]	RW	tx_i2s_precision	Data sampling precision. I^2S normal mode: 00: reserved 01: 16 bits 10: 24 bits 11: reserved PCM normal mode: 00: 8 bits 01: 16 bits Other values: reserved
[1:0]	RW	tx_mode	Interface mode of the TX channel. 00: I^2S mode 01: PCM mode Other values: reserved

TX_DSP_CTRL

TX_DSP_CTRL is a TX channel control register.

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Offset Address	Register Name	Total Reset Value
0x2004	TX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		tx_disable_done	tx_enable	bypass_en	reserved			fade_out_rate				fade_in_rate				reserved	volume							reserved						mute_fade_en	mute_en
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29]	RO	tx_disable_done	TX channel stop/complete identifier. 0: not complete 1: complete
[28]	RW	tx_enable	TX channel start/stop indicator. 0: stop 1: start
[27]	RW	bypass_en	Operation bypass enable (the control function still takes effect). 0: disabled 1: enabled (the functions such as volume control, trackmode, and fade-in/fade-out are bypassed)
[26:24]	RW	reserved	Reserved.
[23:20]	RW	fade_out_rate	0000: The fade-out rate changes every one sampling point. 0001: The fade-out rate changes every two sampling points. 0110: The fade-out rate changes every four sampling points. 0011: The fade-out rate changes every eight sampling points. 0100: The fade-out rate changes every 16 sampling points. 0101: The fade-out rate changes every 32 sampling points. 0110: The fade-out rate changes every 64 sampling points. 0111: The fade-out rate changes every 128 sampling points. Other values: reserved

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[19:16]	RW	fade_in_rate	0000: The fade-in rate changes every one sampling point. 0001: The fade-in rate changes every two sampling points. 0010: The fade-in rate changes every four sampling points. 0011: The fade-in rate changes every eight sampling points. 0100: The fade-in rate changes every 16 sampling points. 0101: The fade-in rate changes every 32 sampling points. 0110: The fade-in rate changes every 64 sampling points. 0111: The fade-in rate changes every 128 sampling points. Other values: reserved
[15]	RW	reserved	Reserved.
[14:8]	RW	volume	Volume 0x00−0x28: mute 0x29: −80 dB … 0x7E: +5 dB 0x7F: +6 dB
[7:2]	RW	reserved	Reserved. This field can be used to control the volume precision. For example, the decimal places of the volume (in dB) can be controlled.
[1]	RW	mute_fade_en	Mute fade-in/fade-out control. 0: disabled 1: enabled
[0]	RW	mute_en	Mute control. 0: unmuted 1: muted

TX_DSP_STATUS

TX_DSP_STATUS is a TX channel status register.

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Offset Address	Register Name	Total Reset Value
0x2008	TX_DSP_STATUS	0x4000_0079

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_enable	tx_axi_afifo_rd_aempty	tx_if_afifo_wr_full	proc_256bit_done	if_fifo_wr_en	tx_dsp_stop_done_req	tx_rd_bus_fifo_cnt		state_clr_end	cur_fifo_id			cur_state				reserved								tx_axi_afifo_rd_empty	mute_fade_vol						
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31]	RO	tx_enable	TX enable. 0: disabled 1: enabled
[30]	RO	tx_axi_afifo_rd_aempty	Bus FIFO almost empty status of the current channel. 0: non-almost empty 1: almost empty
[29]	RO	tx_if_afifo_wr_full	Interface FIFO full status of the current channel. 0: not full 1: full
[28]	RO	proc_256bit_done	256-bit processing complete status of the current channel. 0: not complete 1: complete
[27]	RO	if_fifo_wr_en	Write interface FIFO enable for the current channel. 0: disabled 1: enabled
[26]	RO	tx_dsp_stop_done_req	DSP stop request for the current channel. 0: no request 1: request
[25:24]	RO	tx_rd_bus_fifo_cnt	Read bus FIFO counter. The FIFO is read twice each time.
[23]	RO	state_clr_end	Status clear complete. 0: not complete 1: complete
[22:19]	RO	cur_fifo_id	ID of the current channel.
[18:16]	RO	cur_state	Status of the state machine.
[15:8]	RO	reserved	Reserved.

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[7]	RO	tx_axi_afifo_rd_empty	Bus FIFO empty status of the current channel. 0: not empty 1: empty
[6:0]	RO	mute_fade_vol	Mute fade-in/fade-out volume. 0x00−0x28: mute 0x291: −80 dB … 0x7E1: +5 dB 0x7F: +6 dB

TX_IF_STATUS

TX_IF_STATUS is a TX control interface status register.

Offset Address	Register Name	Total Reset Value
0x200C	TX_IF_STATUS	0x0100_0060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	if_fifo_empty_cnt				reserved		i2s_tx_afifo_raddr	i2s_tx_afifo_rd_aempty	reserved						i2s_tx_afifo_waddr	i2s_tx_afifo_wr_afull	tx_bit_cnt								reserved	i2s_tx_ctrl_stop_done	i2s_tx_afifo_rd_empty	reserved			cur_state	
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	if_fifo_empty_cnt	Interface FIFO empty counter.
[27:26]	RO	reserved	Reserved.
[25]	RO	i2s_tx_afifo_raddr	Interface FIFO read address.
[24]	RO	i2s_tx_afifo_rd_aempty	Interface FIFO write almost empty.
[23:18]	RO	reserved	Reserved.
[17]	RO	i2s_tx_afifo_waddr	Interface FIFO write address.
[16]	RO	i2s_tx_afifo_wr_afull	Interface FIFO write almost full.
[15:8]	RO	tx_bit_cnt	TX bit counter
[7]	RO	reserved	Reserved.

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[6]	RO	i2s_tx_ctrl_stop_done	IF ctrl stop complete.
[5]	RO	i2s_tx_afifo_rd_empty	Interface FIFO empty.
[4:3]	RO	reserved	Reserved.
[2:0]	RO	cur_state	Status of the rx_if_ctrl state machine.

TX_DMAR_STATUS

TX_DMAR_STATUS is a TX DMAW status register.

Offset Address	Register Name	Total Reset Value
0x2010	TX_DMAR_STATUS	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		tx_fifo_raddr						reserved		tx_fifo_waddr						reserved	tx_fifo_full	state_clr_end	trans_finish_ind	vcmdready	vtrans	tx_buf_empty	tx_fifo_afull	reserved				cur_state			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:24]	RO	tx_fifo_raddr	Read pointer of the bus FIFO.
[23:22]	RO	reserved	Reserved.
[21:16]	RO	tx_fifo_waddr	Write pointer of the bus FIFO.
[15]	RO	reserved	Reserved.
[14]	RO	tx_fifo_full	Bus FIFO full.
[13]	RO	state_clr_end	Status clear complete.
[12]	RO	trans_finish_ind	Burst transfer complete. 0: not complete 1: complete
[11]	RO	vcmdready	Transfer command complete. 0: not complete 1: complete
[10]	RO	vtrans	Transfer command start.
[9]	RO	tx_buf_empty	Buffer empty.

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[8]	RO	tx_fifo_afull	Bus FIFO almost full.
[7:3]	RO	reserved	Reserved.
[2:0]	RO	cur_state	Status of the DMAR state machine.

TX_WS_CNT

TX_WS_CNT is a WS cyclic count status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2020	TX_WS_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ws_count																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RO	ws_count	FSCLK cyclic count register. The unit is FSCLK.

TX_BCLK_CNT

TX_BCLK_CNT is a BCLK cyclic count status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2024	TX_BCLK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bclk_count																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RO	bclk_count	BCLK cyclic count register. The unit is BCLK.

TX_BUFF_SADDR

TX_BUFF_SADDR is a DDR buffer start address register for the TX channel.

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Offset Address	Register Name	Total Reset Value
0x2080	TX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_buff_saddr	Start address for the DDR buffer of the TX channel. Its unit is byte. **NOTE** The start address must be 128x2-bit-aligned.

TX_BUFF_SIZE

TX_BUFF_SIZE is a DDR buffer size register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2084	TX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	tx_buff_size	DDR buffer size of the TX channel. Its unit is byte. **NOTE** The buffer size must be an integral multiple of 32 bytes.

TX_BUFF_WPTR

TX_BUFF_WPTR is a DDR buffer write address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2088	TX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_wptr																							

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Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	tx_buff_wptr	Write address for the DDR buffer of the TX channel. **NOTE** • The write address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The available space of the TX buffer must be greater than or equal to 32 bytes. • The software operation is performed by byte, and the hardware operation is performed by 32 bytes.

TX_BUFF_RPTR

TX_BUFF_RPTR is a DDR buffer read address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x208C	TX_BUFF_RPTR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_buff_rptr					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	tx_buff_rptr	Read address for the DDR buffer of the TX channel. **NOTE** • The read address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The address must be 128x2-bit-aligned.

TX_BUFF_ALEMPTY_TH

TX_BUFF_ALEMPTY_TH is a DDR buffer almost empty threshold register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2090	TX_BUFF_ALEMPTY_TH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_buff_alempty_th					

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Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	tx_buff_alempty_th	Almost empty threshold for the DDR buffer of the TX channel. Its unit is byte. If the available space of the DDR buffer is below the almost empty threshold, the almost empty raw interrupt is generated. **NOTE** If the tx_alempty_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x20.

TX_TRANS_SIZE

TX_TRANS_SIZE is a data transfer length register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2094	TX_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_trans_size					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:0]	RW	tx_trans_size	After the TX channel transmits the audio data with the length of tx_trans_size (in byte), a transfer completion interrupt is generated.

TX_RPTR_TMP

TX_RPTR_TMP is a read address storage register for the TX channel upon reporting of the transfer completion interrupt.

Offset Address	Register Name	Total Reset Value
0x2098	TX_RPTR_TMP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tx_rptr_tmp					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

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[23:0]	RO	tx_rptr_tmp	This field is used to save the read address for the TX channel when the transfer completion interrupt is reported.

TX_INT_ENA

TX_INT_ENA is an interrupt enable register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A0	TX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_ena	tx_mfade_int_ena	tx_stop_int_ena	tx_ififo_empty_int_ena	tx_bfifo_empty_int_ena	tx_alempty_int_ena	tx_empty_int_ena	tx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7]	RW	tx_dat_break_int_ena	Interface data break interrupt enable for the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	tx_mfade_int_ena	Mute fade-in/fade-output completion interrupt enable for the TX channel. 0: disabled 1: enabled
[5]	RW	tx_stop_int_ena	Stop interrupt enable for the TX channel. 0: disabled 1: enabled
[4]	RW	tx_ififo_empty_int_ena	Interface FIFO underflow interrupt enable for the TX channel. 0: disabled 1: enabled
[3]	RW	tx_bfifo_empty_int_ena	Bus FIFO underflow interrupt enable for the TX channel. 0: disabled 1: enabled

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[2]	RW	tx_alempty_int_ena	DDR buffer almost empty interrupt enable for the TX channel. 0: disabled 1: enabled
[1]	RW	tx_empty_int_ena	DDR buffer empty interrupt for the TX channel. 0: disabled 1: enabled
[0]	RW	tx_trans_int_ena	Transfer completion interrupt enable for the TX channel. 0: disabled 1: enabled

TX_INT_RAW

TX_INT_RAW is a raw interrupt register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A4	TX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_raw	tx_mfade_int_raw	tx_stop_int_raw	tx_ififo_empty_int_raw	tx_bfifo_empty_int_raw	tx_alempty_int_raw	tx_empty_int_raw	tx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	tx_dat_break_int_raw	Interface data break raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	tx_mfade_int_raw	Mute fade-in/fade-output completion raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RO	tx_stop_int_raw	Stop raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

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[4]	RO	tx_ififo_empty_int_raw	Interface FIFO underflow raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RO	tx_bfifo_empty_int_raw	Bus FIFO underflow raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	tx_alempty_int_raw	DDR buffer almost empty raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	tx_empty_int_raw	DDR buffer empty raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	tx_trans_int_raw	Transfer completion raw interrupt of the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.

TX_INT_STATUS

TX_INT_STATUS is an interrupt status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A8	TX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_status	tx_mfade_int_status	tx_stop_int_status	tx_ififo_empty_int_status	tx_bfifo_empty_int_status	tx_alempty_int_status	tx_empty_int_status	tx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	tx_dat_break_int_status	Status of the interface data break interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.

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[6]	RO	tx_mfade_int_status	Status of the mute fade-in/fade-output completion interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	tx_stop_int_status	Status of the stop interrupt of the TX interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	tx_ififo_empty_int_status	Status of the interface FIFO underflow interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_bfifo_empty_int_status	Status of the bus FIFO underflow interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	tx_alempty_int_status	DDR buffer almost empty interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_empty_int_status	Status of the DDR buffer empty interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	tx_trans_int_status	Status of the transfer completion interrupt of the TX channel. 0: No interrupt is generated. 1: An interrupt is generated.

TX_INT_CLR

TX_INT_CLR is an interrupt clear register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20AC	TX_INT_CLR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						tx_dat_break_int_clear	tx_mfade_int_clear	tx_stop_int_clear	tx_ififo_empty_int_clear	tx_bfifo_empty_int_clear	tx_alempty_int_clear	tx_empty_int_clear	tx_trans_int_clear

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Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	WC	tx_dat_break_int_clear	Interface data break interrupt clear for the TX channel. 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	WC	tx_mfade_int_clear	Mute fade-in/fade-output completion interrupt clear for the TX channel. 0: not cleared 1: cleared
[5]	WC	tx_stop_int_clear	Stop interrupt clear for the TX channel. 0: not cleared 1: cleared
[4]	WC	tx_ififo_empty_int_clear	Interface FIFO underflow interrupt clear for the TX channel. 0: not cleared 1: cleared
[3]	WC	tx_bfifo_empty_int_clear	Bus FIFO underflow interrupt clear for the TX channel. 0: not cleared 1: cleared
[2]	WC	tx_alempty_int_clear	DDR buffer almost empty interrupt clear for the TX channel. 0: not cleared 1: cleared
[1]	WC	tx_empty_int_clear	DDR buffer empty interrupt clear for the RX channel. 0: not cleared 1: cleared
[0]	WC	tx_trans_int_clear	Transfer completion interrupt clear for the TX channel. 0: not cleared 1: cleared

12.2 Audio CODEC

12.2.1 Overview

The Hi3516A is integrated with high-performance audio CODECs, including high-quality stereo playback DAC (96 dB DR A-weighted), single-ended line out; high-quality stereo recording ADC (90 dB DR A-weighted), two single-ended stereo inputs; –16.5 dB to 56 dB MIC input, and analog gain control at 1.5 dB step. The I^2S data interface supports a standard

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sampling frequency ranging from 8 kHz to 192 kHz. It can work at two sampling frequencies at the same time. It also supports digital audio mixing.

12.2.2 Features

The audio CODEC module has the following features:

- 96 dBA DR stereo DAC
- Single-ended stereo line out
- DAC digital volume control range: –121 dB to +6 dB, at 1 dB step
- 90 dBA DR stereo ADC
- Analog volume control range of ADC channel: –16.5 dB to 56 dB, at 1.5 dB step
- Digital volume control range of ADC channel: –96 dB to 30 dB, at 1 dB step
- Two alternative single-ended stereo inputs
- Provides internal MIC biasing
- Master and slave I^2S data interfaces, supporting 24 bits, 20 bits, 18 bits, and 16 bits, in binary format
- Audio sampling frequencies: 48 kHz, 44.1 kHz, and 32 kHz

  The sampling frequencies of each series are as follows:
  - The 32 kHz sampling frequencies series include 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz.
  - The 44.1 kHz sampling frequencies series include 11.025 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, and 176.4 kHz. The 48 kHz sampling frequencies series include 12 kHz, 24 kHz, 48 kHz, 96 kHz, and 192 kHz.
- The jitter tolerance of the analog clock CLKIN is 300 ps RMS.

12.2.3 Function Description

The audio CODEC module provides the recording and playing function. In the case of audio recording, analog signals are input from the MIC or line-in end, the gain is amplified at the analog part, and the signals converted into digital signals and output from the I^2S interface. Stereo recording is supported. In the case of playback, audio signals are input through the I^2S interface, converted into analog signals by the DAC, and then output. Stereo playing is supported.

Recording Mode

In recording mode, the MIC or line-in signals are input from the analog input end, processed by using the programmable gain method, converted by the ADC, filtered and volume-adjusted at the digital part, and finally output from the I^2S interface. Then, the entire recording procedure is complete.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Input analog audio signals to start recording. Signals are then output from the I^2S interface.

----End

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Playing Mode

In playing mode, audio signals are transmitted from the I^2S interface to the DAC digital part for filtering and volume control, filtering is performed at the analog part, and finally output by the lineout end.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Transmit signals from the I^2S interface, and then output analog audio signals from the lineout end.

----End

12.2.4 Register Summary

The audio CODEC is controlled by using the registers of the system controller with the base address 0x2012_0000. The offset addresses of these registers are 0x00C8, 0x00CC, 0x00D0, 0x00D4 and 0x00D8. That is, no interface is provided for controlling the audio CODEC.

12.2.5 Register Description

For details about the registers related to the audio CODEC, see section 3.5.5.1 "Register Summary" and section 3.5.5.2 "Register Description."

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Contents

13 Peripherals 13-1
13.1 I²C Controller 13-1
13.1.1 Overview 13-1
13.1.2 Function Description 13-1
13.1.3 Operating Mode 13-1
13.1.4 Register Summary 13-4
13.1.5 Register Description 13-5
13.2 UART 13-27
13.2.1 Overview 13-27
13.2.2 Features 13-28
13.2.3 Function Description 13-28
13.2.4 Operating Mode 13-29
13.2.5 Register Summary 13-32
13.2.6 Register Description 13-33
13.3 SPI 13-45
13.3.1 Overview 13-45
13.3.2 Features 13-45
13.3.3 Function Description 13-46
13.3.4 Peripheral Bus Timings 13-47
13.3.5 Operating Mode 13-54
13.3.6 Register Summary 13-56
13.3.7 Register Description 13-57
13.4 MMC/SD/SDIO Controller 13-66
13.4.1 Function Description 13-66
13.4.2 Application Notes 13-73
13.4.3 Register Summary 13-86
13.4.4 Register Description 13-88
13.5 IR Interface 13-116
13.5.1 Overview 13-116
13.5.2 Features 13-116
13.5.3 Function Description 13-117
13.5.4 Operating Mode 13-125

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13.5.5 Register Summary 13-127
13.5.6 Register Description 13-128
13.6 GPIO 13-143
13.6.1 Overview 13-143
13.6.2 Features 13-144
13.6.3 Operating Mode 13-144
13.6.4 Register Summary 13-146
13.6.5 Register Description 13-147
13.7 USB 2.0 Host 13-152
13.7.1 Overview 13-152
13.7.2 Function Description 13-152
13.7.3 Operating Mode 13-155
13.7.4 Register Summary 13-157
13.7.5 Register Description 13-160
13.8 LSADC_CTRL 13-242
13.8.1 Overview 13-242
13.8.2 Features 13-242
13.8.3 Operating Mode 13-242
13.8.4 Register Summary 13-245
13.8.5 Register Description 13-245
13.9 PWM 13-251
13.9.1 Overview 13-251
13.9.2 Features 13-251
13.9.3 Operating Mode 13-251
13.9.1 Register Summary 13-252
13.9.2 Register Description 13-253

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Figures

Figure 13-1 Process of receiving data by a single operation through the I^2C master 13-2
Figure 13-2 Process of continuously receiving and transmitting data by the I^2C master..... 13-3
Figure 13-3 Typical application block diagram of the UART..... 13-28
Figure 13-4 Frame format of the UART 13-29
Figure 13-5 Application block diagram when the SPI is connected to a single slave device 13-46
Figure 13-6 SPI single frame format (SPO = 0, SPH = 0)..... 13-47
Figure 13-7 SPI continuous frame format (SPO = 0, SPH = 0)..... 13-47
Figure 13-8 SPI single frame format (SPO = 0, SPH = 1)..... 13-48
Figure 13-9 SPI continuous frame format (SPO = 0, SPH = 1)..... 13-48
Figure 13-10 SPI single frame format (SPO = 1, SPH = 0)..... 13-49
Figure 13-11 SPI continuous frame format (SPO = 1, SPH = 0) 13-49
Figure 13-12 SPI single frame format (SPO = 1, SPH = 1)..... 13-50
Figure 13-13 SPI continuous frame format (SPO = 1, SPH = 1)..... 13-50
Figure 13-14 SPI timings..... 13-51
Figure 13-15 TI synchronous serial single frame format 13-51
Figure 13-16 TI synchronous serial continuous frame format 13-52
Figure 13-17 National semiconductor microwire single frame format..... 13-52
Figure 13-18 National semiconductor microwire continuous frame format..... 13-53
Figure 13-19 Functional block diagram of the MMC controller 13-66
Figure 13-20 Typical application circuit of the MMC controller..... 13-67
Figure 13-21 Format of an MMC command..... 13-68
Figure 13-22 Format of the response to an MMC command..... 13-69
Figure 13-23 Operations by running an MMC non-data transfer command..... 13-69
Figure 13-24 Single-block and multi-block read operations..... 13-70
Figure 13-25 Single-block and multi-block write operations 13-71
Figure 13-26 Data transfer format in 1-bit mode 13-72

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Figure 13-27 Data transfer format in 4-bit mode 13-72

Figure 13-28 Structure of the dual-buffer descriptor 13-80

Figure 13-29 Structure of the linked descriptor 13-80

Figure 13-30 Internal structure of 32-bit descriptors 13-81

Figure 13-31 Frame format for transmitting a single NEC with simple repeat code 13-119

Figure 13-32 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously 13-119

Figure 13-33 Definitions of bit0 and bit1 of the NEC with simple repeat code 13-120

Figure 13-34 Format for transmitting a single NEC with simple repeat code 13-120

Figure 13-35 Code format for transmitting consecutive NEC with simple repeat codes 13-120

Figure 13-36 Frame format for transmitting a single NEC with full repeat code 13-121

Figure 13-37 Frame format for transmitting NEC with full repeat codes by pressing the key continuously 13-121

Figure 13-38 Definitions of bit0 and bit1 of the NEC with full repeat code 13-121

Figure 13-39 Format for transmitting a single NEC with full repeat code 13-121

Figure 13-40 Frame format for transmitting a single TC9012 code 13-122

Figure 13-41 Frame format for transmitting TC9012 codes by pressing the key continuously 13-122

Figure 13-42 Definitions of bit0 and bit1 of the TC9012 code 13-123

Figure 13-43 Format for transmitting a single TC9012 code 13-123

Figure 13-44 Format for transmitting consecutive TC9012 codes (C0 = 1) 13-123

Figure 13-45 Format for transmitting consecutiveTC9012 codes (C0 = 0) 13-123

Figure 13-46 Frame format for transmitting a single SONY code 13-124

Figure 13-47 Frame format for continuously transmitting SONY codes by pressing the key 13-124

Figure 13-48 Definitions of bit0 and bit1 of a SONY code 13-124

Figure 13-49 Process of initializing the IR module 13-125

Figure 13-50 Process of reading the decoded data 13-126

Figure 13-51 Logic block diagram of the USB 2.0 host controller 13-152

Figure 13-52 Logic block diagram of the USB 2.0 device controller 13-153

Figure 13-53 Reference design of the USB 2.0 host controller 13-154

Figure 13-54 Single scanning procedure 13-243

Figure 13-55 Channel polling in continuous scanning mode 13-243

Figure 13-56 Continuous scanning procedure 13-244

Figure 13-57 Low-power timing 13-244

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Tables

Table 13-1 Summary of I^2C registers (base addresses 0x200D_0000, 2024_0000, and 0x2025_0000 for I^2C0, I^2C1, and I^2C2 respectively.) 13-4

Table 13-2 Summary of UART registers 13-32

Table 13-3 Timing parameters of the SPI 13-51

Table 13-4 Summary of SPI registers 13-56

Table 13-5 Load parameters of signal lines 13-68

Table 13-6 Transmission mode 13-72

Table 13-7 Default values of MMC_CMD when a non-data transfer command is executed 13-76

Table 13-8 Default values of MMC_CMD when a single data block or multiple data blocks are read. 13-77

Table 13-9 Default values of MMC_CMD when a single data block or multiple data blocks are written 13-79

Table 13-10 Definition of each bit of DES0 13-81

Table 13-11 Definition of each bit of DES1 13-82

Table 13-12 Definition of each bit of DES2 13-82

Table 13-13 Definition of each bit of DES3 13-82

Table 13-14 Reference configuration of MMC_CMDARG when the resume operation is performed . 13-85

Table 13-15 Summary of MMC registers (the base address for SDIO0 is 0x206e_0000 and for SDIO1 is 0x206f_0000) 13-86

Table 13-16 Code formats of the received infrared data (NEC with simple repeat code) 13-117

Table 13-17 Code formats of the received infrared data (NEC with full repeat code) 13-118

Table 13-18 Code formats of the received infrared data (TC9012 code and SONY code) 13-118

Table 13-19 Summary of IR registers (base address: 0x2007_0000) 13-127

Table 13-20 Base addresses for 16 groups of GPIO registers 13-146

Table 13-21 Summary of GPIO registers 13-147

Table 13-22 Variables in the offset addresses for USB 2.0 registers 13-156

Table 13-23 Summary of USB 2.0 registers (base address: 0x1004_0000) 13-157

Table 13-24 USB device register overview (base address: 0x1008_0000) 13-157

Table 13-25 Summary of LSADC_CRTL registers (base address: 0x200B_0000) 13-245

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Table 13-26 Base addresses for the registers of PWM*n* 13-252

Table 13-27 Summary of PWM0 registers (base address: 0x2013_0000) 13-253

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13 Peripherals

13.1 I²C Controller

13.1.1 Overview

The inter-integrated circuit (I^2C) module is used to read or write to the slave device connected on the I^2C bus through the CPU. When writing data to and reading data from the slave device, the CPU configures the I^2C configuration register over the bus and transmits the control information and the data to be used to the I^2C data communication register. After parsing the commands, the I^2C module transmits the data of the data channel register to the slave device over I^2C bus and notifies the CPU of the final status to the CPU by using interrupts after transmitting the data. The CPU reads data from the slave device in the similar way.

13.1.2 Function Description

The I^2C module has the following features:

- The Hi3516A provides the master I^2C interface. The working reference clock of the I^2C module is the 1/4 of the bus clock.
- Supports the bus arbitration in the case of multiple master devices.
- Supports clock synchronization and bit and byte waiting.
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- CBUS components are not supported.
- Supports the DMA operation.

13.1.3 Operating Mode

Process of Receiving and Transmitting Data by a Single Operation through the I²C Master

Figure 13-1 shows the process of receiving data by a single operation through the I^2C master.

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Figure 13-1 Process of receiving data by a single operation through the I²C master

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Process of Continuously Receiving and Transmitting Data by the I²C Master

Figure 13-2 shows process of continuously receiving and transmitting data by the I²C master.

Figure 13-2 Process of continuously receiving and transmitting data by the I²C master

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13.1.4 Register Summary

The Hi3516A contains three I^{2}C modules and Table 13-1 describes I^{2}C registers.

Table 13-1 Summary of I^{2}C registers (base addresses 0x200D_0000, 2024_0000, and 0x2025_0000 for I^{2}C0, I^{2}C1, and I^{2}C2 respectively.)

Offset Address	Register	Description	Page
0x000	I2C_CON	I^{2}C control register	13-5
0x004	I2C_TAR	I^{2}C access slave device address register	13-6
0x010	I2C_DATA_CMD	I^{2}C data operation register	13-6
0x01C	I2C_SCL_HCNT	I2C_SCL high level configuration register	13-7
0x020	I2C_SCL_LCNT	I2C_SCL low level configuration register	13-8
0x02C	I2C_INTR_STAT	I^{2}C masked interrupt status register	13-8
0x030	I2C_INTR_MASK	I^{2}C interrupt mask register	13-10
0x034	I2C_INTR_RAW	I^{2}C raw interrupt status register	13-11
0x038	I2C_RX_TL	RX_FIFO threshold configuration register	13-13
0x03C	I2C_TX_TL	TX_FIFO threshold configuration register	13-14
0x040	I2C_CLR_INTR	I^{2}C interrupt clear register	13-14
0x06C	I2C_ENABLE	I^{2}C enable register	13-15
0x070	I2C_STATUS	I^{2}C status register	13-15
0x074	I2C_TXFLR	TX_FIFO valid data indicator register	13-16
0x078	I2C_RXFLR	RX_FIFO valid data indicator register	13-16
0x07C	I2C_SDA_HOLD	SDA hold time register	13-17
0x080	I2C_TX_ABRT_SRC	I^{2}C TX failure interrupt source register	13-17
0x088	I2C_DMA_CR	I^{2}C DMA interface control register	13-20
0x08C	I2C_DMA_TDLR	TX_FIFO DMA operation threshold register	13-20
0x090	I2C_DMA_RDLR	RX_FIFO DMA operation threshold register	13-21
0x0A0	I2C_SCL_SWITCH	I^{2}C anti-suspend enable register	13-21
0x0A4	I2C_SCL_SIM	I^{2}C anti-suspend analog register	13-22

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Offset Address	Register	Description	Page
0x0AC	I2C_LOCK	I^2C lock register	13-23
0x00B0	I2C_MST_SINGLE_CTRL	I2C_MST_SINGLE_CTRL register	13-23
0x00B4	I2C_MST_SINGLE_CMD	I2C_MST_SINGLE_CMD register	13-25
0x00B8	I2C_SEQUENCE_CMD0	I2C_SEQUENCE_CMD0 register	13-25
0x00BC	I2C_SEQUENCE_CMD1	I2C_SEQUENCE_CMD1 register	13-27
0x00C0	I2C_SEQUENCE_CMD2	I2C_SEQUENCE_CMD2 register	13-27

13.1.5 Register Description

I2C_CON

I2C_CON is an I^2C control register.

Offset Address	Register Name	Total Reset Value
0x000	I2C_CON	0x0000_0065

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									reserved	restart_en	reserved	reserved			reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RW	restart_en	Restart command TX enable in master mode 0: disabled 1: enabled **NOTE** If the Restart function is disabled, the following functions are not supported: 1. Sending the start bit 2. High-speed mode 3. Read operation in 10-bit addressing mode 4. Combined addressing mode
[4]	RO	reserved	Reserved
[3:1]	RO	reserved	Reserved

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[0]	RO	reserved	Reserved

I2C_TAR

I2C_TAR is an I^{2}C access slave device address register.

Offset Address	Register Name	Total Reset Value
0x004	I2C_TAR	0x0000_002C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			master_10bit	special	gc_or_start	i2c_tar									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	master_10bit	Address length in master mode 0: 7 bits 1: 10 bits
[11]	RW	special	General call or start byte function enable 0: disabled 1: enabled
[10]	RW	gc_or_start	I^{2}C command to be executed when the Special bit is 1 0: general call command (After the general call command is sent, you can perform only write operations. If you perform read operations, tx_abort interrupt is triggered. For details about the definition, see the I2C_TX_ABRT_SOURCE bit[9].) 1: start byte command
[9:0]	RW	i2c_tar	Slave address that is accessed by the I^{2}C when I^{2}C acts as a master device **NOTE** If the address length of the slave device is set to 7 bits, only bit [6:0] are valid.

I2C_DATA_CMD

I2C_DATA_CMD is an I^{2}C data operation register.

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Offset Address	Register Name	Total Reset Value
0x010	I2C_DATA_CMD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5 4	3 2 1 0
Name	reserved						reserved	data	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	reserved	Reserved
[7:0]	RW	data	Data to be transmitted or received through the I^2C bus Read: The data received from the I^2C bus is read. Write: The written data is transmitted to the I^2C.

I2C_SCL_HCNT

I2C_SCL_HCNT is an I2C_SCL high level configuration register

Offset Address	Register Name	Total Reset Value
0x01C	I2C_SCL_HCNT	0x0000_0010

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				i2c_scl_hcnt			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_fs_scl_hcnt	Number of SCL clock high-level cycles. The unit is the I^2C working frequency i2c_clk (50 MHz in normal mode). **NOTE** 1. The field must be configured to obtain the appropriate I/O timing before data is transmitted through the I2C bus. 2. You can perform write operations only when the I2C interface is disabled (I2C_ENABLE = 0).

The following example assumes that the I^2C reference working clock is 50 MHz, i2c_scl_hcnt is set to *m*, and the SCL high-level period is DelTim. DelTim is calculated as follows:

Deltim = (1/50) x (*m* + 1), (in μs)

If the required SCL high-level period is 5 μs, the value *m* of i2c_scl_hcnt is:

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$m = (5 \times 50) - 1 = 249$

As the I^2C reference working clock is 50 MHz, the maximum SCL high-level period is 1310.72 µs.

I2C_SCL_LCNT

I2C_SCL_LCNT is an I2C_SCL low level configuration register.

Offset Address	Register Name	Total Reset Value
0x020	I2C_SCL_LCNT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_scl_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_scl_lcnt	Number of SCL clock low-level cycles. The unit is the I^2C working frequency i2c_clk (50 MHz in normal mode). **NOTE** 1. The field must be correctly configured to obtain the appropriate I/O timing before data is transmitted through the I^2C bus. 2. You can perform write operations only when the I^2C interface is disabled (I2C_ENABLE = 0).

The following example assumes that the I^2C reference working clock is 50 MHz, i2c_scl_lcnt is set to *m*, and the SCL low-level period is DelTim. DelTim is calculated as follows:

Deltim =(1/50) x (*m* + 1), (in µs)

If the required SCL low-level period is 5 µs, the value m of i2c_scl_lcnt is:

$m = (5 \times 50) - 1 = 249$

As the I^2C reference working clock is 50 MHz, the maximum SCL low-level period is 1310.72 µs.

I2C_INTR_STAT

I2C_INTR_STAT is an interrupt status register after the I^2C is masked.

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Offset Address	Register Name	Total Reset Value
0x02C	I2C_INTR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RO	gen_call	Status of the interrupt indicating that a general call request is received 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	start_det	Status of the start detect interrupt indicating the I^2C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	stop_det	Status of the start detect interrupt indicating the I^2C bus interface has the STOP condition 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	activity	Activity interrupt status. The I^2C activity status is recorded until the interrupt is cleared. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	reserved	Reserved
[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Status of the interrupt indicating that TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

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[2]	RO	rx_full	Status of the interrupt indicating that RX_FIFO reaches or is above the threshold 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_under	Read data overflow (that is, the CPU reads the FIFO when RX_FIFO is empty) interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

I2C_INTR_MASK

I2C_INTR_MASK is an I^2C interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x030	I2C_INTR_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call_mask	start_det_mask	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	gen_call_mask	Interrupt mask when a general call request is received 0: not masked 1: masked
[10]	RW	start_det_mask	Start detect interrupt mask 0: not masked 1: masked
[9]	RW	stop_det	Stop detect interrupt mask 0: not masked 1: masked
[8]	RW	activity	Activity interrupt mask 0: not masked 1: masked

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[7]	RO	reserved	Reserved
[6]	RW	tx_abrt	TX abort interrupt mask 0: not masked 1: masked
[5]	RO	reserved	Reserved
[4]	RW	tx_empty	Interrupt mask when TX_FIFO reaches or is below the threshold 0: not masked 1: masked
[3]	RW	tx_over	TX_FIFO overflow interrupt mask 0: not masked 1: masked
[2]	RW	rx_full	Interrupt mask when RX_FIFO reaches or is below the threshold 0: not masked 1: masked
[1]	RW	rx_over	RX_FIFO overflow interrupt mask 0: not masked 1: masked
[0]	RW	rx_under	Interrupt mask when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: not masked 1: masked

I2C_INTR_RAW

I2C_INTR_RAW is an I^{2}C raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x034	I2C_INTR_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

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[11]	RO	gen_call	Interrupt status when a general call request is received 0: No interrupt is generated. 1: The slave receives the general call. **NOTE** This bit is set to 1 only when the general call request is received and confirmed. This value is retained unless being cleared.
[10]	RO	start_det	Start detect interrupt status, indicating whether the I^2C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: The START or RESTART condition is detected.
[9]	RO	stop_det	Stop detect interrupt status, indicating whether the I^2C bus interface has the STOP condition 0: No interrupt is generated. 1: The STOP condition is detected.
[8]	RO	activity	Activity interrupt status. The I^2C activity status is recorded until the interrupt is cleared. 0: idle 1: busy
[7]	RO	reserved	Reserved
[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason for sending the interrupt. If this bit is set to a value, the I^2C clears TX_FIFO. TX_FIFO remains in this state until the interrupt is cleared. After the interrupt is cleared, TX_FIFO reads more data over the APB interface.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Interrupt status when TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When data amount of TX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, TX_FIFO is cleared.
[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

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[2]	RO	rx_full	Interrupt status when RX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 when RX_FIFO reaches or is below the threshold set by I2C_RX_TL. When RX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, RX_FIFO and this interrupt are automatically cleared.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 if RX_FIFO is full but still receives bytes from the external I^2C device. The I^2C responds to data received over the I^2C bus. However, bytes received after RX_FIFO is full are lost.
[0]	RO	rx_under	Interrupt status when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: No interrupt is generated. 1: An interrupt is generated.

I2C_RX_TL

I2C_RX_TL is an RX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x038	I2C_RX_TL	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	rx_tl	RX_FIFO threshold **NOTE** Valid values: 0–15. The actual value is the configured value plus 1. An rx_full interrupt is triggered when the number of data items in RX_FIFO is greater than or equal to the value. The upper threshold is configured as the RX_FIFO depth by default if the configured value is greater than the RX_FIFO depth.

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I2C_TX_TL

I2C_TX_TL is a TX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x03C	I2C_TX_TL	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	tx_tl	TX_FIFO threshold **NOTE** Valid values: 0–15. The actual value is equal to the configured value. A tx_empty interrupt is triggered when the amount of data in TX_FIFO is smaller than or equal to the value. The upper threshold is configured as the TX_FIFO depth by default if the configured value is greater than the TX_FIFO depth.

I2C_CLR_INTR

I2C_CLR_INTR is an I^2C interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x040	I2C_CLR_INTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clr_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	clr_intr	Combined interrupts, all independent interrupts, and the I2C_TX_ABRT_SOURCE register are cleared when 1 is written to this bit. This bit clears only software interrupts that can be cleared. The I2C_TX_ABRT_SOURCE register can be cleared by referring to I2C_TX_ABRT_SOURCE[abrt_sbyte_norstrt].

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I2C_ENABLE

I2C_ENABLE is an I^{2}C enable register.

Offset Address	Register Name	Total Reset Value
0x06C	I2C_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	enable	I^{2}C enable 0: disabled 1: enabled

I2C_STATUS

I2C_STATUS is an I^{2}C status register.

Offset Address	Register Name	Total Reset Value
0x070	I2C_STATUS	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									reserved	mst_activity	rx_fifo_full	rx_fifo_nempty	tx_fifo_nempty	tx_fifo_full	i2c_activity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RO	mst_activity	I^{2}C master activity status 0: The master enters the idle state, and the I^{2}C is deactivated. 1: The master does not enter the idle state, and the I^{2}C is activated.
[4]	RO	rx_fifo_full	RX_FIFO full flag 0: not full 1: full

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[3]	RO	rx_fifo_nempty	RX_FIFO non-empty flag 0: empty 1: non-empty
[2]	RO	tx_fifo_nempty	TX_FIFO empty flag 0: non-empty 1: empty
[1]	RO	tx_fifo_full	TX_FIFO non-full flag 0: full 1: not full
[0]	RO	i2c_activity	I^2C operating status 0: idle 1: active

I2C_TXFLR

I2C_TXFLR is a TX_FIFO valid data indicator register.

Offset Address	Register Name	Total Reset Value
0x074	I2C_TXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	tx_flr	Number of valid data items in TX_FIFO The register is cleared when the I^2C is disabled (I2C_CONF bit[0] set to 0) or a tx_abort interrupt is generated.

I2C_RXFLR

I2C_RXFLR is an RX_FIFO valid data indicator register.

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Offset Address	Register Name	Total Reset Value
0x078	I2C_RXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	rx_flr	Number of valid data items in RX_FIFO The register is cleared when the I^2C is disabled (I2C_CONF bit[0] is set to 0) or a tx_abort interrupt is generated.

I2C_SDA_HOLD

I2C_SDA_HOLD is an SDA hold time register.

Offset Address	Register Name	Total Reset Value
0x07C	I2C_SDA_HOLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sda_hold_fs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sda_hold_fs	SDA hold time. The unit is the I^2C working frequency i2c_clk (50 MHz in normal mode). **NOTE** This bit indicates the delay from the SCL falling edge to SDA change. The SDA changes after the SCL falling edge and the delay (value of sda_hold_fs x cycle of i2c_clk). **NOTE** This bit must be set based on the speed mode.

I2C_TX_ABRT_SRC

I2C_TX_ABRT_SRC is an I^2C TX failure interrupt source register.

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Offset Address	Register Name	Total Reset Value
0x080	I2C_TX_ABRT_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved	reserved	reserved	arb_lost	reserved	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	reserved	abrt_sbyte_ackdet	reserved	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	reserved	Reserved
[14]	RO	reserved	Reserved
[13]	RO	reserved	Reserved
[12]	RO	arb_lost	Whether an error occurs after the master loses the bus control permission 0: No error occurs. 1: An error occurs. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[11]	RO	reserved	Reserved
[10]	RO	abrt_10b_rd_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and the master attempts to initiate a read operation in 10-bit mode 0: No error occurs. 1: An error occurs. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[9]	RO	abrt_sbyte_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and a user attempts to initiate a start operation 0: No error occurs. 1: An error occurs. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[8]	RO	reserved	Reserved

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[7]	RO	abrt_sbyte_ackdet	Whether an error occurs when the master sends a start command and receives a response 0: No error occurs. 1: An error occurs. (The slave does not need to respond to the start command.) **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[6]	RO	reserved	Reserved
[5]	RO	abrt_gcall_read	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request, but the user initiates a read operation after the request. **NOTE** This bit is cleared together with the tx_abort interrupt.
[4]	RO	abrt_gcall_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request but does not receive a response from the slave over the bus. **NOTE** This bit is cleared together with the tx_abort interrupt.
[3]	RO	abrt_txdata_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: After the master sends an address and receives a response from the slave, the master sends data to the slave but does not receive any response. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[2]	RO	abrt_10addr2_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[10:8] the second time but does not receive any response from the slave when the master operates in 10-bit mode. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.

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[1]	RO	abrt_10addr1_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[7:0] the first time but does not receive any response from the slave when the master operates in 10-bit mode. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.
[0]	RO	abrt_7b_addr_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends an address but does not receive the response from any slave on the bus when the master operates in 7-bit mode. **NOTE** This bit is cleared when the I2C_CLR_INTR register or the I2C_CLR_TX_ABRT register is read.

I2C_DMA_CR

I2C_DMA_CR is an I^2C DMA interface control register.

Offset Address	Register Name	Total Reset Value
0x088	I2C_DMA_CR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rdmae	tdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rdmae	DMA enable for the TX FIFO 0: disabled 1: enabled
[0]	RW	tdmae	DMA enable for the RX FIFO 0: disabled 1: enabled

I2C_DMA_TDLR

I2C_DMA_TDLR is a TX_FIFO DMA operation threshold register.

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Offset Address	Register Name	Total Reset Value
0x08C	I2C_DMA_TDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_txtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_txtl	TX FIFO DMA threshold. When the number of data items of the TX FIFO is smaller than or equal to this value, a DMA operation request is sent. The DMA moves data to the TX FIFO.

I2C_DMA_RDLR

I2C_DMA_RDLR is an RX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x090	I2C_DMA_RDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_rxtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_rxtl	RX FIFO DMA threshold. When the number of data items of the TX FIFO is greater than or equal to this value, a DMA operation request is sent. The DMA moves data of the RX FIFO to the specified destination. The actual value is equal to the configured value plus 1.

I2C_SCL_SWITCH

I2C_SCL_SWITCH is an I^2C anti-suspend enable register.

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Offset Address	Register Name	Total Reset Value
0x0A0	I2C_SCL_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_switch	Master simulate SCL signal enable 0: disabled 1: enabled

I2C_SCL_SIM

I2C_SCL_SIM is an I^2C anti-suspend analog register.

Offset Address	Register Name	Total Reset Value
0x0A4	I2C_SCL_SIM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_sim
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_sim	SCL enable signals simulated by the master 0: The output SCL is 0. 1: The output SCL is 1.

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I2C_LOCK

I2C_LOCK is an I^{2}C lock register.

Offset Address	Register Name	Total Reset Value
0x0AC	I2C_LOCK	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															i2c_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	i2c_lock	I^{2}C lock register. To unlock the register, write 1ACCE551 to the register. To lock the register, write other values. When this register is read: 0: The register is unlocked, and all registers can be configured. 1: The register is locked, and only this register can be configured.

I2C_MST_SINGLE_CTRL

I2C_MST_SINGLE_CTRL is an I2C_MST_SINGLE_CTRL register.

Offset Address	Register Name	Total Reset Value
0x00B0	I2C_MST_SINGLE_CTRL	0x0030_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_model_en	single_model	single_addr_model	single_data_model	single_mst_tx_abrt_clr	single_tx_cmd_fifo_over_clr	single_rx_cmd_fifo_under_clr	single_rx_cmd_fifo_over_clr	single_mst_tx_abrt	single_tx_cmd_fifo_over	single_tx_cmd_fifo_not_full	single_tx_cmd_fifo_empty	reserved				single_tx_cmd_fifo_cnt				single_rx_cmd_fifo_under	single_rx_cmd_fifo_over	single_rx_cmd_fifo_full	single_rx_cmd_fifo_not_empty	reserved				single_rx_cmd_fifo_cnt			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	single_model_en	I^{2}C master single operation enable control 0: disabled 1: enabled

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[30]	RW	single_model	I^2C master single operation mode control 0: write 1: read
[29]	RW	single_addr_model	I^2C master single operation address mode control 0: The slave register has an 8-bit address width. 1: The slave register has a 16-bit address width.
[28]	RW	single_data_model	I^2C master single operation data mode control 0: The slave register has an 8-bit data width. 1: The slave register has a 16-bit data width.
[27]	WC	single_mst_tx_abrt_clr	Transmission failure indicator clear in single-operation mode
[26]	WC	single_tx_cmd_fifo_over_clr	SINGLE_TX_FIFO overflow indicator clear
[25]	WC	single_rx_cmd_fifo_under_clr	SINGLE_RX_FIFO read data overflow indicator clear
[24]	WC	single_rx_cmd_fifo_over_clr	SINGLE_RX_FIFO overflow indicator clear
[23]	RO	single_mst_tx_abrt	Transmission failure indicator in single-operation mode 0: No transmission failures occur. 1: A transmission failures occurs.
[22]	RO	single_tx_cmd_fifo_over	SINGLE_TX_FIFO overflow indicator 0: Data in SINGLE_TX_FIFO does not overflow. 1: Data in SINGLE_TX_FIFO overflows.
[21]	RO	single_tx_cmd_fifo_not_full	SINGLE_TX_FIFO non-full indicator 0: SINGLE_TX_FIFO is full. The FIFO has at least 16 data items. 1: SINGLE_TX_FIFO is not full. The FIFO has less than 16 data items.
[20]	RO	single_tx_cmd_fifo_empty	SINGLE_TX_FIFO empty indicator 0: There is data in the FIFO. 1: There is no data in the FIFO.
[19:17]	RO	reserved	Reserved
[16:12]	RO	single_tx_cmd_fifo_cnt	Number of valid data items in SINGLE_TX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL bit[31] set to 0).
[11]	RO	single_rx_cmd_fifo_under	Overflow status when read data overflows (The CPU reads the FIFO when SINGLE_RX_FIFO is empty.) 0: No read data overflows. 1: Read data overflows.

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[10]	RO	single_rx_cmd_fifo_over	SINGLE_RX_FIFO overflow status 0: Data in SINGLE_RX_FIFO does not overflow. 1: Data in SINGLE_RX_FIFO overflows.
[9]	RO	single_rx_cmd_fifo_full	SINGLE_RX_FIFO full indicator 0: SINGLE_RX_FIFO is not full. The FIFO has less than 16 data items. 1: SINGLE_RX_FIFO is full. The FIFO has at least 16 data items.
[8]	RO	single_rx_cmd_fifo_not_empty	SINGLE_RX_FIFO non-empty indicator 0: There is no data in the FIFO. 1: There is data in the FIFO.
[7:5]	RO	reserved	Reserved
[4:0]	RO	single_rx_cmd_fifo_cnt	Number of valid data items in SINGLE_RX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL bit[31] set to 0).

I2C_MST_SINGLE_CMD

I2C_MST_SINGLE_CMD is an I2C_MST_SINGLE_CMD register.

Offset Address	Register Name	Total Reset Value
0x00B4	I2C_MST_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_addr																single_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	WO	single_addr	Address of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.
[15:0]	RW	single_data	Data of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD0

I2C_SEQUENCE_CMD0 is an I2C_SEQUENCE_CMD0 register.

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Offset Address	Register Name	Total Reset Value
0x00B8	I2C_SEQUENCE_CMD0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_mode_en	sequential_rw	sequential_addr_mode		reserved		reserved		reserved	add_cnt_full	sequential_busy	sequential_finish	sequential_tx_fifo_cnt																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sequential_mode_en	Sequential mode enable (This function must be used together with the DMA.) 0: disabled 1: enabled
[30]	RW	sequential_rw	Operation type in sequential mode 0: read 1: write
[29:28]	RW	sequential_addr_mode	Start address type in sequential mode 00: 8 bits 00: 16 bits 10: 24 bits 11: 32 bits
[27]	RW	reserved	Reserved
[26:24]	RO	reserved	Reserved
[23]	RW	reserved	Reserved
[22]	RO	add_cnt_full	Start address transmission completion indicator, indicating that the DMA can be started
[21]	RO	sequential_busy	Operation busy indicator in sequential mode
[20]	RO	sequential_finish	Operation completion indicator in sequential mode
[19:0]	RO	sequential_tx_fifo_cnt	Number of completed operations in sequential mode

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I2C_SEQUENCE_CMD1

I2C_SEQUENCE_CMD1 is an I2C_SEQUENCE_CMD1 register.

Offset Address	Register Name	Total Reset Value
0x00BC	I2C_SEQUENCE_CMD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_addr	Start address in sequential mode **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD2

I2C_SEQUENCE_CMD2 is an I2C_SEQUENCE_CMD2 register.

Offset Address	Register Name	Total Reset Value
0x00C0	I2C_SEQUENCE_CMD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_length																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_length	Sequential mode length The configured value is the actual value minus 1.

13.2 UART

13.2.1 Overview

The universal asynchronous receiver transmitter (UART) is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect the Hi3516A with the UART of an external chip so that the two chips can communicate with each other.

The Hi3516A provides four UART units (UART0 to UART3).

- UART0: a two -wire UART for debugging

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- UART1: a four-wire UART for controlling the pan, tile, and zoom (PTZ).
- UART2: a two-wire UART for generating alarms or connecting to a universal UART device
- UART3: a two-wire UART for generating alarms or connecting to a universal UART device

13.2.2 Features

The UART unit has the following features:

- Supports 64x8-bit transmit first-in, first-out (FIFO) and 64x12-bit RX FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports RX FIFO interrupts, TX FIFO interrupts, RX timeout interrupts, and error interrupts.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the TX/RX function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA operations.

13.2.3 Function Description

Application Block Diagram

Figure 13-3 shows the typical application of the UART.

Figure 13-3 Typical application block diagram of the UART

The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

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Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 13-4. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 13-4 Frame format of the UART

The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

  It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.
- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.
- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the

  UART_LCR_H register.
- Stop signal (stop bit)

  It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

13.2.4 Operating Mode

13.2.4.1 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock/(16 x Frequency divider). The frequency of the UART reference clock may be the APB bus clock frequency (50 MHz) or 6 MHz.

The clock frequency divider consists of the integral part and the fractional part that correspond to UART_IBRD and UART_FBRD respectively.

For example, assume that the frequency of the UART reference clock is 60 MHz. If UART_IBRD is set to 0x1E and UART_FBRD is set to 0x00, the current baud rate is calculated as follows: 60/(16 x 30) = 0.125 Mbit/s

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The typical UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.

The following examples show how to calculate the clock divider and how to configure the clock divider register:

If the required baud rate is 230,400 bit/s and the frequency of the UART reference clock is 100 MHz, the clock divider is calculated as follows: $(100x10^6)/(16 \times 230,400) = 27.1267$. The integral part IBRD is 27 and the fractional part FBRD is 0.1267.

To calculate the value of the 6-bit UART_FBRD register, do as follows: calculate the value of *m* by using the following formula: $m = \text{integer}(FBRD \times 2^n + 0.5) = (0.1267 \times 2^6 + 0.5) = 8$(n = the width of UART_FBRD). Then set UART_IBRD to 0x001B and set UART_FBRD to 0x08.

If the fractional part of the frequency divider is set to 8, the actual divisor of the baud rate is 27 + 8/64 = 27.125, the baud rate is (100 x 16)/(16 x 27.125) = 230,414.75, and the error rate is (230,414.75 – 230,400)/230,400 x 100 = 0.006%.

The maximum error rate is 1/64 x 100 = 1.56% when the 6-bit UART_FBRD is used. If the value of *m* is 1, the total error rate is greater than 64 clock cycles.

13.2.4.2 Soft Reset

The UART controller can be separately reset by configuring the CRG registers.

- The UART0 controller can be separately reset by setting PERI_CRG57[uart0_srst_req] to 1.
- The UART1 controller can be separately reset by setting PPERI_CRG57[uart1_srst_req] to 1.
- The UART2 controller can be separately reset by setting PERI_CRG57[uart2_srst_req] to 1.
- The UART3 controller can be separately reset by setting PERI_CRG57[uart3_srst_req] to 1.

NOTE

For details about reset registers, see section 3.2.7 "Register Description."

After reset, the configuration registers are restored to default values. Therefore, these registers must be initialized again.

13.2.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to UART_CR bit[0] to disable the UART.

Step 2 Write to UART_IBRD and UART_FBRD to configure the transfer rate.

Step 3 Configure UART_CR and

Step 4 UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the thresholds of TX and RX FIFOs.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.

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Step 7 Write 1 to UART_CR bit[0] to enable the UART.

----End

Data Transmission

To transmit data, perform the following steps:

Step 1 Write the data to be transmitted to UART_DR and start data transmission.

Step 2 In query mode, check the TX_FIFO status by reading UART_FR bit[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.

Step 3 Check whether the UART transmits all data by reading UART_FR bit[7]. If UART_FR bit[7] is 1, the UART transmits all data.

----End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.
- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

13.2.4.4 Data Transfer in DMA Mode

Initialization

To initialize the UART, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Write values to UART_IBRD and UART_FBRD to configure the data transfer rate.

Step 3 Configure UART_CR and

Step 4 UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the TX and RX FIFO thresholds.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable corresponding interrupts. If the driver runs in query mode, disable the generation of corresponding interrupts.

Step 7 Write 1 to UART_CR[uarten] to enable the UART.

----End

Data Transfer

To transmit data, perform the following steps (the following is an example using the DMA to transmit data):

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Step 1 Configure the DMA data channel, including the transfer source address, transfer destination address, number of data items to be transferred, and transfer type. For details, see the description in xx "DMAC."

Step 2 Set UART_DMACR to 0x2 to enable the DMA transfer function of the UART.

Step 3 Check whether the data is transferred completely based on the interrupt report status of the DMA. If all data is transferred, disable the DMA transfer function of the UART.

----End

Data Reception

To receive data, perform the following steps (the following is an example using the DMA to receive data):

Step 1 Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data items to be transferred, and transfer type.

Step 2 Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.

Step 3 Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

----End

13.2.5 Register Summary

The Hi3516A provides four UART units: UART0, UART1, UART2, and UART3. Their base addresses are as follows:

- The base address of UART0 registers is 0x2008_0000.
- The base address of UART1 registers is 0x2009_0000.
- The base address of UART2 registers is 0x200A_0000.
- The base address of UART3 registers is 0x2023_0000.

Table 13-2 describes the UART registers.

Table 13-2 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	13-33
0x004	UART_RSR	Receive status register or error clear register	13-34
0x018	UART_FR	Flag register	13-35
0x024	UART_IBRD	Integral baud rate register	13-36
0x028	UART_FBRD	Fractional baud rate register	13-36
0x02C	UART_LCR_H	Line control register	13-37
0x030	UART_CR	Control register	13-38

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Offset Address	Register	Description	Page
0x034	UART_IFLS	Interrupt FIFO threshold select register	13-40
0x038	UART_IMSC	Interrupt mask register	13-41
0x03C	UART_RIS	Raw interrupt status register	13-42
0x040	UART_MIS	Masked interrupt status register	13-43
0x044	UART_ICR	Interrupt clear register	13-44
0x048	UART_DMACR	DMA control register	13-45

13.2.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	RO	reserved	Reserved
[11]	RO	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the RX FIFO is full.
[10]	RO	be	Break error 0: No break error occurs. 1: A break error occurs. That is, the time of RX data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[9]	RO	pe	Parity error 0: No parity error occurs. 1: A parity error occurs.

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[8]	RO	fe	Frame error 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3]	RW	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and an overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error 0: No break error occurs. 1: A break error occurs. A break error occurs when the time of the RX data signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[1]	RW	pe	Parity error 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the

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			top of the FIFO.
[0]	RW	fe	Frame error 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is empty.

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[3]	RO	busy	UART busy/idle status 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the TX FIFO is not empty.
[2:0]	RO	reserved	Reserved

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.
- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (216 - 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.

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Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a line control register. The registers

UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated,

UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RW	sps	Parity select When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	TX/RX FIFO enable

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			0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The RX logic does not check for the 2-bit stop bit during data reception.
[2]	RW	eps	Parity select during data transmission and reception 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H [fen] is 0, this bit becomes invalid.
[1]	RW	pen	Parity enable 0: The parity is disabled. 1: The parity is generated on the TX side and checked on the RX side.
[0]	RW	brk	Break transmit 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. **NOTE** This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear

Step 4 UART_LCR_H [fen].

Step 5 Configure UART_CR.

Step 6 Write 1 to UART_CR[uarten] to enable the UART.

----End

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Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable 0: disabled 1: enabled. The data reception request is raised only when the RX FIFO has available space.
[13:12]	RO	reserved	Reserved
[11]	RW	rts	Request transmit This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.
[7]	RW	lbe	Loopback enable 0: disabled 1: UARTTXD is looped back to UARTRXD.
[6:1]	RO	reserved	Reserved

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[0]	RW	uarten	UART enable 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	rxiflsel	RX interrupt FIFO threshold select. An RX interrupt is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: RX FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101–111: reserved
[2:0]	RW	txiflsel	TX interrupt FIFO threshold select. A TX interrupt is triggered when any of the following conditions is met: 000: TX FIFO ≤ 1/8 full 001: TX FIFO ≤ 1/4 full 011: TX FIFO ≤ 3/4 full 010: TX FIFO ≤ 1/2 full 100: TX FIFO ≤ 7/8 full 101–111: reserved

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UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RW	oeim	Mask status of the overflow error interrupt 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt 0: masked 1: not masked
[6]	RW	rtim	Mask status of the RX timeout interrupt 0: masked 1: not masked
[5]	RW	txim	Mask status of the TX interrupt 0: masked 1: not masked
[4]	RW	rxim	Mask status of the RX interrupt 0: masked 1: not masked
[3:0]	RO	reserved	Reserved

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UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oeris	Status of the raw overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txris	Status of the raw TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

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UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oemis	Status of the masked overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txmis	Status of the masked TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

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UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	WO	oeic	Overflow error interrupt clear 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear 0: invalid 1: cleared
[6]	WO	rtic	RX timeout interrupt clear 0: invalid 1: cleared
[5]	WO	txic	TX interrupt clear 0: invalid 1: cleared
[4]	WO	rxic	RX interrupt clear 0: invalid 1: cleared
[3:0]	RO	reserved	Reserved

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UART_DMACR

UART_DMACR is a DMA control register. It is used to enable or disable the DMAs of the TX and RX FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	RO	reserved	Reserved
[2]	RW	dmaonerr	DMA enable for the RX channel when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is invalid.
[1]	RW	txdmae	TX FIFO DMA enable 0: disabled 1: enable
[0]	RW	rxdmae	RX FIFO DMA enable 0: disabled 1: enable

13.3 SPI

13.3.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

13.3.2 Features

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CAUTION

The Hi3516A has two serial peripheral interfaces (SPIs). SPI0 supports a CS, whereas SPI1 supports three CSs.

The Hi3516A SPIs are master interfaces. The working reference clock is the APB bus clock. SPI_CLK output by the SPI supports the maximum working frequency of 25 MHz.

The SPI controller has the following features:

- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as an RX FIFO and the other one acts as a TX FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

13.3.3 Function Description

Typical Application

Figure 13-5 shows the application block diagram when the SPI is connected to a slave device. The default chip select pin SPI_CSN0 is used.

Figure 13-5 Application block diagram when the SPI is connected to a single slave device

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13.3.4 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 13-6 to Figure 13-13 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

1. **SPO = 0, SPH = 0**

Figure 13-6 shows the SPI single frame format.

Figure 13-6 SPI single frame format (SPO = 0, SPH = 0)

Figure 13-7 shows the SPI continuous frame format.

Figure 13-7 SPI continuous frame format (SPO = 0, SPH = 0)

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SIP_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. At this time, both the master and slave data become valid. The SPI_CLK pin changes to high level in the next half SPI_CLK clock cycle. Then,

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data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For continuous transfer, the SPI_CS_N signal must pull up the SPI_CLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CS_N signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

2. **SPO = 0, SPH = 1**

Figure 13-8 shows the SPI single frame format.

Figure 13-8 SPI single frame format (SPO = 0, SPH = 1)

Figure 13-9 shows the SPI continuous frame format.

Figure 13-9 SPI continuous frame format (SPO = 0, SPH = 1)

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer start if the SPI_CS_N signal is set to low. The master and slave data become valid on their respective transfer line half SPI_CLK clock cycle later. Meanwhile, SPI_CLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

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For a continuous transfer, SPI_CS_N remains low between the transfers of two words. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

3. **SPO = 1, SPH = 0**

Figure 13-10 shows the SPI single frame format.

Figure 13-10 SPI single frame format (SPO = 1, SPH = 0)

Figure 13-11 shows the SPI continuous frame format.

Figure 13-11 SPI continuous frame format (SPO = 1, SPH = 0)

When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level after one SPI_CLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CS_N signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the internal serial device register. SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

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4. **SPO = 1, SPH = 1**

Figure 13-12 shows the SPI single frame format.

Figure 13-12 SPI single frame format (SPO = 1, SPH = 1)

Figure 13-13 shows the SPI continuous frame format.

Figure 13-13 SPI continuous frame format (SPO = 1, SPH = 1)

When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. Half SPI_CLK clock cycle later, the master data and slave data are valid on respective transfer line. Meanwhile, SPI_CLK becomes valid from a falling edge of SPI_CLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock. If a single word is being transmitted, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CS_N signal remains low. SPI_CS_N is restored to high level one SPI_CLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CS_N remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

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5. **Interface timings**

Figure 13-14 SPI timings

Table 13-3 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	–3.5	5	ns
Tds	Input control signal setup time	23	None	ns
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 13-15 shows the TI synchronous serial single frame format.

Figure 13-15 TI synchronous serial single frame format

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Figure 13-16 shows the TI synchronous serial continuous frame format.

Figure 13-16 TI synchronous serial continuous frame format

When the SPI is idle in this mode:

- The SPI_CK signal is set to low.
- The SPI_CS_N signal is set to low.
- The transfer data line SPI_DO retains high impedance.

If there is data in the TX FIFO, SPI_CS_N generates a high-level pulse in one SPI_CK clock cycle. Then, the data to be transmitted is transferred from the TX FIFO to the TX logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_DO on the next rising edge of the SPI_CK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_CK clock. The RX serial register transmits the data to the RX FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 13-17 shows the national semiconductor microwire single frame format.

Figure 13-17 National semiconductor microwire single frame format

0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

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Figure 13-18 shows the national semiconductor microwire continuous frame format.

Figure 13-18 National semiconductor microwire continuous frame format

0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high level.
- The TX data signal SPI_DO is forced to low level.

Writing one control byte to the TX FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CS_N. The data of the TX FIFO is sent to the serial shift register. The MSB of the 8-bit control frame is transmitted to the SPI_DO pin. During frame transfer, SPI_CS_N remains low. Whereas SPI_DI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_CLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_DI on the falling edge of the SPI_CK clock. For a single data transfer, SPI_CS_N is pulled up at the end of the frame one clock cycle after the last bit is written to the RX serial register. In this way, the RX data is transmitted to the RX FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CS_N retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_CLK clock.

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13.3.5 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

Clock and Reset

The frequency of the output SPI clock is calculated as follows:

Fsspclkout = Fsspclk/[CPSDVR x (1 + SCR)]

Fsspclk is the working reference clock of the SPI and its value is 1/4 of the bus clock.

For details about CPSDVR and SCR, query the corresponding registers.

The SPI of the Hi3516A supports separately soft reset, which is controlled by the PERI_CRG57 bit[6:5] register. To disable the soft reset on the SPI, write 0 to corresponding bits. To enable soft-reset on the SPI, write 1 to corresponding bits. The default value is 0 when the SPI is powered on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  RX FIFO interrupt request. When there are four or more valid data segments in the RX FIFO, the interrupt is set to 1.
- SPITXINTR

  TX FIFO interrupt request. When there are four or less valid data segments in the TX FIFO, the interrupt is set to 1.
- SPIRORINTR

  RX overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the RX shift register rather than the FIFO.
- SPIRTINTR

  RX timeout interrupt request. When the RX FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the RX FIFO needs to be transmitted. When the RX FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.
- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

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Initialization

The initialization is implemented as follows:

Step 1 Write 0 to SPICR1[sse] to disable the SPI.

Step 2 Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.

Step 3 Configure SPICPSR to set the required clock divider.

Step 4 In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.

Step 5 Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.

Step 6 Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

----End

Data Transfer in Query Mode

The full status of the TX or RX FIFO is not considered, because the depth of the TX FIFO or RX FIFO is 512.

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to enable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Poll SPISR until SPISR[BSY] is 0, SPISR[TFE] is 1, and SPISR[RNE] is 1. If SPISR[BSY] is 0, the bus is busy; if SPISR[TFE] is 1, the TX FIFO is empty; if SPISR[RNE] is 1, the RX FIFO is not empty.

Step 4 Read data until the RX FIFO is empty. You can check whether the RX FIFO is empty by querying SPISR[RNE].

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in Interrupt Mode

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to disable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

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Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 4 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in DMA Mode

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Write 1 to SPICR1[sse] to disable the SPI.

Step 3 Transmit data.

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SPI TX FIFO for the data transfer.
3. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.

Step 4 Receive data

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SSP RX FIFO for the data transfer.
3. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

13.3.6 Register Summary

Table 13-4 describes the registers.

- The base address of SPI registers is 0x200C_0000.
- The base address of SPI registers is 0x200E_0000.

Table 13-4 Summary of SPI registers

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	13-57
0x004	SPICR1	Control register 1	13-58
0x008	SPIDR	Data register	13-59
0x00C	SPISR	Status register	13-59

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Offset Address	Register	Description	Page
0x010	SPICPSR	Clock divider register	13-60
0x014	SPIIMSC	Interrupt mask register	13-61
0x018	SPIRIS	Raw interrupt status register	13-62
0x01C	SPIMIS	Masked interrupt status register	13-62
0x020	SPIICR	Interrupt clear register	13-63
0x024	SPIDMACR	DMA control register	13-63
0x028	SPITXFIFOCR	TX FIFO control register	13-64
0x02C	SPIRXFIFOCR	RX FIFO control register	13-65

13.3.7 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the TX and RX bit rates of the SPI. The formula is as follows: FSSPCLK/(CPSDVSR (1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPICLKOUT phase. For details, see the "SPI frame format of Peripheral Bus Timings" in section 13.3.4.
[6]	RW	SPO	SPICLKOUT polarity. For details, see the "SPI Frame Format of Peripheral Bus Timings" in section 13.3.4.
[5:4]	RW	FRF	Frame format select. 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National microwire frame format 11: reserved
[3:0]	RW	DSS	Data width.

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			0011: 4 bits 1000: 9 bits 1101: 14 bits 0100: 5 bits 1001: 10 bits 1110: 15 bits 0101: 6 bits 1010: 11 bits 1111: 16 bits 0110: 7 bits 1011: 12 bits 0111: 8 bits 1100: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved			BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.
[7:5]	RO	reserved	Reserved
[4]	RW	BigEnd	Data endian mode 0: little endian 1: big endian

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[3]	RO	reserved	Reserved
[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: reserved
[1]	RW	SSE	SPI enable 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode 0: A normal serial port operation is enabled. 1: The output of the TX serial shift register is connected to the input of the RX serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	TX or RX FIFO Read: RX FIFO Write: TX FIFO If the data is less than 16 bits, the data must be aligned to the right. The TX logic ignores the unused upper bits, and the RX logic automatically aligns the data to the right.

SPISR

SPISR is a status register.

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Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RO	reserved	Reserved
[4]	RW	BSY	SPI busy flag 0: idle 1: busy
[3]	RW	RFF	Whether the RX FIFO is full 0: not full 1: full.
[2]	RW	RNE	Whether the RX FIFO is not empty 0: empty 1: not empty
[1]	RW	TNF	Whether the TX FIFO is not full 0: full 1: not full
[0]	RW	TFE	Whether the TX FIFO is empty 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the input clock SPICLK. The LSB is read as 0.

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SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RW	TXIM	TX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the TX FIFO. 1: The interrupt is not masked when only half of or less data is left in the TX FIFO.
[2]	RW	RXIM	RX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the RX FIFO. 1: The interrupt is not masked when only half of or less data is left in the RX FIFO.
[1]	RW	RTIM	RX timeout interrupt mask 0: masked 1: not masked
[0]	RW	RORIM	RX overflow interrupt mask 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the RX FIFO is full, the SPI stops transmitting data.

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SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXRIS	Raw TX FIFO interrupt status
[2]	RO	RXRIS	Raw RX FIFO interrupt status
[1]	RO	RTRIS	Raw RX timeout interrupt status
[0]	RO	RORRIS	Raw RX overflow interrupt status

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXMIS	Status of the masked TX FIFO interrupt
[2]	RO	RXMIS	Status of the masked RX FIFO interrupt
[1]	RO	RTMIS	Status of the masked RX timeout interrupt
[0]	RO	RORMIS	Status of the masked RX overflow interrupt

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SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved
[1]	RO	RTIC	RX timeout interrupt clear
[0]	RO	RORIC	RX overflow interrupt clear

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved
[1]	WO	TXDMAE	DMA TX FIFO enable 0: disabled 1: enabled
[0]	WO	RXDMAE	DMA RX FIFO enable 0: disabled 1: enabled

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SPITXFIFOCR

SPITXFIFOCR is a TX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	TXINTSize	Threshold for generating the TX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMATXBRSize	Threshold for generating the TX FIFO request DMA transfer burst. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – DMATXBRSize), DMATXBREQ is valid. The width of the TX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

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SPIRXFIFOCR

SPIRXFIFOCR is an RX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	RXINTSize	Threshold for generating the RX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the RX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the RX FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the TX FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

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13.4 MMC/SD/SDIO Controller

13.4.1 Function Description

Functional Block Diagram

The MMC/SD/SDIO controller (MMC controller for short) controls the read/write operations on the secure digital (SD) card and multimedia card (MMC), and supports various extended devices such as Bluetooth and Wi-Fi devices based on the secure digital input/output (SDIO) protocol. The Hi3516A provides two MMC controllers for controlling the SD card, MMC, and SDIO device.

The MMC controller can control the devices that comply with the following protocols:

- Secure Digital Memory (SD mem-version 3.0)
- Secure Digital I/O (SDIO-version 2.0)
- MultiMediaCard (MMC-version 4.3)

Figure 13-19 shows the functional block diagram of the MMC controller.

Figure 13-19 Functional block diagram of the MMC controller

NOTE

S indicates slave interface and M indicates master interface.

Connected to the system through the internal bus, the MMC controller consists of the following parts:

- Command path

  It is used to transmit commands and receive responses.
- Data path

  It is used to perform data read and write operations by working with the command path.

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- Interface clock control unit

  It is used to change the frequency of the interface clock as required and enable or disable the interface clock. SDIO_CLK_OUT can be generated by dividing CCLK_IN.

The MMC controller has the following features:

- Transfers data by using the internal direct memory access controller (IDMAC).
- Supports one TX FIFO and one RX FIFO. The depth of each FIFO is 256 words.
- Supports configurable burst size during DMA transfer and configurable FIFO threshold.
- Supports FIFO overflow and underflow interrupts to avoid errors during data transfer.
- Supports the cyclic redundancy check (CRC) generation and check for data and commands.
- Supports programmable frequency of the interface clock.
- Disables the MMC clock and interface clock in low-power mode.
- Supports 1-bit or 4-bit data width based on the connected component.
- Reads or writes data blocks with the size of 1 byte to 65,535 bytes.
- Reads/writes stream data from/to the MMC card.
- Supports the suspend operation, resume operation, and read wait operation on the SDIO card.

Typical Application

Figure 13-20 shows the typical application circuit of the MMC controller.

Figure 13-20 Typical application circuit of the MMC controller

The MMC controller exchanges commands and data with the connected card over a clock signal line, a bidirectional command signal line, and four bidirectional data signal lines. Both the command signal line and data signal lines work in pull-up mode. Table 13-5 describes the pull-up resistors and the load capacitance of each signal line.

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Table 13-5 Load parameters of signal lines

Parameter	Min.	Max.	Description
R_{DAT} R_{CMD}	10 kΩ	100 kΩ	Pull-up resistors
Load capacitance Cx	None	30 pF	$C_x = C_{mmchost} + C_{bus} + C_{card}$The maximum capacitance of each card (C_{card}) is 10 pF; therefore, the sum of $C_{mmchost}$ and C_{bus} must be less than 30 pF.
Inductance of each signal line	None	16 nH	Fpp ≤ 20 MHz

CAUTION

Besides the signal lines inFigure 13-20, the card slot also provides the mechanical write protection signal and card detection signal. However, the signal interfaces are not provided in Figure 13-20.

Commands and Responses

All interactions between the MMC controller and the card, including initializing the card, reading/writing to registers, querying the status, and transferring data, are implemented by using commands.

A MMC command is a segment of 48-bit serial data consisting of a start bit, a transmission bit, a command sequence, a CRC bit, and an end bit. After receiving a command, the card returns a 48-bit or a 136-bit response based on the command type.

Figure 13-21 Format of an MMC command

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Figure 13-22 Format of the response to an MMC command

Commands are classified into the following two types based on whether data is transferred:

- Non-data transfer command

  The MMC controller transmits/receives commands to/from the card through the command signal line.
- Data transfer command

  Besides the interaction on the command line, data is also transferred through the data lines DAT0 to DAT3.

1. Non-data transfer command

Figure 13-23 shows the operations between the MMC controller and the card by running a non-data transfer command.

Figure 13-23 Operations by running an MMC non-data transfer command

2. Data transfer command

The MMC supports the following data transfer commands:

- Stream data read/write command

  Only the MMC card supports the stream data read/write command. In this case, only the data line DAT0 is used for data transfer, and no CRC check is performed.
- Single-block read/write command

  After this command is executed, one single data block is read and written each time. No stop command is required for stopping each data transfer.
- Multi-block read/write command

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– Predefined block count mode

Before the multi-block read/write command is executed, the block count command is transmitted to specify the number of data blocks to be transferred.

– Open-ended mode

After a read/write command is transmitted, a stop command is required for stopping data transfer at the end of data transfer.

The difference between the two modes lies on how the MMC controller notifies the card of the end of each data transfer. The SD card supports only the open-ended mode, whereas the MMC supports both modes.

The multi-block read/write command for the SDIO card is different from the preceding two modes. To be specific, the command parameter contains the number of data blocks to be transferred when the read/write command is transmitted.

Responses are classified into the following three types:

- Command without response

  For example, the card reset command.
- Short response command

  For example, the data transfer command and card status query command.
- Long response command

  This type of commands are used to read only the information about the card identification (CID) and card specific data (CSD) registers of a card.

Data Transfer

The single-block read/write command and the multi-block read/write command are widely used during data transfer. The data block during the data transfer of the SD card and MMC is 512 bytes; the block size during the data transfer of the SDIO card can be customized

NOTE

During the data transfer by using the block read/write command, the total data amount to be transferred must be an integral multiple of the block size.

All data transfer commands are short response commands with data transferred through data lines. Figure 13-24 and Figure 13-25 show the relationships among the commands, responses, and timings of data lines.

1. Single-block and multi-block read operations

Figure 13-24 Single-block and multi-block read operations

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The MMC controller transmits a single-block or multi-block command to a card. When a response is being received, data is received by blocks. Each data block contains a CRC check bit for ensuring the integrity of the transferred data.

In a single-block read operation, the data transfer is completed after the MMC controller receives a data block. In a multi-block read operation, the MMC controller needs to transmit a stop command to end the data transfer after receiving multiple data blocks only in open-ended mode.

2. Single-block and multi-block read operations

Figure 13-25 Single-block and multi-block write operations

The MMC controller transmits a single-block or multi-block command to a card. After receiving a response, the MMC controller starts to transmit data to the card by blocks. Each data block contains a CRC bit. The card performs CRC on each data block and transfers the CRC status to the MMC controller. This ensures that data is transferred properly.

In a single-block write operation, the data transfer is completed after the MMC controller transmits a data block. In a multi-block write operation, the MMC controller needs to transmit a stop command to end the data transfer after transmitting multiple data blocks only in open-ended mode. After a write operation, the card may be busy in programming the flash memory. The MMC controller can perform the next operation on the card only after it confirms that the card is not busy by querying the status of the signal line DAT0.

3. Data transfer format

During the block read/write operations, the 1- or 4-bit data line can be used to transfer data between the MMC controller and the card. Before a data transfer command is transmitted, the data transfer widths of the MMC controller and card must be the same (1 bit or 4 bits). You can set the data bit width of the MMC controller by configuring MMC_CTYPE and set the data bit width of the card by transmitting the corresponding command.

Figure 13-26 shows the data transfer format in 1-bit mode, and Figure 13-27 shows the data transfer format in 4-bit mode.

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Figure 13-26 Data transfer format in 1-bit mode

Figure 13-27 Data transfer format in 4-bit mode

Speed Mode and Voltage Switching Supported by SD3.0

The MMC controller supports SD 3.0 ultra high speed (UHS-1) and allows the voltage to be switched in SD mode. Table 13-6 describes the relationship between the transmission modes and voltages.

Table 13-6 Transmission mode

Mode	Input Clock (MHz)	Clock on the Card Side	Maximum Data Bit Width	Voltage
SDR50	100 MHz	100 MHz	4 bit	1.8 V
DDR50	50 MHz	50 MHz	4 bit	1.8 V
SDR25	50 MHz	50 MHz	4 bit	1.8 V
SDR12	25 MHz	25 MHz	4 bit	1.8 V
HS	50 MHz	50 MHz	4 bit	3.3 V
DS	25 MHz	25 MHz	4 bit	3.3 V
MMC HS	50 MHz	50 MHz	4 bit	3.3 V

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13.4.2 Application Notes

NOTE

For details about clock reset registers, see section 3.2.7 "Register Description."

Clock Gating

When the software completes the current command or data transfer and does not start a new data transfer, the SDIO_CCLK_OUT clock can be disabled if the MMC controller is idle.

Perform the following steps:

Step 1 Read MMC_STATUS.

Step 2 If both MMC_STATUS[Command fsm_states] and MMC_STATUS[data_state_mc_busy] are 0, write 0 to MMC_CTRL to mask the MMC interrupt and enable the DMA request, and go to Step 3. If any of [Command fsm_states] and [data_state_mc_busy] is not 0, wait with delay, and go to Step 1.

Step 3 Write 0 to PERI_CRG49 bit[1] to disable the SDIO0 clock, and write 0 to PERI_CRG49 bit[9] to disable the SDIO1 clock.

NOTE

To enable the SDIO0 clock, write 1 to PERI_CRG49 bit[1]. To enable the SDIO1 clock, write 1 to PERI_CRG49 bit[9].

----End

Soft Reset

If the MMC controller cannot be restored to the idle state due to data transfer exceptions, you can write 1 to PERI_CRG49 bit[0] to soft reset SDIO0, and write 1 to PERI_CRG49 bit[8] to soft reset SDIO1. In addition, you can query MMC_STATUS[Data_busy] to check whether the MMC controller is idle.

Before using the MMC controller, you are advised to soft-reset the MMC controller after hot-swapping the card.

Configuring the Working Clock

Before using the MMC controller, you need to configure the frequency of its working clock. You can set the frequency of the MMC working clock to 25 MHz, 50 MHz, 75 MHz, or 100 MHz, SDIO0 by configuring PERI_CRG49 bit[2], configure SDIO0 by setting PERI_CRG49bit[3:2], and configure SDIO1 by setting PERI_CRG49 bit[11:10].

Configuring the Interface Clock

Clock frequencies vary according to the MMCs complying with different protocols and the status of MMCs. The MMC controller provides an internal even frequency divider that generates appropriate interface clocks by dividing the frequency of the working clock. The relationship between the frequencies of the working clock CCLK_IN and the interface clock SDIO_CCLK_OUT of the MMC controller is as follows:

$F_{SDIO_CCLK_OUT} = F_{CCLK_IN}/(2 \times clk_divider)$

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Where, clk_divider is the value of MMC_CLKDIV[clk_divider]. Clock frequencies vary according to card types. The maximum value of $F_{SDIO_CCLK_OUT}$ is 100 MHz.

Before changing the clock frequency of an MMC, ensure that no data or command is being transferred. In addition, to avoid the occurrence of glitches in the output clock of the MMC, you need to perform the following steps:

Step 1 Disable the interface clock.

Set MMC_CLKENA to 0x0000_0000, set MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only], and MMC_CMD[Wait_prvdata_complete] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 2 Set the clock divider.

Configure MMC_CLKDIV based on the required clock frequency, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 3 Enable the interface clock again.

Set MMC_CLKENA to 0x0000_0001, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

----End

CAUTION

The values of MMC_CMD and MMC_CMD are loaded only after MMC_CLKDIV[Start_cmd] and MMC_CLKENA[Update_clk_only] are set to 1. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically. If a command is being executed, a hardware locked error (HLE) interrupt is generated. In this case, you need to clear the interrupt, and then transmit a command again.

When a command is being executed or data is being transferred, the clock parameter values of the card cannot be changed.

Initialization

Before commands and data are exchanged between a card and the MMC controller, the MMC controller needs to be initialized. Perform the following steps:

Step 1 Configure the frequency of the working clock of the MMC controller. For details, see "Working Clock Configuration" in section 13.4.2 "Application Notes."

Step 2 Soft-reset the MMC controller after the card is powered on and the command and data signal lines are pulled up and become stable. For details, see "Soft Reset" in section 13.4.2 "Application Notes."

Step 3 Clear interrupts. Set all bits of MMC_RINTSTS bit[15:0] to 1 to clear raw interrupt status bits.

Step 4 Configure MMC_INTMASK. Set all bits of MMC_INTMASK bit[15:0] to 1 to enable all interrupt sources.

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If data is transferred in DMA mode, set MMC_INTMASK bit[4] and MMC_INTMASK bit[5] to 0 to mask the TX/RX FIFO data request interrupts.

Step 5 Set MMC_CTRL[Int_enable] to 1 to enable the MMC interrupt.

Step 6 Configure the timeout parameter register

Step 7 MMC_TMOUT.

Step 8 Configure the FIFO parameter register MMC_FIFOTH.

----End

After the preceding steps, the interface clock can be configured and commands can be transmitted to the card.

Non-Data Transfer Command

If the MMC controller receives a response (correct response, error response, or timeout response) after transmitting a command, the MMC controller sets MMC_RINTSTS bit[2] to 1. Short responses are stored in MMC_RESP0, and long responses are stored in MMC_RESP0 to MMC_RESP3. MMC_RESP3 bit[31] is the MSB, and MMC_RESP0 bit[0] is the LSB. After a command is transmitted, its error status is reflected by the response command and the corresponding error bit of MMC_RINTSTS.

To transmit a non-data transfer command, perform the following steps:

Step 1 Set the corresponding command parameters of MMC_CMDARG.

Step 2 Configure the command register MMC_CMD based on the description in Table 13-7.

Step 3 Wait until the MMC controller runs the command. If the command is executed, the MMC controller clears MMC_CMD[Start_cmd] automatically.

Step 4 Check whether an HLE interrupt is generated by MMC_RINTSTS bit[12].

Step 5 Wait until the command is executed. If the MMC controller receives a response (correct response, error response, or timeout response), the MMC controller sets MMC_RINTSTS bit[2] to 1. This indicates that the command is executed.

Step 6 Check whether there is any response exception and read the response value if necessary.

You can check the response timeout error, response CRC error, and response error by reading MMC_RINTSTS bit[8], MMC_RINTSTS bit[6], and MMC_RINTSTS bit[1] respectively.

----End

CAUTION

The values of MMC_CMD, MMC_CMDARG, MMC_BYTCNT, and MMC_BLKSIZ are loaded only after MMC_CMDARG[Start_cmd] is set to 1 and MMC_CMD[Update_clock_registers_only] is set to 0. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically.

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If other commands are being executed, an HLE interrupt is generated. In this case, you need to perform the preceding operations again. When a non-data transfer command is executed, the values of MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 13-7 Default values of MMC_CMD when a non-data transfer command is executed

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
data_transfer_expected	0	Indicates a non-data transfer command.
card_number	0	-
cmd_index	Cmd index	Command index
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
response_length	0	Indicates that this bit is set to 1 when the response is a long response.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
Wait_prvdata_complete	1 or 0	Indicates that the MMC controller must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status during data transfer or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading a Single Data Block or Multiple Data Blocks

To read a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the number of bytes to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for reading data to MMC_CMDARG.

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Step 5 Configure MMC_CMD according to the description in Table 13-8.

For the SD card or MMC, you need to read a single data block by running CMD17, and read multiple data blocks by running CMD18; for the SDIO card, you need to read a single data block or multiple data blocks by running CMD53.

The MMC controller starts to run commands after MMC_CMD is written. After commands are transferred to the bus, the cmd_done interrupt is generated.

Step 6 Check the values of MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10]. If any or both of them are 1, read the data in the FIFO by reading MMC_CARDTHRCTL. This ensures that the MMC controller can receive the subsequent data. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. In this case, you can transmit a stop command to stop the data transfer by using the software.

Step 7 If MMC_RINTSTS bit[3] is 1, data transfer is complete. In this case, read the remaining data in the FIFO by reading MMC_CARDTHRCTL.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 13.4.2 "Application Notes."

----End

Table 13-8 Default values of MMC_CMD when a single data block or multiple data blocks are read

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 13.4.2 "Application Notes."
transfer_mode	0	Indicates block transfer.
read/write	0	Indicates that data is read from the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.

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Parameter	Value	Description
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	Indicates the command index.
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Writing a Single Data Block or Multiple Data Blocks

To write a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the size of the data to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for writing data to MMC_CMDARG.

Step 5 Write data to the FIFO by writing to MMC_CARDTHRCTL. The FIFO needs to be filled with data completely at the very beginning.

Step 6 Configure MMC_CMD according to the description in Table 13-9.

For the SD card or MMC, you need to write a single data block by running CMD24, and write multiple data blocks by running CMD25; for the SDIO card, you need to write a single data block or multiple data blocks by running CMD53.

Step 7 Check the values of MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If any or both of them are 1, fill the FIFO with data by writing to MMC_CARDTHRCTL. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. If necessary, you can transmit a stop command to stop the data transfer by using the software. If MMC_RINTSTS bit[3] is 1, data transfer is complete.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 13.4.2 "Application Notes."

Step 9 Query and wait until the value of MMC_STATUS[data_busy] is changed from 1 to 0.

----End

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Table 13-9 Default values of MMC_CMD when a single data block or multiple data blocks are written

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 13.4.2 "Application Notes."
transfer_mode	0	Indicates block transfer.
read_write	1	Indicates that data is written to the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	-
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading/Writing Stream Data

The modes of reading/writing stream data are the same as those of reading/writing data blocks, except that MMC_CMD[Transfer_mode] needs to be set to 1. During a stream data transfer, the auto-stop function is required.

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Transferring Data by Using the IDMAC

The MMC controller has an embedded IDMAC that transfers data from the original address to the destination address based on the specified descriptor.

Descriptor

The IDMAC supports the following two types of descriptors:

- Dual-buffer descriptor. For this type of descriptor, the span between two descriptors is determined by the DSL bit of MMC_BMOD. Figure 13-28 shows the structure of the dual-buffer descriptor.

Figure 13-28 Structure of the dual-buffer descriptor

- Linked descriptor. For this type of descriptor, each descriptor points to a unique buffer and the next descriptor. Figure 13-29 shows the structure of the linked descriptor.

Figure 13-29 Structure of the linked descriptor

Each descriptor must be word-aligned, and each descriptor contains 16-byte control and status information. Figure 13-30 shows the internal structure of 32-bit descriptors.

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Figure 13-30 Internal structure of 32-bit descriptors

DES0 is used to protect the control and status information. Table 13-10 describes the definition of each bit.

Table 13-10 Definition of each bit of DES0

Bits	Register	Description
31	OWN	Indicates the attributes of the descriptor. 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the IDMAC. After data is transferred by using the IDMAC, the IDMAC clears this bit.
30	CES	Indicates the error status when a card is read. 0: No error occurs. 1: An error occurs.
29:6	RES	Reserved
5	ER	Indicates the link end of the descriptor. 0: The descriptor is not the last one on the link. 1: The descriptor is the last one on the link. This bit is valid only for the dual-buffer descriptor.
4	CH	Indicates the definition of the second address in DES3. 0: The second address in DES3 is the address of the second buffer. 1: The second address in DES3 is the address of the next descriptor. When this bit is 1, DES1[25:13] must be 0.
3	FS	Indicates that the descriptor contains the first data buffer when this bit is 1. If the size of the first data buffer is 0, the next descriptor contains the start data.
2	LD	Indicates that the descriptor points to the last data buffer when this bit is 1.
1	DIC	Indicates that the data transfer completion interrupt is

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Bits	Register	Description
		masked when this bit is 1.
0	RES	Reserved

DES1 is used to specify the buffer size. Table 13-11 describes the definition of each bit of DES1.

Table 13-11 Definition of each bit of DES1

Bits	Register	Description
31: 26	RES	Reserved
25: 13	BS2	Indicates the number of bytes in the second data buffer. This value must be an integral multiple of 4. This bit is invalid when DES0[4] is 1.
12: 0	BS1	Indicates the number of bytes in the first data buffer. This value must be an integral multiple of 4.

DES2 is the address pointer of the first data buffer. Table 13-12 describes the definition of each bit of DES2.

Table 13-12 Definition of each bit of DES2

Bits	Register	Description
31: 0	BAP1	Indicates the physical address of the first data buffer. The address must be word-aligned.

DES3 indicates the second address. Table 13-13 describes the definition of each bit of DES3.

Table 13-13 Definition of each bit of DES3

Bits	Register	Description
31: 0	BAP2	Indicates the physical address of the second data buffer when dual-buffer descriptors are used, or indicates the physical address of the next descriptor when DES0[4] is 1.

Initialization

Perform the following steps:

Step 1 Configure MMC_BMOD to set bus parameters.

Step 2 Configure MMC_IDINTEN to mask unnecessary registers.

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Step 3 Create TX/RX descriptor linked lists, configure MMC_DBADDR, and set the start address.

Step 4 The IDMAC attempts to obtain descriptors from the descriptor linked lists.

----End

Transmission

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, set DES0 bit[31] (OWN bit) to 1, and provide data buffers.

Step 2 Write data commands to MMC_CMD.

Step 3 Set TX_Wmark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from data buffers to the internal FIFO of the MMC controller when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Reception

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, and set the DES0 bit[31] (OWN bit) to 1.

Step 2 Write read commands to MMC_CMD.

Step 3 Set RX_WMark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from the internal FIFO of the MMC controller to the external data buffers when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Auto-Stop Function Configuration

When multiple data blocks are read or written, a stop command is required to stop each data transfer. The stop command can be transmitted in non-data transfer command mode or by using the auto-stop function.

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The auto-stop function is applicable in the following scenarios:

- SD card

  Multi-block read/write operation by running CMD18 or CMD25
- MMC
  - Stream data read/write operation
  - Multi-block read/write operation in open-ended mode by running CMD18 or CMD25

Before using the auto-stop function of the MMC controller, you are advised to perform the followings steps:

Step 1 Set MMC_CMD[Send_auto_stop] to 1 during the block transfer command operation.

Step 2 After data transfer, the MMC controller automatically transmits a stop command to enable the card to restore to the corresponding state.

Step 3 Read MMC_RINTSTS[auto_cmd_done] to check whether the stop command is executed. The response is stored in MMC_RESP1.

----End

Stopping or Aborting the Data Transfer

The stop command is used to interrupt the data transfer between the MMC controller and the card, whereas the abort command is used to interrupt the I/O data transfer only in SDIO_IOONLY or SDIO_COMBO mode.

The two commands are used as follows:

- Stop command

  This command can be transmitted at any time during data transfer, because this command is used to stop the data transfer. In this case, you need to set MMC_CMD bit[5:0] to CMD12, MMC_CMD bit[14] to 1, and MMC_CMD bit[13] to 0.
- Abort command

  This command is available only for SDIO_IOONLY or SDIO_COMBO. To abort the data transfer, you need to configure the CCCR[ASx] register of the SDIO card by running the CMD52 command.

Suspend and Resume Operations

An SDIO card can store the data of a maximum of seven functional devices. The MMC controller can suspend the data transfer of a device by performing the suspend operation. Then the SD interface bus is available for another device with higher priority. After the device with higher priority transfers data, the MMC controller can resume the suspended data transfer of the previous device.

The suspend and resume operations are implemented by configuring the corresponding bits of the CCCR register of the SDIO card. The CCCR register is written or read by running the CMD52 command.

To implement a suspend operation, perform the following steps:

Step 1 Query the SBS bit of the CCCR register to check whether the SDIO card supports suspend and resume operations.

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Step 2 Query the FSx and bus status (BS) bits of the CCCR register to check whether the functional device to be suspended is transferring data.

If the BS bit is 1, the device specified by the FSx bit is transferring data.

Step 3 Set the bus release (BR) bit of the CCCR register to 1 to suspend the current data transfer.

Step 4 Check whether the BS and the BR bits of the CCCR register are cleared.

The BS bit retains 1 when the data bus is being used. The BR bit retains 1 before the bus is released completely. When both the BR and BS bits are 0, the data transfer of the selected functional device is suspended.

Step 5 If the current read operation is suspended, MMC_CTRL[Abort_read_data] needs to be set to 1 to restart the data transfer function of the MMC controller after the suspend operation. Then MMC_CTRL[Abort_read_data] is cleared automatically.

Step 6 Read MMC_TCBCNT to query the number of transferred bytes.

----End

To implement a resume operation, perform the following steps:

Step 1 Query the transfer status of the card to check whether the bus is idle.

Step 2 If the card is disconnected, run the CMD7 command to select it. The card status can be queried by running the CMD52 or CMD53 command.

Step 3 Check whether the device to be resumed is ready for data transfer by querying the RF bit of the CCCR register. If the RF bit is 1, the device is ready for data transfer.

Step 4 Run the CMD52 command to write the device ID to the FS bit of the CCCR register to resume the data transfer, and enable the MMC controller to enter the data transfer state (that is, write the block size to MMC_BLKSIZ, and write the amount of remaining data to be transferred to MMC_BYTCNT).

For details about the configuration of MMC_CMDARG, see Table 13-14. The configuration of MMC_CMD is similar to the configuration during block transfer.

Step 5 The data transfer is resumed after the CMD52 command is transmitted successfully. Read the resume data flag (DF) bit of the SDIO device. If this bit is 1, data transfer starts when the transfer function is resumed. If this bit is 0, no data is ready for transferring.

Step 6 If the DF bit is 0, the MMC generates a data timeout error interrupt a period of time later during data read.

----End

Table 13-14 Reference configuration of MMC_CMDARG when the resume operation is performed

MMC_CMDARG	Value	Description
Bit[31]	1	Indicates the read/write flag.
Bit[30:28]	0	Indicates the ID of a functional device that accesses the CCCR register.
Bit[27]	1	Indicates the real-time flag, that is,

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		write-to-read.
Bit[26]	None	-
Bit[25:9]	0x0D	Indicates the register address.
Bit[8]	None	-
Bit[7:0]	ID of the functional device that is resumed	Indicates write data.

CAUTION

The MMC controller cannot be woken up after the system enters the low-power mode.

Read Wait Operation

The read wait operation is performed to suspend the data transfer of the device that is using the SDIO card. The MMC controller determines the duration of pausing the data transfer.

To implement a read wait operation, perform the following steps:

Step 1 Check whether the card supports the read wait operation.

You can read the SRW bit of the CCCR register by running the CMD52 command. If the SRW bit is 1, all the devices supporting the card support the read wait operation.

Step 2 Set MMC_CTRL[Read_wait] to 1.

Step 3 If you want to resume the data transfer, clear MMC_CTRL[Read_wait].

----End

13.4.3 Register Summary

Table 13-15 describes the MMC registers.

Table 13-15 Summary of MMC registers (the base address for SDIO0 is 0x206e_0000 and for SDIO1 is 0x206f_0000)

Offset Address	Register	Description	Page
0x0000	MMC_CTRL	MMC control register	13-88
0x0004	MMC_PWREN	Power_en control register	13-90
0x0008	MMC_CLKDIV	Clock divider register	13-90
0x000C	MMC_CLKSRC	Clock source select register of the SD card	13-91
0x0010	MMC_CLKENA	Clock enable register	13-91

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Offset Address	Register	Description	Page
0x0014	MMC_TMOUT	Timeout register	13-92
0x0018	MMC_CTYPE	Card type register	13-92
0x001C	MMC_BLKSIZ	Block size configuration register	13-93
0x0020	MMC_BYTCNT	Block transfer count register	13-93
0x0024	MMC_INTMASK	Interrupt mask register	13-94
0x0028	MMC_CMDARG	Command parameter register	13-95
0x002C	MMC_CMD	Command register	13-95
0x0030	MMC_RESP0	Response register 0	13-98
0x0034	MMC_RESP1	Response register 1	13-99
0x0038	MMC_RESP2	Response register 2	13-99
0x003C	MMC_RESP3	Response register 3	13-100
0x0040	MMC_MINTSTS	Masked interrupt status register	13-100
0x0044	MMC_RINTSTS	Raw interrupt status register	13-101
0x0048	MMC_STATUS	Status register	13-102
0x004C	MMC_FIFOTH	FIFO threshold register	13-103
0x0050	MMC_CDETECT	Card detection register	13-105
0x0054	MMC_WRTPRT	Card write protection register	13-105
0x005C	MMC_TCBCNT	Count of bytes transmitted to the card register	13-106
0x0060	MMC_TBBCNT	Count of bytes transmitted from the bus interface unit (BIU) FIFO register	13-106
0x0064	MMC_DEBNCE	Dejitter count register	13-107
0x0074	MMC_UHS_REG	UHS-1 register	13-107
0x0080	MMC_BMOD	Bus mode register	13-107
0x0084	MMC_PLDMND	Poll demand register	13-109
0x0088	MMC_DBADDR	Base address register of the descriptor linked list	13-109
0x008C	MMC_IDSTS	IDMAC status register	13-110
0x0090	MMC_IDINTEN	IDMAC interrupt enable register	13-111
0x0094	MMC_DSCADDR	Address register of the current descriptor	13-112
0x0098	MMC_BUFADDR	Address register of the current data	13-112

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Offset Address	Register	Description	Page
		buffer	
0x0100	MMC_CARDTHRCTL	Threshold control register	13-113
0x0108	MMC_UHS_REG_EXT	UHS extension register	13-114
0x010C	MMC_DDR_REG	DDR start bit detection control register	13-115
0x0110	MMC_ENABLE_SHIFT	Phase shift register	13-115
0x0200	MMC_DATA	Data register (entrance address of the FIFO)	13-116

13.4.4 Register Description

MMC_CTRL

MMC_CTRL is a MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						Use_internal_dmac	reserved																Abort_read_data	Send_irq_response	Read_wait	Dma_enable	Int_enable	reserved	Dma_reset	Fifo_reset	Controller_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	Use_internal_dmac	Whether to transfer data by using the IDMAC. 0: The CPU transfers data by using the slave interface. 1: The CPU transfers data by using the IDMAC.
[24:9]	RO	reserved	Reserved

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[8]	RW	Abort_read_data	Whether to abort the data transfer during data read. 0: invalid 1: After transmitting a suspend command during data read, the software polls the card to check when suspend occurs. After the suspend occurs, the software sets the bit to 1. This enables the data transfer state machine to be restored to idle state for the next block transfer. After the state machine restores to the idle status, this bit is cleared automatically.
[7]	RW	Send_irq_response	TX interrupt response control. 0: invalid 1: An interrupt request (IRQ) response is transmitted automatically. After the response is transmitted, this bit is cleared automatically. To wait for the interrupt generated by the MMC controller, the host transmits the CMD40 command and waits for the interrupt response from the MMC controller. If you do not want the host to keep in the interrupt wait state, set this bit to 1 and transmit the CMD40 command to restore the host to the idle state.
[6]	RW	Read_wait	Read wait control. 0: disabled 1: enabled This bit is valid only for the SDIO card that supports the read wait function.
[5]	RW	Dma_enable	Reserved. The system uses the IDMAC.
[4]	RW	Int_enable	Global interrupt enable. 0: disabled 1: enabled The interrupt output is valid only when this bit is valid and the interrupt source is enabled.
[3]	RO	reserved	Reserved
[2]	RW	Dma_reset	Soft reset control for the IDMAC. 0: invalid 1: reset the internal DMA interface This bit is automatically reset after two AHB clock cycles.
[1]	RW	Fifo_reset	Soft reset control for the internal FIFO. 0: invalid 1: reset the FIFO pointer This bit is reset automatically after the reset operation is complete.

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[0]	RW	Controller_reset	Soft reset control for the controller. 0: invalid 1: reset the MMC/SD/SDIO host module

MMC_PWREN

MMC_PWREN is a Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Power_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	Power_enable	Power control. 0: power off 1: power on This value is used to drive the SDIOn_CARD_POWER_EN (n = 0 or 1) pin.

MMC_CLKDIV

MMC_CLKDIV is a clock divider register that shows the ratio of the frequency of the module output clock to the frequency of the input clock. For example, if the module input clock is 40 MHz and the register value is set to 1, the output clock is 20 MHz.

The clock divider is 2 x N. If the value of *N* is 0x0, it indicates no frequency division (2 x 0 = 0); if the value of *N* is 0x1, the frequency is divided by 2; if the value of *N* is 0xFF, the frequency is divided by 510.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Clk_divider0							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	Clk_divider0	Clock divider 0. The clock divider is 2 x N. If the value of N is 0, it indicates no frequency division; if the value of N is 0x1, the frequency is divided by 2; if the value of N is 0xFF, the frequency is divided by 510.

MMC_CLKSRC

MMC_CLKSRC is a clock source select register of the SD card.

Offset Address	Register Name	Total Reset Value
0x000C	MMC_CLKSRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														clk_source	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	Clk_source	This bit must be set to 0.

MMC_CLKENA

MMC_CLKENA is a clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Cclk_low_power	reserved															Cclk_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved

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[16]	RW	Cclk_low_power	Card low-power control for disabling the card clock. 0: non lower-power mode 1: low-power mode When the card is idle, the card clock is disabled. This function is used only for the MMC and SD card, because the card clock of the SDIO card must be retained for detecting interrupts.
[15:1]	RO	reserved	Reserved
[0]	RW	Cclk_enable	Card clock enable. 0: disabled 1: enabled

MMC_TMOUT

MMC_TMOUT is a timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Data_timeout																								response_timeout							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	Data_timeout	Timeout during the data transfer of the card, in unit of the mmc_clk cycle of the card. The timeout is also the data starvation timeout of the CPU
[7:0]	RW	response_timeout	Response timeout, in unit of the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is a card type register.

Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Card_width	reserved														Card_width1

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	Card_width_0	Bus width of the card. This field must be set to 0 (non 8-bit mode). The bus width of the card is set to 1-bit mode or 4-bit mode, which depends on the value of bit[0].
[15:1]	RO	reserved	Reserved
[0]	RW	Card_width_1	Bus width of the card. 0: 1-bit mode 1: 4-bit mode

MMC_BLKSIZ

MMC_BLKSIZ is a block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Block_size															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	Block_size	Block size. The initial size of each block is 512 bytes.

MMC_BYTCNT

MMC_BYTCNT is a block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Byte_count	Number of transferred bytes. The number must be an integral multiple of the block size.

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			If the data transfer is not block transfer, this register must be set to 0. In this case, the software needs to transmit a stop or an abort command to control the data transfer.

MMC_INTMASK

MMC_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Sdio_int_mask	Int_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	Sdio_int_mask	SDIO interrupt mask. 0: masked 1: enabled

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[15:0]	RW	Int_mask	Interrupt mask. 0: masked 1: enabled Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation-by-host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_CMDARG

MMC_CMDARG is a command parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd_arg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Cmd_arg	Command parameter that is transferred to the card. The command parameter is related to the protocol, and each command corresponds to a command parameter.

MMC_CMD

MMC_CMD is a command register.

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Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Start_cmd	reserved			Boot_mode	Disable_boot	Expect_boot_ack	Enable_boot	reserved		Update_clock_registers_only	Card_number					Send_initialization	Stop_abort_cmd	wait_prvdata_complete	Send_auto_stop	Transfer_mode	Read_write	data_transfer_expected	Check_response_crc_	Response_length	Response_expect	Cmd_index					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	Start_cmd	Start control 0: do not start 1: start a command After the command is transferred to the card interface unit (CIU), this bit is cleared. The CPU does not allow modifications to this register. Otherwise, an HLE interrupt is generated. After transmitting a command, the CPU queries this bit, and transmits the next command when the value of this bit changes to 0.
[30:28]	RO	reserved	Reserved
[27]	RW	Boot_mode	Boot mode 0: boot mode 1: alternative boot mode
[26]	RW	Disable_boot	Boot disable If the software enables this bit and the Start_cmd bit at the same time, the controller aborts the boot operation. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[25]	RW	Expect_boot_ack	Boot response enable If the software enables this bit and the Enable_boot bit at the same time, the controller detects the boot response signal in "0–1–0" sequence.
[24]	RW	Enable_boot	Boot enable This bit is available when the boot mode is mandatory. If the software enables this bit and the Start_cmd bit, the controller pulls down the CMD signal to start the boot process. The Enable_boot and Disable_boot bits cannot be enabled at the same time.

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[23:22]	RO	reserved	Reserved
[21]	RW	Update_clock_registers_only	Automatic update 0: The normal command sequence is used. That is, the values of MMC_CMD, MMC_CMDARG, MMC_TMOUT, MMC_CTYPE, MMC_BLKSIZ, and MMC_BYTCNT are transferred from the BIU to the CIU. The CIU uses the new values of registers when running new commands. 1: No command is transmitted, and only the clock register values in the card clock domain are updated. The values of MMC_CLKDIV, MMC_CLKSRC, and MMC_CLKENA are transferred to the card clock domain. The card clock can be changed (frequency change and clock enable) even no command is transmitted. Each time the card clock is changed; this bit must be set to 1. In this case, no command is transmitted to the card, and no command done interrupt is generated.
[20:16]	RW	Card_number	Serial number of the card that is being used
[15]	RW	Send_initialization	Whether to transmit the initialization sequence 0: do not transmit the initialization sequence before transmitting the Send_initialization command (high level in 80 clock cycles) 1: transmit the initialization sequence before transmitting the Send_initialization command When a card is powered on, the initialization sequence must be transmitted for initialization before any command is transmitted. That is, this bit must be set to 1.
[14]	RW	Stop_abort_cmd	Whether to transmit the stop/abort command when data is being transferred in open-ended mode or in fixed length mode. 0: do not transmit the stop/abort command 1: transmit the stop/abort command for stopping the current data transfer
[13]	RW	wait_prvdata_complete	Whether to transmit a command immediately 0: transmit a command immediately even though the previous data transfer is not complete 1: transmit a command only when the previous data transfer is complete The typical value is 0. If this bit is set to 0, the transfer status can be read during data transfer, and the interrupt transfer is supported.
[12]	RW	Send_auto_stop	Whether to transmit the stop command 0: do not transmit the stop command after data transfer 1: transmit the stop command after data transfer In non-data transfer mode, this bit is ignored.

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[11]	RW	Transfer_mode	Transfer mode 0: block transfer mode 1: stream transfer mode In non-data transfer mode, this bit is ignored.
[10]	RW	Read_write	Read/write control 0: read data from the card 1: write data to the card In non-data transfer mode, this bit is ignored.
[9]	RW	data_transfer_expected	Data transfer indicator 0: No data is output from the card. 1: Data is output from the card.
[8]	RW	Check_response_crc_	Whether to perform the CRC check 0: Do not check the CRC response. 1: Check the CRC response. No valid CRC is returned when some commands are responded. To prevent the host from performing CRC, the software needs to disable this function based on related commands.
[7]	RW	Response_length	Response length 0: Short responses are output from the card 1: Long responses are output from the card The length of a long response is 128 bits, whereas the length of a short response is 32 bits.
[6]	RW	Response_expect	Whether to output response. 0: No response is output from the card. 1: Responses are output from the card.
[5:0]	RW	Cmd_index	Command index.

MMC_RESP0

MMC_RESP0 is response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response0	Bit[31:0] of a response

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MMC_RESP1

MMC_RESP1 is response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response1	Bit[63:32] of a long response After the CIU transmits an auto-stop command, the corresponding response is stored in this register, and the response to the previous command is still stored in MMC_RESP0. The auto-stop command is available only during data transfer, and the corresponding response is always a short response.

MMC_RESP2

MMC_RESP2 is response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response2	Bit[95:64] of a long response

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MMC_RESP3

MMC_RESP3 is response register 3.

Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Response3							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	Response3	Bit[127:96] of a long response

MMC_MINTSTS

MMC_MINTSTS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17	16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				Sdio_interrupt	Int_status			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	Sdio_interrupt	SDIO interrupt mask status The SDIO interrupt is valid only when MMC_INTMASK [sdio_int_mask] is enabled. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card.
[15:0]	RO	Int_status	Status of each interrupt Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC)

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			Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_RINTSTS

MMC_RINTSTS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17	16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				Sdio_interrupt	Int_status			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	Sdio_interrupt	Raw SDIO interrupt status 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card. The value of the interrupt status bit is independent of the interrupt mask status.
[15:0]	RW	Int_status	Raw status of each interrupt. Writing 1 clears the bits, and writing 0 has no effect. The value of the interrupt status bit is independent of the interrupt mask status. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DRTO)/Boot Data Start (BDS) Bit[8]: response timeout (RTO)/Boot Ack Received (BAR) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR)

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			Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_STATUS

MMC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				FIFO_count												Response_index					data_state_mc_busy	Data_busy	Data_3_status	Commandfsm_states				Fifo_full	Fifo_empty	Fifo_tx_watermark	Fifo_rx_watermark
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:17]	RO	FIFO_count	FIFO count
[16:11]	RO	Response_index	Serial number of the previous response, including the response to the auto-stop command
[10]	RO	data_state_mc_busy	0: The data TX/RX state machine is idle. 1: The data TX/RX state machine is busy.
[9]	RO	Data_busy	This field value depends on the reverse level of DATA0. 0: idle (DATA0 is high level) 1: busy (DATA0 is low level)
[8]	RO	Data_3_status	Card detection signal. This field value depends on the level of DATA3. 0: No card is inserted (DATA3 is low level). 1: A card is inserted (DATA3 is high level).
[7:4]	RO	Commandfsm_states	Status of the command state machine 0x0: idle 0x1: send init sequence 0x2: Tx cmd start bit 0x3: Tx cmd tx bit 0x4: Tx cmd index + arg 0x5: Tx cmd crc7

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			0x6: Tx cmd end bit 0x7: Rx resp start bit 0x8: Rx resp IRQ response 0x9: Rx resp tx bit 0xA: Rx resp cmd idx 0xB: Rx resp data 0xC: Rx resp crc7 0xD: Rx resp end bit 0xE: Cmd path wait NCC 0xF: wait, CMD-to-response turnaround
[3]	RO	Fifo_full	FIFO full flag 0: empty 1: full
[2]	RO	Fifo_empty	FIFO empty flag 0: not empty 1: empty
[1]	RO	Fifo_tx_watermark	Whether the FIFO reaches the TX threshold 0: no 1: yes
[0]	RO	Fifo_rx_watermark	Whether the FIFO reaches the RX threshold 0: no 1: yes

MMC_FIFOTH

MMC_FIFOTH is a FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x60FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	Multiple_Transaction_Size			RX_Wmark												reserved				TX_Wmark											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

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[30:28]	RW	Multiple_Transaction_Size	Transferred burst length 000: 1; 001: 4; 010: 8; 011: 16; 100: 32; 101: 64; 110: 128; 111: 256.
[27:16]	RW	RX_Wmark	FIFO threshold during data read. If the data amount in the FIFO is above the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: RX_WMark ≤ FIFO_DEPTH – 2 Recommendation: A request is raised when the value of [(FIFO_DEPTH/2) – 1] is above the threshold.
[15:12]	RO	reserved	Reserved
[11:0]	RW	TX_Wmark	FIFO threshold during data transmission. If the data amount in the FIFO is below the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: TX_WMark ≤ FIFO_DEPTH – 2 Recommendation: This field must be less than or equal to FIFO_DEPTH/2.

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MMC_CDETECT

MMC_CDETECT is a card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Card_detect_n
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	Card_detect_n	Card detection signal The value depends on the SDIO_CARD_DETECT pin.

MMC_WRTPRT

MMC_WRTPRT is a card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Write_protect
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	Write_protect	Card write protection signal The value depends on the SDIO_CWPR pin.

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MMC_TCBCNT

MMC_TCBCNT is a count of bytes transmitted to the card register.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_card_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_card_byte_count	Count of bytes transmitted from the CIU to the card When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_TBBCNT

MMC_TBBCNT is a count of bytes transmitted from the BIU FIFO register.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_count	Count of bytes transferred between the CPU/DMA and BIU FIFO. When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

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MMC_DEBNCE

MMC_DEBNCE is a dejitter count register.

Offset Address	Register Name	Total Reset Value
0x0064	MMC_DEBNCE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								debounce_count																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	debounce_count	Number of bus clock cycles used by the dejitter filter logic. Generally, the dejitter duration ranges from 5 ms to 25 ms.

MMC_UHS_REG

MMC_UHS_REG is a UHS-1 register.

Offset Address	Register Name	Total Reset Value
0x0074	MMC_UHS_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															ddr_reg	reserved															volt_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	ddr_reg	DDR mode control 0: non-DDR mode 1: DDR mode
[15:1]	RO	reserved	Reserved
[0]	RW	volt_reg	Voltage mode control 0: 3.3 V 1: 1.8 V

MMC_BMOD

MMC_BMOD is a bus mode register.

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Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					PBL			DE	DSL					FB	SWR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	PBL	Length of the IDMAC burst transfer. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 256
[7]	RW	DE	IDMAC enable. 0: disabled 1: enabled
[6:2]	RW	DSL	Span between two descriptors, that is, number of words between two non-linked descriptors. This bit is valid only for the dual-buffer descriptor.
[1]	RW	FB	Fixed burst length type. 0: single and INCR burst types 1: single, INCR4, INCR8, and INCR16 burst types
[0]	RW	SWR	Soft reset control for the internal register of the IDMAC. 0: not reset 1: reset After reset, this bit is automatically cleared one clock cycle later.

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MMC_PLDMND

MMC_PLDMND is a poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	PD	If DES0[OWN] is 0, the IDMAC enters the suspend state. The CPU can write any value to this register to enable the IDMAC to obtain descriptors again.

MMC_DBADDR

MMC_DBADDR is a base address register of the descriptor linked list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	SDL	Start address of the descriptor linked list, that is, the base address of the first descriptor.

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MMC_IDSTS

MMC_IDSTS is an IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																FSM				EB		AIS	NIS	reserved		CES	DU	reserved	FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:13]	RO	FSM	Current state of the IDMAC state machine. 0x0: DMA_IDLE 0x1: DMA_SUSPEND 0x2: DESC_RD 0x3: DESC_CHK 0x4: DMA_RD_REQ_WAIT 0x5: DMA_WR_REQ_WAIT 0x6: DMA_RD 0x7: DMA_WR 0x8: DESC_CLOSE Other values: reserved
[12:10]	RW	EB	Bus error type. 001: The transmit operation is aborted. 010: The receive operation is aborted. Other values: reserved
[9]	RW	AIS	Abnormal total interrupt. The value of this bit is obtained after the values of FBE, DU, and CES bits are ORed. Writing 1 clears this bit.
[8]	RW	NIS	Normal total interrupt. The value of this bit is obtained after the values of the TI and RI bits are ORed. Writing 1 clears this bit.
[7:6]	RO	reserved	Reserved
[5]	RW	CES	Card error indicator. This bit indicates the card status when data is being received.
[4]	RW	DU	Descriptor invalid interrupt. When DES0[OWN] is 0, this bit is set to 1. Writing 1 clears this bit.
[3]	RO	reserved	Reserved

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[2]	RW	FBE	Fatal bus error interrupt. If this bit is set to 1, the IDMAC stops all accesses through the bus. Writing 1 clears this bit.
[1]	RW	RI	Receive done interrupt. This bit indicates that the data of a descriptor is received. Writing 1 clears this bit.
[0]	RW	TI	Transmit done interrupt. This bit indicates that a descriptor finishes transmitting data. Writing 1 clears this bit.

MMC_IDINTEN

MMC_IDINTEN is an IDMAC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						AI	NI	reserved		CES	DU	reserved	FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	AI	Abnormal interrupt enable. 0: disabled 1: The FBE, DU, and CES interrupts are enabled.
[8]	RW	NI	Normal interrupt enable. 0: disabled 1: The TI and RI interrupts are enabled.
[7:6]	RO	reserved	Reserved
[5]	RW	CES	Card error interrupt enable. 0: disabled 1: enabled
[4]	RW	DU	Descriptor invalid interrupt enable. 0: disabled 1: enabled
[3]	RO	reserved	Reserved
[2]	RW	FBE	Fatal bus error interrupt enable. 0: disabled 1: enabled

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[1]	RW	RI	RX interrupt enable. 0: disabled 1: enabled
[0]	RW	TI	TX interrupt enable. 0: disabled 1: enabled

MMC_DSCADDR

MMC_DSCADDR is an address register of the current descriptor.

Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HAD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HAD	Descriptor pointer. The value is automatically refreshed during data transfer. The register points to the start address of the descriptor that will be used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is an address register of the current data buffer.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HBA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HBA	Data buffer pointer. The value is automatically refreshed during data transfer. The register points to the start address of the data buffer that is being used by the IDMAC.

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MMC_CARDTHRCTL

MMC_CARDTHRCTL is a threshold control register.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_CARDTHRCTL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved	cardrdthreshold			reserved				BsyClrIntEn	cardrdthr_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cardrdthreshold	Read threshold The maximum value is 512.
[15:2]	RO	reserved	Reserved
[1]	RW	BsyClrIntEn	Busy clear interrupt enable 0: disabled 1: enabled
[0]	RW	cardrdthr_en	Read threshold enable 0: disabled 1: enabled

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MMC_UHS_REG_EXT

MMC_UHS_REG_EXT is a UHS extension register.

Offset Address	Register Name	Total Reset Value
0x0108	MMC_UHS_REG_EXT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	clk_drv_phase_ctrl	reserved	clk_smpl_phase_ctrl	reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:23]	RW	clk_drv_phase_ctrl	clk_in_drv clock phase control 3'b000: 0° 3'b001: 45° 3'b010: 90° 3'b011: 135° 3'b100: 180° 3'b101: 225° 3'b110: 270° 3'b111: 315°
[22:19]	RO	reserved	Reserved
[18:16]	RW	clk_smpl_phase_ctrl	clk_in_sample clock phase control 3'b000: 0° 3'b001: 45° 3'b010: 90° 3'b011: 135° 3'b100: 180° 3'b101: 225° 3'b110: 270° 3'b111: 315°
[15:0]	RO	reserved	Reserved

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MMC_DDR_REG

MMC_DDR_REG is a DDR start bit detection control register.

Offset Address	Register Name	Total Reset Value
0x010C	MMC_DDR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															half_start_bit
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	half_start_bit	When this bit is set to 1'b1, RINTSTS[15] is set to 1 when CMD12 is received in DDR mode.

MMC_ENABLE_SHIFT

MMC_ENABLE_SHIFT is a phase shift register.

Offset Address	Register Name	Total Reset Value
0x0110	MMC_ENABLE_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable Phase Shift Register
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

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[1:0]	RW	Enable Phase Shift Register	Phase shift control 00: default phase shift 01: Phase shift on the next rising edge 10: Phase shift on the next falling edge 11: Reserved

MMC_DATA

MMC_DATA is a data register (entrance address of the FIFO). The FIFO overflow must be read first before the data is read from or written to the FIFO.

Offset Address	Register Name	Total Reset Value
0x0200	MMC_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data	Address for reading/writing to the FIFO. If the address ranges from 0x200 to 0x200 + FIFO_DEPTH, the FIFO is selected.

13.5 IR Interface

13.5.1 Overview

The infrared (IR) module receives data over the IR interface.

13.5.2 Features

The IR module has the following features:

- Allows you to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the RX data overflow interrupt, RX data frame format error interrupt, RX data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the RX symbol overflow interrupt, RX symbol interrupt, symbol timeout interrupt, and combined interrupt.
- Supports the query of the raw interrupt status and the masked interrupt status.

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- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.
- Supports the reference clock frequency ranging from 1 MHz to 128 MHz and controls the clock frequency divider by software programming, enabling the frequency of the working clock to be prescaled to 1 MHz.

13.5.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the ARM system. The ARM system performs corresponding operations according to the received codes, which implements expected functions. The IR module connects to the APB of the ARM subsystem. When the chip is in the low-power state (the CPU is at a low frequency), the IR module generates an interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Table 13-16 to Table 13-18 describe the code formats of the received infrared data.

NOTE

The values in Table 13-16 to Table 13-18 indicate previously measured values and may be inaccurate. Therefore, they are only for reference. You are advised to use the actual tested data when using the chip.

Table 13-16 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		NEC with Simple Repeat Code			
		uPD6121G	D6121/BU5777/D1913	LC7461M-C13	AEHA
Lead code (10 μs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 μs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 μs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 μs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 μs)		55	55	55	42.2
Frame length (10 μs)		108,00	10,800	10,800	8,777.6 – 12,828.8

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Data Format	NEC with Simple Repeat Code			
	uPD6121G	D6121/BU5777/D1913	LC7461M-C13	AEHA
Valid data bit	32	32	42	48

Table 13-17 Code formats of the received infrared data (NEC with full repeat code)

Data Format		NEC with Full Repeat Code						
		uPD6121G	LC7461M-C13	MN6024-C5D6	MN6014-C6D6	MATNEW	MN6030	PANASONIC
Lead code (10 µs)	LEAD_S	900	900	337.6	349.2	348.8	349	352
	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 µs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 µs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 µs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 µs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400
Valid data bit		32	42	22	24	48	22	22

Table 13-18 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 µs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 µs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 µs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60

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Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 µs)		56	None	None	None	None
Frame length (10 µs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

13.5.3.1 NEC with Simple Repeat Code

Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

Figure 13-31 shows the frame format of transmitting a single NEC with simple repeat code.

Figure 13-31 Frame format for transmitting a single NEC with simple repeat code

If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure 13-32 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 13-32 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously

Code Format

Figure 13-33 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

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Figure 13-33 Definitions of bit0 and bit1 of the NEC with simple repeat code

Figure 13-34 shows the format for transmitting a single NEC with simple repeat code. Figure 13-35 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 13-34 Format for transmitting a single NEC with simple repeat code

Figure 13-35 Code format for transmitting consecutive NEC with simple repeat codes

NOTE

- The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-16 to Table 13-18.
- The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

13.5.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, its LSB is received first. Burst signal: It is used to receive the last data bit. Figure 13-36 shows the frame format for transmitting a single NEC with full repeat code.

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Figure 13-36 Frame format for transmitting a single NEC with full repeat code

If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 13-37 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 13-37 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

Figure 13-36 and Figure 13-37 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

Code Format

Figure 13-38 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 13-38 Definitions of bit0 and bit1 of the NEC with full repeat code

Figure 13-39 shows the format for transmitting a single NEC with full repeat code.

Figure 13-39 Format for transmitting a single NEC with full repeat code

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NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-16 to Table 13-18.

13.5.3.3 TC9012 Code

Frame Format

CAUTION

According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

Figure 13-40 shows the frame format for transmitting a single TC9012 code.

Figure 13-40 Frame format for transmitting a single TC9012 code

When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 13-41 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 13-41 Frame format for transmitting TC9012 codes by pressing the key continuously

Code Format

Figure 13-42 shows the definitions of bit0 and bit1 of the TC9012 code.

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Figure 13-42 Definitions of bit0 and bit1 of the TC9012 code

Figure 13-43 shows the format for transmitting a single TC9012 code.

Figure 13-43 Format for transmitting a single TC9012 code

Figure 13-44 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

Figure 13-44 Format for transmitting consecutive TC9012 codes (C0 = 1)

Figure 13-45 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 13-45 Format for transmitting consecutiveTC9012 codes (C0 = 0)

NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-16 to Table 13-18. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

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13.5.3.4 SONY Code

Frame Format

A SONY code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

During reception, the LSB is received first. Figure 13-46 shows the frame format for transmitting a single SONY code.

Figure 13-46 Frame format for transmitting a single SONY code

When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 13-47 shows the frame format for continuously transmitting SONY codes by pressing the key.

Figure 13-47 Frame format for continuously transmitting SONY codes by pressing the key

Code Format

Figure 13-48 shows the definitions of bit0 and bit1 of a SONY code.

Figure 13-48 Definitions of bit0 and bit1 of a SONY code

NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-16 to Table 13-18.

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13.5.4 Operating Mode

Soft Reset

When PERI_CRG24[ir_srst_req] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 13-49 shows the process of initializing the IR module.

Figure 13-49 Process of initializing the IR module

To initialize the IR module, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Set IR_EN bit [0] to 1 to enable the IR receive module.

Step 3 Read IR_BUSY to check the current status of the IR module.

- If the value of IR_BUSY is 1, the IR module is busy. Then continue to read IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.

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- If the value of is 0, the IR module is idle. Then go to Step 4.

Step 4 Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK. Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.

Step 5 Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

----End

Figure 13-50 Process of reading the decoded data

To read the decoded data, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Wait in interrupt or query mode until data frames are received.

- In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[intms_rcv]. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, repeat Step 2 to wait for an interrupt.
- In query mode, continuously read the value of IR_INT_STATUS[intrs_rcv] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, the IR module does not receive any data frame. Then, repeat Step 2 to continue the query.

Step 3 Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.

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Step 4 Read IR_DATAL.

Step 5 Clear the data receive interrupt.

----End

13.5.5 Register Summary

Table 13-19 describes IR registers.

Table 13-19 Summary of IR registers (base address: 0x2007_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	13-128
0x004	IR_CFG	IR configuration register	13-128
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-130
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-131
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-132
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-133
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-134
0x01C	IR_BUSY	Configuration busy flag register	13-135
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)	13-136
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR received symbol width register (IR_CFG[ir_mode] = 1)	13-137
0x028	IR_INT_MASK	IR interrupt mask register	13-137
0x02C	IR_INT_STATUS	IR interrupt status register	13-139
0x030	IR_INT_CLR	IR interrupt clear register	13-141
0x034	IR_START	IR start configuration register	13-143

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13.5.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

CAUTION

Before configuring other registers, you must set IR_EN[ir_en] to 1 by using software. When IR_EN[ir_en] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ir_en	IR receive module enable. 0: disabled 1: enabled.

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before configuring this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value is retained after configuration.

The reference clock frequency supported by the IR module ranges from 1 MHz to 128 MHz. The relationship between the frequency and the clock frequency divider ir_freq is as follows:

- When the reference clock frequency is 1 MHz, ir_freq must be set to 0x00.
- If the reference clock frequency is 128 MHz, ir_freq must be set to 0x7F.

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When the frequency of the IR reference clock is not an integer ranging from 1 MHz to 128 MHz, the clock frequency divider is rounded off. For example, if the reference clock frequency is 12.1 MHz, the clock frequency divider is 0x0B; if the reference clock frequency is 12.8 MHz, the clock frequency divider is 0x0C.

The relationship between the frequency offset and the count deviation is as follows: If the base frequency is f and the frequency variation is D_f, the frequency offset ratio is D_f/f. If the count deviation of the counter is Dcnt, and the judge level width is s (in µs), the count deviation Dcnt is calculated as follows: Dcnt = |0.1 x s x ratio|Therefore, when the clock has frequency offset, the valid range of the parameter value needs to be changed. If the frequency increases, the corresponding margin range is changed to [min + Dcnt, max + Dcnt]. Where, min and max indicate the margins without frequency offset. If the frequency decreases, the offset range is changed to [min – Dcnt, max – Dcnt]. Take the margin of the start bit in the lead code as an example. If the base frequency is 100 MHz, and the frequency increases by 0.1 MHz, then the ratio is 0.001 (0.1/100). Assume that s is 9000 µs. Dcnt is calculated as follows: Dcnt = |0.1 x 9,000 x 0.001| = 1. In this case, the margin range of ir_leads must be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14	13 12	11 10 9 8	7	6 5 4	3 2 1 0
Name	ir_max_level_width				ir_format	ir_bits		ir_mode	ir_freq	
Reset	0 0 1 1	1 1 1 0	1 0 0 0	0 0 0 0	0 0	0 1	1 1 1 1	0	0 0 0	1 0 1 1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[ir_mode] is 0. Indicates the maximum level width (in 10 µs) of a symbol whenIR_CFG[ir_mode] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Indicates the data code format when IR_CFG[ir_mode] is 0. 00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 13-16 to Table 13-18. Indicates the symbol format when IR_CFG[ir_mode] is 1. bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.
[13:8]	RW	ir_bits	Indicates the number of data bits in a frame when IR_CFG[ir_mode] is 0. 0x00–0x2F: 1–48 data bits in a frame 0x30–0x3F: reserved

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			If ir_bits is set to a value ranging from 0x30 to 0x3F by using software, the setting has no effect and the original value is retained. Indicates the symbol receive interrupt threshold when IR_CFG[ir_mode] is 1. bit[13]: reserved bit[12:8]: 0x0–0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode. 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock. 0x00–0x7F: correspond to the working clock divider 1–128 respectively.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set Register Description[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specified code types, see the values of LEAD_S in Table 13-16 to Table 13-18.

- For a pulse width whose typical value is greater than or equal to 400 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC

- For a pulse width whose typical value is less than 400 (10 µs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example. If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

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Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved						cnt_leads_min										reserved						cnt_leads_max									
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code 0x000–0x007: reserved
[15:10]	RO	reserved	Reserved
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code 0x000–0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 13-16 to Table 13-18.

- For the pulse width whose typical values is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6
- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

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cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leade_min								reserved								cnt_leade_max							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code 0x000–0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 13-16 to Table 13-18.

- For a pulse width whose typical value is greater than or equal to 225 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3

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- For a pulse width whose typical value is less than 225 (10 µs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cnt_sleade_min		reserved		cnt_sleade_max	
Reset	0 0 0 0	0 0 0 0	1 1 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code 0x000–0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type to accurately judging bit0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 13-16 to Table 13-18. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 µs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

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cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43

- For details about the typical value of the SONY code, see the values of B0_L in Table 13-16 to Table 13-18. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0 0x000–0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 13-16 to Table

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13-18. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB

- For details about the typical value of the SONY code, see the values of B1_L in Table 13-16 to Table 13-18. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved								cnt1_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1 0x000–0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

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[0]	RO	ir_busy	Busy status flag 0: idle. In this case, software can configure data. 1: Indicates the busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 13-16 to Table 13-18.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	ir_datah	Indicates the upper 16 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the symbol count in the symbol FIFO when IR_CFG[ir_mode] is 1. bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO

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IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR receive symbol width register (IR_CFG[ir_mode] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Indicates the lower 32 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the width of the symbol received by the IR module when IR_CFG[ir_mode] is 1. The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

CAUTION

- Before setting this register, you must set IR_EN[ir_en] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[ir_mode] is 0, IR_INT_MASK bit[3:0] are valid; when IR_CFG[ir_mode] is 1, IR_INT_MASK bit[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- RX data overflow interrupt

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If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw RX data overflow error interrupt is reported.

- RX data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw RX frame format error interrupt is reported.

- RX data frame interrupt

  After a complete frame data is received, a raw RX data frame interrupt is reported.

- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.

- RX symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw RX symbol overflow error interrupt is reported.

- RX symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw RX symbol interrupt is reported.

- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_frame_error	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked

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[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[16]	RW	intm_symb_rcv	RX N symbol interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[15:4]	-	reserved	Reserved
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[2]	RW	intm_overflow	RX data overflow interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[1]	RW	intm_frame_error	RX data frame format error interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[0]	RW	intm_rcv	RX data frame interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked

IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

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Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_frame_error	intms_rcv	reserved				intrs_overrun	intrs_time_out	intrs_symb_rcv		reserved				intrs_release	intrs_overflow	intrs_frame_error	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	intms_symb_rcv	Masked RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	RO	reserved	Reserved
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	intms_overflow	Masked RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	intms_frame_error	Masked RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	RO	reserved	Reserved.

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[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	RO	reserved	Reserved
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	intrs_frame_error	Raw RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.

IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_CLR bit[3:0] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_CLR bit[18:16] are valid.

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Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_frame_error	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	WC	intc_overrun	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared
[16]	WC	intc_symb_rcv	When IR_CFG[ir_mode] is 1, this bit indicates whether the RX symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	RO	reserved	Reserved
[3]	WC	intc_release	When IR_CFG[ir_mode] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared
[2]	WC	intc_overflow	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data overflow error interrupt request is cleared. 0: no effect 1: cleared
[1]	WC	intc_frame_error	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame format error interrupt request is cleared. 0: no effect 1: cleared

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[0]	WC	intc_rcv	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame interrupt request is cleared. 0: no effect 1: cleared If an RX data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	ir_start	IR start configuration register

13.6 GPIO

13.6.1 Overview

The Hi3516A supports 16 groups of general purpose input/output (GPIO) pins, that is, GPIO0 to GPIO15. Each group of GPIO pins provides eight programmable input/output pins (GPIO15 has only three pins). Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

The GPIO can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) signal provides an indicator to the interrupt controller, indicating that an interrupt occurs.

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CAUTION

- For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins, see chapter 2 "Hardware." For details about control modes, see section 2.3 "Pin Multiplexing Registers."
- For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.
- The power of the pins SDIO0_CCLK_OUT, SDIO0_CCMD, and SDIO0_CDATA0–3 (corresponding to GPIO2_0, GPIO2_4, GPIO2_5, GPIO2_6, GPIO2_7, and GPIO1_1) are supplied by power switch 0 in the chip. Therefore, when these pins function as GPIO pins, MISC_CTRL3[powerswitch0_sel_mux] needs to be set to 0x1 so that power switch 0 is controlled by the MISC_CTRL3 register. If these pins need to support the 3.3 V voltage, MISC_CTRL3[powerswitch0_sel] needs to be set to 0x0. If these pins need to support the 1.8 V voltage, MISC_CTRL3[powerswitch0_sel] needs to be set to 0x1 and the power pin DVDD18_SDIO needs to connect to the 1.8 V power.
- The power of the pins SDIO1_CCLK_OUT, SDIO1_CCMD, and SDIO1_CDATA0–3 (corresponding to GPIO11_0, GPIO11_4, GPIO11_5, GPIO11_6, GPIO11_7, and GPIO1_2) are supplied by power switch 1 in the chip. Therefore, when these pins function as GPIO pins, MISC_CTRL3[powerswitch1_sel_mux] needs to be set to 0x1 so that power switch 1 is controlled by the MISC_CTRL3 register. If these pins need to support the 3.3 V voltage, MISC_CTRL3[powerswitch1_sel] needs to be set to 0x0. If these pins need to support the 1.8 V voltage, MISC_CTRL3[powerswitch1_sel] needs to be set to 0x1 and the power pin DVDD18_SDIO needs to connect to the 1.8 V power.

13.6.2 Features

Each GPIO pin can be configured as input or output.

- As input, each GPIO pin can act as an interrupt source.
- As output, each GPIO can be set to 0 or 1 separately.

13.6.3 Operating Mode

Interface Reset

The GPIO is reset during chip power-on reset or system reset, and GPIO pins are in input state after being reset.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

Step 1 Enable the required GPIO pins by configuring corresponding pins according to the description of multiplexing registers.

Step 2 Configure the GPIO as input or output by using the GPIO_DIR register.

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Step 3 When the GPIO pins are in input mode, read the GPIO_DATA register to check the input signal value. When the GPIO pins are in output mode, write the output value to the GPIO_DATA register to control the output level of the GPIO pins.

---End

CAUTION

When the GPIO pins are in output mode, do not enable the GPIO interrupt. Otherwise, the GPIO interrupt will be generated when output signals meet interrupt generation conditions.

Interrupt Operation

The GPIO interrupt is controlled through seven registers (such as GPIO_IS). These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of the GPIO, see section 3.3 "Interrupt Systems."

When multiple interrupts are generated at the same time, these interrupts are combined into an interrupt and then reported. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt Systems."

The

GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status, respectively. GPIO_IEV controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status.

Perform the following operations to configure GPIO pins to the interrupt mode:

Step 1 Select the edge-sensitive mode or level-sensitive mode by configuring the

Step 2 GPIO_IS register.

Step 3 Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.

Step 4 If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

Step 5 Write 0xFF to the GPIO_IC register to clear the interrupt.

Step 6 Set the GPIO_IE to 1 to enable the interrupt.

---End

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CAUTION

Ensure that data in GPIO pins is stable during initialization to prevent pseudo interrupts.

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

13.6.4 Register Summary

Table 13-20 lists the base addresses for 16 groups of GPIO registers.

Table 13-20 Base addresses for 16 groups of GPIO registers

Register	Base Address
GPIO15	0x2026_0000
GPIO14	0x2022_0000
GPIO13	0x2021_0000
GPIO12	0x2020_0000
GPIO11	0x201F_0000
GPIO10	0x201E_0000
GPIO9	0x201D_0000
GPIO8	0x201C_0000
GPIO7	0x201B_0000
GPIO6	0x201A_0000
GPIO5	0x2019_0000
GPIO4	0x2018_0000
GPIO3	0x2017_0000
GPIO2	0x2016_0000
GPIO1	0x2015_0000
GPIO0	0x2014_0000

Table 13-21 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO15 also have the same internal GPIO registers.

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NOTE

- Register address of GPIOn = GPIOn base address + Offset address of the register
- The value of n ranges from 0 to 15.

Table 13-21 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000–0x3FC	GPIO_DATA	GPIO data register	13-147
0x400	GPIO_DIR	GPIO direction control register	13-148
0x404	GPIO_IS	GPIO interrupt trigger register	13-149
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	13-149
0x40C	GPIO_IEV	GPIO interrupt trigger event register	13-150
0x410	GPIO_IE	GPIO interrupt mask register	13-150
0x414	GPIO_RIS	GPIO raw interrupt status register	13-150
0x418	GPIO_MIS	GPIO masked interrupt status register	13-151
0x41C	GPIO_IC	GPIO interrupt clear register	13-151

13.6.5 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example:

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA bit[7:0] are valid.

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- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA bit[7] is valid.

Offset Address	Register Name	Total Reset Value
0x000–0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit can be controlled separately. 0: input 1: output

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GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

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GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							

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Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: No interrupt occurs. 1: An interrupt is generated.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid. 1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: no effect

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			1: cleared

13.7 USB 2.0 Host

13.7.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using in the controller, the following functions are achieved:

- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.
- Provide interfaces (such as the interrupt vector interface) for the driver.

The USB 2.0 device controller supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s) data transfer modes. It also supports host/device intelligent switching.

13.7.2 Function Description

Logic Block Diagram

Figure 13-51 shows the logic block diagram of the USB 2.0 host controller.

Figure 13-51 Logic block diagram of the USB 2.0 host controller

Figure 13-52 shows the logic block diagram of the USB 2.0 device.

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Figure 13-52 Logic block diagram of the USB 2.0 device controller

NOTE

- UTMI: USB2.0 transceiver macrocell interface
- EHCI: enhanced host controller interface
- OHCI: open host controller interface

Typical Application

Figure 13-53 shows the reference design of the USB 2.0 host controller.

CAUTION

- The impedance of DP or DM is 45 Ω ±1% and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electro static discharge (ESD) components are used, 1 pF capacitors are recommended.

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Figure 13-53 Reference design of the USB 2.0 host controller

Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

The USB 2.0 device controller has the following features:

- Complies with the USB 2.0 standard.
- Supports high-speed, full-speed, and low-speed devices.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.

Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode applies to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.
- Bulk transfer

  This mode applies to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and

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many data transfers are delayed. Bulk transfer can be performed after all other types of data transfers are complete. In bulk transfer mode, data is transferred between the USB Host and USB Device without errors by using an error detection and retransmission mechanism.

- Isochronous transfer

  This mode applies to the stream data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

  This mode applies to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

13.7.3 Operating Mode

Host/Device Switching

You can configure the MISC_CTRL30[usb_chipid] to operate in host or device mode.

To enable the register to operate in host mode, set MISC_CTRL30[usb_chipid] to 0 and MISC_CTRL30[usb2_phy_dmpulldown] and MISC_CTRL30[usb2_phy_dppulldown] to 1.

To enable the register to operate in device mode, set MISC_CTRL30[usb_chipid] to 1 and MISC_CTRL30[usb2_phy_dmpulldown] and MISC_CTRL30[usb2_phy_dppulldown] to 0.

Pin Polarity Control

The valid polarity of USB_PWREN can be configured by setting MISC_CTRL30[usbpwr_p_ctrl].

The valid polarity of USB0_OVRCUR and USB1_OVRCUR can be configured by setting MISC_CTRL30[usbovr_p_ctrl].

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

Step 1 Write 1 to PERI_CRG46 [usbphy_port0_treq], PERI_CRG46[usbphy_req], PERI_CRG46[usb_ctrl_utmi0_req], PERI_CRG46[usb_ctrl_hub_req], and PERI_CRG46[usb_ahb_srst_req] respectively to reset the USB controller and PHY.

Step 2 Set PERI_CRG46 [usb_cken] to 0 to disable the clocks of the USB 2.0 host controller.

---End

To enable the clock, perform the following steps:

Step 1 Set PERI_CRG46 [usb_cken] to 1 to enable the clocks of the USB 2.0 host controller.

Step 2 Deassert the reset on the USB controller and PHY. For details, see "Reset Deassert"

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---End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

Step 1 Delay at least 10 μs.

Step 2 Write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the soft reset on USB PHY port0.

Step 3 Write 0 to PERI_CRG46[usbphy_req] and PERI_CRG46 [usb_otg_phy_srst_req] to deassert the reset on the USB PHY.

Step 4 After 250 μs delay, write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the soft reset on USB controller port0; write 0 to PERI_CRG46[usb_ctrl_hub_req] to deassert the soft reset on the hub of the USB controller.

Step 5 Write 0 to PERI_CRG46[usb_ahb_srst_req] to deassert the soft reset on the USB bus.

---End

Separately Resetting Ports During the Working Process

To reset port separately during the working process, perform the following steps:

Step 1 Write 1 to PERI_CRG46[usb_ctrl_utmi0_req] to soft-reset port0 of the USB controller.

Step 2 Write 1 to PERI_CRG46[usbphy_port0_treq] and PERI_CRG46 [usb_otg_phy_srst_req] to soft-reset port0 of the USB PHY.

Step 3 After 200 μs delay, write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the reset on port0 of the USB PHY.

Step 4 Write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the reset on port0 of the USB controller.

---End

Variables in the Offset Addresses for USB 2.0 Registers

Table 13-22 describes the value ranges and meanings of the variables in the offset addresses of registers.

Table 13-22 Variables in the offset addresses for USB 2.0 registers

Variable	Value Range	Description
FIFO_num	0–14	Number of FIFOs
n	0–15	Endpoint *n*

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13.7.4 Register Summary

USB HOST Register

Table 13-23 describes USB 2.0 registers.

Table 13-23 Summary of USB 2.0 registers (base address: 0x1004_0000)

Offset Address	Register	Description	Page
0x90	INTNREG00	Micro-frame length configuration register	13-160
0x94	INSNREG01	PBUF OUT/IN register	13-161
0x98	INSNREG02	PBUF depth register	13-161
0x9C	INSNREG03	Interrupt memory transfer enable register	13-161
0xA0	INTNREG04	Debug register	13-162
0xA4	INTNREG05	UTMI Vendor control and status register	13-163
0xA8	INTNREG06	AHB error status register	13-164
0xAC	INTNREG07	AHB error address register	13-164

NOTE

The base address of the EHCI register is 0x100B_0000 and the base address of the OHCI register is 0x100A_0000. The base address of Table 13-23 is that of the EHCI register.

USB Device Register Overview

Table 13-24 describes the UBS device register overview.

Table 13-24 USB device register overview (base address: 0x1008_0000)

Offset Address	Name	Description	Page
0x0000	GOTGCTL	Device behavior control and status query register	13-165
0x0004	GOTGINT	Device interrupt generation indicator/clear register	13-167
0x0008	GAHBCFG	AHB configuration register	13-168
0x000C	GUSBCFG	USB configuration register	13-170
0x0010	GRSTCTL	Reset hardware feature register	13-173
0x0014	GINTSTS	System interrupt register	13-176
0x0018	GINTMSK	System interrupt mask register	13-179
0x001C	GRXSTSR	RX status debug read register	13-183

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Offset Address	Name	Description	Page
0x0020	GRXSTSP	RX status read&pop register	13-184
0x0024	GRXFSIZ	RX FIFO size configuration register	13-185
0x0028	GNPTXFSIZ	Non-periodic TX FIFO size configuration register	13-185
0x002C	GNPTXSTS	Non-periodic TX FIFO and non-periodic TX request query register	13-185
0x0030	GI2CCTL	I^2C access register	13-186
0x0034	GPVNDCTL	PHY vendor control register	13-188
0x0038	GGPIO	GPIO register	13-189
0x003C	GUID	User ID query register	13-189
0x0040	GSNPSID	Synopsys ID query register	13-189
0x0044	GHWCFG1	User hardware configuration register 1	13-190
0x0048	GHWCFG2	User hardware configuration register 2	13-190
0x004C	GHWCFG3	User hardware configuration register 3	13-192
0x0050	GHWCFG4	User hardware configuration register 4	13-194
0x0054	GLPMCFG	LPM configuration register	13-196
0x0058	GPWRDN	Power-down register	13-199
0x005C	GDFIFOCFG	DFIFO software configuration register	13-201
0x0060	GADPCTL	ADP timer control and status register	13-202
0x0100	HPTXFSIZ	TX FIFO configuration register	13-204
0x0104 + 0x0004 x FIFO_num	DPTXFSIZN	Device periodic TX FIFO-n size register	13-205
0x0104 + 0x0004 x FIFO_num	DIEPTXFN	Device IN endpoint TX FIFO size register	13-205
0x0800	DCFG	Device configuration register	13-206
0x0804	DCTL	Device control register	13-207
0x0808	DSTS	Device status register	13-209
0x0810	DIEPMSK	Common interrupt mask register for device IN endpoints	13-210
0x0814	DOEPMSK	Common interrupt mask register for device OUT endpoints	13-211
0x0818	DAINT	Interrupt register for all device endpoints	13-212
0x081C	DAINTMSK	Interrupt mask register for all endpoints	13-213

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Offset Address	Name	Description	Page
0x0820	DTKNQR1	Device IN token learning sequence queue read register 1	13-213
0x0824	DTKNQR2	Device IN token learning sequence queue read register 2	13-214
0x0830	DTKNQR3	Device IN token learning sequence queue read register 3	13-215
0x0834	DTKNQR4	Device IN token learning sequence queue read register 4	13-215
0x0828	DVBUSDIS	Device VBUS discharge time register	13-216
0x082C	DVBUSPULSE	Device VBUS pulsing time register	13-216
0x0830	DTHRCTL	Device threshold control register	13-216
0x0834	DIEPEMPMSK	FIFO empty interrupt mask register for device IN endpoints	13-218
0x0838	DEACHINT	Interrupt register for each device endpoint	13-218
0x083C	DEACHINTMSK	Interrupt register for each device endpoint	13-218
0x0840 + (0x0004 x *n*)	DIEPEACHMSKN	Interrupt register for each device IN endpoint-n	13-219
0x0880 + (0x0004 x *n*)	DOEPEACHMSKN	Interrupt register for each device OUT endpoint-n	13-220
0x0900	DIEPCTL0	Control register for device control IN endpoint 0	13-222
0x0B00	DOEPCTL0	Control register for device control OUT endpoint 0	13-224
0x0900 + (0x0020 x *n*)	DIEPCTLN	Device IN endpoint-n control register	13-226
0x0B00 + (0x0020 x *n*)	DOEPCTLN	Device OUT endpoint-n control register	13-229
0x0908 + (0x0020 x *n*)	DIEPINTn	Device IN endpoint-n interrupt register	13-231
0x0B08 + (0x0020 x *n*)	DOEPINTn	Device OUT endpoint-n interrupt register	13-234
0x0910	DIEPTSIZ0	Transfer size register for device IN endpoint 0	13-236
0x0B10	DOEPTSIZ0	Transfer size register for device OUT endpoint 0	13-237
0x0910 + (0x0020 x *n*)	DIEPTSIZn	Transfer size register for device IN Endpoint-n	13-238

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Offset Address	Name	Description	Page
0x0B10 + (0x0020 x *n*)	DOEPTSIZn	Transfer size register for device OUT endpoint-n	13-238
0x0914 + (0x0020 x *n*)	DIEPDMAN	Device IN endpoint-n DMA address register	13-239
0x0B14 + (0x0020 x *n*)	DOEPDMAN	Device OUT endpoint-n DMA address register	13-240
0x091C + (0x0020 x *n*)	DIEPDMABN	Device IN endpoint-n DMA buffer address register	13-240
0x0B1C + (0x0020 x *n*)	DOEPDMABN	Device OUT endpoint-n DMA buffer address register	13-241
0x0938	DTXFSTSn	Device IN endpoint TX FIFO status register	13-241

13.7.5 Register Description

13.7.5.1 USB HOST Register Description

INTNREG00

INTNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		val													en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.
[13:1]	RW	val	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 µs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	en	Micro-frame length register enable. 0: disabled 1: enabled

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INSNREG01

INTNREG01 is a PBUF out/in configuration register.

Offset Address	Register Name	Total Reset Value
0x94	INSNREG01	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_threshold																in_threshold															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	out_threshold	TX threshold. If the data amount in the PBUF is above the TX threshold, data starts to be transmitted. The depth is measured by 32 bits.
[15:0]	RW	in_threshold	RX threshold. If the data amount in the PBUF is above the RX threshold, data is read from the PBUF. The depth is measured by 32 bits.

INSNREG02

INSNREG02 is a PBUF depth configuration register.

Offset Address	Register Name	Total Reset Value
0x98	INSNREG02	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pbuf_depth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	pbuf_depth	PBUF depth. The depth is measured by 32 bits.

INSNREG03

INSNREG03 is an interrupt memory transfer enable register.

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Offset Address	Register Name	Total Reset Value
0x9C	INSNREG03	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	dis	ctrl		val		fetch		offset							brk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	dis	256 MHz clock check enable0: disabled 1: enabled
[13]	RW	ctrl	Line state ignore during TESTSE0 NAK. 0: disabled 1: enabled
[12:10]	RW	val	tx-tx turnaround delay addition
[9]	RW	fetch	Instruction fetching from the periodic frame list, valid only in CONFIG1 mode 0: The controller fetches instructions from the periodic linked list only in micro-frame 0. 1: The controller fetches instructions from the periodic linked list in every micro-frame.
[8:1]	RW	offset	Available time offset.
[0]	RO	brk_en	Interrupt memory transfer enable. 0: disabled 1: enabled

INTNREG04

INTNREG04 is a debug register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_en	nak_reldfix_en	reserved	scaledwn_enum_time	hccparam_en	hcsparam_en

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Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5]	RW	auto_en	Automatic feature enable. 0: enabled. The suspend signal is valid when the run/stop bit is reset by software, but the hchalted bit is not set. 1: disabled. The port is not suspended when software clears the run/stop bit. The default value is 0.
[4]	RW	nak_reldfix_en	NAK reload enable. 0: enabled 1: disabled
[3]	-	reserved	Reserved.
[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable. 0: disabled 1: enabled
[1]	RW	hccparam_en	HCCPARAMS register write enable. 0: disabled 1: enabled
[0]	RW	hcsparam_en	HCSPARAMS register write enable. 0: disabled 1: enabled

INTNREG05

INTNREG05 is a UTMI Vendor control and status register. It is used to read or write to the UTMI PHY.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18	17	16	15 14 13	12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				vbusy	vport		vcontrol_loadm	reserved	reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0	1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved

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[17]	RO	vbusy	The value 1 indicates that the hardware is writing data. This bit is cleared only when the process ends.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12]	RW	vcontrol_loadm	Load enable. 0: enabled 1: disabled
[11:8]	RO	reserved	Reserved
[7:0]	RO	reserved	Reserved

INTNREG06

INTNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_capture	reserved																			hbusrt_err				num_beat_err				num_beat_ok			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	err_capture	AHB error
[30:12]	RO	reserved	Reserved
[11:9]	RO	hbusrt_err	hbrust value during a control transfer when an AHB error occurs.
[8:4]	RO	num_beat_err	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00–0x10: valid 0x11–0x1F: reserved
[3:0]	RO	num_beat_ok	Number of completed beats during a burst transfer when an AHB error occurs.

INTNREG07

INTNREG07 is an AHB error address register.

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Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address during a control transfer when an AHB error occurs.

13.7.5.2 USB Device Register Description

GOTGCTL

GOTGCTL is a device behavior control and status query register.

Offset Address	Register Name	Total Reset Value
0x0000	GOTGCTL	0x04C1_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chirpen	multvalidbc					reserved	otgver	bsesvld	asesvld	dbnctime	conidsts	reserved				devhnpen	hstsethnpen	hnpreq	hstnegscs	bvalidovval	bvalidoven	avalidovval	avalidoven	vbvalidovval	vbvalidoven	sesreq	sesreqscs
Reset	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	chirpen	Chirp on enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_BC_SUPPORT is 1. If OTG_BC_SUPPORT is not 1, this bit is reserved.
[26:22]	RO	multvalidbc	BC ACA input Bit[26]: rid_float Bit[25]: rid_gnd Bit[24]: rid_a Bit[23]: rid_b Bit[22]: rid_c
[21]	RO	reserved	Reserved

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[20]	RW	otgver	Device version 0: Device version 1.3 1: Device version 2.0
[19]	RO	bsesvld	Transceiver status in device mode 0: B-session invalid 1: B-session valid
[18]	RO	asesvld	Transceiver status in host mode 0: A-session invalid 1: A-session valid
[17]	RO	dbnctime	Dejitter time 0: long dejitter time 1: short dejitter time
[16]	RO	conidsts	USB_ID status 0: 0: The device works in A-device mode. 1: The device works in B-device mode.
[15:12]	RO	reserved	Reserved
[11]	RW	devhnpen	Device HNP enable 0: disabled 1: enabled
[10]	RW	hstsethnpen	Host HNP enable 0: disabled 1: enabled
[9]	RW	hnpreq	HNP request 0: no 1: yes
[8]	RO	hstnegscs	Host negotiation indicator 0: Host negotiation fails. 1: Host negotiation is successful.
[7]	RW	bvalidovval	Bvalid setting 0: Bvalid = 0 1: Bvalid = 1 When GOTGCTL[bvalidoven] is 1, this bit is valid.
[6]	RW	bvalidoven	Bvalid signal overwrite enable 0: Bvalid can be overwritten. 1: Bvalid cannot be overwritten.

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[5]	RW	avalidovval	Avalid setting 0: Avalid = 0 1: Avalid = 1 When GOTGCTL[avalidoven] is 1, this bit is valid.
[4]	RW	avalidoven	Avalid signal overwrite enable 0: Avalid can be overwritten. 1: Avalid cannot be overwritten.
[3]	RW	vbvalidovval	vbusvalid setting 0: vbusvalid = 0 1: vbusvalid = 1 When GOTGCTL[vbvalidoven] is 1, this bit is valid.
[2]	RW	vbvalidoven	vbusvalid signal overwrite enable. 0: vbusvalid can be overwritten. 1: vbusvalid cannot be overwritten.
[1]	RW	sesreq	Session request 0: no 1: yes
[0]	RO	sesreqscs	Session request status 0: failure 1: success

GOTGINT

GOTGINT is a device interrupt generation indicator/clear register.

Offset Address	Register Name	Total Reset Value
0x0004	GOTGINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											multvalipchng	dbncedone	adevtoutchg	hstnegdet		reserved						hstnegsucstschng	sesreqsucstschng	reserved					sesenddet	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved

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[20]	RO	multvalipchng	An interrupt is generated when the value of at least one ACA pin changes. Setting this bit to 1 clears the interrupt. This bit is valid only when OTG_BC_SUPPORT is 1.
[19]	RO	dbncedone	An interrupt is generated when dejitter is successful. Setting this bit to 1 clears the interrupt. This bit is valid only when the HNP Capable or SRP Capable bit is set to 1.
[18]	RO	adevtoutchg	An interrupt is generated when waiting for the connection of device B times out. Setting this bit to 1 clears the interrupt.
[17]	RO	hstnegdet	An interrupt is generated when host negotiation is detected. Setting this bit to 1 clears the interrupt.
[16:10]	RO	reserved	Reserved
[9]	RO	hstnegsucstschng	An interrupt is generated when the host negotiation request fails or is successful. Setting this bit to 1 clears the interrupt.
[8]	RO	sesreqsucstschng	An interrupt is generated when the session request fails or is successful. Setting this bit to 1 clears the interrupt.
[7:3]	RO	reserved	Reserved
[2]	RO	sesenddet	An interrupt is generated when utmiotg_bvalid is deasserted. Setting this bit to 1 clears the interrupt.
[1:0]	RO	reserved	Reserved

GAHBCFG

GAHBCFG is an AHB configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	GAHBCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							invdescendianness	ahbsingle	notialldmawrit	remmemsupp		reserved												nptxfemplvl	reserved	dmaen	hbstlen				glblintrmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved

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[24]	RW	invdescendianness	Descriptor byte invert 0: The descriptor byte sequence is similar to the AHB master byte sequence. 1: When the AHB master byte sequence is big endian, the descriptor byte sequence is little endian. When the AHB master byte sequence is little endian, the descriptor byte sequence is big endian.
[23]	RW	ahbsingle	Transfer in DMA mode 0: The remaining data is transmitted based on the INCR burst size. 1: The remaining data is transmitted based on the single burst size.
[22]	RW	notialldmawrit	DMA write operation notification. This bit is valid only when GAHBCFG[remmemsupp] is 1.
[21]	RW	remmemsupp	Remote memory support 0: int_dma_req and int_dma_done are not set to **1**, and the controller core handles the XferComp interrupt immediately after the DMA write operation is complete. 1: int_dma_req is set to **1** when the HSOTG DMA starts writing data to an external memory; int_dma_done is set to **1** when the transfer of the controller core is complete, indicating that the HSOTG write operation is complete. In this case, the controller core waits until the system sys_dma_done signal becomes valid, and then starts the next DMA transfer.
[20:8]	RO	reserved	Reserved
[7]	RW	nptxfemplvl	Empty status level of the non-periodic TX FIFO. 0: The TxFEmp interrupt indicates that the TX FIFO at the IN endpoint is half empty. 1: The TxFEmp interrupt indicates that the TX FIFO at the IN endpoint is empty.
[6]	RO	reserved	Reserved
[5]	RW	dmaen	DMA mode enable 0: The core works in slave mode. 1: The core works in DMA mode.
[4:1]	RW	hbstlen	Burst length/type for both the external and internal DMA modes In external DMA mode: 0000: 1 word 0001: 4 words 0010: 8 words 0011: 16 words 0100: 32 words 0101: 64 words 0110: 128 words 0111: 256 words

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			Other values: reserved In internal DMA mode: 0000: Single 0001: INCR 0011: INCR4 0101: INCR8 0111: INCR16 Other values: reserved
[0]	RW	glblintrmsk	Global interrupt mask 0: masked 1: not masked

GUSBCFG

GUSBCFG is a USB configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	GUSBCFG	0x0000_1400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	corrupttxpkt	forcedevmode	forcehstmode	txenddelay	usbtrafctl	ic_usbcap	ulpi	indicator	complement	termseldlpulse	ulpiextvbusindicator	ulpiextvbusdrv	ulpiclksusm	ulpiautores	ulpifsls	otgi2csel	phylpwrclksel	reserved	usbtrdtim				hnpcap	srpcap	ddrsel	physel	fsintf	ulpi_utmi_sel	phyif	toutcal		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WO	corrupttxpkt	Unexpected TX packet. This bit is for debugging only and is always set to 0.
[30]	RW	forcedevmode	Forcible device mode. 0: normal mode 1: forcible device mode
[29]	RW	forcehstmode	Forcible host mode 0: normal mode 1: forcible host mode.
[28]	RW	txenddelay	TX end delay enable 0: disabled 1: enabled

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[27]	RW	usbtrafctl	USB pull-up/pull-down resistor control (traffic signaling) 0: Pull-up and pull-down resistors are attached. 1: Pull-up and pull-down resistors are detached. **NOTE** This bit is valid only when OTG_ENABLE_IC_USB and USBCFG [ic_usbcap] are 1.
[26]	RO	ic_usbcap	IC_USB enable 0: The IC_USB PHY interface is not selected. 1: The IC_USB PHY interface is selected.
[25]	RW	ulpi	ULPI interface protection enable 0: enabled 1: disabled
[24]	RW	indicator	Indicator pass through 0: The complementary output signal is determined by the vbusvalid comparator. 1: The complementary output signal is not determined by the vbusvalid comparator. When TG_HSPHY_INTERFACE is 1, this bit is read-only. When TG_HSPHY_INTERFACE is 0, this bit is reserved.
[23]	RW	complement	Indicator complement 0: The PHY does not invert the ExternalVbusIndicator signal. 1: The PHY inverts the ExternalVbusIndicator signal.
[22]	RW	termseldlpulse	SRP line pulse drive 0: utmi_txvalid drives the line pulse. 1: utmi_termsel drives the line pulse.
[21]	RW	ulpiextvbusindicator	ULPI external VBUS over-current indicator 0: The PHY uses the internal vbusvalid comparator. 1: The PHY uses the external vbusvalid comparator. This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[20]	RW	ulpiextvbusdrv	ULPI external VBUS drive 0: The PHY uses the internal charge pump to drive VBUS. 1: The PHY uses the external power supply to drive VBUS. **NOTE** This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[19]	RW	ulpiclksusm	ULPI clock suspend. 0: The PHY disables the internal clock in suspend mode. 1: The PHY does not disable the internal clock in suspend mode. This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.

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[18]	RW	ulpiautores	ULPI automatic restore 0: The PHY does not use the automatic restore feature. 1: The PHY uses the automatic restore feature. **NOTE** This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[17]	RW	ulpifsls	ULPI FS/LS select 0: ULPI interface 1: ULPI FS/LS serial interface **NOTE** Set GUSBCFG.ULPI_UTMI_SEL to 1 before setting this bit.
[16]	RW	otgi2csel	UTMI or I^2C interface select 0: UTMI USB 1.1 full-speed interface. 1: I^2C interface **NOTE** This bit is valid only when OTG_I2C_INTERFACE is 2. Reading this bit returns 0.
[15]	RW	phylpwrclksel	PHY low-power clock select. 0: internal 480 MHz PLL clock 1: external 48 MHz clock
[14]	-	reserved	Reserved
[13:10]	RW	usbtrdtim	USB turnaround time 0101: This field is set to this value when the MAC interface is a 16-bit UTMI+ interface. 1001: This field is set to this value when the MAC interface is an 8-bit UTMI+ interface. Other values: reserved
[9]	RW	hnpcap	HNP enable 0: disabled 1: enabled
[8]	RW	srpcap	SRP enable 0: disabled 1: enabled
[7]	RW	ddrsel	ULPI DDR select 0: single-rate ULPI interface 1: double-rate ULPI interface This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.

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[6]	RW	physel	USB 2.0 high-speed PHY or USB 1.1 full-speed serial transceiver 0: USB 2.0 high-speed UTMI+ or ULPI PHY interface 1: USB 1.1 full-speed serial transceiver If the USB 1.1 full-speed serial transceiver is not selected, this bit is always 0 and read-only. If the USB 2.0 high-speed PHY is not selected, this bit is always 1 and read-only. If the preceding interface types are not selected (non-zero value), this bit is used to select the interface to be activated, and this bit can be read or written.
[5]	RW	fsintf	Full-speed serial interface select. 0: 6-pin unidirectional full-speed serial interface 1: 3-pin bidirectional full-speed serial interface If the USB 1.1 full-speed serial transceiver is not selected, this bit is always 0 and write-only. If the USB 1.1 full-speed interface is selected, this bit can be used to select the 3-pin or 6-pin interface and can be read or written.
[4]	RW	ulpi_utmi_sel	ULPI or UTMI select 0: UTMI+ interface 1: ULPI interface
[3]	RW	phyif	PHY interface 0: 8 bits 1: 16 bits
[2:0]	RW	toutcal	HS/FS timeout calibration High-speed operations: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

GRSTCTL

GRSTCTL is a reset hardware feature register.

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Offset Address	Register Name	Total Reset Value
0x0010	GRSTCTL	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahbidle	dmareq	reserved																			txfnum					txfflsh	rxfflsh	intknqflsh	frmcntrrst	reserved	csftrst
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ahbidle	Whether the AHB master state machine is idle 0: no 1: yes
[30]	RO	dmareq	DMA request signal, indicating that the DMA request is being processed. This bit is only for debugging. 0: other cases 1: The DMA request is being processed.
[29:11]		reserved	Reserved
[10:6]	RW	txfnum	TX FIFO ID, which must be updated by using the TX FIFO flush bit. This field cannot be overwritten before the controller core clears the TX FIFO flush bit. 0x0: In host mode, non-periodic TX FIFOs are flushed. During shared FIFO operations, non-periodic TX FIFOs are flushed in device mode. In dedicated FIFO mode, TX FIFO 0 is flushed in device mode. 0x1: In host mode, periodic TX FIFOs are flushed. During shared FIFO operations, periodic TX FIFO 1 is flushed in device mode. In dedicated FIFO mode, TX FIFO 1 is flushed in device mode. 0x2: During shared FIFO operations, periodic TX FIFO 2 is flushed in device mode. In dedicated FIFO mode, TX FIFO 2 is flushed in device mode. 0xF: During shared FIFO operations, periodic TX FIFO 15 is flushed in device mode. In dedicated FIFO mode, TX FIFO 15 is flushed in device mode. 0x10: All TX FIFOs are flushed in device or host mode.

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[5]	R_WS_SC	txfflsh	TX FIFO flush This bit can be used to refresh one or all TX FIFOs but FIFOs cannot be refreshed during transactions. This bit can be written only after the application program confirms that the controller core does not read or write to the TX FIFO. It takes eight clock cycles to clear this bit, during which the application program must wait. 0: not flushed 1: flushed
[4]	RO	rxfflsh	RX FIFO flush This bit can be used to refresh all RX FIFOs but FIFOs cannot be refreshed during transactions. This bit can be written only after the application program confirms that the controller core does not read or write to the RX FIFO. It takes eight clock cycles to clear this bit, during which the application program must wait. 0: not flushed 1: flushed
[3]	R_WS_SC	intknqflsh	In token sequence learning queue flush This bit is valid only when OTG_EN_DED_TX_FIFO is 0. 0: not flushed 1: flushed
[2]	RO	frmcntrrst	Host frame counter reset This bit is used to reset the frame number counter. When the frame number counter is reset, the ID of next transmitted SOF micro-frames is 0. 0: not reset 1: reset
[1]	RO	reserved	Reserved
[0]	RW	csftrst	Core soft interrupt 1. All interrupts and the CSR register excluding the following bits are cleared: – PCGCCTL.RstPdwnModule – PCGCCTL.GateHclk – PCGCCTL.PwrClmp – PCGCCTL.StopPPhyLPwrClkSelclk – GUSBCFG.PhyLPwrClkSel – GUSBCFG.DDRSel – GUSBCFG.PHYSel – GUSBCFG.FSIntf – GUSBCFG.ULPI_UTMI_Sel – GUSBCFG.PHYIf – GUSBCFG.TxEndDelay – GUSBCFG.TermSelDLPulse

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			– GUSBCFG.ULPIClkSusM – GUSBCFG.ULPIAutoRes – GUSBCFG.ULPIFsLs – GGPIO – GPWRDN – GADPCTL – HCFG.FSLSPclkSel – DCFG.DevSpd – DCTL.SftDiscon 2. All module state machines are reset to the idle status, and all TX FIFOs and RX FIFOs are refreshed. 3. All transactions on the AHB master are interrupted as soon as possible, and all USB transactions are immediately interrupted. 4. When the hibernation or ADP feature is enabled, the PMU module is not soft-reset by the core.

GINTSTS

GINTSTS is a system interrupt register.

Offset Address	Register Name	Total Reset Value
0x0014	GINTSTS	0x0800_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupint	sessreqint	disconnint	conidstschng	lpm_int	ptxfemp	hchint	prtint	resetdet	fetsusp	incomplpincompisoout	incompisoin	oepint	iepint	epmis	rstrdoneint	eopf	isooutdrop	enumdone	usbrst	usbsusp	erlysusp	i2cint	ulpickinti2cckint	goutnakeff	ginnakeff	nptxfemp	rxflvl	sof	otgint	modemis	curmod
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	wkupint	Suspend/Resume detection interrupt. Setting this bit to 1 clears the interrupt.
[30]	RWSC	sessreqint	In host mode, an interrupt is generated when a device session request is detected. In device mode, an interrupt is generated when utmisrp_bvalid is 1. Setting this bit to 1 clears the interrupt.

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[29]	RWSC	disconnint	An interrupt is generated when the system detects that the device is disconnected. Setting this bit to 1 clears the interrupt.
[28]	RWSC	conidstschng	An interrupt is generated when the slot ID changes. Setting this bit to 1 clears the interrupt.
[27]	RWSC	lpm_int	In device mode, an interrupt is generated when the device receives an LPM transaction and transmits a response indicating no errors. In host mode, an interrupt is generated when the device receives an LPM transaction and transmits a response indicating no errors, or when the host core completes the preset LPM transactions. **NOTE** This bit is valid only when LPMCapable or OTG_ENABLE_LPM is 1. Setting this bit to 1 clears the interrupt.
[26]	RO	ptxfemp	An interrupt is generated when the periodic TX FIFO is empty or half empty.
[25]	RO	hchint	In host mode, an interrupt is generated in a core channel. This bit is cleared by clearing the corresponding status bit.
[24]	RO	prtint	In host mode, an interrupt is generated when the status of a port of the DWC_otg core changes. **NOTE** This bit is cleared by clearing the corresponding bit in the host port control and status register.
[23]	RWSC	resetdet	In device mode, an interrupt is generated when the device is suspended and the system detects that the USB module is reset in power-down module. In host mode, this interrupt is not generated. **NOTE** Setting this bit to 1 clears the interrupt.
[22]	RWSC	fetsusp	This interrupt is valid only in DMA mode. This interrupt indicates that the core stops obtaining data from IN endpoints.
[21]	RWSC	incomplpincompisoout	In host mode, an interrupt is generated if there are pending transactions. In device mode, an interrupt is generated when there are isochronous OUT transfers to be completed. **NOTE** Setting this bit to 1 clears the interrupt.
[20]	RWSC	incompisoin	An interrupt is generated when there are isochronous IN transfers to be completed. In scatter/gather DMA mode, this interrupt is not generated. **NOTE** Setting this bit to 1 clears the interrupt.

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[19]	RO	oepint	In device mode, an interrupt is generated on an OUT endpoint. This interrupt is cleared by clearing the corresponding status bit in the DOEPINT*n* register.
[18]	RO	iepint	In device mode, an interrupt is generated on an IN endpoint. This interrupt is cleared by clearing the corresponding status bit in the DOEPINT*n* register.
[17]	RO	epmis	An interrupt is generated when endpoints mismatch. This bit is valid only during shared FIFO operations. **NOTE** Setting this bit to 1 clears the interrupt.
[16]	RWSC	rstrdoneint	An interrupt is caused by the restore command after hibernation. **NOTE** This bit is valid only when the hibernation function is enabled.
[15]	RWSC	eopf	Periodic frame end interrupt. Setting this bit to 1 clears the interrupt.
[14]	RWSC	isooutdrop	Isochronous OUT packet drop interrupt. **NOTE** Setting this bit to 1 clears the interrupt.
[13]	RWSC	enumdone	Speed enumeration completion interrupt. **NOTE** Setting this bit to 1 clears the interrupt.
[12]	RWSC	usbrst	USB reset detection interrupt. **NOTE** Setting this bit to 1 clears the interrupt.
[11]	RWSC	usbsusp	USB suspend detection interrupt. **NOTE** Setting this bit to 1 clears the interrupt.
[10]	RWSC	erlysusp	USB idle 3 ms detection interrupt. **NOTE** Setting this bit to 1 clears the interrupt.
[9]	RWSC	i2cint	An interrupt is generated when I^2C access through the I^2C interface is complete. This bit is enabled only when OTG_I2C_INTERFACE is 1. **NOTE** Setting this bit to 1 clears the interrupt.
[8]	RWSC	ulpickinti2cckint	When the ULPI Carkit interrupt is generated, the core sets the interrupt bit to 1. This bit is valid only when OTG_ULPI_CARKIT is 1; otherwise, reading this bit returns 0. When the I^2C Carkit interrupt is generated, the core sets the

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			interrupt bit to 1. This bit is valid only when OTG_I2C_INTERFACE is 1; otherwise, reading this bit returns 0. **NOTE** Setting this bit to 1 clears the interrupt.
[7]	RO	goutnakeff	The global OUT NAK bit in the device control register is set. This interrupt is cleared by clearing the global OUT NAK bit.
[6]	RO	ginnakeff	An interrupt is generated when the global non-periodic IN NAK is set in the device control register.
[5]	RO	nptxfemp	An interrupt is generated when the non-periodic TX FIFO is empty or half empty.
[4]	RO	rxflvl	There is at least a pending packet to be read by the RX FIFO.
[3]	RWSC	sof	In host mode, an SOF, micro-SOF, or keep-active is being transmitted. In device mode, an SOF token is received by the USB module.
[2]	RO	otgint	An OTG even is in progress. This interrupt is cleared by clearing the corresponding bit in the GOTGINT register.
[1]	RWSC	modemis	Mode mismatch interrupt When the core works in device mode, a register in host mode needs to be accessed. When the core works in host mode, a register in device mode needs to be accessed. **NOTE** Setting this bit to 1 clears the interrupt. 0: invalid 1: valid
[0]	RO	curmod	Current operating mode 0: device mode 1: host mode

GINTMSK

GINTMSK is a system interrupt mask register.

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Offset Address	Register Name	Total Reset Value
0x0018	GINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupintmsk	sessreqintmsk	disconnintmsk	conidstschngmsk	lpm_intmsk	ptxfempmsk	hchintmsk	prtintmsk	resetdetmsk	fetsuspmsk	incomplpmskincompisooutmsk	incompisoinmsk	oepintmsk	iepintmsk	epmismsk	rstrdoneintmsk	eopfmsk	isooutdropmsk	enumdonemsk	usbrstmsk	usbsuspmsk	erlysuspmsk	i2cintmsk	ulpickintmsk	goutnakeffmsk	ginnakeffmsk	nptxfempmsk	rxflvlmsk	sofmsk	otgintmsk	modemismsk	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wkupintmsk	Resume/Remote wakeup detection interrupt mask. 0: masked 1: not masked
[30]	RW	sessreqintmsk	Session request/new session detection interrupt mask. 0: masked 1: not masked
[29]	RW	disconnintmsk	Disconnect detection interrupt mask. 0: masked 1: not masked
[28]	RW	conidstschngmsk	Connector ID status change interrupt mask. 0: masked 1: not masked
[27]	RW	lpm_intmsk	LPM transaction RX interrupt mask. 0: masked 1: not masked
[26]	RW	ptxfempmsk	Periodic TX FIFO empty interrupt mask. 0: masked 1: not masked
[25]	RW	hchintmsk	Host channel interrupt mask. 0: masked 1: not masked
[24]	RW	prtintmsk	Host port interrupt mask 0: masked 1: not masked

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[23]	RW	resetdetmsk	Reset detection interrupt mask. 0: masked 1: not masked
[22]	RW	fetsuspmsk	Data fetch suspended interrupt mask. 0: masked 1: not masked
[21]	RW	incomplpmskincompisooutmsk	Incomplete periodic transfer interrupt mask. 0: masked 1: not masked Incomplete isochronous OUT transfer interrupt mask. 0: masked 1: not masked
[20]	RW	incompisoinmsk	Incomplete isochronous in transfer interrupt mask. 0: masked 1: not masked This bit can be enabled only when periodic endpoints are enabled in dedicated TX FIFO mode.
[19]	RW	oepintmsk	OUT endpoint interrupt mask. 0: masked 1: not masked
[18]	RW	iepintmsk	IN endpoint interrupt mask. 0: masked 1: not masked
[17]	RW	epmismsk	Endpoint mismatch interrupt mask. 0: masked 1: not masked
[16]	RW	rstrdoneintmsk	Restore done interrupt mask. 0: masked 1: not masked This bit is valid only when the hibernation function is enabled (OTG_EN_PWROPT = 2).
[15]	RW	eopfmsk	End of periodic frame interrupt mask. 0: masked 1: not masked
[14]	RW	isooutdropmsk	Device only isochronous OUT packet drop interrupt mask. 0: masked 1: not masked

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[13]	RW	enumdonemsk	Enumeration done interrupt mask. 0: masked 1: not masked
[12]	RW	usbrstmsk	USB reset interrupt mask. 0: masked 1: not masked
[11]	RW	usbsuspmsk	USB suspend interrupt mask. 0: masked 1: not masked
[10]	RW	erlysuspmsk	Early suspend interrupt mask. 0: masked 1: not masked
[9]	RW	i2cintmsk	I^2C interrupt mask. 0: masked 1: not masked
[8]	RW	ulpickintmsk	ULPI Carkit interrupt mask. 0: masked 1: not masked I^2C Carkit interrupt mask. 0: masked 1: not masked
[7]	RW	goutnakeffmsk	Global OUT NAK effective interrupt mask. 0: masked 1: not masked
[6]	RW	ginnakeffmsk	Global non-periodic IN NAK effective interrupt mask. 0: masked 1: not masked
[5]	RW	nptxfempmsk	Non-periodic TX FIFO empty interrupt mask. 0: masked 1: not masked
[4]	RW	rxflvlmsk	RX FIFO non-empty interrupt mask. 0: masked 1: not masked
[3]	RW	sofmsk	Start of (micro) frame interrupt mask. 0: masked 1: not masked

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[2]	RW	otgintmsk	Device interrupt mask. 0: masked 1: not masked
[1]	RW	modemismsk	Mode mismatch interrupt mask. 0: masked 1: not masked
[0]	RW	reserved	Reserved.

GRXSTSR

GRXSTSR is an RX status debugging read register.

Offset Address	Register Name	Total Reset Value
0x001C	GRXSTSR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved_devicemode		fn_devicemode	pktsts_devicemode	dpid_devicemode	bcnt_devicemode		chnum_devicemode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved_devicemode	Reserved.
[24:21]	RO	fn_devicemode	Number of frames.
[20:17]	RO	pktsts_devicemode	Data packet status. 0001: global OUT NAK (interrupt triggered) 0010: IN data packet received 0011: IN transfer completion (interrupt triggered) 0101: data toggle error (interrupt triggered) 0111: channel stop (interrupt triggered) Other values: reserved
[16:15]	RO	dpid_devicemode	Data PID of the received packet. 00: DATA0 10: DATA1 01: DATA2 11: MDATA
[14:4]	RO	bcnt_devicemode	Byte size of the received IN data packets.

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[3:0]	RO	chnum_devicemode	Number of channels from which the current data packets are received.

GRXSTSP

GRXSTSP is an RX status read&pop register.

Offset Address	Register Name	Total Reset Value
0x0020	GRXSTSP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved_devicemode		fn_devicemode	pktsts_devicemode	dpid_devicemode	bcnt_devicemode		chnum_devicemode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved_devicemode	Reserved.
[24:21]	RO	fn_devicemode	Number of frames.
[20:17]	RO	pktsts_devicemode	Data packet status. 0001: global OUT NAK (interrupt triggered) 0010: IN data packet received 0011: IN transfer completion (interrupt triggered) 0101: data toggle error (interrupt triggered) 0111: channel stop (interrupt triggered) Other values: reserved
[16:15]	RO	dpid_devicemode	Data PID of the received packet. 00: DATA0 10: DATA1 01: DATA2 11: MDATA
[14:4]	RO	bcnt_devicemode	Byte size of the received IN data packets.
[3:0]	RO	chnum_devicemode	Number of channels from which the current data packets are received.

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GRXFSIZ

GRXFSIZ is an RX FIFO size configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	GRXFSIZ	0x0000_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rxfdep															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rxfdep	RX FIFO depth. Its value range is 16−32768.

GNPTXFSIZ

GNPTXFSIZ is a non-periodic TX FIFO size configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	GNPTXFSIZ	0x0100_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ineptxf0dep																ineptxf0staddr															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	ineptxf0dep	Depth of IN endpoint TX FIFO 0. Its value range is 16−32768.
[15:0]	RW	ineptxf0staddr	Start address for the TX RAM of IN endpoint FIFO 0.

GNPTXSTS

GNPTXSTS is a non-periodic TX FIFO and non-periodic TX request query register.

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Offset Address	Register Name	Total Reset Value
0x002C	GNPTXSTS	0x0008_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	nptxqtop							nptxqspcavail								nptxfspcavail															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:24]	RO	nptxqtop	Non-periodic TX request queue top. Bit[30:27]: number of channels or endpoints bit[26:25]: 00: IN/OUT token 01: zero-length transmit packet (device IN/host OUT) 10: PING/CSPLIT token 11: channel stop command Bit[24]: stop (the selected channel or endpoint is used for attempting)
[23:16]	RO	nptxqspcavail	Available space for the non-periodic TX request queue. 0x0: The non-periodic TX request queue is full. 0x1: One address is available. 0x2: Two addresses are available. 0xn: n addresses ($0 \le n \le 8$) are available. Other values: reserved
[15:0]	RO	nptxfspcavail	Total available space for the non-periodic TX request queue. 0x0: The non-periodic TX FIFO is full. 0x1: One word is available. 0x2: Two words are available. 0xn: n words ($0 \le n \le 32768$) are available. 0x8000: 32768 words are available. Other values: reserved

GI2CCTL

GI2CCTL is an I^2C access register.

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Offset Address	Register Name	Total Reset Value
0x0030	GI2CCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bsydne	rw	reserved	i2cdatse0	i2cdevadr		i2csuspctl	ack	i2cen	addr							regaddr								rwdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	bsydne	I^2C busy/done. 0: done 1: busy
[30]	RW	rw	Read/Write indicator. 0: write 1: read
[29]	RW	reserved	Reserved.
[28]	RW	i2cdatse0	USB mode of the FS interface. 0: VP_VM USB mode 1: DAT_SE0 USB mode
[27:26]	RW	i2cdevadr	I^2C device address. 00: 7'h2C 01: 7'h2D 10: 7'h2E 11: 7'h2F
[25]	RW	i2csuspctl	I^2C suspend control. 0: utmi_suspend_n is used. 1: The suspend bit in the PHY register is edited by using the I^2C write function.
[24]	RO	ack	I^2C ACK. 0: NAK 1: ACK
[23]	RW	i2cen	I^2C transaction enable. 0: disabled 1: enabled
[22:16]	RW	addr	I^2C slave address.
[15:8]	RW	regaddr	I^2C register address.
[7:0]	RW	rwdata	I^2C read//write data.

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GPVNDCTL

GPVNDCTL is a PHY vendor control register.

Offset Address	Register Name	Total Reset Value
0x0034	GPVNDCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disulpidrvr	reserved			vstsdone	vstsbsy	newregreq	reserved		regwr	regaddr						vctrlextregaddr								regdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	disulpidrvr	ULPI interface enable. 0: enabled 1: disabled **NOTE** This bit is valid only when OTG_ULPI_CARKIT is 1. Otherwise, reading this bit returns 0.
[30:28]	RO	reserved	Reserved.
[27]	RWSC	vstsdone	Vendor control access (done). 0: The new register request is set. 1: Vendor control access ends.
[26]	RO	vstsbsy	Vendor control access (busy). 0: Vendor control access ends. 1: Vendor control access is in progress.
[25]	RWSC	newregreq	New vendor control access. 0: no access request 1: new vendor control access request
[24:23]	RO	reserved	Reserved.
[22]	RW	regwr	Register read/write. 0: read 1: write
[21:16]	RW	regaddr	Register access address.
[15:8]	RW	vctrlextregaddr	Address for the UTMI+ vendor control register. bit[15:12]: 4-bit parallel output bus addressing bit[11:8]: utmi_vcontrol[3:0]
[7:0]	RW	regdata	Register data. This bit is valid after the Vstatus Done bit is set.

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GGPIO

GGPIO is a GPIO register.

Offset Address	Register Name	Total Reset Value
0x0038	GGPIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gpo																gpi															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	gpo	General-purpose output, which is driven by gp_o[15:0] of the core.
[15:0]	RW	gpi	General-purpose input, which reflects gp_i[15:0] of the core.

GUID

GUID is a user ID register.

Offset Address	Register Name	Total Reset Value
0x003C	GUID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userid																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	userid	User ID.

GSNPSID

GSNPSID is a Synopsys ID query register.

Offset Address	Register Name	Total Reset Value
0x0040	GSNPSID	0x4F54_300A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	synopsysid																															
Reset	0	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:0]	RW	synopsysid	ID of the current DWC_otg core.

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GHWCFG1

GHWCFG1 is user hardware configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0044	GHWCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epdir																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	epdir	Endpoint direction. The endpoint direction is expressed by two bits. Endpoint bit[31:30]: direction of endpoint 15 bit[29:28]: direction of endpoint 14 ... bit[3:2]: direction of endpoint 1 bit[1:0]: direction of endpoint 0 (always bidirectional) Direction. 00: bidirectional (IN and OUT) endpoint 01: IN endpoint 10: OUT endpoint 11: reserved

GHWCFG2

GHWCFG2 is user hardware configuration register 2.

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Offset Address	Register Name	Total Reset Value
0x0048	GHWCFG2	0x2284_C850

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	otg_enable_ic_usb	tknqdepth					ptxqdepth		nptxqdepth		reserved	multiprocintrpt	dynfifosizing	periosupport	numhstchnl		numdeveps				fsphytype				hsphytype		singpnt	otgarch	otgmode			
Reset	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RO	otg_enable_ic_usb	IC_USB select enable. 0: disabled 1: enabled
[30:26]	RO	tknqdepth	Depth of the IN token sequence learning queue in device mode. The value range is 0−30.
[25:24]	RO	ptxqdepth	Depth of the periodic request queue in host mode. 00: 2 01: 4 10: 8 11: 16
[23:22]	RO	nptxqdepth	Depth of the non-periodic request queue. 00: 2 01: 4 10: 8 Other values: reserved
[21]		reserved	Reserved.
[20]	RW	multiprocintrpt	Multi-processor interrupt enable. 0: disabled 1: enabled
[19]	RO	dynfifosizing	FIFO size dynamic change enable. 0: disabled 1: enabled
[18]	RO	periosupport	Periodic OUT channel support in host mode. 0: not supported 1: supported

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[17:14]	RO	numhstchnl	Number of host channels. 0–15: The value 0 indicates one channel, and the value 15 indicates 16 channels.
[13:10]	RO	numdeveps	Number of device endpoints (excluding endpoint 0). The value range is 1−15.
[9:8]	RO	fsphytype	Type of the full-speed PHY interface. 00: The full-speed interface is not supported. 01: The full-speed interface is supported. 10: FS pins share with UTMI+ pins. 11: FS pins share with ULPI pins.
[7:6]	RO	hsphytype	Type of the high-speed PHY interface. 00: high-speed interface not supported 01: UTMI+ 10: ULPI 11: UTMI+ and ULPI
[5]	RO	singpnt	Point-to-point. 0: multi-point application (hub and split supported) 1: single-point application (hub and split not supported)
[4:3]	RO	otgarch	Device architecture. 00: slave only 01: external DMA 10: internal DMA Other values: reserved
[2:0]	RO	otgmode	Operating mode. 000: HNP- and SRP-capable OTG (host & device) 001: SRP-capable OTG (host & device) 010: non-HNP and non-SRP capable OTG (host & device) 011: SRP-capable device 100: non-OTG device 101: SRP-Capable host 110: non-OTG host Other values: reserved

GHWCFG3

GHWCFG3 is user hardware configuration register 3.

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Offset Address	Register Name	Total Reset Value
0x004C	GHWCFG3	0x0501_54E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfifodepth																lpmmode	bcsupport	hsicmode	adpsupport	rsttype	optfeature	vndctlsupt	i2cintsel	otgen	pktsizewidth			xfersizewidth			
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dfifodepth	DFIFO depth. The value range is 32−32768.
[15]	RO	lpmmode	LPM working mode (configurable).
[14]	RO	bcsupport	Whether the HS device controller supports the battery charger. 0: not supported 1: supported
[13]	RO	hsicmode	HSIC mode select. 0: The HSIC-capable shares with the UTMI PHY interface 1: The HSIC mode is not selected.
[12]	RO	adpsupport	Whether the device controller has an ADP logic. 0: no 1: yes
[11]	RO	rsttype	Reset mode of clock always blocks. 0: asynchronous reset 1: synchronous reset
[10]	RO	optfeature	Feature removal. Features include the user ID register, GPIO interface ports, and SOF toggle and counter ports. 0: not removed 1: removed
[9]	RO	vndctlsupt	Vendor control interface support. 0: not supported 1: supported
[8]	RO	i2cintsel	I^2C interface select. 0: not selected 1: selected
[7]	RO	otgen	Device function enable. 0: disabled 1: enabled

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[6:4]	RO	pktsizewidth	Data packet width. 000: 4 bits 001: 5 bits 010: 6 bits 011: 7 bits 100: 8 bits 101: 9 bits 110: 10 bits Other values: reserved
[3:0]	RO	xfersizewidth	Transfer width. 0000: 11 bits 0001: 12 bits 1000: 19 bits Other values: reserved

GHWCFG4

GHWCFG4 is user hardware configuration register 4.

Offset Address	Register Name	Total Reset Value
0x0050	GHWCFG4	0x4600_8020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	descdma	descdmaen	ineps				dedfifomode	sessendfltr	bvalidfltr	avalidfltr	vbusvalidfltr	iddgfltr	numctleps				phydatawidth		reserved						extndedhibernation	hibernation	ahbfreq	partialpwrdn	numdevperioeps			
Reset	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	descdma	Scatter/Gather DMA. 0: no dynamic configuration 1: dynamic configuration
[30]	RO	descdmaen	PAD slew rate. 0: fast 1: slow

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[29:26]	RO	ineps	Number of IN endpoints in device mode. 0: one IN endpoint 1: two IN endpoints ... 15: 16 IN endpoints
[25]	RO	dedfifomode	Dedicated TX FIFO enable for device IN endpoints. 0: disabled 1: enabled
[24]	RO	sessendfltr	session_end filter enable. 0: disabled 1: enabled
[23]	RO	bvalidfltr	b_valid filter enable. 0: disabled 1: enabled
[22]	RO	avalidfltr	a_valid filter enable. 0: disabled 1: enabled
[21]	RO	vbusvalidfltr	VBUS valid filter enable. 0: disabled 1: enabled
[20]	RO	iddgfltr	IDDIG filter enable. 0: disabled 1: enabled
[19:16]	RO	numctleps	Number of controlled endpoints excluding endpoint 0 in device mode The value range is 0−15.
[15:14]	RO	phydatawidth	Data width of the UTMI+ PHY/ULPI-to-internal UTMI+ wrapper. 00: 8 bits 01: 16 bits 10: 8 bit or 16 bits, which is configured by using software Other values: reserved
[13:8]	RO	reserved	Reserved.
[7]	RO	extndedhibernation	Extended hibernation enable. 0: disabled 1: enabled
[6]	RO	hibernation	Hibernation enable. 0: disabled 1: enabled

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[5]	RO	ahbfreq	Whether the minimum AHB frequency is lower than 60 MHz. 0: no 1: yes
[4]	RO	partialpwrdn	Partial power down enable. 0: disabled 1: enabled
[3:0]	RO	numdevperioeps	Number of periodic IN endpoints in device mode. The value range is 0−15.

GLPMCFG

GLPMCFG is an LPM configuration register.

Offset Address	Register Name	Total Reset Value
0x0054	GLPMCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	invselhsic	hsiccon	rstrslpsts	enbesl	lpm_retrycnt_sts			sndlpm	lpm_retry_cnt				lpm_chnl_indx			l1resumeok	slpsts	corel1res			hird_thres				enblslpm	bremotewake	hird				appl1res	lpmcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	invselhsic	HSIC select (by using HSIC-invert) enable. If if_sel_hsic is 1: InvSelHsic = 1: disabled InvSelHsic = 0: enabled If if_sel_hsic is 0: InvSelHsic = 1: enabled InvSelHsic = 0: disabled
[30]	RW	hsiccon	HSIC-connect. Host mode: When this bit is set to 1, the bus HSIC is driven to idle status and waits for the HSIC connect sequence transmitted from the device. Device mode: When this bit is set to 1, the device waits for the HSIC idle line state on the bus. The HSIC connection starts after the idle line state occurs. **NOTE** This bit is valid only when OTG_ENABLE_HSIC is 1; otherwise, reading this bit returns 0.

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[29]	RW	rstrslpsts	Restore SlpSts. 0: The core enters the shallow sleep mode. 1: The core enters the deep sleep mode.
[28]	RW	enbesl	Best effort service latency (BESL) enable. 0: disabled 1: enabled
[27:25]	RO	lpm_retrycnt_sts	LPM retry count. This field is used to count the remaining retries.
[24]	RWSC	sndlpm	LPM transaction TX.
[23:21]	RW	lpm_retry_cnt	LPM retry count statistics. When a device provides error information, this field shows the extra LPM retries of the host before the device validity signal arrives.
[20:17]	RW	lpm_chnl_indx	LPM channel index. The number of LPM transaction channels is provided. The core automatically calculates the device address and number of endpoints based on the LPM channel index.
[16]	RO	l1resumeok	Resume from the sleep state. 0: resumed 1: not resumed
[15]	RO	slpsts	Port sleep state. 0: resume 1: sleep
[14:13]	RO	corel1res	LPM response. In device mode, this field reflects the response to the LPM transaction. In host mode, this field indicates the handshake response from the device during LPM transaction. 11: ACK 10: NYET 01: STALL 00: error (no handshake response)
[12:8]	RW	hird_thres	BESL or HIRD threshold.
[7]	RW	enblslpm	utmi_sleep_n enable. 0: disabled 1: enabled

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[6]	RW	bremotewake	Remote wake enable. In host mode, the enable signal is transmitted from the wIndex field of the LPM transaction. In device mode (read-only), when the ACK, NYET, or STALL response is transmitted to the LPM transaction, this bit is updated together with the received LPM token, bRemoteWake, and bmAttribute.
[5:2]	RW	hird	When EnBESL is 0: Host-initiated resume period. In host mode, this field is assigned by the LPM transaction. In device mode, this field is updated by LPM token HIRD bmAttribute. Sl. No HIRD[3:0] THIRD (μs) 1 4'b0000 50 2 4'b0001 125 3 4'b0010 200 4 4'b0011 275 5 4'b0100 350 6 4'b0101 425 7 4'b0110 500 8 4'b0111 575 9 4'b1000 650 10 4'b1001 725 11 4'b1010 800 12 4'b1011 875 13 4'b1100 950 14 4'b1101 1025 15 4'b1110 1100 16 4'b1111 1175 When EnBESL is 1: BESL In host mode, the BESL value is transmitted to the LPM transaction In device mode, this field is updated by LPM token BESL bmAttribute.
[1]	RW	appl1res	LPM response. 0: NYET 1: ACK
[0]	RW	lpmcap	LPM enable. 0: disabled 1: enabled

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GPWRDN

GPWRDN is a power down register.

Offset Address	Register Name	Total Reset Value
0x0058	GPWRDN	0x1320_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			multvalidbc					adpint	bsessvld	iddig	linestate		stschngintmsk	stschngint	srpdetectmsk	srpdetect	conndetmsk	connectdet	disconnectdetectmsk	disconnectdetect	resetdetmsk	resetdetected	linestagechangemsk	Instschng	disablevbus	pwrdnswtch	pwrdnrst_n	pwrdnclmp	restore	pmuactv	pmuintsel
Reset	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RO	multvalidbc	BC ACA input. Bit 28 - rid_float Bit 27 - rid_gnd Bit 26 - rid_a Bit 25 - rid_b Bit 24 - rid_c
[23]	RWSC	adpint	An interrupt is generated when the ADP is in progress. Setting this bit to 1 clears this interrupt.
[22]	RO	bsessvld	B session validity. 0: B-Valid = 0 1: B-valid = 1
[21]	RO	iddig	IDDIG signal status indicator. Current operating mode. 0: host mode 1: device mode
[20:19]	RO	linestate	Current line state indicator. 00: DM = 0, DP = 0 01: DM = 0, DP = 1 10: DM = 1, DP = 0 11: undefined
[18]	RW	stschngintmsk	StsChng interrupt mask. 0: masked 1: not masked

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[17]	RWSC	stschngint	StsChng interrupt. The bit indicates whether the status of the IDDIG or BSessVld signal changes. 0: not changed 1: changed
[16]	RW	srpdetectmsk	SRPDetect interrupt mask, valid only in host mode 0: not masked 1: masked
[15]	RWSC	srpdetect	SRP detection. 0: not detected 1: detected
[14]	RW	conndetmsk	Connection detection interrupt mask. 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[13]	RO	connectdet	Connection detection. 0: disconnected 1: connected This bit is valid only when OTG_EN_PWROPT is 2.
[12]	RW	disconnectdetectmsk	Disconnection detection interrupt mask. 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[11]	RWSC	disconnectdetect	Disconnection detection. 0: not disconnected 1: disconnected This bit is valid only when OTG_EN_PWROPT is 2.
[10]	RW	resetdetmsk	Reset detection interrupt mask. 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[9]	RWSC	resetdetected	Reset detection. 0: not reset 1: reset This bit is valid only when OTG_EN_PWROPT is 2.
[8]	RW	linestagechangemsk	Line state change interrupt mask. 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.

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[7]	RWSC	lnstschng	Line state change detection. 0: not changed 1: changed This bit is valid only when GPWRDN.PMUActv is 1 and OTG_EN_PWROPT is 2.
[6]	RW	disablevbus	Vbus disable. In host mode: 0: PrtPwr is not 0. 1: PrtPwr is 0. In device mode: 0: The level of the bvalid signal is high. 1: The level of the bvalid signal is low. This bit is valid only when GPWRDN.PMUActv is 1.
[5]	RW	pwrdnswtch	Power down switch. 0: on 1: off
[4]	RW	pwrdnrst_n	Power down reset. 0: reset 1: not reset
[3]	RW	pwrdnclmp	Power down beat enable. 0: disabled 1: enabled
[2]	RW	restore	Restore. 0: DWC_otg is in normal mode. 1: DWC_otg is in restore mode. This bit is valid only when OTG_EN_PWROPT is 2.
[1]	RW	pmuactv	PMU enable. 0: disabled 1: enabled
[0]	RW	pmuintsel	PMU interrupt select. 0: internal DWC_otg_core interrupt 1: external DWC_otg_core interrupt

GDFIFOCFG

GDFIFOCFG is a DFIFO software configuration register.

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Offset Address	Register Name	Total Reset Value
0x005C	GDFIFOCFG	0x0501_0511

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epinfobaseaddr																gdfifocfg															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	epinfobaseaddr	Start address for the EP info controller.
[15:0]	RW	gdfifocfg	DFIFO size, which is dynamically configured.

GADPCTL

GADPCTL is an ADP timer control and status register.

Offset Address	Register Name	Total Reset Value
0x0060	GADPCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ar		adptoutmsk	adpsnsintmsk	adpprbintmsk	adptoutint	adpsnsint	adpprbint	adpen	adpres	enasns	enaprb	rtim										prbper		prbdelta		prbdschg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:27]	RW	ar	Access request. 00: read/write 01: read-only 10: write-only 11: reserved
[26]	RW	adptoutmsk	ADP timeout interrupt mask. 0: masked 1: not masked **NOTE** This bit is valid only when OTG_Ver is 1.

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[25]	RW	adpsnsintmsk	ADP sense interrupt mask. 0: masked 1: not masked NOTE This bit is valid only when OTG_Ver is 1.
[24]	RWC	adpprbintmsk	ADB probe interrupt mask. 0: masked 1: not masked NOTE This bit is valid only when OTG_Ver 1.
[23]	RWC	adptoutint	ADP timeout interrupt. Setting this bit to 1 clears this interrupt. NOTE This bit is valid only when OTG_Ver 1.
[22]	RWC	adpsnsint	ADP sense interrupt. Setting this bit to 1 clears this interrupt. NOTE This bit is valid only when OTG_Ver 1.
[21]	RWC	adpprbint	ADP probe interrupt. Setting this bit to 1 clears this interrupt. NOTE This bit is valid only when OTG_Ver 1.
[20]	RW	adpen	ADP enable. 0: disabled 1: enabled NOTE This bit is valid only when OTG_Ver 1.
[19]	RWC	adpres	ADP reset. 0: not reset +1: reset NOTE This bit is valid only when OTG_Ver 1.
[18]	RW	enasns	Sense enable. 0: disabled 1: enabled NOTE This bit is valid only when OTG_Ver 1.

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[17]	RW	enaprb	Probe enable. 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_Ver 1.
[16:6]	RO	rtim	Ramp time. The following is the mapping between the values and 32 kHz clock cycle: 0x000: 1 cycles 0x001: 2 cycles 0x002: 3 cycles ... 0x7FF: 2048 cycles
[5:4]	RW	prbper	Probe period. 00: 0.625s to 0.925s (0.775s typically) 01: 1.25s to 1.85s (1.55s typically) 10: 1.9s to 2.6s (2.275s typically) 11: reserved
[3:2]	RW	prbdelta	Probe delta. The following is the mapping between the values and 32 kHz clock cycle: 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
[1:0]	RW	prbdschg	Probe discharge. TADP_DSCHG time 00: 4 ms 01: 8 ms 10: 16 ms 11: 32 ms

HPTXFSIZ

HPTXFSIZ is a TX FIFO configuration register.

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Offset Address	Register Name	Total Reset Value
0x0100	HPTXFSIZ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ptxfsize																ptxfstaddr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ptxfsize	Depth of the host periodic TX FIFO. Its value range is 16−32768.
[15:0]	RW	ptxfstaddr	Start address for the host periodic TX FIFO.

DPTXFSIZN

DPTXFSIZN is a device periodic TX FIFO-*n* size register.

NOTE

This register is valid only in shared FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104 + 0x0004 x FIFO_num (FIFO_num = 0−14)	DPTXFSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dptxfsize																dptxfstaddr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dptxfsize	Size of the device periodic TX FIFO. The value range is 4−768.
[15:0]	RW	dptxfstaddr	Start address for the device periodic TX FIFO RAM.

DIEPTXFN

DIEPTXFN is a device IN endpoint TX FIFO size register.

NOTE

This register is valid only in dedicated FIFO mode.

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Offset Address	Register Name	Total Reset Value
0x0104 + 0x0004 x FIFO_num (FIFO_num = 0−14)	DIEPTXFN	0x0300_0251

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inepntxfdep																inepntxfstaddr															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	inepntxfdep	Depth of the IN endpoint TX FIFO. The value range is 16−32768.
[15:0]	RW	inepntxfstaddr	Start address for the IN endpoint FIFO*n* TX RAM.

DCFG

DCFG is a device configuration register.

Offset Address	Register Name	Total Reset Value
0x0800	DCFG	0x8100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	resvalid						perschintvl		descdma	epmiscnt					reserved				endevoutnak		perfint	devaddr							ena32khzsusp	nzstsouthshk	devspd	
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	resvalid	Resume time control. This bit is valid only when DCFG[ena32khzsusp] is 1.
[25:24]	RW	perschintvl	Ratio of the (micro) frames in scatter/gather DMA mode. 00: 25% of (micro) frames 01: 50% of (micro) frames 10: 75% of (micro) frames 11: reserved
[23]	RW	descdma	Scatter/Gather DMA enable in device mode. 0: disabled 1: enabled
[22:18]	RW	epmiscnt	IN endpoint mismatch statistics.
[17:14]	RW	reserved	Reserved.

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[13]	RW	endevoutnak	Device OUT NAK enable. 0: disabled 1: enabled
[12:11]	RW	perfrint	Periodic frame interval. 00: 80% of the (micro) frame interval 01: 85% 10: 90% 11: 95%
[10:4]	RW	devaddr	Device address.
[3]	RW	ena32khzsusp	32 kHz suspend mode enable. 0: disabled 1: enabled
[2]	RW	nzstsouthshk	Non-zero-length status OUT handshake select.
[1:0]	RW	devspd	Device speed. 00: high speed (30 MHz or 60 MHz USB 2.0 PHY clock) 01: full speed (30 MHz or 60 MHz USB 2.0 PHY clock) 10: low speed (6 MHz USB 1.1 transceiver clock) 11: full speed (48 MHz USB 1.1 transceiver clock)

DCTL

DCTL is a device control register.

Offset Address	Register Name	Total Reset Value
0x0804	DCTL	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														encontonbna	nakonbble	ignrfrmnum	reserved			pwronprgdone	cgoutnak	sgoutnak	cgnpinnak	sgnpinnak	tstctl			goutnaksts	gnpinnaksts	sftdiscon	rmtwkupsig
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17]	RW	encontonbna	Continue on BNA enable. 0: disabled 1: enabled

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[16]	RW	nakonbble	NAK on babble error. 0: no operation 1: NAK configured on the received babble
[15]	RW	ignrfrmnum	Whether the number of frames on isochronous endpoints is ignored. 0: not ignored 1: ignored
[14:12]	RW	reserved	Reserved.
[11]	RW	pwronprgdone	Resume from the power-down mode. 0: not woken up 1: woken up
[10]	WO	cgoutnak	Global OUT NAK clear. 0: no operation 1: cleared
[9]	WO	sgoutnak	Global OUT NAK. 0: no operation 1: configured
[8]	WO	cgnpinnak	Global non-periodic IN NAK clear. 0: no operation 1: cleared
[7]	WO	sgnpinnak	Global non-periodic IN NAK. 0: no operation 1: configured
[6:4]	RW	tstctl	Test control. 000: test mode disabled 001: Test_J mode 010: Test_K mode 011: Test_SE0_NAK mode 100: Test_Packet mode 101: Test_Force_Enable Other values: reserved
[3]	RO	goutnaksts	Global OUT NAK status. 0: handshake TX 1: NAK handshake TX
[2]	RO	gnpinnaksts	Global non-periodic IN NAK status. 0: handshake TX 1: NAK handshake TX

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[1]	RW	sftdiscon	Soft disconnection. 0: common mode 1: The core drives phy_opmode_o to 2'b01, and then triggers USB disconnection.
[0]	RW	rmtwkupsig	Remote wakeup signal TX. 0: not woken up remotely 1: woken up remotely

DSTS

DSTS is a device status query register.

Offset Address	Register Name	Total Reset Value
0x0808	DSTS	0x0007_FF02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								devlnsts				soffn												reserved				errticerr	enumspd		suspsts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:22]	RO	devlnsts	Logic level of the current USB data line. bit[23]: logic level of D+ bit[22]: logic level of D−
[21:8]	RO	soffn	Number of frames or micro frames in the received SOF packets.
[7:4]	RO	reserved	Reserved.
[3]	RO	errticerr	Irregular error indicator The controller core sets this bit to **1** when any irregular error (for example, phy_rxvalid_i is set to **1** and retains this value for 2 ms due to an PHY error) occurs in the UTMI+ interface. 0: No irregular error occurs in the UTMI+ interface. 1: An irregular error occurs in the UTMI+ interface.
[2:1]	RO	enumspd	Enumeration speed. 00: high speed (30 MHz or 60 MHz PHY clock) 01: full speed (30 MHz or 60 MHz PHY clock) 10: low speed (6 MHz PHY clock). 11: full speed (48 MHz PHY clock).
[0]	RO	suspsts	Suspend status. When the suspend conditions are detected, this bit is 1.

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DIEPMSK

DIEPMSK is a common interrupt mask register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0810	DIEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nakmsk	reserved			bnainintrmsk	txfifoundrnmsk	reserved	inepnakeffmsk	intknepmismsk	intkntxfempmsk	timeoutmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13]	RW	nakmsk	NAK interrupt mask. 0: masked 1: not masked
[12:10]	RO	reserved	Reserved.
[9]	RW	bnainintrmsk	BNA interrupt mask. 0: masked 1: not masked
[8]	RW	txfifoundrnmsk	FIFO underrun interrupt mask. 0: masked 1: not masked
[7]	RO	reserved	Reserved.
[6]	RW	inepnakeffmsk	IN endpoint NAK effective interrupt mask. 0: masked 1: not masked
[5]	RW	intknepmismsk	IN token received with EP mismatch interrupt mask. 0: masked 1: not masked
[4]	RW	intkntxfempmsk	IN token received when TX FIFO empty interrupt mask. 0: masked 1: not masked

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[3]	RW	timeoutmsk	Timeout interrupt mask. 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask. 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask. 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask. 0: masked 1: not masked

DOEPMSK

DOEPMSK is a common interrupt mask register for device OUT endpoints.

Offset Address	Register Name	Total Reset Value
0x0814	DOEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	nyetmsk	nakmsk	bbleerrmsk	reserved		bnaoutintrmsk	outpkterrmsk	reserved	back2backsetupmsk	stsphsercvdmsk	outtknepdismsk	setupmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RW	nyetmsk	NYET interrupt mask. 0: masked 1: not masked
[13]	RW	nakmsk	NAK interrupt mask. 0: masked 1: not masked
[12]	RW	bbleerrmsk	Babble error interrupt mask. 0: masked 1: not masked

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[11:10]	RO	reserved	Reserved.
[9]	RW	bnaoutintrmsk	BNA interrupt mask. 0: masked 1: not masked
[8]	RW	outpkterrmsk	OUT packet error interrupt mask. 0: masked 1: not masked
[7]	RO	reserved	Reserved.
[6]	RW	back2backsetupmsk	Back-to-back setup packets received interrupt mask. 0: masked 1: not masked
[5]	RW	stsphsercvdmsk	Status phase received interrupt mask. 0: masked 1: not masked
[4]	RW	outtknepdismsk	W OUT token received when endpoint disabled interrupt mask. 0: masked 1: not masked
[3]	RW	setupmsk	Setup phase done interrupt mask. 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask. 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask. 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask. 0: masked 1: not masked

DAINT

DAINT is an interrupt register for all device endpoints.

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Offset Address	Register Name	Total Reset Value
0x0818	DAINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepint																inepint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	outepint	OUT endpoint interrupt. Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RO	inepint	IN endpoint interrupt. Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DAINTMSK

DAINTMSK is an interrupt mask register for all endpoints.

Offset Address	Register Name	Total Reset Value
0x081C	DAINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepmsk																inepmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	outepmsk	OUT endpoint interrupt mask. Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RW	inepmsk	IN endpoint interrupt mask. Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DTKNQR1

DTKNQR1 is device IN token sequence learning queue read register 1.

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Offset Address	Register Name	Total Reset Value
0x0820	DTKNQR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																								wrapbit	reserved			intknwptr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 5 Bit[27:24]: endpoint ID of token 4 … Bit[15:12]: endpoint ID of token 1 Bit[11:8]: endpoint ID of token 0
[7]	RO	wrapbit	Wrapping bit 0: The learning queue of the IN token is cleared. 1: The write pointer is wrapped.
[6:5]	RO	reserved	Reserved.
[4:0]	RO	intknwptr	IN token queue write pointer.

DTKNQR2

DTKNQR2 is device IN token sequence learning queue read register 2.

Offset Address	Register Name	Total Reset Value
0x0824	DTKNQR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 13 Bit[27:24]: endpoint ID of token 12 … Bit[7:4]: endpoint ID of token 7

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			Bit[3:0]: endpoint ID of token 6

DTKNQR3

DTKNQR3 is device in token sequence learning queue read register 3.

Offset Address	Register Name	Total Reset Value
0x0830	DTKNQR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 21 Bit[27:24]: endpoint ID of token 20 … Bit[7:4]: endpoint ID of token 15 Bit[3:0]: endpoint ID of token 14

DTKNQR4

DTKNQR4 is device IN token sequence learning queue read register 4.

Offset Address	Register Name	Total Reset Value
0x0834	DTKNQR4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 29 Bit[27:24]: endpoint ID of token 28 … Bit[7:4]: endpoint ID of token 23 Bit[3:0]: endpoint ID of token 22

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DVBUSDIS

DVBUSDIS is a device VBUS discharge time register.

Offset Address	Register Name	Total Reset Value
0x0828	DVBUSDIS	0x0000_17D7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dvbusdis															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	dvbusdis	Device VBUS discharge time

DVBUSPULSE

DVBUSPULSE is a device VBUS pulsing time register.

Offset Address	Register Name	Total Reset Value
0x082C	DVBUSPULSE	0x0000_05B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dvbuspulse											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	dvbuspulse	Device VBUS pulse time.

DTHRCTL

DTHRCTL is a device threshold control register.

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Offset Address	Register Name	Total Reset Value
0x0830	DTHRCTL	0x0C10_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				arbprken	reserved	rxthrlen									rxthren	reserved				ahbthrratio				txthrlen						isothren	nonisothren
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27]	RW	arbprken	Arbitrator parking enable. 0: disabled 1: enabled
[26]	RW	reserved	Reserved.
[25:17]	RW	rxthrlen	RX threshold length.
[16]	RW	rxthren	RX threshold enable Some RX FIFO problems may be caused after the RX threshold is enabled, especially when there are RX and babble errors. 0: disabled 1: enabled
[15:13]	RO	reserved	Reserved.
[12:11]	RW	ahbthrratio	AHB threshold ratio. 00: AHB threshold = MAC threshold 01: AHB threshold = MAC threshold/2 10: AHB threshold = MAC threshold/4 11: AHB threshold = MAC threshold/8
[10:2]	RW	txthrlen	TX threshold length.
[1]	RW	isothren	ISO IN endpoint threshold enable. 0: disabled 1: enabled
[0]	RW	nonisothren	Non-ISO IN endpoint threshold enable. 0: disabled 1: enabled

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DIEPEMPMSK

DIEPEMPMSK is a FIFO empty interrupt mask register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0834	DIEPEMPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ineptxfempmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	ineptxfempmsk	IN EP TX FIFO empty interrupt mask. Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DEACHINT

DEACHINT is an interrupt register for each device endpoint.

Offset Address	Register Name	Total Reset Value
0x0838	DEACHINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepint																echinepint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	echoutepint	OUT endpoint interrupt. Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RW	echinepint	IN endpoint interrupt. Bit 15: IN endpoint 0 ... Bit 0: IN endpoint 15

DEACHINTMSK

DEACHINTMSK is an interrupt mask register for each device endpoint.

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Offset Address	Register Name	Total Reset Value
0x083C	DEACHINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepmsk																echinepmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	echoutepmsk	OUT endpoint interrupt mask. Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15 0: masked 1: not masked
[15:0]	RW	echinepmsk	IN endpoint interrupt mask. Bit 16: IN endpoint 0 ... Bit 31: IN endpoint 15 0: masked 1: not masked

DIEPEACHMSKN

DIEPEACHMSKN is an interrupt register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0840 + (0x0004 x *n*) (*n* = 0−15)	DIEPEACHMSKN	0x0040_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nakmsk	reserved			bnainintrmsk	txfifoundrnmsk	reserved	inepnakeffmsk	intknepmismsk	intkntxfempmsk	timeoutmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.

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[13]	RW	nakmsk	NAK interrupt mask. 0: masked 1: not masked
[12:10]	RO	reserved	Reserved.
[9]	RW	bnainintrmsk	BNA interrupt mask. 0: masked 1: not masked
[8]	RW	txfifoundrnmsk	FIFO underrun interrupt mask. 0: masked 1: not masked
[7]	RO	reserved	Reserved.
[6]	RW	inepnakeffmsk	IN endpoint NAK effective interrupt mask. 0: masked 1: not masked
[5]	RW	intknepmismsk	IN token received with EP mismatch interrupt mask. 0: masked 1: not masked
[4]	RW	intkntxfempmsk	IN token received when TX FIFO empty interrupt mask. 0: masked 1: not masked
[3]	RW	timeoutmsk	Timeout interrupt mask (non-isochronous endpoints). 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask. 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disable interrupt mask. 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completion interrupt mask. 0: masked 1: not masked

DOEPEACHMSKN

DOEPEACHMSKN is an interrupt register for device OUT endpoint *n*.

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Offset Address	Register Name	Total Reset Value
0x0880 + (0x0004 x *n*) (*n* = 0−15)	DOEPEACHMSKN	0x0080_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	nyetmsk	nakmsk	bbleerrmsk	reserved		bnaoutintrmsk	outpkterrmsk	reserved	back2backsetup	reserved	outtknepdismsk	setupmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RW	nyetmsk	NYET interrupt mask. 0: masked 1: not masked
[13]	RW	nakmsk	NAK interrupt mask. 0: masked 1: not masked
[12]	RW	bbleerrmsk	Babble error interrupt mask. 0: masked 1: not masked
[11:10]	RO	reserved	Reserved.
[9]	RW	bnaoutintrmsk	BNA interrupt mask. 0: masked 1: not masked
[8]	RW	outpkterrmsk	OUT packet error interrupt mask. 0: masked 1: not masked
[7]	RO	reserved	Reserved.
[6]	RW	back2backsetup	Back-to-back setup packets received interrupt mask. 0: masked 1: not masked
[5]	RO	reserved	Reserved.
[4]	RW	outtknepdismsk	OUT token received when endpoint disabled interrupt mask. 0: masked 1: not masked

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[3]	RW	setupmsk	Setup phase done interrupt mask. 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask. 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask. 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completion interrupt mask. 0: masked 1: not masked

DIEPCTL0

DIEPCTL0 is a control register for device control IN endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0900	DIEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	txfnum				stall	reserved	eptype		naksts	reserved	usbactep	nextep			reserved										mps	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable When the IN endpoint works in scatter or gather DMA mode, this bit indicates that the descriptor structure and data buffer used for transmitting data have been set up. When the scatter or gather DMA mode is disabled, this bit indicates that data to be transmitted is ready. 0: invalid 1: valid
[30]	RWSC	epdis	Endpoint disable The application program sets this bit to **1** to end the data transmission of this endpoint. This bit is enabled only in DMA mode. 0: invalid 1: valid

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[29:28]	RO	reserved	Reserved
[27]	WO	snak	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. The controller core can set this bit of an endpoint after this endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	cnak	NAK clear Writing to this bit clears the NAK bit of the endpoint. 0: invalid 1: valid
[25:22]	RW	txfnum	Number of TX FIFOs
[21]	RWSC	stall	Stall handshake The application program can set this bit. The controller core clears this bit after the endpoint receives the setup packet. 0: invalid 1: valid
[20]	RO	reserved	Reserved
[19:18]	RO	eptype	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	naksts	NAK status. 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	reserved	Reserved.
[15]	RO	usbactep	USB activation endpoint 0 This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid 1: valid
[14:11]	RO	nextep	Next endpoint. This field specifies the ID of the next endpoint that receives data.
[10:2]	RO	reserved	Reserved.

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[1:0]	RW	mps	Minimum packet size 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DOEPCTL0

DOEPCTL0 is a control register for device control OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B00	DOEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	reserved				stall	snp	eptype		naksts	reserved	usbactep	reserved													mps	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable. When the scatter/gather DMA is enabled: 0: The descriptor structure and the data RX function of the data buffer are disabled. 1: The descriptor structure and the data RX function of the data buffer are enabled. When the scatter/gather DMA is disabled: 0: The function of receiving data from the USB module to the memory is disabled. 1: The function of receiving data from the USB module to the memory is enabled.
[30]	RO	epdis	Endpoint disable The application program cannot disable OUT control transfer endpoint 0. 0: enabled 1: disabled
[29:28]	RO	reserved	Reserved.

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[27]	WO	snak	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. The controller core can set this bit of an endpoint after this endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	cnak	NAK clear Writing to this bit clears the NAK bit of the endpoint. 0: invalid 1: valid
[25:22]	RO	reserved	Reserved
[21]	RWSC	stall	Stall handshake The application program can set this bit. The controller core clears this bit after the endpoint receives the setup packet. 0: invalid 1: valid
[20]	RW	snp	Snooping mode This bit is used to set the endpoint to the snooping mode. In snooping mode, the controller core checks whether the OUT packet is correct after it sends the packet to the application memory. 0: invalid 1: valid
[19:18]	RO	eptype	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	naksts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	reserved	Reserved
[15]	RO	usbactep	USB activation endpoint 0 This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid 1: valid
[14:2]	RO	reserved	Reserved.

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[1:0]	RW	mps	Minimum packet size. 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DIEPCTLN

DIEPCTLN is a control register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + (0x0020 x *n*) (*n* = 0−15)	DIEPCTLN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EPEna	EPDis	SetD1PID_SetOddFr	SetD0PID_SetEvenFr	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID_EO_FrNum	USBActEP	NextEp					MPS									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable. When the scatter or gather DMA is enabled: 0: The descriptor structure and the data TX function of the data buffer are disabled. 1: The descriptor structure and the data TX function of the data buffer are disabled. When the scatter/gather DMA is disabled: 0: The data on endpoints is not ready. 1: The data on endpoints is ready.
[30]	RWSC	EPDis	Endpoint disable This bit applies to the IN and OUT endpoints. The application program can set this bit to **1** to stop the data transmission/reception of an IN/OUT endpoint. 0: enabled 1: disabled

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[29]	WO	SetD1PID_SetOddFr	DATA1 PID/odd micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA1 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to odd micro-frames by setting this bit to **1**. 0: invalid 1: valid
[28]	WO	SetD0PID_SetEvenFr	DATA0 PID/even micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA0 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to even micro-frames by setting this bit to **1**. 0: invalid 1: valid
[27]	WO	SNAK	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. For an OUT endpoint, this bit is set after the controller core receives the transfer completion interrupt or the OUT endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	CNAK	NAK clear Writing to this bit clears the NAK bit of an IN/OUT endpoint. 0: invalid 1: valid
[25:22]	RW	TxFNum	Number of TX FIFOs. Shared FIFO operation: 0: non-periodic TX FIFO Other values: specified periodic TX FIFO number Dedicated FIFO operation: Number of FIFOs. This field is valid only for IN endpoints.

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[21]	RW	Stall	Stall handshake (RW) This bit applies to the non-control transfer and non-real-time transfer IN and OUT endpoints. If this bit is set to **1**, the application program blocks the token packets transmitted from the USB host controller to the endpoint. 0: invalid 1: valid For the control endpoint (RWSC), this bit is set to **1** by the application program and cleared by the controller core only when the endpoint receives the setup token. 0: invalid 1: valid
[20]	RW	Snp	Snooping mode This bit is used to set the OUT endpoints to the snooping mode. In snooping mode, the controller core does not check whether the OUT packet is correct before sending the packet to the application memory. 0: invalid 1: valid
[19:18]	RW	EPType	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	NAKSts	NAK status. 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	DPID_EO_FrNum	Endpoint data PID. 0: DATA0 1: DATA1 Even/Odd frame. Non-scatter/Gather DMA mode: 0: even frame 1: odd frame Scatter/Gather DMA mode: Reserved.
[15]	RWSC	USBActEP	USB activation endpoint 0 This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid 1: valid

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[14:11]	RW	NextEp	Next endpoint. This field specifies the ID of the next endpoint that receives data.
[10:0]	RW	MPS	Maximum packet size.

DOEPCTLN

DOEPCTLN is a control register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B00 + (0x0020 x *n*) (*n* = 0−15)	DOEPCTLN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EPEna	EPDis	SetD1PID_SetOddFr	SetD0PID_SetEvenFr	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID_EO_FrNum	USBActEP	NextEp			MPS											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable. When the scatter or gather DMA is enabled: 0: The descriptor structure and the data RX function of the data buffer are disabled. 1: The descriptor structure and the data RX function of the data buffer are enabled. When the scatter/gather DMA is disabled: 0: The function of receiving data from the USB module to the memory is disabled. 1: The function of receiving data from the USB module to the memory is enabled.
[30]	RWSC	EPDis	Endpoint disable This bit applies to the IN and OUT endpoints. The application program can set this bit to **1** to stop the data transmission/reception of an IN/OUT endpoint. 0: enabled 1: disabled

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[29]	WO	SetD1PID_SetOddFr	DATA1 PID/odd micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA1 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to odd micro-frames by setting this bit to **1**. 0: invalid 1: valid
[28]	WO	SetD0PID_SetEvenFr	DATA0 PID/even micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA0 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to even micro-frames by setting this bit to **1**. 0: invalid 1: valid
[27]	WO	SNAK	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. For an OUT endpoint, this bit is set after the controller core receives the transfer completion interrupt or the OUT endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	CNAK	NAK clear Writing to this bit clears the NAK bit of an IN/OUT endpoint. 0: invalid 1: valid
[25:22]	RW	TxFNum	Number of TX FIFOs. Shared FIFO operation: 0: non-periodic TX FIFO Other values: specified periodic TX FIFO.number Dedicated FIFO operation: Number of FIFOs. This field is valid only for IN endpoints.
[21]	RW	Stall	Stall handshake (RW). Endpoint control (RWSC).

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[20]	RW	Snp	Snooping mode This bit is used to set the OUT endpoint to the snooping mode. In snooping mode, the controller core does not check whether the OUT packet is correct before sending the packet to the application memory. 0: invalid 1: valid
[19:18]	RW	EPType	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	NAKSts	NAK status. 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	DPID_EO_FrNum	Endpoint data PID. 0: DATA0 1: DATA1 Even/Odd frame. Non-scatter/Gather DMA mode: 0: even frame 1: odd frame Scatter/Gather DMA mode: Reserved.
[15]	RWSC	USBActEP	USB activation endpoint This bit applies to the IN and OUT endpoints and indicates whether an endpoint is valid. 0: invalid 1: valid
[14:11]	RW	NextEp	Next endpoint. This field specifies the ID of the next endpoint that receives data.
[10:0]	RW	MPS	Maximum packet size.

DIEPINTn

DIEPINTn is an interrupt register for device IN endpoint *n*.

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Offset Address	Register Name	Total Reset Value
0x0908 + (0x0020 x *n*) (*n* = 0−15)	DIEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	TxfifoUndm_OutPktErr	TxFEmp	INEPNakEff_Back2BackSETup	INTknEPMis_StsPhseRcvd	INTknTXFEmp_OUTTknEPdis	TimeOUT_SetUp	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RWSC	StupPktRcvd	Whether setup packets are received. 0: no 1: yes
[14]	RWSC	NYETIntrpt	NYET interrupt. NYET response TX interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[13]	RWSC	NAKIntrpt	NAK interrupt. NAK TX interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[12]	RWSC	BbleErrIntrpt	Babble error interrupt. Endpoint received babble interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[11]	RWSC	PktDrpSts	Packet drop status interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[10]	RO	reserved	Reserved.

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[9]	RWSC	BNAIntr	BNA interrupt. An interrupt is generated when descriptor access is not ready. 0: An interrupt is cleared. 1: An interrupt is generated.
[8]	RWSC	TxfifoUndrn_OutPktErr	FIFO underrun interrupt. An interrupt is generated when the FIFO underrun conditions are transmitted. The interrupt is valid when the following conditions are met: • OTG_EN_DED_TX_FIFO is 1. • Thresholding is enabled. OUT packet error. An interrupt is generated when an overrun or CRC error is detected. The interrupt is valid when the following conditions are met: • OTG_EN_DED_TX_FIFO is 1. • Thresholding is enabled.
[7]	RO	TxFEmp	TX FIFO empty status interrupt. An interrupt is generated when the TX FIFO is empty or half empty. **NOTE** This bit is valid only for IN endpoints. 0: An interrupt is cleared. 1: An interrupt is generated.
[6]	RWSC	INEPNakEff_Back2BackSETup	IN endpoint NAK effective interrupt. An interrupt is generated when the IN endpoint bit is set. Back-to-back setup package received interrupt. An interrupt is generated when the core receives more than three back-to-back setup packets. 0: An interrupt is cleared. 1: An interrupt is generated.
[5]	RWSC	INTknEPMis_StsPhseRcvd	An interrupt is generated when the IN tokens with mismatch EP are received. A control write pulse is received. 0: An interrupt is cleared. 1: A control write pulse is received.
[4]	RWSC	INTknTXFEmp_OUTTknEPdis	An interrupt is generated if IN tokens are received when the corresponding TX FIFO is empty. An interrupt is generated if OUT tokens are received when endpoints are disabled. 0: An interrupt is cleared. 1: An interrupt is generated.

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[3]	RWSC	TimeOUT_SetUp	Timeout interrupt. An interrupt is generated when timeout conditions are detected. Setup phase done interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[2]	RWSC	AHBErr	AHB error interrupt. An interrupt is generated when an AHB error occurs during AHB read/write operations in internal DMA mode. 0: An interrupt is cleared. 1: An interrupt is generated.
[1]	RWSC	EPDisbld	Endpoint disable interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[0]	RWSC	XferCompl	Transfer completion interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.

DOEPINTn

DOEPINTn is an interrupt register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B08 + (0x0020 x *n*) (*n* = 0−15)	DOEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	TxfifoUndrn_OutPktErr	TxFEmp	INEPNakEff_Back2BackSETup	INTknEPMis_StsPhseRcvd	INTknTXFEmp_OUTTknEPdis	TimeOUT_SetUp	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RWSC	StupPktRcvd	Whether setup packets are received. 0: no 1: yes

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[14]	RWSC	NYETIntrpt	NYET interrupt. NYET response TX interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[13]	RWSC	NAKIntrpt	NAK interrupt. NAK TX interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[12]	RWSC	BbleErrIntrpt	Babble error interrupt. Endpoint received babble interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[11]	RWSC	PktDrpSts	Packet drop status interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[10]	RO	reserved	Reserved.
[9]	RWSC	BNAIntr	BNA interrupt. An interrupt is generated when descriptor access is not ready. 0: An interrupt is cleared. 1: An interrupt is generated.
[8]	RWSC	TxfifoUndrn_OutPktErr	FIFO underrun interrupt. An interrupt is generated when the FIFO underrun conditions are transmitted. The interrupt is valid when the following conditions are met: – OTG_EN_DED_TX_FIFO is 1. – Thresholding is enabled. OUT packet error. An interrupt is generated when an overrun or CRC error is detected. The interrupt is valid when the following conditions are met: – OTG_EN_DED_TX_FIFO is 1. – Thresholding is enabled.
[7]	RO	TxFEmp	TX FIFO empty status interrupt. An interrupt is generated when the TX FIFO is empty or half empty. This bit is valid only for IN endpoints. 0: An interrupt is cleared. 1: An interrupt is generated.

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[6]	RWSC	INEPNakEff_Back2BackSETup	IN endpoint NAK effective interrupt. An interrupt is generated when the IN endpoint bit is set. Back-to-back setup package received interrupt. An interrupt is generated when the core receives more than three back-to-back setup packets. 0: An interrupt is cleared. 1: An interrupt is generated.
[5]	RWSC	INTknEPMis_StsPhseRcvd	An interrupt is generated when the IN tokens with mismatch EP are received. A control write pulse is received. 0: An interrupt is cleared. 1: An interrupt is generated.
[4]	RWSC	INTknTXFEmp_OUTTknEPdis	An interrupt is generated if IN tokens are received when the corresponding TX FIFO is empty. An interrupt is generated if OUT tokens are received when endpoints are disabled. 0: An interrupt is cleared. 1: An interrupt is generated.
[3]	RWSC	TimeOUT_SetUp	Timeout interrupt. An interrupt is generated when timeout conditions are detected. Setup phase done interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[2]	RWSC	AHBErr	AHB error interrupt. An interrupt is generated when an AHB error occurs during AHB read/write operations in internal DMA mode. 0: An interrupt is cleared. 1: An interrupt is generated.
[1]	RWSC	EPDisbld	Endpoint disable interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.
[0]	RWSC	XferCompl	Transfer completion interrupt. 0: An interrupt is cleared. 1: An interrupt is generated.

DIEPTSIZ0

DIEPTSIZ0 is a transfer size register for device IN endpoint 0.

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Offset Address	Register Name	Total Reset Value
0x0910	DIEPTSIZ0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			PktCnt	reserved			XferSize
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:19]	RW	PktCnt	Number of packets.
[18:7]	RO	reserved	Reserved.
[6:0]	RW	XferSize	Transferred data size.

DOEPTSIZ0

DOEPTSIZ0 is a transfer size register for device OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B10	DOEPTSIZ0	0x0000_0000

Bit	31	30 29	28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	SUPCnt		reserved		PktCnt	reserved				XferSize
Reset	0	0 0	0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:29]	RW	SUPCnt	Number of setup packets. 00: 0 packets 01: 1 packet 10: 2 packets 11: 3 packets
[28:20]	RO	reserved	Reserved.
[19]	RW	PktCnt	Number of packets.
[18:7]	RO	reserved	Reserved.
[6:0]	RW	XferSize	Transferred data size.

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DIEPTSIZn

DIEPTSIZn is a transfer size register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0910 + (0x0020 x *n*) (*n* = 0−15)	DIEPTSIZn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	mc_rxdpid_supcnt			PktCnt								XferSize																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:29]	RW	mc_rxdpid_supcnt	Number of packets (IN endpoint, RW). 00: 0 packets 01: 1 packet 10: 2 packets 11: 3 packets Number of packets (non-periodic IN endpoints, RO). This field is valid only in internal DMA mode. PID of the received data (isochronous OUT endpoints, RO). 00: DATA0 01: DATA2 10: DATA1 11: MDATA Number of setup packets (OUT endpoint, RW). 01: 1 packet 10: 2 packets 11: 3 packets
[28:19]	RW	PktCnt	Number of packets.
[18:0]	RW	XferSize	Transferred data size.

DOEPTSIZn

DOEPTSIZn is a transfer size register for device OUT endpoint *n*.

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Offset Address	Register Name	Total Reset Value
0x0B10 + (0x0020 x *n*) (*n* = 0−15)	DOEPTSIZn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	mc_rxdpid_supcnt			PktCnt								XferSize																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:29]	RW	mc_rxdpid_supcnt	Number of packets (IN endpoint, RW). 00: 0 packets 01: 1 packet 10: 2 packets 11: 3 packets Number of packets (non-periodic IN endpoints, RO). This field is valid only in internal DMA mode. PID of the received data (isochronous OUT endpoints, RO). 00: DATA0 01: DATA2 10: DATA1 11: MDATA Number of setup packets (OUT endpoint, RW). 01: 1 packet 10: 2 packets 11: 3 packets
[28:19]	RW	PktCnt	Number of packets.
[18:0]	RW	XferSize	Transferred data size.

DIEPDMAN

DIEPDMAN is a DMA address register for device IN endpoint *n*.

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Offset Address	Register Name	Total Reset Value
0x0914 + (0x0020 x *n*) (*n* = 0−15)	DIEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address.

DOEPDMAN

DOEPDMAN is a DMA address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B14 + (0x0020 x n) (*n* = 0−15)	DOEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address.

DIEPDMABN

DIEPDMABN is a DMA buffer address register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x091C + (0x0020 x *n*) (*n* = 0−15)	DIEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address.

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DOEPDMABN

DOEPDMABN is a DMA buffer address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B1C + (0x0020 x *n*) (*n* = 0−15)	DOEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address.

DTXFSTSn

DTXFSTSn is a TX FIFO status register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0938	DTXFSTSn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																INEPTxFSpcAvail															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	INEPTxFSpcAvail	Available space for the IN endpoint TX FIFO. 0x0: The endpoint TX FIFO is full. 0x1: One word is available. 0x2: Two words are available. 0xn: *n* words (0 ≤ *n* ≤ 32768) are available. 0x8000: 32768 words are available. Other values: reserved

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13.8 LSADC_CTRL

13.8.1 Overview

The successive approximation register analog-to-digital converter controller (LSADC_CTRL) provides an ADC controller interface to connect to the on-chip LSADC for driving the LSADC developed by HiSilicon and reporting key values.

13.8.2 Features

The LSADC has the following features:

- 3.3 V power voltage
- maximum scanning frequency of 200000 times per second

The LSADC_CTRL has the following features:

- Single start, one channel scanned at a time, interrupt, query, and no deglitch
- Continuous scanning
  - Channels are polled based on ch_vld.
  - Continuous query is started based on Tscan (scanning interval).
  - Deglitch is performed based on Tglitch and the glitch validity is determined.
  - The LSADC conversion result and corresponding channel IDs are reported.
  - The key press interrupt and key change interrupt are reported.

13.8.3 Operating Mode

Single Scanning Procedure

In single read mode (LSADC_CTRL0[model_sel] = 0), the CPU configures the ID of the channel to scanned, scanning mode, and key value mapping table and starts the LSADC to complete a channel scanning. The LSADC_CTRL obtains the ADC conversion value and sets the conversion completion indicator bit while reporting an interrupt. No deglitch is performed in single read mode.

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Figure 13-54 Single scanning procedure

Continuous Scanning Procedure

In continuous scanning mode (LSADC_CTRL0[model_sel] = 1), the CPU configures the continuous scanning interval (Tscan), glitch width (Tglitch), and valid channel ID (ch_vld) based on the application scenario, and starts the LSADC_CTRL. The LSADC_CTRL scans a valid channel within Tscan, and scans the next valid channel when the next scanning time reaches. After all valid channels are scanned, the LSADC_CTRL cyclically scans them again. See Figure 13-56. Figure 13-55 illustrates channel polling in continuous scanning mode.

Figure 13-55 Channel polling in continuous scanning mode

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Figure 13-56 Continuous scanning procedure

Deglitch Procedure

The deglitch circuit adopts the majority decision algorithm. In the deglitch window, if the levels sampled by the ADC are the levels when keys are pressed, the value is considered as a valid key value; otherwise, a glitch signal is considered.

In continuous mode, when valid scanning values are obtained after deglitch, a key press interrupt is reported, and the scanning completion indicator bits are set. As there are sampling errors, the precision of the LSADC result is 6 bits.

Hardware deglitch can be enabled or disabled as required.

Low-Power Mode

The LSADC_CTRL supports the low-power access mode. When the low-power access mode is enabled, the LSADC enters the lower-power sleep mode after conversion. When the next scanning time reaches, the LSADC is woken up from the sleep mode and then ADC conversion is started. See Figure 13-57.

Figure 13-57 Low-power timing

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The LSADC is in the low-power status by default (PD = 1). Before LSADC scanning, the LSADC needs to be woken up (PD = 0) and then enabled (CS = 0) when the rising edge of the next clock arrives to start conversion. The conversion duration is Twork. After conversion, the CS is pulled up to disable the LSADC, and the PD signal is pulled up when the rising edge of the next clock arrives to enable the LSADC to enter the low-power status. When the next scanning time (Tscan) arrives, the preceding operations are repeated.

13.8.4 Register Summary

Table 13-25 describes LSADC_CRTL registers.

Table 13-25 Summary of LSADC_CRTL registers (base address: 0x200B_0000)

Offset Address	Register	Description	Page
0x0000	LSADC_CTRL0	LSADC_CTRL configuration register	13-245
0x0004	LSADC_CTRL1	Deglitch configuration register	13-247
0x0008	LSADC_CTRL2	Scanning interval configuration register	13-247
0x000C	LSADC_CTRL3	LSADC data hold register	13-248
0x0010	LSADC_CTRL4	Interrupt enable register	13-248
0x0014	LSADC_CTRL5	Interrupt status register	13-248
0x0018	LSADC_CTRL6	Interrupt clear register	13-249
0x001C	LSADC_CTRL7	Start configuration register	13-250
0x0020	LSADC_CTRL8	Stop configuration register	13-250

13.8.5 Register Description

LSADC_CTRL0

LSADC_CTRL0 is an LSDAC_CTRL configuration register.

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Offset Address	Register Name	Total Reset Value
0x0000	LSADC_CTRL0	0x0000_80FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lsadc_active_bit								lsadc_data_delta				reserved		deglitch_bypass	reserved	lsadc_reset	power_down_model	model_sel	reserved			ch_b_vld	ch_a_vld	lsadc_zero							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	lsadc_active_bit	LSADC conversion result precision (only eight types of precisions are supported). 8'b11111111: 8-bit precision 8'b11111110: 7-bit precision 8'b11111100: 6-bit precision 8'b11111000: 5-bit precision 8'b11110000: 4-bit precision 8'b11100000: 3-bit precision 8'b11000000: 2-bit precision 8'b10000000: 1-bit precision
[23:20]	RW	lsadc_data_delta	Error range of the LSADC conversion result. In continuous scanning mode, if the difference between two conversion results falls within the error range, the two results are considered as the same.
[19:18]	RO	reserved	Reserved.
[17]	RW	deglitch_bypass	Deglitch bypass (used in continuous scanning mode). 1: bypassed 0: enabled
[16]	RO	reserved	Reserved.
[15]	RW	lsadc_reset	Whether the LSADC enters the reset status. 1: The LSADC enters the reset status. 0: The LSADC exits the reset status.
[14]	RW	power_down_model	Whether power_down is supported. 0: not supported 1: supported
[13]	RW	model_sel	Scanning mode of the LSADC_CTRL. 0: single scanning mode 1: continuous scanning mode

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[12:10]	RO	reserved	Reserved.
[9]	RW	ch_b_vld	LSADC channel B validity. 0: invalid 1: valid
[8]	RW	ch_a_vld	LSADC channel A validity. 0: invalid 1: valid
[7:0]	RW	lsadc_zero	LSADC value when no key is pressed.

LSADC_CTRL1

LSADC_CTRL1 is a deglitch configuration register

Offset Address	Register Name	Total Reset Value
0x0004	LSADC_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	glitch_sample																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	glitch_sample	Deglitch time window (in ms typically). When the LSADC conversion result is retained in the deglitch time window, the conversion result is considered as a valid value; otherwise, a glitch is considered. The deglitch time window cannot be 0 in continuous scanning mode.

LSADC_CTRL2

LSADC_CTRL2 is a scanning interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	LSADC_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	time_scan																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	time_scan	Interval of scanning two channels in continuous scanning mode (in the unit of 0.333 ms). The interval must be greater than the LSADC conversion time, that is, the configured value must be greater than or equal to 14.

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LSADC_CTRL3

LSADC_CTRL3 is an LSADC data hold register.

Offset Address	Register Name	Total Reset Value
0x000C	LSADC_CTRL3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		reserved		lsadc_data_inb		lsadc_data_ina	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RO	reserved	Reserved
[15:8]	RO	lsadc_data_inb	Scanned value of LSADC channel B.
[7:0]	RO	lsadc_data_ina	Scanned value of LSADC channel A.

LSADC_CTRL4

LSADC_CTRL4 is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0010	LSADC_CTRL4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								int_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	int_enable	Scanned value invalid interrupt enable. 0: disabled 1: enabled

LSADC_CTRL5

LSADC_CTRL5 is an interrupt status register.

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Offset Address	Register Name	Total Reset Value
0x0014	LSADC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											lsadc_auto_busy	reserved	reserved	int_flag_inb	int_flag_ina
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[4]	RO	lsadc_auto_busy	LSADC busy indicator in automatic scanning mode. 1: busy 0: idle
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved
[1]	RO	int_flag_inb	Scanned value valid interrupt status of channel B. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_flag_ina	Scanned value valid interrupt status of channel A. 0: No interrupt is generated. 1: An interrupt is generated.

LSADC_CTRL6

LSADC_CTRL6 is an interrupt clear register.

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Offset Address	Register Name	Total Reset Value
0x0018	LSADC_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												reserved	reserved	clr_int_flag_inb	clr_int_flag_ina
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved
[1]	WO	clr_int_flag_inb	Channel B interrupt clear. 1: cleared 0: not cleared
[0]	WO	clr_int_flag_ina	Channel A interrupt clear. 1: cleared 0: not cleared

LSADC_CTRL7

LSADC_CTRL7 is a start configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	LSADC_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	start	LSADC_CTRL start signal. Writing any value to this register starts the LSADC_CTRL.

LSADC_CTRL8

LSADC_CTRL8 is a stop configuration register.

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Offset Address	Register Name	Total Reset Value
0x0020	LSADC_CTRL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	stop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	stop	Automatic scanning stop. In automatic scanning mode, writing any value to this register stops automatic scanning of the LSADC_CTRL. Automatic scanning is restarted only after the start bit is enabled.

13.9 PWM

13.9.1 Overview

The Hi3516A has eight independent pulse width modulation (PWM) outputs in two groups.

13.9.2 Features

Each PWM output has the following features:

- Supports the optional 3 MHz, 24 MHz or 50 MHz clock source.
- Provides an internal 26-bit counter with configurable output frequency. The maximum frequency of the output square waves is 25 MHz (50 MHz/2), and the minimum frequency of the output square waves is 0.045 Hz (3 MHz/67108863).
- Allows you to set the number of high-level beats (26 bits).
- Provides a 10-bit internal counter and allows you to set the number of pulses. A maximum of 1023 pulses are supported. The number of output pulses can be fixed at a value and the always output mode is supported.
  - When pwmn_keep is set to 0 (PWM*n* indicates the PWM ID), PWM*n* outputs the square waves of a specific number, which depends on the setting of the pwmn_num register.
  - When pwmn_keep is set to 1, PWM*n* always outputs square waves.

13.9.3 Operating Mode

The internal working clock of the PWM module is 3 MHz, 24 MHz or 50 MHz. The following takes PWM0 as an example to configure 1-channel PWM output:

Step 1 Select an appropriate clock source, and calculate the number of required cycles and high-level beats.

Step 2 Write the corresponding values to PWM0_CFG0, PWM0_CFG1, and PWM0_CFG2.

Step 3 Set PWM0_CTRL bit[0] to 1 to enable the PWM output.

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----End

For example, to output a 3 kHz waveform with 72.5% high levels and 10 pulses (the duty ratio is 72.5%), calculate the number of high levels as follows:

- If the 3 MHz clock is the source clock, Cycle = 3 MHz/1 kHz ≈ 1000 (0x00003E8 in hexadecimal)
- Number of high levels = Cycle x Duty ratio = 1000 x 72.5% = 725 (0x00002D5 in hexadecimal)

To output a desired waveform, perform the following steps:

Step 1 Write 0x2 to PERI_CRG14, write 0 to PERI_CRG65 bit[10], select the 3 MHz clock as the PWM clock source, and enable the PWM clock.

Step 2 Read PWM0_STATE2 bit[10] until it is 0. This indicates that the PWM module is idle and can output square waves.

Step 3 Write 0x0000_03E8 to PWM0_CFG0.

Step 4 Write 0x0000_02D5 to PWM0_CFG1.

Step 5 Write 0x0000_000A to PWM0_CFG2.

Step 6 Write 0x1 to PWM0_CTRL.

NOTE

The following steps can be skipped. They are used to check whether the square wave is output as expected.

Step 7 Read PWM0_STATE2 bit[10] until it is 1. This indicates that the PWM module is outputting square waves.

Step 8 Read PWM0_STATE0 and compare the queried value with 0x0000_03E8.

Step 9 Read PWM0_STATE1 and compare the queried value with 0x0000_02D5.

Step 10 Read PWM0_STATE2 bit[9:0] and compare the queried value with 0x0A. If PWM0_STATE2 bit[10] is 1, the PWM module is outputting square waves. If PWM0_STATE2 bit[10] is 0, the configured number of square waves are output.

----End

13.9.1 Register Summary

The registers of PWM*n* (*n* = 0−7) have the same functions but their base addresses are different. See Table 13-26.

Table 13-26 Base addresses for the registers of PWM*n*

Value of n	Base Address
0	0x2013_0000
1	0x2013_0020
2	0x2013_0040

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Value of n	Base Address
3	0x2013_0060
4	0x2013_1000
5	0x2013_1020
6	0x2013_1040
7	0x2013_1060

Table 13-27 describes PWM0 registers as an example.

Table 13-27 Summary of PWM0 registers (base address: 0x2013_0000)

Offset Address	Register	Description	Page
0x0000	PWM0_CFG0	PWM0 configuration 0 register	13-253
0x0004	PWM0_CFG1	PWM0 configuration 1 register	13-254
0x0008	PWM0_CFG2	PWM0 configuration 2 register	13-254
0x000C	PWM0_CTRL	PWM0 control register	13-254
0x0010	PWM0_STATE0	PWM0 status 0 register	13-255
0x0014	PWM0_STATE1	PWM0 status 1 register	13-255
0x0018	PWM0_STATE2	PWM0 status 2 register	13-256

13.9.2 Register Description

PWM0_CFG0

PWM0_CFG0 is a PWM0 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						pwm0_period																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.

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[25:0]	RW	pwm0_period	Number of cycles for PWM0. NOTE The configured value must be greater than or equal to 2.

PWM0_CFG1

PWM0_CFG1 is a PWM0 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						pwm0_duty																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:0]	RW	pwm0_duty	Number of level beats for PWM0. If the number is greater than or equal to the number of cycles, the output level is always high. NOTE The configured value must be greater than or equal to 1.

PWM0_CFG2

PWM0_CFG2 is a PWM0 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						pwm0_num										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RW	pwm0_num	Number of square waves output by PWM0.

PWM0_CTRL

PWM0_CTRL is a PWM0 control register.

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Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																													pwm0_keep	pwm0_inv	pwm0_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	pwm0_keep	PWM output mode. 0: PWM0 outputs a fixed number of square waves. 1: PWM0 always outputs square waves.
[1]	RW	pwm0_inv	PWM output control. 0: PWM0 outputs square waves in normal mode. 1: PWM0 outputs square waves in inverted mode.
[0]	RW	pwm0_enable	PWM enable. 0: disabled 1: enabled

PWM0_STATE0

PWM0_STATE0 is a PWM0 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						pwm0_period_st																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:0]	RO	pwm0_period_st	Number of count cycles for the internal module of PWM0.

PWM0_STATE1

PWM0_STATE1 is a PWM0 status 1 register.

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Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	pwm0_duty_st						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25:0]	RO	pwm0_duty_st	Number of high level beats for the internal module of PWM0.

PWM0_STATE2

PWM0_STATE2 is a PWM0 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11	10	9 8	7 6 5 4	3 2 1 0
Name	reserved			pwm0_cnt_st		pwm0_keep_st	pwm0_busy	pwm0_period_st		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:12]	RO	pwm0_cnt_st	Number of remaining square waves output by PWM0. This field is valid only when the following conditions are met: pwm0_busy = 1, pwm0_keep_st = 0
[11]	RO	pwm0_keep_st	Square wave output mode for the internal module of PWM0. 0: PWM0 outputs a fixed number of square waves 1: PWM0 always outputs square waves.
[10]	RO	pwm0_busy	Working status of PWM0. 0: Wave output is complete and PWM0 is idle. 1: PWM0 is outputting square waves.
[9:0]	RO	pwm0_period_st	Number of output square waves for the internal module of PWM0.

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Contents

A Ordering Information A-1

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A Ordering Information

Figure A-1 shows the Hi3516A mark.

Figure A-1 Hi3516A mark

Figure A-2 shows the Hi3516D mark.

Figure A-2 Hi3516D mark

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Table A-1 describes the Hi3516A/Hi3516D mark.

Table A-1 Meaning of the Hi3516A/Hi3516D mark

No.	Item	Description
1	Version number	It indicates the chip version number.
2	Temperature flag	The letter C stands for commercial. It indicates that the chip is for commercial use.
3	Package flag	The letter B indicates the ball grid array (BGA) package.
4	Environmental protection flag	The letter R stands for Restriction of Hazardous Substances (RoHS).
5	Product differentiation flag	It is the last digit of a chip name for differentiating one chip from another one. A stands for the Hi3516A, and D stands for the Hi3516D.

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