Hi3516A/Hi3516D Hardware Design

User Guide

Issue 06

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About This Document

Purpose

This document describes the design recommendations for the schematic diagrams, printed circuit board (PCB), and board heat dissipation of the Hi3516A/Hi3516D.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 06 (2016-10-28)

This issue is the sixth official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

Section 1.3.8 is modified.

Issue 05 (2016-03-28)

This issue is the fifth official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.3.5, the description of the design for VI interfaces are modified.

Section 1.2.5 and section 1.3.8 are modified.

Issue 04 (2015-11-02)

This issue is the fourth official release, which incorporates the following changes:

Chapter 2 PCB Design Recommendations

The description in section 2.1.3 is modified.

Issue 03 (2015-06-15)

This issue is the third official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

The descriptions in sections 1.1.3, 1.2.1, and 1.4 are modified.

Issue 02 (2015-02-10)

This issue is the second official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

The description in section 1.2.5 is modified.

Issue 01 (2014-12-20)

This issue is the first official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

Figure 1-14 and figure 1-15 are modified. Figure 1-18 and figure 1-19 are added.

Chapter 2 PCB Design Recommendations

The description in section 2.1.3 is updated.

The contents related to the Hi3516D are added.

Issue 00B04 (2014-10-20)

This issue is the fourth draft release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

Figure 1-2 and figure 1-17 are modified.

Issue 00B03 (2014-09-25)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.3.3.2, VI interfaces are updated.

Issue 00B02 (2014-09-14)

This issue is the second draft release, which incorporates the following changes:

Chapter 3 is added and other chapters are modified.

Issue 00B01 (2014-07-25)

This issue is the first draft release.

Contents

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Tables

1 Design Recommendations for Schematic Diagrams

NOTE

- This document uses the Hi3516A as an example. Unless otherwise stated, Hi3516D and Hi3516A contents are consistent.
- The Hi3516A DDRC supports the 16-bit or 32-bit data width, whereas the Hi3516D DDRC supports only the 16-bit data width.

1.1 Requirements on External Circuits for Small System

1.1.1 Clocking Circuit

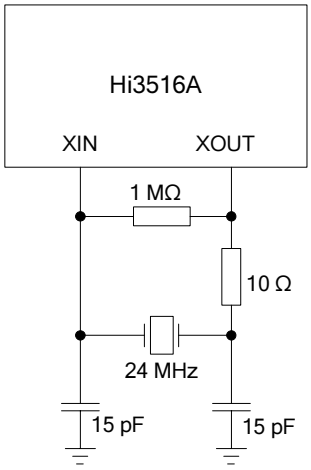
The system clock circuit can be generated by combining the internal feedback circuit of the Hi3516A with an external 24 MHz crystal oscillator circuit.

Figure 1-1 shows the recommended connection mode of the crystal oscillator.

CAUTION

The selected capacitors must match the load capacitor of the crystal oscillator, and it is recommended that the capacitor material be NPO.

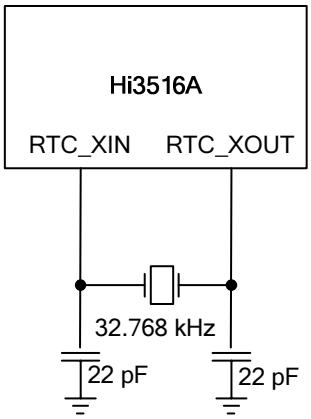
Figure 1-1 Crystal oscillator circuit



The system clock can also be generated by using the external clock circuit and input over the XIN pin.

The Hi3516A integrates a real-time clock (RTC), for which the board must provide the clock circuit. Figure 1-2 shows the recommended connection mode of the crystal oscillator and component specifications.

Figure 1-2 Recommended connection mode of the crystal oscillator and component specifications for the RTC



NOTE

The capacitance of the capacitors in Figure 1-1 must match the load capacitance of the actual crystal oscillator. The inherent load capacitance varies according to the brand and model of the crystal oscillator.

1.1.2 Reset and Watchdog Circuits

The internal or external reset mode of the Hi3516A can be selected based on the status of the POR_SEL pin during power-on.

The WDG_RSTN signal is multiplexed with the SYS_RSTN_OUT signal. When the internal reset mode is selected, the T4 pin is multiplexed as the SYS_RSTN_OUT function. When the external reset mode is selected, the T4 pin is multiplexed as the WDG_RSTN function.

- When the POR_SEL level is low, internal reset is selected. After the master chip is powered on, the internal power-on-reset (POR) circuit resets the entire chip (the reset pulse width is about 130 ms), and the RSTN pin is invalid. In internal reset mode, the RSTN pin can be floated.

  In internal reset mode, peripherals related to the small system (such as the boot flash memory) must release the reset signal before the Hi3516A or they release the reset signals simultaneously. Otherwise, exceptions such as system boot failure may occur.

  You are advised to multiplex the T4 pin of the Hi3516A as the SYS_RSTN_OUT function. Then a reset signal is output to reset the peripherals related to the small system (such as the boot flash memory).
- When the POR_SEL level is high, external reset is selected. In this case, the RSTN pin is a reset signal input pin. The valid reset signal must have low-level pulse, and the pulse width must be greater than 12 input clock cycles of the XIN pin. Typically, the reset pulse width is 100–300 ms.

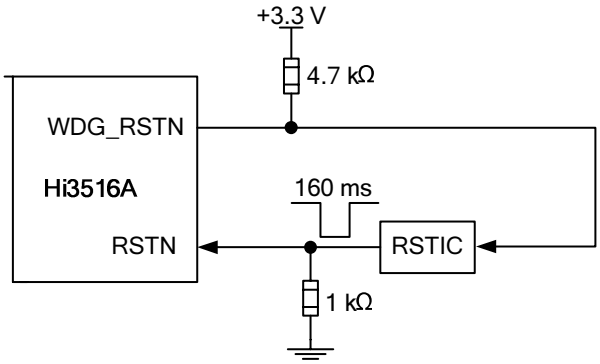
  When the WDG takes effect, the WDG_RSTN pin outputs low level continuously and is restored to high level until the RSTN pin detects a low level reset signal. The WDG_RSTN/SYS_RSTN_OUT pin must not be connected to the RSTN pin directly.

CAUTION

Because the WDG_RSTN pin is an open drain (OD) output pin, it must connect to an external pull-up resistor. A 4.7 kΩ resistor is recommended.

Figure 1-3 shows the typical external reset and watchdog circuit.

Figure 1-3 Typical external reset and watchdog circuit



1.1.3 JTAG Interface

Table 1-1 describes the signals of the JTAG interface.

Table 1-1 Signals of the JTAG interface

Signal	Description
TCK	JTAG clock input. This signal must connect to a pull-down resistor on the board when the JTAG function is used.
TDI	JTAG data input. This signal must connect to a pull-up resistor on the board when the JTAG function is used.
TMS	JTAG mode select input. This signal must connect to a pull-up resistor on the board when the JTAG function is used.
TRSTN	JTAG reset input. This signal must connect to a pull-down resistor on the board when the JTAG function is used.
TDO	JTAG data output. This signal must connect to a pull-up resistor on the board when the JTAG function is used.

NOTE

For details about the impedance of the pull-up and pull-down resistors on the board, see Figure 1-3.

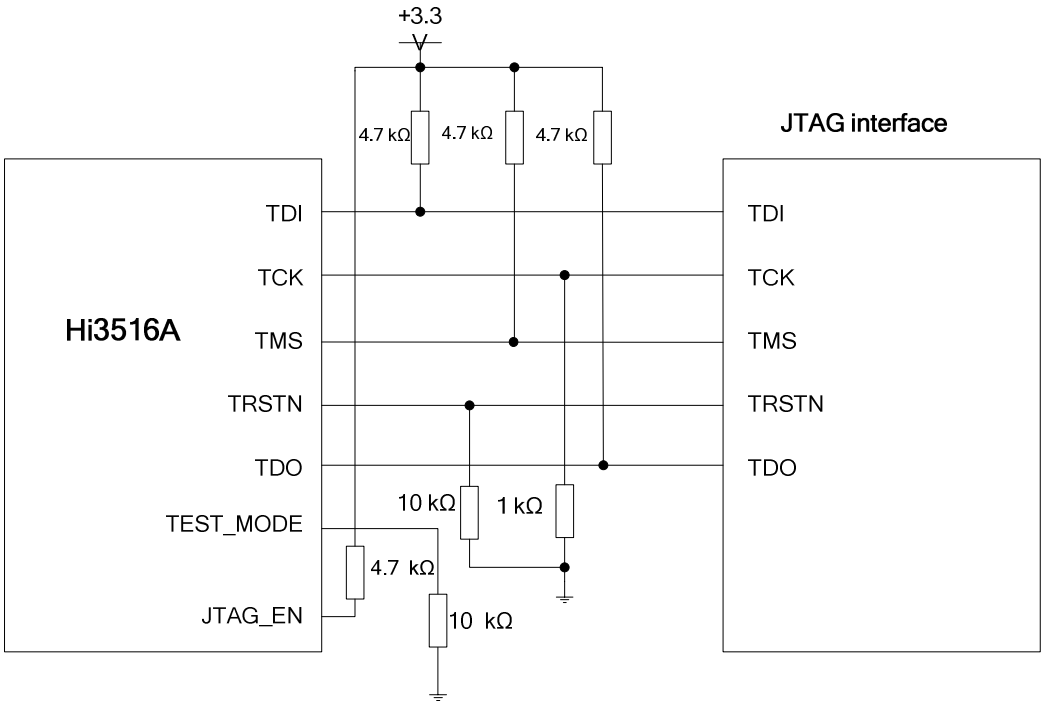
The Hi3516A can be set to normal mode or test mode by configuring the TEST_MODE pin. For details, see Table 1-2.

Table 1-2 TEST_MODE pin configuration

TEST_MODE	Description
0	The Hi3516A works in normal mode.
1	The Hi3516A works in test mode. In this case, the design for testability (DFT) test can be conducted.

Figure 1-4 shows the JTAG connection mode and standard connector pins. If the JTAG function is used, connect the JTAG_EN pin on the board to a 4.7 kΩ pull-up resistor.

Figure 1-4 JTAG connection mode and standard connector pins



1.1.4 System Configuration Circuit for Hi3516A Hardware Initialization

The working mode of each module needs to be configured based on the pull-up and pull-down resistor status of configuration pins during the Hi3516A initialization. Table 1-3 describes hardware configuration signals.

Table 1-3 Hardware configuration signals

Signal	Direction	Description
JTAG_EN	I	JTAG debug enable 0: disabled 1: enabled
BOOT_SEL	I	Boot mode select 0: SPI flash 1: NAND flash
SFC_DEVICE_MODE	I	SPI flash select 0: SPI NOR flash 1: SPI NAND flash
SFC_BOOT_MODE	I	Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode

Signal	Direction	Description
		1: 4-byte address mode Boot mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire mode 1: 4-wire mode
SFC_NAND_BOOT_PIN[1:0]	I	Error correcting code (ECC) type of the SPI NAND flash 00: reserved 01: 8-bit ECC 10: reserved 11: 24-bit ECC
SFC_NAND_BOOT_PIN2	I	Page size of the SPI NAND flash 0: 2 KB 1: 4 KB
POR_SEL	I	Reset mode select 0: reset by the internal POR module 1: reset by the external reset pin
BOOTROM_SEL	I	BOOTROM boot enable 0: booting from the other space (determined by BOOT_Sel) 1: booting from the BOOTROM
TEST_MODE	I	Mode select 0: functional mode 1: test mode

1.1.5 DDR Circuit

1.1.5.1 Introduction

The Hi3516A DDRC interface supports the DDR3 and DDR3L.

The Hi3516A DDRC has 15 address lines and 32-bit data lines. Each DDR3 supports DDR training and a maximum of 4 Gbits capacity and 1600 Mbit/s bit rate.

1.1.5.2 DDR Topology

Figure 1-5 shows the topology of the Hi3516A connected to one 16-bit DDR3/DDR3L SDRAM.

Figure 1-5 Topology of the Hi3516A connected to one 16-bit DDR3/DDR3L SDRAM

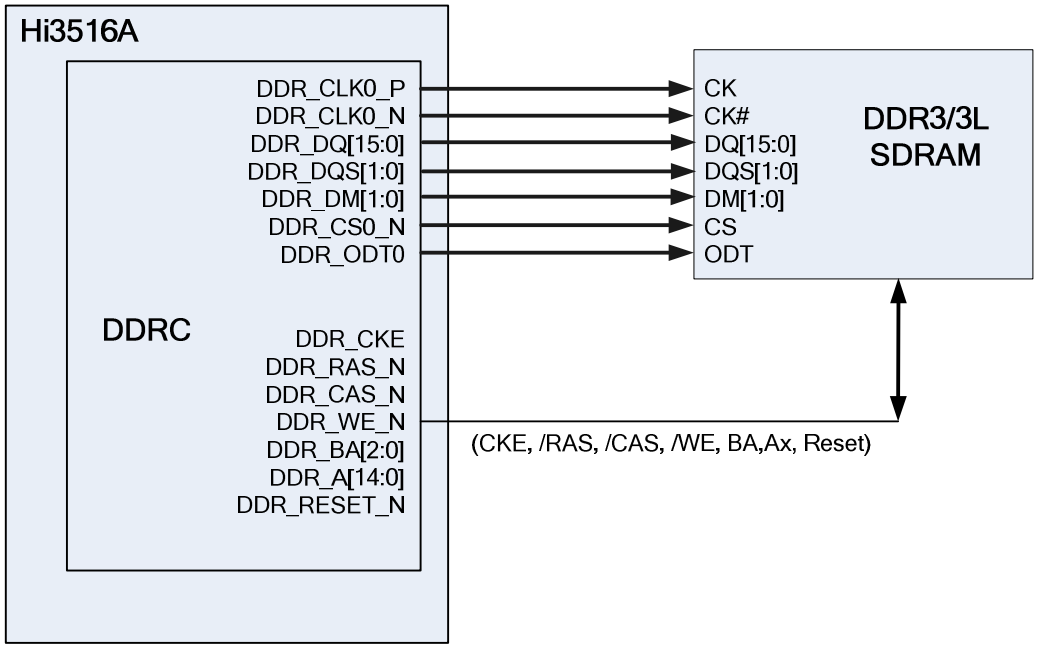
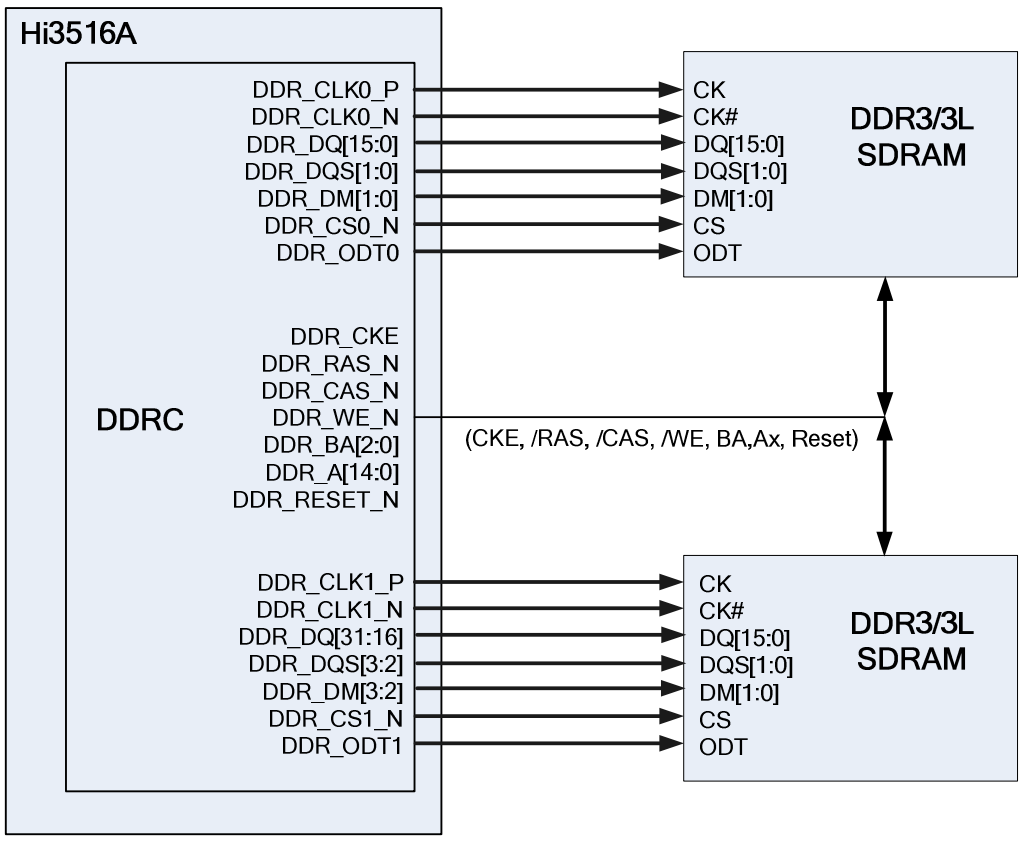


Figure 1-6 shows the topology of the Hi3516A connected to two 16-bit DDR3/DDR3L SDRAMs.

Figure 1-6 Topology of the Hi3516A connected to two 16-bit DDR3/DDR3L SDRAMs



1.1.5.3 Design Recommendations for Matched Modes

Bidirectional DQ and DQS Signals

The DQ, DQS_P, and DQS_N signals of the Hi3516A connect directly to the DQ, DQS_P, and DQS_N signals of the DDR respectively.

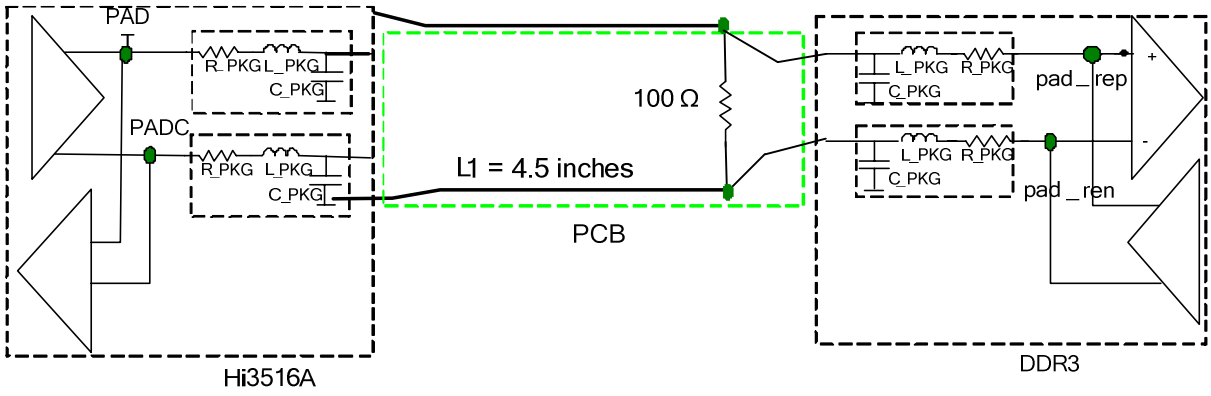
Differential Clocks

The following describes how to connect DDR differential clock signals of the Hi3516A to the DDR.

The Hi3516A has two pairs of differential clock signals: DDR3_CLK0_N/DDR3_CLK0_P and DDR3_CLK1_N/DDR3_CLK1_P.

In one-drive-one mode, a 100 Ω±1% resistor is connected between the DDR_CLK_N and DDR_CLK_P signals at the load end, as shown in Figure 1-7.

Figure 1-7 Differential clock signals DDR_CLK_N and DDR_CLK_P in one-drive-one mode



1.1.5.4 Address Signals and Command Signals

When the DDRC connects to one 16-bit DDR3/DDR3L, a 33 Ω resistor must be connected in series at the source end for the address and command signals in one-drive-one mode, as shown in Figure 1-8.

When the DDRC connects to two 16-bit DDR3/DDR3L SDRAMs, two 33 Ω resistors must be connected in series at the T point for the address and command signals in one-drive-two mode, as shown in Figure 1-9.

Figure 1-8 Address and command signals in one-drive-one mode

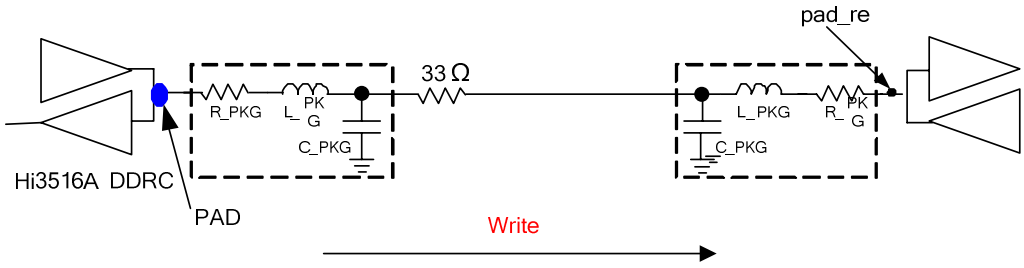
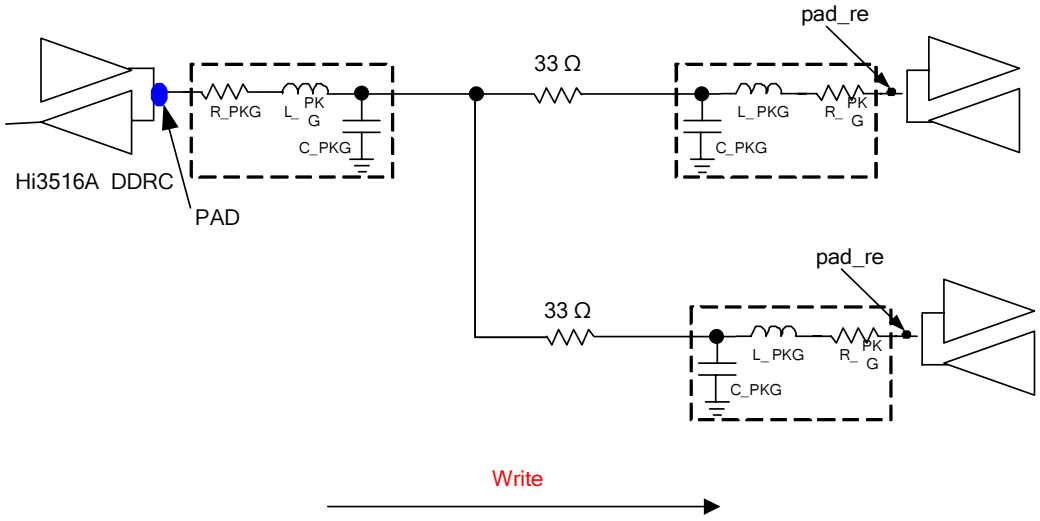


Figure 1-9 Address and command signals in one-drive-two mode



1.1.5.5 DM Signals

The data mask (DM) signals of the Hi3516A connect directly to the DM signals of the DDR.

1.1.6 SPI Flash Circuit

1.1.6.1 Introduction

The Hi3516A SPI flash controller supports the SPI NOR flash and SPI NAND flash. The NAND flash controller supports parallel NAND flash memories.

When the Hi3516A boots from the SPI flash, the Hi3516A reads the boot from the flash memory controlled by the SFC_CS1N pin (R3 pin) by default after releasing the reset signal. In this case, you are advised to connect the CS pin of the boot flash memory to the SFC_CS1N pin of the SPI flash controller.

When the Hi3516A boots from the NAND flash, the Hi3516A reads the boot from the flash memory controlled by the NF_CSN0 pin (L1 pin) by default after releasing the reset signal. In this case, you are advised to connect the CS pin of the boot flash memory to the NF_CSN0 pin of the NAND flash controller.

The Hi3516A NAND flash controller can automatically adapt to NAND flash memories with various specifications and it does not need to be adapted externally.

1.1.6.2 Signal Processing

Matched Design for the SPI Flash

Table 1-4 describes the recommended design when an external SPI flash is connected.

Table 1-4 Recommended design when an SPI flash is connected

Signal	Recommended Design
SFC_CLK	The signal connects to a 33 Ω resistor in series at the Hi3516A end.
SFC_DIO SFC_DOI SFC_WP SFC_HOLD SFC_CSN	The signals are connected directly. SFC_WP needs to connect to a 4.7 kΩ pull-down resistor. SFC_HOLD and SFC_CSN need to connect to a 4.7 kΩ pull-up resistor.

Matched Design for the NAND Flash

The NAND flash interface supports the 8-bit single-level cell (SLC) or multi-level cell (MLC) NAND flash.

Table 1-5 describes the recommended design when an external NAND flash is connected.

Table 1-5 Recommended design when a NAND flash is connected

Signal	Recommended Design
NF_WEN NF_REN	The signal connects to a 33 Ω resistor in series at the Hi3516A end.
NF_DQ[0:7] NF_ALE NF_CLE	The signals are directly connected.

1.2 Power Supply Design

For details about the power supply design parameters for the Hi3516A, see section 2.7 "Electrical Specifications" in the *Hi3516A/Hi3516D HD IP Camera SoC Data Sheet*.

1.2.1 Core Power Supplies

The Hi3516A has four types of core power supplies:

- VDD_MEDIA: core power of the Media that connects to the 1.1 V power. The capacity of the power chip must be greater than or equal to 2 A. It is recommended that the power implement the selective voltage binning (SVB) function. For details, see the latest schematic diagram of the Hi3516A demo board.
- VDD_DDR: core power of the DDR that connects to the 1.1 V power. The current of the power chip must be greater than or equal to 1 A. It is recommended that the SVB voltage adjustment function be reserved. For details, see the latest schematic diagram of the Hi3516A demo board.
- VDD_CPU: core power of the CPU that connects to the 1.1 V power. The current of the power chip must be greater than or equal to 1 A. It is recommended that the SVB voltage adjustment function be reserved. For details, see the latest schematic diagram of the Hi3516A demo board.
- VDD: core power of the parts excluding the Media, DDR and CPU that connects to the 1.1 V power. The current of the power chip must be greater than or equal to 1 A. It is recommended that the SVB voltage adjustment function be reserved. For details, see the latest schematic diagram of the Hi3516A demo board.

NOTE

For details about the Hi3516A core power design solutions, see the latest *Hi3516A/Hi3516D Core Power Combination Solutions and Power Consumption Comparison* and *Description of the Hi3516A/Hi3516D Power Consumption, PCB Design, and Tailoring Design*.

1.2.2 DDR Power Supply

The Hi3516A DDRC supports the DDR3 and DDR3L. The power voltage and reference voltage (Vref) are 1.5 V and 0.75 V for the DDR3 or 1.35 V and 0.675 V for the DDR3L respectively. The Hi3516A and DDR must share the 1.5 V or 1.35 V power.

A separate power chip must be provided on the board to supply power to the DDR3 or DDR3L and the 1.5 V or 1.35 V power pins (VDDIO_DDR and VDDIO_CK_DDR pins) of the Hi3516A DDRC.

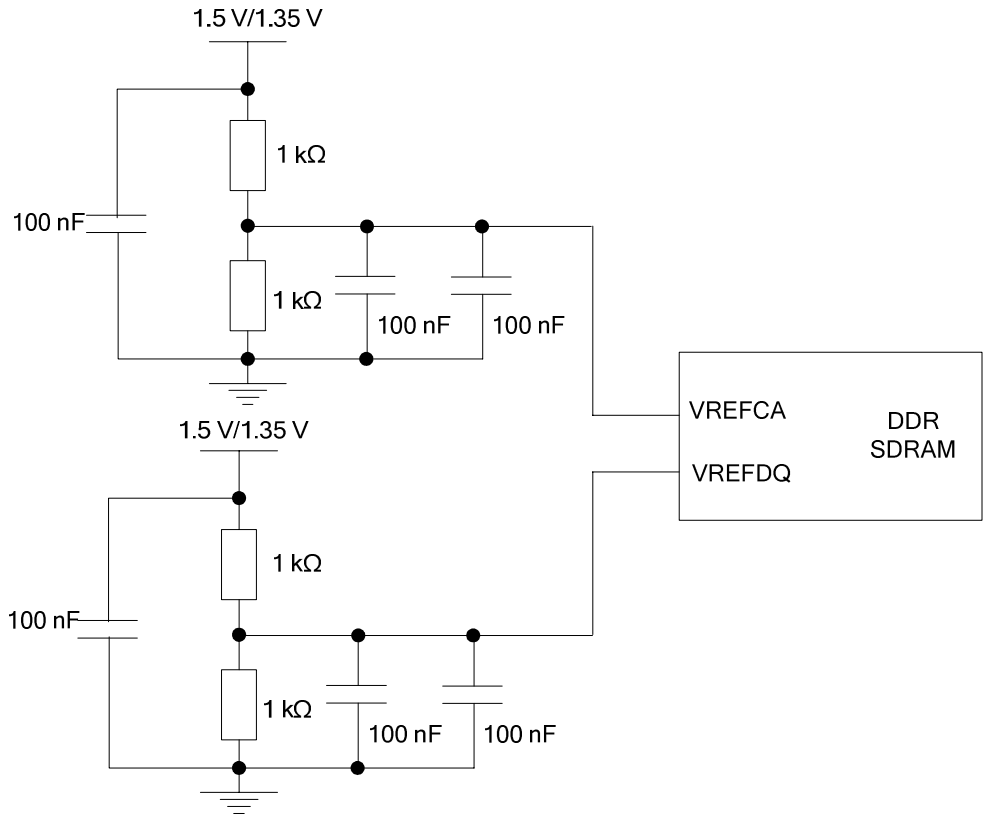
The DDR phase-locked loop (PLL) power pins (AVDD_DDRPLL) connect to the 3.3 V power. The pins must be isolated from the 3.3 V I/O power of the master chip by using 1 kΩ@100 MHz electromagnetic interference (EMI) beads.

The power is supplied to the Vref pins of the DDR3/DDR3L (0.75 V/0.675 V) by using 1 kΩ±1% voltage-divider resistors. A 0.1 μF decoupling capacitor is connected close to each power pin and reference power pin.

The Vref power of the master chip is integrated, and therefore no external design is required.

Figure 1-10 shows the reference design of the DDR3/DDR3L Vref power. Note that power must be separately supplied to VREFCA and VREFDQ.

Figure 1-10 Reference design of the DDR3/DDR3L voltage-divider circuit (at the DDR side)



1.2.3 I/O Power Supplies

The I/O power pins (DVDD33) connect to the 3.3 V digital power.

The I/O power pins for the ETH interface (DVDDIO_RGMII) support 3.3 V, 2.5 V, or 1.8 V power, and the levels of the connected power and interface must be the same.

The I/O power for the sensor clock, reset, and configuration pins (DVDD3318_SENSOR) supports the 3.3 V or 1.8 V voltage, and the levels of the connected power and interface must be the same.

The power pins of the mobile industry processor interface (MIPI)/low-voltage differential signaling (LVDS) interface (AVDD18_MIPI) connect to the 3.3 V or 1.8 V power.

The MIPI and LVDS pins of the Hi3516A can be multiplexed as the parallel data function, and the level can be 3.3 V or 1.8 V, and the levels of the connected power and interface must be the same.

When the MIPI or LVDS module is used, AVDD18_MIPI must connect to the 1.8 V power.

When the MIPI and LVDS pins are multiplexed as the parallel data function, AVDD18_MIPI must connect to the 3.3 V or 1.8 V power.

The power pins of the video input (VI) interfaces (DVDD3318_VI) support 3.3 V or 1.8 V power, and the levels of the connected power and interface must be the same.

1.2.4 PLL Power Supplies

The Hi3516A has two PLL power supplies:

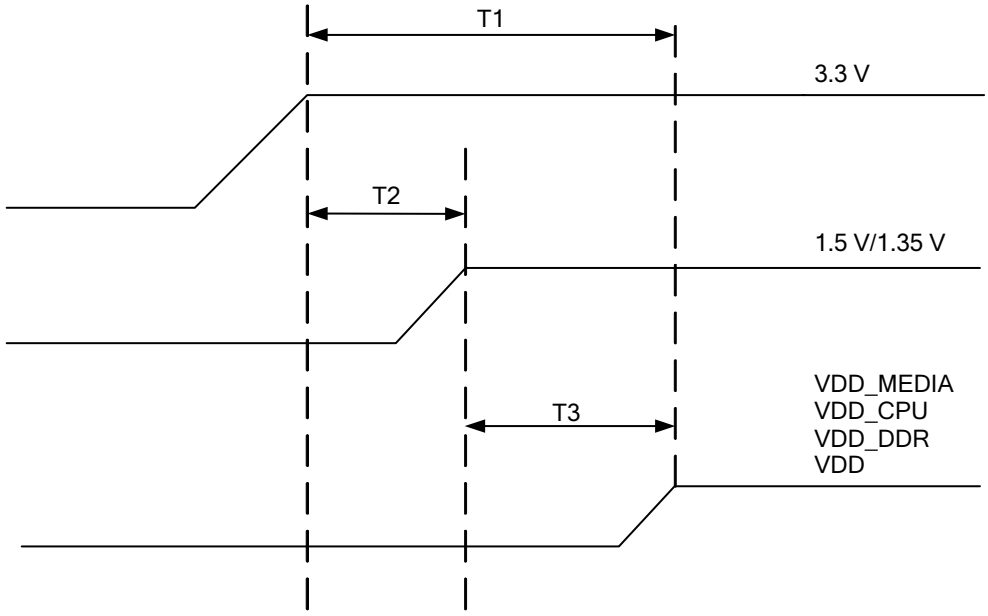
- AVDD11_PLL: connects to the 1.1 V power.
- AVDD33_PLL: connects to the 3.3 V power.

It is recommended that the PLL power supplies be isolated by using 1 kΩ@100 MHz EMI beads. For details, see the schematic diagram of the Hi3516A demo board.

1.2.5 Power-On and Power-Off Sequences

Figure 1-11 and Figure 1-12 show the requirements on the power-on and power-off sequences of the core power supplies, DDR power supplies, and I/O power supplies respectively.

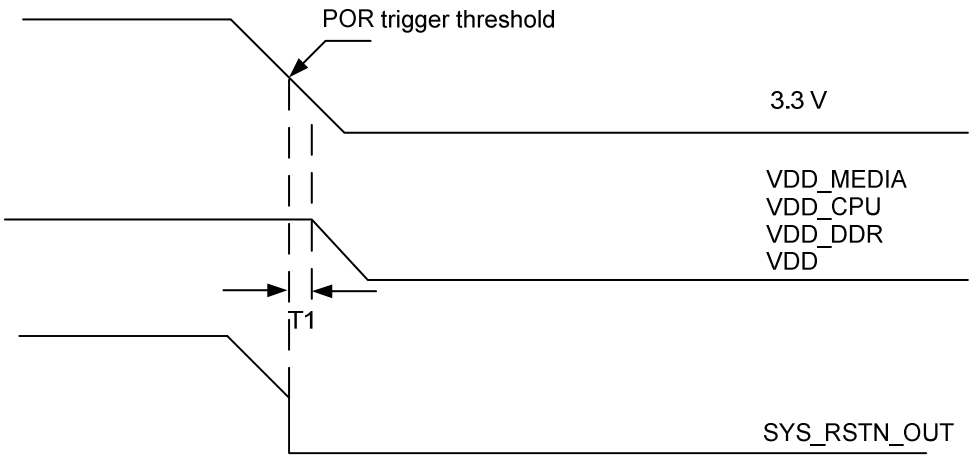
Figure 1-11 Power-on sequence



NOTE

- 0 < T1 ≤ 100 ms, T2 > 0, T3 > 0
- The VDD_MEDIA, VDD_CPU, and VDD_DDR core power supplies must be power on simultaneously. Then after about 10 ms, the VDD core power supply is powered on.

Figure 1-12 Power-off sequence



NOTE

- T1 > 0
- Power off the 3.3 V and 1.35 V/1.5 V power supplies in sequence. When the level of the 3.3 V power decreases to the POR trigger threshold (2.1 V to 2.6 V), the POR is triggered, and then the four core power supplies start to be turned off.

CAUTION

During power-off, the POR module may be in any of the following states:

- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is greater than 2.6 V at the 5 μs time point, the POR module considers that there is a power fluctuation and does not trigger reset, and the SYS_RSTN_OUT pin retains the high level.
- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is greater than 2.1 V but less than or equal to 2.6 V at the 5 μs time point, the POR module triggers reset at this moment (5 μs time point during the timing) and the SYS_RSTN_OUT pin outputs low level.
- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is less than or equal to 2.1 V within 5 μs after timing starts, the POR module triggers reset when the voltage of DVDD33 decreases to 2.1 V and the SYS_RSTN_OUT pin outputs low level.

1.2.6 Precautions

Ensure that the output voltage of each power supply meets the requirements even when ripples and noises occur. For details about the power supply requirements of each module, see

section the section "Electrical Specifications" in the *Hi3516A 720p IP Camera SoC Data Sheet*.

1.3 Peripheral Interfaces

1.3.1 USB Port

USB Power Supply

The analog power AVDD33_USB must be isolated from the digital power. You are advised to use planes to reduce the parasitic effect, coupling noise, and power supply impedance. In addition, filter capacitors are placed close to pins.

1.3.2 MAC Interface

Interface Design

The MAC interface supports the reduced gigabit media-independent interface (RGMII), reduced media-independent interface (RMII), media independent interface (MII) modes. Figure 1-13 to Figure 1-15 show the signal connection in the three modes.

Figure 1-13 Signal connection in RGMII mode

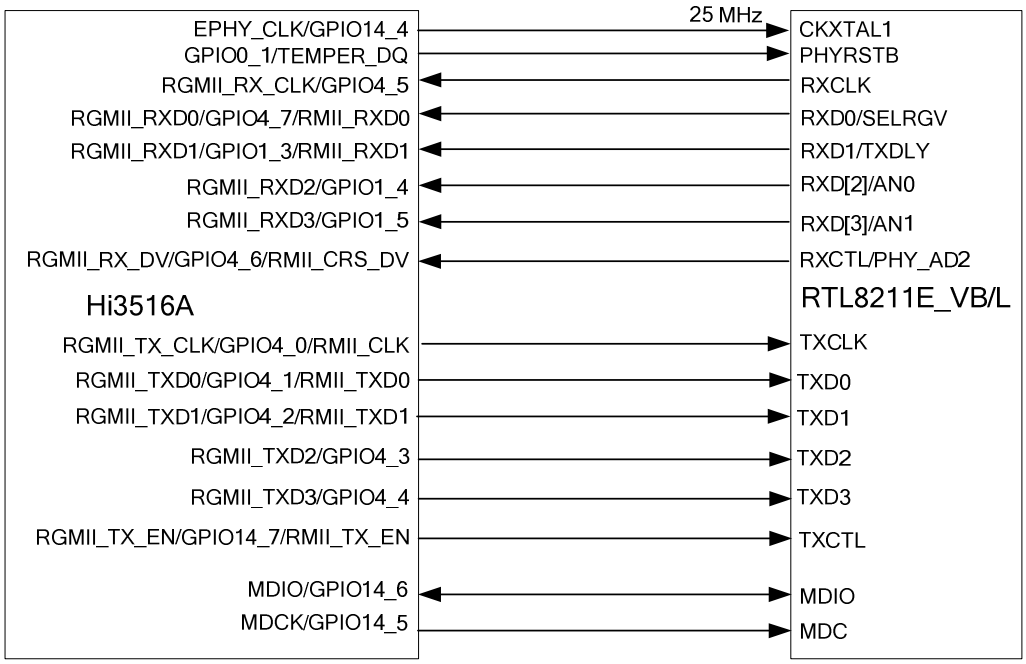
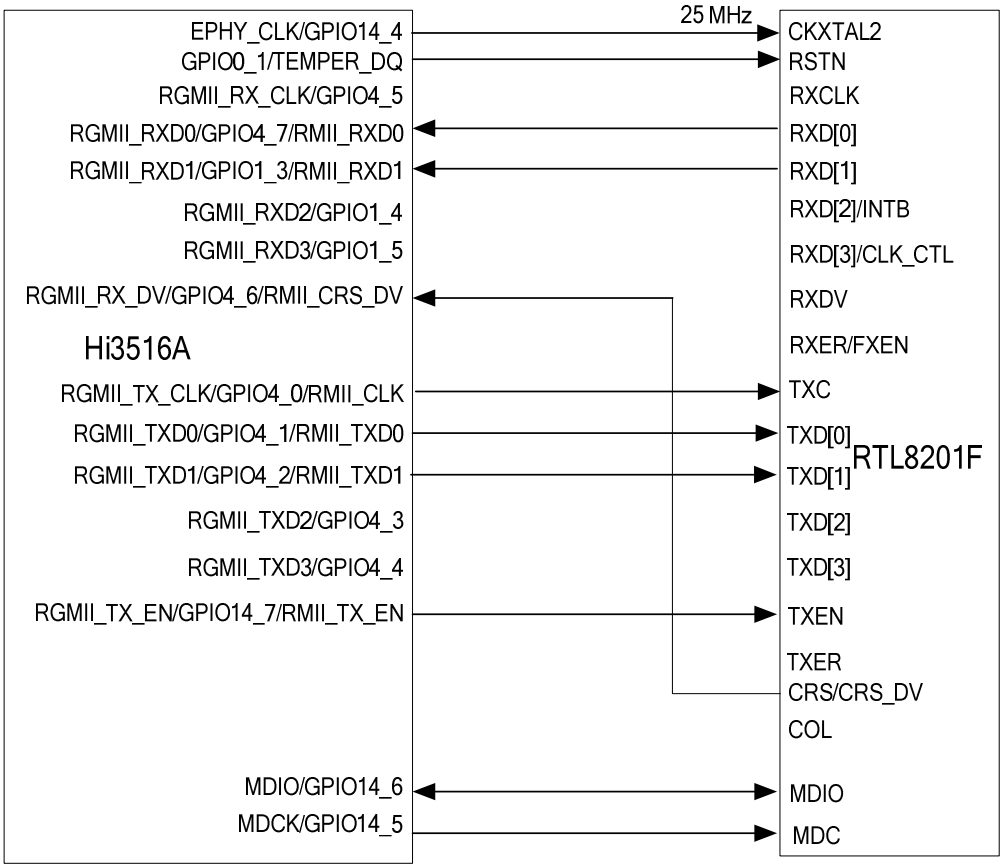


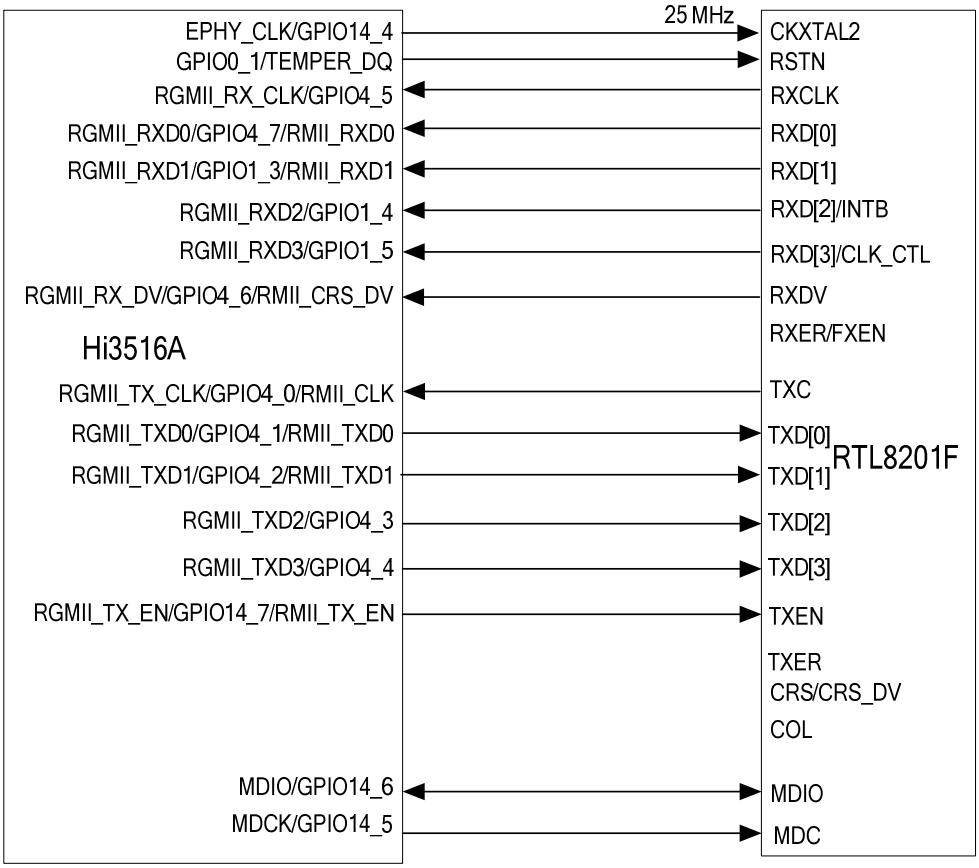
Figure 1-14 Signal connection in RMII mode



NOTE

The TXD[2], TXD[3], and TXER pins of RTL8201F have internal weak pull-down resistors and can be floated externally.

Figure 1-15 Signal connection in MII mode



NOTE

The TXER pin of RTL8201F has internal weak pull-down resistors and can be floated externally.

All MAC signals are connected in point-to-point topology. The design recommendations are as follows:

- Connect a 4.7 kΩ pull-up resistor to the MDIO signal.
- It is recommended that the MDCK signal connect to a 33 Ω resistor in series close to the source end to ensure the signal quality.
- It is recommended that the TXCK, TXD0−TXD3, RXCK, and RXD0−RXD3 signals connect to 33 Ω resistors in series close to the source end to ensure the signal quality.

1.3.3 Audio and Video Interfaces

1.3.3.1 Analog Video Interface

The Hi3516A has a video digital-to-analog converter (VDAC) the supports the maximum resolution of 960H.

- The VDAC_CVBS pin must connect to an external 75 Ω±1% pull-down resistor.
- The analog power pin AVDD33_VDAC of the VDAC interface must be isolated from the 3.3 V digital power by using an EMI bead, and sufficient filter capacitor must be placed close to the AVDD33_VDAC pin.

- The external reference resistor pin VDAC_IREF must connect to a 1kΩ±1% pull-down resistor.
- The Hi3516A supports automatic composite video broadcast signal (CVBS) detection. If no CVBS monitor is connected, the Hi3516A automatically disables the VDAC module to reduce power consumption. If the CVBS detection function is required, no video buffer needs to be designed. If isolation and ESD are essential in some applications, the video buffer is recommended.

1.3.3.2 Analog Audio Interface

The Hi3516A provides stereo input/output interfaces (AC_LINEL, AC_LINER, AC_OUTL, and AC_OUTR).

- The 3.3 V power for the audio digital-to-analog converter (ADAC) must be isolated from the 3.3 V system power, and the filter capacitor connected to the AC_VREF pin must be greater than or equal to 10 μF.
- AC_LINEL and AC_LINER can act as the line or MIC input channels. If the input device is a passive MIC device, the MIC_BIAS must be added to the input signal. If the input device is an active line-in device (such as a PC), no bias is required.
- The blocking capacitors connected to the audio input signal must be placed close to the Hi3516A. The 4.7 μF capacitors are recommended.
- The audio output signals AC_OUTL and AC_OUTR each must connect to a 470 kΩ pull-down resistor.
- The output amplitude of the ADAC at full scale is 0.875 Vrms.
- You are advised to connect an audio amplifier and filter circuit to the audio output pins AC_OUTL and AC_OUTR, which ensures excellent audio quality.
- The following are the overall design recommendations (including but not limited to) for the intercom application scenario:
  - Ensure that the MIC and speaker are as far as possible to minimize coupling between them.
  - The MIC must be sealed to prevent sound passing from the mechanical part to the MIC. The speaker should also be sealed.
  - Ensure that the size of the speaker cavity opening is more than 15% of the sectional area of the cavity. Typically, a larger sound cavity indicates better low-frequency audio quality but poorer echo cancellation effect.
  - The MIC opening is typically a round hole with 0.8−1.2 mm diameter. No sound cavity is designed for the MIC, that is, the MIC opening is a straight hole.
  - The MIC is sealed with rubber or foam to prevent the crosstalk of the speaker in the IP camera or crosstalk to the MIC due to the sound vibration of the IP camera. Ensure that there is no crosstalk and resonance in the IP camera.

1.3.4 I²S Interface

The Hi3516A has an inter-IC sound (I^2S) interface. The I^2S signals multiplexed with the VI, secure digital input/output (SDIO), and UART2 & JTAG pins are derived from the same source. Figure 1-16 and Figure 1-17 show the 5-wire connections in I^2S master mode and I^2S slave mode respectively.

Figure 1-16 5-wire connection in I²S master mode

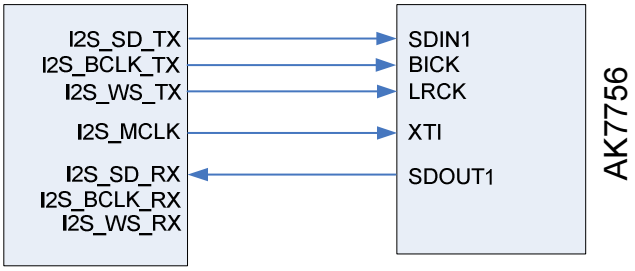
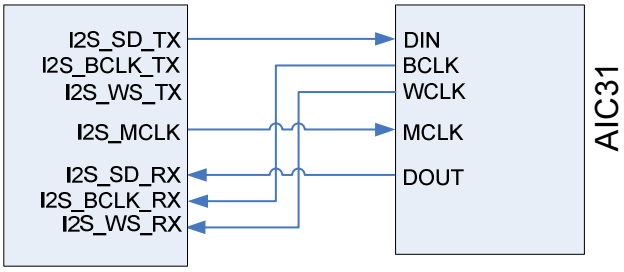


Figure 1-17 5-wire connection in I²S slave mode



1.3.5 VI Interfaces

There are two types of VI interfaces: parallel CMOS VI interface and multi-mode VI interface. Only one of them takes effect at a time.

- The parallel CMOS VI interface supports 1.8 V or 3.3 V voltage.

The parallel CMOS interface supports data in the formats of RAW, BT.1120, BT.656, and BT.601, and its maximum frequency is 148.5 MHz.

- The multi-mode VI interface can be multiplexed as the parallel CMOS interface or MIPI/LVDS interface by configuring registers.
  - When the multi-mode VI interface is multiplexed as the parallel CMOS interface, all the functions are the same as those of the parallel CMOS VI interface.
  - When the multi-mode VI interface is multiplexed as the MIPI/LVDS interface, it has two groups of differential clock signals. Each group of differential clock signals corresponds to four groups of differential data signals. A group of differential clock signals and the corresponding four groups of differential data signals are called MIPI0, and the other group of differential clock signals and the corresponding four groups of differential data signals are called MIPI1.

    If the output signals of the connected sensor include a pair of differential clock signals and more than four pairs of differential data signals, the Hi3516A does not support this sensor.

    The maximum frequency of the MIPI/LVDS interface is 500 MHz.

    The MIPI interface has an embedded 100 Ω matched resistor. Therefore, there is no need to design or reserve external resistors.
  - It is recommended that the 16-bit CMOS interface sensor be connected to D0−D15 in sequence (the reverse order D15−D0 is also supported).

– It is recommended that the *n*-bit ($n < 16$) CMOS interface sensor be connected to D0−D_{n-1} in sequence (any consecutive *n* bits are supported).

1.3.6 VO Interface

The Hi3516A has only one physical video output (VO) interface.

- The video output unit (VOU) supports the BT.656 and BT.1120 outputs but not the BT.601 output. The maximum resolution is 1080p@60 fps for the BT.1120 output or D1@30 fps for the BT.656 output.
- The BT.1120 output can be in the format of YUV 4:2:2. The upper eight bits are the Y (luminance) signal, and the lower eight bits are the C (chrominance) signal.
- The VOU has no HS and VS pins, and the line/field signals are embedded in data.

1.3.7 SPI and I²C interfaces

- The Hi3516A has two groups of serial peripheral interface (SPI) pins. SPI0 is used to configure the sensor, and the interface level can be 1.8 V or 3.3 V.
- SPI1 is used to connect to a peripheral, and the interface level must be 3.3 V.
- The Hi3516A has three groups of inter-integrated circuit (I^2C) pins. I^2C0 is used to configure the sensor and is multiplexed with SCLK and SDO of SPI0, and the interface level can be 1.8 V or 3.3 V.
- I^2C1 is used to connect to a peripheral and is multiplexed with SCLK and SDO of SPI1, and the interface level must be 3.3 V.
- I^2C2 is used to connect to a peripheral, and the interface level must be 3.3 V.

1.3.8 SDIO interface

The Hi3516A has two SDIO interfaces. Each interface supports the secure digital extended capacity (SDXC) card and secure digital high capacity (SDHC) card.

The DATA and CMD signals of SDIO must connect to the 10 kΩ pull-up resistors and then connect to the SDIO_VOUT pin.

The requirements on the design of the SDIO0/1_CARD_DETECT and CWPR signals are as follows:

- When the SD card is connected, the SDIO0/1_CARD_DETECT and CWPR signals must connect to 10 kΩ external pull-up resistors, and pull up to 3.3 V power supply.
- When the TF card is connected, SDIO0/1_CARD_DETECT must connect to a 10 kΩ external pull-up resistor, and pull up to 3.3 V power supply, SDIO0/1_CWPR must connect to a 4.7 kΩ external pull-down resistor.
- When the Wi-Fi, 4G, or IC module that is irrelevant to the DETECT and CWPR applications is connected, the SDIO0/1_CARD_DETECT and SDIO0/1_CWPR signals must connect to 4.7 kΩ external pull-down resistors.

CAUTION

When the SDXC interface of the Hi3516A functions as the GPIO interface, for details about the usage method, see the content related to the GPIO interface in the *Hi3516A/Hi3516D Professional HD IP Camera SoC Data Sheet*.

1.3.9 ADC

The Hi3516A supports two analog signal input pins that support AD conversion with 8-bit resolution. The two pins can be multiplexed as general-purpose input/output (GPIO) signals.

Note that the ADC interface cannot be directly connected to the battery when the ADC interface is used to measure the battery level. Otherwise, the battery discharges to IO_VDD through D1 when IO_VDD is powered off and the battery working time is shortened, as shown in Figure 1-18. To measure the battery level by using the ADC interface, the circuit in Figure 1-19 is recommended and the resistance of R1 must be greater than 100 kΩ.

Figure 1-18 Circuit with internal ESD protection

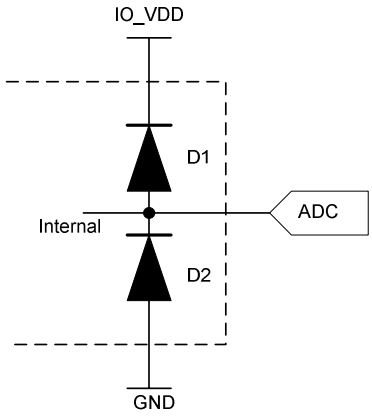
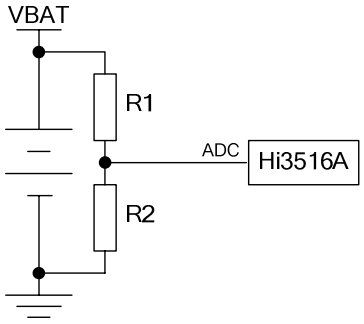


Figure 1-19 Recommended circuit for detecting the battery level by using the ADC interface



1.3.10 RTC

In fixed frequency-division mode, the timing accuracy of the embedded RTC depends on the external crystal oscillator. Select an appropriate crystal oscillator based on its frequency deviation and temperature offset. If high timing accuracy is required, the external integrated RTC is recommended.

1.3.11 PWM

The Hi3516A has eight pulse width modulation (PWM) interfaces.

It is recommended that PWM0 to PWM3 be used to adjust the voltages of four core power supplies. All the PWM interfaces can be multiplexed as GPIOs when they are not used.

1.3.12 UART

The Hi3516A supports four universal asynchronous receiver transmitter (UART) signals. UART0 is used for system debugging.

1.3.13 eFUSE

The AVDD_EFUSE pin must connect to ground (GND).

1.4 Unused Pins

Process unused pins as follows:

- If the JTAG function is not used, connect the JTAG_EN pin to a pull-down resistor (the 4.7 kΩ resistor is recommended), configure the JTAG_TCK, JTAG_TMS, JTAG_TRSTN, JTAG_TDO, and JTAG_TDI pins as GPIO pins. In this case, the JTAG_TCK, JTAG_TMS, JTAG_TRSTN, JTAG_TDO, and JTAG_TDI pins can be floated.
- If internal POR is selected to reset the master chip, connect the POR_SEL pin to a pull-down resistor. In this case, the RSTN pin can be floated.
- If the NAND flash is not used, configure the corresponding pins as GPIO pins. In this case, the pins can be floated.
- If the over-current protection function is not used for the USB module, configure the USB_OVRCUR pin as a GPIO pin. In this case, this pin can be floated.

Process unused module power supplies as follows:

- The 3.3 V or 1.8 V power must be supplied to DVDD3318_VI even if it is not used.
- When the RTC module is not used, AVDD33_RTC needs to connect to the 3.3 V power and cannot be floated, whereas AVDD_BAT can be floated.
- When the USB, audio CODEC, and video DAC are not used, the power pins AVDD33_USB, AVDD33_AC, and AVDD33_VDAC need to connect to the 3.3 V power, and these modules need to be enabled to enter the power-down mode.
- If the SDXC card is used, the DVDD18_SDIO pin can be floated.

2 PCB Design Recommendations

2.1 Small System

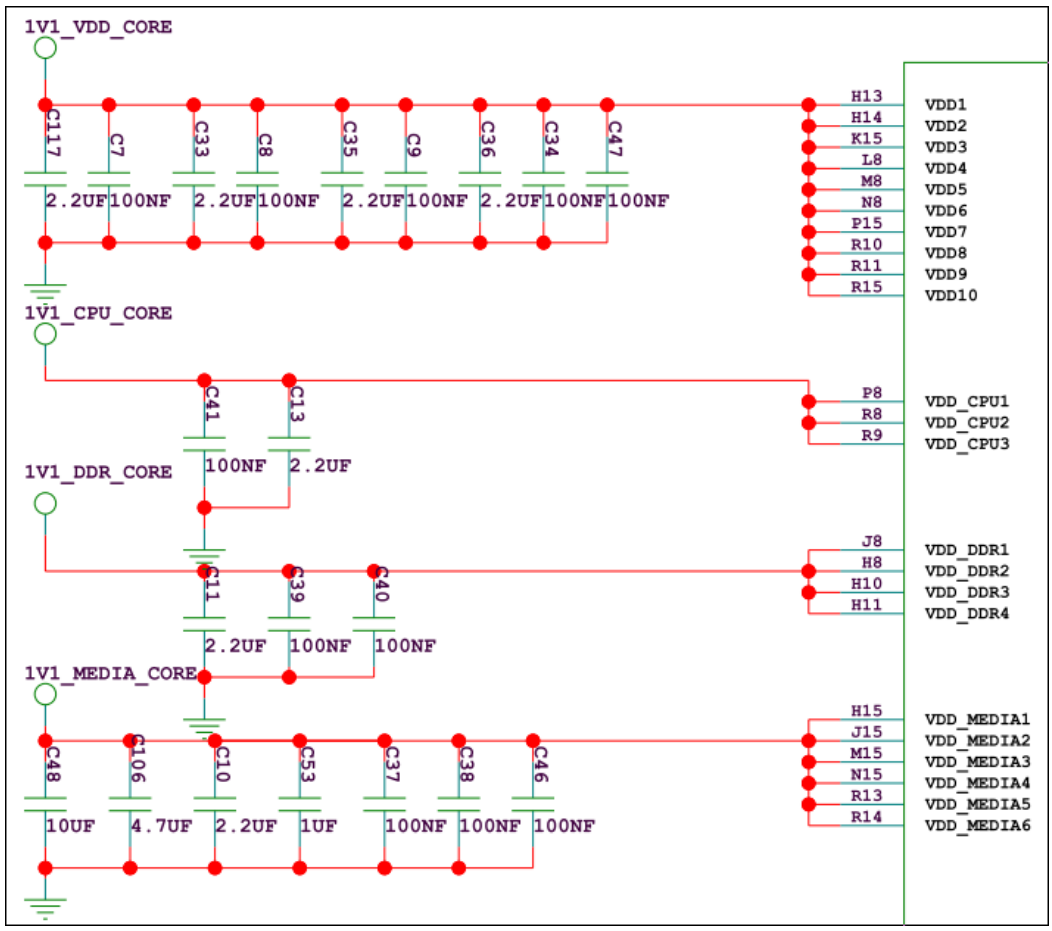
2.1.1 Power Supplies for the Small System

2.1.1.1 Core Power Supply

Type and Number of Filter Capacitors

You are advised to design the type, number, and layout of filter capacitors for the core power supply on a 6-layer or 8-layer PCB by following the design of the Hi3516A demo board or on a 4-layer PCB by following the design of the Hi3516A reference board. The recommended material for the filter capacitors is X7R. Figure 2-1 shows the diagram of the type of filter capacitors for the core power supply.

Figure 2-1 Type of filter capacitors for the core power supply



Routing Mode and Filter Capacitor Layout

Note that the current of the VDD_MEDIA power channel must be at least 2 A and the current of the VDD, VDD_CPU, and VDD_DDR power channels must be at least 1 A.

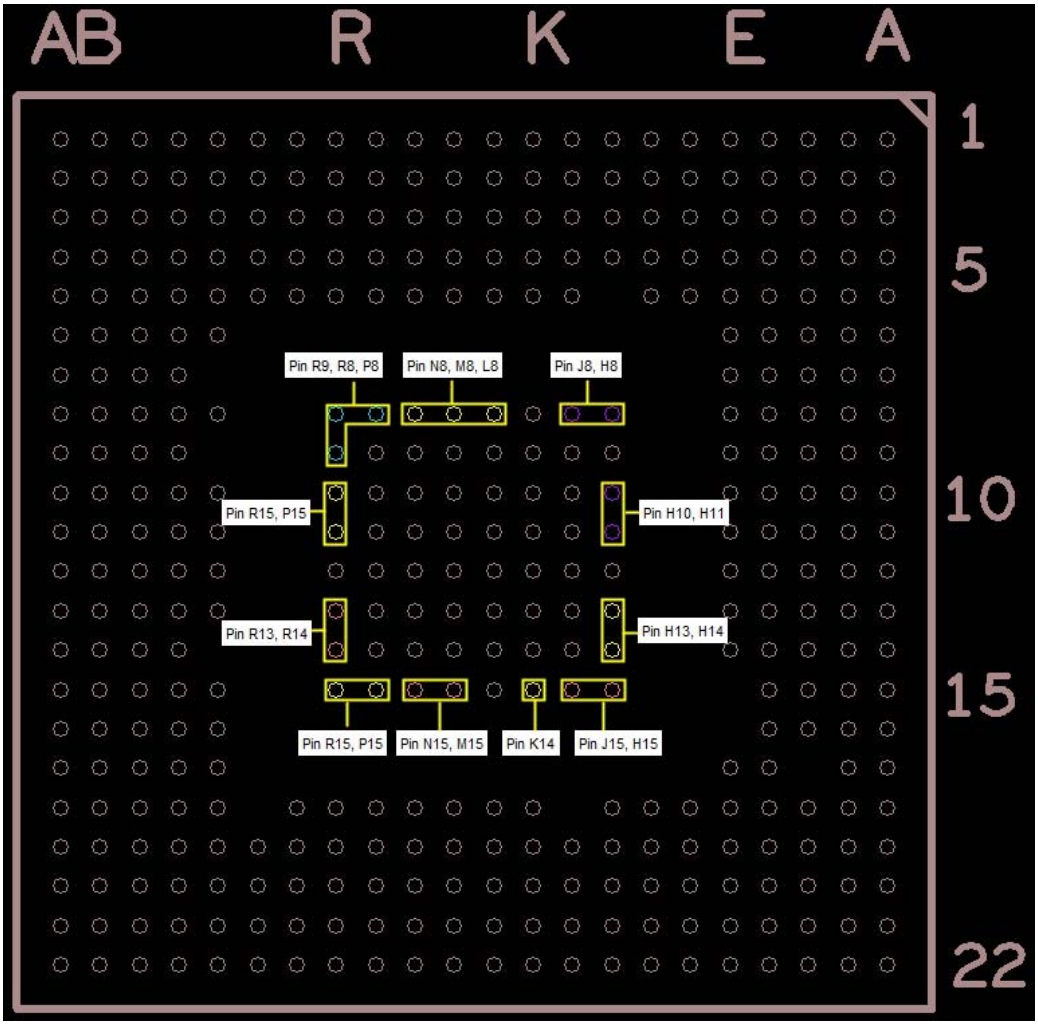
The core power supply design is as follows:

If the core power plane is used, each 100 nF filter capacitor must be placed close to the power pin to reduce the parasitic inductance. Figure 2-2 shows the core power pins on the Hi3516A. Connect decoupling capacitors to these pins as follows:

- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins R9, R8, and P8 each.
- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins N8, M8, and L8 each.
- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins J8 and H8 each.
- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins H13 and H14 each.
- Connect at least one 100 nF capacitor close to the pins N15, M15, J15 and H15 each and a 4.7 µF capacitor shared by these pins.

- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins R15 and P15 each.
- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins R13 and R14 each.
- Connect at least one 2.2 µF capacitor and one 100 nF capacitor close to the pins R10 and R11 each.
- Connect at least one 100 nF capacitor close to the K14 pin.
- Connect at least one 100 nF capacitor close to the pins H10 and H11 each.

Figure 2-2 Core power pins on the Hi3516A



2.1.1.2 DDR Power Supply

The 1.5 V/1.35 V power pins of the DDR3/DDR3L and the Hi3516A DDR need to be connected on the same power network, and decoupling capacitors need to be placed close to the power pins. At least one 10 µF grounding filter capacitor is connected to the Hi3516A DDR power supply.

The VREF power supplies (0.75 V for the DDR3 SDRAM and 0.675 V for the DDR3L SDRAM) must be isolated from other power supplies. You can connect the Hi3516A and the

DDR3 SDRAM or DDR3L SDRAM by using 20-mil or wider traces. Ensure that decoupling capacitors are placed close to each power pin and the VREF is surrounded with GND traces on the PCB. The 1.5 V/1.35 V power pins of the DDR3/DDR3L and the Hi3516A DDR need to be connected on the same power network, and decoupling capacitors need to be placed close to the power pins.

2.1.1.3 I/O Power Supply

At least one 10 μF grounding filter bypass capacitor is connected to the DVDD33 power supply, and each DVDD33 pin is connected to a 100 nF decoupling capacitor close to the power pin. At least one 2.2 μF decoupling capacitor is connected to a group of two or more pins close to the power pin.

2.1.2 Clocking Circuit

Clock

The power and GND pins of the Hi3516A PLL unit include AVDD11_PLL, AVDD33_PLL, and AVSS_PLL. Design the PCB based on the following guidelines:

- AVDD11_PLL is the 1.1 V PLL power. You are advised to isolate it from the 1.1 V board power by using EMI beads. The level deviation of the 1.1 V power must be within ±5%.
- AVDD33_PLL is the 3.3 V PLL power. You are advised to isolate it from the 3.3 V board power by using EMI beads. The level deviation of the 3.3 V power must be within ±5%.
- AVSS_PLL is the reference GND of the PLL circuit. The decoupling capacitors for AVDD11_PLL and AVDD33_PLL must be connected by referring to AVSS_PLL as the GND plane. AVSS_PLL must connect to the digital board GND through a single point.
- The system clock traces of the crystal oscillator circuit must be as short as possible, and be surrounded with GND traces.

2.1.3 DDR Signals

Table 2-1 DDR signal trace lengths in the Hi3516A

Signal Name	Trace Length (mil)
DDR3_A0	201.83
DDR3_A1	164.32
DDR3_A2	196.42
DDR3_A3	206.61
DDR3_A4	148.23
DDR3_A5	218.09
DDR3_A6	275.90
DDR3_A7	226.35
DDR3_A8	146.30
DDR3_A9	219.60

Signal Name	Trace Length (mil)
DDR3_A10	155.01
DDR3_A11	122.30
DDR3_A12	223.65
DDR3_A13	175.30
DDR3_A14	202.66
DDR3_BA0	231.12
DDR3_BA1	151.12
DDR3_BA2	115.77
DDR3_CAS_N	248.99
DDR3_CKE	170.95
DDR3_CLK0_N	167.14
DDR3_CLK0_P	164.24
DDR3_CLK1_N	239.71
DDR3_CLK1_P	235.69
DDR3_CS0_N	153.99
DDR3_CS1_N	264.46
DDR3_ODT_0	109.18
DDR3_ODT_1	228.23
DDR3_RAS_N	222.80
DDR3_RESET_N	190.87
DDR3_WE_N	176.70
DDR3_ZQ	171.95
DDR3_DQ0	222.57
DDR3_DQ1	167.46
DDR3_DQ2	152.33
DDR3_DQ3	133.53
DDR3_DQ4	137.01
DDR3_DQ5	138.90
DDR3_DQ6	226.39
DDR3_DQ7	138.82
DDR3_DM0	162.82

Signal Name	Trace Length (mil)
DDR3_DQS0_N	185.85
DDR3_DQS0_P	178.58
DDR3_DQ8	250.46
DDR3_DQ9	161.06
DDR3_DQ10	197.59
DDR3_DQ11	136.37
DDR3_DQ12	195.56
DDR3_DQ13	164.73
DDR3_DQ14	155.90
DDR3_DQ15	219.89
DDR3_DM1	154.91
DDR3_DQS1_N	184.36
DDR3_DQS1_P	178.48
DDR3_DQ16	124.60
DDR3_DQ17	186.55
DDR3_DQ18	155.31
DDR3_DQ19	145.20
DDR3_DQ20	216.91
DDR3_DQ21	170.24
DDR3_DQ22	241.29
DDR3_DQ23	217.52
DDR3_DM2	166.93
DDR3_DQS2_N	188.39
DDR3_DQS2_P	185.54
DDR3_DQ24	140.91
DDR3_DQ25	244.58
DDR3_DQ26	192.32
DDR3_DQ27	169.03
DDR3_DQ28	170.73
DDR3_DQ29	225.08
DDR3_DQ30	204.54

Signal Name	Trace Length (mil)
DDR3_DQ31	110.28
DDR3_DQS3_N	170.16
DDR3_DQS3_P	173.23
DDR3_DM3	167.88

You are advised to design the DDR traces based on the reference PCB design of HiSilicon.

For details about the DDR traces on a 4-layer PCB, see the Hi3516A reference board. For details about the DDR traces on a 6-layer or 8-layer PCB, see the Hi3516A demo board.

CLK Signals

The following are requirements on the trace length of the clock signal CLK:

- The maximum trace length of the CLK0 and CLK1 signals is 2000 mils.
- The trace of the CLK1 signal is routed based on the CLK0 trace length, and the length deviation must be within ±200 mils.
- The CLK differential signals must be routed in differential mode, and the length deviation of each pair of differential traces must be within ±5 mils.

DQS Signals

The following are requirements on the trace length of DQS signals:

- The maximum trace length of the DQS0, DQS1, DQS2, and DQS3 signals is 1000 mils.
- The trace length of the DQS0 and DQS1 signals must be less than that of the CLK0 signal.
- The trace length of the DQS2 and DQS3 signals must be less than that of the CLK1 signal.
- The DQS differential signals must be routed in differential mode, and the length deviation of each pair of differential traces must be within ±5 mils.

Data Signals DQ[0:31]

The maximum trace length of the data signals DQ[31:0] is 1000 mils.

DM Signals

The maximum trace length of the DM signals is 1000 mils.

Address Signals ADDR[0:14]

The maximum trace length of the address signals ADDR[0:14] and BA[0:2] is 3000 mils.

Control Signals

The maximum trace length of the control signals ODT[0:1], CS[0:1], WE_N, CAS_N, RAS_N, CKE, and RESET is 3000 mils.

PCB Routing Requirements

Route DDR3 signal traces on a PCB based on the following guidelines:

- Ensure that signal traces are as short as possible. Minimize the use of vias to ensure the impedance continuity of traces. The impedance of the single-ended signal trace is 50 Ω, and the impedance of the differential signal trace is 100 Ω.
- Ensure that the reference layer and the layer on which DQ signal traces are routed are not changed. If the reference layer is changed, it is recommended that vias for the GND traces that are used to surround DQ signal traces be punched near the vias for the signal traces. In the ideal situation, one GND via is required for one via of a signal trace. (If the space is insufficient, it is recommended that every two or three vias for the signal traces share one GND via. The number of signal traces that share the same GND via need to be decreased as the DDR working frequency is increased. It is best when one GND via corresponds to one via of the signal trace.)
- Ensure that the distance between the signal trace and the reference plane is far less than the airgap between adjacent parallel signal traces. It is recommended that the airgap between adjacent parallel signal traces be three times the distance between the signal trace and the reference plane. (The airgap can be two and a half times the distance for the 4-layer board due to the space limit, and the routing of the signal traces must comply with the 3W rule.)

2.1.4 ETH Signals

As the rate of GMAC signals is high, you are advised to design the PCB routing based on the following guidelines to reduce signal crosstalk:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Determine the signal trace length based on the clock trace length, and ensure that the length deviation is within ±200 mils.
- Ensure that the GND under the transformer is void.
- The spacing between adjacent traces complies with the 3W rule.
- It is recommended that a 33 Ω resistor connect to the clock signal in series to ensure the signal quality.
- Each pair of differential traces (MDI+_0, MDI-_0, MDI+_1, MDI-_1, MDI+_2, MDI-_2, MDI+_3, and MDI-_3) has the same length. The length deviation must be within ±5 mils, and the impedance of each pair of differential traces is 100 Ω±10%.

2.2 PCB Design Recommendations for Typical Peripheral Interfaces

2.2.1 USB Port

2.2.1.1 PCB Design Recommendations

To ensure good signal quality, route the data lines of the USB 2.0 port in differential mode. You are advised to design the PCB routing based on the following guidelines to provide the 480 MHz/s USB 2.0 port:

- The differential data traces must be short and straight, and the internal differential traces must have the same length. The length deviation must be within ±5 mils.
- Ensure that the impedance of each differential data trace is 90 Ω±10%.
- Route differential data traces on the plane that is close to the GND plane and never change the routing plane.
- Route differential data traces by referencing a complete GND plane, and do not cross the plane splits.
- Minimize the use of vias and corners when routing differential data traces. When corners are required, use arcs or 135° turns rather than a 90° turn. This reduces the signal reflection and impedance variance.
- Keep the differential data traces more than 50 mils away from other high-speed cyclic signals and strong current signals to reduce crosstalk. Keep the differential data traces at least 20 mils away from low-speed non-periodic signals.
- Place the REXT resistor as close as possible to the Hi3516A.

2.2.1.2 USB Power Supply

The Hi3516A has one USB 2.0 port. The USB power pin is AVDD33_USB (3.3 V), and the GND pin is AVSS_USB (3.3 V). The design recommendations are as follows:

AVDD33_USB is the 3.3 V analog power, and AVSS_USB is the 3.3 V analog GND. You are advised to isolate the 3.3 V analog USB power from the 3.3 V digital board power by using EMI beads, and place filter capacitors close to the AVDD33_USB and AVSS_USB pins.

2.2.2 Audio/Video Circuit Design

2.2.2.1 Analog Audio Interface

The Hi3516A has one analog audio interface. Design the PCB routing based on the following guidelines:

- Place the pull-down capacitor connected to AC_VREF close to the Hi3516A.
- Surround the analog audio input and output signal traces with GND traces.
- It is recommended that the DC blocking capacitor connected to AC_LINER and AC_LINEL be placed close to the Hi3516A. For details about the design of resistors and capacitors, see the latest schematic diagram of the Hi3516A peripheral board.
- When the microphone (MIC) input is used, it is recommended that the chip divide a signal into two channels at the near end of the AC_MICBIAS output pin as the corresponding bias levels of the audio-left and audio-right channels, which ensures

excellent audio quality. For details, see the latest schematic diagram of the Hi3516A demo board.

- A 470 kΩ pull-down resistor is connected to AC_OUTL and AC_OUTR close to the output interface to reduce the pop noise during power-on and power-off.

2.2.2.2 VDAC Interface

The Hi3516A provides one VDAC interface.

To ensure the output video quality of the VDAC, design the PCB routing based on the following guidelines:

- Connect the VDAC output pin to a pull-down resistor close to the Hi3516A.
- Place the analog video filter circuit close to the Hi3516A.
- Use a VDAC to drive only a single load. If you need to drive multiple loads to output multi-channel video signals, drives are recommended.
- Do not use the analog video GND plane as the reference plane for other signal traces.
- When corners are required, use arcs or 45° turns rather than a 90° turn, reducing signal reflection.

VDAC Power Supply

AVDD33_VDAC of the VDAC unit is an analog video power pin. Design the PCB routing based on the following guidelines:

- Use a GND plane as the analog video GND and digital GND.
- The deviation of the 3.3 V analog video power must be within ±5%.
- Isolate the 3.3 V analog VDAC power from the 3.3 V board digital power by using EMI beads, and place filter capacitors close to the AVDD33_VDAC pin.

2.2.2.3 VI Interfaces

Design the PCB routing for the parallel CMOS interface based on the following guidelines:

- The length deviation of the data signal traces and clock signal traces must be within ±300 mils.
- The traces must comply with the 3W rule.

When the multi-mode VI interface is multiplexed as the parallel CMOS interface, design the PCB routing based on the same requirements on the parallel CMOS interface.

When the multi-mode VI interface is multiplexed as the MIPI/LVDS interface, design the PCB routing based on the following guidelines:

- The maximum trace length of the MIPI signals is 5000 mils.
- The length deviation of the CK0 and CK1 traces for the MIPI must be within ±500 mils.
- Ensure that each pair of differential signal traces have the same length, the length deviation of each pair of differential signal traces must be within ±5 mils, and the differential impedance must be 100 Ω±10%.
- The length deviation of the MIPI0 data traces and CK0 traces must be within ±300 mils.
- The length deviation of the MIPI1 data traces and CK1 traces must be within ±300 mils.

2.2.2.4 VO Interfaces

The Hi3516A has one BT.1120 VO interface. Design the PCB routing based on the following guidelines:

- The length deviation of the data signal traces and clock signal traces must be within ±300 mils.
- The traces must comply with the 3W rule.

3 ESD Design Recommendations

3.1 Background

As the chip performance and clock frequency become higher, the entire system is more sensitive to external interference. Therefore, you need to pay special attention to the electrostatic discharge (ESD) design during the entire system design.

The ESD tests of the Hi3516A are conducted based on the JEDEC standard. The Hi3516A has passed the ±2000 V test, which meets the industrial standards. However, you need to evaluate the board hardware design and entire system design based on your ESD test standards. This document provides the design recommendations and workarounds based on ESD design risks during the entire system design.

3.2 ESD Design Recommendations

The ESD design recommendations are as follows:

- When designing the 24 MHz system clock, use the 4-pin surface mount device (SMD) crystal oscillator, and ensure that its two GND pins and the board GND are completely in contact to improve the anti-interference capability. Route other traces far away from the crystal oscillator area, that is, never route traces under the crystal oscillator.
- During the PCB component layout design, keep the circuits of the small system away from metal interfaces as far as possible to alleviate impacts exerted by ESD.
- Add ESD protective components for the peripheral interfaces (such as the audio/video input/output interfaces, USB port, Ethernet port, and alarm port) to improve their anti-interference capability.
- When the entire system is designed as a floating ground device, never use GND plane splits on the board.
  - Design only one digital GND on the board and never split the protective GND.
  - Use metal vias as the positioning holes of the board and connect them to the digital GND, and ensure that the board GND and the metal cover are completely in contact through the positioning holes.
- When the entire system is designed as a grounding device, connect the metal cover to the earth, and connect the protective GND splits to the board digital GND in single-point mode. Ensure that the single point is far away from the circuits of the small system and close to the power connector of the entire system.

- Use the metal cover for the interface connectors (such as the HDMI and USB port with positioning screws or the RJ45 connector with a tab), and ensure that the connectors and the metal cover of the entire system are completely in contact (using the conductive pillar or conductive gasket if necessary).
- Design the positioning holes of the board close to the backplane connectors and far away from the small system, and ensure that the board GND and the metal cover of the entire system are completely in contact.
- You are advised to use the full metal cover for the entire system. The design of a metal base cover and a plastic upper cover may cause a high ESD risk, because the space radiation is strong, and therefore a metal shielding cover is required.
- You are advised not to use the full plastic cover. If the full plastic cover design is used, you need to lower ESD test standards or take more measures to shield the space radiation (for example, installing a metal shielding cover on the back side of the small system).

You need to evaluate the preceding recommendations based on your standards and project experience.

3.2.1 USB Protective Circuit

A USB protective circuit is required to implement ESD protection. To protect signals along USB traces from being attenuated by protective components, design the PCB based on the following guidelines:

- Place protective components close to the USB port connector.
- Use the TVS tubes with low parasitic capacitors as protective components, and ensure that the breakdown voltage is 8 kV, and the breakdown time is less than 1 ns.
- Connect parasitic capacitors that are less than 1 pF to the protective components on the high-speed USB 2.0 port.

3.2.2 Protective Circuit of the VDAC Port

A protective circuit for the VDAC output port is required to implement ESD protection. You are advised to design the PCB based on the following guidelines:

- Use the video buffer circuit for video output to separate the video port of the Hi3516A from the add-on port.
- Place protective components close to the connector of the VDAC output port.
- Use TVS tubes or switch diodes as protective components.

3.3 Thermal Design Recommendations

3.3.1 Operating Conditions

For details about power consumption parameters, temperature parameters, and thermal resistance parameters for the Hi3516A, see section 2.7 "Electrical Specifications" in the *Hi3516A HD IP Camera SoC Data Sheet*.

3.3.2 Reference Thermal Design for Circuits

3.3.2.1 Principles

Power supply

Ensure that the efficiency of the board power tree is the highest as long as the power supplies are stable. That is, design the board power supplies optimally and use fewer LDO components with large voltage difference to reduce the heat produced during power conversion.

It is recommended that the core power supply implement the SVB function to reduce the power consumption and heat.

Low-Power Configurations for Idle Modules

Modules such as the DAC, SDXC, and VO may not be used in actual scenarios. You can set the modes of these modules to power-down mode or default mode.

3.3.2.2 PCB

Component Layout

Lay out components based on the following product architecture and heat dissipation design:

- Place the components that consume much power and generate much heat in a distributed manner to avoid overheating of some parts and ensure the reliability and efficiency of components. You are advised to place the Hi3516A far away from power supplies.
- The product architecture is optimally designed to ensure that the heat produced internally can be dissipated.

Trace Routing

The thermal design recommendations for routing traces are as follows:

- For the connection style of the vias under the Hi3516A, select the full connection style but not the thermal connection style to improve the board heat dissipation efficiency.
- The power and GND signals of the Hi3516A are connected over copper sheets. When the signal over-current capability is ensured, more vias are recommended on copper sheets.
- Increase the size of copper planes under and around the components that produce much heat to ensure that PCB heat can be effectively dissipated. Place inductors and power chips in a distributed manner and increase the size of copper planes around them.
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