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Hi3520D/Hi3515A/Hi3515C H.264 Codec Processor

user guide

Document version 02

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Part CodeN/A

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Notice

Due to product version upgrades or other reasons, the content of this document will be updated from time to time. Unless otherwise agreed, this document is only used as a guide, and all statements, information and suggestions in this document do not constitute any express or implied guarantee.

foreword

overview

This document introduces the characteristics and logical structure of the Hi3520D/Hi3515A/Hi3515C chip, describes in detail the functions, working methods, and definitions of related registers of each module, gives the timing relationship and related parameters of the interface in the form of a chart, and describes the chip in detail. Pin definition and usage, as well as chip performance parameters and package size.

product version

The product versions corresponding to this document are as follows.

product name	product version
Hi3520D	V100
Hi3515A	V100
Hi3515C	V100

Readers

This document is primarily intended for the following engineers:

Electronic product design and maintenance

personnel Electronic product component marketing and sales personnel

convention symbol convention

The following symbols may appear in this document, and their meanings are as follows.

symbol	illustrate
 危险	Text beginning with this symbol indicates a hazard with a high level of potential which, if not avoided, will result in death or serious injury.

symbol	illustrate
警告	Text beginning with this symbol indicates a hazard with a medium or low level of potential which, if not avoided, may result in minor or moderate injury.
注意	Text beginning with this symbol indicates potential hazards, which, if ignored, may result in equipment or component damage, data loss, reduced equipment performance, or unpredictable results.
窍门	Text beginning with this symbol can help you solve a problem or save you time.
说明	The text starting with this symbol is the additional information of the main text, and it is the emphasis and supplement to the main text.

General formatting conventions

Format	illustrate
Times New Roman	The text is expressed in Song font.
black body	Level 1, level 2, and level 3 headings are in bold.
italics	Warnings, prompts and other content are all in italics, and lines are added before and after the content to separate them from the main text.
"Terminal Display" format The "Terminal Display" format represents screen output information. In addition, the information input by the user from the terminal mixed with the screen output information is indicated in bold font.	

Form content agreement

content	illustrate
-	A contentless cell in a table.
*	The content in the table can be configured by the user as required.

Register Access Type Conventions

type description		type description	
RO is read-only, not writable.		W0C	Readable, write 0 to clear, write 1 to keep unchanged.
WO write only.		W1S can be read, write 1 to set, write 0 to keep unchanged.	

type description	type description		
RW can read and write.		W0S can be read, write 0 to set, write 1 to keep unchanged.	
RC reads to clear.		OR	Readable, after writing 1, the chip will be self-cleared, that is, a pulse will be generated.
W1C can be read, write 1 to clear, write 0 to keep unchanged.			

Numerical unit convention

The expressions of data capacity, frequency, data rate, etc. are explained below.

category	symbol	corresponding value
Data capacity (such as RAM capacity)	1K	1024
	1M	1,048,576
	1G	1,073,741,824
frequency, data rate, etc.	1 k	1000
	1M	1,000,000
	1G	1,000,000,000

The address and data expressions are described below.

symbol	example	illustrate
0x	0xFE04ÿ0x18	Data value and address value expressed in hexadecimal.
0b	0b000, 0b00 00000000 represent binary data values and binary sequences (except in register descriptions).	

revision history

A revision record accumulates descriptions of each documentation update. The latest version of the documentation contains updates from all previous versions of the documentation.

revision date version		Revision Notes
2013-06-21	02	Added the description of **Hi3515C .** Chapter **3** System 3.4.6 Register Description When PERIPHCTRL15 bit[11:0] is 10, the meaning is changed to Hi3515C. 3.8.2 Added the description of "RTC supports fixed frequency division mode". New registers sdm_coef_ouside_h and sdm_coef_ousside_l. Modify TEMP_SEL bit[2] to sdm_sel.
2013-05-22	01	Chapter **2** Hardware Supplement the power consumption parameters of Hi3520D and Hi3515A. Revised minimum and maximum values for some power supplies in Table 2-63 and Table 2-64. 2.8.3.2 The minimum value and maximum value of parameter Tov in MDIO interface timing sequence are changed to 0 and 300 respectively. Chapter **3** System 3.4.6 Added PERIPHCTRL15 in register description.
2013-04-03	00B04	Add the description of Hi3515A.
2013-03-31	00B03	The third version is released.
2013-02-07	00B02	The second version is released.
2013-01-15	00B01	Draft version.

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1 product description

说明

This document is applicable to Hi3520D and Hi3515A. Unless otherwise specified, Hi3520D is used as an example for description.

1.1 Application scenarios

Hi3520D/Hi3515A is a professional SOC chip developed for multi-channel D1 and multi-channel high-definition DVR, NVR product applications. Hi3520D/Hi3515A has a built-in high-performance A9 processor, an engine with up to 8-channel D1 (Hi3515A supports up to 4-channel D1) multi-protocol codec capability; it integrates excellent video engine and codec algorithm, combined with multi-channel high-definition display output capability, fully meets High-quality image experience for customer products. Hi3520D/Hi3515A is highly integrated and rich in peripheral interfaces, which greatly reduces the cost of ebom while meeting the requirements of customers' differentiated product functions, performance and image quality:

Single chip Hi3520D DVR solution

Single-chip Hi3515A DVR solution Single-chip

Hi3520D NVR solution Single-chip Hi3515A

NVR solution

1.1.1 Single-chip Hi3520D DVR solution

Hi3520D single chip 4D1+4CIF encoding+4D1 decoding DVR

ÿ 4D1+4CIF dual stream real-time encoding + JPEG D1 capture @8fps +4D1 real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3520D single chip 4x960H+4CIF encoding+1x960H solution DVR

ÿ 4x960H+4CIF real-time encoding+1x960H real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3520D single chip 8xCIF+8QCIF encoding+8xCIF decoding DVR ÿ 8xCIF+8QCIF

real-time encoding+JPEG D1 capture@16fps+8xCIF real-time decoding

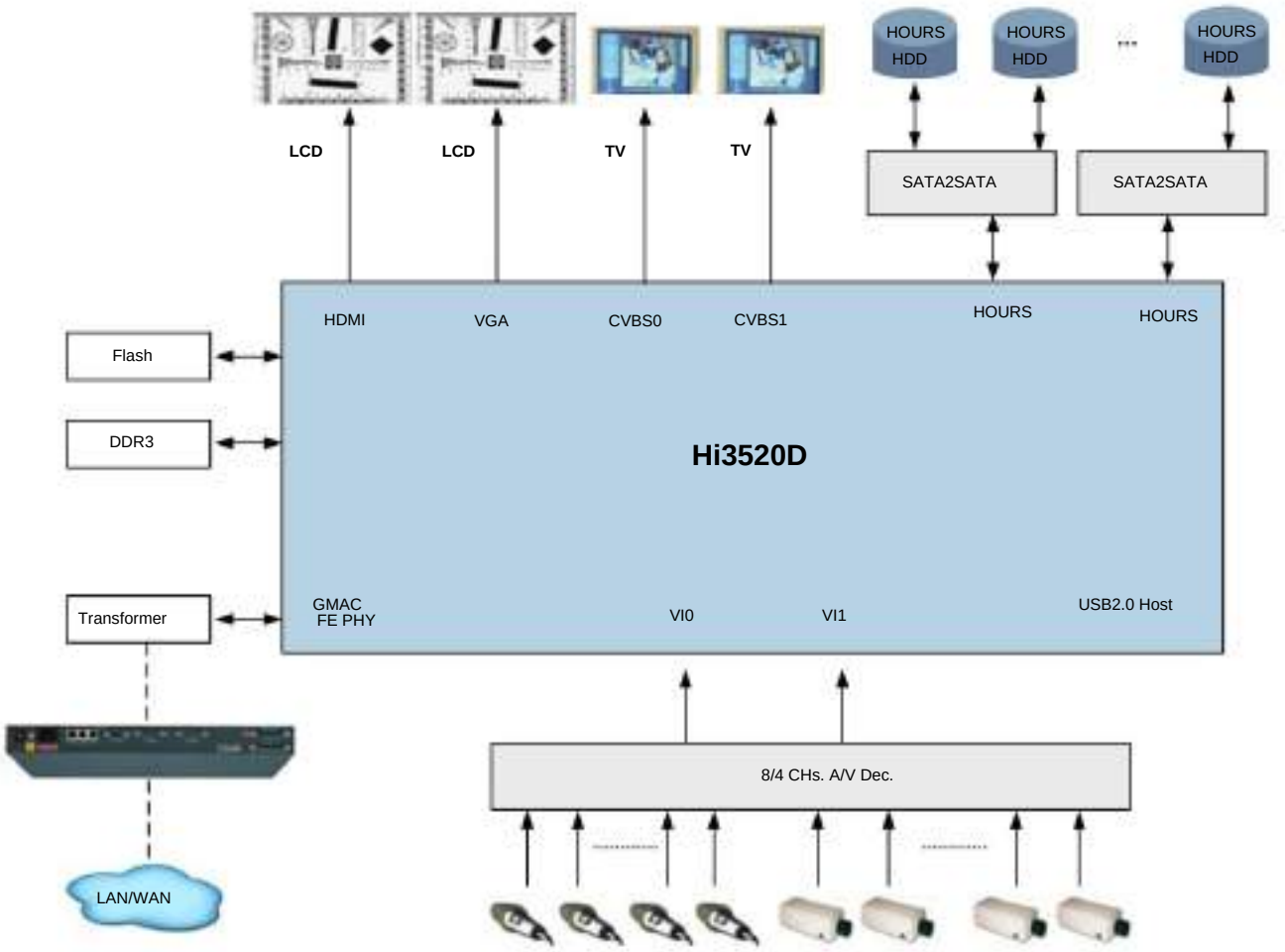
ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3520D single-chip 8D1 encoding+8CIF encoding+1D1 decoding (non-real-time)

ÿ 8D1@6fps + 8CIF@6fps dual stream encoding + 1D1@6fps decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-1 Hi3520D single-chip DVR application block diagram



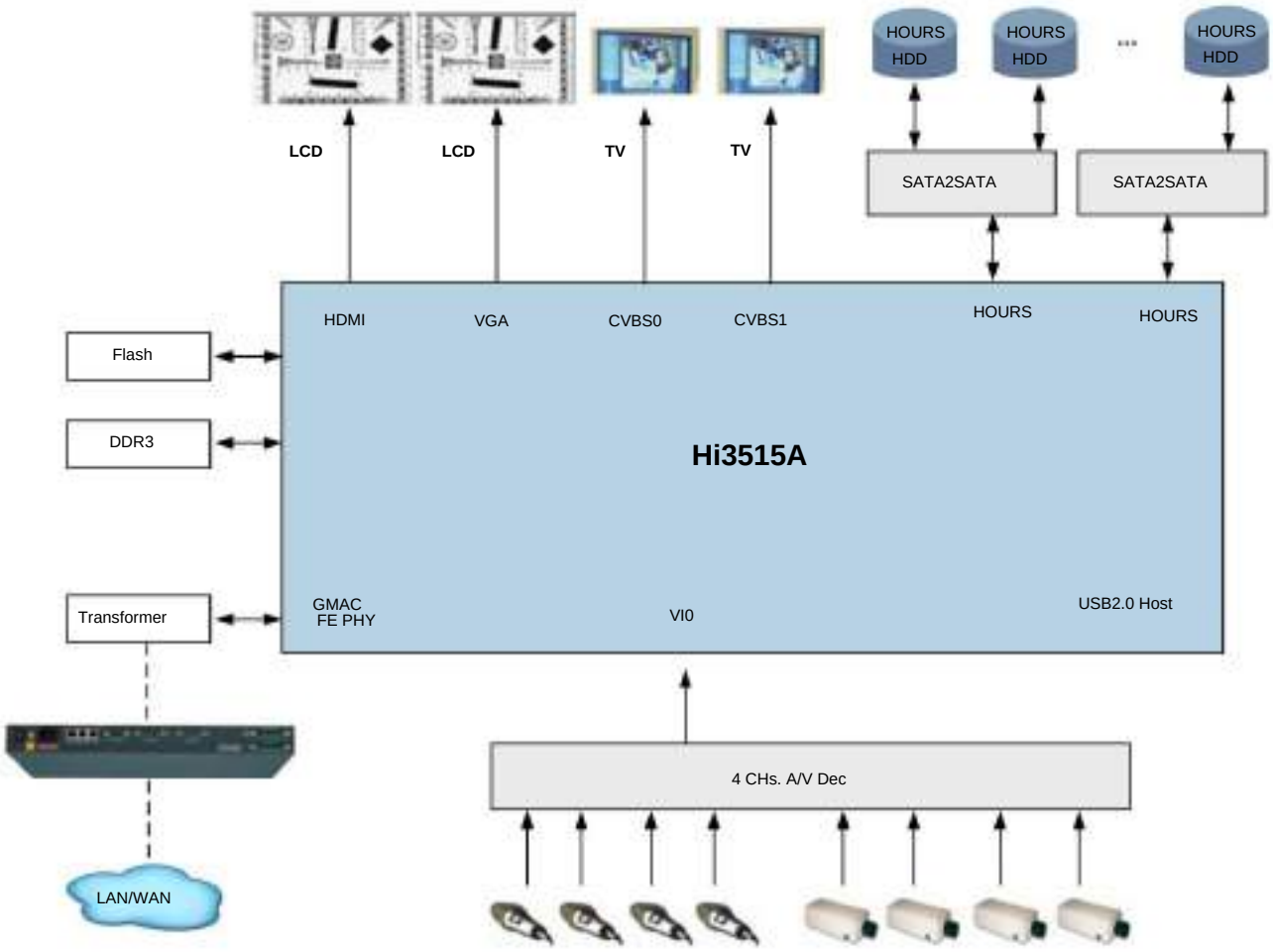
1.1.2 Single-chip Hi3515A DVR solution

Hi3515A single chip 4D1+4CIF encoding+1D1 decoding DVR

ÿ 4D1+4CIF dual stream real-time encoding + JPEG D1 capture @8fps +1D1 real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-2 Hi3515A single-chip DVR application block diagram



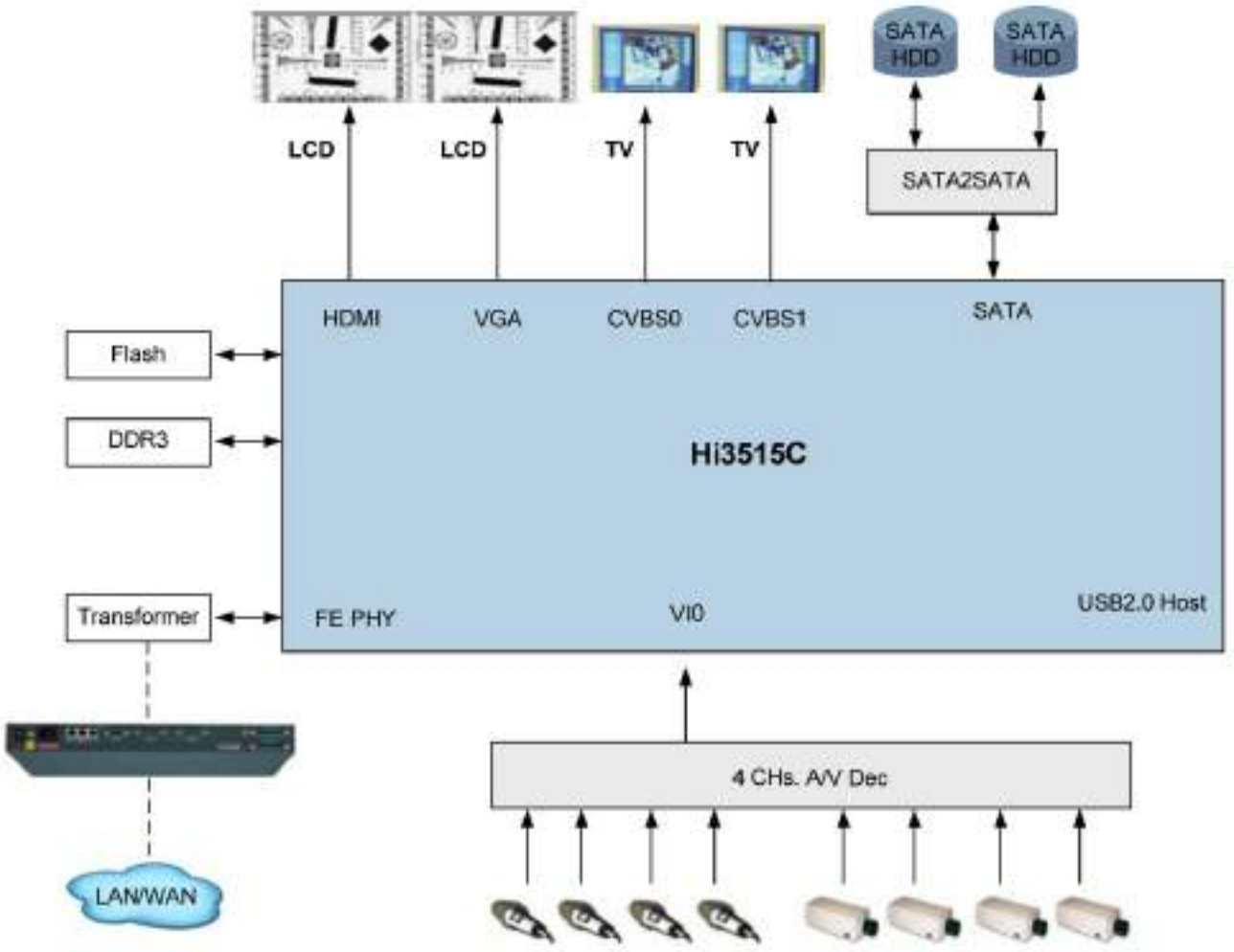
1.1.3 Single-chip Hi3515C DVR solution

Hi3515C single chip 4D1+4CIF encoding+1D1 decoding DVR

ÿ 4D1+4CIF dual stream real-time encoding + JPEG D1 capture @8fps +1D1 real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-3 Hi3515C single-chip DVR application block diagram



1.1.4 Single-chip Hi3520D NVR solution

Hi3520D single chip 8D1 NVR

ÿ 8D1 real-time decoding

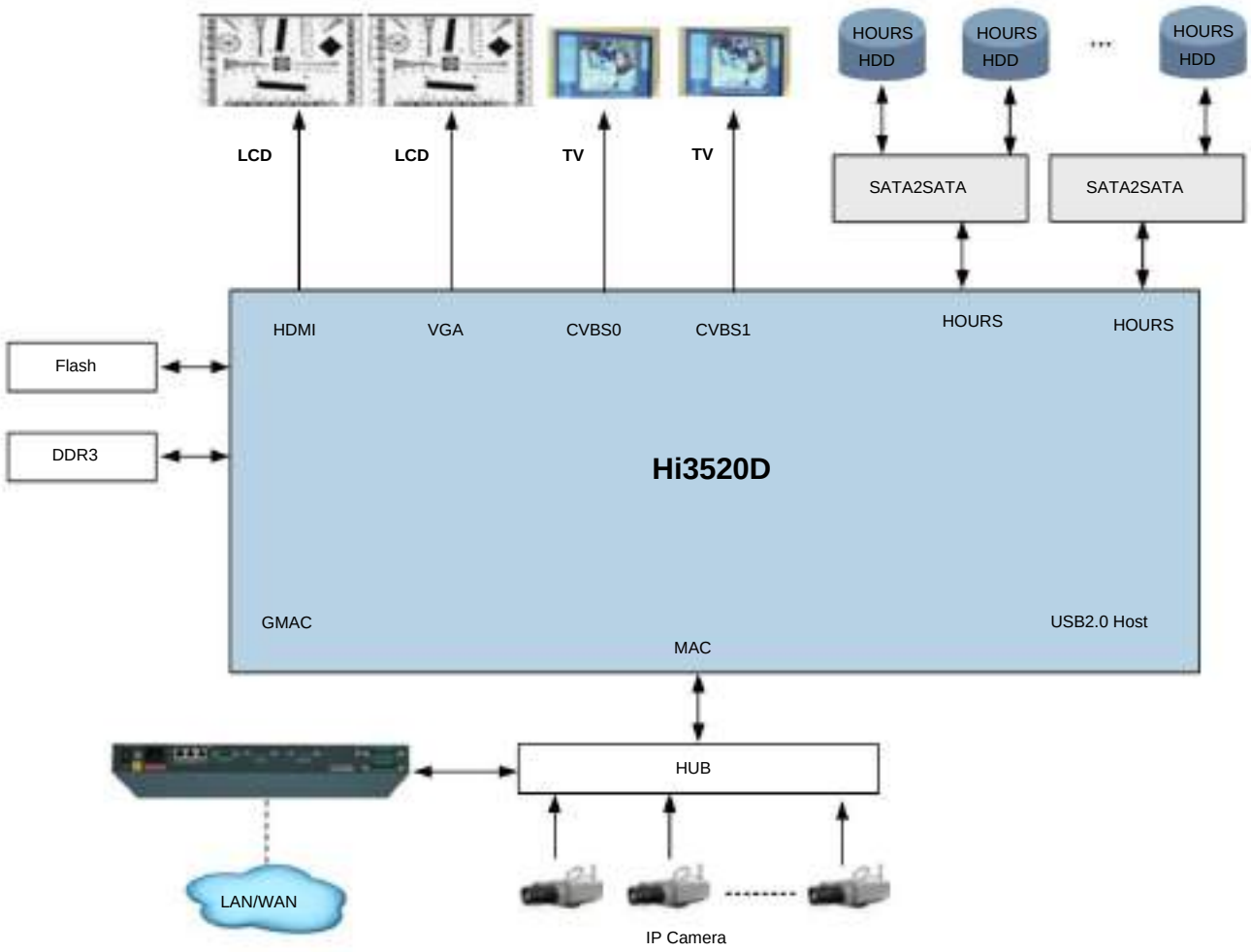
ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3520D single-chip 4x720p NVR ÿ 4-

channel 720p real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-4 Hi3520D NVR application block diagram



1.1.5 Single-chip Hi3515A NVR solution

Hi3515A Single Chip 4D1 NVR

ÿ 4D1 real-time decoding

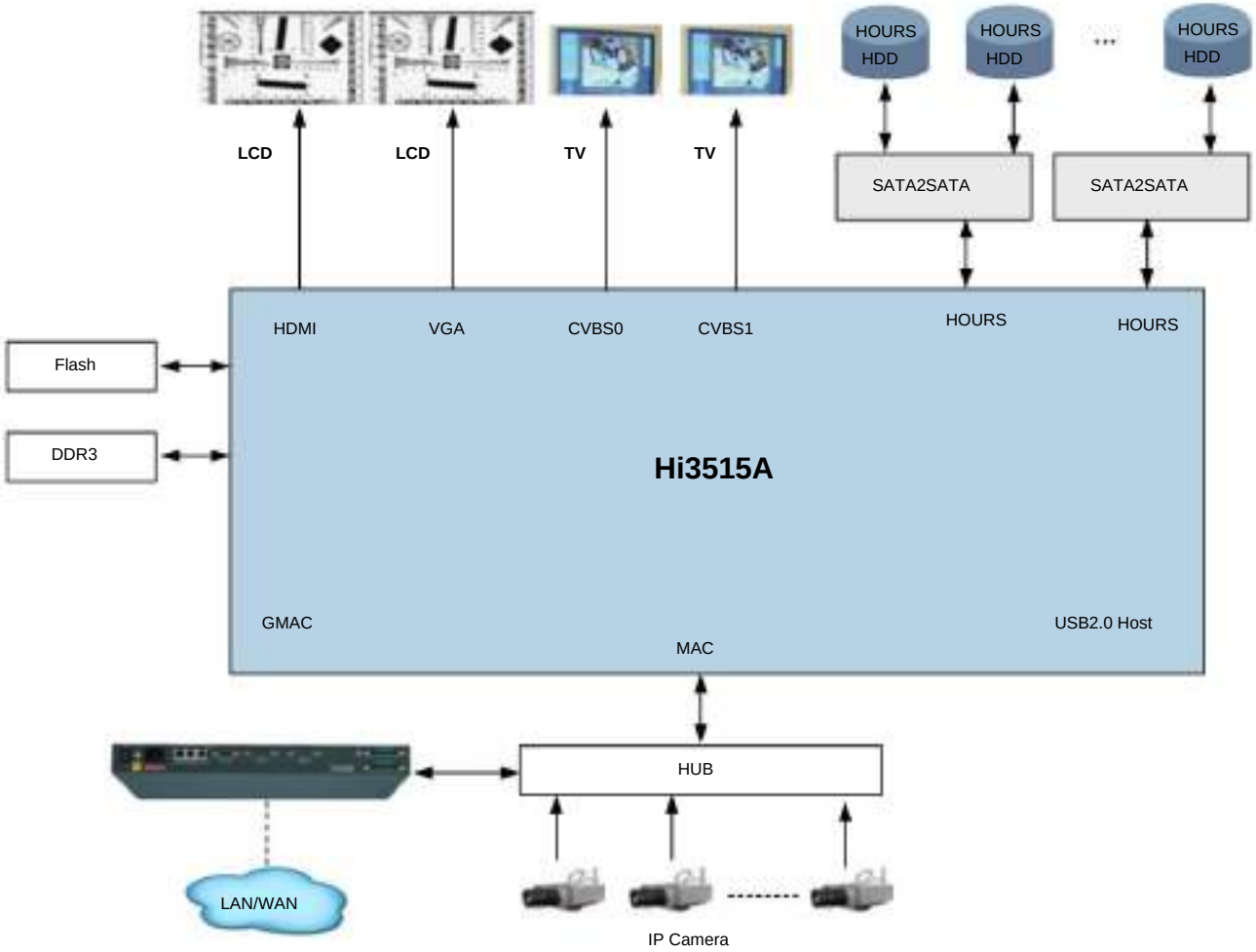
ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3515A single-chip 2x720p NVR ÿ 2-channel

720p real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-5 Hi3515A single-chip NVR application block diagram



1.1.6 Single-chip Hi3515C NVR solution

Hi3515C Single Chip 4D1 NVR

ÿ 4D1 real-time decoding

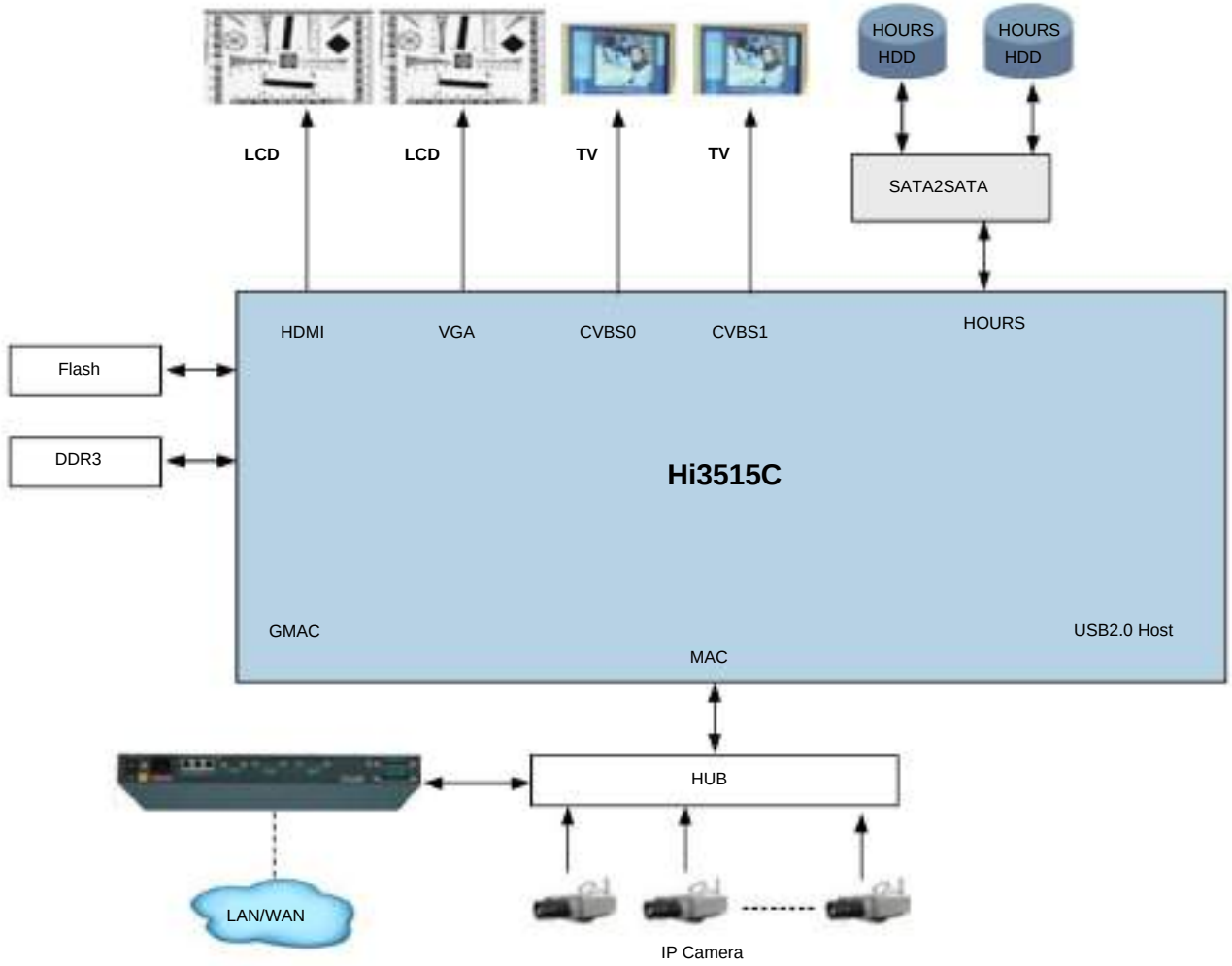
ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Hi3515C single-chip 2x720p NVR ÿ 2-channel

720p real-time decoding

ÿ HDMI+VGA 1080P@60fps homologous output + 2 channels of CVBS output

Figure 1-6 Hi3515C single-chip NVR application block diagram

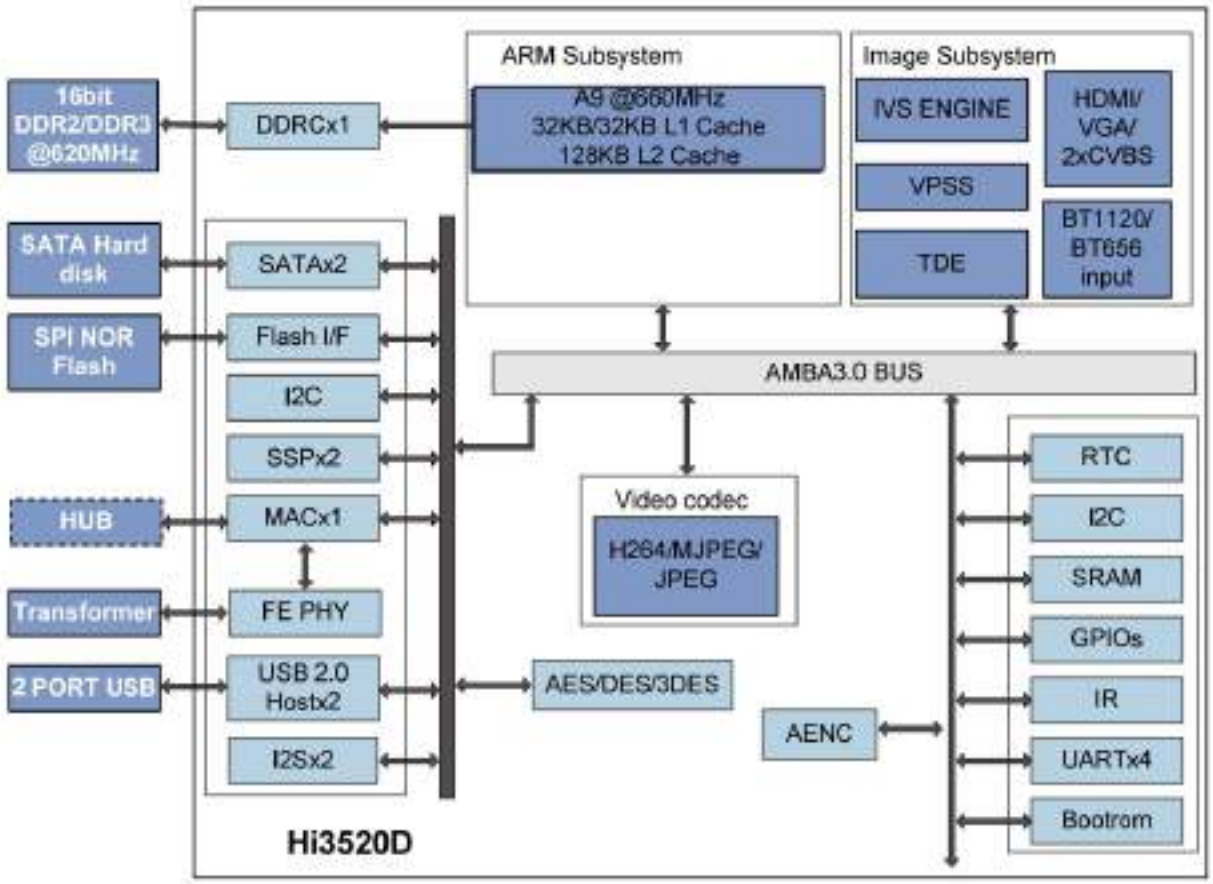


1.2 Architecture

1.2.1 Overview

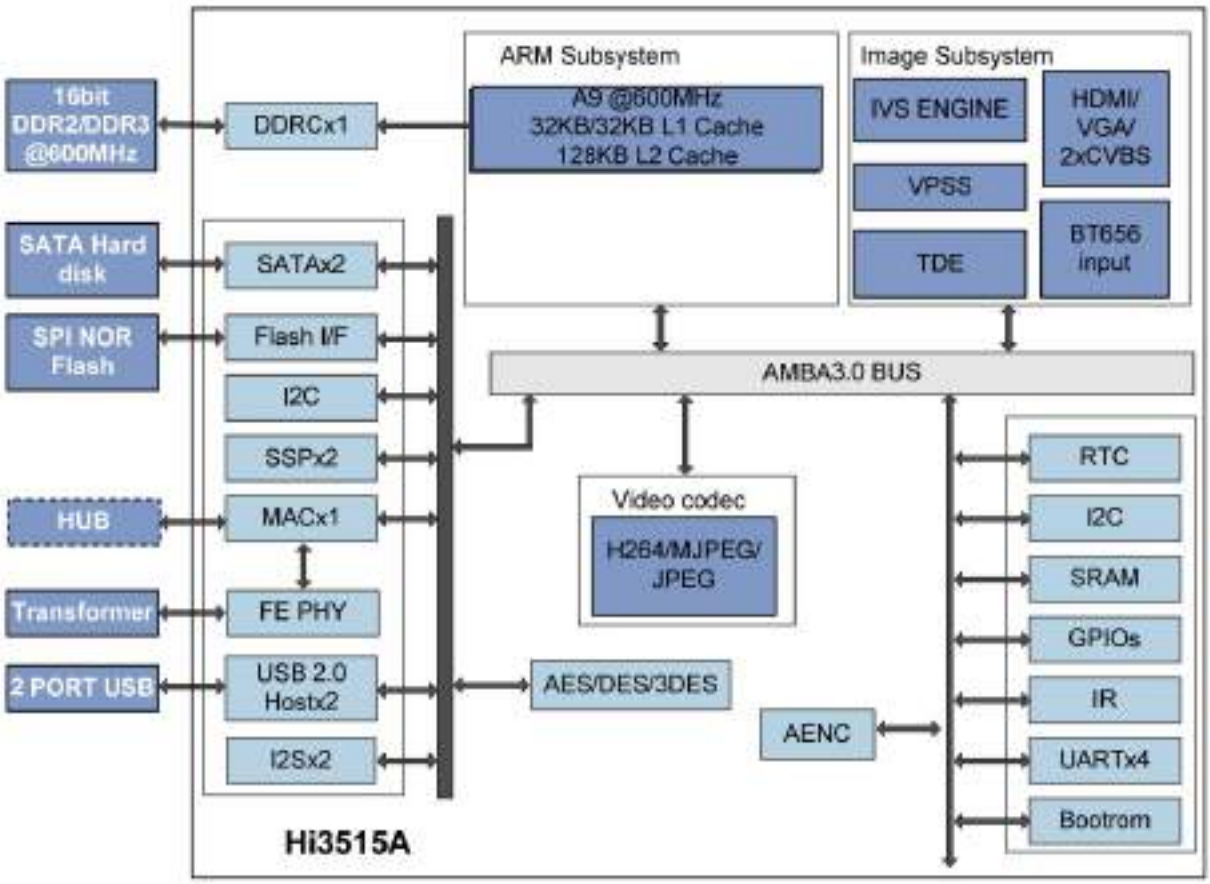
The logical block diagram of the Hi3520D chip is shown in Figure 1-3 .

Figure 1-7 Logic block diagram of Hi3520D chip



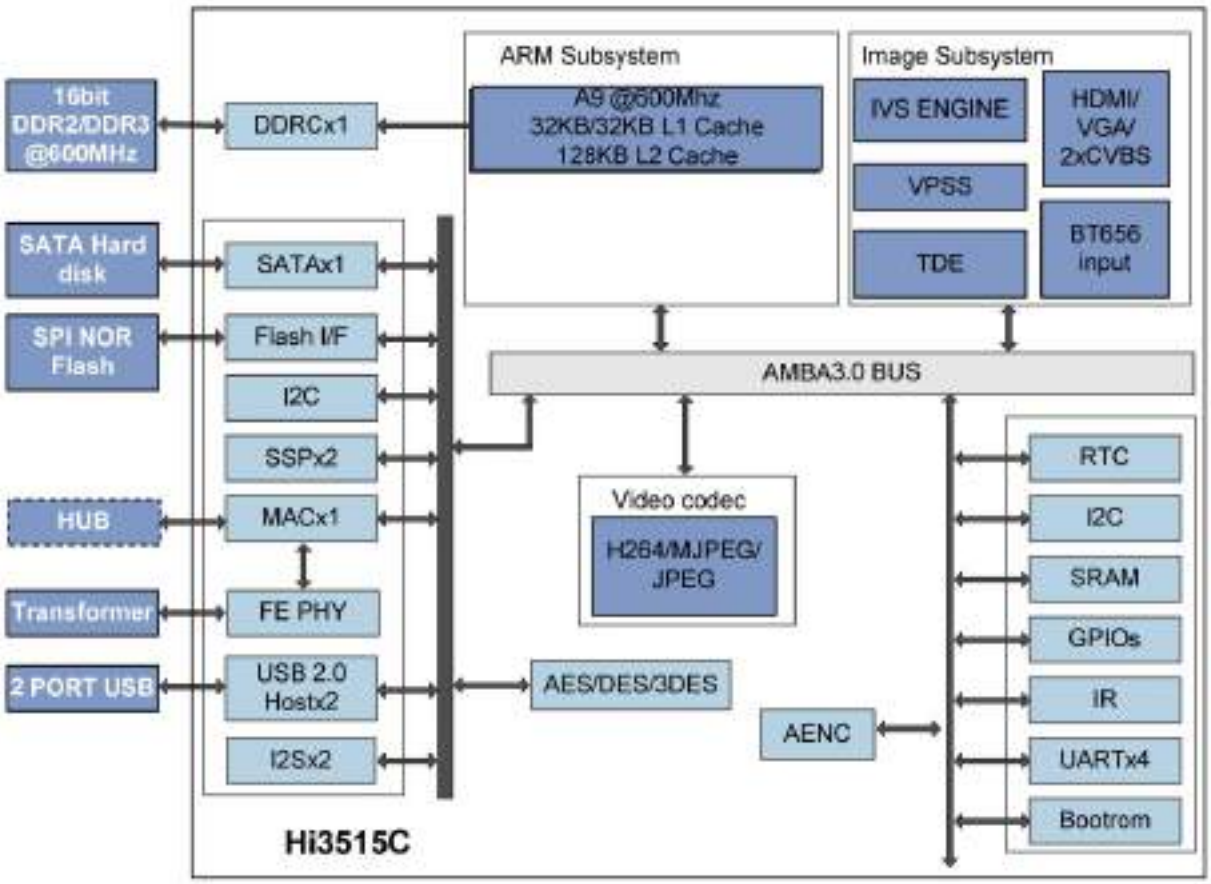
The logical block diagram of the Hi3515A chip is shown in Figure 1-6 .

Figure 1-8 Logic block diagram of Hi3515A chip



The logical block diagram of the Hi3515C chip is shown in Figure 1-9 .

Figure 1-9 Logic block diagram of Hi3515C chip



1.2.2 Processor Core

ARM Cortex A9 @Max. 660MHz (Hi3515A/Hi3515C frequency is 600MHz)

32KB L1 I-Cacheÿ32KB L1 D-Cache

128KB L2 Cache

1.2.3 Multi-protocol video codec

H.264 Baseline/Main/High Profile Level4.2 codec

MJPEG/JPEG Baseline codec

1.2.4 Video codec processing

Hi3520D: H.264&JPEG multi-stream encoding and

decoding performance ÿ 8xD1@6fps+8CIF@6fps encoding+8xD1@6fps decoding+JPEG

D1 capture@16fps ÿ 8xCIF@30fps+8QCIF@30fps encoding+8xCIF@30fps decoding+JPEG D1

capture@ 16fps ÿ 4xD1@30fps+4CIF@30fps encoding+4xD1@30fps decoding+JPEG

capture D1@8fps ÿ 4x960H@30fps+4CIF@30fps encoding+1x960H@30fps decoding+JPEG capture 960H@8fps

ÿ 8xD1@30fps H.264 decodingÿ

4x720P@30fps H.264 decodingÿ

2x1080P @30fps H.264 decoding

Hi3515A/Hi3515C: H.264&JPEG multi-stream encoding and decoding performance ÿ

4xD1@30fps+4CIF@30fps encoding+1xD1@30fps decoding+ JPEG capture D1@8fps ÿ 4xD1 @30fps H.264 decodingÿ 2x720P

@30fps H.264 decodingÿ 1x1080P@30fps

H.264 decoding

CBR/VBR code rate control, 16Kbit/sÿ40Mbit/s encoding frame rate

supports 1 fpsÿ60fps Support region of interest

(ROI) encoding Provide color to gray encoding

1.2.5 Intelligent Video Analysis

The integrated intelligent analysis acceleration engine supports various intelligent analysis applications such as intelligent motion detection, perimeter prevention, and video diagnosis.

1.2.6 Video and Graphics Processing

Support pre- and post-processing such as de-interlace, image enhancement, edge enhancement, 3D denoising,

etc. Support video and graphic output anti-flicker

processing Support video 1/8~16x zoom

Support graphics 1/2~2x zoom Support

8 areas before encoding Handle OSD overlay video layer, graphics

layer Alpha overlay

1.2.7 Audio Codec

Hardware implements multi-protocol audio encoding, supports ADPCM, G.711, G.726 software

implements multi-protocol audio encoding and decoding

1.2.8 Security Engine

Hardware implementation of AES/DES/3DES encryption and decryption algorithms

1.2.9 Video interface

Hi3520D: Video input interface ÿ

2xBT656@108/144MHz, support 8CIF/8D1/8 x 960H real-time video input ÿ 2xBT656@148.5MHz, support 2x720P real-

time video input ÿ 1xBT1120@148.5MHz, support 1x1080p real-time video input Hi3515A/

Hi3515C: video input interface

ÿ 1xBT656@108/144MHz, support 4CIF/4D1/4 x 960H real-time video input ÿ 1xBT656@148.5MHz, support 1x720P real-time video input Video output interface

ÿSupport HDMI 1.3+VGA +2xCVBS multi-video output; HDMI and VGA homologous output

ÿ The highest resolution of HDMI/VGA supports 1080P@60fps .

1920x1080

ÿProvide a layer of hardware mouse layer, the format is RGB1555, RGB8888 can be configured, the maximum resolution is 128x128

ÿ Multiplexing of CVBS0 and HD video PIP layer

1.2.10 Audio interface

2 Standard I ^{2}S interface

1 support input 1

support input output

1.2.11 Network interface

1 Ethernet port

Built-in FE PHY

Can choose to use the MDI interface of the physical layer or the RMII interface of the MAC layer

Support 10/100Mbit/s

Support full-duplex or half-duplex mode

1.2.12 Peripheral Interface

2 SATA2.5 ports (Hi3515C only has 1 SATA 2.5 port)

ÿSupport PM function

ÿSupport eSATA 4

UART interfaces

1 SPI interface, support 2 chip selects

IR interface, I ^{2}C interface, GPIO interface

2 USB 2.0 HOST ports, support Hub function

1.2.13 Memory Interface

1 16bit DDR2/3 SDRAM controller interface

ÿMaximum frequency 660MHz (Hi3515C maximum frequency 600MHz)

ÿSupport ODT function

ÿThe maximum capacity supports 512MB

ÿSupport automatic power consumption control

SPI Nor Flash interface

ÿ 1ÿ2ÿ4bit SPI Nor Flash

ÿ 2 chip selects

ÿThe maximum capacity of each chip selection supports 8Gbit

Built-in 4KB bootrom and 10KB SRAM

1.2.14 RTC powered independently

RTC can be independently powered by battery

The built-in temperature sensor can

automatically correct the RTC counting frequency according to the temperature

1.2.15 Multiple startup modes can be configured

bootrom start

SPI NOR flash boot

1.2.16 SDK

Provide a development kit based on Linux 3.0

Provide a high-performance PC decoding library for H.264

1.2.17 Chip physical specifications

Power

consumption ÿ 2.5W typical power

consumption ÿ supports multi-level power consumption control

Operating Voltage

ÿ Core voltage is 1.25V ÿ IO voltage

is 3.3V

ÿ DDR2/3 SDRAM interface voltage is 1.8/1.5V

encapsulation

ÿ RoHS, Epad-LQFP256 ÿPin spacing:

0.4mm ÿ 28mmx28mm package size

1.3 Start mode

The following two startup methods are supported:

Boot from bootrom storage

Boot from off-chip SPI Flash memory space

1.3.1 Start from bootrom

When booting from the on-chip bootrom, the boot medium is the on-chip ROM. At this time, it is necessary to set the pull-down level of BOOT_SEL (multiplexed with the external pin AIO_MCLK of the chip) to select whether to boot from the BOOTROM;

When BOOT_SEL=1, the chip starts from the on-chip ROM;

When the chip starts from the on-chip ROM, it will start the serial communication mechanism, establish communication with the corresponding software on the PC through the serial port, and complete the startup after downloading the boot program (please refer to "Fastboot Tool Instructions");
at the same time, if the BOOTROM starts with The serial communication timeout does not respond, and it will start from SPI FLASH.

1.3.2 Boot from SPI Flash

When booting directly from SPI Flash (not jumping from BOOTROM as mentioned above), the externally connected memory is SPI Flash. At this time, it is necessary to set the pull-up and pull-down level of BOOT_SEL (multiplexed with the external pin AIO_MCLK of the chip) to select the Boot memory. .

When BOOT_SEL=0, the chip supports booting from the SPI Flash connected to the SFC interface.

1.3.3 Address Space Mapping

Address space mapping is shown in Table 1-1 .

Table 1-1 Address space mapping table

start address end address function		size description	
0xC000_0000 0xFFFF_FFFF reserved		1GB	
0x8000_0000 0xBFFF_FFFF DDR External DDR device address is empty between		1GB	
0x5C00_0000 0x7FFF_FFFF Reserved		576MB -	
0x5800_0000 0x5BFF_FFFF SPI FLASH storage space		64MB -	
0x5400_0000 0x57FF_FFFF reserved		64MB -	
0x5000_0000 0x53FF_FFFF reserved		64MB -	
0x4000_0000 0x4FFF_FFFF Reserved		256MB -	
0x3000_0000 0x3FFF_FFFF Reserved		256MB -	
0x2082_0000 0x2FFF_FFFF Reserved		248MB -	
0x2081_0000 0x2081_FFFF reserved		64KB	-
0x2080_0000 0x2080_FFFF reserved		64KB	-
0x2070_0000 0x207F_FFFF L2 CACHE space		1MB	
0x206E_0000 0x206F_FFFF reserved		128KB -	
0x206D_0000 0x206D_FFFF DDR test module		64KB	-

start address end address function	size description
0x206C_0000 0x206C_FFFF MD register	64KB
0x206B_0000 0x206B_FFFF VCMP register	64KB
0x2068_0000 0x206A_FFFF reserved	192KB -
0x2067_0000 0x2067_FFFF JPGD Register	64KB
0x2066_0000 0x2066_FFFF JPGE Register	64KB
0x2065_0000 0x2065_FFFF AIO Register	64KB
0x2064_0000 0x2064_FFFF VOIE Register	64KB
0x2063_0000 0x2063_FFFF reserved	64KB
0x2062_0000 0x2062_FFFF VEDU register	64KB
0x2061_0000 0x2061_FFFF TDE Register	64KB
0x2060_0000 0x2060_FFFF VPSS Register	64KB
0x205F_0000 0x205F_FFFF reserved	64KB
0x205E_0000 0x205E_FFFF IVE register	64KB
0x205D_0000 0x205D_FFFF reserved	64KB
0x205C_0000 0x205C_FFFF VDP Register	64KB
0x2058_0000 0x205B_FFFF VICAP register	256KB -
0x2052_0000 0x2057_FFFF reserved	384KB -
0x2040_0000 0x2051_FFFF ARM DEBUG	1152KB -
0x2031_0000 0x203F_FFFF reserved	896KB -
0x2030_0000 0x2030_FFFF ARM wdg/timer/gic and other internal registers memory	64KB
0x2020_0000 0x202F_FFFF reserved	1024KB -
0x201F_0000 0x201F_FFFF HDMI register	64KB
0x201E_0000 0x201E_FFFF reserved	64KB
0x201D_0000 0x201D_FFFF GPIO8 register	64KB
0x201C_0000 0x201C_FFFF GPIO7 Register	64KB
0x201B_0000 0x201B_FFFF GPIO6 register	64KB
0x201A_0000 0x201A_FFFF GPIO5 register	64KB
0x2019_0000 0x2019_FFFF GPIO4 Register	64KB -

start address end address function	size description
0x2018_0000 0x2018_FFFF GPIO3 register	64KB
0x2017_0000 0x2017_FFFF GPIO2 Register	64KB
0x2016_0000 0x2016_FFFF GPIO1 Register	64KB
0x2015_0000 0x2015_FFFF GPIO0 register	64KB
0x2014_0000 0x2014_FFFF TIMER3 Register	64KB
0x2013_0000 0x2013_FFFF TIMER2 Register	64KB
0x2012_0000 0x2012_FFFF PWM Register	64KB
0x2011_0000 0x2011_FFFF DDRC register	64KB
0x2010_0000 0x2010_FFFF reserved	64KB
0x200F_0000 0x200F_FFFF IO config register	64KB
0x200E_0000 0x200E_FFFF Reserved	64KB
0x200D_0000 0x200D_FFFF I2C Register	64KB
0x200C_0000 0x200C_FFFF SPI Register	64KB
0x200B_0000 0x200B_FFFF UART3 register	64KB
0x200A_0000 0x200A_FFFF UART2 Register	64KB
0x2009_0000 0x2009_FFFF UART1 Register	64KB
0x2008_0000 0x2008_FFFF UART0 register	64KB
0x2007_0000 0x2007_FFFF IR Register	64KB
0x2006_0000 0x2006_FFFF RTC register	64KB
0x2005_0000 0x2005_FFFF SYS_CTRL register	64KB
0x2004_0000 0x2004_FFFF WDG register	64KB
0x2003_0000 0x2003_FFFF CRG register	64KB
0x2002_0000 0x2002_FFFF reserved	64KB
0x2001_0000 0x2001_FFFF Timer1 Register	64KB
0x2000_0000 0x2000_FFFF Timer0 Register	64KB
0x101E_0000 0x1FFF_FFFF Reserved	256MB -
0x1016_0000 0x101D_FFFF reserved	512KB -
0x1015_0000 0x1015_FFFF reserved	64KB
0x100D_0000 0x1014_FFFF reserved	512KB -

start address end address function			size description	
0x100C_0000	0x100C_FFFF	CIPHER Register	64KB	
0x100B_0000	0x100B_FFFF	USB EHCI Register	64KB	
0x100A_0000	0x100A_FFFF	USB OHCI Register	64KB	
0x1009_0000	0x1009_FFFF	ETH Register	64KB	
0x1008_0000	0x1008_FFFF	SATA Register	64KB	
0x1002_0000	0x1007_FFFF	reserved	384KB -	
0x1001_0000	0x1001_FFFF	SPI NOR FLASH register 64KB		
0x1000_0000	0x1000_FFFF	reserved	64KB	
0x0402_0000	0x0FFF_FFFF	Reserved	192MB -	
0x0401_0000	0x0401_FFFF	On-chip RAM address space	The actual size of 64KB is only 10KB.	
0x0400_0000	0x0400_FFFF	BOOTROM address space	64KB The actual size is only 4KB.	
0x0000_0000	0x03FF_FFFF	When the address is remapped: this address points to the boot address space. After address remapping is cancelled: this address space points to Hi3520D on-chip RAM	When the 64MB address is remapped, the system boot address space points to different storage spaces according to different boot modes: 1. When the boot mode is boot from BOOTROM, the system boot address space is the storage space of the on-chip BOOTROM. 2. When the boot mode is slave SPI When FLASH starts, the system start address space is SPI FLASH storage space. For the description of the startup mode, please refer to chapter 1.3 "Startup Mode".	

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2 hardware features

2.1 Package and Pin Distribution

2.1.1 Packaging

The Hi3520D chip is packaged in Epad-LQFP256, the package size is 28mmX28mm, the pin pitch is 0.4mm, the total number of pins is 256, and the Epad size is 7.70mmX7.70mm. Please refer to Figure 2-1 to Figure 2-4 for detailed packaging, and Figure 2-5 for package size parameters.

Figure 2-1 Top view of chip package

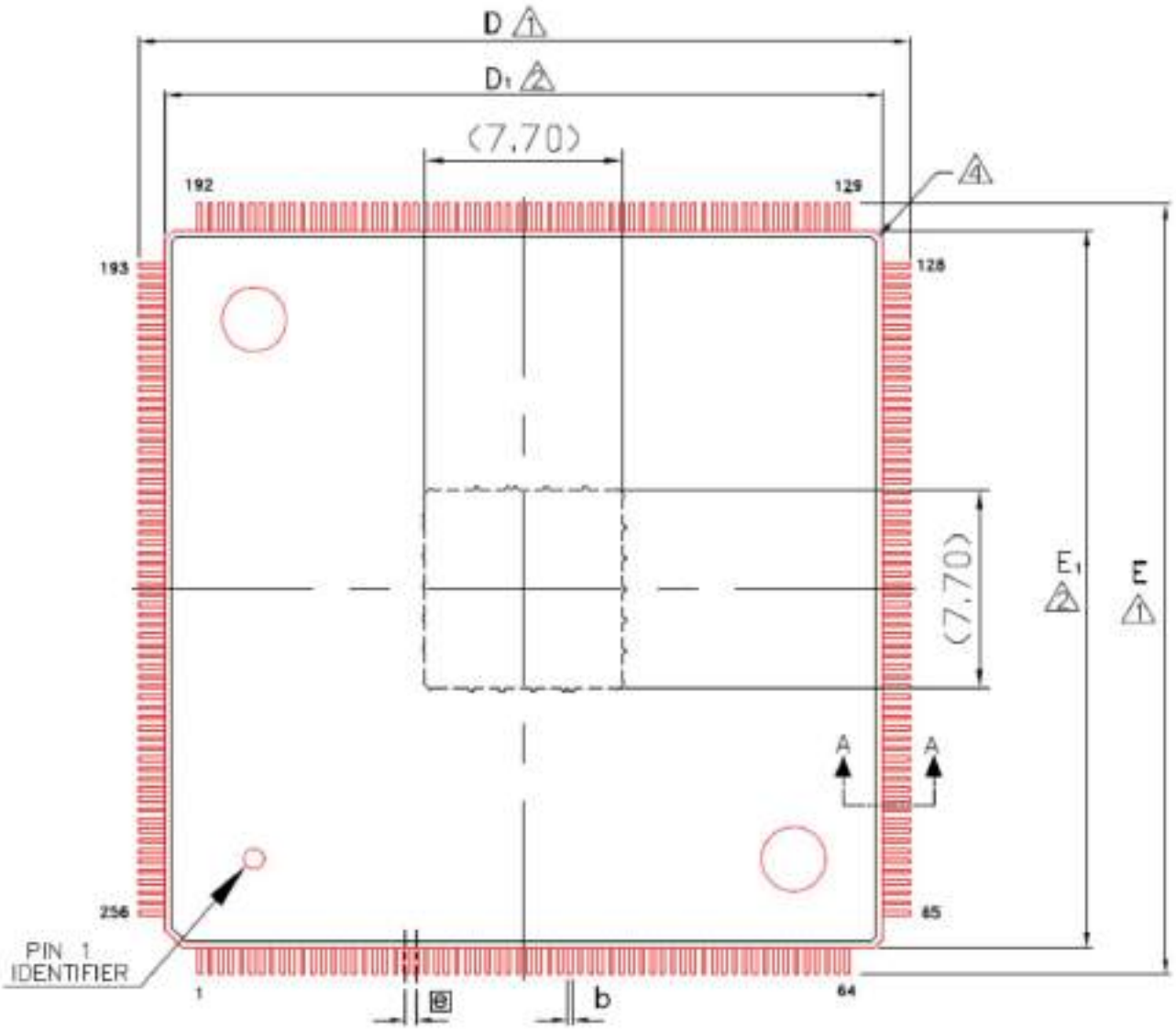


Figure 2-2 Side view of chip package

Figure 2-3 Enlarged view of Detail B

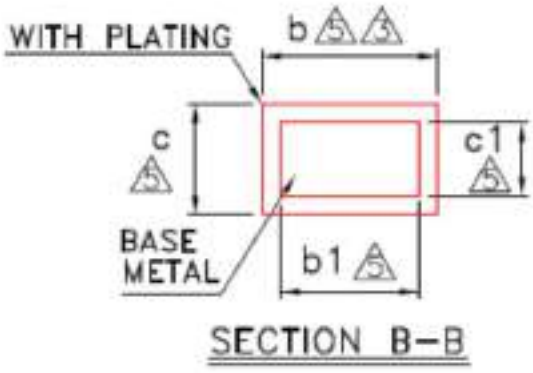


Figure 2-4 Enlarged view of Detail A

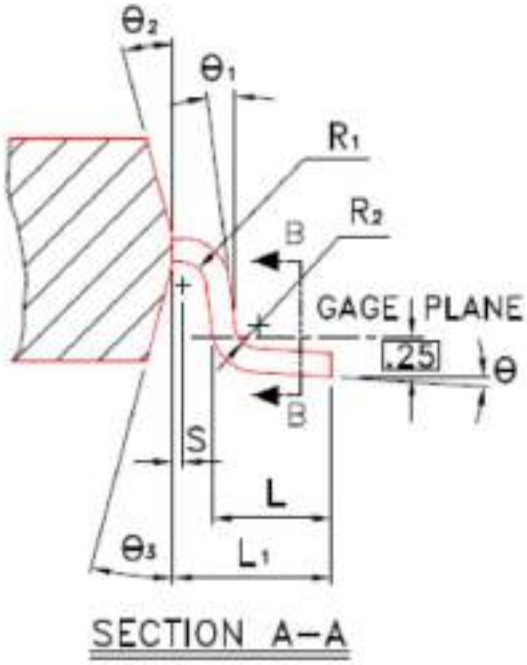


Figure 2-5 Package parameter description

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.127	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D_1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E_1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	7° REF			7° REF		
θ_2	12° REF			12° REF		
θ_3	12° REF			12° REF		
ccc	0.08			0.003		

2.1.2 Pin distribution

Pin layout

Hi3520D pin distribution is shown in Figure 2-6 and Figure 2-7 .

Figure 2-6 Pin layout part1

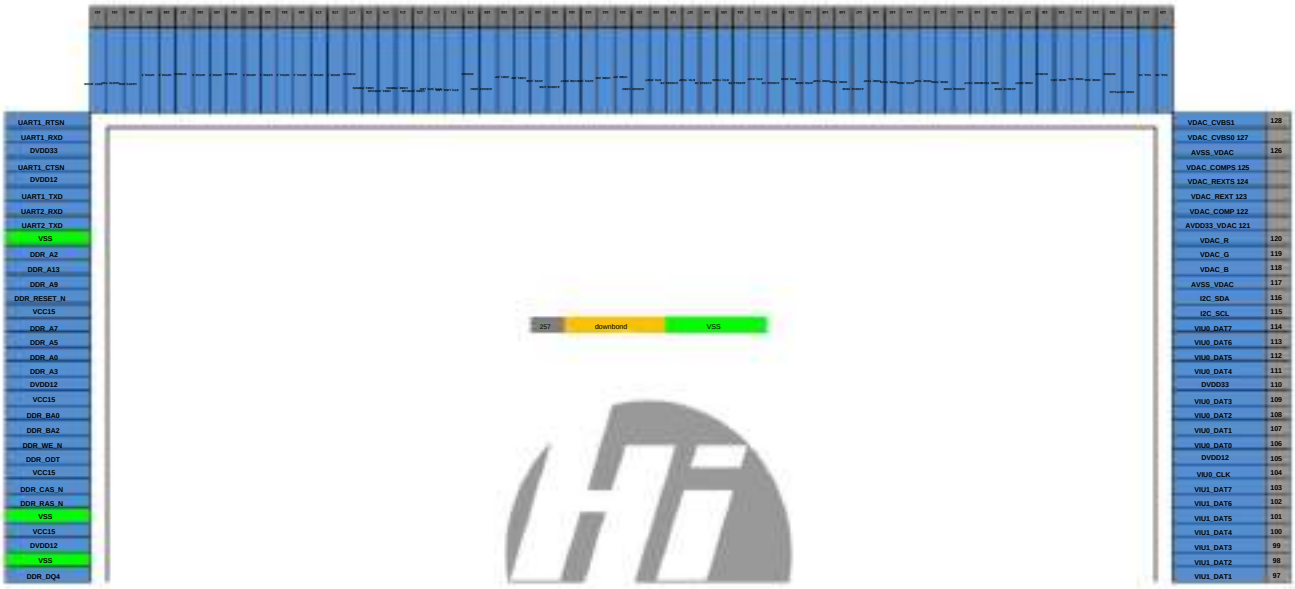
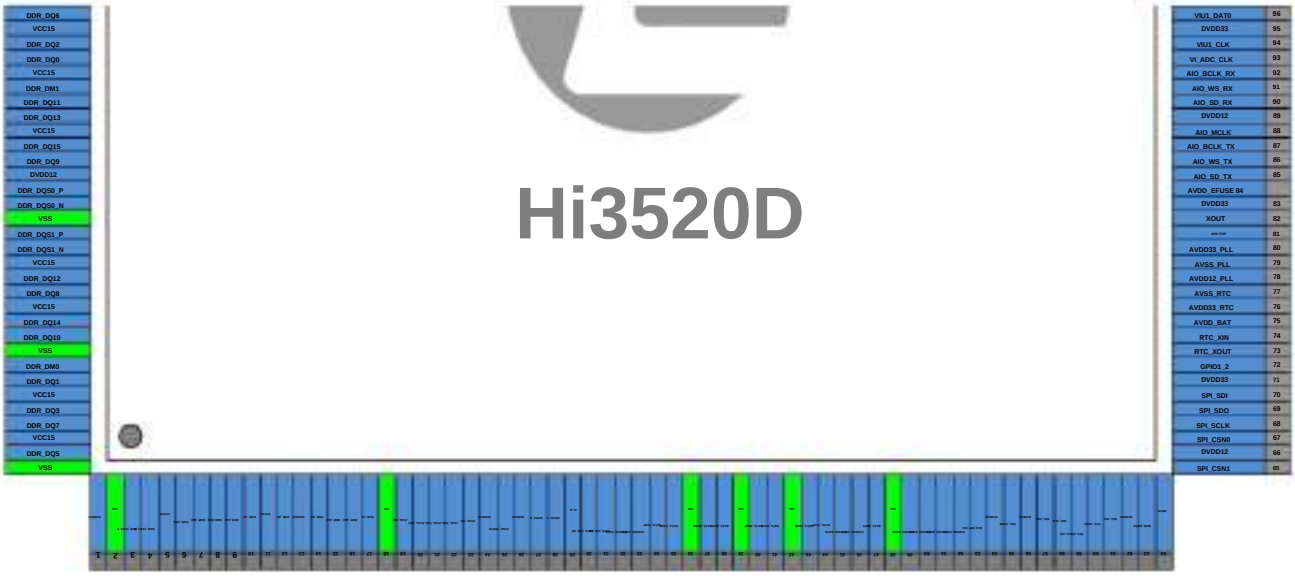


Figure 2-7 Pin layout part2



Pin arrangement table

The pins of the Hi3520D are arranged by position as shown in Table 2-1 .

Table 2-1 Pin arrangement table

Location	Pin name	Location	Pin name
1	DVDD12	129	VGA_HS

Location	Pin name	Location	Pin name
2	VSS	130	VGA_VS
3	DDR_CLK1_P	131	HDMI_HOTPLUG
4	DDR_CLK1_N	132	DVDD33
5	VCC15	133	HDMI_SDA
6	DDR_CKE	134	HDMI_SCL
7	DDR_A10	135	HDMI_CEC
8	DDR_BA1	136	DVDD12
9	DDR_A12	137	HDMI_REXT
10	DDR_A4	138	AVDD12_HDMI
11	VCC15	139	HDMI_TXCN
12	DDR_A6	140	HDMI_TXCP
13	DVDD12	141	AVDD12_HDMI
14	DDR_A8	142	HDMI_TX0N
15	DDR_A11	143	HDMI_TX0P
16	DDR_A14	144	AVSS_HDMI
17	DDR_A1	145	HDMI_TX1N
18	VSS	146	HDMI_TX1P
19	JTAG_EN	147	AVDD12_HDMI
20	JTAG_TDO	148	HDMI_TX2N
21	JTAG_TCK	149	HDMI_TX2P
22	JTAG_TMS	150	AVSS_HDMI
23	JTAG_TDI	151	ETH_RXIN
24	DVDD33	152	AVDD12_FE
25	JTAG_TRSTN	153	ETH_RXIP
26	DVDD12	154	AVSS12_FE
27	GPIO1_0	155	ETH_TXON
28	GPIO1_1	156	AVSS33_FE
29	IR_IN	157	ETH_TXOP
30	SATA_LED_N0	158	AVDD33_FE
31	SATA_LED_N1	159	ETH_RSET
32	AVDD12_SATA	160	AVDD33_USB0

Location	Pin name	Location	Pin name
33	AVDD33_SATA	161	USB0_DP
34	SATA_TX0P	162	USB0_DM
35	SATA_TX0M	163	AVSS_USB
36	VSS	164	USB_REXT
37	SATA_RX0M	165	AVDD33_USB
38	SATA_RX0P	166	AVSS_USB
39	VSS	167	USB1_DM
40	SATA_RX1P	168	USB1_DP
41	SATA_RX1M	169	AVDD33_USB1
42	VSS	170	DVDD12
43	SATA_TX1M	171	ETH_LED1
44	SATA_TX1P	172	ETH_LED0
45	AVDD33_SATA	173	USB0_OVRCUR
46	AVDD12_SATA	174	USB0_PWREN
47	SATA_REXT	175	USB1_OVRCUR
48	VSS	176	USB1_PWREN
49	AVDD33_SATA	177	DVDD33
50	AVDD12_SATA	178	GPIO0_7
51	AVDD12_SATA	179	GPIO0_4
52	AVDD33_SATA	180	GPIO1_4
53	SFC_WP_IO2	181	GPIO1_3
54	DVDD33	182	GPIO0_1
55	SFC_CS0N	183	GPIO0_3
56	DVDD12	184	DVDD12
57	SFC_DIO	185	GPIO0_2
58	SFC_CLK	186	GPIO0_0
59	SFC_HOLD_IO3	187	DVDD33
60	SFC_CS1N	188	GPIO0_6
61	SFC_DOI	189	GPIO0_5
62	DVDD33	190	UART0_RXD
63	WDG_RSTN	191	UART0_TXD

Location	Pin name	Location	Pin name
64	RSTN	192	TEST_MODE
65	SPI_CSN1	193	UART1_RTSN
66	DVDD12	194	UART1_RXD
67	SPI_CSN0	195	DVDD33
68	SPI_SCLK	196	UART1_CTSN
69	SPI_SDO	197	DVDD12
70	SPI_SDI	198	UART1_TXD
71	DVDD33	199	UART2_RXD
72	GPIO1_2	200	UART2_TXD
73	RTC_XOUT	201	VSS
74	RTC_XIN	202	DDR_A2
75	AVDD_BAT	203	DDR_A13
76	AVDD33_RTC	204	DDR_A9
77	AVSS_RTC	205	DDR_RESET_N
78	AVDD12_PLL	206	VCC15
79	AVSS_PLL	207	DDR_A7
80	AVDD33_PLL	208	DDR_A5
81	ASK FOR	209	DDR_A0
82	XOUT	210	DDR_A3
83	DVDD33	211	DVDD12
84	AVDD_EFUSE	212	VCC15
85	AIO_SD_TX	213	DDR_BA0
86	AIO_WS_TX	214	DDR_BA2
87	AIO_BCLK_TX	215	DDR_WE_N
88	AIO_MCLK	216	DDR_ODT
89	DVDD12	217	VCC15
90	AIO_SD_RX	218	DDR_CAS_N
91	AIO_WS_RX	219	DDR_RAS_N
92	AIO_BCLK_RX	220	VSS
93	VI_ADC_CLK	221	VCC15
94	VIU1_CLK	222	DVDD12

Location	Pin name	Location	Pin name
95	DVDD33	223	VSS
96	VIU1_DAT0	224	DDR_DQ4
97	VIU1_DAT1	225	DDR_DQ6
98	VIU1_DAT2	226	VCC15
99	VIU1_DAT3	227	DDR_DQ2
100	VIU1_DAT4	228	DDR_DQ0
101	VIU1_DAT5	229	VCC15
102	VIU1_DAT6	230	DDR_DM1
103	VIU1_DAT7	231	DDR_DQ11
104	VIU0_CLK	232	DDR_DQ13
105	DVDD12	233	VCC15
106	VIU0_DAT0	234	DDR_DQ15
107	VIU0_DAT1	235	DDR_DQ9
108	VIU0_DAT2	236	DVDD12
109	VIU0_DAT3	237	DDR_DQS0_P
110	DVDD33	238	DDR_DQS0_N
111	VIU0_DAT4	239	VSS
112	VIU0_DAT5	240	DDR_DQS1_P
113	VIU0_DAT6	241	DDR_DQS1_N
114	VIU0_DAT7	242	VCC15
115	I2C_SCL	243	DDR_DQ12
116	I2C_SDA	244	DDR_DQ8
117	AVSS_VDAC	245	VCC15
118	VDAC_B	246	DDR_DQ14
119	VDAC_G	247	DDR_DQ10
120	VDAC_R	248	VSS
121	AVDD33_VDAC	249	DDR_DM0
122	VDAC_COMP	250	DDR_DQ1
123	VDAC_REXT	251	VCC15
124	VDAC_REXTS	252	DDR_DQ3
125	VDAC_COMPS	253	DDR_DQ7

Location	Pin name	Location	Pin name
126	AVSS_VDAC	254	VCC15
127	VDAC_CVBS0	255	DDR_DQ5
128	VDAC_CVBS1	256	VSS
		257(Epad) VSS	

2.2 Pin Description

2.2.1 Description of pin types

The pin I/O type description is shown in Table 2-2 .

Table 2-2 Pin I/O Type Description

I/O	illustrate
I	input signal.
IPD	Input signal, internally pulled down.
CUP	Input signal, internal pull-up.
IS	Input signal with Schmitt trigger.
ISPD	Input signal with Schmitt trigger, internal pull-down.
ISPU	Input signal, with Schmitt trigger, internally loaded.
O	output signal.
OOD	Output, open-drain.
I/O	Bidirectional input/output signals.
IPD/O	Bi-directional, input pull-down.
IPU/O	Bidirectional, input pull-up.
ISPU/O	Bidirectional, input pull-up, with Schmitt trigger.
IPD/OOD	Bidirectional, input pull-down, output open-drain.
IPU/OOD	Bidirectional, input pull-up, output open-drain.
IS/O	Bidirectional, input with Schmitt trigger.
IS/OOD	Bi-directional, input with Schmitt trigger, output open-drain.
CIN	Crystal Oscillator, crystal oscillator input.

I/O	illustrate
COUT	Crystal Oscillator, crystal oscillator output.
P	power supply.
G	land.

2.2.2 Pin information description

AIO pins

AIO pins are shown in Table 2-3 .

Table 2-3 AIO pins

Pin pin name	Type drive (mA)		Voltage (IN)	describe
92 AIO_BCLK_RX	I/O configurable, please refer to the system control register PERIPHCTRL28		3.3	Function 0: **AIO_BCLK_RX** S or I ^{2} PCM receive clock Function **1: GPIO7_4** general-purpose input and output
87 AIO_BCLK_TX	I/O configurable, please refer to the system control register PERIPHCTRL28		3.3	Function 0: **AIO_BCLK_TX** S or I ^{2} PCM transmit clock Function **1: GPIO7_1** general-purpose input and output
88 AIO_MCLK	IPD/O can be configured, please refer to the system control register PERIPHCTRL28		3.3	Function **0: AIO_MCLK** S or PCM I ^{2} interface master clock bell, can be used as audio CODEC working clock Function **1: GPIO7_0** general input and output Function **2: BOOT_SEL** boot space selection: 0: SPI FLASH storage space 1ÿBOOTROM
90 AIO_SD_RX	I/O	4	3.3	Function 0: **AIO_SD_RX**

Pin pin name	Type drive (mA)	Voltage (IN)	describe
			I 2 S or PCM interface data input. Function **1: GPIO7_6** general-purpose input and output
85 AIO_SD_TX	IPD/O 4	3.3 Function 0:	**AIO_SD_TX** S or I 2 PCM interface data output. Function **1: GPIO7_3** general purpose input and output function **2: JTAG_SEL** JTAG feature selection: 0ÿA9 1: HOURS
91 AIO_WS_RX	I/O is configurable, please refer to system control register PERIPHCTRL28	3.3 Function 0:	**AIO_WS_RX** S I 2 receives left and right channel selection signals, or PCM receives frame synchronization signals Function **1: GPIO7_5** general-purpose input and output
86 AIO_WS_TX	I/O can be configured, please refer to the system control register PERIPHCTRL28	3.3 Function 0:	**AIO_WS_TX** S I 2 sends left and right channel selection signals, or PCM sends frame synchronization signals Function **1: GPIO7_2** general-purpose input and output

Power and Ground Pins

The power and ground pins are shown in Table 2-4 .

Table 2-4 Power and ground pins

Pin	Pin Name Type Drive (mA)			Voltage (V) Description	
1ÿ13ÿ26ÿ 56ÿ66ÿ 89ÿ105ÿ 136ÿ170ÿ 184ÿ197ÿ 211ÿ222ÿ 236	DVDD12 P		·	1.25	Chip core power supply
24ÿ54ÿ 62ÿ71ÿ 83ÿ 95ÿ 110ÿ132ÿ 177ÿ187ÿ 195	DVDD33 P		·	3.3	Chip I/O Digital Power
257	VSS	G	·	-	chip ground

DDR pins

The DDR power and ground pins are shown in Table 2-5 .

Table 2-5 DDR power and ground pins

Pin	Pin name	Type drive (mA)		Voltage (V) Description	
5ÿ11ÿ206ÿ 212ÿ217ÿ 221ÿ226ÿ 229ÿ233ÿ 242ÿ245ÿ 251ÿ254	VCC15	P	·	1.8/1.5	DDR IO Power
2ÿ18ÿ36ÿ 39ÿ42ÿ48ÿ 201ÿ220ÿ 223ÿ239ÿ 248ÿ256	VSS	G -		·	DDR IO ÿ

The DDR signal pins are shown in Table 2-6 .

Table 2-6 DDR pins

Pin Name	Type	Drive (mA)			Voltage (V)	Description
209	DDR_A0	O			1.8/1.5	DDR SDRAM address signal 0
17	DDR_A1	O			1.8/1.5	DDR SDRAM address signal 1
202	DDR_A2	O			1.8/1.5	DDR SDRAM address signal 2
210	DDR_A3	O			1.8/1.5	DDR SDRAM address signal 3
10	DDR_A4	O			1.8/1.5	DDR SDRAM address signal 4
208	DDR_A5	O			1.8/1.5	DDR SDRAM address signal 5
12	DDR_A6	O			1.8/1.5	DDR SDRAM address signal 6
207	DDR_A7	O			1.8/1.5	DDR SDRAM address signal 7
14	DDR_A8	O			1.8/1.5	DDR SDRAM address signal 8
204	DDR_A9	O			1.8/1.5	DDR SDRAM address signal 9
7	DDR_A10	O			1.8/1.5	DDR SDRAM address signal 10
15	DDR_A11	O			1.8/1.5	DDR SDRAM address signal 11
9	DDR_A12	O			1.8/1.5	DDR SDRAM address signal 12
203	DDR_A13	O			1.8/1.5	DDR SDRAM address signal 13
16	DDR_A14	O			1.8/1.5	DDR SDRAM address signal 14
213	DDR_BA0	O			1.8/1.5	DDR SDRAM Bank address signal 0
8	DDR_BA1	O			1.8/1.5	DDR SDRAM Bank address signal 1
214	DDR_BA2	O			1.8/1.5	DDR SDRAM Bank address signal 2
218	DDR_CAS_N	O			1.8/1.5	DDR SDRAM Column Address Selection
6	DDR_CKE	O			1.8/1.5	DDR SDRAM clock enable
4	DDR_CLK1_N	O			1.8/1.5	DDR SDRAM Reverse Differential Clock 1
3	DDR_CLK1_P	O		-	1.8/1.5	DDR SDRAM Positive Differential Clock 1

Pin Name	Type	Drive (mA)		Voltage (V)	Description
249	DDR_DM0	I/O		1.8/1.5	DDR SDRAM data mask signal 0
230	DDR_DM1	I/O		1.8/1.5	DDR SDRAM data mask signal 1
228	DDR_DQ0	I/O		1.8/1.5	DDR SDRAM data line 0
250	DDR_DQ1	I/O		1.8/1.5	DDR SDRAM data line 1
227	DDR_DQ2	I/O		1.8/1.5	DDR SDRAM data line 2
252	DDR_DQ3	I/O		1.8/1.5	DDR SDRAM data line 3
224	DDR_DQ4	I/O		1.8/1.5	DDR SDRAM data line 4
255	DDR_DQ5	I/O		1.8/1.5	DDR SDRAM data line 5
225	DDR_DQ6	I/O		1.8/1.5	DDR SDRAM data line 6
253	DDR_DQ7	I/O		1.8/1.5	DDR SDRAM data line 7
244	DDR_DQ8	I/O		1.8/1.5	DDR SDRAM data line 8
235	DDR_DQ9	I/O		1.8/1.5	DDR SDRAM data line 9
247	DDR_DQ10	I/O		1.8/1.5	DDR SDRAM data line 10
231	DDR_DQ11	I/O		1.8/1.5	DDR SDRAM data line 11
243	DDR_DQ12	I/O		1.8/1.5	DDR SDRAM data line 12
232	DDR_DQ13	I/O		1.8/1.5	DDR SDRAM data line 13
246	DDR_DQ14	I/O		1.8/1.5	DDR SDRAM data line 14
234	DDR_DQ15	I/O		1.8/1.5	DDR SDRAM data line 15
238	DDR_DQS0_N	I/O		1.8/1.5	DDR reverse DQS Strobe signal 0, corresponding to DQ[7:0]
237	DDR_DQS0_P	I/O		1.8/1.5	DDR forward DQS Strobe signal 0, corresponding to DQ[7:0]
241	DDR_DQS1_N	I/O		1.8/1.5	DDR reverse DQS Strobe signal 1, corresponding to DQ[15:8]
240	DDR_DQS1_P	I/O	-	1.8/1.5	DDR forward DQS Strobe signal 1, corresponding to DQ[15:8]

Pin Name	Type	Drive (mA)			Voltage (V)	Description
216	DDR_ODT				1.8/1.5	DDR external matching reference resistor
219	DDR_RAS_N	O			1.8/1.5	DDR SDRAM Row Address Selection
205	DDR_RESET_N	O			1.8/1.5	DDR3 SDRAM reset signal
215	DDR_WE_N	O		-	1.8/1.5	DDR SDRAM write enable signal

FE PHY pins

The FE PHY pins are shown in Table 2-7 .

Table 2-7 FE PHY pins

Pin	Name	Type	Drive (mA)			Voltage (IN)	describe
171	ETH_ LED1	I/O		4		3.3	Function **0: GPIO5_6** general-purpose input and output Function **1: ETH_ LED1** fephy status LED1, under the initial configuration, this light will be on when the connection is successful. (Note: The function of this **LED** can be customized by the user, please refer to the **FEPHY** description chapter for specific operations)
172	ETH_ LED0	I/O		4		3.3	Function 0: GPIO5_7 general-purpose input and output Function 1: ETH_ LED0 fephy status LED0, under the initial configuration, this light will blink when data is transmitted. (Note: The function of this **LED** can be customized by the user, please refer to the **FEPHY** description chapter for specific operations)
152	AVDD12_FE	P				1.25	FE_PHY Power
154	AVSS12_FE	G					FE_PHY Ground
158	AVDD33_FE	P				3.3	FE_PHY Power
156	AVSS33_FE	G				-	FE_PHY Ground

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
159	ETH_RSET	I/O				Internal reference voltage, this pin needs an external 1% precision 2.49Kÿ resistor to ground
151	ETH_RXIN	I/O			3.3	Differential receive signal.
153	ETH_RXIP	I/O			3.3	Differential receive signal.
155	ETH_TXON	I/O			3.3	Differential transmit signal.
157	ETH_TXOP	I/O		-	3.3	Differential transmit signal.

GPIO pins

GPIO pins are shown in Table 2-8 .

Table 2-8 GPIO pins

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
186	GPIO0_0	I/O	12		3.3	Function **0: GPIO0_0** GPIO Function **1: RMII_CLK** RMII interface clock
182	GPIO0_1	I/O	8		3.3	Function **0: GPIO0_1** GPIO function **1: RMII_TX_EN** RMII send enable, indicating that the data sent is valid when the signal is valid
185	GPIO0_2	I/O	8		3.3	Function **0: GPIO0_2** GPIO Function **1: RMII_TXD0** RMII send data
183	GPIO0_3	I/O	8		3.3	Function **0: GPIO0_3** GPIO function **1: RMII_TXD1** RMII send data

Pin Name	Type	Drive (mA)		Voltage (IN)	describe
179	GPIO0_4	I/O	4	3.3	Function **0: GPIO0_4** GPIO function **1: RMII_CRS_DV** RMII receive data valid and carrier detection
189	GPIO0_5	I/O	4	3.3	Function **0: GPIO0_5** GPIO function **1: RMII_RXD0** RMII receive data
188	GPIO0_6	I/O	4	3.3	Function **0: GPIO0_6** GPIO function **1: RMII_RXD1** RMII receive data
178	GPIO0_7	I/O	4	3.3	Function **0: GPIO0_7** general-purpose input and output function **1: RMII_RX_ER** RMII receiving error, indicating that the received data is wrong, mac can discard it
27	GPIO1_0	I	4	3.3/5.0	Function **0: GPIO1_0** General purpose input and output function **1: UART3_TXD** UART3 data transmission
28	GPIO1_1	CUP	4	3.3/5.0	Function **0: GPIO1_1** General purpose input and output function **1: UART3_RXD** UART3 data reception
72	GPIO1_2	I/O	4	3.3	Function **0: GPIO1_2** general-purpose input and output Function **1: TEMPER_DQ** temperature acquisition, used to communicate with external temperature acquisition chips.
181	GPIO1_3	I/O	8	3.3	Function **0: GPIO1_3** GPIO Function **1: MDCK**

Pin Name Type Drive (mA)				Voltage (IN)	describe
					MDIO0 interface clock output
180	GPIO1_4	I/O	4	3.3 Function	**0: GPIO1_4** general input and output function **1: MDIO** Input/output signal of MDIO0 interface

HDMI pin

HDMI pins are shown in Table 2-9 .

Table 2-9 HDMI pins

Pin pin name		Type drive (mA)		Voltage (IN)	describe
138ÿ 141ÿ 147	AVDD12_HDMI P			1.25 HDMI	Analog Power
144ÿ 150	AVSS_HDMI	G			HDMI analog ground
135 HDMI_CEC		CUP	4	3.3/5.0 Function	**0: GPIO6_5** General purpose input and output function **1: HDMI_CEC** Control channel signal for HDMI interface
131 HDMI_HOTPLUG IPU			4	3.3/5.0 Function	**0: GPIO6_4** General purpose input and output function **1: HDMI_HOTPLUG** Hot plug signal for HDMI interface
137 HDMI_REXT		I/O		-	External resistor 6.67Kÿ to ground. For details, please refer to "Hi3520D Hardware Design User Guide".
134 HDMI_SCL		CUP	4	3.3/5.0 Function	**0: GPIO6_7** General purpose input and output function **1: HDMI_SCL** HDMI I2C bus clock, OD output

Pin pin name	Type drive (mA)		Voltage (IN)	describe
133 HDMI_SDA	CUP	4	3.3/5.0	Function **0: GPIO6_6** General purpose input and output function **1: HDMI_SDA** HDMI I2C bus data/address, OD output
142 HDMI_TX0N	O	-	1.2	Channel 0 serial differential signal
143 HDMI_TX0P	O	-	1.2	Channel 0 serial differential signal
145 HDMI_TX1N	O	-	1.2	Channel 1 serial differential signal
146 HDMI_TX1P	O	-	1.2	Channel 1 serial differential signal
148 HDMI_TX2N	O	-	1.2	Channel 2 serial differential signal
149 HDMI_TX2P	O	-	1.2	Channel 2 serial differential signal
139 HDMI_TXCN	O	-	1.2	Differential Pixel Clock
140 HDMI_TXCP	O	-	1.2	Differential Pixel Clock

I2C pins

The I2C pins are shown in Table 2-10 .

Table 2-10 I2C pins

Pin Name	Type	Drive (mA)		Voltage (IN)	describe
115	I2C_SCL	CUP	4	3.3/5.0	function **0: GPIO1_7** general purpose input and output function **1: I2C_SCL** I2C bus clock, OD output
116	I2C_SDA	IPU	4	3.3/5.0	function **0: GPIO1_6** general purpose input and output function **1: I2C_SDA** I2C bus data/address, OD output

IR pin

The IR pins are shown in Table 2-11 .

Table 2-11 IR pins

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
29	IR_IN	CUP	4		3.3/5.0	Function **0: GPIO7_7** GPIO function **1:** **IR_IN** infrared input

JTAG pins

The JTAG pins are shown in Table 2-12 .

Table 2-12 JTAG pins

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
19	JTAG_EN	IPD			3.3	JTAG pin enable: 0: Disable JTAG. 1: Enable JTAG.
21	JTAG_TCK	IPD/O		4	3.3	Function **0: GPIO2_4** GPIO Function **1: JTAG_TCK** JTAG clock input
23	JTAG_TDI	IPU/O		4	3.3	Function **0: GPIO2_7** General purpose input and output function **1: JTAG_TDI** JTAG data input
20	JTAG_TDO	I/O		4	3.3	Function **0: GPIO2_6** General purpose input and output function **1: JTAG_TDO** JTAG data output
22	JTAG_TMS	IPU/O		4	3.3	Function **0: GPIO2_5** general input and output function **1: JTAG_TMS**

Pin Name Type Drive (mA)				Voltage (IN)	describe
					JTAG mode select input, or data output for software trace. Two mode selections are controlled in the CPU
25	JTAG_TRSTN IPD/O		4	3.3 Function	**0: GPIO2_3** general-purpose input and output function **1: JTAG_TRSTN** JTAG reset input

SYS pin

The SYS pins are shown in Table 2-13 .

Table 2-13 SYS pins

Pin Name Type Drive (mA)				Voltage (IN)	describe
64	RSTN	CUP		3.3	System power-on reset signal input, active low
192	TEST_MODE IPD			3.3	Function mode and test mode selection: 0: Function mode 1: Test mode
63	WDG_RSTN I/O		4	3.3	Watchdog reset output, active low, OD output

RTC pin

RTC pins are shown in Table 2-14 .

Table 2-14 RTC pins

Pin Name Type Drive (mA)				Voltage (IN)	describe
75	AVDD_BAT P			3.3	RTC battery power
76	AVDD33_RTC P			3.3	RTC Analog Power
77	AVSS_RTC G			-	RTC Ground

74	RTC_XIN	I	-	3.3	RTC crystal input
73	RTC_XOUT O		-	3.3	RTC crystal output

SATA pins

The SATA pins are shown in Table 2-15 .

Table 2-15 SATA pins

Pin pin name		Type drive (mA)		Voltage (V) Description	
32ÿ 46ÿ 50ÿ51	AVDD12_SATA P		-	1.25	SATA power supply
33ÿ 45ÿ 49ÿ52	AVDD33_SATA P		-	3.3	SATA power supply
36ÿ 39ÿ 42ÿ48	VSS	G -		-	SATA land
30	SATA_LED_N0 IPU		4	3.3/5.0 function **0: GPIO2_1** general input and output Function 1: **SATA_LED_N0** SATA0 port LED indication, low effective	
31	SATA_LED_N1 IPU		4	3.3/5.0 Function **0: GPIO2_2** general-purpose input and output Function 1: **SATA_LED_N1** SATA1 port LED indication, low effective	
47	SATA_REXT	I/O	-	3.3	External resistor, the resistance is 191+/-1% ohms
37	SATA_RX0M	I	-	3.3	Differential signal received by channel 0
38	SATA_RX0P	I	-	3.3	Differential signal received by channel 0
41	SATA_RX1M	I	-	3.3	Differential signal received by channel 1

Pin pin name		Type drive (mA)		Voltage (V)	Description
40	SATA_RX1P	I	-	3.3	Differential signal received by channel 1
35	SATA_TX0M	O	-	3.3	Differential signal sent by channel 0
34	SATA_TX0P	O	-	3.3	Differential signal sent by channel 0
43	SATA_TX1M	O	-	3.3	Differential signal sent by channel 1
44	SATA_TX1P	O	-	3.3	Differential signal sent by channel 1

SFC pins

The SFC pins are shown in Table 2-16 .

Table 2-16 SFC pins

Pin pin name		Type Drive (mA)	Voltage (IN)	describe
58	SFC_CLK	IPD/O 11	3.3	Function **0: SFC_CLK** sends the clock signal to SPI Flash, the high and low levels of the clock stop are optional Function 1: **SFC_ADDR_MODE** sfc 3byte/ 4byte address mode selection: 0ÿ3byte 1ÿ4byte
55	SFC_CS0N	O	4	3.3 Chip select 0 signal, low effective
60	SFC_CS1N	O	4	3.3 Chip select 1 signal, low effective, used to hook up the booted SPI flash.
57	SFC_DIO	I/O configurable, see system control register PERIPHCT RL29	3.3	In Standard SPI mode, it is a data output signal; in Dual SPI mode, it is a data input and output signal; in Quad SPI mode, it is a data input and output signal.
61	SFC_DOI	I/O can be configured, please refer to the system control register	3.3	In Standard SPI mode, it is data input signal; in Dual SPI mode, it is data input signal

Pin pin name		Type Drive (mA) Voltage		(IN)	describe
			PERIPHCT RL29		Data input and output signals; In Quad SPI mode, it is data input and output signals.
59	SFC_HOLD_IO3 I/O can be configured, please refer to the system control register PERIPHCT RL29			3.3 In Standard SPI mode, as a hold function, low is effective; in Dual SPI mode, as a hold function, low is effective; In Quad SPI mode, it is the input and output signal for data.	
53	SFC_WP_IO2	I/O can be configured, please refer to the system control register PERIPHCT RL29		3.3 In Standard SPI mode, as a write protect function, low effective; in Dual SPI mode, as a write protect function, low effective; in Quad SPI mode, it is a data input and output signal.	

SPI pins

The SPI pins are shown in Table 2-17 .

Table 2-17 SPI pins

Pin Name	Type Drive (mA) Voltage		(IN)	describe
67	SPI_CSN0 IPU/O 4		3.3 Function **0: GPIO8_3** General purpose input and output function **1: SPI_CSN0** SPI chip select 0 output	
65	SPI_CSN1 I/O	4	3.3 Function **0: GPIO8_4** GPIO Function **1: SPI_CSN1** SPI chip select 1 output function **2: PWM_SVB** pwm output for svb	
68	SPI_SCLK I/O is configurable, please refer to 3.3 Function **0: GPIO8_0**			

Pin Name	Type	Drive (mA)	Voltage		(IN)	describe
				System Control Register PERIPHCTRL28		GPIO function **1:** **SPI_SCLK** SPI clock signal
70	SPI_SDI	I/O	4		3.3	Function **0: GPIO8_2** General purpose input and output function **1: SPI_SDI** SPI data input
69	SPI_SDO	I/O	can be configured, please refer to the	system control register PERIPHCTRL28	3.3	Function **0: PLL_TEST_OUT0** APLL_FOUTPOSTDIV 16 frequency division test clock output function **1:** **SPI_SDO** SPI data output function **2:** **PLL_TEST_OUT1** VPLL0_FOUT1PH0 4 frequency division test clock output function **3:** **PLL_TEST_OUT2** EPLL_FOUTPOSTDIV 8 frequency division test clock output function **4: GPIO8_1** general input and output

UART pins

The UART pins are shown in Table 2-18 .

Table 2-18 UART pins

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
190	UART0_RXD	IPU		4	3.3/5.0	UART0 data reception
191	UART0_TXD	I		4	3.3/5.0	UART0 data transmission
196	UART1_CTSN	I/O		4	3.3	Function **0: GPIO5_2** general-purpose input and output function **1: UART1_CTSN** Modem status input: Clear To Send. Low effective.

Pin Name Type Drive (mA)			Voltage (IN)	describe
				Function **2: PWM_SVB** pwm output for svb
193 UART1_RTSN I/O		4	3.3	Function **0: GPIO5_0** General-purpose input and output function **1:** **UART1_RTSN** Modem status output: request to send, active low. Reset value is 0
194 UART1_RXD IPU/O		4	3.3	Function **0: GPIO5_1** GPIO Function **1: UART1_RXD** UART1 data reception
198 UART1_TXD I/O		4	3.3	Function **0: GPIO5_3** General purpose input and output function **1: UART1_TXD** UART1 data transmission
199 UART2_RXD IPU/O		4	3.3	Function **0: GPIO5_4** General purpose input and output function **1: UART2_RXD** UART2 data reception
200 UART2_TXD I/O		4	3.3	Function **0: GPIO5_5** general input and output function **1: UART2_TXD** UART2 data transmission

USB pins

The USB pins are shown in Table 2-19 .

Table 2-19 USB pins

Pin pin name	Type drive (mA)		Voltage (IN)	describe
160 AVDD33_USB0 P		-	3.3	USB analog power
169 AVDD33_USB1 P		-	3.3	USB analog power

Pin pin name		Type drive (mA)		Voltage (IN)	describe
163ÿ 166	AVSS_USB	P	-	-	USB analog ground
164	USB_REXT	I/O	-	3.3	USB external resistor interface, the resistance value is 43.2±1%ÿ, the external pin
162	USB0_DM	I/O	-	0.4/3.3	USB0 D- signal, in high speed mode, the maximum voltage of this port is 800mV or 400mV, in full speed and low speed mode, the voltage of this port is 3.3V
161	USB0_DP	I/O	-	0.4/3.3	USB0 D+ signal, in high speed mode, the maximum voltage of this port is 800mV or 400mV, in full speed and low speed mode, the voltage of this port is 3.3V
173	USB0_OVRCUR	I/O	4	3.3	Function **0: GPIO6_0** General purpose input and output function **1: USB0_OVRCUR** The port overcurrent indication signal of USB port 0, high and low levels can be configured, and the default is high level active
174	USB0_PWREN	I/O	4	3.3	Function **0: GPIO6_1** general input and output function **1: USB0_PWREN** USB port 0 power control output pin, high and low level can be configured, the default is low level active
167	USB1_DM	I/O	-	0.4/3.3	USB D-signal, in high speed mode, the maximum voltage of this port is 800mV or 400mV, in full speed and low speed mode, the voltage of this port is 3.3V
168	USB1_DP	I/O	-	0.4/3.3	USB D+ signal, in high speed mode, the maximum voltage of this port is 800mV or 400mV, in full speed and low speed mode, the voltage of this port is 3.3V
175	USB1_OVRCUR	I/O	4	3.3	Function **0: GPIO6_2** general input and output

Pin pin name	Type drive (mA)	Voltage (IN)	describe
			Function **1: USB1_OVRCUR** Port overcurrent indication signal of USB port 1, high and low levels can be configured, and the default is high level active
176 USB1_PWREN I/O	4	3.3	Function **0: GPIO6_3** General purpose input and output function **1: USB1_PWREN** USB port 1 power control output pin, high and low level can be configured, the default is low level active

VDAC pin

The VDAC pins are shown in Table 2-20 .

Table 2-20 VDAC pins

Pin pin name	Type drive (mA)	Voltage (IN)	describe
121 AVDD33_VDAC P		3.3	VDAC power supply
117ÿ AVSS_VDAC G 126			VDAC ground
122 VDAC_COMP I/O		3.3	The external decoupling reference voltage of the RBG channel is connected to a 0.01uf ceramic capacitor and a 10uF tantalum capacitor in parallel to AVDD33_VDAC
125 VDAC_COMPS I/O		3.3	The external decoupling reference voltage of the CVBS0/1 channel, connect a 0.01uf ceramic capacitor and a 10uF tantalum capacitor in parallel to AVDD33_VDAC
127 VDAC_CVBS0 O		1.0	CVBS0 channel output
128 VDAC_CVBS1 O		1.0	CVBS1 channel output
118 VDAC_B	O	1.0	B channel output of VGA
119 VDAC_G	O	1.0	G channel output for VGA
120 VDAC_R	O	1.0	R channel output of VGA

Pin pin name	Type drive (mA)	Voltage (IN)	describe
123 VDAC_REXT I/O			DAC external resistor of RBG channel, the resistance value of the connected resistor TBDÿ
124 VDAC_REXTS I/O			DAC external resistor of CVBS0/1 channel, the resistance value of the connected resistor TBDÿ

VGA pin

The VGA pins are shown in Table 2-21 .

Table 2-21 VGA pins

Pin Name	Type Drive (mA)	Voltage		(IN)	describe
129 VGA_HS	I/O	configurable, please refer to the system control register PERIPHCTRL28		3.3	Function **0: GPIO2_0** General purpose input and output function **1: VGA_HS** VGA line sync output
130 VGA_VS	I/O	configurable, please refer to the system control register PERIPHCTRL28		3.3	Function **0: GPIO1_5** General purpose input and output function **1: VGA_VS** VGA field sync output

VI_ADC pin

VI_ADC pins are shown in Table 2-22 .

Table 2-22 VI_ADC pins

Pin Name	Type Drive (mA)	Voltage		(IN)	describe
93 VI_ADC_CLK	I/O	configurable, please refer to the system control register PERIPHCTRL28		3.3	Function **0: GPIO8_5** GPIO Function **1: VI_ADC_CLK** Vedio ADC working clock, please refer to CRG register for details

Pin Name Type Drive (mA) Voltage				(IN)	describe
					Register PERI_CRG11[19:18] Function 2: **CLK_TEST_OUT0** APB test clock output, 1/4 of the bus clock Function 3: **CLK_TEST_OUT1** hdmi_asclk or usb_phy_clk12 test clock output, please refer to the specific configuration CRG register PERI_CRG57[19] function 4: **CLK_TEST_OUT2** hdmi_osclk or usb_phy_freeclk test clock output, please refer to the specific configuration CRG register PERI_CRG57[19] function 5: **CLK_TEST_OUT3** hdmi_vk2x 4 frequency division or sata_ckword 2 frequency division test clock output, please refer to the specific configuration CRG register PERI_CRG57[19] function 6: **RTC_TEST_CLK** RTC test clock output, please refer to RTC internal register RTC_CLK[1:0] for specific configuration

VIU0 pin

VIU0 pins are shown in Table 2-23 .

Table 2-23 VIU0 pins

Pin Name Type Drive (mA)				Voltage (IN)	describe
104	VIU0_CLK I/O		4	3.3	Function **0: VIU0_CLK**

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
						Clock signal for VIU0. Function **1: GPIO8_6** general purpose input and output function **2:** **fephy_dbg_adccki** fephy debug adc clock function **3: VIU0_DAT0** Data input for VIU0
106	VIU0_DAT0	I/O		4	3.3	Function **0: VIU0_DAT0** VIU0 data input function **1:** **GPIO3_0** general input and output function **2:** **fephy_dbg_out0** fephy debug adc output function **3: VIU0_DAT1** Data input for VIU0
107	VIU0_DAT1	I/O		4	3.3	Function **0: VIU0_DAT1** Data input for VIU0 Function **1: GPIO3_1** general purpose input and output function **2:** **fephy_dbg_out1** fephy debug adc output function **3: VIU0_DAT2** Data input for VIU0
108	VIU0_DAT2	I/O		4	3.3	Function **0: VIU0_DAT2** Data input for VIU0 Function **1: GPIO3_2** general purpose input and output function **2:** **fephy_dbg_out2** fephy debug adc output function **3: VIU0_DAT3** Data input for VIU0
109	VIU0_DAT3	I/O		4	3.3	Function **0: VIU0_DAT3** Data input function 1 of VIU0 : **GPIO3_3**

Pin Name	Type	Drive (mA)			Voltage (IN)	describe
						GPIO function **2:** **fephy_dbg_out3** fephy debug adc output function **3: VIU0_DAT4** Data input for VIU0
111	VIU0_DAT4	I/O		4	3.3	Function **0: VIU0_DAT4** Data input for VIU0 Function **1: GPIO3_4** general input and output function **2: fephy_dbg_out4** fephy debug adc output function **3: VIU0_DAT5** Data input for VIU0
112	VIU0_DAT5	I/O		4	3.3	Function **0: VIU0_DAT5** Data input for VIU0 Function **1: GPIO3_5** general purpose input and output function **2:** **fephy_dbg_out5** fephy debug adc output function **3: VIU0_DAT6** Data input for VIU0
113	VIU0_DAT6	I/O		4	3.3	Function **0: VIU0_DAT6** Data input for VIU0 Function **1: GPIO3_6** general purpose input and output function **2:** **fephy_dbg_out6** fephy debug adc output function **3: VIU0_DAT7** Data input for VIU0
114	VIU0_DAT7	I/O		4	3.3	Function **0: VIU0_DAT7** Data input for VIU0 Function **1: GPIO3_7** general purpose input and output function **2: fephy_dbg_out7**

Pin Name Type Drive (mA)				Voltage (IN)	describe
					fephy debug adc output function **3: VIU0_CLK** clock signal of VIU0.

VIU1 pin

The VIU1 pins are shown in Table 2-24 .

注意

In Hi3515A chip, VIU1 data input is invalid, but all VIU1 pins can still be used as other functions, such as GPIO.

Table 2-24 VIU1 pins

Pin Name Type Drive (mA) Voltage (V) Description					
94	VIU1_CLK I/O		4	3.3	Function **0: VIU1_CLK** VIU1 clock signal. Function **1: GPIO8_7** general purpose input and output function **3: VIU1_DAT0** Data input for VIU1
96	VIU1_DAT0 I/O		4	3.3	Function **0: VIU1_DAT0** Data input for VIU1 Function **1: GPIO4_0** general input and output Function **2: fephy_dbg_out8** fephy debug adc output function **3: VIU1_DAT1** Data input for VIU1
97	VIU1_DAT1 I/O		4	3.3	Function **0: VIU1_DAT1** Data input for VIU1 Function **1: GPIO4_1** general input and output

Pin Name	Type	Drive (mA)	Voltage (V)	Description	
					Function **2: fephy_dbg_out9** fephy debug adc output function **3: VIU1_DAT2** Data input for VIU1
98	VIU1_DAT2	I/O	4	3.3	Function **0: VIU1_DAT2** Data input for VIU1 Function **1: GPIO4_2** general-purpose input and output Function 2: **fephy_dbg_out10** fephy debug adc output function **3: VIU1_DAT3** Data input for VIU1
99	VIU1_DAT3	I/O	4	3.3	Function **0: VIU1_DAT3** Data input for VIU1 Function **1: GPIO4_3** general input and output Function 2: **fephy_dbg_out11** fephy debug adc output function **3: VIU1_DAT4** Data input for VIU1
100	VIU1_DAT4	I/O	4	3.3	Function **0: VIU1_DAT4** Data input for VIU1 Function **1: GPIO4_4** general input and output Function 2: **fephy_dbg_out12** fephy debug adc output function **3: VIU1_DAT5** Data input for VIU1
101	VIU1_DAT5	I/O	4	3.3	Function **0: VIU1_DAT5** Data input function **1 of VIU1: GPIO4_5** general-purpose input and output Function 2:

Pin Name Type Drive (mA) Voltage (V) Description					
					fephy_dbg_out13 fephy debug adc output function **3:** **VIU1_DAT6** Data input for VIU1
102	VIU1_DAT6 I/O		4	3.3	Function **0: VIU1_DAT6** Data input for VIU1 Function **1: GPIO4_6** general-purpose input and output Function 2: **fephy_dbg_out14** fephy debug adc output function **3:** **VIU1_DAT7** Data input for VIU1
103	VIU1_DAT7 I/O		4	3.3	Function **0: VIU1_DAT7** VIU1 data input function **1: GPIO4_7** general input and output function 2: **fephy_dbg_out15** fephy debug adc output function **3:** **VIU1_CLK** VIU1 clock signal.

OSC pin

The OSC pins are shown in Table 2-25 .

Table 2-25 OSC pins

Pin Name Type Drive (mA) Voltage (V) Description					
81	ASK FOR	I	·	3.3	Crystal input
82	XOUT	O	-	3.3	Crystal output

EFUSE pin

The EFUSE pins are shown in Table 2-26 .

Table 2-26 EFUSE pins

Pin Name	Type	Drive (mA)	Voltage (V)	Description	
84	AVDD_EFUSE	P		2.5	EFUSE 2.5V programming power supply Note: Please refer to the Hardware Design User Guide for hardware design.

PLL pins

PLL pins are shown in Table 2-27 .

Table 2-27 PLL pins

Pin	pin name	Type	drive (mA)	Voltage (V)	Description
78	AVDD12_PLL	P		1.25	Analog power supply for PLL
80	AVDD33_PLL	P		3.3	Analog power supply for PLL
79	AVSS_PLL	G	-	-	Analog ground for PLL

2.3 Pin multiplexing control register

2.3.1 Overview of Multiplexing Registers

An overview of multiplexed registers is shown in Table 2-28 .

Table 2-28 Overview of multiplexed registers (base address is 0x200F_0000)

offset address	name	describe	page number
0x000	muxctrl_reg0	VI_ADC_CLK pin mux control register	2-39
0x004	muxctrl_reg1	VIU0_CLKÿVIU0_DAT0ÿVIU0_DAT1ÿ VIU0_DAT2ÿVIU0_DAT3ÿVIU0_DAT4ÿ Multiplexing control register for VIU0_DAT5, VIU0_DAT6, VIU0_DAT7 pins	2-40
0x008	muxctrl_reg2	VIU1_CLKÿVIU1_DAT0ÿVIU1_DAT1ÿ VIU1_DAT2ÿVIU1_DAT3ÿVIU1_DAT4ÿ VIU1_DAT5, VIU1_DAT6, VIU1_DAT7 tubes	2-42

offset address	name		page number
		Multiplexing control register describing pin	
0x00C	muxctrl_reg3	VGA_HS pin mux control register	2-44
0x010	muxctrl_reg4	VGA_VS pin mux control register	2-44
0x014	muxctrl_reg5	AIO_MCLK pin mux control register	2-45
0x018	muxctrl_reg6	AIO_BCLK_TX pin mux control register	2-45
0x01C	muxctrl_reg7	AIO_WS_TX pin mux control register	2-46
0x020	muxctrl_reg8	AIO_SD_TX pin mux control register	2-46
0x024	muxctrl_reg9	AIO_BCLK_RX pin mux control register	2-46
0x028	muxctrl_reg10	AIO_WS_RX pin mux control register	2-47
0x02C	muxctrl_reg11	AIO_SD_RX pin mux control register	2-47
0x030	muxctrl_reg12	SPI_SCLK pin mux control register	2-48
0x034	muxctrl_reg13	SPI_SDO pin mux control register	2-48
0x038	muxctrl_reg14	SPI_SDI pin mux control register	2-49
0x03C	muxctrl_reg15	Multiplexing control register for SPI_CSN0 pin	2-49
0x040	muxctrl_reg16	Multiplexing control register for SPI_CSN1 pin	2-50
0x044	muxctrl_reg17	I2C_SDA pin mux control register	2-50
0x048	muxctrl_reg18	I2C_SCL pin mux control register	2-51
0x04C	muxctrl_reg19	UART1_RTSN pin mux control register	2-51
0x050	muxctrl_reg20	UART1_RXD pin mux control register	2-52
0x054	muxctrl_reg21	Mux control register for UART1_CTSN pin	2-52
0x058	muxctrl_reg22	UART1_TXD pin mux control register	2-53
0x05C	muxctrl_reg23	UART2_RXD pin mux control register	2-53
0x060	muxctrl_reg24	UART2_TXD pin mux control register	2-54
0x064	muxctrl_reg25	IR_IN pin mux control register	2-54
0x068	muxctrl_reg26	USB0_OVRCUR pin mux control register 2-55	
0x06C	muxctrl_reg27	USB0_PWREN pin mux control register	2-55
0x070	muxctrl_reg28	USB1_OVRCUR pin mux control register 2-56	
0x074	muxctrl_reg29	USB1_PWREN pin mux control register	2-56
0x078	muxctrl_reg30	HDMI_HOTPLUG pin multiplexing control register 2-57	

offset address	name	describe	page number
0x07C	muxctrl_reg31	HDMI_CEC pin mux control register	2-57
0x080	muxctrl_reg32	HDMI_SDA pin mux control register	2-58
0x084	muxctrl_reg33	HDMI_SCL pin mux control register	2-58
0x088	muxctrl_reg34	Multiplexing control register for SATA_LED_N0 pin	2-59
0x08C	muxctrl_reg35	Multiplexing control register for SATA_LED_N1 pin	2-59
0x090	muxctrl_reg36	Multiplexing control register for ETH_LED1 pin	2-60
0x094	muxctrl_reg37	ETH_LED0 pin multiplexing control register	2-60
0x098	muxctrl_reg38	GPIO0_0 pin mux control register	2-61
0x09C	muxctrl_reg39	GPIO0_1 pin mux control register	2-61
0x0A0	muxctrl_reg40	GPIO0_2 pin mux control register	2-62
0x0A4	muxctrl_reg41	GPIO0_3 pin mux control register	2-62
0x0A8	muxctrl_reg42	GPIO0_4 pin mux control register	2-63
0x0AC	muxctrl_reg43	GPIO0_5 pin mux control register	2-63
0x0B0	muxctrl_reg44	GPIO0_6 pin mux control register	2-64
0x0B4	muxctrl_reg45	GPIO0_7 pin mux control register	2-64
0x0B8	muxctrl_reg46	GPIO1_0 pin mux control register	2-65
0x0BC	muxctrl_reg47	GPIO1_1 pin mux control register	2-65
0x0C0	muxctrl_reg48	GPIO1_2 pin mux control register	2-66
0x0C4	muxctrl_reg49	GPIO1_3 pin mux control register	2-66
0x0C8	muxctrl_reg50	GPIO1_4 pin mux control register	2-67

2.3.2 Multiplexing register description

muxctrl_reg0

VI_ADC_CLK pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg0	The specific multiplexing of VI_ADC_CLK pin. 000ÿGPIO8_5ÿ 001ÿVI_ADC_CLKÿ 010ÿCLK_TEST_OUT0ÿ 011ÿCLK_TEST_OUT1ÿ 100ÿCLK_TEST_OUT2ÿ 101ÿCLK_TEST_OUT3ÿ 110: RTC_TEST_CLK; Others: Reserved.

muxctrl_reg1

VIU0_CLK pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg1	Simultaneously control the 1st to 9th group pins. Group 1: Specific multiplexing of VIU0_CLK pin. 00ÿVIU0_CLKÿ 01ÿGPIO8_6ÿ 10ÿfephy_dbg_adcckiÿ

			11: VIU0_DAT0. Group 2: The specific multiplexing of VIU0_DAT0 pins. 00ÿVIU0_DAT0ÿ 01ÿGPIO3_0ÿ 10: fephy_dbg_out0; 11: VIU0_DAT1. Group 3: The specific multiplexing of VIU0_DAT1 pins. 00ÿVIU0_DAT1ÿ 01ÿGPIO3_1ÿ 10ÿfephy_dbg_out1ÿ 11: VIU0_DAT2. Group 4: The specific multiplexing of VIU0_DAT2 pins. 00ÿVIU0_DAT2ÿ 01ÿGPIO3_2ÿ 10ÿfephy_dbg_out2ÿ 11: VIU0_DAT3. Group 5: The specific multiplexing of VIU0_DAT3 pin. 00ÿVIU0_DAT3ÿ 01ÿGPIO3_3ÿ 10: fephy_dbg_out3; 11: VIU0_DAT4. Group 6: The specific multiplexing of VIU0_DAT4 pins. 00ÿVIU0_DAT4ÿ 01ÿGPIO3_4ÿ 10ÿfephy_dbg_out4ÿ 11: VIU0_DAT5. Group 7: The specific multiplexing of VIU0_DAT5 pin. 00ÿVIU0_DAT5ÿ 01ÿGPIO3_5ÿ 10ÿfephy_dbg_out5ÿ 11: VIU0_DAT6. Group 8:

			The specific multiplexing of VIU0_DAT6 pin. 00ÿVIU0_DAT6ÿ 01ÿGPIO3_6ÿ 10ÿfephy_dbg_out6ÿ 11: VIU0_DAT7. Group 9: The specific multiplexing of VIU0_DAT7 pins. 00ÿVIU0_DAT7ÿ 01ÿGPIO3_7ÿ 10ÿfephy_dbg_out7ÿ 11ÿVIU0_CLKÿ

muxctrl_reg2

VIU1_CLK pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg2	Simultaneously control the 1st to 9th group pins. Group 1: The specific multiplexing of the VIU1_CLK pin. 00ÿVIU1_CLKÿ 01ÿGPIO8_7ÿ 11: VIU1_DAT0; Others: Reserved. Group 2: The specific multiplexing of the VIU1_DAT0 pin. 00ÿVIU1_DAT0ÿ 01ÿGPIO4_0ÿ 10ÿfephy_dbg_out8ÿ 11ÿ VIU1_DAT1ÿ

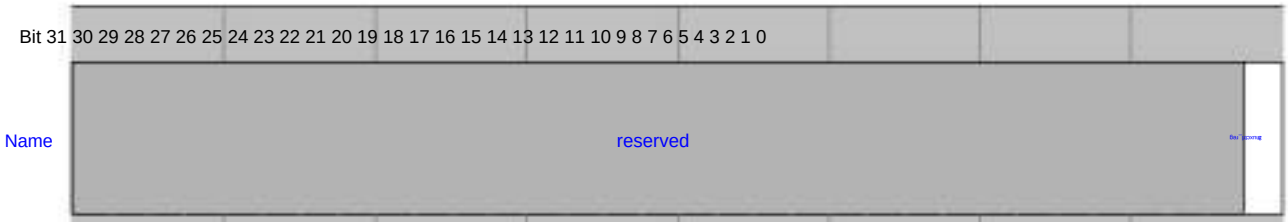
			Group 3: specific multiplexing of VIU1_DAT1 pins. 00ÿVIU1_DAT1ÿ 01ÿGPIO4_1ÿ 10ÿfephy_dbg_out9ÿ 11: VIU1_DAT2. Group 4: The specific multiplexing of the VIU1_DAT2 pin. 00ÿVIU1_DAT2ÿ 01ÿGPIO4_2ÿ 10: fephy_dbg_out10; 11: VIU1_DAT3. Group 5: The specific multiplexing of VIU1_DAT3 pins. 00ÿVIU1_DAT3ÿ 01ÿGPIO4_3ÿ 10ÿfephy_dbg_out11ÿ 11: VIU1_DAT4. Group 6: The specific multiplexing of VIU1_DAT4 pins. 00ÿVIU1_DAT4ÿ 01ÿGPIO4_4ÿ 10ÿfephy_dbg_out12ÿ 11: VIU1_DAT5. Group 7: The specific multiplexing of the VIU1_DAT5 pin. 00ÿVIU1_DAT5ÿ 01ÿGPIO4_5ÿ 10ÿfephy_dbg_out13ÿ 11: VIU1_DAT6. Group 8: The specific multiplexing of VIU1_DAT6 pins. 00ÿVIU1_DAT6ÿ 01ÿGPIO4_6ÿ 10ÿfephy_dbg_out14ÿ 11: VIU1_DAT7. Group 9: The specific multiplexing of VIU1_DAT7 pins.

			00ÿVIU1_DAT7ÿ 01ÿGPIO4_7ÿ 10ÿfephy_dbg_out15ÿ 11ÿVIU1_CLKÿ

muxctrl_reg3

VGA_HS pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

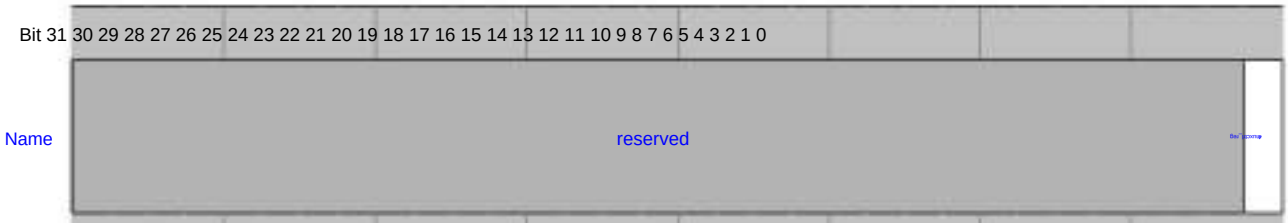


Bits	Access	Name	Description
[0]	RW	muxctrl_reg3	The specific multiplexing of the VGA_HS pin. 0ÿGPIO2_0ÿ 1ÿVGA_HSÿ

muxctrl_reg4

VGA_VS pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000



Bits	Access	Name	Description
[0]	RW	muxctrl_reg4	The specific multiplexing of the VGA_VS pin. 0ÿGPIO1_5ÿ 1ÿVGA_VSÿ

muxctrl_reg5

AIO_MCLK pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg5	The specific multiplexing of the AIO_MCLK pin. 00ÿAIO_MCLKÿ 01ÿGPIO7_0ÿ 10: BOOT_SEL; Others: reserved.

muxctrl_reg6

AIO_BCLK_TX pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg6	The specific multiplexing of the AIO_BCLK_TX pin. 0ÿAIO_BCLK_TXÿ 1ÿGPIO7_1ÿ

muxctrl_reg7

AIO_WS_TX pin mux control register.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[0]	RW	muxctrl_reg7	The specific multiplexing of the AIO_WS_TX pin. 0ÿAIO_WS_TXÿ 1ÿGPIO7_2ÿ

muxctrl_reg8

AIO_SD_TX pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg8	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[1:0]	RW	muxctrl_reg8	The specific multiplexing of the AIO_SD_TX pin. 00ÿAIO_SD_TXÿ 01ÿGPIO7_3ÿ 10: JTAG_SEL; Others: Reserved.

muxctrl_reg9

AIO_BCLK_RX pin mux control register.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[0]	RW	muxctrl_reg9	The specific multiplexing of the AIO_BCLK_RX pin. 0ÿAIO_BCLK_RXÿ 1ÿGPIO7_4ÿ

muxctrl_reg10

AIO_WS_RX pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

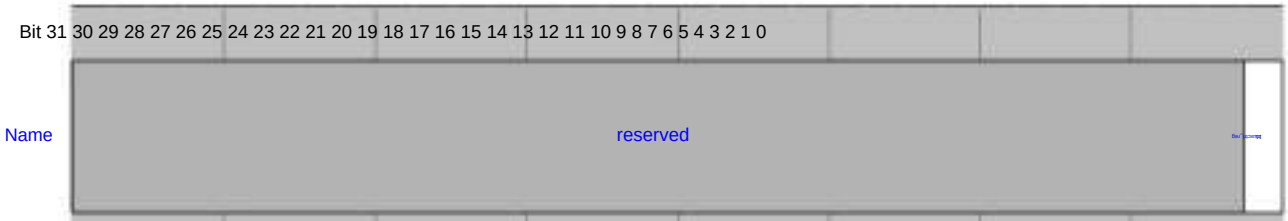
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[0]	RW	muxctrl_reg10	The specific reuse of the AIO_WS_RX pin. 0ÿAIO_WS_RXÿ 1ÿGPIO7_5ÿ

muxctrl_reg11

AIO_SD_RX pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

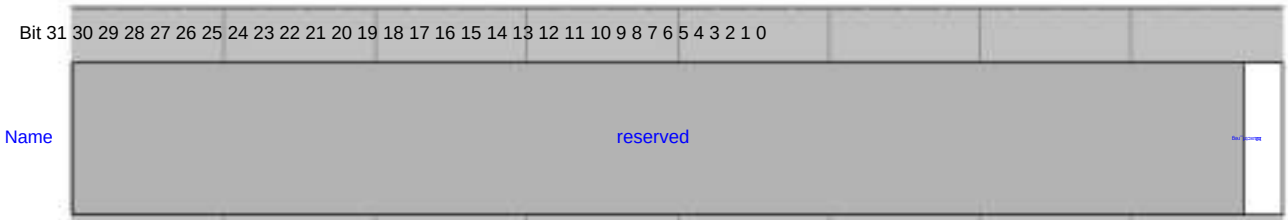


Bits	Access	Name	Description
[0]	RW	muxctrl_reg11	The specific multiplexing of the AIO_SD_RX pin. 0ÿAIO_SD_RXÿ 1ÿGPIO7_6ÿ

muxctrl_reg12

SPI_SCLK pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000



Bits	Access	Name	Description
[0]	RW	muxctrl_reg12	The specific multiplexing of the SPI_SCLK pin. 0ÿGPIO8_0ÿ 1ÿSPI_SCLKÿ

muxctrl_reg13

SPI_SDO pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg13	The specific multiplexing of the SPI_SDO pin. 000ÿPLL_TEST_OUT0ÿ 001ÿSPI_SDOÿ 010ÿPLL_TEST_OUT1ÿ 011ÿPLL_TEST_OUT2ÿ 100: GPIO8_1; Others: Reserved.

muxctrl_reg14

SPI_SDI pin mux control register.

Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

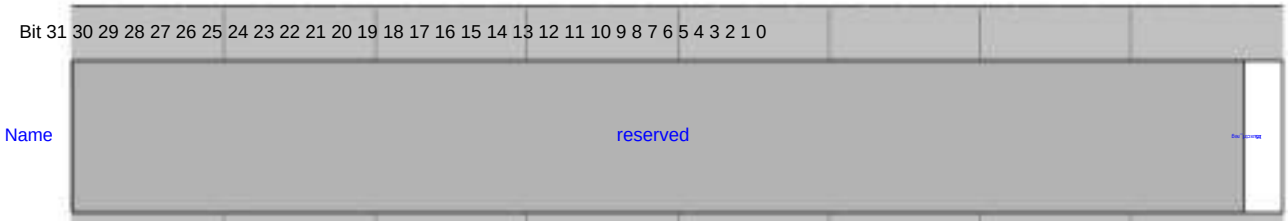
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg14	The specific multiplexing of the SPI_SDI pin. 0ÿGPIO8_2ÿ 1ÿSPI_SDIÿ

muxctrl_reg15

SPI_CSN0 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

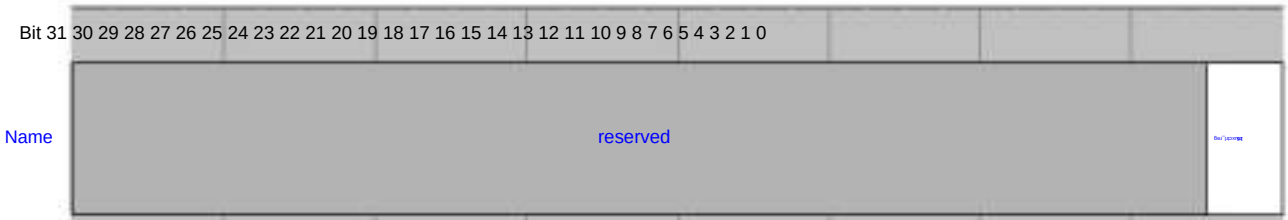


Bits	Access Name		Description
[0]	RW	muxctrl_reg15	The specific multiplexing of the SPI_CSN0 pin. 0ÿGPIO8_3ÿ 1ÿSPI_CSN0ÿ

muxctrl_reg16

SPI_CSN1 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

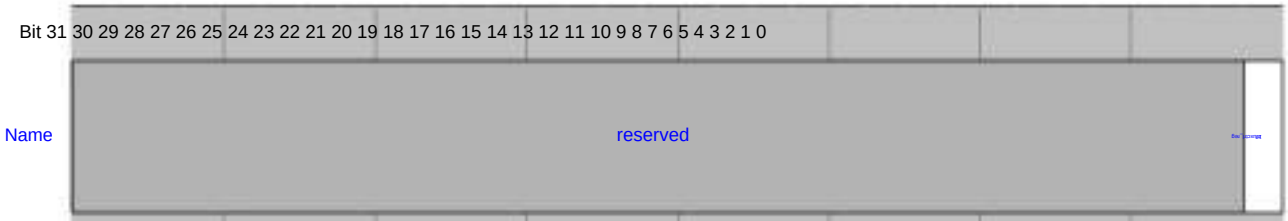


Bits	Access Name		Description
[1:0]	RW	muxctrl_reg16	The specific multiplexing of the SPI_CSN1 pin. 00ÿGPIO8_4ÿ 01ÿSPI_CSN1ÿ 10: PWM_SVB; Others: Reserved.

muxctrl_reg17

I2C_SDA pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

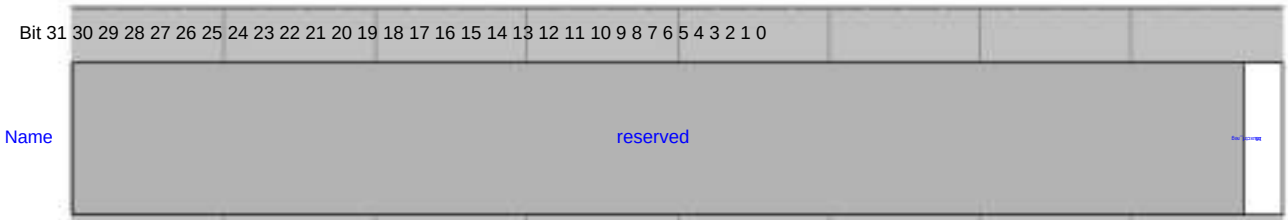


Bits	Access Name		Description
[0]	RW	muxctrl_reg17	The specific multiplexing of the I2C_SDA pin. 0ÿGPIO1_6ÿ 1ÿI2C_SDAÿ

muxctrl_reg18

I2C_SCL pin mux control register.

Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000



Bits	Access Name		Description
[0]	RW	muxctrl_reg18	The specific multiplexing of the I2C_SCL pin. 0ÿGPIO1_7ÿ 1ÿI2C_SCLÿ

muxctrl_reg19

UART1_RTSN pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[0]	RW	muxctrl_reg19	The specific reuse of UART1_RTSN pin. 0ÿGPIO5_0ÿ 1ÿUART1_RTSNÿ

muxctrl_reg20

UART1_RXD pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

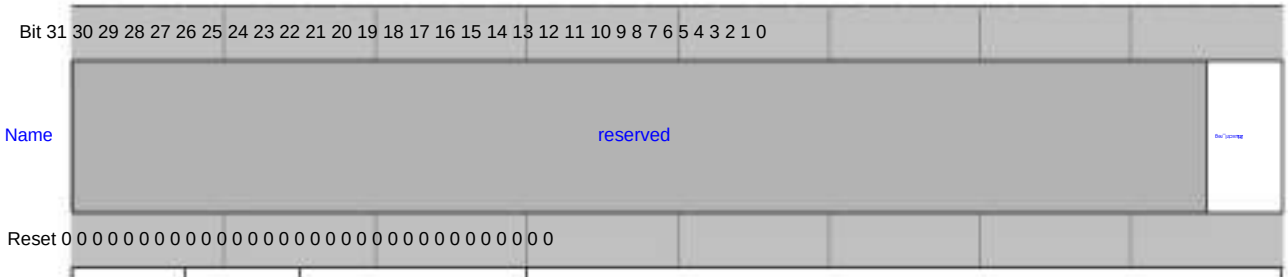
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[0]	RW	muxctrl_reg20	The specific reuse of UART1_RXD pin. 0ÿGPIO5_1ÿ 1ÿUART1_RXDÿ

muxctrl_reg21

UART1_CTSN pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

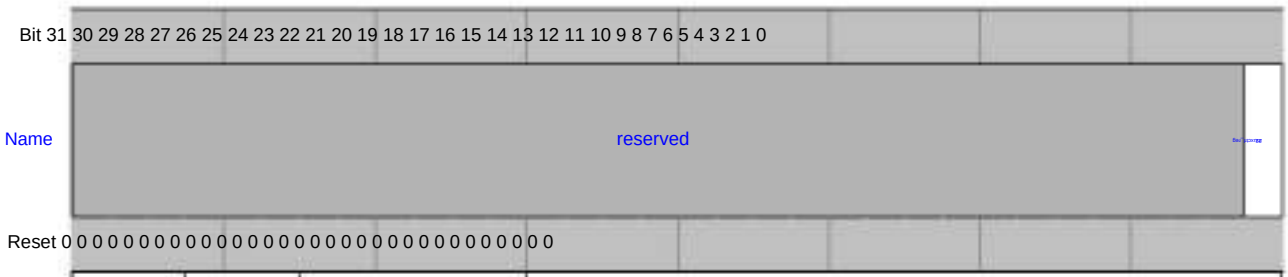


Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg21	The specific reuse of UART1_CTSN pin. 00ÿGPIO5_2ÿ 01ÿUART1_CTSNÿ 10: PWM_SVB; Others: Reserved.

muxctrl_reg22

UART1_TXD pin mux control register.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

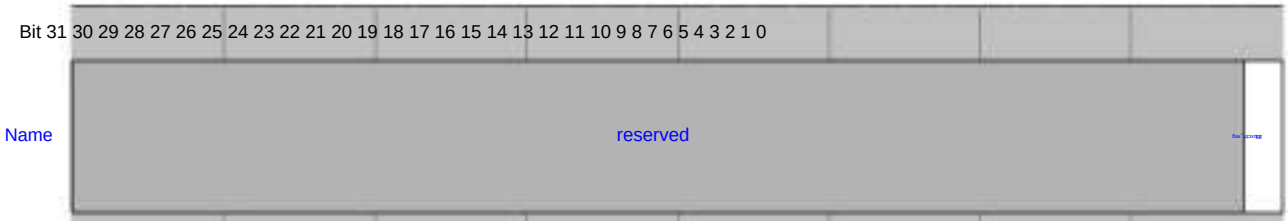


Bits	Access	Name	Description
[0]	RW	muxctrl_reg22	The specific multiplexing of UART1_TXD pin. 0ÿGPIO5_3ÿ 1ÿUART1_TXDÿ

muxctrl_reg23

UART2_RXD pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

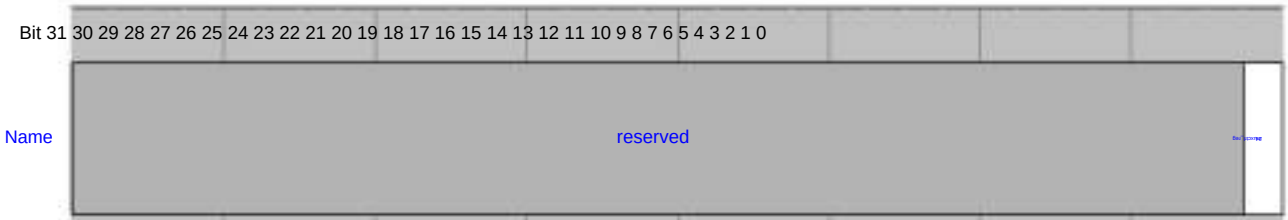


Bits	Access Name		Description
[0]	RW	muxctrl_reg23	The specific reuse of UART2_RXD pin. 0ÿGPIO5_4ÿ 1ÿUART2_RXDÿ

muxctrl_reg24

UART2_TXD pin mux control register.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

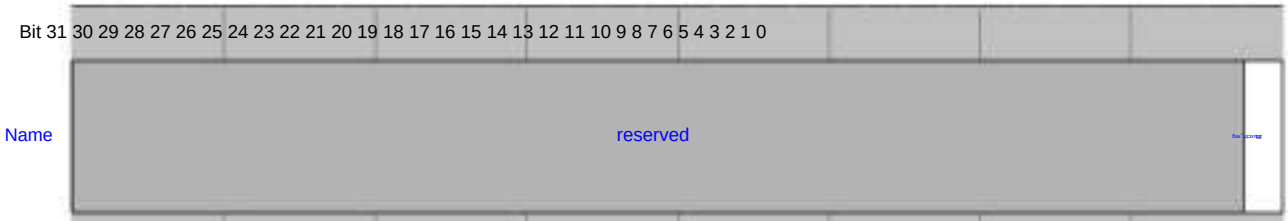


Bits	Access Name		Description
[0]	RW	muxctrl_reg24	The specific multiplexing of UART2_TXD pin. 0ÿGPIO5_5ÿ 1ÿUART2_TXDÿ

muxctrl_reg25

IR_IN pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

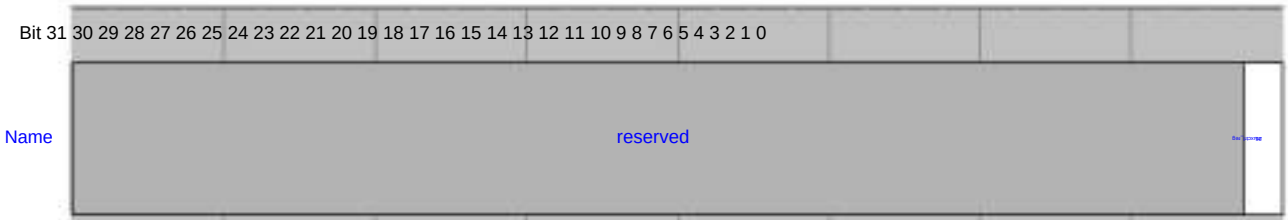


Bits	Access	Name	Description
[0]	RW	muxctrl_reg25	The specific multiplexing of the IR_IN pin. 0ÿGPIO7_7ÿ 1ÿIR_INÿ

muxctrl_reg26

USB0_OVRCUR pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000



Bits	Access	Name	Description
[0]	RW	muxctrl_reg26	The specific multiplexing of the USB0_OVRCUR pin. 0ÿGPIO6_0ÿ 1ÿUSB0_OVRCURÿ

muxctrl_reg27

USB0_PWREN pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[0]	RW	muxctrl_reg27	The specific multiplexing of the USB0_PWREN pin. 0ÿGPIO6_1ÿ 1ÿUSB0_PWRENÿ

muxctrl_reg28

USB1_OVRCUR pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[0]	RW	muxctrl_reg28	The specific multiplexing of the USB1_OVRCUR pin. 0ÿGPIO6_2ÿ 1ÿUSB1_OVRCURÿ

muxctrl_reg29

USB1_PWREN pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg29	The specific multiplexing of the USB1_PWREN pin. 0ÿGPIO6_3ÿ 1ÿUSB1_PWRENÿ

muxctrl_reg30

HDMI_HOTPLUG pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

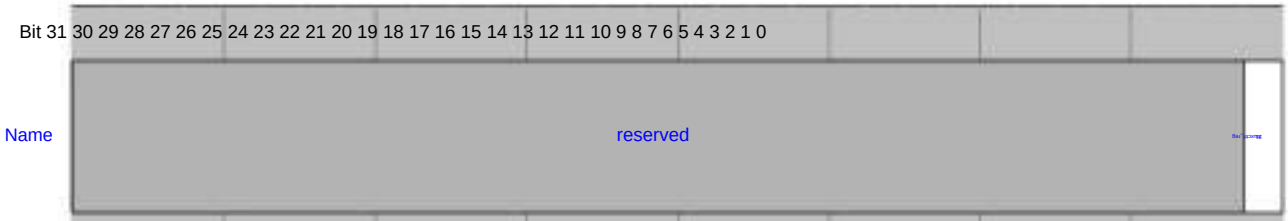
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg30	The specific multiplexing of HDMI_HOTPLUG pin. 0ÿGPIO6_4ÿ 1ÿHDMI_HOTPLUGÿ

muxctrl_reg31

HDMI_CEC pin mux control register.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

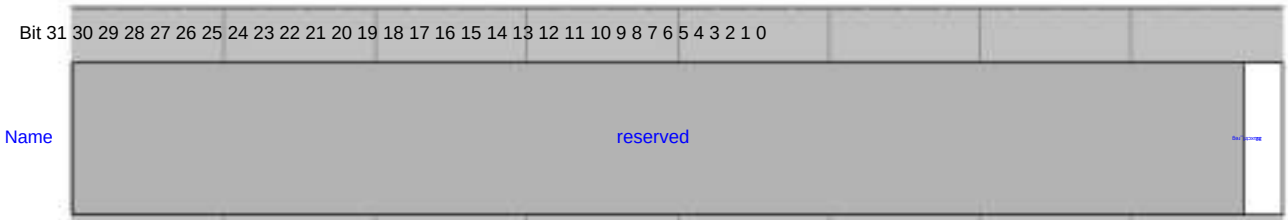


Bits	Access Name		Description
[0]	RW	muxctrl_reg31	The specific multiplexing of HDMI_CEC pin. 0ÿGPIO6_5ÿ 1ÿHDMI_CECÿ

muxctrl_reg32

HDMI_SDA pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

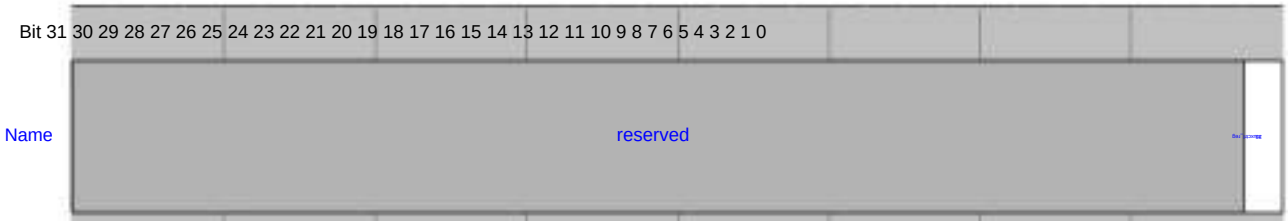


Bits	Access Name		Description
[0]	RW	muxctrl_reg32	The specific multiplexing of HDMI_SDA pin. 0ÿGPIO6_6ÿ 1ÿHDMI_SDAÿ

muxctrl_reg33

HDMI_SCL pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

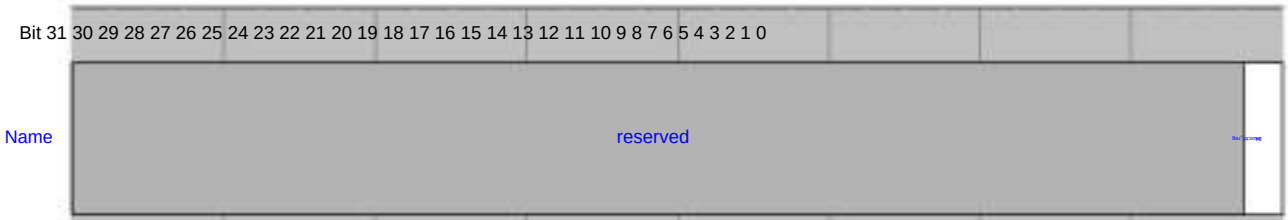


Bits	Access Name		Description
[0]	RW	muxctrl_reg33	The specific multiplexing of HDMI_SCL pin. 0ÿGPIO6_7ÿ 1ÿHDMI_SCLÿ

muxctrl_reg34

SATA_LED_N0 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

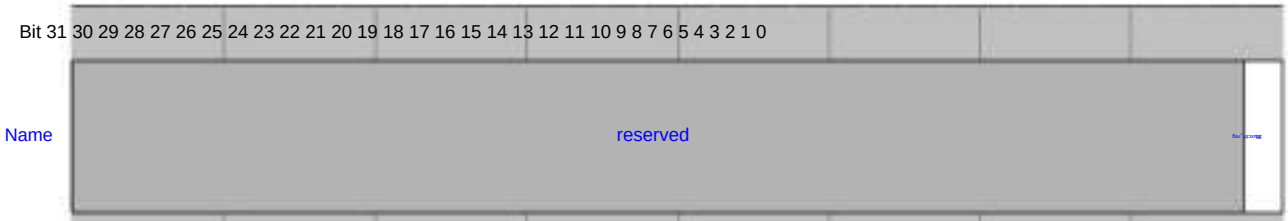


Bits	Access Name		Description
[0]	RW	muxctrl_reg34	The specific multiplexing of the SATA_LED_N0 pin. 0ÿGPIO2_1ÿ 1ÿSATA_LED_N0ÿ

muxctrl_reg35

SATA_LED_N1 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

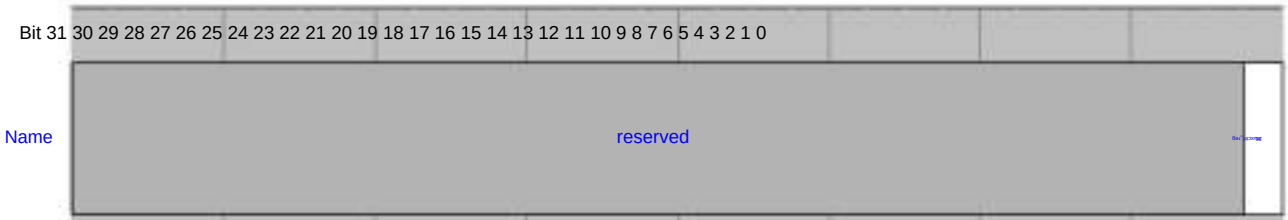


Bits	Access Name		Description
[0]	RW	muxctrl_reg35	The specific multiplexing of the SATA_LED_N1 pin. 0ÿGPIO2_2ÿ 1ÿSATA_LED_N1ÿ

muxctrl_reg36

ETH_LED1 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000



Bits	Access Name		Description
[0]	RW	muxctrl_reg36	The specific multiplexing of the ETH_LED1 pin. 0ÿGPIO5_6ÿ 1ÿETH_LED1ÿ

muxctrl_reg37

ETH_LED0 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg37	The specific multiplexing of ETH_LED0 pin. 0ÿGPIO5_7ÿ 1ÿETH_LED0ÿ

muxctrl_reg38

GPIO0_0 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg38	The specific multiplexing of GPIO0_0 pin. 0ÿGPIO0_0ÿ 1ÿRMII_CLKÿ

muxctrl_reg39

GPIO0_1 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg39	The specific multiplexing of GPIO0_1 pin. 0ÿGPIO0_1ÿ 1ÿRMII_TX_ENÿ

muxctrl_reg40

GPIO0_2 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

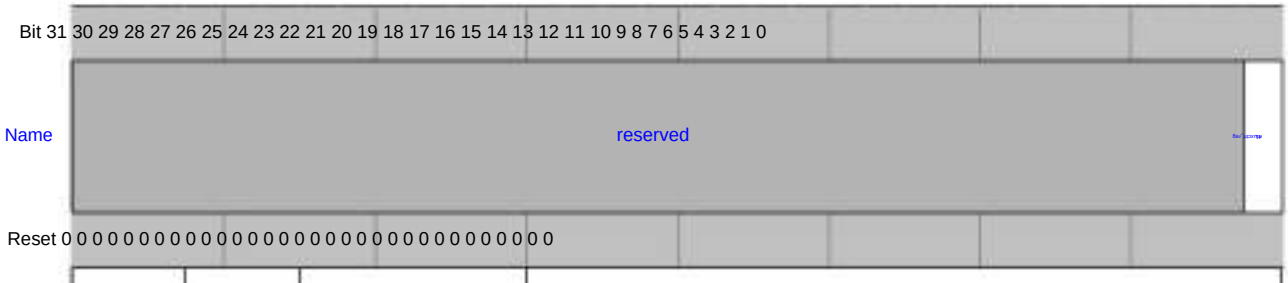
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg40	The specific multiplexing of GPIO0_2 pins. 0ÿGPIO0_2ÿ 1ÿRMII_TXD0ÿ

muxctrl_reg41

GPIO0_3 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

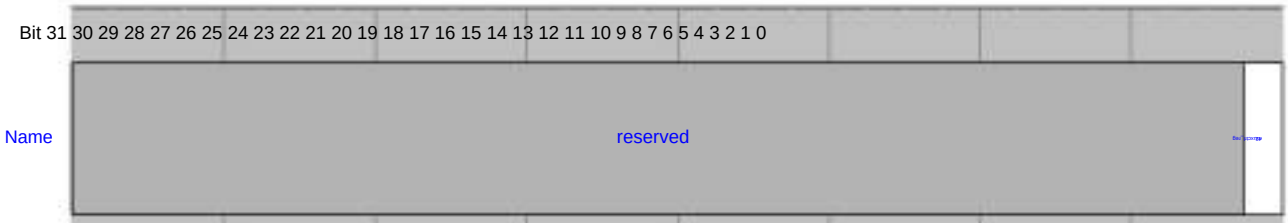


Bits	Access	Name	Description
[0]	RW	muxctrl_reg41	The specific multiplexing of GPIO0_3 pins. 0ÿGPIO0_3ÿ 1ÿRMII_TXD1ÿ

muxctrl_reg42

GPIO0_4 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000



Bits	Access	Name	Description
[0]	RW	muxctrl_reg42	The specific multiplexing of GPIO0_4 pin. 0ÿGPIO0_4ÿ 1ÿRMII_CRS_DVÿ

muxctrl_reg43

GPIO0_5 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg43	The specific multiplexing of GPIO0_5 pin. 0ÿGPIO0_5ÿ 1ÿRMII_RXD0ÿ

muxctrl_reg44

GPIO0_6 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg44	The specific multiplexing of GPIO0_6 pin. 0ÿGPIO0_6ÿ 1ÿRMII_RXD1ÿ

muxctrl_reg45

GPIO0_7 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg45	The specific multiplexing of GPIO0_7 pin. 0ÿGPIO0_7ÿ 1ÿRMII_RX_ERÿ

muxctrl_reg46

GPIO1_0 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

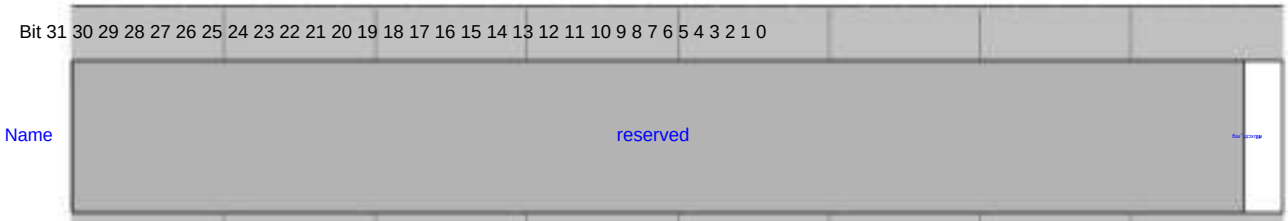
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg46	The specific multiplexing of GPIO1_0 pin. 0ÿGPIO1_0ÿ 1ÿUART3_TXDÿ

muxctrl_reg47

GPIO1_1 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

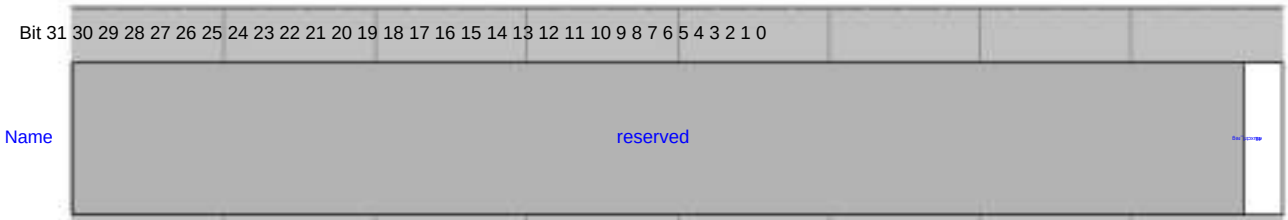


Bits	Access	Name	Description
[0]	RW	muxctrl_reg47	The specific multiplexing of GPIO1_1 pin. 0ÿGPIO1_1ÿ 1ÿUART3_RXDÿ

muxctrl_reg48

GPIO1_2 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000



Bits	Access	Name	Description
[0]	RW	muxctrl_reg48	The specific multiplexing of GPIO1_2 pins. 0ÿGPIO1_2ÿ 1ÿTEMPER_DQÿ

muxctrl_reg49

GPIO1_3 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[0]	RW muxctrl_reg49	The specific multiplexing of GPIO1_3 pins. 0ÿGPIO1_3ÿ 1ÿMDCKÿ

muxctrl_reg50

GPIO1_4 pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[0]	RW muxctrl_reg50	The specific multiplexing of GPIO1_4 pins. 0ÿGPIO1_4ÿ 1ÿAVERAGEÿ

2.4 Software Multiplexed Pins

VI_ADC

The software multiplexing pins of VI_ADC are shown in Table 2-29 .

Table 2-29 VI_ADC software multiplexing pins

Pin Pad signal		Multiplexing Control Register Multiplexing Signals		
93 VI_ADC_CLK	muxctrl_reg0	Multiplexing signal 0 GPIO8_5		
			Multiplexing signal 1	VI_ADC_CLK
			Multiplexing signal 2	CLK_TEST_OUT0
			Multiplexing signal 3	CLK_TEST_OUT1
			Multiplexing signal 4	CLK_TEST_OUT2
			Multiplexing signal 5	CLK_TEST_OUT3
			Multiplexing signal 6	RTC_TEST_CLK

The software multiplexing pins of VI_ADC are shown in Table 2-30 .

Table 2-30 VI_ADC software multiplexing pin description

Signal name	direction	illustrate
CLK_TEST_OUT0	O	Master Test Clock Output
CLK_TEST_OUT1	O	Master Test Clock Output
CLK_TEST_OUT2	O	Master Test Clock Output
CLK_TEST_OUT3	O	Master Test Clock Output
GPIO8_5	I/O	GPIO
RTC_TEST_CLK	O	RTC test clock output
VI_ADC_CLK	O	Vedio ADC working clock

VIU0

The software multiplexing pins of VIU0 are shown in Table 2-31 .

Table 2-31 Software multiplexing pins of VIU0

Pin Pad	Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	multiplexed signal 3
104	VIU0_CLK	muxctrl_reg1	VIU0_CLK	GPIO8_6	fephy_dbg_adccki	VIU0_DAT0
106	VIU0_DAT0	muxctrl_reg1	VIU0_DAT0	GPIO3_0	fephy_dbg_out0	VIU0_DAT1

Pin Pad Signal Multiplexing Control Register Multiplexing Signal 0 Multiplexing Signal 1 Multiplexing Signal 2	multiplexed signal 3
107 VIU0_DAT1 muxctrl_reg1 VIU0_DAT1 GPIO3_1 fephy_dbg_out1 VIU0_DAT2	
108 VIU0_DAT2 muxctrl_reg1 VIU0_DAT2 GPIO3_2 fephy_dbg_out2 VIU0_DAT3	
109 VIU0_DAT3 muxctrl_reg1 VIU0_DAT3 GPIO3_3 fephy_dbg_out3 VIU0_DAT4	
111 VIU0_DAT4 muxctrl_reg1 VIU0_DAT4 GPIO3_4 fephy_dbg_out4 VIU0_DAT5	
112 VIU0_DAT5 muxctrl_reg1 VIU0_DAT5 GPIO3_5 fephy_dbg_out5 VIU0_DAT6	
113 VIU0_DAT6 muxctrl_reg1 VIU0_DAT6 GPIO3_6 fephy_dbg_out6 VIU0_DAT7	
114 VIU0_DAT7 muxctrl_reg1 VIU0_DAT7 GPIO3_7 fephy_dbg_out7 VIU0_CLK	

The software multiplexing pins of VIU0 are shown in Table 2-32 .

Table 2-32 Description of software multiplexing pins of VIU0

Signal name	direction	illustrate
fephy_dbg_adccki	I	fephy debug adc clock
fephy_dbg_out0	O	fephy debug adc output
fephy_dbg_out1	O	fephy debug adc output
fephy_dbg_out2	O	fephy debug adc output
fephy_dbg_out3	O	fephy debug adc output
fephy_dbg_out4	O	fephy debug adc output
fephy_dbg_out5	O	fephy debug adc output
fephy_dbg_out6	O	fephy debug adc output
fephy_dbg_out7	O	fephy debug adc output
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO

Signal name	direction	illustrate
GPIO3_7	I/O	GPIO
GPIO8_6	I/O	GPIO
VIU0_CLK	I	Clock signal for VIU0.
VIU0_CLK	I	Clock signal for VIU0.
VIU0_DAT0	I	Data input for VIU0
VIU0_DAT0	I	Data input for VIU0
VIU0_DAT1	I	Data input for VIU0
VIU0_DAT1	I	Data input for VIU0
VIU0_DAT2	I	Data input for VIU0
VIU0_DAT2	I	Data input for VIU0
VIU0_DAT3	I	Data input for VIU0
VIU0_DAT3	I	Data input for VIU0
VIU0_DAT4	I	Data input for VIU0
VIU0_DAT4	I	Data input for VIU0
VIU0_DAT5	I	Data input for VIU0
VIU0_DAT5	I	Data input for VIU0
VIU0_DAT6	I	Data input for VIU0
VIU0_DAT6	I	Data input for VIU0
VIU0_DAT7	I	Data input for VIU0
VIU0_DAT7	I	Data input for VIU0

LIVE1

The software multiplexing pins of VIU1 are shown in Table 2-33 .

Table 2-33 The software multiplexing pins of VIU1

Pin Pad Signal Multiplexing	Control Register Multiplexing	Signal 0 Multiplexing	Signal 1 Multiplexing	Signal 2	multiplexed signal 3
94 VIU1_CLK	muxctrl_reg2	VIU1_CLK	GPIO8_7	VIU1_DAT0	-
96 VIU1_DAT0	muxctrl_reg2	VIU1_DAT0	GPIO4_0	fephy_dbg_out8 VIU1_DAT1	

Pin Pad Signal Multiplexing Control Register Multiplexing Signal 0 Multiplexing Signal 1 Multiplexing Signal 2	multiplexed signal 3
97 VIU1_DAT1 muxctrl_reg2 VIU1_DAT1 GPIO4_1 fephy_dbg_out9 VIU1_DAT2	
98 VIU1_DAT2 muxctrl_reg2 VIU1_DAT2 GPIO4_2 fephy_dbg_out10 VIU1_DAT3	
99 VIU1_DAT3 muxctrl_reg2 VIU1_DAT3 GPIO4_3 fephy_dbg_out11 VIU1_DAT4	
100 VIU1_DAT4 muxctrl_reg2 VIU1_DAT4 GPIO4_4 fephy_dbg_out12 VIU1_DAT5	
101 VIU1_DAT5 muxctrl_reg2 VIU1_DAT5 GPIO4_5 fephy_dbg_out13 VIU1_DAT6	
102 VIU1_DAT6 muxctrl_reg2 VIU1_DAT6 GPIO4_6 fephy_dbg_out14 VIU1_DAT7	
103 VIU1_DAT7 muxctrl_reg2 VIU1_DAT7 GPIO4_7 fephy_dbg_out15 VIU1_CLK	

The software multiplexing pins of VIU1 are shown in Table 2-34 .

Table 2-34 Description of the software multiplexing pins of VIU1

Signal name	direction	illustrate
fephy_dbg_out10	O	fephy debug adc output
fephy_dbg_out11	O	fephy debug adc output
fephy_dbg_out12	O	fephy debug adc output
fephy_dbg_out13	O	fephy debug adc output
fephy_dbg_out14	O	fephy debug adc output
fephy_dbg_out15	O	fephy debug adc output
fephy_dbg_out8	O	fephy debug adc output
fephy_dbg_out9	O	fephy debug adc output
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO

Signal name	direction	illustrate
GPIO8_7	I/O	GPIO
VIU1_CLK	I	Clock signal for VIU1.
VIU1_CLK	I	Clock signal for VIU1.
VIU1_DAT0	I	Data input for VIU1
VIU1_DAT0	I	Data input for VIU1
VIU1_DAT1	I	Data input for VIU1
VIU1_DAT1	I	Data input for VIU1
VIU1_DAT2	I	Data input for VIU1
VIU1_DAT2	I	Data input for VIU1
VIU1_DAT3	I	Data input for VIU1
VIU1_DAT3	I	Data input for VIU1
VIU1_DAT4	I	Data input for VIU1
VIU1_DAT4	I	Data input for VIU1
VIU1_DAT5	I	Data input for VIU1
VIU1_DAT5	I	Data input for VIU1
VIU1_DAT6	I	Data input for VIU1
VIU1_DAT6	I	Data input for VIU1
VIU1_DAT7	I	Data input for VIU1
VIU1_DAT7	I	Data input for VIU1

VGA

VGA software multiplexed pins are shown in Table 2-35 .

Table 2-35 VGA software multiplexing pins

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
129	VGA_HS	muxctrl_reg3	GPIO2_0	VGA_HS
130	VGA_VS	muxctrl_reg4	GPIO1_5	VGA_VS

Table 2-36 shows the software multiplexing pins of VGA .

Table 2-36 Description of VGA software multiplexing pins

Signal name	direction	illustrate
GPIO1_5	I/O	GPIO
GPIO2_0	I/O	GPIO
VGA_HS	O	VGA line sync output
VGA_VS	O	VGA field sync output

AIO

The AIO software multiplexing pins are shown in Table 2-37 .

Table 2-37 AIO software multiplexing pins

Pin Pad signal	Multiplexing control register	multiplexing signal 0	Multiplex signal 1	Multiplex signal 2
88 AIO_MCLK	muxctrl_reg5	AIO_MCLK	GPIO7_0	BOOT_SEL
87 AIO_BCLK_TX	muxctrl_reg6	AIO_BCLK_TX	GPIO7_1	
86 AIO_WS_TX	muxctrl_reg7	AIO_WS_TX	GPIO7_2	
85 AIO_SD_TX	muxctrl_reg8	AIO_SD_TX	GPIO7_3	JTAG_SEL
92 AIO_BCLK_RX	muxctrl_reg9	AIO_BCLK_RX	GPIO7_4	
91 AIO_WS_RX	muxctrl_reg10	AIO_WS_RX	GPIO7_5	
90 AIO_SD_RX	muxctrl_reg11	AIO_SD_RX	GPIO7_6	

The AIO software multiplexing pins are shown in Table 2-38 .

Table 2-38 AIO software multiplexing pin description

Signal name	directions	
AIO_BCLK_RX I/O		I^2S or PCM receive clock
AIO_BCLK_TX I/O		I^2S or PCM send clock
AIO_MCLK	O	I^2S or PCM interface main clock, can be used as the working clock of audio CODEC

Signal name	directions	
AIO_SD_RX	I	I²S or PCM interface data input.
AIO_SD_TX	O	I²S or PCM interface data output.
AIO_WS_RX	I/O	I²S receives the left and right channel selection signal, or PCM receives the frame synchronization signal
AIO_WS_TX	I/O	I²S sends left and right channel selection signals, or PCM sends frame synchronization signals
BOOT_SEL	I	Boot space selection: 0:SPI FLASH storage space 1:BOOTROM
GPIO7_0	I/O general purpose input and output	
GPIO7_1	I/O general purpose input and output	
GPIO7_2	I/O general purpose input and output	
GPIO7_3	I/O general purpose input and output	
GPIO7_4	I/O general purpose input and output	
GPIO7_5	I/O general purpose input and output	
GPIO7_6	I/O general purpose input and output	
JTAG_SEL	I	JTAG feature selection: 0ÿA9 1: HOURS

SPI

The SPI software multiplexing pins are shown in Table 2-39 .

Table 2-39 SPI software multiplexing pins

Pin Pad Signal Multiplexing Control Register Multiplexing Signal 0 Multiplexing Signal 1 Multiplexing Signal 2 Multiplexing Signal 3 Multiplexing Signal 4							
68	SPI_SCLK	muxctrl_reg12	GPIO8_0		SPI_SCLK	-			
69	SPI_SDO	muxctrl_reg13	PLL_TEST_OUT0	SPI_SDO	PLL_TEST_OUT1		PLL_TEST_OUT2	GPIO8_1
70	SPI_SDI	muxctrl_reg14	GPIO8_2		SPI_SDI	-			
67	SPI_CSN0	muxctrl_reg15	GPIO8_3		SPI_CSN0	-			
65	SPI_CSN1	muxctrl_reg16	GPIO8_4		SPI_CSN1	PWM_SVB	-		-

The SPI software multiplexing pins are shown in Table 2-40 .

Table 2-40 SPI software multiplexing pin description

Signal name	direction	illustrate
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
GPIO8_3	I/O	GPIO
GPIO8_4	I/O	GPIO
PLL_TEST_OUT0 O		PLL test clock output
PLL_TEST_OUT1 O		PLL test clock output
PLL_TEST_OUT2 O		PLL test clock output
PWM_SVB	O	pwm output for svb
SPI_CSN0	I/O	SPI chip select 0 output
SPI_CSN1	O	Chip select 1 output of SPI
SPI_SCLK	I/O	SPI clock signal
SPI_SDI	I	SPI data input
SPI_SDO	O	SPI data output

2C

The software multiplexed pins of I2C are shown in Table 2-41 .

Table 2-41 I2C software multiplexing pins

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
116	I2C_SDA	muxctrl_reg17	GPIO1_6	I2C_SDA
115	I2C_SCL	muxctrl_reg18	GPIO1_7	I2C_SCL

The software multiplexed pins of I2C are shown in Table 2-42 .

Table 2-42 I2C software multiplexing pin description

Signal name	direction	illustrate
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
I2C_SCL	I/O	I2C bus clock, OD output
I2C_SDA	I/O	I2C bus data/address, OD output

UART

The software multiplexing pins of UART are shown in Table 2-43 .

Table 2-43 UART software multiplexing pins

Pin Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	multiplexed signal 2
193 UART1_RTSN	muxctrl_reg19	GPIO5_0	UART1_RTSN	-
194 UART1_RXD	muxctrl_reg20	GPIO5_1	UART1_RXD	-
196 UART1_CTSN	muxctrl_reg21	GPIO5_2	UART1_CTSN	PWM_SVB
198 UART1_TXD	muxctrl_reg22	GPIO5_3	UART1_TXD	-
199 UART2_RXD	muxctrl_reg23	GPIO5_4	UART2_RXD	-
200 UART2_TXD	muxctrl_reg24	GPIO5_5	UART2_TXD	-

The software multiplexing pins of UART are shown in Table 2-44 .

Table 2-44 UART software multiplexing pin description

Signal name	directions	
GPIO5_0	I/O general purpose input and output	
GPIO5_1	I/O general purpose input and output	
GPIO5_2	I/O general purpose input and output	
GPIO5_3	I/O general purpose input and output	
GPIO5_4	I/O general purpose input and output	
GPIO5_5	I/O general purpose input and output	

Signal name	directions	
PWM_SVB	O	pwm output for svb
UART1_CTSN	I	Modem status input: Clear To Send. Low effective.
UART1_RTSN	O	Modem status output: request to send, low effective. Reset value is 0
UART1_RXD	I	UART1 data reception
UART1_TXD	O	UART1 data transmission
UART2_RXD	I	UART0 data reception
UART2_TXD	O	UART0 data transmission

AND

The software multiplexing pins of IR are shown in Table 2-45 .

Table 2-45 IR software multiplexing pins

Pin	Pad signal multiplex	control register multiplex signal 0 multiplex signal 1		
29	IR_IN	muxctrl_reg25	GPIO7_7	IR_IN

The software multiplexing pins of IR are shown in Table 2-46 .

Table 2-46 IR software multiplexing pin description

Signal name	direction	illustrate
GPIO7_7	I/O	GPIO
IR_IN	I	Infrared input

USB

The USB software multiplexing pins are shown in Table 2-47 .

Table 2-47 USB software multiplexing pins

Pin	Pad signal	Multiplexing Control Register Multiplexing Signal 0 Multiplexing Signal 1		
173 USB0_OVRCUR		muxctrl_reg26	GPIO6_0	USB0_OVRCUR

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
174	USB0_PWREN	muxctrl_reg27	GPIO6_1	USB0_PWREN
175	USB1_OVRCUR	muxctrl_reg28	GPIO6_2	USB1_OVRCUR
176	USB1_PWREN	muxctrl_reg29	GPIO6_3	USB1_PWREN

The USB software multiplexing pins are shown in Table 2-48 .

Table 2-48 USB software multiplexing pin description

Signal name	direction	illustrate
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
GPIO6_2	I/O	GPIO
GPIO6_3	I/O	GPIO
USB0_OVRCUR I		The port overcurrent indication signal of USB port 0, high and low levels can be configured, and the default is high level active
USB0_PWREN	O	USB port 0 power control output pin, high and low level can be configured, the default is low level active
USB1_OVRCUR I		Port overcurrent indication signal of USB port 1, high and low levels can be configured, and the default is high level active
USB1_PWREN	O	USB port 1 power control output pin, high and low level can be configured, the default is low level active

HDMI

HDMI software multiplexing pins are shown in Table 2-49 .

Table 2-49 HDMI software multiplexing pins

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
131	HDMI_HOTPLUG	muxctrl_reg30	GPIO6_4	HDMI_HOTPLUG
135	HDMI_CEC	muxctrl_reg31	GPIO6_5	HDMI_CEC
133	HDMI_SDA	muxctrl_reg32	GPIO6_6	HDMI_SDA

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
134	HDMI_SCL	muxctrl_reg33	GPIO6_7	HDMI_SCL

HDMI software multiplexing pins are shown in Table 2-50 .

Table 2-50 HDMI software multiplexing pin description

Signal name	direction	illustrate
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO
HDMI_CEC	I/O	Control channel signal for HDMI interface
HDMI_HOTPLUG I		Hot plug signal for HDMI interface
HDMI_SCL	I/O	HDMI I2C bus clock, OD output
HDMI_SDA	I/O	HDMI I2C bus data/address, OD output

HOURS

The SATA software multiplexing pins are shown in Table 2-51 .

Table 2-51 SATA software multiplexing pins

Pin	Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
30	SATA_LED_N0	muxctrl_reg34	GPIO2_1	SATA_LED_N0
31	SATA_LED_N1	muxctrl_reg35	GPIO2_2	SATA_LED_N1

The SATA software multiplexing pins are shown in Table 2-52 .

Table 2-52 SATA software multiplexing pin description

Signal name	direction	illustrate
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO

Signal name	direction	illustrate
SATA_LED_N0	O	SATA0 port LED indication, low effective
SATA_LED_N1	O	SATA1 port LED indication, low effective

ETH

The software multiplexing pins of ETH are shown in Table 2-53 .

Table 2-53 Software multiplexing pins of ETH

Pin Pad signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
171 ETH_LED1	muxctrl_reg36	GPIO5_6	ETH_LED1
172 ETH_LED0	muxctrl_reg37	GPIO5_7	ETH_LED0

The software multiplexing pins of ETH are shown in Table 2-54 .

Table 2-54 ETH software multiplexing pin description

Signal name	directions	
ETH_LED1	O	Fephy status LED1, under the initial configuration, this light will be on when the connection is successful. (Note: The function of this **LED** can be customized by the user, please refer to the **FEPHY** description chapter for specific operations)
ETH_LED0	O	fephy status LED0, under initial configuration, this light will blink when data is being transmitted. (Note: The function of this **LED** can be customized by the user, please refer to the **FEPHY** description chapter for specific operations)
GPIO5_6	I/O general purpose input and output	
GPIO5_7	I/O general purpose input and output	

GPIO

The software multiplexed pins of GPIO are shown in Table 2-55 .

Table 2-55 GPIO software multiplexing pins

Pin	Pad signal	multiplexing control register	Multiplexing signal 0	Multiplexing signal 1
186	GPIO0_0	muxctrl_reg38	GPIO0_0	RMII_CLK

Pin	Pad signal	multiplexing control register	Multiplexing signal 0	Multiplexing signal 1
182	GPIO0_1	muxctrl_reg39	GPIO0_1	RMII_TX_EN
185	GPIO0_2	muxctrl_reg40	GPIO0_2	RMII_TXD0
183	GPIO0_3	muxctrl_reg41	GPIO0_3	RMII_TXD1
179	GPIO0_4	muxctrl_reg42	GPIO0_4	RMII_CRS_DV
189	GPIO0_5	muxctrl_reg43	GPIO0_5	RMII_RXD0
188	GPIO0_6	muxctrl_reg44	GPIO0_6	RMII_RXD1
178	GPIO0_7	muxctrl_reg45	GPIO0_7	RMII_RX_ER
27	GPIO1_0	muxctrl_reg46	GPIO1_0	UART3_TXD
28	GPIO1_1	muxctrl_reg47	GPIO1_1	UART3_RXD
72	GPIO1_2	muxctrl_reg48	GPIO1_2	TEMPER_DQ
181	GPIO1_3	muxctrl_reg49	GPIO1_3	MDCK
180	GPIO1_4	muxctrl_reg50	GPIO1_4	MEDIUM

The software multiplexed pins of GPIO are shown in Table 2-56 .

Table 2-56 GPIO software multiplexing pin description

Signal name	direction	illustrate
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
GPIO0_3	I/O	GPIO
GPIO0_4	I/O	GPIO
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
GPIO1_0	I/O	GPIO
GPIO1_1	I/O	GPIO

Signal name	direction	illustrate
GPIO1_2	I/O	GPIO
GPIO1_3	I/O	GPIO
GPIO1_4	I/O	GPIO
MDCK	O	MDIO0 interface clock output
MEDIUM	I/O	Input/output signal of MDIO0 interface
RMII_CLK	I/O	RMII interface clock
RMII_CRS_DV	I	RMII receive data valid and carrier detection
RMII_RX_ER	I	RMII receive error, indicating that the received data is wrong and the mac can discard it
RMII_RXD0	I	RMII receive data
RMII_RXD1	I	RMII receive data
RMII_TX_EN	O	RMII send enable, indicating that the data sent is valid when the signal is valid
RMII_TXD0	O	RMII send data
RMII_TXD1	O	RMII send data
TEMPER_DQ	I/O	Temperature acquisition, used to communicate with external temperature acquisition chip.
UART3_RXD	I	UART3 data reception
UART3_TXD	O	UART3 data transmission

2.5 Hardware pin multiplexing

SFC pin multiplexing

The multiplexing of SFC pins is shown in Table 2-57 .

Table 2-57 SFC hardware pin multiplexing

Pin	Pad signal	Multiplexing signal 1 (power_on == 1'b1)
58	SFC_CLK	SFC_ADDR_MODE

The hardware multiplexing pins of SFC are shown in Table 2-58 .

Table 2-58 Description of pins multiplexed with SFC

Signal name	direction	illustrate
SFC_ADDR_MODE I		sfc 3byte/4byte address mode selection: 0ÿ3byte 1ÿ4byte

JTAG pin multiplexing

The multiplexing of JTAG pins is shown in Table 2-59 .

Table 2-59 JTAG hardware pin multiplexing

Pin	Pad signal	multiplexing signal 1 (jtag_enable == 1'b0)
25	JTAG_TRSTN	GPIO2_3
21	JTAG_TCK	GPIO2_4
22	JTAG_TMS	GPIO2_5
20	JTAG_TDO	GPIO2_6
23	JTAG_TDI	GPIO2_7

The hardware multiplexing pins of JTAG are shown in Table 2-60 .

Table 2-60 Description of pins multiplexed with JTAG

Signal name	direction	illustrate
JTAG_TRSTN	I	JTAG reset input
JTAG_TCK	I	JTAG clock input
JTAG_TMS	I/O	JTAG mode select input, or data output for software trace. Two mode selections are controlled in the CPU
JTAG_TDO	O	JTAG data output
JTAG_TDI	I	JTAG data input

2.6 Electrical performance parameters

2.6.1 Power Consumption Parameters

The power consumption parameters of Hi3520D and Hi3515A are shown in Table 2-61 and Table 2-62 .

注意

The power consumption parameters are based on the typical working scenarios of the chip. The design of single-board power supply must refer to the hardware design guideline.

Table 2-61 Hi3520D power consumption parameters

symbol	parameter	Typical Value	Maximum	Unit
core power	core power	1200	1500	mA
3.3V power supply	Interface power	220	400	mA
1.5V power supply	DDR interface power supply	140	250	mA

Table 2-62 Hi3515A power consumption parameters

symbol	parameter	Typical Value	Maximum	Unit
core power	core power	1100	1300	mA
3.3V power supply	Interface power	210	400	mA
1.5V power supply	DDR interface power supply	130	250	mA

2.6.2 Temperature and Thermal Resistance Parameters

The temperature and thermal resistance parameters are shown in Table 2-63 .

说明

The thermal resistance is given based on the JEDEC JESD51-2 standard. The system design and environment of the application may be different from the JEDEC JESD51-2 standard, and it needs to be analyzed according to the application conditions. The chip junction temperature is directly

proportional to the chip power consumption. It is necessary to consider controlling the chip junction temperature within a reasonable range to match the power supply specification.

For heat dissipation design, please refer to the hardware design guide

Table 2-63 Temperature and thermal resistance parameters

parameter	Symbol	Min	Typ	Max	Unit
ambient temperature	FACING	0	·	70	ÿ
Limit junction temperature	TJMAX	–20	·	105	ÿ
Junction-to-ambient thermal resistance ÿJA		·	19	·	ÿ/W
Junction-to-board thermal resistance	ÿJB	·	10	·	ÿ/W
Junction-to-case thermal resistance	ÿJC	·	6	-	ÿ/W

2.6.3 Working conditions

The working conditions of the Hi3520D are shown in Table 2-64 .

Table 2-64 Working conditions

symbol	describe	Min	Typ	Max	Unit
DVDD12	core power	1.2	1.25	1.3	IN
DVDD33	I/O power supply	2.97	3.3	3.63	IN
DDR_VDDQ	DDR2 I/O Power 1.7		1.8	1.9	IN
	DDR3 I/O Power 1.425		1.5	1.575	IN
AVDD12_PLL	PLL Analog Power 1.2		1.25	1.3	IN
AVDD33_PLL	PLL Analog Power 2.97		3.3	3.63	IN
AVDD12_SATA	SATA analog power supply 1.2		1.25	1.3	IN
AVDD33_SATA	SATA analog power supply 2.97		3.3	3.63	IN
AVDD12_HDMI	HDMI Analog Power 1.2		1.25	1.3	IN
AVDD33_VDAC	VDAC Analog Power 2.97		3.3	3.63	IN
AVDD12_FE	FE Analog Power 1.2		1.25	1.3	IN
AVDD33_FE	FE Analog Power 2.97		3.3	3.63	IN

symbol	describe	Min Typ Max Unit			
AVDD33_USB AVDD33_USB0 AVDD33_USB1	USB Analog Power 3.201		3.3	3.63	IN
AVDD_BAT	RTC Battery Power 1.6		3.0	3.0	IN
AVDD33_RTC RTC analog	power supply 2.97		3.3	3.63	IN

2.6.4 Power on and off sequence

Please refer to "Hi3520D/Hi3515A Hardware Design User Guide".

2.6.5 DC/AC electrical parameters

Hi3520D DC electrical parameters are listed in Table 2-65 .

Table 2-65 DC electrical parameter list (DVDD33ÿ3.3V, some interfaces are compatible with 5V input)

symbol	parameter	minimum value	typical value	maximum value	unit	illustrate
DVDD12 core voltage		1.2	1.25	1.3 V		
DVDD33 interface voltage		2.97	3.3	3.63 V -		
HIV	High level input voltage 2.0			Some 5.5 V interfaces		support 5V input, and the maximum input requirement is not higher than 5.5V, including GPIO1_0/ GPIO1_1/IR_IN/ SATA_LED/ I2C/HDMI control interface/ UART0 interface, etc.
WILL	Low level input voltage – 0.3			0.8 V -		
THE	Input Leakage Current-			±1	µA -	
IOZ	Three-State Output Leakage Current-			±1	µA -	
VOH	High level output voltage 2.4				IN -	
VOL	Low Level Output Voltage -			0.4 V -		
RPUs	Internal pull-up resistor 33		41	62	kÿ	driving non-adjustable IO
RPD	Internal pull-down resistor 33		42	68	kÿ	driving non-adjustable IO
RPU_progamio drive	adjustable IO internal pull-up resistor	59.8	74.5	112 kÿ	drives	adjustable IOs including AIO, SPI, and VGA etc.
RPD_progamio drive	adjustable IO internal pull-down resistor	57	71.6	118 kÿ	drives	adjustable IOs including AIO, SPI, and VGA etc.

symbol	parameter	minimum value	typical value	maximum value	unit	illustrate
RPU_5k_progamio	drive adjustable IO low internal pull-up resistor	3	5	7	kÿ	drives adjustable IOs, including AIO, SPI, and VGA etc.
RPD_5k_progamio	drive adjustable IO low internal pull-down resistor	3	5	7	kÿ	drives adjustable IOs, including AIO, SPI, and VGA etc.

In DDR2 mode, the DC electrical parameters are shown in Table 2-66 .

Table 2-66 DC electrical parameter table (DDR_VDDQ =1.8V, DDR2 SSTL18 mode)

symbol	parameter	Min Typ Max			unit description	
DDR_VDDQ	interface voltage	1.7	1.8	1.9	IN -	
Vref	reference voltage	833	900	969	mV ÿ0.49~0.51ÿx DVDD1518	
MTB	Termination voltage	Vref-40	Vref	Vref+40	mV -	
VIH(DC) high level input voltage		Vref+0.125	-	DDR_VDDQ+0.3	V -	
VIL(DC) low level input voltage		– 0.3		Vref-0.125	IN -	
John	High level output current	8			mA	drive configurable
IOL	Low level output current	|–8|			mA	drive configurable

In DDR2 mode, AC electrical parameters are shown in Table 2-67 .

Table 2-67 AC electrical parameter table (DDR_VDDQ =1.8V, DDR2 mode)

Symbolic parameters		400ÿ533 Mbps		667ÿ800 Mbps		unit description	
		minimum value	maximum value	minimum value	maximum value		
VIH(AC) AC high level input voltage		Vref + 0.25	-	Vref+0.2	-	IN -	
VIL(AC) AC low level input voltage		-	Vref–0.25	-	Vref–0.2	IN	-

In DDR3 mode, the DC electrical parameters are shown in Table 2-68 .

Table 2-68 DC electrical parameter table (DDR_VDDQ =1.5V, DDR3 mode)

symbol	parameter	minimum value	Typical Max.		unit description	
DDR_VDD Q	interface voltage	1.425	1.5	1.575	IN	-
Vref	reference voltage	698	750	803	mV ÿ0.49~0.51ÿ x DDR_DVDD IO	
MTB	Termination voltage	698	750	803	mV -	
VIH (DC) high level input voltage Vref+0.1			-	DDR_VDDQ+0. 3	IN	-
VIL(DC) low level input voltage – 0.3			-	Vref–0.1	IN	-
John	High level output current |8|		-	-	mA drive configurable	
IOL	Low level output current |–8|		-	-	mA drive configurable	

In DDR3 mode, AC electrical parameters are shown in Table 2-69 .

Table 2-69 AC electrical parameter table (DDR_VDDQ =1.5V, DDR3 mode)

Symbolic parameters		minimum value	maximum value	unit description	
VIH(AC) high level input voltage Vref + 0.175			DDR_VDDQ +0.3	IN	-
VIL(AC) low level input voltage-			Vref–0.175	IN	-

2.7 PCB Design Recommendations

For details of PCB design, please refer to "Hi3520D Hardware Design User Guide".

2.8 Interface Timing

2.8.1 DDR Interface Timing

2.8.1.1 Write Operation Timing

Write operation timing of dqs_out relative to dq_out

The main timing parameters for the write timing of dqs_out relative to dq_out are tDS and tDH. In DDR2-800, tDS and tDH are 0.05ns and 0.125ns respectively.

Figure 2-8 The write operation timing diagram of dqs_out relative to dq_out in DDR2

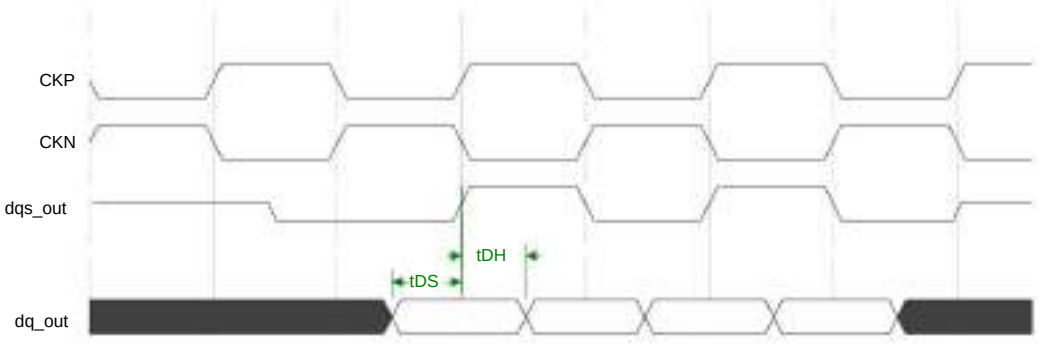
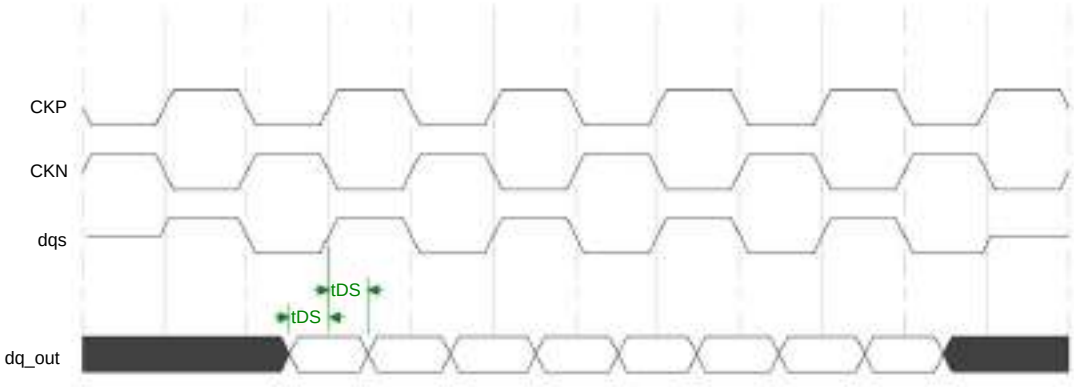


Figure 2-9 The write operation timing diagram of dqs_out relative to dq_out in DDR3



The write operation timing of dqs_out relative to ck

The write operation timing of dqs_out relative to ck. The timing of DDR2 and DDR3 is shown in Figure 2-10 and Figure 2-11 .

Figure 2-10 Timing diagram of write operation of dqs_out relative to ck in DDR2

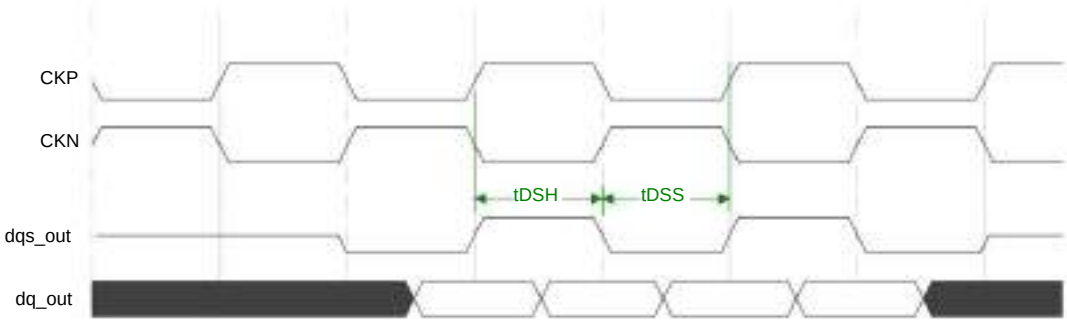
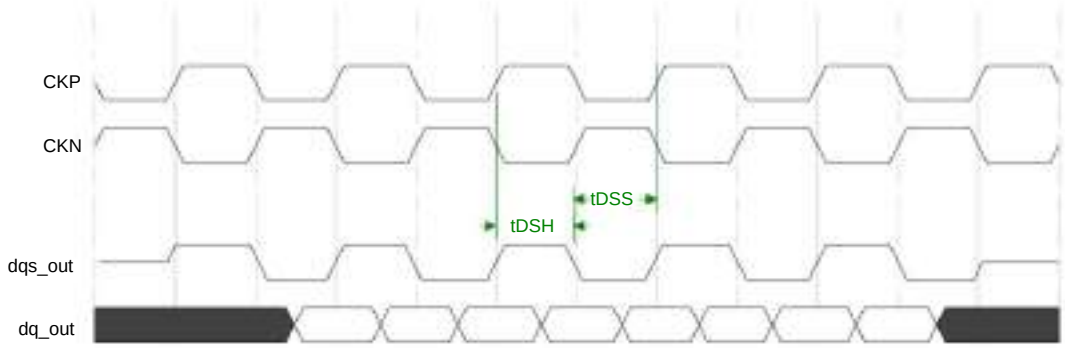


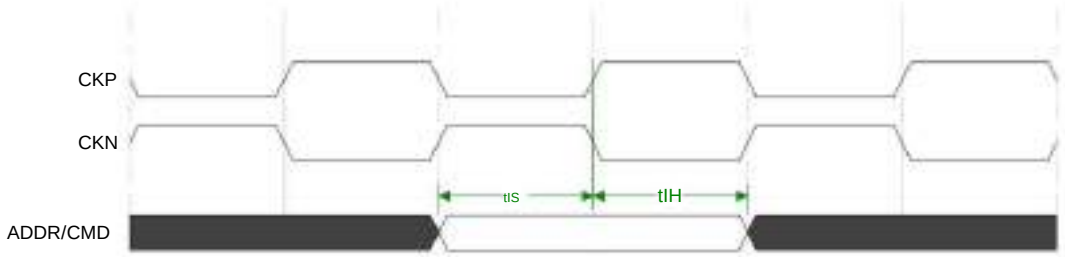
Figure 2-11 Timing diagram of write operation of dqs_out relative to ck in DDR3



Command and address write timing relative to ck

The write operation timing of commands and addresses relative to ck is shown in Figure 2-12 .

Figure 2-12 Timing diagram of write operation of command and address relative to ck



2.8.1.2 Read Operation Timing

Command and address read timing relative to ck

"Command and address read operation timing relative to ck" is the same as "command and address write operation timing relative to ck " .

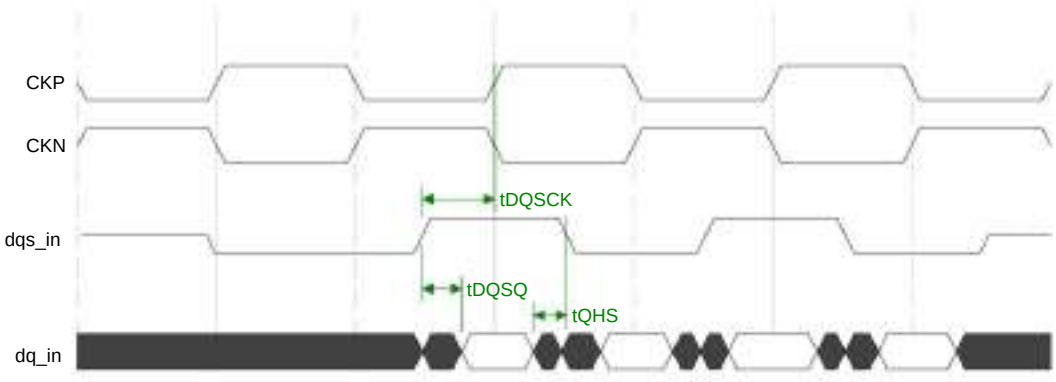
Read operation timing of dqs_in relative to dq_in

The read operation timing of dqs_in relative to dq_in is divided into DDRn SDRAM output timing and DDRPHY terminal dqs_in and dq_in timing.

For DDR SDRAM output timing, ideally, DQS and ck are in the same phase, but in reality, DQS has a skew of tDQSCK relative to CK. tDQSCK is 0.35ns. tDQSQ is the jitter between dq and dqs, it is the jitter of the latest effective dq relative to dqs, the value is 0.2ns, tQHS is the jitter of the earliest effective dq relative to dqs, its value is 0.3ns.

DDRn SDRAM output timing is shown in Figure 2-13 .

Figure 2-13 DDRn SDRAM output timing diagram



2.8.1.3 Timing parameters

The timing of the DDR interface meets the standard protocol of JEDEC (JESD79-2E and JESD79-3B). The timing described in this article is the timing of the output of the DDR PHY side.

For Hi3520D, it is based on the timing parameters of DDR2-800 and DDR3-1066.

DDR2-800 SDRAM clock parameters are shown in Table 2-70 and Table 2-71 .

DDR3-1066 SDRAM clock parameters are shown in Table 2-72 and Table 2-73 .

Table 2-70 DDR2 Clock Parameters

parameter	typical unit	
memory clock frequency	400.00	MHz
PLL Jitter	0.200	ns
PLL duty cycle	48.000 %	
clock skew	0.100	ns

The DDR2 SDRAM memory parameters are shown in Table 2-71 .

Table 2-71 DDR2 SDRAM memory parameter list (DDR2-800)

parameter	Symbol Typical	Value Unit	
DQS falling edge relative to DDR clock setup time	tDSS	0.2	TCK
DQS falling edge hold time relative to DDR clock	tDSH	0.2	TCK
DQ/DM setup time relative to DQS	tDS	0.050	ns
DQ/DM hold time relative to DQS	tDH	0.125	ns
Skew of DQS and DQ	tDQSQ 0.200		ns

parameter	Symbol Typical	Value Unit	
data retention skew	tQHS	0.300	ns
Address and command setup time relative to DDR clock	tIS	0.175	ns
Address and command hold time relative to DDR clock	tIH	0.250	ns
Skew relative to DDR clock at DQS output	tDQSCK 0.350		ns

Note: Some timing parameters can be found in the following timing diagrams.

Table 2-72 DDR3 clock parameter list

parameter	typical value	unit
memory clock frequency	660.00	MHz
PLL Jitter	0.200	ns
PLL duty cycle	47.000	%
clock skew	0.100	ns

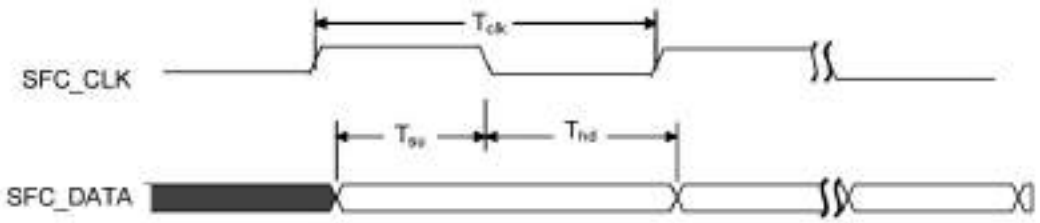
Table 2-73 DDR3 SDRAM memory parameter table (DDR3-1066)

parameter	Symbol Typical	Value Unit	
DQS falling edge relative to DDR clock setup time	tDSS	0.2	TCK
DQS falling edge hold time relative to DDR clock	tDSH	0.2	TCK
DQ/DM setup time relative to DQS	tDS	0.025	ns
DQ/DM hold time relative to DQS	tDH	0.100	ns
Skew of DQS and DQ	tDQSQ 0.150		ns
Address and command setup time relative to DDR clock	tIS	0.125	ns
Address and command hold time relative to DDR clock	tIH	0.200	ns
Skew relative to DDR clock at DQS output	tDQSCK 0.300		ns

2.8.2 SFC Interface Timing

The timing sequence of SFC input direction is shown in Figure 2-14 .

Figure 2-14 Timing diagram of SFC input direction



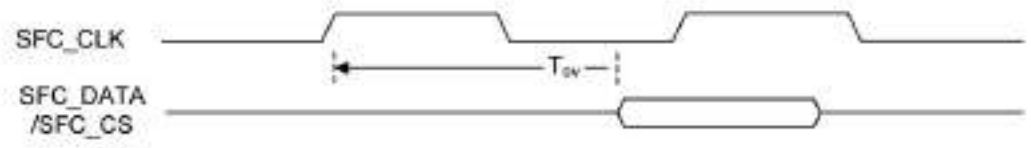
The timing parameters of the SFC input direction are shown in Table 2-74 .

Table 2-74 SFC Input Direction Timing Parameters

parameter	Symbol	Min	Typ	Max	Unit
SFC_CLK clock period Tclk		16		83.2	ns
Input signal settling time requirement Tsu		8			ns
Input signal hold time requirement Thd		1.2			ns

The timing sequence of SFC output direction is shown in Figure 2-15 .

Figure 2-15 SFC output direction timing diagram



The timing parameters of the SFC output direction are shown in Table 2-75 .

Table 2-75 SFC output direction timing parameter table

parameter	Symbol	Min	Typ	Max	Unit
SFCCLK clock period	T	16		83.2	ns
Output data signal delay	Mix	-5		3.0	ns
Output chip select signal delay	Mix	-5	-	3.0	ns

2.8.3 Ethernet MAC Interface Timing

2.8.3.1 RMII Interface Timing

Figure 2-16 shows the 100Mbit/s receiving timing of the RMII interface .

Figure 2-16 RMII interface 100Mbit/s receiving timing

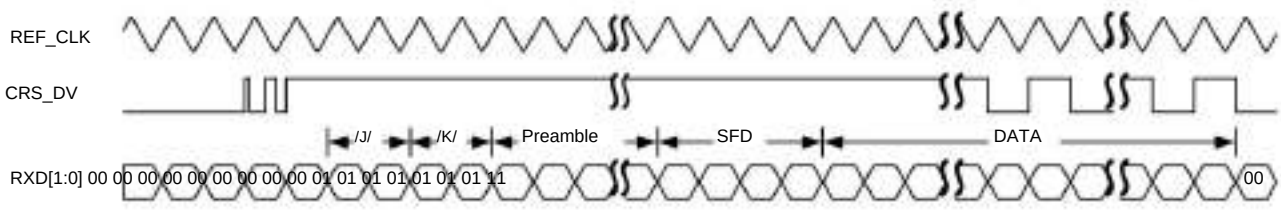


Figure 2-17 shows the 100Mbit/s transmission timing of the RMII interface .

Figure 2-17 RMII interface 100Mbit/s sending timing

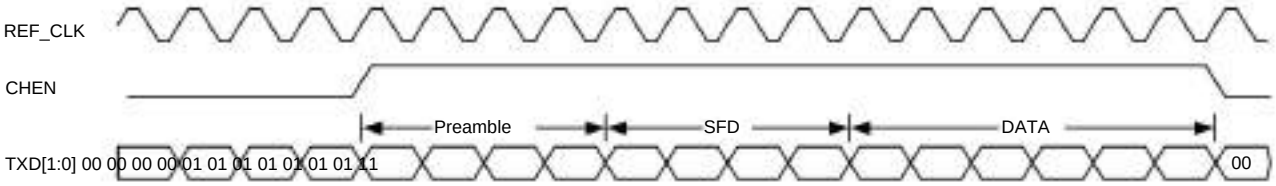


Figure 2-18 shows the 10Mbit/s receiving timing of the RMII interface .

Figure 2-18 RMII interface 10Mbit/s receiving timing

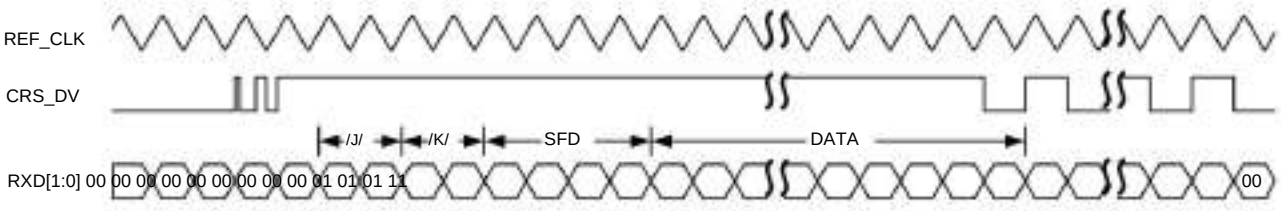
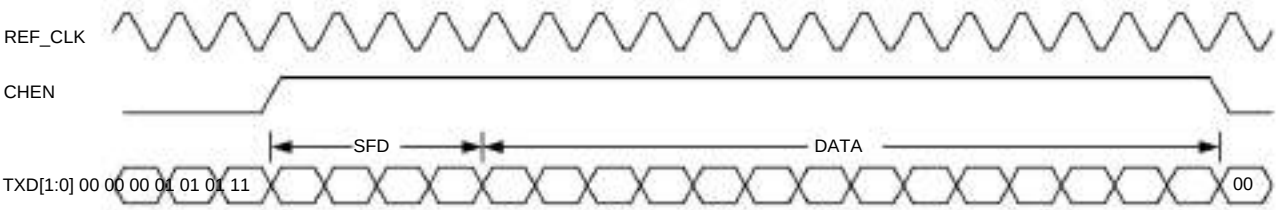


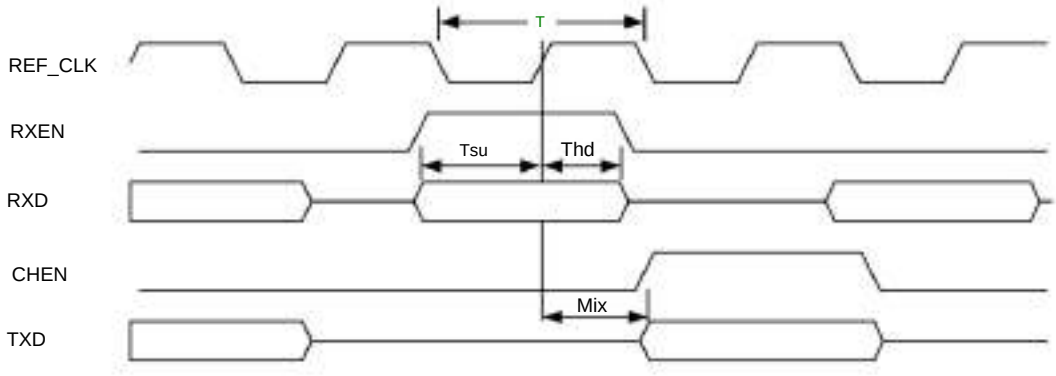
Figure 2-19 shows the 10Mbit/s transmission timing of the RMII interface .

Figure 2-19 RMII interface 10Mbit/s sending timing



The timing parameters of the RMII interface are shown in Figure 2-20 .

Figure 2-20 RMII interface timing parameters



The timing parameters of the RMII interface are shown in Table 2-76 .

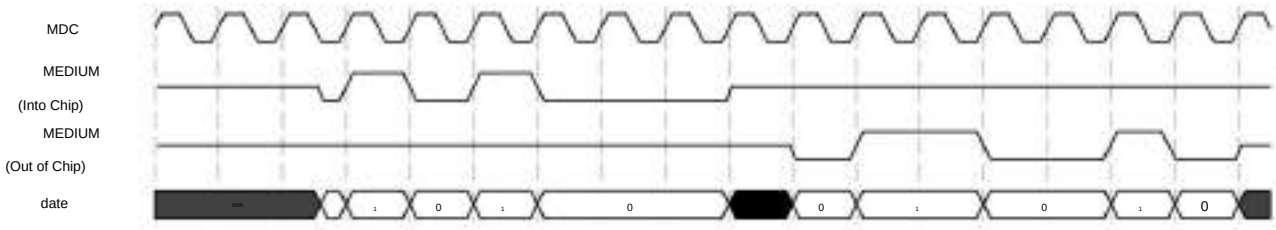
Table 2-76 RMII interface timing parameter description

parameter	symbol	Signal	min max unit		
RMII signal setup time Tsu(RX)		CRS_DV/RXD[1:0] 4			ns
RMII signal hold time Thd (RX)		CRS_DV/RXD[1:0] 2			ns
RMII output signal delay Tov	ÿRMITXÿ	TXEN/TXD[1:0]	2	16	ns

2.8.3.2 MDIO Interface Timing

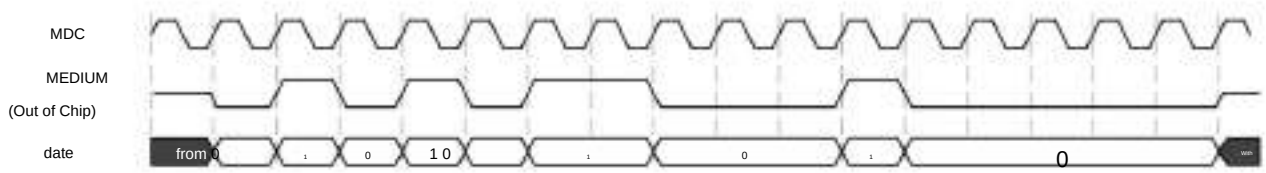
MDIO interface read timing is shown in Figure 2-21 .

Figure 2-21 MDIO interface read timing



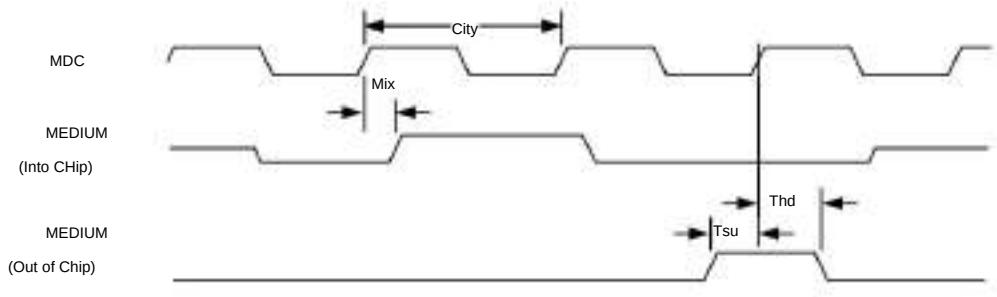
The write sequence of MDIO interface is shown in Figure 2-22 .

Figure 2-22 MDIO interface write timing



The timing parameters of the MDIO interface are shown in Figure 2-23 .

Figure 2-23 MDIO interface receiving timing parameters



The timing parameters of the MDIO interface are described in Table 2-77 .

Table 2-77 MDIO interface timing parameters

parameter	Symbol Signal Min Max Unit				
MDIO receive data delay time Tov MDIO			0	300	ns
MDIO clock cycle	Tp MDCK 92.5			7407	ns
MDIO send data setup time Tsu MDIO			10		ns
MDIO send data hold time Thd MDIO			10	-	ns

Note: The MDC clock period Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]), and choose the frequency division of the Ethernet working clock by 100, 50 or other frequency divisions. Tov is 5 working clock cycles.

2.8.4 VI Interface Timing

The VI clock is provided externally. When the VI works in slave mode, all of them are input interfaces.

The timing sequence of the VI interface is shown in Figure 2-24 .

Figure 2-24 Timing diagram of VI interface

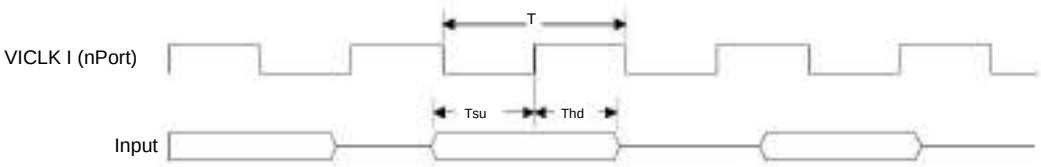


Table 2-78 lists the timing parameters of the VI interface .

Table 2-78 Timing parameter list of VI interface

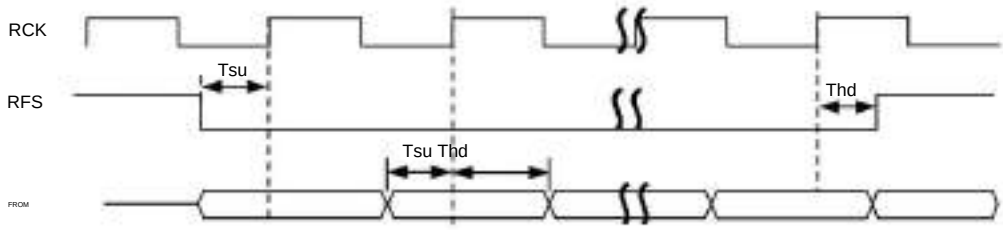
parameter	Symbol	Min	Typ	Max	Unit
VICLK clock period	T		6.74		ns
Input Signal Settling Time Requirements	Tsu	1.5			ns
Input Signal Hold Time Requirements	Thd	1.0		-	ns

2.8.5 AIO Interface Timing

2.8.5.1 I2S interface timing

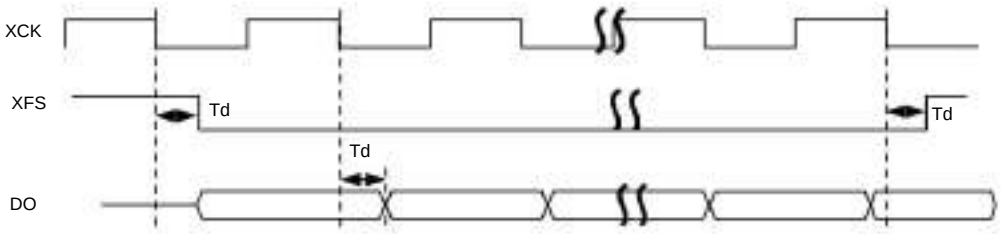
I 2 Figure 2-25 shows the receiving sequence of the S interface.

Figure 2-25 I 2 S interface receiving timing diagram



I 2 Figure 2-26 shows the sending sequence of the S interface.

Figure 2-26 I 2 S interface sending timing diagram



I 2 Table 2-79 lists the timing parameters of the S interface .

Table 2-79I 2 S interface timing parameter table

parameter	Symbol Min Typ Max Unit				
Input signal settling time	Tsu	10			ns
Input signal hold time	Thd	10			ns
output signal delay	Td	0	-	8	ns

2.8.5.2 PCM Mode Interface Timing

Figure 2-27 shows the receiving timing of the PCM interface.

Figure 2-27 PCM interface receiving timing diagram

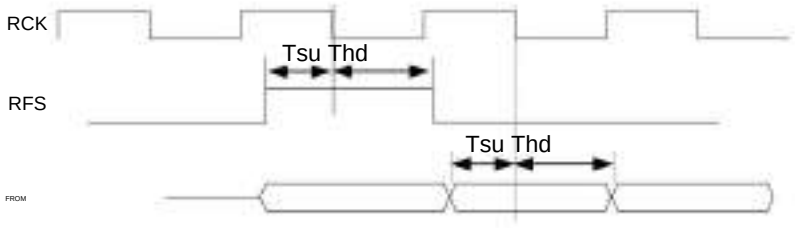


Figure 2-28 shows the sending sequence of the PCM interface.

Figure 2-28 PCM interface sending timing diagram

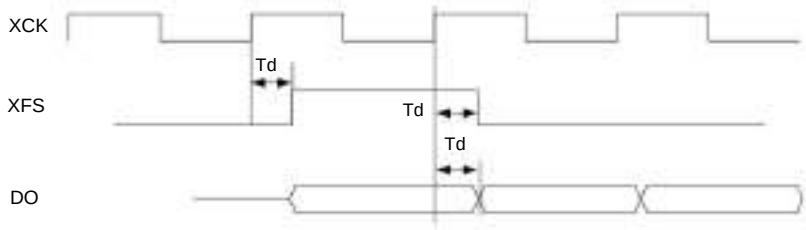


Table 2-80 lists the timing parameters of the PCM interface .

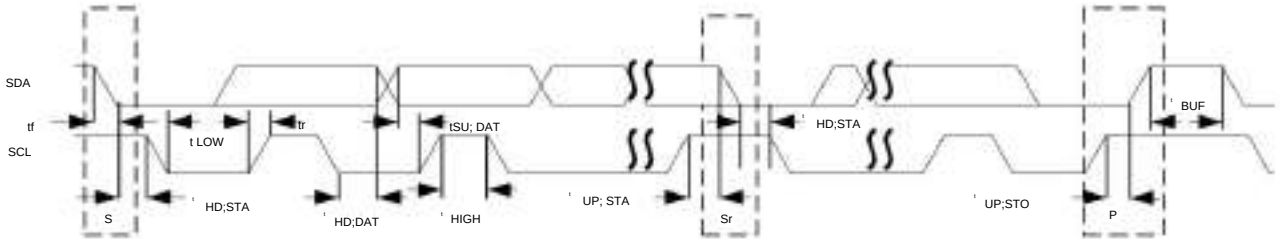
Table 2-80 PCM interface timing parameter table

parameter	Symbol Min Typ Max Unit				
Input signal settling time	Tsu	10			ns
Input signal hold time	Thd	10			ns
output signal delay	Td	0	-	8	ns

2.8.6 I2C Timing

I 2 C The transmission timing is shown in Figure 2-29 .

picture 2-29 I 2 C Transmission Timing Diagram



I 2 The timing parameters of the C interface are shown in Table 2-81 .

Table 2-81I 2 C interface timing parameter table

parameter	symbol	standard mode		fast mode		unit
		min max min max				
SCL clock frequency	fSCL	0	100	0	400	kHz
Start hold time	tHD;STA	4.0	·	0.6	·	ÿs
SCL low period	tLOW	4.7	·	1.3	·	ÿs
SCL high level period	tHIGH	4.0	·	0.6	·	ÿs
boot build time	tSU;STA	4.7	·	0.6	·	ÿs
data hold time	tHD;DAT 0		3.45	0	0.9	ÿs
data creation time	tSU; DAT	250	·	100	·	ns
SDA, SCL rise time tr		·	1000	20+0.1Cb 300		ns
SDA, SCL fall time tf		·	300	20+0.1Cb 300		ns
end build time	tSU;STO	4.0	·	0.6	·	ÿs
Bus release time between start and end	tBUF	4.7	·	1.3	·	ÿs
bus load	Cb	·	400	·	400	pF
Low level noise margin	VnL	0.1VDD -		0.1VDD	·	IN
High level noise margin	VnH	0.2VDD -		0.2VDD	-	IN

2.8.7 SPI Interface Timing

说明

In Figure 2-30 to Figure 2-32 , the meanings of the following abbreviations or letters remain unchanged:

MSB:Most Significant Bit

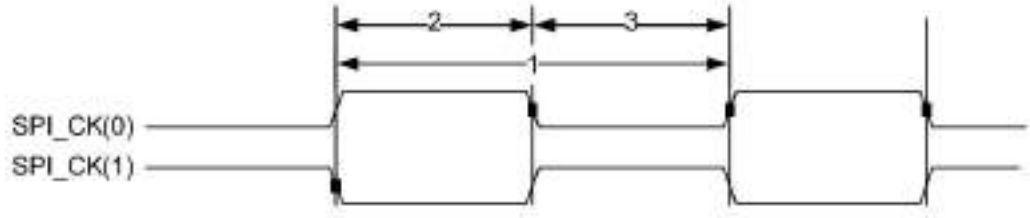
LSB:Least Significant Bit

SPI_CK(0):spo=0

SPI_CK(1):spo=1

The clock sequence of the SPI interface is shown in Figure 2-30 .

Figure 2-30 SPICK Timing



The interface timing in SPI master mode is shown in Figure 2-31 and Figure 2-32 respectively .

Figure 2-31 Interface Timing in SPI Master Mode (sph=0)

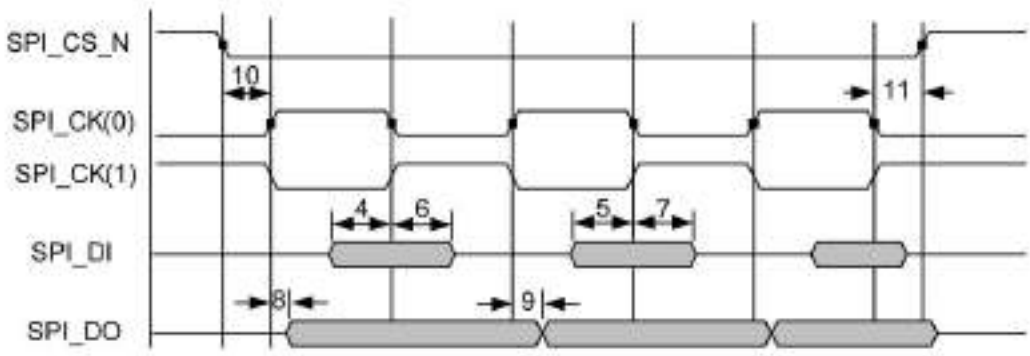
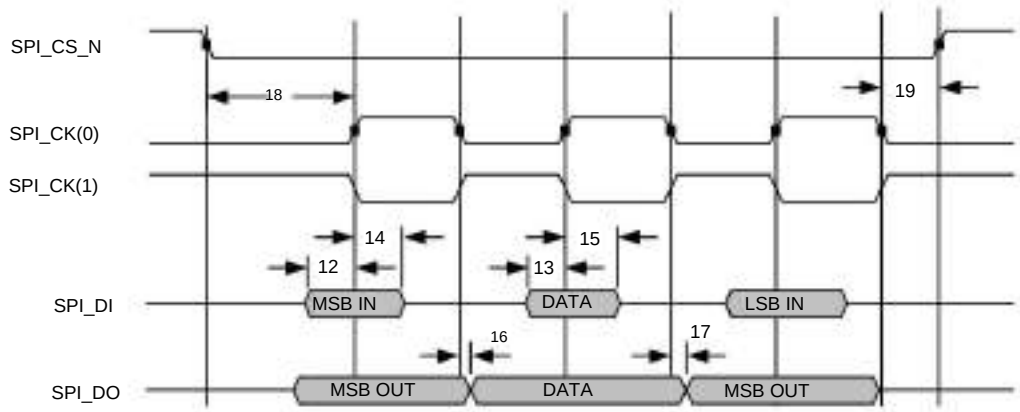


Figure 2-32 Interface Timing in SPI Master Mode (sph=1)



The timing parameters of the SPI interface are shown in Table 2-82 .

Table 2-82 SPI interface timing parameters

No number		Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc				ns
2	Pulse duration, SPI_CK high (All Master Modes)	tw1				ns
3	Pulse duration. SPI_CK low (All Master Modes)	tw2				ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1				ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2				ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1				ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2				ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1				ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2				ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3			-	ns

No number		Symbol	Min	Typ	Max	Unit
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	-	-	-	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	-	-	-	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	-	-	-	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	-	-	-	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	-	-	-	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	-	-	-	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	-	-	-	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	-	-	-	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	-	-	-	ns

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3 system

3.1 Reset

3.1.1 Overview

The reset management module performs unified management on the reset of the entire chip and the reset of each functional module, including:

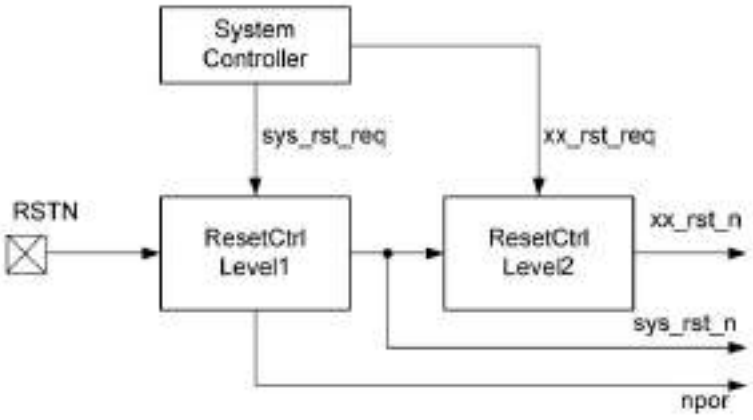
- Management and control of power-on reset
- System soft reset, function module independent soft reset control reset signal
- is synchronized to the corresponding clock domain of each module

The reset management module generates reset signals for each functional module inside the chip.

3.1.2 Reset Control

The reset signal control is shown in Figure 3-1 .

Figure 3-1 Reset signal control diagram



RSTN	The power-on reset signal comes from the chip pin RSTN input. Global soft reset request signal originating from the system controller. sys_rst_req Sub-module independent soft reset request signal, derived from CRG control register.
xx_rst_req	
xx_rst_n, sys_rst_n, npor	Reset signal.

The classification of reset signals is shown in Table 3-1 .

Table 3-1 Reset signal classification table

Reset signal type generation method		use
Global hard reset npor from reset pin RSTN		Perform a global reset on the entire chip.
Global soft reset sys_rst_n	Software configures the global soft reset register of the system controller	Perform a global reset on all modules in the entire chip except the clock reset circuit and the test circuit.
Submodule reset xx_rst_n	Software configuration of the submodule reset control register of the CRG control register	Individual reset of each sub-module of the chip.

3.1.3 Reset configuration

power on reset

RSTN is the functional reset input pin of the Hi3520D chip. To complete the power-on reset process, the following conditions must be met at the same time:

- The power-on reset pin inputs a low level pulse.
- The clock input from the crystal oscillator clock input pin XIN is stable.
- The input power-on reset signal low-level maintenance time is greater than 12 XIN crystal oscillator clock periods.

system reset

There are two ways to implement a system reset:

- Power-on reset.
- Global soft reset, controlled by the system controller.

soft reset

Soft reset control is realized by configuring the corresponding system controller. For specific configuration, please refer to the description of the reset register of each module.

注意

After the system soft reset request is issued, the circuit must wait for at least 360 system clock cycles to complete the reset deactivation. Each module's individual soft reset will not be canceled automatically. For example, when the reset of a module is configured as 1, the module is in the reset state. It must be configured as 0 again to cancel the reset of the module.

3.2 Clock

3.2.1 Overview

The clock management module performs unified management on chip clock input, clock generation and control, including:

Management and control of clock inputs

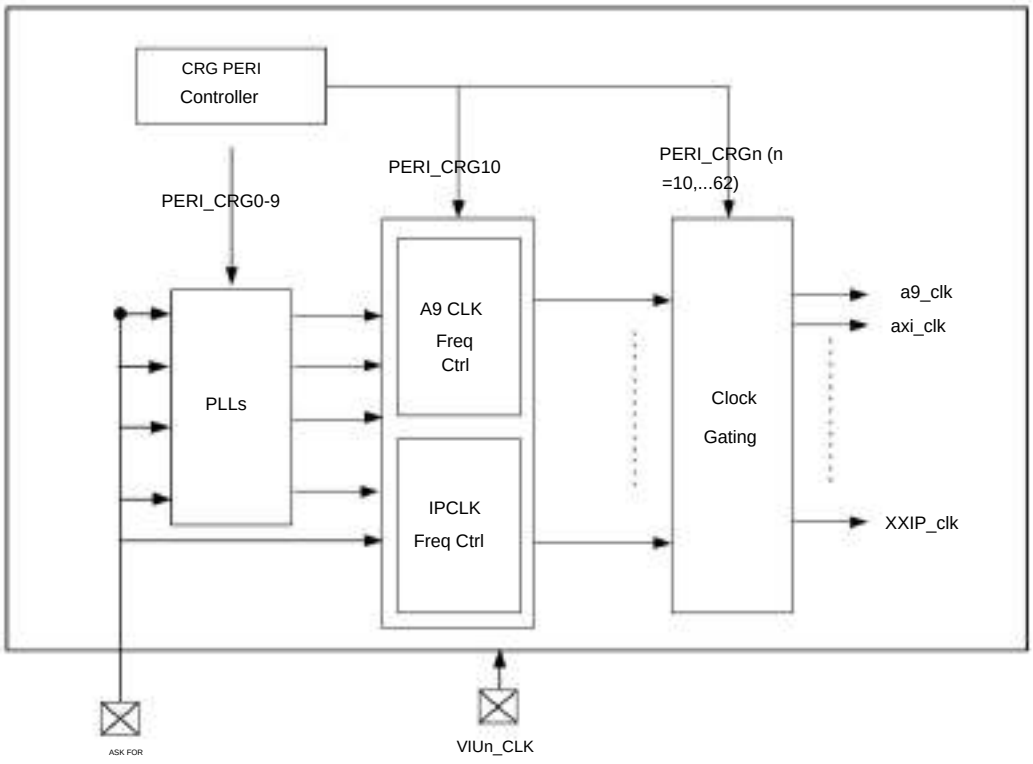
Clock Division and Control

Generate the working clock of each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the clock management module .

Figure 3-2 Functional block diagram of the clock management module



The clock management module has the following two parts of input:

Clock input from chip pins: XIN, VIUn_CLK.

ÿ XIN is the PLL input clock, which is fixedly connected to a 24MHz crystal ÿ VIUn_CLK is the video

input clock (n=0 or 1), which comes from the clock control register of the CRG

system controller.

ÿ PLL frequency configuration

ÿ IP clock frequency configuration

ÿ Clock gating configuration

The functional body of the clock management module mainly includes three parts:

PLL unit, used to generate A9 and bus clock, and other clocks required by peripherals.

A9 Frequency control unit A9 Freq Ctrl and module clock frequency control unit IPCLK Freq Ctrl.

Clock gating management unit Clock Gating.

3.2.3 Clock configuration

PLL configuration

Hi3520D internally uses 3 PLLs, and each PLL uses two sets of configuration registers, the corresponding relationship is shown in Table 3-2 .

Table 3-2 Configuration registers corresponding to Hi3520D PLL

PLL	Configuration Register 1	Configuration Register 0
APLL	PERI_CRG0	PERI_CRG1
VPLL0	PERI_CRG2	PERI_CRG3
EPLL	PERI_CRG8	PERI_CRG9

Table 3-3 shows the correspondence between PLLs and functional modules .

Table 3-3 Correspondence between Hi3520D PLL and each functional module

PLL	PLL Output Pin Purpose	
APLL	FOUTVCO	The default is 1240MHz. Divide the frequency by two to get 660MHz, which is used as A9/DDR working clock. The DDR clock is divided to obtain bus clocks such as AXI and APB.
VPLL0	ERROR1PH0	Configured as 148.5MHz, as HDMI/VDP HD working clock.

PLL	PLL Output Pin Purpose	
EPLL	FOUTVCO	Configured for 1350MHz. After dividing by 2, 675MHz is obtained, which is used as the source clock of MCLK of the SIO module. After 6 frequency division, 225MHz is obtained, which is used as the working clock of VEDU/VPSS module. After dividing by 7, 193MHz is obtained, which is used as the working clock of JPGE/VAPU module. After 12 frequency division, 112.5MHZ is obtained, as SFC/MDU/JPGE/CIPHER source clock. After frequency division, 54MHz is obtained, which is used as the source clock of VDP SD.
	FOUTPOSTDIV is configured as	150MHz, and 50MHZ is obtained after dividing by three, as SATA/ETH RMII reference clock or interface clock. Configured
	foot3	as 25MHz as FE PHY input clock.

All PLLs use the crystal oscillator clock input from pin XIN as the input clock, and the PLL output frequency configuration method is shown in Table 3-4 .

Table 3-4 Hi3520D PLL frequency calculation method

PLL Pin Calculation Method	Description	Precautions
FREF	PLL input reference clock	Hi3520D requires fixed input 24MHz
FOUTVCO	FREF x (fbdiv + frac/2^24) / refdiv	PLL operating frequency, required to be greater than or equal to 600MHz, and less than or equal to 1.6GHz
FOUTPOSTDIV FOUTVCO	/ (pstdiv1 x pstdiv2)	.
ERROR1PH0	FOUTVCO / (pstdiv1 x pstdiv2 x 2)	.
foot2	FOUTVCO / (pstdiv1 x pstdiv2 x 4)	.
foot3	FOUTVCO / (pstdiv1 x pstdiv2 x 6)	.
FOUT4	FOUTVCO / (pstdiv1 x pstdiv2 x 8)	.

Take the configuration of VPLL0 as an example, VPLL0 outputs FOUT1PH0 to the VDP module, the VDP module works in HD mode, the working clock is 148.5MHz, the value of the calculation configuration register is as follows:

Take postdiv2=2, postdiv1=2, according to FOUT1PH0= FOUTVCO / (pstdiv1 x pstdiv2 x 2), then FOUTVCO=1188MHz.

Take refdiv=2, then 24 x (fbdiv + frac/2^24)/2=1188MHz. Inferred from the above conditions: fbdiv=99, frac=000000.

A9 frequency configuration

A9 Frequency clock configuration method is shown in Table 3-5 .

Table 3-5 A9 frequency configuration

Signal name	describe
freqmode_a9_sys	A9 clock down-conversion configuration. A9 frequency reduction can be realized through Mask A9 clock pulse, and the frequency ratio between it and AXI clock can be adjusted. 11ÿA9:AXI = 1:1ÿ Others: A9:AXI = 2:1; This signal can be controlled by configuring PERI_CRG10 bit[3:2].

Table 3-6 lists the relationship between the status of the system controller and the clock switching .

Table 3-6 Correspondence between system controller status and clock switching

System Controller Status	46.875kHz clock enable status	24MHz crystal oscillator enable status	APLL enable status	System Clock Status
NORMAL enabled		Enable	Enable	The working clock of the ARM subsystem comes from the PLL output.
SLOW enable		Enable	The working clock of the	disabled ARM subsystem comes from the 24MHz crystal oscillator input.
DOZE enabled		Enable	The working clock of the	disabled ARM subsystem comes from the 46.875KHz clock obtained by dividing the 24MHz crystal oscillator clock.

Module clock frequency configuration

Table 3-7 shows the VICAP clock configuration mode .

VICAP supports a total of 2 ports and 8 channels, and each port corresponds to four channels; among them, the clock frequency division ratio of CH0/1/4/5 channels can be configured.

Table 3-7 VICAP clock frequency configuration

Signal name	describe
vich0_divsel	VI Ch0 clock selection. 00: div2 (indicating 2 frequency division); 01: div4 (represents 4 frequency division); 10: div1 (represents 1 frequency division, that is, no frequency division); 11: Reserved. This signal can be controlled by configuring PERI_CRG11 bit[31:30].
vich1_divsel	VI Ch1 clock selection. 00: div2 (indicates division by 2); 01: div4 (indicates division by 4); 1x: reserved. This signal can be controlled by configuring PERI_CRG11 bit[29:28].
vich4_divsel	VI Ch4 clock selection. 00: div2 (indicating 2 frequency division); 01: div4 (represents 4 frequency division); 10: div1 (indicating 1 frequency division, ie no frequency division); 11: Reserved. This signal can be controlled by configuring PERI_CRG11 bit[27:26].
vich5_divsel	VI Ch5 Clock selection. 00: div2 (indicating frequency division by 2); 01: div4 (indicating frequency division by 4); 1x: reserved. This signal can be controlled by configuring PERI_CRG11 bit[25:24].
we_selftest	VICAP selftest mode configuration. 0: Normal working mode, select IO input clock; 1: Self-test mode, select on-chip 24M test clock. This signal can be controlled by configuring PERI_CRG11 bit[22].
vi1_sc_sel	VI Port1 clock source selection. 0: select vi0 pad input clock; 1: select vi1 pad input clock. This signal can be controlled by configuring PERI_CRG11 bit[21].

Signal name	describe
vi0_sc_sel	VI Port0 clock source selection. 0: select vi0 pad input clock; 1: select vi1 pad input clock. This signal can be controlled by configuring PERI_CRG11 bit[20].
vi_adc_cksel	Off-chip VICAP ADC clock frequency select. 00ÿ54Mÿ 01ÿ27Mÿ 1Xÿ24Mÿ This signal can be controlled by configuring PERI_CRG11 bit[19:18].
vi0_pctrl	VI Port0 input with channel clock phase control. The default is positive. 0: clock forward; 1: Reverse clock. This signal can be controlled by configuring PERI_CRG11 bit[3].
vi1_pctrl	VI Port1 input with channel clock phase control. The default is positive. 0: clock forward; 1: Reverse clock. This signal can be controlled by configuring PERI_CRG11 bit[2].

Table 3-8 shows the clock configuration mode of the VDP module .

Table 3-8 VDP module clock frequency configuration

Signal name	describe
vou_xx_cken	VOU xx (xx = SD0/SD1/HD/Bus/VDAC) Module Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock. This signal can be controlled by configuring PERI_CRG13 bit[11:6].

HDMI clock configuration is shown in Table 3-9 .

Table 3-9 HDMI pin output clock frequency configuration

Signal name	describe
hdmi_cec_clk_sel HDMI CEC	CLK clock gate select. 0: XTAL div12 clock; 1: PLL divides 2.04MHz clock. This signal can be controlled by configuring PERI_CRG15 bit[6].
hdmi_asclk_sel	HDMI ASCLK clock selection. 0: HDMI PHY clock; 1: PLL clock. This signal can be controlled by configuring PERI_CRG15 bit[5].
hdmi_osclk_sel	HDMI OSCLK clock selection. 0: HDMI PHY clock; 1: PLL clock. This signal can be controlled by configuring PERI_CRG15 bit[4].

Table 3-10 shows the clock configuration mode of the ETH module .

Table 3-10 ETH clock frequency configuration

Signal name	describe
mii_rmii_mode	ETH MII, RMII mode configuration. 0: MII mode; 1: RMII mode. This signal can be controlled by configuring PERI_CRG51[3].
eth_rmiick_sel	ETH RMII CLK clock source selection. 0: select internal CRG clock; 1: Select PAD input clock. This signal can be controlled by configuring PERI_CRG51[4].

The clock configuration of the SATA module is shown in Table 3-11 .

Table 3-11 SATA clock frequency configuration

Signal name	describe
sata_clk_sel	SATA phy reference clock selection. 0: 150MHz clock; 1: 50MHz clock. This signal can be controlled by configuring PERI_CRG45 bit[11].
cko_alive_cksel	SATA Ctrl cko_alive Source clock selection. 0: Select internal CRG 50MHz clock; 1: Select SATAPHY cko_alive clock. This signal can be controlled by configuring PERI_CRG45 bit[12].

Table 3-12 shows the clock configuration mode of the SFC module .

Table 3-12 SFC clock frequency configuration

Signal name	describe
sfc_cksel	SFC2X clock source selection. x0: 24MHz clock; 01: 75MHz clock; 11: 112.5 MHz clock. This signal can be controlled by configuring PERI_CRG48 bit[3:2].

The clock configuration of the PWM module is shown in Table 3-13 .

Table 3-13 PWM clock frequency configuration

Signal name	describe
pwm_cksel	PWM clock select register. 0ÿ3MHzÿ 1ÿ24 MHzÿ This signal can be controlled by configuring PERI_CRG14 bit[2].

The AIO clock frequency configuration method is shown in Table 3-14 . AIO contains three independent channels AIP, AOP0 and AOP1.

Table 3-14 AIP/AOP0/AOP1 clock frequency configuration

Signal name	describe
aip_clk_sel	AIP BCLK/FSCLK clock selection. 0: Share AOP0 BCLK/FSCLK configuration; 1: Not share. This signal can be controlled by configuring PERI_CRG32 bit[24].
aip_ckcfg[23:0]	The frequency division clock configuration value of AIP mclk, the configuration value is (MCLK/AIP clock source frequency)ÿx2^27. The clock source frequency is 675MHz. MCLK maximum support 62.5MHz, this signal can be controlled by configuring PERI_CRG32 bit[23:0].
aop0_ckcfg[23:0]	The frequency division clock configuration value of AOP0 mclk, the configuration value is (MCLK/AOP0 clock source frequency)ÿx2^27. The clock source frequency is 675MHz. MCLK maximum support 62.5MHz, this signal can be controlled by configuring PERI_CRG33 bit[23:0].
aop1_ckcfg[23:0]	The frequency division clock configuration value of AOP1 mclk, the configuration value is (MCLK/AOP1 clock source frequency)ÿx2^27. The clock source frequency is 675MHz. MCLK maximum support 62.5MHz, this signal can be controlled by configuring PERI_CRG34 bit[23:0].
aip_fsclk_div	Frequency division relationship between AIP bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is divided by 128 of BCLK; 101: FS is divided by 256 of BCLK; Others: FS is divided by 8 of BCLK. This signal can be controlled by configuring PERI_CRG36 bit[14:12].

Signal name	describe
aip_bclk_div	AIP main clock MCLK and bit clock BCLK frequency division relationship. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is divided by 48 of MCLK; 1011: BCLK is divided by 64 of MCLK; Others: BCLK is divided by 8 of MCLK. This signal can be controlled by configuring PERI_CRG36 bit[11:8].
aop0_fsclk_div	Frequency division relationship between AOP0 bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK. This signal can be controlled by configuring PERI_CRG37 bit[14:12].

Signal name	describe
aop0_bclk_div	AOP0 Main clock MCLK and bit clock BCLK frequency division relationship. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is divided by 48 of MCLK; 1011: BCLK is divided by 64 of MCLK; Others: BCLK is divided by 8 of MCLK. This signal can be controlled by configuring PERI_CRG37 bit[11:8].
aop1_fsclk_div	Frequency division relationship between AOP1 bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK. This signal can be controlled by configuring PERI_CRG38 bit[14:12].

Signal name	describe
aop1_bclk_div	The frequency division relationship between the main clock MCLK and the bit clock BCLK of AOP1. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is divided by 48 of MCLK; 1011: BCLK is divided by 64 of MCLK; Others: BCLK is divided by 8 of MCLK. This signal can be controlled by configuring PERI_CRG38 bit[11:8].

In general application scenarios, the sampling rate clock frequency FSCLK is given, and the bit clock BCLK and the main clock MCLK have variable multiples relative to FSCLK. The clock frequency configuration method is as follows:

The clock source of AIO fractional frequency division is fixed at 675MHz. At this time, it is required to configure the AIO working clock frequency as FSCLK=48kHz, MCLK=256FSCLK=12.288MHz, BCLK=16FSCLK=768KHz. The configuration method is as follows:

The frequency division ratio from 675MHz to MCLK is calculated as: N=12.288/675, then aio_ckcfg[23:0]= $N \times 2^{27}$ is calculated as 2443359 according to the rounding principle, so configure aio_ckcfg=0x0025_485F to get the correct frequency of CLK.

BCLK is obtained by MCLK frequency division, and the frequency division ratio is BCLK/MCLK=16/256=1/16, so according to the corresponding relationship in the configuration table, configure aio_bclk_div[3:0]=0b0111 (corresponding to 16 frequency division) to get correct frequency of BCLK.

FSCLK is obtained by frequency division of BCLK, and the frequency division ratio is 1/16. Therefore, according to the corresponding relationship in the configuration table, configure aio_fsclk_div=0b000 (corresponding to 16 frequency division) to obtain the correct frequency of FSCLK.

Precautions

The clock configuration needs to pay attention to the following items:

The A9 working clock defaults to the crystal oscillator mode when it is powered on, that is, the crystal oscillator clock input by XIN is selected.

When the PLL changes the frequency configuration, it needs to wait for 0.1ms to output a stable clock. Changing the PLL frequency configuration can only be done when the system is in SLOW mode.

When the PLL output clock is not stable, the system cannot switch to the PLL mode. You can judge whether the PLL is LOCK by observing the PLL LOCK indicator bit. The PLL LOCK indicator bit can be read by PERI_CRG58 bit[2:0] status acquisition.

3.2.4 Register overview

An overview of the CRG register is shown in Table 3-15 .

Table 3-15 CRG register overview (base address is 0x2003_0000)

offset address name		describe	page number
0x0000	PERI_CRG0	APLL Configuration Register 0	3-16
0x0004	PERI_CRG1	APLL Configuration Register 1	3-17
0x0008	PERI_CRG2	VPLL0 Configuration Register 0	3-18
0x000C PERI_CRG3		VPLL0 Configuration Register 1	3-19
0x0020	PERI_CRG8	EPLL Configuration Register 0	3-20
0x0024	PERI_CRG9	EPLL Configuration Register 1	3-21
0x0028	PERI_CRG10	A9 Frequency mode and reset configuration register	3-22
0x002C	PERI_CRG11	VICAP Clock and Reset Configuration Register	3-24
0x0034	PERI_CRG13	VOU Clock and Reset Control Register	3-26
0x0038	PERI_CRG14	PWM Clock and Reset Control Register	3-27
0x003C	PERI_CRG15	HDMI Clock and Reset Control Register	3-28
0x0040	PERI_CRG16	VEDU clock and soft reset control register	3-29
0x0048	PERI_CRG18	VPSS Clock and Soft Reset Control Register	3-30
0x0058	PERI_CRG22	TDE Clock and Soft Reset Control Register	3-30
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-31
0x0064	PERI_CRG25	JPGD clock and soft reset control register	3-32
0x0068	PERI_CRG26	MDU clock and soft reset control register	3-32
0x006C PERI_CRG27		VAPU clock and soft reset control register	3-33
0x0070	PERI_CRG28	VOIE related clock and soft reset control register 3-34	
0x0074	PERI_CRG29	VCMP related clock and soft reset control register 3-34	
0x007C	PERI_CRG31	CIPHER related clock and soft reset control register	3-35
0x0080	PERI_CRG32	AIP MCLK Control Register	3-36

offset address name		describe	page number
0x0084	PERI_CRG33	AOP0 MCLK Control Register	3-36
0x0088	PERI_CRG34	AOP1 MCLK Control Register	3-37
0x008C	PERI_CRG35	AIO Bus Clock Reset Control Register	3-37
0x0090	PERI_CRG36	AIP related clock and soft reset control register 3-38	
0x0094	PERI_CRG37	AOP0 related clock and soft reset control register 3-40	
0x0098	PERI_CRG38	AOP1 related clock and soft reset control register 3-41	
0x00B4	PERI_CRG45	SATA related clock and soft reset control register 3-43	
0x00B8 PERI_CRG46		USB related clock and soft reset control register 3-45	
0x00C0	PERI_CRG48	SFC related clock and soft reset control register 3-46	
0x00CC PERI_CRG51		Clock and soft reset control registers related to ETH interface	3-47
0x00D4	PERI_CRG53	SCD related clock and soft reset control register 3-47	
0x00D8 PERI_CRG54		DDRTEST and EFUSE related clock and soft reset control registers	3-48
0x00E4	PERI_CRG57	Other CRG Interface Module Soft Reset Control Register 3-49	
0x00E8	PERI_CRG58	CRG status register	3-51
0x00F4	PERI_CRG61	SpeedMonitor Control Register	3-52
0x00F8	PERI_CRG62	SpeedMonitor Status Register 1	3-52

3.2.1 Register description

PERI_CRG0

PERI_CRG0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG0	0x1100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																	apll_frac															
Reset	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	apll_bypass	APLL clock divider bypass (bypass) control. 0: no bypass; 1: Bypass.
[29:27]	RW	apll_postdiv2	The second stage of APLL outputs the frequency division factor.
[26:24]	RW	apll_postdiv1	APLL first-stage output frequency division coefficient.
[23:0]	RW	apll_frac	APLL Fractional division factor.

PERI_CRG1

PERI_CRG1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG1	0x007C_309B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																appll_refdiv								apll_fbdiv							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1	1	0	1	1		

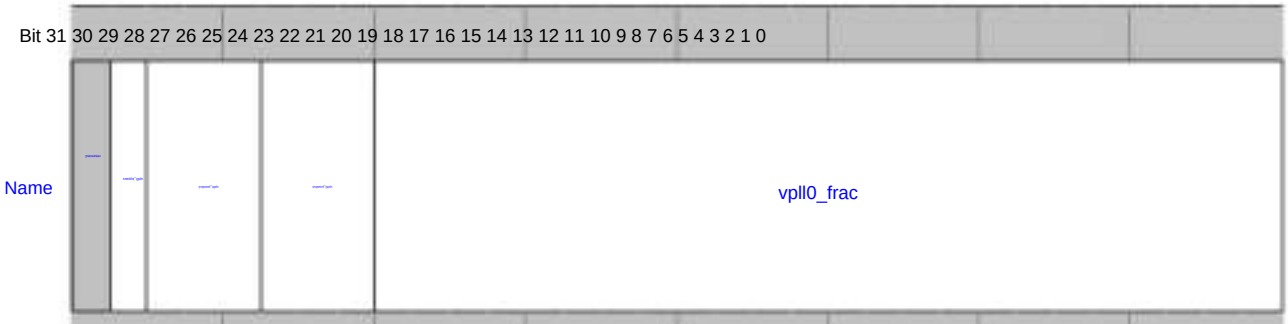
Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23] RW apll_dacpd			APLL test signal control. 0: power down working state; 1: normal working state.
[22] RW apll_dsmpd			APLL Fractional divider control. 0: Decimal mode; 1: Integer mode.
[21] RW apll_pd			APLL Power Down control. 0: power down working state; 1: normal working state.
[20] RW apll_foutvcopd			APLL VCO output Power Down control. 0: no clock output; 1: Normal output clock.
[19] RW apll_postdivpd			APLL POSTDIV Output Power Down control. 0: no clock output; 1: normal clock output.
[18] RW apll_fout4phasepd			APLL FOUT output Power Down control. 0: no clock output; 1: Normal clock output.
[17:12] RW apll_refdiv			APLL reference clock division factor.
[11:0] RW apll_fbdiv			APLL integer multiplication factor.

PERI_CRG2

PERI_CRG2 Configuration register 0 for VPLL0.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_CRG2	0x1200_0000

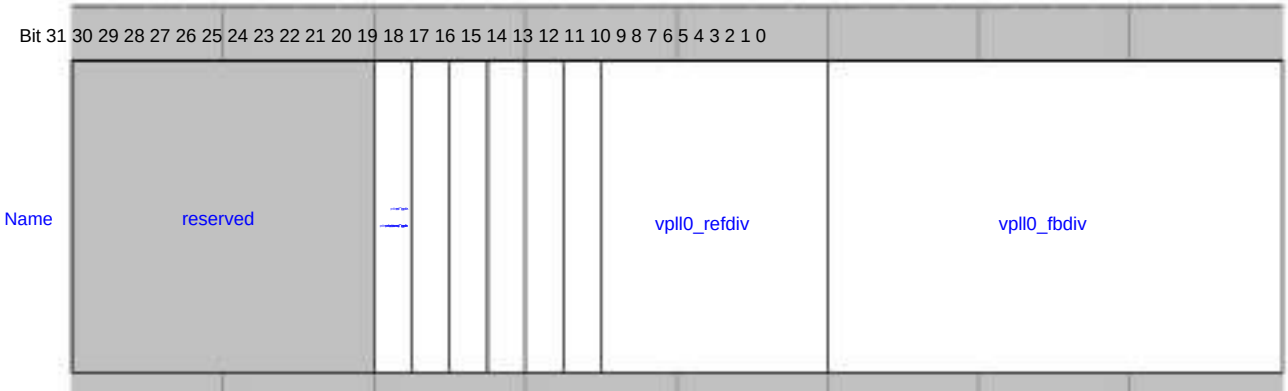


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	vpll0_bypass	VPLL0 clock divider bypass (bypass) control. 0: no bypass; 1: Bypass.
[29:27]	RW	vpll0_postdiv2	VPLL0 second stage output frequency division factor.
[26:24]	RW	vpll0_postdiv1	VPLL0 first stage output frequency division factor.
[23:0]	RW	vpll0_frac	VPLL0 Fractional division factor.

PERI_CRG3

PERI_CRG3 Configuration Register 1 for VPLL0.

Offset Address	Register Name	Total Reset Value
0x000C	PERI_CRG3	0x007C_2063



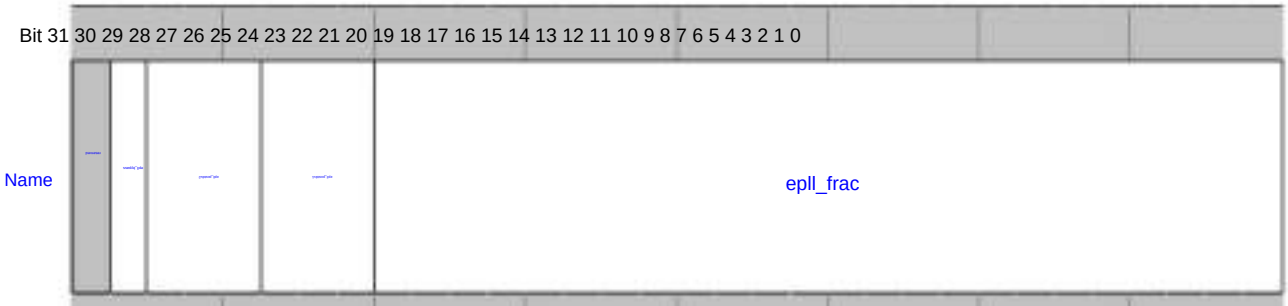
Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23] RW vpll0_dacpd	VPLL0 test signal control. 0: power down working state; 1: normal working state.
[22] RW vpll0_dsmpd	VPLL0 Fractional divider control. 0: Decimal mode; 1: Integer mode.
[21] RW vpll0_pd	VPLL0 Power Down Control. 0: power down working state; 1: normal working state.
[20] RW vpll0_foutvcopd	VPLL0 VCO output Power Down control. 0: no clock output; 1: Normal output clock.
[19] RW vpll0_postdivpd	VPLL0 POSTDIV Output Power Down control. 0: no clock output; 1: normal clock output.
[18] RW vpll0_fout4phasepd	VPLL0 FOUT output Power Down control. 0: no clock output; 1: Normal clock output.
[17:12] RW vpll0_refdiv	VPLL0 reference clock division factor.
[11:0] RW vpll0_fbdiv	VPLL0 integer multiplication factor.

PERI_CRG8

PERI_CRG8 Configuration register 0 for EPLL.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG8	0x1B00_0000

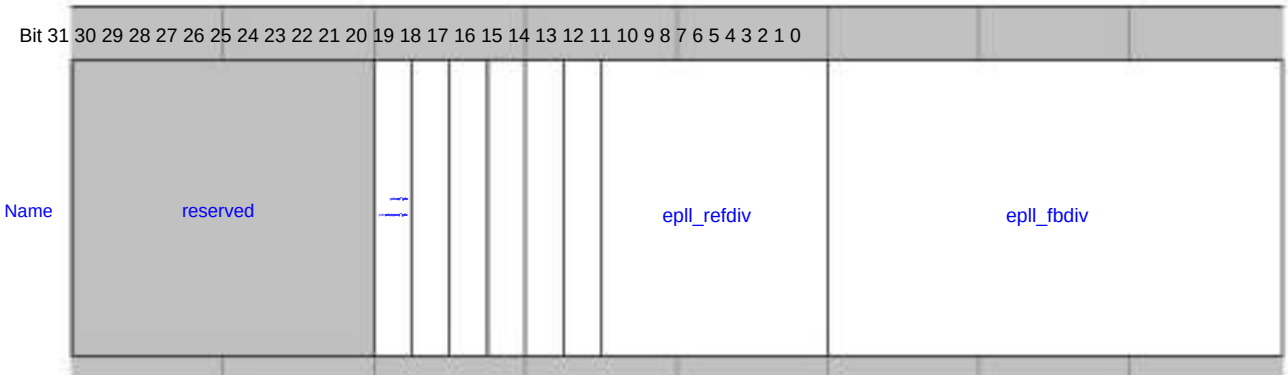


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	epll_bypass	EPLL clock divider bypass (bypass) control. 0: no bypass; 1: Bypass.
[29:27]	RW	epll_postdiv2	The second stage of EPLL outputs the frequency division factor.
[26:24]	RW	epll_postdiv1	The first stage of EPLL outputs the frequency division factor.
[23:0]	RW	epll_frac	EPLL Fractional division factor.

PERI_CRG9

PERI_CRG9 Configuration register 1 for EPLL.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG9	0x007C_40E1



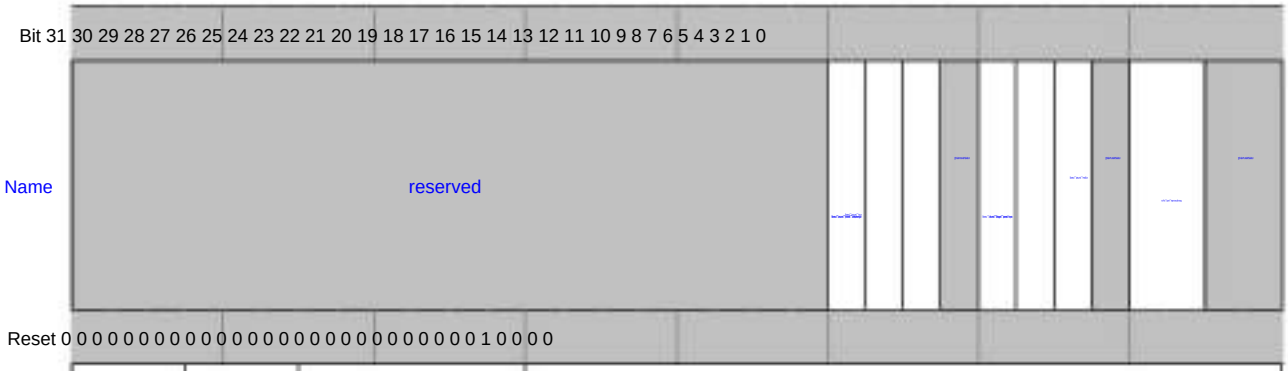
Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23] RW epll_dacpd			EPLL test signal control. 0: power down working state; 1: normal working state.
[22] RW epll_dsmpd			EPLL Fractional divider control. 0: Decimal mode; 1: Integer mode.
[21] RW epll_pd			EPLL Power Down control. 0: power down working state; 1: normal working state.
[20] RW epll_foutvcopd			EPLLVCO output Power Down control. 0: no clock output; 1: Normal output clock.
[19] RW epll_postdivpd			EPLL POSTDIV Output Power Down control. 0: no clock output; 1: normal clock output.
[18] RW epll_fout4phasepd			EPLLFOUT Output Power Down control. 0: no clock output; 1: Normal clock output.
[17:12] RW epll_refdiv			EPLL reference clock division factor.
[11:0] RW epll_fbdiv			EPLL integer multiplication factor.

PERI_CRG10

PERI_CRG10 is A9 frequency mode and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0010



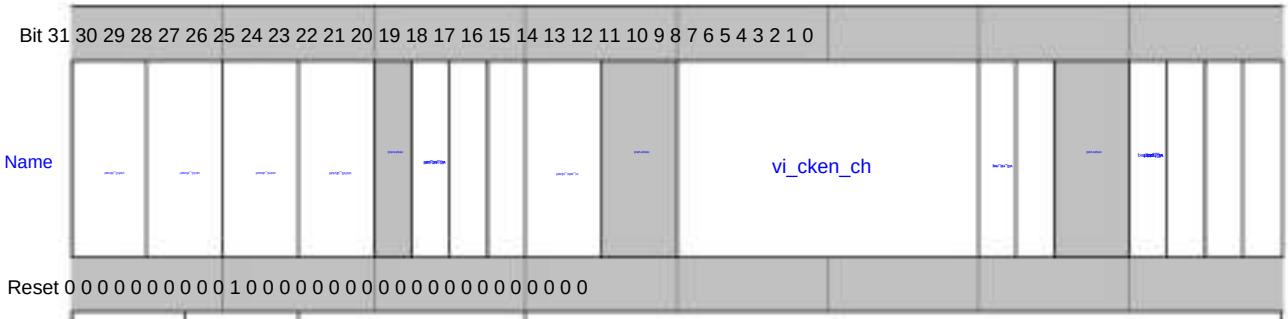
Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11]	RW	cs_srst_req	CS soft reset request. 0: cancel reset; 1: Reset.
[10]	RW	SCU. cluster_scu_srst_re	Soft reset request for 0: undo reset; q 1: Reset.
[9]	RW	PERI. cluster_peri_srst_re	Soft reset request for 0: cancel reset; q 1: reset.
[8]	RO	reserved	reserve
[7]	RW	sc_wd_srst_req	Soft reset request for WDG. 0: cancel reset; 1: reset.
[6]	RW	module. cluster_dbg_srst_re	Soft reset request for DBG 0: undo reset; q 1: reset.
[5]	RW	cpu_srst_req	The soft reset request of the CPU is only valid in the slave loading mode. 0: cancel reset; 1: reset.
[4]	RO	reserved	reserve

[3:2] RW	freqmode_a9_sys		A9 clock down-conversion configuration. A9 frequency reduction can be realized through Mask A9 clock pulse, and the frequency ratio between it and AXI clock can be adjusted: 11ÿA9:AXI = 1:1ÿ Others: A9:AXI= 2:1.
[1:0] RO		reserved	reserve.

PERI_CRG11

PERI_CRG11 is VICAP clock and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0020_0000



Bits	Access	Name	Description
[31:30]	RW	vich0_divsel	VI Ch0 clock selection. 00ÿdiv2ÿ 01ÿdiv4ÿ 10ÿdiv1ÿ 11: Reserved.
[29:28]	RW	vich1_divsel	VI Ch1 clock selection. 00ÿdiv2ÿ 01ÿdiv4ÿ 1X: reserved.
[27:26]	RW	vich4_divsel	VI Ch4 Clock Select 00ÿdiv2ÿ 01ÿdiv4ÿ 10ÿdiv1ÿ 11: Reserved.

[25:24] RW	vich5_divsel		VI Ch5 Clock selection. 00ÿdiv2ÿ 01ÿdiv4ÿ 1X: reserved.
[23] RO		reserved	reserve.
[22] RW	vi_selftest		VICAP selftest mode configuration. 0: Normal working mode, select IO input clock; 1: Self-test mode, select on-chip 24MHz test clock.
[21] RW	vi1_sc_sel		VI Port1 clock source selection. 0: select vi0 pad input clock; 1: select vi1 pad input clock.
[20] RW	vi0_sc_sel		VI Port0 clock source selection. 0: select vi0 pad input clock; 1: select vi1 pad input clock.
[19:18] RW	we_adc_cksel		Off-chip VICAP ADC clock frequency selection. 00ÿ54MHzÿ 01ÿ27MHzÿ 1Xÿ24MHzÿ
[17:16] RO		reserved	reserve.
[15:8] RW	vi_cken_ch		VI chn (0~7) Clock gating. 0: clock off; 1: Clock is on. Bit[15] corresponds to VI ch7, and Bit[8] corresponds to VI ch0.
[7] RW	vi0_rst_req		Soft reset request for VI0. 0: cancel reset; 1: Reset.
[6] RW	vi1_rst_req		Soft reset request for VI1. 0: cancel reset; 1: Reset.
[5:4] RO		reserved	reserve.
[3] RW	vi0_pctrl		VI0 input with channel clock phase control. 0: clock forward; 1: Reverse clock.

[2] RW vi1_pctrl			VI1 input with channel clock phase control. 0: clock forward; 1: Reverse clock.
[1] RW vi_hcken			VI bus clock gating. 0: clock off; 1: Clock is on.
[0] RW vi_hrst_req			Soft reset request on the VI bus side. 0: cancel reset; 1: reset.

PERI_CRG13

PERI_CRG13 is the VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0037

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0									
Name	reserved									
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1								1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11]	RW	vou_sd1_cken	VOU SD1 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[10]	RW	vou_sd0_cken	VOU SD0 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[9]	RW	vou_hd_cken	VOU HD Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.

[8] RW vou_hcken			VOU Bus Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[7] RW sddac_cken			SD DAC clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[6] RW hddac_cken			HD DAC clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[5:3] RO		reserved	reserve
[2] RW vo_sd_srst_req			Soft reset request for VOU SD. 0: cancel reset; 1: Reset.
[1] RW vo_hd_srst_req			Soft reset request for VOU HD. 0: cancel reset; 1: Reset.
[0] RW vo_hrst_req			VOU Bus soft reset request. 0: cancel reset; 1: reset.

PERI_CRG14

PERI_CRG14 is PWM clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_CRG14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

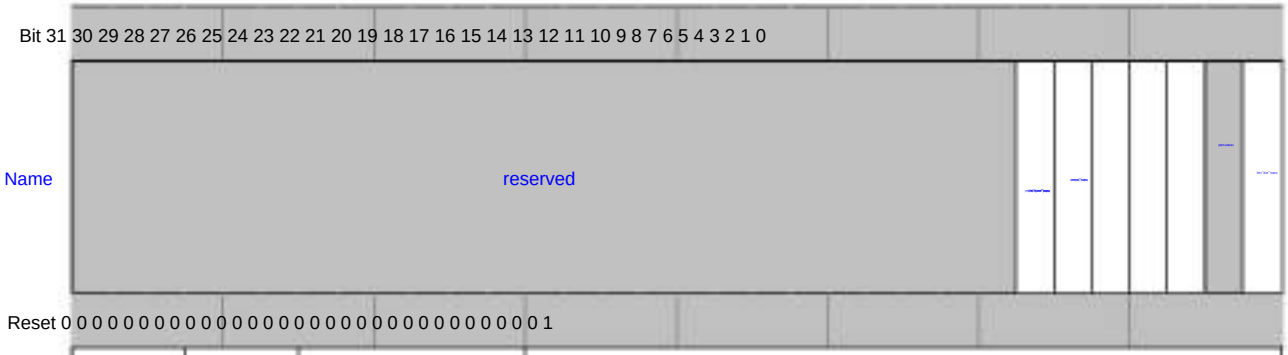
Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.

[2] RW	pwm_cksel		PWM clock select register. 0ÿ3 MHzÿ 1ÿ24 MHzÿ
[1] RW	pwm_cken		PWM clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0] RW	pwm_srst_req		Soft reset request for PWM. 0: cancel reset; 1: reset.

PERI_CRG15

PERI_CRG15 is HDMI clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_CRG15	0x0000_0001



Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	hdmi_cec_clk_sel	HDMI CEC CLK clock gate selection. 0: XTAL div12 clock; 1: PLL frequency division 2.04M clock.
[5]	RW	hdmi_asclk_sel	HDMI ASCLK clock selection. 0: HDMI PHY clock; 1: PLL clock.
[4]	RW	hdmi_osclk_sel	HDMI OSCLK clock selection. 0: HDMI PHY clock; 1: PLL clock.

[3] RW hdmi_idcken			HDMI pixel clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[2] RW hdmi_hcken			HDMI bus clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[1]	RO	reserved	reserve
[0] RW hdmi_srst_req			Soft reset request for HDMI. 0: cancel reset; 1: reset.

PERI_CRG16

PERI_CRG16 is the VEDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0C03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1		

Bits	Access Name		Description
[31:12] RO		reserved	reserve.
[11] RW sed_cken			SED clock gating configuration register, 0: disable the clock; 1: enable the clock.
[10] RW sed_srst_req			Soft reset request for SED. 0: cancel reset; 1: reset.
[9:2] RO		reserved	reserve.

[1] RW wedu_cken			VEDU Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0] RW vedu_srst_req			Soft reset request for VEDU. 0: cancel reset; 1: reset.

PERI_CRG18

PERI_CRG18 is the VPSS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	vps_cken	VPSS clock gating configuration register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW	vps_srst_req	Soft reset request for VPSS. 0: cancel reset; 1: reset.

PERI_CRG22

PERI_CRG22 is TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1		

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	tde_cken	TDE Clock Gating Configuration Register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW	tde_srst_req	Soft reset request for TDE. 0: cancel reset; 1: Reset.

PERI_CRG24

PERI_CRG24 is JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1		

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	jpge_cken	JPGE Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.

[0] RW	jpge_srst_req		Soft reset request for JPGE. 0: cancel reset; 1: reset.

PERI_CRG25

PERI_CRG25 is the JPGD clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_CRG25	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	jpgd_cken	JPGD clock gating configuration register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW	jpgd_srst_req	Soft reset request for JPGD. 0: cancel reset; 1: reset.

PERI_CRG26

PERI_CRG26 is the MDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	mdu_cken	MDU clock gating configuration register, 0: turn off the clock; 1: turn on the clock.
[0]	RW	mdu_srst_req	Soft reset request for MDU. 0: cancel reset; 1: reset.

PERI_CRG27

PERI_CRG27 is the VAPU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	vapu_cken	VAPU clock gating configuration register, 0: turn off the clock; 1: Turn on the clock.

[0] RW	vapu_srst_req		Soft reset request for VAPU. 0: cancel reset; 1: reset.

PERI_CRG28

PERI_CRG28 is the clock and soft reset control register related to VOIE.

Offset Address	Register Name	Total Reset Value
0x0070	PERI_CRG28	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	channel_cken	VOIE Clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RO	reserved	reserve.

PERI_CRG29

PERI_CRG29 is the clock and soft reset control register related to VCMP.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_CRG29	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	vcmp_cken	VCMP Clock Gating Configuration Register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW	vcmp_srst_req	Soft reset request from VCMP. 0: cancel reset; 1: Reset.

PERI_CRG31

PERI_CRG31 is the clock and soft reset control register related to CIPHER.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

[1] RW cipher_cken			CIPHER Clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0] RW cipher_srst_req			Soft reset request for CIPHER. 0: cancel reset; 1: reset.

PERI_CRG32

PERI_CRG32 is the AIP MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									aip_ckcfg						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	aip_clk_sel	AIP BCLK/FSCLK clock selection. 0: share AOP0 BCLK/FSCLK configuration; 1: Not shared.
[23:0]	RW	aip_ckcfg	The frequency division clock configuration value of AIP MCLK, the configuration value is (MCLK/AIO clock source frequency)ÿ×2^27. The clock source frequency is 675 MHz. MCLK maximum support 62.5 MHzÿ

PERI_CRG33

PERI_CRG33 is the AOP0 MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_CRG33	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_ckcfg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop0_ckcfg	The frequency division clock configuration value of AOP0 MCLK, the configuration value is (MCLK/AIO clock source frequency)ÿ×2^27. The clock source frequency is 675 MHz. Mclk maximum support 62.5 MHzÿ

PERI_CRG34

PERI_CRG34 is the AOP1 MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0088	PERI_CRG34	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_ckcfg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	reserve.
[23:0]	RW	aop1_ckcfg	The frequency division clock configuration value of AOP1 mclk, the configuration value is (MCLK/AIO clock source frequency)ÿ×2^27. The clock source frequency is 675 MHz. MCLK maximum support 62.5 MHzÿ

PERI_CRG35

PERI_CRG35 is the AIO bus clock reset control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:2]	RO reserved	reserve.
[1]	RW aio_hcken	AIO bus clock gating configuration register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW aio_hrst_req	AIO bus side soft reset request. 0: cancel reset; 1: Reset.

PERI_CRG36

PERI_CRG36 is the clock and soft reset control register related to AIP.

Offset Address	Register Name	Total Reset Value
0x0090	PERI_CRG36	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aip_fsclk_div				aip_bclk_div				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:16]	RO reserved	reserve.

[15:12]	RW	aip_fsclk_div	Frequency division relationship between AIP bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is divided by 32 of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK.
[11:8]	RW	aip_bclk_div	AIP main clock MCLK and bit clock BCLK frequency division relationship. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is 48 frequency division of MCLK; 1011: BCLK is 64 frequency division of MCLK; Others: BCLK is divided by 8 of MCLK.
[7:5]	RO	reserved	reserve.
[4]	RW	aip_bclk_sel	AIP BCLK clock selection. 0: Select externally generated bclk; 1: Select internally generated bclk.
[3]	RW	aip_bclkout_pctrl	AIP Polarity control for BCLK OUT. 0: forward; 1: Reverse.
[2]	RW	aip_bclk_pctrl	Polarity control of AIP BCLK. 0: forward; 1: Reverse.
[1]	RW	aip_cken	AIP clock gating. 0: turn off the clock; 1: Turn on the clock.

[0] RW aip_srst_req			AIP soft reset request. 0: cancel reset; 1: reset.

PERI_CRG37

PERI_CRG37 is the clock and soft reset control register related to AOP0.

Offset Address	Register Name	Total Reset Value
0x0094	PERI_CRG37	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			aop0_bclk_div												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	aop0_fsclk_div	Frequency division relationship between AOP0 bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK.

[11:8] RW	aop0_bclk_div		AOP0 Main clock MCLK and bit clock BCLK frequency division relationship. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is 48 frequency division of MCLK; 1011: BCLK is 64 frequency division of MCLK; Others: BCLK is divided by 8 of MCLK.
[7:5] RO		reserved	reserve.
[4] RW	aop0_bclk_sel		AOP0 BCLK clock selection. 0: Select externally generated bclk; 1: Select internally generated bclk.
[3] RW	aop0_bclkout_pctrl		Polarity control for AOP0 BCLK OUT. 0: Forward; 1: Reverse.
[2] RW	aop0_bclk_pctrl		Polarity control of AOP0 BCLK. 0: forward; 1: Reverse.
[1] RW	aop0_cken		AOP0 clock gating: 0: disable clock; 1: enable clock.
[0] RW	aop0_srst_req		Soft reset request for AOP0. 0: cancel reset; 1: reset.

PERI_CRG38

PERI_CRG38 is the clock and soft reset control register related to AOP1.

Offset Address	Register Name	Total Reset Value
0x0098	PERI_CRG38	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				aop1_bclk_div											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	aop1_fsclk_div	Frequency division relationship between AOP1 bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK.
[11:8]	RW	aop1_bclk_div	The frequency division relationship between the main clock MCLK and the bit clock BCLK of AOP1. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is 48 frequency division of MCLK; 1011: BCLK is 64 frequency division of MCLK; Others: BCLK is divided by 8 of MCLK.
[7:5]	RO	reserved	reserve.

[4] RW	aop1_bclk_sel		AOP1 BCLK clock selection. 0: Select externally generated bclk; 1: Select internally generated bclk.
[3] RW	aop1_bclkout_pctrl	1: Reverse.	Polarity control for AOP1 BCLK OUT. 0: Forward;
[2] RW	aop1_bclk_pctrl		Polarity control of AOP1 BCLK. 0: forward; 1: Reverse.
[1] RW	aop1_cken		AOP1 clock gating. 0: turn off the clock; 1: Turn on the clock.
[0] RW	aop1_srst_req		Soft reset request for AOP1. 0: cancel reset; 1: Reset.

PERI_CRG45

PERI_CRG45 is the clock and soft reset control register related to SATA.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_CRG45	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	cko_alive_cksel	SATA Ctrl cko_alive source clock selection: 0: select internal CRG50M clock; 1: Select SATAPHY cko_alive clock.

[11] RW	sata_clk_sel		SATA phy reference clock selection: 0: 150M clock; 1: 50M clock.
[10] RW	sata_cken		SATA PHY and bus clock status. 0: off; 1: open.
[9] RW	sata0_cken		SATA controller Port0 clock status. 0: off; 1: open.
[8] RW	sata1_cken		SATA controller Port1 clock status. 0: off; 1: open.
[7] RW	rst_alive_s		SATA controller alive Clock domain soft reset control. 0: cancel reset; 1: Reset.
[6] RW	rst_rx1_s		SATA controller rx1 clock domain soft reset control. 0: cancel reset; 1: reset.
[5] RW	rst_rx0_s		SATA controller rx0 clock domain soft reset control. 0: cancel reset; 1: Reset.
[4] RW	rst_tx1_s		SATA controller tx1 clock domain soft reset control. 0: cancel reset; 1: Reset.
[3] RW	rst_tx0_s		SATA controller tx0 clock domain soft reset control. 0: cancel reset; 1: reset.
[2] RW	rst_sata_s		SATA controller interface soft reset control. 0: cancel reset; 1: Reset.
[1] RW	handful_sata_s		SATA controller bus soft reset control. 0: cancel reset; 1: Reset.

[0] RW	rst_sataphy_s		SATA PHY soft reset control. 0: cancel reset; 1: reset.

PERI_CRG46

PERI_CRG46 is the clock and soft reset control register related to USB.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_00FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved									
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	usb_cken	USB PHY reference clock gating. 0: off; 1: open.
[6]	RW	usb_ctrl_utmi1_req	Soft reset request for USB controller port1. 1: Reset. 0: Cancel reset;
[5]	RW	usb_ctrl_utmi0_req	Soft reset request for USB controller port0. 0: cancel reset; 1: Reset.
[4]	RW	usb_ctrl_hub_req	A soft reset request for the USB controller hub. 0: cancel reset; 1: Reset.
[3]	RW	usbphy_port1_treq	Soft reset request for USB PHY PORT1. 1: Reset. 0: Cancel reset;

[2] RW	usbphy_port0_treq	1: Reset.	Soft reset request for USB PHY PORT0. 0: Cancel reset;
[1] RW	usbphy_req		Soft reset request for USB PHY. 0: cancel reset; 1: reset.
[0] RW	usb_ahb_srst_req		USB controller bus soft reset request. 0: cancel reset; 1: reset.

PERI_CRG48

PERI_CRG48 is the clock and soft reset control register related to SFC.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

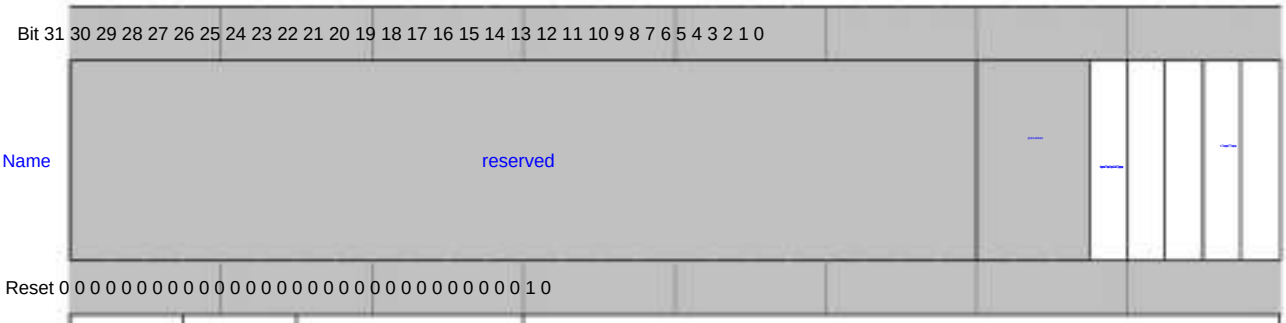
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:2]	RW	sfc_cksel	SFC2X clock source selection. x0: 24MHz clock; 01: 75MHz clock; 11: 112..5MHz clock.
[1]	RW	sfc_cken	SFC Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	sfc_srst_req	Soft reset request for SFC. 0: cancel reset; 1: reset.

PERI_CRG51

PERI_CRG51 is the clock and soft reset control register related to ETH interface.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_0002



Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	eth_rmiick_sel	ETH RMII CLK clock source selection. 1: Select PAD input clock; 0: Select internal CRG clock.
[3]	RW	mii_rmii_mode	ETH MII, RMII mode configuration. 0: MII model; 1: RMII mode.
[2]	RW	fephy_srst_req	Soft reset request for FE PHY. 0: cancel reset; 1: reset. **Note: The reset holding time of FEPHY is required to be >10ms, which needs to be guaranteed by software.**
[1]	RW	eth_cken	ETH clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	hrst_eth_s	Soft reset request for ETH. 0: cancel reset; 1: reset.

PERI_CRG53

PERI_CRG53 is the SCD related clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D4	PERI_CRG53	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	scd_cken RW		SCD Clock Gating Configuration Register. 0: Turn off the clock; 1: Turn on the clock.
[2]	RO	reserved	reserve.
[1]	RW scd_srst_req		Soft reset request for SCD. 0: cancel reset; 1: reset.
[0]	RO	reserved	reserve.

PERI_CRG54

PERI_CRG54 is the clock and soft reset control register related to DDRTEST and EFUSE.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

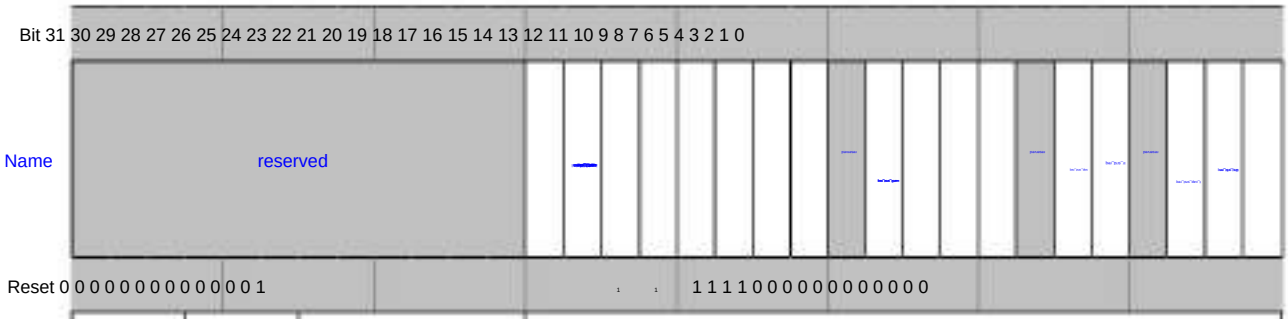
Bits	Access Name		Description
[31:4]	RO	reserved	reserve.

[3] RW ddrtest_cken			DDRTEST Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[2] RW ddrtest_srst_req			Soft reset request for DDRTEST. 0: cancel reset; 1: reset.
[1] RW efuse_cken			EFUSE Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0] RW efuse_srst_req			Soft reset request for EFUSE. 0: cancel reset; 1: Reset.

PERI_CRG57

PERI_CRG57 is the soft reset control register for other CRG interface modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x0007_F000



Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RW	test_clk_sel	Test clock group selection. 1: Select the first set of test clocks (USB and PCLK); 0: Select the second set of test clocks (HDMI).
[18]	RW	uart3_cken	UART3 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.

[17] RW	uart2_cken		UART2 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[16] RW	uart1_cken		UART1 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[15] RW	uart0_cken		UART0 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[14] RW	uart_cksel		UART clock selection. 1: Select 2M clock; 0: Select APB clock.
[13] RW	ssp_cken		SSP clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[12] RW	ir_cken		IR Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[11] RO		reserved	reserve.
[10] RW	uart3_srst_req		Soft reset request for UART3. 0: cancel reset; 1: reset.
[9] RW	uart2_srst_req		Soft reset request for UART2. 0: cancel reset; 1: Reset.
[8] RW	uart1_srst_req		Soft reset request for UART1. 0: cancel reset; 1: reset.
[7] RW	uart0_srst_req		Soft reset request for UART0. 0: cancel reset; 1: reset.
[6]	RO	reserved	reserve.

[5] RW	ssp_srst_req		Soft reset request for SSP. 0: cancel reset; 1: reset.
[4] RW	ir_srst_req		Soft reset request for IR. 0: cancel reset; 1: reset.
[3]	RO	reserved	reserve.
[2] RW	t_cap_srst_req		Soft reset request for t_cap. 0: cancel reset; 1: reset.
[1] RW	i2c_srst_req		I²C's soft reset request. 0: cancel reset; 1: Reset.
[0] RW	test_clk_en		Test clock enable register. 0: all test clocks are off; 1: All test clocks are on.

PERI_CRG58

PERI_CRG58 is the CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

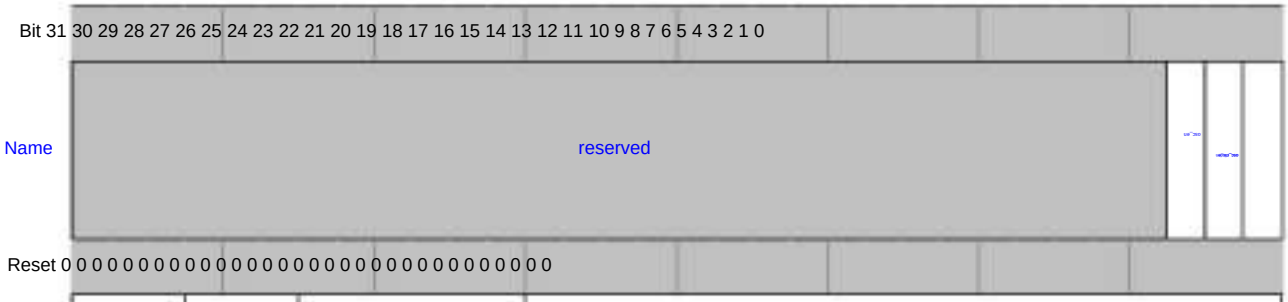
Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RO	epll_lock	EPLL LOCK status. 0ÿUnlockÿ 1ÿLockedÿ

[1]	RO	vpll0_lock	VPLL0 LOCK status. 0ÿUnlockÿ 1ÿLockedÿ
[0]	RO	apll_lock	APLL LOCK status. 0ÿUnlockÿ 1ÿLockedÿ

PERI_CRG61

PERI_CRG61 is the SpeedMonitor control register.

Offset Address	Register Name	Total Reset Value
0x00F4	PERI_CRG61	0x0000_0000



Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	osc_en	SpeedMonitor Enable control. 0ÿdisableÿ 1ÿenalbleÿ
[1]	RW	osc_mode	SpeedMonitor mode configuration. 0ÿ150 step levelÿ 1ÿ200 step levelÿ
[0]	RW	osc_clk_en	SpeedMonitor clock enable control. 0ÿdisableÿ 1ÿenableÿ

PERI_CRG62

PERI_CRG62 is SpeedMonitor status register 1.

Offset Address	Register Name	Total Reset Value
0x00F8	PERI_CRG62	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													osc_value		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:10]	RO	reserved	reserve.
[9]	RO	osc_valid	Whether SpeedMonitor is valid. 0ÿinvalidÿ 1ÿvalidÿ
[8:0]	RO	osc_value	SpeedMonitor count value.

3.3 Interrupt System

The chip uses the interrupt controller GIC integrated in Cortex-A9, which can support up to 96 interrupt sources, and the corresponding interrupt mapping is shown in Table 3-16 .

Table 3-16 A9 interrupt source allocation table

interrupt bit	interrupt source	interrupt bit	interrupt source
0–31	For A9 internal use	64	A9_PMU_INT0
32	COMMTX[0]	65	WAY
33	COMMRX[0]	66	HDMI
34	Watchdog	67	VDP
35	Timer0	68	VICAP
36	Timer1	69	VPSS
37	Timer2	70	TDE
38	Timer3	71	VCMP
39	RTC	72	OURS
40	UART0	73	JPGE
41	UART1	74	JPGD

interrupt bit interrupt source		interrupt bit	interrupt source
42	UART2	75	Reserved
43	UART3	76	MD
44	SSP	77	IVE
45	2C	78	Reserved
46	AND	79	GPIO0
47	AIO	80	GPIO1
48	Reserved	81	GPIO2
49	Reserved	82	GPIO3
50	SFC	83	GPIO4
51	Reserved	84	GPIO5
52	HOURS	85	GPIO6
53	USB_EHCI	86	GPIO7
54	USB_OHCI	87	GPIO8
55	Cipher	88	Reserved
56	ETH	89	TEM_CAP_INT
57	FE PHY	90	Reserved
58	Reserved	91	Reserved
59	Reserved	92	Reserved
60	Software int	93	Reserved
61	L2CACHE_CHK0_INT	94	Reserved
62	L2CACHE_CHK1_INT	95	Reserved
63	L2CACHE_INT_COMB		

3.4 System Controller

3.4.1 Overview

The system controller controls the operating mode of the system, monitors the operating status of the system, manages important functions in the system, and completes the configuration of certain functions of the peripherals.

3.4.2 Features

The system controller has the following characteristics:

Control and monitor the operating mode of the

system Provide system clock control and status query

Provide control and status monitoring of system address remapping

Provides general-purpose peripheral registers

Provides the write protection function for key registers

Provides the identification register of the chip

3.4.3 Functional description

3.4.4 System operation mode control

The system works in the following three working modes:

NORMAL mode

The system works normally in NORMAL mode. In this mode, the system is driven by the output clock of the on-chip APLL. All modules can work normally with this clock source. (Some peripherals can be selected to be driven by the output clock of VPLL0 and EPLL) SLOW mode SLOW mode is a slow mode. In this mode, the

system is driven by

an external crystal oscillator clock, and only some on-chip peripherals (such as system controller, Timer, SFC, etc.) can work. All modules that require a high-speed clock cannot work under this clock, such as DDRC and so on.

DOZE mode DOZE

mode is a low speed mode. Only a few on-chip peripherals can work in DOZE mode. In this mode, the system is driven by a 46.875kHz low-frequency clock divided by an external crystal oscillator. Most of the on-chip peripherals cannot work, and the memory interface cannot work. The CPU and a small number of modules (such as system controller, Timer and IR, etc.) can work in this mode.

The system controller provides a system mode switching mechanism for controlling the switching of the system clock source. Mode switching is configured by the mode control register SC_CTRL[modectrl]. These 3 bits define the current operating mode that the system needs to enter:

000: Reserved

001: System switched to DOZE mode 010: System

switched to SLOW mode 100: System switched to

NORMAL mode Others: Reserved

When the required system operation mode has been specified in the system mode control register, the system mode control system starts to switch to the specified mode, and no other software (command) intervention is required during this period.

The current system status can be obtained by reading SC_CTRL[modestatus]. The current state of the system described by this bit field includes the above-mentioned main modes: NORMAL, SLOW, DOZE, and also includes

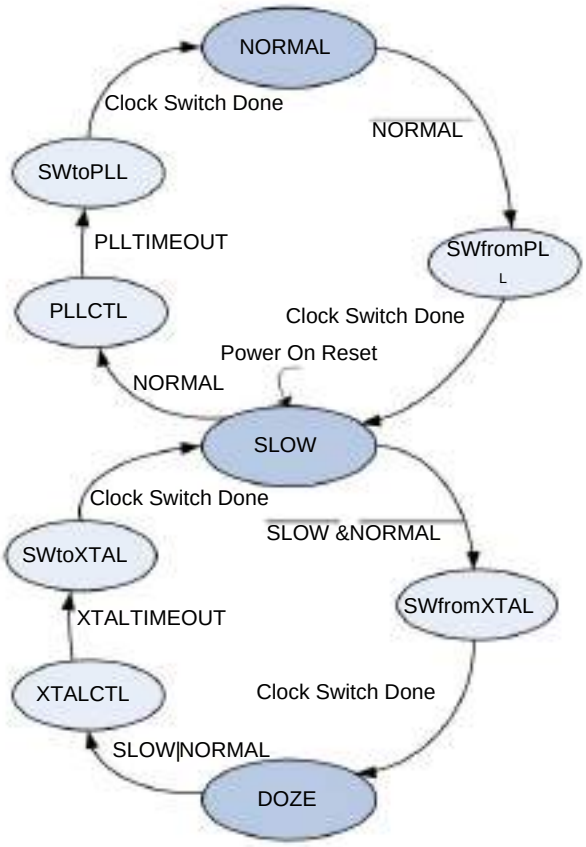
Several intermediate states: SWfromPLL, SWtoPLL, PLLCTL, SWfromXTAL, SWtoXTAL, XTALCTLÿ

说明

NORMAL, SLOW, DOZE three modes can be configured as direct switching. If the system is currently in NORMAL mode, it can enter DOZE mode by configuring the register SC_CTRL [modectrl] as "001". However, during the actual system operation, it has experienced "SWfromPLL", "SLOW", "SWfromXTAL" and other modes or intermediate states.

The state switching process of the system is shown in Figure 3-3 .

Figure 3-3 System mode switching diagram



The operations involved in switching between various modes are as follows:

Set the highest bit of SC_CTRL[modectrl] to 0, the system will leave the NORMAL mode and switch to the slow mode SLOW. When the system

enters the SLOW mode from NORMAL mode, the system first enters the SWfromPLL intermediate state. This marks the system clock source to switch from PLL to crystal. When the clock switch is completed (Clock Switch Done), the system enters SLOW mode.

After power-on reset, the system is in SLOW mode. Setting the highest bit of SC_CTRL[modectrl] to 1 can make the system enter NORMAL mode. In the process of switching to NORMAL mode, first enter the PLLCTL intermediate state to enable ARMPLL, after a fixed waiting time (the waiting time is affected by SC_XTALCTRL[plltime]), enter the SWtoPLL intermediate state to switch the clock source, and the switching is completed (Clock Switch Done), the system enters NORMAL mode. Setting the upper two bits of SC_CTRL[modectrl] to 0 can make the system switch to the low-speed DOZE mode. The system will first enter the SWfromXTAL intermediate state. This indicates that the system clock source will switch from the crystal oscillator clock to the 46.875kHz low-frequency clock obtained by dividing the crystal oscillator clock. When the clock switching is completed (Clock Switch Done), the system enters DOZE mode. Setting one of the high two bits of SC_CTRL[modectrl] to 1 can make the system switch to the slow SLOW mode. In the process of switching to SLOW mode, first enter the XTALCTL intermediate state to initialize the clock module, after a fixed waiting time (the waiting time is affected by SC_XTALCTRL[xtaltime]), enter the SWtoXTAL intermediate state to switch the clock source, and the switching is completed (Clock Switch Done) and then the system enters SLOW mode.

For the relationship between the state machine state of the system controller and the system clock, see Table 3-6.

Soft Reset Control

The system controller supports soft reset for the global and local modules of the chip:

After configuring the global soft reset register SC_SYSRES , the system controller will initiate a request to the on-chip reset module, and the chip will be reset.

System Address Remapping Control

Please refer to chapter "1.3 Start Mode".

Write protection for critical registers

In order to prevent the misoperation of the software on the system controller from seriously affecting the entire system, the system controller provides a write protection function for some key configuration registers. include:

Mode switching control register: SC_CTRL System global soft

reset control register: SC_SYSRES

Before writing to these key registers, the register SC_LOCKEN must be configured to enable write protection. After the operation is completed, the configuration register SC_LOCKEN closes the write protection, so that these key registers will not be rewritten by the software at will.

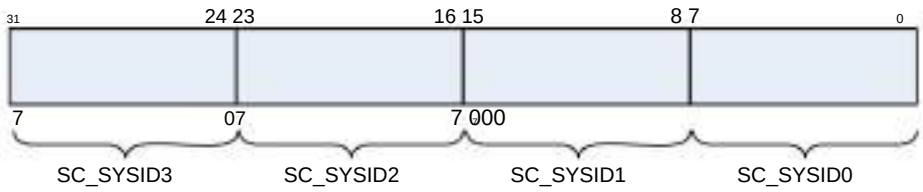
说明

By default, the system does not write-protect these key registers after reset. To enable this feature, it is recommended to use this register to write-protect these critical registers at system startup.

chip identification register

The system controller provides the chip identification (ID) register SC_SYSID. This identification register is a conceptual 32-bit identification read-only register, which actually consists of four 8-bit identification registers: SC_SYSID3, SC_SYSID2, SC_SYSID1, SC_SYSID0. Read out the values of these 4 registers, and obtain the value 0x3520_D100 of the chip's 32-bit identification read-only register through combination. The combination method is shown in Figure 3-4 .

Figure 3-4 Chip ID register bit allocation diagram



3.4.5 Register overview

An overview of the system controller registers is shown in Table 3-17 .

Table 3-17 Overview of system controller registers (base address is 0x2005_0000)

offset address name		describe	page number
0x000	SC_CTRL	System Control Register	3-60
0x004	SC_SYSRES	System Soft Reset Register	3-63
0x008	SC_IMCTRL	Interrupt Mode Control Register	3-63
0x00C	SC_IMSTAT	Interrupt Mode Status Register	3-64
0x010	SC_XTALCTRL Crystal Oscillator	Control Register	3-65
0x014	SC_PLLCTRL	PLL Control Register	3-66
0x01C	PERIPHCTRL0 Peripheral Contro	Register 0	3-67
0x0020	PERIPHCTRL1 Peripheral Contro	Register 1 (soft interrupt register) 3-68	
0x0034	PERIPHCTRL2 Peripheral Contro	Register 2	3-69
0x0038	PERIPHCTRL3 Peripheral Contro	Register 3 (SATA PHY Control Register device)	3-69
0x003C PERIPHCTRL4 Peripheral Control Register 4			3-70
0x0040	PERIPHCTRL5 Peripheral Contro	Register 5 (MEDIA0 bus Master port Timeout control register 0)	3-72
0x0044 SC_LOCK		Lock Register 3-73 of the Critical System Control Register	
0x0048	PERIPHCTRL6 Peripheral Contro	Register 6 (MEDIA0 bus Master port Timeout control register 1)	3-74
0x0054	PERIPHCTRL9 Peripheral Contro	Register 9 (MEDIA0 bus Master Port Priority Control Register)	3-75
0x0058	PERIPHCTRL10 Peripheral Contro	Register 10 (System Bus Master Port Timeout Control Register 0)	3-76

offset address name	describe	page number
0x005C PERIPHCTRL11 Peripheral Control Register 11 (System Bus Master Port Timeout Control Register 1)		3-76
0x0064	PERIPHCTRL13 Peripheral Control Register 13 (System Bus Master Port Timeout Control Register 1)	3-77
0x0068	PERIPHCTRL14 Peripheral control register 14 (system bus Slave end Port Priority Control Register)	3-78
0x006C PERIPHCTRL15 Peripheral Control Register 15 (CHIP ID Register) 3-79		
0x0070	PERIPHCTRL16 Peripheral Control Register 16 (MEDIA1 bus Master port Timeout control register 0)	3-79
0x0074	PERIPHCTRL17 Peripheral Control Register 17 (MEDIA1 bus Master port Timeout control register 1)	3-80
0x0078	PERIPHCTRL18 Peripheral Control Register 18 (MEDIA1 bus Master port Timeout control register 2)	3-81
0x007C PERIPHCTRL19 peripheral control register 19 (MEDIA1 bus Master Port Priority Control Register)		3-82
0x0080	PERIPHCTRL20 Peripheral Control Register 20 (USB Control Register) 3-83	
0x0084	PERIPHCTRL21 Peripheral Control Register 21 (USB PHY Control Register 0)	3-85
0x0088	PERIPHCTRL22 Peripheral Control Register 22 (USB PHY Control Register 1)	3-88
0x008C SYSSTAT	System Status Register (PLL_LOCK)	3-90
0x0090	PERIPHCTRL23 Peripheral Control Register 23 (MDDRC out-of-order configuration outtodr_ctrl register)	3-92
0x0094	PERIPHCTRL24 Peripheral Control Register 24 (FE PHY Configuration Register device)	3-94
0x0098	PERIPHCTRL25 Peripheral Control Register 25 (SATA PHY Control Register 1)	3-94
0x00A4 PERIPHCTRL28 Peripheral Control Register 28 (IO Control Register 0)		3-95
0x00A8 PERIPHCTRL29 Peripheral Control Register 29 (IO Control Register 1)		3-98
0xEE0	SCSYSID0	Chip ID Register 0	3-99
0xEE4	SCSYSID1	Chip ID Register 1	3-100
0xEE8	SCSYSID2	Chip ID Register 2	3-100
0xEEC	SCSYSID3	Chip ID Register 3	3-100

3.4.6 Register description

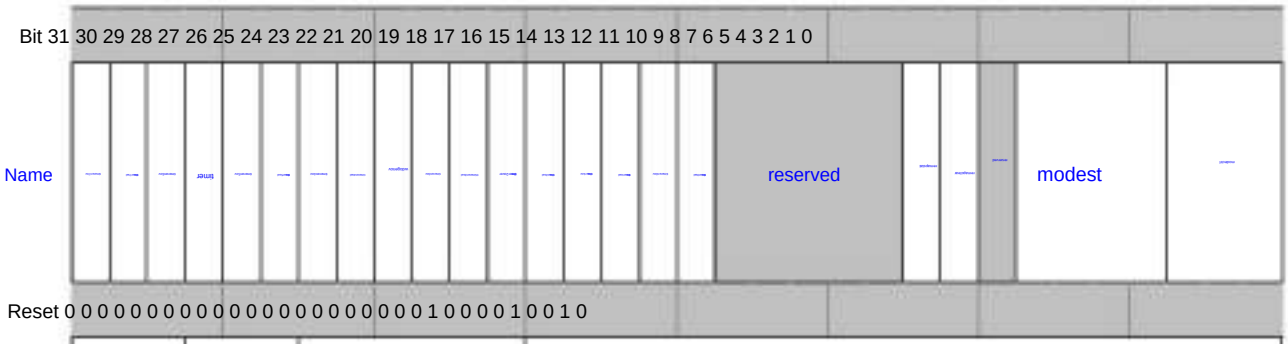
SC_CTRL

SC_CTRL is the system control register. Used to specify actions that require the system to complete.

注意

This register can be write-protected by the register SC_LOCKEN . Only when the write protection mode is not used, the write operation to this register is valid.

Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0212



Bits	Access	Name	Description
[31]	RW	timeren7ov	Timer7 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren7sel]; 1: Counting by the bus clock.
[30]	RW	timeren7sel	Timer7 counting clock frequency selection. Must be configured as 0. 0: use 3MHz clock for counting; 1: Reserved.
[29]	RW	timeren6ov	Timer6 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren6sel]; 1: Counting by the bus clock.
[28]	RW	timeren6sel	Timer6 counting clock frequency selection. Must be configured as 0. 0: use 3MHz clock for counting; 1: Reserved.

[27] RW timeren5ov			Timer5 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren5sel]; 1: Counting by the bus clock.
[26] RW timeren5sel			Timer5 counting clock frequency selection. Must be configured as 0. 0: use 3MHz clock for counting; 1: Reserved.
[25] RW timeren4ov			Timer4 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren4sel]; 1: Counting by the bus clock.
[24] RW timeren4sel			Timer4 counting clock frequency selection. Must be configured as 0. 0: Use 3MHz clock for counting; 1: Reserved.
[23] RW wdogenov			WDG count clock selection. 0: WDG uses 3MHz clock to count; 1: WDG uses the bus clock for counting.
[22] RW timer3ov			Timer3 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren3sel]; 1: Counting by the bus clock.
[21] RW timeren3sel			Timer3 counting clock frequency selection. Must be configured as 0. 0: use 3MHz clock for counting; 1: Reserved.
[20] RW timer2ov			Timer2 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren2sel]; 1: Counting by the bus clock.
[19] RW timeren2sel			Timer2 counting clock frequency selection. Must be configured as 0. 0: Use 3MHz clock for counting; 1: Reserved.
[18] RW timeren1ov			Timer1 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren1sel]; 1: Counting by the bus clock.

[17] RW timeren1sel			Timer1 counting clock frequency selection. Must be configured as 0. 0: use 3MHz clock for counting; 1: Reserved.
[16] RW timeren0ov			Timer0 count clock selection. 0: The enable signal is obtained by using the reference clock, and the selection of the reference clock is specified by [timeren0sel]; 1: Counting by the bus clock.
[15] RW timeren0sel			Timer0 counting clock frequency selection. Must be configured as 0. 0: Use 3MHz clock for counting; 1: Reserved.
[14:10] RO		reserved	reserve. Returns 0 on read, no effect on write.
[9]	RO	remapstat	Status of address remapping. 0: no address remapping; 1: Perform address remapping. bootrom or SFC CS1 is remapped to address 0ÿ
[8] RW remapclear			Address remapping clears the selection. 0: Keep Remap status. 1: Clear Remap. For the address mapping relationship before and after Clear Remap, see Address Allocation.
[7]	RO	reserved	reserve. Returns 0 on read, no effect on write.
[6:3] RW modestatus			mode status bit. Returns the current operating mode of the system. 0x0: reserved; 0x1ÿDOSESÿ 0x2ÿSLOWÿ 0x3ÿXTAL CTLÿ 0x4ÿNORMALÿ 0x6ÿPLL CTLÿ 0x9ÿSW from XTALÿ 0xAÿSW from PLLÿ 0xBÿSW to XTALÿ 0xE: SW to PLL; Others: reserved, not used.

[2:0] RW modectrl			mode control bit. Defines the operating modes that the system controller is required to enter. 000: reserved; 001ÿDOZEÿ 010ÿSLOWÿ 100ÿNORMALÿ

SC_SYSRES

SC_SYSRES is the system soft reset register. Writing any value to this register will cause the system controller to send a system soft reset request to the reset module, and the reset module will perform a system soft reset.

注意

This register can be write-protected by the register SC_LOCKEN , and the write operation to this register is valid only when the write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name		Description
[31:0]	WO	softresreq	Any write operation to this register will cause a soft reset of the system.

SC_IMCTRL

SC_IMCTRL is the interrupt mode control register. Used to control the system mode when an interrupt occurs.

Offset Address	Register Name	Total Reset Value
0x008	SC_IMCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:8]	RO reserved	reserve. Returns 0x000000 when reading, and has no effect when writing.
[7]	RW inmdtype	The type of interrupt that triggers the system to enter interrupt mode. 0: Only FIQ interrupt can make the system enter interrupt mode; 1: Both FIQ interrupt and IRQ interrupt can make the system enter interrupt mode.
[6:4]	RO reserved	reserve.
[3:1]	RW itmdctrl	The lowest working mode of the system in interrupt mode, the value of this register is ORed with the value of SC_CTRL[modectrl] as the working mode of the system after the interrupt occurs. It is defined as follows: 000ÿSLEEPÿ 001ÿDOZEÿ 01XÿSLOWÿ 1XXÿNORMALÿ
[0]	RW itm	Interrupt mode enable. 0: forbidden; 1: Enable (enter interrupt mode when interrupt occurs).

SC_IMSTAT

SC_IMSTAT is the interrupt mode status register. It is used to monitor whether the system is in the interrupt mode, and the system can also be forced to enter the interrupt mode by configuring this register.

注意

The interrupt mode must be cleared manually when the interrupt service routine is finished.

Offset Address	Register Name	Total Reset Value
0x00C	SC_IMSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															itmdstat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:1]	RO reserved	reserve. Returns 0x00000000 when reading, and has no effect when writing.
[0]	RW itmdstat	Interrupt mode status. Can be used for software control to directly enter interrupt mode. When reading this register: 0: not currently in interrupt mode; 1: currently in interrupt mode. When writing this register: 0: software does not control to enter interrupt mode; 1: software controls to enter interrupt mode.

SC_XTALCTRL

SC_XTALCTRL is crystal oscillator control register. It is used to control the stable waiting time of the initialization clock module, that is, the waiting time for jumping from the XTAL CTL intermediate state to the SW to XTAL intermediate state.

Offset Address	Register Name	Total Reset Value
0x010	SC_XTALCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														xtaltime	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:19]	RO reserved	Reserved, return 0x0000 when read, no effect when written.
[18:3]	RW xtaltime	Crystal switching wait time. The value of this field is used to specify the waiting time for switching from XTAL CTL state to SW to XTAL state when the system mode is switched. The number of waiting cycles can be calculated (T46.8K is a 46.8KHz low-frequency clock cycle): (65536 – xtaltime)xT46.8K.

[2]	RO	reserved	reserve. Returns 0x0 when reading, and has no effect when writing.
[1:0] RO		reserved	reserve. Returns the written value on read, has no effect on write.

SC_PLLCTRL

SC_PLLCTRL is the PLL control register. It is used to control the enable control of the on-chip ARM phase-locked loop (ARMPLL), which is enabled by software control or by system mode switching. In addition, this register is also used to set the ARMPLL PLL stabilization wait time.

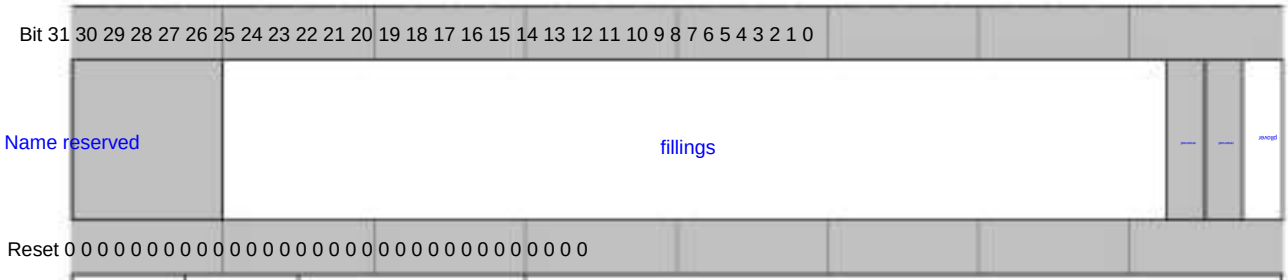
注意

This register can be write-protected by the register SC_LOCKEN , and the write operation to this register is valid only when the write protection is disabled.

When it is in the "Enable ARMPLL phase-locked loop controlled by system mode switching" (controlled by SC_PLLCTRL[pllover]), ARMPLL is automatically turned off when the system is in non-NORMAL mode.

The clock frequency of ARMPLL is controlled by CRG registers PERI_CRG0 and PERI_CRG1. The system requires the PLL to wait for 0.5ms to output a stable clock when changing the frequency configuration. Therefore, the plltime configuration of this register must meet this requirement.

Offset Address	Register Name	Total Reset Value
0x014	SC_PLLCTRL	0x0000_0000



Bits	Access Name		Description
[31:28] RO		reserved	reserve. Returns 0x0 when reading, and has no effect when writing.
[27:3] RW plltime			ARMPLL PLL stabilization wait time. This period of time is used to wait for the PLL to start and the PLL output to reach a stable state, which is to specify the waiting time for switching from the PLL CTL state to the SW to PLL state when switching from the system mode. The timeout value is calculated by the following formula (TXIN is the clock cycle of the external crystal oscillator): (33554432 - plltime)xTXIN.
[2]	RO	reserved	reserve. Returns 0x0 when reading, and has no effect when writing.
[1]	RO	reserved	reserve.

[0] RW pllover			Allows the ARLPLL PLL to be enabled directly under software control, rather than being controlled by system mode state changes. Must be configured as 0. 0: Enable the ARMPLL phase-locked loop by switching the system mode; 1: Reserved.

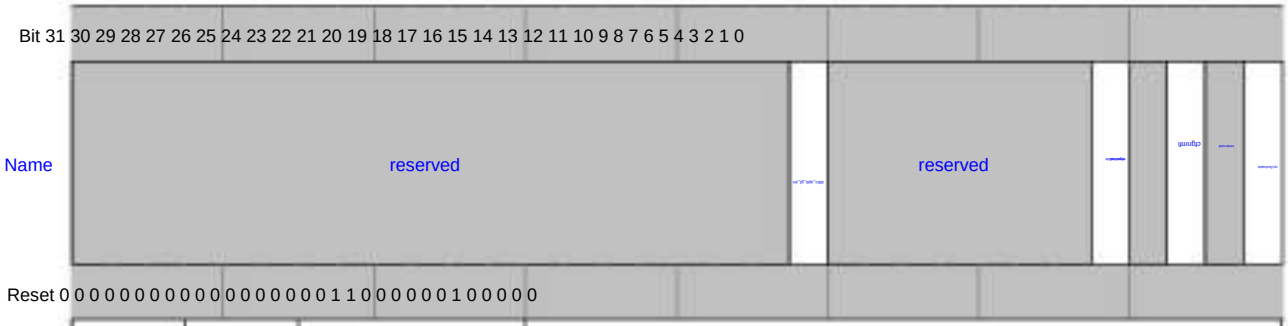
PERIPHCTRL0

PERIPHCTRL0 is the peripheral control register 0.

注意

This register can be write-protected by the register SC_LOCKEN , and the write operation to this register is valid only when the write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x01C	PERIPHCTRL0	0x0000_1000



Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RW ddrc_apb_gt_en			MDDRC APB clock gating. 0: Disable APB clock; 1: Enable APB clock.
[11:5] RO		reserved	reserve.
[4] RW cfgsdisable			cpu set[4]. Shield the write access to the processor's internal key configuration registers, including ICDDCR[0]=EnableSecure, the security interrupt defined in ICDICTR and ICCICR (excluding the EnableNS control bit). 0: disable; 1: enable.
[3]	RO	reserved	reserve.

[2] RW cfgnmfi			cpu set[2]ÿ The CPU fast interrupt is used as a non-maskable interrupt enable. 0: disable; 1: Enable CPU fast interrupt as non-maskable interrupt.
[1]	RO	reserved	reserve.
[0] RW cp15sdisable			cpu set[0]. Shields write access to the processor's internal security registers, including c1 (SCTLR), c2 (TTBR0 and TTBCR), c3 (DACR), c10 (PRRR and NMRR), c12 (VBAR and MVBAR), c13 in the CP15 coprocessor (FCSEIDR). 0: disable; 1: enable.

PERIPHCTRL1

PERIPHCTRL1 is the peripheral control register 1 (soft interrupt register).

注意

This register can be write-protected by the register SC_LOCKEN , and the write operation to this register is valid only when the write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x0020	PERIPHCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	reserve.
[0]	RW	software_int	Software interrupt. 0: no interrupt is generated; 1: Generate an interrupt.

PERIPHCTRL2

PERIPHCTRL2 is Peripheral Control Register 2.

Offset Address	Register Name	Total Reset Value
0x0034	PERIPHCTRL2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	rom_pgen	ROM power enable. 0: enable; 1: Disable.

PERIPHCTRL3

PERIPHCTRL3 is the peripheral control register 3 (SATA PHY control register).

Offset Address	Register Name	Total Reset Value
0x0038	PERIPHCTRL3	0x5D75_F000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		sata_phy0_ref_clk_sel
Reset	0 1 0 1	1 0 1 0 1	1 0 1 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0

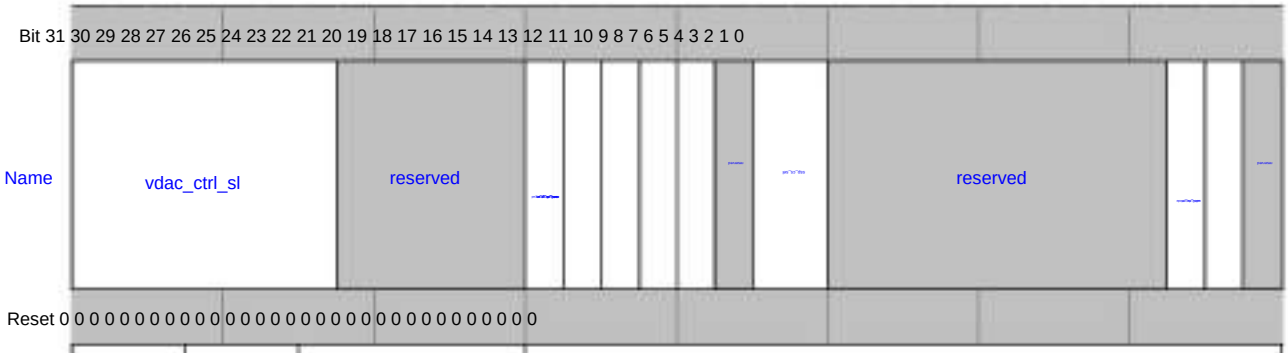
Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.

[9:8] RW		sata_phy0_mpll_ss _sel	Spread spectrum selection. Reserved, must be set to 0.
[7:0] RW		the MPLL. sata_phy0_ref_clk_ sel	Reference clock frequency selection. Sets a fixed ppm phase shift on the clock output from 0x00: no phase shift (default); 0x01~0xFF: reserved.

PERIPHCTRL4

PERIPHCTRL4 is the peripheral control register 4.

Offset Address	Register Name	Total Reset Value
0x003C	PERIPHCTRL4	0x0000_0000



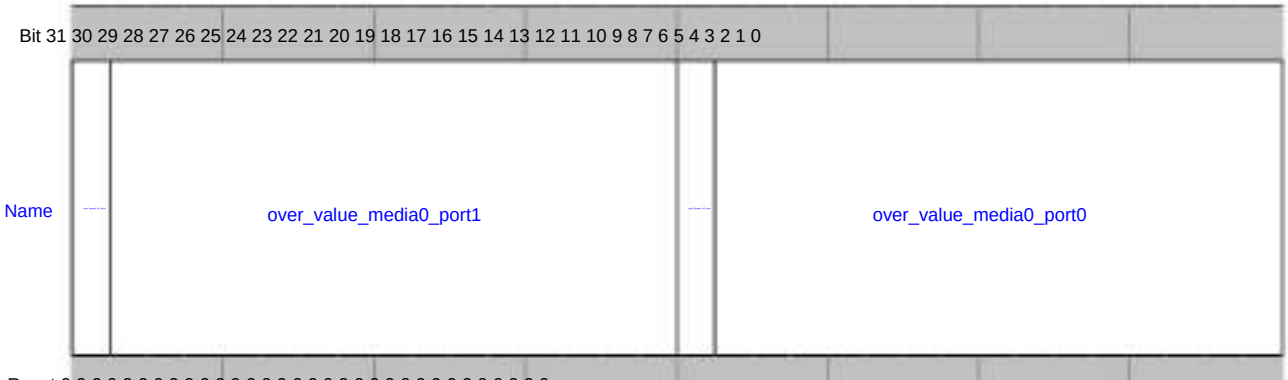
Bits	Access	Name	Description
[31:25]	RW	vdac_ctrl_sl	VDAC channel power down control. vdac_ctrl_sl[0](PERIPHCTRL4[25]). 0: r channel enable; 1: The r channel is powered off. vdac_ctrl_sl[1](PERIPHCTRL4[26]). 0: g channel is enabled; 1: g channel is powered off. vdac_ctrl_sl[2](PERIPHCTRL4[27]). 0: b channel is enabled; 1: Channel b is powered off. vdac_ctrl_sl[3](PERIPHCTRL4[28]). 0: cvbs0 channel enable; 1: The cvbs0 channel is powered off. vdac_ctrl_sl[4](PERIPHCTRL4[29]). 0: cvbs1 channel enable; 1: Power off the cvbs1 channel. vdac_ctrl_sl[5](PERIPHCTRL4[30]). 0: cvbs0/1 enabled; 1: cvbs0/1 powered off. vdac_ctrl_sl[6](PERIPHCTRL4[31]). 0: rgb enabled; 1: rgb powered off.
[24:20]	RO	reserved	reserve.
[19]	RW	ram2_ck_gt_en	RAM2 clock gating function is enabled. 0: forbidden; 1: enable.

[18] RW	ram1_ck_gt_en		RAM1 clock gating function is enabled. 0: forbidden; 1: enable.
[17] RW	ram0_ck_gt_en		RAM0 clock gating function is enabled. 0: disable; 1: enable.
[16] RW	cbar_en		cbar_en Output enable. 0: forbidden; 1: enable.
[15] RW	mdu_ddrt_mst_sel		MDU and DDRT function selection. 0: MDU is enabled, DDRT is not enabled; 1: DDRT is enabled, MDU is not enabled.
[14] RO		reserved	reserve.
[13:12] RW	ssp_cs_sel		SSP chip select selection. 00: chip selection 0; 01: chip selection 1; 10: reserved; 11: reserved.
[11:2] RO		reserved	reserve.
[1] RW	uart1_rts_ctrl		UART1 RTS output control. 0: Normal output; 1: Negative output.
[0]	RO	reserved	reserve.

PERIPHCTRL5

PERIPHCTRL5 is peripheral control register 5 (Timeout control register 0 of MEDIA0 bus Master port).

Offset Address	Register Name	Total Reset Value
0x0040	PERIPHCTRL5	0x0000_0000



Bits	Access Name	Description
[31] RW	count_en_media0_ 0:	Timeout count enable for JPGE port. disable; port1 1: enable.
[30:16] RW	JPGE port. over_value_media0_port	The timeout count value for the 1 count value=over_value_media0_port1x2.
[15] RW	count_en_media0_0:	Timeout count enable for VENC port. disable; port0 1: enable.
[14:0] RW	port. over_value_media0_port	The timeout count value for the VENC 0 count value=over_value_media0_port0x2.

SC_LOCKEN

SC_LOCKEN is the lock register for key system control registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Lock register for key system control registers. The involved registers include SC_CTRL, SC_SYSRES, SC_SYSSTAT, SC_PLLCTRL, SC_PLLFCTRL, PERIPHCTRL0, PERIPHCTRL1. Write 0x1ACC_E551 to this register to open the write permission of all registers, and write other values to close the write permission. Reading this register returns the status of the lock rather than the value written to this register. 0x0000_0000: Allow the above write access (unlocked); 0x0000_0001: Forbid the above write access (locked).

PERIPHCTRL6

PERIPHCTRL6 is peripheral control register 6 (Timeout control register 1 of MEDIA0 bus Master port).

Offset Address	Register Name	Total Reset Value
0x0048	PERIPHCTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	----	over_value_media0_port3															----	over_value_media0_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

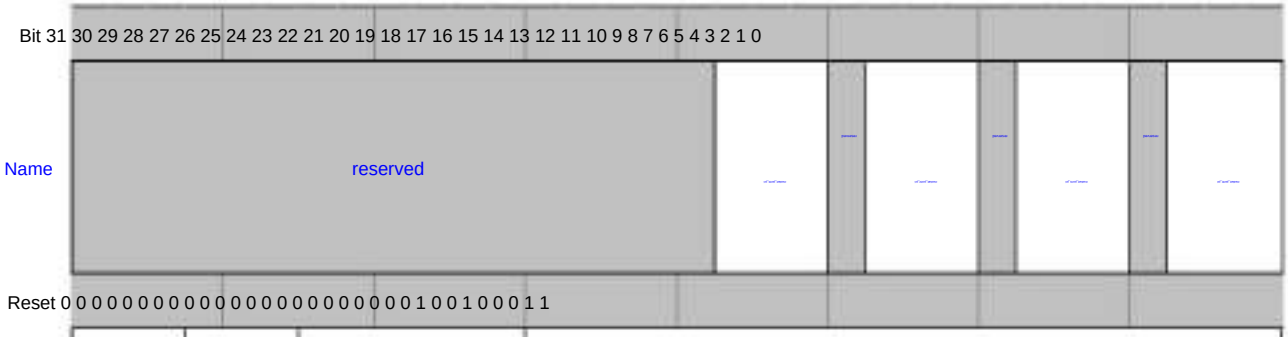
Bits	Access	Name	Description
[31]	RW	count_en_media0_	Timeout count enable for MDU_DDRT port. 0: disable; port3 1: enable.
[30:16]	RW	over_value_media0_port3	The timeout count value of the MDU_DDRT port. count value=over_value_media0_port3x2.

[15] RW		count_en_media0_ 0:	Timeout count enable for JPGD port. disable; port2 1: enable.
[14:0] RW		port. over_value_media0_port	The timeout count value for the JPGD 2 count value=over_value_media0_port2x2.

PERIPHCTRL9

PERIPHCTRL9 is the peripheral control register 9 (the MEDIA0 bus Master port priority control register).

Offset Address	Register Name	Total Reset Value
0x0054	PERIPHCTRL9	0x0000_0123

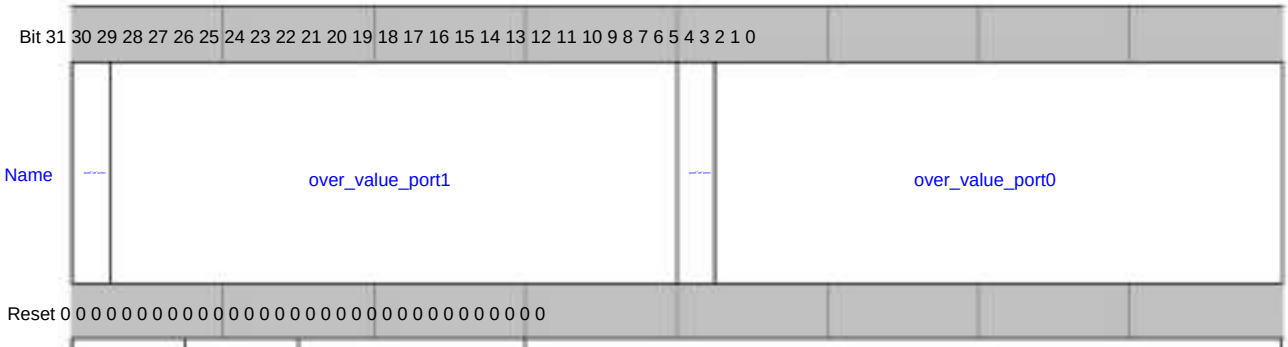


Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	media0_port3_pri	MD/DDRT priority. 3 is the highest priority.
[11]	RO	reserved	reserve.
[10:8]	RW	media0_port2_pri	JPGD priority. 3 is the highest priority.
[7]	RO	reserved	reserve.
[6:4]	RW	media0_port1_pri	JPGE priority. 3 is the highest priority.
[3]	RO	reserved	reserve.
[2:0]	RW	media0_port0_pri	VENC priority. 3 is the highest priority.

PERIPHCTRL10

PERIPHCTRL10 is peripheral control register 10 (system bus Master port Timeout control register 0).

Offset Address	Register Name	Total Reset Value
0x0058	PERIPHCTRL10	0x0000_0000

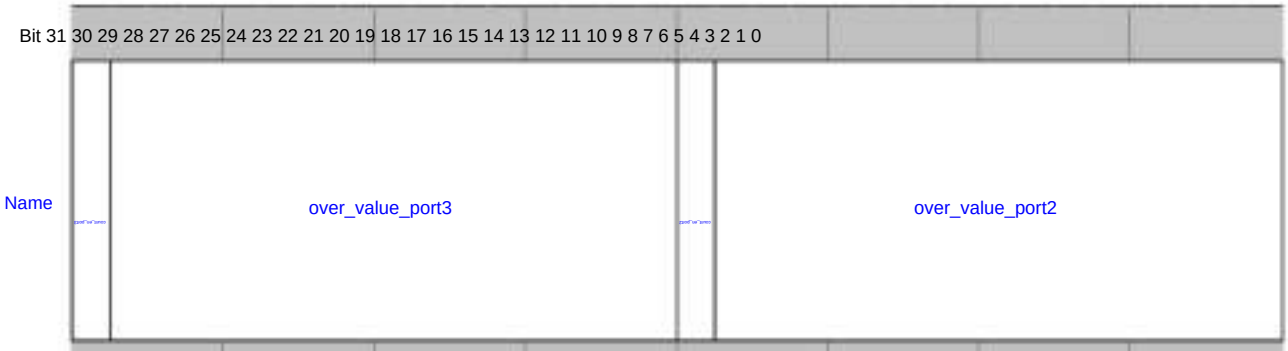


Bits	Access	Name	Description
[31]	RW	count_en_port1	Timeout count enable for AHB bridge 1 port. 0: forbidden; 1: enable.
[30:16]	RW	over_value_port1	The timeout count value of AHB bridge 1 port. count value = over_value_port1x2.
[15]	RW	count_en_port0	Timeout count enable for AHB bridge 0 port. 0: forbidden; 1: enable.
[14:0]	RW	over_value_port0	Timeout count value of AHB bridge 0 port. count value = over_value_port0x2.

PERIPHCTRL11

PERIPHCTRL11 is peripheral control register 11 (system bus Master port Timeout control register 1).

Offset Address	Register Name	Total Reset Value
0x005C	PERIPHCTRL11	0x0000_0000

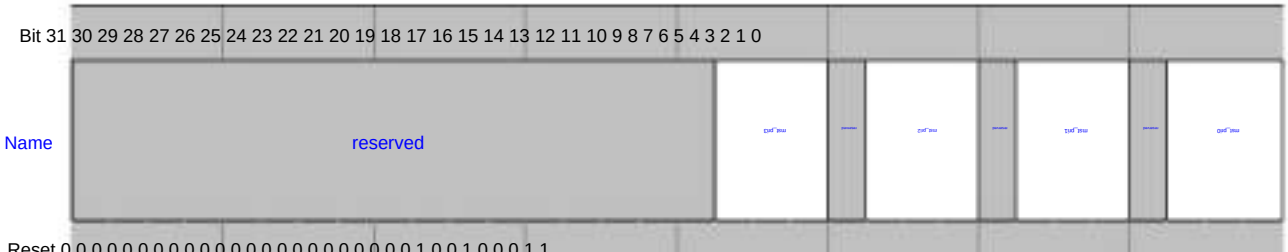


Bits	Access	Name	Description
[31]	RW	count_en_port3	Timeout count enable for A9 port. 0: forbidden; 1: enable.
[30:16]	RW	over_value_port3	Timeout count value of A9 port. count value = over_value_port3x2.
[15]	RW	count_en_port2	Timeout count enable for IVE port. 0: forbidden; 1: enable.
[14:0]	RW	over_value_port2	The timeout count value for the IVE port. count value = over_value_port2x2.

PERIPHCTRL13

PERIPHCTRL13 is peripheral control register 13 (system bus Master port priority control register).

Offset Address	Register Name	Total Reset Value
0x0064	PERIPHCTRL13	0x0000_0123



Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.

[14:12] RW	mst_pri3		A9 priority. 3 is the highest priority.
[11] RO		reserved	reserve.
[10:8] RW	mst_pri2		IVE priority. 3 is the highest priority.
[7]	RO	reserved	reserve.
[6:4] RW	mst_pri1		AHB bridge 1 priority. 3 is the highest priority.
[3]	RO	reserved	reserve.
[2:0] RW	mst_pri0		AHB bridge 0 priority. 3 is the highest priority.

PERIPHCTRL14

PERIPHCTRL14 is the peripheral control register 14 (system bus Slave port priority control register).

Offset Address	Register Name	Total Reset Value
0x0068	PERIPHCTRL14	0x0012_3456

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	slave_priority_s4	SYS AXI s4 port MDDRC0 bus access priority. 3 is the highest priority.
[11]	RO	reserved	reserve.
[10:8]	RW	slave_priority_s3	SYS AXI s3 port APB_MEDIA bus access priority. 3 is the highest priority.
[7]	RO	reserved	reserve.

[6:4] RW	slave_priority_s2		SYS AXI s2 port APB_SYS bus access priority. 3 is the highest priority.
[3]	RO	reserved	reserve.
[2:0] RW	slave_priority_s1		SYS AXI s1 Port AHB bus access priority. 3 is the highest priority.

PERIPHCTRL15

PERIPHCTRL15 is the peripheral control register 15 (CHIP ID register).

Offset Address	Register Name	Total Reset Value
0x006C	PERIPHCTRL15	

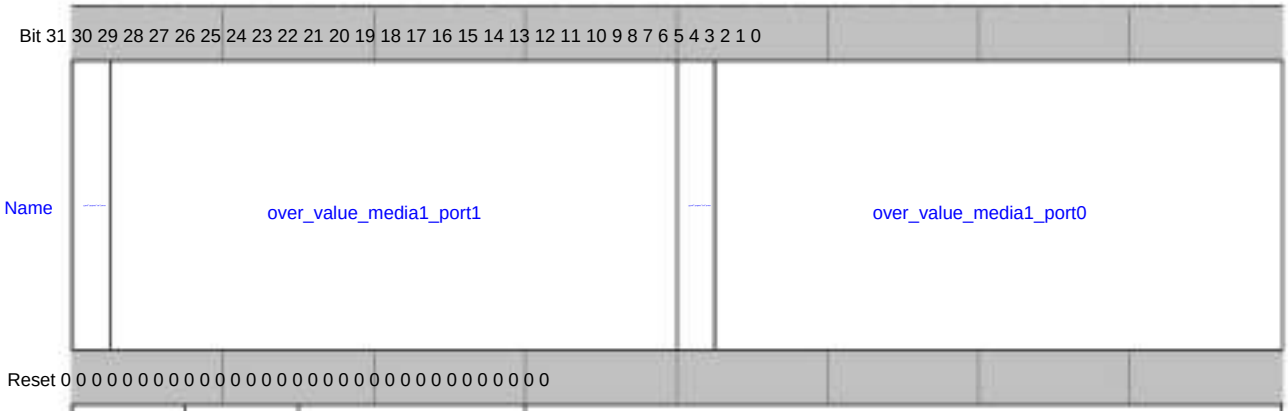
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	chipid
Reset	? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?	? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RO	chipid	Chip version description. 00: reserved; 01ÿHi3515Aÿ 10ÿHi3515Cÿ 11ÿHi3520Dÿ

PERIPHCTRL16

PERIPHCTRL16 is the peripheral control register 16 (the MEDIA1 bus Master port Timeout control register 0).

Offset Address	Register Name	Total Reset Value
0x0070	PERIPHCTRL16	0x0000_0000

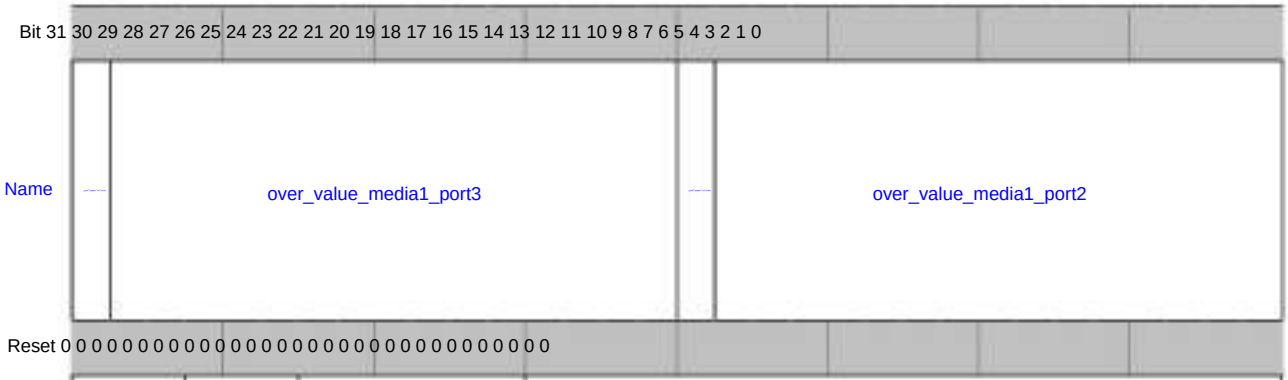


Bits	Access Name	Description
[31] RW	count_en_media1_ 0:	Timeout count enable for TDE port. disable; port1 1: enable.
[30:16] RW	TDE port.	The timeout count value for the over_value_media1_port1 count value = over_value_media1_port1x2.
[15] RW	enabled. count_en_media1_0: disable; port0	The timeout counting of VPSS port is 1: enable.
[14:0] RW	VPSS port.	The timeout count value for the over_value_media1_port0 count value = over_value_media1_port0x2.

PERIPHCTRL17

PERIPHCTRL17 is the peripheral control register 17 (MEDIA1 bus Master port Timeout control register 1).

Offset Address	Register Name	Total Reset Value
0x0074	PERIPHCTRL17	0x0000_0000

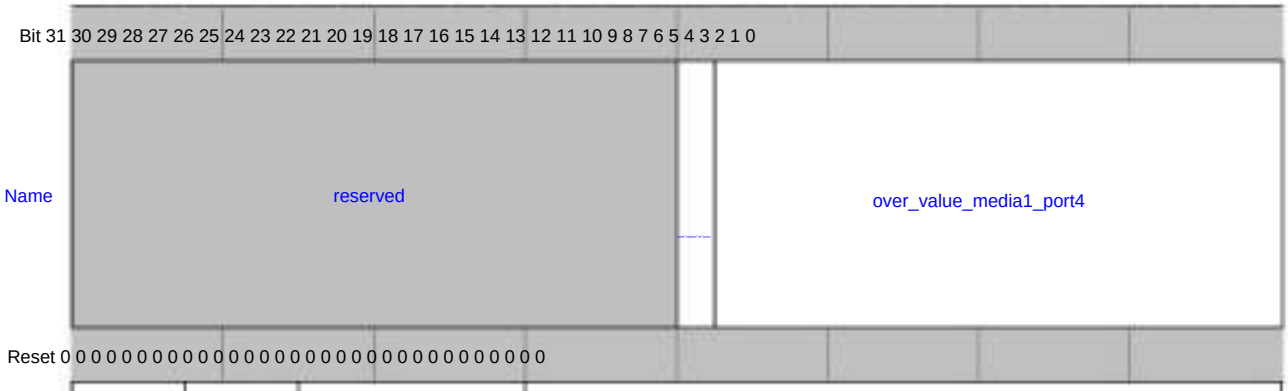


Bits	Access Name	Description
[31] RW	count_en_media1_ 0: port3	Timeout count enable for VOIE port. disable; 1: enable.
[30:16] RW	port.	The timeout count value of the VOIE over_value_media1_port3 count value = over_value_media1_port3x2.
[15] RW	enabled. count_en_media1_ 0: disable; port2	The timeout counting of VCMP ports is 1: enable.
[14:0] RW	over_value_media1_port2 count	Timeout count value for VCMP ports. value = over_value_media1_port2x2.

PERIPHCTRL18

PERIPHCTRL18 is peripheral control register 18 (Timeout control register 2 of MEDIA1 bus Master port).

Offset Address	Register Name	Total Reset Value
0x0078	PERIPHCTRL18	0x0000_0000

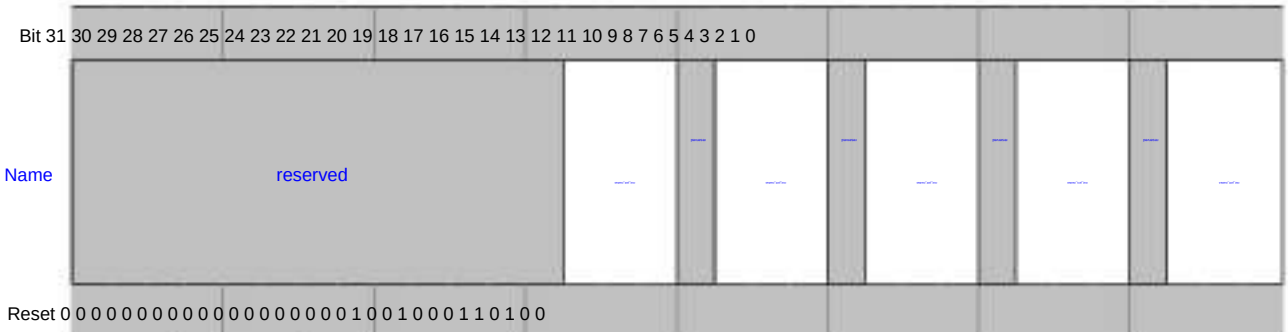


Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15] RW		count_en_media1_ 0:	Timeout count enable for AIO port. disable; port4 1: enable.
[14:0] RW		port. over_value_media1_port4	The timeout count value for the AIO count value=over_value_port4_media1x2.

PERIPHCTRL19

PERIPHCTRL19 is peripheral control register 19 (Master port priority control register of MEDIA1 bus).

Offset Address	Register Name	Total Reset Value
0x007C	PERIPHCTRL19	0x0000_1234



Bits	Access Name		Description
[31:19] RO		reserved	reserve.
[18:16] RW	mst_pri4_media1		AIO priority. 7 is the highest priority.

[15] RO		reserved	reserve.
[14:12] RW	mst_pri3_media1		VOIE priority. 7 is the highest priority.
[11] RO		reserved	reserve.
[10:8] RW	mst_pri2_media1		VCMP priority. 7 is the highest priority.
[7]	RO	reserved	reserve.
[6:4] RW	mst_pri1_media1		TDE priority. 7 is the highest priority.
[3]	RO	reserved	reserve.
[2:0] RW	mst_pri0_media1		VPSS priority. 7 is the highest priority.

PERIPHCTRL20

PERIPHCTRL20 is Peripheral Control Register 20 (USB Control Register).

Offset Address	Register Name	Total Reset Value
0x0080	PERIPHCTRL20	0x0003_33A8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	0	1	0	1	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20]	RW	preamble_sel	The number of full-speed idle cycles after the full-speed signal preamble packet is selected. 0: There are 5 full-speed idle cycles after the leading packet of the full-speed signal; 1: There are 4 full-speed idle cycles after the full-speed signal leading packet.

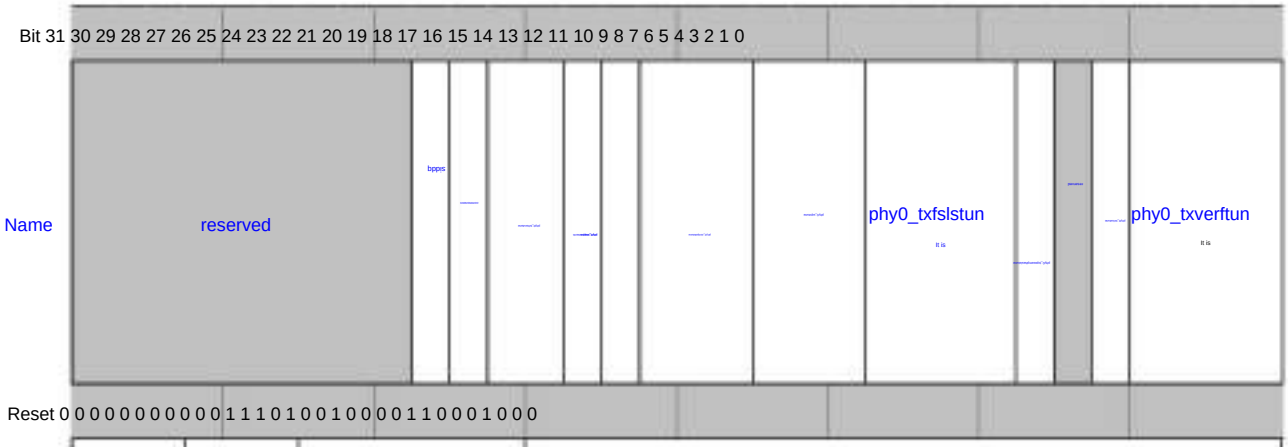
[19]	RW	ovr_merge_en	The two ports share the same overcurrent signal enable (that is, the overcurrent signal of the port whose [phy1_ovrcur_en] or [phy0_ovrcur_en] is 1). 0: forbidden; 1: enable.
[18]	RW	pwr_merge_en	Both [phy1_pwr_en] and [phy0_pwr_en] are enabled as long as one port is powered on. 0: forbidden; 1: enable.
[17]	RW	usbovr_p_ctrl	Polarity control for overcurrent protection. 0: Low level active; 1: Active high.
[16]	RW	usbpwr_p_ctrl	Power supply enable polarity control. 0: Active at low level; 1: Active at high level.
[15]	RW	phy1_ovrcur_en	PHY1 overcurrent protection shutdown control. 0: close the overcurrent protection; 1: Enable overcurrent protection.
[14]	RW	phy0_ovrcur_en	PHY0 overcurrent protection shutdown control. 0: close the overcurrent protection; 1: Enable overcurrent protection.
[13]	RW	phy1_pwr_en	PHY1 power shutdown control. 0: Turn off the power; 1: Enable the power output of the controller.
[12]	RW	phy0_pwr_en	PHY0 power is off. 0: turn off the power; 1: Enable the power output of the controller.
[11:10]	RO	reserved	reserve.
[9]	RW	ss_ena_incr16_i	AHB burst16 enable signal. 0: forbidden; 1: enable.
[8]	RW	ss_ena_incr8_i	AHB burst8 enable signal. 0: forbidden; 1: enable.

[7] RW	ss_ena_incr4_i		AHB burst4 enable signal. 0: forbidden; 1: enable.
[6] RW		signal. ss_ena_incrx_align 0: disable; _i 1: enable.	burst alignment enable
[5] RW		when over-current. ss_autoppd_on_ove 0: disabled; rcur_en_i	Automatically shut down the port power enable 1: enable.
[4]	RO	reserved	reserve.
[3] RW	ulpi_bypass_on		ULPI bypass control. Must be set to 1. 0ÿWolf modeÿ 1ÿutmi modeÿ
[2] RW	app_start_clk_i		OHCI clock control signal. 0: OHCI works normally; 1: Turn on OHCI clock in Suspend mode.
[1] RW	ohci_susp_lgcy_i	OHCI suspend strap input signal.	
[0] RW	wordinterface		UTMI interface data width selection signal. 0ÿ8bitÿ 1ÿ16bitÿ

PERIPHCTRL21

PERIPHCTRL21 is Peripheral Control Register 21 (USB PHY Control Register 0).

Offset Address	Register Name	Total Reset Value
0x0084	PERIPHCTRL21	0x001D_2188



Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22]	RW	siddq	Analog shutdown test enable signal for the PHY. 0: Do not turn off the analog power supply; 1: Turn off the analog power supply. Note: The default is **0, and it needs to be 0 during BIST** testing .
[21]	RW	commononn	Whether XO BIAS BANDGAP PLL works when PHY is in suspend. The default is 0. 0: clk48m_ohci output is valid at any time (including suspend); 1: clk48m_ohci output is valid except when suspend.
[20:19]	RW	phy0_txhsxvtune	DP/DM crossover voltage regulation. 00: reserved; 01ÿ-15mVÿ 10ÿ+15mVÿ 11: Reserved.
[18]	RW	phy0_sleepm	Sleep mode control for port 0. 0: sleep mode; 1: normal mode.
[17]	RW	phy0_loopbackenb	must be configured as 0. Enable signal for loopback test (loopback to D+D-) of phy0.

[16:14] RW	phy0_compdistune		HOSDISCONNECT threshold level debug signal for PHY0. 000ÿ-6%ÿ 001ÿ-4.5%ÿ 010ÿ-3%ÿ 100: default value; 101ÿ+1.5%ÿ 110ÿ+3%ÿ 111ÿ+4.5%ÿ Other: reserved.
[13:11] RW	phy0_sqrxtune		Squelch circuit debug signal for PHY0. 000ÿ+20%ÿ 001ÿ+15%ÿ 010ÿ+10%ÿ 011ÿ+5%ÿ 100: default value; 101ÿ-5%ÿ 110ÿ-10%ÿ 111ÿ-15%ÿ
[10:7] RW	phy0_txfslstune		FS LS impedance debug signal for PHY0. 0x0ÿ+5%ÿ 0x1ÿ+2.5%ÿ 0x3: default value; 0x7ÿ-2.5%ÿ 0xFÿ-5%ÿ Other: reserved.
[6] RW		signal. phy0_txpreemphasi stun	HS mode of PHY0 sends pre-emphasis enable 0: disable; 1: enable.
[5]	RO	reserved	reserve.
[4] RW	phy0_txrisetune		High-speed signal rise/fall time adjustment for PHY0. 0: default value; 1ÿ-8%ÿ

[3:0]	RW	phy0_txverftune	DC level adjustment in HS mode of PHY0. 0x0ÿ-10%ÿ 0x1ÿ-8.75%ÿ 0x2ÿ-7.5%ÿ 0x3ÿ-6.25%ÿ 0x4ÿ-5%ÿ 0x5ÿ-3.75%ÿ 0x6ÿ-2.5%ÿ 0x7ÿ-1.25%ÿ 0x8: default value; 0x9ÿ+1.25%ÿ 0xAÿ+2.5%ÿ 0xBÿ+3.7%ÿ 0xCÿ+5%ÿ 0xDÿ+6.25%ÿ 0xEÿ+7.5%ÿ 0xFÿ+8.75%ÿ

PERIPHCTRL22

PERIPHCTRL22 is Peripheral Control Register 22 (USB PHY Control Register 1).

Offset Address	Register Name	Total Reset Value
0x0088	PERIPHCTRL22	0x701D_2188

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.

[20:19]	RW	phy1_txhsxvtune	DP/DM crossover voltage regulation. 00: reserved; 01ÿ-15mVÿ 10ÿ+15mVÿ 11: Default value.
[18]	RW	phy1_sleepm	Sleep mode control for port 1. 0: sleep mode; 1: normal mode.
[17]	RW	phy1_loopbackenb The default value is 0, must be configured as 0.	Enable signal for loopback test (loopback to D+D-) of PHY1.
[16:14]	RW	phy1_compdistune	HOSDISCONNECT threshold level debug signal for PHY1. 000ÿ-6%ÿ 001ÿ-4.5%ÿ 010ÿ-3%ÿ 100: default value; 101ÿ+1.5%ÿ 110ÿ+3%ÿ 111: +4.5%; Others: Reserved.
[13:11]	RW	phy1_sqrxtune	Squelch circuit debug signal for PHY1. 000ÿ+20%ÿ 001ÿ+15%ÿ 010ÿ+10%ÿ 011ÿ+5%ÿ 100: default value; 101ÿ-5%ÿ 110ÿ-10%ÿ 111ÿ-15%ÿ
[10:7]	RW	phy1_txfslstune	FS LS impedance debug signal for PHY1. 0x0ÿ+5%ÿ 0x1ÿ+2.5%ÿ 0x3: default value; 0x7ÿ-2.5%ÿ 0xFÿ-5%ÿ Other: reserved.

[6] RW		phy1_txpreemphasi	HS mode of PHY1 sends pre-emphasis enable signal. The default value is 0. 0: disable; stun 1: enable.
[5]	RO	reserved	reserve.
[4] RW	phy1_txrisetune		High-speed signal rise/fall time adjustment for PHY1. 0: default value; 1ÿ-8%ÿ
[3:0] RW	phy1_txvreftune		DC level regulation in HS mode of PHY1. 0x0ÿ-10%ÿ 0x1ÿ-8.75%ÿ 0x2ÿ-7.5%ÿ 0x3ÿ-6.25%ÿ 0x4ÿ-5%ÿ 0x5ÿ-3.75%ÿ 0x6ÿ-2.5%ÿ 0x7ÿ-1.25%ÿ 0x8: default value; 0x9ÿ+1.25%ÿ 0xAÿ+2.5%ÿ 0xBÿ+3.7%ÿ 0xCÿ+5%ÿ 0xDÿ+6.25%ÿ 0xEÿ+7.5%ÿ 0xFÿ+8.75%ÿ

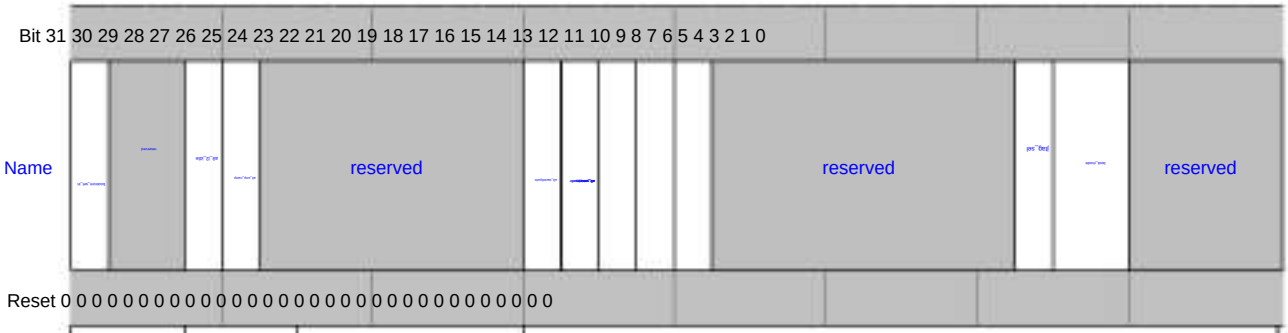
SYSSTAT

SYSSTAT is the system status register (PLL_LOCK).

Offset Address: 0x008C

Register Name: SYSSTAT

Total Reset Value: 0x0000_0000



Bits	Access	Name	Description
[31]	RO	bootrom_sel_in	Indicates whether to boot from bootrom. 0: Do not start from bootrom; 1: Start from bootrom.
[30:29]	RO	reserved	reserve.
[28]	RO	a9_l2_idle	Indicates L2 cache activity status. 0: non-idle state; 1: IDLE state.
[27]	RO	a9_smp_namp	Indicates whether the Cortex-A9 processor is in balanced or unbalanced mode. 0: unbalanced; 1: balanced.
[26:20]	RO	reserved	reserve.
[19]	RO	a9_standbywfe	Indicates whether the Cortex-A9 processor is in WFE state. 0: not in WFE state; 1: In WFE state.
[18]	RO	a9_standbywfi	Indicates whether the Cortex-A9 processor is in WFI state. 0: not in WFI state; 1: In WFI state.
[17]	RO	a9_pmupriv	Indicates the status of the Cortex-A9 processor. 0: in user mode; 1: in privileged mode.
[16]	RO	a9_secure	Indicates the Cortex-A9 processor security status. 0: In the Non-secure state; 1: In Secure state.

[15] RO		sfc_addr_mode	SPI FLASH default working address mode. 0: 3Byte address mode; 1: 4Byte address mode.
[14:7] RO	reserved		reserve.
[6]	RO jtag_sel		The debug mode selected by the chip. 0: debug A9; 1ÿdebug SATA PHYÿ
[5:4] RO	boot_mode		The boot mode selected by the chip. 00: Boot from SPI Flash; Others: Reserved.
[3:0] RO	reserved		reserve.

PERIPHCTRL23

PERIPHCTRL23 is peripheral control register 23 (MDDRC out-of-order configuration outtodr_ctrl register).

Offset Address	Register Name	Total Reset Value
0x0090	PERIPHCTRL23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21] RO		reserved	reserve.
[20] RW	a9_ctrl		A9 Whether access to DDR is allowed out of order. 0: Disorder is not allowed; 1: Disorder is allowed.
[19:18] RO		reserved	reserve.
[17] RW	ive_ctrl		IVE Whether access DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[16] RO		reserved	reserve.

[15] RW ddrtest_ctrl			Whether AIO accesses DDR is allowed out of sequence. 0: Disorder is not allowed; 1: Out of order is allowed.
[14] RW voie_ctrl			Whether VOIE is allowed to access DDR out of order. 0: Disorder is not allowed; 1: Disorder is allowed.
[13] RW vcmp_ctrl			Whether VCMP accesses DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[12] RO		reserved	reserve.
[11] RW tde_ctrl			Whether TDE accesses DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[10] RW vpss_ctrl			Whether VPSS accesses DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[9:8] RO		reserved	reserve.
[7] RW mdu_ctrl			Whether MDU/DDRTEST access DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[6] RW jpgd_ctrl			Whether JPGD accesses DDR to allow out-of-sequence. 0: Disorder is not allowed; 1: Disorder is allowed.
[5] RW jpge_ctrl			Whether JPGE accesses DDR to allow disorder. 0: Disorder is not allowed; 1: Out of order is allowed.
[4]	RO	reserved	reserve.
[3] RW vedu_ctrl			Whether VEDU accesses DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.
[2]	RO	reserved	reserve.
[1] RW vicap_ctrl			Whether VICAP is allowed to access DDR out of order. 0: Disorder is not allowed; 1: Out of order is allowed.

[0] RW vou_ctrl			Whether VOU accesses DDR is allowed out of order. 0: Disorder is not allowed; 1: Out of order is allowed.

PERIPHCTRL24

PERIPHCTRL24 is the peripheral control register 24 (FE PHY address configuration register).

Offset Address	Register Name	Total Reset Value
0x0094	PERIPHCTRL24	0x0000_1000

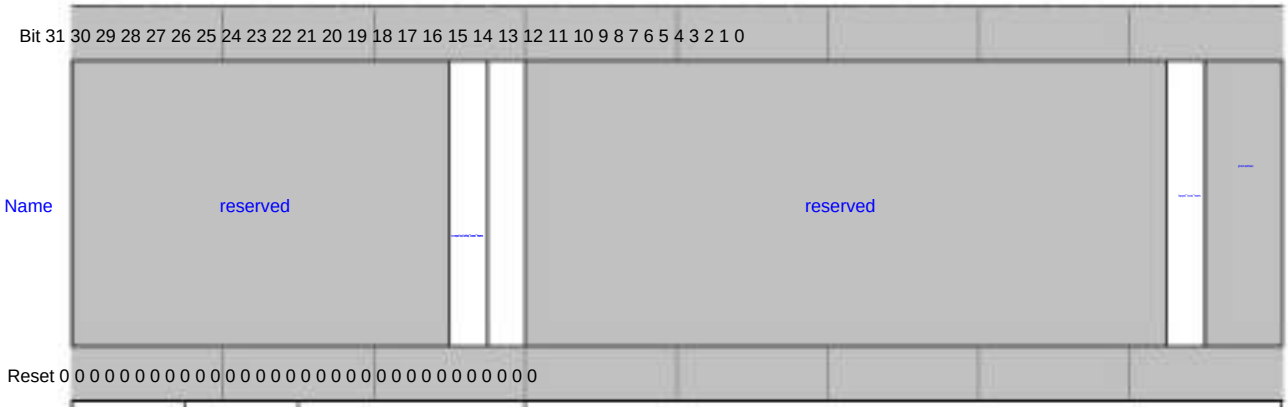
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														fephy_ad	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	fephy_led_ctrl	FE PHY led light polarity control. 0: Polarity is not reversed; 1: The polarity is reversed.
[11:9]	RO	reserved	reserve.
[8]	RW	fephy_sel	FE PHY selection. 0: Select the internally integrated FE PHY; 1: Select external FE PHY.
[7:5]	RO	reserved	reserve.
[4:0]	RW	fephy_ad	PHY address of internally integrated FE PHY

PERIPHCTRL25

PERIPHCTRL25 is Peripheral Control Register 25 (SATA PHY Control Register 1).

Offset Address	Register Name	Total Reset Value
0x0098	PERIPHCTRL25	0x0000_0000

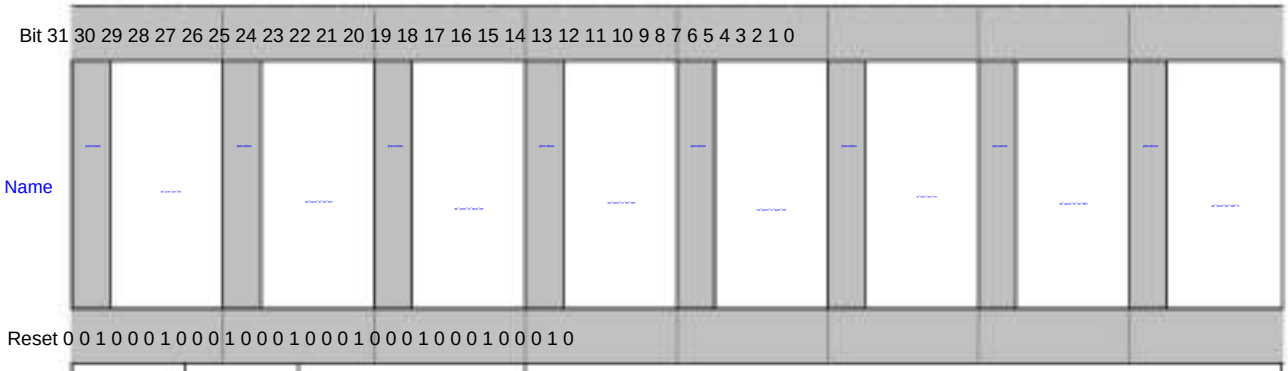


Bits	Access Name		Description
[31:22] RO		reserved	reserve.
[21] RW		test coverage. It is sata_test_byp_mod	All the input interfaces of SATA in the enable ASIC are connected to the output terminals through pure combinational logic to improve the interface 0: disabled; 1: enable.
[20] RW		disable; sata_test_burnin_m	SATA burn-in test mode is enabled. 0: 1: enable. ode Note: Enable as many internal logic flips as possible, **use** with [sata_test_byp_mode] signal during burn-in test .
[19:3] RO		reserved	reserve.
[2] RW	sata_test_pddq		SATA PHY power on and off control. 0: no power off; 1: Power off.
[1:0] RO		reserved	reserve.

PERIPHCTRL28

PERIPHCTRL28 is the peripheral control register 28 (IO control register 0).

Offset Address	Register Name	Total Reset Value
0x00A4	PERIPHCTRL28	0x2222_2222



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	spi_sclk_ioctrl_ds	spi_sclk Output drive capability selection. 000: 0mA (High Z); 001ÿ3mAÿ 010ÿ4mAÿ 011: reserved; 100: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ
[27]	RO	reserved	reserve.
[26:24]	RW	aio_ws_tx_ioctrl_d 011ÿ ÿÿÿ s	aio_ws_tx output drive capability selection. 000ÿ0mA(High Z)ÿ 001ÿ3mAÿ 010ÿ4mAÿ 100: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ
[23]	RO	reserved	reserve.

[22:20] RW		aio_bclk_tx_ioctrl_ ds 011ÿ7mAÿ	aio_bclk_tx output drive capability selection (@SS,125ÿ 2.97V/1.08V Io1 at 0.4V). 000ÿ0mA(High Z)ÿ 001ÿ 3mA(Active)ÿ 010ÿ4mA(Active)ÿ 100ÿ4mAÿ 101ÿ7mAÿ 110ÿ8mA(Active)ÿ 111ÿ11mA(Active)ÿ
[19] RO		reserved	reserve.
[18:16] RW		aio_ws_rx_ioctrl_d 011: s	aio_ws_rx_ioctrl_ds Output drive capability selection. 000ÿ0mA(High Z)ÿ 001ÿ3mAÿ 010: 4mA; reserved; 100: reserved; 101: reserved; 110ÿ8mA(Active)ÿ 111ÿ 11mA(Active)ÿ
[15] RO		reserved	reserve.
[14:12] RW		aio_bclk_rx_ioctrl_ 011: 100: reserved;	aio_bclk_rx Output drive capability selection. 000ÿ0mA(High Z)ÿ 001ÿ3mAÿ 010: 4mA; reserved; ds 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ
[11] RO		reserved	reserve.

[10:8] RW	aio_mclk_ioctrl_ds	100: Reserved;	aio_mclk Output drive capability selection. 000ÿ0mA(High Z)ÿ 001ÿ3mAÿ 010ÿ4mAÿ 011: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ
[7]	RO	reserved	reserve.
[6:4] RW		vga_hs_vs_ioctrl_d 011ÿ12mAÿ s 100ÿ12mAÿ 101ÿ16mAÿ 110ÿ20mAÿ 111ÿ24mAÿ	vga_hs and vga_vs output drive capability selection. 000: 0mA (High Z); 001ÿ4mAÿ 010ÿ8mAÿ
[3]	RO	reserved	reserve.
[2:0] RW		vi_adc_clk_ioctrl_d 011: reserved; s 100: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ	vi_adc_clk Output drive capability selection. 000: 0mA (High Z); 001ÿ3mAÿ 010: 4mA;

PERIPHCTRL29

PERIPHCTRL29 is peripheral control register 29 (IO control register 1).

Offset Address	Register Name	Total Reset Value
0x00A8	PERIPHCTRL29	0x0000_0022

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6:4]	RW	sfc_ioctrl_ds	SFC data pad output drive capability. 000: 0mA (High Z); 001ÿ3mAÿ 010ÿ4mAÿ 011: reserved; 100: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ
[3]	RO	reserved	reserve.
[2:0]	RW	spi_sdo_ioctrl_ds	spi_sdo output drive capability. 000ÿ0mA(High Z)ÿ 001ÿ3mAÿ 010ÿ4mAÿ 011: reserved; 100: reserved; 101: reserved; 110ÿ8mAÿ 111ÿ11mAÿ

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	sysid0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0xD1

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	1	1	0	1	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0xD1.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x20

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x20.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name		Description
[7:0]	RO	sysid3		Reading this register returns 0x35.

3.5 CIPHER

3.5.1 Overview

CIPHER is a module that implements DES (Data Encryption Standard)/3DES and AES (Advanced Encryption Standard) encryption and decryption processing. The implementation of DES/3DES and AES algorithms complies with FIPS46-3/FIPS 197 standards. The working mode of DES/3DES and AES complies with FIPS -81/NIST special800-38a standard.

The CIPHER module is suitable for efficient encryption and decryption processing of large amounts of data, and can support the encryption and decryption of a single packet or the encryption and decryption of multiple packets at a time.

3.5.2 Features

The CIPHER module has the following characteristics:

The AES key length supports 128 bits, 192 bits, and 256 bits. When the key is configured by the chip key management module, the key length only supports 128 bits.

The DES key length supports 64 bits, and the value of 0, 8, 16, 24, 32, 40, 48, and 56 bits is the parity value of each byte, which is not used in actual encryption and decryption operations.

3DES supports the mode of 3 keys and also supports the mode of 2 keys. When the key is configured by the chip key management module, it only supports the mode of 2 keys.

AES supports several working modes of ECB (Electronic CodeBook), CBC (Cipher Block Chaining), 1/8/128- CFB (Cipher FeedBack), 128-OFB (Output FeedBack) and CTR (Counter), and the working mode complies with NIST special800- 38a standard.

DES/3DES supports ECB, CBC, 1/8/64-CFB, 1/8/64-OFB several working modes, and the working mode complies with the FIPS-81 standard.

In ECB, CBC, CFB, OFB, and CTR working modes, it supports the encryption and decryption operations of multiple packets at one time, and also supports the encryption and decryption operations of a single packet at one time.

In the CTR working mode of AES, it supports the encryption and decryption operation of multiple packets at one time, and also supports the encryption and decryption operation of a single packet at one time.

Provide encryption and decryption keys for 8 CPU configurations, which can be configured as 64bits, 128bits, 192bits or 256bitsÿ

Provide 8 keys configured by the chip key management module, fixed at 128bits, and the main CPU cannot read and write. Provide a single packet

encryption and decryption channel and 7 channels of multi-packet encryption and decryption channels. The single-packet encryption and decryption channel can only complete one single-packet encryption and decryption at a time, and the data is written into the channel register by the CPU, and the result is read by the CPU. The multi-packet encryption and decryption channel automatically reads data from DDR by logic, completes encryption and decryption, and then automatically

writes back to DDR. Each channel adopts the weighted round-robin working method. Except the weight value of the single group channel is 1 by default, the weight value of other multi-group channels can be configured.

Any channel can use the same set of keys or a different set of keys.

When the multi-packet channel data is not an integer multiple of the encryption and decryption block, the last data less than one block will not be encrypted

and decrypted. The multi-packet channel supports logical splicing data, that is, the last reserved data of the last linked list data block is less than one encrypted and decrypted packet, and it is not the last linked list data block of the data to be processed. No data filling is required, and the data left over from the linked list data It is spliced together with the data of the next linked list data block for encryption and decryption.

Multi-packet encryption and decryption channels support

byte addresses. The multi-packet encryption and decryption channel supports multi-linked list structure, and supports splicing multiple linked list data. The length of each linked list is represented by 20 bits, that is, the

maximum data volume is 1M-1 byte. Provide interrupt status query, interrupt mask

and interrupt clear functions. Each channel provides individual

interrupt handling and control. Support multi-packet interrupt and aging time interrupt.

3.5.3 Functional description

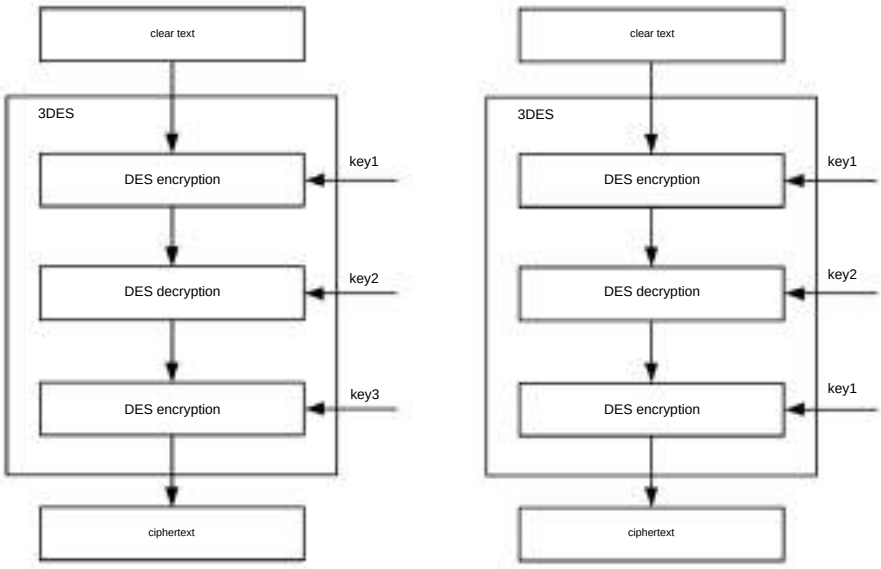
Several working modes supported by DES/3DES and AES algorithms comply with FIPS-81 standard and NIST special800-38a standard respectively. For DES/3DES and AES algorithms, ECB, CBC and CFB work modes are the same, OFB and CTR (only in AES algorithm Including) the working mode is slightly different.

3DES algorithm

3DES supports the operation of 3 keys and 2 keys. The operation of 2 keys can be regarded as a simplified case of 3 keys. The third key (key3) in the operation of 2 keys Both use the first key (key1) instead.

The 3DES encryption operation process of 3 keys and 2 keys is shown in Figure 3-5 .

Figure 3-5 3DES encryption operation with 3 keys and 2 keys

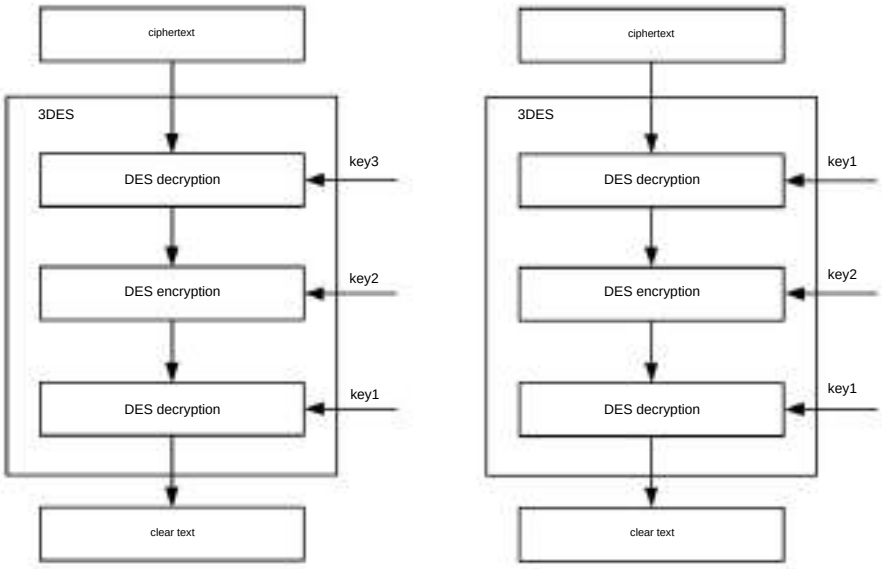


Cryptographic operations with 3 keys

Cryptographic operations with 2 keys

The 3DES decryption operation process of 3 keys and 2 keys is shown in Figure 3-6 .

Figure 3-6 3DES decryption operation with 3 keys and 2 keys



Decryption operation with 3 keys

Decryption operation with 2 keys

ECB mode

In ECB (Electronic CodeBook) mode, the encryption and decryption algorithms are directly applied to each packet data, and the operations of each packet are independent. This feature enables the encryption operation of the plaintext and the decryption operation of the ciphertext to be performed in parallel. The electronic codebook (ECB) modes of AES/DES and 3DES are shown in Figure 3-7 and Figure 3-8 respectively .

Figure 3-7 Electronic Code Book (ECB) mode of AES/DES

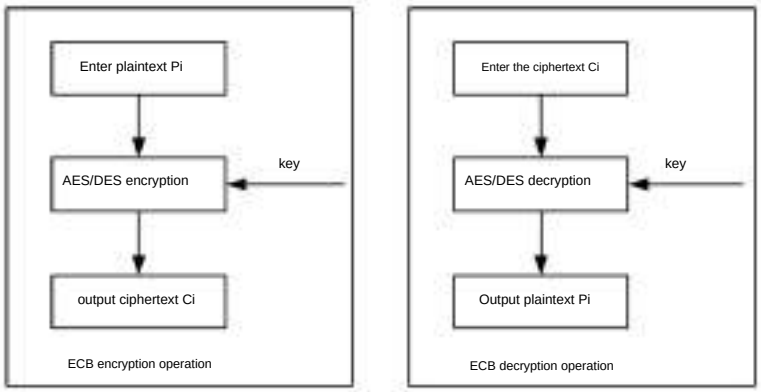
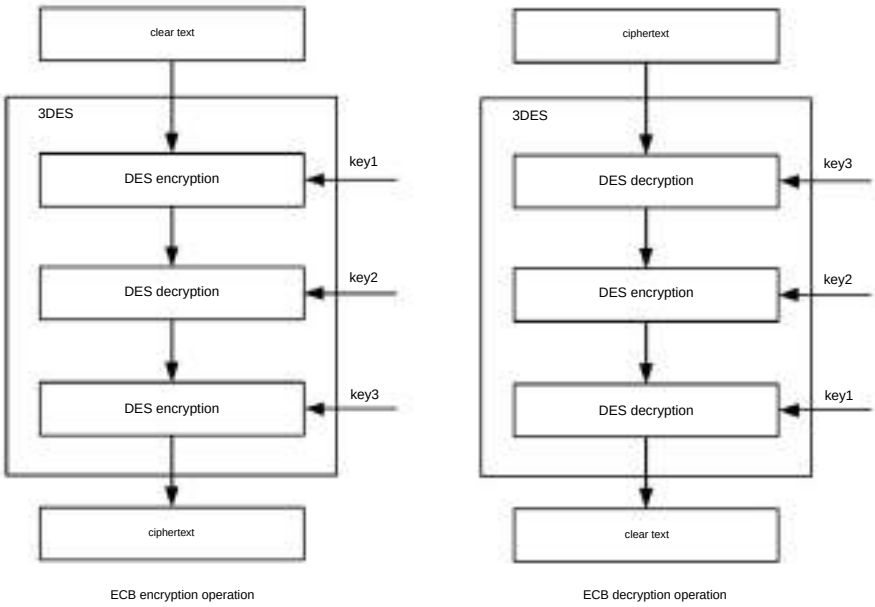


Figure 3-8 Electronic Code Book (ECB) mode of 3DES



CBC mode

In CBC (Cipher Block Chaining) mode, the encrypted input plaintext group needs to be XORed with the input vector IV (Intialization Vector) before entering the encryption operation, and the encryption processing of each plaintext group is the same as that of the previous plaintext group. The results (ie, ciphertext) are correlated, so encryption operations in CBC mode cannot be processed in parallel. However, the decryption operation does not depend on the plaintext output of the previous packet, and can be processed in parallel. The cipher block chaining (CBC) modes of AES/DES and 3DES are shown in Figure 3-9 and Figure 3-10 , respectively .

Figure 3-9 Cipher block chaining (CBC) mode of AES/DES

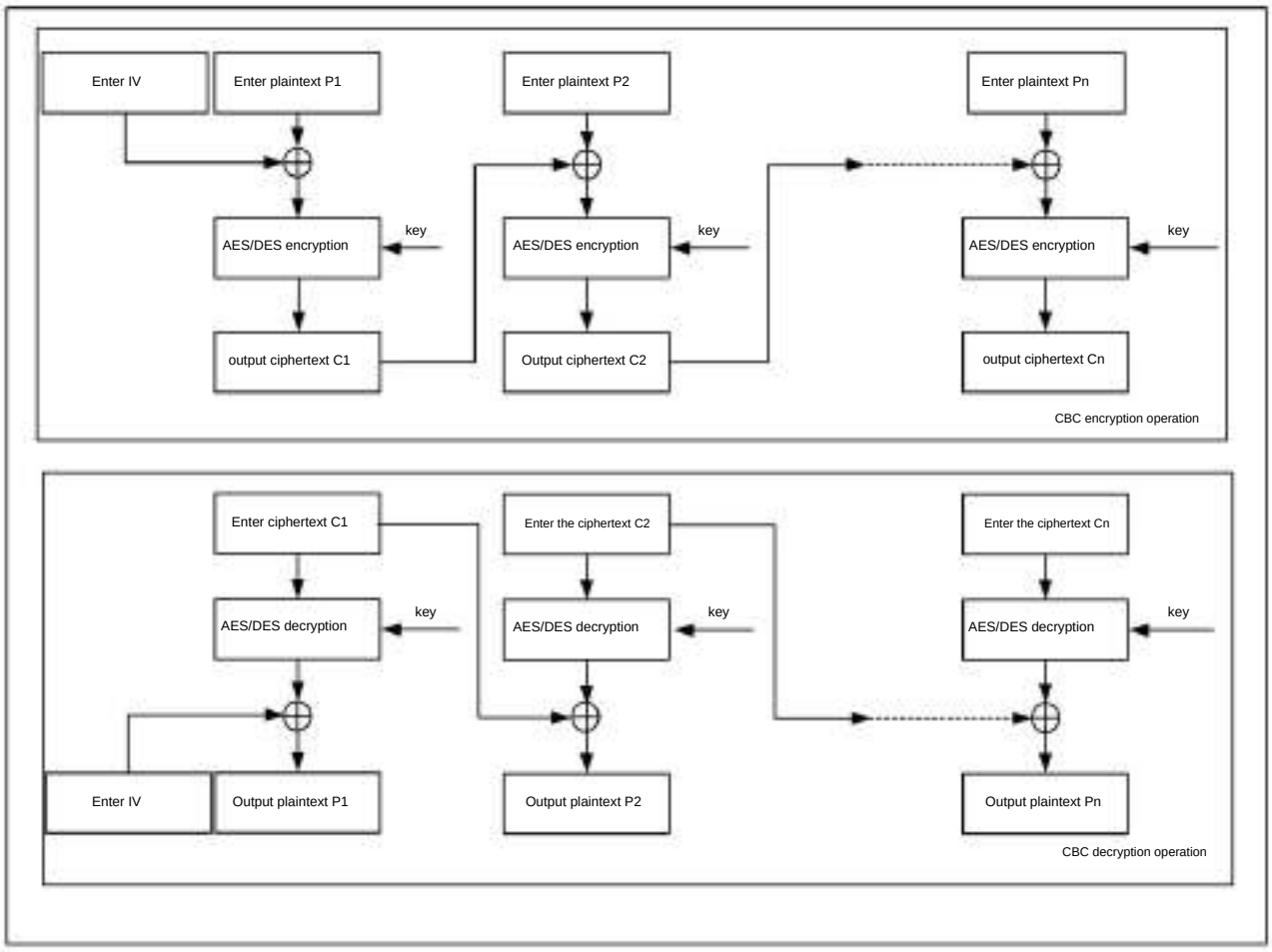
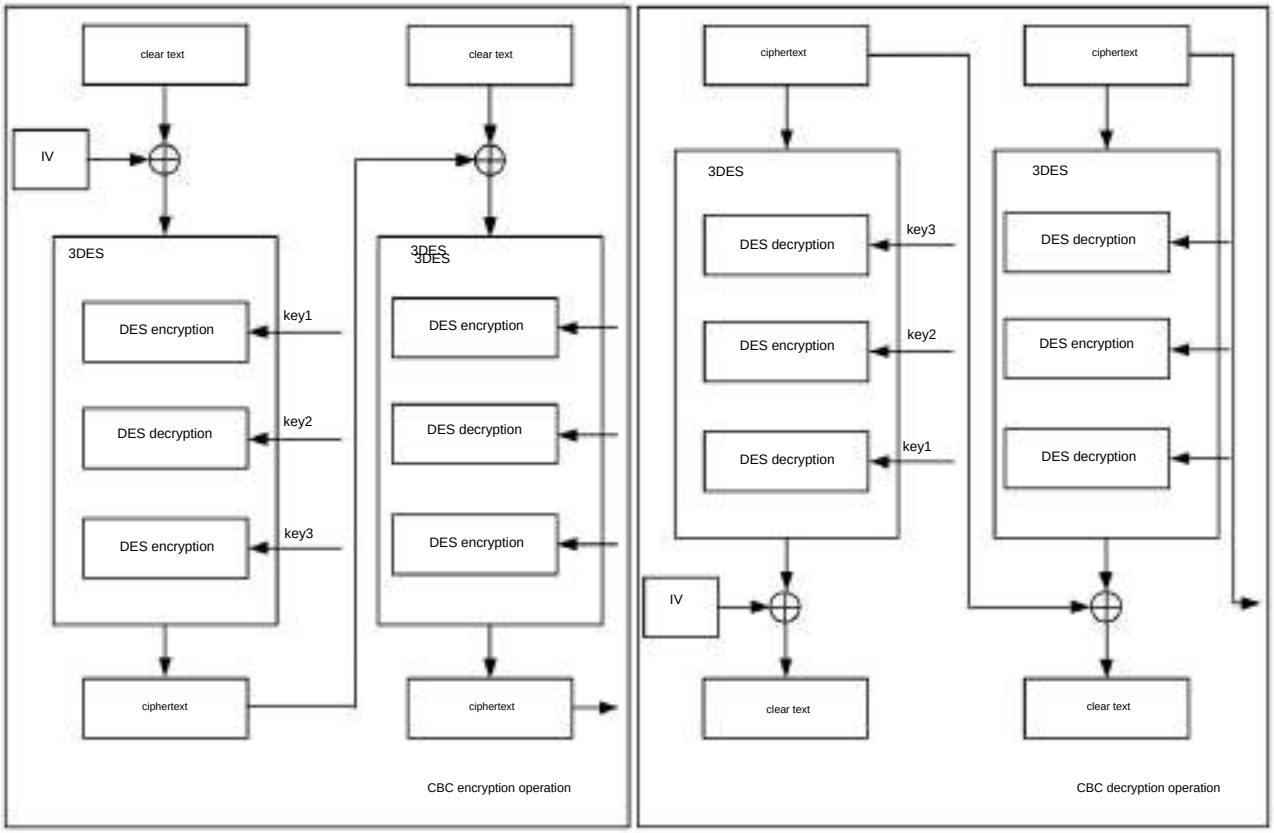


Figure 3-10 Cipher block chaining (CBC) mode of 3DES



CFB mode

The CFB (Cipher FeedBack) mode is a working mode for converting block ciphers into stream ciphers, which can be realized by selecting the number of CFB operations. The number of bits in the shift operation is represented by s bits, and there are the following two situations regarding the s bits:

For DES/3DES, s bits can be 1, 8, or 64 bits. For AES, s bits can be 1

bit, 8 bits, or 128 bits.

The s-bit cipher feedback (CFB) mode of AES/DES and the s-bit cipher feedback (CFB) mode of 3DES are shown in Figure 3-11 and Figure 3-12 respectively .

Figure 3-11 s-bit cipher feedback (CFB) mode of AES/DES

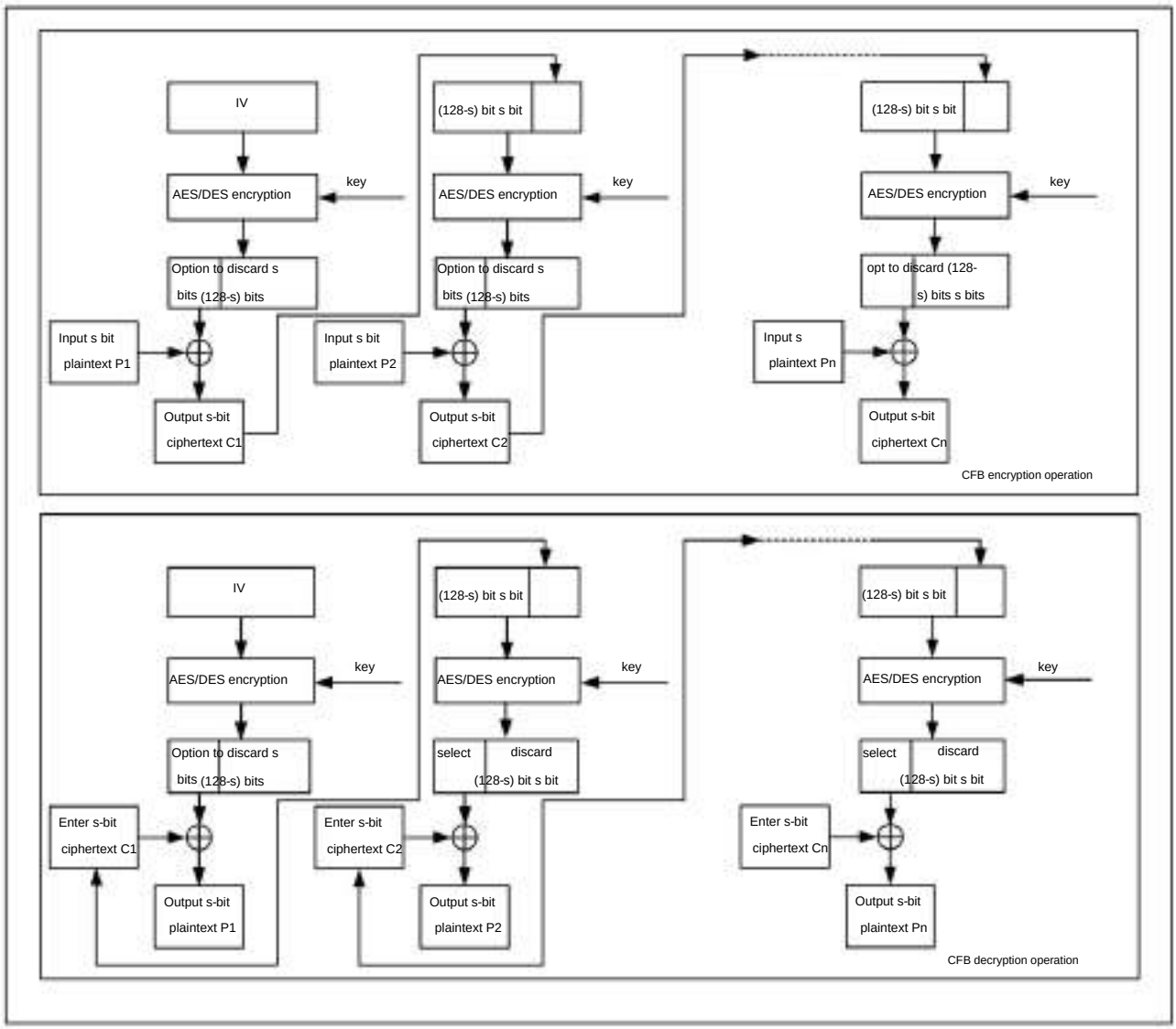
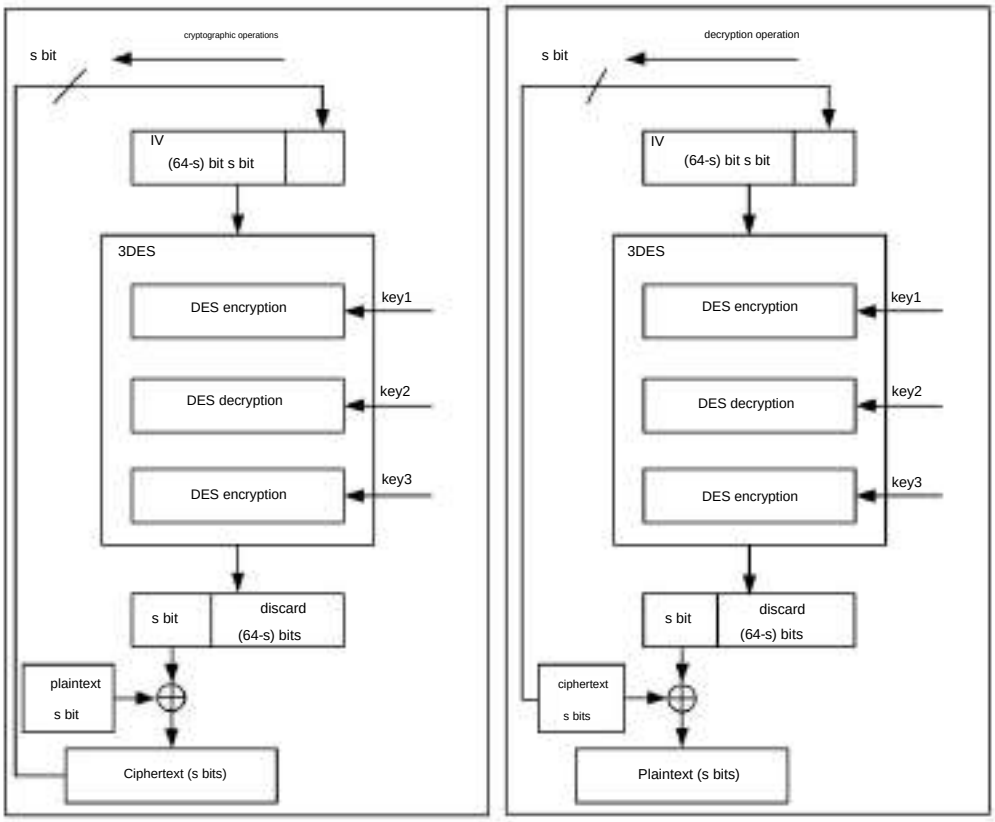


Figure 3-12 s-bit cipher feedback (CFB) mode of 3DES



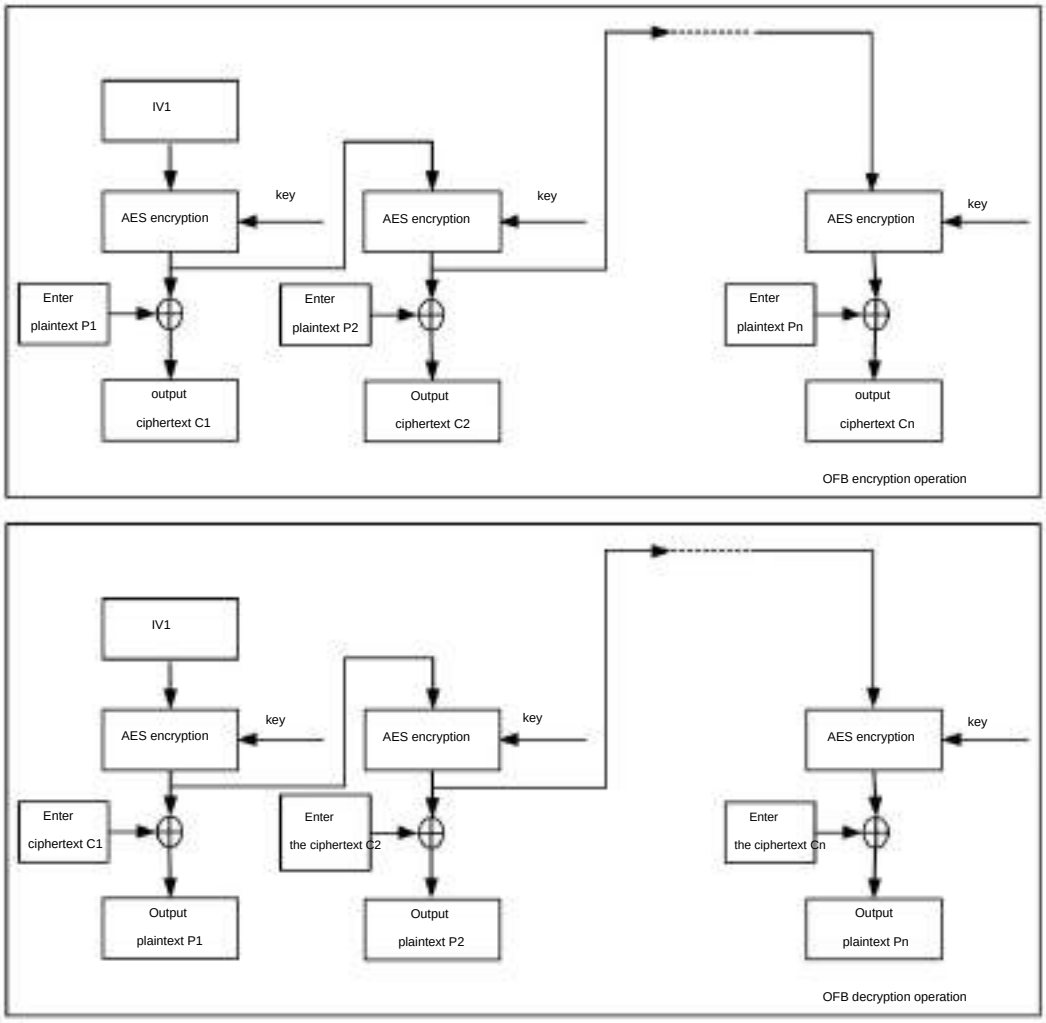
OFB mode

In the OFB (Output FeedBack) mode, the IV is directly used as the input of the encryption operation, so in the case of the same key operation, different IVs should be used to avoid reducing the security of the operation. Regarding the s bit, there are the following 2 situations:

For DES/3DES, s bits can be 1, 8, or 64 bits. For AES, the s bits can only be 128 bits.

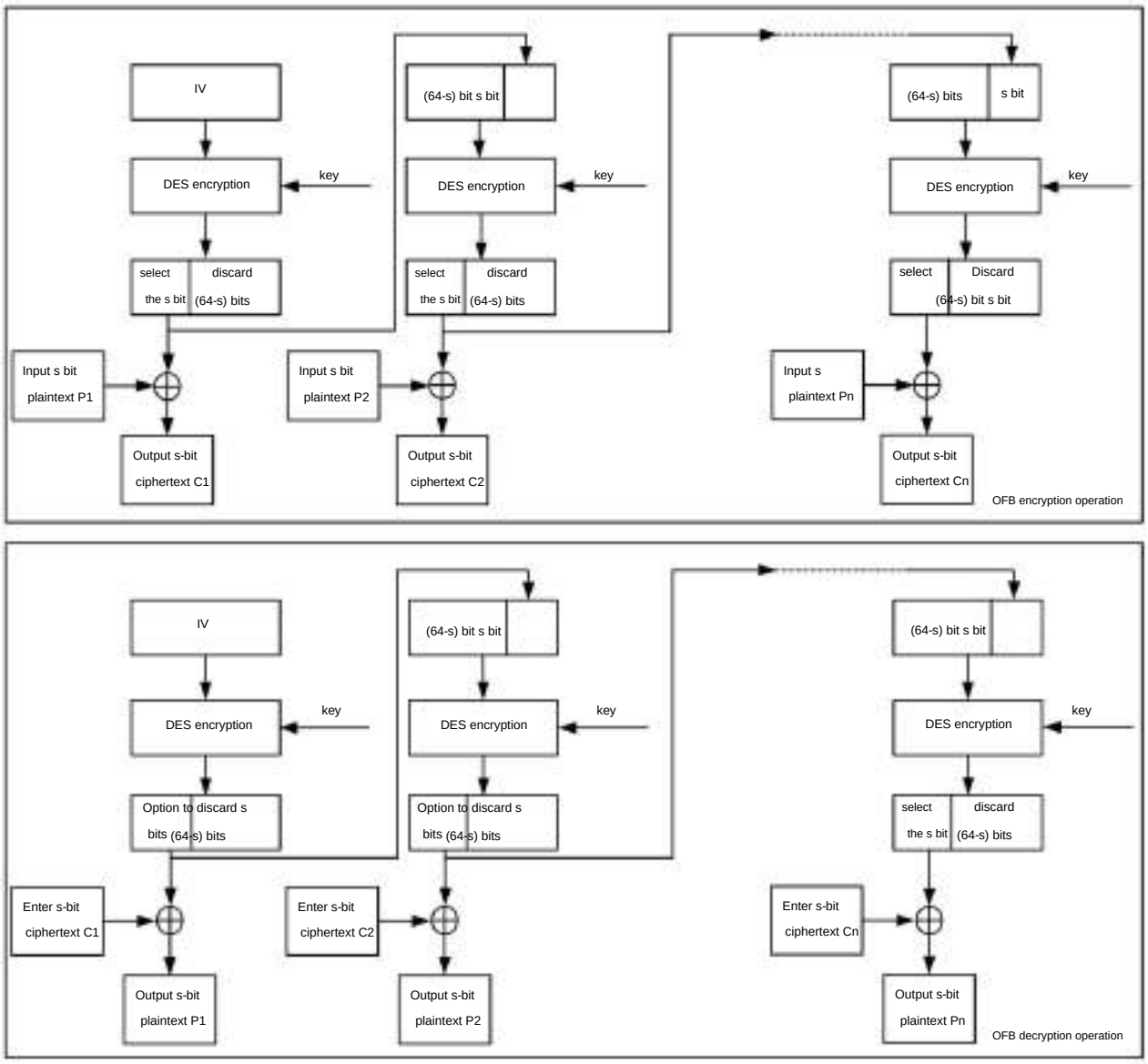
The output feedback (OFB) mode of AES is shown in Figure 3-13 .

Figure 3-13 Output Feedback (OFB) Mode of AES



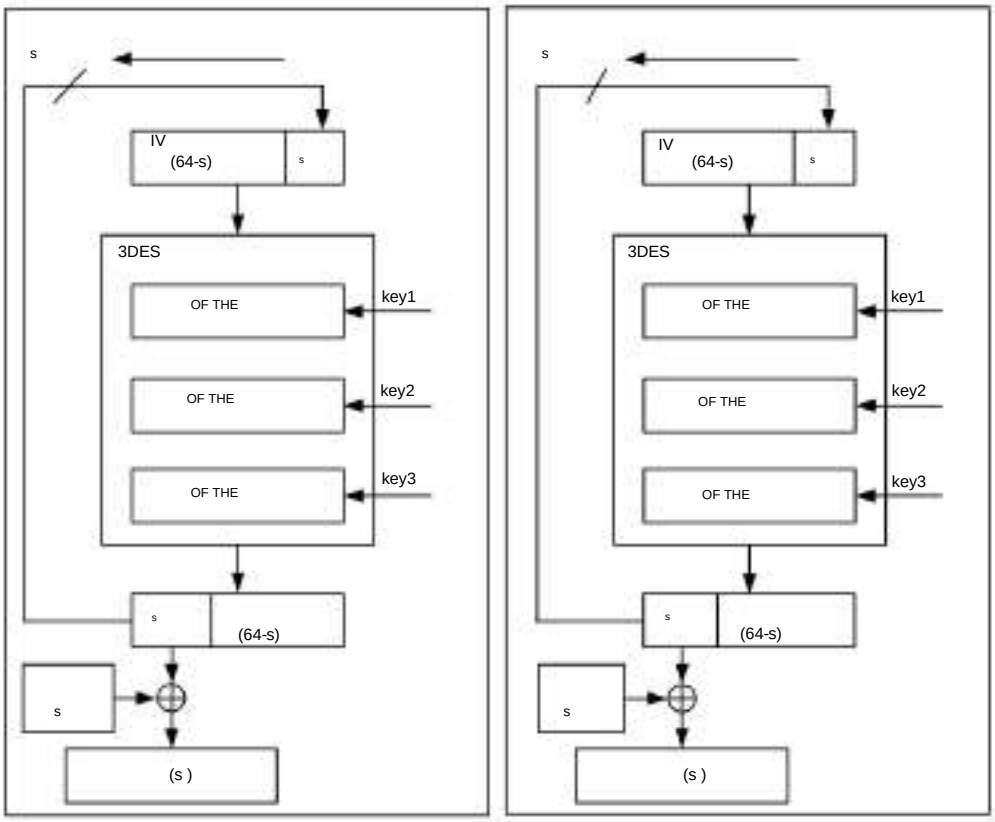
The s-bit output feedback mode of DES is shown in Figure 3-14 .

Figure 3-14 s-bit output feedback (OFB) mode of DES



The s-bit output feedback mode of 3DES is shown in Figure 3-15 .

Figure 3-15 s-bit output feedback (OFB) mode of 3DES



CTR mode

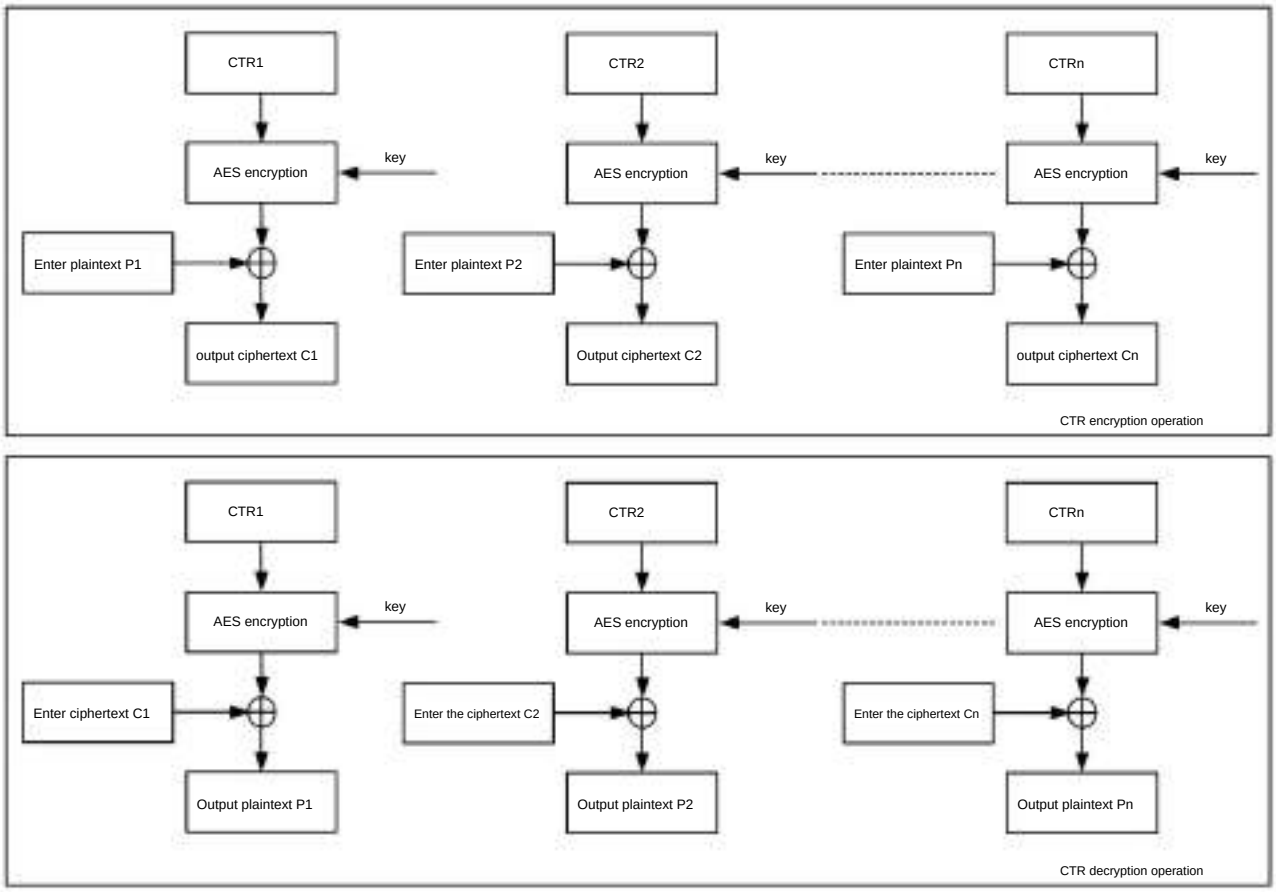
In CTR (Counter) mode, different data is input to the AES encryption or decryption processing module to ensure the security of data processing, and this data can be a count value. Therefore, the selection of the count value CTRn also determines the security of the application of this method.

说明

CTRn is generally obtained by accumulative counting.

The CTR mode of AES is shown in Figure 3-16 .

Figure 3-16 CTR mode of AES



3.5.4 Working method

CIPHER's single group operation process

CIPHER provides channel 0 as a single packet encryption and decryption channel, the operation process is as follows:

1. Query the ch0_busy field of channel 0 configuration register CHAN0_CFG . If channel 0 is not busy, configure the data input of channel 0 and write the relevant configuration information into the register of channel 0.
2. Write the ch0_start field of channel 0 configuration register CHAN0_CFG to start channel 0 encryption and decryption.
3. There are two ways to judge the end of encryption and decryption of channel 0:
4. The query waits for ch0_busy to become unbusy after the encryption and decryption of channel 0 is completed.
5. Enable the channel 0 interrupt and read the data after the channel 0 data complete interrupt is asserted.
6. The encryption and decryption of channel 0 is completed, and the corresponding results are read from the CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT registers of channel 0.

----Finish

CIPHER's multi-group operation process

The CIPHER module provides 7 multi-packet encryption and decryption channels, and the software can set the weight of each channel according to the rate of each channel. The multi-packet encryption and decryption channel automatically reads data from DDR, and writes data into DDR after completing encryption and decryption.

CIPHER's multi-group operation process is as follows:

1. Channel initialization configuration. That is, the input queue depth and output queue depth of each channel, the first address of the input and output queues, the number of multi-packet interrupts and the aging interrupt time, and configure the CTRL register information of each channel.

2. When there is data that needs to be encrypted and decrypted, query the CHANn_IBUF_CNT register. If the value of this register is less than the value of CHANn_IBUF_NUM , configure the head of the data link list to be encrypted and decrypted in the input queue, and enter step 4; otherwise, enter step 3;

3. Open the interrupt corresponding to the input queue channel, and wait for the interrupt to occur. Read the CHANn_IEMPTY_CNT register to represent the number of packets processed by the input queue. The software can clear the interrupt by writing the corresponding value to the register, and then add it to the input queue. new data.

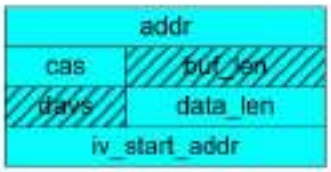
4. Add the corresponding output buffer list header to the output queue;

5. Open the output queue channel corresponding to the interrupt;

6. When the output queue interrupt occurs, the software takes the output queue data and writes the number of packets received this time to CHANn_OFULL_CNT to clear the interrupt.

----Finish

Figure 3-17 The structure of the multi-packet encryption and decryption channel link list is as follows:



addr indicates the first address of the Buffer pointed to by the head of the linked list, which can be a byte address.

data_len indicates the length of valid data indicated by the head of the linked list. cas

represents the control information of cipher encryption and decryption, the specific number of bits is as follows:

Table 3-18 CAS bit flags

ÿ iv_set: indicates that the data indicated by the head of the current linked list needs to be replaced with the initial vector. At this time, it needs to pass iv_start_addr indicates the initial address of the current IV in DDR, and this address must be a WORD-aligned address.

ÿ last_lst: Indicates that the data indicated by the head of the current linked list is the last linked list of a data block. If the logic encounters less than one encrypted and decrypted group of data at the end of the linked list processing, the logic will directly write the remaining data to the output Buffer. Perform encryption and decryption.

clock gating

When no encryption operation is required and the CIPHER module is in an idle state, the clock of the CIPHER module can be turned off by configuring the registers of the system controller to reduce power consumption.

soft reset

The CIPHER module can be soft reset by configuring the registers of the system controller.

3.5.5 Register overview

An overview of the CIPHER registers is shown in Table 3-19 .

Table 3-19 CIPHER register overview (base address is 0x100C_0000)

offset address	name	describe	page number
0x0000ÿ 0x000C	CHAN0_CIPHER_DOUT	CIPHER module channel 0 (single packet encryption and decryption) output register	3-116
0x0010ÿ 0x001C	CHAN0_CIPHER_IVOUT	Vector output register after CIPHER operation completes	3-117
0x0020ÿ 0x008C	CHAN_CIPHER_IVOUT	Channel 1~7 vector output register	3-118
0x0090ÿ 0x018C	CIPHER_KEY	CIPHER Module CPU Configuration Key Register 3-118	
0x1000	CHAN0_CIPHER_CTRL	Channel 0 encryption and decryption control register	3-120
0x1004ÿ 0x1010	CHAN0_CIPHER_IVIN	Input register for the vector grouping of channel 0 of the CIPHER module	3-123
0x1014ÿ 0x1020	CHAN0_CIPHER_DIN	128-Bit Packed Input Register for CIPHER Module 3-123	
0x1000+ nx0x128	CHANn_IBUF_NUM	channel n (n is 1~7) input queue total depth, which is the total number of registers that can configure the head of the linked list	3-124
0x1000+ nx0x128+ 0x4	CHANn_IBUF_CNT	The number register of the number of data buffers to be processed in the channel n input queue	3-125

offset address	name	describe	page number
0x1000+ nx0x128+ 0x8	CHANn_IEMPTY_CNT	The processed data in the channel n input queue Buffer count register	3-125
0x1000+ nx0x128+ 0xC	CHANn_INT_ICNTCFG	Channel n Input Queue Multipacket Interrupt Watermark Register	3-125
0x1000+ nx0x128+ 0x10	CHANn_CIPHER_CTRL	Channel n encryption and decryption control register	3-126
0x1000+ nx0x128+ 0x14	CHANs_SRC_LST_SADDR	Channel n Input Queue Start Address Register	3-128
0x1000+ nx0x128+ 0x18	CHAN_IAGE_TIMIS	Channel n Input Queue Interrupt Aging Time Configuration Register	3-128
0x1000+ nx0x128+ 0x3C	CHANn_OBUF_NOM	The total depth of the channel n output queue, that is, the total number of registers that can configure the head of the linked list	3-129
0x1000+ nx0x128+ 0x40	CHANs_OBUF_CNT	Number of data buffers to be processed in the output queue of channel n	3-129
0x1000+ nx0x128+ 0x44	CHANs_OFULL_CNT	The processed data in the channel n output queue Buffer count register	3-130
0x1000+ nx0x128+ 0x48	CHANn_INT_OCNTCFG	Channel n Output Queue Multipacket Interrupt Watermark Register	3-130
0x1000+ nx0x128+ 0x4C	CHANn_DEST_LST_SADDR	Channel n Output Queue Start Address Register	3-130
0x1000+ nx0x128+ 0x50	CHANn_OAGE_TIMIS	Channel n Output Queue Interrupt Aging Time Configuration Register	3-131
0x1400	INT_STATUS	Interrupt Status Register	3-131
0x1404	INT_EN	interrupt enable register	3-132
0x1408	INT_RAW	Raw Interrupt Status Register	3-133
0x140C	RST_STATUS	Reset Status Indication Register	3-134
0x1410	CHAN0_CFG	Channel 0 Configuration Register	3-135

The value range and meaning of the variables in the CIPHER register offset address are shown in Table 3-20 .

Table 3-20 CIPHER register offset address variable table

variable name	Ranges	describe
n	1ÿ7	Channel 1 to Channel 7 of the CIPHER module.

3.5.6 Register description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is the output register of CIPHER module channel 0 (single packet encryption and decryption).

Note when reading this register:

The data read from this register is the result data of a single group operation. The situation corresponding to AES operation and DES or 3DES operation is different:

If AES operation is selected ÿ If 1-

CFB mode is selected, the lowest bit is valid, that is, CIPHER_DOUT bit[0] is valid data. ÿ If 8-CFB mode is selected, the

lower 8 bits are valid, that is, CIPHER_DOUT bit[7:0] is valid data. ÿIf 128-CFB operation is selected, all 128-bit data are valid.

ÿ128 -bit data is valid in other modes. If DES or 3DES operation is selected

ÿ If 1-CFB or 1-OFB mode is selected, the lower 1 bit

is valid, that is, CIPHER_DOUT bit[0] is valid

data.

ÿIf 8-CFB or 8-OFB mode is selected, the lower 8 bits are valid, that is, CIPHER_DOUT bit[7:0] is active

valid data.

ÿ If 64-CFB or 64-OFB mode is selected, the lower 64-bit data is valid, that is, CIPHER_DOUT bit[63:0] is valid data. ÿIn

other modes, the lower 64-bit

data is valid, that is, CIPHER_DOUT bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x0000ÿ0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	chan0_cipher_dout	The CIPHER module outputs 128-bit groups, and each address corresponds to 32-bit data. CIPHER_DOUT[31:0]: 0x0000 address; CIPHER_DOUT[63:32]: 0x0004 address; CIPHER_DOUT[95:64]: 0x0008 address; CIPHER_DOUT[127:96]: 0x000C address.

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is the vector output register after the CIPHER operation is completed.

Note when reading this register:

If the ECB or CTR mode is implemented, this register does not need to be

concerned. If you choose to process a single packet, the data in this register is the vector result output of this packet, which can be used as the vector input for the next

packet operation of the same data packet. ÿ If AES operation is

selected, all 128-bit data is valid. ÿIf DES or 3DES operation is selected (CIPHER_CTRL[cipher_mode]=0b00, 0b01 or 0b11), the lower 64-bit data is valid, that is, CIPHER_IVOUT bit[63:0] is valid data. If

you choose to perform multi-group processing, the data read in this register is the vector result output of the last group

operation. ÿ If AES operation is selected, all 128-bit data is valid.

ÿ If DES or 3DES operation is selected, the lower 64-bit data is valid, that is, CIPHER_IVOUT bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x0010ÿ0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	chan0_cipher_ivout	The output of the vector IV after the operation of the CIPHER module is completed (no need to pay attention in the ECB and CTR working modes), and each address corresponds to 32 bits of data. CIPHER_IVOUT[31:0]: 0x0010 address; CIPHER_IVOUT[63:32]: 0x0014 address; CIPHER_IVOUT[95:64]: 0x0018 address; CIPHER_IVOUT[127:96]: 0x001C address.

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is the channel 1~7 vector output register.

Offset Address	Register Name	Total Reset Value
0x0020ÿ0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	chan_cipher_ivout	0x0020~0x002C: channel 1; 0x0030~0x003C: channel 2; 0x0040~0x004C: channel 3; 0x0050ÿ0x005C: channel 4; 0x0060ÿ0x006C: channel 5; 0x0070~0x007C: channel 6; 0x0080~0x008C: Channel 7.

CIPHER_KEY

CIPHER_KEY is the CPU configuration key register of the CIPHER module, the key is the CPU configuration value, and the CPU can read and write.

Note when configuring this register:

When DES operation is selected, the lower 64-bit data is valid, that is, CIPHER_KEY[63:0] is valid data. Select

3DES operation: When

selecting 3 key operations (CIPHER_CTRL[key_length]=0b00, 0b01 or 0b10), the lower 192 bits of data are valid, at this time: ÿ CIPHER_KEY

bit[63:0] indicates the first key.

ÿ CIPHER_KEY bit[127:64] indicates the second key.

ÿ CIPHER_KEY bit[191:128] indicates the third key. When two key

operations are selected (ie CIPHER_CTRL[key_length]=0b11), the lower 128 bits of data are valid, at this time: ÿ CIPHER_KEY

bit[63:0] indicates the first key.

ÿ CIPHER_KEY bit[127:64] indicates the second key. When AES

operation is selected: ÿ If

128-bit key operation is selected, the lower 128-bit data is valid, that is, CIPHER_KEY bit[127:0] is valid data.

ÿ If 192-bit key operation is selected, the lower 192 bits of data are valid, that is, CIPHER_KEY bit[191:0] is valid data.

ÿIf 256-bit key operation is selected, all 256-bit data are valid.

The CIPHER module supports the configuration of 8 keys in total, each channel can be configured to use one of the keys, and multiple channels can share the same key.

Offset Address	Register Name	Total Reset Value
0x0090ÿ0x018C	CIPHER_KEY	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cipher_key
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	For the key input of the CIPHER module, each address corresponds to a 32-bit wide data. CIPHER_KEY[31:0]: 0x0090 address; CIPHER_KEY[63:32]: 0x0094 address; CIPHER_KEY[95:64]: 0x0098 address; CIPHER_KEY[127:96]: 0x009C address; CIPHER_KEY[159:128]: 0x00A0 address; CIPHER_KEY[191:160]: 0x00A4 address; CIPHER_KEY[223:192]: 0x00A8 address; CIPHER_KEY[255:224]: 0x00AC address. 0x0090ÿ 0x00AC: host_key0; 0x00B0ÿ0x00CC: host_key1; 0x00D0ÿ0x00ECÿhost_key2ÿ 0x00F0ÿ0x010Cÿhost_key3ÿ 0x0110ÿ 0x012Cÿhost_key4ÿ 0x0130ÿ0x014Cÿhost_key5ÿ 0x0150ÿ0x016Cÿhost_key6ÿ 0x0170ÿ0x018Cÿhost_key7ÿ

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is the encryption and decryption control register of channel 0, and channel 0 is the single packet encryption and decryption channel.

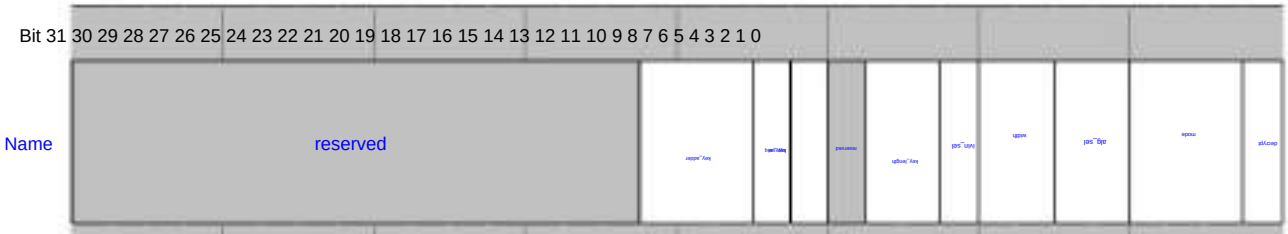
Note when configuring this register:

This register must be configured before configuring other registers of the module.

Except CFB mode under AES, it is not allowed to set CIPHER_CTRL[width] to 01 or 10 in other modes.

In DES/3DES except CFB and OFB modes, other modes do not allow CIPHER_CTRL[width] to be configured as 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:14]	RW	key_adder	The sequence number of the Key used by the current channel. 000ÿhost_key0ÿ 001ÿhost_key1ÿ 010ÿhost_key2ÿ 011ÿhost_key3ÿ 100ÿhost_key4ÿ 101ÿhost_key5ÿ 110ÿhost_key6ÿ 111ÿhost_key7ÿ
[13]	RW	key_sel	Select the key currently configured by the CPU or the key generated by the chip key management module. 0: Use the key configured by the CPU; 1: Use the key generated by the chip key management module.
[12]	RO	reserved	reserve.
[11]	RO	reserved	reserve.
[10:9]	RW	key_length	Key length control. Under the AES algorithm: 00: 128-bit key length; 01: 192-bit key length; 10: 256-bit key length; 11: 128-bit key length. Under DES algorithm: 00: 3 keys; 01: 3 keys; 10: 3 keys; 11: 2 keys.

[8] RW ivin_sel			Input selection control for CIPHER_IVIN. 0: CIPHER_IVIN does not need to be configured; 1: CIPHER_IVIN needs to be configured.
[7:6] RW width			bit width control. Under DES/3DES algorithm: 00: 64- bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 64-bit mode. Under AES algorithm: 00: 128-bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 128-bit mode.
[5:4] RW alg_sel			Algorithm type selection control. 00: DES operation; 01: 3DES operation; 10: AES operation; 11: DES operation.
[3:1] RW mode			Work mode control. Under the AES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; 100: CTR mode; Others: ECB mode. Under DES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; Others: ECB mode.
[0] RW decrypt			Encryption and decryption control. 0: encryption; 1: decryption.

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is the input register for the vector grouping of channel 0 of the CIPHER module.

Note when configuring this register:

If you choose to use channel 0 for single-packet encryption and decryption and the execution is not in ECB mode (CIPHER_CTRL[mode]=0b001, 0b010, 0b011 or 0b100):

If you choose not to configure the input vector (CIPHER_CTRL[ivin_sel]=0b0), you don't need to configure this register.

If you choose to configure the input vector (CIPHER_CTRL[ivin_sel]=0b1), you need to configure this register. If AES operation is selected at this time (ie CIPHER_CTRL [alg_sel]=0b10), CIPHER_IVIN bit[127:0] is valid data; if DES or 3DES operation is selected (CIPHER_CTRL[alg_sel]=0b00, 0b01 or 0b11), the lower 64 Bit data is valid, that is, CIPHER_IVIN bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x1004ÿ0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
chan0_cipher_ivin	CIPHER_IVIN[63:32]: 0x1008	The 128-bit IV vector of the channel 0 CIPHER module or the data input by the Counter, each address corresponds to a 32-bit wide data. CIPHER_IVIN[31:0]: 0x1004 address; [31:0] RW address; CIPHER_IVIN[95:64]: 0x100C address; CIPHER_IVIN[127:96]: 0x1010 address.

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is the 128-bit group input register of the CIPHER module.

Note when configuring this register:

If channel 0 is selected for single packet processing, this register needs to be configured:

If AES operation is selected (CIPHER_CTRL[alg_sel]=0b10) ÿ If 1-CFB operation is selected, the lower 1 bit is valid, that is, CIPHER_DIN bit[0] is valid data. ÿ If 8-CFB operation is selected, the lower 8 bits are valid, that is, CIPHER_DIN bit[7:0] is valid data. ÿIf 128-CFB operation is selected, all 128-bit data are valid. ÿIf other operation modes are selected, 128-bit data is valid.

If you choose to perform DES or 3DES operation (CIPHER_CTRL[alg_sel]=0b00, 0b01 or 0b11)

ÿ If 1-CFB/1-OFB operation is selected, the lower 1 bit is valid, that is, CIPHER_DIN bit[0] is a valid number according to.

ÿIf 8-CFB/8-OFB operation is selected, the lower 8 bits are valid, that is, CIPHER_DIN bit[7:0] is a valid number according to.

ÿ If 64-CFB/64-OFB operation is selected, the lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid data.

ÿ If other operation modes are selected, the lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is the valid number according to.

Offset Address	Register Name	Total Reset Value
0x1014ÿ0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_cipher_din
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RW chan0_cipher_din	128-bit group input of channel 0CIPHER module, each address corresponds to a 32-bit wide data. CIPHER_DIN[31:0]: 0x1014 address; CIPHER_DIN[63:32]: 0x1018 address; CIPHER_DIN[95:64]: 0x101c address; CIPHER_DIN[127:96]: 0x1020 address.

CHANn_IBUF_NUM

CHANn_IBUF_NUM is CHANn_IBUF_BUN is channel n (n is 1~7) input queue total depth, which is the total number of configurable linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+n*128	CHANn_IBUF_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ibuf_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RO reserved	reserve.
[15:0]	RW ibuf_num	Enter the queue depth, that is, the total number of linked list header information that can be configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is the number of data buffers to be processed in the input queue of channel n. When the software writes this register, the logic will add the value newly written by the software to the original value of the register; after the logic processes a Buffer block, the value of this register will be reduced by 1.

Offset Address	Register Name	Total Reset Value
0x1000+nx0x128+0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ibuf_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	-	reserved	reserve.
[15:0]	RW ibuf_cnt		Enter the number of data buffers to be processed in the queue.

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is the number of processed data buffers in the channel n input queue. When the software writes this register, the logic will subtract the value newly written by the software from the original value of the register. After the logic processes a Buffer block, the register The value will be incremented by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iempty_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	-	reserved	reserve.
[15:0]	RW iempty_cnt		Input the number of processed Buffers in the queue.

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is the channel n input queue multi-packet interrupt watermark. When the number of input queue buffers completed by logic processing is greater than or equal to this value, the input queue interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name | reserved | int_icnt_cfg

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold.

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is the encryption and decryption control register for channel n.

Note when configuring this register:

Before starting the encryption and decryption processing of this channel, this register must be configured first.

Except CFB mode under AES, it is not allowed to set CIPHER_CTRL[width] to 01 or 10 in other modes.

In DES/3DES except CFB and OFB modes, other modes do not allow CIPHER_CTRL[width] to be configured as 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name | weight | reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	-	weight	The weight of the current channel, the unit is 64bytes.
[21:17]	-	reserved	reserve.
[16:14]	RW	key_adder	The serial number of the Key used by the current channel can be configured to select a Key from addresses 0 to 7.
[13]	RW	key_sel	Select the key currently configured by the CPU or the key generated by the chip key management module. 0: Use the key configured by the CPU; 1: Use the key generated by the chip key management module.

[12:11] -		reserved	reserve.
[10:9] RW key_length			Key length control. Under the AES algorithm: 00: 128-bit key length; 01: 192-bit key length; 10: 256- bit key length; 11: 128-bit key length. Under the DES algorithm: 00: 3 keys; 01: 3 keys; 10: 3 keys; 11: 2 keys.
[8]		reserved	reserve.
[7:6] RW width			bit width control. Under DES/3DES algorithm: 00: 64-bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 64-bit mode. Under AES algorithm: 00: 128-bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 128-bit mode.
[5:4] RW alg_sel			Algorithm type selection control. 00: DES operation; 01: 3DES operation; 10: AES operation; 11: DES operation.

[3:1] RW mode			Work mode control. Under AES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; 100: CTR mode; Others: ECB mode. Under DES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; Others: ECB mode.
[0] RW decrypt			Encryption and decryption control. 0: encryption; 1: Decrypt.

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is the starting address of the channel n input queue, which must be a WORD-aligned address.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	The start address of the input queue.

CHAN_IAGE_TIMER

CHANn_IAGE_TIMER is configured for the aging time of the input queue interrupt of channel n. If the aging time counter overflows and the number of Buffers processed by the input queue is greater than 0, the input queue processing completion interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x18	CHAN_IAGE_TIMER	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iage_hours
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	iage_timer	Aging interrupt timer.

CHANs_OBUF_NUM

CHANn_OBUF_NUM is the total depth of the channel n output queue, that is, the total number of configurable linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x3C	CHANs_OBUF_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	obuf_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	obuf_num	Total output queue depth.

CHANn_OBUF_CNT

CHANn_OBUF_CNT is the number of data buffers to be processed in the output queue of channel n. When the software writes this register, the logic will add the value newly written by the software to the original value of the register; after the logic processes a Buffer block, the value of this register will be reduced by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	obuf_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.

[15:0] RW	obuf_cnt		The number of data buffers to be processed in the output queue.

CHANn_OFULL_CNT

CHANn_OFULL_CNT is the number of processed data buffers in the channel n output queue. When the software writes this register, the logic will subtract the value newly written by the software from the original value of the register. After the logic processes a Buffer block, the register The value will be incremented by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ofull_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	ofull_cnt	The number of Buffers processed in the output queue.

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is the multi-packet interrupt watermark of the output queue of channel n. When the number of output queue buffers completed by logic processing is greater than or equal to this value, the output queue interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	int_ocnt_cfg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold.

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is the starting address of the channel n output queue, which must be a WORD-aligned address.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dest_lst_saddr	The starting address of the output queue.

CHAN_OAGE_TIMER

CHANn_OAGE_TIMER is configured for the aging time of the output queue interrupt of channel n. If the aging time counter overflows and the number of Buffers processed by the output queue is greater than 0, an output queue processing completion interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ nx0x128+0x50	CHAN_OAGE_TIMER	0x0000_0000

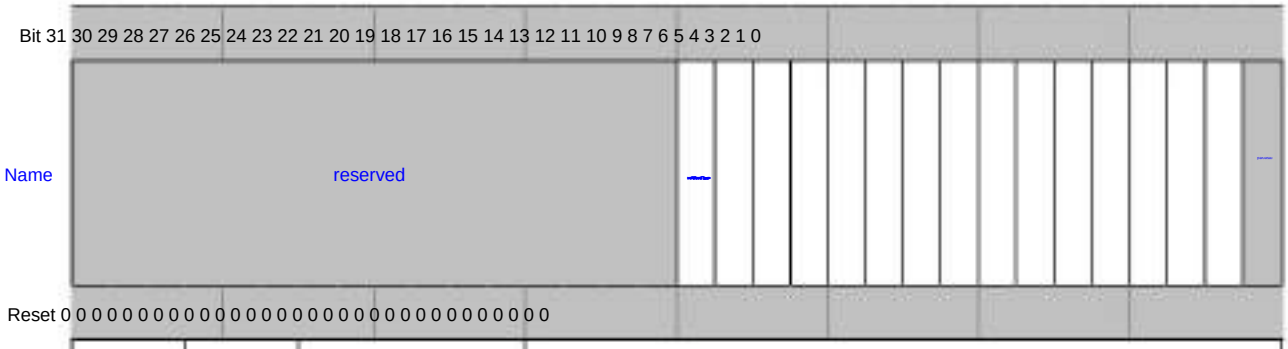
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_hours															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:16]	- reserved	reserve.
[15:0]	RW oage_timer	Aging interrupt timer.

INT_STATUS

INT_STATUS is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

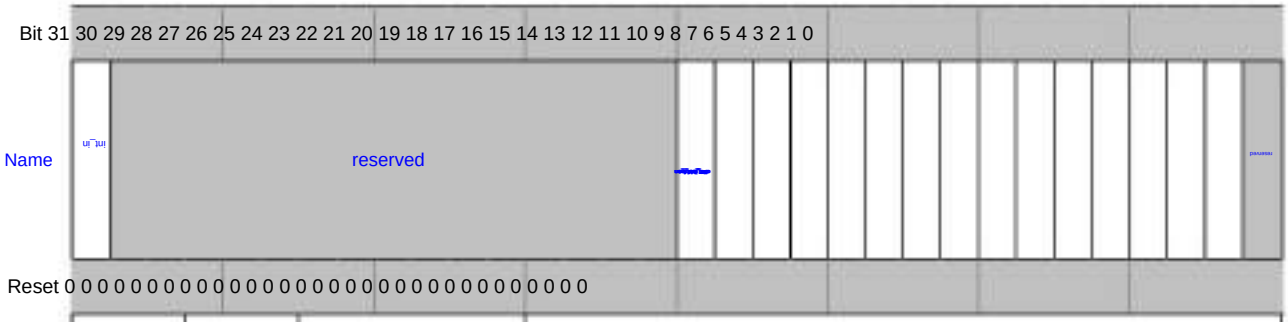


Bits	Access Name		Description
[31:16] -		reserved	reserve.
[15] RO		ch7_ibuf_int Channel 7 input queue data interrupt.	
[14] RO		ch6_ibuf_int Channel 6 input queue data interrupt.	
[13] RO		ch5_ibuf_int Channel 5 input queue data interrupt.	
[12] RO		ch4_ibuf_int Channel 4 input queue data interrupt.	
[11] RO		ch3_ibuf_int Channel 3 input queue data interrupt.	
[10] RO		ch2_ibuf_int Channel 2 input queue data interrupt.	
[9]	RO	ch1_ibuf_int Channel 1 input queue data interrupt.	
[8]	RO	ch0_ibuf_int Channel 0 data transaction complete interrupt.	
[7]	RO	ch7_obuf_int Channel 7 output queue data interrupt.	
[6]	RO	ch6_obuf_int Channel 6 output queue data interrupt.	
[5]	RO	ch5_obuf_int Channel 5 output queue data interrupt.	
[4]	RO	ch4_obuf_int Channel 4 output queue data interrupt.	
[3]	RO	ch3_obuf_int Channel 3 output queue data interrupt.	
[2]	RO	ch2_obuf_int Channel 2 output queue data interrupt.	
[1]	RO	ch1_obuf_int Channel 1 output queue data interrupt.	
[0]	-	reserved	reserve.

INT_EN

INT_EN is the interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

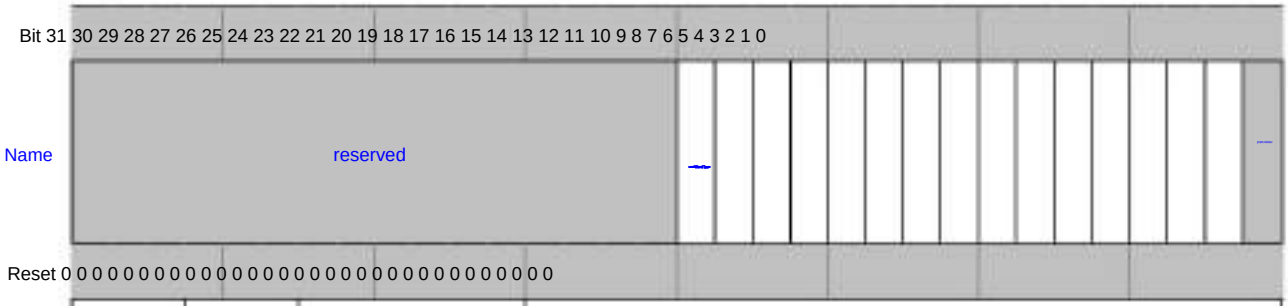


Bits	Access	Name	Description
[31]	RW	int_en	Global interrupt enable for the Cipher module.
[30:16]	-	reserved	reserve.
[15]	RW	ch7_ibuf_en	Channel 7 input queue data interrupt enable.
[14]	RW	ch6_ibuf_en	Channel 6 input queue data interrupt enable.
[13]	RW	ch5_ibuf_en	Channel 5 input queue data interrupt enable.
[12]	RW	ch4_ibuf_en	Channel 4 input queue data interrupt enable.
[11]	RW	ch3_ibuf_en	Channel 3 input queue data interrupt enable.
[10]	RW	ch2_ibuf_en	Channel 2 input queue data interrupt enable.
[9]	RW	ch1_ibuf_en	Channel 1 input queue data interrupt enable.
[8]	RW	ch0_ibuf_en	Channel 0 data processing complete interrupt enable.
[7]	RW	ch7_obuf_en	Channel 7 output queue data interrupt enable.
[6]	RW	ch6_obuf_en	Channel 6 output queue data interrupt enable.
[5]	RW	ch5_obuf_en	Channel 5 output queue data interrupt enable.
[4]	RW	ch4_obuf_en	Channel 4 output queue data interrupt enable.
[3]	RW	ch3_obuf_en	Channel 3 output queue data interrupt enable.
[2]	RW	ch2_obuf_en	Channel 2 output queue data interrupt enable.
[1]	RW	ch1_obuf_en	Channel 1 output queue data interrupt enable.
[0]	-	reserved	reserve.

INT_RAW

INT_RAW is the raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000



Bits	Access Name	Description
[31:16] -	reserved	reserve.
[15] RWC	ch7_ibuf_raw	Channel 7 input queue data raw interrupt.
[14] RWC	ch6_ibuf_raw	Channel 6 input queue data raw interrupt.
[13] RWC	ch5_ibuf_raw	Channel 5 input queue data raw interrupt.
[12] RWC	ch4_ibuf_raw	Channel 4 input queue data raw interrupt.
[11] RWC	ch3_ibuf_raw	Channel 3 input queue data raw interrupt.
[10] RWC	ch2_ibuf_raw	Channel 2 input queue data raw interrupt.
[9]	RWC ch1_ibuf_raw	Channel 1 input queue data raw interrupt.
[8]	RWC ch0_ibuf_raw	Channel 0 data processing complete raw interrupt.
[7]	RWC ch7_obuf_raw	Channel 7 output queue data raw interrupt.
[6]	RWC ch6_obuf_raw	Channel 6 output queue data raw interrupt.
[5]	RWC ch5_obuf_raw	Channel 5 output queue data raw interrupt.
[4]	RWC ch4_obuf_raw	Channel 4 output queue data raw interrupt.
[3]	RWC ch3_obuf_raw	Channel 3 output queue data raw interrupt.
[2]	RWC ch2_obuf_raw	Channel 2 output queue data raw interrupt.
[1]	RWC ch1_obuf_raw	Channel 1 output queue data raw interrupt.
[0]	- reserved	reserve.

RST_STATUS

Module reset status indication signal.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]		reserved	reserve.
[0]	RO	rst_status	CIPHER module reset status indication signal. 0: CIPHER is currently in reset state; 1: CIPHER is currently working normally.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]		reserved	reserve.
[1]	RO	ch0_busy	Channel 0 status signal.
[0]	RW	ch0_start	Channel 0 encryption and decryption start signal.

3.6 Timers

3.6.1 Overview

The Timer module mainly implements the timing and counting functions, which can be used as the system clock by the operating system, and can also be used by the application program as timing and counting. Hi3520D provides 4 groups of Dual-Timer modules: Dual-Timer0, Dual-Timer1, Dual-Timer2ÿDual-Timer3ÿ

Dual-Timer0 includes Timer0 and Timer1, they share the same base address and the same interrupt line.

Dual-Timer1 includes Timer2 and Timer3, they share the same base address and the same interrupt line.

Dual-Timer2 includes Timer4 and Timer5, they share the same base address and the same interrupt line.

Dual-Timer3 includes Timer6 and Timer7, they share the same base address and the same interrupt line.

Each group of Dual-Timer modules contains two Timers with identical functions.

3.6.2 Features

The Dual-Timer module has the following features:

There are two 32bit/16bit down timer/counters with programmable 8-bit prescaler. The counting clock is

configurable. When the system is in NORMAL mode, the counting clock of Dual-Timer0 and Dual-Timer1 can be selected as system bus clock or crystal oscillator clock. Three counting modes are supported:

free-running mode, periodic mode and one-shot counting mode. There are 2 methods to load the initial

value of the count, which are realized through the TIMERx_LOAD and TIMERx_BGLOAD registers respectively. The current count value can be read at

any time. An interrupt is generated when

the count reaches zero.

3.6.3 Functional description

Functional principle

Timer is based on a 32bit/16bit (configurable) down counter. The value of the counter is decremented by 1 at each rising edge of the count clock. When the count value decrements to zero, the Timer will generate an interrupt.

Timer has the following 3 counting modes:

free run mode

The timer keeps counting, and when the count value decreases to 0, it automatically turns back to its maximum value and continues counting. When the count length is 32bit, the maximum value is 0xFFFF_FFFF. When the count length is 16bit, the maximum value is 0xFFFF. In free mode, it is also possible to load the count value and immediately count down from the loaded value, but wrap around to its maximum value when it reaches 0.

The periodic

mode timer keeps counting, when the count value decreases to 0, reload the initial value from the TIMERx_BGLOAD register and continue counting. one-

shot mode

Load the counting initial value into the timer. When the count value of the timer decreases to 0, it stops counting, and does not start counting again until it is reloaded with a new value and the timer is enabled.

Each Timer has a prescaler (prescaler), which can divide its working clock by 1, 16 or 256 again inside the Timer. Further improve the selection flexibility of counting clock frequency.

The method of loading the counting initial value to the timer is as follows:

By writing the TIMERx_LOAD register, the timer can be loaded with the counting initial value. When the timer is in the working state, if you write a value to the TIMERx_LOAD register, it will cause the timer to restart counting from the new value immediately. Applies to all counting modes. The counting period of the period counting mode

can be set by writing the TIMERx_BGLOAD register. Writing this register will not affect the current count of the timer immediately, and the timer will continue to count until the count value decreases to 0. Then the new value loaded into the TIMERx_BGLOAD register starts counting.

3.6.4 Working method

initialization

The Timer should be initialized when the system is initialized. When initializing TimerX (the value of "X" in TimerX is 0, 1, 2, 3, 4, 5, 6, 7), it should be configured according to the following steps:

1. Write the TIMERx_LOAD register to load the initial count value for the Timer.
2. When the Timer is required to work in the period counting mode, and the counting period is different from the initial counting value loaded into the Timer, Write the TIMERx_BGLOAD register to set the count period of the Timer.
3. Configure the system control register to set the reference clock of the clock enable signal of the Timer.
4. Configure the TIMERx_CONTROL register, set the timer counting mode, counter length, prescaler factor and interrupt mask, and start the timer counting at the same time.

----Finish

interrupt handling

Timer is mainly used to generate interrupts regularly, so the interrupt processing of Timer is mainly to activate the process waiting for timing interrupts. The operation steps are as follows:

1. Configure the TIMERx_INTCLR register to clear the Timer interrupt.
2. Activate the process waiting for the interrupt to continue execution.
3. When all the processes waiting for the interrupt are completed or executed again to the dormant state waiting for the interrupt, resume the interrupted site, Continue to execute the currently interrupted program.

----Finish

clock selection

Dual-Timer0, Dual-Timer1, Dual-Timer2, Dual-Timer3 all have 2 kinds of counting clocks to choose from. Taking Timer0 as an example, the clock selection configuration process is as follows:

Select bus clock for counting

The steps to select the bus clock for counting are as follows:

1. Configure SC_CTRL [timeren0ov]=1 for the system controller.
2. Initialize the Timer and start counting.

----Finish

Select crystal clock for counting

The steps to select a 3MHz clock for counting are as follows:

1. Configure SC_CTRL [timeren0ov]=0 for the system controller.
2. Configure SC_CTRL [timeren0sel]=0 for the system controller.
3. Initialize the Timer and start counting.

----Finish

3.6.5 Register overview

Each of the 8 timers in the Timer module has a set of registers, and these 8 sets of registers have the same characteristics except that the base address and offset address are different. in:

Timer0 and Timer1 share a base address: 0x2000_0000.

Timer2 and Timer3 share a base address: 0x2001_0000.

Timer4 and Timer5 share a base address: 0x2013_0000.

Timer6 and Timer7 share a base address: 0x2014_0000.

说明

"x" in TIMERx takes values 0, 1, 2, 3, 4, 5, 6, 7. in:

The registers of Timer0~Timer7 are the same, and the description of the registers is described using Timer0 as an example.

The base addresses of Timer0, Timer2, Timer4, and Timer6 are different, but the offset addresses are the same; Timer1, Timer3,

The base addresses of Timer5 and Timer7 are different, but the offset addresses are the same.

Table 3-21 Timer register overview (base address is 0x2000_0000, 0x2001_0000, 0x2013_0000, 0x2014_0000)

Offset address of Timer0/2/4/6	Offset address of Timer1/3/5/7	name	describe	page number
0x000	0x020	TIMERx_LOAD counting initial value register 3-139		
0x004	0x024	TIMERx_VALUE Current Count Value Register 3-139		
0x008	0x028	TIMERx_CONTROL Timer Control Register 3-140		
0x00C	0x02C	TIMERx_INTCLR Interrupt Clear Register 3-141		
0x010	0x030	TIMERx_RIS	Raw Interrupt Register 3-142	

Offset address of Timer0/2/4/6	Offset address of Timer1/3/5/7	name	describe	page number
0x014	0x034	TIMERx_MIS	Masked Interrupt Register	3-142
0x018	0x038	TIMERx_BGLOAD period mode count initial value register		3-143

3.6.6 Register description

TIMERx_LOAD

TIMERx_LOAD is the counting initial value register. It is used to configure the counting initial value of the timer. Each of Timer0~Timer3 has a counting initial value register.

说明

The minimum valid value to write to the TIMERx_LOAD register

is 1. When writing 0 to TIMERx_LOAD, Dual-Timer will generate an interrupt immediately.

The difference between TIMERx_LOAD and TIMERx_BGLOAD :

If the value is written to both the TIMERx_BGLOAD register and the TIMERx_LOAD register before the rising edge of TIMCLK enabled by TIMCLKENx arrives, the current count value is first updated to the written value of TIMERx_LOAD on the next rising edge of TIMCLK enabled by TIMCLKENx . When writing a value to the TIMERx_LOAD register, the value of TIMERx_BGLOAD will also be overwritten, so when reading TIMERx_BGLOAD, the returned value is the value of the latest written register among TIMERx_LOAD and TTIMERx_BGLOAD . When the timer is in periodic mode and the count value decreases to 0, it will reload the initial value from the TIMERx_BGLOAD register and continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0_load
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	The initial count value of Timer0.

TIMERx_VALUE

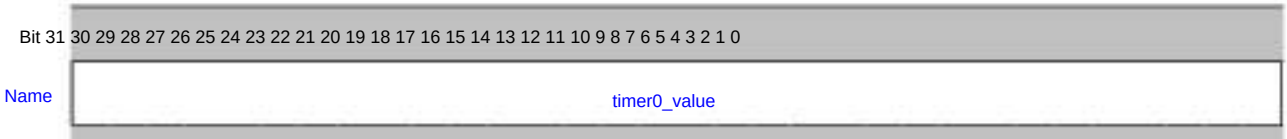
TIMERx_VALUE is the current count value register. Used to give the current value of a counter that is being decremented. Each of Timer0~7 has a current count value register.

When the write operation to the TIMERx_LOAD register occurs, TIMERx_VALUE immediately reflects the new load value of the counter in the PCLK clock domain, without waiting for the next TIMCLK clock edge enabled by TIMCLKENx to arrive.

说明

When the timer is in 16bit mode, the upper 16bits of the 32bit TIMERx_VALUE register are not automatically set to 0. If the timer was in 32bit mode before and TIMERx_LOAD has never been written since entering 16bit mode , the upper 16 bits of the TIMERx_VALUE register may have a non-zero value.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF



Bits	Access Name	Description
[31:0] RO	timer0_value	Current value of Timer0 being decremented.

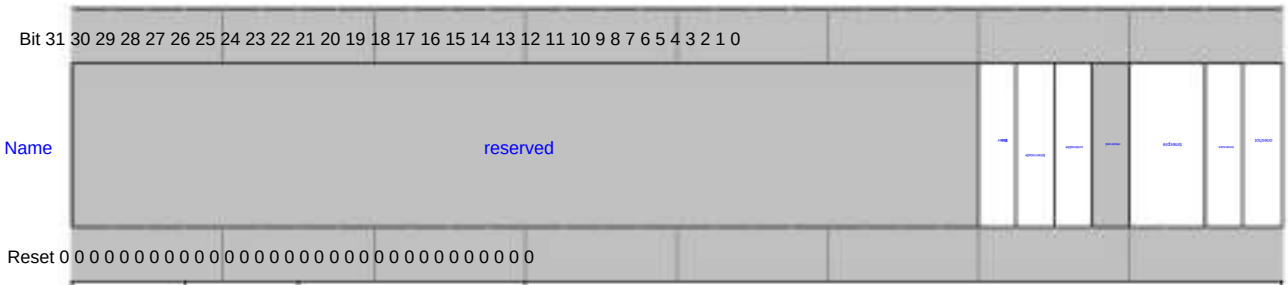
TIMERx_CONTROL

TIMERx_CONTROL is the TIMER control register. Each of Timer0~3 has a control register.

说明

When you choose to count in period mode, you need to set TIMERx_CONTROL[timermode] to 1, TIMERx_CONTROL[oneshot] is set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000



Bits	Access Name	Description
[31:8] RO	reserved	reserve.
[7] The RW	timer	The timer is enabled. 0: Disable Timer; 1: Timer enabled.

[6] RW timer mode			The counting mode of the timer. 0: free running mode; 1: Periodic mode.
[5] Untenable RW			TIMERx_RIS interrupt mask. 0: mask the interrupt; 1: do not mask the interrupt.
[4]	RO	reserved	reserve.
[3:2] RW timerpre			This field is used to set the prescale factor of Timer. 00: No prescaler, the clock frequency is divided by 1; 01: 4-level prescaler, the Timer clock frequency is divided by 16; 10: 8-level prescaler, divide the Timer clock frequency by 256; 11: Undefined, if set to this value, it is equivalent to 8-level prescaler, divide the Timer clock frequency by 256.
[1] RW timersize			Select 16bit/32bit counter operation mode. 0: 16bit counter; 1: 32bit counter.
[0] RW oneshot			Select the count mode as one-shot count mode or period count mode. 0: Period counting mode or free running mode; 1: Single counting mode.

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. Any write to this register will clear the interrupt status of the corresponding counter. Each of Timer0~Timer3 has an interrupt clear register.

注意

This register is a write-only register, if any value is written in, it will cause the timer to be cleared and interrupted, and the written value is not memorized internally, and there is no reset value.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0_intclr
Reset	? ?

Bits	Access Name		Description
[31:0]	WO	timer0_intclr	Write this register to clear the interrupt output of Timer0.

TIMERx_RIS

TIMERx_RIS is the raw interrupt register. Timer0~Timer3 each have a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x030	TIMER0_RIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve. Writing is invalid and returns 0 when reading.
[0]	RO	timer0ris	Raw interrupt status of Timer0. 0: no interrupt is generated; 1: An interrupt has been generated.

TIMERx_MIS

TIMERx_MIS is the masked interrupt register. Timer0~Timer3 each have a masked interrupt register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.

[0]	RO	timer0mis	Masked interrupt status of Timer0. 0: Interrupt is invalid; 1: Interrupt is active.

TIMERx_BGLOAD

TIMERx_BGLOAD is the counting initial value register in period mode. Each of Timer0~Timer3 has a period mode count initial value register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload the initial count value when the count value of the timer is decremented to 0 in periodic mode.

This register provides an alternate method of accessing the TIMERx_LOAD register. The difference is that writing a value to the TIMERx_BGLOAD register does not cause the timer to immediately start counting from the newly written value.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0bgload
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	timer0bgload	The initial count value of Timer0. Note: It is different from the **TIMERX_LOAD** register, please refer to Description of the TIMERx_LOAD register.

3.7 Watchdog

3.7.1 Overview

The watchdog WatchDog is used to send a reset signal within a certain period of time to reset the entire system when the system is abnormal.

3.7.2 Features

WatchDog has the following features:

- There is a 32bit down counter inside, and the counting clock source can be configured.
- It supports configurable timeout interval (that is, the initial count value).
- Support register lock to prevent registers from being changed by mistake. Support timeout interrupt generation.

Support reset signal generation.

Debug mode is supported.

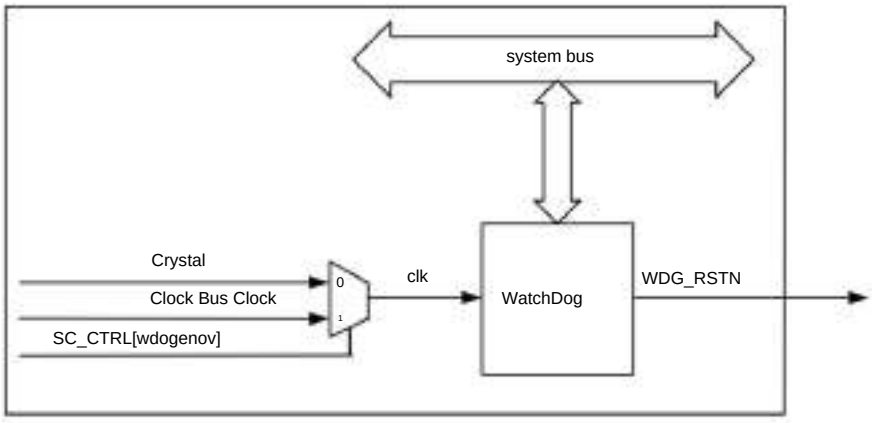
3.7.3 Functional description

Application Block Diagram

The system selects the configuration clock for WatchDog through SC_CTRL [wdogenov], and configures the register parameter values for WatchDog through the system bus. WatchDog sends interrupt requests to the system regularly, and when the system does not respond to the interrupt (such as: crash), it sends a WDG_RSTN reset signal to reset the system and achieve the purpose of monitoring system operation.

The block diagram of the WatchDog application is shown in Figure 3-18 .

Figure 3-18 WatchDog application block diagram



Functional principle

The operation of WatchDog is based on a 32bit down counter, and the initial counting value is loaded by the register WDG_LOAD . When the WatchDog clock is enabled, the count value is decremented by 1 at each rising edge of the count clock. When the count value decrements to 0, WatchDog will generate an interrupt. Then at the rising edge of the next counting clock, the counter reloads the counting initial value from the register WDG_LOAD and starts counting down.

If the count value of the counter counts down to 0 for the second time, the CPU has not cleared the WatchDog interrupt, then the WatchDog will send a reset signal WDG_RSTN, and the counter will stop counting.

According to actual application needs, you can enable or disable WatchDog to generate interrupt and reset signals by configuring WDG_CONTROL :

When interrupt generation is disabled, the counter will stop counting. When

interrupts are turned back on, WatchDog will start counting from the value set by WDG_LOAD instead of the value it was at when the counter was last stopped. Before the interrupt arrives, the initial value can be reloaded.

The counting clock of WatchDog can choose crystal oscillator clock or bus clock, which is convenient for choosing different counting time ranges.

By configuring the WDG_LOCK register, you can prohibit writing to the WatchDog internal registers:

Write 0x1ACC_E551 to WDG_LOCK to open the write permission of all WatchDog registers. Writing any other value to the WDG_LOCK register disables write access to all WatchDog registers except the WDG_LOCK register.

This feature protects WatchDog's registers from being incorrectly modified by software, so that in abnormal conditions, WatchDog will not be incorrectly terminated by software.

In debug mode, WatchDog is automatically turned off to prevent interference with normal debug operations.

3.7.4 Working method

Count Clock Frequency Configuration

The system supports 2 WatchDog counting clocks: 3MHz clock and bus clock, which can be configured through SC_CTRL [wdogenov].

WatchDog counts time as TWDG:

$$T_{WDG} = Value_{WDG\_LOAD} \times \left(\frac{1}{f_{clk}}\right)$$

说明

In the above formula, the meanings of each parameter are: TWDG means WatchDog counting time; ValueWDG_LOAD means WatchDog counting initial value; fclk means WatchDog counting clock frequency.

The counting time range values of WatchDog under different clocks are as follows:

When the 3MHz clock is selected, the counting time range is 0s~1400s.

When the bus clock is selected (take 100MHz as an example), the counting time range is 0s~42s.

System initialization configuration

After the system is powered on and reset, the WatchDog counter is in the stop counting state. During the system initialization process, the WatchDog needs to be initialized and started to run. The initialization process of WatchDog is as follows:

1. Write the register WDG_LOAD to set the counting initial value.
2. Write register WDG_CONTROL to enable interrupt mask and start WatchDog counting.
3. Write the register WDG_LOCK to lock the WatchDog to prevent the software from modifying the WatchDog configuration by mistake.

----Finish

interrupt handling

After receiving the interrupt from WatchDog, the interrupt status should be cleared in time, and it should be loaded with the initial counting value to start counting again. The process of WatchDog interrupt handling is as follows:

1. Write 0x1ACC_E551 to WDG_LOCK to unlock the WatchDog.

2. Write the register WDG_INTCLR to clear the interrupt status of WatchDog, and at the same time make WatchDog automatically load the initial counting value and start counting again.

3. Write any value other than 0x1ACC_E551 to the register WDG_LOCK to lock the WatchDog.

----Finish

close watchdog

Write 0 or 1 to the register WDG_CONTROL[inten] control bit to control the status of WatchDog:

0: Turn off WatchDog; 1:

Turn on WatchDog.

3.7.5 Register overview

An overview of WatchDog registers is shown in Table 3-22 .

Table 3-22 WatchDog register overview (base address is 0x2004_0000)

offset address name	describe	page number
0x0000 WDG_LOAD	Count initial value register	3-146
0x0004 WDG_VALUE counter current value register		3-147
0x0008 WDG_CONTROL control register		3-147
0x000C WDG_INTCLR interrupt clear register		3-148
0x0010 WDG_RIS	raw interrupt register	3-148
0x0014 WDG_MIS	Masked Interrupt Register	3-149
0x0018ÿ RESERVED 0x0BFC	reserve	
0x0C00 WDG_LOCK	LOCK register	3-149

3.7.6 Register description

WDG_LOAD

WDG_LOAD is the counting initial value register. It is used to configure the counting initial value of WatchDog's internal counter.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	etc_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	etc_load	Count initial value.

WDG_VALUE

WDG_VALUE is the counter current value register. It is used to read the current count value of WatchDog's internal counter.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	WatchDog counter current value.

WDG_CONTROL

WDG_CONTROL is the control register. Used to control the On/Off, Interrupt and Reset functions of the WatchDog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

[1] RW reset			WatchDog reset signal output enable. 0: forbidden; 1: enable.
[0] RW inten			WatchDog interrupt signal output enable. 0: The counter stops counting, the count value keeps the current value unchanged, and the WatchDog is turned off; 1: Both start counter and enable interrupt, WatchDog is started.

WDG_INTCLR

WDG_INTCLR is the interrupt clear register. It is used to clear the WatchDog interrupt and make WatchDog reload the initial value for counting. This register is a write-only register, if any value is written in, it will cause the WatchDog to be cleared and interrupted, and the written value is not memorized internally, and there is no reset value.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wdg_intclr
Reset	? ?

Bits	Access Name		Description
[31:0]	WO	etc_intclr	Writing any value to this register can clear the WatchDog interrupt and make WatchDog reload the initial count from the register WDG_LOAD .

WDG_RIS

WDG_RIS is the raw interrupt register. Used to reflect the WatchDog raw interrupt status.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.

[0]	RO	wdogris	WatchDog raw interrupt status, this bit is set to 1 when the count value of the counter is decremented to 0. 0: no interrupt is generated; 1: An interrupt has been generated.

WDG_MIS

WDG_MIS is the masked interrupt register. Used to reflect the shielded WatchDog interrupt status.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	wdogmis	Interrupt state after WatchDog masking. 0: Interrupt not generated or interrupt masked; 1: Interrupt generated.

WDG_LOCK

WDG_LOCK is the LOCK register. Used to control the read and write permissions of WatchDog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wdg_lock
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Write 0x1ACC_E551 to this register to open the write permission of all registers; Writing other values to this register disables write access. Reading this register returns the status of the lock rather than the value written to this register: 0x0000_0000: write access allowed (unlocked); 0x0000_0001: write access disabled (locked).

3.8 Real Time Clock

3.8.1 Overview

The real time clock RTC (Real Time Clock) is used to realize time display and timing alarm function.

3.8.2 Features

RTC has the following characteristics:

It has a 16bit day counter, 5bit hour counter, 6bit minute counter, 6bit second counter and 7bit 10ms counter inside.

Counting clock 100Hz counting initial value

can be configured

Count comparison value configurable

Support timeout interrupt generation

Support soft reset

Support fixed frequency division

mode Provide automatic thermometer correction function

Provide temperature saving of the chip position where the RTC module is located

3.8.3 Functional description

The operation of RTC is based on a common 40bit (day, hour, minute, second, 10ms) addition counter .

RTC_LR_D_H is loaded. When the count value is added to the register and RTC_MR_10MS, RTC_MR_S,

When the RTC_MR_M, RTC_MR_H, RTC_MR_D_L, RTC_MR_D_H register values are equal, the RTC will generate an interrupt, and then the counter will continue to count up on the next rising edge of the counting clock.

According to actual application needs, RTC can be enabled or disabled to generate interrupt signals by configuring RTC_IMSC . At this point, there are the following two situations:

When interrupts are disabled, the RTC counter continues to count up, and no external interrupts will be generated. The interrupt status after masking is displayed in RTC_MSC_INT , and the original interrupt status is displayed in RTC_RAW_INT .

When the interrupt is restarted, the RTC counter still continues to count up. When the count value is added to the RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H,
The RTC will generate an interrupt when the RTC_MR_D_H register values are equal.

The counting clock of RTC adopts 100Hz clock, and provides 16bit day counting at the same time, which is convenient to convert the day counting value into specific year, month and day.

3.8.4 Working method

3.8.4.1 Count clock frequency

The RTC uses a 100Hz clock to count, and the maximum counting time is:

$$T_{RTC} = 65536 \text{ (days)}$$

说明

TRTC represents RTC count time.

3.8.4.2 Soft reset

By configuring the RTC reset register RTC_POR_N, an individual soft reset of the RTC can be realized. After the soft reset, the values of each RTC configuration register are restored to the default values, so these registers need to be initialized and configured again after the soft reset.

The soft reset steps are as follows:

1. Write 0 to RTC_POR_N to soft reset RTC.
2. Wait for 30ms.

----Finish

3.8.4.3 RTC initialization

When the RTC is powered on for the first time, the system needs to initialize the RTC. The initialization process of RTC is as follows:

1. Configure RTC_POR_N, reset RTC.
2. Wait for 30ms.
3. Configure RTC_IMSC, set the RTC interrupt mask bit.
4. ÿÿ RTC_MR_10MSÿRTC_MR_SÿRTC_MR_MÿRTC_MR_HÿRTC_MR_D_Lÿ
   RTC_MR_D_H, set the RTC comparison value.

5. ÿÿ RTC_LR_10MSÿRTC_LR_SÿRTC_LR_MÿRTC_LR_HÿRTC_LR_D_Lÿ
   RTC_LR_D_H, set the initial value of RTC count.

6. Configure RTC_LORD as 1, so that the initial value of the RTC count is loaded into the RTC counter.

7. The RTC counts from RTC_LR_10MS, RTC_LR_S, RTC_LR_M,
   The values in RTC_LR_H, RTC_LR_D_L, RTC_LR_D_H start counting, when counting to
   RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L,
   When the value in RTC_MR_D_H , it will determine whether to generate an interrupt according to the setting of RTC_IMSC .

   ----Finish

3.8.4.4 Interrupt Handling

After the system receives the interrupt from the RTC, it means that the time is up, and the user can perform the corresponding user-defined operation, and the RTC counter still keeps counting up. The process of RTC interrupt processing is as follows:

1. Set RTC_INT_CLR to 1 to clear the RTC interrupt status.

2. If you need to continue to set the timing time, write to the registers RTC_MR_10MS, RTC_MR_S,
   RTC_MR_M, RTC_MR_H, RTC_MR_D_L, RTC_MR_D_H write new comparison values.

   ----Finish

3.8.4.5 RTC register access

RTC registers are inside the RTC module, not on the APB bus. The RTC registers on the APB bus only provide access to the RTC internal registers, not real RTC internal registers.

The steps to write RTC internal registers are as follows:

1. Configure SPI_CLK_DIV; if the apb bus clock is 120MHz and the expected SPI clock is 12MHz, then
   spi_clk_div should be configured as (120MHz/12MHz)/2 -1 =4=0x04. (This step can be omitted if it is already configured and you do not want to change the clock frequency of the SPI).

2. Read SPI_RW until SPI_RW [31]=0.

3. Configure SPI_RW; if you want to write 0x10 to RTC_MR_10MS , the internal address of this register in RTC is
   0x06, so SPI_RW should be configured as 0x01060010
   (spi_start=1, spi_rw=0, spi_add=0x06, spi_wdata=0x10).

   ----Finish

The steps to read RTC internal registers are as follows:

4. Configure SPI_CLK_DIV; if the APB bus clock is 120MHz and the expected SPI clock is 12MHz, then spi_clk_div should be configured as (120MHz/12MHz)/2 -1 =4=0x04. (This step can be omitted if it has already been configured and you do not want to change the clock frequency of the spi).

5. Read SPI_RW until SPI_RW [31]=0.

6. Configure SPI_RW; if you want to read RTC_MR_10MS, the internal address of this register in RTC is 0x06, so SPI_RW should be configured as 0x01860000 (spi_start=1, spi_rw=1, spi_add=0x06).

7. Read SPI_RW until SPI_RW [31]=0. Then SPI_RW [15:8] is the readback of RTC_MR_10MS value.

----Finish

3.8.4.6 RTC Automatic Thermometer Calibration

When the temperature changes, the output frequency of the crystal will also change. The relationship between the temperature and the output frequency of the crystal is definite (for a certain crystal), and this relationship has been clarified by configuring the relevant registers when the RTC is initialized. Therefore, the temperature value is collected in a certain period (for example, one minute) and written into the temperature input of the calibration algorithm, so that the RTC can generate an accurate 100Hz clock to count. There are two temperature sources for the RTC correction algorithm, one is the internal t_sensor, and the other is the external measurement value. When the chip is powered on, if the internal t_sensor is selected, considering that the internal temperature value of the chip read by the internal t_sensor is not the actual ambient temperature, the software periodically (1, 4, 8, 16 minutes) reads the internal temperature value of the chip from the internal t_sensor, Then subtract an empirical deviation value from the external ambient temperature and write it into OUTSIDE_TEMP ; when selecting an external measurement value, the scheme also provides two options, one is to use SAR_ADC + temperature sensitive resistor; the other is to connect an external temperature sensor DS1820 (DS18B20). At this time, the system will collect the temperature within a certain period and write the collection result into the external temperature register of RTC. Since the update cycle of RTC for temperature is fixed at 1, 4, 8, and 16 minutes, it is recommended that the temperature collection cycle of the system be consistent with the temperature update cycle of RTC.

When the chip is powered off, the chip temperature obtained by the internal t_sensor is basically the same as the ambient temperature, so it is recommended to directly use the chip temperature obtained by the internal t_sensor as the input of the calibration circuit. Please refer to the register TEMP_SEL to select the temperature source .

Taking the external temperature sensor DS1820 as an example, the process of RTC temperature correction is as follows:

1. Set fix_mode (TEMP_SEL bit[1]) to 0, temp_sel (TEMP_SEL bit[0]) to 1, select external internal temperature mode.
2. Set sample_time (RTC_SAR_CTRL bit[1:0]) to 0, and select the temperature update cycle as 1 minute.
3. Set INT_MASK to 0 to enable the temperature sensor acquisition interrupt.
4. Set CONVER_T to 1 to start temperature sensor acquisition.
5. Wait for the temperature sensor acquisition completion interrupt to be generated.
6. Set INT_CLEAR to 1 to clear the interrupt.
7. Read T_VALUE, and convert the temperature code word to the temperature code word of t_sensor. Then the converted temperature codeword Write to RTC internal register OUTSIDE_TEMP .
8. Wait 1 minute and repeat steps 4 to 8.

----Finish

3.8.5 Register overview

An overview of the RTC APB registers is shown in Table 3-23 .

Table 3-23 RTC APB register overview (base address is 0x2006_0000)

offset address name		describe	page number
0x0000	SPI_CLK_DIV	Clock Rate Value Register for SPI Interface	3-157
0x0004	SPI_RW	SPI interface read and write operation register	3-158
0x0080 CONVER_T		Temperature sensor acquisition control register	3-159
0x0084 CRC_EN		Temperature sensor acquisition CRC check enable control register	3-159
0x0088 INT_MASK		Temperature Sensor Acquisition Interrupt Mask Register	3-160
0x008C INT_CLEAR		Temperature sensor acquisition interrupt clear register	3-160
0x0090 BUSY		Temperature sensor acquisition status register	3-161
0x0094 INT_RAW		Temperature Sensor Acquisition Raw Interrupt Status Register 3-161	
0x0098	INT_TCAP	Temperature Sensor Acquisition Interrupt Status Register	3-162
0x009C T_VALUE		Temperature sensor acquisition result register	3-162
0x00A0 FILTER_NUM		Glitch filter width configuration register	3-163

Table 3-24 Overview of RTC internal registers (base address is 0x00)

offset address name		describe	page number
0x00	RTC_10MS_COUNT	RTC 10ms count value register	3-163
0x01	RTC_S_COUNT	RTC Second Count Value Register	3-164
0x02	RTC_M_COUNT	RTC minute counter value register	3-164
0x03	RTC_H_COUNT	RTC Time Count Value Register	3-165
0x04	RTC_D_COUNT_L	Low 8-bit register of RTC day count value	3-165
0x05	RTC_D_COUNT_H	RTC day count value high 8-bit register	3-166
0x06	RTC_MR_10MS	RTC 10ms timer value register	3-166
0x07	RTC_MR_S	RTC Second Timing Value Register	3-167
0x08	RTC_MR_M	RTC minute timer value register	3-167
0x09	RTC_MR_H	RTC Timer Value Register	3-168

offset address	name	describe	page number
0x0A	RTC_MR_D_L	Low 8-bit register of RTC daily value	3-168
0x0B	RTC_MR_D_H	High 8-bit register of RTC day time value	3-169
0x0C	RTC_LR_10MS	RTC 10ms set value register	3-169
0x0D	RTC_LR_S	RTC Second Setting Value Register	3-170
0x0E	RTC_LR_M	RTC minute setting value register	3-170
0x0F	RTC_LR_H	RTC Time Set Value Register	3-171
0x10	RTC_LR_D_L	Low 8-bit register of RTC day setting value	3-171
0x11	RTC_LR_D_H	High 8-bit register of RTC day setting value	3-171
0x12	RTC_LORD	RTC setting value enable load register	3-172
0x13	RTC_IMSC	RTC Interrupt Enable Register	3-172
0x14	RTC_INT_CLR	RTC Interrupt Clear Register	3-173
0x15	RTC_MSC_INT	RTC mask interrupt status register	3-173
0x16	RTC_RAW_INT	RTC Raw Interrupt Status Register	3-174
0x17	RTC_CLK	RTC output clock selection register	3-174
0x18	RTC_POR_N	RTC Reset Control Register	3-175
0x1A	RTC_SAR_CTRL	RTC internal t_sensor control register	3-175
0x1C	TOT_OFFSET_L	The lower 8-bit register of the correction value of tot_offset in the correction algorithm	3-176
0x1D	TOT_OFFSET_H	The upper 1-bit register of the correction value of tot_offset in the correction algorithm	3-176
0x1E	TEMP_OFFSET	Corrects the offset value register of the temperature code word of the input correction LUT	3-177
0x1F	OUTSIDE_TEMP	External ambient temperature value register	3-177
0x20	THE_TEMP	The temperature value provided by the internal t_sensor of the RTC, the code word indicates -40 to 140 degrees	3-178
0x21	TEMP_SEL	Selection of Input Temperature Sources for Calibration Algorithms	3-178
0x22	LUT1	LUT1 for temperature correction algorithm	3-179
0x23	LUT2	LUT2 for temperature correction algorithm	3-179
0x24	LUT3	LUT3 for temperature correction algorithm	3-180
0x25	LUT4	LUT4 for temperature correction algorithm	3-180

offset address	name	describe	page number
0x26	LUT5	LUT5 for temperature correction algorithm	3-180
0x27	LUT6	LUT6 for temperature correction algorithm	3-181
0x28	LUT7	LUT7 for temperature correction algorithm	3-181
0x29	LUT8	LUT8 for temperature correction algorithm	3-181
0x2A	LUT9	LUT9 for temperature correction algorithm	3-182
0x2B	LUT10	LUT10 for temperature correction algorithm	3-182
0x2C	LUT11	LUT11 for temperature correction algorithm	3-182
0x2D	LUT12	LUT12 for temperature correction algorithm	3-183
0x2E	LUT13	LUT13 for temperature correction algorithm	3-183
0x2F	LUT14	LUT14 for temperature correction algorithm	3-183
0x30	LUT15	LUT15 for temperature correction algorithm	3-184
0x31	LUT16	LUT16 for temperature correction algorithm	3-184
0x32	LUT17	LUT17 for temperature correction algorithm	3-184
0x33	LUT18	LUT18 for temperature correction algorithm	3-185
0x34	LUT19	LUT19 for temperature correction algorithm	3-185
0x35	LUT20	LUT20 for temperature correction algorithm	3-185
0x36	LUT21	LUT21 for temperature correction algorithm	3-186
0x37	LUT22	LUT22 for temperature correction algorithm	3-186
0x38	LUT23	LUT23 for temperature correction algorithm	3-186
0x39	LUT24	LUT24 for temperature correction algorithm	3-187
0x3A	LUT25	LUT25 for temperature correction algorithm	3-187
0x3B	PRAYER26	LUT26 for temperature correction algorithm	3-187
0x3C	LUT27	LUT27 for temperature correction algorithm	3-188
0x3D	LUT28	LUT28 for temperature correction algorithm	3-188
0x3E	LUT29	LUT29 for temperature correction algorithm	3-188
0x3F	LUT30	LUT30 for temperature correction algorithm	3-189
0x40	LUT31	LUT31 for temperature correction algorithm	3-189
0x41	LUT32	LUT32 for temperature correction algorithm	3-189
0x42	LUT33	LUT33 for temperature correction algorithm	3-190

offset address	name	describe	page number
0x43	LUT34	LUT34 for temperature correction algorithm	3-190
0x44	LUT35	LUT35 for temperature correction algorithm	3-190
0x45	LUT36	LUT36 for temperature correction algorithm	3-191
0x46	LUT37	LUT37 for temperature correction algorithm	3-191
0x47	LUT38	LUT38 for temperature correction algorithm	3-191
0x48	LUT39	LUT39 for temperature correction algorithm	3-192
0x49	LUT40	LUT40 for temperature correction algorithm	3-192
0x4A	LUT41	LUT41 for temperature correction algorithm	3-192
0x4B	LUT42	LUT42 for temperature correction algorithm	3-193
0x4C	LUT43	LUT43 for temperature correction algorithm	3-193
0x4D	LUT44	LUT44 for temperature correction algorithm	3-193
0x4E	LUT45	LUT45 for temperature correction algorithm	3-194
0x4F	LUT46	LUT46 for temperature correction algorithm	3-194
0x50	LUT47	LUT47 for temperature correction algorithm	3-194
0x51	sdm_coef_ouside_h	Higher 4 digits of frequency division coefficient in fixed frequency division mode	3-195
0x52	sdm_coef_ouside_l	Low 8 bits of frequency division coefficient in fixed frequency division mode	3-195

3.8.6 APB register description

SPI_CLK_DIV

SPI_CLK_DIV is the clock rate value register of SPI interface.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	spi_clk_div
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1	1 0 1 1

Bits	Access	Name	Description
[31:8]	-	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		spi_clk_div
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1	1 0 1 1

Bits	Access Name	Description
[7:0]	RW spi_clk_div	Clock rate of the SPI interface. The SPI clock must not exceed 20MHz, it is recommended to configure 12MHzÿ The value range is 1 to 255. The value of spi_clk_div is used to generate the bit rate of SPI transmission and reception, the formula is FSPICLK=FAPBCLK/(2x(spi_clk_div+1)). where FAPBCLK is Clock frequency of the APB bus. For example, the APB bus clock is 120MHz, and the expected SPI clock is 12MHz, then spi_clk_div should be configured as (120MHz/12MHz)/2 -1 =4

SPI_RW

SPI_RW reads and writes registers for the SPI interface.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	spi_add	spi_rdata / spi_wdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31]	RO spi_busy	SPI interface read and write busy status indicator. 0: Idle, new SPI read and write operations can be initiated; 1: SPI interface is being read and written, and new SPI read and write operations cannot be initiated.
[30:25]	- reserved	reserve.
[24]	W1_PULSE spi_start	Initiates an SPI read and write operation. Write 1 to auto-clear. Writing is invalid when spi_busy is 1. That is, a new SPI operation will not be started until the last read and write operation is completed. If it is started, the hardware will ignore this start request.

[23] RW spi_rw			Type of SPI operation. 0: write operation; 1: Read operation.
[22:16] RW spi_add			Address for SPI operations. The value range is 0~127.
[15:8] RO		spi_rdata	The data read back by the SPI interface.
[7:0] RW spi_wdata			Data to be written to the SPI interface.

CONVER_T

CONVER_T is the temperature sensor acquisition control register.

Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

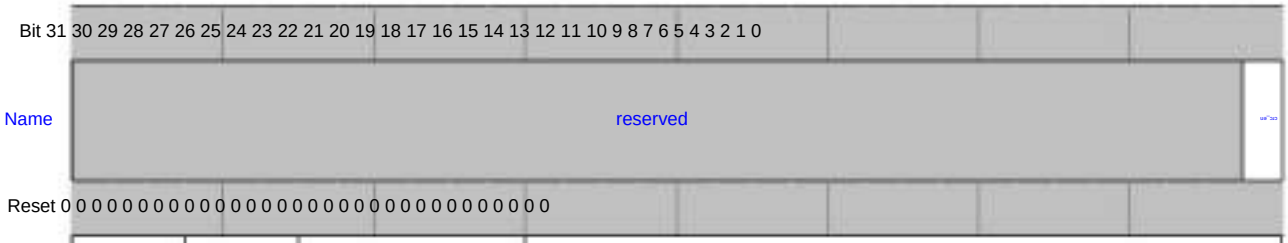
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]		reserved	reserve.
[0] RW conver_t			The temperature sensor acquisition control register start. Must be set to 1. 1: start, the hardware will automatically reset to zero when the interrupt is cleared.

CRC_EN

CRC_EN is the temperature sensor acquisition CRC check enable control register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

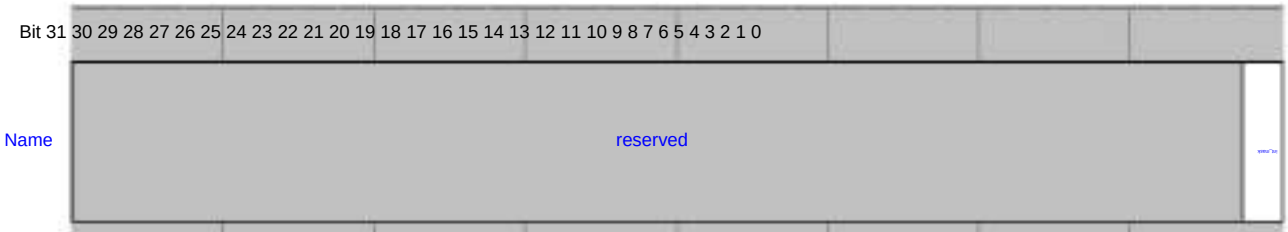


Bits	Access Name		Description
[31:1]		reserved	reserve.
[0] RW crc_en			Temperature sensor acquisition CRC check enable control register. 0ÿdisableÿ 1ÿenableÿ

INT_MASK

INT_MASK is the temperature sensor acquisition interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000



Bits	Access Name		Description
[31:1]		reserved	reserve.
[0] RW int_mask			Temperature sensor acquisition interrupt mask register. 0: no shielding; 1: Shielded.

INT_CLEAR

INT_CLEAR is the temperature sensor acquisition interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]		reserved	reserve
[0] RW int_clear			Temperature sensor acquisition interrupt clear register. Write 1 to clear interrupt. Hardware will automatically reset to zero after the interrupt is cleared.

BUSY

BUSY is the temperature sensor acquisition status register.

Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

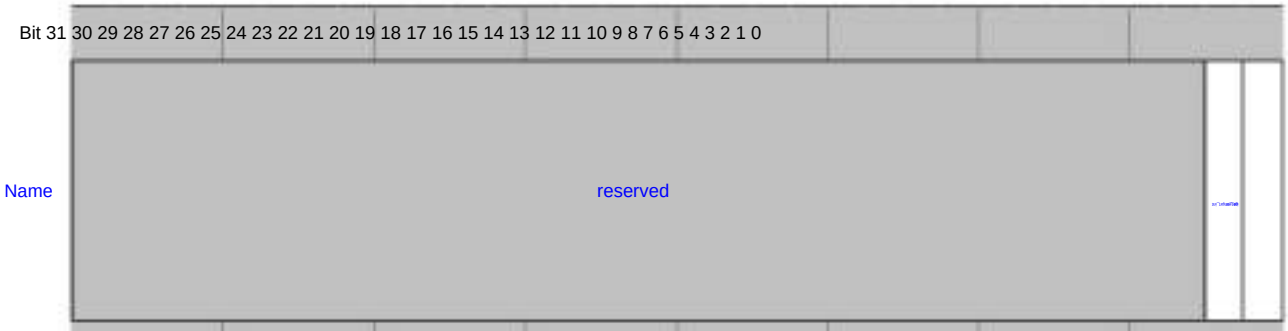
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]		reserved	reserve
[0]	RO	busy	The temperature sensor acquisition status. 0ÿreadyÿ 1ÿbusyÿ

INT_RAW

INT_RAW is the temperature sensor acquisition raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

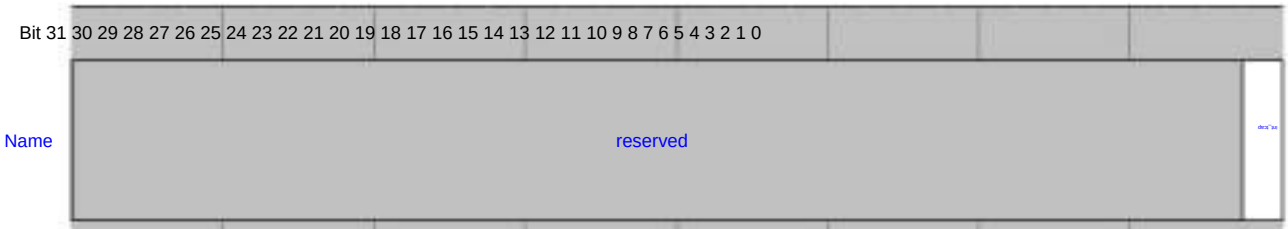


Bits	Access Name		Description
[31:2]	-	reserved	reserve.
[1]	RO	int_err	Error interrupt register.
[0]	RO	get_tmprt_int	Temperature collection complete interrupt.

INT_TCAP

INT_TCAP is the temperature sensor acquisition interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000



Bits	Access Name		Description
[31:1]	-	reserved	reserve.
[0]	RO	int_tcap	Masked interrupt status. 0: no interrupt; 1: interrupt.

T_VALUE

T_VALUE is the temperature sensor acquisition result register.

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	t_value
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	-	reserved	reserve.
[11:0]	RO	t_value	The temperature sensor collects the result.

FILTER_NUM

FILTER_NUM Filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Name	reserved	filter_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0

Bits	Access	Name	Description
[31:4]		reserved	reserve.
[3:0]	RW	filter_num	Select the input glitch width to filter N+1 APB clock width glitches.

3.8.7 Internal register description

RTC_10MS_COUNT

RTC_10MS_COUNT is the RTC 10ms count value register.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	-	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	-	reserved	reserved
[6:0]	RO	rtc_10ms_count	The value range of RTC 10ms counter value, indicating the number of 10ms time currently counted. is 0~99.

RTC_S_COUNT

RTC_S_COUNT is the RTC second count value register.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	-		rtc_s_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	reserve.
[5:0]	RO	rtc_s_count	RTC second counter value, indicating the number of seconds currently counted. The value range is 0-59.

RTC_M_COUNT

RTC_M_COUNT is the RTC sub-count value register

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_m_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	reserve.
[5:0]	RO	rtc_m_count	RTC minute counter value, indicating the number of minute time currently counted. The range is 0-59.

RTC_H_COUNT

RTC_H_COUNT is the RTC hour counter value register.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	-	reserved reserved	
[4:0]	RO	rtc_h_count	RTC hour counter value, indicating the number of hours currently counted. The range is 0-23.

RTC_D_COUNT_L

RTC_D_COUNT_L is the low 8-bit register of the RTC day count value.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	The lower 8 bits of the RTC day counter value, in conjunction with RTC_D_COUNT_H, indicates the number of days currently counted, and the value range is 0ÿ65535ÿ

RTC_D_COUNT_H

RTC_D_COUNT_H is the high 8-bit register of the RTC day count value.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	The upper 8 bits of the RTC day counter value cooperate with RTC_D_COUNT_L to indicate the number of days currently counted, and the value range is 0 to 65535.

RTC_MR_10MS

RTC_MR_10MS is RTC 10ms timer value register.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	-----	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RW	reserved	reserve.
[6:0]	RW	rtc_mr_10ms	RTC 10ms timing value, indicating the timing value of 10ms. The value range is 0~99.

RTC_MR_S

RTC_MR_S is RTC second timing value register.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	-----		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	reserve.
[5:0]	RW	rtc_mr_s	RTC second timing value, which indicates the timing second time value. The value range is 0-59.

RTC_MR_M

RTC_MR_M is RTC minute value register.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved
[5:0]	RW	rtc_mr_m	RTC sub-timer value, indicating the sub-time value of timing. The value range is 0-59.

RTC_MR_H

RTC_MR_H is the timer value register for RTC.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RW	reserved	Reserved
[4:0]	RW	rtc_mr_h	RTC hourly timer value, indicating the hourly time value of the timer. The value range is 0~23.

RTC_MR_D_L

RTC_MR_D_L is the lower 8-bit register of RTC daily value.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	The lower 8 bits of the RTC day value, cooperate with RTC_MR_D_H, to indicate the time value of the day, and the value range is 0~65535.

RTC_MR_D_H

RTC_MR_D_H is the high 8-bit register of RTC daily value.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	The high 8 bits of the RTC day value, in conjunction with RTC_MR_D_L, represent the day time value of the timer, and the value range is 0 to 65535.

RTC_LR_10MS

RTC_LR_10MS Set value register for RTC 10ms.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	-----	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	reserved	reserve.

[6:0]	RW	rtc_lr_10ms	RTC 10ms setting value, indicating the set 10ms time value. The value range is 0-99.

RTC_LR_S

RTC_LR_S Set value register for RTC seconds.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	----		rtc_lr_s					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved
[5:0]	RW	rtc_lr_s	RTC second setting value, indicating the set second time value. The value range is 0-59.

RTC_LR_M

RTC_LR_M is the RTC minute set value register.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	----		rtc_lr_m					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	reserve.
[5:0]	RW	rtc_lr_m	RTC minute setting value, indicating the set minute time value. The value range is 0-59.

RTC_LR_H

RTC_LR_H Set value register for RTC.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	-----			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:5]	RW	reserved		reserve.
[4:0]	RW	rtc_lr_h		RTC hour setting value, indicating the set hour time value. The value range is 0-23.

RTC_LR_D_L

RTC_LR_D_L is the lower 8-bit register of RTC day setting value.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:0]	RW	rtc_lr_d_l		The lower 8 bits of the RTC day setting value, cooperate with RTC_LR_D_H to indicate the set day time, and the value range is 0~65535.

RTC_LR_D_H

RTC_LR_D_H is the high 8-bit register of RTC day setting value.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:0]	RW	rtc_lr_d_h		The high 8 digits of the RTC day setting value, cooperate with RTC_LR_D_L to indicate the set day time, and the value range is 0~65535.

RTC_LORD

RTC_LORD Enable load register for RTC setting value.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:1]		reserved	reserved	
[0]	RW	rtc_load		Enable signal to write the RTC time configuration value into the RTC accumulator. After the software writes 1, the hardware will automatically clear to 0 after the loading is successful.

RTC_IMSC

RTC_IMSC is the RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							[illegible]
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	reserve.
[0]	RW	rtc_imsc	RTC timer interrupt output enable bit. 0: no output interrupt; 1: Output interrupted.

RTC_INT_CLR

RTC_INT_CLR is RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							[illegible]
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	reserve.
[0]	RW	rtc_int_clr	RTC timer interrupt clear register, after the software writes 1, the hardware will automatically clear it to 0 after the interrupt is cleared successfully.

RTC_MSC_INT

RTC_MSC_INT is RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							[illegible]
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	reserve.
[0]	RO	mask_int	mask int Status register.

RTC_RAW_INT

RTC_RAW_INT is RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							[illegible]
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	reserve.
[0]	RO	raw_int	raw int status register.

RTC_CLK

RTC_CLK is the RTC output clock selection register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]		reserved	reserve.
[1:0]	RW	clk_out_sel	Test clock selection for RTC output. 00: Output crystal oscillator clock; 01: output corrected 100Hz clock; 1X: Output 1Hz clock.

RTC_POR_N

RTC_POR_N is the RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]		reserved	reserve.
[0]	RW	rtc_por_n	Reset signal for RTC module. Set to 1 automatically after successful reset. 0: Reset.

RTC_SAR_CTRL

RTC_SAR_CTRL is the internal t_sensor control register of RTC.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_SAR_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							- -
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	reserved	reserve.
[3]	RW	reserved	reserve.
[2]	RW	reserved	reserve.
[1:0]	RW	sample_time	The temperature update time. 00: 1 minute; 01: 4 minutes; 10: 8 minutes; 11: 16 minutes.

TOT_OFFSET_L

TOT_OFFSET_L is the lower 8-bit register of the correction value of tot_offset in the correction algorithm.

Offset Address	Register Name	Total Reset Value
0x1C	TOT_OFFSET_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	tot_offset_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	tot_offset_l	The correction value of tot_offset in the correction algorithm is complement code, which means 256~255, that is to say, the value of tot_offset in the correction algorithm is 1990+(-256~255). The lower 7 bits of the register value.

TOT_OFFSET_H

TOT_OFFSET_H is the upper 1-bit register of the correction value of tot_offset in the correction algorithm.

Offset Address	Register Name	Total Reset Value
0x1D	TOT_OFFSET_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]		reserved	reserved
[0]	RW	tot_offset_h	The correction value of tot_offset in the correction algorithm is complement code, which means 256~255, that is to say, the value of tot_offset in the correction algorithm is 1990+(-256~255). The register value is the upper 1 bit.

TEMP_OFFSET

TEMP_OFFSET is the offset value register for the temperature code word of the input calibration LUT.

Offset Address	Register Name	Total Reset Value
0x1E	TEMP_OFFSET	0x00

Bit	7	6	5	4	3	2	1	0
Name			temp_offset					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]		reserved	reserved
[5:0]	RW	temp_offset	For the offset value of the temperature code word input to the calibration LUT, it is a complement code, indicating -32~31.

OUTSIDE_TEMP

OUTSIDE_TEMP is the external ambient temperature value register.

Offset Address	Register Name	Total Reset Value
0x1F	OUTSIDE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	outside_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	outside_temp	The external environment temperature value, the code word indicates -40°Cÿ140°C.

THE_TEMP

DIE_TEMP is the temperature value register provided by RTC internal t_sensor

Offset Address	Register Name	Total Reset Value
0x20	THE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	the_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	die_temp	The temperature value provided by the t_sensor inside the RTC, that is, the internal temperature of the chip, the code word indicates -40°C to 140°C.

TEMP_SEL

TEMP_SEL is the calibration input temperature selection register.

Offset Address	Register Name	Total Reset Value
0x21	TEMP_SEL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RW	reserved	reserve.

[2] RW sd_sel			Cooperate with fix_model and temp_sel to indicate whether to perform temperature compensation. When the chip is powered on and off: { temp_sel, fix_mode, temp_sel } 0xx: Turn on temperature compensation, the mode is determined by {fix_mode, temp_sel}; 110: No temperature compensation, the RTC clock directly adopts the clock after fractional frequency division, see 0x51 and 0x52 for the frequency division coefficient register; Other: reserved.
[1] RW fix_mode			Cooperating with temp_sel, it indicates the input temperature source of the calibration algorithm. See temp_sel for detailed description.
[0] RW temp_sel			Cooperating with fix_mode, it indicates the input temperature source of the correction algorithm. When the chip is powered on: {fix_mode,temp_sel} 00: Select DIE_TEMP as the temperature source; 01: Select OUTSIDE_TEMP as the temperature source; 1X: Select OUTSIDE_TEMP as the temperature source. When the chip is powered off: {fix_mode,temp_sel} 0X: Select DIE_TEMP as the temperature source; 1X: Select OUTSIDE_TEMP as the temperature source.

LUT1

LUT1 is the calibration LUT1 register.

Offset Address	Register Name	Total Reset Value
0x22	LUT1	0xAC

Bit	7	6	5	4	3	2	1	0
Name	lut1							
Reset	1	0	1	0	1	1	0	0

Bits	Access	Name		Description
[7:0]	RW	lut1		LUT1 for the temperature correction algorithm.

LUT2

LUT2 is the calibration LUT2 register.

Offset Address	Register Name	Total Reset Value
0x23	LUT2	0xB4

Bit	7	6	5	4	3	2	1	0
Name	lut2							
Reset	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut2	LUT2 for temperature correction algorithm.

LUT3

LUT3 is the calibration LUT3 register.

Offset Address	Register Name	Total Reset Value
0x24	LUT3	0xBB

Bit	7	6	5	4	3	2	1	0
Name	lot3							
Reset	1	0	1	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut3	LUT3 for temperature correction algorithm.

LUT4

LUT4 is the calibration LUT4 register.

Offset Address	Register Name	Total Reset Value
0x25	LUT4	0xC2

Bit	7	6	5	4	3	2	1	0
Name	lut4							
Reset	1	1	0	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut4	LUT4 for temperature correction algorithm.

LUT5

LUT5 is the calibration LUT5 register.

Offset Address	Register Name	Total Reset Value
0x26	LUT5	0xC8

Bit	7	6	5	4	3	2	1	0
Name	lut5							
Reset	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut5	LUT5 for temperature correction algorithm.

LUT6

LUT6 is the calibration LUT6 register.

Offset Address	Register Name	Total Reset Value
0x27	LUT6	0xCF

Bit	7	6	5	4	3	2	1	0
Name	lut6							
Reset	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut6	LUT6 for temperature correction algorithm.

LUT7

LUT7 is the calibration LUT7 register.

Offset Address	Register Name	Total Reset Value
0x28	LUT7	0xD5

Bit	7	6	5	4	3	2	1	0
Name	lut7							
Reset	1	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut7	LUT7 for temperature correction algorithm.

LUT8

LUT8 is the calibration LUT8 register.

Offset Address	Register Name	Total Reset Value
0x29	LUT8	0xDC

Bit	7	6	5	4	3	2	1	0
Name	lut8							
Reset	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut8	LUT8 for temperature correction algorithm.

LUT9

LUT9 is the calibration LUT9 register.

Offset Address	Register Name	Total Reset Value
0x2A	LUT9	0xE2

Bit	7	6	5	4	3	2	1	0
Name	lut9							
Reset	1	1	1	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut9	LUT9 for temperature correction algorithm.

LUT10

LUT10 is the calibration LUT10 register.

Offset Address	Register Name	Total Reset Value
0x2B	LUT10	0xE8

Bit	7	6	5	4	3	2	1	0
Name	fight 10							
Reset	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut10	LUT10 for temperature correction algorithm.

LUT11

LUT11 is the calibration LUT11 register.

Offset Address	Register Name	Total Reset Value
0x2C	LUT11	0xEE

Bit	7	6	5	4	3	2	1	0
Name	lut11							
Reset	1	1	1	0	1	1	1	0

Bits	Access	Name		Description
[7:0]	RW	lut11		LUT11 for temperature correction algorithm.

LUT12

LUT12 is the calibration LUT12 register.

Offset Address	Register Name	Total Reset Value
0x2D	LUT12	0xF3

Bit	7	6	5	4	3	2	1	0
Name	lut12							
Reset	1	1	1	1	0	0	1	1

Bits	Access	Name		Description
[7:0]	RW	lut12		LUT12 for temperature correction algorithm.

LUT13

LUT13 is the calibration LUT13 register.

Offset Address	Register Name	Total Reset Value
0x2E	LUT13	0xF9

Bit	7	6	5	4	3	2	1	0
Name	lut13							
Reset	1	1	1	1	1	0	0	1

Bits	Access	Name		Description
[7:0]	RW	lut13		LUT13 for temperature correction algorithm.

LUT14

LUT14 is the calibration LUT14 register.

Offset Address	Register Name	Total Reset Value
0x2F	LUT14	0xFE

Bit	7	6	5	4	3	2	1	0
Name	lut14							
Reset	1	1	1	1	1	1	1	0

Bits	Access	Name		Description
[7:0]	RW	lut14		LUT14 for temperature correction algorithm.

LUT15

LUT15 is the calibration LUT15 register.

Offset Address	Register Name	Total Reset Value
0x30	LUT15	0x03

Bit	7	6	5	4	3	2	1	0
Name	lut15							
Reset	0	0	0	0	0	0	1	1

Bits	Access	Name		Description
[7:0]	RW	lut15		LUT15 for temperature correction algorithm.

LUT16

LUT16 is the calibration LUT16 register.

Offset Address	Register Name	Total Reset Value
0x31	LUT16	0x08

Bit	7	6	5	4	3	2	1	0
Name	lut16							
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name		Description
[7:0]	RW	lut16		LUT16 for temperature correction algorithm.

LUT17

LUT17 is the calibration LUT17 register.

Offset Address	Register Name	Total Reset Value
0x32	LUT17	0x0D

Bit	7	6	5	4	3	2	1	0
Name	lut17							
Reset	0	0	0	0	1	1	0	1

Bits	Access	Name		Description
[7:0]	RW	lut17		LUT17 for temperature correction algorithm.

LUT18

LUT18 is the calibration LUT18 register.

Offset Address	Register Name	Total Reset Value
0x33	LUT18	0x12

Bit	7	6	5	4	3	2	1	0
Name	lut18							
Reset	0	0	0	1	0	0	1	0

Bits	Access	Name		Description
[7:0]	RW	lut18		LUT18 for temperature correction algorithm.

LUT19

LUT19 is the calibration LUT19 register.

Offset Address	Register Name	Total Reset Value
0x34	LUT19	0x17

Bit	7	6	5	4	3	2	1	0
Name	lut19							
Reset	0	0	0	1	0	1	1	1

Bits	Access	Name		Description
[7:0]	RW	lut19		LUT19 for temperature correction algorithm.

LUT20

LUT20 is the calibration LUT20 register.

Offset Address	Register Name	Total Reset Value
0x35	LUT20	0x1B

Bit	7	6	5	4	3	2	1	0
Name	lut20							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name		Description
[7:0]	RW	lut20		LUT20 for temperature correction algorithm.

LUT21

LUT21 is the correction LUT21 register.

Offset Address	Register Name	Total Reset Value
0x36	LUT21	0x1F

Bit	7	6	5	4	3	2	1	0
Name	lut21							
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name		Description
[7:0]	RW	lut21		LUT21 for temperature correction algorithm.

LUT22

LUT22 is the calibration LUT22 register.

Offset Address	Register Name	Total Reset Value
0x37	LUT22	0x23

Bit	7	6	5	4	3	2	1	0
Name	lut22							
Reset	0	0	1	0	0	0	1	1

Bits	Access	Name		Description
[7:0]	RW	lut22		LUT22 for temperature correction algorithm.

LUT23

LUT23 is the correction LUT23 register.

Offset Address	Register Name	Total Reset Value
0x38	LUT23	0x27

Bit	7	6	5	4	3	2	1	0
Name	lut23							
Reset	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut23	LUT23 for temperature correction algorithm.

LUT24

LUT24 is the calibration LUT24 register.

Offset Address	Register Name	Total Reset Value
0x39	LUT24	0x2B

Bit	7	6	5	4	3	2	1	0
Name	lut24							
Reset	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut24	LUT24 for temperature correction algorithm.

LUT25

LUT25 is the calibration LUT25 register.

Offset Address	Register Name	Total Reset Value
0x3A	LUT25	0x2E

Bit	7	6	5	4	3	2	1	0
Name	lut25							
Reset	0	0	1	0	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut25	LUT25 for temperature correction algorithm.

PRAYER26

LUT26 is the calibration LUT26 register.

Offset Address	Register Name	Total Reset Value
0x3B	PRAYER26	0x32

Bit	7	6	5	4	3	2	1	0
Name	pray26							
Reset	0	0	1	1	0	0	1	0

Bits	Access	Name		Description
[7:0]	RW	lut26		LUT26 for temperature correction algorithm.

LUT27

LUT27 is the calibration LUT27 register.

Offset Address	Register Name	Total Reset Value
0x3C	LUT27	0x35

Bit	7	6	5	4	3	2	1	0
Name	lut27							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name		Description
[7:0]	RW	lut27		LUT27 for temperature correction algorithm.

LUT28

LUT28 is the calibration LUT28 register.

Offset Address	Register Name	Total Reset Value
0x3D	LUT28	0x38

Bit	7	6	5	4	3	2	1	0
Name	lut28							
Reset	0	0	1	1	1	0	0	0

Bits	Access	Name		Description
[7:0]	RW	lut28		LUT28 for temperature correction algorithm.

LUT29

LUT29 is the calibration LUT29 register.

Offset Address	Register Name	Total Reset Value
0x3E	LUT29	0x3B

Bit	7	6	5	4	3	2	1	0
Name	lut29							
Reset	0	0	1	1	1	0	1	1

Bits	Access	Name		Description
[7:0]	RW	lut29		LUT29 for temperature correction algorithm.

LUT30

LUT30 is the calibration LUT30 register.

Offset Address	Register Name	Total Reset Value
0x3F	LUT30	0x3E

Bit	7	6	5	4	3	2	1	0
Name	lute30							
Reset	0	0	1	1	1	1	1	0

Bits	Access	Name		Description
[7:0]	RW	lut30		LUT30 for temperature correction algorithm.

LUT31

LUT31 is the calibration LUT31 register.

Offset Address	Register Name	Total Reset Value
0x40	LUT31	0x41

Bit	7	6	5	4	3	2	1	0
Name	lut31							
Reset	0	1	0	0	0	0	0	1

Bits	Access	Name		Description
[7:0]	RW	lut31		LUT31 for temperature correction algorithm.

LUT32

LUT32 is the calibration LUT32 register.

Offset Address	Register Name	Total Reset Value
0x41	LUT32	0x43

Bit	7	6	5	4	3	2	1	0
Name	lut32							
Reset	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut32	LUT32 for temperature correction algorithm.

LUT33

LUT33 is the correction LUT33 register.

Offset Address	Register Name	Total Reset Value
0x42	LUT33	0x45

Bit	7	6	5	4	3	2	1	0
Name	lut33							
Reset	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut33	LUT33 for temperature correction algorithm.

LUT34

LUT34 is the calibration LUT34 register.

Offset Address	Register Name	Total Reset Value
0x43	LUT34	0x48

Bit	7	6	5	4	3	2	1	0
Name	lut34							
Reset	0	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut34	LUT34 for temperature correction algorithm.

LUT35

LUT35 is the calibration LUT35 register.

Offset Address	Register Name	Total Reset Value
0x44	LUT35	0x4A

Bit	7	6	5	4	3	2	1	0
Name	lut35							
Reset	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut35	LUT35 for temperature correction algorithm.

LUT36

LUT36 is the calibration LUT36 register.

Offset Address	Register Name	Total Reset Value
0x45	LUT36	0x4B

Bit	7	6	5	4	3	2	1	0
Name	lut36							
Reset	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut36	LUT36 for temperature correction algorithm.

LUT37

LUT37 is the calibration LUT37 register.

Offset Address	Register Name	Total Reset Value
0x46	LUT37	0x4D

Bit	7	6	5	4	3	2	1	0
Name	lut37							
Reset	0	1	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut37	LUT37 for temperature correction algorithm.

LUT38

LUT38 is the calibration LUT38 register.

Offset Address	Register Name	Total Reset Value
0x47	LUT38	0x4F

Bit	7	6	5	4	3	2	1	0
Name	lut38							
Reset	0	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut38	LUT38 for temperature correction algorithm.

LUT39

LUT39 is the calibration LUT39 register.

Offset Address	Register Name	Total Reset Value
0x48	LUT39	0x50

Bit	7	6	5	4	3	2	1	0
Name	lut39							
Reset	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut39	LUT39 for temperature correction algorithm.

LUT40

LUT40 is the calibration LUT40 register.

Offset Address	Register Name	Total Reset Value
0x49	LUT40	0x51

Bit	7	6	5	4	3	2	1	0
Name	lut40							
Reset	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut40	LUT40 for temperature correction algorithm.

LUT41

LUT41 is the calibration LUT41 register.

Offset Address	Register Name	Total Reset Value
0x4A	LUT41	0x52

Bit	7	6	5	4	3	2	1	0
Name	lut41							
Reset	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut41	LUT41 for temperature correction algorithm.

LUT42

LUT42 is the calibration LUT42 register.

Offset Address	Register Name	Total Reset Value
0x4B	LUT42	0x53

Bit	7	6	5	4	3	2	1	0
Name	lut42							
Reset	0	1	0	1	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut42	LUT42 for temperature correction algorithm.

LUT43

LUT43 is the calibration LUT43 register.

Offset Address	Register Name	Total Reset Value
0x4C	LUT43	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut43							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut43	LUT43 for temperature correction algorithm.

LUT44

LUT44 is the calibration LUT44 register.

Offset Address	Register Name	Total Reset Value
0x4D	LUT44	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut44							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name		Description
[7:0]	RW	lut44		LUT44 for temperature correction algorithm.

LUT45

LUT45 is the calibration LUT45 register.

Offset Address	Register Name	Total Reset Value
0x4E	LUT45	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut45							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name		Description
[7:0]	RW	lut45		LUT45 for temperature correction algorithm.

LUT46

LUT46 is the calibration LUT46 register.

Offset Address	Register Name	Total Reset Value
0x4F	LUT46	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut46							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name		Description
[7:0]	RW	lut46		LUT46 for temperature correction algorithm.

LUT47

LUT47 is the calibration LUT47 register.

Offset Address	Register Name	Total Reset Value
0x50	LUT47	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut47							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut47	LUT47 for temperature correction algorithm.

Sdm_coef_ouside_h

Sdm_coef_ouside_h is the high 4-bit register of the external frequency division coefficient.

Offset Address	Register Name	Total Reset Value
0x51	Sdm_coef_ouside_h	0x8

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Sdm_coef_ouside_h			
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]		reserved	reserve.
[3:0]	RW	Sdm_coef_ousi de_h	Higher 4 bits of frequency division coefficient in fixed frequency division mode.

Sdm_coef_ouside_l

Sdm_coef_ouside_l is the lower 8-bit register of the external frequency division coefficient.

Offset Address	Register Name	Total Reset Value
0x52	Sdm_coef_ouside_l	0x1B

Bit	7	6	5	4	3	2	1	0
Name	Sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	Sdm_coef_ousi	The lower 8 bits of the frequency division factor in the fixed frequency division mode. Note: When reading/writing de_l to the frequency division coefficient register (0x51, 0x52), you should first read/write the high 4 bits, and then read/write the low 8 bits, and the continuous operation from the high bit to the low bit is required to complete the read/write operation .

3.9 Power Management and Low Power Mode Control

3.9.1 Overview

The low power consumption mode of the chip is used to effectively reduce the power consumption of the chip. The chip provides a variety of low power consumption controls to dynamically reduce the power consumption of the chip.

System working mode control In addition to NORMAL mode, various modes have a certain effect on reducing power consumption, and different working modes can be selected according to actual power consumption requirements and functional requirements.

Clock Gating and Clock Frequency Adjustment

Provides a clock shutdown function, which can turn off unnecessary clocks and reduce power consumption of the chip. The clock frequency of the system can be adjusted, and the clock frequency can be adjusted to reduce the power consumption of the chip when the function is satisfied. Module-level low-power control provides module-level low-power control. When a module is not working, turn off the module or put the module in a low-power state to reduce chip power consumption.

DDR low power consumption control The DDR controller and related pins have a dynamic power consumption control function. You can choose to start this function to reduce chip power consumption, and you can also start the DDR self-refresh mode to reduce the power consumption of the entire product. .

3.9.2 System working mode

The system provides two working modes:

Normal working mode: corresponding to the NORMAL mode in the system running mode control. When the system normally works in NORMAL mode, the power consumption during operation can be reduced by controlling the running clock frequency and setting the low power consumption control of the module and DDR. Standby mode: corresponding to the SLOW mode and DOZE mode in the system operation mode control. ÿThe working system in standby working mode operates at a very low working clock, and the clocks of most unused modules are turned off, so the power consumption is low.

ÿ In SLOW or DOZE mode, the standby power consumption can be directly reduced by turning off the power of the non-working modules.

Mode switching is configurable in the system controller. See the System Controller chapter.

3.9.3 Clock Gating and Clock Frequency Adjustment

The system provides the clock gating function of each module. When the module is idle, the corresponding clock can be turned off to reduce the power consumption of the chip. For the operation process, please refer to the clock gating part of each module.

In NORMAL mode, the system can reduce chip power consumption by adjusting the operating frequency, as follows:

Close the service module so that it does not access DDR.

The system switches to run in on-chip memory.

Configure DDRC_SREFCTRL[sr_seq] as valid value, DDRC will control DDRn SDRAM to enter self-refresh mode.

1. Configure SC_PLLCTRL[27:3] as the PLL stabilization time.
2. Configure PERI_CRG0 and PERI_CRG1 to control the PLL frequency division ratio.
3. According to the configuration requirements of DDRC, after waiting for a certain period of time, configure DDRC_SREFCTRL to exit self-refresh new, for normal operation.
4. The program jumps to run in DDR.

----Finish

In addition to the adjustment of the system operating frequency, the operating frequency of some modules can also be adjusted independently. Adjusting the operating frequency of these modules can also further reduce the power consumption of the system. For details, refer to the section on clock source selection of each module in "3.2.3 Clock Configuration".

3.9.4 Module level low power consumption control

PHY modules such as USB 2.0 Host, SATA, Video DAC and PLL in the chip can provide low power consumption working modes. (Refer to the register description of the system controller, clock, etc.)

Low power consumption control of USB 2.0

Host module ÿ Set PERI_CRG46 bit[7] to 0 to turn off the clock of USB 2.0 Host. ÿSet

PERIPHCTRL21 bit[22] to 1, turn off the USB PHY power supply.

Low power consumption control of

SATA module ÿ Set PERI_CRG45 bit[9]/PERI_CRG45 bit[8] to 0, turn off SATA Port0 and SATA Clock for Port1.

ÿSet PERIPHCTRL25 bit[2] to 1, and turn off the power of SATA PHY.

Low power consumption control when Video DAC

is not in use ÿ Set PERI_CRG13 bit[7] to 0, turn off VOU SD DAC clock.

ÿ When PERI_CRG13 bit[6] is 0, the VOU HD DAC clock is turned off.

ÿ When PERIPHCTRL4 bit[30] is 1, the VOU SD DAC power supply is turned off.

ÿ When PERIPHCTRL4 bit[31] is 1, the VOU HD DAC power supply is turned off.

PLL provides the function of low power consumption. If the PLL is not used, the PLL can be turned off to make the system in a

low power consumption state: ÿ If APLL is not needed, configure PERI_CRG1 bit[21] to 0, disable APLL, and make APLL in low power state.

ÿ If you do not need to use VPLL0, configure PERI_CRG3 bit[21] as 0, disable VPLL0, and make VPLL0 is in a low power state.

ÿ If EPLL is not needed, configure PERI_CRG9 bit[21] to 0, disable EPLL, and make EPLL in a low power consumption state.

BOOTROM, etc. provide internal ROM power-off control. (See System Controller Register Description)

Low power consumption control of BOOTROM module: PERIPHCTRL2 bit[0] is 1, turn off the power supply of ROM inside BOOTROM module.

3.9.5 DDR Low Power Control

For details about DDRC low power control, please refer to "Low Power Configuration" in "DDRC Working Mode".

3.10 Processor Subsystem

3.10.1 ARM Cortex-A9 Processor

Hi3520D uses ARM Cortex-A9MPCore single-core processor, which has the following characteristics:

The maximum operating frequency of the processor is 660MHz.

L1 Cache includes 32KB Instruction Cache and 32KB Data Cache.

Contains 128KB L2 Cache, L2 Cache has the same frequency as the processor, and the operating frequency relationship register with the AXI bus can be configured. As shown in Table 3-25 , two frequency relationships are supported.

Table 3-25 The working frequency relationship between CPU and AXI bus

L2 Cache to AXI Bus Frequency Ratio		frequency description
Bus frequency 330MHz	2:1	L2 frequency 660MHz, bus frequency 330MHz
	1:1	L2 frequency 330MHz, bus frequency 330MHz

The processor integrates the interrupt controller GIC (Generic Interrupt Controller), which supports the processing of 96 interrupt sources, including 64 external interrupts.

The processor is an out-of-order dual-issue structure, based on a single-thread structure, 2.5DMIPS.

The processor uses eight-stage

pipeline. Contains MMU (Memory Management Unit). Support Vxworks,

Linux and other operating systems. Supports branch prediction

based on GHB (Global History Buffer), and the accuracy of branch prediction reaches 95%. Support JTAG debug interface.

3.10.2 L2 Cache

L2 Cache has the following characteristics:

128KB in size.

Based on physical address and physical tag.

Cache Lockdown of Format C is supported. Lockdown classifies instructions and data operations, and the RAM space locked down can be used as TCM (Tightly Coupled Memory) of the processor.

The size of Cache Line is fixed at 32byte (8word/256bit), and the write operation supports writing by byte. Support write back

(write back), write through (write through), read Allocate and write Allocate operations, the actual mode is determined based on the page table.

Support PipeLine access to TAG RAM and DATA RAM, which can be completed once per clock cycle
TAG RAM query, and DATA RAM read and write. Three LFBs

(Line Fill Buffer) are provided. The function of this Buffer is to cache the data from the memory Allocate until the data fills up a Line before submitting it to the L2 Memory. Provide 2 LRB (Line Read Buffer) for each Slave

port, the function of this Buffer is to supply the Cache Line of L1 cache after the cache hits. Provide 3 EB (Eviction Buffer), the function of this Buffer is to cache the data replaced by L2

Cache and ready to be written into the main memory.

Provide 3 WB (Write Buffer), the Buffer cache is written from L1, and the data that needs to be written into memory and L2 Cache; the Buffer includes 1 address space and 256bit data space, and supports data writing within 1 Line 1 data slot.

Supports the forced write Allocate function, which forces all cacheable write operations to occur Allocate operations. Shared mode

setting is supported. By default, Shared operations are identified as Cacheable and Not Allocate.

Support keyword priority.

Support atomic Sync operation.

Support pseudo-random replacement algorithm, which is related to the actual Lockdown state (the replacement algorithm will not work in the case of direct

connection). Provide Exclusive Cache function, which can be enabled by software configuration; when enabled, data can be prohibited from existing in L1 level and L2 level at the same time.

Clean (clean up) and Invalidate (invalid) are supported according to Way (road), Way+Index (Lujia index), and Address (address). Support ECC of Cache Memory,

Tag RAM and Data RAM both support 1bit error correction. Support Cache Disable function, under this function,

Cache is bypassed, and all L1 operations are transparently transmitted to
memoryÿ

Support L2 Cache performance statistics, Cache provides statistics including Cache access events, write back events, miss events, miss and wait events. It supports

the statistics of events inside the Cluster, and supports the configuration of special signals inside the Cluster.

说明

For the principle of Format C Lockdown, please refer to ARM Architecture Reference Manual.

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4 memory interface

4.1 DDRC

4.1.1 Overview

DDRC (DDR2/3 SDRAM Controller) realizes the access control to the dynamic memory DDR2/3 SDRAM. In the following, DDRn SDRAM will be used instead of DDR2/3 SDRAM.

说明

Hi3520D/Hi3515A has 1 DDRC, which supports 16bit DDR bit width.

4.1.2 Features

Features of DDRC:

DDRC provides a DDRn SDRAM chip select space, supports a data bus width of 16 bits, and an address bus width of up to 15 bits. The maximum

supported storage space is: 4Gbit in 16bit mode. Support

660MHz DDRn SDRAM bus operating frequency. Support low

power consumption modes such as Power Down and SELF Refresh of DDRn SDRAM. Support

burst4, burst8 transfer mode of DDR2 SDRAM; burst8 transfer mode of DDR3 SDRAM.

4.1.3 Functional description

4.1.3.1 Application Block Diagram

DDRC realizes the data access of external memory DDRn SDRAM from CPU and other main devices in the SoC system. Configure the timing parameter register of DDRC through CPU to support DDR2 SDRAM device and DDR3 SDRAM device conforming to JEDEC (JESD79) standard. Table 4-1 lists the DDR2 SDRAMs of several mainstream DRAM manufacturers supported by DDRC. This table describes the working frequency of DDR2 SDRAM without considering the limitations of capacity and other factors.

Table 4-1 List of DDR2 SDRAM supported by DDRC

manufacturers	200MHz	333MHz	400MHz	Remark
JESD79 ÿDDR2 Standardÿ	DDR2-400 DDR2-533 DDR2-667 DDR2-800	DDR2-667 DDR2-800	DDR2-800	1ÿ2
Micron	-5E DDR2-400 -37E DDR2-533 -3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-25 DDR2-800 -25E DDR2-800	1ÿ2
ELPIDA	-4A DDR2-400 -5C DDR2-533 -6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-8E DDR2-800 1ÿ2	
Hynix	- E3 DDR2-400 -C4 DDR2-533 -Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-S5 DDR2-800 -S6 DDR2-800	1ÿ2
Samsung	-CC DDR2-400 -D5 DDR2-533 -E6 DDR2-667 - E7 DDR2-800	-E6 DDR2-667 - E7 DDR2-800	-E7 DDR2-800 1ÿ2	

Note:

1. DDRC supports DRAM devices that meet the JESD79 standard. In different operating modes, DDRC can only support devices whose DRAM operating frequency is higher than or equal to DDRC operating frequency. When using devices from manufacturers other than those listed in the table, you can refer to this standard to select devices.

2. In the table, the operating frequency of each manufacturer's DDR2 SDRAM is used as the basic element for judgment. In real device products, there are various series versions of capacity and bit width for the same operating frequency, but as long as the operating frequency of the DDR2 SDRAM is in this list, DDRC can support the DDR2 SDRAM. For the selection of capacity and bit width, the choice is made according to the actual application scenario of the chip.

The list of DDR3 SDRAM supported by DDRC is shown in Table 4-2 .

Table 4-2 List of DDR3 SDRAM supported by DDRC

manufacturers	400MHz	533MHz	800MHz	Remark
JESD79 ÿDDR3 Standardÿ	DDR3-800 DDR3-1066 DDR3-1333		-	3ÿ4

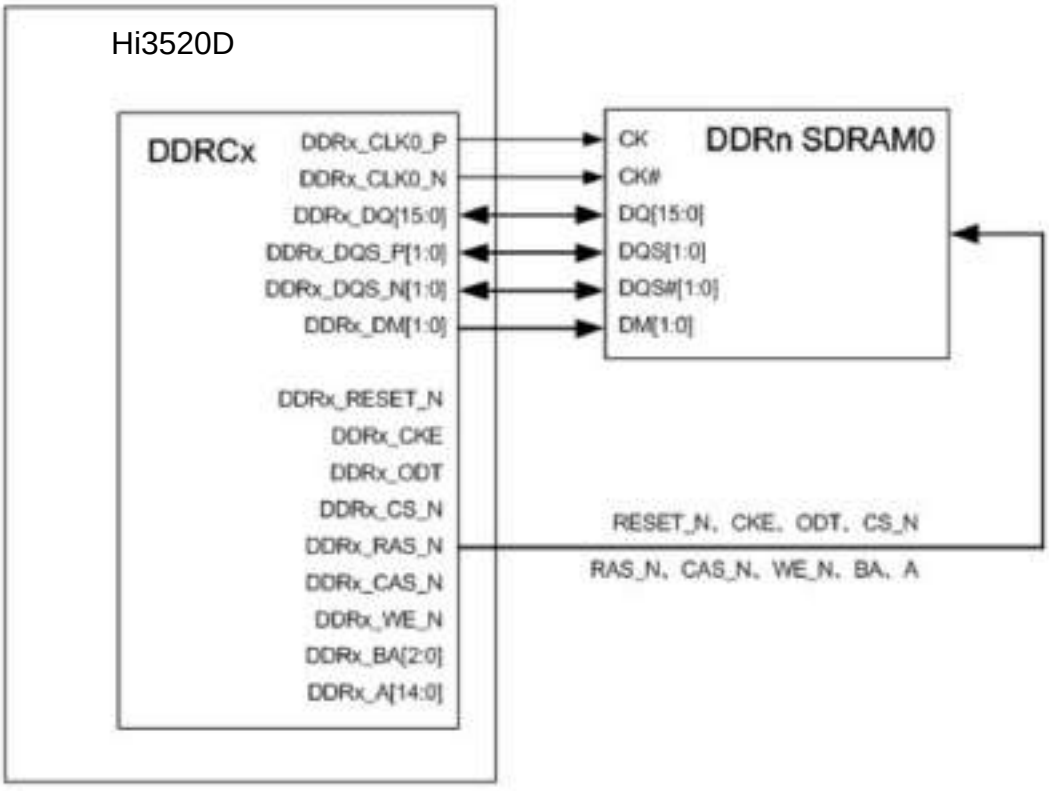
Note:

3. If the working frequency of DDRC is 400MHz, all supported DDR3 can be down-clocked to 400MHz.

4. The supported device types here are based on the JEDEC standard.

DDRC supports 16bit interconnect mode. In this mode, DDRC is connected to one piece of DDRn SDRAM with a data bus width of 16bit or two pieces of DDRn SDRAM with a data bus width of 8bit. Taking a piece of 16bit DDRn SDRAM as an example, the connection diagram is shown in Figure 4-1 .

Figure 4-1 Schematic diagram of the interconnection between a single DDRC and a piece of DDRn SDRAM



Connection

instructions: 1. x=0 or 1 in DDRCx and DDRx means the xth DDR controller.

2. DDRn SDRAMx is a storage device with a data bus width of 16 bits.

3. DDRC command control signals: DDRx_CKE, DDRx_RESET_N, DDRx_ODT, DDRx_CS_N, DDRx_RAS_N, DDRx_CAS_N, DDRx_WE_N, DDRx_BA[2:0], DDRx_A[13:0] are connected to the command control signal of DDRn SDRAM, that is, the command control bus of DDRC is a connection mode of 1 drive 1. 4. When the DDR2 SDRAM capacity is less than 1Gbit, the DDRx_BA[2] address signal output of DDRC is suspended. 5. In DDR2 mode, DDRx_RESET_N is floating.

4.1.3.2 Functional principle

The DDRC interface timing meets the JESD79 standard, and completes the data access and state control of the DDRn SDRAM by sending the command word of the DDRn SDRAM. Including DDRn SDRAM read and write access, automatic refresh, low power consumption control and other functions.

command truth table

DDRC supports the read and write and control command words of DDRn SDRAM. The command truth table of DDRC is shown in Table 4-3 .

Table 4-3 DDRC command truth table

FUNCTION DDRn_	CKE	DDRn_ CSN	DDRn_ Rasna	DDRn_ CASN	DDRn_ WEN	DDRn_ADR			DDRn_ NOT
						11 AP(10) 9:0			
DESELECT H		H	X	X	X	X X		X X	
ACTIVE	H	L	L	H	H	V V		V V	
READ	H	L	H	L	H	V V		V V	
WRITE	H	L	H	L	L	V V		V V	
PRECHARGE H		L	L	H	L	X L		X V	
PRECHARGE ALL	H	L	L	H	L	X H		X X	
AUTO REFRESH	H	L	L	L	H	X X		X X	
SELF REFRESH	L	L	L	L	H	X X		X X	
MODE REGISTER SET	H	L	L	L	L	V V		V V	
ZQCL	H	L	H	H	L	X H		X X	
ZQCS	H	L	H	H	L	X L		X X	

H: Indicates high level; L: Indicates low level; V: Indicates valid; X: Indicates don't care.

ZQCL (ZQ Calibration Long): It is used to start the ZQ Calibration operation of DDR3 when DDR3 SDRAM is powered on and initialized.

ZQCS (ZQ Calibration Short): It is used to start the ZQ Calibration operation of DDR3 when the environmental conditions of the chip change.

Auto Refresh

When configuring DDRC_TIMING2 [taref] as a non-zero value, DDRC automatically generates periodic AUTO REFRESH commands to complete the refresh operation on DDRn SDRAM. At normal temperature, DDRn SDRAM requires 8,192 auto-refresh operations to be completed within 64ms, that is, the cycle of auto-refresh operations is 7.8μs. The relationship between the configuration value (Taref) of DDRC_TIMING2[taref] and the automatic refresh period (T=7.8μs or 3.9μs) is:

TarefýT / (16 x DDR clock period)

When DDRC_TIMING2[taref] is configured , the counter inside DDRC will automatically load the Taref value to count down. When the counter value is 0, DDRC initiates an automatic refresh operation and reloads the Taref value to count.

Low Power Management

DDRC supports low-power management in two modes: normal low-power mode and self-refresh low-power mode.

When the system is in an idle state (the DDRC bus interface has no read/write DDR access for a certain period of time), it automatically controls the DDRn SDRAM to enter the normal low power consumption mode.

When the system needs to enter the standby mode, the DDRn SDRAM can be controlled to enter the self-refresh low-power mode by configuring the DDRC_SREFCTRL[sr_req] register. In this mode, the power consumption of DDRn SDRAM can be reduced to the minimum, and the data in DDRn SDRAM can be kept at the same time, but the system cannot access DDRn SDRAM at this time.

arbitration mechanism

DDRC implements a priority scheduling algorithm. Configure DDRC_QOS[pri] register, DDRC will add priority attribute to the command of the bus, and then schedule according to the priority attribute of the command to achieve high-efficiency access to DDRn SDRAM. Configure DDRC_QOS[qos_en] and DDRC_QOSx[qos], DDRC will add the response delay (timeout) attribute to the bus command, and then realize the guarantee of the bus command response delay according to the scheduling algorithm of response delay priority. Configure DDRC_FLUX[flux_port_en] and DDRC_FLUX[flux], DDRC will add flow control attributes to the ports of the bus, and allocate the traffic of each bus port under the premise that the delay time is not exhausted, so as to ensure that each port is busy when DDRC accesses bandwidth.

address mapping method

DDRC realizes the conversion of the access address of the system bus to the access address of DDRn SDRAM. Configure the registers DDRC_RNKCFG[mem_map], DDRC_RNKCFG[mem_row] and DDRC_RNKCFG[mem_col], DDRC converts the system bus address to DDRn SDRAM address according to the address mapping algorithm.

The following example illustrates the mapping algorithm of system bus address and DDRn SDRAM address. Suppose the system bus address is BUSADR[28:0], the effective address is BUSADR[m-1:0], the address of DDRn SDRAM is DDRADR[13:0]. When DDRADR[13:0] is used as a row address, its effective address is DDRROW[x-1:0], when it is used as a column address, its effective address is DDRCOL[y-1:0], and the BANK address of DDR is DDRBA[z 1:0], the storage data bus width of DDRC is DW, and the address mapping relationship at this time is:

When DDRC_RNKCFG[mem_map] is 0b00, RBC mapping method:

BUSADR[m-1:0] = {DDRROW[x-1:0],DDRBA[z-1:0],DDRCOL[y-1:0],DW{b0}}

When DDRC_RNKCFG[mem_map] is 0b01, BRC mapping method:

BUSADR[m-1:0] = {DDR_BA[z-1:0],DDRROW[x-1:0],DDRCOL[y-1:0],DW{b0}}

In the above expression, the relation of parameters satisfies: m = x+y+z+DW.

When DDRC is in 16bit application mode, DW is 1.

When DDRC_RNKCFG[mem_map] is 0b00 and A10 is used as the AP function bit of DDR, the mapping table from system bus address to DDRn SDRAM address is shown in Table 4-4.

This table illustrates the address mapping relationship in RBC mode. In BRC mode, the address mapping is performed according to the above expression.

Table 4-4 DDRC 16bit mode address mapping table

Memory Type Row Address		column address	DDR BA			row address	DDR ADR								
Mbit×bw	width	width	2 1 0			column address	13 12 11 10/AP 9 8 [7:0]								
256Mbit 4bank															
16×16	13	9		11 10		Row Address -		24 23 22				21 20 [19:12]			
						column address -			- AP				9 [8:1]		
512Mbit 4bank															
32×16	13	10		12 11		Row Address -		25 24 23				22 21 [20:13]			
						column address -			- AP			10 9 [8:1]			
1024Mbit 8bank															
64×16	13	10	13 12 11			row address 26 25 24						23 22 [21:14]			
						column address -			- AP			10 9 [8:1]			
2048Mbit 8bank															
128×16	14	10	13 12 11			row address 27 26 25 24						23 22 [21:14]			
						column address -		-	- AP			10 9 [8:1]			

4.1.4 Working method

4.1.4.1 Clock gating

After the system enters the low power consumption mode, the working clock of DDRC can be turned off. Also, before the system returns to normal mode, the working clock of DDRC needs to be turned on.

DDRC enters low power consumption mode and the clock is turned off:

1. The system enters into Flash or TCM to run.
2. Set DDRC_SREFCTRL[sr_req] to 1 to request to enter self-refresh mode.
3. Check DDRC_STATUS[in_sr] until its value is 1, then enter low power consumption mode.
4. Set DDRC_PHY_REG4 [phy_ck_en] to 0x0, turn off the DDR clock.
5. Turn off the DDRC clock.
6. The system enters a low power state.

----Finish

DDRC exits low power consumption mode, the process of clock opening:

1. The system enters the normal working mode and turns on the DDRC clock.
2. Configure DDRC_CONFIG1 to 0x0040_0785; configure DDRC_PHY_REG4 [phy_ck_en] to 0x1, Turn on the DDR clock.
3. Configure the register DDRC_PHYCTRL (offset address: 0x408) to 0x0 to start the initialization of ddrphy change.
4. The software waits for a period of time (500ns), and queries the register DDRC_PHYSTATUS[phy_init_done] (offset address: 0x404) until it is 1.
5. Set DDRC_SREFCTRL[sr_req] to 0 to request to exit the self-refresh mode.
6. Check the DDRC_STATUS[in_sr] bit until its value is 0, indicating that the DDR low power consumption mode has been exited.
7. The system can access DDR normally.

----Finish

4.1.4.2 Soft reset

DDRC cannot perform a single reset operation. DDRC can only be reset during global soft reset. After reset, DDRn SDRAM needs to be re-initialized according to the initialization process.

4.1.4.3 DDR2 initial configuration process

After the system is powered on, the initialization of DDR2 SDRAM must be completed before the system can access DDR2 SDRAM. The following points need to be noted before initialization:

When powering on DDR2 SDRAM, the JEDEC standard needs to be followed. That is, first provide VDD, then provide VDDQ, and finally provide VREF and VTT. This initialization process needs to be carried out after the system enters NORMAL mode.

In DDRC 16bit mode, assuming that the storage space is composed of two DDR2 SDRAMs with a capacity of 2Gbit and a data bus width of 8bit, the initialization steps of DDR2 SDRAM are as follows:

1. The software waits for more than 200μs.
2. Configure the DDRC_PHYCTRL register (offset address: 0x408) to 0x0 to start initializing ddrphy change.
3. The software waits for a period of time (500ns), and queries the register DDRC_PHYSTATUS[phy_init_done] (offset address: 0x404) until it is 1.
4. According to the operating frequency and device requirements, configure the DDRC_EMRS01 register and DDRC_EMRS23 register to set the DDR read delay (cas latency), write recovery delay (write recovery), burst length (burst length), DDR device output drive impedance and Input ODT impedance, etc.

说明

cas latency must be set to the same value as DDRC_TIMING1[cl].

The DDRC_EMRS01 register corresponds to the mode register (MRS) and extended mode register 1 (EMRS1) of DDR2 SDRAM. When configuring this register, you only need to configure the A15-A0 bits of the mode register in the DDR2 SDRAM device manual (the actual effective bits are: A13~A0), and you do not need to configure the highest 3 bits A18~A16 register selection bits of the mode register, that is, bank address. However, the bank address of some DDRn SDRAM manufacturers is: A17~A15.

The extended mode register 1 (EMRS1) of **DDR2 SDRAM** needs special attention: both **RDQS** and DQS# in the mode register are configured as disabled mode (disable).

5. Set the DDRC_CONFIG0 register to 0x8000_0500, which means DDRC is in 16bit DDR2 SDRAM mode, where [pd_en] is set to 0, and power down is prohibited. DDRC_CONFIG1 register is 0x0000_0785, where [read_mode]=0, [wr_rcv_mode]=1, [clkratio]=0x1, [ecc_en]=0x0, [zqc_en]=0x1.

   说明

   The power-on reset value of the low-power configuration is off. During the initialization process, the low-power automatic entry function and the clock automatic shutdown function must be turned off. However, in normal use, it is recommended to enable low-power control to reduce power consumption.

   The DDRC_CONFIG1[wr_rcv_mode] bit must be set to 1, otherwise the chip bus may hang.

6. According to the operating frequency and device requirements, configure DDRC_TIMING2 bit[31:11], and configure [taref] as 0x000 to disable auto refresh.

7. Configure the DDRC_RNKCFG0~3 registers to 0x0000_0142 according to the single chip capacity of the device. The bus address mapping mode is RBC-DW mode, the AP is A10, the column address width is 10, and the row address width is 15.

8. According to the operating frequency and device requirements, configure DDRC_TIMING0, DDRC_TIMING1, DDRC_TIMING3ÿ

9. Configure the storage space base address register DDRC_BASEADDR as 0x8000_0000.

10. According to the actual application, configure DDRC_QOSCFG0 and DDRC_QOSCFG1; DDRC_QOS (DDRC_RDQOS0~DDRC_RDQOS15). For these registers, default configuration values can also be used.

11. Configure DDRC_ODTCFG[wodt0]=0x1, DDRC_ODTCFG[rodt0]=0x0.

12. Configure DDRC_DTRCTRL register [train_mode]=1, [train_en]=0, use ddrphy read dqs to automatically Gated training mode.

13. Configure the DDRC_SREFCTRL register as 0x0 to exit the self-refresh state.

14. Query DDRC_STATUS [in_sr] until in_sr is 0 or the software waits for more than 1μs.

15. Configure DDRC_INITCTRL register (address: 0x008) to 0x1 to start SDRAM initialization operation.

16. The software waits for a period of time (500ns), and queries DDRC_STATUS[in_init] (address: 0x0) until 0x1.

17. According to the working frequency, configure DDRC_PHYREG4A[cas latency] (address: 0x838), and configure DDRC_PHYREG4A[additive latency] to 0.

18. Configure the DDRC_PHYREG2 (address: 0x808) register to 0x1 to start the automatic motion training operation.

19. The software waits for a period of time (500ns) and queries DDRC_PHYREG62[phy_cal_done_h] (address: 0xB48) and DDRC_PHYREG62[phy_cal_done_l] until DDRC_PHYREG62[phy_cal_done_h] =0x1 ÿ DDRC_PHYREG62=0x1ÿ

20. Configure DDRC_PHYREG2 (address: 0x808) as 0x0 to disable PHY read dqs training operation.

21. According to the actual working frequency, configure DDRC_TIMING2[taref] to enable auto refresh.

22. Start the software gating training mode until the gating signal training of reading dqs is completed.

----Finish

After completing the above steps, DDR2 SDRAM can work normally.

4.1.4.4 DDR3 initial configuration process

After the system is powered on, the initialization of DDR3 SDRAM must be completed before the system can access DDR3 SDRAM.
The following points need to be noted before initialization:

When powering on DDR3 SDRAM, the JEDEC standard needs to be followed. That is, first provide VDD, then provide VDDQ, and finally provide VREF and VTT. This initialization process needs to be carried

out after the system enters NORMAL mode.

In DDRC 16bit mode, assuming that the storage space is composed of two DDR3 SDRAMs with a capacity of 2Gbit and a data bus width of 8bit, the initialization steps of DDR3 SDRAM are as follows:

1. The software waits for more than 200μs.

2. Configure the DDRC_PHYCTRL register (offset address: 0x408) to 0x0 to start initializing ddrphy change.

3. The software waits for a period of time (500ns), and queries the register DDRC_PHYSTATUS[phy_init_done] (offset address: 0x404) until it is 1.

4. According to the operating frequency and device requirements, configure the DDRC_EMRS01 register and DDRC_EMRS23 register, To set the DDR read delay (cas latency), write delay (cas write latency), write recovery delay (write recovery), burst length (burst length), DDR device output drive impedance and input ODT impedance, etc.

说明

cas latency must be set to the same value as DDRC_TIMING1[cl].

The DDRC_EMRS01 register corresponds to the mode register (MRS) and extended mode register 1 (EMRS1) of DDR3 SDRAM. When configuring this register, you only need to configure the A15-A0 bits of the mode register in the DDR2 SDRAM device manual (the actual effective bits are: A13~A0), and you do not need to configure the highest 3 bits A18~A16 register selection bits of the mode register, that is, bank address. However, the bank address of some DDRn SDRAM manufacturers is: A17~A15.

5. Set the DDRC_CONFIG0 register to 0x8000_0600, indicating that DDRC is in 16bit DDR3 SDRAM mode, where [pd_en] is configured as 0x0, and power down is prohibited. The DDRC_CONFIG1 register is 0x0000_0785, where [read_mode]=0, [wr_rcv_mode=0x1], [clkratio]=0x1, [ecc_en]=0x0, [zqc_en]=0x1.

说明

The power-on reset value of the low-power configuration is off. During the initialization process, the low-power automatic entry function and the clock automatic shutdown function must be turned off. However, in normal use, it is recommended to enable low-power control to reduce power consumption.

The DDRC_CONFIG1[wr_rcv_mode] bit must be set to 1, otherwise the chip bus may hang.

6. According to the operating frequency and device requirements, configure DDRC_TIMING2 bit[31:11], and configure [taref] as 0x000 to disable auto refresh.

7. Configure the DDRC_CTRL register to 0x0001, and configure DDR3 SDRAM to exit the reset state.

8. The software waits for more than 500μs.

9. Configure the DDRC_RNKCFG0~3 registers to 0x0000_0142 according to the single chip capacity of the device. The bus address mapping mode is RBC-DW mode, the AP is A10, the column address width is 10, and the row address width is 15.
10. According to the operating frequency and device requirements, configure DDRC_TIMING0, DDRC_TIMING1, DDRC_TIMING3ÿ
11. Configure the storage space base address register DDRC_BASEADDR to 0x8000_0000.
12. According to the actual application, configure DDRC_QOSCFG0 and DDRC_QOSCFG1; DDRC_QOS (DDRC_RDQOS0~DDRC_RDQOS15). For these registers, default configuration values can also be used.
13. Configure DDRC_ODTCFG[wodt0]=0x1, DDRC_ODTCFG[rodt0]=0x0.
14. Configure DDRC_DTRCTRL[train_mode]=0x1, DDRC_DTRCTRL[train_en]=0, use ddrphy read dqs Auto-gated training mode.
15. Configure the DDRC_SREFCTRL register as 0x0 to exit the self-refresh state.
16. Query DRC_STATUS[in_sr] until it is 0 or the software waits for more than 1µs.
17. Configure DDRC_INITCTRL register (address: 0x008) to 0x1 to start SDRAM initialization operation.
18. The software waits for a period of time (500ns), and queries DDRC_STATUS[in_init] (address: 0x0) until 1ÿ
19. According to the working frequency, configure DDRC_PHYREG4A[cas latency] (address: 0x838), and configure DDRC_PHYREG4A[additive latency] to 0.
20. Configure the DDRC_PHYREG2 (address: 0x808) register to 0x1 to start the automatic motion training operation.
21. The software waits for a period of time (500ns) and queries DDRC_PHYREG62[phy_cal_done_h] (address: 0xB48) and DDRC_PHYREG62[phy_cal_done_l] until DDRC_PHYREG62[phy_cal_done_h] =0x1 ÿ DDRC_PHYREG62=0x1ÿ
22. Configure DDRC_PHYREG2 (address: 0x808) as 0x0 to disable PHY read dqs training operation.
23. According to the actual working frequency, configure DDRC_TIMING2 [taref] to enable auto refresh.
24. Start the software gating training mode until the gating signal training of reading dqs is completed.

----Finish

After completing the above steps, DDR3 SDRAM can work normally.

4.1.4.5 Low Power Configuration

DDRC supports two low-power modes of DDRn SDRAM: DDRn SDRAM PowerDown mode and DDRn SDRAM self-refresh mode.

Configure DDRC_CONFIG0[pd_en] and DDRC_CONFIG0[pd_prd] as valid values, and DDRC will automatically control DDRn SDRAM to enter a low power consumption state when the system is idle. When DDRC_CONFIG0[pd_en] is configured as 1, DDRC will control DDRn SDRAM to enter low power consumption mode without any access operation in DDRC_CONFIG0[pd_prd] bus clock cycles.

Configure DDRC_SREFCTRL[sr_seq] as valid value, DDRC will control DDRn SDRAM to enter self-refresh mode. When DDRC_SREFCTRL[sr_req] is configured as 1, after DDRC completes the access being executed, it controls DDRn SDRAM to enter the self-refresh mode and no longer responds to the request on the bus.

4.1.4.6 DDR IO impedance configuration

In the application scenario of DDRn SDRAM, DDRC has the function of automatically calibrating the sending impedance and receiving impedance of DDR IO.

The default configuration is to enable the auto-calibration function. You can also configure DDRC_PHY_REG11, DDRC_PHY_REG12ÿDDRC_PHY_REG16ÿDDRC_PHY_REG18ÿ DDRC_PHY_REG22ÿDDRC_PHY_REG24ÿDDRC_PHY_REG25ÿ DDRC_PHY_REG27, DDRC_PHY_REG28 These registers are set manually.

4.1.5 Register overview

The value range and meaning of variables in the register offset address of DDRC are shown in Table 4-5 .

Table 4-5 Register offset address variable table of DDRC

variable name	Ranges	describe
white	0ÿ1	Number of ByteLanes supported by DDRC.
dq_hf	0ÿ7	The number of registers for DQ bit delay adjustment, the maximum is 1/2 of the DQ bit width.
id0s	0ÿ15	DDRC supports the number of priority configuration registers.
ports	0ÿ4	Number of AXI ports.

An overview of the DDRC registers is shown in Table 4-6 .

Table 4-6 DDRC register overview (base address is 0x2011_0000)

offset address name		describe	page number
0x000	DDRC_STATUS	DDRC Status Register	4-14
0x004	DDRC_SREFCTRL	DDRC self-refresh control register	4-15
0x008	DDRC_INITCTRL	DDRC initialization control register	4-16
0x010	DDRC_CTRL	DDRC Control Register	4-16
0x014	DDRC_EMRS01	Mode configuration register for DDR	4-17
0x018	DDRC_EMRS23	Extended Mode Configuration Register for DDR	4-17
0x01C	DDRC_CONFIG0	Configure register 0 of DDRC function	4-18
0x020	DDRC_CONFIG1	Register 1 for configuring the DDRC function	4-20

offset address name		describe	page number
0x024	DDRC_CMDCFG	DDRC Command Configuration Register	4-23
0x028	DDRC_CMDEXE	DDRC Software Configuration Command Start Register	4-23
0x02C	DDRC_RNKCFG	Registers to configure DDR features	4-24
0x040	DDRC_BASEADDR	DDR space base address configuration register	4-25
0x050	DDRC_TIMING0	DDR Timing Parameter Register 0	4-26
0x054	DDRC_TIMING1	DDR Timing Parameter Register 1	4-27
0x058	DDRC_TIMING2	DDR Timing Parameter Register 2	4-28
0x05C	DDRC_TIMING3	DDR Timing Parameter Register 3	4-29
0x0AC	DDRC_DTRCTRL	DDRC Gating Training Control Register	4-30
0x0F0	DDRC_AXISTATUS	DDRC interface status register	4-31
0x0F4	DDRC_ODTCFG	DDR ODT Feature Configuration Register 4-32	
0x100	DDRC_QOSCFG0	DDRC QoS algorithm configuration register 0	4-33
0x104	DDRC_QOSCFG1	DDRC QoS algorithm configuration register 1	4-34
0x150+0x4 x id0s	DDRC_QOS	DDRC Command Priority Configuration Register 4-35	
0x200+0x4 x ports	DDRC_FLUX	DDRC AXI Port Bandwidth Flow Control Configuration Register	4-36
0x240	DDRC_TEST0	DDRC Test Status Register	4-37
0x260	DDRC_TEST7	DDRC performance statistics control register	4-38
0x264	DDRC_TEST8	DDRC write command statistics register	4-39
0x268	DDRC_TEST9	DDRC read command statistics register	4-39
0x26C	DDRC_TEST10	DDRC DMC command waiting number statistics register	4-39
0x280	DDRC_TEST12	DDRC Test Status Register	4-40
0x400	DDRC_PHYSRST	DDRPHY soft reset control signal	4-40
0x404	DDRC_PHYSTATUS	DDRPHY status register	4-41
0x408	DDRC_PHYCTRL	DDRPHY Control Register	4-41
0x800	DDRC_PHY_REG1	DDRPHY register 1	4-42
0x808	DDRC_PHY_REG2	DDRPHY register 2	4-43
0x804	DDRC_PHY_REG3	DDRPHY register 3	4-43

offset address	name	describe	page number
0x824	DDRC_PHY_REG4	DDRPHY register 4	4-44
0x838	DDRC_PHY_REG4A	DDRPHY Register 4A	4-45
0x83C	DDRC_PHY_REG4B	DDRPHY Register 4B	4-46
0x8D4	DDRC_PHY_REG6	DDRPHY register 6	4-46
0x8D8	DDRC_PHY_REG7	DDRPHY register 7	4-47
0x8E0	DDRC_PHY_REG8	DDRPHY Register 8	4-48
0x914	DDRC_PHY_REG9	DDRPHY Register 9	4-50
0x918	DDRC_PHY_REG10	DDRPHY register 10	4-50
0x920	DDRC_PHY_REG11	DDRPHY Register 11	4-51
0x840	DDRC_PHY_REG12	DDRPHY Register 12	4-53
0x844	DDRC_PHY_REG13	DDRPHY Register 13	4-53
0x848	DDRC_PHY_REG14	DDRPHY Register 14	4-53
0x84C	DDRC_PHY_REG15	DDRPHY Register 15	4-55
0x854	DDRC_PHY_REG16	DDRPHY Register 16	4-56
0x858	DDRC_PHY_REG17	DDRPHY Register 17	4-56
0x85C	DDRC_PHY_REG18	DDRPHY Register 18	4-56
0x860	DDRC_PHY_REG19	DDRPHY Register 19	4-58
0x864	DDRC_PHY_REG20	DDRPHY Register 20	4-59
0x868	DDRC_PHY_REG21	DDRPHY Register 21	4-59
0x870	DDRC_PHY_REG22	DDRPHY Register 22	4-60
0x874	DDRC_PHY_REG23	DDRPHY Register 23	4-61
0x878	DDRC_PHY_REG24	DDRPHY Register 24	4-61
0x880	DDRC_PHY_REG25	DDRPHY Register 25	4-62
0x884	DDRC_PHY_REG26	DDRPHY Register 26	4-62
0x888	DDRC_PHY_REG27	DDRPHY Register 27	4-63
0x88C	DDRC_PHY_REG28	DDRPHY Register 28	4-63
0x9C0	DDRC_PHY_REG29	DDRPHY Register 29	4-64
0xAC4	DDRC_PHY_REG30	DDRPHY Register 30	4-65
0xAC8	DDRC_PHY_REG31	DDRPHY Register 31	4-66

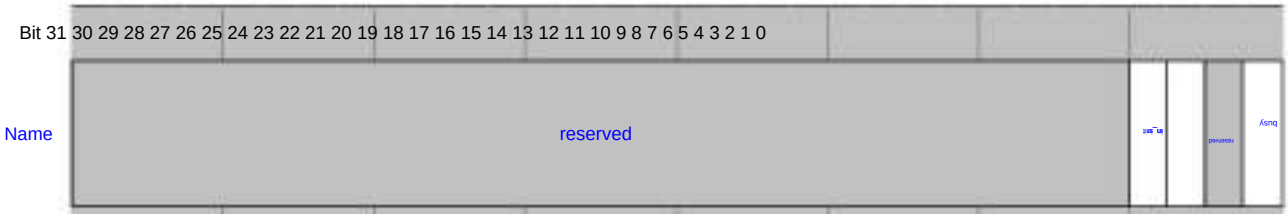
offset address	name	describe	page number
0xACC	DDRC_PHY_REG32	DDRPHY Register 32	4-66
0xAD0	DDRC_PHY_REG33	DDRPHY Register 33	4-67
0xAD4	DDRC_PHY_REG34	DDRPHY Register 34	4-67
0xAD8	DDRC_PHY_REG35	DDRPHY Register 35	4-68
0xADC	DDRC_PHY_REG36	DDRPHY Register 36	4-68
0xAE0	DDRC_PHY_REG37	DDRPHY Register 37	4-69
0xAE4	DDRC_PHY_REG38	DDRPHY Register 38	4-69
0xAE8	DDRC_PHY_REG39	DDRPHY Register 39	4-70
0xAEC	DDRC_PHY_REG40	DDRPHY Register 40	4-70
0xAF0	DDRC_PHY_REG41	DDRPHY Register 41	4-71
0xAF4	DDRC_PHY_REG42	DDRPHY Register 42	4-71
0xAF8	DDRC_PHY_REG43	DDRPHY Register 43	4-72
0xAFC+0x4 x dq_hf	DDRC_PHY_TXDQSKE IN	DDRPHY register	4-72
0xB1C	DDRC_PHY_REG52	DDRPHY Register 52	4-73
0xB20	DDRC_PHY_REG53	DDRPHY Register 53	4-74
0xB24	DDRC_PHY_REG54	DDRPHY Register 54	4-74
0xB28	DDRC_PHY_REG55	DDRPHY Register 55	4-74
0xB2C+0x4 x dq_hf	DDRC_PHY_RXDQSK THAT ONE	DDRPHY register	4-75
0xB4C	DDRC_PHY_REG5E	DDRPHY register 5E	4-76
0xBE0+0x4 *white	DDRC_PHY_REG60	DDRPHY register 60	4-76
0xBE8	DDRC_PHY_REG61	DDRPHY Register 61	4-77
0xBC4	DDRC_PHY_REG62	DDRPHY Register 62	4-77

4.1.6 Register description

DDRC_STATUS

DDRC_STATUS is the DDRC status register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_STATUS	0x0000_0005

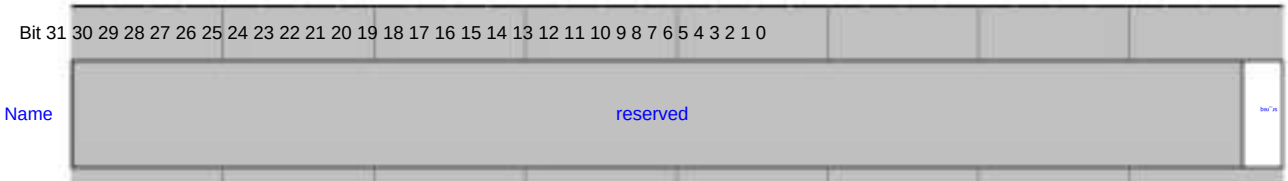


Bits	Access Name		Description
[31:4]	RO	Reserved	reserve.
[3]	RO	in_init	Controller initialization state. 0: normal state; 1: initialization state.
[2]	RO	in_sr	Controller self-refresh status. 0: normal state; 1: Self-refresh state.
[1]	RO	Reserved	reserve.
[0]	RO	busy	Controller busy status register. 0: idle; 1: Command processing.

DDRC_SREFCTRL

DDRC_SREFCTRL is the DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x004	DDRC_SREFCTRL	0x0000_0001



Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	sr_req	SDRAM self-refresh request. 0: Exit the self-refresh state; 1: Enter self-refresh state.

DDRC_INITCTRL

DDRC_INITCTRL is the initialization control register for DDRC.

Offset Address	Register Name	Total Reset Value
0x008	DDRC_INITCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	init_req	Initialization starts. 0: Completed initialization or in normal working state; 1: Start SDRAM initialization operation.

DDRC_CTRL

DDRC_CTRL is the DDRC control register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	Reserved	reserve.
[0]	RW	ddr_rst_n	DDR3 SDRAM reset. 0: reset is valid; 1: Reset is invalid. Note: Only valid for DDR3 SDRAM, the default configuration is 0.

DDRC_EMRS01

DDRC_EMRS01 is the mode configuration register of DDR.

Offset Address	Register Name	Total Reset Value
0x014	DDRC_EMRS01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	emrs1	mrs
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDRn SDRAM Extended Mode Register 1. Corresponds to Mode Register 1 (MR1) [15:0] in DDRn SDRAM manual. Among them, MR1[15:14] of most DDR devices is not used, and [31:30] of DDRC_EMRS01 is reserved and set to 0b00. **Note:** **For the specific explanation of MR1 ,** please refer to the manual of **the DDRn SDRAM** used .
[15:0]	RW	mrs	DDRn SDRAM mode register. Corresponds to Mode Register 0 (MR0) [15:0] in DDRn SDRAM manual. Among them, MR0[15:14] of most DDR devices is not used, then DDRC_EMRS01 [15:14] is reserved and set to 0b00. **Note: For the specific explanation of MR0 ,** please refer to the manual of **the DDRn SDRAM** used .

DDRC_EMRS23

DDRC_EMRS23 is the extended mode configuration register of DDR.

Offset Address	Register Name	Total Reset Value
0x018	DDRC_EMRS23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	emrs3	emrs2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

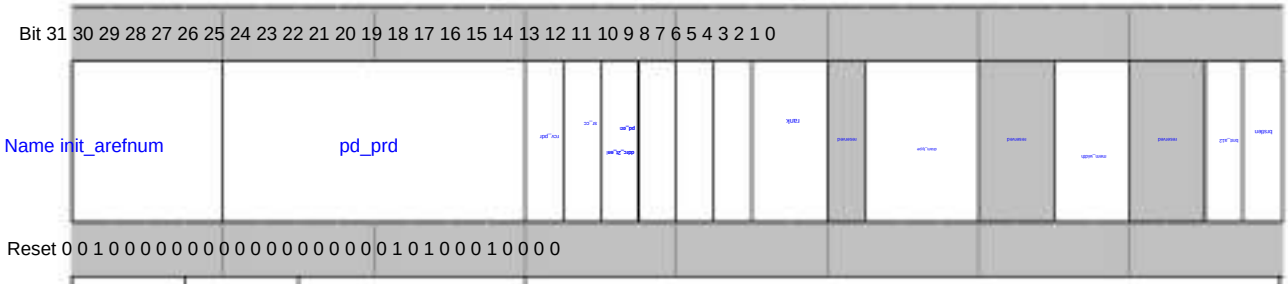
Bits	Access	Name	Description
[31:16]	RW	emrs3	DDRn SDRAM Extended Mode Register 3. Corresponds to Mode Register 3 (MR3) [15:0] in DDRn SDRAM manual. Among them, MR3[15:14] of most DDR devices is not used, and DDRC_EMRS23 [31:30] is reserved and set to 0b00. **Note:** **For the specific explanation of MR3 ,** please refer to the manual of **the DDRn SDRAM** used .

[15:0]	RW	emrs2	DDRn SDRAM Extended Mode Register 2. Corresponds to Mode Register 2 (MR2) [15::0] in DDRn SDRAM manual. Among them, MR2[15:14] of most DDR devices is not used, and DDRC_EMRS23 [15:14] is reserved and set to 0b00. **Note: For the specific explanation of MR2 ,** please refer to the manual of **the DDRn SDRAM** used .

DDRC_CONFIG0

DDRC_CONFIG0 is register 0 for configuring DDRC function.

Offset Address	Register Name	Total Reset Value
0x01C	DDRC_CONFIG0	0x2000_0510



Bits	Access	Name	Description
[31:28]	RW	init_arefnum	Number of auto-refresh operations issued during DDRn SDRAM initialization. 0x0ÿ0x2: 2 times; 0x3~0xF: n times.
[27:20]	RW	pd_prd	SDRAM low power consumption (Power Down) cycle configuration. When DDRC does not receive a command in consecutive pd_prd cycles, it controls SDRAM to enter a low power consumption state, and when a new command arrives, it controls SDRAM to exit a low power consumption state. 0x00: 1 clock cycle; 0x01~0xFF: n clock cycles. Note: This parameter is only valid when **pd_en** is **1 ;** the clock cycle is **the DDRC** bus clock cycle.
[19]	RW	rcv_pdr	DDR receive IO dynamic Power Down control enable. When enabled, DDRC will turn off the receive buffer of DDR data IO in the non-read state. 0: forbidden; 1: enable.
[18]	RW	sr_cc	Self-refresh mode, SDRAM clock control. 0: Do not turn off the SDRAM clock; 1: Disable SDRAM clock.

[17] RW pd_cc			Low power mode (PowerDown), SDRAM clock control. 0: Do not turn off the SDRAM clock; 1: Disable SDRAM clock. Note: This parameter is only valid when the external DDR is LPDDR/LPDDR2 SDRAM.
[16] RW pd_en			SDRAM automatic low power enable. 0: forbidden; 1: enable.
[15] RW ddrc_2t_sel			2t timing mode selection. 0: On the DDR interface, the CS_N signal is valid for one cycle, RAS_N, CAS_N and WE_N are valid for two cycles, and the address is valid for two cycles; 1: On the DDR interface, the CS_N signal is always active low, and RAS_N, CAS_N and WE_N are valid for one cycle , the address is valid for two cycles.
[14] RW ddrc_2t_en			2t timing enable control. 0: forbidden; 1: enable.
[13:12] RW rank			Controller Rank configuration. 00: 1 rank; 01: 2 ranks; 10: 3 ranks; 11: 4 ranks.
[11] RO		reserved	reserve.
[10:8] RW dram_type			External memory type. 101ÿDDR2ÿ 110ÿDDR3ÿ Others: reserved.
[7:6] RO		reserved	reserve.
[5:4] RW mem_width			Store data bus width. 00ÿ16bitÿ 01ÿ32bitÿ Others: reserved.
[3:2] RO		reserved	reserve.

[1] RW	brst_a12		DDR3 SDRAM A12 command enable. 0: disable A12 function bit; 1: Enable A12 function bit. Note: The recommended configuration is 0.
[0] RW	brushes		Controller Burst Length configuration. 0ÿBL4ÿ 1ÿBL8ÿ When the frequency ratio of DDRC to PHY is 1:1, DDR2 can be configured as Burst4 and Burst8, and DDR3 can only be configured as Burst8 mode; when the frequency ratio of DDRC to PHY is 1:2, both DDR2 and DDR3 can only be configured as Burst4 mode.

DDRC_CONFIG1

DDRC_CONFIG1 is register 1 for configuring DDRC function.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CONFIG1	0x0000_A380

Bits	Access	Name	Description
[31:28]	RW	sref_arefnum	DDRn SDRAM In the DFS process, the number of auto-refresh operations issued after exiting self-refresh. 0x0~0x1: Send 1 Auto Refresh operation; 0x2~0xF: Send n Auto Refresh operations. Note: Valid when **train_en=1 .** When **train_en=0 ,** self-refresh will be exited directly, and no **Auto Refresh** operation will be sent.
[27:23]	RO	reserved	reserve.
[22]	RW	sref_zqc_en	ZQ Calibration Long is enabled when DDR exits self-refresh. 0: forbidden; 1: enable. Note: Valid for **DDR3** and **LPDDR2** modes. If **the DDR** is in the self-refresh state for a long time, it needs to be configured as 1.

[21] RO		reserved	reserve.
[20] RW clk_switch			DDRC Low Power Clock Switching Control. Whether DDRC enters the low power consumption state (DDR Self Refresh) and backpressures the AXI interface command. 0: No back pressure command, directly return ERROR corresponding; 1: Back pressure interface command, after the clock switching is completed, continue to execute the original command.
[19:18] RO		reserved	reserve.
[17] RW odis_ddrio			Output shutdown configuration for DDR command and data IO. 0: Do not turn off the pin output; 1: Disable pin output. Note: This configuration is a static configuration. It is recommended that after configuring **DDR** to enter **self_refresh ,** it can be configured as 1 to turn off the output of **DDR** command and data **IO .** Before configuring **DDR** to exit **self_refresh ,** configure it as 0 to enable the output of **DDR** commands and data **IO .**
[16] RW pd_ac			Low power mode (PowerDown), SDRAM address command dynamic shutdown control. 0: Do not turn off the pin output; 1: Disable pin output. Note: It is valid when **pd_en** is enabled, and the control pins do not include **CKE, ODT, CSN** and **RESET_N.**
[15:14] RW pd_pst_opn			Before exiting the low power consumption mode (PowerDown), the SDRAM address command pin is turned on in advance. 00: advance 0 clock cycle; 01: advance 1 clock cycle; 10: 2 clock cycles ahead; 11: 3 clock cycles ahead. Note: It is valid when **pd_en** is enabled, and the control pins do not include **CKE** and RESET_N; this clock cycle is **the DDR SDRAMn** working clock cycle.
[13:12] RW pd_pre_cls			SDRAM address command shutdown delay after entering low power consumption mode (PowerDown). 00: delay 0 clock cycle; 01: delay 1 clock cycle; 10: delay 2 clock cycles; 11: Delayed by 3 clock cycles. Note: It is valid when **pd_en** is enabled, and the control pins do not include **CKE** and RESET_N; this clock cycle is **the DDR SDRAMn** working clock cycle.
[11] RO		reserved	reserve.

[10] RW auto_pre_en	The Auto Precharge function is enabled. 0: forbidden; 1: enable.
[9] RW wr_rcv_mode	DDRC AXI port write command receive mode selection. 0: write command direct receiving mode; 1: write command needs to wait for the corresponding write data to arrive before being received.
[8] RW exclu_en	Exclusive commands are enabled. 0: forbidden; 1: enable.
[7] RW lock_en	WRAP command lock enable. 0: forbidden; 1: enable.
[6] RW aref_mode	Auto refresh mode selection. 0: Perform 1 auto-refresh operation every 1 tREFI cycle; 1: Perform 8 auto-refresh operations every 9 tREFI cycles.
[5] RW wrlvl_en	DDR3 WriteLVL hardware automatic control enable. 0: forbidden; 1: enable.
[4] RW reserved	reserve. Must be configured as 0.
[3] RW read_mode	Controller read mode selection. 0: Read along with the road mode; 1: Delayed read mode. The read-associated mode means that the controller completes data sampling according to the data valid signal sent by the PHY. Delayed read mode refers to the internal delay of the controller to wait for the completion of sampling the data sent by the PHY. Note: This value must be configured as **0** when **DDRC_DTRCTRL[train_mode] is** configured as 0.
[2] RW clkratio	Controller working mode. When the frequency ratio of DDRC and PHY is 1:1, configure it as 0; when the frequency ratio of DDRC and PHY is 1:2, configure it as 1.
[1] RW ecc_en	Controller ECC enabled. 0: forbidden; 1: enable.

[0] RW zqc_en			DDR3 SDRAM ZQ enable. 0: forbidden; 1: enable. Note: Only valid for **DDR3 SDRAM ,** the default configuration is 0.

DDRC_CMDCFG

DDRC_CMDCFG is the DDRC command configuration register.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CMDCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_mrs																cmd_ba								cmd_rank							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cmd_mrs	When configuring the LMR command, the DDR mode register configures the value.
[15:8]	RW	cmd_ba	DDR BA configuration value when configuring LMR command.
[7:4]	RW	cmd_rank	Rank of the executed command. 0: Execute the configuration command; 1: Do not execute configuration commands. Each bit corresponds to a storage Rank control. **Note: Hi3520D** only has **rank0, cmd_rank** can only be configured as **0x0** or **0x1.**
[3:2]	RO	reserved	reserve.
[1:0]	RW	cmd_type	DDR command configuration. 00: Enter Deep Power Down; 01: Exit Deep Power Down; 10: Load Mode Reigser (LMR) command; 11ÿZQCLÿ

DDRC_CMDEXE

DDRC_CMDEXE is the DDRC software configuration command enable register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CMDEXE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	cmd_req	The controller configuration command executes the request. 0: Do not execute the command or automatically clear the parameter to zero when the command is executed; 1: Request to execute the command.

DDRC_RNKCFG

DDRC_RNKCFG is a register for configuring DDR features.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_RNKCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:14]	RO	reserved	reserve.
[13:12]	RW	mem_map	SDRAM address decoding mode. 00ÿ{Rank,Row,Ba,Col,DW}= AXI_Addressÿ 01: {Rank, Ba, Row, Col, DW} = AXI_Address; Others: reserved.
[11:9]	RO	reserved	reserve.

[8] RW	mem_bank		Single chip SDRAM Bank number. 0ÿ4 Bankÿ 1ÿ8 Bankÿ When there are multiple ranks, different configurations are supported for each rank in the same channel. But in dual-channel mode, both channels must use the same configuration.
[7]	RO	reserved	reserve.
[6:4] RW	mem_row		Single-chip SDRAM row address bit width configuration. 000ÿ11 bitÿ 001ÿ12 bitÿ 010ÿ13 bitÿ 011ÿ14 bitÿ 100ÿ15 bitÿ 101ÿ16 bitÿ Others: reserved.
[3]	RO	reserved	reserve.
[2:0] RW	mem_col		Single-chip SDRAM column address bit width configuration. 000ÿ8 bitÿ 001ÿ9 bitÿ 010ÿ10 bitÿ 011ÿ11 bitÿ 100ÿ12 bitÿ Others: reserved.

DDRC_BASEADDR

DDRC_BASEADDR is the DDR space base address configuration register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_BASEADDR	0x0000_0000

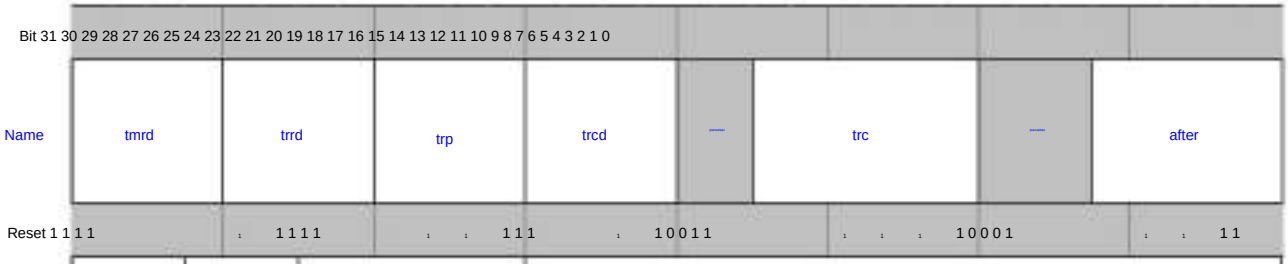
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mem_base_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mem_base_addr	The starting base address configuration of DDR memory space in the whole chip system.

DDRC_TIMING0

DDRC_TIMING0 is DDR timing parameter register 0.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_TIMING0	0xFFFF_3F1F



Bits	Access Name	Description
[31:28]	RW tmrd	Wait period for the Load Mode Register (LMR) command. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[27:24]	RW trrd	Waiting period from opening BANK A to opening BANK B (ACT bank a to ACT bank b). 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[23:20]	RW trp	The wait period for the shutdown (PRE period) command. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[19:16]	RW trcd	Same as BANK activation to read or write (ACT to READ or WRITE) command wait period. 0x0~0x3: 3 clock cycles; 0x4~0xF: n clock cycle.
[15:14]	RO reserved	reserve.
[13:8]	RW trc	It is the same as the wait period from active command to active command (active a bank to active a bank) of BANK. 0x00~0x01: 1 clock cycle; 0x02~0x3F: n clock cycles.
[7:5]	RO reserved	reserve.
[4:0]	RW tras	It is the same as the wait period from BANK activation command to close command (ACT to PRE). 0x00~0x01: 1 clock cycle; 0x02~0x0F: n clock cycles.

DDRC_TIMING1

DDRC_TIMING1 is DDR timing parameter register 1.

Offset Address	Register Name	Total Reset Value
0x054	DDRC_TIMING1	0xFF01_45FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								tired				trtw				twl				tcl				trfc							
Reset	1	1	1	1					1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Exit the wait cycle from Self-Refresh to Read Command. 0x0: 1 clock cycle; 0x01 ÿ0xFF: nx2 clock cycles. For DDR3 SDRAM, this value configures the tXSDLL value.
[23:20]	RW	trdlat	DDRPHY inherent latency. 0x0~0xF: n+1 cycles. When using Dolphin PHY, it is configured as 0x5. Valid when read_mode=1 (delayed read mode).
[19:16]	RW	trtw	Latency from last read data to first write data. 0x0~0x1: 1 clock cycle; 0x2~0xF: n+1 clock cycle.
[15:12]	RW	stupid	Wait period from write command to write data. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles. For example: 0x3: 3 clock cycles. **Note: In DDR2 mode, twl** is configured as **tcl-1, and twl –taond** ÿ 1 should be satisfied when twl is configured . The time parameter is calculated according to **the ddr sram** clock cycle.
[11:8]	RW	tcl	DDR read command to read data delay (CAS Latency). 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles. Note: This time parameter is calculated according to **ddr sram** clock cycle.
[7:0]	RW	trfc	Auto refresh command period and auto refresh to active (AREF period or AREF to ACT) command wait period. This register selects a large value for configuration max{trfc,tzqcs}. 0x00~0x01: 1 clock cycle; 0x02~0xFF: n clock cycles.

DDRC_TIMING2

DDRC_TIMING2 is DDR timing parameter register 2.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_TIMING2	0xF3F3_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				twr				—				wow				—				tariff							
Reset	1	1	1	1	0	0	1	1	1				1	0	0	1					1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	The minimum time to maintain a low power state. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles. This value needs to configure the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE. When using Dophin's DDRPHY, the value of this register is configured as max{tCKSRx,tCKE}+3.
[27:24]	RW	twtr	The wait cycle for the last write data to read command (write to read) of the write operation. 0x0~0x1: 1 clock cycle; 0x2~0xf: n clock cycles. Such as 0x3: 3 clock cycles.
[23:20]	RW	tower	Write recovery wait period. 0x0~0x1: 1 clock cycle; 0x2~0xf: n clock cycles. Note: When **DFS** is required, the tWR parameter needs to be configured according to the highest possible frequency of the chip in **DFS .** And the configuration of **tWR** cannot be modified with the frequency change of **DDR .**
[19:18]	RO	reserved	reserve.
[17:12]	RW	tfaw	4 consecutive active command cycles. 0x00~0x3F: n clock cycles; such as 0x14: 20 clock cycles.
[11]	RO	reserved	reserve.

[10:0] RW	taref		Automatic refresh cycle. 0x000: Automatic refresh disabled; 0x001~0x7FF: SDRAM refresh cycle time is 16xn clock cycles. Such as 0x008: 128 clock cycles (16x8). The configuration interval time is (tREFI = 7800ns)/16/tclk. Tclk is twice the operating cycle when SDRAM is used. When DDRC_CONFIG1[aref_mode]=1, this register needs to be configured with an interval time of 8 x tREFI.

DDRC_TIMING3

DDRC_TIMING3 is DDR timing parameter register 3.

Offset Address	Register Name	Total Reset Value
0x05C	DDRC_TIMING3	0xFFDF_F0F2

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tzq_prd	tzzinit	year	bad	trtp
Reset	1111	1111	1011	1111	0000 1110 0010

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	ZQCS command cycle. 0x000: ZQCS command disabled; 0x001ÿ0x3FF: nx128 AREF cycles. ZQCS command cycle time is nx128 taref clock cycles.
[21:12]	RW	tzqinit	ZQ initialization delay period. 0x0~0x1ff: n+1 clock cycles. This value configures the maximum value of tZQINIT, tDLLK.
[11:8]	RW	taond	ODT (On-die termination) open and close cycle. In DDR2 mode (taond/taofd): 0x0ÿ2/2.5ÿ 0x1ÿ3/3.5ÿ 0x2ÿ4/4.5ÿ 0x3ÿ5/5.5ÿ Others: reserved. In DDR3 mode, this value is configured as tWL-1. Note: This time parameter is calculated according to **ddr sram** clock cycle.

[7:4] RW xard			Exit DDR low-power state wait cycle. 0x0ÿ 0xF: n clock cycles, n represents a decimal number; eg: 0x7: 7 clock cycles. Take the maximum value among {tXP,tXARD,tXARDS,tXS}. In DDR3 mode, when this register is configured as tXS, txard only needs to be configured as an equivalent clock cycle of 10ns.
[3:0] RW trtp			Wait delay from read command to close command. 000~010: 2 clock cycles; 011~111: n clock cycles. The calculation formula of Trtp is AL+BL/2+Max(trtp,2)-2

DDRC_DTRCTRL

DDRC_DTRCTRL is the DDRC gate training control register.

Offset Address	Register Name	Total Reset Value
0x0AC	DDRC_DTRCTRL	0x0000_0401

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dt_byte								reserved								reserved				rinse			train_mode	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:24]	RW	dt_byte	Byte training enabled. 0: disable byte training; 1: Enable byte training. bit[31]~bit[24]: corresponding to DDRC Byte7~DDRC Byte0 training enable in sequence.
[23:16]	RO	reserved	reserve.
[15:12]	RO	reserved	reserve.
[11:9]	RW	rinse	Read enable latency period. 000~011: n clock cycles. Others: reserved.
[8]	RW	train_mode	Gated training method selection. 0: other training methods; 1: Normal training method.

[7:4] RO		reserved	reserve.
[3]	RO	reserved	reserve.
[2] RW track_en			Gated position auto-update enabled. 0: forbidden; 1: enable Note: There must be a set of read operations between two **train** operations, and the continuous access length is greater than **DDRBURST8.**
[1] RW train_en			Gated position training enabled. 0: disable; 1: enable;
[0]	RO	reserved	reserve.

DDRC_AXISTATUS

DDRC_AXISTATUS is the DDRC interface status register.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_AXISTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7]	RO	axi_st7	Controller bus interface 7 status. 0: idle; 1: There is a command to execute.
[6]	RO	axis_st6	Controller bus interface 6 status. 0: idle; 1: There is a command to execute.
[5]	RO	axi_st5	Controller bus interface 5 status. 0: idle; 1: There is a command to execute.

[4]	RO	axi_st4	Controller bus interface 4 status. 0: idle; 1: There is a command to execute.
[3]	RO	axi_st3	Controller bus interface 3 status. 0: idle; 1: There is a command to execute.
[2]	RO	axi_st2	Controller bus interface 2 status. 0: idle; 1: There is a command to execute.
[1]	RO	axi_st1	Controller bus interface 1 status. 0: idle; 1: There is a command to execute.
[0]	RO	axis_st0	Controller bus interface 0 status. 0: idle; 1: command execution.

DDRC_ODTCFG

DDRC_ODTCFG is the ODT feature configuration register for DDR.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_ODTCFG	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved rodt0 reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RW	reserved	reserve. Must be configured as 0.
[16]	RW	rodt0	Rank0 reads ODT configuration. 0: disable reading ODT; 1: Enable read ODT.
[15:1]	RW	reserved	reserve. Must be configured as 0.

[0] RW wodt0			Rank0 writes ODT configuration. 0: prohibit writing ODT; 1: Enable write ODT.

DDRC_QOSCFG0

DDRC_QOSCFG0 is the QoS algorithm configuration register 0 of DDRC.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_QOSCFG0	0x0000_000F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved — dmc_fifo_lvl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	idmap_mode	ID mapping mode: 0: Use the id_map mapping method configured by the register (default); 1: Use the AXI interface to configure the Qos mapping mode along with the read and write commands (only when the macro definition of this mode is enabled in the RTL code). Note: It must be configured as 1, that is, the channel-associated configuration **Qos** mapping mode is used.
[5]	RW	id_order_ctl	Enable out-of-order execution for the specified ID. 0: forbidden; 1: enable. The controller does not guarantee the order in which the address (DDR line address) conflict occurs between the read and write commands of the specified ID and the commands of other IDs. Data consistency is guaranteed by Master.
[4]	RW	order_en	Commands with the same priority are executed in sequence. 0: forbidden; 1: enable.
[3:0]	RW	dmc_fifo_lvl	In DMC, the depth of the command register FIFO. 0x0~0xF: n+1 command depth. **Note:** The maximum configuration of Hi3520D is 0xB, and the recommended configuration is **0x7.**

DDRC_QOSCFG1

DDRC_QOSCFG1 is the QoS algorithm configuration register 1 of DDRC.

Offset Address	Register Name	Total Reset Value
0x104	DDRC_QOSCFG1	0x3210_3210

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	id_map_rd	id_map_wr
Reset	0 0 1 1 0 0 1 0 0 0 0 1 0 0 0 0	0 0 1 1 0 0 1 0 0 0 0 1 0 0 0 0

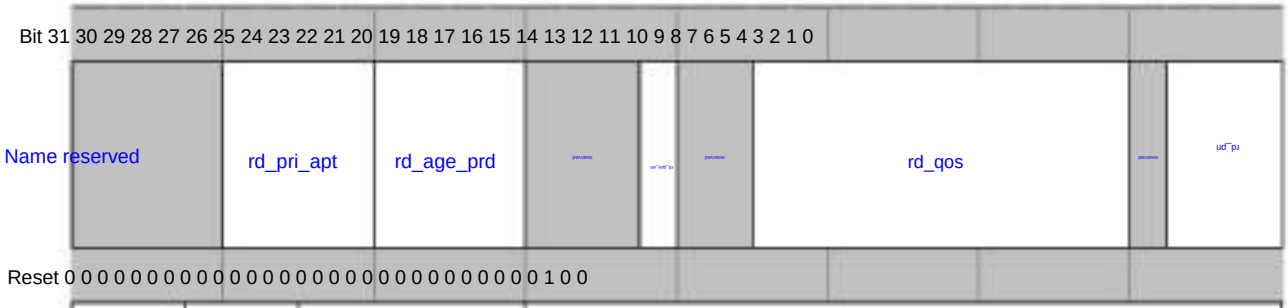
Bits	Access	Name	Description
[31:16]	RW	id_map_rd	For the read command, select 4 bits according to the read ID from the bus for QOS configuration selection: bit[15:12]: bit[3] for configuration ID mapping; bit[11:8]: bit[2] for configuration ID mapping ; bit[7:4]: bit[1] of configuration ID mapping; bit[3:0]: bit[0] of configuration ID mapping. For example: ID_MAP is configured as 0x5320, which indicates {ID[5], ID[3], ID[2], ID[0]} of the bus ID are used for ID mapping to complete the priority DDRC will insert a 3-bit ID into the 9th, 8th and 7th bits of the original 13-bit ID to represent the AXI port number, so the ID bit width mapped by DDRC is 16 bits in total. 000ÿaxi port 0ÿ 001ÿaxi port 1ÿ 010ÿ axi port 2ÿ 011ÿaxi port 3ÿ 100ÿaxi port 4ÿ 101ÿaxi port 5ÿ 110ÿaxi port 6ÿ 111ÿaxi port 7ÿ

[15:0] RW	id_map_wr		For the write command, select 4 bits for QOS configuration selection according to the write ID from the bus. bit[15:12]: bit[3] of configuration ID mapping; bit[11:8]: bit[2] of configuration ID mapping; bit[7:4]: bit[1] of configuration ID mapping; bit[3:0]: bit[0] of configuration ID mapping. For example: ID_MAP is configured as 0x5320, which indicates {ID[5], ID[3], ID[2], ID[0]} of the bus ID are used for ID mapping to complete the priority configuration. DDRC will insert a 3-bit ID into the 9th, 8th and 7th bits of the original 13-bit ID to represent the AXI port number, so the ID bit width mapped by DDRC is 16 bits in total. 000ÿaxi port 0ÿ 001ÿaxi port 1ÿ 010ÿaxi port 2ÿ 011ÿaxi port 3ÿ 100ÿaxi port 4ÿ 101ÿaxi port 5ÿ 110ÿaxi port 6ÿ 111ÿaxi port 7ÿ

DDRC_QOS

DDRC_QOS is the command priority configuration register of DDRC.

Offset Address	Register Name	Total Reset Value
0x150+0x4 x id0 id0s(0ÿ15)	DDRC_QOS	0x0000_0004



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	pri_apt	Command priority adaptive configuration. 0x0: disable the priority adaptive function; 0x1~0xF: Nx16 clock cycles.

[23:20] RW	age_prd		Command aging time configuration. 0x0: Aging function disabled; 0x1~0xF: Nx16 clock cycles.
[19:17] RO		reserved	reserve.
[16] RW	qos_en		Command QOS enable (timeout). 0: forbidden; 1: enable.
[15:14] RO		reserved	reserve.
[13:4] RW	qos		Command QoS configuration (timeout). 0x1ÿ0x3FF: n clock cycles; others: reserved. Note: The actual **timeout** value used is an integer multiple of **16 ,** and the lower **4** bits of **rd_qos** will be ignored .
[3]	RO	reserved	reserve.
[2:0] RW	pri		Command priority configuration. 000: highest priority; 001: second highest priority; …… 111: Lowest priority.

DDRC_FLUX

DDRC_FLUX is the bandwidth flow control configuration register for DDRC AXI port.

Offset Address	Register Name	Total Reset Value
0x200+0x4 x ports ports(0ÿ4)	DDRC_FLUX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flux_lvl / flux
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.

[21] RW	flux_port_en		AXI interface DDRC traffic statistics enable. 0: disable flow control function; 1: Flow control enabled.
[20] RW	flux_ovfl		AXI interface flow overflow is enabled. 0: disable; 1: enable. When configured as 1, when the AXI port traffic exceeds the bandwidth limit, and there is no AXI port without traffic overflow, when there is a command request, the bandwidth of this AXI port is allowed to exceed the configured traffic.
[19:17] RO		reserved	reserve.
[16:12] RW	flux_lvl		AXI interface flow overflow allows watermark. 0x0~0x10: DMC waterline depth that allows flow overflow. Others: reserved. When the flow of the AXI port exceeds the configured bandwidth of flux, under the condition of flux_ovfl=1, the number of pending commands in the DMC is less than the configured waterline, and then it is allowed to send. Otherwise no arbitration will be given.
[11:10] RO		reserved	reserve.
[9:0] RW	flux		Allowed bandwidth configuration for the AXI interface. 0x0~0x3FF: The ratio of the maximum DDR bandwidth allowed to be accessed by the AXI interface to the total bandwidth. The total bandwidth is 1024, and the configured value is the proportion of the total bandwidth.

DDRC_TEST0

DDRC_TEST0 is the test status register of DDRC.

Offset Address	Register Name	Total Reset Value
0x240	DDRC_TEST0	0x0000_0000

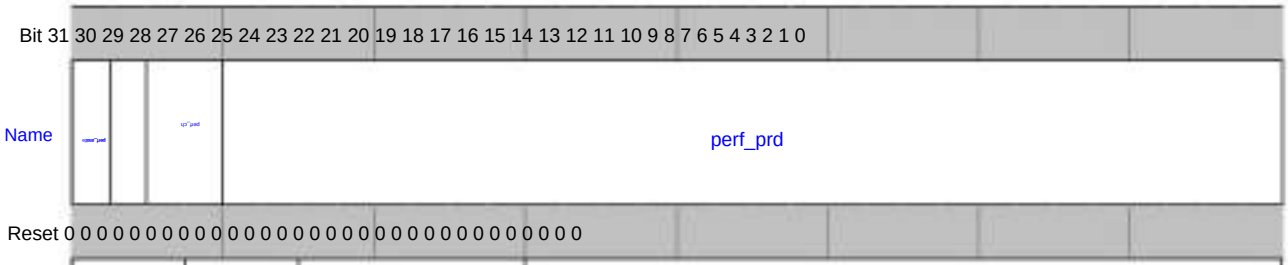
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dmc_ct	dmc_cv
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	Controller command type.
[15:0]	RO	dmc_cv	The command the controller is processing.

DDRC_TEST7

DDRC_TEST7 is the DDRC performance statistics control register.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_TEST7	0x0000_0000



Bits	Access	Name	Description
[31]	RW	perf_mode	performance statistics mode. 0: Continuous trigger mode. Counters related to performance statistics count continuously. It can guarantee that in the continuous statistics mode, the statistics will not overflow within 1s (533MHz). 1: Single trigger mode. After the performance statistics time expires perf_prd, the statistics results will be kept and the statistics will stop. Note: When the statistical value overflows, it will wrap around **WRAP .**
[30]	RW	perf_en	Enable performance statistics. 0: disable; 1: enable. Note: When **perf_mode=0 ,** enabling this bit means that the performance statistics register will start counting in circles. When **perf_mode=1 ,** this bit is automatically cleared after a statistics is completed.
[29:28]	RW	perf_ch	Read and write command statistics channel. 00: forbidden; 01: channel 0; 10: channel 1; 11: all channels. Note: This register limits the number of channels counted by the read and write commands of **DDRC_TEST8** and **DDRC_TEST9 .**
[27:0]	RW	perf_prd	Performance statistics cycle. 0x0~0xFFF_FFFF: Statistics period. The actual statistical cycle is perf_prd*4*tclk (Tclk is the clock cycle of the DDRC bus). Note: This configuration is only valid when **perf_mode=1 .** In the continuous statistics mode of **perf_mode=0 ,** performance statistics related counters will always count.

DDRC_TEST8

DDRC_TEST8 is the DDRC write command statistics register.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_TEST8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RWC wr_num	Count the number of write commands within the time limit. This register is cleared on write. Support Wrap loop count.

DDRC_TEST9

DDRC_TEST9 is the DDRC read command statistics register.

Offset Address	Register Name	Total Reset Value
0x268	DDRC_TEST9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RWC rd_num	Within the statistical time limit, the number of read commands. This register is cleared on write. Support Wrap loop count.

DDRC_TEST10

DDRC_TEST10 is the statistic register for the waiting count of DDRC DMC commands.

Offset Address	Register Name	Total Reset Value
0x26C	DDRC_TEST10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dmc_cmd_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RWC	dmc_cmd_num	Count the number of waiting DMC commands in DDRC within the statistical time limit. This register is cleared on write. Support Wrap loop count. Note: limited by the bit width of the register, in order to ensure that it does not overflow within **1s at 660MHz .** The statistical result displayed in this register is the count value after dividing the real statistical result by **2 .**

DDRC_TEST12

DDRC_TEST12 is the test status register of DDRC.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_TEST12	0x0000_0FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	wfifo_f		wfifo_e
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1	1 1

Bits	Access	Name	Description
[31:16]	RO	wfifo_f	Write FIFO full status.
[15:0]	RO	wfifo_e	Write FIFO empty status. **Note:** In Hi3520D, only **12bit** reset value is **0xFFF.**

DDRC_PHYSRST

DDRC_PHYSRST is the DDRPHY soft reset control signal.

Offset Address	Register Name	Total Reset Value
0x400	DDRC_PHYSRST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	ddrphy_srst	DDRPHY reset control. 0: Reset is valid; 1: Reset is invalid.

DDRC_PHYSTATUS

DDRC_PHYSTATUS is the DDRPHY status register.

Offset Address	Register Name	Total Reset Value
0x404	DDRC_PHYSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	phy_init_done	DDRPHY initialization complete flag. 0: DDRPHY initialization is not completed; 1: DDRPHY initialization is complete.

DDRC_PHYCTRL

DDRC_PHYCTRL is the DDRPHY control register.

Offset Address	Register Name	Total Reset Value
0x408	DDRC_PHYCTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	phy_init_start	DDRPHY initialization request. 0: the request is valid; 1: Invalid request.

DDRC_PHY_REG1

DDRC_PHY_REG1 is DDRPHY register 1.

Offset Address	Register Name	Total Reset Value
0x800	DDRC_PHY_REG1	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:4]	RW	phy_rfifo_en	RX FIFO enable. 01: 8 bits read DQ signal; 11: 16 bits read DQ signal.
[3:0]	-	reserved	Reserved, the initial value is non-zero.

DDRC_PHY_REG2

DDRC_PHY_REG2 is DDRPHY register 2.

Offset Address	Register Name	Total Reset Value
0x808	DDRC_PHY_REG2	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved phy_mem_ty cal_start reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	phy_mem_type	Memory selection. 0ÿDDR3ÿ 1ÿDDR2ÿ
[5:2]	RW	reserved	reserve.
[1]	RW	cal_mode	DQS squelch correction mode selection. 0: non-bypass mode; 1: bypass mode. **Note: DQS squelch** correction, that is, the internal logic of the chip automatically repeatedly increases or decreases the delay training for the external asynchronous signal reading **DQS** gating signal, and finally the gating signal can be properly gated to read **DQS.**
[0]	RW	cal_start	DQS squelch auto-calibration enable, valid in non-bypass mode. 1: enable; 0: disabled.

DDRC_PHY_REG3

DDRC_PHY_REG3 is DDRPHY register 3.

Offset Address	Register Name	Total Reset Value
0x804	DDRC_PHY_REG3	0x0000_0025

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													reserved_nz		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:1]	RW	reseverd_nz	Reserved, initial value is non-zero.
[0]	RW	phy_bl	Correct burst length selection. 0ÿburst4ÿ 1ÿburst8ÿ

DDRC_PHY_REG4

DDRC_PHY_REG4 is DDRPHY register 4.

Offset Address	Register Name	Total Reset Value
0x824	DDRC_PHY_REG4	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	phy_ck_en	CK/CKB I/O Enable. 0: enable; 1: disable.
[5:4]	RW	reserved_nz	Reserved, initial value is non-zero.
[3]	RW	phy_odt_en	ODT I/O enable. 0: enable; 1: disable.

Offset Address	Register Name	Total Reset Value
0x824	DDRC_PHY_REG4	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access Name	Description
[2] RW	phy_cs_en	CS I/O enable. 0: enable; 1: Disabled.
[1] RW	phy_cmd_en	CMD I/O enable. 0: always enable; 1: Enabled when a command is received.
[0] RW	phy_cke_en	CKE I/O Enable. 0: enable; 1: disable.

DDRC_PHY_REG4A

DDRC_PHY_REG4A is DDRPHY register 4A.

Offset Address	Register Name	Total Reset Value
0x838	DDRC_PHY_REG4A	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													phy_cl		phy_al
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access Name	Description
[31:8] RO	reserved	reserve.
[7:4] RW	phy_cl	CL (CAS latency) delay value. DDR2/DDR3 CL latency.
[3:0] RW	phy_al	AL (additive latency) value. DDR2/DDR3 AL latency.

DDRC_PHY_REG4B

DDRC_PHY_REG4B is DDRPHY register 4B.

Offset Address	Register Name	Total Reset Value
0x83C	DDRC_PHY_REG4B	0x0000_0009

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_dqssq_dly_h	In bypass mode, DQS gate delay selection for upper eight data bits DQ[15:8].
[2:0]	RW	phy_dqssq_dly_l	In bypass mode, the DQS gate delay selection of the lower eight bits of data DQ[15:8].

DDRC_PHY_REG6

DDRC_PHY_REG6 is DDRPHY register 6.

Offset Address	Register Name	Total Reset Value
0x8D4	DDRC_PHY_REG6	0x0000_000C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x8D4	DDRC_PHY_REG6	0x0000_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access Name	Description
selection. 0: no delay; [4] RW phy_ltxdqdll_byp		In bypass mode, left channel transmit DQ DLL phase delay 1: 90° delay.
[3] RW phy_ltxdqdll_en		Left channel transmit DQ DLL enable. 0: disabled; 1: enable.
[2:0] RW phy_ltxdqdll_dly		Left channel transmit DQ DLL phase delay selection. 000: no delay; 001: 22.5° delay; 010: 45° delay; 011: 67.5° delay; 100: 90° delay; 101: 112.5° delay; 110: 135° delay; 111: 157.5° delay.

DDRC_PHY_REG7

DDRC_PHY_REG7 is DDRPHY register 7.

Offset Address	Register Name	Total Reset Value
0x8D8	DDRC_PHY_REG7	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	

Bits	Access Name	Description
[31:5]	RO reserved	reserve.
selection. 0: no delay; [4]	RW phy_ltxdqsdll_bypss	In bypass mode, the left channel transmits DQS DLL phase delay 1: 90° delay.
[3]	RW phy_ltxdqsdll_en	Left channel transmit DQS DLL enable. 0: disabled; 1: enable.
[2:0]	RW phy_ltxdqsdll_dly	Left channel transmit DQS DLL phase delay select. 000: no delay; 001: 22.5° delay; 010: 45° delay; 011: 67.5° delay; 100: 90° delay; 101: 112.5° delay; 110: 135° delay; 111: 157.5° delay.

DDRC_PHY_REG8

DDRC_PHY_REG8 is DDRPHY register 8.

Offset Address	Register Name	Total Reset Value
0x8E0	DDRC_PHY_REG8	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	phy_ldqssqdll_en	Left channel receive DQS squelch DLL enable. 0: enable; 1: disable.
[5:3]	RW	phy_ldqssqdll_dly	Left channel receive DQS squelch DLL phase delay selection. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.
[2]	RW	phy_lrxdqsdll_en	Left channel receive DQS latching DLL enable. 0: enable; 1: disable.
[1:0]	RW	phy_lrxdqsdll_dly	The left channel receives DQS latching DLL phase delay selection. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay.

DDRC_PHY_REG9

DDRC_PHY_REG9 is DDRPHY register 9.

Offset Address	Register Name	Total Reset Value
0x914	DDRC_PHY_RE9	0x0000_000C

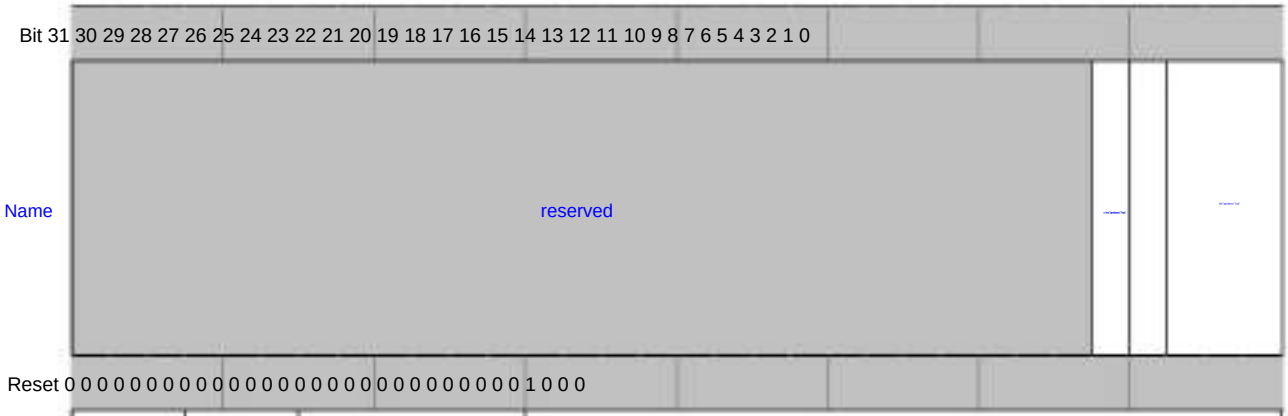
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	phy_rtxdqdll_byph	In bypass mode, right channel transmit DQ DLL phase delay selection. 0: no delay; 1: 90° delay.
[3]	RW	phy_rtxdqdll_en	Right channel transmit DQ DLL enable. 0: disabled; 1: enable.
[2:0]	RW	phy_rtxdqdll_dly	Right channel transmit DQ DLL phase delay selection. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.

DDRC_PHY_REG10

DDRC_PHY_REG10 is DDRPHY register 10.

Offset Address	Register Name	Total Reset Value
0x918	DDRC_PHY_RE10	0x0000_0008



Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	phy_rtxdqsdll_bypsel ection.h	In bypass mode, the right channel transmits DQS DLL phase delay 0: no delay; 1: 90° delay.
[3]	RW	phy_rtxdqsdll_en	Right channel transmit DQS DLL enable. 0: disabled; 1: enable.
[2:0]	RW	phy_rtxdqsdll_dly	Right channel transmit DQS DLL phase delay select. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.

DDRC_PHY_REG11

DDRC_PHY_REG11 is DDRPHY register 11.

Offset Address	Register Name	Total Reset Value
0x920	DDRC_PHY_REG11	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	phy_rdqssqdll_en	Right channel receive DQS squelch DLL enable. 0: enable; 1: disable.
[5:3]	RW	phy_rdqssqdll_dly	Right channel receive DQS squelch DLL phase delay selection. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.
[2]	RW	phy_rrxdqsdll_en	Right channel receive DQS latching DLL enable. 0: enable; 1: disable.
[1:0]	RW	phy_rrxdqsdll_dly	The left channel receives DQS latching DLL phase delay selection. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay.

DDRC_PHY_REG12

DDRC_PHY_REG12 is DDRPHY register 12.

Offset Address	Register Name	Total Reset Value
0x840	DDRC_PHY_REG12	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	phy_cmd0pu_str	phy_cmd0pd_str
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0		

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_cmd0pu_str	CMD0 I/O pull-up drive strength control.
[3:0]	RW	phy_cmd0pd_str	CMD0 I/O pull-down drive strength control.

DDRC_PHY_REG13

DDRC_PHY_REG13 is DDRPHY register 13.

Offset Address	Register Name	Total Reset Value
0x844	DDRC_PHY_REG13	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	phy_cmd0_rsl	phy_cmd0_fsl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0		

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_cmd0_rsl	CMD0 I/O rising slope control.
[3:0]	RW	phy_cmd0_fsl	CMD0 I/O falling slope control.

DDRC_PHY_REG14

DDRC_PHY_REG14 is DDRPHY register 14.

Offset Address	Register Name	Total Reset Value
0x848	DDRC_PHY_REG14	0x0000_0073

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
enable; [7]	RW	phy_cmd0sdll_lpen	CMD0 Slave DLL low power enable. 0: 1: disable.
[6]	RW	phy_cmd0dly_en	CMD0 One clock (2xclk) cycle delay selection. 0: no delay; 1:1 cycle.
[5]	RW	phy_rstn_pu	RESETN Weak pull-up enable. 0: enable; 1: disable.
[4]	RW	phy_rstn_pd	RESETN Weak pull-down enable. 0: disabled; 1: enable.
[3]	RW	phy_cmd0_pu	CMD0 weak pull-up enable. 0: enable; 1: disable.
[2]	RW	phy_cmd0_pd	CMD0 weak pull-down enable. 0: disabled; 1: enable.
[1]	RW	phy_cmd0pu_msb	CMD0 pull-up drive strength control, the highest bit.
[0]	RW	phy_cmd0pd_msb	CMD0 pull-down drive strength control, the highest bit.

DDRC_PHY_REG15

DDRC_PHY_REG15 is DDRPHY register 15.

Offset Address	Register Name	Total Reset Value
0x84C	DDRC_PHY_REG15	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	phy_cmd0fb_en	CMD0 feedback enable. 0: disabled; 1: enable.
reverse; [4]	RW	phy_cmd0sdll_inv	CMD0 is selected from DLL reverse mode. 0: no 1: Reverse.
[3]	RW	phy_cmd0sdll_en	CMD0 is enabled from DLL. 0: disabled; 1: enable.
[2:0]	RW	phy_cmd0txsdll_dl 11:	CMD0 Transmit Slave DLL Phase Delay Select. 00: no delay; 01: 22.5° delay; 10: 45° delay; 67.5° delay; y 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.

DDRC_PHY_REG16

DDRC_PHY_REG16 is DDRPHY register 16.

Offset Address	Register Name	Total Reset Value
0x854	DDRC_PHY_REG16	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved phy_cmd1pu_str phy_cmd1pd_str
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_cmd1pu_str	CMD1 pull-up drive strength control.
[3:0]	RW	phy_cmd1pd_str	CMD1 pull-down drive strength control.

DDRC_PHY_REG17

DDRC_PHY_REG17 is DDRPHY register 17.

Offset Address	Register Name	Total Reset Value
0x858	DDRC_PHY_REG17	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved phy_cmd1_rsl phy_cmd1_fsl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_cmd1_rsl	CMD1 rising slope control.
[3:0]	RW	phy_cmd1_fsl	CMD1 falling slope control.

DDRC_PHY_REG18

DDRC_PHY_REG18 is DDRPHY register 18.

Offset Address	Register Name	Total Reset Value
0x85C	DDRC_PHY_REG18	0x0000_0053

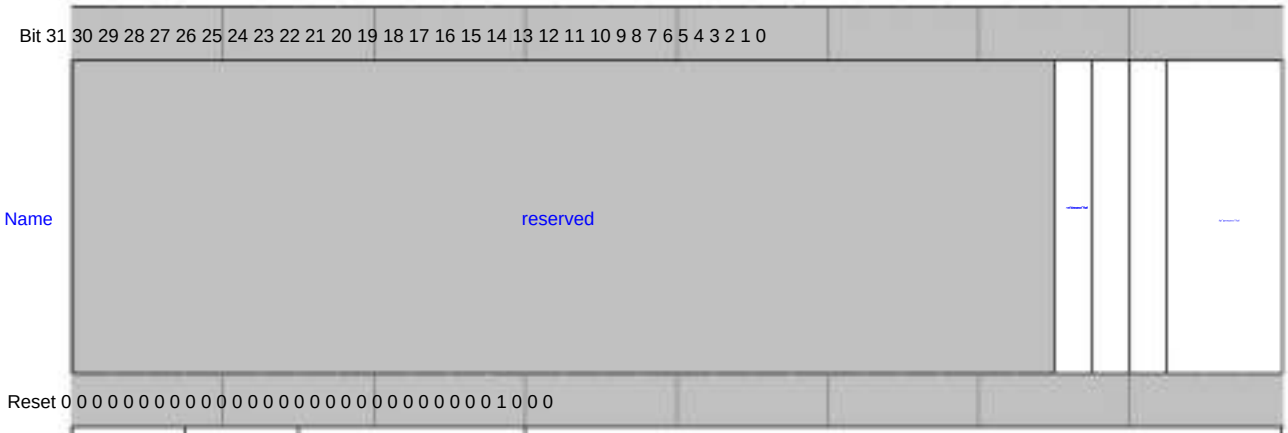
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
enable; [7]	RW	phy_cmd1sdll_lpen	CMD1 Slave DLL low power enable. 0: 1: disable.
[6]	RW	phy_cmd1dly_en	CMD1 One clock (2xclk) cycle delay selection. 0: no delay; 1:1 cycle.
[5]	RW	phy_rstn_pu	CKE Weak pull-up control. 0: enable; 1: disable.
[4]	RW	phy_rstn_pd	CKE weak pull-down enable. 0: disabled; 1: enable.
[3]	RW	phy_cmd1_pu	CMD1 weak pull-up enable. 0: enable; 1: disable.
[2]	RW	phy_cmd1_pd	CMD1 weak pull-down enable. 0: disabled; 1: enable.
[1]	RW	phy_cmd1pu_msb	CMD1 pull-up drive strength control, the highest bit.
[0]	RW	phy_cmd1pd_msb	CMD1 pull-down drive strength control, highest bit.

DDRC_PHY_REG19

DDRC_PHY_REG19 is DDRPHY register 19.

Offset Address	Register Name	Total Reset Value
0x860	DDRC_PHY_REG19	0x0000_0008



Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	phy_cmd1fb_en	CMD1 feedback enable. 0: disabled; 1: enable.
[4]	RW	phy_cmd1sdll_inv	CMD1 Select from DLL reverse mode. 0: no reverse; 1: Reverse.
[3]	RW	phy_cmd1sdll_en	CMD1 Enable from DLL. 0: disabled; 1: enable.
[2:0]	RW	phy_cmd1txsdll_dl	CMD1 Transmit Slave DLL Phase Delay Select. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; y 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.

DDRC_PHY_REG20

DDRC_PHY_REG20 is DDRPHY register 20.

Offset Address	Register Name	Total Reset Value
0x864	DDRC_PHY_REG20	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	phy_cmd1obv_en	CMD1 observation enable. 0: disabled 1: enable
[2:1]	RW	reserved_nz	Reserved, initial value non-zero.
[0]	RW	phy_ckdly_en	CK One clock (2xclk) cycle delay selection. 0: no delay; 1: 1 cycle.

DDRC_PHY_REG21

DDRC_PHY_REG21 is DDRPHY register 21.

Offset Address	Register Name	Total Reset Value
0x868	DDRC_PHY_REG21	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	phy_cksdll_inv	CK is selected from DLL reverse mode. 0: no reverse; 1: Reverse.
[2:0]	RW	phy_cktxsdll_dly	CK transmit from DLL phase delay select. 00: no delay; 01: 22.5° delay; 10: 45° delay; 11: 67.5° delay; 000: 90° delay; 001: 112.5° delay; 010: 135° delay; 011: 157.5° delay.

DDRC_PHY_REG22

DDRC_PHY_REG22 is DDRPHY register 22.

Offset Address	Register Name	Total Reset Value
0x870	DDRC_PHY_REG22	0x0000_0088

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												phy_ckpu_str			phy_ckpd_str
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x870	DDRC_PHY_REG22	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		phy_ckpu_str	phy_ckpd_str
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0	1 0 0 0

Bits	Access	Name	Description
[7:4]	RW	phy_ckpu_str	CK pull-up drive strength control.
[3:0]	RW	phy_ckpd_str	CK pull-down drive strength control.

DDRC_PHY_REG23

DDRC_PHY_REG23 is DDRPHY register 23.

Offset Address	Register Name	Total Reset Value
0x874	DDRC_PHY_REG23	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		phy_ck_rsl	phy_ck_fsl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0	1 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_ck_rsl	CK rising slope control.
[3:0]	RW	phy_ck_fsl	CK falling slope control.

DDRC_PHY_REG24

DDRC_PHY_REG24 is DDRPHY register 24.

Offset Address	Register Name	Total Reset Value
0x878	DDRC_PHY_REG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														~~~	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	phy_ckpu_msb	CK pull-up drive strength control, highest bit.
[0]	RW	phy_ckpd_msb	CK pull-down drive strength control, MSB.

DDRC_PHY_REG25

DDRC_PHY_REG25 is DDRPHY register 25.

Offset Address	Register Name	Total Reset Value
0x880	DDRC_PHY_REG25	0x0000_0088

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												phy_dqpu_str			phy_dqpd_str
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_dqpu_str	DQ pull-up drive strength control.
[3:0]	RW	phy_dqpd_str	DQ pull-down drive strength control.

DDRC_PHY_REG26

DDRC_PHY_REG26 is DDRPHY register 26.

Offset Address	Register Name	Total Reset Value
0x884	DDRC_PHY_REG26	0x0000_0088

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved phy_dq_rsl phy_dq_fsl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	phy_dq_rsl	DQ rising slope control.
[3:0]	RW	phy_dq_fsl	DQ falling slope control.

DDRC_PHY_REG27

DDRC_PHY_REG27 is DDRPHY register 27.

Offset Address	Register Name	Total Reset Value
0x888	DDRC_PHY_REG27	0x0000_0024

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_dqpu_odt	DQ pull-up ODT control.
[2:0]	RW	phy_dqpd_odt	DQ pull-down ODT control.

DDRC_PHY_REG28

DDRC_PHY_REG28 is DDRPHY register 28.

Offset Address	Register Name	Total Reset Value
0x88C	DDRC_PHY_REG28	0x0000_0037

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1			1 1

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	phy_dqpd_msb	DQ pull-down drive strength control, highest bit.
[4]	RW	phy_dqpu_msb	DQ pull-up drive strength control, the highest bit.
[3]	RW	phy_dqpu_en	DQ weak pull-up enabled. 0: enable 1: disable
[2]	RW	phy_dqpd_en	DQ weak pull-down enable. 1: enable 0: disabled
[1]	RW	phy_dqpu_odtmsb	DQ pull-up ODT control, the highest bit.
[0]	RW	phy_dqpd_odtmsb	DQ pull-down ODT control, highest bit.

DDRC_PHY_REG29

DDRC_PHY_REG29 is DDRPHY register 29.

Offset Address	Register Name	Total Reset Value
0x9C0	DDRC_PHY_REG29	0x0000_002D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	reserved_nz1	Reserved, initial value non-zero.
[4:3]	RW	phy_dqssq_2xdly_h	The upper eight bits receive the clock (2xclk) cycle delay selection for the DQS squelch. 11: 3 cycles 10: 2 cycles 01: 1 cycle 00: no delay
[2]	RW	reserved_nz0	Reserved, initial value is non-zero.
[1:0]	RW	phy_dqssq_2xdly_l	The lower eight bits receive the clock (2xclk) cycle delay selection for the DQS squelch. 11: 3 cycles 10: 2 cycles 01: 1 cycle 00: no delay

DDRC_PHY_REG30

DDRC_PHY_REG30 is DDRPHY register 30.

Offset Address	Register Name	Total Reset Value
0xAC4	DDRC_PHY_REG30	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a1	A1 delay.
[2:0]	RW	phy_skew_a0	A0 delay.

DDRC_PHY_REG31

DDRC_PHY_REG31 is DDRPHY register 31.

Offset Address	Register Name	Total Reset Value
0xAC8	DDRC_PHY_REG31	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a3	A3 delay.
[2:0]	RW	phy_skew_a2	A2 delay.

DDRC_PHY_REG32

DDRC_PHY_REG32 is DDRPHY register 32.

Offset Address	Register Name	Total Reset Value
0xACC	DDRC_PHY_REG32	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a5	A5 delayed.
[2:0]	RW	phy_skew_a4	A4 delayed.

DDRC_PHY_REG33

DDRC_PHY_REG33 is DDRPHY register 33.

Offset Address	Register Name	Total Reset Value
0xAD0	DDRC_PHY_REG33	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a7	A7 delay.
[2:0]	RW	phy_skew_a6	A6 delay.

DDRC_PHY_REG34

DDRC_PHY_REG34 is DDRPHY register 34.

Offset Address	Register Name	Total Reset Value
0xAD4	DDRC_PHY_REG34	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a9	A9 delay.
[2:0]	RW	phy_skew_a8	A8 delay.

DDRC_PHY_REG35

DDRC_PHY_REG35 is DDRPHY register 35.

Offset Address	Register Name	Total Reset Value
0xAD8	DDRC_PHY_REG35	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a11	A11 delay.
[2:0]	RW	phy_skew_a10	A10 delay.

DDRC_PHY_REG36

DDRC_PHY_REG36 is DDRPHY register 36.

Offset Address	Register Name	Total Reset Value
0xADC	DDRC_PHY_REG36	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_a13	A13 delay.
[2:0]	RW	phy_skew_a12	A12 delay.

DDRC_PHY_REG37

DDRC_PHY_REG37 is DDRPHY register 37.

Offset Address	Register Name	Total Reset Value
0xAE0	DDRC_PHY_REG37	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_b1	B1 delay.
[2:0]	RW	phy_skew_b0	B0 delay.

DDRC_PHY_REG38

DDRC_PHY_REG38 is DDRPHY register 38.

Offset Address	Register Name	Total Reset Value
0xAE4	DDRC_PHY_REG38	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_rasb	RASB delay.
[2:0]	RW	phy_skew_b2	B2 delay.

DDRC_PHY_REG39

DDRC_PHY_REG39 is DDRPHY register 39.

Offset Address	Register Name	Total Reset Value
0xAE8	DDRC_PHY_REG39	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_web	WEB latency.
[2:0]	RW	phy_skew_casb	CASB delay.

DDRC_PHY_REG40

DDRC_PHY_REG40 is DDRPHY register 40.

Offset Address	Register Name	Total Reset Value
0xAEC	DDRC_PHY_REG40	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_ckb1	CKB1 delay.
[2:0]	RW	phy_skew_ck1	CK1 delay.

DDRC_PHY_REG41

DDRC_PHY_REG41 is DDRPHY register 41.

Offset Address	Register Name	Total Reset Value
0xAF0	DDRC_PHY_REG41	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_cke	CKE delay.
[2:0]	RW	phy_skew_odt	ODT delay.

DDRC_PHY_REG42

DDRC_PHY_REG42 is DDRPHY register 42.

Offset Address	Register Name	Total Reset Value
0xAF4	DDRC_PHY_REG42	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	phy_skew_rstn	RESETN delay.

DDRC_PHY_REG43

DDRC_PHY_REG43 is DDRPHY register 43.

Offset Address	Register Name	Total Reset Value
0xAF8	DDRC_PHY_REG43	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_txskew_dm1	TX DM1 delay.
[2:0]	RW	phy_txskew_dm0	TX DM0 delay.

DDRC_PHY_TXDQSKEW

DDRC_PHY_TXDQSKEW is the DDRPHY register.

Offset Address	Register Name	Total Reset Value
0xAFC+0x4*dq_hf dq_hf(0~7)	DDRC_PHY_TXDQSKEW	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_txskew_dq_o	TX DQ[2*dq_hf+1] delay.
[2:0]	RW	phy_txskew_dq_e	TX DQ[2*dq_hal] delay.

DDRC_PHY_REG52

DDRC_PHY_REG52 is the DDRPHY register.

Offset Address	Register Name	Total Reset Value
0xB1C	DDRC_PHY_REG52	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_txskew_dqs1	TX DQS1 delay.
[2:0]	RW	phy_txskew_dqs0	TX DQS0 delay.

DDRC_PHY_REG53

DDRC_PHY_REG53 is DDRPHY register 53.

Offset Address	Register Name	Total Reset Value
0xB20	DDRC_PHY_REG53	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	phy_skew_a14	A14 delay.

DDRC_PHY_REG54

DDRC_PHY_REG54 is DDRPHY register 54.

Offset Address	Register Name	Total Reset Value
0xB24	DDRC_PHY_REG54	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_skew_ckb0	CKB0 delay.
[2:0]	RW	phy_skew_ck0	CK0 delay.

DDRC_PHY_REG55

DDRC_PHY_REG55 is DDRPHY register 55.

Offset Address	Register Name	Total Reset Value
0xB28	DDRC_PHY_REG55	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_rxskew_dm1	RX DM1 delay.
[2:0]	RW	phy_rxskew_dm0	RX DM0 delay.

DDRC_PHY_RXDQSKEW

DDRC_PHY_RXDQSKEW is the DDRPHY register.

Offset Address	Register Name	Total Reset Value
0xB2C+0x4*dq_hf dq_hf(0~7)	DDRC_PHY_RXDQSKEW	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_rxskew_dq_o	RX DQ[2*dq_hf+1] delay.
[2:0]	RW	phy_rxskew_dq_e	RX DQ[2*dq_hal] delay.

DDRC_PHY_REG5E

DDRC_PHY_REG5E is DDRPHY register 5E.

Offset Address	Register Name	Total Reset Value
0xB4C	DDRC_PHY_REG5E	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5:3]	RW	phy_rxskew_dqs1	RX DQS1 latency.
[2:0]	RW	phy_rxskew_dqs0	RX DQS0 delay.

DDRC_PHY_REG60

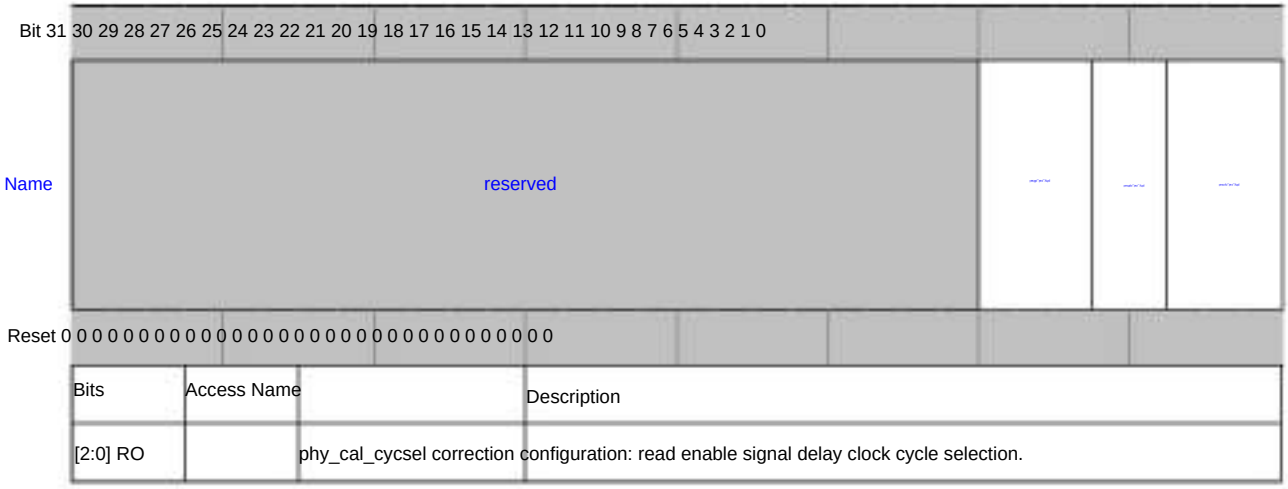
DDRC_PHY_REG60 is DDRPHY register 60.

Offset Address	Register Name	Total Reset Value
0xBE0+0x4*blanes white(0~1)	DDRC_PHY_REG60	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:5]	RO	phy_cal_dllsel	Calibration configuration: DLL phase delay selection.
[4:3]	RO	phy_cal_ophsel	correction configuration: gating delay clock period selection.

Offset Address	Register Name	Total Reset Value
0xBE0+0x4*blanes white(0~1)	DDRC_PHY_REG60	0x0000_0000

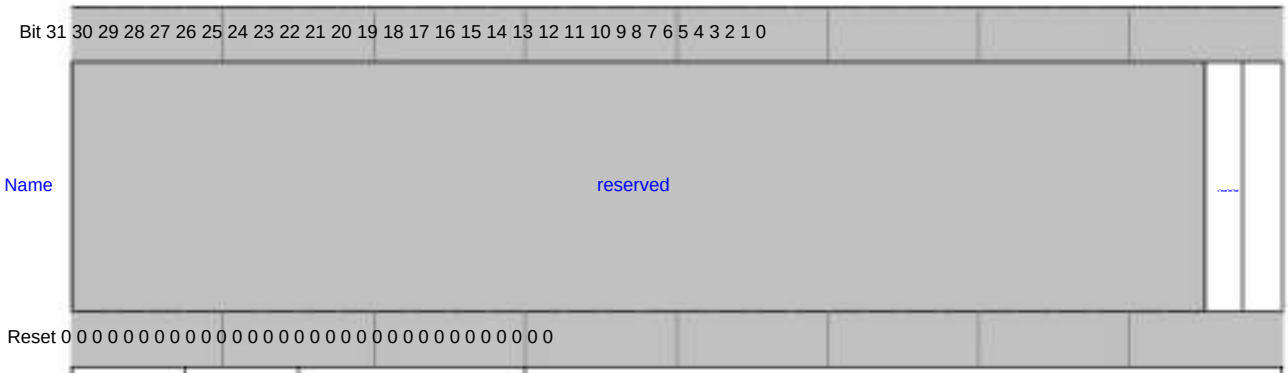


Bits	Access Name		Description
[2:0]	RO	phy_cal_cycsel	correction configuration: read enable signal delay clock cycle selection.

DDRC_PHY_REG61

DDRC_PHY_REG61 is DDRPHY register 61.

Offset Address	Register Name	Total Reset Value
0xBE8	DDRC_PHY_REG61	0x0000_0000



Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	phy_cal_done_h	DQS gating signal correction completion signal of high eight-bit data DQ[15:8].
[0]	RO	phy_cal_done_l	DQS gate control signal of the lower eight bits of data DQ[15:8] Calibration complete signal.

DDRC_PHY_REG62

DDRC_PHY_REG62 is DDRPHY register 62.

Offset Address	Register Name	Total Reset Value
0xBC4	DDRC_PHY_REG62	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

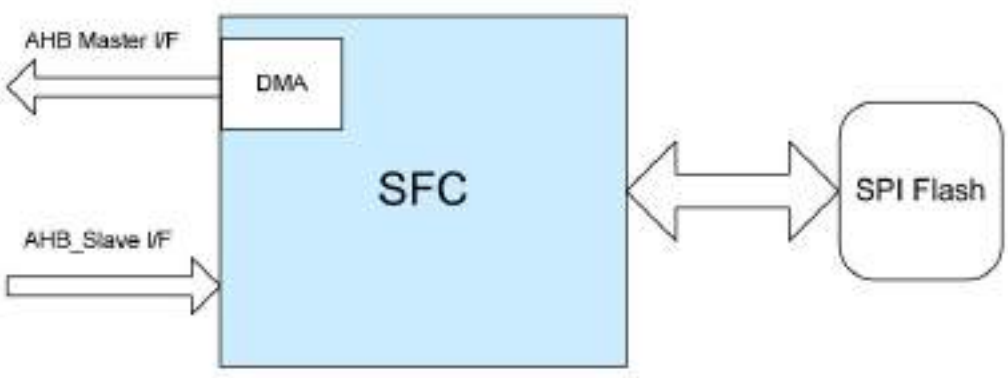
Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	phy_idqe_h DQS gate signal	sampling DQS value of high eight-bit data DQ[15:8].
[0]	RO	phy_idqs_l DQS gate signal	sampling DQS value of the lower eight bits of data DQ[7:0].

4.2 SFC

4.2.1 Overview

SFC (Serial Peripheral Interface Flash Controller) is a SPI Flash controller. The service side provides an AHB (Advanced High performance Bus) Slave interface, which mainly completes the access control function of the AHB channel to the SPI Flash; provides an AHB Master interface for reading and writing Flash in DMA mode.

Figure 4-2 SFC application block diagram



4.2.2 Features

4.2.2.1 AHB Slave interface

The AHB Slave interface has the following characteristics:

An AHB Slave interface is provided, which can access internal configuration registers or directly access SPI flash memory according to different selection

signals. Support AMBA2.0 protocol.

Only little-endian is supported.

4.2.2.2 AHB Master interface

The AHB Master interface has the following characteristics:

Provide an AHB Master interface for transferring data between memory and Flash by DMA.

Support AMBA2.0 protocol. Only

little-endian is

supported. Only Single, INCR4, INCR8, INCR16 transfer types. Early

Termination is not supported. Support

bus lock.

4.2.2.3 Memory Interface

The memory interface has the following characteristics:

Supports 2 chip selects. The storage space supports up to 128Mbit (3byte address mode)/8Gbit (4byte address mode). SPI Flash can be mapped to the system address space respectively, the mapping base address can be configured, and the mapping system space is limited to 0x58000000~0x5BFFFFFF space.

Address Alias is supported, and address Alias can be used to map address 0 to CS1 after power-on, and the chip starts from CS1.

ÿÿ Standard SPIÿDual-Output/Dual-Input SPIÿQuad-Output/Quad-Input SPIÿ
Dual-I/O SPI, Quad-I/O SPI, Full DIO SPI, Full QIO SPI seven interface types. After power-on, it supports Standard SPI interface type by default, and the interface type can be switched through register configuration. Support 3byte

and 4byte Flash address modes. The default address mode can be selected by pulling the pin SFC_ADDR_MODE (multiplexed with the pin SFC_CLK) up and down, and the address mode can also be switched through the configuration register. The 3byte mode supports a maximum of 128Mbit, and the 4byte mode supports a maximum of 8Gbit.

SPI Flash read and write operations support three methods: bus direct read and write, register programming read and write, and DMA read and write. Various

write protection operations are supported.

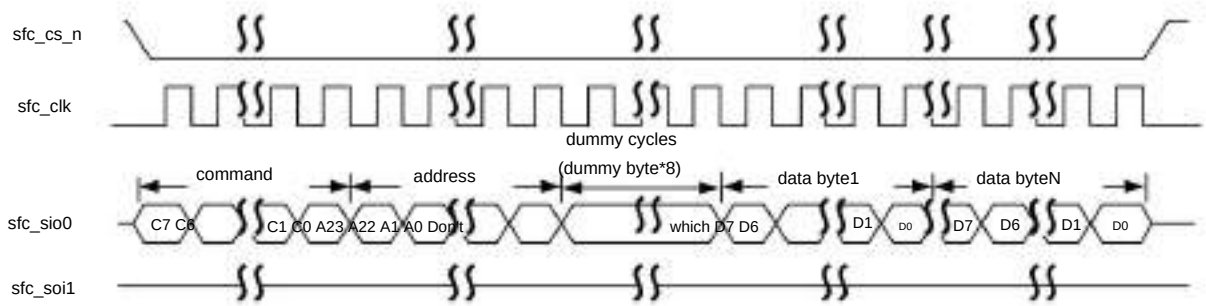
4.2.3 Functional description

4.2.3.1 Interface Mode Timing

Standard SPI

The Standard SPI interface mode has a 1bit data input line and a 1bit data output line, and the interface timing is shown in Figure 4-3 and Figure 4-4 .

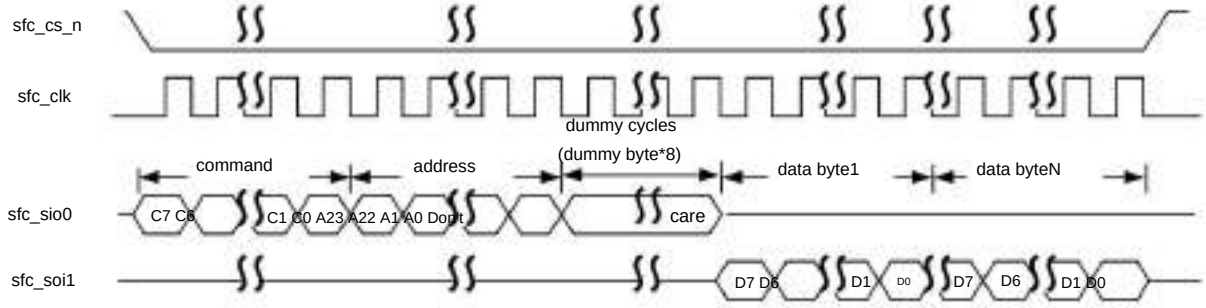
Figure 4-3 Standard SPI (write) interface timing diagram



Note: Opcode/Address/DummyByte is output on sfc_sio0 line in single-bit serial mode.

Data is output on the sfc_sio0 line in single-bit serial mode.

Figure 4-4 Standard SPI (read) interface timing diagram



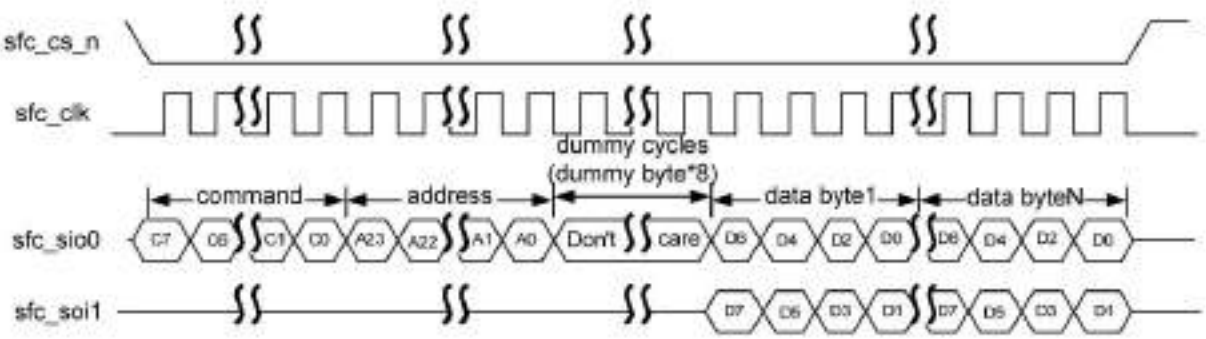
Note: Opcode/Address/DummyByte is output on sfc_sio0 line in single-bit serial mode.

Data is input on the sfc_soi1 line in single-bit serial mode.

Dual Input/Dual Output SPI

The Dual Input/Dual Output SPI interface mode has a 2-bit bidirectional data line, and the interface timing is shown in Figure 4-5 .

Figure 4-5 Sequence Diagram of Dual Input/Dual Output SPI Interface



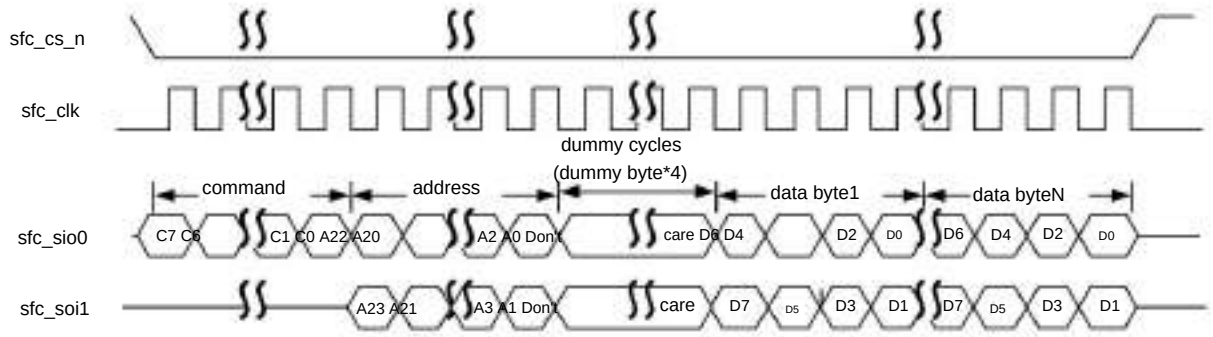
Note: Opcode/Address/DummyByte is output on the sfc_sio0 line in single-bit serial mode.

Data is output (write) or input (read) on the sfc_sio0/sfc_soi1 line in the form of Dual Bits.

Dual I/O SPI

The Dual I/O SPI interface mode has a 2-bit bidirectional data line, and the interface timing is shown in Figure 4-6 .

Figure 4-6 Dual I/ O SPI interface timing diagram

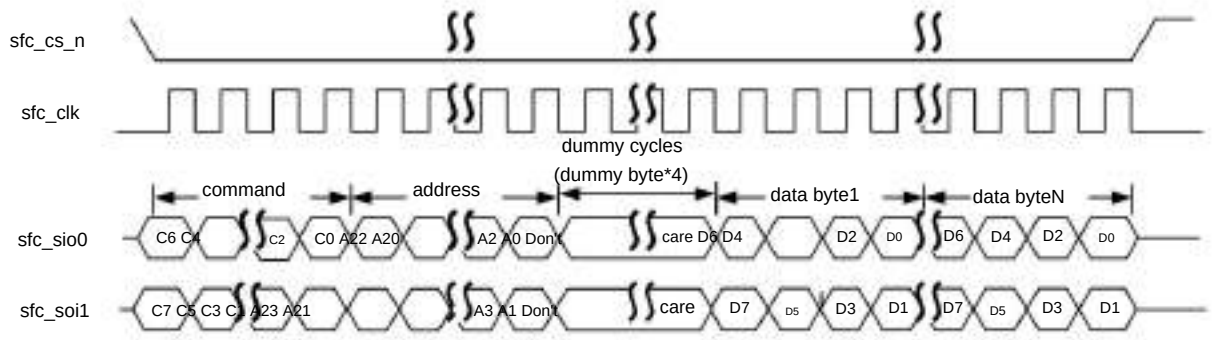


Note: Opcode is output on sfc_sio0 line in single-bit serial mode. Address/DummyByte is output on the sfc_sio0/sfc_soi1 line in the form of Dual Bits. Data is output (write) or input (read) on the sfc_sio0/sfc_soi1 line in the form of Dual Bits.

Full Dual I/O SPI

The Dual Input/Dual Output SPI interface mode has a 2-bit bidirectional data line, and the interface timing is shown in Figure 4-7 .

Figure 4-7 Full Dual I/O SPI interface timing diagram

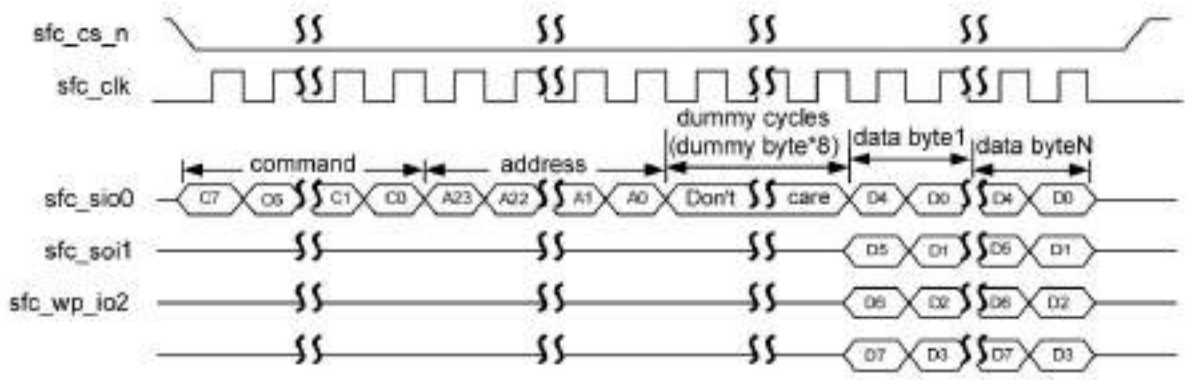


Note: Opcode/Address/DummyByte is output on sfc_sio0/sfc_soi1 line in Dual Bits mode. Data is output (write) or input (read) on the sfc_sio0/sfc_soi1/sfc_wp/sfc_hold line in the form of Dual Bits.

Quad Input/Quad Output SPI

The Quad Input/Quad Output SPI interface mode has a 4-bit bidirectional data line, and the interface timing is shown in Figure 4-8 .

Figure 4-8 Quad Input/Quad Output SPI interface timing diagram

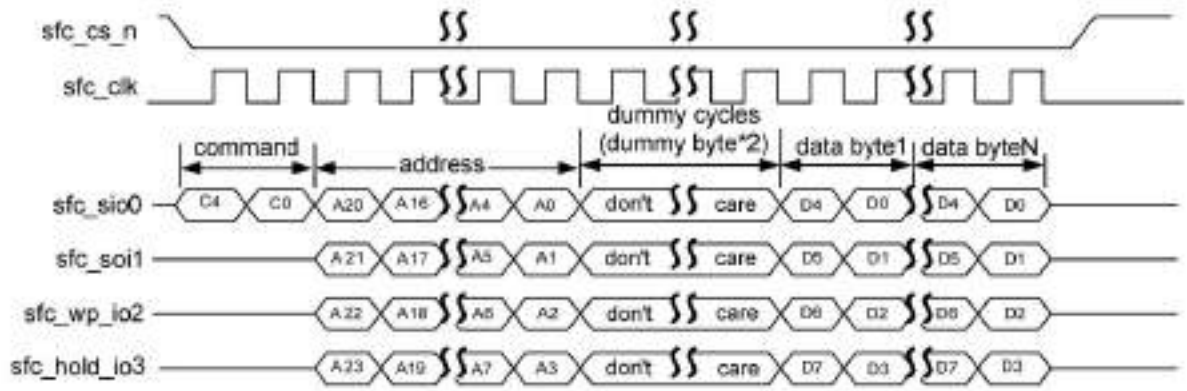


Note: Opcode/Address/DummyByte is output on the sfc_sio0 line in single-bit serial mode.
Data is output (write) or input (read) on the sfc_sio0/sfc_soi1/sfc_wp/sfc_hold line in Quad Bits mode.

Quad I/O SPI

The Quad SPI interface mode has a 4bit bidirectional data line, and the interface timing is shown in Figure 4-9 .

Figure 4-9 Quad I/O SPI Interface Timing Diagram

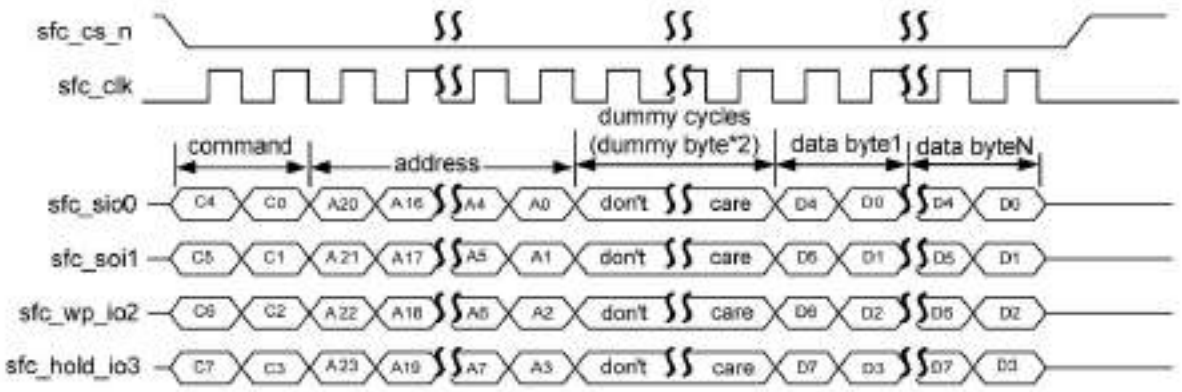


Note: Opcode is output on sfc_sio0 line in single-bit serial mode. Address/DummyByte is output on the sfc_sio0/
sfc_soi1/sfc_wp/sfc_hold line in Quad Bits mode. Data is output (write) or input (read) on the sfc_sio0/sfc_soi1/sfc_wp/sfc_hold line in Quad Bits mode.

Full Quad SPI

The Full Quad SPI interface mode has a 4bit bidirectional data line, and the interface timing is shown in Figure 4-10 .

Figure 4-10 Full Quad SPI interface timing diagram



Note: Opcode/Address/DummyByte is output on the sfc_sio0/sfc_soi1/sfc_wp/sfc_hold line in Quad Bits mode.
Data is output (write) or input (read) on the sfc_sio0/sfc_soi1/sfc_wp/sfc_hold line in Quad Bits mode.

4.2.3.2 Read and write Flash operation

There are three ways to read and write Flash:

Send SPI Flash Program, Read and other commands through register configuration to read and write Flash. This method requires the CPU to directly control the Flash commands and parameters to be sent.

The CPU reads and writes Flash through the AHB Slave interface in a manner similar to reading and writing ordinary Memory. The SFC module will automatically map the read and write operation timing of the AHB bus to the SPI Flash read and write commands. Data is moved between Flash and memory through DMA.

4.2.3.3 Other operations

Other operations on Flash such as Erase, reading Device ID, etc. must be realized through register access.

4.2.3.4 Flash Address Mode Switching

This module supports two Flash address modes of 3Bytes and 4Bytes. The initial default address mode can be selected by pulling the pin up and down, or the address mode can be dynamically switched through the configuration register after the chip is started.

The default address mode configuration when the chip starts:

Pull down the pin SFC_ADDR_MODE (multiplexed with the pin SFC_CLK), the default addressing mode is 3Bytes addressing mode. Pull up the pin SFC_ADDR_MODE

(multiplexed with the pin SFC_CLK), and the default addressing mode is 4Bytes addressing mode.

After the chip starts up, the steps to switch the Flash address mode are as follows:

1. No Flash operation or guaranteed completion of previous Flash operations.
2. According to the requirements of the device, use the register method to send specific commands to configure Flash to enter 4B mode.
3. Configure the Flash address mode of SFC to 4B mode (GLOBAL_CONFIG[flash_addr_mode])

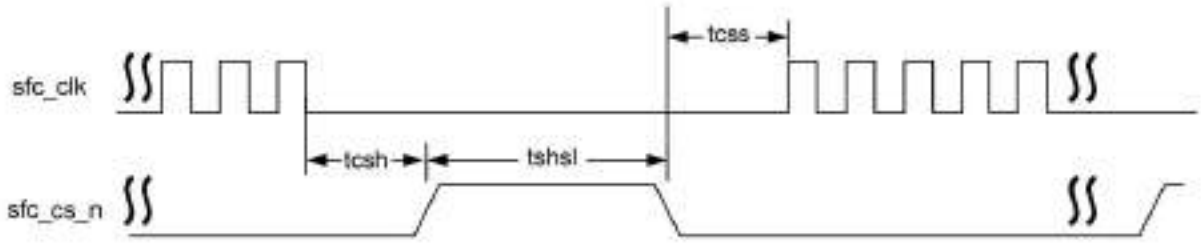
----Finish

Specific SPI Flash address mode switching command. Please find the relevant device manual.

4.2.3.5 Timing description

The sequence and parameter description are shown in Figure 4-11 .

Figure 4-11 SPI output timing diagram



ÿÿ

tcshÿCS setup timeÿ tcssÿ
CS hold timeÿ

tshsl: Chip selection deselect time.

4.2.4 Workflow

4.2.4.1 Initialization process

The initialization process is as follows:

1. (If you need to adjust the Timing parameter) Configure the Timing register.
2. (If you need to use the Flash 4Bytes address mode), please refer to "4.2.3.4 Flash Address Mode Switching".
3. Configure the bus operation mode register:

   a. Configure BUS_FLASH_SIZE according to the actual Flash size (the device model can be obtained by sending the Read ID command to Flash query).

   b. Configure CS1_BUS_BASE_ADDR ,

   The BUS_ALIAS_ADDR mapping space should be within the address space allocated to SFC_MEM by the system bus.

   Usually BUS_ALIAS_ADDR corresponds to the address mapped when starting from Flash, only the default value is meaningful, so it is generally fixed and not modified.

   c. Some devices require to enter the non-Standard SPI read and write sequence and need to configure the Flash with special commands in advance. according to

   The device needs to send a specific command to configure the Flash with the register method.

   d. Configure bus read and write operation instructions and parameters.

   Configure BUS_CONFIG1/BUS_CONFIG2.

   e. If bus write operation needs to be enabled, enable bus write. The bus write function is disabled by default.

   Configure BUS_CONFIG1[wr_enable] to 1.

说明

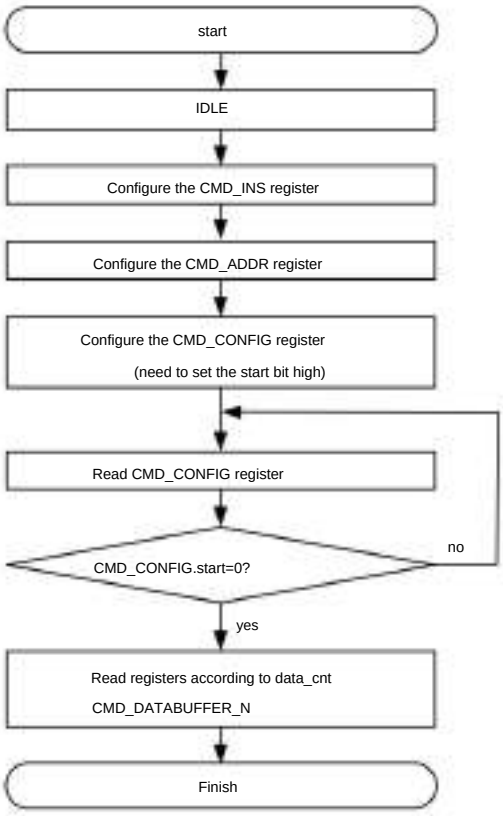
The flash mode of register operation does not need to be initialized, and each operation needs to be reconfigured. Note that the above initialization process is for reference only, please make adjustments depending on device differences.

----Finish

4.2.4.2 Operation flow of reading Flash through register

The operation process of reading Flash through the register is shown in Figure 4-12 (query mode).

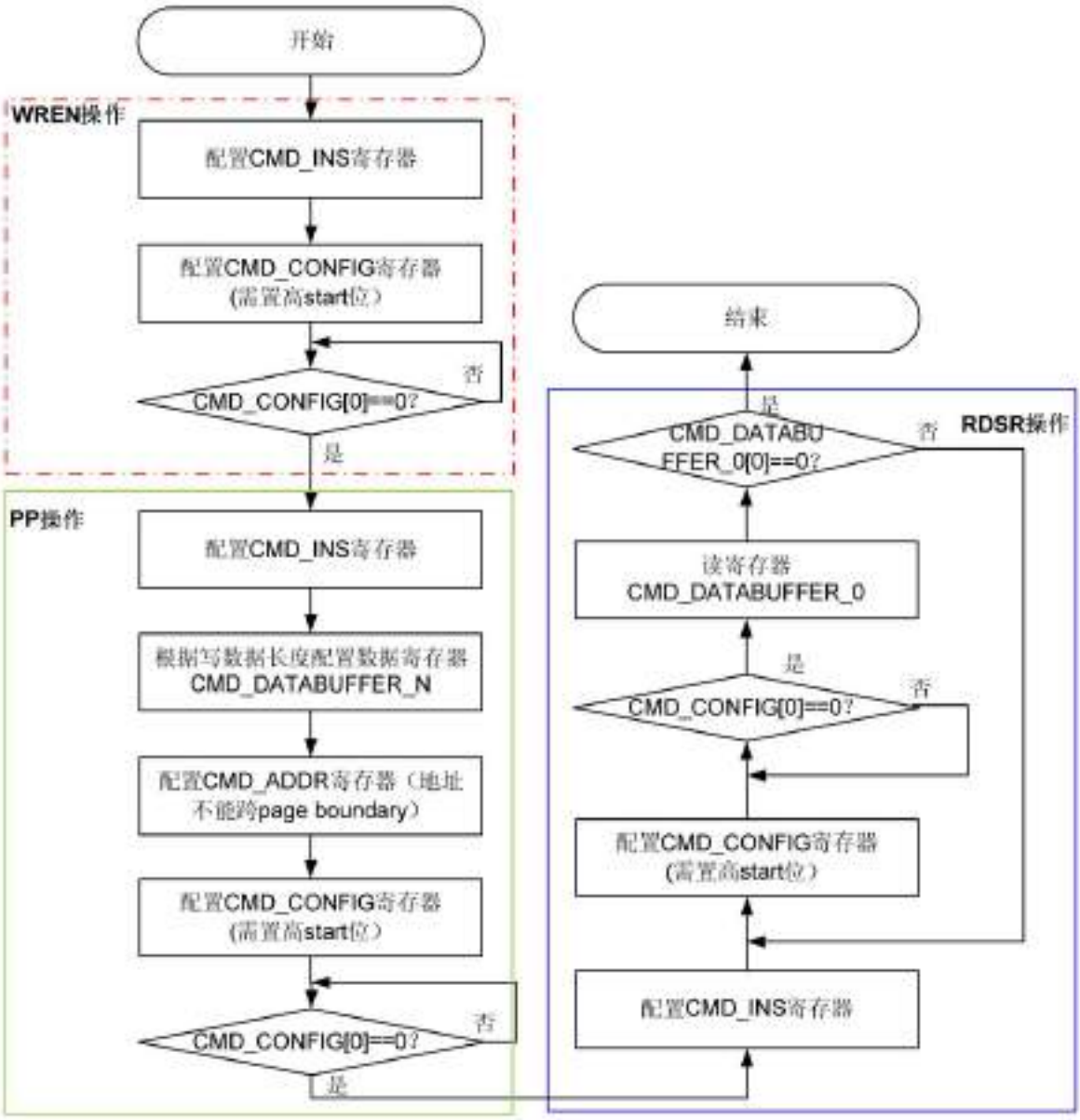
Figure 4-12 Operation process of reading Flash through registers (query mode)



4.2.4.3 Write Flash operation flow through register

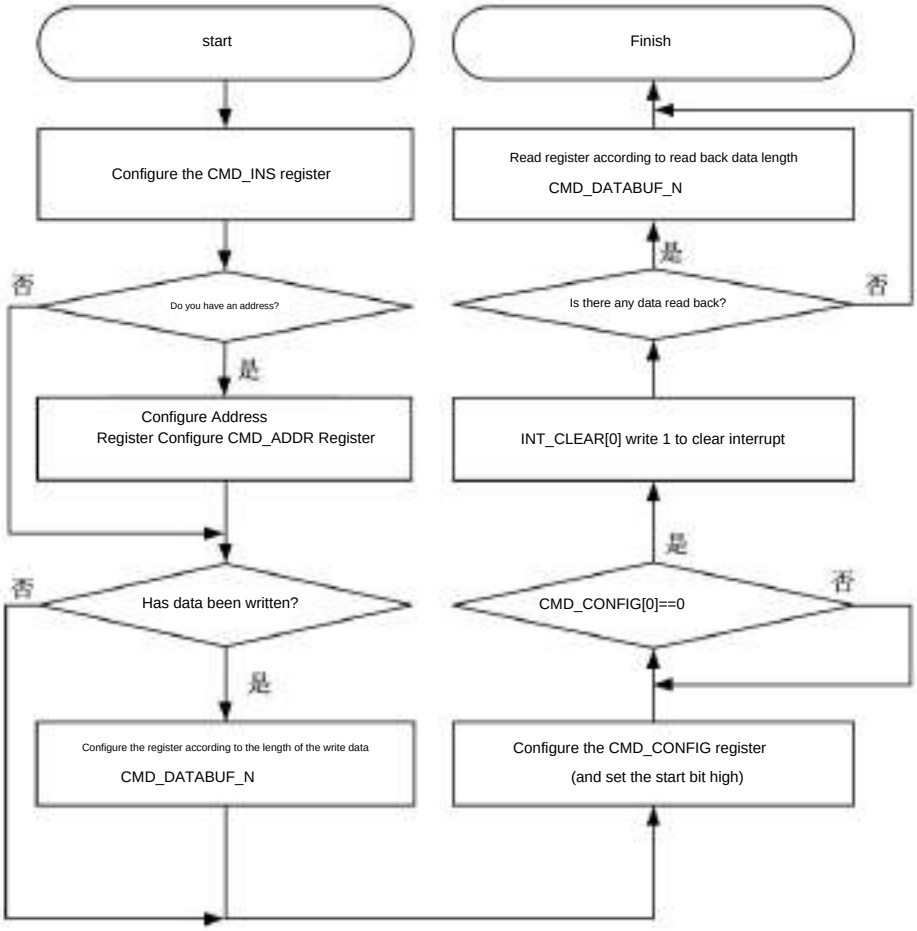
Figure 4-13 shows the operation process of writing Flash through registers (interrupt mode).

Figure 4-13 Operation flow of writing Flash through registers (interrupt mode)



4.2.4.4 Other operation processes through registers

Figure 4-14 Other operation flow through register mode



4.2.4.5 Directly read and write Flash operation flow through AHB Slave

After power-on reset, the default configuration is Standard SPI timing mode. Flash can be read directly without additional configuration.

By default, writing Flash through AHB Slave is disabled. It is necessary to configure BUS_CONFIG1[wr_enable] to 1 to enable bus write operations.

If you need to adjust the bus read and write configuration, please refer to "4.2.4.1 Initialization Process".

4.2.4.6 Operation flow of reading and writing Flash via DMA

DMA operation flow:

1. If you need to adjust the timing configuration of the bus operation mode, please refer to the initialization process.

2. Configure the start address of the memory end, the start address of the Flash end (Flash offset address), and the data length of the DMA operation.

3. Configure the read and write directions.

4. Enable DMA operation (configuration register BUS_DMA_CTRL [start] is 1).

5. Wait for the dma_done interrupt trigger (interrupt mode) or poll the DMA operation to complete (BUS_DMA_CTRL [start] changes to to 0).

说明

During DMA operation, Flash register command operation can be carried out simultaneously.

During the DMA operation, the Flash can be directly accessed through the AHB Slave at the same time, but it is necessary to ensure that the configuration related to the bus operation is not modified in the middle.

----Finish

4.2.5 Register overview

The register overview is shown in Table 4-7 .

Table 4-7 SFC register overview (base address is 0x1001_0000)

offset address name		describe	page number
0x0100 GLOBAL_CONFIG global configuration register			4-89
0x0110	TIMING	Timing configuration register	4-90
0x0120 INT_RAW_STATUS interrupt raw status register			4-90
0x0124	INT_STATUS	Masked Interrupt Status Register	4-91
0x0128 INT_MASK		interrupt mask register	4-92
0x012C INT_CLEAR		Interrupt Clear Register	4-92
0x01F8	VERSION	version register	4-93
0x01FC VERSION_SEL version selection register			4-94
0x0200	BUS_CONFIG1 bus operation mode configuration register 1		4-94
0x0204	BUS_CONFIG2 bus operation mode configuration register 2		4-96
0x0210	BUS_FLASH_SIZE Bus operation mode mapping size register		4-96
0x0214	CS0_BUS_BASE_A DDR	Chip select 0 bus operation mode mapping base address register	4-97
0x0218	CS1_BUS_BASE_A DDR	Chip Select 1 Bus Operation Mode Mapping Base Address Register	4-97
0x021C BUS_ALIAS_ADDR Bus operation mode Alias mapping base address register 4-98			
0x0240 BUS_DMA_CTRL DMA operation control register			4-98
0x0244 BUS_DMA_MEM_S ADDR		DMA operation DDR start address register	4-99
0x0248 BUS_DMA_FLASH_ SADDR		DMA operation Flash start address register	4-100

offset address	name	describe	page number
0x024C	BUS_DMA_LEN	DMA operation handling data length register	4-100
0x0250	BUS_DMA_AHB_CTRL	DMA operation AHB burst operation control register	4-100
0x0300	CMD_CONFIG	command operation mode configuration register	4-101
0x0308	CMD_INS	Command Operation Mode Instruction Register	4-103
0x030C	CMD_ADDR	Command operation mode address register	4-103
0x0400+4xN	CMD_DATABUF_N	command operation mode data Buffer register N	4-103

4.2.6 Register description

GLOBAL_CONFIG

GLOBAL_CONFIG is the global configuration register.

Offset Address	Register Name	Total Reset Value
0x0100	GLOBAL_CONFIG	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:3]	RW	reserved	reserve. Must write 0.
[2]	RW	flash_addr_mode	SPI address mode 0ÿ3Bytes address mode (default)ÿ 1ÿ4Bytes address modeÿ Writing is invalid when CMD.start is 1.
[1]	RW	wp_en	Hardware write protection is enabled, after setting to 1, the WP pin is forcibly pulled low. 0: Disable hardware write protection 1: Enable hardware write protection

[0] RW mode			SPI mode setting. 0: Support Mode0; 1: Support Mode3.

TIMING

TIMING configures the register for Timing.

Offset Address	Register Name	Total Reset Value
0x0110	TIMING	0x0000_660F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			tcsh	reserved			tcss			reserved				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	tcsh	Set the hold time for chip selection. 000~111: n+1 clock cycles. n is 0, 1, 2, . . . , 7.
[11]	RW	reserved	reserve.
[10:8]	RW	tcss	Set the setup time of chip selection. 000~111: n+1 clock cycles. n is 0, 1, 2, . . . , 7.
[7:4]	RO	reserved	reserve
[3:0]	RW	tshsl	Set the Deselect time of chip selection, which is equivalent to the time interval between two Flash operations. 0000~1111: n+2 clock cycles. n is 0, 1, 2, ..., 15.

INT_RAW_STATUS

INT_RAW_STATUS is the interrupt raw status register.

Offset Address	Register Name	Total Reset Value
0x0120	INT_RAW_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	dma_done_int_raw	DMA operation complete interrupt raw state (unmasked). 0: operation not done; _status 1: Operation completed.
[0]	RO	cmd_op_end_raw_	The instruction operation ends the raw interrupt state (unmasked). 0: operation not completed; status 1: Operation completed.

INT_STATUS

INT_STATUS is the masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0124	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.

[1]	RO	dma_done_int_stat 0: us	DMA operation complete interrupt raw state (masked). operation not completed; 1: Operation completed.
[0]	RO	completed; cmd_op_end_status 1:	The instruction operation ends the interrupt state (masked). 0: The operation has not been The operation has been completed.

INT_MASK

INT_MASK is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0128	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RW	bit. dma_done_int_mas 0:	DMA operation complete interrupt mask mask interrupt; k 1: Do not mask interrupts.
[0]	RW	bit. cmd_op_end_int_m 0:	Instruction operation end interrupt mask mask interrupt; ask 1: Do not mask interrupts.

INT_CLEAR

INT_CLEAR is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x012C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	WO	dma_done_int_clr	DMA operation complete interrupt clear bit, writing 1 to this bit will clear dma_done_status and dma_done_raw_status. 0: Do not clear interrupts; 1: Clear interrupt. This bit automatically returns to 0 after the clear operation is complete.
[0]	WHERE	cmd_op_end_int_cl r	0: Do not clear interrupt; 1: Clear interrupt. Instruction operation end interrupt clear bit, writing 1 to this bit will clear cmd_op_end_status and cmd_op_end_raw_status. This bit automatically returns to 0 after the clear operation is complete.

VERSION

VERSION is the version register.

Offset Address	Register Name	Total Reset Value
0x01F8	VERSION	0x0000_0350

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

Bits	Access Name		Description
[31:0]	RO	VERSION	SFC version number.

VERSION_SEL

VERSION_SEL is the version selection register.

Offset Address	Register Name	Total Reset Value
0x01FC	VERSION_SEL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	version_sel	Old and new register bank indication signal. 0: old register set; 1: New version register set.

BUS_CONFIG1

BUS_CONFIG1 is the bus operation mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0200	BUS_CONFIG1	0x8080_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			wr_ins								rd_ins																					
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	rd_enable	Bus read control, bus read data returns 0. 0: Disable bus read function. 1: Enable bus read function

[30] RW	wr_enable		Bus write control, bus write operation is ignored. 0: Disable bus write function. 1: Enable bus write function
[29:22] RW	wr_ins		write command
[21:19] RW	wr_dummy_bytes		Bus write operation DummyByte 0: no DummyByte 1ÿ1 Byte 2ÿ2 Bytes ... 7ÿ7 Bytes
[18:16] RW	wr_mem_if_type		The bus write operation specifies the connected SPI FLASH interface type. 000: Standard SPI interface type; 001ÿDual-Input/Dual-Output SPIÿ 010ÿDual-I/O SPIÿ 011ÿFull DIO SPIÿ 100ÿreservedÿ 101ÿQuad-Input/Dual-Output SPIÿ 110ÿQuad-I/O SPIÿ 111ÿFulll QIO SPIÿ
[15:8] RW	rd_ins		read command
[7:6] RW	rd_prefetch_cnt		Bus access Flash mode (non-fixed-length read) prefetch cycle. 00: No prefetch; (default) 01: Prefetch 1 clock cycle data; 10: Prefetch 2 clock cycle data; 11: Prefetch 3 clock cycle data.
[5:3] RW	rd_dummy_bytes		Bus read operation DummyByte. 0: no DummyByte; 1ÿ1 Byteÿ 2ÿ2 Bytesÿ ... 7ÿ7 Bytesÿ

[2:0]	RW	rd_mem_if_type	The bus read operation specifies the connected SPI FLASH interface type. 000: Standard SPI interface type; 001ÿDual-Input/Dual-Output SPIÿ 010ÿDual-I/O SPIÿ 011ÿFull DIO SPIÿ 100ÿreservedÿ 101ÿQuad-Input/Dual-Output SPIÿ 110ÿQuad-I/O SPIÿ 111ÿFulll QIO SPIÿ

BUS_CONFIG2

BUS_CONFIG2 configures register 2 for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x0204	BUS_CONFIG2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	reserved	reserve. Must write 0.

BUS_FLASH_SIZE

BUS_FLASH_SIZE is the map size register for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x0210	BUS_FLASH_SIZE	0x0000_0909

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	flash_size_cs1	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 0 1		

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.

[11:8]	RW	flash_size_cs1	Specify the capacity of SPI Flash connected to chip select 1. 0000: No SPI FLASH connected; 0001ÿ512Kbitÿ 0010ÿ1Mbitÿ 0011ÿ2Mbitÿ 0100ÿ4Mbitÿ 0101ÿ8Mbitÿ 0110ÿ16Mbitÿ 0111ÿ32Mbitÿ 1000ÿ64Mbitÿ 1001ÿ128Mbit(default)ÿ 1010ÿ256Mbitÿ 1011ÿ512Mbitÿ 1100ÿ1Gbitÿ 1101ÿ2Gbitÿ 1110ÿ4Gbitÿ 1111ÿ8Gbitÿ
[7:0]	RW	reserved	reserve.

CS0_BUS_BASE_ADDR

CS0_BUS_BASE_ADDR is the base address register for bus operation mode mapping.

Offset Address	Register Name	Total Reset Value
0x0214	CS0_BUS_BASE_ADDR	0x5A00_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cs0_bus_base_addr_high	reserved
Reset	0 1 0 1	1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cs0_bus_base_addr CS0 _high	flash is mapped to the system space base address.
[15:0]	RO	reserved	reserve.

CS1_BUS_BASE_ADDR

CS1_BUS_BASE_ADDR maps the base address register for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x0218	CS1_BUS_BASE_ADDR	0x5800_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cs1_bus_base_addr_high	reserved
Reset	0 1 0 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cs1_bus_base_addr_high	CS1 flash is mapped to the system space base address.
[15:0]	RO	reserved	reserve.

BUS_ALIAS_ADDR

BUS_ALIAS_ADDR is the Alias mapping base address register for the bus operation mode.

Offset Address	Register Name	Total Reset Value
0x021C	BUS_ALIAS_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flash_alias_addr	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	flash_alias_addr	Flash is mapped to the second base address of system space.
[15:0]	RO	reserved	reserve.

BUS_DMA_CTRL

BUS_DMA_CTRL is the DMA operation control register.

Offset Address	Register Name	Total Reset Value
0x0240	BUS_DMA_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	rw	[illegible]
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access Name	Description
[31:5] RO	reserved	reserve.
[4] RW reserved		DMA operations specify chip selects. 0: chip select 0 adopts DMA mode; 1: Chip select 1 adopts DMA mode.
[3:2] RO	reserved	reserve.
[1] RW rw		DMA read and write instructions. 0: Write operation (write to Flash). 1: Read operation (read from Flash).
[0] RW start		DMA transfer enable control. 0: No operation or operation complete. 1: Write 1 to enable DMA operation, read back 1 to indicate DMA operation in progress. Automatically returns to zero after DMA is completed.

BUS_DMA_MEM_SADDR

BUS_DMA_MEM_SADDR is the DDR start address register for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0244	BUS_DMA_MEM_SADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_mem_saddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RW	dma_mem_saddr	DMA operating system memory start address register. Must be aligned to 4bytes.

BUS_DMA_FLASH_SADDR

BUS_DMA_FLASH_SADDR is the flash start address register for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0248	BUS_DMA_FLASH_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_flash_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dma_flash_saddr	DMA operation Flash start address register.

BUS_DMA_LEN

BUS_DMA_LEN is the transfer data length register for DMA operation.

Offset Address	Register Name	Total Reset Value
0x024C	BUS_DMA_LEN	0x0000_0000

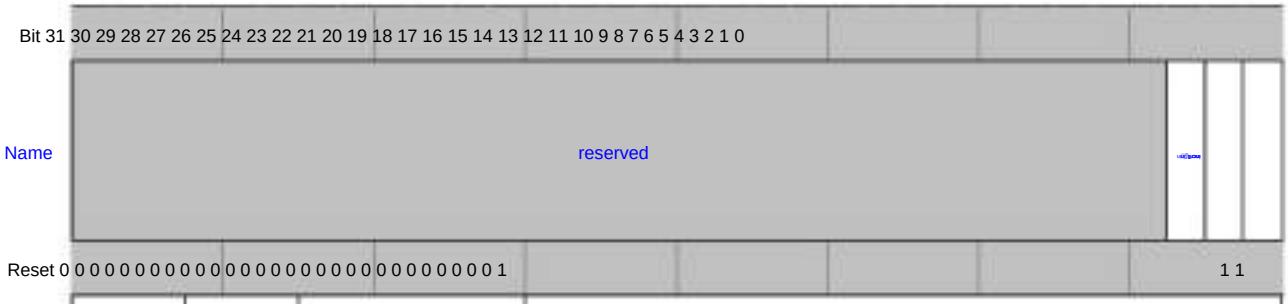
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	dma_len																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:30]	RW reserved	reserve.
[29:0]	RW dma_len	DMA operation data transfer length. Up to 256MB.

BUS_DMA_AHB_CTRL

BUS_DMA_AHB_CTRL is the AHB burst operation control register for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0250	BUS_DMA_AHB_CTRL	0x0000_0007

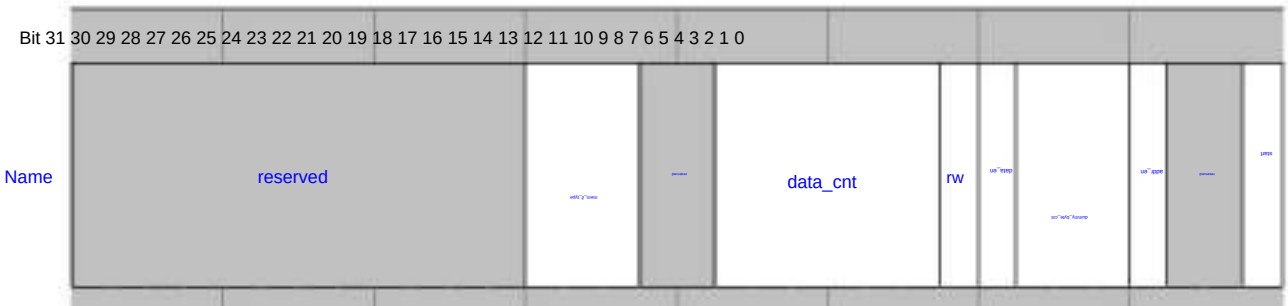


Bits	Access	Name	Description
[31:3]	RW	reserved	reserve.
[2]	RW	incr16_en	INC16 burst type enable. 0: Disabled. 1: enable.
[1]	RW	incr8_en	INC8 burst type enable. 0: Disabled. 1: enable.
[0]	RW	incr4_en	INC4 burst type enable. 0: Disabled. 1: enable.

CMD_CONFIG

CMD_CONFIG is the configuration register for the command operation mode.

Offset Address	Register Name	Total Reset Value
0x0300	CMD_CONFIG	0x0000_7E00



Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.

[19:17]	RW	mem_if_type	Specify the SPI FLASH interface type connected by the register command operation mode. 000: Standard SPI interface type; 001ÿDual-Input/Dual-Output SPIÿ 010ÿDual-I/O SPIÿ 011ÿFull DIO SPIÿ 100ÿreservedÿ 101ÿQuad-Input/Dual-Output SPIÿ 110ÿQuad-I/O SPIÿ 111ÿFulll QIO SPIÿ
[16:15]	RW	reserved	reserve. Must be written as 0.
[14:9]	RW	data_cnt	Read and write data length N+1Bytes.
[8]	RW	rw	To identify the data read and write of this operation, data_en needs to be 1. 0: write, there is sending data; 1: read, there is return data.
[7]	RW	data_en	Indicates whether there is data for this operation. 0: no data; 1: There is data.
[6:4]	RW	dummy_byte_cnt	The register command operation mode is DummyByte. 0: no DummyByte; 1ÿ1 Byteÿ 2ÿ2 Bytesÿ ... 7ÿ7 Bytesÿ
[3]	RW	addr_en	Whether there is an address for this operation. 0: no address; 1: There is an address.
[2]	RO	reserved	reserve.
[1]	RW	reserved	Chip select signal. 0: chip selection 0; 1: chip selection 1.
[0]	RW	start	Indicates the beginning of the instruction operation. 0: operation ended; 1: Start operation. This bit will automatically return to 0 after the operation is completed.

CMD_INS

CMD_INS is the instruction register of command operation mode.

Offset Address	Register Name	Total Reset Value
0x0308	CMD_INS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / REG_INS
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:8]	RO reserved	reserve.
[7:0]	RW REG_INS	Register access instruction code in Flash mode.

CMD_ADDR

CMD_ADDR is the command operation mode address register.

Offset Address	Register Name	Total Reset Value
0x030C	CMD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	— / cmd_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:30]	RO reserved	reserve.
[29:0]	RW cmd_addr	Register access operation address in Flash mode.

CMD_DATABUF_N

CMD_DATABUF_N is the data buffer register of command operation mode.

Offset Address	Register Name	Total Reset Value
0x0400+4xN	CMD_DATABUF_N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_databuf_n																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_databuf_n	The register accesses the Nth data Buffer in Flash mode. Register offset address 0x400+4xN. N is 0 to 15.

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5 Ethernet interface

5.1 ETH

5.1.1 Overview

The Ethernet module provides an Ethernet MAC to receive and send network interface data, can work in 10Mbit/s or 100Mbit/s mode, supports full-duplex or half-duplex working mode, and provides MII interface for the built-in PHY , provide RMII interface for off-chip, provide configurable 8 sets of DMAC address filtering table, can selectively filter and receive the input frame of the network port, and realize the function of limiting the flow of CPU port to protect the CPU from being attacked by large flow.

5.1.2 Functional description

The Ethernet module has the following features:

Support 1 Ethernet MAC. Support 10Mbit/
s or 100Mbit/s rate. Can work in full-duplex or half-duplex
mode. It supports external RMII interface and provides
MII interface for built-in PHY. Support collision fallback retransmission and late collision
in half-duplex mode.
Support the sending of flow control frames in full-duplex mode.
Supports frame length validity detection, and discards ultra-long frames and
ultra-short frames. Supports CRC check for input frames, and can discard frames with
check errors. Support adding CRC check to the
output frame. Support short frame
filling function. Support inner loopback and outer loopback in port full
duplex mode. Provide self-adaptive function to automatically obtain the working status of
the PHY chip. Provide MDIO interface, MDIO interface clock frequency can be
adjusted. Provides 64 common frame management queues for receiving
and sending. Provide flow limit function to prevent traffic attacks against CPU.
Supports statistical counting of received and sent frames.

Provide input buffer of 512byte and output buffer of 1536byte. Support 8

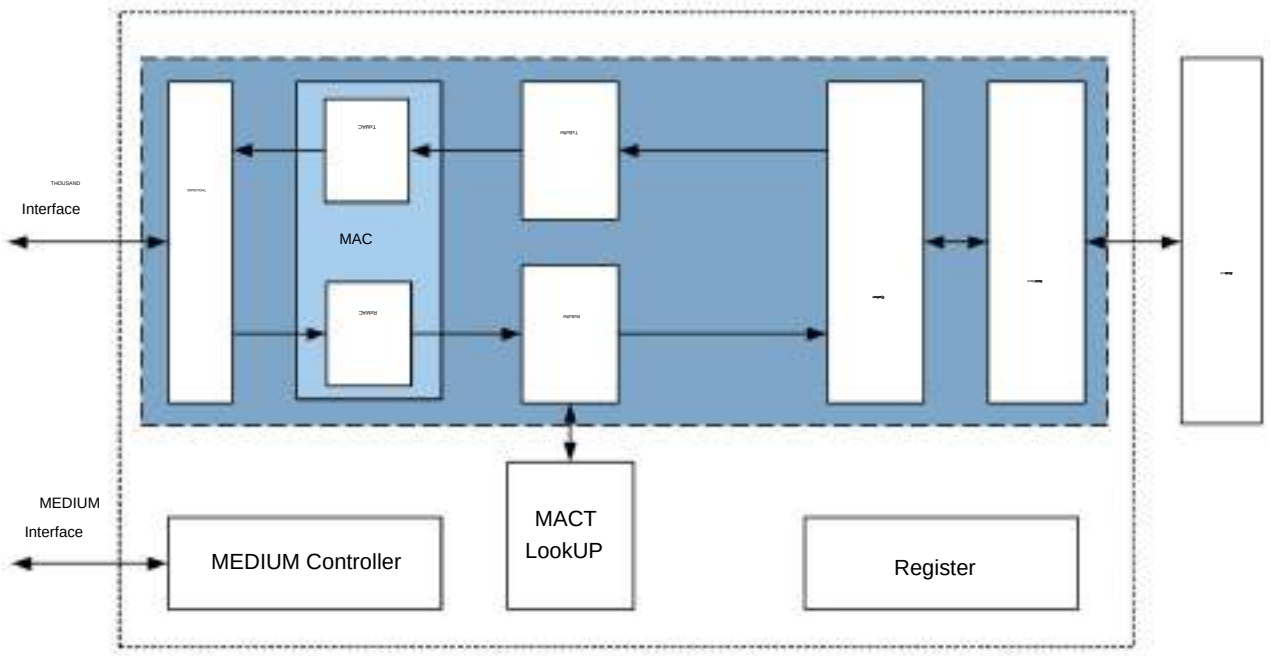
configurable DMAC address filtering tables.

For broadcast frames, multicast frames and unicast frames, it can be configured whether to forward or discard.

Support 802.3az (Energy Efficient Ethernet) for built-in PHY.

The logical block diagram of the Ethernet module is shown in Figure 5-1 .

Figure 5-1 Logic block diagram of Ethernet module



5.1.3 Signal description

The Ethernet interface signals are shown in Table 5-1 and Table 5-2 .

Table 5-1 MDIO interface signal description

Signal name	direction description		Corresponding pin
MDCK	O	MDIO interface clock output.	MDCK
MEDIUM	I/O	Input/output signal of MDIO interface. MDIO	

Table 5-2 MII interface signal description

Signal name	direction description		Corresponding pin
RMII_REF_CLK	I/O Uplink RMII interface reference clock.		RMII_REFCLK

Signal name	direction description		Corresponding pin
MII_TXCK	I	MII transmit data clock.	MII_TXCK
MII_TXD[3:0]/ RMII_TXD[3:0]	O	MII/RMII send data.	MII_TXD3ÿ MII_TXD0
MII_TXEN/ RMII_TXEN	O	MII/RMII send data valid.	MII_TXEN
MII_TXER	O	MII send data error flag	MII_TXER
MII_RXCK	I	The MII interface receives the data clock.	MII_RXCK
MII_RXD[3:0]/ RMII_RXD[1:0]	I	The MII/RMII interface receives data.	MII_RXD3ÿ MII_RXD0
MII_RXDV/ RMII_CRS_DV	I	MII/RMII interface receiving data is valid. MII_RXDV	
MII_RXER	I	MII interface receiving data error	MII_RXER
THOUSAND_CRS	I	MII interface carrier effective signal.	THOUSAND_CRS
THOUSANDS_COL	I	MII interface conflict signal.	THOUSANDS_COL

5.1.4 Working method

5.1.4.1 Frame receiving process

The software needs to complete the following operations during initialization:

The software needs to apply for the same number of buffers as the configured input queue depth, and the size of each buffer is 2KB, and then write the first address of the buffer into the frame input queue in sequence, and the number of times of writing should be exactly equal to the depth of the configured input queue. The

software needs to ensure that the configured buffer cannot be released when the frame is received. If the configured first address is a non-word-aligned address, it is necessary to ensure that the byte address corresponding to this address is a writable address.

When the CPU knows that there is a frame of data to be received, perform the following steps:

1. Read the frame descriptor in the register UD_GLB_IQFRM_DES (including the start address and frame length information of the input frame breath).
2. Process the data, and write 1 to clear GLB_IRQ_RAW[iraw_rx_up] to clear 0 (indicating that the CPU has finished receiving frames).

----Finish

After receiving one frame of data, the software needs to re-apply for a 2KB buffer, and rewrite the first address into the current input queue frame descriptor. Otherwise, the depth of the input queue that can be actually used is not equal to the value configured by the CPU, but equal to the number of buffers actually allocated by the CPU.

Table 5-3 shows the sub-data structure of CPU received frame description .

Table 5-3 CPU received frame description sub-data structure

bit name		describe
[63:32] rxfrm_saddr Start address of received frame.		
[31:18] reserved		
[17:12] fd_in_addr input queue (iq)		the relative address of the frame to be received, and store the absolute address as the frame Index value (0ÿiq_len–1).
[11:0] fd_in_len Input queue		frame length to be received.

说明

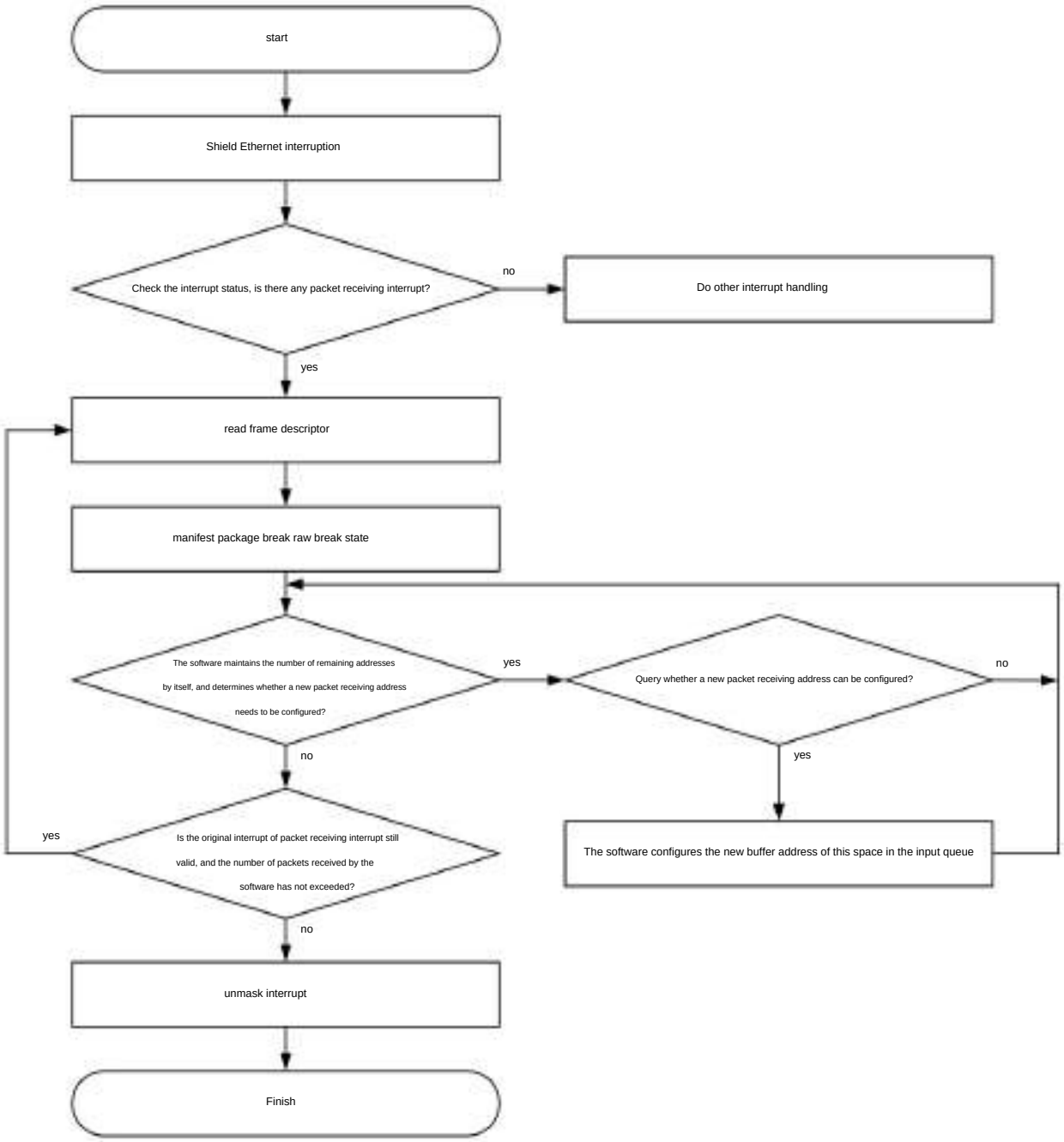
Query UD_GLB_ADDRQ_STAT to obtain the length of the receive queue.

The CPU can receive frames in interrupt mode or query mode.

a. Frame receiving in interrupt mode

When the CPU enables the frame reception interrupt, according to whether there is a frame to be received, the hardware will generate a frame reception interrupt (single-packet interrupt and multi-packet interrupt) int_rx_up (report 1 interrupt every time a 1 interrupt is reported when the number of packets is reached) to notify the CPU to receive the frame. The frame receiving process in interrupt mode is shown in Figure 5-2 .

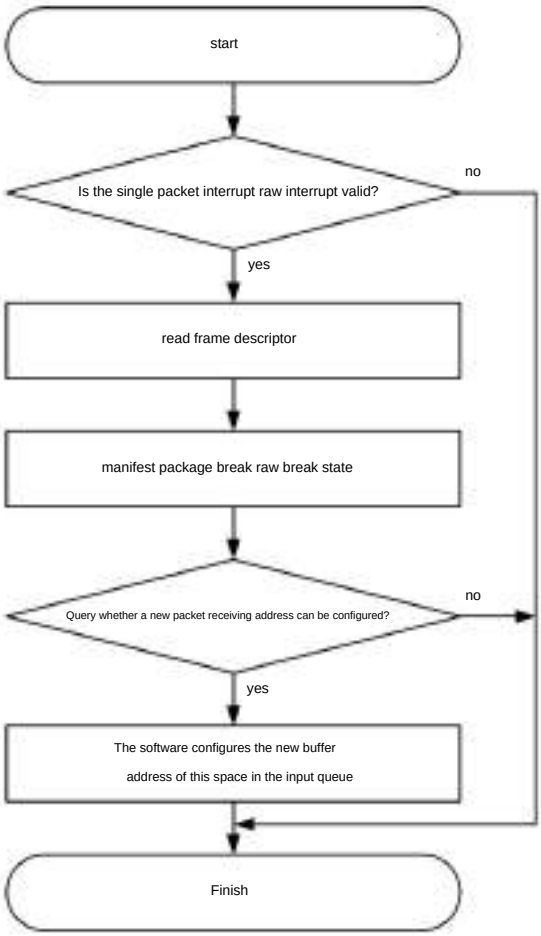
Figure 5-2 Flow chart of frame receiving in interrupt mode



b. Receive frames in query mode

The CPU does not enable the frame reception interrupt GLB_IRQ_ENA[ien_rx_up], and the CPU automatically queries GLB_IRQ_RAW[iraw_rx_up], which is 1, indicating that there is a frame that needs to be received by the CPU. The frame receiving process in query mode is shown in Figure 5-3 .

Figure 5-3 Frame receiving flow chart in query mode



5.1.4.2 Frame sending process

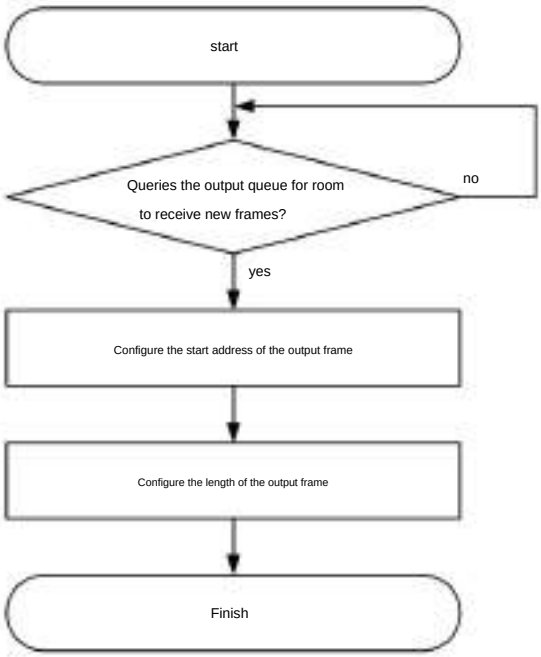
When the CPU has a frame to be sent, it judges whether the current queue has space to send. If there is space to send, write the first address and frame length of the frame Buffer to the frame descriptor of the output queue respectively. The CPU first writes the first address, and then writes the frame length of the sent frame. Writing the frame length of the sending frame triggers the hardware to write the first address and frame length information of the output frame into the output queue for sending. Therefore, the software should control that the frame length register cannot be written arbitrarily, and each write to this register will cause a data packet to be sent.

The frame format is as follows:

Destination MAC Source MAC		Type	Data	FCS

Figure 5-4 shows the frame sending process of the CPU .

Figure 5-4 CPU frame sending flow chart



When the frame sent by CPU is buffered in SDRAM, the frame descriptor is not included. Write the frame descriptor to UD_GLB_EQ_ADDR and UD_GLB_EQFRM_LEN, and notify Ethernet to enqueue the frame (descriptor). Table 5-4 shows the sub-data structure of CPU sending frame description .

Table 5-4 CPU send frame description sub-data structure

bit	name	describe
[42:11]	start_addr_eq	Send the first address of a frame.
[10:0]	fm_len	Frame length, unit: byte.

Note: Frames with fm_len less than 20byte and greater than 1900byte will be discarded, that is, the sending range is between 20 and 1900.

说明

Query UD_GLB_ADDRQ_STAT to get the current CPU send queue usage.

The CPU can send frames in interrupt mode or query mode.

a. Frame sending in interrupt mode

The CPU enables the Ethernet packet sending queue from not empty to empty interrupt (int_freeeq_up), and at the same time, it is set to allow the interrupt to notify the CPU. At this time, if the Ethernet output queue changes from not empty to empty, it means that the Ethernet can send frames, and the hardware generates an interrupt to notify the CPU, indicating that the CPU can send frames.

If software needs to send a frame, but the current output queue is full, software can enable this interrupt. When the output queue is empty, an interrupt is generated to notify the software to send the waiting frame. Software can use this interrupt to send a group of frames at a time while freeing the buffer for the last group of frames sent while the interrupt is asserted.

b. Send frame in query mode

The software checks its own internal sending frame count. If the count is less than the configured output queue length, it can directly notify the Ethernet of the frame to be sent, and at the same time establish a corresponding frame sending index table. The content of the index table item is written to the Ethernet output queue. Output frame start address. After the Ethernet sends a frame, the address of the output queue is used to inform the CPU to release the corresponding sending buffer, and the CPU finds the corresponding sending buffer through the address of the output queue and releases it.

5.1.4.3 Interrupt Management

Interrupt Status Register

Indicates the type of interrupt generated, see "GLB_IRQ_STAT" in "5.1.6.3 Global Control Register" for details.

interrupt enable register

Control whether to generate the corresponding interrupt, please refer to "GLB_IRQ_ENA" in "5.1.6.3 Global Control Register" for details.

If an interrupt is enabled, its interrupt status will be written to the corresponding interrupt status register.

Raw Interrupt Status Register

A certain type of raw interrupt can be read and sent to the CPU. For details, please refer to "GLB_IRQ_RAW" in "5.1.6.3 Global Control Register ".

Interrupt status clearing must clear the original interrupt of the interrupt, after the original interrupt is cleared, the interrupt status will be cleared automatically.

5.1.4.4 Flow Control

For the frames received by the software, when the frames received in the unit time interval exceed the upper limit of the software configuration, the subsequent received frames are selectively discarded according to the configuration. The software can be configured to discard broadcast frames, multicast frames or unicast frames after exceeding the traffic limit (configured through UD_GLB_FC_DROPCTRL). The flow limit threshold is set by UD_GLB_FC_RXLIMIT .

Software can configure the register UD_GLB_FC_TIMECTRL to set the time interval of flow limit. Using a 10bit time interval register, the maximum can be 1023 time granularities. The time interval granularity uses a 17bit counter to count the main clock, the default value is 100000, and the time granularity of the 100MHz main clock is 1ms. The software can configure (20bit register) the size of the flow limit upper limit value, if configured as 0, it means all receiving without flow limit.

5.1.4.5 Typical applications

clock gating

说明

When the ETH module is not in use, its clock can be shut down to reduce power consumption.

The steps to turn off the Ethernet clock are as follows:

1. Disable the link state of the port so that Ethernet cannot send and receive packets.

2. Clear the packet receiving queue of the port, so that there is no packet receiving interruption report on the Ethernet.

3. The software issues a command to reset the Ethernet logic, and the reset will not be canceled.

4. Set PERI_CRG51 [eth_cken] to 0 to turn off the Ethernet clock.

----Finish

The steps to turn on the Ethernet clock are as follows:

1. Hold reset without undoing. Set PERI_CRG51 [eth_cken] to 1 to enable Ethernet clock.

2. Set PERI_CRG51 [hrst_eth_s] to 0 to cancel the reset.

3. Turn on the link status of the port, and the Ethernet will resume normal operation.

----Finish

soft reset

The steps of Ethernet global soft reset are as follows:

1. Turn off the Ethernet port link status and packet receiving interrupt enable, so that the software cannot receive packets, and the software will no longer send packets.
Bag.

2. After the software finishes processing the current sending and receiving packets of the port, clear the sending and receiving packet queue, and at the same time, the queue length remains
the value before the soft reset, and the relevant pointers and queue count values return to 0.

3. Set PERI_CRG51 [hrst_eth_s] to 1, and issue the Ethernet soft reset command.

4. Set PERI_CRG51 [hrst_eth_s] to 0 to cancel the Ethernet soft reset.

5. If you want to start sending and receiving packets again, the software also needs to initialize the port sending and receiving packet queue.

6. Turn on the link status of the port, and the Ethernet will resume normal operation.

----Finish

initialization

The port initialization steps are as follows:

1. Configure the port status acquisition method.

Ethernet can adapt to the PHY working state or configure its working state by software. Configured at initialization time
UD_MAC_PORTSEL[stat_ctrl] to select:

When the configuration is 1, select the software to configure the working state of the port, and
execute 2. When the configuration is 0, select adaptive acquisition working status, go to 3.

Select the software to set the working state of the port when resetting.

2. Configure the working status and PHY chip working status.

If the working state of the configuration port is configured through software, the software needs to be configured according to the actual operating environment
The speed, connection status and duplex mode status information in UD_MAC_PORTSET , and configure these information into the relevant
registers of the PHY chip.

Ethernet provides MDIO interface to realize read and write control of PHY chip. When the software operates, the data,

The address of the PHY chip, register address and related control information are written into the MDIO_RWCTRL register, and then

MDIO_RWCTRL[finish] is found to be 1, indicating that the hardware has completed the read and write operations on the PHY chip. For specific configuration content, please refer to the data sheet of the relevant PHY chip.

After the configuration is complete, go to 4.

3. Configure the adaptive working state.

If the port is configured to obtain the working status of the PHY chip in an adaptive manner, it is necessary to specify the address of the PHY chip speed, duplex mode, connection register and the offset address in each register of these status bits. Realized by configuring UD_MDIO_ANEG_CTRL .

4. Receive and send frame queue depth setting.

Set the input queue depth and output queue depth in register UD_GLB_QLEN_SET :

The input queue depth indicates the maximum number of frames that can be buffered when receiving data.

The output queue depth indicates the maximum number of frames that can be buffered when sending data.

Since the input queue and output queue share 64 management spaces, the sum of the input queue depth and output queue depth cannot exceed 64, and the input queue depth and output queue depth must be at least 1. If the sum of the input queue depth and output queue depth set by the software is greater than 64, the item configured first by the software will be given priority, and the other item will be the result of subtracting the first configured item from 64.

In addition, you can set the multi-packet interrupt configuration register, set the register UD_GLB_IRQN_SET[int_frm_cnt] to configure how many packets to report a multi-packet interrupt, and configure the aging time register UD_GLB_IRQN_SET[int_timer].

5. Initialize the receive frame queue buffer.

After reset, the software needs to apply for the same number of buffers as the configured input queue depth, and the size of each buffer is 2KB, and then write the first address of the buffer into the frame input queue in sequence, and the number of times of writing should be exactly equal to the depth of the configured input queue.

6. Module soft reset.

Software configuration ETH module soft reset can reset the logic circuit and frame management queue inside Ethernet, so that the ETH module returns to the initialization state, but all registers inside Ethernet retain the value before soft reset. After the soft reset is released by the software, it is necessary to re-apply for the packet receiving buffer and initialize the input queue, otherwise the Ethernet cannot receive network packets.

说明

After Ethernet soft reset, the registers set by software will not change. For specific registers that can be soft reset, please refer to the description of each register.

----Finish

Interrupt frame receiving process

The steps to interrupt receiving frames are as follows:

1. After entering the interrupt handler, shield the Ethernet interrupt.

2. Check the interrupt status GLB_IRQ_STAT[int_rx_up] for frame receiving interrupt. If yes, go to 3; if not, go to other Ethernet interrupt processing.

3. Read the frame descriptor UD_GLB_IQFRM_DES, and read the corresponding length according to the frame head address corresponding to fd_in_addr (fd_in_len) frame data.

4. The list packet interrupt raw interrupt signal GLB_IRQ_RAW[iraw_rx_up] is 0, notifying the hardware that the reception is complete.

5. The software determines whether a new receiving address needs to be configured according to the number of remaining available addresses it maintains. if not required To configure, go to 8. Complete a package collection.

6. Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new packet receiving address can be configured. If unfit, then returns 5.

7. The software configures the new buffer address to the input queue through the register UD_GLB_IQ_ADDR . return 5.

8. Read and judge the single packet interrupt raw interrupt signal GLB_IRQ_RAW[iraw_rx_up]. If this bit is valid and the software If you can continue to receive packets (the number of packets received has not exceeded the limit), then return 3.

9. Unmask the Ethernet interrupt.

----Finish

Query frame receiving process

Disable the frame receive interrupt GLB_IRQ_ENA[ien_cpu_rx], the CPU automatically queries the single-packet interrupt raw interrupt signal GLB_IRQ_RAW[iraw_rx_up], if it is 1, it means there is a frame to receive.

The steps to query received frames are as follows:

1. Read single packet interrupt raw interrupt signal GLB_IRQ_RAW[iraw_rx_up]. If the bit is invalid, then directly end bundle.

2. Read the frame descriptor UD_GLB_IQFRM_DES, and read the corresponding length according to the frame head address corresponding to fd_in_addr (fd_in_len) frame data.

3. Write 1 to clear the single-packet interrupt raw interrupt signal GLB_IRQ_RAW[iraw_rx_up] to notify the hardware that the reception is complete.

4. Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new packet receiving address can be configured. if invalid, then Straight to the end.

5. The software configures the new buffer address to the input queue through the register UD_GLB_IQ_ADDR .

----Finish

Frame sending process

The steps to send a frame are as follows:

1. Read UD_GLB_ADDRQ_STAT[eq_in_rdy] to check if there is space left in the Ethernet output queue Receive a new send frame. If not, continue to wait and query.

2. Configure the first address UD_GLB_EQ_ADDR of the frame to be output .

3. Configure the length UD_GLB_EQFRM_LEN of the frame to be output. Complete the sending configuration of 1 frame.

----Finish

5.1.5 Register overview

MDIO Control Register

An overview of the MDIO control registers is shown in Table 5-5 .

Table 5-5 MDIO control register overview (base address is 0x1009_0000)

offset address name		describe	page number
0x1100	MDIO_RWCTRL	MDIO Command Word Register	5-16
0x1104	AVERAGE_RO_DATE	MDIO read data register	5-18
0x0108	UD_MDIO_PHYADDR	PHY Physical Address Register	5-18
0x010C	UD_MDIO_RO_STAT	PHY Chip Status Register	5-18
0x0110	UD_MDIO_ANEG_CTRL Offset address setting register for each state of the PHY chip		5-19
0x0114	UD_MDIO_RACE	Port Status Change Scan Mask Register 5-20	

MAC Control Register

An overview of the MAC control registers is shown in Table 5-6 .

Table 5-6 Overview of MAC Control Registers (base address is 0x1009_0000)

offset address name	describe	page number
0x0200 UD_MAC_PORTSEL	Port Working Status Control Register 5-21	
0x0204 UD_MAC_RO_STAT	Port Status Register	5-22
0x0208 UD_MAC_PORTSET	Port Setting Working Status Register 5-23	
0x020C UD_MAC_STAT_CHANGE port status change indication register 5-23		
0x0210 UD_MAC_SET	MAC function setting register	5-24
0x0480 UD_MAC_EEE_INT	EEE Raw Interrupt Register	5-26
0x0484 UD_MAC_EEE_INTEN	EEE Interrupt Enable Register	5-27
0x0488 UD_MAC_EEE_ENA	EEE Enable Register	5-28
0x048C UD_MAC_EEE_TIMER	EEE timing controller	5-29
0x0490 UD_MAC_EEE_LINK_STATUS EEE link status configuration		5-29

offset address	name	describe	page number
0x0494	UD_MAC_EEE_CLK_CNT	EEE timing unit counter	5-30

Global Control Register

An overview of the Ethernet global control registers is shown in Table 5-7 .

Table 5-7 Overview of global control registers (base address is 0x1009_0000)

offset address	name	describe	page number
0x1300	GLB_HOSTMAC_L32	The lower 32bit register of the local MAC address	5-30
0x1304	GLB_HOSTMAC_H16	The high 16bit of the local MAC address register	5-31
0x1308	GLB_SOFT_RESET	Internal Soft Reset Register	5-31
0x1310	GLB_FWCTRL	Forwarding Control Register	5-32
0x1314	GLB_MACTCTRL	MAC Filter Table Control Register	5-33
0x1318	GLB_ENDIAN_MOD	endian control register	5-34
0x1330	GLB_IRQ_STAT	Interrupt Status Register	5-34
0x1334	GLB_IRQ_ENA	interrupt enable register	5-36
0x1338	GLB_IRQ_RAW	raw interrupt register	5-38
0x1400	GLB_MAC0_L32	MAC filter 0	5-39
0x1404	GLB_MAC0_H16	MAC filter 0	5-40
0x1408	GLB_MAC1_L32	MAC filter 1	5-41
0x140C	GLB_MAC1_H16	MAC filter 1	5-41
0x1410	GLB_MAC2_L32	MAC filter 2	5-42
0x1414	GLB_MAC2_H16	MAC filter 2	5-42
0x1418	GLB_MAC3_L32	MAC filter 3	5-43
0x141C	GLB_MAC3_H16	MAC filter 3	5-43
0x1420	GLB_MAC4_L32	MAC filter 4	5-44
0x1424	GLB_MAC4_H16	MAC filter 4	5-44
0x1428	GLB_MAC5_L32	MAC filter 5	5-45
0x142C	GLB_MAC5_H16	MAC filter 5	5-45

offset address	name	describe	page number
0x1430	GLB_MAC6_L32	MAC filter 6	5-46
0x1434	GLB_MAC6_H16	MAC filter 6	5-47
0x1438	GLB_MAC7_L32	MAC filter 7	5-47
0x143C	GLB_MAC7_H16	MAC filter 7	5-48
0x0340	UD_GLB_IRQN_SET	Multipacket Interrupt Configuration Register	5-48
0x0344	UD_GLB_QLEN_SET	Queue Length Configuration Register	5-49
0x0348	UD_GLB_FC_LEVEL	flow control register	5-50
0x034C	UD_GLB_CAUSE	The message is sent to the Cause register of the CPU	5-50
0x0350	UD_GLB_RXFRM_SADDR Input frame start address register		5-51
0x0354	UD_GLB_IQFRM_DES Input Frame Descriptor Subregister		5-51
0x0358	UD_GLB_IQ_ADDR	Input frame first address register	5-52
0x035C	UD_GLB_BFC_STAT	Forwarding cache flow control status and multi-packet interrupt aging time counter	5-53
0x0360	UD_GLB_EQ_ADDR	Output Queue Head Address Register	5-53
0x0364	UD_GLB_EQFRM_LEN Output Queue Frame Length Configuration Register		5-54
0x0368	UD_GLB_QSTAT	Queue Status Register	5-54
0x036C	UD_GLB_ADDRQ_STAT Address Queue Status Register		5-55
0x0370	UD_GLB_FC_TIMECTRL Flow Limit Time Configuration Register		5-56
0x0374	UD_GLB_FC_RXLIMIT Flow Limit Watermark Configuration Register		5-56
0x0378	UD_GLB_FC_DROPCTRL Flow Limit Packet Drop Control Register		5-57

Statistical Count Control Register

Table 5-8 shows an overview of the statistical counting control registers .

Table 5-8 Overview of statistical counting control registers (base address is 0x1009_0000)

offset address	name	describe	page number
0x0584	UD_STS_PORTCNT Port Section Status Counter		5-58
0x05A0	UD_PORT2CPU_PKTS CPU received total packets register		5-58

offset address	name	describe	page number
0x05A4	UD_CPU2IQ_ADDRCNT CPU configuration receiving address queue times register		5-59
0x05A8	UD_RX_IRQCNT	Report single packet interrupt times register	5-59
0x05AC	UD_CPU2EQ_PKTS	The total number of packets sent by the CPU to the sending port register	5-59

Statistics result register

Table 5-9 shows the overview of statistical result registers .

Table 5-9 Overview of statistical result registers (base address is 0x1009_0000)

offset address	name	describe	page number
0x0600	UD_RX_DVCNT	RXDV Rising Edge Count Register	5-60
0x0604	UD_RX_OCTS	Total Bytes Received Registers	5-60
0x0608	UD_RX_RIGHTOCTS Register the total number of bytes of received correct packets device		5-61
0x060C	UD_HOSTMAC_PKTS Match the number of packets sent by the local MAC memory		5-61
0x0610	UD_RX_RIGHTPKTS Port Received Total Packets Register		5-62
0x0614	UD_RX_BROADPKTS Correct Broadcast Packets Register		5-62
0x0618	UD_RX_MULTPKTS Correct multicast packet number register		5-62
0x061C	UD_RX_UNIPKTS	Correct Unicast Packet Count Register	5-63
0x0620	UD_RX_ERRPKTS	Error packet total packet number register	5-63
0x0624	UD_RX_CRCERR_PKTS CRC Error Times Register		5-64
0x0628	UD_RX_LENERR_PKTS Invalid Packet Length Register		5-64
0x062C	UD_RX_OCRCERR_PKTS Odd number of Nibble CRC error packets register		5-64
0x0630	UD_RX_PAUSE_PKTS Received flow control packets register		5-65
0x0634	UD_RF_OVERCNT	RXFIFO Overflow Count Register	5-65
0x0638	UD_FLUX_TOL_IPKTS The total number of packets sent by the traffic limit entrance memory		5-66

offset address	name	describe	page number
0x063C	UD_FLUX_TOL_DPKTS	The total number of packets dropped by the flow limit memory	5-66
0x064C	UD_MN2CPU_PKTS	Due to MAC restrictions not forwarded to Packet Count Register for CPU Port	5-66
0x0780	UD_TX_PKTS	Register 5-67 of the total number of packets sent successfully	
0x0784	UD_TX_BROADPKTS	Register the number of successfully sent broadcast packets device	5-67
0x0788	UD_TX_MULTPKTS	Register the number of successfully sent multicast packets device	5-68
0x078C	UD_TX_UNIPKTS	Successfully sent unicast packet count register	5-68
0x0790	UD_TX_OCTS	Total Bytes Sent Register 5-68	
0x0794	UD_TX_PAUSE_PKTS	Number of Flow Control Frames Transmitted Register 5-69	
0x0798	UD_TX_RETRYCNT	The total number of retransmissions sent during sending memory	5-69
0x079C	UD_TX_COLCNT	Total Number of Collisions Register 5-69	
0x07A0	UD_TX_LC_PKTS	LateCollision occurred packet number register	5-70
0x07A4	UD_TX_COLOK_PKTS	The number of packets with conflicts but successfully sent register	5-70
0x07A8	UD_TX_RETRY15_PKTS	retransmission over 15 discarded packets register	5-71
0x07AC	UD_TX_RETRYN_PKTS	The number of packets whose collision times are equal to the field value register	5-71

5.1.6 Register description

5.1.6.1 MDIO Control Register

MDIO_RWCTRL

MDIO_RWCTRL is the MDIO command word register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1100	MDIO_RWCTRL	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cpu_data_in	MDIO module writes data to PHY. When performing a write operation, the CPU first writes the 16-bit data to be written into the MDIO into this register.
[15]	RW	finish	The PHY read/write operation is complete. 0: not completed; 1: Done. When the second read/write operation is to be performed, the CPU must first clear this bit to 0.
[14]	RO	reserved	reserve.
[13]	RW	rw	Controls whether access to the PHY is read or write. 0: read operation; 1: Write operation.
[12:8]	RW	phy_exaddr	The corresponding external physical address of the PHY for external operations. 1 MDIO can read and write access to multiple external PHYs. Each PHY has 1 corresponding address. When only one PHY chip is connected externally, the configuration value is consistent with the values of registers UD_MDIO_PHYADDR[phy0_addr] and UD_MDIO_PHYADDR[phy1_addr].
[7:5]	RW	frq_dv	The frequency division factor of MDCK (MDIO interface clock) when reading and writing to the external PHY. Taking the main clock frequency of 54MHz as an example, the relationship between frq_dv and MDC frequency is as follows: 000: Divide the main clock by 50, and the frequency after division is 1.1MHz; 001: Divide the main clock by 100, and the frequency after division is 552KHz; 010: Divide the main clock by 150, and the frequency after division is 552KHz; The frequency is 368 KHz; 011: Divide the main clock by 200, and the frequency after division is 276 KHz; 100: Divide the frequency of the working main clock by 250, and the frequency after frequency division is 221 KHz; 101: Divide the main clock by 300, and the frequency after division is 184 KHz; 110: Divide the main clock by 350, and the frequency after division is 158 KHz; 111: Divide the main clock by 400, the frequency after division is 184 KHz; The latter frequency is 138 KHz.

[4:0] RW	phy_inaddr		The internal register address of the externally operated PHY chip is represented by a 5-bit binary number.

AVERAGE_RO_DATE

MDIO_RO_DATAMDIO is the read data register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1104	AVERAGE_RO_DATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cpu_data_out
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	cpu_data_out	The data register used for the MDIO module to read the PHY, write the 16bit data read from the PHY into this register first.

UD_MDIO_PHYADDR

UD_MDIO_PHYADDR is the PHY physical address register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0108	UD_MDIO_PHYADDR	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	phy_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:0]	RW	phy_addr	The external physical address of the externally connected PHY chip.

UD_MDIO_RO_STAT

UD_MDIO_RO_STAT is to obtain the PHY chip status register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x010C	UD_MDIO_RO_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2]	RO	speed_mdio2mac	The working state of the port speed obtained from the MDIO interface is in 10Mbit/s or 100Mbit/s working mode. 0: 10Mbit/s working mode; 1: 100Mbit/s working mode.
[1]	RO	link_mdio2mac	Port link status obtained from MDIO interface. 0: no link; 1: link.
[0]	RO	duplex_mdio2mac	Port duplex working status obtained from MDIO interface. 0: half duplex; 1: Full duplex.

UD_MIDDLE_ANEG_CTRL

UD_MDIO_ANEG_CTRLPHY is the offset address setting register for each state of the chip. This register does not support soft reset.

说明

If the speed status of the PHY chip is located in bit[14] of the register whose address is 17, you can configure internal_addr_speed as 0x11 and speed_index as 0xE, then you can read this bit value through the MDIO interface as the current speed mode information of the PHY .

Offset Address	Register Name	Total Reset Value
0x0110	UD_MIDDLE_ANEG_CTRL	0x0463_1EA9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												internal_addr_link										speed_index					link_index			duplex_index		
Reset	0	0	0	0	0	1	0	0	0	1			1	0	0	0	1				1	0	0	0	1				1	0	1	0	0	1

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:22]	RW	internal_addr_speed	The address of the register where the PHY chip stores state information (speed). The default value is set according to Intel 9785.
[21:17]	RW	internal_addr_link	The address of the register where the PHY chip stores state information (link). The default value is set according to Intel 9785.
[16:12]	RW	internal_addr_dupl	The address of the register where the PHY chip stores state information (duplex). The default value is set according to Intel 9785.
[11:8]	RW	speed_index	The offset address where the speed information is stored in the PHY chip status register. The default value is set according to Intel 9785.
[7:4]	RW	link_index	The offset address where the link information is stored in the PHY chip status register. The default value is set according to Intel 9785.
[3:0]	RW	duplex_index	The offset address where the duplex information is stored in the PHY chip status register. The default value is set according to Intel 9785.

UD_MDIO_RACE

UD_MDIO_IRQENA is the port status change scan mask register. This register does not support soft reset.

说明

If the PHY status information connected to the port cannot be obtained by scanning through UD_MDIO_ANEG_CTRL , the user can scan the PHY status register through MDIO_RWCTRL to obtain whether the port status has changed, and generate an interrupt to notify the software for

processing. The link_partner state change refers to the change of any one of the link, speed, and duplex of the PHY state.

Offset Address	Register Name	Total Reset Value
0x0114	UD_MDIO_RACE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	link_partner_ch_m 0:	Port link partner status scan change interrupt mask. shield; ask 1: No shielding.
[2]	RW	speed_ch_mask	Port speed mode scan change interrupt mask. 0: shielded; 1: No shielding.
[1]	RW	link_ch_mask	Port connection mode scan change interrupt mask. 0: shielded; 1: not shielded.
[0]	RW	duplex_ch_mask	Port duplex mode scan change interrupt mask. 0: shielded; 1: No shielding.

5.1.6.2 MAC Control Register

The MAC control register is a port control register. When the port status is valid, a soft reset is required after configuring the MAC control register.

OUT_MAC_PORTSEL

UD_MAC_PORTSEL is the port working state control register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0200	OUT_MAC_PORTSEL	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	mii_rmii	Port interface mode selection. 0: MII connector; 1: RMII interface.
[0]	RW	stat_ctrl	Port working state information selection control register. 0: Use the status information obtained from the MDIO interface; 1: Use the status information set by the CPU.

UD_MAC_RO_STAT

UD_MAC_RO_STAT is the port status register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0204	UD_MAC_RO_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RO	speed_stat	The current speed mode of the port. 0: 10Mbit/s mode; 1: 100Mbit/s mode.
[1]	RO	link_stat	The current link status of the port. 0: no link; 1: There is a link.

[0]	RO	duplex_stat	The current duplex mode of the port. 0: half duplex; 1: Full duplex.

OUT_MAC_PORTSET

UD_MAC_PORTSET Sets the working status register for the port. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0208	OUT_MAC_PORTSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2]	RW	speed_stat_dio	The CPU sets the port speed mode. 0: 10Mbit/s mode; 1: 100Mbit/s mode.
[1]	RW	link_stat_dio	The CPU sets the port link state. 0: no link; 1: link.
[0]	RW	duplex_stat_dio	The CPU sets the port duplex mode. 0: half duplex; 1: Full duplex.

UD_MAC_STAT_CHANGE

UD_MAC_STAT_CHANGE is the port status change indication register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x020C	UD_MAC_STAT_CHANGE	0x0000_0000

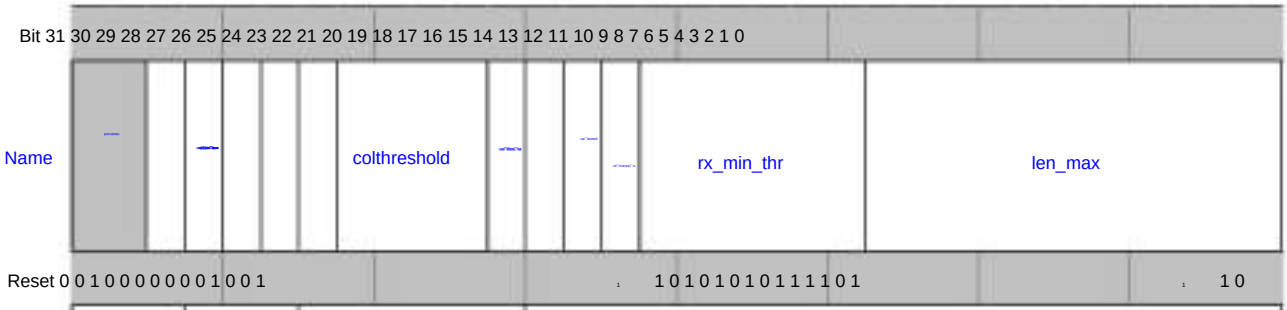
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	WC	speed_stat_ch	Port speed mode change indication. 0: no change; 1: change. Write 1 to clear this register.
[1]	WC	link_stat_ch	Port link state change indication. 0: no change; 1: change. Write 1 to clear this register.
[0]	WC	duplex_stat_ch	Port duplex mode change indication. 0: no change; 1: change. Write 1 to clear this register.

OUT_MAC_SET

UD_MAC_SET is the MAC function setting register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0210	OUT_MAC_SET	0x2027_55EE



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RW	add_path_en	Automatically add PAD enable when the port sends. 0: forbidden; 1: enable.
[28]	RW	crcgen_dis	Port CRC generation inhibit control. 0: Output frame recalculates CRC; 1: Output frame does not recalculate CRC.
[27]	RW	cntr_rdclr_en	Port statistics counter read clear enable. 0: forbidden; 1: enable.
[26]	RW	cntr_clr_all	Port statistics counter clearing control. 0: do not clear; 1: Clear. Note: If **cntr_clr_all** is 1, it needs to be set to **0** and then set to **1** in the next full clear to perform the full clear operation.
[25]	RW	cntr_roll_dis	Port statistics acyclic count enable. 0: forbidden; 1: enable.
[24:21]	RW	colthreshold	Statistical threshold of the number of port conflicts. The default is 0x1, which means the number of frames with one conflict.
[20]	RW	in_loop_en	Port inloop is enabled. 0: forbidden; 1: enable. Note: Outer loopback and inner loopback cannot be enabled at the same time. When the network port is in normal working state, it is necessary to perform a soft reset on the module after the internal and external loopback configurations are changed.

[19] RW ex_loop_en			Port outloop is enabled. 0: forbidden; 1: enable. Note: Outer loopback and inner loopback cannot be enabled at the same time. When the network port is in normal working state, it is necessary to perform a soft reset on the module after the internal and external loopback configurations are changed.
[18] RW pause_en			Port flow control frame transmission is enabled. 0: forbidden; 1: enable.
[17] RW rx_shframe_en			The port short frame reception is enabled. 0: forbidden; 1: enable. **Note: When rx_shframe_en** is set to **1 ,** the minimum frame length allowed to be received by the port is **the rx_min_thr configuration frame length; when rx_shframe_en** is set to **0 ,** the minimum frame length allowed to be received by the port defaults to **64 bytes (including CRC).**
[16:11] RW rx_min_thr			The minimum frame size the port allows to receive. The value range is 42byte to 63byte, and the default is 42byte. Note: If **the rx_min_thr** configuration value is less than 42, the value will be **42.**
[10:0] RW len_max			The maximum frame length that the port allows to receive, the default is 1518byte. The value range is 1518byte to 1535byte. Note: If **the len_max** configuration is greater than 2000, the value will be **2000; if the len_max** configuration is less than 256, the value will be **256.**

UD_MAC_EEE_INT

UD_MAC_EEE_INT is the EEE raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0480	UD_MAC_EEE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	tx_entry_start	ETH TX direction allows access to LPI's raw interrupts. 0: no interrupt; 1: There is an interrupt.
[3]	RO	rx_leave_lpi	Raw interrupt for exiting LPI in RX direction. 0: no interrupt; 1: There is an interrupt.
[2]	RO	rx_entry_lpi	Raw interrupt for RX direction into LPI. 0: no interrupt; 1: interrupt.
[1]	RO	tx_leave_lpi	TX direction exits the original interrupt of LPI. 0: no interrupt; 1: There is an interrupt.
[0]	RO	tx_entry_lpi	Raw interrupt from TX direction into LPI. 0: no interrupt; 1: There is an interrupt.

OUT_MAC_EEE_INTEN

UD_MAC_EEE_INTEN is the EEE interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0484	OUT_MAC_EEE_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:10]	RO	reserved	reserve.
[9]	RW	tx_entry_start_msk	ETH TX direction allows entry into LPI's raw interrupt mask
[8]	RW	rx_leave_lpi_msk	Raw interrupt mask for exiting LPI in RX direction
[7]	RW	rx_entry_lpi_msk	RX direction enters the original interrupt mask of LPI
[6]	RW	tx_leave_lpi_msk	TX direction exits the original interrupt mask of LPI
[5]	RW	tx_entry_lpi_msk	TX direction enters the original interrupt mask of LPI
[4]	RO	tx_entry_start_en	ETH TX direction allows entry to LPI's raw interrupt enable
[3]	RO	rx_leave_lpi_en	RX direction exits the original interrupt enable of LPI
[2]	RO	rx_entry_lpi_en	RX direction enters the raw interrupt enable of LPI
[1]	RO	tx_leave_lpi_en	TX direction exits the original interrupt enable of LPI
[0]	RO	tx_entry_lpi_en	TX direction enters the raw interrupt enable of LPI

UD_MAC_EEE_ENA

UD_MAC_EEE_ENA is the EEE enable register.

Offset Address	Register Name	Total Reset Value
0x0488	UD_MAC_EEE_ENA	0x00F4_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eee_ls_timer																															
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	LS_TIMER
[3:2]	RW	reserved	reserve.
[1]	RW	eee_assert	EEE enters the configuration.
[0]	RW	eee_enable	EEE enable switch.

UD_MAC_EEE_TIMER

UD_MAC_EEE_TIMER is the TIMER register that EEE needs to set.

Offset Address	Register Name	Total Reset Value
0x048C	UD_MAC_EEE_TIMER	0x001E_2710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_wk_timer																lpi_cond_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	tx_wk_timer	TX_WK_TIMER
[15:0]	RW	lpi_cond_timer	LPI_COND_TIMER

UD_MAC_EEE_LINK_STATUS

UD_MAC_EEE_LINK_STATUS is the network port link status register specially set for EEE.

Offset Address	Register Name	Total Reset Value
0x0490	UD_MAC_EEE_LINK_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	reserve.
[2]	RW	auto_eee	No software participation is required, and the EEE process is automatically controlled by logic.
[1]	RW	eee_tx_press	The back pressure data flow in the TX direction makes the exit process of EEE conform to the time requirement of wk_timer in 802.3az.
[0]	RW	phy_link_status	PHY link status.

UD_MAC_EEE_CLK_CNT

UD_MAC_EEE_CLK_CNT is the EEE clock unit counter.

Offset Address	Register Name	Total Reset Value
0x0494	UD_MAC_EEE_CLK_CNT	0x0000_0063

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	eee_clk_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 1

Bits	Access	Name	Description
[31:0]	RW	eee_clk_cnt	EEE clock unit counter.

5.1.6.3 Global Control Registers

GLB_HOSTMAC_L32

GLB_HOSTMAC_L32 is the lower 32bit register of the local MAC address. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1300	GLB_HOSTMAC_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	local_mac																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	local_mac	The lower 32 bits of the local MAC.

GLB_HOSTMAC_H16

GLB_HOSTMAC_H16 is the high 16bit register of the local MAC address. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1304	GLB_HOSTMAC_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																local_mac[47:32]															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	local_mac[47:32]	The upper 16 bits of the local MAC.

GLB_SOFT_RESET

GLB_SOFT_RESET is the internal soft reset register. This register does not support soft reset.

说明

All soft reset times must be kept above 2ms.

Offset Address	Register Name	Total Reset Value
0x1308	GLB_SOFT_RESET	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	soft_reset	Internal soft reset. 0: no reset; 1: Reset. After entering the soft reset state, if you want to cancel the soft reset, you need to set this bit to 0.

GLB_FWCTRL

GLB_FWCTRL is the forwarding control register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1310	GLB_FWCTRL	0x0000_0020

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	fwall2cpu_up	Whether all incoming valid frames of the port are forcibly forwarded to the CPU port. 0: No; 1: Yes.
[6]	RO	reserved	reserve.

[5] RW	fw2cpu_ena_up		Port input frame forwarding to CPU port enable. 0: forbidden; 1: enable.
[4:0] RO		reserved	reserve.

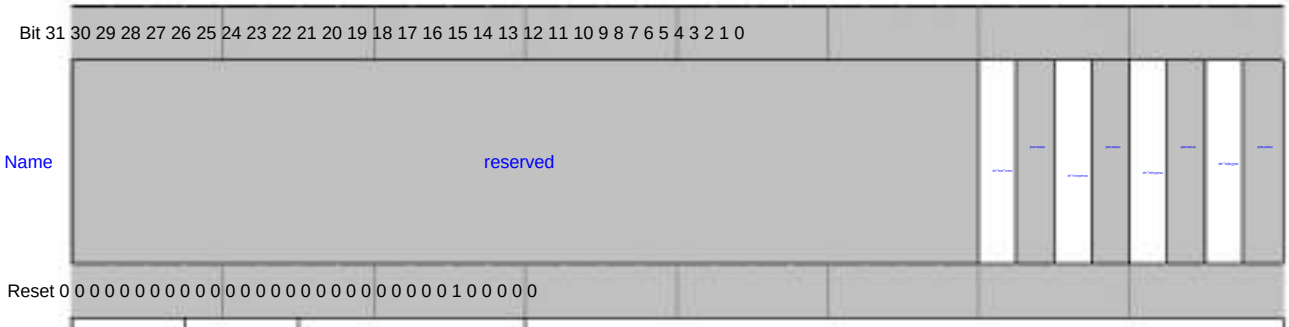
GLB_MACTCTRL

GLB_MACTCTRL is the MAC filter table control register. This register does not support soft reset.

说明

If the highest byte of the destination MAC address is an even number, it is a unicast frame. The highest byte of the destination MAC address is an odd number, which is a multicast frame. All bytes of the destination MAC address are all 0xFF are broadcast frames.

Offset Address	Register Name	Total Reset Value
0x1314	GLB_MACTCTRL	0x0000_0020



Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	mact_ena_up	General enable bit of all MAC filters on the port. 0: Do not use any MAC filter; 1: Use MAC filter.
[6]	RO	reserved	reserve.
[5]	RW	broad2cpu_up	Whether the broadcast frame input by the port is forwarded to the CPU port. 0: Do not forward to the CPU port; 1: Forward to CPU port.
[4]	RO	reserved	reserve.
[3]	RW	multi2cpu_up	Whether the multicast frames in the non-filtered table entered by the port are forwarded to the CPU port. 0: Do not forward to the CPU port; 1: Forward to CPU port.
[2]	RO	reserved	reserve.

[1] RW uni2cpu_up			Whether unicast frames in the unfiltered table entered by the port are forwarded to the CPU port. 0: Do not forward to the CPU port; 1: Forward to CPU port.
[0]	RO	reserved	reserve.

GLB_ENDIAN_MOD

GLB_ENDIAN_MOD is the big and small endian control register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1318	GLB_ENDIAN_MOD	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	in_edian	Receive packets and write SDRAM big and small endian configuration. 0: big-endian mode; 1: little-endian mode. Data is flipped byte by byte.
[0]	RW	out_edian	Send a packet to read SDRAM big and small endian configuration. 0: big-endian mode; 1: little-endian mode.

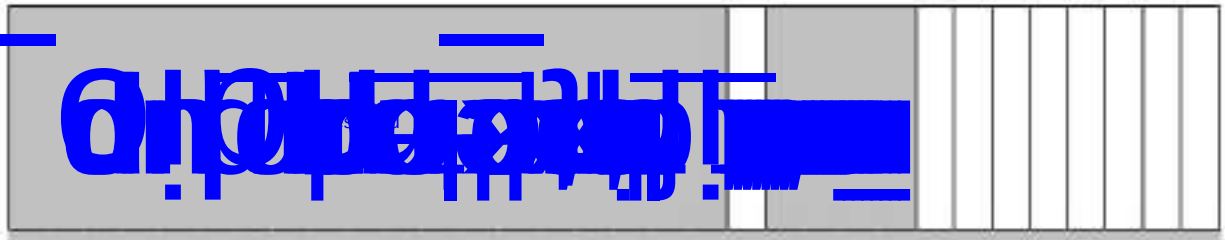
GLB_IRQ_STAT

GLB_IRQ_STAT is the interrupt status register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1330	GLB_IRQ_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name



Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

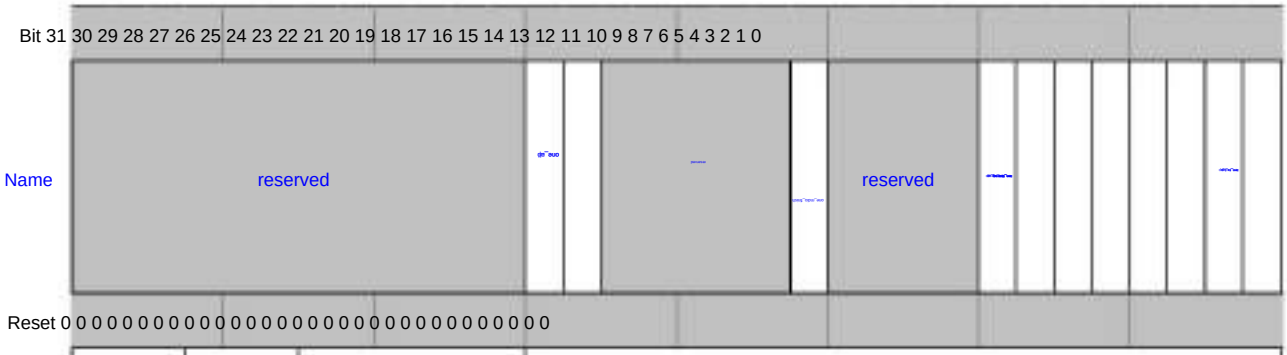
Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RO int_mdio_finish			MDIO Complete CPU operation instructions. 0: MDIO has not completed CPU operation; 1: MDIO has completed the CPU operation, generating an interrupt. After entering the interrupt program, query MDIO_RWCTRL[finish] to judge whether the MDIO operation is completed.
[11:8] RO		reserved	reserve.
[7]	RO	int_rxd_up	The port has (multiple) frames waiting for the CPU to receive an interrupt indication (multipacket interrupt). 0: Interrupt is invalid; 1: The interrupt is valid, and there are frames waiting for the CPU to receive in the input queue. When the interrupt occurs, it is necessary to check whether the GLB_IRQ_RAW[iraw_rxd_up] signal is valid to determine whether there are frames waiting to be received.
[6]	RO	int_freeeq_up	The port output queue is interrupted from not empty to empty, indicating that the output queue buffer is not empty to empty, indicating that the CPU can write a new group of frames to be sent. 0: no interrupt is generated; 1: The output queue is interrupted from not empty to empty. After entering the interrupt program, the software judges whether the current output queue is empty by querying UD_GLB_ADDRQ_STAT[eq_cnt]. If it is not empty, it means that the interrupt is an invalid interrupt.
[5]	RO	int_stat_up	Port state change interrupt signal, indicating that MDIO is adaptive to PHY chip speed change, duplex mode change and connection state change to generate an interrupt. 0: no interrupt is generated; 1: Port state change interrupt. After entering the interrupt program, the software determines what state changes according to the configuration value of UD_MDIO_IRQENA .

[4]	RO	int_duplex_up	Port duplex mode change interrupt indication. 0: Duplex mode does not change; 1: The duplex mode changes, an interrupt is generated. After entering the interrupt program, query UD_MAC_STAT_CHANGE[duplex_stat_ch] to determine whether the duplex state has changed.
[3]	RO	int_speed_up	Port speed mode change interrupt indication. 0: The speed mode does not change; 1: The speed mode changes, an interrupt is generated. After entering the interrupt program, query UD_MAC_STAT_CHANGE[speed_stat_ch] to determine whether the speed status has changed.
[2]	RO	int_link_up	Port connection status change interrupt indication. 0: The connection status does not change; 1: The connection status changes, and an interrupt is generated. After entering the interrupt program, query UD_MAC_STAT_CHANGE[link_stat_ch] to determine whether the connection status has changed.
[1]	RO	int_tx_up	Indicates that the port has finished sending 1 frame of data from the CPU. 0: not finished sending; 1: The transmission has been completed and an interrupt is generated. When the interrupt occurs, it is necessary to query the current dequeue address eq_out_index of the output queue in UD_GLB_QSTAT to determine whether to release the buffer space of the output frame.
[0]	RO	int_rx_up	The port has a frame waiting for the CPU to receive an interrupt indication. 0: Interrupt is invalid; 1: The interrupt is valid, and there are frames waiting for the CPU to receive in the input queue. When the interrupt occurs, it is necessary to check whether the GLB_IRQ_RAW[iraw_rxd_up] signal is valid to determine whether there are frames waiting to be received.

GLB_IRQ_ENA

GLB_IRQ_ENA is the interrupt enable register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1334	GLB_IRQ_ENA	0x0000_0000



Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RW	ien_all	All interrupts are enabled. 0: disabled (all interrupts cannot be reported); 1: Enable (all interrupts are reported according to the corresponding configuration).
[18]	RW	ien_up	All upstream port interrupts are enabled. 0: Disabled (all uplink port interrupts cannot be reported); 1: Enabled (all uplink port interrupts are reported according to the configuration).
[17:13]	RO	reserved	reserve.
[12]	RW	ien_mdio_finish	MDIO Completed CPU operation indication enable. 0: forbidden; 1: enable.
[11:8]	RO	reserved	reserve.
[7]	RW	one_rxd_up	The upstream port has (multiple) frames waiting for the CPU to receive enable (multi-packet interrupt). 0: disable; 1: enable.
[6]	RW	one_freeeq_up	The upstream port output queue is enabled by the not-empty-to-empty interrupt signal. 0: forbidden; 1: enable.
[5]	RW	ien_stat_up	Upstream port status change interrupt signal enable. 0: forbidden; 1: enable.
[4]	RW	ien_duplex_up	Upstream port duplex mode change interrupt enable. 0: disable; 1: enable.

[3] RW	ien_speed_up		Upstream port speed mode change interrupt enable. 0: forbidden; 1: enable.
[2] RW	ien_link_up		Uplink port connection status change interrupt enable. 0: disable; 1: enable.
[1] RW	ien_tx_up		When the uplink port finishes sending 1 frame of data from the CPU, the indication is enabled. 0: forbidden; 1: enable.
[0] RW	ien_rx_up		The uplink port has frames waiting for the CPU to receive enable. 0: forbidden; 1: enable.

GLB_IRQ_RAW

GLB_IRQ_RAW is the raw interrupt register. This register does not support soft reset, it is write 1 clear 0 register.

Offset Address	Register Name	Total Reset Value
0x1338	GLB_IRQ_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	WC	iraw_mdio_finish	MDIO completes the raw interrupt status of CPU operations. 0: no interrupt; 1: interrupt.
[11:8]	RO	reserved	reserve.

[7] WC iraw_rxd_up			Raw interrupt status (multi-packet interrupt) where the upstream port has frame(s) waiting to be received by the CPU. 0: no interrupt; 1: There is an interrupt.
[6] WC iraw_freeeq_up			The original interrupt status of the output queue of the uplink port is from not empty to empty, indicating that the output queue buffer is from not empty to empty, indicating that the CPU can write a new set of frames to be sent. 0: no interrupt; 1: There is an interrupt.
[5] WC iraw_stat_up			The original interrupt status of the status change of the uplink port indicates that the MDIO is adaptive to the speed change of the PHY chip, the duplex mode changes and the connection status changes to generate an interrupt. 0: no interrupt; 1: There is an interrupt.
[4] WC iraw_duplex_up			Raw interrupt status for uplink port duplex mode change. 0: no interrupt; 1: There is an interrupt.
[3] WC iraw_speed_up			Raw interrupt status for uplink port speed mode change. 0: Interrupt is invalid; 1: Velocity mode changes, an interrupt is generated. Write 1 to clear this register.
[2] WC iraw_link_up			Raw interrupt status for uplink port connection status changes. 0: no interrupt; 1: interrupt.
[1] WC iraw_tx_up			The upstream port finishes sending the raw interrupt status from the CPU. 0: no interrupt; 1: There is an interrupt.
[0] WC iraw_rx_up			The upstream port has a raw interrupt status with frames waiting to be received by the CPU. 0: no interrupt; 1: There is an interrupt.

GLB_MAC0_L32

GLB_MAC0_L32 is the low 32bit register of MAC0 in the filtering table.

Offset Address	Register Name	Total Reset Value
0x1400	GLB_MAC0_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac0	The lower 32 bits of MAC0 in the filtering table.

GLB_MAC0_H16

GLB_MAC0_H16 is the high 16bit register of filter table MAC0.

Offset Address	Register Name	Total Reset Value
0x1404	GLB_MAC0_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														flt_mac0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac0_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.
[15:0]	RW	flt_mac0	The upper 16 bits of the filter table MAC0.

GLB_MAC1_L32

GLB_MAC1_L32 is the low 32-bit register of MAC1 filter table.

Offset Address	Register Name	Total Reset Value
0x1408	GLB_MAC1_L32	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flt_mac1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	flt_mac1	The lower 32 bits of the filter table MAC1.

GLB_MAC1_H16

GLB_MAC1_H16 is the high 16-bit register of the filter table MAC1.

Offset Address	Register Name	Total Reset Value
0x140C	GLB_MAC1_H16	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved				flt_mac1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac1_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.
[15:0]	RW	flt_mac1	High 16bit of filter table MAC1.

GLB_MAC2_L32

GLB_MAC2_L32 is the low 32bit register of MAC2 filter table.

Offset Address	Register Name	Total Reset Value
0x1410	GLB_MAC2_L32	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flt_mac2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	flt_mac2	The lower 32bits of the filter table MAC2.

GLB_MAC2_H16

GLB_MAC2_H16 is the high 16-bit register of the filter table MAC2.

Offset Address	Register Name	Total Reset Value
0x1414	GLB_MAC2_H16	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved				flt_mac2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac2_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.

[15:0]	RW	flt_mac2	High 16bit of filter table MAC2.

GLB_MAC3_L32

GLB_MAC3_L32 is the low 32bit register of MAC3 filter table.

Offset Address	Register Name	Total Reset Value
0x1418	GLB_MAC3_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac3	The lower 32 bits of the filter table MAC3.

GLB_MAC3_H16

GLB_MAC3_H16 is the high 16-bit register of filter table MAC3.

Offset Address	Register Name	Total Reset Value
0x141C	GLB_MAC3_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.

[17] RW	mac3_up		This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16] RO		reserved	reserve.
[15:0] RW	flt_mac3		High 16bit of filter table MAC3.

GLB_MAC4_L32

GLB_MAC4_L32 is the low 32bit register of MAC4 filter table.

Offset Address	Register Name	Total Reset Value
0x1420	GLB_MAC4_L32	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flt_mac4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0] RW	flt_mac4		The lower 32bits of the filter table MAC4.

GLB_MAC4_H16

GLB_MAC4_H16 is the high 16-bit register of the filter table MAC4.

Offset Address	Register Name	Total Reset Value
0x1424	GLB_MAC4_H16	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved				flt_mac4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22] RO		reserved	reserve.

[21] RW	fw2cpu_up		When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18] RO		reserved	reserve.
[17] RW	mac4_up		This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16] RO		reserved	reserve.
[15:0] RW	flt_mac4		High 16bit of filter table MAC4.

GLB_MAC5_L32

GLB_MAC5_L32 is the low 32bit register of filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x1428	GLB_MAC5_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac5	The lower 32 bits of the filter table MAC5.

GLB_MAC5_H16

GLB_MAC5_H16 is the high 16-bit register of the filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x142C	GLB_MAC5_H16	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flt_mac5
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac5_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.
[15:0]	RW	flt_mac5	High 16bit of filter table MAC5.

GLB_MAC6_L32

GLB_MAC6_L32 is the low 32bit register of MAC6 filter table.

Offset Address	Register Name	Total Reset Value
0x1430	GLB_MAC6_L32	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flt_mac6
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	flt_mac6	The lower 32 bits of the filter table MAC6.

GLB_MAC6_H16

GLB_MAC6_H16 is the high 16bit register of filter table MAC6.

Offset Address	Register Name	Total Reset Value
0x1434	GLB_MAC6_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																flt_mac6															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac6_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.
[15:0]	RW	flt_mac6	High 16bit of filter table MAC6.

GLB_MAC7_L32

GLB_MAC7_L32 is the low 32-bit register of MAC7 filter table.

Offset Address	Register Name	Total Reset Value
0x1438	GLB_MAC7_L32	0x0000_0000

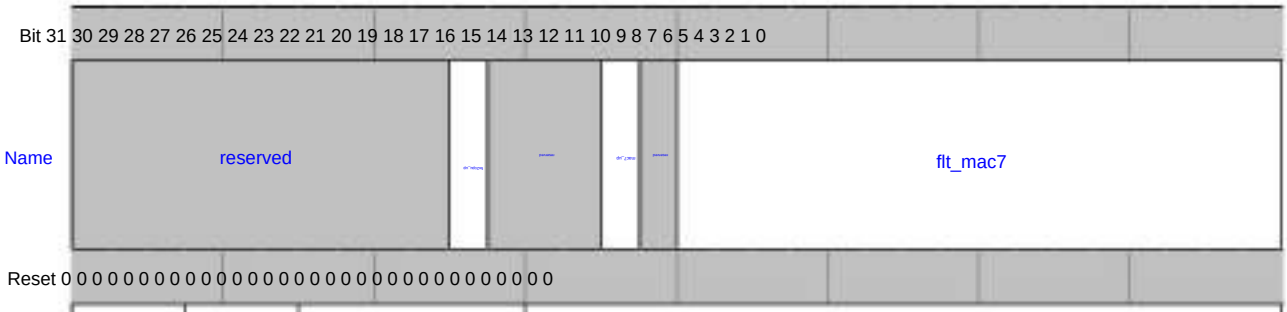
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac7	The lower 32 bits of the filtering table MAC7.

GLB_MAC7_H16

GLB_MAC7_H16 is the high 16-bit register of filter table MAC7.

Offset Address	Register Name	Total Reset Value
0x143C	GLB_MAC7_H16	0x0000_0000



Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	fw2cpu_up	When this filter is enabled on the uplink port, whether the input frame on the uplink port hits this filter is forwarded to the CPU port. 0: No; 1: Yes.
[20:18]	RO	reserved	reserve.
[17]	RW	mac7_up	This filter is configured as uplink port usage control. 0: The uplink port does not use this filter; 1: The uplink port uses this filter.
[16]	RO	reserved	reserve.
[15:0]	RW	flt_mac7	High 16bit of filter table MAC7.

UD_GLB_IRQN_SET

UD_GLB_IRQN_SET is the multi-packet interrupt configuration register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0340	UD_GLB_IRQN_SET	0x0800_003A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							int_frm_cnt					reserved												age_timer							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	int_frm_cnt	This setting is used for the multi-packet interrupt function, which is defined as reporting a multi-packet interrupt for every number of packets received. **Note: The minimum value of int_frm_cnt** can be configured as 1, at this time, multi-packet interrupt is equivalent to single-packet interrupt.
[23:16]	RO	reserved	reserve.
[15:0]	RW	age_timer	After the multi-packet interrupt function is enabled, the number of received packets has not reached the number of packets required to report the multi-packet interrupt after a certain period of time. This period of time is defined as the aging time of the multi-packet interrupt. **Note: age_timer** counts the period of the main clock divided by **256 .**

UD_GLB_QLEN_SET

UD_GLB_QLEN_SET is the queue length configuration register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0344	UD_GLB_QLEN_SET	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		iq_len										eq_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:8]	RW	iq_len	Enter (receive) queue length configuration. **Note: iq_len** must not be configured as 0, otherwise it will be forcibly set to 1; the sum of the configured **iq_len** and **eq_len** must not be greater than 64, otherwise the value of **iq_len** (not **0)** is satisfied first , and eq_len takes **64–iq_len.**
[7:6]	RO	reserved	reserve.

[5:0] RW	eq_len		Output (packet sending) queue length configuration. **Note: eq_len** must not be configured as 0, otherwise it will be forcibly set to 1.

UD_GLB_FC_LEVEL

UD_GLB_FC_LEVEL is the flow control register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0348	UD_GLB_FC_LEVEL	0x3018_0508

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																										qlimit_up					qlimit_down	
Reset	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14]	RW	qlimit_ena	Receive queue flow control is enabled. 0: Disabled (do not send flow control information according to the status of the receiving queue); 1: Enable (flow control information can be sent according to the status of the receiving queue).
[13:8]	RW	qlimit_up	Receive queue flow control upper limit. When the remaining available queue space of the input queue is less than the upper limit, if the receive queue flow control is enabled, the flow control information will be sent to the peer. Note: If the upper limit value **qlimit_up** is set to 0, it will not be able to enter the flow control state; the upper limit value **qlimit_up** must be smaller than the lower limit value **qlimit_down .**
[7:6]	RO	reserved	reserve.
[5:0]	RW	qlimit_down	The receive queue releases the flow control lower limit. When the remaining available queue space of the input queue is greater than or equal to the lower limit and is in the receive flow control state, the current flow control state is released.

UD_GLB_CAUSE

UD_GLB_CAUSE is the Cause register for sending the message to the CPU. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x034C	UD_GLB_CAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mact_cause	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RO	mact_cause	The matching result type of the packet lookup MAC table. 000: Mandatory forwarding; 001: The destination MAC is the message of the local MAC; 010: broadcast message; 011: Match the message in the MAC table; 100: Multicast packets that do not match the MAC table; 101: Unicast packets that do not match the MAC table; Other: reserved.

UD_GLB_RXFRM_SADDR

UD_GLB_RXFRM_SADDR is the input frame start address register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0350	UD_GLB_RXFRM_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxfrm_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxfrm_saddr	The starting address of the received frame.

UD_GLB_IQFRM_DES

UD_GLB_IQFRM_DES is the input frame description sub-register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0354	UD_GLB_IQFRM_DES	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	fd_vlanid	fd_in_addr	fd_in_len
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17:12]	RO	fd_in_addr	The relative address of the first frame waiting to be received in the input queue (iq) is used as the index value of the absolute address of the frame storage (0~iq_len–1).
[11:0]	RO	fd_in_len	Enter the frame length of the frames to be received in the queue.

UD_GLB_IQ_ADDR

UD_GLB_IQ_ADDR is the first address register of the input frame. This register does not support soft reset.

说明

If the address allocated by the software is not word-aligned, the logic will write data according to the word address, but the previously written data is invalid. For example, if the configured frame header address is 0xF000_8002 (non-word-aligned address), the logic will write 0x00 (or other data) at both addresses 0xF000_8000 and 0xF000_8001, and write the first byte of the received frame at 0xF000_8002 (valid data), write the second byte (valid data) of the received frame at 0xF000_8003, and write the subsequent data into the buffer in turn. If it is other non-word aligned addresses, the operation is similar.

Offset Address	Register Name	Total Reset Value
0x0358	UD_GLB_IQ_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	startaddr_iq
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	startaddr_iq	The first address of the storage space corresponding to the input frame configured by the CPU. The receiving frame applies for the bus according to this address.

UD_GLB_BFC_STAT

UD_GLB_BFC_STAT is the forwarding cache flow control status and multi-packet interrupt aging time counter. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x035C	UD_GLB_BFC_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timerover_cnt	flowctrl_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	timerover_cnt	Multi-packet interrupt aging time counter overflows (counts to the configured value) times counter. Note: If **the timerover_cnt** value is too large per unit time , it means that **the setting of UD_GLB_IRQN_SET[int_frm_cnt] is unreasonable, and the multi-packet interrupt is mainly** triggered by the aging time, so the configuration value needs to be reduced.
[15:0]	RO	flowctrl_cnt	The counter for the number of times the forwarding buffer of the uplink port (or downlink port) enters the flow control state. Note: If the value of **flowctrl_cnt** is too large per unit time , it means that the setting of **UD_GLB_FC_LEVEL[blimit_up] or UD_GLB_FC_LEVEL[blimit_down] is too small, or the external network** status deteriorates, and the configuration value may need to be reduced.

UD_GLB_EQ_ADDR

UD_GLB_EQ_ADDR is the first address register of the output queue. This register does not support soft reset.

说明

If the first address of the output frame is not word-aligned, the logic will read in data according to the word address, but the previously read data is discarded as invalid data. For example, if the first address of the configured sending frame is 0xF000_8102 (non-word-aligned address), the logic will directly discard the byte data read from addresses 0xF000_8100 and 0xF000_8101, and the data read in at 0xF000_8102 will be regarded as the first byte of the sending frame (valid data), the data read in at 0xF000_8103 is the second byte (valid data) of the sending frame, and the subsequent data are all valid data (until the data of the specified frame length is read). If it is other non-word aligned addresses, the operation is similar.

Offset Address	Register Name	Total Reset Value
0x0360	UD_GLB_EQ_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	add_fd_addr_out	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	add_fd_addr_out	The first address of the transmit frame that the CPU adds to the output queue.

UD_GLB_EQFRM_LEN

UD_GLB_EQFRM_LEN is the output queue frame length configuration register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0364	UD_GLB_EQFRM_LEN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / add_fd_len_out
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:11]	RO	reserved	reserve.
[10:0]	RW	add_fd_len_out	The frame length of the send frame that the CPU adds to the output queue. Configure this register to trigger the hardware to write the first address and frame length of the sent frame into the output queue for sending. When the software sends a frame, it must first write the first address of the frame, and then write the frame length of the frame. **Note: frames with add_fd_len_out** less than **20byte** and greater than **1600byte** will be discarded, that is, the sending range is between **20byte and 1600byte .**

UD_GLB_QSTAT

UD_GLB_QSTAT is the queue status register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0368	UD_GLB_QSTAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	— / iq_in_index / — / cpuw_index / — / eq_in_index / — / eq_out_index
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

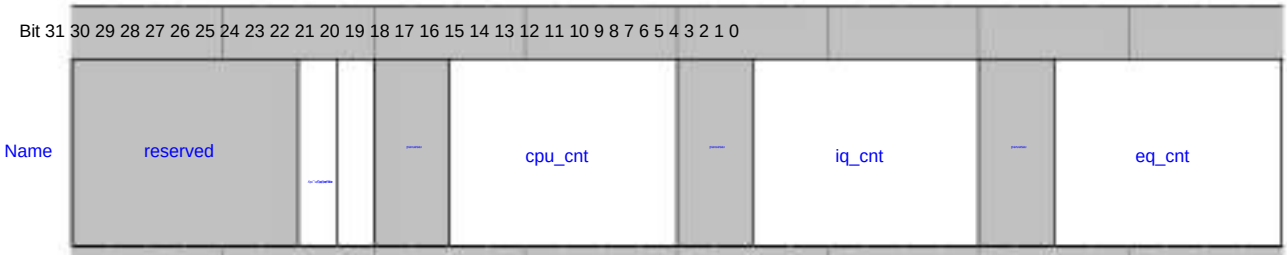
Bits	Access Name		Description
[31:30]	RO	reserved	reserve.
[29:24]	RO	iq_in_index	Input (packet receiving) queue entry index.
[23:22]	RO	reserved	reserve.
[21:16]	RO	cpuw_index	Input (receive) the first address of the queue frame into the queue index.
[15:14]	RO	reserved	reserve.
[13:8]	RO	eq_in_index	Output (packet sending) queue descriptor entry index.

[7:6] RO		reserved	reserve.
[5:0] RO		eq_out_index Output (packet sending) queue descriptor out of queue index.	

UD_GLB_ADDRQ_STAT

UD_GLB_ADDRQ_STAT is the address queue status register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x036C	UD_GLB_ADDRQ_STAT	0x0300_0000



Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RO	cpuaddr_in_rdy	Whether the CPU can configure the first address of the input queue frame. 0: No; 1: Yes. **Note: cpuaddr_in_rdy and eq_in_rdy** are 0 when reset , but will be set to 1 by the circuit immediately after reset. That is, **the iq** address queue and the **eq** description subqueue can be configured after reset .
[24]	RO	eq_in_rdy	Whether the CPU can configure the output queue frame descriptor (frame head address and frame length) 0: No; 1: Yes.
[23:22]	RO	reserved	reserve.
[21:16]	RO	cpu_cnt	The input queue counts the number of available frame start addresses allocated by the CPU.
[15:14]	RO	reserved	reserve.
[13:8]	RO	iq_cnt	The input queue has already used the length (0~iq_len).
[7:6]	RO	reserved	reserve.
[5:0]	RO	eq_cnt	The output queue has used length (0~eq_len).

UD_GLB_FC_TIMECTRL

UD_GLB_FC_TIMECTRL is the flow limit time configuration register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0370	UD_GLB_FC_TIMECTRL	0x07FF_86A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																flux_timer_cfg															flux_timer_inter														
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	0	0	0	0	1	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:17]	RW	flux_timer_cfg	The flow limit time interval counter counts the divided clock generated by flux_timer_inter. Configured as 0, no flow restriction is performed.
[16:0]	RW	flux_timer_inter	Flow limit time granularity counter, counts the main clock, the default is 100000, and it is 1ms when the main clock is 100MHz.

UD_GLB_FC_RXLIMIT

UD_GLB_FC_RXLIMIT is the flow limit watermark configuration register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0374	UD_GLB_FC_RXLIMIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				flux_cfg													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	flux_cfg	Flow limit upper limit threshold register, this group limits the number of frames received by the software within the flow limit time interval, and frames exceeding the configured value are selectively discarded or received according to the configuration. When configured as all 0s, it means no traffic restriction.

UD_GLB_FC_DROPCTRL

UD_GLB_FC_DROPCTRL is the flow limit packet loss control register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0378	UD_GLB_FC_DROPCTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	flux_uni	Whether to discard unicast packets when the traffic limit exceeds the upper limit. 0: No; 1: Yes.
[1]	RW	flux_multi	Whether to discard multicast packets when the traffic limit exceeds the upper limit. 0: No; 1: Yes.
[0]	RW	flux_broad	Whether to discard broadcast packets when the traffic limit exceeds the upper limit. 0: No; 1: Yes.

5.1.6.4 Statistical counting control register

UD_STS_PORTCNT

UD_STS_PORTCNT is the status counter of the port part. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0584	UD_STS_PORTCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0							
Name	rxsof_cnt	rxeof_cnt	rxcrcok_cnt	rxcrcbad_cnt	txsof_cnt	txeof_cnt	txcrcok_cnt	txcrcbad_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0							

Bits	Access	Name	Description
[31:28]	RO	rxsof_cnt	Port received frame header count.
[27:24]	RO	rxeof_cnt	End of frame count received by the port.
[23:20]	RO	rxcrcok_cnt	port received CRC check correct count.

[19:16] RO		rxcrcbad_cnt	Port received CRC check error count.
[15:12] RO		txsof_cnt	Port sent frame header count.
[11:8] RO		txeof_cnt	The port sends the end-of-frame count.
[7:4] RO		txcrcok_cnt	port sends CRC check correct count.
[3:0] RO		txcrcbad_cnt	Port transmit CRC check error count.

UD_PORT2CPU_PKTS

UD_PORT2CPU_PKTS is the register for the total number of packets received by the CPU from the uplink or downlink port. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A0	UD_PORT2CPU_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	pkts_cpu
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	WC	pkts_cpu	The number of all packets received by the CPU port, writing 0 to this register will clear it to 0, and writing 1 is invalid.

UD_CPU2IQ_ADDRCNT

UD_CPU2IQ_ADDRCNT is used to configure the receiving address queue times register for the CPU. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A4	UD_CPU2IQ_ADDRCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	addr_cpu
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	WC	addr_cpu	The number of times the CPU has successfully configured the packet receiving address queue. Writing 0 to this register clears 0, and writing 1 is invalid.

UD_RX_IRQCNT

UD_RX_IRQCNT is the register for the number of interrupts reported by the uplink or downlink port. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A8	UD_RX_IRQCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	pkts_port
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	WC	pkts_port	Reported frame receiving interrupt count, writing 0 to this register clears 0, writing 1 is invalid.

UD_CPU2EQ_PKTS

UD_CPU2EQ_PKTS is the register for the total number of packets sent by the CPU to the uplink or downlink send port. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05AC	UD_CPU2EQ_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	pkts_cpu2tx
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	WC	pkts_cpu2tx	The count of all packets sent from the CPU port to the port. Writing 0 to this register clears 0, and writing 1 is invalid.

5.1.6.5 Statistics result register

Statistical results can be configured in two modes: read-only and read-clear 0 (UD_MAC_SET[cntr_rdclr_en] is set to 1 to indicate read-clear 0 mode, and set to 0 to indicate read-only mode). The following introduction to the register is for the read-only mode.

UD_RX_DVCNT

UD_RX_DVCNT is the RXDV rising edge times register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0600	UD_RX_DVCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rxdvrise
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rxdvrise	Count of all rxdv rising edges.

UD_RX_OCTS

UD_RX_OCTS is the total bytes received register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0604	UD_RX_OCTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ifinoctets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	ifinoctets	A count of all received bytes, including good frames, error frames, and bytes in the Preamble. Frames without a valid SFD (Start of Frame Delimiter) are not counted.

UD_RX_RIGHTOCTS

UD_RX_RIGHTOCTS is the register for the total number of bytes of received correct packets. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0608	UD_RX_RIGHTOCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_rx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	octets_rx	Count of received bytes, including good and errored frames, but excluding preamble bytes. Frames with no valid SFD detected are not counted.

UD_HOSTMAC_PKTS

UD_HOSTMAC_PKTS is the packet number register matching the local MAC. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x060C	UD_HOSTMAC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	local_mac_match																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	local_mac_match	The count of the correct frames with the same destination MAC address and the local MAC address in the received frame, excluding ultra-short frames, ultra-long frames, CRC error frames, flow control frames and transmission error frames.

UD_RX_RIGHTPKTS

UD_RX_RIGHTPKTS is the total number of packets received by the port register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0610	UD_RX_RIGHTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	pts	Count of all frames.

UD_RX_BROADPKTS

UD_RX_BROADPKTS is the correct broadcast packet count register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0614	UD_RX_BROADPKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	broadcastpkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	broadcastpkts	The count of broadcast frames with valid frame length and correct CRC, but not including flow control frames and transmission error frames.

UD_RX_MULTPKTS

UD_RX_MULTPKTS is the correct multicast packet count register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0618	UD_RX_MULTPKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	multicastpkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	multicastpkts	The count of multicast frames with valid frame length and correct CRC, but not including flow control frames and transmission error frames.

UD_RX_UNIPKTS

UD_RX_UNIPKTS is the correct unicast packet count register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x061C	UD_RX_UNIPKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ifinucastpkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	ifinucastpkts	The count of unicast frames with valid frame length and correct CRC, but not including flow control frames and transmission error frames.

UD_RX_ERRPKTS

UD_RX_ERRPKTS is the total number of error packets register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0620	UD_RX_ERRPKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ifinerrors
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	ifinerrors	Count of all error frames received, including CRC error frames, underruns, overruns, and transmit errors.

UD_RX_CRCERR_PKTS

UD_RX_CRCERR_PKTS is the CRC error times register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0624	UD_RX_CRCERR_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	crcerr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	crcerr	The frame length of the received frame is valid (not ultra-short or ultra-long frame), but the number of frames whose CRC or Alignment check is wrong.

UD_RX_LENERR_PKTS

UD_RX_LENERR_PKTS is the packet count register with invalid packet length. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0628	UD_RX_LENERR_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	abnormalsizepkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	abnormalsizepkts	The number of invalid frame lengths (less than the set minimum effective frame length, or the frame length is greater than the set maximum effective frame length) (ultra-short frame, ultra-long frame).

UD_RX_OCRCERR_PKTS

UD_RX_OCRCERR_PKTS is the CRC error packet number register for odd Nibble. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x062C	UD_RX_OCRCERR_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dot3alignmenterr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	dot3alignmenterr	received an odd number of Nibble CRC error frames.

UD_RX_PAUSE_PKTS

UD_RX_PAUSE_PKTS is the number of flow control packets received register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0630	UD_RX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3pause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	dot3pause	The number of flow control frames received.

UD_RF_OVERCNT

UD_RF_OVERCNT is the RXFIFO overflow times register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0634	UD_RF_OVERCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dropevents																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	dropevents	The cumulative number of RXFIFO overflow events during frame reception.

UD_FLUX_TOL_IPKTS

UD_FLUX_TOL_IPKTS is the register of the total number of packets of flow limit entry. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0638	UD_FLUX_TOL_IPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_frame_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	flux_frame_cnt	The flow limit enters the total count of correct frames, excluding runt frames, jumbo frames, CRC error frame, flow control frame and transmission error frame.

UD_FLUX_TOL_DPKTS

UD_FLUX_TOL_DPKTS is the total number of packets discarded by flow limit register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x063C	UD_FLUX_TOL_DPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_drop_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_drop_cnt	Flow limit discards the count of correct frames, excluding runny frames, jumbo frames, CRC error frames, flow control frames, and transmission error frames.

UD_MN2CPU_PKTS

UD_MN2CPU_PKTS is the register for MAC to limit the number of packets not forwarded to the CPU port. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x064C	UD_MN2CPU_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_not2cpu_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	mac_not2cpu_pkts	Number of packets not forwarded on CPU ports due to MAC restrictions.

UD_TX_PKTS

UD_TX_PKTS is the total number of packets sent successfully register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0780	UD_TX_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pkts_tx	The count of all configured sending frames, excluding frames discarded after timeout and sending frames whose configuration length of UD_GLB_EQFRM_LEN is not within the valid range.

UD_TX_BROADPKTS

UD_TX_BROADPKTS is the number register of successfully sent broadcast packets. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0784	UD_TX_BROADPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	broadcastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	broadcastpkts_tx	Count of successfully sent broadcast frames (excluding retransmissions).

OUT_TX_MULTPKTS

UD_TX_MULTPKTS is the register for the number of successfully sent multicast packets. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0788	OUT_TX_MULTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	multicastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	multicastpkts_tx	Count of successfully sent multicast frames (excluding retransmissions).

UD_TX_UNIPKTS

UD_TX_UNIPKTS is the register for the number of successfully sent unicast packets. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x078C	UD_TX_UNIPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifoutucastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifoutucastpkts_tx	Count of successfully sent unicast frames (excluding retransmissions).

UD_TX_OCTS

UD_TX_OCTS is the total bytes sent register. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0790	UD_TX_OCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	octets_tx	The total number of bytes sent, including retransmitted frames, correct frames, and error frames, but preamble bytes are not counted.

UD_TX_PAUSE_PKTS

UD_TX_PAUSE_PKTS is the register for the number of flow control frames sent. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0794	UD_TX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3outpause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3outpause	The number of flow control frames sent by dot3outpause.

UD_TX_RETRYCNT

UD_TX_RETRYCNT is the total number of retransmission registers during sending. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0798	UD_TX_RETRYCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	retry_times_tx
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	retry_times_tx	configures the total number of retransmissions for sending frames.

UD_TX_COLCNT

UD_TX_COLCNT is the total number of collision registers. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x079C	UD_TX_COLCNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	collisions
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	collisions	The number of times conflicts occurred.

UD_TX_LC_PKTS

UD_TX_LC_PKTS is the packet count register where LateCollision occurs. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A0	UD_TX_LC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dot3latecol
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RO	dot3latecol The number of packets where Latecollission occurred.

UD_TX_COLOK_PKTS

UD_TX_COLOK_PKTS is the register for the number of packets that have conflicts but are successfully sent. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A4	UD_TX_COLOK_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dot3col_ok
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RO	dot3col_ok The number of successfully sent packets after a collision.

UD_TX_RETRY15_PKTS

UD_TX_RETRY15_PKTS is the register for the number of discarded packets retransmitted over 15 times. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A8	UD_TX_RETRY15_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dot3excessivecol
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RO	dot3excessivecol Number of packets discarded due to retransmission times greater than 15.

UD_TX_RETRYN_PKTS

UD_TX_RETRYN_PKTS is the packet count register whose number of collisions is equal to the domain value. This register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07AC	UD_TX_RETRYN_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3colcnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	dot3colcnt	The number of packets whose collision times are equal to the collision threshold is set by UD_MAC_SET[colthreshold].

5.2 FE PHY

5.2.1 Overview

10/100M Ethernet physical layer transceiver IP includes physical coding sublayer (PCS), physical medium additional sublayer (PMA), Twisted Pair Physical Media Dependent Sublayer (TP-PMD), 10Base-TX Codec, and Twisted Pair Media Access Unit (TPMAU). The 10/100M Ethernet physical layer transceiver IP supports auto flip.

5.2.2 Features

Complies with IEEE Std 802.3az-2010 standard.

Compliant with 100Base-TX IEEE 802.3u standard. Compliant with 10Base-T IEEE 802.3 standard. Support full/half duplex operation. Support twisted pair or fiber mode output. Auto-negotiation is supported. Support power-down mode.

Supports operation in power-saving mode when disconnected. Support baseline drift compensation.

Support automatic flip.

Support interrupt function. Wake on LAN is supported.

Supports adaptive equalization.

Support automatic polarity correction.

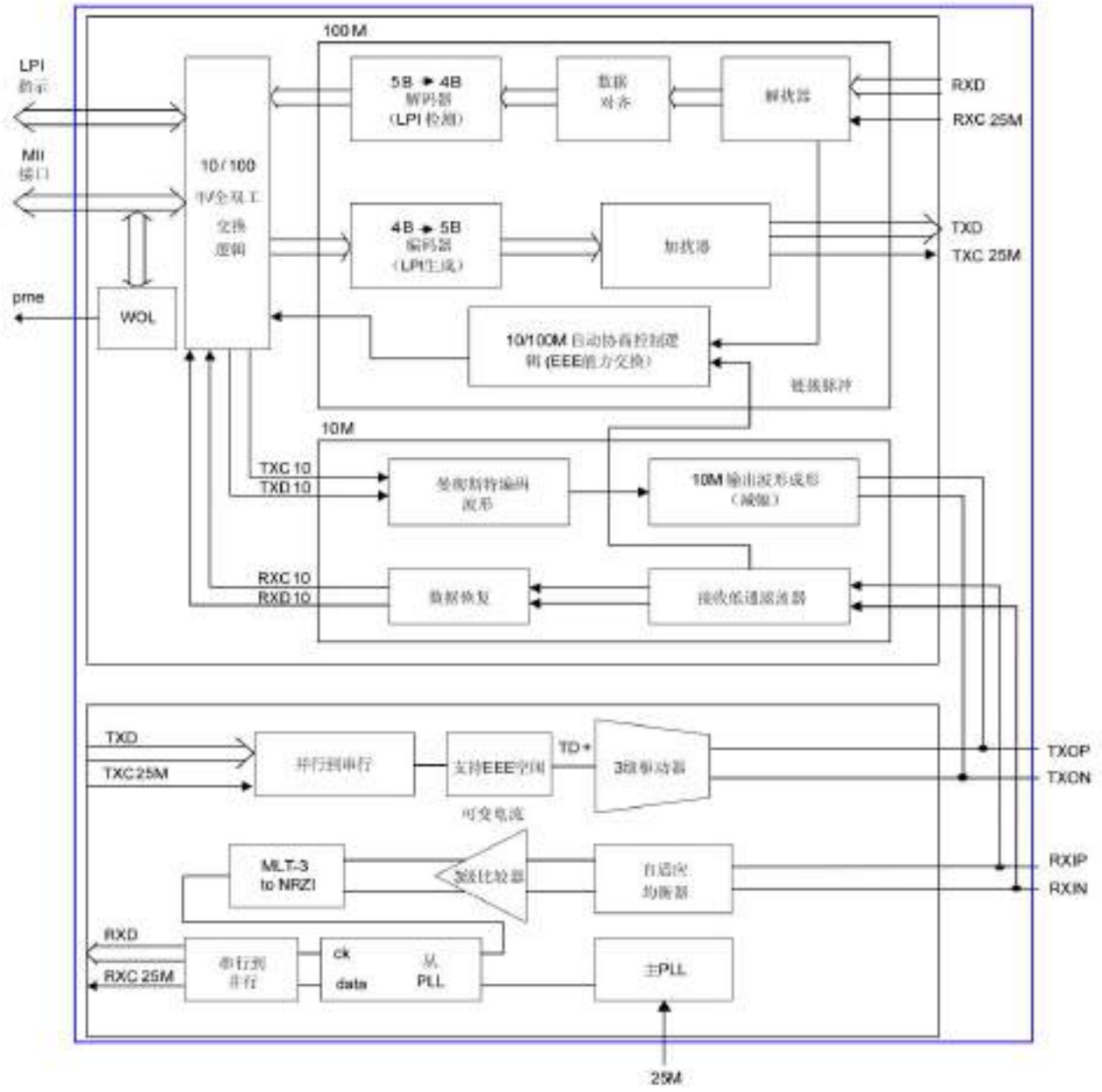
Three custom LEDs are supported.

Supports 25 MHz clock input.

Support reading and writing PHY internal registers through MDIO interface.

5.2.3 Functional description

Figure 5-5 System block diagram



5.2.3.2 Auto-negotiation and parallel detection

The 10/100M Ethernet physical layer transceiver IP supports auto-negotiation defined by IEEE 802.3u clause 28 to communicate with other transceivers that support auto-negotiation. 10/100M Ethernet Physical Layer Transceiver IP Auto-Detect Link Pair

Based on the capabilities of the end devices, determine the highest speed or duplex configuration between the two devices. If the link peer device does not support auto-negotiation, the 10/100M Ethernet physical layer transceiver IP enables half-duplex mode and enters parallel detection mode. The 10/100M Ethernet Physical Layer Transceiver IP transmits Fast Link Pulse (FLP) by default and waits for a response from the link peer. If the 10/100M Ethernet physical layer transceiver IP receives a fast link pulse, it will continue the auto-negotiation process. If a normal link pulse (NLP) is received, the 10/100M Ethernet physical layer transceiver IP will switch to 10Mbit/s and half-duplex mode. If a 100Mbit/s idle mode is received, the 10/100M Ethernet Physical Layer Transceiver IP will switch to 100 Mbit/s and half-duplex mode.

5.2.3.3 Power-down and line-down power-saving modes

Two power-saving mode operations are supported. Describes how to implement each mode in software.

Table 5-10 Power saving mode pin configuration

model	describe
LDPS sets the 15th bit of register 24 to 1 to make the 10/100M Ethernet physical layer transceiver IP in the offline (power saving) mode	Mode. In drop-off mode, the 10/100M physical layer transceiver IP will detect the link state to determine whether to close the transmission function. If the link is down, fast link bursts, 100 Mbit/s idle mode and 10 Mbit/s normal link bursts will not be transmitted. However, something like a normal link pulse will be transmitted. Once the leveled signal is detected, the transceiver will stop these signals and retransmit the fast link pulse, 100 Mbit/s idle mode or 10 Mbit/s normal link pulse. When disconnected, it will save 60%~80% of power.
PWD	Setting bit 11 of register 0 to 1 puts the transceiver in power-down mode (PWD). This is the ideal power-saving mode when the transceiver is powered. In power-down mode, the physical transceiver will shut down all analog/digital functions except the MDC/MDIO management interface. Therefore, if the transceiver is in power-down mode and the MAC wants to call the PHY layer again, the PHY layer must create the MDC/MDIO sequence itself (this operation is done by software).

5.2.3.4 10/100M sending and receiving

100Base-TX Transmit Operation

Convert four-bit data (txd0~txd3) transmitted at a clock frequency of 25 MHz (txc) into 5B symbol codes (4B/5B encoding). Scrambling, serialization and conversion are clocked at 125 MHz, followed by NRZ-to-NRZI transcoding. Transmits the NRZI signal to the MLT-3 encoder and then to the transmit line driver. The transmitter retracts asserting the transmit enable signal. Before sending the data pattern, the transmitter will send a /J/K symbol (frame start qualifier), data symbols, and a T/R symbol (frame end qualifier). For better EMI performance, the start source of the scrambler is based on the PHY address. In a hub/switch environment, the 10/100M Ethernet PHY Transceiver IP has a different scrambler enable source so that the MLT-3 output signal can be distributed.

100Base-TX Receive Operation

The received signal is compensated by an adaptive equalizer to compensate for signal loss due to cable attenuation and inter-symbol interference. Baseline drift correction monitoring and dynamic correction signal equalization process. The phase-locked loop then recovers timing information from the signal and the received clock. In this way, the received signal is sampled to form NRZI data. The next steps are NRZI-to NRZ code conversion, descrambling data, parallel to serial conversion, 5B to 4B code conversion and sending 4B encoded four-bit data to MII interface.

10Base-T send operation

Send four bits of data (txd0~txd3) to the parallel-serial converter with a clock frequency of 25 MHz (txc). The output 10 Mbit/s NRZ signal is sent to the Manchester encoder. The Manchester encoder converts the 10 Mbit/s NRZ data into a Manchester encoded data stream for the TP transmitter and adds an initial null pulse at the end of the data packet as specified by IEEE 802.3. Finally, the encoded data stream is processed and sent by the bandwidth-limited filter embedded in the 10/100M Ethernet physical layer transceiver IP.

10Base-T receive operation

In 10Base-T receive mode, the Manchester encoder embedded in the 10/100M Ethernet physical layer transceiver IP converts the Manchester decoded data stream into NRZ data by decoding the data and removing initial null pulses. The serial NRZ data stream is converted to parallel four-bit signals (rxd0~rxd3).

5.2.3.5 PHY reset

The 10/100M Ethernet physical layer transceiver IP can be reset by pulling the PHY_RSTB_L interface low for 10 ms and then pulling it high. Resetting the transceiver clears and reinitializes registers. The media interface will disconnect and restart the auto-negotiation or parallel detection process.

PHY reset can also be achieved by setting bit 15 of register 0 to 1 (soft reset). See chapter 3.4 for details.

5.2.3.6 Automatic Polarity Correction

The 10/100M Ethernet Physical Layer Transceiver IP automatically corrects polarity errors on the receive pair in 10Base-T mode based on the detection of valid interval link pulses and automatic link pulses. Automatic polarity correction starts during the MDI cross detection phase and is locked when the 10Base-T link is up. Polarity correction is unlocked when the link is down. In 100Base-TX mode, no polarity correction is involved.

LED function

10/100M Ethernet PHY Transceiver IP supports three LEDs in four configurable modes of operation. Three LEDs are driven low during different LED operations. The following sections describe the various LED operations.

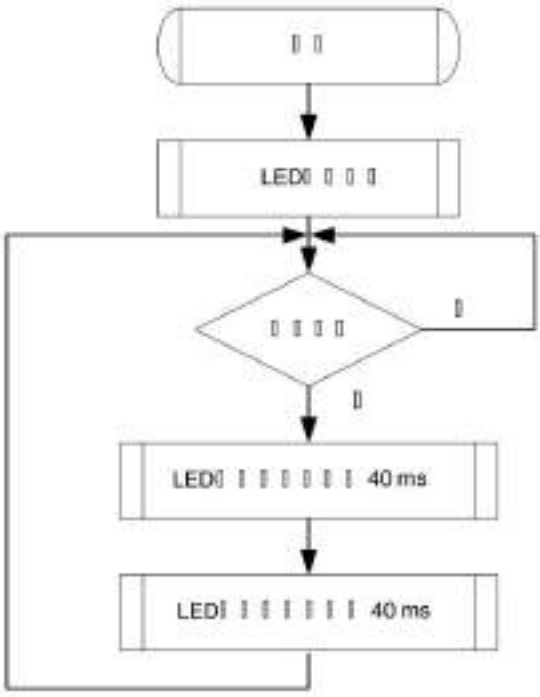
link monitoring

Link monitoring detects link integrity, such as LINK10, LINK100, LINK10/ACT or LINK100/ACT. When link status is established, the specific link LED pin is driven low. Once the cable is disconnected, the link LED pin is driven high to indicate that no network connection exists.

Receive LED

In 10/100M mode, the Receive LED blinks to indicate that data is being received.

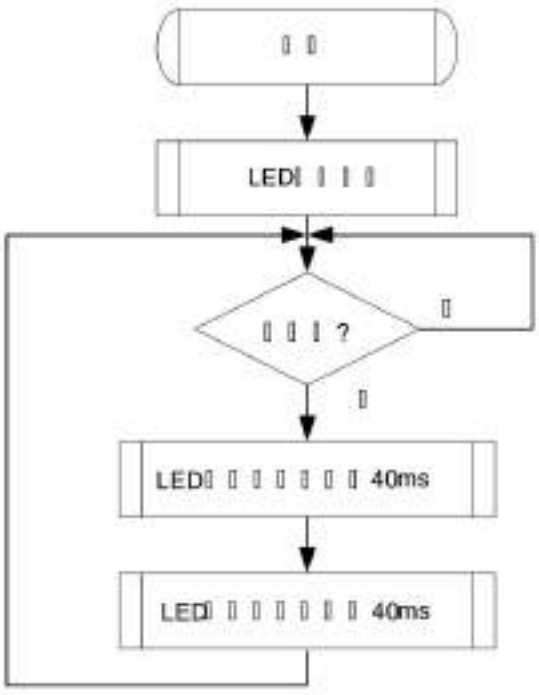
Figure 5-6 Receive LED



Send LED

In 10/100M mode, the send LED blinks to indicate that data is being sent.

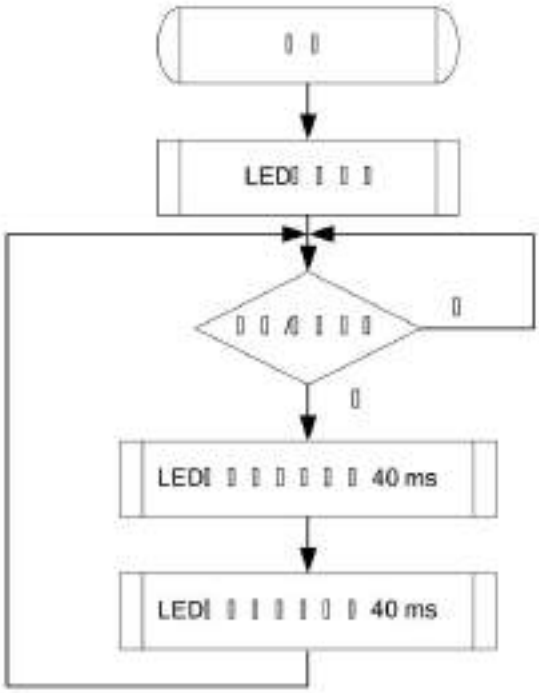
Figure 5-7 Send LED



Send/Receive LED

In 10/100M mode, the send/receive LED blinks to indicate sending/receiving data.

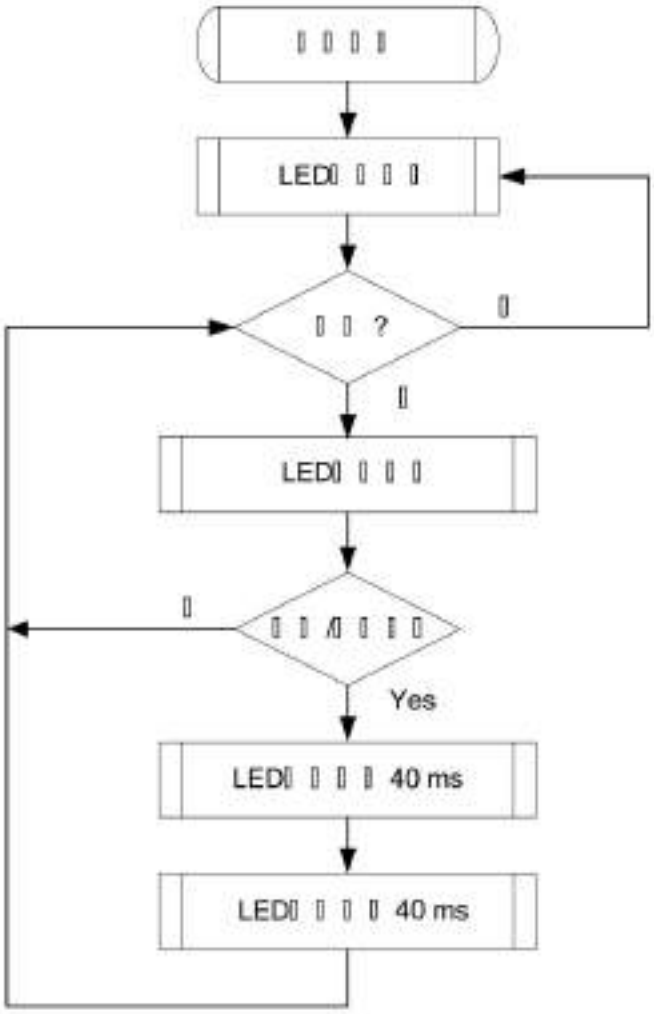
Figure 5-8 Send/Receive LED



Link/Operation LED

In 10/100M mode, the link/operation light flashes to indicate that the 10/100M Ethernet physical layer transceiver IP is connected and operating normally. If the LED is driven high for an extended period of time, there is a link problem.

Figure 5-9 Link/Operation LED

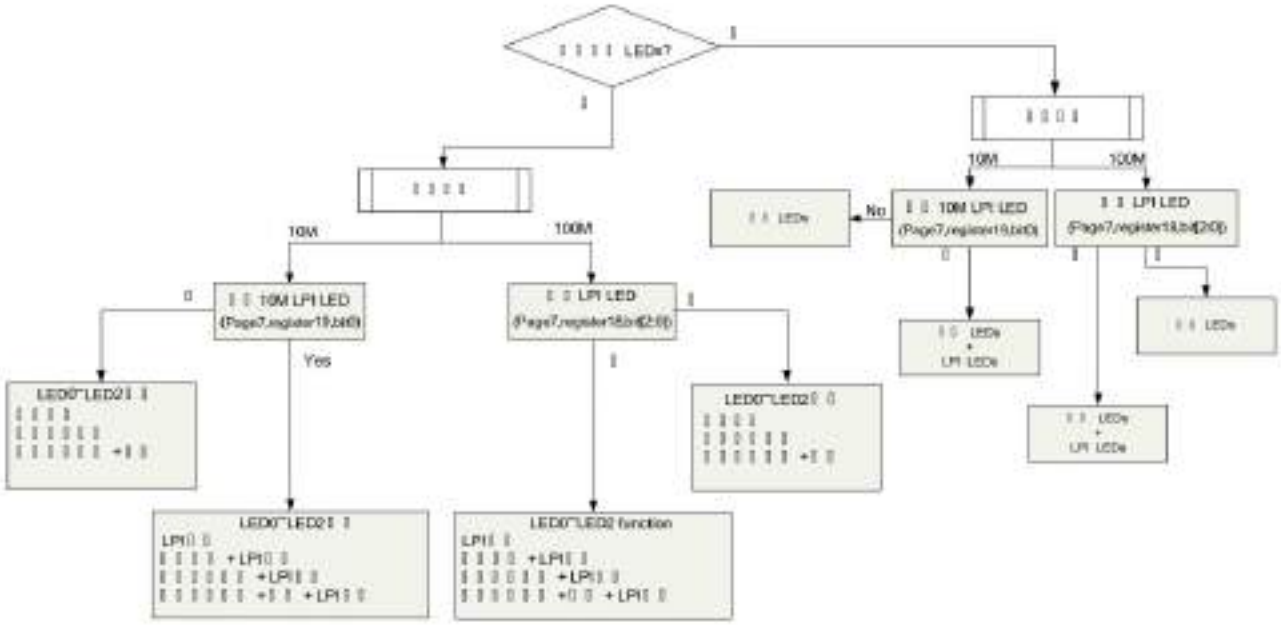


Custom LEDs

10/100M Ethernet PHY Transceiver IP supports programmable LEDs in 10/100 Mbit/s mode. by setting

Set the third bit of register 19 to enable or disable this function.

Figure 5-10 Custom LED with/without LPI LED mode

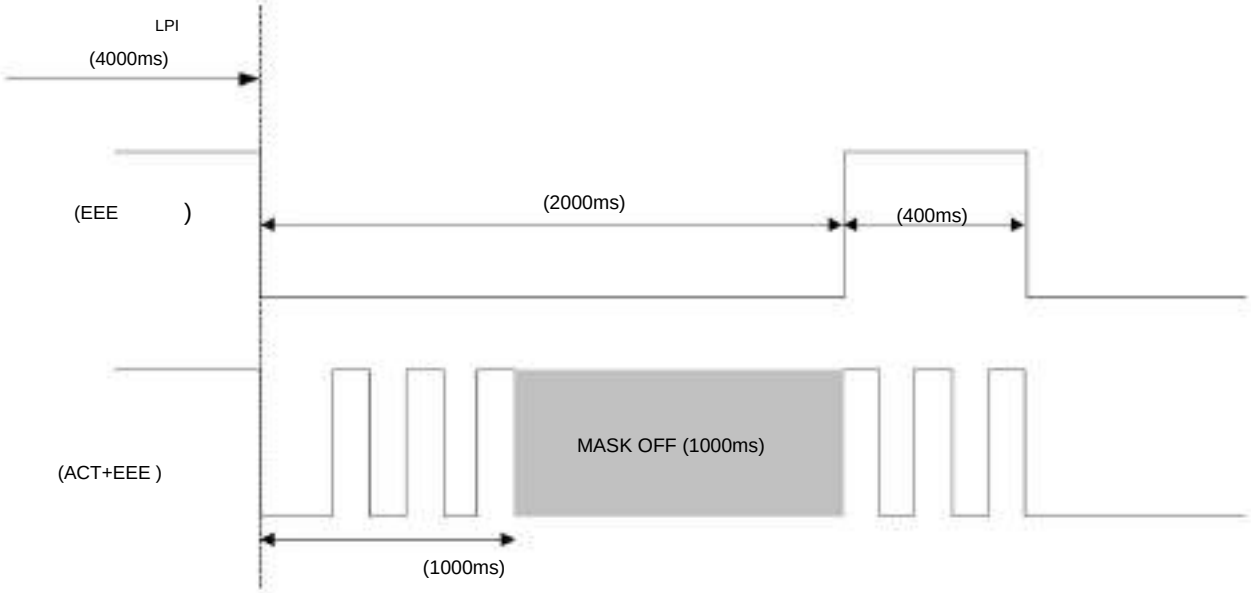


EEE LED operating status

EEE idle mode: LED blinks continuously and slowly.

EEE active mode: LED blinks fast and slow (packets sent and received).

Figure 5-11 EEE LED running status



5.2.3.7 Energy Efficient Ethernet (EEE)

10/100M Ethernet PHY Transceiver IP supports IEEE 802.3az 2010 (also known as Energy Efficient Ethernet) in 10 Mbit/s and 100 Mbit/s modes. The device provides a protocol to coordinate transitions to/from low power levels (low power idle mode) based on link utilization. When no data packets are sent, the system enters the low-power idle mode. When a packet needs to be sent, the system reverts to normal mode without changing the link state and without dropping/destroying frames.

To save power, most circuits are disabled when the system is in low-power idle mode. However, the transition time from low-power idle mode is small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method that enables a link partner to determine whether it supports EEE.

For EEE capability, the MAC may assert/deassert transmit LPI. For EEE

capabilities, the PHY may assert/deassert receive LPI. For EEE

capability, the PHY can use the asserted CRS (defined as EEE CRS) to advertise that the MAC is still asserting to send LPI, and use the deasserted CRS to notify the MAC that it can send packets because the MAC has deasserted sending LPI, and the PHY wake-up timer has expired.

MAC does not support EEE and there is no signaling for LPI. However, when there is no traffic, the only thing a buffered PHY can do is generate a send LPI request.

For EEE capabilities, the PHY may assert/deassert receive LPI.

MAC does not support EEE and does not require EEE CRS from PHY.

5.2.4 Register overview

The register overview is shown in Table 5-11 .

Table 5-11 Register overview

offset address	name	describe	page number
0x0	BMCR	Basic Mode Control Register	5-81
0x1	BMSR	Basic Mode Status Register	5-83
0x2	PHYID1	PHY Identification Register 1	5-85
0x3	PHYID2	PHY Identification Register 2	5-85
0x4	ANAR	Auto-Negotiation Notification Register	5-86
0x5	APPROACHES	Auto-Negotiation Link Party Capability Register	5-87
0x6	OTHER	Auto-Negotiation Extension Register	5-88
0xD	MACR	MMD access control register	5-89
0xE	MADDR	MMD access address data register	5-89
0x18	PSMR	Power Saving Mode Register	5-90
0x1C	LPM	loopback register	5-90
0x1E	IN	Interrupt indication and signal-to-noise ratio display register	5-91

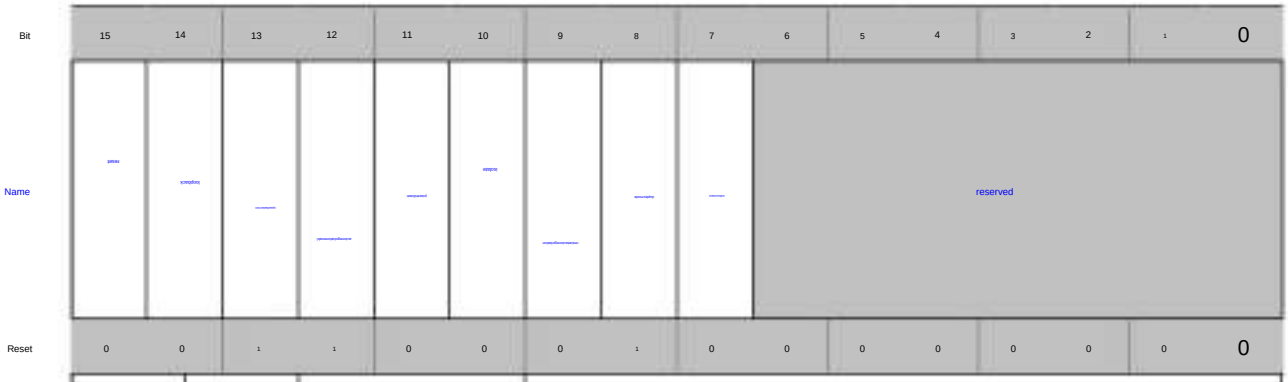
offset address	name	describe	page number
0x1F	PGSEL	page select register	5-91
device3_0x0	EEEPC1R	PCS control register (MMD device No. 3, address: 0x00)	5-92
device3_0x1	EEEPS1R	PCS status register (MMD device No. 3, address: 0x01)	5-92
device3_0x14	EEECR	EEE Capability Register (MMD Device No. 3; Address: 0x14)	5-93
device3_0x16	EVER	EEE Wakeup Error Register (MMD Device No. 3; Address: 0x16).	5-93
device7_0x3C	EEEAR	EEE Notification Register (MMD Device No. 7; Address: 0x3C).	5-94
device7_0x3D	EEELPAR	EEE Link Party Capability Register (MMD Device No. 7; Address: 0x3D).	5-94

5.2.5 Register description

BMCR

BMCR is the basic mode control register.

Offset Address	Register Name	Total Reset Value
0x0	BMCR	0x3100



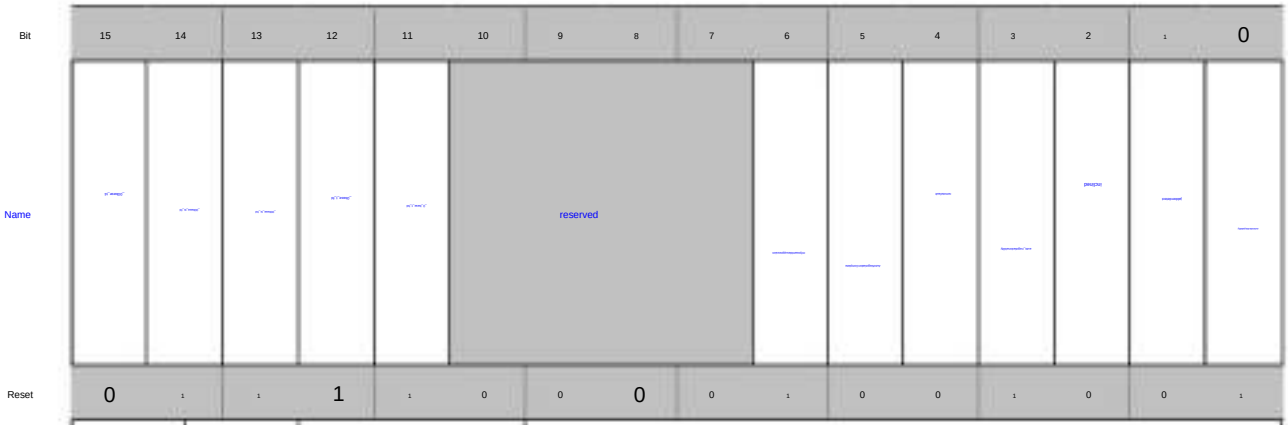
Bits	Access	Name	Description
[15]	RWSC	reset	Sets the status and control registers of the PHY in its default state. This bit is self-clearing. 0: normal operation; 1: Soft reset. Registers 0 and 1 are restored to default values after software reset (set bit[15] to 1). This operation may change the state of the internal PHY and the state of the physical link associated with the internal PHY.
[14]	RW	loopback	Enables 4 bits (txd0~txd3) of transmit data looping back to the receive data path. 0: normal operation; 1: enable loopback.
[13]	RW	speedselection	Set the network speed. 0ÿ10 Mbit/sÿ 1ÿ100 Mbit/sÿ After the auto-negotiation is completed, this bit reflects the status of the network speed. 0ÿ10Base-Tÿ 1ÿ100Base-Tÿ
[12]	RW	transmission mode	Auto-negotiation enable control. 0: Disable auto-negotiation. Bit[13] and bit[8] are used to determine the link speed and data respectively; autonegotiationena bl 1: enable automatic negotiation. bit[13] and bit[8] are ignored. Note: After disabling auto-negotiation and setting bit[13] and bit[8] to determine the link speed, set bit[15] to 1 for software reset.
[11]	RW	powerdown	Turn off the power of the PHY chip. MDC and MDIO are still powered and can be used to access the MAC. 0: normal operation; 1: Power off.

[10] RW isolate			0: Normal operation; when this field is enabled or disabled, the MII transmits and receives data with a one-cycle glitch. 1: Galvanic isolation of PHY and MII. The PHY can still respond to MDC or MDIO.
[9]	RWSC	restartautonegotiati 0: on	normal operation; 1: Reset autonegotiation. restart autonegotiation.
[8] RW duplexmode			When auto-negotiation is disabled (bit[12]=0), this bit is used to set the duplex mode. 0: half duplex; 1: Full duplex. After auto-negotiation is completed, this bit reflects the duplex status. 0: half duplex; 1: Full duplex.
[7] RW collisiontest			crash test. 0: normal operation; 1: Enable bump test. Setting this field causes the COL signal to be pulled high in response to TXEN within 512 bits. This signal will be pulled low in response to TXEN being pulled low within 4 bit times.
[6:0] RW reserved			reserve.

BMSR

BMSR is the base mode status register.

Offset Address: 0x1 | Register Name: BMSR | Total Reset Value: 0x7849



Bits	Access	Name	Description
[15]	RO	_00base_t4	0: Disable 100Base-T4; 1: Enable 100Base-T4.
[14]	RO	_00base_tx_fd	0: Disable 100Base-TX full duplex; 1: Enable 100Base-TX full duplex.
[13]	RO	_00base_tx_hd	0: disable 100Base-TX half-duplex; 1: Enable 100Base-TX half-duplex.
[12]	RO	_0base_t_fd	0: disable 10Base-T full duplex; 1: enable 10Base-T full duplex.
[11]	RO	_0_base_t_hd	0: disable 10Base-T half-duplex; 1: Enable 10Base-T half-duplex.
[10:7]	RO	reserved	reserve.
[6]	RO	frames mfpreamblesuppression	By suppressing the preamble, the PHY can receive MDIO After reset, the first MDIO operation requires at least 32 preamble bits. According to the sion IEEE802.3u specification, one bit idle time is required between any two MDIO operations.
[5]	RW	completed; AutoNegotiationComplete	0: Auto-negotiation not 1: Auto-negotiation completed.
[4]	RC	remotefault	0: no remote fault detected; 1: Remote fault detected (read to clear).
[3]	RO	negotiation; auto_negotiationability	0: PHY cannot perform auto- 1: PHY can perform auto-negotiation.

[2]	RO	inclined	0: no valid link established; 1: valid link established. This bit indicates whether the link has been lost since the last read. Read this register twice to get the current link status.
[1]	RO	jabberdetect	0: Timeout transmission not detected; 1: Timeout transmission detected.
[0]	RO	extendedcapability	0: Non-extendable register capability; 1: Extensible register capability (permanently=1).

PHYID1

PHYID1 is the PHY identification register 1.

Offset Address	Register Name	Total Reset Value
0x2	PHYID1	0x001C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Yes															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[15:0]	RO	Yes	Consists of bits 6 to 21 of the Organizationally Unique Identifier (OUI), respectively.

PHYID2

PHYID2 is the PHY identification register 2.

Offset Address	Register Name	Total Reset Value
0x3	PHYID2	0xC816

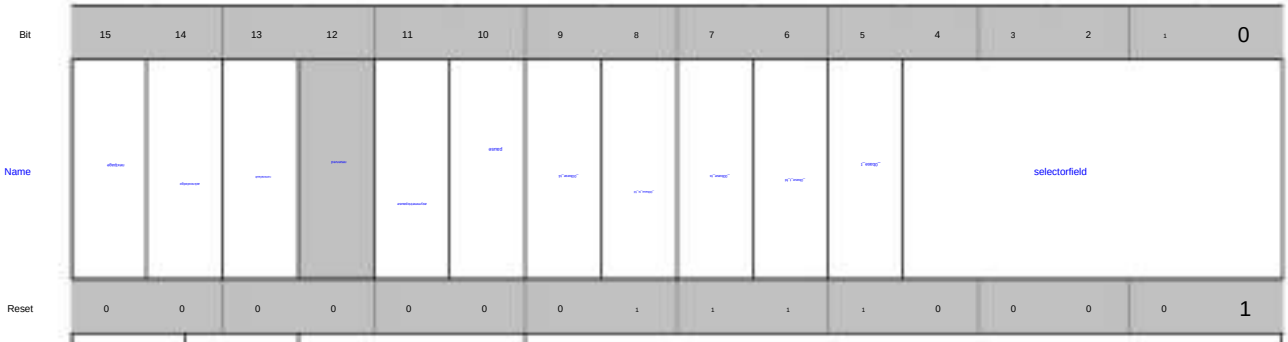
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	yes_lsb						modelnumber						revisionnumber			
Reset	1	1	0	0	1	0	0	0	0	0	0	1	0	1	1	0

Bits	Access	Name	Description
[15:10]	RO	yes_lsb	Assigned to bits 0 to 5 of the OUI.
[9:4]	RO	modelnumber	model.
[3:0]	RO	revisionnumber	The revision number.

ANAR

ANAR is the Auto-Negotiation Notification Register.

Offset Address	Register Name	Total Reset Value
0x4	ANAR	0x01E1



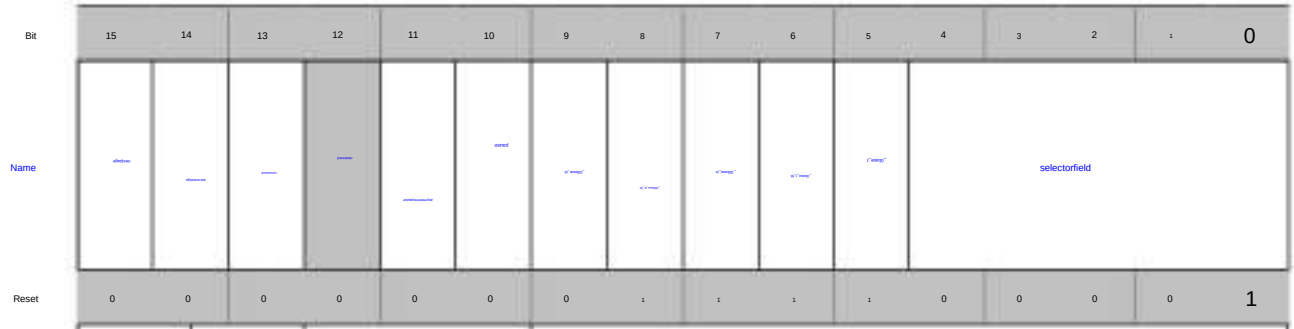
Bits	Access	Name	Description
[15]	RW	nextpage	next page bit. 0: transmit the main capability data page; 1: Transfer protocol-specific data pages.
[14]	RO	acknowledge	0: Do not confirm the ability of the receiver; 1: Confirm the capability of the receiver.
[13]	RW	remotefault	0: Do not notify the remote fault detection capability; 1: Advertise remote fault detection capabilities.
[12]	RO	reserved	reserve.
[11]	RW	asymmetricpause	0: Notify that asymmetric pause frames are not supported; 1: Notify that asymmetric pause frames are supported.
[10]	RW	pause	0: Layer 2 MAC has no flow capability; 1: Advertise the Layer 2 MAC with flow control capability.
[9]	RO	_00base_t4	0: The local node does not support 100Base-T4; 1: The local node supports 100Base-T4.
[8]	RW	_00base_tx_fd	0: The local node does not support 100Base-TX full duplex; 1: The local node supports 100Base-TX full duplex.
[7]	RW	_00base_tx	0: The local node does not support 100Base-TX; 1: The local node supports 100Base-TX.
[6]	RW	_0base_t_fd	0: The local node does not support 10Base-T full duplex; 1: The local node supports 10Base-T full duplex.
[5]	RW	_0base_t	0: The local node does not support 10Base-T; 1: The local node supports 10Base-T.

[4:0] RO		selectorfield	A selector for binary encodings supported by this node. Currently only CSMA/CD 00001 is specified. Other protocols are not supported.

APPROACHES

ANLPAR is the Auto-Negotiation Link Party Capability Register.

Offset Address	Register Name	Total Reset Value
0x5	APPROACHES	0x01E1



Bits	Access	Name	Description
[15]	RW	nextpage	next page bit. 0: transmit the main capability data page; 1: Transfer protocol-specific data pages.
[14]	RW	acknowledge	0: Do not confirm the ability of the receiving link party; 1: Confirm the ability of the receiving link party.
[13]	RW	remotefault	0: Do not advertise the remote fault detection capability; 1: Notify the remote fault detection capability.
[12]	RO	reserved	reserve.
[11]	RW	asymmetricpause	0: Notify that asymmetric pause frames are not supported; 1: Notify that asymmetric pause frames are supported.
[10]	RW	pause	0: Layer 2 MAC has no flow capability; 1: Advertise the Layer 2 MAC with flow control capability.
[9]	RO	_00base_t4	0: The local node does not support 100Base-T4; 1: The local node supports 100Base-T4.
[8]	RW	_00base_tx_fd	0: The local node does not support 100Base-TX full duplex; 1: The local node supports 100Base-TX full duplex.
[7]	RW	_00base_tx	0: The local node does not support 100Base-TX; 1: The local node supports 100Base-TX.

[6] RW _0base_t_fd			0: The local node does not support 10Base-T full duplex; 1: The local node supports 10Base-T full duplex.
[5] RW _0base_t			0: The local node does not support 10Base-T; 1: The local node supports 10Base-T.
[4:0] RW selectorfield			A selector for binary encodings supported by this node. Currently only CSMA/CD 00001 is specified. Other protocols are not supported.

OTHER

ANER is the auto-negotiation extension register.

Offset Address: 0x6 | Register Name: OTHER | Total Reset Value: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:5] RO		reserved	reserve.
[4]	RC	parallel detectionfau lt	1: 0: No fault detected by parallel detection function; Fault detected by parallel detection function.
[3] RW		page ability; linkpartnernextpage ability	0: The link partner does not have the next 1: The link partner has the next page ability.
[2] RW		localnextpageabilit y	1: 0: The local node has no next page capability; The local node has the next page capability. the
[1]	RC	pagereceived	0: A new page has not been received; 1: A new page has been received.

[0] RW		as follows: linkpartnerauto_ne gotiationability	If auto-negotiation is enabled. The bit is defined 0: The link party does not have auto-negotiation capability; 1: The link party has auto-negotiation capability.

MACR

MACR is MMD access control register.

Offset Address	Register Name	Total Reset Value
0xD	MACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	function		reserved								Devad					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[15:14]	WO	function	00: address; 01: data, no post-increment; 10: Data, both reading and writing have post-increment; 11: Data, only write operations have a post-increment.
[13:5]	RO	reserved	reserve.
[4:0]	WO	devad	device address.

MADDR

MADDR is MMD access address data register.

Offset Address	Register Name	Total Reset Value
0xE	MADDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addressdata															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[15:0]	RW	addressdata	When bit[15:14] = 00, bit[13:0] indicates MMD DEVAD address; when bit[15:14] = 01, 10 or 11, bit[13:0] indicates MMD DEVAD data, by its Address register content indication.

PSMR

PSMR is the power saving mode register.

Offset Address: 0x18 | Register Name: PSMR | Total Reset Value: 0x8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved														
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	enpwrsave	Enable power saving mode.
[14:0]	RO	reserved	reserve.

LPM

LPM is the loopback register.

Offset Address: 0x1C | Register Name: LPM | Total Reset Value: 0x0006

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													[illegible]	[illegible]	[illegible]
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[15:3]	RO	reserved	reserve.
[2]	RW	en_automdix	Enable auto MDIX function.
[1]	RW	force_mdi	Force start of MDI/MDIX mode. If the automatic MDIX function is enabled, this field is set as follows: 0: Forced to start MDIX mode; 1: Forcibly start MDI mode.

[0]	RO	reserved	reserve.

IN

INTR is an interrupt indicator and signal-to-noise ratio display register.

Offset Address	Register Name	Total Reset Value
0x1E	IN	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reserved						snr_o			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RC	anerr	Autonegotiation error abort.
[14]	RC	spdchg	Speed mode change interrupt.
[13]	RC	duplexchg	Duplex mode change interrupt.
[12]	RO	reserved	reserve.
[11]	RC	linkstatuschg	Link status change interrupt.
[10:4]	RO	reserved	reserve.
[3:0]	RO	snr_o	These 4 bits show the SNR value.

PGSEL

PGSEL is the page select register.

Offset Address	Register Name	Total Reset Value
0x1F	PGSEL	0x0000

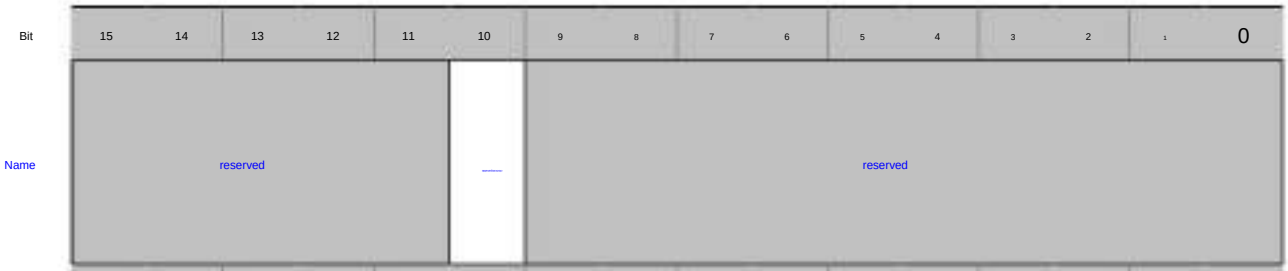
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pagesel							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	reserve.
[7:0]	RW	pagesel	Selected page address range: 00000000~11111111.

EEEPC1R

EEEPC1R is the PCS control register (No. 3 MMD device, address: 0x00).

Offset Address	Register Name	Total Reset Value
device3_0x0	EEEPC1R	0x0000

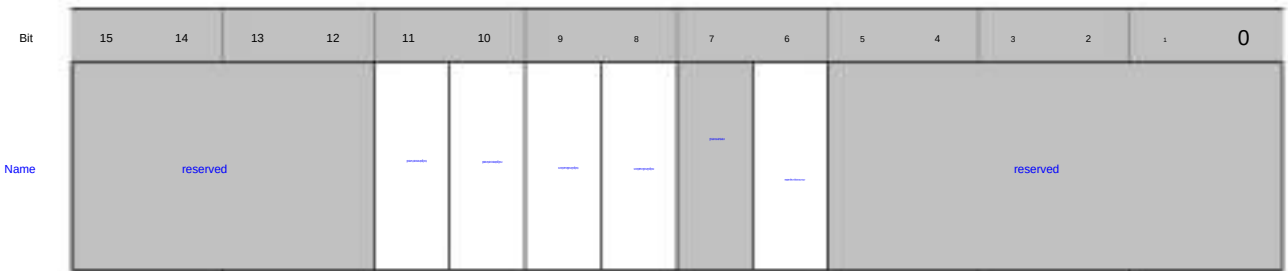


Bits	Access	Name	Description
[15:11]	RW	reserved	reserve.
[10]	RW	clockstopenable	0: RXC does not stop sending RXC stop (default value); 1: PHY stops sending RXC at LPI.
[9:0]	RW	reserved	reserve.

EEEPS1R

EEEPS1R is the PCS status register (No. 3 MMD device, address: 0x01).

Offset Address	Register Name	Total Reset Value
device3_0x1	EEEPS1R	0x0000



Bits	Access	Name	Description
[15:12]	RO	reserved	reserve.
[11]	RO	txlpireceived	0: send PCS but not receive LPI; 1: Sending PCS has received LPI.

[10] RO		rxlpireceived	0: The receiving PCS has not received the LPI; 1: The receiving PCS has received the LPI.
[9]	RO	txlpiindication	0: Sending PCS is not receiving LPI; 1: Transmitting PCS is receiving LPI.
[8]	RO	rxlpiindication	0: The receiving PCS is not receiving LPI; 1: The receiving PCS is receiving LPI.
[7]	RO	reserved	reserve.
[6]	RO	clockstopcapable	0: Set TXC to "unstoppable" (the component of TXC is RL6307); 1: Stop sending TXC in LPI.
[5:0] RO		reserved	reserve.

EEECR

EEECR is the EEE capability register (MMD device no. 3; address: 0x14).

Offset Address	Register Name	Total Reset Value
device3_0x14	EEECR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access Name		Description
[15:2] RO		reserved	reserve.
[1]	RO	_00base_txeee	0: does not support 100Base-TX EEE; 1: Support 100Base-TX EEE.
[0]	RO	reserved	reserve.

EVER

EEEWER is the EEE wakeup error register (MMD device No. 3; address: 0x16).

Offset Address	Register Name	Total Reset Value
device3_0x16	EVER	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eeewake error counter															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[15:0] RC	because the r eeewakeerrorcounte	Used by PHYs that support EEE to count wake-up time errors. These errors are generated PHY cannot complete its normal timing within the time required by the specific type of PHY.

EEEAR

EEEAR is the EEE notification register (MMD device No. 7; address: 0x3C).

Offset Address	Register Name	Total Reset Value
device7_0x3C	EEEAR	0x0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name	Description
[15:2] RW	reserved	reserve.
[1] RW	_00base_txeee	100Base-TX EEE capability notification control. 0: no notification; 1: Notify.
[0] RW	reserved	reserve.

EEELPAR

EEELPAR is the EEE linker capability register (MMD device No. 7; address: 0x3D).

Offset Address	Register Name	Total Reset Value
device7_0x3D	EEELPAR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[15:2] RO		reserved	reserve.
[1]	RO	lp100base_txeee	0: The linker does not support 100Base-TX EEE; 1: The link side supports 100Base-TX EEE.
[0]	RO	reserved	reserve.

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6 video encoding

6.1 Overview

The video encoding unit is a multi-protocol encoder supporting H.264/JPEG, including VENC and JPGE. Among them, VENC realizes the encoding of H.264 protocol, and JPGE realizes the encoding of JPEG protocol.

6.2 SALE

6.2.1 Overview

VENC (Video Encode Unit) is a hardware-implemented encoder that supports the H.264 video standard. VENC has the advantages of low CPU usage, small bus bandwidth, low latency, and low power consumption.

6.2.2 Features

VENC encoders have the following features:

Support ITU-T H.264 High Profile/Main Profile/Baseline Profile@Leve4.2 encoding

ÿSupport 1/2, 1/4 pixel precision motion compensation

ÿSupport inter-frame prediction 16x16, 16x8, 8x16, 8x8 four sub-block types ÿSupport all

Intra4x4, Intra8x8, Intra16x16 prediction modes

ÿSupport Trans4x4, Trans8x8

ÿSupport CABAC, CAVLC entropy coding ÿSupport

De-blocking filter ÿSupport I_PCM

coding

Supported input image format: Semi-Planar YCbCr4:2:0 H.264 Video

encoding performance: ÿ

16xD1@6fps+8CIF@6fps encodingÿ 16xCIF

@30fps+8QCIF@30fps encodingÿ 8xD1

@30fps+4CIF@30fps encodingÿ 8x960H @

30fps+4CIF@30fps encoding

Support image resolution configurable

ÿ Minimum image resolution: 160x64

ÿ Maximum image resolution: 1920x2048

ÿ The configuration step of image width/height is 4

Support for region of interest coding

ÿSupports coding of interest for up to 8 regions ÿCoding of

interest function enables/disables support for OSD

region coding protection

OSD area coding protection function can enable/disable support

video front-end OSD overlay processing

ÿSupport pre-encoding OSD overlay of up to 8 regions ÿSupport OSD

overlay at any position and the maximum image size ÿSupport 129-level alpha overlay

ÿ OSD overlay function can be enabled/disabled

Support CBR/VBR two code rate control modes Output code

rate range: 2kbpsÿ40Mbps

6.2.3 Functional description

The functional block diagram of VENC is shown in Figure 6-1 .

VENC encoding realizes protocol/algorithm processing such as motion estimation/inter prediction, intra prediction, motion vector prediction, transformation/quantization, inverse quantization/inverse transformation, VLC (Variable Length Code) encoding and code stream generation, de-blocking filtering, etc. , ARM software completes encoding control processing such as code rate control and interrupt processing.

Before starting VENC for video encoding, the software needs to allocate the following three types of buffers in the external memory (DDR SDRAM).

input image buffer

VENC will read the original image to be encoded from this buffer during the encoding process. This buffer is usually written by the video input unit. Reconstructed image/

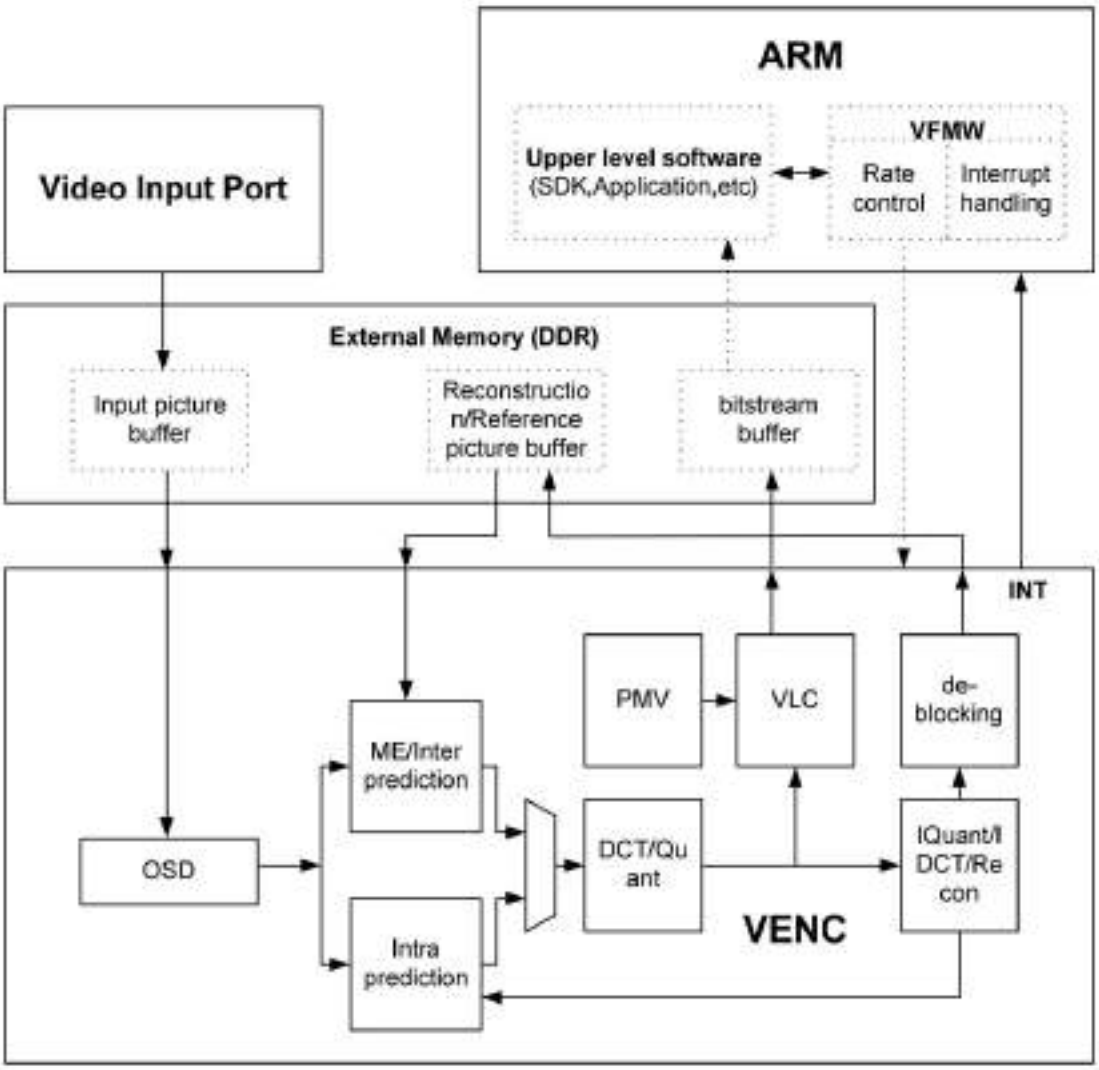
reference image buffer

During the encoding process, VENC will write the reconstructed image into the buffer as the reference image of the subsequent image, and read the reference image from the buffer when encoding the P frame.

stream buffer

The buffer is used to store the encoded output code stream. VENC will write the code stream into this buffer during the encoding process. This buffer is normally read by software.

Figure 6-1 Functional block diagram of VENC encoding



6.3 JPGE

6.3.1 Overview

JPGE (JPEG Encoder) is a hardware-implemented high-performance JPEG encoder, which can realize up to 67.1M pixel picture capture or high-definition image MJPEG encoding business.

6.3.2 Features

JPGE has the following characteristics:

Support ISO/IEC 10918-1 (CCITT T.81) Baseline Process (DCT Sequential) encoding Support YCbCr4:2:0, YCbCr4:2:2, YCbCr4:4:4 image encoding in three chroma sampling formats

The MCU adopts the interleaved sequence organization to support the following input image formats:

ÿ Planar YCbCr4:2:0

ÿ Planar YCbCr4:2:2

ÿ Planar YCbCr4:4:4

ÿ Semi-Planar YCbCr4:2:0

ÿ Semi-Planar YCbCr4:2:2

ÿ PackageYUYV

The highest performance can reach 67.1M (8192x8192) pixel/s Support

image resolution can be configured

ÿMinimum image resolution: 64x64

ÿMaximum image resolution: 8192x8192

Image width/height is configured in steps of 4

Quantization tables are configurable

Each of the three components of Y, Cb, and Cr provides a quantization

table to support video front-end OSD overlay processing

ÿSupport pre-encoding OSD overlay of up to 8 regions

ÿSupport OSD overlay of any size and position (not exceeding image size and position)

ÿSupport 129-level alpha overlay

ÿ OSD overlay function can be enabled/disabled

6.3.3 Functional description

The JPGE function is shown in Figure 6-2 .

It can be seen from the figure that the JPGE hardware implements protocol processing with a large amount of computation, such as OSD, level shift, DCT, quantization, scanning, VLC encoding, and code stream generation, while the ARM software completes encoding control processing such as quantization table configuration and interrupt processing.

Before starting JPGE for video encoding, the software needs to allocate the following two types of buffers in the external memory (DDR SDRAM):

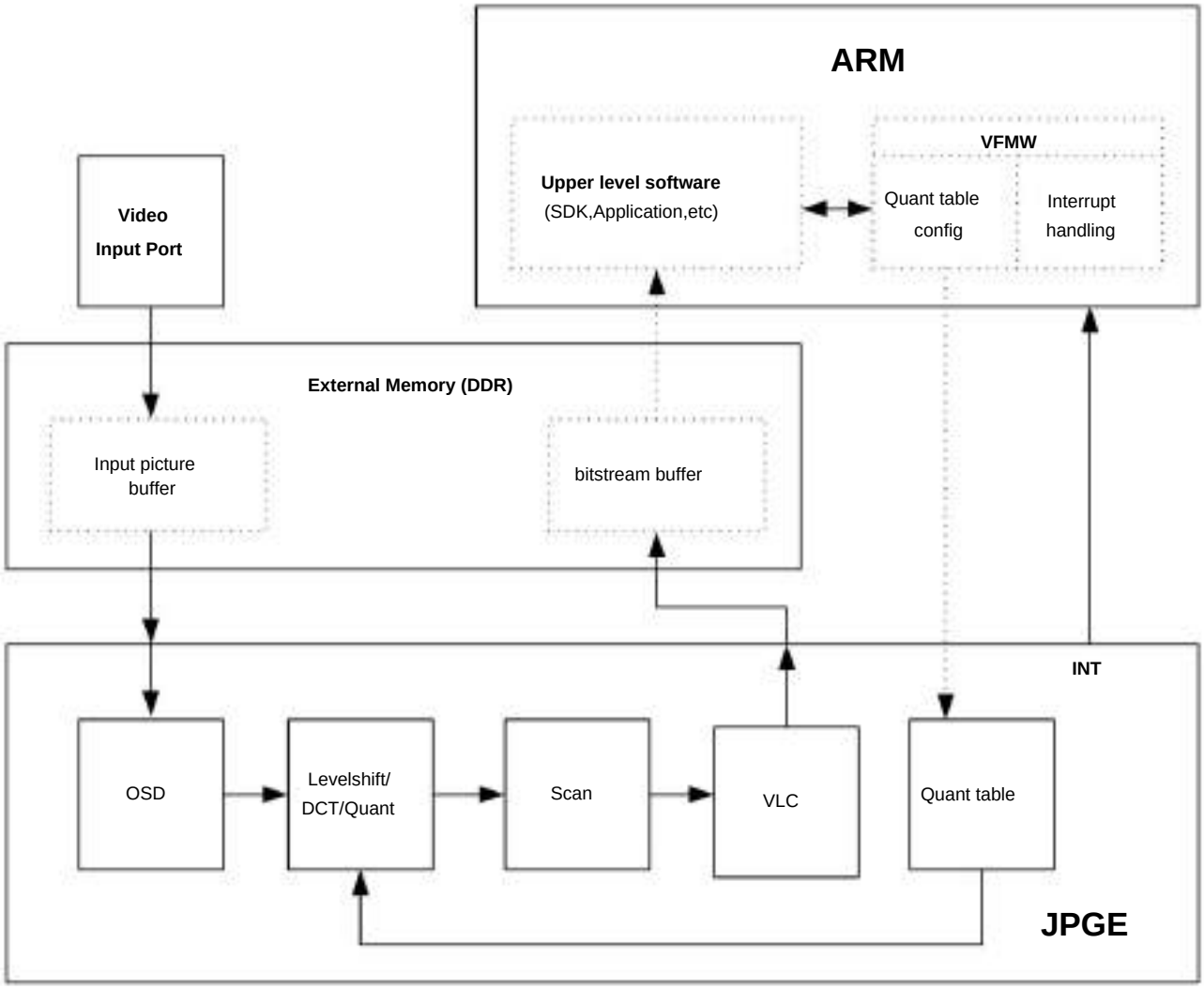
input image buffer

JPGE reads the raw image to be encoded from this buffer during the encoding process. This buffer is usually written by the video input unit.

stream buffer

The buffer is used to store the encoded output code stream. JPGE writes the codestream to this buffer during encoding. This buffer is normally read by software.

Figure 6-2 JPGE functional block diagram



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7 video decoding

7.1 VDH

7.1.1 Overview

The video decoder is composed of VFMW (Video Firmware) running on the ARM processor and the embedded hardware video decoding engine VDH. VFMW obtains the code stream from the upper layer software, analyzes the code stream and invokes VDH to generate a decoded image sequence. The decoded image sequence is output to the monitor or other devices by VDP under the control of the upper layer software.

7.1.2 Functional description

The video codec has the following characteristics:

Support ITU-T H.264 High Profile/Main Profile/Baseline Profile@Leve4.2 decoding

ÿSupport 1/2, 1/4 pixel precision motion compensation

ÿSupport inter-frame prediction 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4 and other sub-block types ÿSupport all Intra4x4,

Intra8x8, Intra16x16 prediction modes

ÿSupport Trans4x4, Trans8x8

ÿSupport CABAC, CAVLC entropy decoding ÿ Support

De-blocking filter ÿSupport I_PCM decoding

ÿDo not support ASO/FMO ÿDo

not support B slice decoding ÿDo

not support field decoding ÿDo not

support MBAFF

ÿ Weighted forecasting is not supported

H.264 video decoding performance:

ÿ 16xD1@6fps+8CIF@6fps decodingÿ 16xCIF

@30fps+8QCIF@30fps decodingÿ 8xD1 @30fps+4CIF@30fps

decodingÿ 8x960H@30fps+4CIF@30fps decoding

ÿ 4x720P@30fps H.264 decoding

Supported image resolution

ÿ Minimum image resolution: 80x64 ÿ Maximum

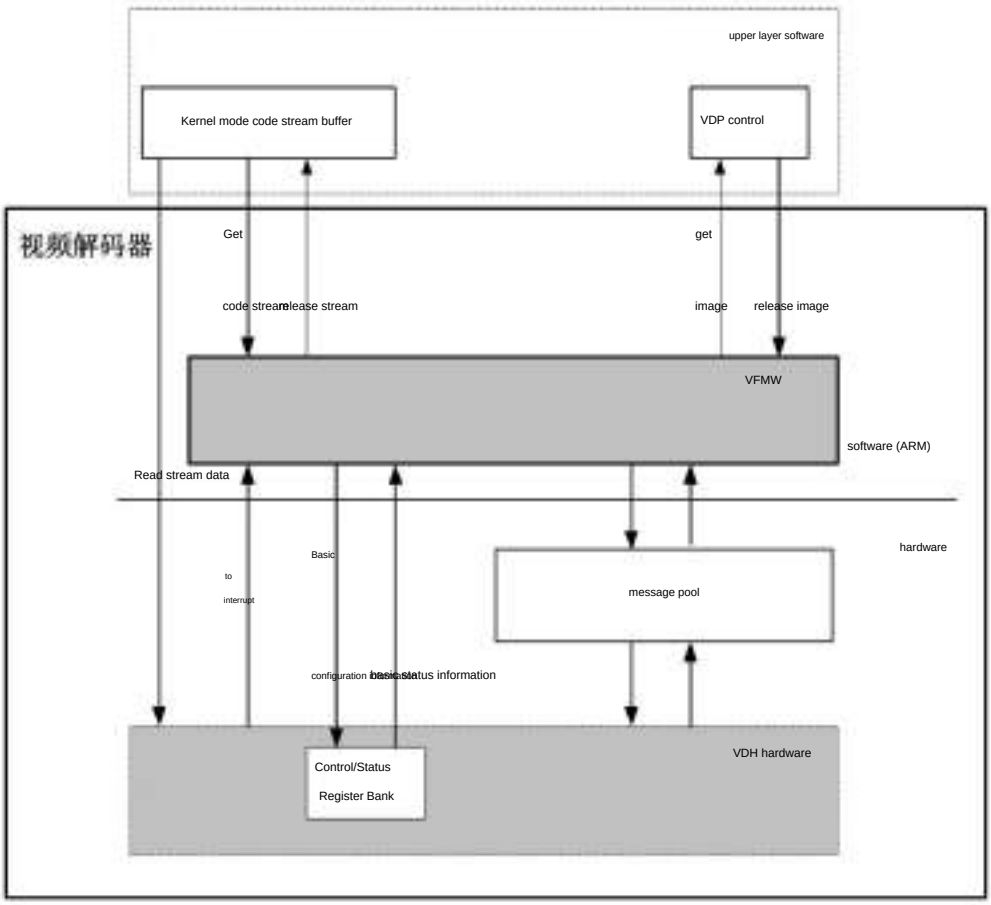
image resolution: 1920x2048

Support the reporting function of the whole frame brightness statistics information

7.1.3 Working method

The video decoder architecture is shown in Figure 7-1 .

Figure 7-1 Video decoder architecture



VDH: Video Decoding Module For High Definition, high-definition video decoding module.

VFMW: Video Firmware, video firmware, is actually a software component running on the main processor, responsible for scheduling the video decoding engine to complete video decoding. Message pool: the storage space for

information exchange between VFMW and VDH, which is opened in the external SDRAM memory and can be read and written by VDH and VFMW.

VDH and VFMW interaction mode:

The H264 protocol interacts with a batch of slices to complete the decoding, and VFMW completes the decoding of the slice header and above.

VDH hardware completes the decoding of slice data and below;

Video decoding steps are as follows:

Step 1 Create and initialize the decoder.

Step 2 Store the code stream into the code stream buffer.

Step 3 Get images through the image output interface of VFMW.

Step 4 After the image is displayed, release the image through the image recovery interface of VFMW.

Step 5 Repeat steps 2 to 4 until the code stream decoding is completed.

Step 6 After playing, destroy the decoder.

----Finish

7.2 JPGD

7.2.1 Overview

JPGD is a JPEG (Joint Picture Expert Group) static image decoding module, the function of this module is to support Decoding of JPEG/Motion-JPEG images.

7.2.2 Functional description

The JPGD module has the following features:

AXI interface is supported.

Interrupts are

supported. Partially supports ITU-T81 Baseline profile decoding. That is:

ÿSupport YUV three-component JPEG image decoding, support YUV 4:0:0, YUV4:2:0, YUV4:2:2 1x2, YUV4:2:2 2x1, YUV 4:4:4 five formats.

ÿMaximum 4 Huffman tables are supported, including 2 DC tables and 2 AC tables.

ÿUp to 3 quantization tables are supported.

ÿSupport sequential format decoding. ÿSupport

JPEG format decoding based on DCT transformation. ÿSupports 8bit

sampling precision. ÿSupport interleaved

scan mode. Support frequency domain

scaling of three scales of 1/2, 1/4, and 1/8. The maximum supported

resolution is 8192 x 8192 for static image decoding, and the minimum supported resolution is 1 x 1 for static image decoding. The maximum output storage format that

supports semi-planar is 8192 x 8192. Support segmented decoding of compressed code

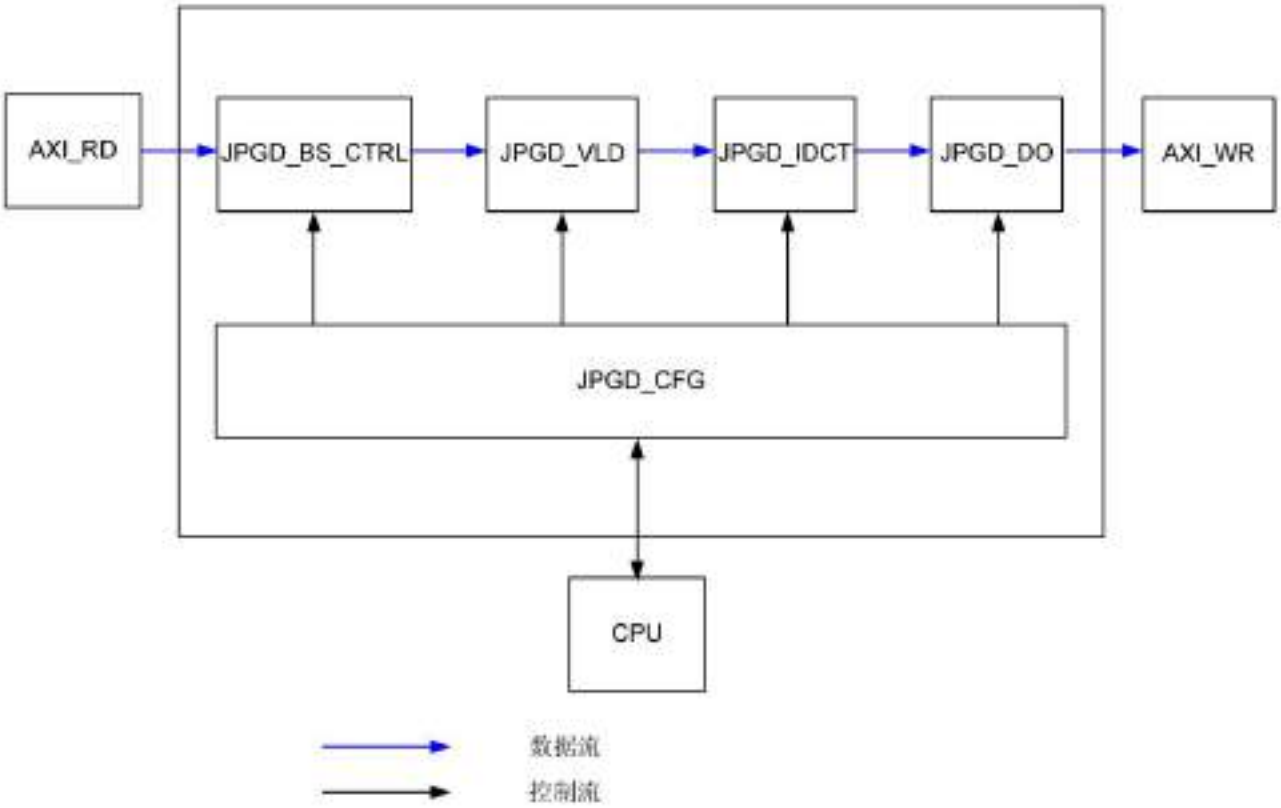
stream. It provides 40Mpixel/s or 3-way

Motion-JPEG D1 30fps decoding capability, and can be used in various decoding systems that have high requirements for real-time performance. Supports frequency domain

scaling, which greatly reduces memory and bandwidth usage during decoding.

The overall structure of JPGD is shown in Figure 7-2 .

Figure 7-2 JPGD overall structure diagram



JPGD internal module description is shown in Table 7-1 .

Table 7-1 JPGD internal module description

module name	Function
JPGD_BS_CTRL code stream reading and shift processing, including a Barrel-Shift, will send the effective code stream to the downstream module for decoding.	
JPGD_VLD	Huffman variable length code decoding, while descanning and dequantizing the decoded coefficients.
JPGD_IDCT performs IDCT transformation and frequency domain compression.	
JPGD_DO	Responsible for storing the decoded data into the specified memory space.
JPGD_CFG receives the configuration information of HOST, and configures the configuration information to each functional module. At the same time, it is responsible for starting the entire decoder, generating interrupts and feeding back the internal state of the decoder to HOST.	

7.2.3 Working method

7.2.3.1 Software and hardware division

The JPEG stream structure is shown in Figure 7-3 .

Figure 7-3 JPEG stream structure diagram

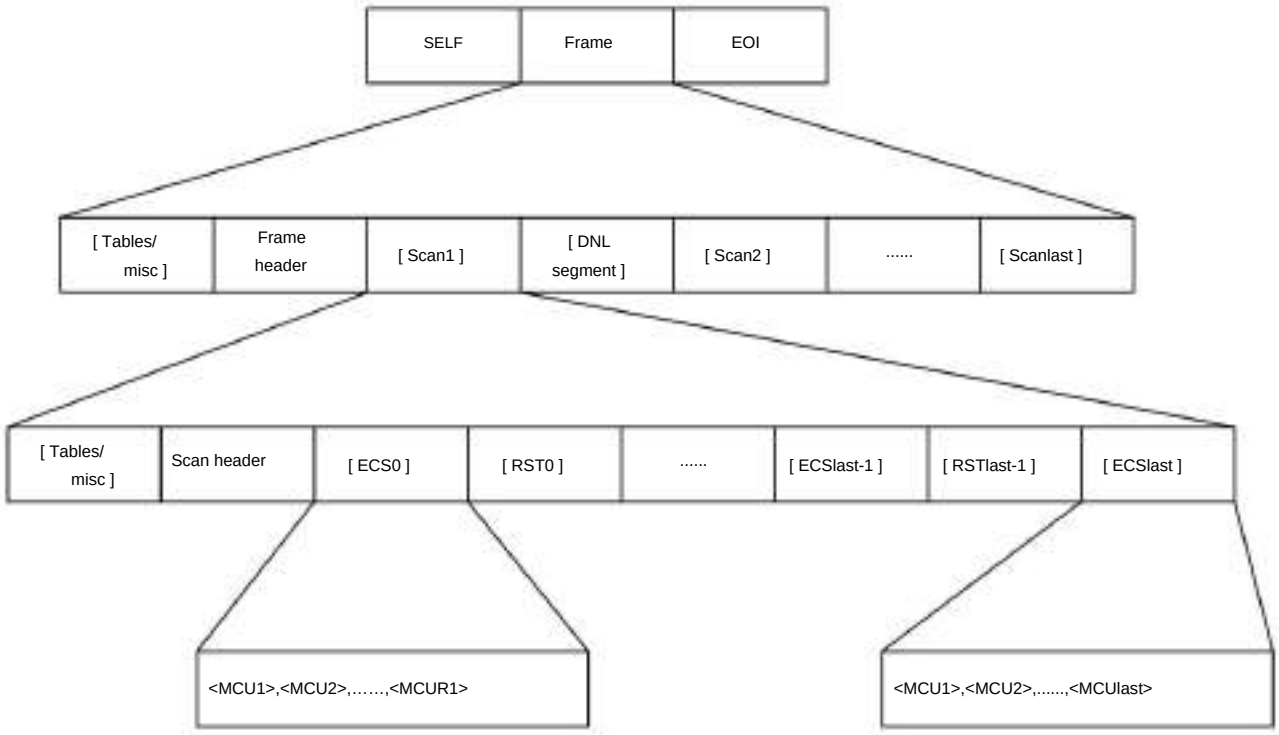


Figure 7-3 is a generalized structure diagram. For the JPEG code stream, the software parses the Scan header and above parts, and the hardware parses the ECS layer and RSTn flag.

7.2.3.2 Interaction between hardware and software

JPEG decoding is completed by both hardware and software, so there is interaction between hardware and software in decoding.

The interaction between software and hardware is carried out at the frame level except for the

continuous code stream: ÿ For JPEG images, each image frame is interacted once.

ÿ For Motion-JPEG, the image is interacted once per frame. The hardware and software

can interact in two ways: query and interrupt. The interrupt generation methods are as follows: ÿThe interrupt generated by the completion of the current

image decoding indicates that the current image has been completely decoded and written into the external memory, and the JPEG decoding work is over (because The Baseline image has only one scan layer, so the completion of decoding of one scan layer also means the end of decoding of one image).

ÿThe interrupt generated by the completion of the consumption of a segment of the currently configured code stream indicates that an error has occurred during the decoding of the current image, JPGD cannot continue decoding, and the

work is over. ÿThe consumption of the currently configured bit stream is completed, wait for the software to configure the next bit stream, and then start the decoder to continue decoding.

7.2.3.3 Continued stream

Due to memory limitations, it is impossible to read all code streams into memory at one time when decoding images. Therefore, the continuation stream mechanism is adopted to read a piece of code stream at a time. When the code stream is exhausted, the continuous code stream operation is started, and then the next code stream is read into the memory.

In order to simplify the software and hardware interaction in the continuation stream process, the steps to define the continuation stream are as follows:

Step 1 JPGD only receives a segment of continuous code stream for decoding each time. That is, before starting decoding each time, the firmware only needs to configure JPGD with a code stream physical storage start address and a code stream physical storage end address (both in bytes), and then JPGD can be started to start decoding.

Step 2 When JPGD consumes the current code stream, stop decoding and report that the continuous code stream is interrupted.

Step 3 After the software receives the interruption of the continuous code stream, it only needs to configure the start and end addresses of the next code stream to restart JPGD. The way to start is to write 1 to the JPGD_RESUME_START register. It should be noted that the code stream cannot be less than 64 bytes each time decoding is started.

Step 4 JPGD obtains a new code stream for decoding until the decoding of the current image is completed.

----Finish

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8 Video and Graphics Processing

8.1 TDE

8.1.1 Overview

The 2D graphics acceleration engine TDE (Two Dimensional Engine) utilizes hardware for graphics rendering, which can greatly reduce CPU usage and improve resource utilization of memory bandwidth. TDE reads and writes bitmap data, filter scaling coefficients, linked list node parameter information, and some linked list information through the AXI Master bus interface; obtains CPU register configuration information through the APB Slave bus interface.

The graphics data interface includes two channels, source 1 and source 2, and its functions are as follows:

Source 1 completes the functions of direct copy and direct filling during single-source operation.

Source 2 can complete various complex operations, such as image scaling, anti-flicker, etc., when operating as a single source.

When source 1 and source 2 work together, they can perform operations such as color mixing, and are used to support the processing of images in macroblock format.

8.1.2 Functional description

The TDE module has the following features:

Source bitmap 1 supports ARGB4444, ARGB1555, ARGB8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB,

YCbCr444MB format. Source bitmap 2 supports ARGB4444, ARGB1555, ARGB8888,

YCbCr422ÿYCbCr400MBÿYCbCr422MBHÿYCbCr422MBVÿYCbCr420MBÿ

YCbCr444MB format. The output

bitmap supports ARGB4444, ARGB1555, ARGB8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB,

YCbCr444MB format. Only little-endian

systems are supported.

Support source bitmap 1, source bitmap 2 and output bitmap formats can be configured

separately. Support Gamma correction, brightness and contrast

adjustment. Support conversion between RGB

and YCbCr. Direct copy is supported.

Direct filling is supported.

Support 2D-resize operation.

Supports anti-flicker operation.

Support clip operation.

Support alpha blending operation. Support

colorkey operation. Support clip mask

function. Provides a status interrupt.

8.2 VPSS

8.2.1 Overview

The video processing subsystem VPSS (Video Processing Sub System) realizes the video processing function. Contains Gaussian noise 3D adaptive noise reduction, image detail enhancement before encoding, de-interlacing, scaling, sharpening, contrast, image bordering and block processing functions.

VPSS features are as follows:

Supports single-frame processing of 960H video

sources Supports the same-source preview function of

the encoding channel Supports simultaneous output of encoding channel size

code stream and preview Supports independent configuration of image frame size and color, but the 4 frames of the image must be the same color Supports

1080P block processing Function supports register

linked list configuration function

Support across 4K boundaries

The input and output data format is 420/422, but it does not support the conversion from input 420 to output 422. It supports outstanding

configuration. It supports clock gate low

power consumption mode of MEM.

8.2.2 Features

Gaussian noise removal function: NR module (noise reduction), which can remove Gaussian noise in the image through parameter configuration, making the image smoother and reducing the encoding bit rate.

Image enhancement function: IE module (image enhancement), which can identify the detailed areas in the image, highlight the image details, make the image clear, and increase the contrast of the image. De-interlacing function: DEI module (de-

interlace), which can restore interlaced interlaced video source to progressive video source. Image sharpening function: HSP module extracts the high-

frequency components of the image after zooming, and performs frequency compensation on the image after the low-frequency filter (scaler), so that the edge of the image is sharp and the outline is clear.

Image frame adding function: add a frame to the edge of the image, the width of the image frame (top, bottom, left, and right) can be set independently, and the color of the frame can be set separately.

Image block processing function: When the single frame width of the input image is greater than 960, the image block processing function can be used; in the block processing mode, the maximum width of the processed image is 1920.

Scaling function: Low-frequency filtering processing with different input and output resolutions. The zoom factor is 8 times reduction and 16 times enlargement.

8.3 VCMP

8.3.1 Overview

VCMP uses graphics bandwidth compression algorithm to compress image data, and the compressed code stream is read by VDP and decompressed for display, so as to save the occupation of system bandwidth. VCMP reads the bitmap data through the AXI Master bus interface and writes out the compressed code stream; obtains the register configuration information of the CPU through the APB bus interface.

The graphics data interface includes a read path and four write paths, and its functions are as follows:

The read path reads the image data to be compressed from the memory.

The write channel writes the compressed code stream into the memory, which is divided into four channels: A, R, G, and B.

8.3.2 Features

The VCMP module has the following features:

The image data to be compressed supports two formats, ARGB1555 and ARGB8888.

The compressed code stream is stored by component, and the compressed data of the four components A, R, G, and B are stored in different addresses.

Support variable length code compression

algorithm. Support output compressed data, in byte. Support moving

pictures directly as a self-test mode. Provides a job completion interrupt.

8.3.3 Register Configuration Restrictions

The configuration of the related working registers of the VCMP module has the following restrictions:

All VCMP work-related registers can only be configured after VCMP reports an interrupt. When VCMP is working, VCMP registers cannot be configured.

The start address (SRC_ADDR) and stride (SRC_STRIDE) of

the picture to be compressed support 128bit alignment.

A, R, G, B component compressed data write-back address (VCMP_A_ADDR, VCMP_R_ADDR,
VCMP_G_ADDR, VCMP_B_ADDR) and stride support 128bit alignment. The compressed data write-back width needs

to be configured as (integer multiple of 256 - 1), such as 255, 511, 767, 1023, etc., and must be less than or equal to the stride of the compressed data write-back.

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9 motion detection unit

9.1 Overview

MDU (Motion Detect Unit) is a high-performance motion detection and video occlusion detection hardware acceleration IP, which can efficiently model the video background and calculate the information of the motion area. The MDU reads the image information through the AXI Master bus interface, and writes out the refreshed background image information, SAD (Sum of absolute differences) value and motion area information. Get configuration register information through APB Slave bus.

9.2 Functional description

The MDU supports the following functions:

- Supports SAD value calculation and output in 8x8 or 16x16 units. Support motion area detection and motion area information output. Support background image update.

9.3 Working method

9.3.1 Software and hardware division of MDU motion detection service

The software realizes the preparation of the image to be encoded, including:

- Allocate storage space in DDR. Call other hardware to complete video capture, scaling and other processing. Scheduling of multiple motion detections, designation of areas to be detected, division and generation of address information, etc.

The hardware implementation calculates the SAD value of the input image:

- According to the calculation result of SAD and the set threshold, the motion area is detected, and the background is updated.
- Output the information of the moving area, background image or SAD value according to the setting of the software.

9.3.2 Software and hardware division of MDU video occlusion detection service

The software uses the area information of the motion area output by the hardware to determine whether the occlusion threshold is reached. If it is reached, the hardware will not update the background, but continue to detect the motion area. When the area of the motion area continuously exceeds the set occlusion threshold, the occlusion will be performed Call the police.

9.4 Register overview

An overview of the MDU registers is shown in Table 9-1 .

Table 9-1 MDU register overview (base address is 0x206C_0000)

offset address name	describe	page number
0x0000 MDU_INTSTAT interrupt status signal register		9-3
0x0004 MDU_INTEN	Interrupt Enable Signal Register	9-4
0x0008 MDU_RAWINT Raw interrupt signal register		9-5
0x000C MDU_INTCLR interrupt clear register		9-6
0x0020 MDU_VEDIMGSIZE image size configuration register		9-6
0x0024 MDU_MODE	Mode Configuration Register	9-7
0x0028 MDU_START	MDU start register	9-8
0x002C MDU_AXI_OUTSTD_NUM	AXI OUTSTANDING CONFIGURATION REGISTER	9-9
0x0040 MDU_REF_YADDR Reference image brightness storage address register		9-9
0x0044 MDU_REF_YSTRIDE	Reference Image Brightness Stride Register	9-9
0x0048 MDU_CUR_YADDR current image brightness storage address register		9-10
0x004C MDU_CUR_YSTRIDE	Current image brightness Stride register	9-10
0x0060 MDU_MBSAD_ADDR	Macroblock SAD value storage address register	9-11
0x0064 MDU_MBSAD_STRIDE	Macroblock SAD value storage Stride register	9-11
0x0070 MDU_BACKGROUND_ADDR	Background image brightness storage address register	9-12
0x0074 MDU_BACKGROUND_STRIDE	Background Image Brightness Stride Register	9-12
0x0078 MDU_OBJ_ADDR Motion area storage address register		9-12

9.5 Register Description

MDU_INTSTAT

MDU_INTSTAT is the interrupt status signal register.

Offset Address	Register Name	Total Reset Value
0x0000	MDU_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	---		reserved																												---	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RO	mdu_bus_err	Bus read and write errors.
[30]	RO	mdu_cfg_err	register configuration error.
[29:2]	RO	reserved	reserve.
[1]	RO	mdu_timeout	MDU timeout work interrupt, when the MDU is configured to open the timeout detection mode, and the MDU working time has exceeded the threshold configured by the software in the register MDU_TIMEOUT , this interrupt is valid.
[0]	RO	mdu_endofpic	MDU current picture end indication, active high.

MDU_INTEN

MDU_INTEN is the interrupt enable signal register.

Offset Address	Register Name	Total Reset Value
0x0004	MDU_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	---		reserved																												---	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

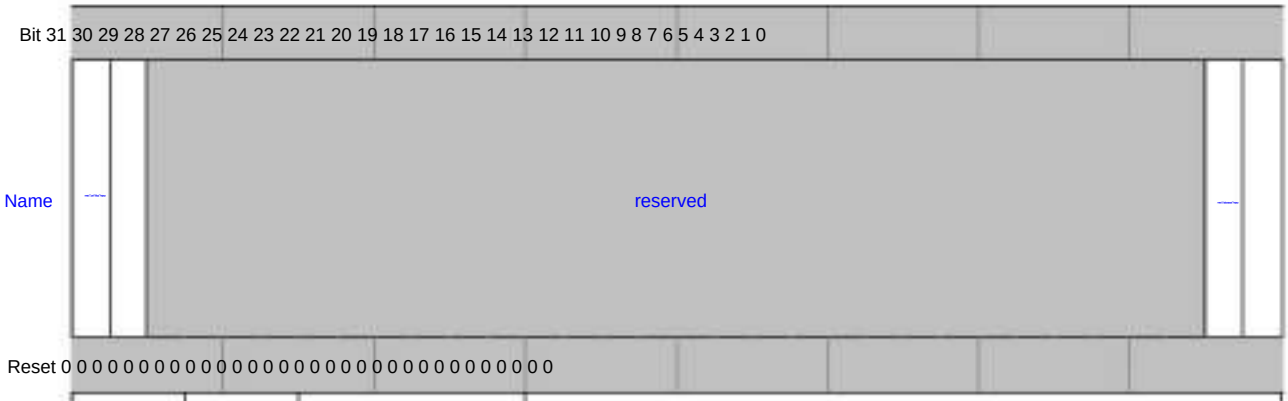
Bits	Access Name		Description
[31]	RW	mdu_bus_err_en	Interrupt enable on bus read or write errors. 0: forbidden; 1: enable.

[30] RW	mdu_cfg_err_en		Register configuration error interrupt enable. 0: forbidden; 1: enable.
[29:2] RO		reserved	reserve.
[1] RW	mdu_timeout_en		Mdu timeout work interrupt, when mdu is configured to open the timeout detection mode, and the mdu working time has exceeded the threshold configured by the software in the register MDU_TIMEOUT , this interrupt is valid. 0: forbidden; 1: enable.
[0] RW	mdu_endofpic		MDU current image end interrupt enable. 0: forbidden; 1: enable.

MDU_RAWINT

MDU_RAWINT is the raw interrupt signal register.

Offset Address	Register Name	Total Reset Value
0x0008	MDU_RAWINT	0x0000_0000

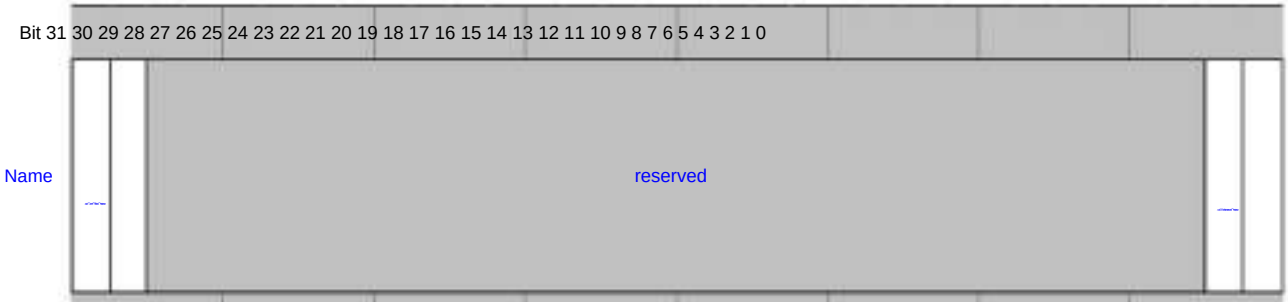


Bits	Access	Name	Description
[31]	RO	mdu_bus_err_raw	Bus read and write error indication, active high.
[30]	RO	mdu_cfg_err_raw	register configuration error indication, active high.
[29:2]	RO	reserved	reserve.
[1]	RO	mdu_timeout_raw	MDU timeout interrupt, active high.
[0]	RO	mdu_endofpic_raw	MDU current picture end indication, active high.

MDU_INTCLR

MDU_INTCLR is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x000C	MDU_INTCLR	0x0000_0000

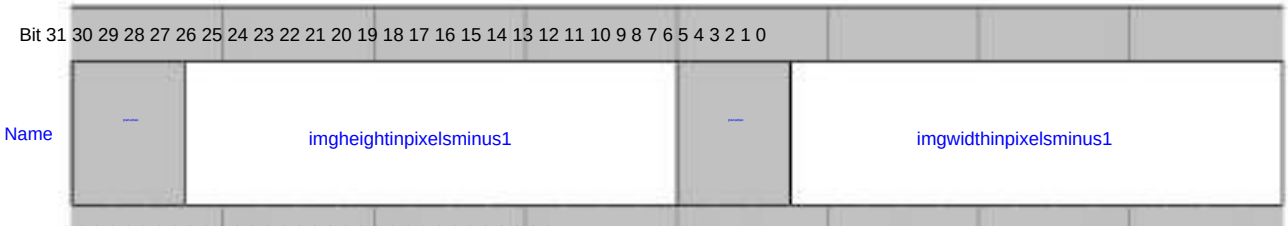


Bits	Access	Name	Description
[31]	RW	mdu_bus_err_clr	Bus read and write error clear, active high.
[30]	RW	mdu_cfg_err_clr	register configuration error clear, active high.
[29:2]	RO	reserved	reserve.
[1]	RW	mdu_timeout_clr	MDU timeout work interrupt, when the MDU is configured to open the timeout detection mode, and the MDU working time has exceeded the threshold configured by the software in the register MDU_TIMEOUT , this interrupt is valid.
[0]	RW	mdu_endofpic_clr	MDU current picture end indication clear, active high.

MDU_VEDIMGSIZE

MDU_VEDIMGSIZE configures the register for the image size.

Offset Address	Register Name	Total Reset Value
0x0020	MDU_VEDIMGSIZE	0x0000_0000



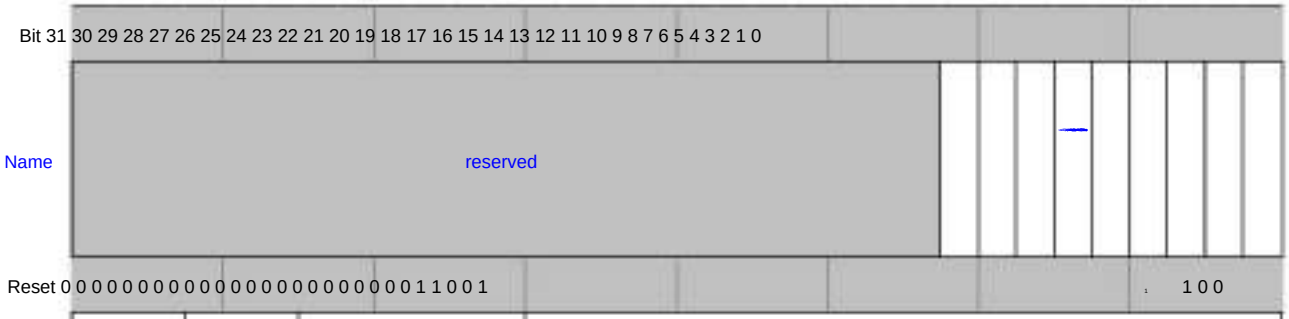
Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	imgheightinpixelsminus1	Image height. In pixels, the actual width is minus 1. For example, if the image width is 352, this register should be configured as 351.

[15:13] RO		reserved	reserve.
[12:0] RW		height are imgwidthinpixelsminus1	Image width. In pixels, the actual height is minus 1. For example, if the image width and 288, this register should be configured as 287.

MDU_MODE

MDU_MODE is the mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	MDU_MODE	0x0000_019C



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	mcpi_clkgate_en	Clock gate switch.
[7]	RW	mcpi_wrlock_en	Register configuration lock switch, when it is turned on, the configuration registers are invalid after starting the MDU and before the end of the detection, preventing the registers from being rewritten during use.
[6]	RW	timeout_en	The mdu timeout detection switch can automatically detect the upper limit of the number of working cycles configured by the software in the register MDU_TIMEOUT when it is turned on. 0: Turn off the timeout detection function; 1: Turn on the timeout detection function.
[5]	RW	md_mod	Motion detection mode. 0: Based on the background algorithm; 1: Based on the frame difference algorithm.
[4]	RW	bg_update_en	Background update switch. 0: do not update the background; 1: Update the background. This register is valid when md_mod is set to be based on the background algorithm, and if it is based on the frame difference algorithm, any value of this register will be invalid.

[3] RW eg_find_en			Motion zone connection detection switch. 0: Do not use motion area Unicom detection; 1: Use motion area connectivity detection. When based on the background algorithm, this switch only turns off the last background-based regional connectivity detection.
[2] RW obj_out_en			Motion area output switch, if this switch is turned on, the address and interval register of the motion area information storage memory must be set. 0: No output of motion area information; 1: Output of motion area information.
[1] RW sad_out_en			SAD output switch, if this switch is on, the SAD storage memory address and interval register must be set. 0: The generated SAD is not output; 1: Generated SAD output.
[0] RW sad_mad_sel			SAD outputs bit number selection signal. 0ÿ8bitÿ 1ÿ16bitÿ

MDU_START

MDU_START is the MDU start register.

Offset Address	Register Name	Total Reset Value
0x0028	MDU_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WO	mdu_start	The MDU job trigger starts. 0: not working; 1: Trigger job.

MDU_AXI_OUTSTD_NUM

MDU_AXI_OUTSTD_NUM is the AXI OUTSTANDING configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	MDU_AXI_OUTSTD_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	----
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	axi_outstd_num	AXI outstanding configuration register, counts from 0 (actual value is incremented by 1).

MDU_REF_YADDR

MDU_REF_YADDR is the reference image brightness storage address register.

Offset Address	Register Name	Total Reset Value
0x0040	MDU_REF_YADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mdu_ref_yaddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mdu_ref_yaddr	Reference image Y component storage address. The input original image must be Qword (128bit) aligned, that is, the lower 4 bits of the address are 0. The hardware will automatically set the lower 4 bits of the address to 0.

MDU_REF_YSTRIDE

MDU_REF_YSTRIDE is the reference image brightness Stride register.

Offset Address	Register Name	Total Reset Value
0x0044	MDU_REF_YSTRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	mdu_ref_ystride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	mdu_ref_ystride	Brightness Stride, in byte. In order to ensure that the address remains 128-bit aligned after the image wraps, the lower 4 bits of Ystride should also be set to 0. The hardware will automatically set the lower 4 bits of Ystride to 0. STRIDE needs to be configured as an integer multiple of 64byte.

MDU_CUR_YADDR

MDU_CUR_YADDR is the storage address register for the current image brightness.

Offset Address	Register Name	Total Reset Value
0x0048	MDU_CUR_YADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mdu_cur_yaddr	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mdu_cur_yaddr	The storage address of the Y component of the original image. The input original image must be Qword (128bit) aligned, that is, the lower 4 bits of the address are 0. The hardware will automatically set the lower 4 bits of the address to 0.

MDU_CUR_YSTRIDE

MDU_CUR_YSTRIDE is the current image brightness Stride register.

Offset Address	Register Name	Total Reset Value
0x004C	MDU_CUR_YSTRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	mdu_cur_ystride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	mdu_cur_ystride	Brightness Stride, in byte. In order to ensure that the address remains 128-bit aligned after the image wraps, the lower 4 bits of Ystride should also be set to 0. The hardware will automatically set the lower 4 bits of Ystride to 0. STRIDE needs to be configured as an integer multiple of 64byte.

MDU_MBSAD_ADDR

MDU_MBSAD_ADDR is the macroblock SAD value storage address register.

Offset Address	Register Name	Total Reset Value
0x0060	MDU_MBSAD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mdu_mbsad_addr	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mdu_mbsad_addr	Macroblock SAD storage address. The address must be qword aligned, so its lower 4 bits are 0.

MDU_MBSAD_STRIDE

MDU_MBSAD_STRIDE Stores the Stride register for the macroblock SAD value.

Offset Address	Register Name	Total Reset Value
0x0064	MDU_MBSAD_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	mdu_mbsad_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

RW	mdu_mbsad_stride	so the lower 4 bits are always 0.	Macroblock sad row spacing. The stride unit is byte. Stride is 128bit aligned, [15:0]

MDU_BACKGROUND_ADDR

MDU_BACKGROUND_ADDR is the background image brightness storage address register.

Offset Address	Register Name	Total Reset Value
0x0070	MDU_BACKGROUND_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	bg_yaddr	URL of the background image. The address must be qword aligned, so its lower 4 bits are 0ÿ

MDU_BACKGROUND_STRIDE

MDU_BACKGROUND_STRIDE is the brightness Stride register of the background image.

Offset Address	Register Name	Total Reset Value
0x0074	MDU_BACKGROUND_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bg_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	bg_ystride	Background image line spacing. The stride unit is byte. Stride is 128bit aligned, so the lower 4 bits are always 0.

MDU_OBJ_ADDR

MDU_OBJ_ADDR stores the address register for the motion area.

Offset Address	Register Name	Total Reset Value
0x0078	MDU_OBJ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obj_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	obj_addr	Motion area storage address. The address must be qword aligned, so its lower 4 bits are 0. The storage format is that a motion area uses 4 16bits to store 4 points in the order of left, top, right, and bottom; therefore, a motion area uses 3 32bit memories, and the software should use 2 x 32bit x maximum motion when allocating memory The number of regions is used as the minimum value of memory.

MDU_BG_UP_WEIGHT

MDU_BG_UP_WEIGHT Update weight register for background image.

Offset Address	Register Name	Total Reset Value
0x007C	MDU_BG_UP_WEIGHT	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								src_weight							weight_sum_exp_2			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	src_weight	New image weights.
[7:0]	RW	weight_sum_exp_2	Exponent of the sum of weights to 2. When the MDU superimposes the source image and the background to generate a new background, it uses the following calculation formula: (background pixel value X ((1<<weight_sum_exp_2)-src_weight) + source image X bg_weight) >> weight_sum_exp_2). The weight bg_weight of the background image is: ((1<<weight_sum_exp_2)-src_weight), if the background weight is set larger than src_weight, the background update speed will be slower. Default: 0x1, the maximum value is 8.

MDU_MBSAD_TH

MDU_MBSAD_TH is the macro block dynamic and static judgment threshold register.

Offset Address	Register Name	Total Reset Value
0x0080	MDU_MBSAD_TH	0x0000_001E

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	mdu_mbsad_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	mdu_mbsad_th	4% 4 block dynamic and static judgment threshold. All calculations inside the MDU use 4%4 blocks

MDU_TIMEOUT

MDU_TIMEOUT is the TIMEOUT upper limit register.

Offset Address	Register Name	Total Reset Value
0x0084	MDU_TIMEOUT	0x0360_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mdu_timeout	
Reset	0 0 0 0 0 0 1 1 0 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mdu_timeout	The upper limit of the working cycle number.

MDU_WND_SIZE

MDU_WND_SIZE is the SAD value output window configuration register.

Offset Address	Register Name	Total Reset Value
0x0090	MDU_WND_SIZE	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access Name	Description
[31:1] RO	reserved	reserve.
[0] RW	sad_wnd_size	sad output window size. The calculation is performed in units of 4 x 4 blocks inside the MDU. After enabling the sad_out_en in the mode register, the MDU will add up multiple 4 x 4 blocks according to this register when outputting, and then output to the DDR. 0ÿ8 x 8ÿ 1:16 x 16. (Defaults)

MDU_MIN_OBJ_SIZE

MDU_MIN_OBJ_SIZE is the minimum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0094	MDU_MIN_OBJ_SIZE	0x0300_0101

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	egsearch_timeout	min_obj_size_h	min_obj_size_w
Reset	0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1		

Bits	Access Name	Description
[31:16] RW	egsearch_timeout	Edge search timeout, if the number of points searched in a motion area exceeds this value, the edge search of this motion area will be stopped and the next area search will be performed.
[15:8] RW	min_obj_size_h	The lower limit of the height of the movement size, and the movement area lower than this height will not be reported. A size of 1 here represents a 4 x 4 block.
[7:0] RW	min_obj_size_w	The lower limit of the width of the motion size, the motion area smaller than this width will not be reported. A size of 1 here represents a 4 x 4 block.

MDU_MAX_OBJ_CNT

MDU_MAX_OBJ_CNT is the maximum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0098	MDU_MAX_OBJ_CNT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								max_obj_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	max_obj_cnt	Upper limit value for detecting moving objects.

MDU_OBJ_CNT

MDU_OBJ_CNT is the readback register for motion area information.

Offset Address	Register Name	Total Reset Value
0x009C	MDU_OBJ_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index																obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index	Maximum motion region index. The statistics register without a number suffix is the statistical information obtained by using the frame difference method, or using the background method to calculate the SAD and search for the motion area for the first time.
[15:0]	RO	obj_cnt	The number of detected moving objects.

MDU_MAX_OBJ_SIZE

MDU_MAX_OBJ_SIZE is the maximum motion area readback register.

Offset Address	Register Name	Total Reset Value
0x00A0	MDU_MAX_OBJ_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	max_obj_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	max_obj_size	The maximum motion area is used to detect video occlusion. The value output here is the pixel area. The software uses this value to calculate the percentage of the motion area and compares it with the threshold value. If it is greater than the motion area threshold, the frame is considered to be occluded, and the following frame for video occlusion detection stops updating the image background and detects whether the area of the motion area is continuous Exceeding the threshold, when the occlusion time exceeds the threshold, it is considered that video occlusion occurs and an alarm is required.

MDU_TOTAL_OBJ_SIZE

MDU_TOTAL_OBJ_SIZE readback register for total motion area information.

Offset Address	Register Name	Total Reset Value
0x00A4	MDU_TOTAL_OBJ_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	total_obj_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	total_obj_size	The sum of the areas of all motion regions. It is used to detect the occlusion of the camera spray, and the method of use is the same as the area statistics of the maximum motion area. The calculation method inside the MDU is to add up the areas of all sports areas. The value output here is the pixel area (multiplied by 16 by the number of 4 x 4 blocks of a motion area). Notice: In some cases, motion areas may overlap, and this area may exceed the original image area. The 4 x 4 block width and height of each motion zone is calculated as: weight=ÿright-leftÿ+1ÿ heigth= ÿbottom-topÿ+1ÿ

MDU_MOVE_PIX_CNT

MDU_MOVE_PIX_CNT is the motion pixel statistics register of the whole frame.

Offset Address	Register Name	Total Reset Value
0x00A8	MDU_MOVE_PIX_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	move_pix_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	move_pix_cnt	The number of moving pixels in the entire frame can be used for video occlusion detection, and the usage is the same as the area statistics of the moving area. Note: Because this is a statistic based on a single pixel, this area may not be equal to **the total_obj_size** above.

MDU_OBJ_CNT1

MDU_OBJ_CNT1 is the readback register for context-based motion zone information.

Offset Address	Register Name	Total Reset Value
0x00AC	MDU_OBJ_CNT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	max_obj_index1 | obj_cnt1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	max_obj_index1	Background-based index of maximum motion region. All the subsequent statistical registers with a suffix of 1 refer to the statistical information obtained from the second SAD calculation and motion region search when the background method is used.
[15:0]	RO	obj_cnt1	The number of detected moving targets based on the background.

MDU_MAX_OBJ_SIZE1

MDU_MAX_OBJ_SIZE1 is the background-based maximum motion area readback register.

Offset Address	Register Name	Total Reset Value
0x00B0	MDU_MAX_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	max_obj_size1	Based on the maximum motion area of the background, it is used to detect video occlusion. The software uses this value to calculate the percentage of the motion area and compares it with the threshold value. If it is greater than the motion area threshold, the frame is considered to be blocked, and the subsequent video detection frames stop updating the image background and detect whether there is a continuous motion area area. Exceeding the threshold, when the occlusion time exceeds the threshold, it is considered that video occlusion occurs and an alarm is required. in pixels.

MDU_TOTAL_OBJ_SIZE1

MDU_TOTAL_OBJ_SIZE1 readback register for background based total motion area information.

Offset Address	Register Name	Total Reset Value
0x00B4	MDU_TOTAL_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	total_obj_size1	The sum of the areas of all motion regions based on the background. It is used to detect the occlusion of the camera spray, and the method of use is the same as the area statistics of the maximum motion area.

MDU_MOVE_PIX_CNT1

MDU_MOVE_PIX_CNT1 is the background-based motion pixel statistics register of the whole frame.

Offset Address	Register Name	Total Reset Value
0x00B8	MDU_MOVE_PIX_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	move_pix_cnt1	Based on the number of moving pixels in the entire frame of the background, it can be used for video occlusion detection, and the usage is the same as the area statistics of the moving area.

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10 Intelligent Acceleration Engine

10.1 Overview

IVE (IntelligentVideoEngineering) module is a hardware acceleration module in the intelligent analysis system. Realize template filtering, expansion, erosion, image sobel and canny edge extraction, image subtraction, AND, or, image binarization, integral map, histogram statistics. IVE reads and writes data and link list node parameter information through the AXI Master bus interface; configures the register information required for IVE startup and obtains the register status information during operation through the APB Slave bus interface.

10.2 Functional description

The IVE module supports the following features:

DMA is supported.

Supports 3 x 3 mask filtering.

Supports YUV to RGB color space conversion. Composite function of 3 x 3 template filtering plus YUV to RGB color space conversion is supported. Supports gradient calculation in the X/Y direction of operators such as SOBEL/SCHARR. Support CANNY gradient magnitude and direction calculation. Supports 3 x 3 corrosion.

Supports 3 x 3 expansion.

Support image binarization.

Supports the ANDing of two images.

Supports subtraction of two images.

Support phase-or of two images.

Support integral graph calculation. Supports histogram statistics. The maximum operating frequency is 300MHz.

Support for soft reset alone.

Support 64bitAXI bus (Master) and 32bitAPB bus (Slave).

Support linked list level interrupt and node level

interrupt. Query mode

is supported. Support single component, SP420 (semi-planar420), SP422 (semi-planar422) input format. Support single

component, SP420, SP422, RGBpackage, RGBplanar and other output formats. Some operators support

non-8byte alignment for read and write addresses.

10.3 Working method

10.3.1 Hardware usage

The steps to use IVE in query mode are as follows:

Step 1 Create a linked list of tasks in memory.

Step 2 Configure IVE internal registers LIST_POINTER and INT_EN.

Step 3 Configure IVE internal register IVE_START to start IVE.

Step 4 Check the status of IVE_STATUS during running to get the running status of IVE. If the IVE is free, the linked list task is complete. Repeat steps 1 to 4 if necessary .

----Finish

The operation steps of using IVE in interrupt mode are as follows:

Step 1 Create a linked list of tasks in memory.

Step 2 Configure IVE internal registers LIST_POINTER and INT_EN.

Step 3 Configure IVE internal register IVE_START to start IVE.

Step 4 In the interrupt service routine, judge the interrupt type according to INT_STATUS , and configure the IVE internal register INT_RW

The interrupt status of INT_STATUS can be cleared . And judge the IVE status according to IVE_STATUS , if the

IVE_STATUS status is IDLE, it indicates that the link list task is completed, go back to step 1 to start the next link list operation.

----Finish

The IVE task linked list adopts a fixed-length linked list node format, the size of each node is 8 x 8byte, and the number of nodes in the linked list can be any value.

The node structure of the linked list is shown in Figure 10-1 .

Figure 10-1 Schematic diagram of IVE linked list node structure

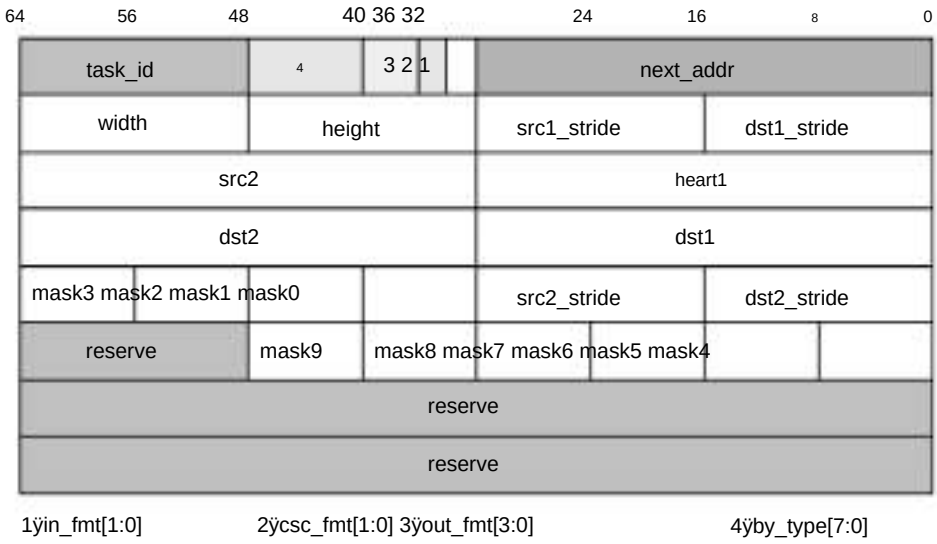


Table 10-1 describes the meaning of each parameter value of the node.

Table 10-1 IVE linked list node parameter description

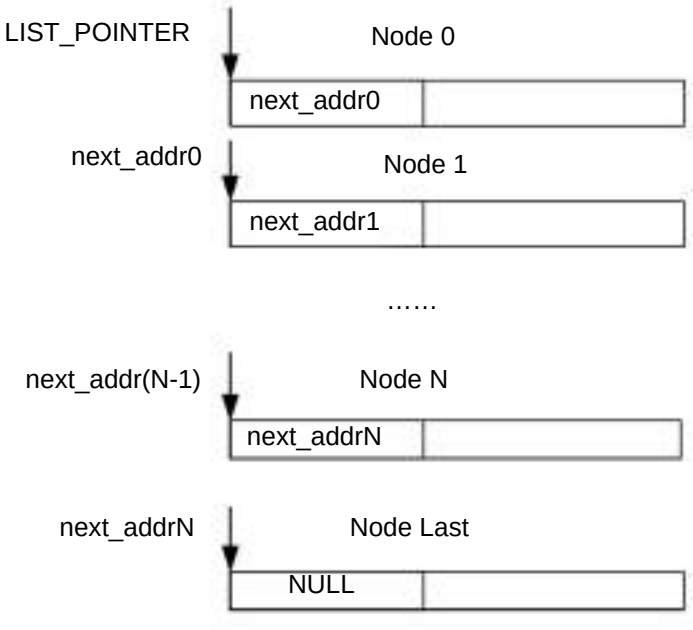
parameter register	describe
next_addr	The address of the next node in memory is 0x00000000, indicating the last node of the current linked list.
in_fmt	Image input format. 00: single component; 01ÿSP420ÿ 10: SP422; 11: reserved.
csc_fmt	CSC mode selection. 00: BT601&BT656, ranging from 16 to 235; 01: BT701, ranging from 16 to 235; 10: BT601&BT656, ranging from 0 to 255; 11: BT701, ranging from 0 to 255.

parameter register	describe
out_fmt	Image output format. CSCÿ 0000ÿpackageÿ 0001ÿplanarÿ CANNYÿ 0000: only output amplitude; 0001: Output amplitude and angle values. THRESHÿ 0000: If it is greater than the threshold, set it to maxvalue, if it is less than the threshold, set it to minvalue; 0001: If it is greater than the threshold, set it to maxvalue, if it is less than the threshold, it will not change; 0010: If it is greater than the threshold, it will not change, and if it is less than the threshold, it will be set as minvalue. SUBSTRACTÿ 0000: difference absolute value output; 0001: The difference value is shifted to the right by one bit and output.
on_type	The operator type that the current node chooses to run. 0x00: fast copy (DMA); 0x01: template filter (FILTER); 0x02: color space conversion (CSC); 0x03: template filter plus color conversion composite function (FILTER+CSC); 0x04: SOEBL gradient (SOBEL); 0x05: SOBEL amplitude and direction (CANNY); 0x06: expansion (DILATE); 0x07: erosion (ERODE); 0x08: image binarization (THRESH); 0x09: two-image AND (AND); 0x0A: two-image subtraction (SUBSTRACT); 0x0B: two-image OR (OR); 0x0C: integral graph (INTEGRAL); 0x0D: histogram (HISTOGRAM).
task_id	The task ID number of the current node.
dst1_stride	Output the stide signal of destination address 1, 8byte aligned.
src1_stride	Stride signal of source image 1, 8byte alignment.
height	The actual height value of the source image.
width	The actual width of the source image, when the input format is 420 and 422, it is an even number.

parameter register	describe
heart1	The starting address of source image 1, FILTER, CSC, FILTER+CSC, SOBELÿCANNYÿDILATEÿERODEÿINTEGRALÿ For operators such as HISTOGRAM, 8byte alignment.
src2	The starting address of source image 2.
dst1	Start address of target 1, FILTER, CSC, FILTER+CSC, SOBELÿCANNYÿDILATEÿERODEÿINTEGRALÿ For operators such as HISTOGRAM, 8byte alignment is required.
dst2	The start address of target 2.
dst2_stride	The stride of target address 2 requires 8byte alignment.
src2_stride	Stride of source image 2, 8byte alignment.
mask0	The template coefficient is 00 or the threshold of the THRESH operator.
mask1	Template coefficient 01 or min_value of THRESH operator.
mask2	Template coefficient 02 or max_value of THRESH operator.
mask3	Template factor 10.
mask4	Template factor 11.
mask5	Template factor 12.
mask6	Template factor 20.
mask7	Template factor 21.
mask8	Template factor 22.
mask9	The sum of FILTER operator coefficients.
reserved	reserved bit.

Template coefficient: the coefficient of the operation template used by the 3×3 operation operators (FILTER, FILTER+CSC, SOBEL, CANNY, DILATE, ERODE).

Figure 10-2 Schematic diagram of using IVE linked list



10.3.2 Interrupts

IVE will generate the following 2 kinds of interrupts:

- All nodes of the current linked list complete the interrupt.
- Operation complete interrupt for current node.

10.3.3 Clock reset

Clock Shutdown Policy

The input clock of IVE can be turned off to reduce power consumption. Before the IVE clock is turned off, it must be ensured that the IVE is in an idle state (query the status register IVE_STATUS as IDLE), and then the clock can be turned off. Clock shutdown does not lose the IVE's register configuration. Before operating the IVE internal registers, the clock must be turned on.

reset strategy

When IVE is reset alone, it does not support reset at any time, otherwise it may cause bus abnormality. When IVE is reset alone, it can only be reset when the IVE status register IVE_STATUS is IDLE.

System reset will clear all internal registers of IVE.

10.3.4 Input and output data format

10.3.4.1 Storage order

The following data storage order is in the memory storage order of the little endian system (little endian). For the convenience of description, Word and Double Word are used as the storage unit for description. Different operators in practical applications have special requirements for the data storage alignment format , see 10.3.4.2 Supported Function Description for specific requirements.

Figure 10-3 When the data format is SemPlanar YCbCr422, Pixel storage in Memory

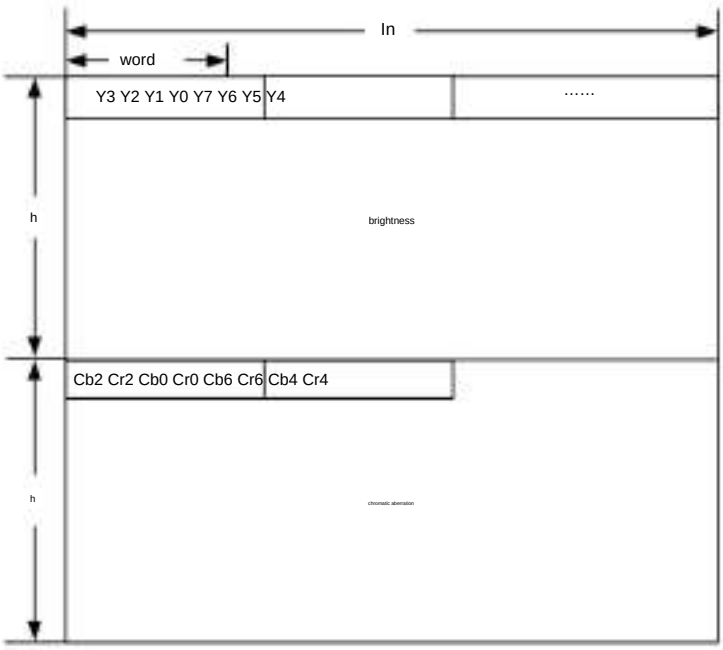


Figure 10-4 Pixel storage in Memory when the data format is SemPlanar YCbCr420

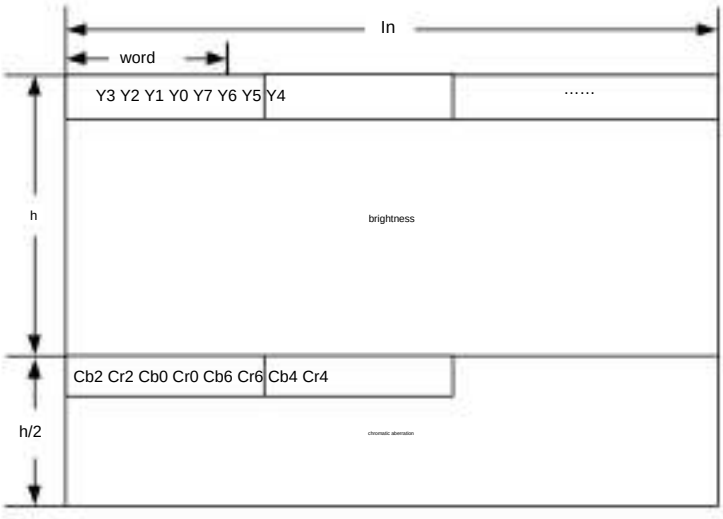


Figure 10-5 Pixel storage in Memory when the data format is single component

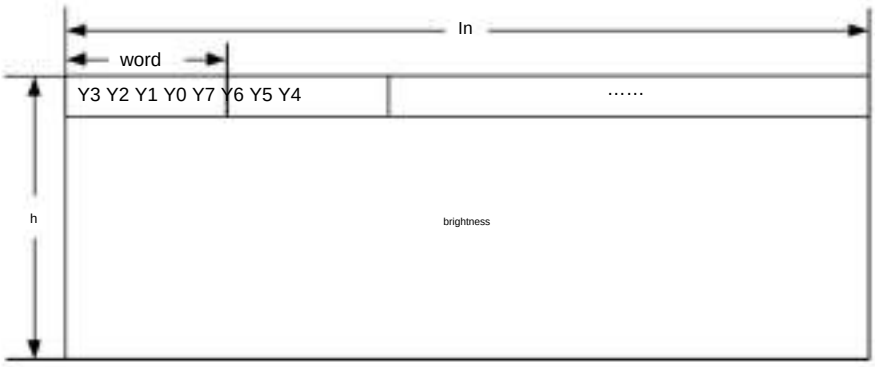


Figure 10-6 Pixel storage in Memory when the data format is RGB package

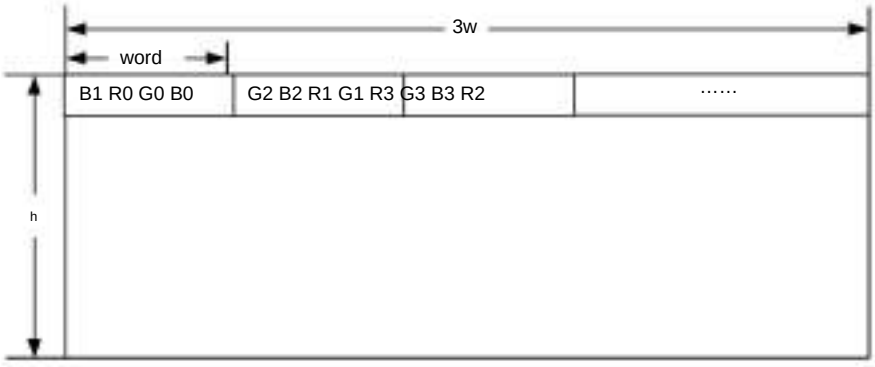


Figure 10-7 Pixel storage in Memory when the data format is RGB planar

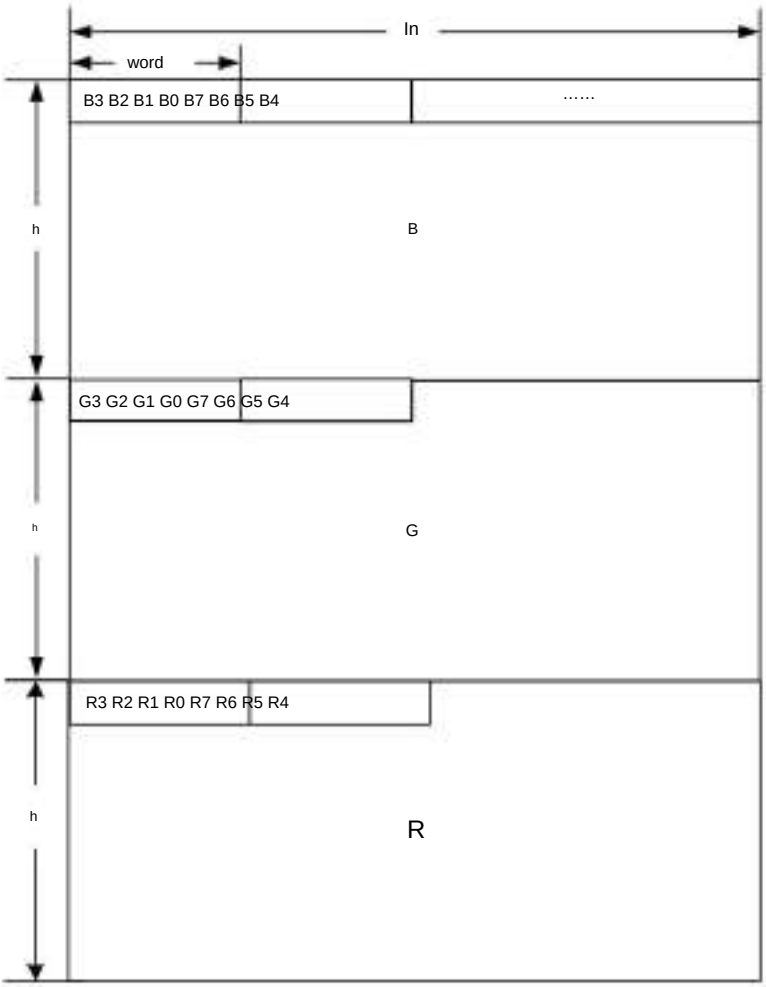


Figure 10-8 Storage of output results in Memory during SOBEL operator

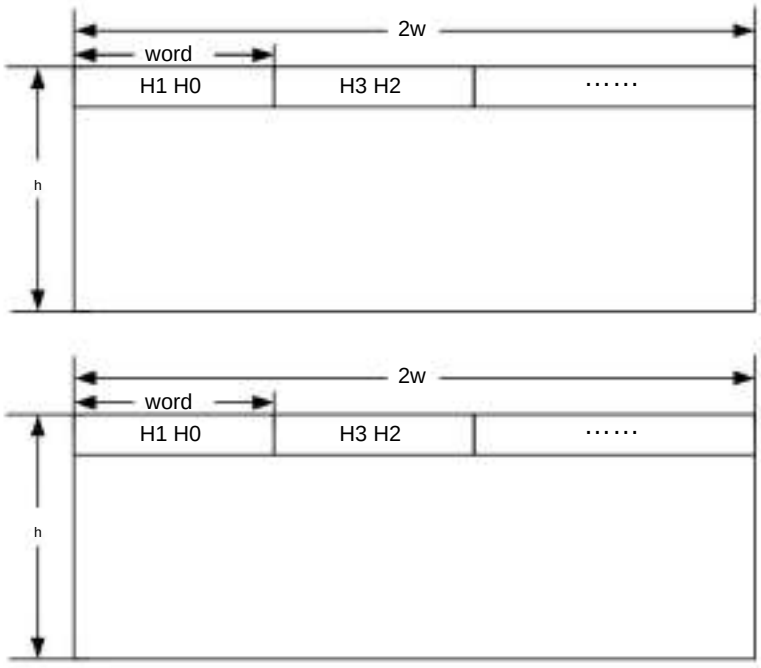


Figure 10-9 CANNY operator, storage of results in Memory

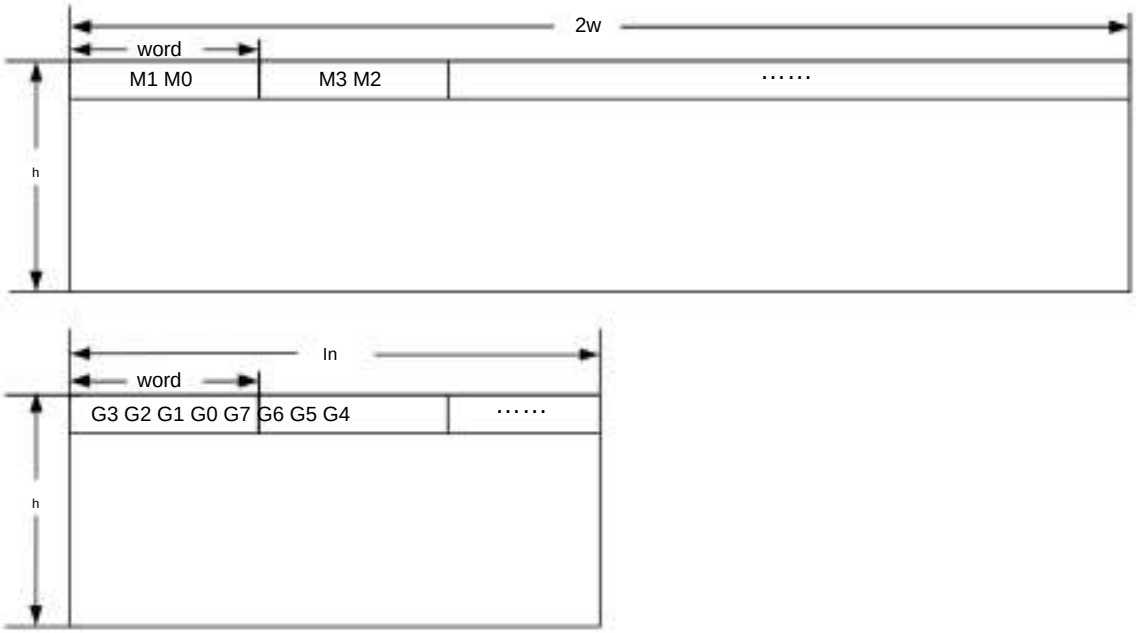


Figure 10-10 Storage of output results in Memory (INTEGRAL_OUT) when integrating graph operators

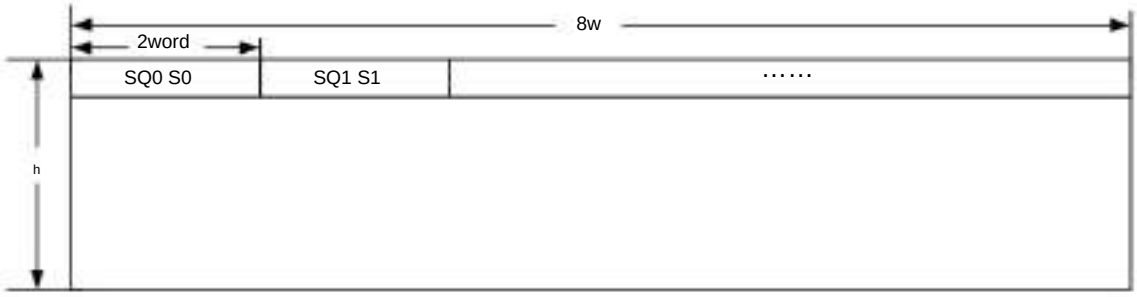
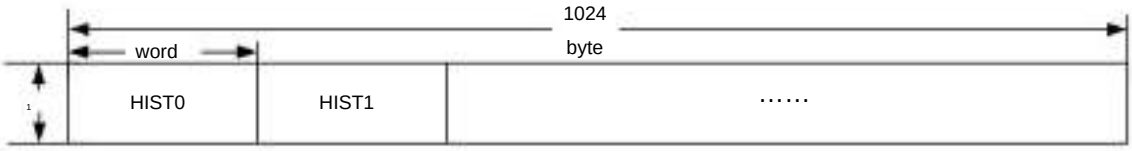


Figure 10-11 When the histogram is counted, the output result is stored in Memory (HIST_OUT)



10.3.4.2 Supported functions

The stride of all IVE operators must meet the following conditions:

When ((src%8) == 0) && *((width%8)* == 0) holds, require

ÿ *stride width* ÿ ÿ ÿ

stride%8 0 =

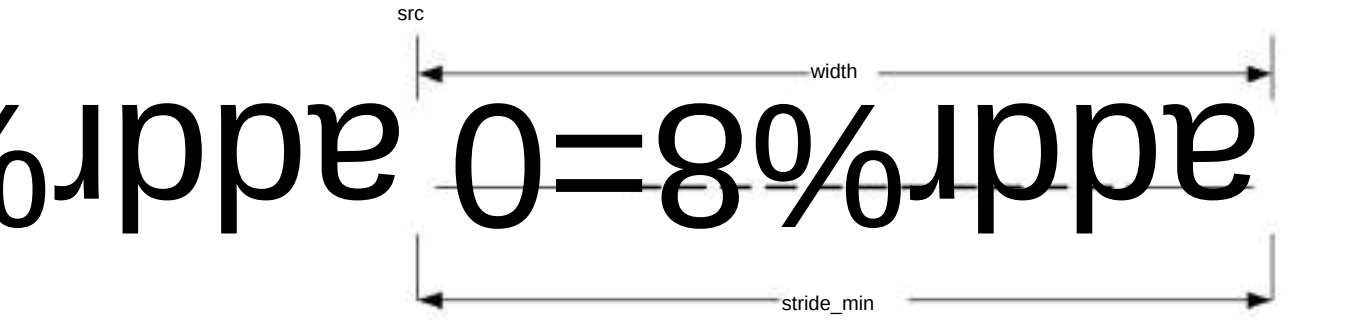
otherwise require

8 ((*width src* %8 %8 +))))(+) *src* %8 *width stride* ÿ +

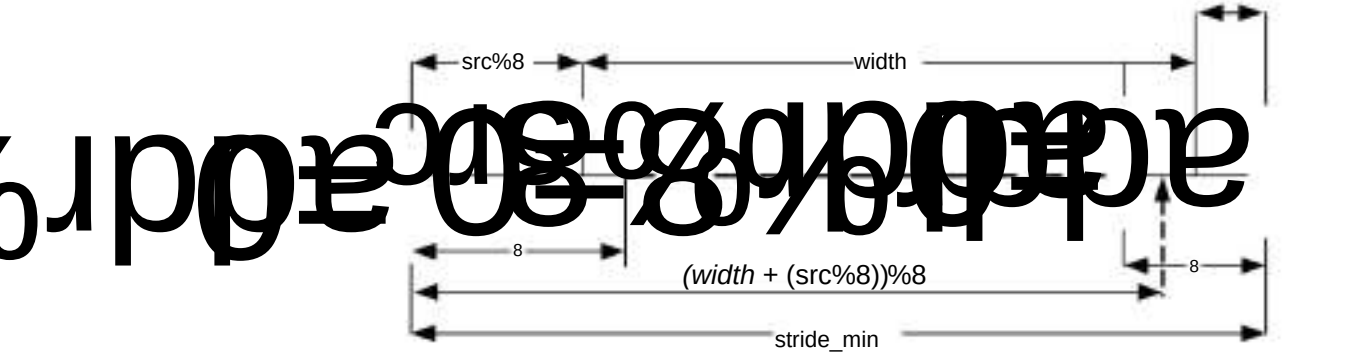
{ (ÿ ÿ ÿ *stride* %8 0 =

Among them, % represents the remainder operation. See Figure 10-12 for an example.

Figure 10-12 The situation when the parameter stride of the operator takes the minimum value



(8 ÿ *((width + src)*%8))%8



quick copy

Realize the fast moving function of the rectangular image area. In DMA mode, the source data will be directly moved to the target area through the internal fast path of the IVE, and directly overwrite the data in the target area.

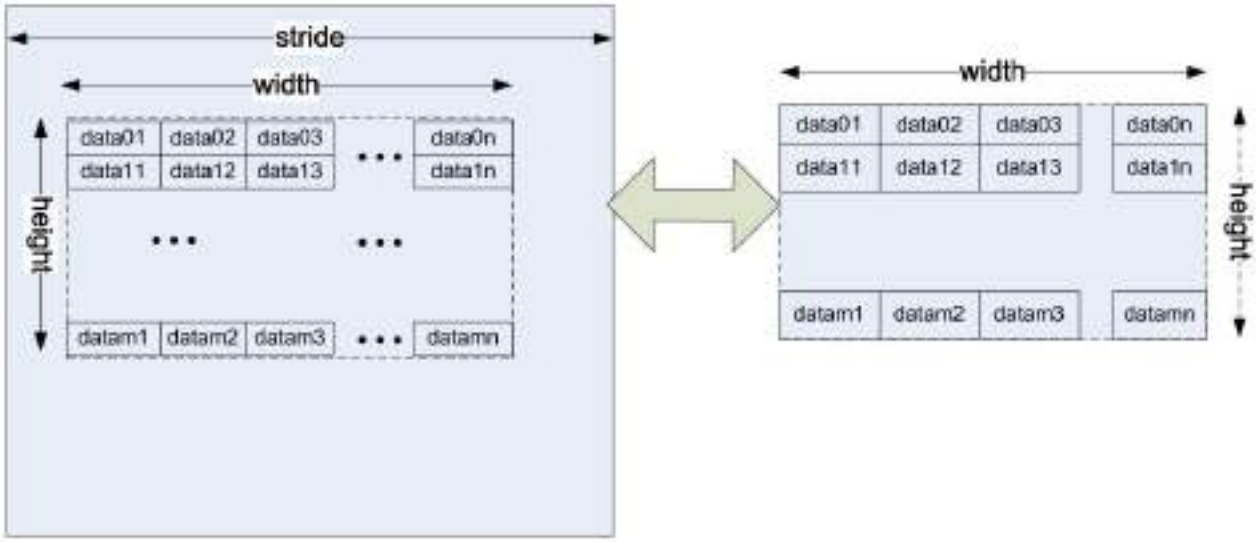
Image resolution: 32 x 1ÿ1920 x 1080

Address alignment: Both input and output addresses require byte alignment.

Input and output formats: single componentÿsingle component.

How to use: Configure the op_type of the nodes in the linked list to be 0x00

Figure 10-13 One of the DMA data handling applications



3×3 template filtering

Output the source image after filtering in 3×3 blocks.

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: single componentÿsingle component; SP420ÿSP420; SP422ÿSP422.

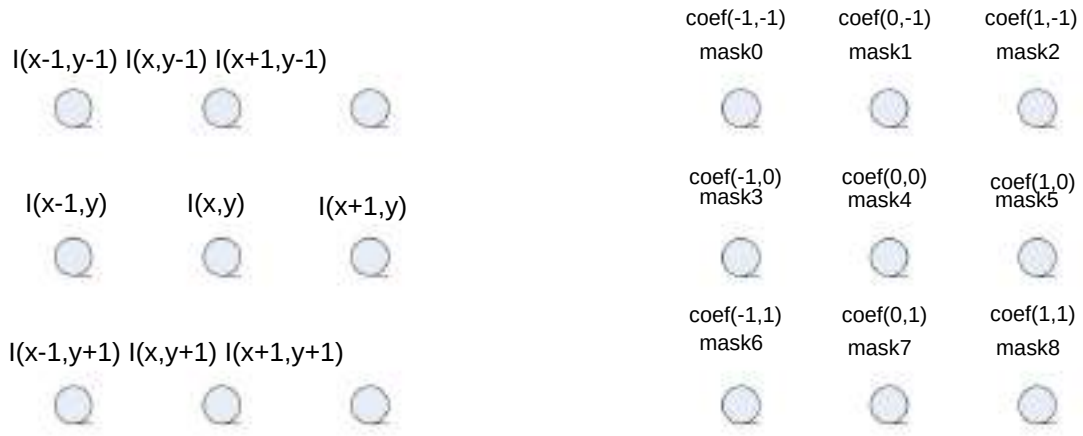
Instructions:

Configure op_type as 0x1.

Configure the input

format. Configuration coefficients mask0, mask1, ... mask9. The range of mask0ÿmask8 is [-128, 127], and the value of mask9 is [0, 10].

Figure 10-14 3×3 template filter calculation formula



$$lout_{yx}(\ ,\ ) = \sum_{j=-1}^{1}\sum_{i=-1}^{1} I(x+i, y+j) \cdot coef(i,j) \quad >> \ mask\ 9$$

Color Space Conversion (CSC)

Color space conversion supports conversion from YUV space to RGB space.

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: SP420ÿRGB package; SP420ÿRGB planar; SP422ÿRGB package; SP422ÿRGB planar.

Instructions:

Configure the op_type of the nodes in the linked list to be 0x02.

Configure the in_fmt of the nodes in the linked list:

01ÿ420

10ÿ422

Configure the out_fmt of the nodes in the

linked list: 0000: package

0001ÿplanar

Configure the csc_fmt of the nodes in the linked list:

00ÿBT601&BT656 ÿ16~235ÿ

01ÿBT709ÿ16~235ÿ

10ÿBT601&BT656 ÿ0~255ÿ

11ÿBT709ÿ0~255ÿ

When csc_fmt = 0 or 1, it is the video conversion from YUV to RGB, and the output satisfies 16ÿR, G, Bÿ235

When csc_fmt = 2 or 3, it is the image conversion from YUV to RGB, and the output satisfies 0ÿR, G, Bÿ255

The input and output requirements of the video matrix for conversion from YUV to RGB are as follows.

16ÿYÿ235

16ÿCbÿCrÿ240

16ÿRÿGÿBÿ235

The video matrix algorithm for converting YUV to RGB is shown in Table 10-2.

Table 10-2 YCbCr to RGB video matrix (BT.601)

RGB to YCbCr color space conversion floating point calculation method:									
R	ÿ 1		xÿYÿ	ÿ 0.0		xÿCb 128ÿ	ÿ	1.371 xÿCr	128ÿ
G	ÿ 1		xÿYÿ	ÿ 0.336	xÿCb 128ÿ			0.698 xÿCr	128ÿ
B	ÿ 1		xÿYÿ	ÿ 1.732	xÿCb 128ÿ		ÿ	0.0	xÿCr 128ÿ

Table 10-3 YCbCr to RGB video matrix (BT.709)

RGB to YCbCr color space conversion floating point calculation method:									
R	ÿ 1		xÿYÿ	ÿ 0.0		xÿCb 128ÿ	ÿ	1.540 xÿCr	128ÿ
G	ÿ 1		xÿYÿ	ÿ 0.183	xÿCb 128ÿ			0.459 xÿCr	128ÿ
B	ÿ 1		xÿYÿ	ÿ 1.816	xÿCb 128ÿ		ÿ	0.0	xÿCr 128ÿ

The input and output requirements of the image matrix for conversion from YUV to RGB are as follows.

16ÿYÿ235

16ÿUÿVÿ240

0ÿRÿGÿBÿ255

The image matrix algorithm for conversion from YUV to RGB is shown in Table 10-4.

Table 10-4 YCbCr to RGB image matrix (BT.601)

RGB to YCbCr color space conversion floating point calculation method:								
R	ÿ 1.164	xÿY-16ÿ		ÿ 0.0		xÿCb-128ÿ ÿ 1.596	xÿCr-128ÿ	

RGB to YCbCr color space conversion floating point calculation method:									
G	ÿ 1.164 xÿY-16ÿ			ÿ 0.391 xÿCb-128ÿ		ÿ 0.813 xÿCr-128ÿ			
B	ÿ 1.164 xÿY-16ÿ			ÿ 2.018 xÿCb-128ÿ		ÿ 0.0			xÿCr-128ÿ

Table 10-5 YCbCr to RGB image matrix (BT.709)

RGB to YCbCr color space conversion floating point calculation method:									
R	ÿ 1.164 xÿY-16ÿ			ÿ 0.0		xÿCb-128ÿ ÿ		1.793 xÿCr-128ÿ	
G	ÿ 1.164 xÿY-16ÿ			ÿ 0.213 xÿCb-128ÿ ÿ				0.534 xÿCr-128ÿ	
B	ÿ 1.164 xÿY-16ÿ			ÿ 2.115 xÿCb-128ÿ ÿ				0.0	xÿCr-128ÿ

3×3 template filter plus CSC

The source image is filtered with a 3 x 3 template, and then output after color space conversion.

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: SP420ÿRGB package; SP420ÿRGB planar; SP422ÿRGB package; SP422ÿRGB planar.

Instructions:

Configure op_type as 0x3.

Configure the CSC

coefficients. Configure the input format

and output format. Configuration coefficients mask0, mask1, ... mask9. The range of mask0ÿmask8 is [-128, 127], and the value of mask9 is [0, 10].

SOBEL x/y direction gradient calculation

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

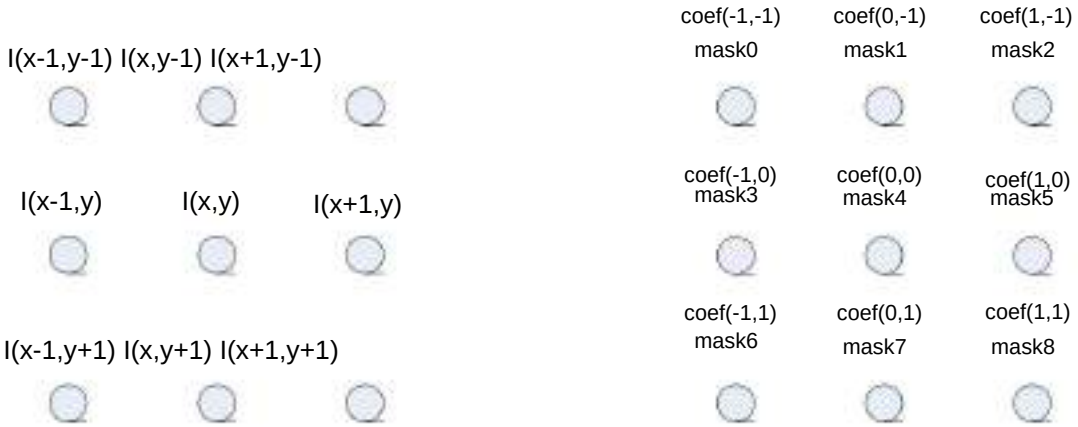
Input and output format: single componentÿSOBEL_OUT.

Instructions:

Configure op_type as 0x4.

Configuration coefficients mask0, mask1, ... mask8. The range of mask0ÿmask8 is [-128, 127].

Figure 10-15 SOBEL gradient calculation formula



$$Wood(x,y) = \sum_{j=-2}^{2} \sum_{i=-2}^{2} I(x+i, y+j) \cdot coef(i,j)$$

$$Vout(x,y) = \sum_{j=-2}^{2} \sum_{i=-2}^{2} I(x+i, y+j) \cdot coef(i,j)$$

CANNY gradient magnitude and angle

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: single componentÿCANNY_OUT1; single componentÿCANNY_OUT2.

Instructions:

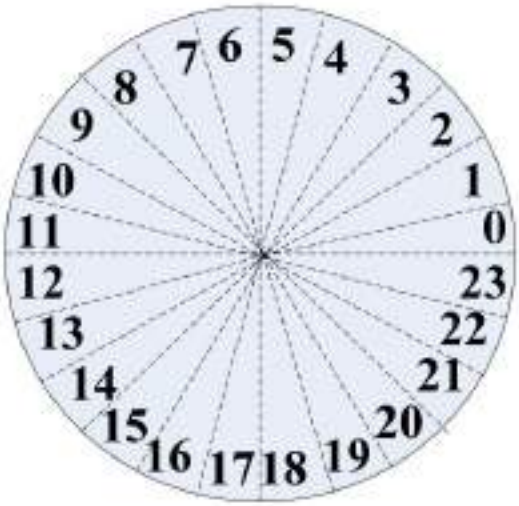
Configure op_type as 0x5.

Configure the output

format. Configuration coefficients mask0, mask1, ... mask8. The range of mask0ÿmask8 is [-128, 127].

Amplitude definition: Mag(x, y) = *abs(Hout(x,* y)) + *abs(Vout(x,* y))

Figure 10-16 CANNY angle quantification definition



Calculate the output angle as: $i = \frac{\arctan(\frac{V}{H}) * 12}{Pi}$

3x3 expansion

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: single componentÿsingle component.

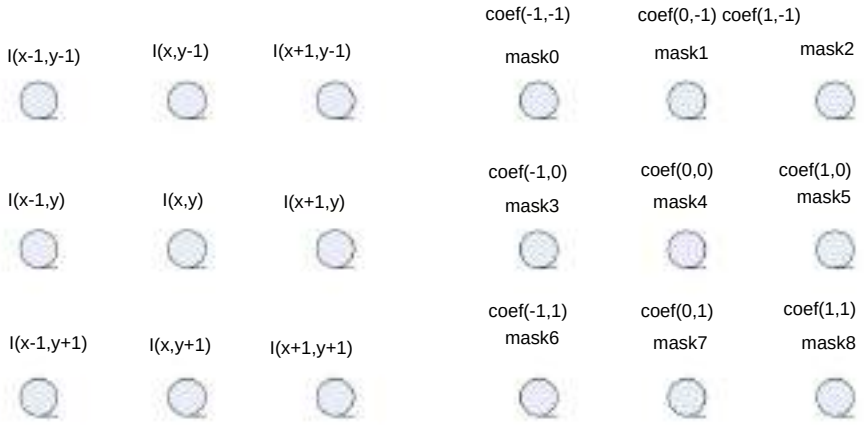
Instructions:

Configure op_type as 0x6. Configuration

coefficients mask0, mask1, ... mask8.

The input and output data are required to be 0 or 255, and the value of mask is 0 or 255.

The calculation formula of 3x3 expansion is as follows, where | in the formula is a bitwise OR operation, & is a bitwise AND operation, and % is a division operation.



$$out(x,y) = \begin{cases} \min\{Max, Ac\} & Th_{min} \le Ac \le Th_{max} \\ Ac & \text{else} \end{cases}$$

$$Ac = \sum_{k=0}^{8} coef\,k\,(k\%3)\,\&\,((k\&3)-1,(k\%3)-1),|,0,8) + y(k\%3)-1)$$

3x3 corrosion

Image resolution: 64 x 64 to 1920 x 1024.

Address alignment: both input and output addresses require 8byte alignment.

Input and output formats: single componentÿsingle component.

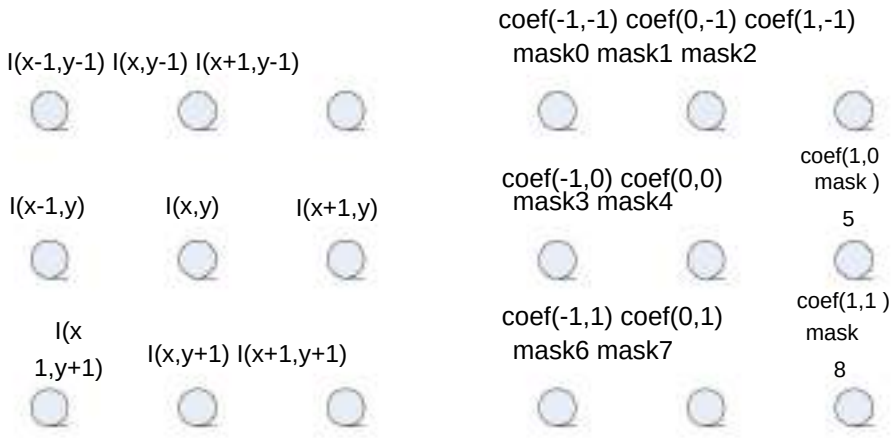
Instructions:

Configure op_type as 0x7.

Configuration coefficients mask0, mask1, ... mask8. The

input and output data are required to be 0 or 255, and the value of mask is 0 or 255.

The calculation formula of 3x3 corrosion is as follows, where | in the formula is a bitwise OR operation, & is a bitwise AND operation, and % is a division operation.



$$out(x,y) = \begin{cases} \min\{Max, Ac\} & Th_{min} \le Ac \le Th_{max} \\ Ac & \text{else} \end{cases}$$

$$Ac = \sum_{k=0}^{8} coef\,k\,(k\%3)\,\&\,((k\&3)-1,(k\%3)-1),\&,0,8) \times I(x+(k\&3)-1,y+(k\%3)-1)$$

Image binarization

Use a fixed threshold to binarize the image. There are three modes:

mode=2: pixel value > threshold threshold, the pixel value remains unchanged, otherwise it is minValue

$$I_{out}(x,y) = \begin{cases} minValue & (x,y) \le threshold \\ I(x,y) & (x,y) > threshold \end{cases}$$

mode=1: pixel value > threshold threshold, then it is maxValue, otherwise the pixel value remains unchanged

$$I_{out}(x,y) = \begin{cases} I(x,y) & (x,y) \le threshold \\ maxValue & (x,y) > threshold \end{cases}$$

mode=0: pixel value > threshold threshold, then maxValue, otherwise minValue

$$I_{out}(x,y) = \begin{cases} minValue & (x,y) \le threshold \\ maxValue & (x,y) > threshold \end{cases}$$

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: Both input and output addresses require byte alignment.

Input and output formats: single componentÿsingle component.

Instructions:

Configure the op_type of the nodes in the linked list to be 0x08;

configure the corresponding threshold, minValue and maxValue of the nodes mask0, mask1 and mask2 in the configured linked list.

Dual Source Image and Computing

注意

The height and width of source image 2 and source image 1 are required to be consistent, but the stride is not required to be consistent.

The data in source image 2 is ANDed with the data in source image 1, and then moved to the destination area.

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: Both input and output addresses require byte alignment.

Input and output formats: single componentÿsingle component.

How to use: configure the op_type of the nodes in the linked list to be 0x09.

$$I_{out}(x,y) = I_{src1}(x,y) \& I_{src2}(x,y)$$

Wherein, & in the formula is a bitwise AND operation.

Dual source image subtraction

注意

The height and width of source image 2 and source image 1 are required to be consistent, but the stride is not required to be consistent.

The data in source image 2 is subtracted from the data in source image 1, and then moved to the destination area. Two working modes are provided:

0000: output the absolute value of the difference, that is, dst[i, j] = *abs(src1[i,* j] ÿ src2[i, j];

0001: The difference value is shifted to the right by 1 bit, and the sign bit is reserved, that is, dst[i, j] = (src1[i, j] ÿ src2[i, j]) >> 1;

For example, the pixel value of a certain position in image 1 is 0x23, and the corresponding pixel value of image 2 is 0x40, then the result is 0x1D in mode 0000, and 0xF1 in mode 0001.

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: Both input and output addresses require byte alignment.

Input and output formats: single componentÿsingle component.

Instructions:

Configure the op_type of the nodes in the linked list as 0x0a;

configure the out_fmt of the nodes in the linked list as 0x0000 or 0x0001.

Dual Source Image OR Operation

注意

The height and width of source image 2 and source image 1 are required to be consistent, but the stride is not required to be consistent.

The data in source image 2 is ORed with the data in source image 1, and then moved to the destination area.

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: Both input and output addresses require byte alignment.

Input and output formats: single componentÿsingle component.

How to use: Configure the op_type of the nodes in the linked list to be 0x0b.

$$I_{out}(x, y) = I_{src1}(x, y) \mid I_{src2}(x, y)$$

Wherein, in the formula | is a bit-OR operation.

Integral graph

Support component cumulative sum and component square cumulative sum, the output format is 64 bits, the component cumulative sum occupies the lower 28 bits, and the component square cumulative sum occupies the upper 36 bits.

Image resolution: 64 x 64 to 1920 x 1080.

Address alignment: both input and output addresses require 8byte alignment.

Input and output format: single component ÿ INTEGRAL_OUT.

How to use: configure the op_type of the nodes in the linked list to be 0x0c.

$$I_{sum}(x, y) = \sum_{i=0}^{x} \sum_{j=0}^{y} I(i, j)$$

$$I_{sq}(x, y) = \sum_{i=0}^{x} \sum_{j=0}^{y} (I(i, j) * I(i, j))$$

$$I_{out}(x, y) = (I_{sum}(x, y) \& 0x\ FFFFFFF) | (I_{sq}(x, y) << 28)$$

Wherein, in this formula, | is a bit-OR operation, & is a bit-AND operation, and << is a left shift operation.

histogram

256-level histogram statistics, the input is a single component, and the output is a 256-level histogram statistical value with a bit width of 32bit.

Image resolution: 64x64ÿ1920x1080.

Address alignment: both input and output addresses require 8byte alignment.

Input and output format: single componentÿHIST_OUT.

How to use: configure the op_type of the nodes in the linked list to be 0x0d.

$$I_{out}(x) = \sum_{i,j} ((I(i, j) == x)?1: 0) \qquad x = 0K255$$

10.4 Register overview

An overview of the IVE registers is shown in Table 10-6 .

Table 10-6 IVE register overview (base address is 0x205E_0000)

offset address name		describe	page number
0x0000	IVE_START	Start signal register	10-23
0x0004	INT_EN	Interrupt Enable Signal Register	10-23
0x0008 INT_RW		Raw Interrupt Signal Register	10-24
0x000C INT_STATUS		Interrupt Status Signal Register	10-25

offset address	name	describe	page number
0x0010	LIST_POINTER	linked list first address register	10-25
0x0014	IVE_STATUS	IVE working status signal register	10-26
0x0018	IVE_TASK_ID	ID register of the task just completed	10-26

10.5 Register Description

IVE_START

IVE_START is the start signal register.

Offset Address	Register Name	Total Reset Value
0x0000	IVE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ive_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WO	ive_start	IVE start signal, active high.

INT_EN

INT_EN is the interrupt enable signal register.

Offset Address	Register Name	Total Reset Value
0x0004	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	list_int_en	Linked list interrupt enable. 0: disable; 1: enable.
[0]	RW	node_int_en	Node interrupt enable. 0: disable; 1: enable.

INT_RW

INT_RW is the raw interrupt signal register.

Offset Address	Register Name	Total Reset Value
0x0008	INT_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	list_int_rw	Linked list-level primitive interrupts. Software clears the interrupt by writing INT_RW after reading the interrupt through INT_STATUS. 0: no interrupt; 1: interrupt.

[0] RW node_int_rw			Node-level raw interrupts. Software clears the interrupt by writing INT_RW after reading the interrupt through INT_STATUS. 0: no interrupt; 1: There is an interrupt.

INT_STATUS

INT_STATUS is the interrupt status signal register.

Offset Address	Register Name	Total Reset Value
0x000C	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2] RO		reserved	reserve.
[1]	RO	list_int_status	Linked list level interrupt status. Software can determine whether there is a list-level interrupt by reading this status bit. 0: no interrupt; 1: There is an interrupt.
[0]	RO	node_int_status	Node-level outage status. Software can determine if there is a node-level interrupt by reading this status bit. 0: no interrupt; 1: There is an interrupt.

LIST_POINTER

LIST_POINTER is the first address register of the linked list.

Offset Address	Register Name	Total Reset Value
0x0010	LIST_POINTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	link_table_header_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	link_table_header_ addr	the address of the first node of the linked list.

IVE_STATUS

IVE_STATUS is the IVE working status signal register.

Offset Address	Register Name	Total Reset Value
0x0014	IVE_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	idle; ive_working_status	The current working state of the IVE. 0: 1: Busy.

IVE_TASK_ID

IVE_TASK_ID is the ID register of the task just completed.

Offset Address	Register Name	Total Reset Value
0x0018	IVE_TASK_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ive_task_id	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	ive_task_id	The ID of the task that was just completed. If a task ID is incrementing, it means that all tasks before this ID have completed.

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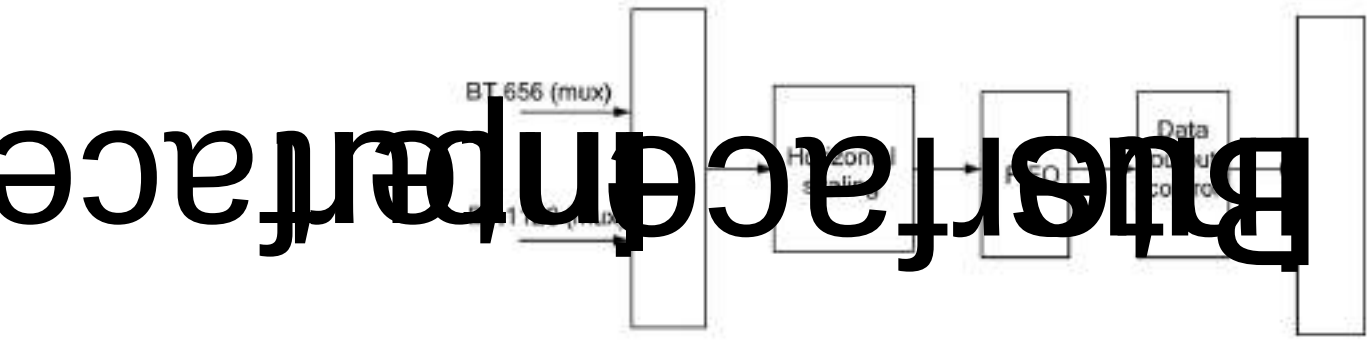
11 video interface

11.1 VICAP

11.1.1 Overview

The video capture unit VICAP (Video capture) can receive video data through the BT.656 (mux)/BT.1120 (mux) interface and store it in the specified memory area. During this process, VICAP can horizontally reduce the video image data (possibly simple downsampling or scaling according to the channel situation) and output multiple different video streams. The functional block diagram of VICAP is shown in Figure 11-1 .

Figure 11-1 Functional block diagram of VICAP



11.1.2 Features

VICAP has the following features:

- Input maximum resolution is 1920x1080
- External support 2 BT.656 interfaces, or 1 BT.1120 interface (Hi3515A only supports 1 BT.656 interface)
- Internally supports 2 ports and 8 channels of video processing, each channel supports interlaced and progressive input modes (Hi3515A supports 1 port and 4 channels)
- Support BT.656 (mux), BT.1120 (mux) and other timing
- Support SMPTE293M/ITU-R BT.1358 timing (480P/576P)

Support SMPTE 274M/BT 1120 timing (1080i/1080P) Support SMPTE 296M (720P)

Support up to 2 times the horizontal integer multiple reduction

Each channel supports 2-level bus priority configurable

Supports data acquisition within a specified window

Supports statistical brightness function of acquired data

Supports horizontal mirror and vertical mirror

output formats Supports storage modes: SPYCbCr 4:2:0 and SPYCbCr 4:2: 2 modes.

11.1.3 Functional Description

11.1.3.1 Typical applications

VICAP is a video input acquisition unit that supports multiple timing inputs. It stores the captured video data in DDR. The system can be configured with different function modes, so that it can flexibly adapt to different external input video interfaces and support a variety of external input device.

VICAP occupies a total of 18 pins, 2 clocks, and 16 data lines.

The VICAP module has 2 ports and 8 channels in total. Each port can analyze the timing of one docking chip, and each channel can process one video signal.

Each port corresponds to 4 channels. The 2 ports are independent of each other and can be combined arbitrarily.

It can connect two docking chips with 8bit data lines, and use two ports.

A docking chip that can be connected to a 16bit data line, using 1 port.

Each port can be connected to any one of 4 channels of D1/960H, 2 channels of D1/960H, 1 channel of D1/960H, and 1 channel of 720P.
1080P60 can only be connected to port 0, the docking chip that connects to the 16bit data line.

The typical input of VICAP has the following 3 types:

8 channels D1/960H

2 channels 720P

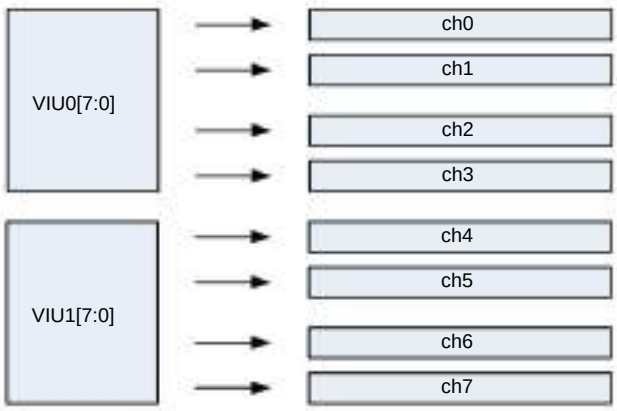
1 channel 1080P

The two BT.656 ports on the pins have a clock respectively, namely VIU0_CLK and VIU1_CLK. If two BT.656 ports are used as a 16-bit data input, VIU0_CLK or VIU1_CLK can be used; if two 8-bit data inputs are used, VIU0 uses VIU0_CLK, and VIU1 uses VIU1_CLK.

8 channels D1/960H

The typical input application of 8-channel D1/960H is shown in Figure 11-2 .

Figure 11-2 Typical input application of 8-channel D1/960H



Each 8bit data pin transmits 4 channels of time-division multiplexed D1/960H, using a total of 16bit pins.

VIU0 means the 0th BT.656 port on the pin VIU1 means the 1st

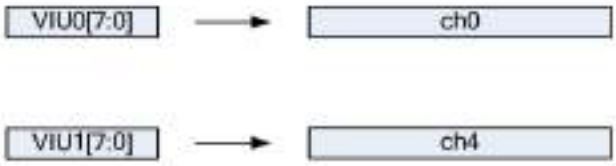
BT.656 port on the pin [7:0] means the 7th to 0bit ch0 to ch7

means channel 0 to channel 7

2 channels 720P

The typical input application of 2 channels of 720P is shown in Figure 11-3 .

Figure 11-3 Typical input application of 2-channel 720P



Each 8bit data pin transmits 1 channel of 720P, using a total of 16bit pins (interleave mode, the 16bit data line of BT.1120 is transmitted through 8bit through time division multiplexing, the C component is in the front, the Y component is in the back, double the clock frequency). in:

VIU0 indicates the 0th BT.656 port on the pin

VIU1 indicates the first BT.656 port on the pin [7:0] indicates the

7th to 0bit ch0 to ch7 indicates

channel 0 to channel 7

1 channel 1080P

A typical input application of 1 channel 1080P is shown in Figure 11-4 .

Figure 11-4 Typical input application of 1 channel 1080P

Two 8bit data pins form one BT.1120 port input and one channel of 1080P, using a total of 16bit pins. in:

VIU0 means the 0th BT.656 port on the pin VIU1 means

the 1st BT.656 port on the pin [7:0] means the 7th to 0bit

ch0 to ch7 means channel 0 to

channel 7

mixed timing input

Different docking chips are independent of each other, do not affect each other, and can be combined arbitrarily. For example, VIU0 inputs 1 channel of HD interleave, and VIU1 inputs 4 channels of D1.

11.1.3.2 Functional principle

ITU-R BT.656 YCbCr4:2:2

(1) Horizontal timing

In the ITU-R BT.656 protocol, the synchronization signal is integrated in the data stream, and the special bytes SAV and EAV in the data stream represent the beginning and end of valid line data respectively. In the video data stream, the terminal of the timing reference codeword composed of FF 00 00 (FF, 00 is the reserved value of image coding data, which is non-image data) marks the next byte as SAV or EAV, ITU- The row data stream format of R BT. 656 is shown in Table 11-1 .

Table 11-1 ITU-R BT.656 YCbCr 4:2:2 row data format

timing reference code	line blanking area	timing reference code	720 effective pixels YCbCr 4:2:2
FF 00 00 EAV 80 10 …	80 10 FF 00 00 SAV	Cb0 Y0 Cr0 Y1 …	Cr718 Y719

The difference between SAV and EAV is distinguished by the special bit "H" of SAV/EAV, and SAV/EAV also includes the vertical blanking bit "V" and the field indicator bit "F". The specific description of SAV/EAV is shown in Table 11-2 .

Table 11-2 SAV/EAV format

bit[7]	bit[6](F)	bit[5](V)	bit[4](H)	bit[3:0](P3ÿP0)
Fixed value 1	field indicator bit 1st fieldÿF=0 2nd fieldÿF=1	vertical blanking bit VBIÿV=1 Active videoÿV=0	SAVÿH=0 EAVÿH=1	Check Digit.

The ITU-R BT.656 protocol uses 8 effective reserved bits to define effective SAV and EAV, and 4 parity bits can correct 1-bit errors and detect 2-bit errors. Valid SAV/EAV values are shown in Table 11-3 .

Table 11-3 Valid SAV/EAV values

coding	binary value	field number	vertical consumption
SAV	10000000	1	-
EAV extension	10011101	1	-
SAV	10101011	1	yes
EAV extension	10110110	1	yes
SAV	11000111	2	-
EAV extension	11011010	2	-
SAV	11101100	2	yes
EAV extension	11110001	2	yes

The 4 effective reserved bits also play the role of error correction. P0, P1, P2, and P3 are determined by F, V, and H bits, as shown in Table 11-4 .

Table 11-4 ITU-R BT.656 error correction code table

F	IN	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

in:

P0=F^V^H

P1=F^V

P2=F^H

P3=V^H

(2) Vertical timing

The vertical timing is also realized through the "F" and "V" of the timing reference code SAV/EAV. The vertical timing of typical 525-line and 625-line video systems is shown in Figure 11-5 and Figure 11-6 .

Figure 11-5 Vertical timing of 525-line 60 field/second video system

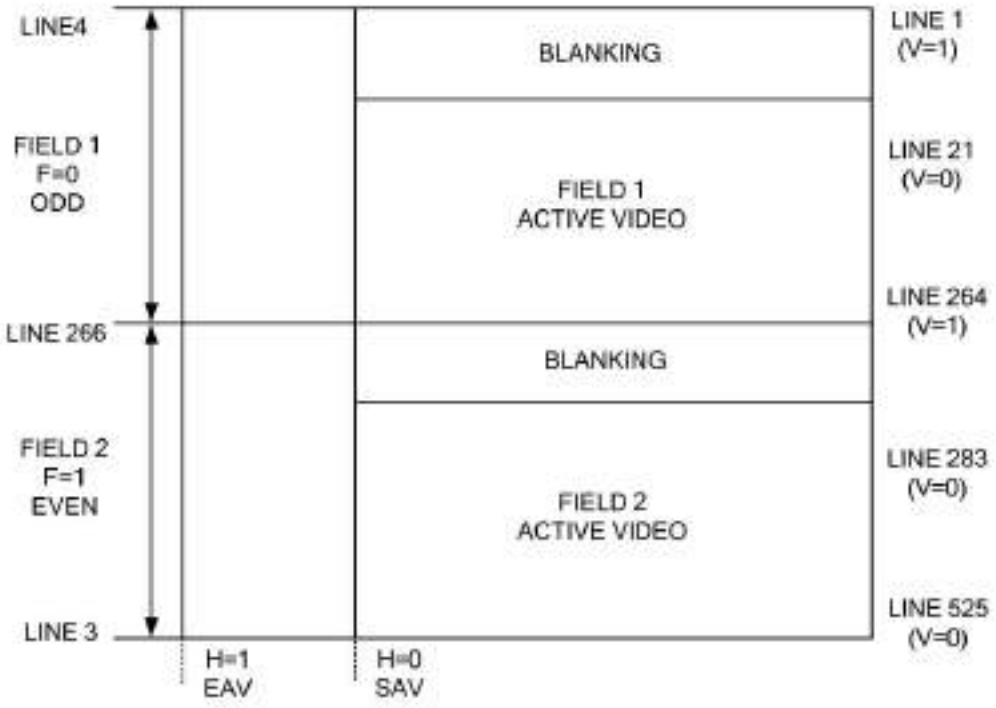
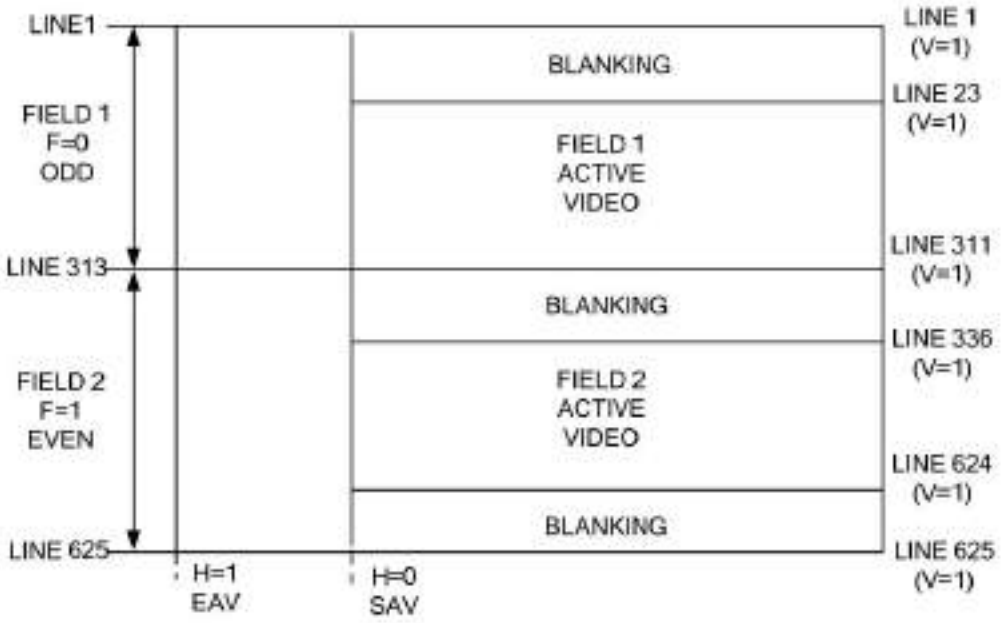


Figure 11-6 Vertical timing of 625-line 50 fields/second video system



Note: VICAP only recognizes vertical timing based on SAV/EAV, and does not limit which row it is in.

BT 1120 (HD) interface timing

VICAP supports the timing sequence of high-definition interface with Y/C separate input. At this time, two ports are needed, one port is used to transmit brightness, and the other port is used to transmit chroma, as shown in Figure 11-7 and Figure 11-8 .

Figure 11-7 HD interface input timing horizontal timing

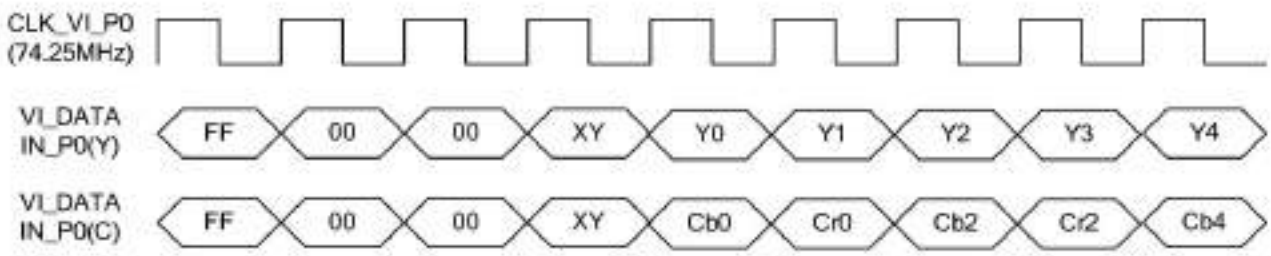
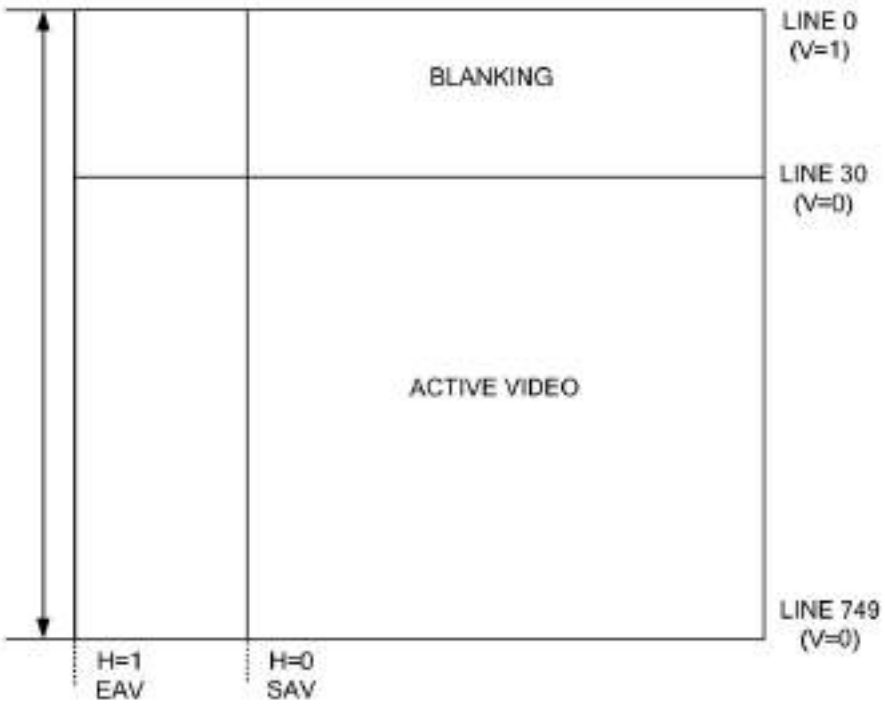


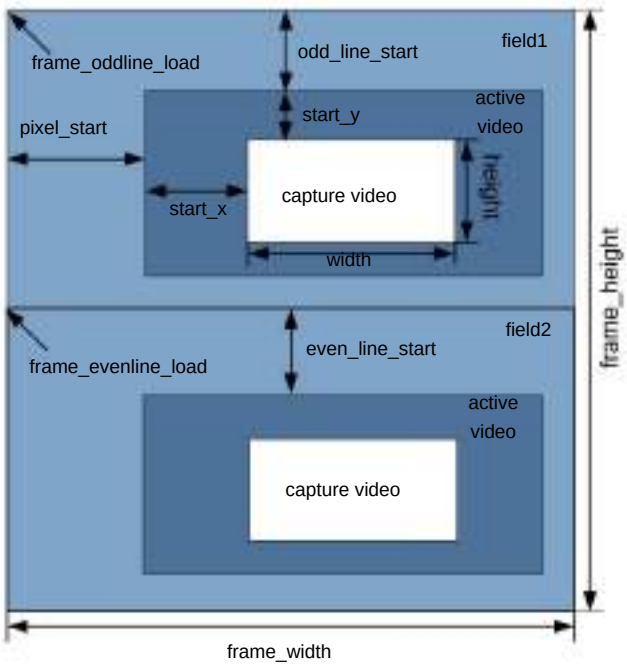
Figure 11-8 HD interface input timing vertical timing



11.1.3.3 Image CROP

The valid video range is shown in Figure 11-9 . Starts after horizontal blanking and vertical blanking. However, the actually displayed viewing area is often included within the range of the effective video, and is slightly reduced relative to the boundary of the effective video, in order to avoid edge effects.

Figure 11-9 Relationship between effective image area and horizontal and vertical blanking



11.1.3.4 Image storage mode

Image storage modes include:

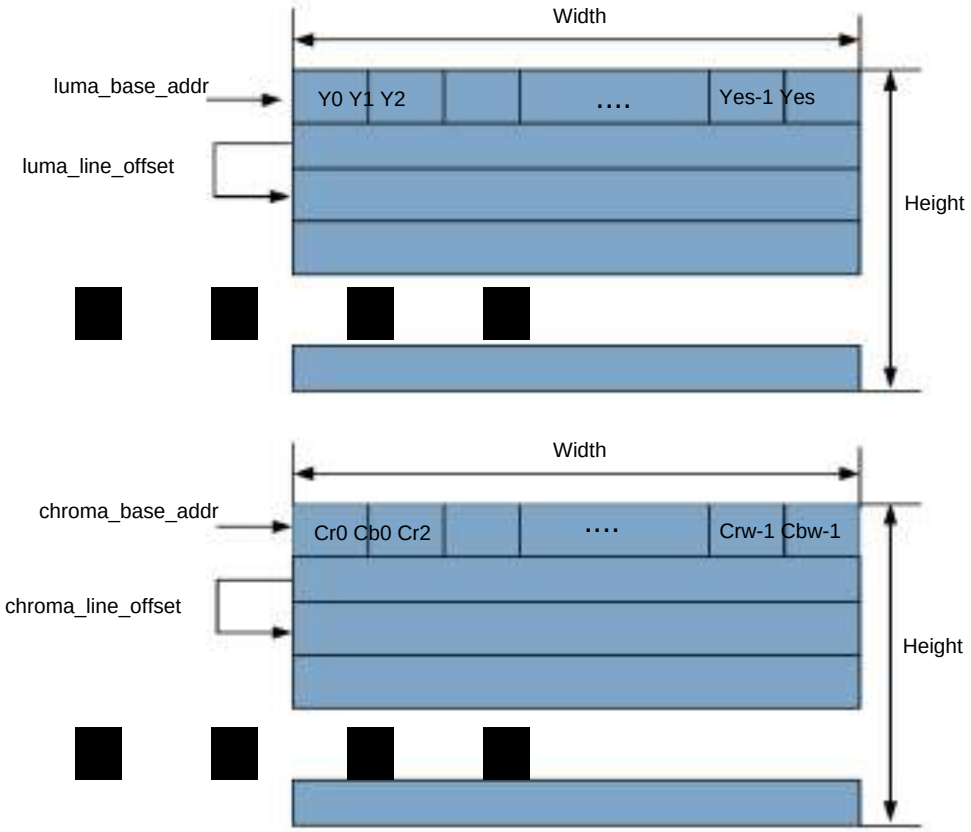
Semi-planar YcbCr storage system After the

view area is set, the read-in data is stored in semi-planar mode, that is, the luminance component and chrominance component are stored in the luminance storage space and chrominance storage space of DDR respectively.

In one line, the luma and chrominance components are stored consecutively. The storage

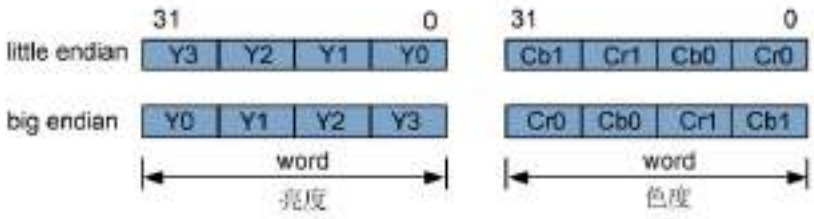
between two consecutive lines can be defined by the system-defined storage interval parameter offset between the beginning of the line and the beginning of the line. The storage location of luma and chrominance components in DDR is indicated by the starting address base_addr. VI Capture is shown in Figure 11-10 .

Figure 11-10 YCbCr4:2:2 storage mode



In DDR, data is stored in word (32bit) units. A 32bit word is composed of 4 8bit pixels. When 4 bytes constitute a word, there are two ways: big endian and little endian. Figure 11-11 uses luma and chroma components as an example to illustrate the storage methods of big endian and little endian.

Figure 11-11 big endian and little endian image storage modes



VICAP only supports DDR which stores data in little endian mode.

11.1.3.5 Horizontal mirror and vertical mirror (mirror and flip)

When the sensor is installed and the lens is horizontally and vertically reversed, the output image can be corrected by the horizontal and vertical mirroring of VICAP. The horizontal and vertical mirroring is realized by writing the reverse processing of the DDR address, but the frame must be guaranteed The starting first address is 128bit aligned.

11.1.4 Working method

11.1.4.1 reg_newer function of VICAP

Before the software enables a VICAP channel, the software should complete the following operations: ÿComplete the configuration of VICAP attribute registers. ÿWrite the reg_newer bit as "1" to inform the VICAP module that the current register is ready. After enabling VICAP, the VICAP logic starts to work. When a field/frame arrives, there will be: ÿ

If reg_newer is 0, VICAP will not receive data, and the hardware state will be set to SNOOZE, etc.

Waiting for the arrival of the data of the next field/frame.

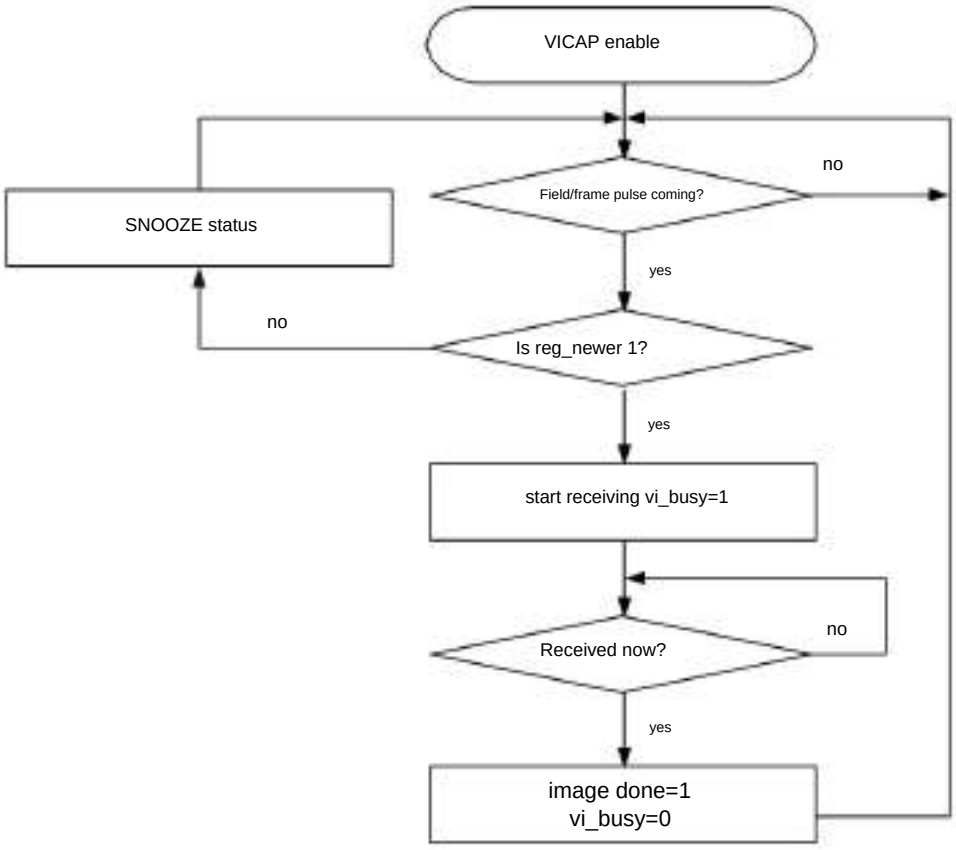
ÿ If reg_newer is 1, start to receive data, give register update interrupt (reg_update_int) at the same time, and set the hardware status to busy.

After receiving the current data, clear the hardware busy state. When the next field/frame arrives, then: ÿ If reg_newer is 0, give up receiving the next field/frame data. ÿIf reg_newer is 1, it can continue to receive the data of the next field/frame following the previous data.

11.1.4.2 Hardware workflow

The hardware workflow of VICAP is shown in Figure 11-12 .

Figure 11-12 VICAP hardware workflow

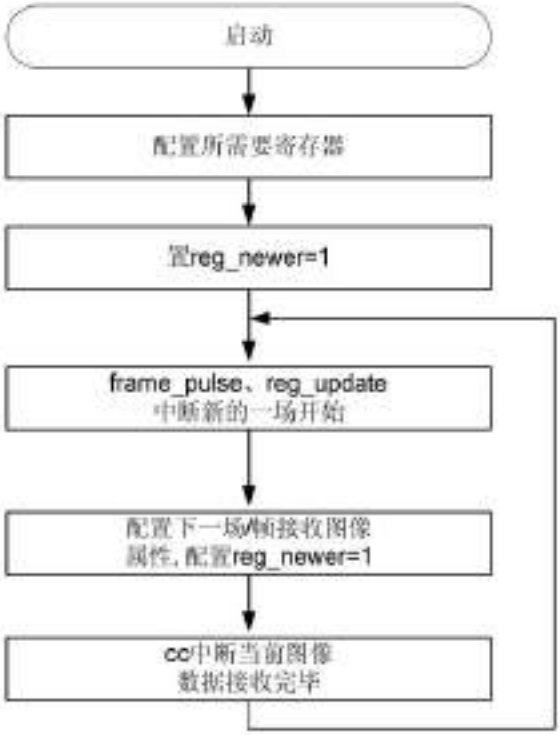


After receiving specified data of one field/frame, VICAP will detect the reg_newer bit when the next field arrives. If the reg_newer bit is 1 (indicating that the software has updated or confirmed the VICAP register), VICAP will automatically load the register value configured by the software to the working register (the working register software cannot be accessed), then clear the reg_newer bit to 0, and start receiving the next field/frame data. Otherwise, start receiving data only when reg_newer is 1 and a new field/frame arrives.

11.1.4.3 Software configuration process

In the interrupt mode, the operating flow of the software is shown in Figure 11-13 .

Figure 11-13 Software operation process



When using BT.656 mode and BT.1120 mode, there is no need to configure the timing register.

11.1.5 Register overview

The VICAP register space allocation is shown in Figure 11-14 .

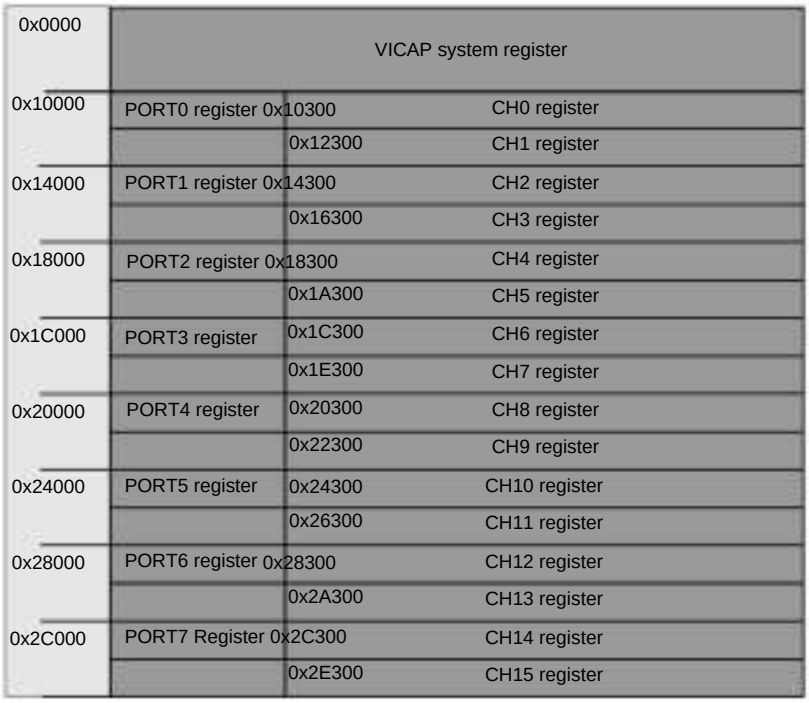
注意

Since there are at most 2 external ports, the registers prefixed with PT_ in Table 11-5 only exist in channels 0 and 4; 0x0000~0x0200 are VICAP system registers.

Data from port 0 can be routed to channels 0, 1, 2, 3. Data

from port 1 can be routed to channels 4, 5, 6, 7.

Figure 11-14 VICAP register space allocation



Note: The address marked with 0x in the figure is the offset address

An overview of the registers is shown in Table 11-5 .

说明

The registers in Table 11-5 are for PORT0 and CH0.

PT_XXX in Table 11-5 is introduced using PORT0 as an example. Compared with PORT0, the registers of PORT1~PORT7 are the same except for the offset address;

CH_XXX in Table 11-5 is introduced using chn0 as an example. CH1 Compared with CH0, the registers of ~CH15 are the same except for the offset address.

Table 11-5 Register overview (base address is 0x2058_0000)

offset address name		describe	page number
0x0000 WK_MODE		Global Working Configuration Register	11-15
0x0004	AXI_CFG	bus configuration register	11-15
0x0008	MIXER0_PRO_CFG0	MASTER priority configuration register	11-16
0x0100	VICAP_INT	Interrupt Indicator Register	11-17

offset address name	describe	page number
0x10000 PT_INTF_MOD	Interface Mode Register	11-18
0x10004 PT_R_MASK_L	R component mask register	11-20
0x10008 PT_B_MASK_L	B component mask register	11-20
0x1000C PT_G_MASK_L	G component mask register	11-20
0x10014 PT_R_OFFSET_L	R component offset register	11-21
0x10018 PT_B_OFFSET_L	B Component Offset Register	11-21
0x1001C PT_G_OFFSET_L	G component offset register	11-22
0x10040 PT_TEST_CFG	Interface Test Configuration Register	11-22
0x10044 PT_ID_STATUS	Interface ID Status Register	11-23
0x10300 CH_INTF_CFG0	Interface Timing Register 0	11-23
0x10304 CH_INTF_CFG1	Interface Timing Register 1	11-24
0x10360 CH_FSTART_DLY	Frame Synchronization Delay Register	11-26
0x10400 CH_CTRL	channel control register	11-26
0x10404 CH_REG_NEWER	Acquisition Control Register	11-27
0x10410 CH_CROP_START	CROP start position register	11-27
0x10414 CH_CROP_SIZE	CROP size register	11-27
0x10418 CH_YDES_SIZE	Original code stream brightness storage size register	11-28
0x1041C CH_CDES_SIZE	Original code stream chroma storage size register	11-28
0x10420 CH_YBASE_ADDR Original code stream brightness storage base address register		11-29
0x10424 CH_CBASE_ADDR Original stream chroma storage base address register		11-29
0x10428 CH_YLINE_OFFSET Raw code stream luminance line offset register		11-30
0x1042C CH_CLINE_OFFSET Original stream chroma line offset register		11-30
0x10430 CH_INT_RAW	Channel Raw Interrupt Register	11-30
0x10434 CH_INT	Channel Interrupt Register	11-32
0x10438 CH_INT_MASK	Channel Interrupt Mask Register	11-33
0x1043C CH_STATUS	Channel Status Register	11-34
0x10440 CH_IPI_STATUS_SIZE channel size indication register		11-35
0x10444 CH_IPI_STATUS_SEAV channel SEAV indication register		11-35
0x10500 CH_DITHER_CFG	Dither configuration register	11-36

offset address name	describe	page number
0x10504 CH_DITHER_COEF0	Dither Coefficient Register 0	11-36
0x10508 CH_DITHER_COEF1	Dither Coefficient Register 1	11-37
0x1050C CH_DITHER_SIZE	Input Image Width Registers 11-37 for Dither Module	
0x10510 CH_MIR_CTRL	Raw stream mirroring control register	11-37
0x10700 CH_MSC_CFG	Block Mask Configuration Register	11-38
0x10710 CH_BLOCK0_START block 0 mask start position register		11-39
0x10714 CH_BLOCK1_START block 1 mask start position register		11-39
0x10718 CH_BLOCK2_START block 2 mask start position register		11-40
0x1071C CH_BLOCK3_START block 3 mask start position register		11-40
0x10750 CH_BLOCK0_SIZE block 0 mask size register		11-41
0x10754 CH_BLOCK1_SIZE block 1 mask size register		11-41
0x10758 CH_BLOCK2_SIZE block 2 mask size register		11-42
0x1075C CH_BLOCK3_SIZE block 3 mask size register		11-42
0x10790 CH_BLOCK0_COLOR block 0 mask color register		11-42
0x10794 CH_BLOCK1_COLOR block 1 mask color register		11-43
0x10798 CH_BLOCK2_COLOR block 2 mask color register		11-43
0x1079C CH_BLOCK3_COLOR block 3 mask color register		11-44
0x10800 CH_VCDS_CFG	Main stream chroma vertical downsampling configuration register 11-44	
0x10808 CH_VCDS_COEF	Main stream chroma vertical downsampling coefficient register 11-45	
0x10940 CH_LHFIR_SPH	Brightness Horizontal Scaling Parameter Configuration Register 11-45	
0x10944 CH_CHFIR_SPH	Chroma Horizontal Scaling Parameter Configuration Register 11-46	
0x10948 CH_LHFIR_OFFSET Brightness scaling horizontal position offset register 11-46		
0x1094C CH_CHFIR_OFFSET Chroma scaling horizontal position offset register 11-47		
0x10B00 CH_Y_CLIP_CFG	Brightness CLIP Configuration Register	11-47
0x10B04 CH_C_CLIP_CFG	Chroma CLIP Configuration Register	11-48
0x10C00 CH_SUM_Y	Input Image Brightness and Statistics Registers 11-48	

11.1.6 Register Description

WK_MODE

WK_MODE is the global working configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RW	pt1_mode	Port 1 working mode. 0: D1 or 960H mode; 1: 720p mode.
[16]	RW	pt0_mode	Port 0 working mode. 0: D1 or 960H mode; 1: 720p or 1080p mode.
[15:1]	RO	reserved	reserve.
[0]	RW	power_mode	clock mode. 0: Low power consumption off; 1: Low power on.

AXI_CFG

AXI_CFG is the bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	AXI_CFG	0xF0F0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																m0_id				reserved											m0_otd	
Reset	1	1	1	1	0	0	0	0	1								1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:16]	RW	m0_id	ID number.
[15:4]	RO	reserved	reserve.
[3:0]	RW	m0_otd	outstanding number. outstanding should be greater than 0 and less than or equal to 4.

MIXER0_PRO_CFG0

MIXER0_PRO_CFG0 is the MASTER priority configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	MIXER0_PRO_CFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_c_pro	ch7_y_pro	ch6_c_pro	ch6_y_pro	ch5_c_pro	ch5_y_pro	ch4_c_pro	ch4_y_pro								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	ch7_c_pro	Channel 7 chroma priority setting, 0 is high priority.
[14]	RW	ch7_y_pro	Channel 7 brightness priority setting, 0 is high priority.
[13]	RW	ch6_c_pro	Channel 6 chroma priority setting, 0 is high priority.
[12]	RW	ch6_y_pro	Channel 6 brightness priority setting, 0 is high priority.
[11]	RW	ch5_c_pro	Channel 5 chroma priority setting, 0 is high priority.
[10]	RW	ch5_y_pro	Channel 5 brightness priority setting, 0 is high priority.
[9]	RW	ch4_c_pro	Channel 4 chroma priority setting, 0 is high priority.
[8]	RW	ch4_y_pro	Channel 4 brightness priority setting, 0 is high priority.

[7] RW ch3_c_pro		Channel 3 chroma priority setting, 0 is high priority.
[6] RW ch3_y_pro		Channel 3 brightness priority setting, 0 is high priority.
[5] RW ch2_c_pro		Channel 2 chroma priority setting, 0 is high priority.
[4] RW ch2_y_pro		Channel 2 brightness priority setting, 0 is high priority.
[3] RW ch1_c_pro		Channel 1 chroma priority setting, 0 is high priority.
[2] RW ch1_y_pro		Channel 1 brightness priority setting, 0 is high priority.
[1] RW ch0_c_pro		Channel 0 chroma priority setting, 0 is high priority.
[0] RW ch0_y_pro		Channel 0 brightness priority setting, 0 is high priority.

VICAP_INT

VICAP_INT is the interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x0100	VICAP_INT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	-
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

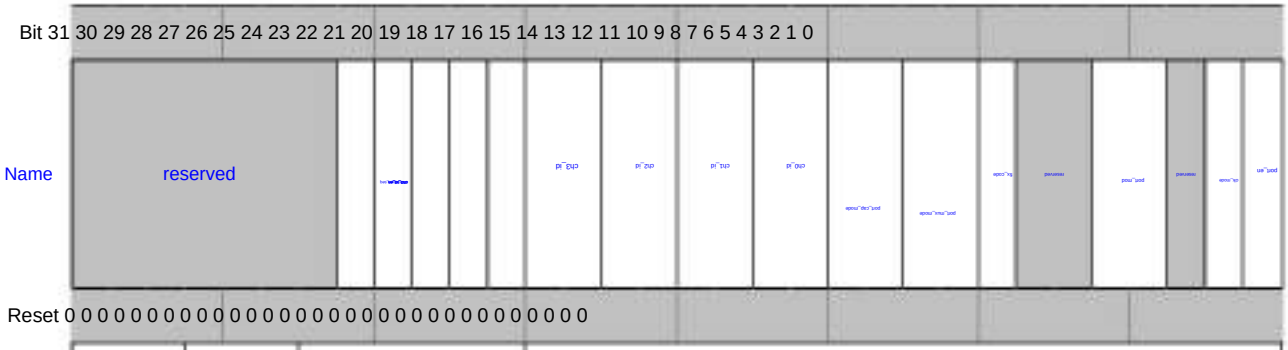
Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RO	int_ch7	Channel 7 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[6]	RO	int_ch6	Channel 6 interrupt indication. 0: no interrupt; 1: interrupt.
[5]	RO	int_ch5	Channel 5 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[4]	RO	int_ch4	Channel 4 interrupt indication. 0: no interrupt; 1: There is an interrupt.

[3]	RO	int_ch3	Channel 3 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[2]	RO	int_ch2	Channel 2 interrupt indication. 0: no interrupt; 1: interrupt.
[1]	RO	int_ch1	Channel 1 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[0]	RO	int_ch0	Channel 0 interrupt indication. 0: no interrupt; 1: There is an interrupt.

PT_INTF_MOD

PT_INTF_MOD is the interface mode register.

Offset Address	Register Name	Total Reset Value
0x10000	PT_INTF_MOD	0x0000_0000



Bits	Access Name		Description
[31:25] -		reserved	Port register, 2 ports in total. Offset address: 0x1_0000ÿ0x1_00FF is the address of port 0; 0x1_8000ÿ 0x1_80FF is the address of port 1; the following only lists the address of port 0, and the registers of other ports are the same as port 0.
[24] RW	interleave_seq		YC order when interleave. 0: C first; 1: Y comes first.

[23] RW ch3_id_en			3 Channel ID enable. 0: Do not detect ID; 1: Select data path by ID.
[22] RW ch2_id_en			2 Channel ID enable. 0: Do not detect ID; 1: Select data path by ID.
[21] RW ch1_id_en			1 Channel ID enable. 0: Do not detect ID; 1: Select data path by ID.
[20] RW ch0_id_en			0 Channel ID enabled. 0: Do not detect ID; 1: Select data path by ID.
[19:18] RW ch3_id			3 When the channel ID is enabled, the data channel is selected according to the ID.
[17:16] RW ch2_id			2 When the channel ID is enabled, the data channel is selected according to the ID.
[15:14] RW ch1_id			1 When channel ID is enabled, data lane is selected according to ID.
[13:12] RW ch0_id			0 When lane ID is enabled, data lane is selected based on ID.
[11:10] RW port_cap_mode			port mode. 00: BT656/BT.1120 mode; 11: interleave mode; Other: reserved.
[9:8] RW port_mux_mode			Composite mode. 00: 1-way compound mode; 01: 2-way compound mode; 10: 4-way compound mode; 11: Reserved.
[7] RW fix_code			The highest bit of synchronization code. 0: The highest bit of the synchronization code is 1; 1: The highest bit of the synchronization code is 0.
[6:5] RO		reserved	reserve.
[4:3] RW port_mod			port mode. 00: single component input; 01: double component input; Other: reserved.
[2]	RO	reserved	reserve.

[1] RW	clk_mode		clock mode. 0: rising edge sampling; 1: Sample on falling edge.
[0] RW	port_en		The port is enabled. 0: off; 1: enable.

PT_R_MASK_L

PT_R_MASK_L is the R component mask register.

Offset Address	Register Name	Total Reset Value
0x10004	PT_R_MASK_L	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	r_mask
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	r_mask	R component mask.

PT_B_MASK_L

PT_B_MASK_L is the B component mask register.

Offset Address	Register Name	Total Reset Value
0x10008	PT_B_MASK_L	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	b_mask
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	b_mask	B component mask.

PT_G_MASK_L

PT_G_MASK_L is the G component mask register.

Offset Address	Register Name	Total Reset Value
0x1000C	PT_G_MASK_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	g_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	g_mask	G component mask.

PT_R_OFFSET_L

PT_R_OFFSET_L is the R component offset register.

Offset Address	Register Name	Total Reset Value
0x10014	PT_R_OFFSET_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														r_offset	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	reserve.
[7:0]	RW	r_offset	R component offset.

PT_B_OFFSET_L

PT_B_OFFSET_L is the B component offset register.

Offset Address	Register Name	Total Reset Value
0x10018	PT_B_OFFSET_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														b_offset	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	reserve.
[7:0]	RW	b_offset	B component offset.

PT_G_OFFSET_L

PT_G_OFFSET_L is the G component offset register.

Offset Address	Register Name	Total Reset Value
0x1001C	PT_G_OFFSET_L	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved g_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:8]	- reserved	reserve.
[7:0]	RW g_offset	G component offset.

PT_TEST_CFG

PT_TEST_CFG is the interface test configuration register.

Offset Address	Register Name	Total Reset Value
0x10040	PT_TEST_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:3]	RO reserved	reserve.
[2]	RW interlace	Interlaced progressive mode. 0: row by row; 1: Interlace.
[1]	RW hsync_sel	Test mode line sync signal selection.
[0]	RW cbar_en	color_bar test enable. 0: off; 1: enable;

PT_ID_STATUS

PT_ID_STATUS is the interface ID status register.

Offset Address	Register Name	Total Reset Value
0x10044	PT_ID_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id3		id2		id1		id0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:6]	RO	id3	Channel 3 ID number.
[5:4]	RO	id2	Channel 2 ID number.
[3:2]	RO	id1	Channel 1 ID number.
[1:0]	RO	id0	Channel 0 ID number.

CH_INTF_CFG0

CH_INTF_CFG0 is interface timing register 0.

Offset Address	Register Name	Total Reset Value
0x10300	CH_INTF_CFG0	0x0000_0000

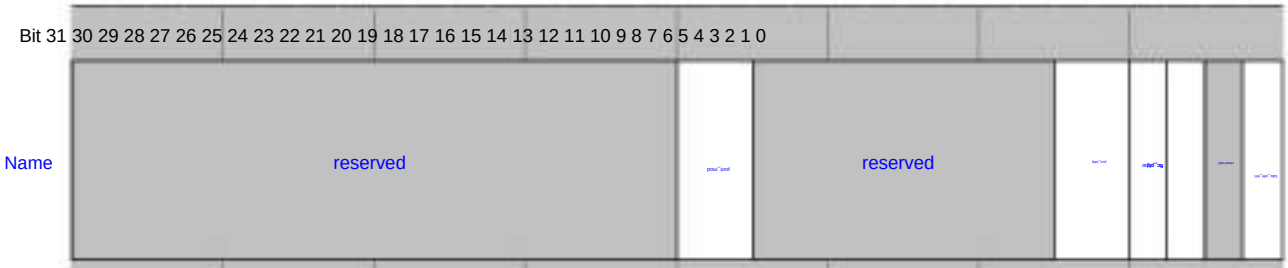
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
Name	reserved	[illegible]	[illegible]	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access Name		Description
[31:9] RO		reserved	Channel registers, 8 channels in total. Offset address: 0x1_0300ÿ0x1_0FFF is the address of channel 0; 0x1_2300ÿ0x1_2FFF is the address of channel 1; 0x1_4300ÿ0x1_4FFF is the address of channel 2; 0x1_6300ÿ0x1_6FFF is the address of channel 3; 0x1_8300ÿ0x1_8FFF is the address of channel 01 ÿ0x1_AFFF is the address of channel 5; 0x1_C300ÿ0x1_CFFF is the address of channel 6; 0x1_E300ÿ0x1_EFFF is the address of channel 7.
[8:7] RW	port_scan_mod		Port data input mode. bit[8]: Scan_mode[1]. 0: Composite mode of luma and chroma; 1: Separate mode of luma and chroma. bit[7]: Scan_mode[0]. 0: Interlaced input mode; 1: Progressive input mode.
[6:5] RW	port_mode		Port data receive mode. 00: BT.656/BT.1120 mode; Other: reserved.
[4:0] RO		reserved	reserve.

CH_INTF_CFG1

CH_INTF_CFG1 is interface timing register 1.

Offset Address	Register Name	Total Reset Value
0x10304	CH_INTF_CFG1	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:14]	RW	port_mod	port mode. 00: single-component input; 01: double-component input; 10: three-component input; 11: reserved.
[13:6]	RO	reserved	reserve.
[5:4]	RW	yuv_seq	YUV input order register. 00ÿUYVYÿ 01ÿVYUYÿ 10ÿYUYVÿ 11: YVYU. When it is two components, it means UV order. 00ÿVUVUÿ 01ÿUVUVÿ 10/11: Reserved.
[3]	RW	ftc_cfg	BT.656 timing reference code highest bit configuration. 0: fixed to 1; 1: Fixed to 0.
[2]	RW	ftc_polar	BT.656 timing reference code field indication bit (F) polarity. 0: 1st field: F=0, 2nd field: F=1 (standard); 1: 1st field: F=1, 2nd field: F=0 (non-standard).
[1]	RO	reserved	reserve.

[0] RW sav_ver_en			SAV(Start of Active Video)/EAV(End of Activevideo) data verification enable. 0: Disable verification; 1: Enable parity.

CH_FSTART_DLY

CH_FSTART_DLY is the frame synchronization delay register.

Offset Address	Register Name	Total Reset Value
0x10360	CH_FSTART_DLY	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	reserved	Frame synchronization delay register.

CH_CTRL

CH_CTRL is the channel control register.

Offset Address	Register Name	Total Reset Value
0x10400	CH_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	ch_en	Channel enable. 0: disable; 1: enable.

CH_REG_NEWER

CH_REG_NEWER is the acquisition control register.

Offset Address	Register Name	Total Reset Value
0x10404	CH_REG_NEWER	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	reg_newer	Channel update register, automatically cleared to 0 every frame.

CH_CROP_START

CH_CROP_START is the CROP start position register.

Offset Address	Register Name	Total Reset Value
0x10410	CH_CROP_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	y_start	reserved	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	y_start	The line number at which to start fetching the image.
[15:12]	RO	reserved	reserve.
[11:0]	RW	x_start	The pixel number at which to start fetching the image.

CH_CROP_SIZE

CH_CROP_SIZE is the CROP size setting register.

Offset Address	Register Name	Total Reset Value
0x10414	CH_CROP_SIZE	0x023F_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								crop_hgt												reserved				crop_wth							
Reset	0	0	0	0	0	0	1	0	0	0	1		1	1	1				1	0	0	0	0	0	0	1	1	1	0	1	1	

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	crop_hgt	Get the height of the image in rows.
[15:12]	RO	reserved	reserve.
[11:0]	RW	crop_wth	Gets the width (in pixels) of one line of the image.

CH_YDES_SIZE

CH_YDES_SIZE is the brightness storage size register.

Offset Address	Register Name	Total Reset Value
0x10418	CH_YDES_SIZE	0x023F_03BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								height												reserved				width							
Reset	0	0	0	0	0	0	1	0	0	0	1		1	1	1				1	0	0	0	0	0	0	1	1	1	0	1	1	

Bits	Access	Name	Description
[31:28]	RW	reserved	reserve.
[27:16]	RW	height	The output height of the Y component in rows.
[15:12]	RO	reserved	reserve.
[11:0]	RW	width	The output width of the Y component in pixels.

CH_CDES_SIZE

CH_CDES_SIZE is the chroma storage size register.

Offset Address	Register Name	Total Reset Value
0x1041C	CH_CDES_SIZE	0x023F_03BF

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	height	reserved	width
Reset	0 0 0 0	0 0 0 1 0 0 0 1	1 1 1 1	1 0 0 0 0 0 0 1 1 1 0 1 1

Bits	Access	Name	Description
[31:28]	RW	reserved	reserve.
[27:16]	RW	height	The output height of the C component in rows.
[15:12]	RO	reserved	reserve.
[11:0]	RW	width	The output width of the C component in pixels.

CH_YBASE_ADDR

CH_YBASE_ADDR is the brightness storage base address register.

Offset Address	Register Name	Total Reset Value
0x10420	CH_YBASE_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ybase_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ybase_addr	Original code stream luminance storage base address.

CH_CBASE_ADDR

CH_CBASE_ADDR is the chroma storage base address register.

Offset Address	Register Name	Total Reset Value
0x10424	CH_CBASE_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cbase_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	cbase_addr	Original stream chroma storage base address.

CH_YLINE_OFFSET

CH_YLINE_OFFSET is the luma line offset register.

Offset Address	Register Name	Total Reset Value
0x10428	CH_YLINE_OFFSET	0x0000_03C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	y_stride	The stride of image storage brightness, in byte.

CH_CLINE_OFFSET

CH_CLINE_OFFSET is the chroma line offset register.

Offset Address	Register Name	Total Reset Value
0x1042C	CH_CLINE_OFFSET	0x0000_03C0

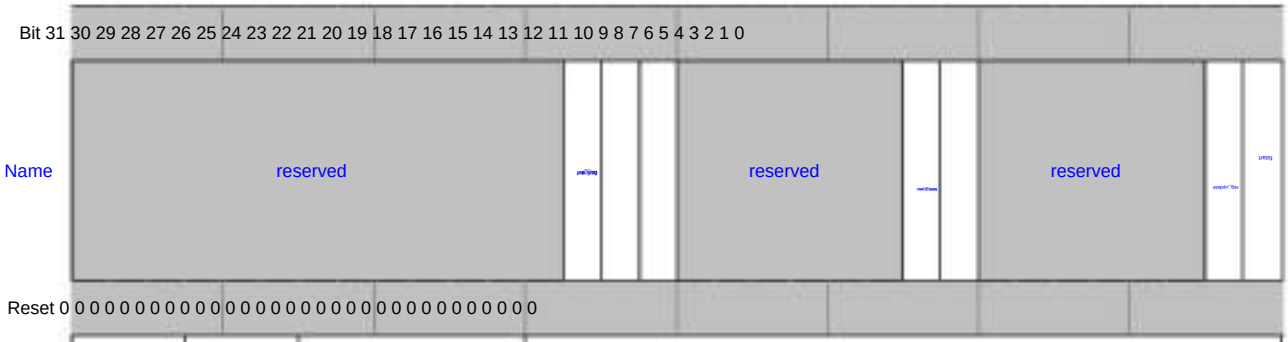
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	c_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	c_stride	The image stores the stride of chroma, in byte.

CH_INT_RAW

CH_INT_RAW is the channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10430	CH_INT_RAW	0x0000_0000



Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	WC	bus_err	Bus error interrupt status, write 1 to clear. 0: no original interrupt; 1: There is a raw interrupt.
[17]	WC	buf_ovf	Internal FIFO overflow error interrupt status, write 1 to clear. 0: no original interrupt; 1: There is a raw interrupt.
[16]	WC	cc_int	After obtaining the interrupt status, write 1 to clear it. 0: no original interrupt; 1: There is a raw interrupt.
[15:10]	RO	reserved	reserve.
[9]	WC	timing_err	Timing error interrupt status, write 1 to clear. 0: no original interrupt; 1: original interrupt.
[8]	WC	field_throw	Field/frame loss interrupt status, write 1 to clear. 0: no original interrupt; 1: There is a raw interrupt.
[7:2]	RO	reserved	reserve.
[1]	WC	reg_update	Register update interrupt status, write 1 to clear. 0: no original interrupt; 1: There is a raw interrupt.
[0]	WC	fstart	Frame/field start interrupt status, write 1 to clear. 0: no original interrupt; 1: There is a raw interrupt.

CH_INT

CH_INT is the channel interrupt register.

Offset Address	Register Name	Total Reset Value
0x10434	CH_INT	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved | reserved | reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RO	bus_err	Bus error interrupt status. 0: no original interrupt; 1: original interrupt.
[17]	RO	buf_ovf	Internal FIFO overflow error interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[16]	RO	cc_int	Get interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[15:10]	RO	reserved	reserve.
[9]	RO	timing_err	Timing error interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[8]	RO	field_throw	Field/frame loss interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[7:2]	RO	reserved	reserve.
[1]	RO	reg_update	Register update interrupt status. 0: no original interrupt; 1: original interrupt.
[0]	RO	fstart	Frame/field start interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

CH_INT_MASK

CH_INT_MASK is the channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10438	CH_INT_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RW	bus_err_en	Bus error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[17]	RW	buf_ovf_en	Internal FIFO overflow error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[16]	RW	cc_int_en	Get complete interrupt enable. 0: mask interrupt; 1: enable interrupt.
[15:10]	RO	reserved	reserve.
[9]	RW	timing_err_en	Timing error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[8]	RW	field_throw_en	Field/frame loss interrupt enable. 0: mask interrupt; 1: enable interrupt.
[7:2]	RO	reserved	reserve.
[1]	RW	reg_update_en	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

[0] RW fstart_en			Frame/field start interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

CH_STATUS

CH_STATUS is the channel status register.

Offset Address	Register Name	Total Reset Value
0x1043C	CH_STATUS	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved | reserved | reserved | reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RO	busy	working status. 0: idle; 1: Busy.
[18]	RO	bus_err	Bus error. 0: The bus is correct; 1: The bus is wrong.
[17]	RO	buf_ovf	Internal buffer overflow. 0: no overflow; 1: Overflow.
[16]	RO	image_done	Obtained. 0: Not accepted; 1: Accepted.
[15:10]	RO	reserved	reserve.
[9]	RO	timing_err	timing error status. 0: timing is correct; 1: Timing error.

[8]	RO	field_throw	Lost field/frame data. 0: not lost; 1: Lost.
[7:1] RO		reserved	reserve.
[0]	RO	field2	Parity field indication. 0: odd field; 1: even field.

CH_IPI_STATUS_SIZE

CH_IPI_STATUS_SIZE is the channel status register.

Offset Address	Register Name	Total Reset Value
0x10440	CH_IPI_STATUS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	height	image height.
[15:0]	RO	reserved	reserve.

CH_IPI_STATUS_SEAV

CH_IPI_STATUS_SEAV is the channel status register.

Offset Address	Register Name	Total Reset Value
0x10444	CH_IPI_STATUS_SEAV	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	SEAV	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RO	SEAV	The value of the SEAV code.
[7:0]	RO	reserved	reserve.

CH_DITHER_CFG

CH_DITHER_CFG is Dither configuration register

Offset Address	Register Name	Total Reset Value
0x10500	CH_DITHER_CFG	0xE000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md				reserved																											
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode selection. 000: 12bit input, 10bit output, no dither, directly truncate; 001: 12bit input, 10bit output, time domain dither; 010: 12bit input, 10bit output, airspace dither; 011: 12bit input, 8bit output, time domain and space domain dither. 100: 12bit input, 10bit output, rounded. 101: 12bit input, 8bit output, rounded. 111ÿDither bypassÿ
[28:0]	RO	reserved	reserve.

CH_DITHER_COEF0

CH_DITHER_COEF0 is Dither coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10504	CH_DITHER_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 used by time domain mode Dither.
[23:16]	RW	dither_coef2	Coefficient 2 used by dither in time domain mode.
[15:8]	RW	dither_coef1	Coefficient 1 used by dither in time domain mode.
[7:0]	RW	dither_coef0	Coefficient 0 used by dither in time domain mode.

CH_DITHER_COEF1

CH_DITHER_COEF1 is Dither coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10508	CH_DITHER_COEF1	0xDD66_4400

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dither_coef7	dither_coef6	dither_coef5	dither_coef4
Reset	1 1 0 1	1 0 1 0 1	1 0 0 1	1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 used by dither in time domain mode.
[23:16]	RW	dither_coef6	Coefficient 6 used by dither in time domain mode.
[15:8]	RW	dither_coef5	Coefficient 5 used by time domain mode dither.
[7:0]	RW	dither_coef4	Coefficient 4 used by dither in time domain mode.

CH_DITHER_SIZE

CH_DITHER_SIZE is the input image width register of Dither module.

Offset Address	Register Name	Total Reset Value
0x1050C	CH_DITHER_SIZE	0x0000_03BF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 0 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RW	reserved	reserve.
[11:0]	RW	width	Input image width for the dither module.

CH_MIR_CTRL

CH_MIR_CTRL is the mirror control register of the original code stream.

Offset Address	Register Name	Total Reset Value
0x10510	CH_MIR_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	flip_en	Vertical inversion enable. 0: disable; 1: enable.
[0]	RW	we_en	Horizontal inversion enable. 0: disable; 1: enable.

CH_MSC_CFG

CH_MSC_CFG is the block mask configuration register.

Offset Address	Register Name	Total Reset Value
0x10700	CH_MSC_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:4]		reserved	reserve.
[3]	RW	msc3_en	Mask block 3 is enabled. 0: Disable; 1: Enable.
[2]	RW	msc2_en	Mask block 2 is enabled. 0: disable; 1: enable.

[1]	RW	msc1_en	Mask block 1 is enabled. 0: disable; 1: enable.
[0]	RW	msc0_en	Shading block 0 is enabled. 0: Disable; 1: Enable.

CH_BLOCK0_START

CH_BLOCK0_START Mask start location register for block 0.

Offset Address	Register Name	Total Reset Value
0x10710	CH_BLOCK0_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start	reserved	x_start
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	y_start	Occlusion block 0 vertical starting point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	x_start	Occlusion Block 0 Horizontal starting point.

CH_BLOCK1_START

CH_BLOCK1_START Block 1 mask start position register.

Offset Address	Register Name	Total Reset Value
0x10714	CH_BLOCK1_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start	reserved	x_start
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	y_start	Block 1 vertical starting point.
[15:12]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x10714	CH_BLOCK1_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start / reserved / x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[11:0]	RW	x_start	Block 1 horizontal start point.

CH_BLOCK2_START

CH_BLOCK2_START Block 2 mask start position register.

Offset Address	Register Name	Total Reset Value
0x10718	CH_BLOCK2_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start / reserved / x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	y_start	Block 2 vertical starting point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	x_start	Block 2 horizontal start point.

CH_BLOCK3_START

CH_BLOCK3_START Block 3 mask start position register.

Offset Address	Register Name	Total Reset Value
0x1071C	CH_BLOCK3_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start / reserved / x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27:16] RW	y_start		Block 3 vertical starting point.
[15:12] RO		reserved	reserve.
[11:0] RW	x_start		Block 3 Horizontal starting point.

CH_BLOCK0_SIZE

CH_BLOCK0_SIZE is the block 0 mask size register.

Offset Address	Register Name	Total Reset Value
0x10750	CH_BLOCK0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	blk_height	reserved	blk_width
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	blk_height	Block 0 vertical height -1.
[15:12]	RO	reserved	reserve.
[11:0]	RW	blk_width	Occlusion Block 0 Horizontal Width -1.

CH_BLOCK1_SIZE

CH_BLOCK1_SIZE is the block 1 mask size register.

Offset Address	Register Name	Total Reset Value
0x10754	CH_BLOCK1_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	blk_height	reserved	blk_width
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	blk_height	Block 1 vertical height -1.
[15:12]	RO	reserved	reserve.
[11:0]	RW	blk_width	Occlusion Block 1 Horizontal Width -1.

CH_BLOCK2_SIZE

CH_BLOCK2_SIZE is the block 2 mask size register.

Offset Address	Register Name	Total Reset Value
0x10758	CH_BLOCK2_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	blk_height	Block 2 vertical height -1.
[15:12]	RO	reserved	reserve.
[11:0]	RW	blk_width	Block 2 horizontal width -1.

CH_BLOCK3_SIZE

CH_BLOCK3_SIZE is the block 3 mask size register.

Offset Address	Register Name	Total Reset Value
0x1075C	CH_BLOCK3_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	blk_height	Block 3 vertical height -1.
[15:12]	RO	reserved	reserve.
[11:0]	RW	blk_width	Block block 3 horizontal width -1.

CH_BLOCK0_COLOR

CH_BLOCK0_COLOR Block 0 mask color register.

Offset Address	Register Name	Total Reset Value
0x10790	CH_BLOCK0_COLOR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	blk_cr	blk_cb	blk_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	blk_cr	Occlusion block 0 fill color Cr component.
[15:8]	RW	blk_cb	Occlusion block 0 fill color Cb component.
[7:0]	RW	blk_y	Occlusion block 0 fill color Y component.

CH_BLOCK1_COLOR

CH_BLOCK1_COLOR is block 1 mask color register.

Offset Address	Register Name	Total Reset Value
0x10794	CH_BLOCK1_COLOR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	blk_cr	blk_cb	blk_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	blk_cr	Occlude block 1 fill color Cr component.
[15:8]	RW	blk_cb	Occlusion block 1 fill color Cb component.
[7:0]	RW	blk_y	Occlusion block 1 fill color Y component.

CH_BLOCK2_COLOR

CH_BLOCK2_COLOR is the block 2 mask color register.

Offset Address	Register Name	Total Reset Value
0x10798	CH_BLOCK2_COLOR	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	blk_cr	blk_cb	blk_y
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	blk_cr	Occlude block 2 fill color Cr component.
[15:8]	RW	blk_cb	Occlusion block 2 fill color Cb component.
[7:0]	RW	blk_y	Occlusion Block 2 Fill color Y component.

CH_BLOCK3_COLOR

CH_BLOCK3_COLOR is the block 3 mask color register.

Offset Address	Register Name	Total Reset Value
0x1079C	CH_BLOCK3_COLOR	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	blk_cr	blk_cb	blk_y
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	blk_cr	Occlusion block 3 fill color Cr component.
[15:8]	RW	blk_cb	Occlusion block 3 fill color Cb component.
[7:0]	RW	blk_y	Occlusion block 3 Fill color Y component.

CH_VCDS_CFG

CH_VCDS_CFG is the chroma vertical downsampling configuration register for the main stream.

Offset Address	Register Name	Total Reset Value
0x10800	CH_VCDS_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	cds_en	Downsampling enabled. 0: Downsampling is off; 1: Downsampling enabled.

CH_VCDS_COEF

CH_VCDS_COEF is the chrominance vertical downsampling coefficient register of the main stream.

Offset Address	Register Name	Total Reset Value
0x10808	CH_VCDS_COEF	0x0000_001F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef1	reserved	coef0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:16]	RW	coef1	Downsampling factor 1.
[15:5]	RO	reserved	reserve.
[4:0]	RW	coef0	The downsampling factor is 0.

CH_LHFIR_SPH

CH_LHFIR_SPH is the brightness horizontal scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x10940	CH_LHFIR_SPH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	hlmsc_en	Horizontal brightness scaling enabled. 0: forbidden; 1: enable.
[30:0]	RO	reserved	reserve.

CH_CHFIR_SPH

CH_CHFIR_SPH is the chroma horizontal scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x10944	CH_CHFIR_SPH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	hchmsc_en	Horizontal chroma scaling enabled. 0: forbidden; 1: enable.
[30:0]	RO	reserved	reserve.

CH_LHFIR_OFFSET

CH_LHFIR_OFFSET is the brightness scaling horizontal position offset register.

Offset Address	Register Name	Total Reset Value
0x10948	CH_LHFIR_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Name	reserved	hluma_offset	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:12]	RW	hluma_offset	Horizontal brightness start position offset. (s,5) format, that is, 1bit sign bit, 4bit integer bit, complement code representation, range -6ÿ 15ÿ
[11:0]	RO	reserved	reserve.

CH_CHFIR_OFFSET

CH_CHFIR_OFFSET is the chroma scaling horizontal position offset register.

Offset Address	Register Name	Total Reset Value
0x1094C	CH_CHFIR_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Name	reserved	hchroma_offset	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:12]	RW	hchroma_offset	The horizontal chroma starting position offset. (s,5) format, that is, 1bit sign bit, 4bit integer bit, complement code representation, range -6ÿ 15ÿ
[11:0]	RO	reserved	reserve.

CH_Y_CLIP_CFG

CH_Y_CLIP_CFG is the brightness CLIP configuration register.

Offset Address	Register Name	Total Reset Value
0x10B00	CH_Y_CLIP_CFG	0x00FF_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	max	reserved	min
Reset	0 0 0 0 0 0 0 1	1 1 1	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	max	The maximum value of the output.
[15:8]	RO	reserved	reserve.
[7:0]	RW	min	The minimum value of the output.

CH_C_CLIP_CFG

CH_C_CLIP_CFG is the chroma CLIP configuration register.

Offset Address	Register Name	Total Reset Value
0x10B04	CH_C_CLIP_CFG	0x00FF_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	max	reserved	min
Reset	0 0 0 0 0 0 0 1	1 1 1	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	max	The maximum value of the output.
[15:8]	RO	reserved	reserve.
[7:0]	RW	min	The minimum value of the output.

CH_SUM_Y

CH_SUM_Y is the brightness and statistics register of the input image.

Offset Address	Register Name	Total Reset Value
0x10C00	CH_SUM_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum_y																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	sum_y	Brightness and statistics.

11.2 VDP

11.2.1 Overview

The VDP (Video Display) module actively reads video and graphics data from the corresponding location in the memory, superimposes the video layer and graphics layer data and sends them out through the display channel.

11.2.2 Functional Description

The overall block diagram of VDP is shown in Figure 11-15 .

Figure 11-15 Overall block diagram of VDP

Surface: Data path for bus input. Its functions include bus data reading and data processing of a single layer. Surface includes: video layer (VHD0, VSD0, VSD1), graphics layer (G0, G2, G3) and mouse layer HC0.

Display Channel: display channel. Including high-definition display channel (DHD0), standard definition display channel (DSD0 and DSD1).

CBM (CrossBar and Mixer, strobe overlay): Video layer/graphics layer overlay.

PARA (Parameter, parameter): handles the update and loading of the ZME (Zoom Engine) coefficients of the video channel.

MAC (Memory Access Controller, memory access controller): The bus application arbitration module of each Surface. Each module reads data from the memory through the AXI (Advanced eXtensible Interface) bus, and the module arbitrates the application made by each Surface.

CAS (Control And Status): This module mainly configures the registers through the APB (Advanced Peripheral Bus, Advanced Peripheral Bus) bus, and the status information of each module is reported to the CPU through this module.

VDP registers are mainly allocated according to module global, Surface and Display Channel:

Module global registers

include bus-related configuration, interrupt, and version registers.

Surface registers

Including video layer, graphics layer configuration registers.

Display Channel registers include DHD,

DSD configuration registers. In-chip coefficient Video

layer ZME

coefficient. Because the data volume of the coefficient is large, it is read through the AXI Master and does not occupy the CPU.

The characteristics of VDP are as follows:

Digital output interface

ÿ HD supports VGA (Video Graphics Array, video graphics array) output, HDMI 1.4a (High Definition Multimedia Interface, high-definition multimedia interface) output

ÿ HDMI and VGA simultaneously display the same channel data analog

output interface ÿ

Standard definition channels DSD0 and DSD1 support CVBS (Composite Video Broadcast Signal, composite TV broadcast signal) output

Video layer (Video Surface) ÿSupport

input pixel format: Semi-Planar YCbCr4:2:2, Semi-Planar YCbCr4:2:0 ÿSupport global alpha value ÿSupport color space conversion

of video layer, support brightness,

contrast, hue, Saturation adjustment ÿ supports vertical chroma upsampling ÿ supports horizontal chroma upsampling

ÿSupport multi-area reading and writing (VHD0 is 16 areas)

ÿSupports up to 8x magnification

Graphics Surface ÿSupports 3 graphics

layers: graphics layer 0, 2, 3 ÿSupports 1 mouse layer: HC0

ÿSupports data formats: ARGB8888,

ARGB1555 ÿSupports global alpha and pixel alpha ÿSupports 3 types of data

extensions Mode: Complement the lower bit with 0, add

the highest bit in the lower bit, add some high

bits in the lower

bit ÿSupport width and

height are even numbers

ÿ G0 minimum input/output resolution is 32x32, maximum input/output resolution is 1920×1080

ÿ The minimum input/output resolution of G2/G3 is 32x32, and the maximum input/output resolution is 720×576

Overlay feature

ÿSupport background layer, 2 video layers, 1 graphics layer, 1 mouse layer with 256 levels of alpha blending, the priority of graphics layer and video layer can be configured (the alpha of the layer with higher priority is used when overlaying).

ÿThe size and position of each overlay layer can be adjusted arbitrarily.

ÿSupport the brightness, contrast, hue, and saturation adjustment of the superimposed image.

VDP includes 1 HD channel, 2 SD channels, each channel has an independent vertical timing interrupt, which marks the end of the frame/field, and 3 low bandwidth interrupts, a write-back complete interrupt and a write-back stop interrupt.

11.2.3 Working method

11.2.3.1 Clock configuration

There are three clock sources for VDP:

VPLL0

VPLL2

AXI bus bus clock

The following clock selections are register configurable:

HDMI interface clock comes from DHD0.

Interface clock corresponding to DAC data port DACR, DACG, DACB. The interface clock comes from DHD0.

Table 11-6 to Table 11-7 show the relationship between the channel interface type and PLL configuration, and the usage method is as follows:

1. Determine the channel.
2. Find the interface type from the table corresponding to the channel.
3. The selection of PLL and the configuration of DATE (Digital part of Analog TV Encoder)/DAC (Digital Analog Converter) can be determined from the row information where the interface type is located.

--Finish

Table 11-6 Clock configuration relationship of DHD0 display channel (interface clock/data comes from DHD0 or DSD0/DSD1)

	DHD0 ÿMHzÿ	DSD0/DSD1 ÿMHzÿ	PLL0/2 ÿMHzÿ	HDATE ÿMHzÿ	DACÿ DAC5 ÿMHzÿ
HDMI 148.5		THAT	PLL0ÿ297ÿ NA		THAT
	74.25	THAT	PLL0 ÿ148.5ÿ	THAT	THAT
VGA 148.5		THAT	PLL0 ÿ148.5ÿ	THAT	148.5
BT656NA		27	PLL2 (27) NA		THAT

Table 11-7 DSD0~DSD1 display channel clock configuration relationship

	DSD0ÿDSD1 PLL0/2	ÿMHzÿ	SDATE ÿMHzÿ	DAC0 ÿMHzÿ
CVBS	27	PLL2ÿ27ÿ	54	54
BT656	27	PLL2ÿ27ÿ	THAT	THAT

11.2.3.2 Reset

VDP reset includes hardware reset and software reset.

VDP has 3 soft resets (write 1 to the corresponding clock reset control bit to reset, write 0 to cancel the reset):

2 standard definition channels SD channel share a soft reset

HD channel HD0 soft reset

AXI bus soft reset

注意

Before doing an AXI bus reset:

Turn all layers off. After

the next frame/field is interrupted (reaching the update point), configure the bus reset request.

11.2.3.3 Bus related configuration

AXI Master

VDP includes a Master interface to improve bus access efficiency:

VDP supports AXI Master, and the data read and write requests of VHD0, VSD0/1, G0/2, HC0, and WBC2 layers can be operated on the bus through MASTER.

APB register configuration

The VDP register is read and written through the APB interface, and the clock of the APB is 165MHz. In Hi3520D, the base address of VDP is 0x205C_0000, the register addressing space is 64KB, and the corresponding address offset range is: 0x0000ÿ0xFFFFÿ

Outstanding configuration

The Outstanding depth of AXI Master can be configured as 0, 1, 2, 3, 4, 5, 6, 7. Among them, when outstanding is 0, AXI Master does not perform any operations on the bus.

11.2.3.4 Analog output interface

The VDP includes the following analog output connectors:

SD channel supports up to 2 CVBS output interfaces

ÿ DSD0->CVBS_0

ÿ DSD1->CVBS_1

ÿ CVBS supports two formats: PAL and NTSC

11.2.3.5 Digital output interface

VDP supports the following digital interface outputs:

HDMI interface

VGA interface

HDMI interface

HDMI is an HDMI interface that supports the 1.4a protocol standard (its source can come from DHD0):

Maximum output resolution: 1920x1200 or 1920x1080

The clock frequency is 74.25MHzÿ165MHz

Support progressive

interlaced display data format is YCbCr444

VGA interface

Support VGA interface (its source can come from DHD0):

Output resolution range: 720P50ÿ1920 x 1200

The clock frequency is 40MHzÿ165MHz

Support progressive

display and realize RGB888 output through configuration interface CSC (Color Space Conversion, color space conversion)

11.2.3.6 HD video layer function

Multi-region read function

VDP has the function of multi-area reading, which can display the pictures of multiple areas at the same time, and the data of each area picture can be from different sources:

The VHD0 video layer supports multi-region specifications.

VHD0 can support up to 16 regions. The size of

each area can be configured, the minimum is 32×32, and the maximum is the maximum resolution of the layer (VHD0: 1920x1200).

Each zone can be enabled individually.

The display position of the area can be configured to be displayed at any position on the screen (configured through the start and end coordinates of the area). The content of each area can come from the same video source or from different video sources.

The starting address of the area source can be assigned (sub-brightness, chrominance address), and the address is 2byte aligned. The area source stride can be allocated (separate luma and chroma addresses), and it is 16byte aligned.

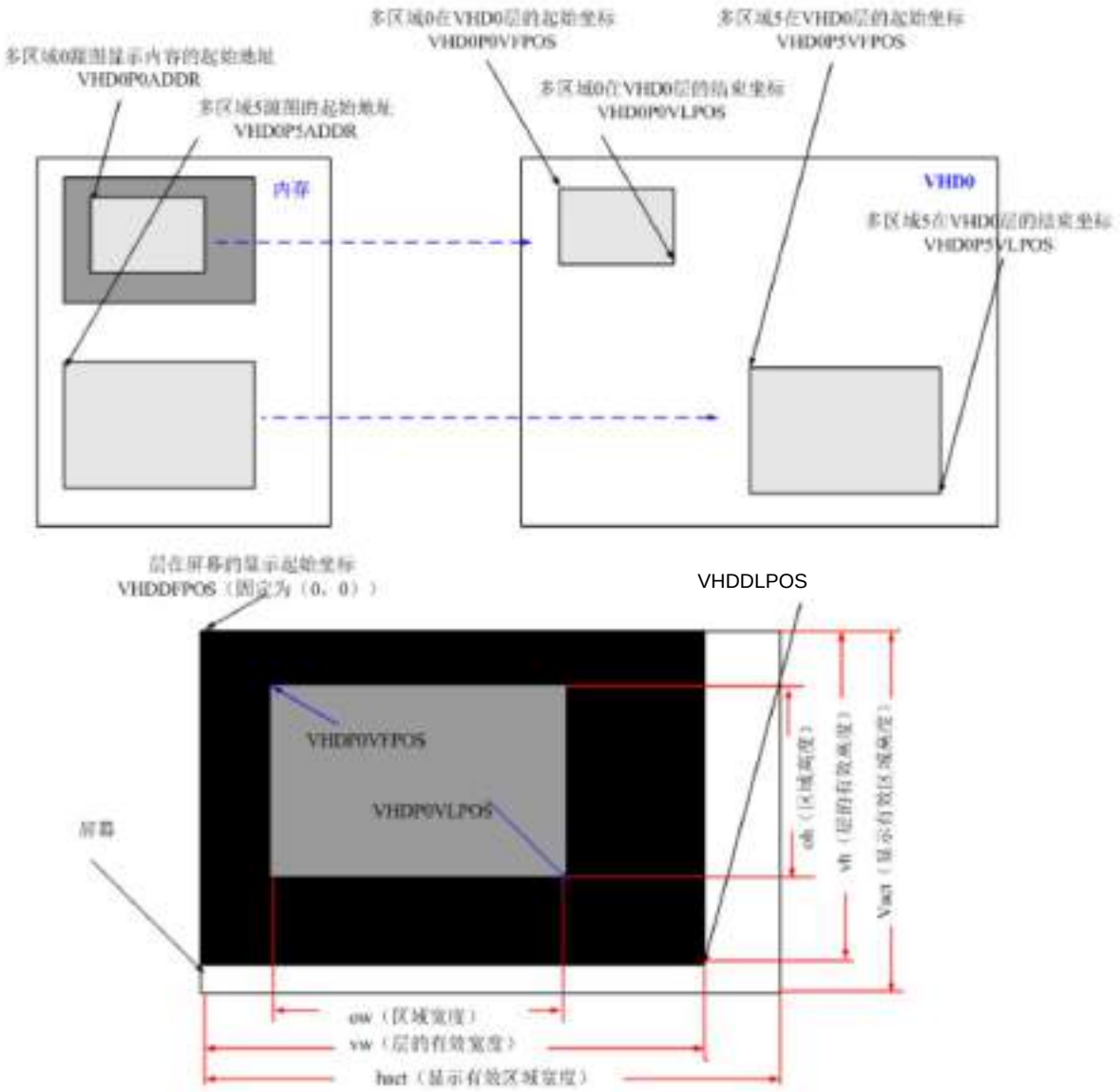
Support progressive mode, interlaced mode.

Show location description

VDP supports video display position can be configured:

There are 3 sets of coordinates in the video layer, which need to read the source start coordinates of the data (the software calculates the start address and configures it to the hardware). The start and end coordinates of the display area relative to the video layer. The start and end coordinates of the video layer displayed on the screen. The combination of the 3 coordinates can display the video source at any position on the screen.

Figure 11-16 Schematic diagram of 3 sets of coordinates



注意

The starting coordinate of the layer on the screen must be set to (0,0).

Zoom function description

VDP has a high-quality scaling engine that supports different magnifications:

- VHD0 supports scaling
- VHD0 only supports zooming in, not zooming out
- Supports video formats semi-plannar420, semi-plannar422

The minimum input resolution of VHD0 is 32×32, and the maximum input resolution is 1920x1200

The minimum output resolution of VHD0 is 32×32, and the maximum output resolution is 1920x1200. It supports

copy mode and filter mode, supports 8-level

horizontal brightness and 4-level horizontal chroma filtering, each with 32 groups of filter coefficients, and the filter coefficient can be

configured to support 6-level vertical brightness. , vertical chroma 4-stage filtering, each with 32 groups of filter coefficients, filter

coefficients can be configured scaling coefficient adopts the strategy of AXI

automatic loading from DDR, supports vertical luminance chroma, horizontal luminance

chroma separate configuration enabling performance: output pixel 1pixel/ 1clk

Notice

Use a scaling strategy where vertical scaling precedes horizontal scaling.

VHD0 does not support scaling up to 1920 for resolutions with a width greater than 1280 and less than 1920.

420-422 (vertical chroma upsampling)

When the input image data is 420, it is necessary to enlarge the chromaticity by 2 times in the vertical direction and convert the data format to 422ÿ

According to different image quality requirements, VHD and VSD have different conversion formats:

VHD conversion data format method: ÿ 4th

order filtering

ÿ copy

Both modes are configurable.

VSD conversion data format method: Copy

IFIR: Horizontal Chroma Upsampling

The main function of the horizontal chroma upsampling is to upsample the chroma in the horizontal direction and convert the 422 data format to 444.

There are 3 ways to achieve chroma level upsampling, which can be configured:

Copy

bilinear interpolation

8th order filter

CSC: Color Space Conversion

Can realize the conversion of YUV709, YUV601 color space can realize the

conversion of RGB, YUV color space

11.2.3.7 SD Video Layer Functions

VDP has multiple SD video layers:

The standard definition video layer includes: VSD0, VSD1, which can only support 1 area

Supported input pixel formats: semi-plannar420, semi-plannar422 The minimum input resolution is 32x32, and the maximum input resolution is 720x576 The minimum output resolution is 32x32, and the maximum output resolution is 720x576

The horizontal resolution of the input is a multiple of 2, and the vertical resolution is a multiple of 4

Support progressive mode, interlaced mode

source start address can be assigned (sub-luminance, chroma address), the address is 2byte alignment

source stride can be assigned (sub-luminance, chroma address), 16byte alignment supports

horizontal chroma upsampling IFIR, Copy mode, bilinear difference, and 6th-order filter mode are optional.

Support YCbCr->RGB color space conversion, support contrast/hue/saturation adjustment

Support configurable display position: display at any position on the screen

Support frame/field update mode

Support global alpha configurable, the configuration range is 0 to 255

11.2.3.8 Graphics Layer Functions

Graphics layers include: G0, G2, G3

decompression function

VDP G0 supports image decompression in lossless compression formats, other graphics layers do not support:

Supported input pixel formats: ARGB1555, ARGB8888 Support progressive compression, interlaced compression mode Support frame/field update mode

G0 minimum input/output resolution 32x32, maximum input/output resolution 2560x1600

G2/G3 minimum input/output resolution 32x32, maximum input/output resolution 720x576 graphics layer vertical resolution multiple of 2

Support configurable display position: display 4 components at any position on the screen to be decompressed separately, the address of the 4 components can be configured (16byte alignment), share a bankwidth (16byte alignment), and share a stride (16byte alignment) Decompression performance: 1pixel /1clk When the format is ARGB1555, the pixel alpha value is not compressed.

Decompression DCMP configuration method: DCMP supports progressive decompression and interlaced decompression, and the storage of compressed data is similar to that of progressive and interlaced source data. The configuration of compressed information mainly includes the first address address, bankwidth information, and stride information. Among them, the 4 components are compressed separately, so there are four first addresses of alpha, R, G, and B components. Secondly, bakwidht is similar to the concept of semi-plannar storage method line, the difference is that a bankwidh may store the compressed data of several component lines; finally, stride is completely consistent with the stride concept of semi-plannar, and is used to determine the compressed data of each row The initial address of .

Figure 11-17 row by row decompression storage method

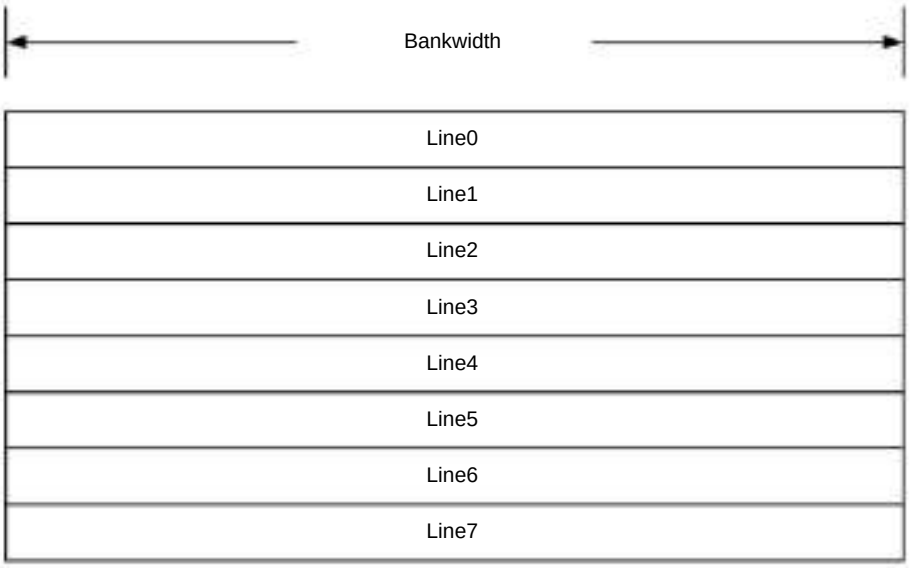
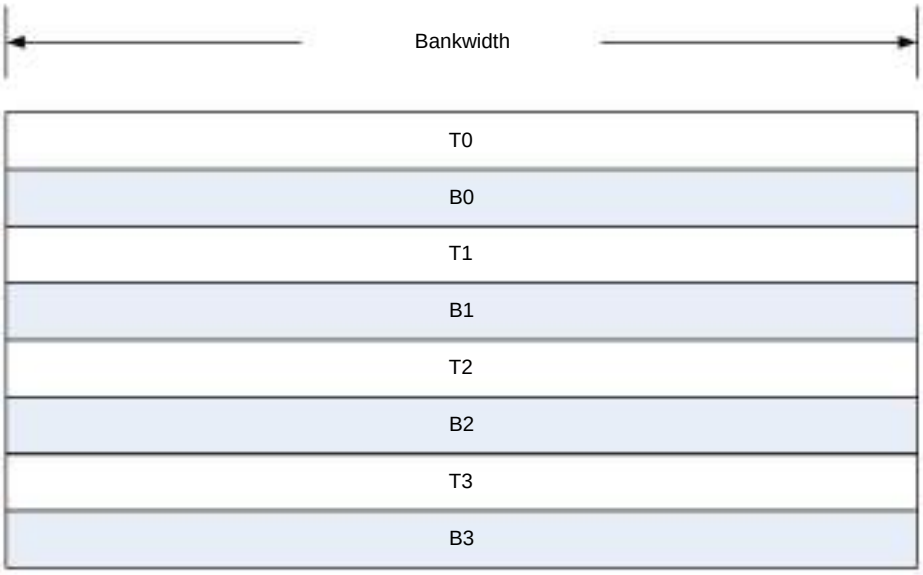


Figure 11-18 Interlaced decompression storage method



The following is the configuration of the decompression mode in different scenarios:

The configuration methods of line-by-line decompression, frame update, and frame

interruption: ÿConfigure the graphics layer as compression

mode. ÿConfigure the base address of 4 components. ÿ

Configure bankwidth and stride information, where the compressed stride is equal to the decompressed stride, ie

stride_dcmp = stride_vcmp. ÿ Configure the graphics layer to

frame update mode. ÿ Configure the interrupt generation mode as

frame interrupt.

Interlaced decompression, frame update, frame interrupt configuration:

ÿ Same configuration as progressive

decompression. ÿ Configure bankwidth and stride information, where stride_dcmp = stride_vcmp/2. ÿ Same configuration as

progressive decompression. ÿ Enable

interlaced decompression. Configuration

methods for interlaced decompression, field update, and field interruption:

ÿ Same configuration as progressive

decompression. ÿ Configure bankwidth and stride information, where stride_dcmp = stride_vcmp/2. ÿ Configure the graphics layer

to field update mode. ÿ Configure the interrupt generation

method as field interrupt, and configure the 4-component storage location of the top field/bottom field in the interrupt service program

site.

CSC Functional Description

Support color space conversion, including: mutual conversion between RGB, YCbCr601, YCbCr709, xvYCC601, xvYCC709.

alpha processing

The alpha value of the graphics layer can come from two sources:

Pixel alpha value: Indicates the overlay property of a certain pixel. Global alpha

value: Indicates the overlay property of a certain layer.

There is a special case of pixel alpha value. In RGB1555 format, the alpha value is only 1 bit. This bit is not the real alpha value, but only the index of alpha. The real alpha value is obtained by selecting the value in the alpha register according to the index value. When the index value is 0, the value is alpha0, otherwise, the value is alpha1.

HC Functional Description

VDP has two hardware mouse layers:

Supported input pixel formats: ARGB1555, ARGB8888 Minimum input resolution 32x32,

maximum input resolution 128x128 Minimum output resolution 32x32, maximum output resolution

128x128 Input vertical resolution in multiples of 2 Support progressive mode, interlaced mode

support frame Update, field update source start

address can be configured, the address is 128bit

(16byte) aligned Source stride can be

configured, 128bit (16byte) aligned Support color space conversion, including: RGB2YUV

709, RGB2YUV 601 Support display position can be configured: on the

screen Any position display supports global alpha configurable, the configuration range is 0~255

Pixel alpha can be enabled and configured, for graphics with pixel alpha value in the pixel format ARGB1555, select ALPHA0 or ALPHA1

11.2.3.9 Layer overlay processing

VDP supports multi-layer overlay function, there are 3 overlays in total, and the corresponding relationship is:

MIX1 —> DHD0

MIX3 —> DSD0

MIX4 —> DSD1

Functional description of MIXER:

Video/graphics layer fixedly bound to MIXER1: VHD0, G0 Video/graphics layer fixedly bound to MIXER3: G2 Video/graphics layer fixedly bound to MIXER4: VSD1, G3

Video/graphics layer optionally bound to MIXER1/3/4: HC0 Video layer optionally bound to MIXER1/3: VSD0 (PIP)

The background color of MIXER1/3/4 can be configured separately

The specific configuration method is as follows:

1. Turn off the corresponding video output interface.
2. Configure sur_attrix to determine the connection relationship of each surface.
3. Configure the relevant registers of each surface.
4. Configure the priority of each surface.
5. Open the corresponding video output interface.

--Finish

Notice

If HC0, VSD0 (PIP) are bound to MIXER1, they can no longer be bound to MIXER3/MIXER4.

HC0 can only be bound to one of MIXER1, MIXER3 or MIXER4.

HC0, VSD0 (PIP) can drive different MIXER, but if switching from driving the current MIXER to driving another MIXER, it cannot be changed in real time. The corresponding video output interface must be closed first, and then change the MIXER driven by the surface.

11.2.3.10 HD channel processing function

timing configuration

The output interface of VDP supports the configuration of various typical and atypical timings to adapt to different docking chip interfaces:

The maximum resolution of DHD0 interface is 1920x1200

Interface level timing parameters can be configured:

ÿHorizontal front shoulder HFB: 16bit=(1-65536), unit: clock ÿHorizontal back shoulder HBB: 16bit=(1-65536), unit: clock ÿHorizontal active HACT: 16bit=(1-65536), unit: clock ÿHorizontal pulse width HPW: 16bit=(1-65536), unit: clock

Interface vertical timing parameters can be configured:

ÿVertical front shoulder VFB: 8bit=(1-256), unit: line ÿVertical back shoulder VBB:8bit=(5-256), unit: line ÿVertical effective VACT:12bit=(1-256), unit: line ÿVertical pulse width VPW:16bit=(1-65536), unit: row

Interlace timing parameters can be configured: ÿBottom field vertical front shoulder BVFB:8bit=(1-256), unit: line ÿBottom field vertical back shoulder BVBB:8bit=(5-256), unit: line ÿBottom field vertical effective BVACT: 12bit=(1-256), unit: line ÿBottom field vertical pulse width BVPW: 16bit=(1-65536), unit: line ÿbottom field half-line configuration HMID: 16bit=(1-65536), unit: clock cycle, relative to Clock period of the first pixel in the active area

Notice

Number of clocks in one row = HFB + HBB + HACT x (n clk/pixel), HPW is smaller than HBB. The number of lines in one frame = VFB + VBB + VACT, VPW is smaller than VBB, BVPW is smaller than BVBB. When all timing parameters are configured, the interface should be closed, and the interface should be opened after the configuration is completed.

DFIR function

DFIR can be configured, and the filtering method is 1, 2, 1, and the performance can reach 1pixel/lclk.

CLIP function

VDP has a flexible and configurable CLIP function:

The protocol of the interface timing requires that the output data must be limited within a certain range. If it exceeds this range, the data needs to be clipped. The clip enable is configurable, the low and high thresholds of the clip are configurable, and the performance can reach 1pixel/lclk.

Each HDMI and VGA interface has a set of independent clip logic.

H_SHARPEN function

The VGA interface of the VDP has a configurable Horizonal Sharpen function:

Horizonal Sharpen is used to enhance the sharpening effect in the horizontal direction on the VGA channel.

The enablement of Horizontal Sharpen is configurable.

11.2.3.11 SD channel processing function

VDP has 2 SD channels:

Standard definition channels include DSD0, DSD1

interface maximum resolution support 720x576

DSD0, DSD1 support CVBS interface Support chroma

downsampling DFIR, DFIR enable can be configured to support CLIP

function, CLIP enable can be configured to configure the low

value threshold and high value threshold of clip

11.2.3.12 WBC2 Channel Write Back Function

When WBC2 is written back as the output of DHD0 channel, the data is scaled and written back to DDR, which is used as the SD input source for HD/SD homologous display.

Write back by/interlaced

VDP's WBC write-back supports progressive/interlaced configurable:

WBC2 write-back enable is configurable.

Input data format: YUV422. The data source of WBC2 can be configured, and the output from MIX2 or VHD0 of CBM can be selected. On input to WBC2, downsampled to the sampling format of YUV422. Output data format: semi-plannar422, semi-plannar420. Support line-by-line write-back and

interlaced write-back. WBC2 progressive write back, interlaced write back is determined by DHD0

channel, when DHD0 is interlaced display, WBC2 interlaced write back, when DHD0 is progressive display, WBC2 progressive write back. Input resolution range: 32x32ÿ1920x1080. The input resolution of WBC2 is determined by the effective width and height of DHD0. When DHD0 is displayed

progressively, the input height is the height of one frame; when DHD0 is displayed interlaced, the input height is the height of one field.

The output resolution can be configured, ranging from 32x32 to 720x576.

WBC2 scaling

VDP's WBC write-back supports high-quality, downscaling with a configurable factor:

WBC2 only supports zooming out, not zooming in

WBC2 scaling minimum input resolution 32x32, maximum input resolution 1920x1920

The minimum output resolution of WBC2 scaling is 32x32, and the maximum output resolution is 720x576. Copy mode and

filter mode are supported

Support horizontal luminance 8-level, horizontal chroma 4-level filtering, each with 32 sets of filter coefficients, and filter coefficients can be configured

The scaling factor adopts the strategy of AXI automatically loading from DDR

Support vertical luminance and chromaticity, horizontal luminance and chromaticity separate

configuration Enabled performance: output pixel 1pixel/1clk

Notice

A scaling strategy in which horizontal scaling precedes vertical scaling is employed.

The zoom factor is up to 16 times, the zoomed luma line buffer size is 720, and the chroma line buffer size is 720. When the output is SPYCbCr420, the maximum reduction factor is 8 times.

11.2.3.13 Interrupts

VDP supports a total of 8 interrupts, divided into 4 categories:

Vertical Timing Interrupt

Low Bandwidth Interrupt

WBC2 Write back complete interrupt

WBC2 Write Back Stop Interrupt

vertical timing interrupt

Each channel of VDP has an independent vertical timing interrupt, and the location of interrupt generation can be flexibly configured:

VDP includes 1 HD channel and 2 SD channels, each channel has an independent vertical timing interrupt, marking the end of the frame/field. There are 3 vertical timing interrupts in VDP. Interrupt generation methods are optional: frame interrupt, field interrupt.

For progressive display, the vertical timing interrupt can only be configured as frame interrupt mode.

For interlaced display, the vertical timing interrupt can be configured as frame interrupt mode or field interrupt mode (it is recommended that HD generate interrupts according to fields, and SD generate interrupts according to frames). Support

interrupt mask can be configured.

Supports configurable vertical timing interrupt threshold.

Each interrupt source can be turned on and off independently, write 1 to clear 0.

low bandwidth interrupt

VDP supports the reporting of low bandwidth status in interrupt mode:

VDP includes 1 HD channel and 2 SD channels, each channel has an independent low-bandwidth interrupt, which marks the low-bandwidth information of the frame/field. VDP has a total of 3 low-bandwidth interrupts. Interrupt generation methods are

optional: frame interrupt, field interrupt.

For progressive display, the vertical timing interrupt can only be configured as frame interrupt mode.

For interlaced display, the vertical timing interrupt can be configured as frame interrupt mode or field interrupt mode (it is recommended that HD generate interrupts according to fields, and SD generate interrupts according to frames).

Support interrupt mask can be configured.

Each interrupt source can be turned on and off independently, write 1 to clear 0.

WBC2 write back complete interrupt

VDP supports reporting the completion status of WBC writing back in interrupt mode:

VDP contains 1 WBC2 write-back channel, so there is 1 WBC write-back interrupt in total, which marks the completion of write-back of frame/field data.

The WBC2 interrupt generation method is determined by the DHD0 interrupt generation method:

ÿ DHD0 is frame interrupt, and WBC2 interrupt mode is frame interrupt.

ÿ DHD0 is a field interrupt, and WBC2's interrupt mode is a field interrupt. Support interrupt mask can be configured. Interrupt sources can be turned on and off independently, write 1 to clear 0.

WBC2 Write Back Stop Interrupt

VDP supports reporting WBC write-back stop status in interrupt mode:

VDP contains 1 WBC2 write-back channel, so there is 1 WBC write-back stop interrupt in total, which marks the write-back stop of frame/field data.

The generation mode of WBC2 interrupt is determined by the interrupt generation mode of DHD0: ÿ If DHD0 is frame interrupt, then the interrupt mode of WBC2 is frame interrupt.

ÿ DHD0 is a field interrupt, and WBC2's interrupt mode is a field interrupt.

Support interrupt mask can be configured. Interrupt sources can be turned on and off independently, write 1 to clear 0.

11.2.3.14 Low Power Control

VDP supports configurable clock gating:

The dynamic clock gating of Mem is implemented through the clock gating signal ck_gate_en: ÿ 0: The clock is normally input to mem. ÿ 1: The clock of mem is forced to be 0. Before enabling dynamic clock gating, all VDP services must be stopped (all layers, channels disabled).

11.2.4 Register overview

Table 10-8 lists the value ranges and meanings of the variables in the register offset address .

Table 11-8 Register offset address variable table

variable name	Ranges	describe
i	0 and 1	SD video layer 0~1
m	0ÿ15	HD video layer region number
	0	SD video layer region number

An overview of the registers is shown in Table 10-9 .

Table 11-9 Register overview (base address is 0x205C_0000)

offset address	name	describe	page number
0x0000	VHDNCTRL	VHD Control Register	10-78
0x0004	VHDNUPD	VHD channel update enable register	10-78
0x0010	VHDNCADDR Current frame address register		10-79
0x0014	VHDNCCADDR The chroma address register of the current frame		10-79
0x0024	VHDNSTRIDE	The stride register of the surface	10-80
0x0028	VHDNIRESO Input Resolution Register		10-80
0x0034	VHDNCBMPARA overlay related parameter register		10-81
0x0060	VHDNDFPOS	Surface at the starting position of the display window (First POSition) register	10-81
0x0064	VHDNDLPOS	Surface at the end of the display window (Last POSition) register	10-82
0x0070	VHDBK	The background color register of the video layer	10-82
0x0080	VHDNCSCIDC color space conversion input DC component register 10-83		
0x0084	VHDNCSCODC color space conversion output DC component register 10-83		
0x0088	VHDNCSCP0 Color Space Conversion Parameter 0 Register		10-84
0x008C	VHDNCSCP1 Color Space Conversion Parameter 1 Register		10-84
0x0090	VHDNCSCP2 Color Space Conversion Parameter 2 Register		10-85
0x0094	VHDNCSCP3 Color Space Conversion Parameter 3 Register		10-86

offset address	name	describe	page number
0x0098	VHDNCSCP4 Color Space Conversion Parameter 4 Register		10-86
0x00C0	VHDNHSP	Horizontal scaling parameter configuration (horizontal Scaling Parameter) register	10-86
0x00C4	VHDNHLOFFSET Brightness horizontal position offset register		10-88
0x00C8	VHDNHCOFFSET Chroma horizontal position offset register		10-88
0x00CC	VHDNVSP	Vertical Scaling Parameter Register	10-88
0x00D0	VHDNVSR	Vertical scaling factor (Luma Vertical Scaling Ratio) register	10-90
0x00D4	VHDNVOFFSET Vertical Luma Offset Register		10-90
0x00D8	VHDNZMEORESO Scale unit output resolution register		10-91
0x00DC	VHDNZMEIRESO Scaling unit input and output resolution register		10-91
0x0180	VHDNIFIRCOEF01 VHD IFIR filter coefficient 0, 1 register		10-92
0x0184	VHDNIFIRCOEF23 VHD IFIR filter coefficient 2, 3 register		10-92
0x0188	VHDNIFIRCOEF45 VHD IFIR filter coefficient 4, 5 register		10-93
0x018C	VHDNIFIRCOEF67 VHD IFIR filter coefficient 6, 7 register		10-93
0x0400ÿm x 0x20	VHDNPMRESO Video Layer Resolution Register 10-94 for VHD Partition m		
0x0404ÿm x 0x20	VHDNPMLADDR Video Layer VHD Partition m Address Register 10-94		
0x0408ÿm x 0x20	VHDNPMCADDR Chroma Address Register 10-95 for Video Layer VHD Partition m		
0x040Cÿm x 0x20	VHDNPMSTRIDE Video layer stride registers for VHD partition m 10-95		
0x0410ÿm x 0x20	VHDNPMVFPOS video layer VHD partition m in the video content start position (First POSition) register		10-96
0x0414ÿm x 0x20	VHDNPMVLPOS Video layer VHD partition m at the end position (First POSition) register of video content		10-96
0x0C04	VHDN64REGIONENL	Video layer VHD 16 partition 0~15 partition enable register	10-97
0x3000ÿi x 0x1000	VSDICTRL	VSD Control Register	10-99

offset address	name	describe	page number
0x3004ÿi x 0x1000	VSDIUPD	VSD channel update enable register	10-100
0x3010ÿi x 0x1000	VSDICADDR Current frame address register		10-101
0x3014ÿi x 0x1000	VSDICCADDR Chroma address register for the current frame		10-101
0x3024ÿi x 0x1000	VSDISTRIDE	The stride register of the surface	10-102
0x3028ÿi x 0x1000	VSDIIRESO	Input Resolution Register	10-102
0x3034ÿi x 0x1000	VSDICBMPARA overlay related parameter register		10-103
0x3060ÿi x 0x1000	VSDIDFPOS	Surface at the starting position of the display window (First POSition) register	10-103
0x3064ÿi x 0x1000	VSDIDLPOS	Surface at the end of the display window (Last POSition) register	10-104
0x3070ÿi x 0x1000	VSDIBK	The background color register of the video layer	10-104
0x3080ÿi x 0x1000	VSDICSCIDC color space conversion input DC component register 10-105		
0x3084ÿi x 0x1000	VSDICSCODC color space conversion output DC component register 10-106		
0x3088ÿi x 0x1000	VSDICSCP0	Color Space Conversion Parameter Register	10-106
0x308Cÿi x 0x1000	VSDICSCP1	Color Space Conversion Parameter 1 Register	10-107
0x3090ÿi x 0x1000	VSDICSCP2	Color Space Conversion Parameter 2 Register	10-107
0x3094ÿi x 0x1000	VSDICSCP3	Color Space Conversion Parameter 3 Register	10-108
0x3098ÿi x 0x1000	VSDICSCP4	Color Space Conversion Parameter 4 Register	10-109
0x3180ÿi x 0x1000	VSDIIFIRCOEF01 VSD IFIR filter coefficient 0, 1 register		10-109
0x3184ÿi x 0x1000	VSDIIFIRCOEF23 VSD IFIR filter coefficient 2, 3 register		10-109

offset address	name	describe	page number
0x3188ÿi x 0x1000	VSDIIFIRCOEF45	VSD IFIR filter coefficient 4, 5 register	10-110
0x318Cÿi x 0x1000	VSDIIFIRCOEF67	VSD IFIR filter coefficient 6, 7 register	10-110
0x3400ÿi x 0x1000	VSDIP0RESO	Video Layer VSD Partition 0 Resolution Registers	10-111
0x3404ÿi x 0x1000	VSDIP0LADDR	Video Layer VSD Partition 0 Address Register	10-111
0x3408ÿi x 0x1000	VSDIP0CADDR	Video Layer VSD Partition 0 Chroma Address Register	10-112
0x340Cÿi x 0x1000	VSDIP0STRIDE	Video Layer VSD Partition 0 stride registers	10-112
0x3410ÿi x 0x1000	VSDIP0VFPOS	video layer VSD partition 0 in the video content start position (First POSition) register	10-113
0x3414ÿi x 0x1000	VSDIP0VLPOS	Video layer VSD partition 0 at the end position (First POSition) register of video content	10-113
0x3C04ÿi x 0x1000	VSDI1REGIONEN	Video Layer VSD Single Region Enable Register	10-114
0x8200	WBC2CTRL	Control register for WBC2	10-114
0x8204	WBC2UPD	WBC2 channel update enable register	10-115
0x8208	WBC2ADDR	CAPTURE write address address register	10-116
0x820C	WBC2STRIDE	The stride register of CAPTURE	10-116
0x8210	WBC2ORESO	Output Resolution Register	10-117
0x8220	WBC2CADDR	CAPTURE Write Address Chroma Address Register	10-117
0x8224	WBC2CSTRIDE	Chroma stride register of CAPTURE	10-118
0x82C0	WBC2HSP	Horizontal scaling parameter configuration (horizontal Scaling Parameter) register	10-118
0x82C4	WBC2HLOFFSET	Brightness horizontal position offset register	10-120
0x82C8	WBC2HCOFFSET	Chroma Horizontal Position Offset Register	10-120
0x82CC	WBC2VSP	Vertical Scaling Parameter Register	10-120
0x82D0	WBC2VSR	Vertical scaling factor (Luma Vertical Scaling Ratio) register	10-122

offset address	name	describe	page number
0x82D4	WBC2VOFFSET Vertical Luma Offset Register		10-122
0x82D8	WBC2ZMEORESO Scale unit output resolution register		10-123
0x82DC	WBC2ZMEIRESO Scaling unit input and output resolution register		10-123
0x9000	G0CTRL	G0 layer control register	10-124
0x9004	G0UPD	Graphics layer update enable register	10-125
0x9008	G0ADDR	graphics layer address register	10-126
0x900C	G0STRIDE	The stride register of the graphics layer	10-126
0x9010	G0CBMPARA overlay related parameter register		10-127
0x9014	G0CKEYMAX	color key maximum value register	10-128
0x9018	G0CKEYMIN	color key minimum value register	10-128
0x901C	G0CMASK	MASK value of color key	10-129
0x9020	G0IRESO	Input Resolution Register	10-129
0x9024	G0ORESO	Output Resolution Register	10-130
0x902C	G0DFPOS	Surface at the starting position of the display window (First POSition) register	10-130
0x9030	G0DLPOS	Surface at the end of the display window (Last POSition) register	10-131
0x90A0	G0CSCIDC	Color Space Conversion Input DC Component Registers 10-131	
0x90A4	G0CSCODC	Color space conversion output DC component register 10-132	
0x90A8	G0CSCP0	Color Space Conversion Parameter 0 Register	10-132
0x90AC	G0CSCP1	Color Space Conversion Parameter 1 Register	10-133
0x90B0	G0CSCP2	Color Space Conversion Parameter 2 Register	10-134
0x90B4	G0CSCP3	Color Space Conversion Parameter 3 Register	10-134
0x90B8	G0CSCP4	Color Space Conversion Parameter 4 Register	10-135
0x91B4	G0DCMPBANKWIDTH	G0 layer compressed data bank width register	10-135
0x91B8	G0DCMPSTRIDE G0 layer compressed data stride register		10-136
0x91BC	G0DCMPAADDR G0 layer A component compressed data start address register 10-136		
0x91C0	G0DCMPRADDR G0 layer R component compressed data start address register 10-137		

offset address	name	describe	page number
0x91C4	G0DCMPGADDR	G0 layer G component compressed data start address register	10-137
0x91C8	G0DCMPBADDR	G0 layer B component compressed data start address register	10-137
0x9400	G2CTRL	G2 layer control register	10-138
0x9404	G2UPD	Graphics layer update enable register	10-139
0x9408	G2ADDR	graphics layer address register	10-139
0x940C	G2STRIDE	The stride register of the graphics layer	10-139
0x9410	G2CBMPARA	overlay related parameter register	10-140
0x9414	G2CKEYMAX	color key maximum value register	10-141
0x9418	G2CKEYMIN	color key minimum value register	10-141
0x941C	G2CMASK	MASK value of color key	10-142
0x9420	G2IRESO	Input Resolution Register	10-142
0x9424	G2ORESO	Output Resolution Register	10-143
0x942C	G2DFPOS	Surface at the starting position of the display window (First POSition) register	10-143
0x9430	G2DLPOS	Surface at the end of the display window (Last POSition) register	10-144
0x94A0	G2CSCIDC	Color Space Conversion Input DC Component Registers	10-144
0x94A4	G2CSCODC	G2 layer color space conversion output DC component register	10-145
0x94A8	G2CSCP0	G2 layer color space conversion parameter 0 register	10-145
0x94AC	G2CSCP1	G2 layer color space conversion parameter 1 register	10-146
0x94B0	G2CSCP2	G2 layer color space conversion parameter 2 register	10-147
0x94B4	G2CSCP3	G2 Layer Color Space Conversion Parameter 3 Register	10-147
0x94B8	G2CSCP4	G2 layer color space conversion parameter 4 register	10-148
0x9600	G3CTRL	G3 layer control register	10-148
0x9604	G3UPD	Graphics layer update enable register	10-149
0x9608	G3ADDR	graphics layer address register	10-150
0x960C	G3STRIDE	The stride register of the graphics layer	10-150
0x9610	G3CBMPARA	overlay related parameter register	10-151
0x9614	G3CKEYMAX	color key maximum value register	10-152

offset address	name	describe	page number
0x9618	G3CKEYMIN	color key minimum value register	10-152
0x961C	G3CMASK	MASK value of color key	10-153
0x9620	G3IRESO	Input Resolution Register	10-153
0x9624	G3ORESO	Output Resolution Register	10-154
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0xC240	DATE_COEFF16 VPS configuration register		10-224
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0xC284	DATE_ISRSTATE Interrupt Status Register		10-233
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offset address	name	describe	page number
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0xC428	DATE1_COEFF10 Teletext configuration register		10-246
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0xC430	DATE1_COEFF12 Closed Caption Configuration Register		10-248
0xC434	DATE1_COEFF13 CGMS Configuration Register		10-248
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0xC440	DATE1_COEFF16 VPS configuration register		10-250
0xC444	DATE1_COEFF17 VPS configuration register		10-251
0xC448	DATE1_COEFF18 VPS configuration register		10-251
0xC44C	DATE1_COEFF19 VPS configuration register		10-252
0xC450	DATE1_COEFF20 Teletext configuration register		10-252
0xC454	DATE1_COEFF21 Output Matrix Control Register		10-253
0xC458	DATE1_COEFF22 DTO initial phase configuration register		10-256
0xC45C	DATE1_COEFF23 VIDEO_OUT delay configuration register		10-257
0xC480	DATE1_ISRMASK Interrupt Mask Register		10-258
0xC484	DATE1_ISRSTATE Interrupt Status Register		10-259
0xC488	DATE1_ISR	interrupt register	10-259
0xC490	DATE1_VERSION version register		10-260
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0xCE0C	VOINTMSK	VOU Interrupt Mask Register	10-265
0xCE10	VOUVERSION1 VOU version 1 register		10-266
0xCE14	VOUVERSION2 VOU version 2 register		10-266
0xCE18 VOMUXDATA VO output interface multiplex data (VOPINTEST) register			10-267
0xCE1C VOMUX		VO output interface check register	10-268
0xCE24	VGACSCIDC color space conversion input DC component register 10-269		

offset address	name	describe	page number
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0xCE2C	VGACSCP0	Color Space Conversion Parameter 0 Register	10-270
0xCE30	VGACSCP1	Color Space Conversion Parameter 1 Register	10-270
0xCE34	VGACSCP2	Color Space Conversion Parameter 2 Register	10-271
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0xCE48	VHDVCOEFAD VHD vertical luma, horizontal chroma filter coefficient address register		10-274
0xCE58	WBC2HCOEFAD WBC2 horizontal luma, horizontal chroma filter coefficient address register		10-274
0xCE5C WBC2VCOEFAD WBC2 vertical luma, horizontal chroma filter coefficient address register			10-275
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0xD200ÿ 0xD284	VHDHCCOEF	VHD Horizontal Chroma Scaling Filter Coefficient Register 10-276	
0xD400ÿ 0xD50C	VHDVLCOEF	VHD Vertical Brightness Scaling Filter Coefficient Register 10-277	
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0xE200ÿ 0xE284	WBCHCCOEF	WBC horizontal chroma scaling filter coefficient register 10-279	
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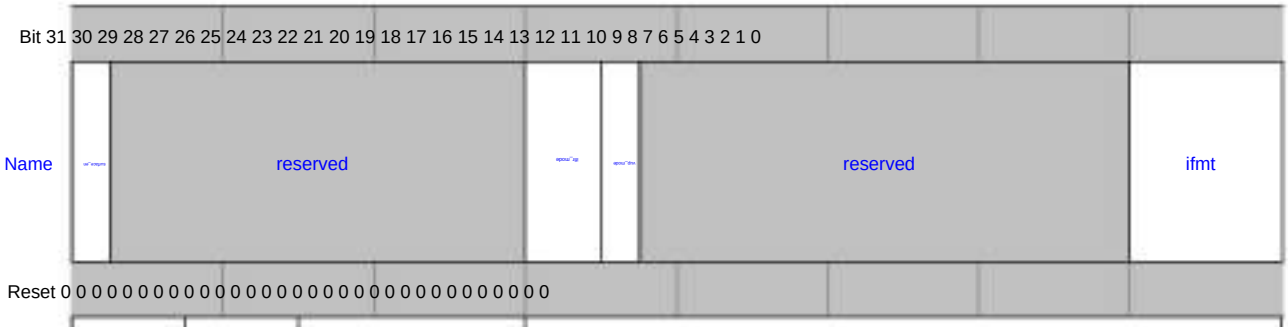
11.2.5 Register Description

VHDNCTRL

VHDNCTRL is the VHD control register. This register can configure the relevant information of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0000	VHDNCTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	surface_en	surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:20]	RO	reserved	reserve.
[19:18]	RW	ifir_mode	Horizontal chroma IFIR mode. 00: reserved. 01: Chroma IFIR copy mode; 10: bilinear interpolation; 11: 6th order FIR.
[17]	RW	vup_mode	Register update mode selection. 0: update by field; 1: Update by frame.
[16:4]	RO	reserved	reserve.
[3:0]	RW	ifmt	Input data format. 0x3ÿSPYCbCr420ÿ 0x4ÿSPYCbCr422ÿ Other: reserved.

VHDNUPD

VHDNUPD Update enable register for VHD channel.

Offset Address	Register Name	Total Reset Value
0x0004	VHDNUPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

VHDNCADDR

VHDNCADDR is the address register of the current frame. For the package pixel format, it is the frame buffer address; for the semi-planar pixel format, it is the luma frame buffer address.

Offset Address	Register Name	Total Reset Value
0x0010	VHDNCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_caddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_caddr	Address of current frame.

VHDNCCADDR

VHDNCCADDR is the chroma address register of the current frame. This address is invalid for the package pixel format; it is the chroma frame buffer address for the semi-planar pixel format.

Offset Address	Register Name	Total Reset Value
0x0014	VHDNCCADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_ccaddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	surface_ccaddr	Chroma address of current frame.

VHDNSTRIDE

VHDDNSTRIDE is the stride register of the surface.

Offset Address	Register Name	Total Reset Value
0x0024	VHDNSTRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_cstride / surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of chroma frame buffer (useful for semi-planaer format), 128bit aligned.
[15:0]	RW	surface_stride	The stride of the frame buffer (for the semi-planaer format, refers to the stride of the brightness), 128bit alignment.

VHDNIRESO

VHDNIRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0028	VHDNIRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / them / iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x0028	VHDNIRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[23:12]	RW ih	Height, unit: line. The actual height is minus 1. Take the frame height as the reference, and use the row unit.
[11:0]	RW iw	Width, unit: pixel. The actual width is minus 1.

VHDNCBMPARA

VHDNCBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0034	VHDNCBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:8]	RW reserved	reserve.
[7:0]	RW galpha	Overlays the global alpha value. The value range is 0~128. 128 is fully opaque; 0 is fully transparent.

VHDNDFPOS

VHDNDFPOS is the Surface's initial position (First POSition) register in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0060	VHDNDFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	disp_yfpos / disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Displays the column start coordinates. Take the frame height as the reference, and use the row unit.
[11:0]	RW	disp_xfpos	Displays the row start coordinates.

VHDNDLPOS

VHDNDLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0064	VHDNDLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	disp_ylpos / disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Displays the column end coordinates. Take the frame height as the reference, and use the row unit.
[11:0]	RW	disp_xlpos	Display line end coordinates.

VHDBK

VHDBK is the background color register of the video layer.

Offset Address	Register Name	Total Reset Value
0x0070	VHDBK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbk_alpha								vbk_y								vbk_cb								vbk_cr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:24]	RW vbk_alpha	The background fill color of the video layer ranges from 0 to 128.
[23:16]	RW vbk_y	Y component.
[15:8]	RW vbk_cb	Cb component.
[7:0]	RW vbk_cr	Cr component.

VHDNCSCIDC

VHDNCSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x0080	VHDNCSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									cscidc2								cscidc1								cscidc0						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:28]	RO reserved	reserve.
[27]	RW csc_en	CSC enable control signal. 0: forbidden; 1: enable.
[26:18]	RW cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

VHDNCSCODC

VHDNCSCODC Output DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x0084	VHDNCSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:18]	RW	cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

VHDNCSCP0

VHDNCSCP0 is the color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0088	VHDNCSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VHDNCSCP1

VHDNCSCP1 is the color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x008C	VHDNCSCP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp10	—	cscp02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VHDNCSCP2

VHDNCSCP2 is the color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0090	VHDNCSCP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp12	—	cscp11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VHDNCSCP3

VHDNCSCP3 is the color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0094	VHDNCSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VHDNCSCP4

VHDNCSCP4 is the color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0098	VHDNCSCP4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscp22
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

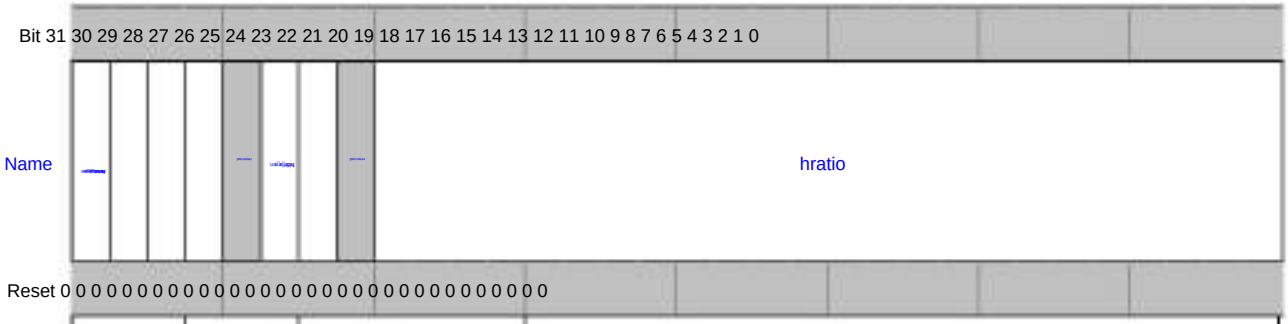
Bits	Access Name		Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VHDNHSP

VHDNHSP is the horizontal scaling parameter configuration (horizontal Scaling Parameter) register.

Zoom ratio = input width / output width

Offset Address	Register Name	Total Reset Value
0x00C0	VHDNHSP	0x0000_0000



Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal brightness scaling enabled. 0: forbidden; 1: enable.
[30]	RW	hchmsc_en	Horizontal chroma scaling enabled. 0: forbidden; 1: enable.
[29]	RW	hlmid_en	Horizontal luma scaling median filter enable (this bit has no effect when hlfir_en is invalid). 0: forbidden; 1: enable.
[28]	RW	hchmid_en	Horizontal chroma scaling median filter enable (this bit has no effect when hchfir_en is invalid). 0: disable; 1: enable.
[27]	RO	reserved	reserve.
[26]	RW	hlfir_en	Horizontal brightness scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).
[25]	RW	hchfir_en	Horizontal chroma scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).
[24]	RO	reserved	reserve.
[23:0]	RW	hratio	Horizontal zoom factor, in (u,4,20) format.

VHDNHLOFFSET

VHDNHLOFFSET is the brightness horizontal position offset register.

Offset Address	Register Name	Total Reset Value
0x00C4	VHDNHLOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_loffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	hor_loffset	Horizontal brightness position offset, in (s,8,20) format. complement representation.

VHDNHCOFFSET

VHDNHCOFFSET is the chroma horizontal position offset register.

Offset Address	Register Name	Total Reset Value
0x00C8	VHDNHCOFFSET	0x0000_0000

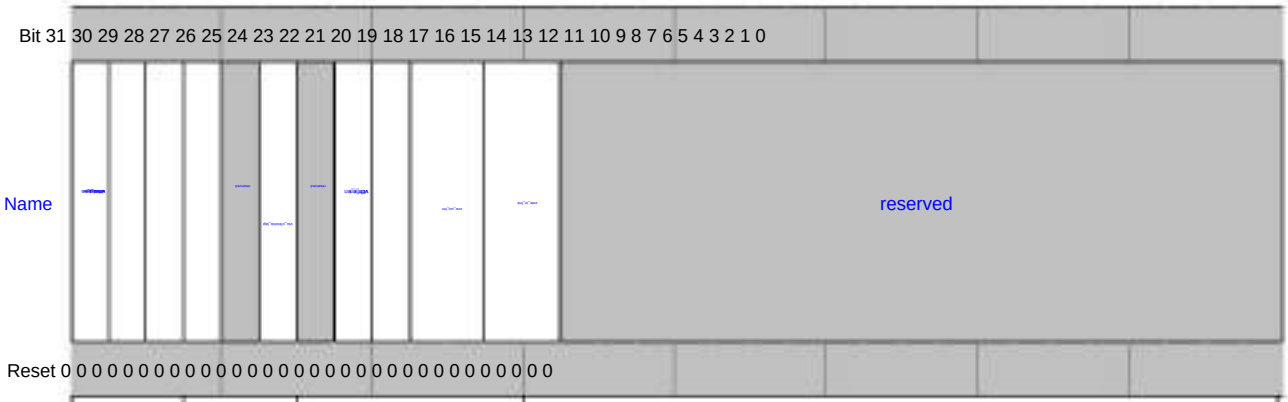
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hor_coffset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	hor_coffset	Horizontal chroma position offset, in (s,8,20) format. complement representation.

VHDNVSP

VHDNVSP is the vertical scaling parameter register.

Offset Address	Register Name	Total Reset Value
0x00CC	VHDNVSP	0x0000_0000



Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical brightness scaling enabled. 0: forbidden; 1: enable.
[30]	RW	vchmsc_en	Vertical chroma scaling enabled. 0: forbidden; 1: enable.
[29]	RW	vlmid_en	Vertical luma scaling median filter enable (this bit has no effect when vlfir_en is invalid). 0: forbidden; 1: enable.
[28]	RW	vchmid_en	Vertical chroma scaling median filter enable (this bit has no effect when vchfir_en is invalid). 0: forbidden; 1: enable.
[27]	RO	reserved	reserve.
[26]	RW	vsc_chroma_tap	Vertical chroma scaling order. 0: 4th order FIR; 1: 2nd order FIR.
[25]	RO	reserved	reserve.
[24]	RW	vlfir_en	Vertical brightness scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).

[23] RW vchfir_en			Vertical chroma scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).
[22:21] RW zme_out_fmt			Scaled output data format. 0ÿ422ÿ Other: reserved.
[20:19] RW zme_in_fmt			Scale input data format. 0ÿ422ÿ 1ÿ420ÿ
[18:0] RO reserved			reserve.

VHDNVSR

VHDNVSR is the Luma Vertical Scaling Ratio register. non-immediate registers.

Zoom ratio = input height/output height.

Offset Address	Register Name	Total Reset Value
0x00D0	VHDNVSR	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																returned															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	is back	Vertical scaling factor, in (u,4,12) format.

VHDNVOFFSET

VHDNVOFFSET is the Vertical Luma Offset register.

The vertical zoom offset is affected by two factors: pan-scan and field offset when repeating frames. When there is no field offset, vluma_offset is the lowest integer bit + decimal place of offset_pan-scan; in YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset = scaling_chroma/2-0.25. When a field offset is required (such as a static frame or a repeated frame), assuming that the bottom field is repeated, the vluma_offset and vchroma_offset of the top field configuration are the same as the above without offset, and the bottom field configuration needs to consider the field offset.

Offset Address	Register Name	Total Reset Value
0x00D4	VHDNVOFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	vluma_offset	vchroma_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	vluma_offset	Vertical brightness offset, complement representation, (s,4,12) format.
[15:0]	RW	vchroma_offset	Vertical chroma offset, complement representation, (s,4,12) format.

VHDNZMEORESO

VHDNZMEORESO is the output resolution register for the scaling unit.

Offset Address	Register Name	Total Reset Value
0x00D8	VHDNZMEORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, unit: line. The actual height is minus 1. When progressive, the frame height is used as a reference, and the unit is row; when interlaced, the field height is used as a reference, and the unit is row.
[11:0]	RW	ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

VHDNZMEIRESO

VHDNZMEIRESO is the I/O resolution register of the scaling unit.

Offset Address	Register Name	Total Reset Value
0x00DC	VHDNZMEIRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	them	iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, unit: line. The actual height is minus 1. When progressive, the frame height is used as a reference, and the line unit is used; when interlaced, the field height is used as a reference, and the line unit is used.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

VHDNIFIRCOEF01

VHDNIFIRCOEF01 is the VHD IFIR filter coefficient 0, 1 register.

Offset Address	Register Name	Total Reset Value
0x0180	VHDNIFIRCOEF01	0x000D_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	coef1	reserved	coef0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef1	IFIR filter factor 1.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef0	IFIR Filter coefficient 0.

VHDNIFIRCOEF23

VHDNIFIRCOEF23 is the VHD IFIR filter coefficient 2 and 3 registers.

Offset Address	Register Name	Total Reset Value
0x0184	VHDNIFIRCOEF23	0x0132_03C1

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef3	reserved	coef2
Reset	0 0 0 0 0 0 0 1 0 0 1	1 0 0 1 0 0 0 0 0 0 0 1	1 1 1 0 0 0 0 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef3	IFIR filter factor3.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef2	IFIR filter factor 2.

VHDNIFIRCOEF45

VHDNIFIRCOEF45 is the VHD IFIR filter coefficient 4, 5 register.

Offset Address	Register Name	Total Reset Value
0x0188	VHDNIFIRCOEF45	0x03C1_0132

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef5	reserved	coef4
Reset	0 0 0 0 0 0 1 1 1	1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef5	IFIR filter factor 5.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef4	IFIR filter factor4.

VHDNIFIRCOEF67

VHDNIFIRCOEF67 is the VHD IFIR filter coefficient 6 and 7 registers.

Offset Address	Register Name	Total Reset Value
0x018C	VHDNIFIRCOEF67	0x0000_000D

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef7	reserved	coef6
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef7	IFIR filter coefficient7.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef6	IFIR filter coefficient6.

VHDNPMRESO

VHDNPMRESO is the resolution register for video layer VHD partition m. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0400ÿm x 0x20 (m = 0ÿ15)	VHDNPMRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	In
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	reserved	reserve.
[11:0]	RW	w	Width, unit: pixel. The actual width is minus 1. Note: Actual width must be an even number.

VHDNPMLADDR

VHDNPMLADDR is the address register of video layer VHD partition m.

Offset Address	Register Name	Total Reset Value
0x0404ÿm x 0x20 (m = 0ÿ15)	VHDNPMLADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	The first address of video layer VHD partition m.

VHDNPMCADDR

VHDNPMCADDR is the chrominance address register of video layer VHD partition m.

Offset Address	Register Name	Total Reset Value
0x0408ÿm x 0x20 (m = 0ÿ15)	VHDNPMCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	The chroma head address of the video layer VHD partition m.

VHDNPMSTRIDE

VHDNPMSTRIDE is the stride register of video layer VHD partition m.

Offset Address	Register Name	Total Reset Value
0x040Cÿm x 0x20 (m = 0ÿ15)	VHDNPMSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Video layer VHD partition m Chroma buffer stride (useful for semi-planaer format), 128bit alignment.

Offset Address	Register Name	Total Reset Value
0x040Cÿm x 0x20 (m = 0ÿ15)	VHDNPMSTRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_cstride	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	surface_stride	The stride of the video layer VHD partition m buffer (for the semi-planaer format, refers to the stride of the brightness), 128bit alignment.

VHDNPMVFPOS

VHDNPMVFPOS is the first POSition register of the video layer VHD partition m in the video content. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0410ÿm x 0x20 (m = 0ÿ15)	VHDNPMVFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	video_yfpos video_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	reserve.
[23:12]	RW	video_yfpos	The starting coordinates of the video content column. Take the frame height as the reference, and use the row unit.
[11:0]	RW	video_xfpos	Video content line start coordinates.

VHDNPMVLPOS

VHDNPMVLPOS is the end position (First POSition) register of the video layer VHD partition m in the video content. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0414ÿm x 0x20 (m = 0ÿ15)	VHDNPMVLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	video_ylpos	video_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name	Description
[31:24]	RW reserved	reserve.
[23:12]	RW video_ylpos	The starting coordinates of the video content column. Take the frame height as the reference, and use the row unit.
[11:0]	RW video_xlpos	The start coordinates of video content line.

VHDN64REGIONENL

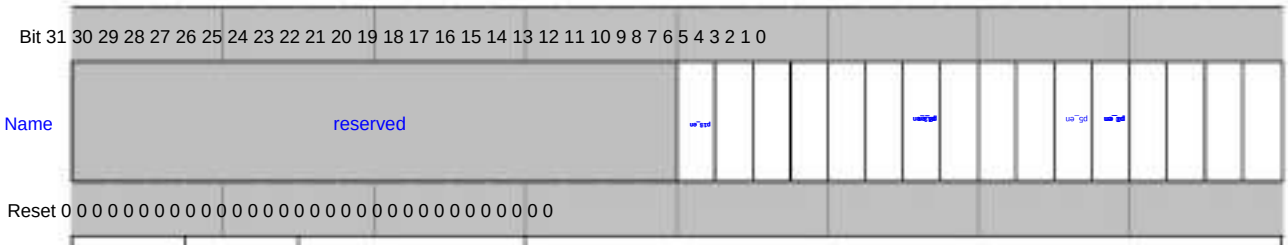
VHDN64REGIONENL is the enable register for 0~15 partitions of VHD 16 partitions in the video layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x0C04	VHDN64REGIONENL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

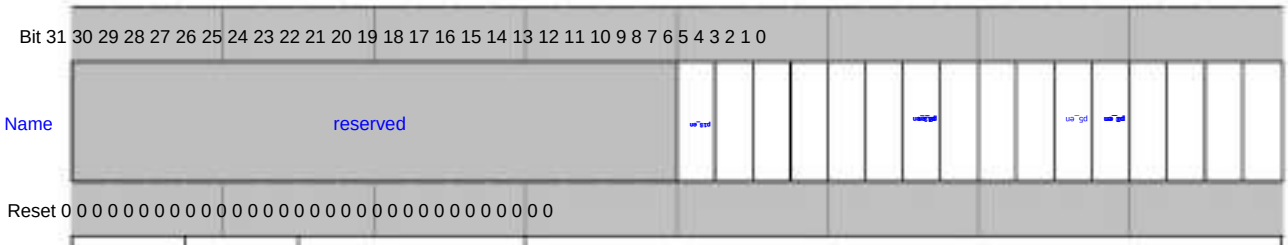
Bits	Access Name	Description
[31:16]	RW reserved	reserve.
[15]	RW p15_en	Enable signal for VHD partition 15. 0: forbidden; 1: enable.
[14]	RW p14_en	Enable signal for VHD partition 14. 0: forbidden; 1: enable.
[13]	RW p13_en	Enable signal for VHD partition 13. 0: forbidden; 1: enable.

Offset Address	Register Name	Total Reset Value
0x0C04	VHDN64REGIONENL	0x0000_0000



Bits	Access	Name	Description
[12]	RW	p12_en	Enable signal for VHD partition 12. 0: forbidden; 1: enable.
[11]	RW	p11_en	Enable signal for VHD partition 11. 0: forbidden; 1: enable.
[10]	RW	p10_en	Enable signal for VHD partition 10. 0: forbidden; 1: enable.
[9]	RW	p9_en	Enable signal for VHD partition 9. 0: forbidden; 1: enable.
[8]	RW	p8_en	Enable signal for VHD partition 8. 0: forbidden; 1: enable.
[7]	RW	p7_en	Enable signal for VHD partition 7. 0: forbidden; 1: enable.
[6]	RW	p6_en	Enable signal for VHD partition 6. 0: forbidden; 1: enable.
[5]	RW	p5_en	Enable signal for VHD partition 5. 0: forbidden; 1: enable.
[4]	RW	p4_en	Enable signal for VHD partition 4. 0: disable; 1: enable.

Offset Address	Register Name	Total Reset Value
0x0C04	VHDN64REGIONENL	0x0000_0000



Bits	Access	Name	Description
[3]	RW	p3_en	Enable signal for VHD partition 3. 0: forbidden; 1: enable.
[2]	RW	p2_en	Enable signal for VHD Partition 2. 0: forbidden; 1: enable.
[1]	RW	p1_en	Enable signal for VHD Partition 1. 0: forbidden; 1: enable.
[0]	RW	p0_en	Enable signal for VHD partition 0. 0: forbidden; 1: enable.

VSDICTRL

VSDICTRL is the VSD control register. This register can configure the relevant information of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3000ÿi x 0x1000 (i = 0ÿ1)	VSDICTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																			[illegible]	[illegible]	reserved								ifmt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:20]	RO	reserved	reserve.
[19:18]	RW	ifir_mode	Horizontal chroma IFIR mode. 00: reserved. 01: Chroma IFIR copy mode; 10: bilinear interpolation; 11: 6th order FIR.
[17]	RW	vup_mode	Register update mode selection. 0: update by field; 1: Update by frame.
[16:4]	RO	reserved	reserve.
[3:0]	RW	ifmt	Input data format. 0x3ÿSPYCbCr420ÿ 0x4ÿSPYCbCr422ÿ Other: reserved.

VSDIUPD

VSDIUPD Update enable register for VSD channel.

Offset Address	Register Name	Total Reset Value
0x3004ÿi x 0x1000 (i = 0ÿ1)	VSDIUPD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1]	RO reserved	reserve.
[0]	RW regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

VSDICADDR

VSDICADDR is the address register of the current frame. For the package pixel format, this address is the frame buffer address; for the semi-planar pixel format, this address is the luma frame buffer address.

Offset Address	Register Name	Total Reset Value
0x3010ÿi x 0x1000 (i = 0ÿ1)	VSDICADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_caddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RW surface_caddr	DIE The address of the current frame.

VSDICCADDR

VSDICCADDR is the chroma address register of the current frame. This address is invalid for the package pixel format; it is the chroma frame buffer address for the semi-planar pixel format.

Offset Address	Register Name	Total Reset Value
0x3014ÿi x 0x1000 (i = 0ÿ1)	VSDICCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_ccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_ccaddr	DIE Chroma address of current frame.

VSDISTRIDE

VSDISTRIDE is the stride register of the surface.

Offset Address	Register Name	Total Reset Value
0x3024ÿi x 0x1000 (i = 0ÿ1)	VSDISTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of chroma frame buffer (useful for semi-planaer format), 128bit aligned.
[15:0]	RW	surface_stride	The stride of the frame buffer (for the semi-planaer format, refers to the stride of the brightness), 128bit alignment.

VSDIIRESO

VSDIIRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3028ÿi x 0x1000 (i = 0ÿ1)	VSDIIRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																them														iw	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, unit: line. The actual height is minus 1. Take the frame height as the reference, and use the row unit.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1.

VSDICBMPARA

VSDICBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3034ÿi x 0x1000 (i = 0ÿ1)	VSDICBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														alpha	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	reserve.
[7:0]	RW	galpha	Overlays the global alpha value. The value range is 0~128. 128 is fully opaque; 0 is fully transparent.

VSDIDFPOS

VSDIDFPOS is the Surface's initial position (First POSition) register in the display window. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3060ÿi x 0x1000 (i = 0ÿ1)	VSDIDFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_yfpos	disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Displays the column start coordinates. Take the frame height as the reference, and use the row unit.
[11:0]	RW	disp_xfpos	Displays the row start coordinates.

VSDIDLPOS

VSDIDLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3064ÿi x 0x1000 (i = 0ÿ1)	VSDIDLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Displays the column end coordinates. Take the frame height as the reference, and use the row unit.
[11:0]	RW	disp_xlpos	Display line end coordinates.

VSDIBK

VSDIBK is the background color register of the video layer.

Offset Address	Register Name	Total Reset Value
0x3070ÿi x 0x1000 (i = 0ÿ1)	VSDIBK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	vbk_alpha	vbk_y	vbk_cb	vbk_cr
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	vbk_alpha	The background fill color of the video layer ranges from 0 to 128.
[23:16]	RW	vbk_y	Y component.
[15:8]	RW	vbk_cb	Cb component.
[7:0]	RW	vbk_cr	Cr component.

VSDICSCIDC

VSDICSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x3080ÿi x 0x1000 (i = 0ÿ1)	VSDICSCIDC	0x0000_0000

Bit	31 30 29 28	27	26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Name	reserved	csc_en	cscidc2	cscidc1	cscidc0
Reset	0 0 0 0	0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	csc_en	CSC enable control signal. 0: forbidden; 1: enable.
[26:18]	RW	cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

VSDICSCODC

VSDICSCODC Output DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x3084ÿi x 0x1000 (i = 0ÿ1)	VSDICSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / cscodc2 / cscodc1 / cscodc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:18]	RW	cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

VSDICSCP0

VSDICSCP0 is the color space conversion parameter register. Instant register.

Offset Address	Register Name	Total Reset Value
0x3088ÿi x 0x1000 (i = 0ÿ1)	VSDICSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	— / cscp01 / — / cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VSDICSCP1

VSDICSCP1 is the color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x308Cÿi x 0x1000 (i = 0ÿ1)	VSDICSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																cscp10								—						cscp02	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VSDICSCP2

VSDICSCP2 is the color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x3090ÿi x 0x1000 (i = 0ÿ1)	VSDICSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																cscp12								—						cscp11	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

Offset Address	Register Name	Total Reset Value
0x3090ÿi x 0x1000 (i = 0ÿ1)	VSDICSCP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp12	— cscp11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VSDICSCP3

VSDICSCP3 is the color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x3094ÿi x 0x1000 (i = 0ÿ1)	VSDICSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	— cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VSDICSCP4

VSDICSCP4 is the color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x3098ÿi x 0x1000 (i = 0ÿ1)	VSDICSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cscp22	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VSDIIFIRCOEF01

VSDIIFIRCOEF01 is the VSD IFIR filter coefficient 0, 1 register.

Offset Address	Register Name	Total Reset Value
0x3180ÿi x 0x1000 (i = 0ÿ1)	VSDIIFIRCOEF01	0x000D_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coef1								reserved						coef0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef1	IFIR filter factor 1.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef0	IFIR Filter coefficient 0.

VSDIIFIRCOEF23

VSDIIFIRCOEF23 is the VSD IFIR filter coefficient 2, 3 register.

Offset Address	Register Name	Total Reset Value
0x3184ÿi x 0x1000 (i = 0ÿ1)	VSDIIFIRCOEF23	0x0132_03C1

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	coef3	reserved	coef2
Reset	0 0 0 0 0 0 0 1	0 0 1	1 0 0 1 0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef3	IFIR filter factor3.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef2	IFIR filter factor 2.

VSDIIFIRCOEF45

VSDIIFIRCOEF45 is the VSD IFIR filter coefficient 4, 5 register.

Offset Address	Register Name	Total Reset Value
0x3188ÿi x 0x1000 (i = 0ÿ1)	VSDIIFIRCOEF45	0x003C_0132

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	coef5	reserved	coef4
Reset	0 0 0 0 0 0 0 0	0 0 1	1 1 1 0 0 0 0 0	0 0 0 1 0 0 1 1 0 0 1 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef5	IFIR filter factor 5.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef4	IFIR filter factor4.

VSDIIFIRCOEF67

VSDIIFIRCOEF67 is the VSD IFIR filter coefficient 6 and 7 registers.

Offset Address	Register Name	Total Reset Value
0x318Cÿi x 0x1000 (i = 0ÿ1)	VSDIIFIRCOEF67	0x0000_000D

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef7	reserved	coef6
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 1 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	coef7	IFIR filter coefficient7.
[15:10]	RO	reserved	reserve.
[9:0]	RW	coef6	IFIR filter coefficient6.

VSDIP0RESO

VSDIP0RESO is the resolution register for VSD partition 0 of the video layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3400ÿi x 0x1000 (i = 0ÿ1)	VSDIP0RESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	h	In
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	reserve.
[23:12]	RW	h	Height, taking the frame height as a reference. Behavior unit, the actual height minus 1. Note: Actual height must be an even number.
[11:0]	RW	w	Width, unit: pixel. The actual width is minus 1. Note: Actual width must be an even number.

VSDIP0LADDR

VSDIP0LADDR is the address register of video layer VSD partition 0.

Offset Address	Register Name	Total Reset Value
0x3404ÿi x 0x1000 (i = 0ÿ1)	VSDIP0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	The first address of video layer VSD partition 0.

VSDIP0CADDR

VSDIP0CADDR is the chroma address register of VSD partition 0 of the video layer.

Offset Address	Register Name	Total Reset Value
0x3408ÿi x 0x1000 (i = 0ÿ1)	VSDIP0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	The first address of chroma in VSD partition 0 of video layer.

VSDIP0STRIDE

VSDIP0STRIDE is the stride register of video layer VSD partition 0.

Offset Address	Register Name	Total Reset Value
0x340Cÿi x 0x1000 (i = 0ÿ1)	VSDIP0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Video layer VSD partition 0 stride of chroma buffer (useful for semi-planaer format), 128bit alignment.

Offset Address	Register Name	Total Reset Value
0x340Cÿi x 0x1000 (i = 0ÿ1)	VSDIP0STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_cstride	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	surface_stride	The stride of the VSD partition 0 buffer of the video layer (for the semi-planaer format, it refers to the stride of the brightness), 128bit alignment.

VSDIP0VFPOS

VSDIP0VFPOS is the first POSition register of video layer VSD partition 0 in video content. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3410ÿi x 0x1000 (i = 0ÿ1)	VSDIP0VFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	video_yfpos	video_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RW	reserved	reserve.
[23:12]	RW	video_yfpos	The starting coordinates of the video content column. Take the frame height as the reference, and use the row unit.
[11:0]	RW	video_xfpos	Video content line start coordinates.

VSDIP0VLPOS

VSDIP0VLPOS is the end position (First POSition) register of video layer VSD partition 0 in video content. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3414ÿi x 0x1000 (i = 0ÿ1)	VSDIP0VLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	video_ylpos video_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW reserved	reserve.
[23:12]	RW video_ylpos	The starting coordinates of the video content column. Take the frame height as the reference, and use the row unit.
[11:0]	RW video_xlpos	The start coordinates of video content line.

VSDI16 REGIONS

VSDI16REGIONEN is the video layer VSD single region enable register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x3C04ÿi x 0x1000 (i = 0ÿ1)	VSDI16 REGIONS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved p0_en
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1]	RW reserved	reserve.
[0]	RW p0_en	Enable signal for VSD partition 0. 0: forbidden; 1: enable.

WBC2CTRL

WBC2CTRL is the control register of WBC2. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x8200	WBC2CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																	reserved															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbc2_en	WBC2 is enabled. 0: disabled; 1: enable.
[30:29]	RO	reserved	reserve.
[28]	RW	wb_stp_en	Write back stopped. When the interface timing completes the effective area, if WBC2 write-back is not completed, the unwritten data of the current frame will not be written back. 0: disabled; 1: enable.
[27]	RO	reserved	reserve.
[26:24]	RW	dfp_sel	Data extraction point selection. 01: Data extraction point 1; From VHD.LBOX; 10: Data extraction point 2; From CBM.Mixer1; Other: reserved.
[23:14]	RO	reserved	reserve.
[13:12]	RW	Wbc0_dft	Output data format of WBC0 00ÿSPYCbCr422ÿ 01ÿSPYCbCr420ÿ Other: reserved.
[11: 0]	RO	reserved	reserve.

WBC2UPD

WBC2UPD Update enable register for WBC2 channel.

Offset Address	Register Name	Total Reset Value
0x8204	WBC2UPD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	Register update for CAPTURE. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

WBC2ADDR

WBC2ADDR is CAPTURE write address address register.

Offset Address	Register Name	Total Reset Value
0x8208	WBC2ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wbcaddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	wbcaddr	Frame buffer address. 4byte bit alignment, the lower 2bit is invalid (supports seamless splicing).

WBC2STRIDE

WBC2STRIDE is the stride register of CAPTURE.

Offset Address	Register Name	Total Reset Value
0x820C	WBC2STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	wbc0stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	ÿ	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x820C	WBC2STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	wbc0stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	wbc0stride	Frame buffer stride. 128bit aligned.

WBC2ORESO

WBC2ORESO is the output resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x8210	WBC2ORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	oh	ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, unit: line. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

WBC2CADDR

WBC2CADDR Write address for CAPTURE chroma address register.

Offset Address	Register Name	Total Reset Value
0x8220	WBC2CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	wbccaddr	Frame chroma buffer address. 4byte bit alignment, the lower 2bit is invalid (supports seamless splicing).

WBC2CSTRIDE

WBC2CSTRIDE is the chroma stride register of CAPTURE.

Offset Address	Register Name	Total Reset Value
0x8224	WBC2CSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wbc0cstride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

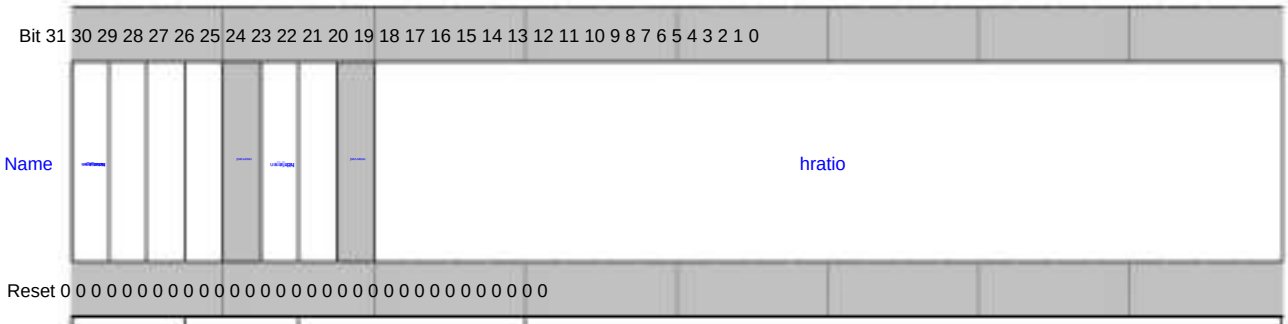
Bits	Access	Name	Description
[31:16]	ÿ	reserved	reserve.
[15:0]	RW	wbc0cstride	Frame chroma buffer stride. 16byte alignment.

WBC2HSP

WBC2HSP is the horizontal scaling parameter configuration (horizontal Scaling Parameter) register. non-immediate registers.

Zoom ratio = input width/output width.

Offset Address	Register Name	Total Reset Value
0x82C0	WBC2HSP	0x0000_0000



Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal brightness scaling enabled. 0: forbidden; 1: enable.
[30]	RW	hchmsc_en	Horizontal chroma scaling enabled. 0: forbidden; 1: enable.
[29]	RW	hlmid_en	Horizontal luma scaling median filter enable (this bit has no effect when hlfir_en is invalid). 0: forbidden; 1: enable.
[28]	RW	hchmid_en	Horizontal chroma scaling median filter enable (this bit has no effect when hchfir_en is invalid). 0: forbidden; 1: enable.
[27]	RO	reserved	reserve.
[26]	RW	hlfir_en	Horizontal brightness scaling mode. 0: Copy mode (filtering disabled); 1: Filtering mode (filtering enabled).
[25]	RW	hchfir_en	Horizontal chroma scaling mode. 0: Copy mode (filtering disabled); 1: Filtering mode (filtering enabled).
[24]	RO	reserved	reserve.
[23:0]	RW	hratio	Horizontal zoom factor, in (u,4,20) format.

WBC2HLOFFSET

WBC2HLOFFSET is the brightness horizontal position offset register. Used for pan-scan. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x82C4	WBC2HLOFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hor_loffset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	hor_loffset	Horizontal brightness position offset, in (s,8,20) format. complement representation.

WBC2HCOFFSET

WBC2HCOFFSET is the chroma horizontal position offset register. Used for pan-scan. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x82C8	WBC2HCOFFSET	0x0000_0000

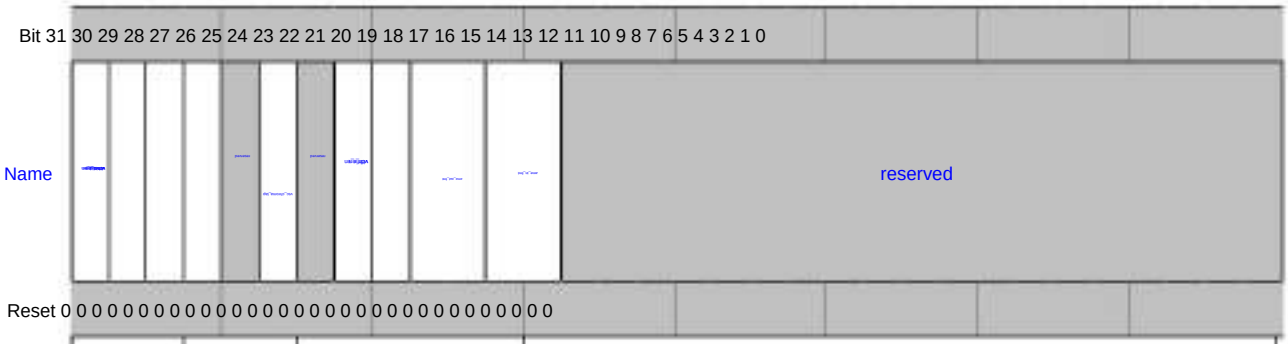
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hor_coffset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	hor_coffset	Horizontal chroma position offset, in (s,8,20) format. complement representation.

WBC2VSP

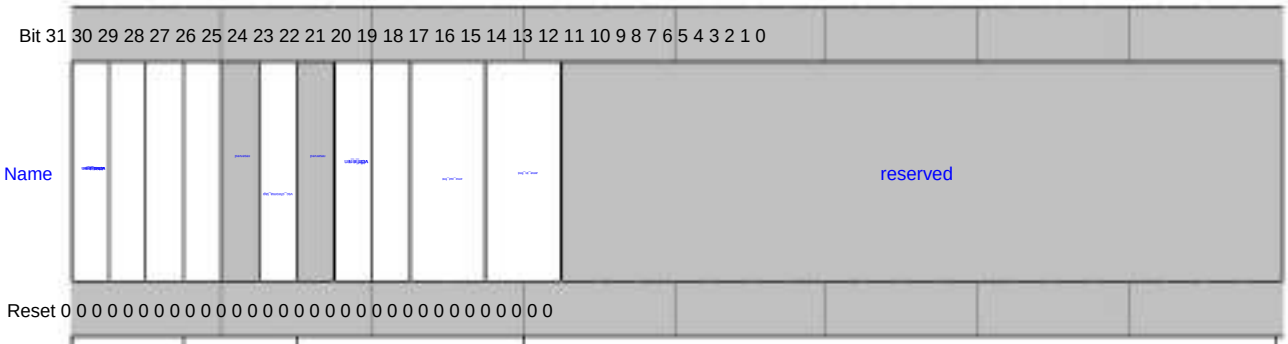
WBC2VSP is the vertical scaling parameter register.

Offset Address	Register Name	Total Reset Value
0x82CC	WBC2VSP	0x0000_0000



Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical brightness scaling enabled. 0: forbidden; 1: enable.
[30]	RW	vchmsc_en	Vertical chroma scaling enabled. 0: forbidden; 1: enable.
[29]	RW	vlmid_en	Vertical luma scaling median filter enable (this bit has no effect when vlfir_en is invalid). 0: forbidden; 1: enable.
[28]	RW	vchmid_en	Vertical chroma scaling median filter enable (this bit has no effect when vchfir_en is invalid). 0: forbidden; 1: enable.
[27]	RO	reserved	reserve.
[26]	RW	vsc_chroma_tap	Vertical chroma scaling order. 0: 4th order FIR; 1: 2nd order FIR.
[25]	RO	reserved	reserve.
[24]	RW	vlfir_en	Vertical brightness scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).
[23]	RW	vchfir_en	Vertical chroma scaling mode. 0: Copy mode (filter disabled); 1: Filter mode (filter enabled).

Offset Address	Register Name	Total Reset Value
0x82CC	WBC2VSP	0x0000_0000



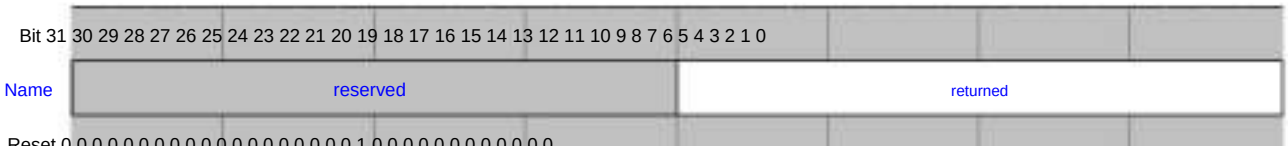
Bits	Access Name	Description
[22:21]	RW zme_out_fmt	Scaled output data format. 0ÿ420ÿ 1ÿ422ÿ
[20:19]	RW zme_in_fmt	Scale input data format. 0ÿ422ÿ Other: reserved.
[18:0]	RO reserved	reserve.

WBC2VSR

WBC2VSR is the Luma Vertical Scaling Ratio register. non-immediate registers.

Zoom ratio = input height/output height.

Offset Address	Register Name	Total Reset Value
0x82D0	WBC2VSR	0x0000_1000



Bits	Access Name	Description
[31:16]	RO reserved	reserve.
[15:0]	RW is back	Vertical scaling factor, in (u,4,12) format.

WBC2VOFFSET

WBC2VOFFSET is the Vertical Luma Offset register.

The vertical zoom offset is affected by two factors: pan-scan and field offset when repeating frames. When there is no field offset, vluma_offset is the lowest integer bit + decimal place of offset_pan-scan; in YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset = scaling_chroma/2-0.25. When a field offset is required (such as a static frame or a repeated frame), assuming that the bottom field is repeated, the vluma_offset and vchroma_offset of the top field configuration are the same as the above without offset, and the bottom field configuration needs to consider the field offset.

Offset Address	Register Name	Total Reset Value
0x82D4	WBC2VOFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	vluma_offset	vchroma_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW vluma_offset	Vertical brightness offset, complement representation, (s,4,12) format.
[15:0]	RW vchroma_offset	Vertical chroma offset, complement representation, (s,4,12) format.

WBC2ZMEORESO

WBC2ZMEORESO is the output resolution register of the scaling unit. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x82D8	WBC2ZMEORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:12]	RW oh	Height, unit: line. The actual height is minus 1. When progressive, the frame height is used as a reference, and the unit is row; when interlaced, the field height is used as a reference, and the unit is row.
[11:0]	RW ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

WBC2ZMEIRESO

WBC2ZMEIRESO is the I/O resolution register of the scaling unit. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x82DC	WBC2ZMEIRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them / iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, unit: line. The actual height is minus 1. When progressive, the frame height is used as a reference, and the unit is row; when interlaced, the field height is used as a reference, and the unit is row.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G0CTRL

G0CTRL is the G0 layer control register. This register can configure the related information register of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9000	G0CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	[illegible] / reserved	[illegible] / ifmt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	surface_en	surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:28]	RO	reserved	reserve.
[27]	RW	upd_mode	update mode. 0: frame update; 1: field update.

Offset Address	Register Name	Total Reset Value
0x9000	G0CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														reserved																	ifmt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[26]	RW	read_mode	Data read mode. 0: Automatically select according to the interface reading mode (read line by line when displaying line by line, read line by line when displaying interlaced); 1: Force to read line by line.
[25]	RW	dcmp_mode	Unzip mode. non-immediate registers. 0: Non-decompression mode; 1: Decompression mode.
[24]	RW	dcmp_inter	Interlaced decompression control, non-immediate registers. 0: decompress line by line; 1: Interlaced decompression.
[23:10]	RW	reserved	reserve.
[9:8]	RW	bitext	Layer input bitmap Bit Bit extension mode. 0X: Extend the low bit with 0; 10: Extend the highest bit with the low bit; 11: Extend the highest bit with the low bit.
[7:0]	RW	ifmt	Input data format. 0x49ÿARGB1555ÿ 0x68ÿARGB8888ÿ Other: reserved.

G0UPD

G0UPD is the graphics layer update enable register.

Offset Address	Register Name	Total Reset Value
0x9004	G0UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

G0ADDR

G0ADDR is the graphics layer address register. In the case of horizontal pixel offset, the address calculation refers to the description of G0SFPOS.

Offset Address	Register Name	Total Reset Value
0x9008	G0ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Surface frame buffer address.

G0STRIDE

G0STRIDE is the stride register of graphics layer.

Offset Address	Register Name	Total Reset Value
0x900C	G0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	ÿ	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x900C	G0STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	surface_stride	The stride of the frame buffer.

G0CBMPARA

G0CBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9010	G0CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	[illegible]				reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	key_mode	Color key mode 0: When Keyminÿ Pixel ÿ Keymax is satisfied, it will be processed as key color 1: When Pixel ÿ Keymin or Pixel ÿ Keymax is satisfied, it will be processed as key color
[14]	RW	key_en	color key enable. 0: forbidden; 1: enable.
[13]	RW	premult_en	The input bitmap is a premultiplied image. 0: non-premultiplied image; 1: Premultiplied map.
[12]	RW	palpha_en	Pixel alpha enabled. 0: forbidden; 1: enable.
[11:8]	RW	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x9010	G0CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved				reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[7:0]	RW galpha	Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

G0CKEYMAX

G0CKEYMAX is the color key maximum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9014	G0CKEYMAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wa0	keyr_max	keyg_max	keyb_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW of 0	alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, replace it with this value.
[23:16]	RW keyr_max	The maximum value of the colry key R component.
[15:8]	RW keyg_max	The maximum value of the color key G component.
[7:0]	RW keyb_max	Color key B component maximum value.

G0CKEYMIN

G0CKEYMIN is the color key minimum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9018	G0CKEYMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	va1	keyr_min	keyg_min	storage_min
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, replace it with this value.
[23:16]	RW	keyr_min	colry key R component minimum value.
[15:8]	RW	keyg_min	The minimum value of the color key G component.
[7:0]	RW	keyb_min	Color key B component minimum value.

G0CMASK

G0CMASK is the MASK value of the color key, which is a non-immediate register. If the corresponding bit is 0, it means that the bit is not concerned during the Key comparison process.

Offset Address	Register Name	Total Reset Value
0x901C	G0CMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	kmsk_r	kmsk_g	kmsk_b
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	kmsk_r	R component of the colry key mask.
[15:8]	RW	kmsk_g	The G component of the colry key mask.
[7:0]	RW	kmsk_b	The B component of the colry key mask.

G0IRESO

G0IRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9020	G0IRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G0ORESO

G0ORESO is the output resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9024	G0ORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G0DFPOS

G0DFPOS is the Surface's initial position (First POSition) register in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x902C	G0DFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_yfpos	disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G0DLPOS

G0DLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9030	G0DLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Line end coordinates.

G0CSCIDC

G0CSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x90A0	G0CSCIDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved	cscidc2	cscidc1	cscidc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access Name	Description
[31:28]	RO reserved	reserve.
[27]	RW csc_en	CSC is enabled. 0: disabled; 1: enable.
[26:18]	RW cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

G0CSCODC

G0CSCODC is the color space conversion output DC component register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90A4	G0CSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access Name	Description
[31:27]	RO reserved	reserve.
[26:18]	RW cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

G0CSCP0

G0CSCP0 is the color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90A8	G0CSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G0CSCP1

G0CSCP1 is the color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90AC	G0CSCP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp10	—	cscp02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G0CSCP2

G0CSCP2 is the color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90B0	G0CSCP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp12	—	cscp11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G0CSCP3

G0CSCP3 is the color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90B4	G0CSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x90B4	G0CSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G0CSCP4

G0CSCP4 is the color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x90B8	G0CSCP4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscp22
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G0DCMPBANKWIDTH

G0DCMPBANKWIDTH is the G0 layer compressed data bank width register.

Offset Address	Register Name	Total Reset Value
0x91B4	G0DCMPBANKWIDTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dcmp_bankwidth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	dcmp_bankwidth	Compressed data bank width, 128bit alignment.

G0DCMPSTRIDE

G0DCMPSTRIDE is the G0 layer compressed data stride register.

Offset Address	Register Name	Total Reset Value
0x91B8	G0DCMPSTRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dcmp_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	dcmp_stride	compressed data stride, 128bit alignment.

G0DCMPAADDR

G0DCMPAADDR is the start address register of compressed data of A component in G0 layer.

Offset Address	Register Name	Total Reset Value
0x91BC	G0DCMPAADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dcmp_addr_a	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	dcmp_addr_a	Compressed data start address.

G0DCMPRADDR

G0DCMPRADDR is the start address register of R component compressed data in G0 layer.

Offset Address	Register Name	Total Reset Value
0x91C0	G0DCMPRADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_r																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dcmp_addr_r	Compressed data start address.

G0DCMPGADDR

G0DCMPGADDR is the G0 layer G component compressed data start address register.

Offset Address	Register Name	Total Reset Value
0x91C4	G0DCMPGADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_g																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dcmp_addr_g	Compressed data start address.

G0DCMPBADDR

G0DCMPBADDR is the start address register of B component compressed data in G0 layer.

Offset Address	Register Name	Total Reset Value
0x91C8	G0DCMPBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_addr_b																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dcmp_addr_b	Compressed data start address.

G2CTRL

G2CTRL is the G2 layer control register. This register can configure the related information register of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9400	G2CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reserved																										ifmt		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31]	RW surface_en	surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:28]	RO reserved	reserve.
[27]	RW upd_mode	update mode. 0: frame update; 1: field update.
[26]	RW read_mode	Data read mode. 0: Automatically select according to the interface reading mode (read line by line when displaying line by line, read line by line when displaying interlaced); 1: Force to read line by line.
[25:10]	RW reserved	reserve.
[9:8]	RW bitext	Layer input bitmap Bit Bit extension mode. 0X: Extend the low bit with 0; 10: Extend the highest bit with the low bit; 11: Extend the highest bit with the low bit.
[7:0]	RW ifmt	Input data format. 0x49ÿARGB1555ÿ 0x68ÿARGB8888ÿ Other: reserved.

G2UPD

G2UPD Update enable register for graphics layer.

Offset Address	Register Name	Total Reset Value
0x9404	G2UPD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1] RO	reserved	reserve.
[0] RW regup		The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

G2ADDR

G2ADDR is the graphics layer address register. In the case of horizontal pixel offset, refer to the G2SFPOS description for address calculation.

Offset Address	Register Name	Total Reset Value
0x9408	G2ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	surface_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RW surface_addr		Surface frame buffer address.

G2STRIDE

G2STRIDE is the stride register of graphics layer.

Offset Address	Register Name	Total Reset Value
0x940C	G2STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	ÿ	reserved	reserve.
[15:0]	RW	surface_stride	The stride of the frame buffer.

G2CBMPARA

G2CBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9410	G2CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	key_mode	color key mode. 0: When Keymin ÿ Pixel ÿ Keymax is satisfied, it will be processed as key color 1: When Pixel ÿ Keymin or Pixel ÿ Keymax is satisfied, it will be processed as key color
[14]	RW	key_en	color key enable. 0: forbidden; 1: enable.
[13]	RO	reserved	reserve.
[12]	RW	palpha_en	Pixel alpha enabled. 0: forbidden; 1: enable.
[11:8]	RW	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x9410	G2CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved [illegible] reserved alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[7:0]	RW galpha	Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

G2CKEYMAX

G2CKEYMAX is the color key maximum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9414	G2CKEYMAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wa0 keyr_max keyg_max keyb_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW of 0	alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, replace it with this value.
[23:16]	RW keyr_max	The maximum value of the colry key R component.
[15:8]	RW keyg_max	The maximum value of the color key G component.
[7:0]	RW keyb_max	Color key B component maximum value.

G2CKEYMIN

G2CKEYMIN is the color key minimum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9418	G2CKEYMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	va1	keyr_min	keyg_min	storage_min
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW va1	alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, replace it with this value.
[23:16]	RW keyr_min	colry key R component minimum value.
[15:8]	RW keyg_min	The minimum value of the color key G component.
[7:0]	RW keyb_min	Color key B component minimum value.

G2CMASK

G2CMASK is the MASK value of the color key, which is a non-immediate register. If the corresponding bit is 0, it means that the bit is not concerned during the Key comparison process.

Offset Address	Register Name	Total Reset Value
0x941C	G2CMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	kmsk_r	kmsk_g	kmsk_b
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:16]	RW kmsk_r	R component of the colry key mask.
[15:8]	RW kmsk_g	The G component of the colry key mask.
[7:0]	RW kmsk_b	The B component of the colry key mask.

G2IRESO

G2IRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9420	G2IRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G2ORESO

G2ORESO is the output resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9424	G2ORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. Progressive output has no such limitation.
[11:0]	RW	ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G2DFPOS

G2DFPOS is the Surface's initial position (First POSition) register in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x942C	G2DFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_yfpos	disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G2DLPOS

G2DLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9430	G2DLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Line end coordinates.

G2CSCIDC

G2CSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x94A0	G2CSCIDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscidc2	cscidc1 cscidc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:28]	RO reserved	reserve.
[27]	RW csc_en	CSC is enabled. 0: disabled; 1: enable.
[26:18]	RW cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

G2CSCODC

G2CSCODC is the G2 layer color space conversion output DC component register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94A4	G2CSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1 cscodc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:27]	RO reserved	reserve.
[26:18]	RW cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

G2CSCP0

G2CSCP0 is the G2 layer color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94A8	G2CSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G2CSCP1

G2CSCP1 is the G2 layer color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94AC	G2CSCP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp10	—	cscp02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G2CSCP2

G2CSCP2 is the G2 layer color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94B0	G2CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							cscp12									—									cscp11						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G2CSCP3

G2CSCP3 is the G2 layer color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94B4	G2CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							cscp21									—									cscp20						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x94B4	G2CSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G2CSCP4

G2CSCP4 is the G2 layer color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x94B8	G2CSCP4	0x0000_0000

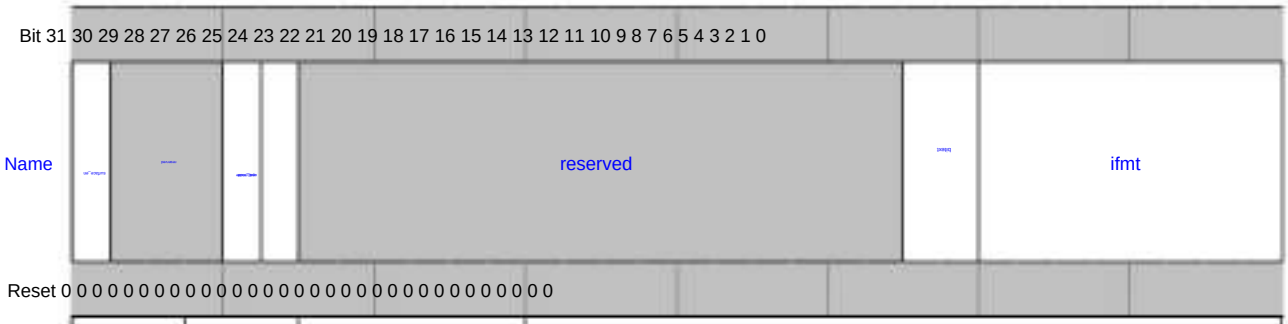
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscp22
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G3CTRL

G3CTRL is the G3 layer control register. This register can configure the related information register of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9600	G3CTRL	0x0000_0000



Bits	Access Name	Description
[31] RW surface_en		surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:28] RO	reserved	reserve.
[27] RW upd_mode		update mode. 0: frame update; 1: field update.
[26] RW read_mode		Data read mode. 0: Automatically select according to the interface reading mode (read line by line when displaying line by line, read line by line when displaying interlaced); 1: Force to read line by line.
[25:10] RO	reserved	reserve.
[9:8] RW bitext		Layer input bitmap Bit Bit extension mode. 0X: Extend the low bit with 0; 10: Extend the highest bit with the low bit; 11: Extend the highest bit with the low bit.
[7:0] RW ifmt		Input data format. 0x49ÿARGB1555ÿ 0x68ÿARGB8888ÿ Other: reserved.

G3UPD

G3UPD Update enable register for graphics layer.

Offset Address	Register Name	Total Reset Value
0x9604	G3UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

G3ADDR

G3ADDR is the graphics layer address register. In the case of horizontal pixel offset, refer to the G3SFPOS description for address calculation.

Offset Address	Register Name	Total Reset Value
0x9608	G3ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Surface frame buffer address.

G3STRIDE

G3STRIDE is the stride register of graphics layer.

Offset Address	Register Name	Total Reset Value
0x960C	G3STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	ÿ	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x960C	G3STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	surface_stride	The stride of the frame buffer.

G3CBMPARA

G3CBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9610	G3CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	key_mode	key_en	premult_en	palpha_en	reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	key_mode	Color key mode 0: when Keymin <= Pixel <= Keymax is satisfied, it is processed as a key color 1: when Pixel <= Keymin or Pixel >= Keymax is satisfied, it is processed as a key color
[14]	RW	key_en	color key enable. 0: disable; 1: enable.
[13]	RW	premult_en	The input bitmap is a premultiplied image. 0: non-premultiplied image; 1: Premultiplied map.
[12]	RW	palpha_en	Pixel alpha enabled. 0: forbidden; 1: enable.
[11:8]	RW	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x9610	G3CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved				reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[7:0]	RW galpha	Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

G3CKEYMAX

G3CKEYMAX is the color key maximum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9614	G3CKEYMAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wa0	keyr_max	keyg_max	keyb_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW of 0	alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, replace it with this value.
[23:16]	RW keyr_max	The maximum value of the colry key R component.
[15:8]	RW keyg_max	The maximum value of the color key G component.
[7:0]	RW keyb_max	Color key B component maximum value.

G3CKEYMIN

G3CKEYMIN is the color key minimum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9618	G3CKEYMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	va1	keyr_min	keyg_min	storage_min
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW va1	alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, replace it with this value.
[23:16]	RW keyr_min	colry key R component minimum value.
[15:8]	RW keyg_min	The minimum value of the color key G component.
[7:0]	RW keyb_min	Color key B component minimum value.

G3CMASK

G3CMASK is the MASK value of the color key, which is a non-immediate register. If the corresponding bit is 0, it means that the bit is not concerned during the Key comparison process.

Offset Address	Register Name	Total Reset Value
0x961C	G3CMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	kmsk_r	kmsk_g	kmsk_b
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:16]	RW kmsk_r	The R component of the colry key mask.
[15:8]	RW kmsk_g	The G component of the colry key mask.
[7:0]	RW kmsk_b	The B component of the colry key mask.

G3IRESO

G3IRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9620	G3IRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G3ORESO

G3ORESO is the output resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9624	G3ORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	ow	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G3DFPOS

G3DFPOS is the Surface's initial position (First POSition) register in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x962C	G3DFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_yfpos	disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G3DLPOS

G3DLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9630	G3DLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Line end coordinates.

G3CSCIDC

G3CSCIDC Input DC component register for G3 layer color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x96A0	G3CSCIDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved	cscidc2	cscidc1	cscidc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	csc_en	CSC is enabled. 0: disabled; 1: enable.
[26:18]	RW	cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

G3CSCODC

G3CSCODC is the G3 layer color space conversion output DC component register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96A4	G3CSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:18]	RW	cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

G3CSCP0

G3CSCP0 is the G3 color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96A8	G3CSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G3CSCP1

G3CSCP1 is the G3 layer color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96AC	G3CSCP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp10	—	cscp02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G3CSCP2

G3CSCP2 is the G3 layer color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96B0	G3CSCP2	0x0000_0000

Bit	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp12	—	cscp11
Reset	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G3CSCP3

G3CSCP3 is the G3 layer color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96B4	G3CSCP3	0x0000_0000

Bit	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x96B4	G3CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							cscp21									—											cscp20					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

G3CSCP4

G3CSCP4 is the G3 layer color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x96B8	G3CSCP4	0x0000_0000

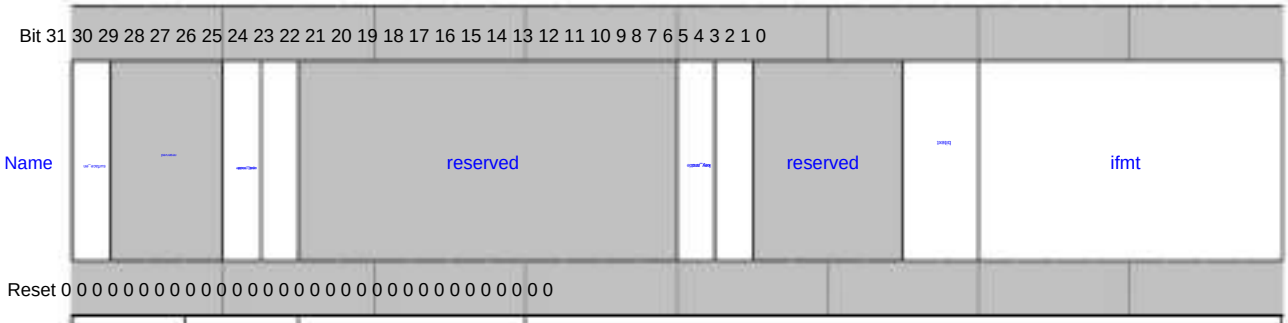
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													cscp22		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

HCCTRL

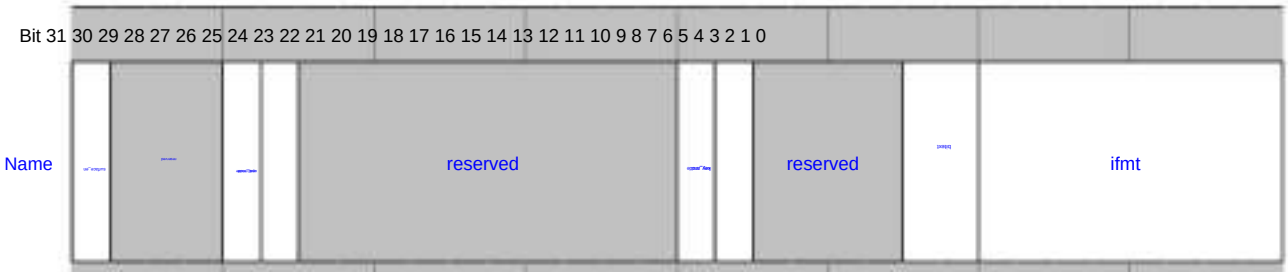
HCCTRL is the HC layer control register. This register can configure the related information register of the layer. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A00	HCCTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	surface_en	surface is enabled. non-immediate registers. 0: forbidden; 1: enable.
[30:28]	RO	reserved	reserve.
[27]	RW	upd_mode	update mode. 0: frame update; 1: field update.
[26]	RW	read_mode	Data read mode. 0: Automatically select according to the interface reading mode (read line by line when displaying line by line, read line by line when displaying interlaced); 1: Force to read line by line.
[25:16]	RO	reserved	reserve.
[15]	RW	key_mode	Color key mode 0: When Keymin <= Pixel <= Keymax is satisfied, it is processed as a key color 1: When Pixel <= Keymin or Pixel >= Keymax is satisfied, it is processed as a key color
[14]	RW	key_en	color key enable. 0: forbidden; 1: enable.
[13:10]	RW	reserved	reserve.
[9:8]	RW	bitext	Layer input bitmap Bit Bit extension mode. 0X: low bit extension 0; 10: The lower bit extends the highest bit; 11: The lower bit extends the highest bit.

Offset Address	Register Name	Total Reset Value
0x9A00	HCCTRL	0x0000_0000

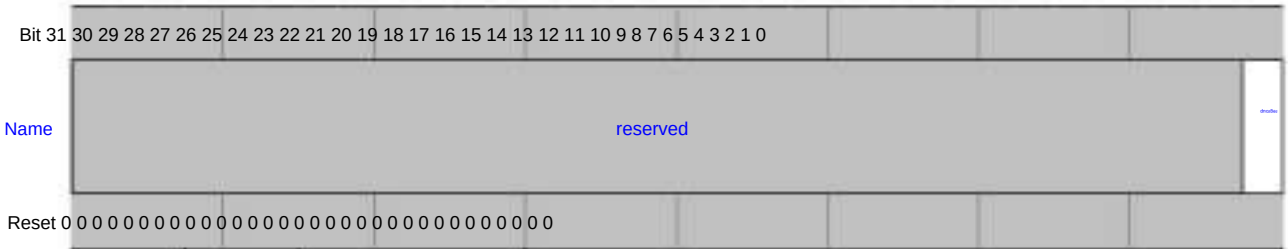


Bits	Access	Name	Description
[7:0]	RW	ifmt	Input data format. 0x49ÿARGB1555ÿ 0x68ÿARGB8888ÿ Other: reserved.

HCUPD

HCUPD Update enable register for graphics layer.

Offset Address	Register Name	Total Reset Value
0x9A04	HCUPD	0x0000_0000



Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

HCADDR

HCADDR is the graphics layer address register. In the case of horizontal pixel offset, address calculation refers to HCSFPOS description.

Offset Address	Register Name	Total Reset Value
0x9A08	HCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	surface_addr	Surface frame buffer address.

HCSTRIDE

HCSTRIDE is the stride register of graphics layer.

Offset Address	Register Name	Total Reset Value
0x9A0C	HCSTRIDE	0x0000_0000

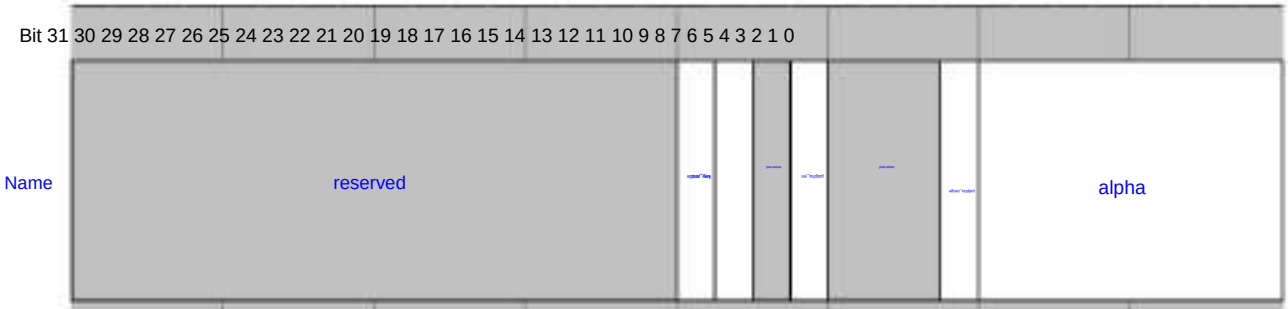
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	ÿ	reserved	reserve.
[15:0]	RW	surface_stride	The stride of the frame buffer.

HCCBMPARA

HCCBMPARA is the overlay related parameter register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A10	HCCBMPARA	0x0000_0000



Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15]	RW	key_mode	color key mode. 0: When Keymin <= Pixel <= Keymax is met, it will be treated as key color; 1: When Pixel <= Keymin or Pixel >= Keymax is met, it will be treated as key color.
[14]	RW	key_en	color key enable. 0: forbidden; 1: enable.
[13]	ÿ	reserved	The input bitmap is a premultiplied image. 0: non-premultiplied image; 1: Premultiplied map.
[12]	RW	palpha_en	Pixel alpha enabled. 0: forbidden; 1: enable.
[11:9]	ÿ	reserved	reserve.
[8]	RW	palpha_range	0: indicates that the alpha range of the pixel is 0~128; 1: Indicates that the alpha range of the pixel is 0~255.
[7:0]	RW	galpha	Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

HCCKEYMAX

HCCKEYMAX is the color key maximum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A14	HCCKEYMAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wa0	keyr_max	keyg_max	keyb_max
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW of 0	alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, replace it with this value.
[23:16]	RW keyr_max	The maximum value of the colry key R component.
[15:8]	RW keyg_max	The maximum value of the color key G component.
[7:0]	RW keyb_max	Color key B component maximum value.

HCCKEYMIN

HCCKEYMIN is the color key minimum value register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A18	HCCKEYMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	va1	keyr_min	keyg_min	storage_min
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW va1	alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, replace it with this value.
[23:16]	RW keyr_min	colry key R component minimum value.
[15:8]	RW keyg_min	The minimum value of the color key G component.
[7:0]	RW keyb_min	Color key B component minimum value.

HCCMASK

HCCMASK is the color key minimum value register. non-immediate registers. If the corresponding bit is 1, it means that the bit is not concerned during the Key comparison process.

Offset Address	Register Name	Total Reset Value
0x9A1C	HCCMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	kmsk_r	kmsk_g	kmsk_b
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	kmsk_r	R component of the colry key mask.
[15:8]	RW	kmsk_g	The G component of the colry key mask.
[7:0]	RW	kmsk_b	The B component of the colry key mask.

HCIRESO

HCIRESO is the input resolution register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A20	HCIRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	them		iw
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	iw	Width, unit: pixel. The actual width is minus 1. Note: The actual width of the layer must be an even number.

HCDFPOS

HCDFPOS is the Surface's initial position (First POSition) register in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A2C	HCDFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	disp_yfpos / disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

HCDLPOS

HCDLPOS is the last position (Last POSition) register of Surface in the display window. in pixels. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9A30	HCDLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	disp_ylpos / disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Line end coordinates.

HCCSCIDC

HCCSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AA0	HCCSCIDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscidc2	cscidc1	cscidc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:29]	RO reserved	reserve.
[28]	RW csc_mode	CSC conversion mode. 0: RGB2YUV 601 (SD); 1: RGB2YUV 709 (g HD).
[27]	RW csc_en	CSC is enabled. 0: disabled; 1: enable.
[26:18]	RW cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

HCCSCODC

HCCSCODC Output DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AA4	HCCSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:27]	RO reserved	reserve.
[26:18]	RW cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

HCCSCP0

HCCSCP0 is the color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AA8	HCCSCP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

HCCSCP1

HCCSCP1 is the color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AAC	HCCSCP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp10	—	cscp02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x9AAC	HCCSCP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	-	cscp10	-	cscp02
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

HCCSCP2

HCCSCP2 is the color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AB0	HCCSCP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	-	cscp12	-	cscp11
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

HCCSCP3

HCCSCP3 is the color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AB4	HCCSCP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp21	—	cscp20
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

HCCSCP4

HCCSCP4 is the color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0x9AB8	HCCSCP4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscp22
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

CBMBKG1

CBMBKG1 is the overlay background color register for HD0.

Offset Address	Register Name	Total Reset Value
0x9E00	CBMBKG1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cbm_bkgy	cbm_bkgcb	cbm_bkgcr
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	cbm_bkgy	Mixer1 overlay background color, Y component.
[15:8]	RW	cbm_bkgcb	Mixer1 Overlay background color, Cb component.
[7:0]	RW	cbm_bkgcr	Mixer1 Overlay background color, Cr component.

CBMBKG3

CBMBKG3 is the overlay background color register for SD0.

Offset Address	Register Name	Total Reset Value
0x9E08	CBMBKG3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cbm_bkgy	cbm_bkgcb	cbm_bkgcr
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	cbm_bkgy	Mixer3 overlay background color, Y component.
[15:8]	RW	cbm_bkgcb	Mixer3 Overlay background color, Cb component.
[7:0]	RW	cbm_bkgcr	Mixer3 overlay background color, Cr component.

CBMBKG4

CBMBKG4 is the overlay background color register for SD1.

Offset Address	Register Name	Total Reset Value
0x9E0C	CBMBKG4	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cbm_bkgy	cbm_bkgcb	cbm_bkgcr
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	cbm_bkgy	Mixer4 overlay background color, Y component.
[15:8]	RW	cbm_bkgcb	Mixer4 Overlay background color, Cb component.
[7:0]	RW	cbm_bkgcr	Mixer4 superimposed background color, Cr component.

CBMATTR

CBMATTR is a configuration register for CrossBar (Cross Bar ConFiGuration).

sur_attr_x indicates whether layer x is connected to Mixer1 or Mixer2.

Offset Address	Register Name	Total Reset Value
0x9E10	CBMATTR	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
Name	reserved	on_attr1	on_attr0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	on_attr1	HC0 link. 0x0ÿMixer1 for DHDÿ 0x1ÿMixer3 for DSDÿ 0x2ÿMixer4 for DSD1ÿ Other: reserved.
[3:0]	RW	on_attr0	VSD link. 0x0ÿMixer1 for DHDÿ 0x1ÿMixer3 for DSDÿ Other: reserved

CBMMIX1

CBMMIX1 is the priority configuration register for Mixer1. Updates are valid at vsync. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0x9E14	CBMMIX1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:12]	RW	mixer_prio3	Overlay priority configuration for Mixer1, representing a priority 3 driver layer. 0x0: means no layer driver; 0x1ÿvhdÿ 0x4ÿvsdÿ 0x9ÿg0ÿ 0xeÿHC0 Other: reserved.
[11:8]	RW	mixer_prio2	Overlay priority configuration for Mixer1, representing a priority 2 driver layer. 0x0: means no layer driver; 0x1ÿvhdÿ 0x4ÿvsdÿ 0x9ÿg0ÿ 0xeÿHC0 Other: reserved.
[7:4]	RW	mixer_prio1	Overlay priority configuration for Mixer1, representing a priority 1 driver layer. 0x0: means no layer driver; 0x1ÿvhdÿ 0x4ÿvsdÿ 0x9ÿg0ÿ 0xeÿHC0 Other: reserved.

Offset Address	Register Name	Total Reset Value
0x9E14	CBMMIX1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	mixer_prio3	mixer_prio2	mixer_prio1	mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[3:0]	RW	mixer_prio0	Overlay priority configuration for Mixer1, representing a priority 0 driver layer. 0x0: means no layer driver; 0x1ÿvhdÿ 0x4ÿvsdÿ 0x9ÿg0ÿ 0xeÿHC0 Other: reserved.

CBMMIX3

CBMMIX3 is the Mixer3 priority configuration register. Updates are valid at vsync.

This register is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x9E1C	CBMMIX3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		mixer_prio2	mixer_prio1	mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	mixer_prio2	Overlay priority configuration for Mixer3, representing a priority 2 driver layer. 0x0: means no layer driver; 0x4ÿvsdÿ 0xbÿg2ÿ 0xeÿHC0ÿ Other: reserved.

Offset Address	Register Name	Total Reset Value
0x9E1C	CBMMIX3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved mixer_prio2 mixer_prio1 mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[7:4]	RW	mixer_prio1	Overlay priority configuration for Mixer3, representing a priority 1 driver layer. 0x0: means no layer driver; 0x4ÿvsdÿ 0xbÿg2ÿ 0xeÿHC0ÿ Other: reserved.
[3:0]	RW	mixer_prio0	Overlay priority configuration for Mixer3, representing a priority 0 driver layer. 0x0: means no layer driver; 0x4ÿvsdÿ 0xbÿg2ÿ 0xeÿHC0ÿ Other: reserved.

CBMMIX4

CBMMIX4 is the Mixer4 priority configuration register. Updates are valid at vsync.

This register is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x9E20	CBMMIX4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved mixer_prio2 mixer_prio1 mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x9E20	CBMMIX4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved mixer_prio2 mixer_prio1 mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[11:8]	RW	mixer_prio2	Overlay priority configuration, representing a priority 2 driver layer. 0x0: no layer driver; 0x5ÿvsd1ÿ 0xcÿg3ÿ 0xeÿHC0ÿ Other: reserved.
[7:4]	RW	mixer_prio1	Overlay priority configuration, representing a priority 1 driver layer. 0x0: means no layer driver; 0x5ÿvsd1ÿ 0xcÿg3ÿ 0xeÿHC0ÿ Other: reserved.
[3:0]	RW	mixer_prio0	Overlay priority configuration, representing a priority 0 driver layer. 0x0: no layer driver; 0x5ÿvsd1ÿ 0xcÿg3ÿ 0xeÿHC0ÿ Other: reserved.

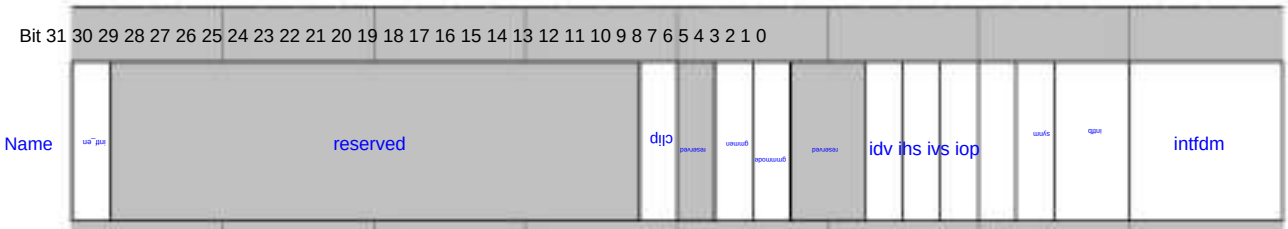
DHDCTRL

DHDCTRL is the overall control register of the display channel.

注意

The configuration of all bits of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA000	DHDCTRL	0x0001_0010



Bits	Access	Name	Description
[31]	RW	intf_en	Displays whether the interface is enabled. When enabled, the interface will output. Instant register. 0: forbidden; 1: enable.
[30:17]	RO	reserved	reserve.
[16]	RW	clipen	Output clamp enable, immediate register. 0: forbidden; 1: enable.
[15:11]	RO	reserved	reserve.
[10]	RW	idv	Data valid signal output inversion enable, immediate register. 0: forbidden; 1: enable.
[9]	RW	ihs	Horizontal sync pulse output inverting enable, immediate register. 0: forbidden; 1: enable.
[8]	RW	ivs	Vertical sync pulse output inversion enable, immediate register. 0: forbidden; 1: enable.
[7]	RW	iop	Progressive or interlaced display, instant register. 0: Interlaced display; 1: Display line by line.
[6]	RW	syn	Synchronous mode, immediate registers. 0: Timing label mode (such as BT.656); 1: Synchronous signal mode (such as LCD display).

Offset Address	Register Name	Total Reset Value
0xA000	DHDCTRL	0x0001_0010

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: intf_en | reserved | clip | reserved | gmmmode | reserved | idv ihs ivs iop | sync | intb | intfdm

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[5:4]	RW	intfb	Output interface bit width mode. Instant register. 00: Single component mode (1 component per clock output); 01: 2 component mode (2 components per clock output); 10: 3 component mode (3 components per clock output); 11: Reserved.
[3:0]	RW	intfdm	Interface data format. Instant register. 0x0: YCbCr422 data format; 0x1~0xB: invalid; 0xC: RGB888/YCbCr444 output. Other: invalid.

DHDVSYNC

DHDVSYNC is the vertical timing register. When interlaced output, this register indicates the vertical synchronization timing of the top field; when outputting progressively, this register indicates the vertical synchronization timing of the frame. This register takes effect immediately after configuration, and will immediately affect the timing of the pin VSYNC.

注意

The configuration of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA004	DHDVSYNC	0x0011_321B

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vfb	vbb	vact
Reset	0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 1 1 0 0 1	0 0 0 0 1 0 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	vfb	For interlaced output: top field vertical blanking front porch; for progressive output: vertical blanking front porch. Unit: row.
[19:12]	RW	etc	For interlaced output: top field vertical blanking back porch; When outputting line by line: the width of the vertical pulse is added to the shoulder after the vertical blanking. Unit: row.
[11:0]	RW	vact	For interlaced output: the height of the active image of the top field; for progressive output: the height of an active image for one frame. The value of this register is minus 1 from the actual value. Unit: row.

DHDHSYNC1

DHDHSYNC1 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA008	DHDHSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal blanking back shoulder, unit: pixel.
[15:0]	RW	hact	The number of horizontal pixels in the active area.

DHDHSYNC2

DHDHSYNC2 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA00C	DHDHSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:16]	RW	Hamid	Bottom field vertical sync valid pixel value (valid data area).
[15:0]	RW	hfb	Horizontal blanking front shoulder, in pixels.

DHDVPLUS

DHDVPLUS is the interlaced bottom field vertical timing register. For interlaced output, this register indicates the vertical sync timing of the bottom field.

注意

The configuration of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA010	DHDVPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							bvfb										bvbb										bvact				
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access Name	Description
[31:28]	RO reserved	reserve.
[27:20]	RW bvfb	For interlaced output: Bottom field vertical blanking front porch. Unit: row
[19:12]	RW bvbb	For interlaced output: the width of the vertical pulse of the porch after the vertical blanking of the bottom field. Unit: line
[11:0]	RW bvact	For interlaced output: the height of the active image in the bottom field. The value of this register is minus 1 from the actual value. Unit: line

DHDPWR

DHDPWR is the sync signal pulse width register.

注意

The configuration of this register must be no later than DHDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA014	DHDPWR	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vpw	hpw
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	vpw	The vertical pulse width is minus 1. Unit: pixel.
[15:0]	RW	hpw	Subtract 1 from the horizontal pulse width. Unit: pixel.

DHDVTTHD

DHDVTTHD is the Vertical Timing Threshold register. Instant register. This register contains two threshold configurations, which can generate two interrupts independently.

Offset Address	Register Name	Total Reset Value
0xA01C	DHDVTTHD	0x0000_0001

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		vtmgthd1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	thd1_mode	Threshold 1 Mode for interrupt generation. 0: Frame mode, threshold counting is performed in units of frames; 1: Field mode, threshold counting is performed in units of fields in interlaced display.
[14:13]	RO	reserved	reserve.
[12:0]	RW	vtmgthd1	The vertical timing threshold value is 1, when the vertical timing counter reaches the threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHDCLIPL

DHDCLIPL handles the lowest threshold register for the display channel Clip. Instant register.

Offset Address	Register Name	Total Reset Value
0xA040	DHDCLIPL	0x4100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipcl2														clipcl1												clipcl0			
Reset	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access Name	Description
[31] RW clipen		CLIP enabled. 0: forbidden; 1: enable.
[30] RW dfir_en		Chroma level downsampling enable signal. 0: forbidden; 1: enable.
[29:20] RW clipcl2		Component 2 Minimum threshold value Y/R, unsigned integer.
[19:10] RW clipcl1		Component 1 is the lowest threshold Cb/G, an unsigned integer.
[9:0] RW clipcl0		Component 0 is the lowest threshold Cr/B, an unsigned integer.

HDCLIP

DHDCLIPH Handles the highest threshold value register for the display channel Clip. Instant register. For example: when BT.656 standard output, CLIP processing is required for the output data.

Offset Address	Register Name	Total Reset Value
0xA044	HDCLIP	0x0EB0_00F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipch2														clipch1												clipch0			
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access Name	Description
[31:30] RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xA044	HDCLIP	0x0EB0_00F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clipch2										clipch1										clipch0							
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[29:20]	RW	clipch2	Component 2 The highest threshold Y/R, an unsigned integer.
[19:10]	RW	clipch1	Component 1 is the highest threshold Cb/G, an unsigned integer.
[9:0]	RW	clipch0	Component 0 is the highest threshold Cr/B, an unsigned integer.

DHDVGACLIPL

DHDVGACLIPL is the lowest threshold value register for display channel Clip processing, and it is an immediate register.

Offset Address	Register Name	Total Reset Value
0xA060	DHDVGACLIPL	0x4401_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clip	reserved			clipcl2										clipcl1										clipcl0							
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clipen	CLIP enabled. 0: forbidden; 1: enable.
[30]	RO	reserved	reserve.
[29:20]	RW	clipcl2	Component 2 Minimum threshold value Y/R, unsigned integer.
[19:10]	RW	clipcl1	Component 1 is the lowest threshold Cb/G, an unsigned integer.
[9:0]	RW	clipcl0	Component 0 is the lowest threshold Cr/B, an unsigned integer.

DHDVGA CLIPH

DHDVGACLIPH is the highest threshold value register for display channel Clip processing, and it is an immediate register. For example BT.656 standard output needs to do CLIP processing on the output data.

Offset Address	Register Name	Total Reset Value
0xA064	DHDVGA CLIPH	0x3ACF_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—			clipch2													clipch1												clipch0				
Reset	0	0	1	1	1	0	1	0	1								1	0	0	1									1	0	0	0	0	0	0

Bits	Access Name	Description
[31:30]	RO reserved	reserve.
[29:20]	RW clipch2	Component 2 The highest threshold Y/R, an unsigned integer.
[19:10]	RW clipch1	Component 1 is the highest threshold Cb/G, an unsigned integer.
[9:0]	RW clipch0	Component 0 is the highest threshold Cr/B, an unsigned integer.

DHDHSPCFG0

DHDHSPCFG0 is VGA channel H sharpen configuration register 0.

Offset Address	Register Name	Total Reset Value
0xA080	DHDHSPCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf0_tmp3								hsp_hf0_tmp2								hsp_hf0_tmp1								hsp_hf0_tmp0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:24]	RW hsp_hf0_tmp3	High frequency filter coefficient 3, signed.
[23:16]	RW hsp_hf0_tmp2	High frequency filter coefficient 2, signed.
[15:8]	RW hsp_hf0_tmp1	High frequency filter coefficient 1, signed.
[7:0]	RW hsp_hf0_tmp0	High frequency filter coefficient 0, signed.

DHDHSPCFG1

DHDHSPCFG1 is VGA channel H sharpen configuration register 1.

Offset Address	Register Name	Total Reset Value
0xA084	DHDHSPCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																													hsp_hf0_coring	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_en	Horizontal sharpening enabled.
[30:8]	RO	reserved	reserve.
[7:0]	RW	hsp_hf0_coring	High frequency coring coefficient, unsigned.

DHDHSPCFG5

DHDHSPCFG5 configures register 5 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA094	DHDHSPCFG5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							hsp_hf0_gainneg									reserved				hsp_hf0_gainpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	hsp_hf0_gainneg	High frequency gain negative polarity coefficient, signed (10.8).
[15:11]	RO	reserved	reserve.
[10:0]	RW	hsp_hf0_gainpos	High frequency gain positive polarity coefficient, signed (10.8).

DHDHSPCFG6

DHDHSPCFG6 Configure register 6 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA098	DHDHSPCFG6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]			reserved										hsp_hf0_mixratio									hsp_hf0_underth								hsp_hf0_overth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_hf0_adpshoot_ High in	frequency adjustment threshold enable.
[30:28]	RW	hsp_hf0_winsize	High frequency window size, unsigned, value range 0-4.
[27:24]	RO	reserved	reserve.
[23:16]	RW	hsp_hf0_mixratio	High frequency adjustment threshold ratio, unsigned (8.7).
[15:8]	RW	hsp_hf0_underth	High frequency adjustment under threshold, unsigned.
[7:0]	RW	hsp_hf0_overth	High frequency adjustment over threshold, unsigned.

DHDHSPCFG7

DHDHSPCFG7 Configure register 7 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA09C	DHDHSPCFG7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf1_tmp3								hsp_hf1_tmp2								hsp_hf1_tmp1								hsp_hf1_tmp0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	hsp_hf1_tmp3	High frequency filter coefficient 3, signed.
[23:16]	RW	hsp_hf1_tmp2	High frequency filter coefficient 2, signed.
[15:8]	RW	hsp_hf1_tmp1	High frequency filter coefficient 1, signed.
[7:0]	RW	hsp_hf1_tmp0	High frequency filter coefficient 0, signed.

DHDHSPCFG8

DHDHSPCFG8 configures register 8 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA0A0	DHDHSPCFG8	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / hsp_hf1_coring
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hsp_hf1_coring	High frequency coring coefficient, unsigned.

DHDHSPCFG12

DHDHSPCFG12 configures register 12 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA0B0	DHDHSPCFG12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / hsp_hf1_gainneg / reserved / hsp_hf1_gainpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	hsp_hf1_gainneg	High frequency gain negative polarity coefficient, signed (10.8).
[15:11]	RW	reserved	reserve.
[10:0]	RW	hsp_hf1_gainpos	High frequency gain positive polarity coefficient, signed (10.8).

DHDHSPCFG13

DHDHSPCFG13 configures register 13 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA0B4	DHDHSPCFG13	0x0000_0000

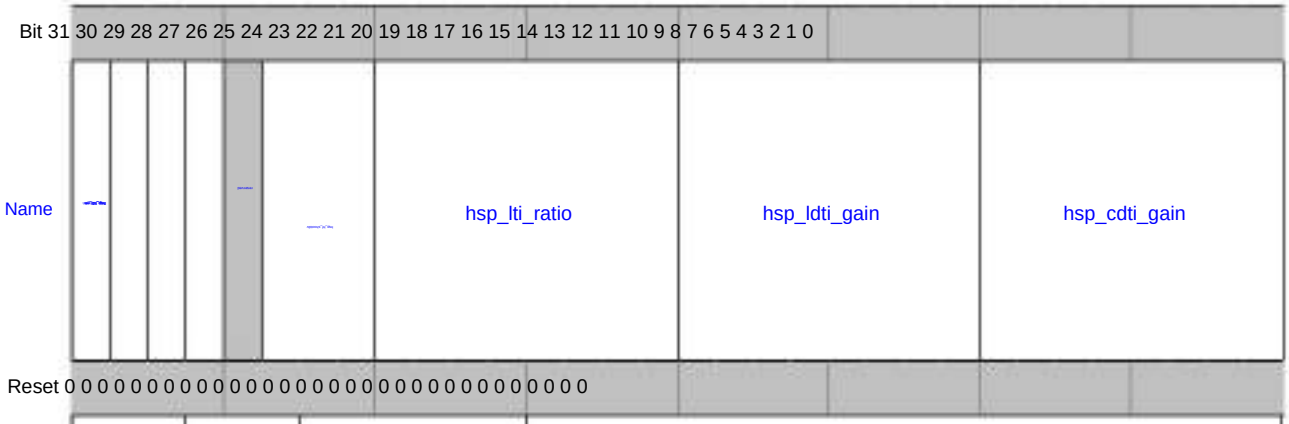
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reserved														hsp_hf1_mixratio								hsp_hf1_underth							hsp_hf1_overth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_hf1_adpshoot_ in	High frequency adjustment threshold enable.
[30:28]	RW	hsp_hf1_winsize	High frequency window size, unsigned, value range 0-4.
[27:24]	RO	reserved	reserve.
[23:16]	RW	hsp_hf1_mixratio	High frequency adjustment threshold ratio, unsigned (8.7).
[15:8]	RW	hsp_hf1_underth	High frequency adjustment under threshold, unsigned.
[7:0]	RW	hsp_hf1_overth	High frequency adjustment over threshold, unsigned.

DHDHSPCFG14

DHDHSPCFG14 Configure register 14 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA0B8	DHDHSPCFG14	0x0000_0000



Bits	Access	Name	Description
[31]	RW	hsp_h0_en	High frequency filter 0 enable.
[30]	RW	hsp_h1_en	High frequency filter 1 enable.
[29]	RW	hsp_ltih_en	Horizontal LTI enable.
[28]	RW	hsp_ctih_en	Horizontal CTI enable.
[27]	RO	reserved	reserve.
[26:24]	RW	hsp_hf_shootdiv	High frequency adjustment shift coefficient, unsigned, value range 1-7.
[23:16]	RW	hsp_lti_ratio	Luminance enhancement ratio, unsigned (8.7).
[15:8]	RW	hsp_ldti_gain	Luminance enhancement gain factor, unsigned (8.5).
[7:0]	RW	hsp_cdti_gain	Chroma enhancement gain factor, unsigned (8.5).

DHDHSPCFG15

DHDHSPCFG15 Configure register 15 for VGA channel H sharpen.

Offset Address	Register Name	Total Reset Value
0xA0BC	DHDHSPCFG15	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19	18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	hsp_peak_ratio	...	hsp_glb_overth	... hsp_glb_underth
Reset	0 0 0 0	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	hsp_peak_ratio	Brightness boost ratio, unsigned (8.7).
[19]	RO	reserved	reserve.
[18:10]	RW	hsp_glb_overth	Brightness boost global high threshold, unsigned.
[9]	RO	reserved	reserve.
[8:0]	RW	hsp_glb_underth	Luminance enhancement global underthreshold, unsigned.

DHDSTATE

DHDSTATE is the DHD status register.

Offset Address	Register Name	Total Reset Value
0xA0F0	DHDSTATE	0x0000_0110

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	...	...	...
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0			

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2]	RO	bottom_field	DHD shows top and bottom field logos. 0: top field; 1: Bottom field.

Offset Address	Register Name	Total Reset Value
0xA0F0	DHDSTATE	0x0000_0110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access Name		Description
[1]	RO	vblank	DHD displays blanking zone identification. 0: effective area; 1: blanking zone.
[0]	RO	vback_blank	Blanking the logo after the DHD display. 0: not the post-blanking zone; 1: It is the rear blanking area.

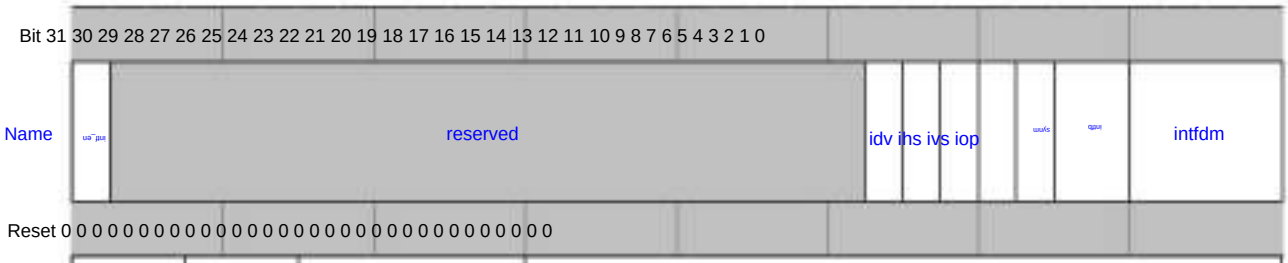
DSDCTRL

DSDCTRL is the overall control register of the display channel.

注意

The configuration of all bits of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA800	DSDCTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	intf_en	Displays whether the interface is enabled. When enabled, the interface will output. Instant register. 0: forbidden; 1: enable.
[30:11]	RO	reserved	reserve.
[10]	RW	idv	Data valid signal output inversion enable, immediate register. 0: forbidden; 1: enable.
[9]	RW	ihs	Horizontal sync pulse output inverting enable, immediate register. 0: forbidden; 1: enable.
[8]	RW	ivs	Vertical sync pulse output inversion enable, immediate register. 0: forbidden; 1: enable.
[7]	RW	iop	Progressive or interlaced display, instant register. 0: Interlaced display; 1: Display line by line.
[6]	RW	syn	Synchronous mode, immediate registers. 0: Timing label mode (such as BT.656); 1: Synchronous signal mode (such as LCD display).
[5:4]	RW	intfb	Output interface bit width mode. Instant register. 00: single component mode (each clock outputs 1 component); others: invalid.
[3:0]	RW	intfdm	Interface data format. Instant register. 0x0: YCbCr422 data format; Other: invalid.

DSDVSYNC

DSDVSYNC is the pendant timing register. When interlaced output, this register indicates the vertical synchronization timing of the top field; when outputting progressively, this register indicates the vertical synchronization timing of the frame. This register takes effect immediately after configuration, and will immediately affect the timing of the pin VSYNC.

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA804	DSDVSYNC	0x0011_511F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1			1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	vfb	For interlaced output: top field vertical blanking front porch; When outputting progressively: vertical blanking leading edge. Unit: row.
[19:12]	RW	etc	For interlaced output: top field vertical blanking back porch; When outputting line by line: the width of the vertical pulse is added to the shoulder after the vertical blanking. Unit: row.
[11:0]	RW	vact	For interlaced output: the height of the active image of the top field; for progressive output: the height of an active image for one frame. The value of this register is minus 1 from the actual value. Unit: row.

DSDHSYNC1

DSDHSYNC1 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA808	DSDHSYNC1	0x0107_02CF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hbb	hact
Reset	0 0 0 0 0 0 0 1 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1 0 1 1 0 0 1 1 1

Bits	Access Name	Description
[31:16]	RW hbb	Horizontal blanking back shoulder, in pixels.
[15:0]	RW hact	The number of horizontal pixels in the active area.

DSDHSYNC2

DSDHSYNC2 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA80C	DSDHSYNC2	0x0000_0017

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hfb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1

Bits	Access Name	Description
[31:16]	RO reserved	reserve.
[15:0]	RW hfb	Horizontal blanking front shoulder, in pixels.

DSDVPLUS

DSDVPLUS is the interlaced bottom field vertical timing register. For interlaced output, this register indicates the vertical sync timing of the bottom field.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA810	DSDVPLUS	0x0011_611F

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	bvfb	bvbb	bvact
Reset	0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 1 0 1 1	0 0 0 0 1 0 0 0 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	bvfb	For interlaced output: Bottom field vertical blanking front porch. Unit: row.
[19:12]	RW	bvbb	For interlaced output: the width of the vertical pulse of the porch after the vertical blanking of the bottom field. Unit: row.
[11:0]	RW	bvact	For interlaced output: the height of the active image in the bottom field. The value of this register is minus 1 from the actual value. Unit: row.

DSDPWR

DSDPWR is the sync signal pulse width register.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xA814	DSDPWR	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vpw	hpw
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	vpw	The vertical pulse width is minus 1. Unit: pixel.
[15:0]	RW	hpw	Subtract 1 from the horizontal pulse width. Unit: pixel.

DSDVTTHD

DSDVTTHD is the Vertical Timing Threshold register. Instant register. This register contains two threshold configurations, which can generate two interrupts independently.

Offset Address	Register Name	Total Reset Value
0xA81C	DSDVTTHD	0x0000_0001

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		vtmgthd1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	thd1_mode	Threshold 1 Mode for interrupt generation. 0: Frame mode, threshold counting is done in units of frames; 1: Field mode, the threshold counting is performed in units of field during interlaced display.
[14:13]	RO	reserved	reserve.
[12:0]	RW	vtmgthd1	The vertical timing threshold is 1, when the vertical timing counter reaches this threshold, the VOINTSTA[dsdvtthd_int1] interrupt is triggered.

DSDCLIPL

DSDCLIPL Handles the lowest threshold register for display channel clips. Instant register.

Offset Address	Register Name	Total Reset Value
0xA840	DSDCLIPL	0x4401_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipcl2														clipcl1												clipcl0			
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	clipen	Output clamp enable, immediate register. 0: forbidden; 1: enable.
[30]	RW	dfir_en	Chroma level downsampling enable signal. 0: forbidden; 1: enable.
[29:20]	RW	clipcl2	Component 2 Minimum threshold value Y/R, unsigned integer.
[19:10]	RW	clipcl1	Component 1 is the lowest threshold Cb/G, an unsigned integer.
[9:0]	RW	clipcl0	Component 0 is the lowest threshold Cr/B, an unsigned integer.

DSDCLIPH

DSDCLIPH Handles the highest threshold value register for the display channel clip. Instant register. For example: when BT.656 standard output, CLIP processing is required for the output data.

Offset Address	Register Name	Total Reset Value
0xA844	DSDCLIPH	0x3ACF_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipch2														clipch1												clipch0			
Reset	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:30]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xA844	DSDCLIPH	0x3ACF_03C0

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	clipch2	clipch1	clipch0
Reset	0 0 1 1	1 0 1 0 1	1 0 0 1 1	1 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[29:20]	RW	clipch2	Component 2 The highest threshold Y/R, an unsigned integer.
[19:10]	RW	clipch1	Component 1 is the highest threshold Cb/G, an unsigned integer.
[9:0]	RW	clipch0	Component 0 is the highest threshold Cr/B, an unsigned integer.

DSDSTATE

DSDSTATE is the DSD status register.

Offset Address	Register Name	Total Reset Value
0xA8F0	DSDSTATE	0x0000_0006

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
Name	reserved	bottom_field	vblank
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	bottom_field	DSD shows top and bottom field identification. 0: top field; 1: Bottom field.
[1]	RW	vblank	DSD shows blanking zone identification. 0: effective area; 1: Blanking zone.

Offset Address	Register Name	Total Reset Value
0xA8F0	DSDSTATE	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vsync_blank	vsync	hsync_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name	Description
[0] RW vback_blank		Blanking logo after DSD display. 0: not the post-blanking zone; 1: It is the rear blanking area.

DSD1CTRL

DSD1CTRL is the overall control register of the display channel.

> **注意**
>
> The configuration of all bits of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC00	DSD1CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	reserved																							idv	ihs	ivs	iop	sync	intdo	intfdm	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31] RW intf_en		Displays whether the interface is enabled. When enabled, the interface will output. Instant register. 0: forbidden; 1: enable.
[30:11] RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xAC00	DSD1CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																				idv	ihs	ivs	iop	[illegible]	[illegible]	intfdm				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[10]	RW idv	Data valid signal output inversion enable, immediate register. 0: forbidden; 1: enable.
[9]	RW ihs	Horizontal sync pulse output inverting enable, immediate register. 0: disable; 1: enable.
[8]	RW ivs	Vertical sync pulse output inversion enable, immediate register. 0: forbidden; 1: enable.
[7]	RW iop	Progressive or interlaced display, instant register. 0: Interlaced display; 1: Display line by line.
[6]	RW syn	Synchronous mode, immediate registers. 0: Timing label mode (such as BT.656); 1: Synchronous signal mode (such as LCD display).
[5:4]	RW intfb	Output interface bit width mode. Instant register. 00: single-component mode (each clock outputs 1 component); others: reserved.
[3:0]	RW intfdm	Interface data format. Instant register. 0x0: YCbCr422 data format; others: reserved.

DSD1VSYNC

DSD1VSYNC is the vertical timing register. When interlaced output, this register indicates the vertical synchronization timing of the top field; when outputting progressively, this register indicates the vertical synchronization timing of the frame. This register takes effect immediately after configuration, and will immediately affect the timing of the pin VSYNC.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC04	DSD1VSYNC	0x0011_511F

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vfb	vbb	vact
Reset	0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 1 0 1 0	1 0 0 0 1 0 0 0 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	vfb	For interlaced output: top field vertical blanking front porch; When outputting progressively: vertical blanking leading edge. Unit: row.
[19:12]	RW	etc	For interlaced output: top field vertical blanking back porch; When outputting line by line: the width of the vertical pulse is added to the shoulder after the vertical blanking. Unit: row.
[11:0]	RW	vact	For interlaced output: the height of the active image of the top field; for progressive output: the height of an active image for one frame. The value of this register is minus 1 from the actual value. Unit: row.

DSD1HSYNC1

DSD1HSYNC1 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC08	DSD1HSYNC1	0x0107_02CF

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hbb		hact
Reset	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 1 0 0 0 0 0 0 1 0 1 1 0 0 1 1 1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal blanking back shoulder, in pixels.
[15:0]	RW	hact	The number of horizontal pixels in the active area.

DSD1HSYNC2

DSD1HSYNC2 is the horizontal timing register. In the case of interlaced or progressive output, the horizontal synchronization configuration register. This register takes effect immediately after configuration, and will immediately affect the timing of the pin HSYNC.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC0C	DSD1HSYNC2	0x0000_0017

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		hfb
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hfb	Horizontal blanking front shoulder, in pixels.

DSD1VPLUS

When DSD1VPLUS is an interlaced output, the vertical synchronization timing register of the bottom field.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC10	DSD1VPLUS	0x0011_611F

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	bvfb	bvbb	bvact
Reset	0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 1 0 1 1	0 0 0 0 1 0 0 0 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	bvfb	For interlaced output: Bottom field vertical blanking front porch. Unit: row.
[19:12]	RW	bvbb	For interlaced output: the width of the vertical pulse of the porch after the vertical blanking of the bottom field. Unit: row.
[11:0]	RW	bvact	For interlaced output: the height of the active image in the bottom field. The value of this register is minus 1 from the actual value. Unit: row.

DSD1PWR

DSD1PWR is the sync signal pulse width register.

注意

The configuration of this register must be no later than DSDCTRL[intf_en], otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xAC14	DSD1PWR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vpw hpw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	vpw	The vertical pulse width is minus 1. Unit: pixel.
[15:0]	RW	hpw	Subtract 1 from the horizontal pulse width. Unit: pixel.

DSD1VTTHD

DSD1VTTHD is the Vertical Timing Threshold register. Instant register. This register contains two threshold configurations, which can generate two interrupts independently.

Offset Address	Register Name	Total Reset Value
0xAC1C	DSD1VTTHD	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vtmgthd1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	thd1_mode	Threshold 1 interrupt generation mode: 0: Frame mode, threshold counting is performed in units of frames; 1: Field mode, threshold counting is performed in units of fields in interlaced display.
[14:13]	RO	reserved	reserve.
[12:0]	RW	vtmgthd1	The vertical timing threshold is 1, when the vertical timing counter reaches this threshold, the VOINTSTA[dsdvtthd_int1] interrupt is triggered.

DSD1CLIPL

DSD1CLIPL is the lowest threshold value register for display channel clip processing. Instant register.

Offset Address	Register Name	Total Reset Value
0xAC40	DSD1CLIPL	0x4401_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipcl2														clipcl1												clipcl0			
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access Name	Description
[31] RW clipen		Output clamp enable, immediate register. 0: forbidden; 1: enable.
[30] RW dfir_en		Chroma level downsampling enable signal. 0: disabled 1: enable.
[29:20] RW clipcl2		Component 2 Minimum threshold value Y/R, unsigned integer.
[19:10] RW clipcl1		Component 1 is the lowest threshold Cb/G, an unsigned integer.
[9:0] RW clipcl0		Component 0 is the lowest threshold Cr/B, an unsigned integer.

DSD1CLIPH

DSD1CLIPH is the highest threshold value register for display channel clip processing. Instant register. For example: when BT.656 standard output, CLIP processing is required for the output data.

Offset Address	Register Name	Total Reset Value
0xAC44	DSD1CLIPH	0x3ACF_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]		clipch2														clipch1												clipch0			
Reset	0	0	1	1	1	0	1	0	1	0	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bits	Access Name	Description
[31:30] RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xAC44	DSD1CLIPH	0x3ACF_03C0

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	-	clipch2	clipch1	clipch0
Reset	0 0 1 1	1 0 1 0 1	1 0 0 1 1	1 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[29:20]	RW	clipch2	Component 2 The highest threshold Y/R, an unsigned integer.
[19:10]	RW	clipch1	Component 1 is the highest threshold Cb/G, an unsigned integer.
[9:0]	RW	clipch0	Component 0 is the highest threshold Cr/B, an unsigned integer.

DSD1STATE

DSD1STATE is the DSD status register.

Offset Address	Register Name	Total Reset Value
0xACF0	DSD1STATE	0x0000_0006

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	-	-
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	bottom_field	DSD shows top and bottom field identification. 0: top field; 1: Bottom field.
[1]	RW	vblank	DSD shows blanking zone identification. 0: effective area; 1: Blanking zone.

Offset Address	Register Name	Total Reset Value
0xACF0	DSD1STATE	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name	Description
[0]	RW vback_blank	Blanking logo after DSD display. 0: not the post-blanking zone; 1: It is the rear blanking area.

DATE_COEFF0

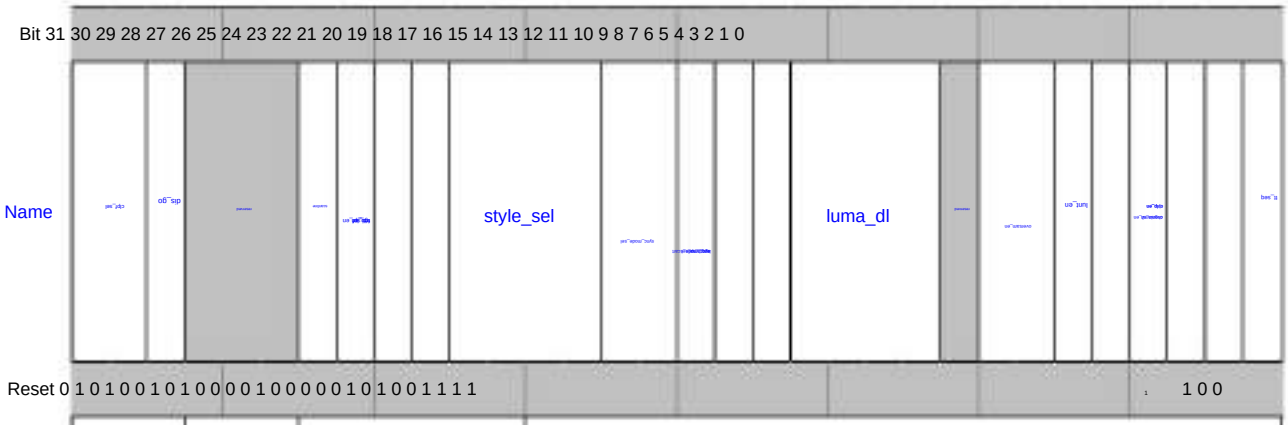
DATE_COEFF0 is the standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																	style_sel								luma_dl								
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0

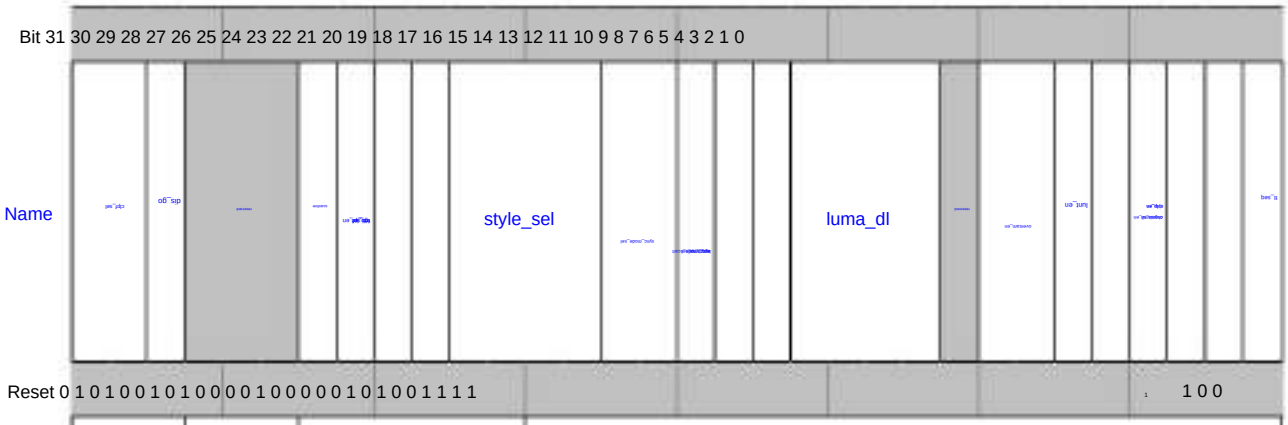
Bits	Access Name	Description
[31:30]	RW clpf_sel	Chroma low pass filter bandwidth selection. 00: 1.1MHz bandwidth (NTSC); 01: 1.3MHz bandwidth (PAL); 10: 1.6MHz bandwidth (test); 11: Reserved.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC



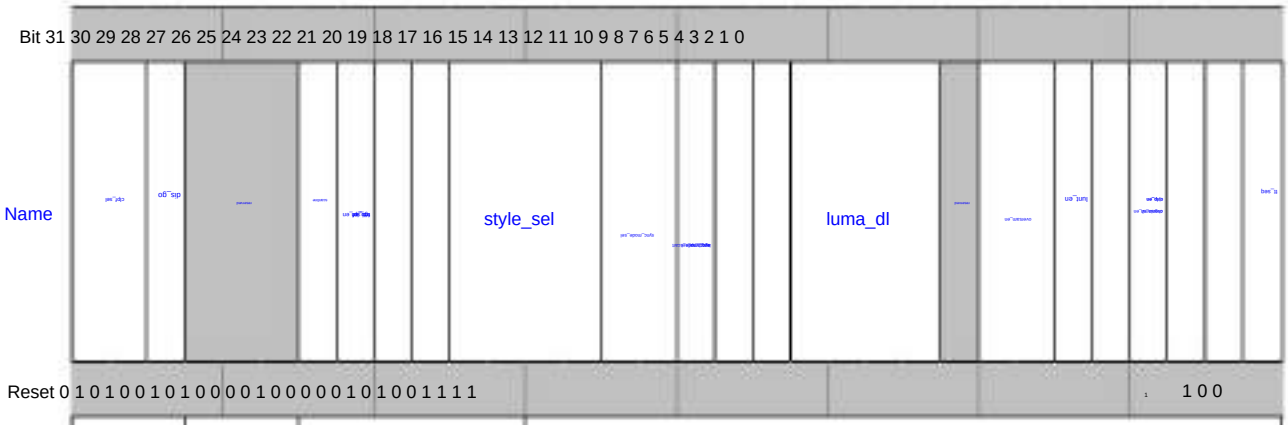
Bits	Access	Name	Description
[29]	RW	dis_ire	For (M)NTSC and (M,N)PAL, the black level is higher than the blanking level 7.5IRE; for other systems, the black level is equal to the blanking level. This bit controls whether the black level should be 7.5 IRE above the blanking level. 0: The black level is higher than the blanking level by 7.5IRE; 1: The black level is equal to the blanking level.
[28:26]	RW	reserved	reserve. Invalid for write, read as 0.
[25]	RW	scanline	Set according to the number of scanning lines contained in each frame under different systems. For (M)NTSC, NTSC-J, (M)PAL, each frame contains 525 lines; for (B, D, J, H, I)PAL, (N)PAL, (Nc)PAL, each frame contains 625 lines. 0: Each frame contains 525 lines; 1: Each frame contains 625 lines.
[24]	RW	rgb_en	When intf_sel is configured as 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr is selected for component signal; 1: Use RGB for component signals.
[23]	RW	vbi_lpf_en	Vbi data low pass filter enable control. 0: No filter processing; 1: filter processing.
[22]	RW	fm_sel	FMsecam FM selection. 0: Secam FM adopts sin; 1: Secam FM adopts cos.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC



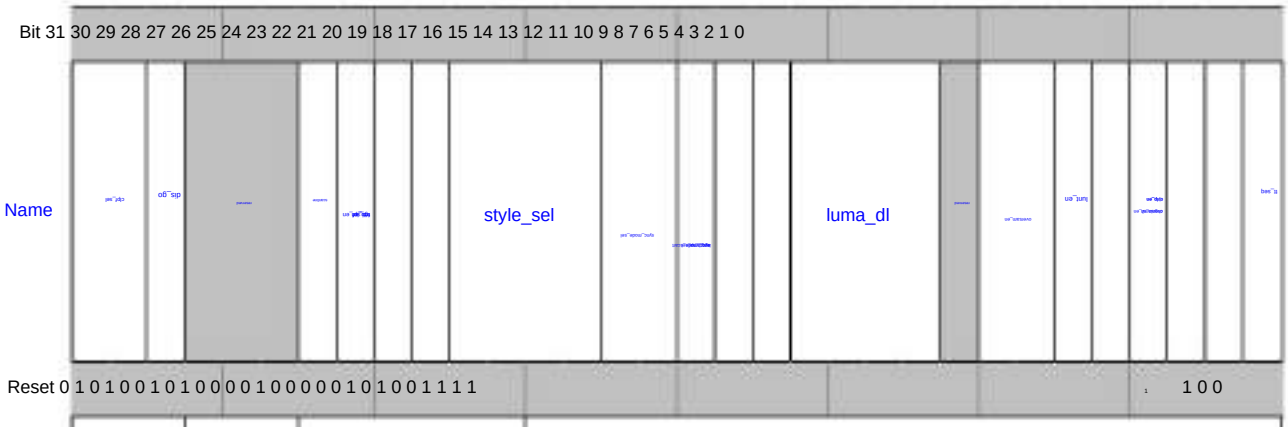
Bits	Access	Name	Description
[21:18]	RW	style_sel	Cooperate with scanline to set the system of CVBS/S-Video output signal. When scanline is 0, that is, each frame contains 525 lines, the meaning is as follows: 0x1: (M)NTSC system; 0x2: NTSC-J system; 0x4: (M)PAL system; Others: Reserved. When scanline is 1, that is, each frame contains 625 lines, the meaning is as follows: 0x1: (B, D, G, H, I) PAL system; 0x2: (N) PAL system; 0x4: (Nc) PAL system; 0x8: SECAM system. Other: reserved.
[17:16]	RW	sync_mode_sel	bit[17]: Indicates whether the component output should include sync signals on all three channels, this control bit only works when sync_mode_scart is configured as 0. This bit is only valid when intf_sel is set to 100, that is, there is component output, meaning: 0: when component output, only one channel contains synchronous signal; 1: During component output, sync signals are included on all three channels. When this bit is set to 0, for YPbPr output, the sync channel can only be Y channel; for RGB output, it can only be G channel. bit[16]: Indicate whether the RGB output has a blanking base. This bit is only valid when intf_sel is set to 100 and rgb_en is set to 1, meaning: 0: No blanking base in RGB output; 1: There is a blanking base in RGB output.
[15]	RW	sync_mode_scart	This bit indicates that the 3 channels of the lower component are not superimposed and synchronized. 0: The component synchronization output is configured according to sync_mode_sel[1] 1: The 3 channels of the component are not superimposed and synchronized. At this time, sync_mode_sel[1] needs to be configured as 0

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC



Bits	Access	Name	Description
[14]	RW	length_sel	Indicates the effective width of the line in pixels that each video line contains. 0: output according to the effective pixel width of the line in BT.601 mode; 1: Output according to the effective pixel width of the line in BT.470 mode. When this bit is 0, the effective width of the row is 720 pixels. When this bit is configured as 1, for the 625-line system, the effective width of the line is 704 pixels; for the 525-line system, the effective width of the line is 712 pixels. The current version does not support the dynamic configuration of BT601 mode and BT470 mode, and the configuration cannot be changed in the middle process after reset according to the needs. It is recommended to configure it as BT601 mode, that is, to use the power-on reset value.
[13]	RW	agc_amp_sel	AGC pulse selection. 0: Refer to the default value inside the image to generate AGC pulse (recommended); 1: Refer to the configuration outside the image to generate AGC pulse DATE_COEFF1[amp_outside].
[12:9]	RW	luma_dl	The amount by which the chroma signal leads or lags relative to the luma signal, in units of half a pixel width. bit[12]: The direction of the displacement of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luma signal; 1: The chroma signal leads the chroma signal. bit[11:9]: The absolute value of the displacement of the chrominance signal relative to the luminance signal, expressed in binary, and the value range is from 0 to 7. 000: Chroma and brightness are aligned, no adjustment is made; 001~111: The chrominance signal leads or lags behind the luminance signal by 1~7 units.
[8]	RW	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC



Bits	Access	Name	Description
[7:6]	RW	oversam_en	The first-level oversampling switch control bits include brightness oversampling switch control bits and chroma oversampling switch control bits. bit[7]: Brightness oversampling switch control bit. 0: Brightness oversampling is off; 1: Luma oversampling is on. bit[6]: chroma oversampling switch control bit. 0: chroma oversampling is off; 1: chroma oversampling is on.
[5]	RW	lunt_en	Brightness notch function switch control bit. 0: The luma notch function is off; 1: The luma notch function is on.
[4]	RW	oversam2_en	The second-stage oversampling switch control bit controls both the luma and chrominance channels. 0: Brightness oversampling is off; 1: Luma oversampling is on.
[3]	RW	chlp_en	Chroma low-pass filter function switch control bit. 0: Chroma low-pass filter function is off; 1: The chroma low-pass filter function is turned on.
[2]	RW	sylp_en	Synchronous low-pass filter function switch control bit. 0: Synchronous low-pass filter function is off; 1: The synchronous low-pass filter function is enabled.
[1]	RW	chgain_en	Chroma gain switch control bit. 0: chroma gain off; 1: Chroma gain is on.

Offset Address	Register Name	Total Reset Value
0xC200	DATE_COEFF0	0x5284_14FC

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: style_sel, luma_dl

Reset 0 1 0 1 0 0 1 0 1 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 1 1 0 0

Bits	Access Name	Description
[0] RW	tt_seq	Configures the order in which bits in the Teletext data byte are sent. 0: from high to low; 1: From low to high.

DATE_COEFF1

DATE_COEFF1 is the amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC204	DATE_COEFF1	0x0000_0000

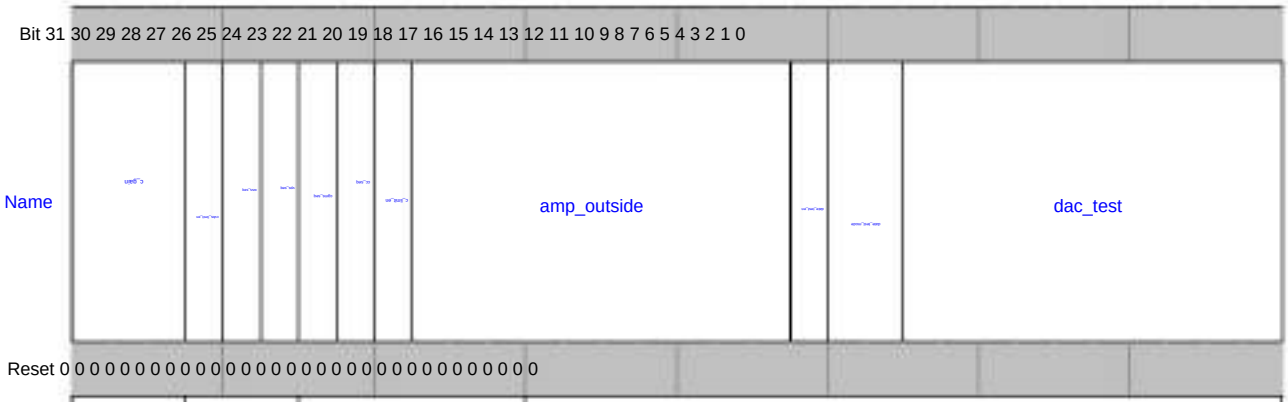
Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: amp_outside, dac_test

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:29] RW	c_gain	Color burst gain adjustment.
[28] RW	cvbs_limit_en	CVBS limit switch control bit. 0: no clipping; 1: clipping.

Offset Address	Register Name	Total Reset Value
0xC204	DATE_COEFF1	0x0000_0000

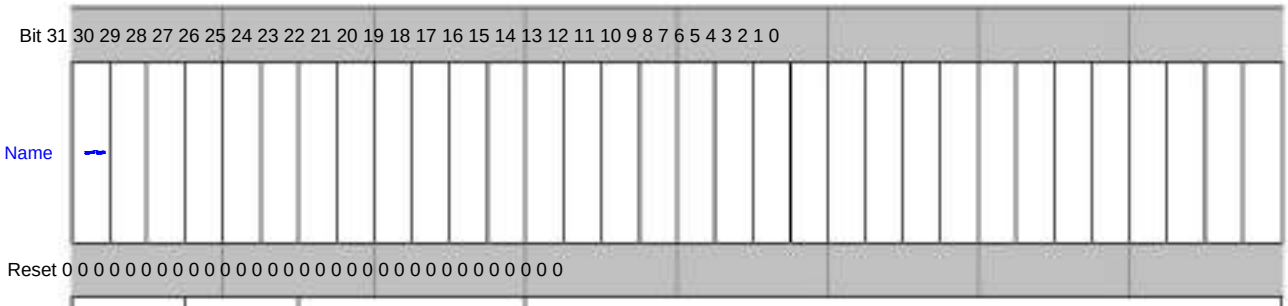


Bits	Access	Name	Description
[27]	RW	wss_seq	Configures the order in which bits in the WSS data byte are sent. 0: from high to low; 1: from low to high.
[26]	RW	vps_seq	Configures the order in which bits in the VPS data byte are sent. 0: from high to low; 1: From low to high.
[25]	RW	cgms_seq	Configures the order in which bits in the CGMS data byte are sent. 0: from high to low; 1: From low to high.
[24]	RW	cc_seq	Configure the order in which bits in the Closed Caption data byte are sent. 0: from high to low; 1: From low to high.
[23]	RW	c_limit_en	Chroma clip switch control bit. 0: unlimited; 1: clipping.
[22:13]	RW	amp_outside	External AGC pulse amplitude input.
[12]	RW	date_test_en	Test for a valid signal. 0: invalid; 1: valid.
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE_COEFF7

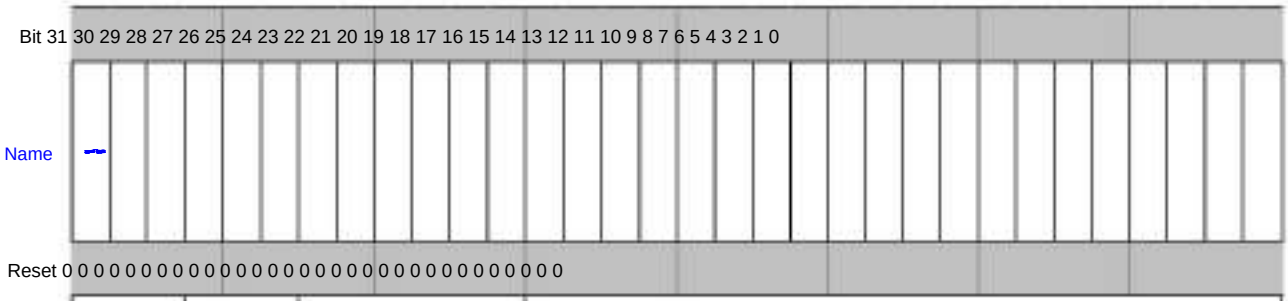
DATE_COEFF7 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000



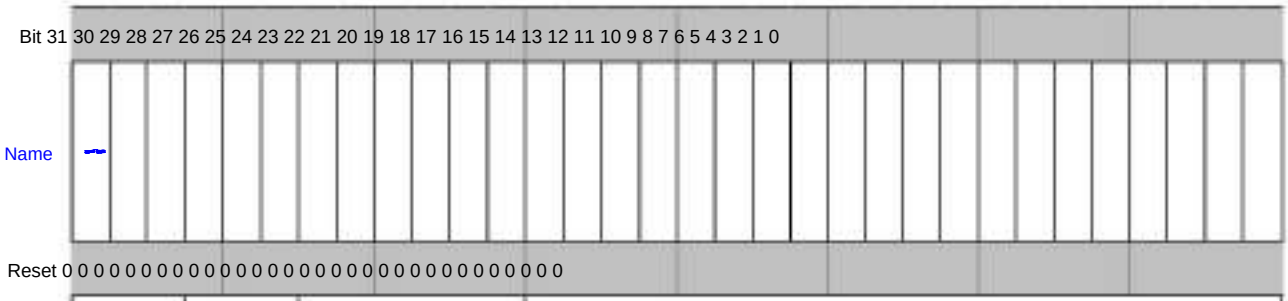
Bits	Access	Name	Description
[31]	RW	tt22_enf1	Odd Field Line 22 Teletext switch control bit. 0: off; 1: open.
[30]	RW	tt21_enf1	Line 21 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[29]	RW	tt20_enf1	Line 20 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[28]	RW	tt19_enf1	Line 19 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[27]	RW	tt18_enf1	Line 18 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[26]	RW	tt17_enf1	Line 17 of the odd field is the Teletext switch control bit. 0: off; 2: open.
[25]	RW	tt16_enf1	Line 16 of the odd field is the Teletext switch control bit. 0: off; 3: on.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000



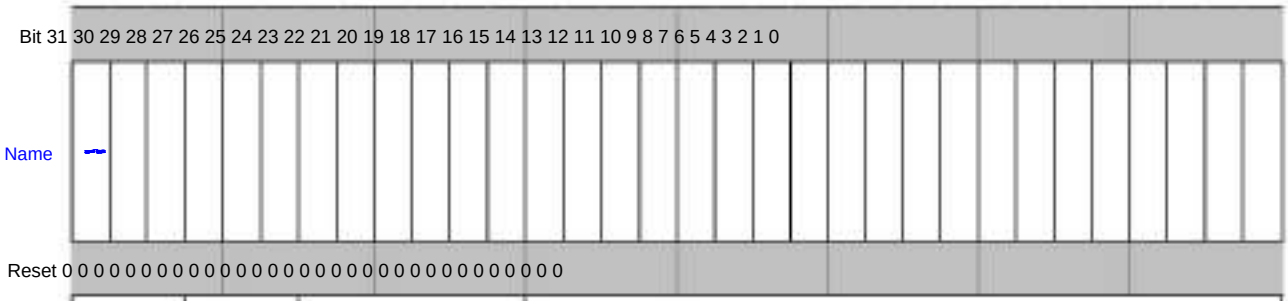
Bits	Access Name	Description
[24]	RW tt15_enf1	Line 15 of the odd field is the Teletext switch control bit. 0: off; 4: on.
[23]	RW tt14_enf1	The 14th line of the odd field is the Teletext switch control bit. 0: off; 5: open.
[22]	RW tt13_enf1	Line 13 of the odd field is the Teletext switch control bit. 0: off; 6: open.
[21]	RW tt12_enf1	Odd Field Line 12 Teletext switch control bit. 0: off; 7: open.
[20]	RW tt11_enf1	Line 11 of the odd field is the Teletext switch control bit. 0: off; 8: open.
[19]	RW tt10_enf1	Odd Field Line 10 Teletext switch control bit. 0: off; 9: on.
[18]	RW tt09_enf1	Odd Field Line 9 Teletext switch control bit. 0: off; 10: open.
[17]	RW tt08_enf1	Odd Field Line 8 Teletext switch control bit. 0: off; 11: open.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000



Bits	Access	Name	Description
[16]	RW	tt07_enf1	Line 7 of odd field Teletext switch control bit. 0: off; 12: open.
[15]	RW	tt22_enf2	Line 22 of the even field is the Teletext switch control bit. 0: off; 1: open.
[14]	RW	tt21_enf2	Line 21 of the even field is the Teletext switch control bit. 0: off; 1: open.
[13]	RW	tt20_enf2	Line 20 of the even field is the Teletext switch control bit. 0: off; 1: open.
[12]	RW	tt19_enf2	Line 19 of the even field is the Teletext switch control bit. 0: off; 1: open.
[11]	RW	tt18_enf2	The 18th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[10]	RW	tt17_enf2	Line 17 of the even field is the Teletext switch control bit. 0: off; 1: open.
[9]	RW	tt16_enf2	Line 16 of the even field is the Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000



Bits	Access	Name	Description
[8]	RW	tt15_enf2	Line 15 of the even field is the Teletext switch control bit. 0: off; 1: open.
[7]	RW	tt14_enf2	The 14th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[6]	RW	tt13_enf2	The 13th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[5]	RW	tt12_enf2	Line 12 of the even field is the Teletext switch control bit. 0: off; 1: open.
[4]	RW	tt11_enf2	The 11th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[3]	RW	tt10_enf2	Line 10 of even field Teletext switch control bit. 0: off; 1: open.
[2]	RW	tt09_enf2	Line 9 of even field Teletext switch control bit. 0: off; 1: open.
[1]	RW	tt08_enf2	Line 8 of even field Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[0]	RW tt07_enf2	Line 7 of even field Teletext switch control bit. 0: off; 1: open.

DATE_COEFF8

DATE_COEFF8 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC220	DATE_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW tt_staddr	Teletext data start address.

DATE_COEFF9

DATE_COEFF9 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC224	DATE_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW tt_edaddr	Teletext data end address.

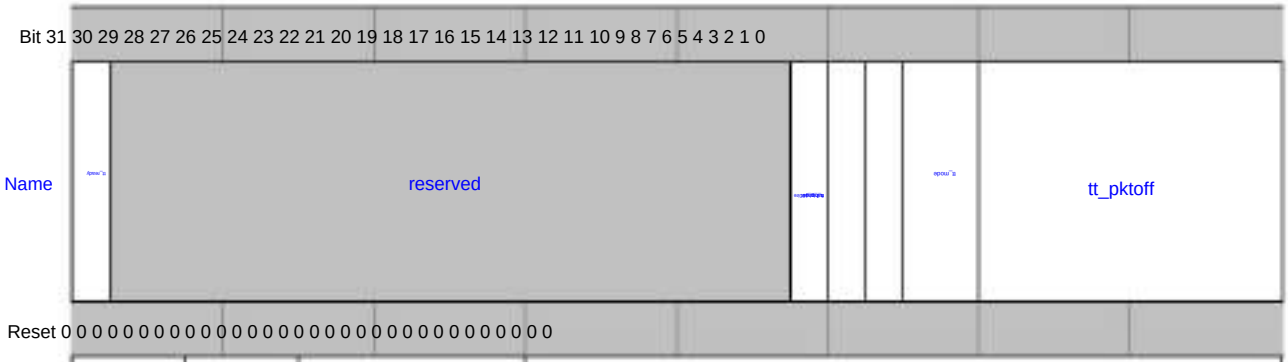
DATE_COEFF10

DATE_COEFF10 configures registers for Teletext.

注意

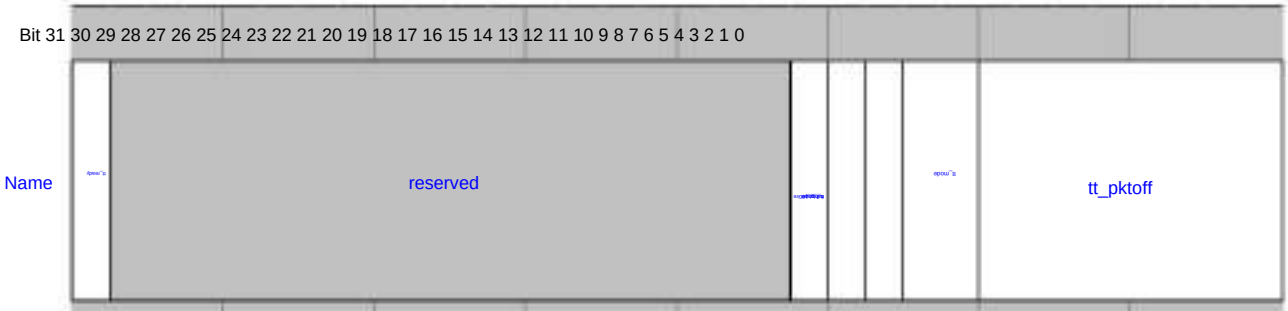
The current version supports Teletext function in both 625-line and 525-line modes. tt_mode is configured as 01 in 625-line mode; tt_mode is configured as 10 in 525-line mode.

Offset Address	Register Name	Total Reset Value
0xC228	DATE_COEFF10	0x0000_0000



Bits	Access	Name	Description
[31]	RW	tt_ready	When the software configures the relevant parameters through the bus, set this bit to 1, and the Teletext module starts to work; When teleltext completes data transmission, the bit is low, and the software can query it, waiting for the software to be configured again.
[30:13]	RW	reserved	reserve. Invalid for write, read as 0.
[12]	RW	nabts_100ire	NABTS-NTSC Data Height Configuration Register. 0ÿ70IREÿ 1ÿ100IREÿ
[11]	RW	full_page	tt Send full page mode control register. 0: normal mode (transmit tt data in blank line); 1: full page mode (transmit tt data in active video area).
[10]	RW	tt_highest	Tt Priority Control Register. 0: tt has the highest priority; 1: tt has the lowest priority.

Offset Address	Register Name	Total Reset Value
0xC228	DATE_COEFF10	0x0000_0000

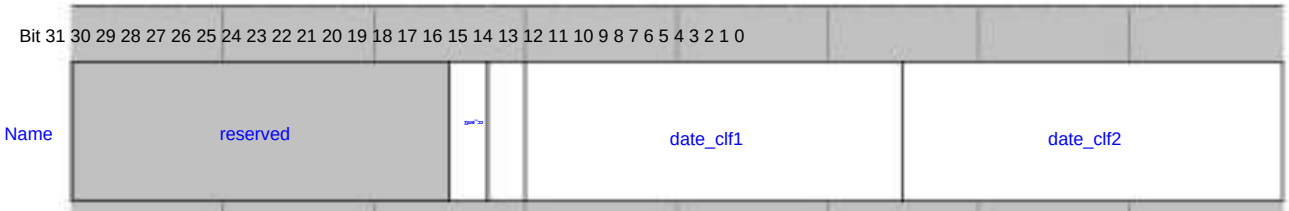


Bits	Access Name	Description
[9:8]	RW tt_mode	TT mode. The configuration in line 625 is 01, representing wst-pal; the configuration in line 525 is 10, representing nabts-ntsc.
[7:0]	RW tt_pktoff	TT packet offset address.

DATE_COEFF11

DATE_COEFF11 is the Closed Caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC22C	DATE_COEFF11	0x0000_0000



Bits	Access Name	Description
[31:22]	RW reserved	reserve.
[21]	RW cc_enf1	Closed Caption Odd field switch control bit. 0: off; 1: open.
[20]	RW cc_enf2	Closed Caption Even field switch control bit. 0: off; 1: open.
[19:10]	RW date_clf1	Closed Caption Odd field configuration line.

Offset Address	Register Name	Total Reset Value
0xC22C	DATE_COEFF11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	[illegible]	date_clf1	date_clf2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[9:0]	RW date_clf2	Closed Caption Even field configuration line.

DATE_COEFF12

DATE_COEFF12 is the Closed Caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC230	DATE_COEFF12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cc_f1data	cc_f2data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW cc_f1data	Closed Caption Odd field data.
[15:0]	RW cc_f2data	Closed Caption Even field data.

DATE_COEFF13

DATE_COEFF13 is the CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC234	DATE_COEFF13	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / cg_enf1 / cg_enf2 / cg_f1data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	reserved	reserve. Invalid for write, read as 0.
[21]	RW	cg_enf1	CGMS odd field switch control bit. 0: off; 1: open.
[20]	RW	cg_enf2	CGMS Even field switch control bit. 0: off; 1: open.
[19:0]	RW	cg_f1data	CGMS odd field data.

DATE_COEFF14

DATE_COEFF14 is the CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC238	DATE_COEFF14	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / cg_f2data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RW	reserved	reserve. Invalid for write, read as 0.
[19:0]	RW	cg_f2data	CGMS even field data.

DATE_COEFF15

DATE_COEFF15 is the WSS configuration register.

注意

WSS is only used in the 625-line system, and it is fixed at 23 lines.

Offset Address	Register Name	Total Reset Value
0xC23C	DATE_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														wss_data	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	reserve. Invalid for write, read as 0.
[14]	RW	wss_en	WSS switch control bit. 0: off; 1: open.
[13:0]	RW	wss_data	WSS data.

DATE_COEFF16

DATE_COEFF16 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC240	DATE_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vps_data	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC240	DATE_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vps_data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[24]	RW	vps_en	VPS switch control bit. 0: off; 1: open.
[23:0]	RW	vps_data	VPS data, bit 23 to bit 0, the lowest bit is bit 0.

DATE_COEFF17

DATE_COEFF17 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC244	DATE_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data, bit 55 to bit 24, the lowest bit is bit 0.

DATE_COEFF18

DATE_COEFF18 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC248	DATE_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data, bit 87 to bit 56, the lowest bit is bit 0.

DATE_COEFF19

DATE_COEFF19 is the VPS configuration register.

注意

VPS only supports 625 rows, fixed at 16 rows.

Offset Address	Register Name	Total Reset Value
0xC24C	DATE_COEFF19	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vps_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	reserved	reserve. Invalid for write, read as 0.
[15:0]	RW	vps_data	VPS data, the 103rd bit to the 88th bit, the lowest bit is the 0th bit.

DATE_COEFF20

DATE_COEFF20 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC250	DATE_COEFF20	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC250	DATE_COEFF20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[2]	RW tt06_enf1	Odd Field Line 6 Teletext switch control bit. 0: off; 1: open.
[1]	RW tt06_enf2	Line 6 of even field Teletext switch control bit. 0: off; 1: open.
[0]	RW tt05_enf2	Teletext switch control bit in line 5 of even field. 0: off; 1: open.

DATE_COEFF21

DATE_COEFF21 is the output matrix control register.

Offset Address	Register Name	Total Reset Value
0xC254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access Name	Description
[31:23]	RW reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	1		1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

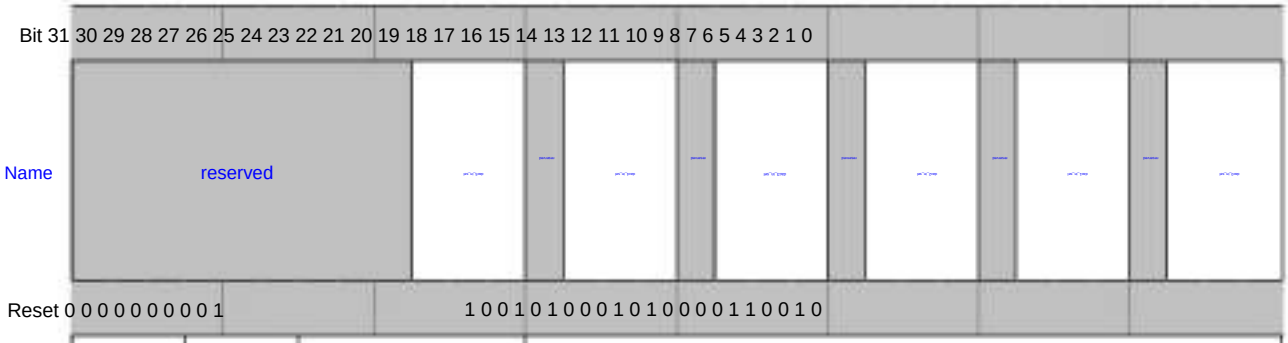
Bits	Access	Name	Description
[22:20]	RW	dac5_in_sel	DAC5 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[19]	RO	reserved	reserve. Invalid for write, read as 0.
[18:16]	RW	dac4_in_sel	DAC4 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[15]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	1		1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access Name		Description
[14:12]	RW	dac3_in_sel	DAC3 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[11]	RO	reserved	reserve. Invalid for write, read as 0.
[10:8]	RW	dac2_in_sel	DAC2 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[7]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC254	DATE_COEFF21	0x0065_1432

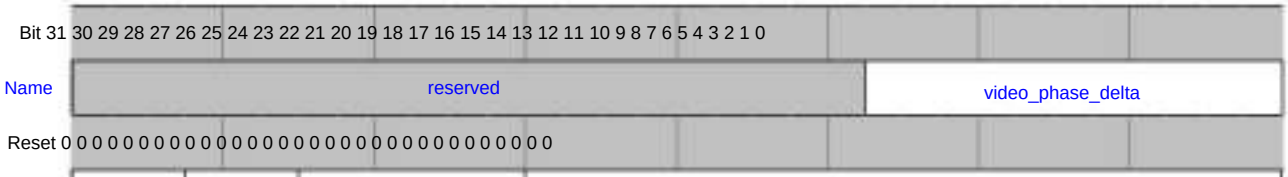


Bits	Access	Name	Description
[6:4]	RW	dac1_in_sel	DAC1 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[3]	RO	reserved	reserve. Invalid for write, read as 0.
[2:0]	RW	dac0_in_sel	DAC0 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ

DATE_COEFF22

DATE_COEFF22 is the DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC258	DATE_COEFF22	0x0000_0000

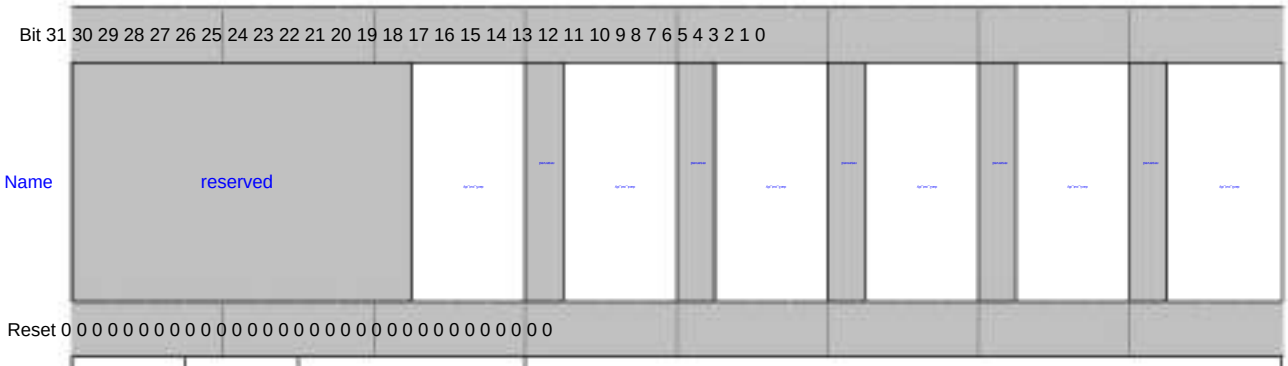


Bits	Access	Name	Description
[31:11]	RW	reserved	reserve. Invalid for write, read as 0.
[10:0]	RW	video_phase_delta	DTO Initial phase configuration register.

DATE_COEFF23

DATE_COEFF23 is the VIDEO_OUT delay configuration register.

Offset Address	Register Name	Total Reset Value
0xC25C	DATE_COEFF23	0x0000_0000



Bits	Access	Name	Description
[31:23]	RW	reserved	reserve. Invalid for write, read as 0.
[22:20]	RW	dac5_out_dly	DAC5 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[19]	RO	reserved	reserve. Invalid for write, read as 0.
[18:16]	RW	dac4_out_dly	DAC4 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[15]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[14:12]	RW	dac3_out_dly	DAC3 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[11]	RO	reserved	reserve. Invalid for write, read as 0.
[10:8]	RW	dac2_out_dly	DAC2 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[7]	RO	reserved	reserve. Invalid for write, read as 0.
[6:4]	RW	dac1_out_dly	DAC1 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[3]	RO	reserved	reserve. Invalid for write, read as 0.
[2:0]	RW	dac0_out_dly	DAC0 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.

DATE_ISRMASK

DATE_ISRMASK is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC280	DATE_ISRMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve. Invalid for write, read as 0.
[0]	RW	tt_mask	Teletext interrupt mask bit. 0: Enable Teletext interrupt; 1: Shield Teletext interrupt.

DATE_ISRSTATE

DATE_ISRSTATE is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC284	DATE_ISRSTATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve. Invalid for write, read as 0.
[0]	W1C	tt_status	Teletext interrupt flag. When DATE has read all the Teletext data, the interrupt flag will be pulled high. To clear the interrupt, you need to write 1 to this bit.

DATE_ISR

DATE_ISR is the interrupt register.

Offset Address	Register Name	Total Reset Value
0xC288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve. Invalid for write, read as 0.
[0]	RW	tt_int	Teletext interrupt register. tt_status Interrupt status after being masked by tt_mask. 0: no interrupt; 1: There is an interrupt.

DATE_VERSION

DATE_VERSION is the version register.

Offset Address	Register Name	Total Reset Value
0xC290	DATE_VERSION	0x0000_0024

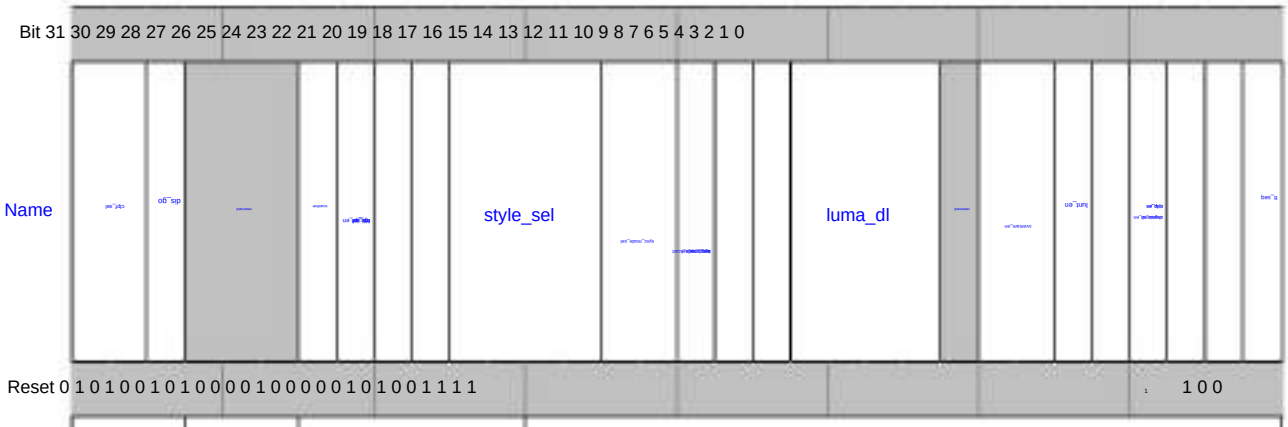
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	reserve. Invalid for write, read as 0.

DATE1_COEFF0

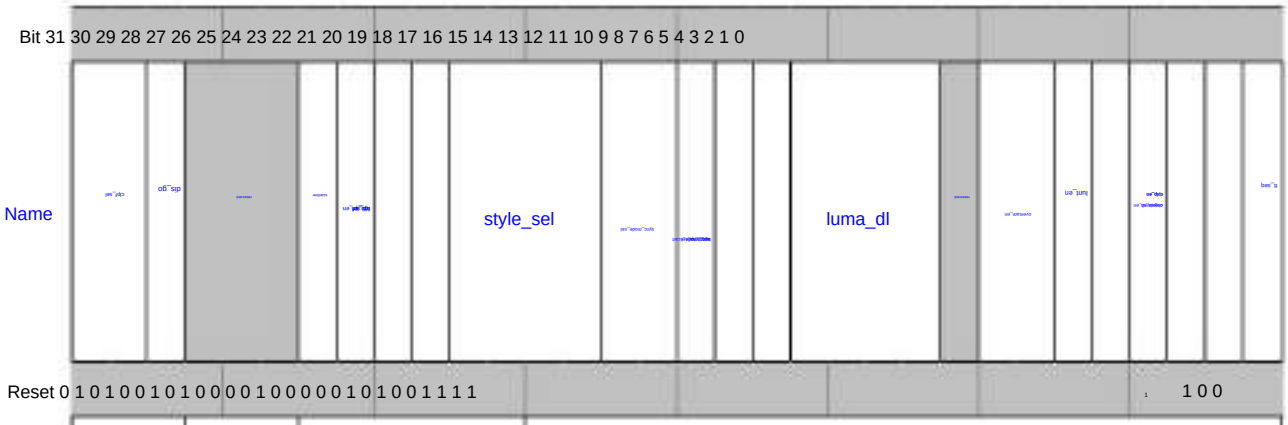
DATE1_COEFF0 is the standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC



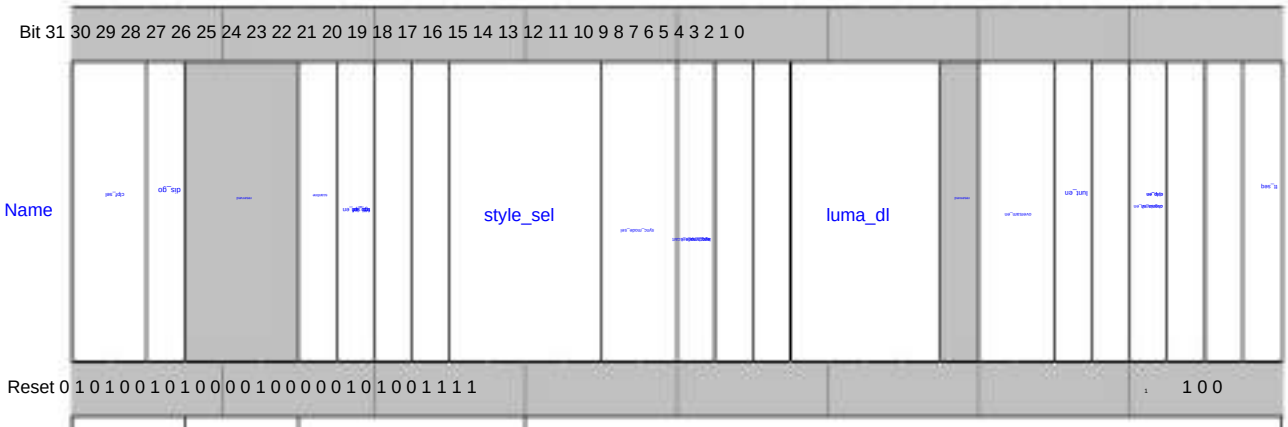
Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Chroma low pass filter bandwidth selection. 00: 1.1MHz bandwidth (NTSC); 01: 1.3MHz bandwidth (PAL); 10: 1.6MHz bandwidth (test); 11: Reserved.
[29]	RW	dis_ire	For (M)NTSC and (M,N)PAL, the black level is higher than the blanking level 7.5IRE; for other systems, the black level is equal to the blanking level. This bit controls whether the black level should be 7.5 IRE above the blanking level. 0: The black level is higher than the blanking level by 7.5IRE; 1: The black level is equal to the blanking level.
[28:26]	RW	reserved	reserve. Invalid for write, read as 0.
[25]	RW	scanline	Set according to the number of scanning lines contained in each frame under different systems. For (M)NTSC, NTSC-J, (M)PAL, each frame contains 525 lines; for (B, D, J, H, I)PAL, (N)PAL, (Nc)PAL, each frame contains 625 lines. 0: Each frame contains 525 lines; 1: Each frame contains 625 lines.
[24]	RW	rgb_en	When intf_sel is configured as 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr is selected for component signal; 1: Use RGB for component signals.
[23]	RW	vbi_lpf_en	Vbi data low pass filter enable control. 0: No filter processing; 1: filter processing.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC



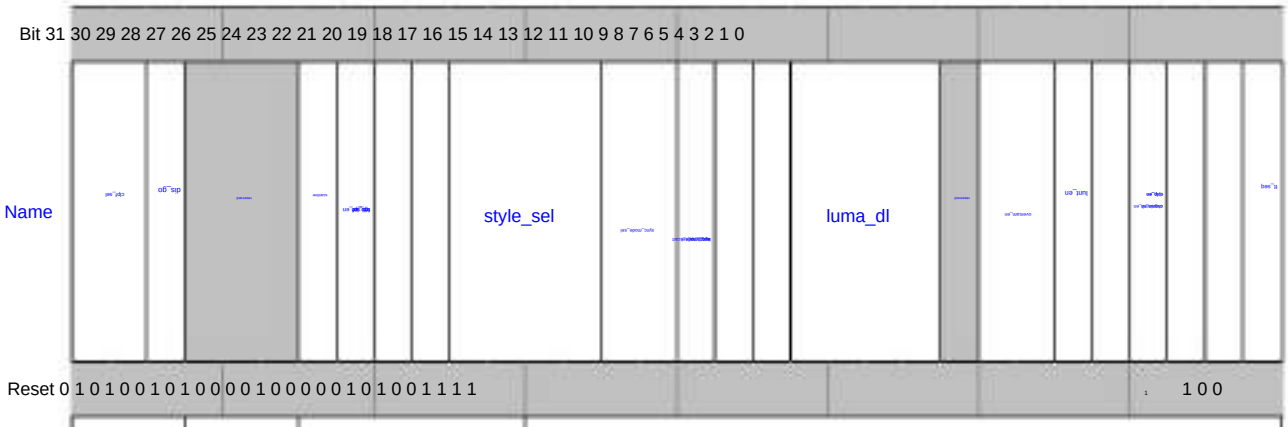
Bits	Access	Name	Description
[22]	RW	fm_sel	FMsecam FM selection. 0: Secam FM adopts sin; 1: Secam FM adopts cos.
[21:18]	RW	style_sel	Cooperate with scanline to set the system of CVBS/S-Video output signal. When scanline is 0, that is, each frame contains 525 lines, the meanings are as follows: 0x1: (M)NTSC system; 0x2: NTSC-J system; 0x4: (M)PAL system; Others: reserved. When scanline is 1, that is, each frame contains 625 lines, the meanings are as follows: 0x1: (B, D, G, H, I) PAL system; 0x2: (N) PAL system; 0x4: (Nc) PAL system; 0x8: SECAM; Others: Reserved.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC



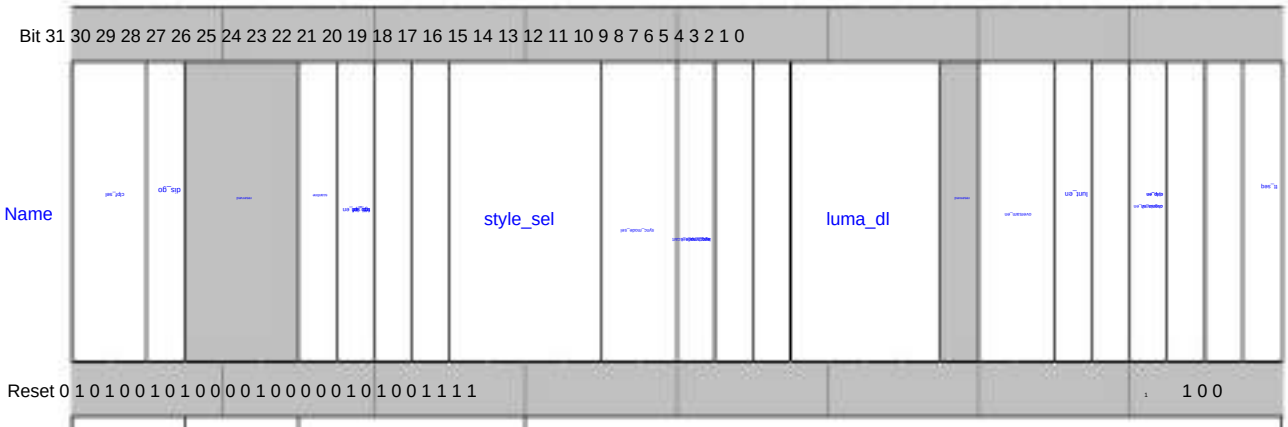
Bits	Access	Name	Description
[17:16]	RW	sync_mode_sel	Bit[17] indicates whether the component output should include sync signals on all three channels, and this control bit will only work when sync_mode_scart is configured as 0. This bit is only valid when intf_sel is set to 100, that is, there is component output, meaning: 0: when component output, only one channel contains synchronous signal; 1: During component output, sync signals are included on all three channels. When this bit is set to 0, for YPbPr output, the sync channel can only be Y channel; for RGB output, it can only be G channel. bit[16]: Indicate whether the RGB output has a blanking base. This bit is only valid when intf_sel is set to 100 and rgb_en is set to 1, meaning: 0: No blanking base in RGB output; 1: There is a blanking base in RGB output.
[15]	RW	sync_mode_scart	Indicates that the 3 channels of the lower component are not superimposed and synchronized. 0: Component synchronous output is configured according to sync_mode_sel[1]; 1: 3 component channels are not superimposed and synchronized, and sync_mode_sel[1] needs to be configured as 0 at this time.
[14]	RW	length_sel	Indicates the effective width of the line in pixels that each video line contains. 0: Output according to the line effective pixel width of BT.601 mode; 1: Output according to the line effective pixel width of BT.470 mode. When this bit is 0, the effective width of the row is 720 pixels. When this bit is configured as 1, for the 625-line system, the effective width of the line is 704 pixels; for the 525-line system, the effective width of the line is 712 pixels. The current version does not support the dynamic configuration of BT601 mode and BT470 mode, and the configuration cannot be changed in the middle process after reset according to the needs. It is recommended to configure it as BT601 mode, that is, to use the power-on reset value.
[13]	RW	agc_amp_sel	0: Refer to the default value inside the image to generate AGC pulse (recommended); 1: Refer to the configuration outside the image to generate AGC pulse DATE_COEFF1[amp_outside].

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC



Bits	Access	Name	Description
[12:9]	RW	luma_dl	The amount by which the chroma signal leads or lags relative to the luma signal, in units of half a pixel width. bit[12]: The direction of the displacement of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luma signal; 1: The chroma signal leads the chroma signal. bit[11:9]: The absolute value of the displacement of the chrominance signal relative to the luminance signal, expressed in binary, and the value range is from 0 to 7. 000: Align chroma and luminance without adjustment; 001~111: Chroma signal leads or lags 1~7 units relative to luminance signal.
[8]	RW	reserved	reserve. Invalid for write, read as 0.
[7:6]	RW	oversam_en	The first-level oversampling switch control bits include brightness oversampling switch control bits and chroma oversampling switch control bits. bit[7]: Brightness oversampling switch control bit. 0: Brightness oversampling is off; 1: Luma oversampling is on. bit[6]: It is the control bit of chroma oversampling switch. 0: chroma oversampling off; 1: chroma oversampling on.
[5]	RW	lunt_en	Brightness notch function switch control bit. 0: Luminance notch function is off; 1: The luma notch function is turned on.
[4]	RW	oversam2_en	The second-stage oversampling switch control bit controls both the luma and chrominance channels. 0: Brightness oversampling is off; 1: Luma oversampling is on.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC

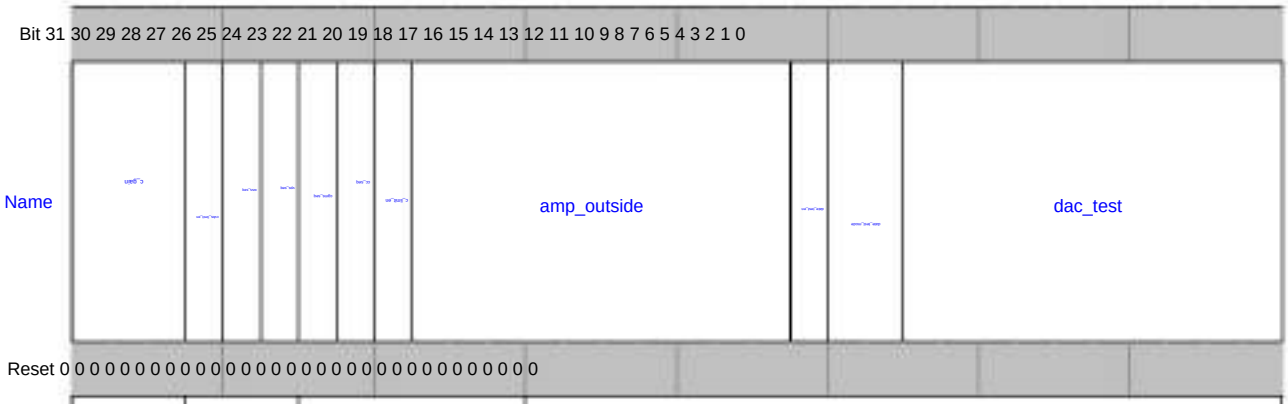


Bits	Access	Name	Description
[3]	RW	chlp_en	Chroma low-pass filter function switch control bit. 0: Chroma low-pass filter function is off; 1: The chroma low-pass filter function is turned on.
[2]	RW	sylp_en	Synchronous low-pass filter function switch control bit. 0: The synchronous low-pass filter function is disabled; 1: The synchronous low-pass filter function is enabled.
[1]	RW	chgain_en	Chroma gain switch control bit. 0: chroma gain off; 1: Chroma gain is on.
[0]	RW	tt_seq	Configures the order in which bits in the Teletext data byte are sent. 0: from high to low; 1: From low to high.

DATE1_COEFF1

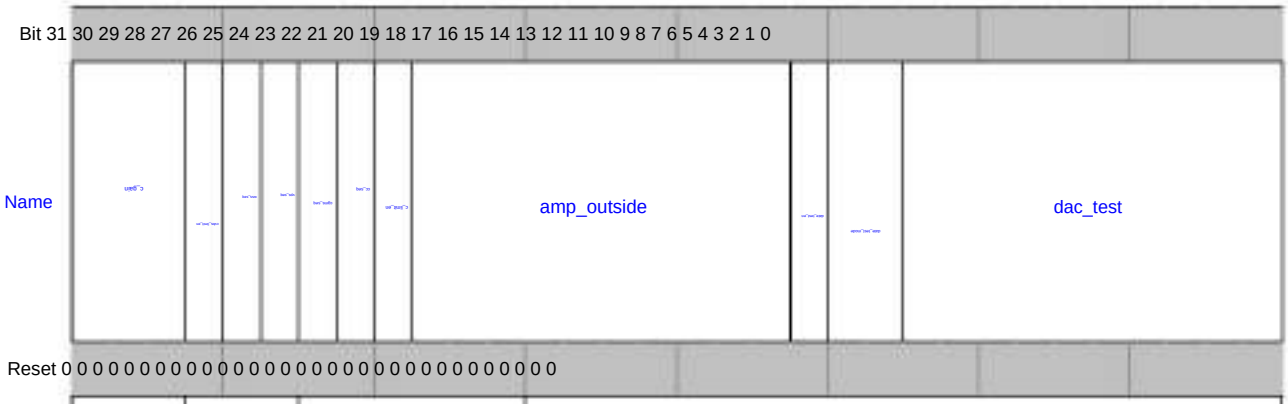
DATE1_COEFF1 is the amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC404	DATE1_COEFF1	0x0000_0000



Bits	Access	Name	Description
[31:29]	RW	c_gain	Color burst gain adjustment.
[28]	RW	cvbs_limit_en	CVBS limit switch control bit. 0: unlimited; 1: clipping.
[27]	RW	wss_seq	Configures the order in which bits in the WSS data byte are sent. 0: from high to low; 1: From low to high.
[26]	RW	vps_seq	Configures the order in which bits in the VPS data byte are sent. 0: from high to low; 1: from low to high.
[25]	RW	cgms_seq	Configures the order in which bits in the CGMS data byte are sent. 0: from high to low; 1: From low to high.
[24]	RW	cc_seq	Configure the order in which bits in the Closed Caption data byte are sent. 0: from high to low; 1: From low to high.
[23]	RW	c_limit_en	Chroma clip switch control bit. 0: no clipping; 1: clipping.
[22:13]	RW	amp_outside	External AGC pulse amplitude input.
[12]	RW	date_test_en	Test for a valid signal. 0: invalid; 1: valid.

Offset Address	Register Name	Total Reset Value
0xC404	DATE1_COEFF1	0x0000_0000

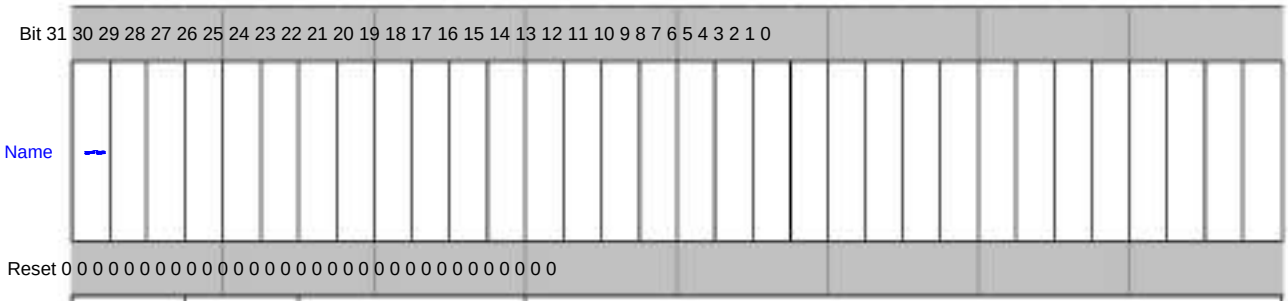


Bits	Access Name	Description
[11:10]	RW date_test_mode	Test mode signal.
[9:0]	RW dac_test	DAC test value input.

DATE1_COEFF7

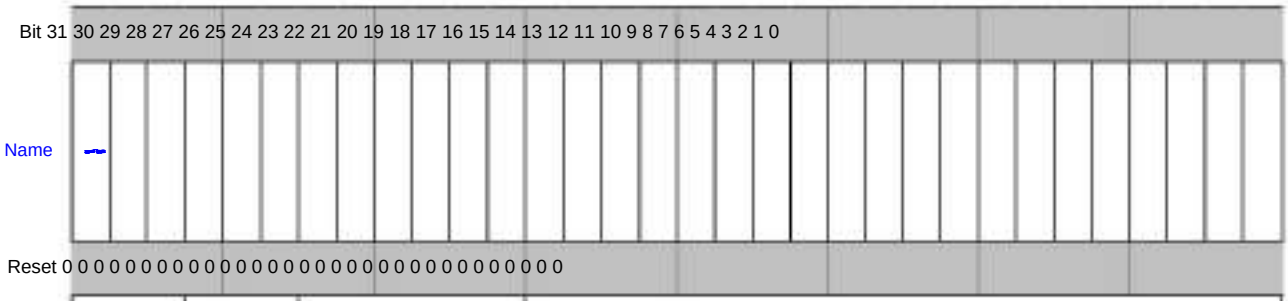
DATE1_COEFF7 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000



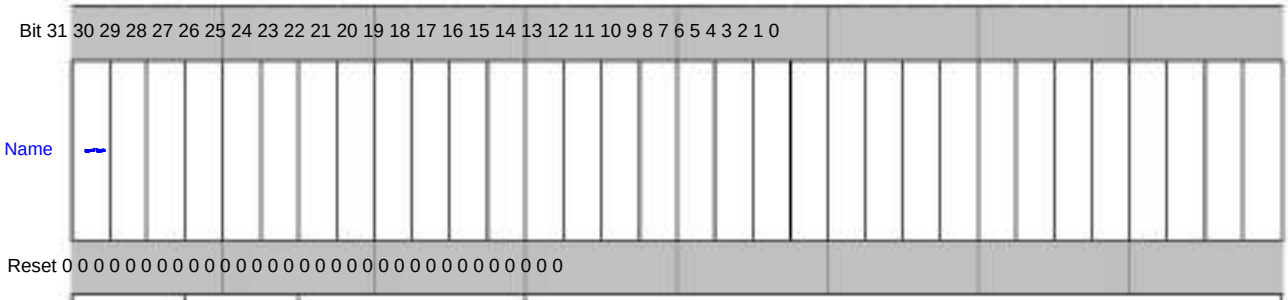
Bits	Access Name	Description
[31]	RW tt22_enf1	Odd Field Line 22 Teletext switch control bit. 0: off; 1: open.
[30]	RW tt21_enf1	Line 21 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[29]	RW tt20_enf1	Line 20 of the odd field is the Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000



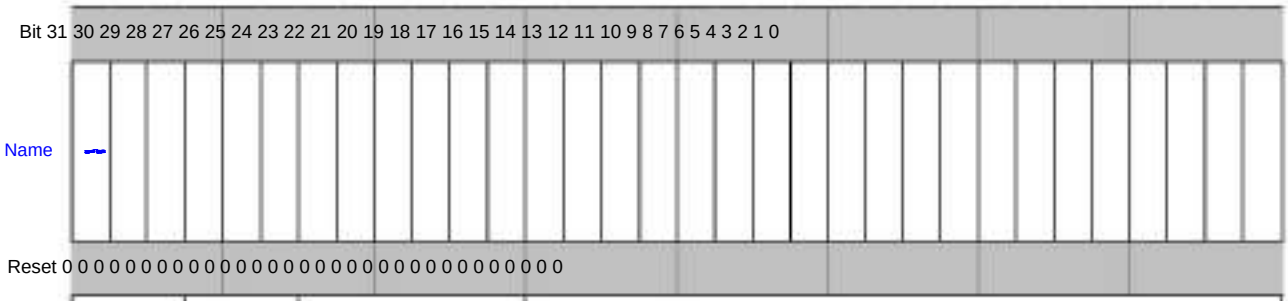
Bits	Access	Name	Description
[28]	RW	tt19_enf1	Line 19 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[27]	RW	tt18_enf1	Line 18 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[26]	RW	tt17_enf1	Line 17 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[25]	RW	tt16_enf1	Line 16 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[24]	RW	tt15_enf1	Line 15 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[23]	RW	tt14_enf1	The 14th line of the odd field is the Teletext switch control bit. 0: off; 1: open.
[22]	RW	tt13_enf1	Line 13 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[21]	RW	tt12_enf1	Odd Field Line 12 Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000



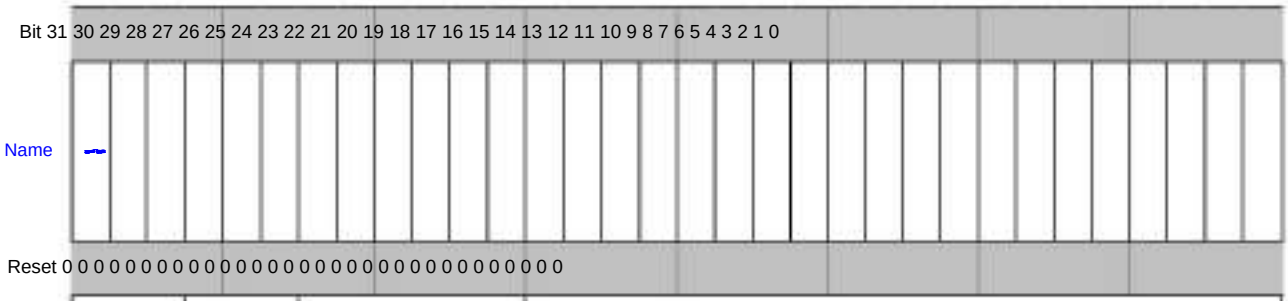
Bits	Access	Name	Description
[20]	RW	tt11_enf1	Line 11 of the odd field is the Teletext switch control bit. 0: off; 1: open.
[19]	RW	tt10_enf1	Odd Field Line 10 Teletext switch control bit. 0: off; 1: open.
[18]	RW	tt09_enf1	Odd Field Line 9 Teletext switch control bit. 0: off; 1: open.
[17]	RW	tt08_enf1	Odd Field Line 8 Teletext switch control bit. 0: off; 1: open.
[16]	RW	tt07_enf1	Line 7 of odd field Teletext switch control bit. 0: off; 1: open.
[15]	RW	tt22_enf2	Line 22 of the even field is the Teletext switch control bit. 0: off; 1: open.
[14]	RW	tt21_enf2	Line 21 of the even field is the Teletext switch control bit. 0: off; 1: open.
[13]	RW	tt20_enf2	Line 20 of the even field is the Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000



Bits	Access	Name	Description
[12]	RW	tt19_enf2	Line 19 of the even field is the Teletext switch control bit. 0: off; 1: open.
[11]	RW	tt18_enf2	The 18th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[10]	RW	tt17_enf2	Line 17 of the even field is the Teletext switch control bit. 0: off; 1: open.
[9]	RW	tt16_enf2	Line 16 of the even field is the Teletext switch control bit. 0: off; 1: open.
[8]	RW	tt15_enf2	Line 15 of the even field is the Teletext switch control bit. 0: off; 1: open.
[7]	RW	tt14_enf2	The 14th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[6]	RW	tt13_enf2	The 13th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[5]	RW	tt12_enf2	Line 12 of the even field is the Teletext switch control bit. 0: off; 1: open.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000



Bits	Access Name	Description
[4]	RW tt11_enf2	The 11th line of the even field is the Teletext switch control bit. 0: off; 1: open.
[3]	RW tt10_enf2	Line 10 of even field Teletext switch control bit. 0: off; 1: open.
[2]	RW tt09_enf2	Line 9 of even field Teletext switch control bit. 0: off; 1: open.
[1]	RW tt08_enf2	Line 8 of even field Teletext switch control bit. 0: off; 1: open.
[0]	RW tt07_enf2	Line 7 of even field Teletext switch control bit. 0: off; 1: open.

DATE1_COEFF8

DATE1_COEFF8 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC420	DATE1_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW tt_staddr	Teletext data start address.

DATE1_COEFF9

DATE1_COEFF9 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC424	DATE1_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW tt_edaddr	Teletext data end address.

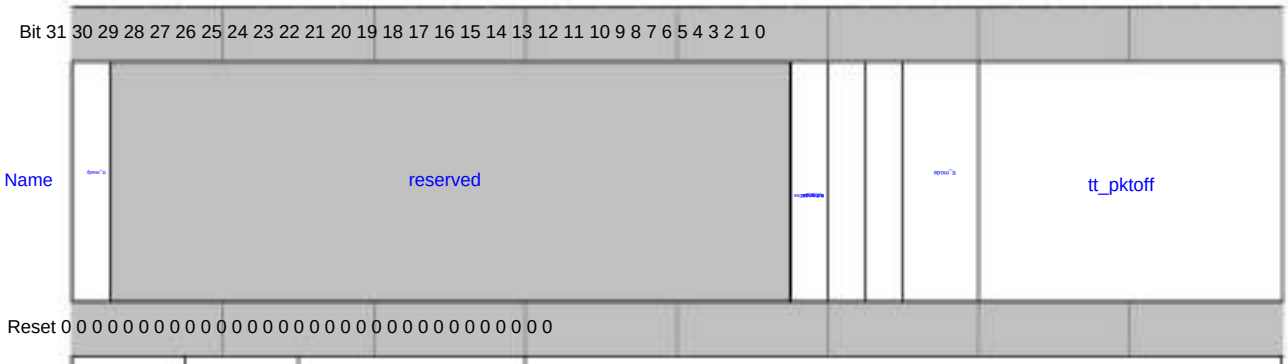
DATE1_COEFF10

DATE1_COEFF10 is a Teletext configuration register.

注意

The current version supports Teletext function in both 625-line and 525-line modes. tt_mode is configured as 01 in 625-line mode; tt_mode is configured as 10 in 525-line mode.

Offset Address	Register Name	Total Reset Value
0xC428	DATE1_COEFF10	0x0000_0000



Bits	Access	Name	Description
[31]	RW	tt_ready	When the software configures the relevant parameters through the bus, set this bit to 1, and the Teletext module starts to work; when the teletext completes data transmission, this bit is low, and the software can query and wait for the software to configure again.
[30:13]	RW	reserved	reserve. Invalid for write, read as 0.
[12]	RW	nabts_100ire	NABTS-NTSC Data Height Configuration Register. 0ÿ70IREÿ 1ÿ100IREÿ
[11]	RW	full_page	tt Send full page mode control register. 0: normal mode (transmit tt data in blank line); 1: full page mode (transmit tt data in active video area).
[10]	RW	tt_highest	Tt Priority Control Register. 0: tt has the highest priority; 1: tt has the lowest priority.
[9:8]	RW	tt_mode	TT mode. The configuration in line 625 is 01, representing wst-pal; the configuration in line 525 is 10, representing nabts-ntsc.
[7:0]	RW	tt_pktoff	TT packet offset address.

DATE1_COEFF11

DATE1_COEFF11 is the Closed Caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC42C	DATE1_COEFF11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	date_clf1 / date_clf2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:22]	RW reserved	reserve.
[21]	RW cc_enf1	Closed Caption Odd field switch control bit. 0: off; 1: open.
[20]	RW cc_enf2	Closed Caption Even field switch control bit. 0: off; 1: open.
[19:10]	RW date_clf1	Closed Caption Odd field configuration line.
[9:0]	RW date_clf2	Closed Caption Even field configuration line.

DATE1_COEFF12

DATE1_COEFF12 is the Closed Caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC430	DATE1_COEFF12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cc_f1data	cc_f2data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW cc_f1data	Closed Caption Odd field data.
[15:0]	RW cc_f2data	Closed Caption Even field data.

DATE1_COEFF13

DATE1_COEFF13 is the CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC434	DATE1_COEFF13	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cg_enf1	cg_enf2	cg_f1data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	reserved	reserve. Invalid for write, read as 0.
[21]	RW	cg_enf1	CGMS odd field switch control bit. 0: off; 1: open.
[20]	RW	cg_enf2	CGMS Even field switch control bit. 0: off; 1: open.
[19:0]	RW	cg_f1data	CGMS odd field data.

DATE1_COEFF14

DATE1_COEFF14 is the CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC438	DATE1_COEFF14	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cg_f2data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RW	reserved	reserve. Invalid for write, read as 0.
[19:0]	RW	cg_f2data	CGMS even field data.

DATE1_COEFF15

DATE1_COEFF15 is the WSS configuration register.

注意

WSS is only used in the 625-line system, and it is fixed at 23 lines.

Offset Address	Register Name	Total Reset Value
0xC43C	DATE1_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														wss_data	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	reserve. Invalid for write, read as 0.
[14]	RW	wss_en	WSS switch control bit. 0: off; 1: open.
[13:0]	RW	wss_data	WSS data.

DATE1_COEFF16

DATE1_COEFF16 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC440	DATE1_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vps_data	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC440	DATE1_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vps_data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[24]	RW vps_en	VPS switch control bit. 0: off; 1: open.
[23:0]	RW vps_data	VPS data, bit 23 to bit 0, the lowest bit is bit 0.

DATE1_COEFF17

DATE1_COEFF17 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC444	DATE1_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW vps_data	VPS data, bit 55 to bit 24, the lowest bit is bit 0.

DATE1_COEFF18

DATE1_COEFF18 is the VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC448	DATE1_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW vps_data	VPS data, bit 87 to bit 56, the lowest bit is bit 0.

DATE1_COEFF19

DATE1_COEFF19 is the VPS configuration register.

> **注意**
>
> VPS only supports 625 rows, fixed at 16 rows.

Offset Address	Register Name	Total Reset Value
0xC44C	DATE1_COEFF19	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vps_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	reserved	reserve. Invalid for write, read as 0.
[15:0]	RW	vps_data	VPS data, the 103rd bit to the 88th bit, the lowest bit is the 0th bit.

DATE1_COEFF20

DATE1_COEFF20 configures registers for Teletext.

Offset Address	Register Name	Total Reset Value
0xC450	DATE1_COEFF20	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC450	DATE1_COEFF20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[2]	RW tt06_enf1	Odd Field Line 6 Teletext switch control bit. 0: off; 1: open.
[1]	RW tt06_enf2	Line 6 of even field Teletext switch control bit. 0: off; 1: open.
[0]	RW tt05_enf2	Teletext switch control bit in line 5 of even field. 0: off; 1: open.

DATE1_COEFF21

DATE1_COEFF21 is the output matrix control register.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access Name	Description
[31:23]	RW reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	1							1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[22:20]	RW	dac5_in_sel	DAC5 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[19]	RO	reserved	reserve. Invalid for write, read as 0.
[18:16]	RW	dac4_in_sel	DAC4 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[15]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	1		1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[14:12]	RW	dac3_in_sel	DAC3 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[11]	RO	reserved	reserve. Invalid for write, read as 0.
[10:8]	RW	dac2_in_sel	DAC2 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[7]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	1																					

Bits	Access Name		Description
[6:4]	RW	dac1_in_sel	DAC1 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ
[3]	RO	reserved	reserve. Invalid for write, read as 0.
[2:0]	RW	dac0_in_sel	DAC0 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100ÿR/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ

DATE1_COEFF22

DATE1_COEFF22 is the DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC458	DATE1_COEFF22	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	video_phase_delta
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:11]	RW	reserved	reserve. Invalid for write, read as 0.
[10:0]	RW	video_phase_delta	DTO Initial phase configuration register.

DATE1_COEFF23

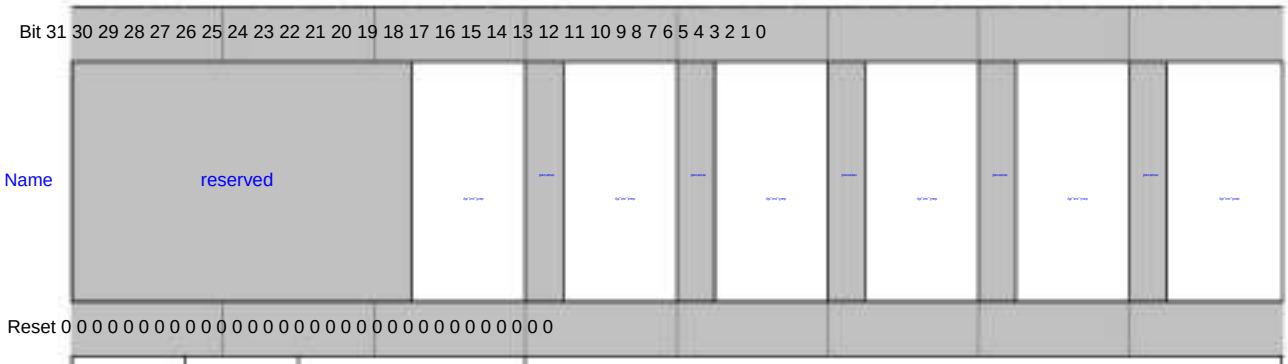
DATE1_COEFF23 is the VIDEO_OUT delay configuration register.

Offset Address	Register Name	Total Reset Value
0xC45C	DATE1_COEFF23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:23]	RW	reserved	reserve. Invalid for write, read as 0.
[22:20]	RW	dac5_out_dly	DAC5 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[19]	RO	reserved	reserve. Invalid for write, read as 0.
[18:16]	RW	dac4_out_dly	DAC4 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[15]	RO	reserved	reserve. Invalid for write, read as 0.

Offset Address	Register Name	Total Reset Value
0xC45C	DATE1_COEFF23	0x0000_0000



Bits	Access Name	Description
[14:12] RW	dac3_out_dly	DAC3 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[11] RO	reserved	reserve. Invalid for write, read as 0.
[10:8] RW	dac2_out_dly	DAC2 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[7]	RO reserved	reserve. Invalid for write, read as 0.
[6:4] RW	dac1_out_dly	DAC1 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.
[3]	RO reserved	reserve. Invalid for write, read as 0.
[2:0] RW	dac0_out_dly	DAC0 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.

DATE1_ISRMASK

DATE1_ISRMASK is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC480	DATE1_ISRMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1]	RW reserved	reserve. Invalid for write, read as 0.
[0]	RW tt_mask	Teletext interrupt mask bit. 0: Enable Teletext interrupt; 1: Shield Teletext interrupt.

DATE1_ISRSTATE

DATE1_ISRSTATE is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC484	DATE1_ISRSTATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1]	RW reserved	reserve. Invalid for write, read as 0.
[0]	W1C tt_status	Teletext interrupt flag. When DATE has read all the Teletext data, the interrupt flag will be pulled high. To clear the interrupt, you need to write 1 to this bit.

DATE1_ISR

DATE1_ISR is the interrupt register.

Offset Address	Register Name	Total Reset Value
0xC488	DATE1_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve. Invalid for write, read as 0.
[0]	RW	tt_int	Teletext interrupt register. tt_status Interrupt status after being masked by tt_mask. 0: no interrupt; 1: There is an interrupt.

DATE1_VERSION

DATE1_VERSION is the version register.

Offset Address	Register Name	Total Reset Value
0xC490	DATE1_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	reserve. Invalid for write, read as 0.

VOCTRL

VOCTRL is the VO control register. The surface bus applies for arbitration mode.

Offset Address	Register Name	Total Reset Value
0xCE00	VOCTRL	0x0000_0000

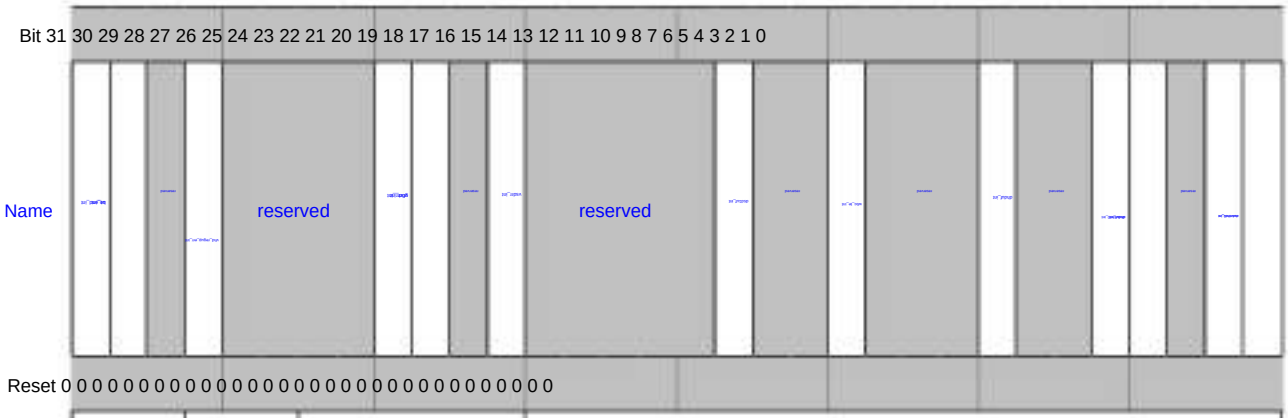
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				awid_cfg			outstd_wid			arid_cfg1			arid_cfg0			outstd_rid			arb_mode													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_ck_gt_en	VOU Clock gating enable. 0: Clock gating is off; 1: Internal clock gating of VOU is on.
[30]	RW	vo_id_sel	VOU read ID number selection 0: VOU selects No. 0 to read ID; 1: VOU selects No. 1 read ID
[29:28]	RO	reserved	reserve.
[27:24]	RW	awid_cfg	ID value written by AXI bus.
[23:22]	RO	reserved	reserve.
[21:20]	RW	bus_dbg_en	Bus test enable 00: bus normal working mode; 01: bus test read and write loopback working mode; 10: bus test write loopback working; Other: reserved.
[19:16]	RW	outstd_wid	AXI bus write ID outstanding
[15:12]	RW	arid_cfg1	No. 1 ID value read by AXI bus.
[11:8]	RW	arid_cfg0	The ID value of No. 0 read by the AXI bus.
[7:4]	RW	outstd_rid	AXI bus read ID outstanding.
[3:0]	RW	arb_mode	Arbitration mode for each surface bus data request inside VO. 0000: polling; 0001: graphic layer priority; others: reserved

WELLNESS

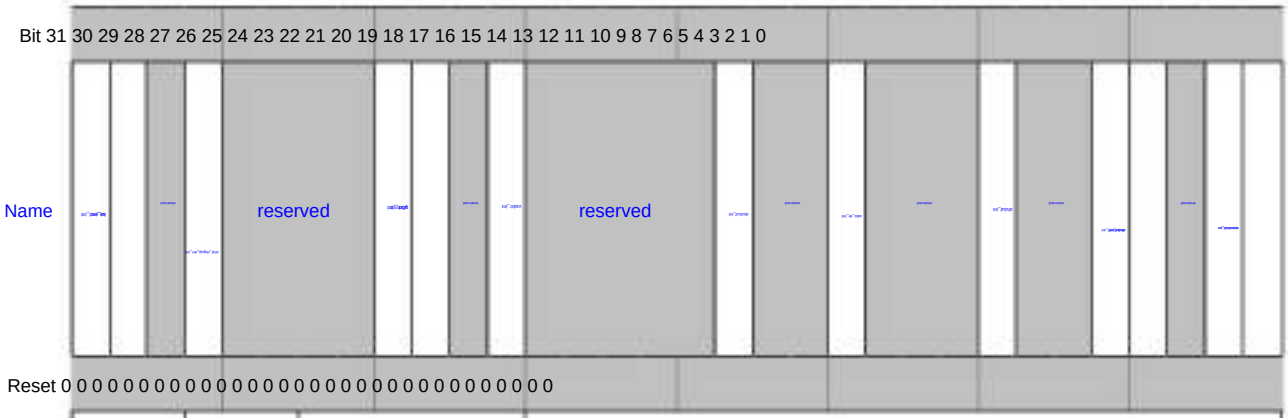
VOINTSTA is the VO interrupt status register. Read-only register.

Offset Address	Register Name	Total Reset Value
0xCE04	WELLNESS	0x0000_0000



Bits	Access	Name	Description
[31]	RO	be_int	Bus error interrupt. (AXI_Master) 0: no interrupt; 1: There is an interrupt.
[30]	RO	ut_end_int	UT frame complete interrupt.
[29]	RO	reserved	reserve.
[28]	RO	vhd_regup_err_int	VHD register update error interrupt.
[27:24]	RO	reserved	reserve.
[23]	RO	g0rr_int	G0 register update interrupt.
[22]	RO	vhdrr_int	VHD register update interrupt.
[21]	RO	reserved	reserve.
[20]	RO	vsdrr_int	VSD register update interrupt.
[19:15]	RO	reserved	reserve.
[14]	RO	dsd1uf_int	SD1 channel low bandwidth alarm interrupt.
[13:12]	RO	reserved	reserve.
[11]	RO	wbc_te_int	WBC Task Completion Interrupt
[10:8]	RO	reserved	reserve.
[7]	RO	dhduf_int	HD channel low bandwidth warning interrupt.
[6:5]	RO	reserved	reserve.
[4]	RO	dhdvtthd0_int	HD0 lane vertical timing interrupt 1.
[3]	RO	dsduf_int	SD channel low bandwidth warning interrupt.
[2]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xCE04	WELLNESS	0x0000_0000

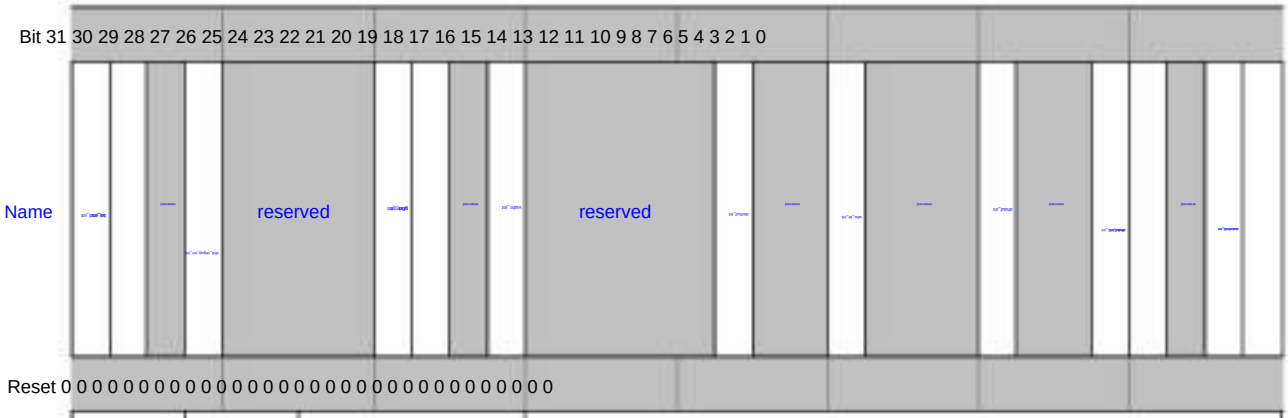


Bits	Access Name		Description
[1]	RO	dsdvtthd1_int	SD1 channel vertical timing interrupt.
[0]	RO	dsdvtthd0_int	SD0 channel vertical timing interrupt 1.

VOMSKINTSTA

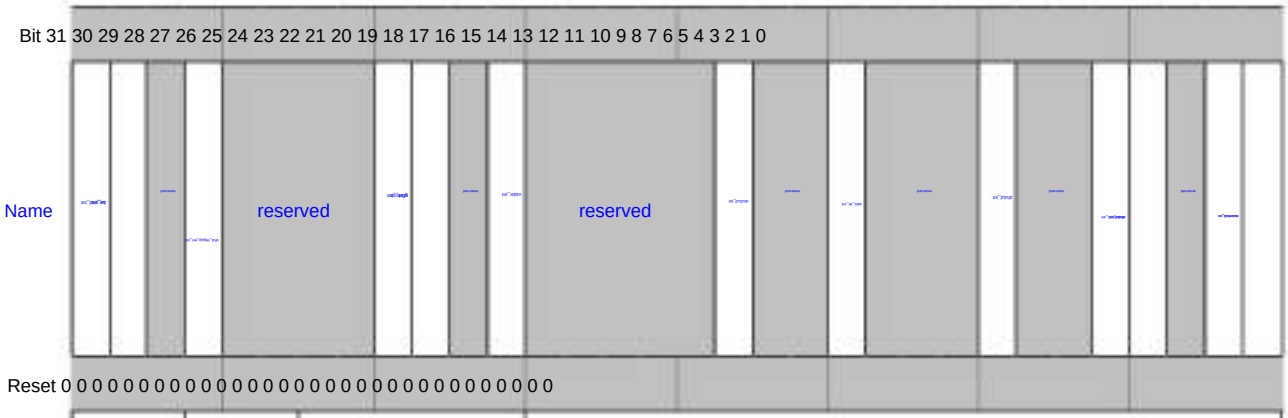
VOMSKINTSTA is the interrupt status register of VO passing Mask. Write 1 to clear.

Offset Address	Register Name	Total Reset Value
0xCE08	VOMSKINTSTA	0x0000_0000



Bits	Access Name		Description
[31]	RWC	be_int	Bus error interrupt. (AXI_Master) 0: no interrupt; 1: There is an interrupt.
[30]	R/WC	ut_end_int	UT frame complete interrupt.
[29]	RO	reserved	reserve.
[28]	RWC	vhd_regup_err_int	VHD register update error interrupt.

Offset Address	Register Name	Total Reset Value
0xCE08	VOMSKINTSTA	0x0000_0000

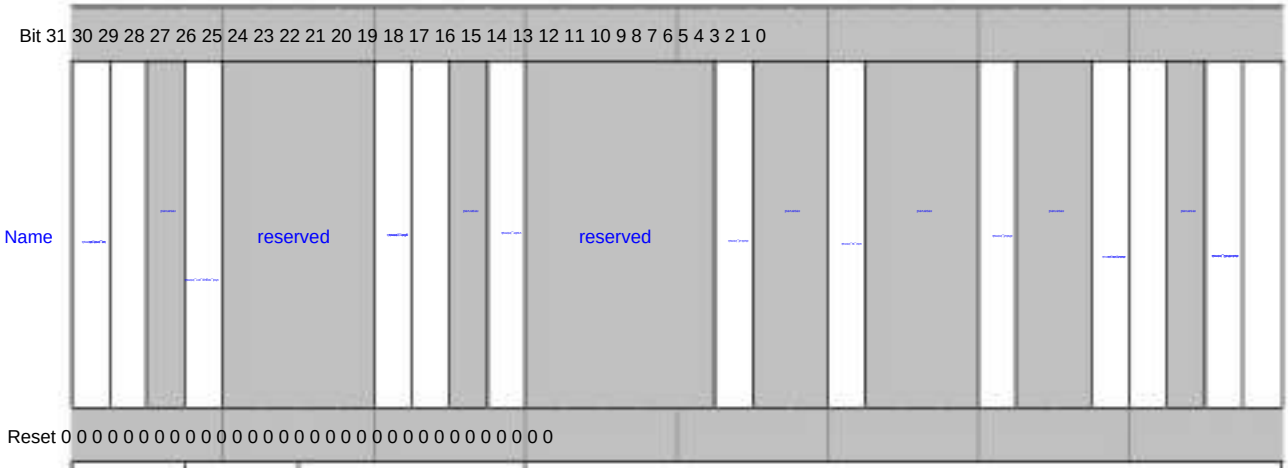


Bits	Access	Name	Description
[27:24]	RO	reserved	reserve.
[23]	RWC	g0rr_int	G0 register update interrupt.
[22]	RWC	vhdrr_int	VHD register update interrupt.
[21]	RO	reserved	reserve.
[20]	R/WC	vsdrr_int	VSD register update interrupt.
[19:15]	RO	reserved	reserve.
[14]	RW	dsd1uf_int	SD1 channel low bandwidth alarm interrupt.
[13:12]	RO	reserved	reserve.
[11]	RO	wbc_te_int	WBC Task Completion Interrupt
[10:8]	RO	reserved	reserve.
[7]	RO	dhduf_int	HD channel low bandwidth warning interrupt.
[6:5]	RO	reserved	reserve.
[4]	RO	dhdvtthd1_int	HD0 channel vertical timing interrupt 1.
[3]	RO	dsduf_int	SD channel low bandwidth warning interrupt.
[2]	RO	reserved	reserve.
[1]	RO	dsdvtthd1_int	SD1 channel vertical timing interrupt.
[0]	RO	dsdvtthd0_int	SD0 channel vertical timing interrupt 1.

VOINTMSK

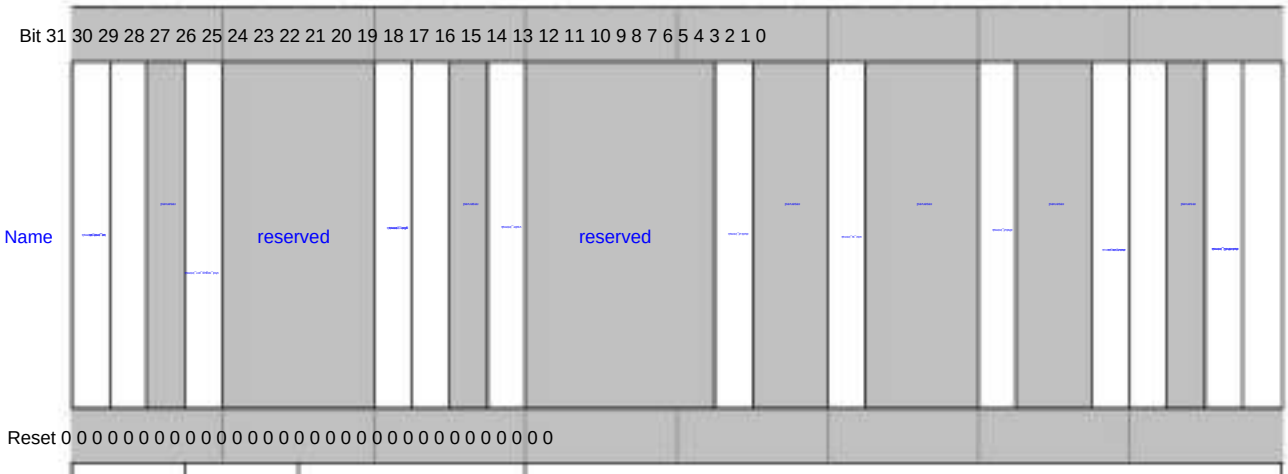
VOINTMSK is the VOU interrupt mask register. Corresponds to VOINTSTA. If the corresponding bit is 1, the interrupt is enabled; if it is 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0xCE0C	VOINTMSK	0x0000_0000



Bits	Access	Name	Description
[31]	RW	be_intmsk	Bus error interrupt. (AXI_Master) 0: no interrupt; 1: There is an interrupt.
[30]	RW	ut_end_intmsk	UT frame complete interrupt.
[29]	RO	reserved	reserve.
[28]	RWC	vhd_regup_err_int	VHD register update error interrupt. msk
[27:24]	RO	reserved	reserve.
[23]	RW	g0rr_intmsk	G0 register update interrupt.
[22]	RW	vhdrr_intmsk	VHD register update interrupt.
[21]	RO	reserved	reserve.
[20]	RW	vsdrr_intmsk	VSD register update interrupt.
[19:15]	RO	reserved	reserve.
[14]	RW	dsd1uf_intmsk	SD1 channel low bandwidth alarm interrupt.
[13:12]	RO	reserved	reserve.
[11]	RO	wbc_te_intmsk	WBC task complete interrupt
[10:8]	RO	reserved	reserve.
[7]	RW	dhduf_intmsk	HD channel low bandwidth warning interrupt.

Offset Address	Register Name	Total Reset Value
0xCE0C	VOINTMSK	0x0000_0000

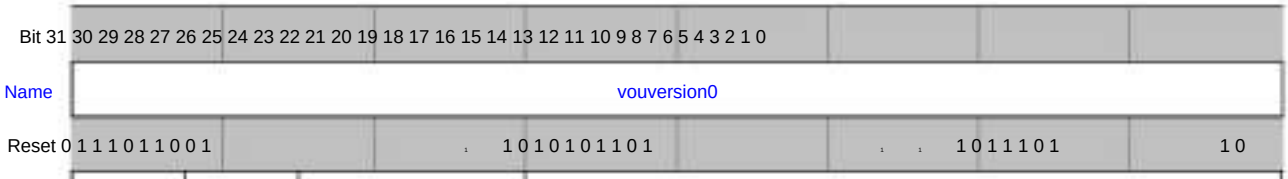


Bits	Access	Name	Description
[6:5]	RO	reserved	reserve.
[4]	RW	dhdvtthd1_intmsk	HD channel vertical timing interrupt 1.
[3]	RW	dsduf_intmsk	SD channel low bandwidth warning interrupt.
[2]	RO	reserved	reserve.
[1]	RW	dsdvtthd1_intmsk	SD1 channel vertical timing interrupt 2.
[0]	RW	dsdvtthd0_intmsk	SD0 lane vertical timing interrupt 1.

VOUVERSION1

VOUVERSION1 is the VOU version 1 register.

Offset Address	Register Name	Total Reset Value
0xCE10	VOUVERSION1	0x7675_6F76



Bits	Access	Name	Description
[31:0]	RO	vouversion0	VOU version register.

VOUVERSION2

VOUVERSION2 is the VOU version 2 register.

Offset Address	Register Name	Total Reset Value
0xCE14	VOUVERSION2	0x3030_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vouversion1																															
Reset	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vouversion1	VOU version register.

VOMUKHDATA

VOMUXDATA is the VO output interface check data (VOPINTEST) register.

Offset Address	Register Name	Total Reset Value
0xCE18	VOMUKHDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pin_test_mode								pin_test_data																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pin_test_en	Pin test mode enabled. 0: forbidden; 1: enable. The values of Vo_pdata, Vo_vsync, Vo_hsync and Vo_dv are respectively defined by bit[23:0], bit[26], bit[25] and bit[24] of this register.
[30:27]	RW	pin_test_mode	reserved.
[26]	RW	vsync_value	In test mode, vertical timing configuration value.
[25]	RW	hsync_value	In test mode, the horizontal timing configuration value.
[24]	RW	dv_value	In test mode, data valid timing configuration value.
[23:0]	RW	pin_test_data	Test mode, configure test data. All DACs use [9:0]. When the component width is greater than 8bit, the highest bit is the padding value. Example: 36bit output[35:24] = {[23:16]ÿ[23:20]}

VOMUX

VOMUX is the multiple selection register of VO output interface.

Offset Address	Register Name	Total Reset Value
0xCE1C	VOMUX	0x0004_001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hdmi_vid								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:23]	RW	reserved	reserve.
[22:16]	RW	hdmi_vid	The reverse enable register needs to be XORed with the timing reverse register in the interface register of INTF, so that the real HDMI input interface timing reverse requirement can be obtained. bit[22] 0: vsync reverse is disabled; 1: vsync reverse is enabled bit[21] 0: hsync reverse is disabled; 1: hsync reverse is enabled bit[20] 0: dv reverse is disabled Enable; 1: dv reverse enable; bit[19]: reserved; bit[18:17]: (default: 100) HDMI video output format selection. The choice of RGB and YCbCr is obtained by configuring the DHD channel. 00: YCbCr444, 30bits synchronous separation mode; 01: RGB444, 30bits synchronous separation mode; 10: YCbCr422, 20bits synchronous separation mode 11: YCbCr422, 10bits synchronous separation mode; bit[16] 0: DHD1 output; 1: DHD0 output;
[15:0]	RO	reserved	reserve.

VGACSCIDC

VGACSCIDC Input DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE24	VGACSCIDC	0x07C3_0180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cscidc2										cscidc1										cscidc0			
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	1					1	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28]	RW	csc_mode	CSC conversion mode. 0: YUV2RGB 601 (SD); 1: YUV2RGB 709 (g HD).
[27]	RW	csc_en	CSC is enabled. 0: forbidden; 1: enable.
[26:18]	RW	cscidc2	Input component 2 DC parameters, MSB is the sign bit. complement representation.
[17:9]	RW	cscidc1	Input component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscidc0	Input component 0 DC parameters, MSB is the sign bit. complement representation.

VGACSCODC

VGACSCODC Output DC component register for color space conversion. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE28	VGACSCODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscodc2										cscodc1						cscodc0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:18]	RW	cscodc2	Output component 2 DC parameters, MSB is the sign bit. complement representation.

Offset Address	Register Name	Total Reset Value
0xCE28	VGACSCODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[17:9]	RW	cscodc1	Output component 1 DC parameter, MSB is the sign bit. complement representation.
[8:0]	RW	cscodc0	Output component 0 DC parameters, MSB is the sign bit. complement representation.

VGACSCP0

VGACSCP0 is the color space conversion parameter 0 register. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE2C	VGACSCP0	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp01	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp00	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VGACSCP1

VGACSCP1 is the color space conversion parameter 1 register. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE30	VGACSCP1	0x0100_015E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							cscp10									—									cscp02						
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp10	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp02	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VGACSCP2

VGACSCP2 is the color space conversion parameter 2 register. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE34	VGACSCP2	0x1FAA_1F4E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							cscp12									—									cscp11						
Reset	0	0	0	1	1	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	1	1	1	1	0	1	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp12	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp11	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VGACSCP3

VGACSCP3 is the color space conversion parameter 3 register. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE38	VGACSCP3	0x01BB_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—						cscp21										—										cscp20					
Reset	0	0	0	0	0	0	0	1	1	0	1						1	1	0	1												

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	cscp21	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.
[15:13]	RO	reserved	reserve.
[12:0]	RW	cscp20	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VGACSCP4

VGACSCP4 is the color space conversion parameter 4 register. Instant register.

Offset Address	Register Name	Total Reset Value
0xCE3C	VGACSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cscp22		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	cscp22	5.8 Data format: 1bit sign bit, 4bit integer bit, 8bit decimal place. complement representation.

VOPARAUP

VOPARAUP Enable register for scaling/GAMMA/ACC coefficient update. The software needs to configure the coefficient address and the coefficient update enable, and the VOU will read the coefficients from the DDR through the AXI Master and store them inside the VOU.

Offset Address	Register Name	Total Reset Value
0xCE40	VOPARAUP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	wbc_vcoef_upd	Whether WBC2 vertical luma and vertical chroma filter coefficients need to be updated. Automatically cleared after hardware update. 0: no update; 1: update.
[6]	RW	wbc_hcoef_upd	Whether WBC2 horizontal luma and horizontal chroma filter coefficients need to be updated. Automatically cleared after hardware update. 0: no update; 1: update.
[5]	RW	dhd_gamma_upd	Whether the DHD Gamma correction operation lookup table needs to be updated. Automatically cleared after hardware update. 0: no update; 1: update.
[4]	RW	video_acc_upd	Whether the video layer ACC operation lookup table needs to be updated. Automatically cleared after hardware update. 0: no update; 1: update.
[3:2]	RO	reserved	reserve.
[1]	RW	vhd_vcoef_upd	Whether the VHD vertical luma and vertical chroma filter coefficients need to be updated. Automatically cleared after hardware update. 0: no update; 1: update.
[0]	RW	vhd_hcoef_upd	Whether the VHD horizontal luma and horizontal chroma filter coefficients need to be updated. Automatically cleared after hardware update. 0: no update; 1: update.

VHDHCOEFAD

VHDHCOEFAD is the VHD horizontal luma, horizontal chroma filter coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE44	VHDHCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	The coefficients are placed at the start address of Local Memory.

VHDVCOEFAD

VHDVCOEFAD is VHD vertical luma, horizontal chroma filter coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE48	VHDVCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	The coefficients are placed at the start address of Local Memory.

WBC2HCOEFAD

WBC2HCOEFAD is WBC2 horizontal luma, horizontal chroma filter coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE58	WBC2HCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	The coefficients are placed at the start address of Local Memory.

WBC2VCOEFAD

WBC2VCOEFAD is the WBC2 vertical luma, horizontal chroma filter coefficient address register.

Offset Address	Register Name	Total Reset Value
0xCE5C	WBC2VCOEFAD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	coef_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	coef_addr	The coefficients are placed at the start address of Local Memory.

VHDHLCOEF

VHDHLCOEF is the VHD horizontal luminance scaling filter coefficient register.

Each filter coefficient is 10bit, which is composed of a sign bit and a decimal place, the highest bit is the sign bit, and the lower 9 bits are the absolute value of the decimal place. Since the coefficients are stored in the on-chip memory, the default value is indeterminate.

The VHD horizontal luminance scaling filter is 8-order 32-phase, because of the symmetrical relationship, a total of 17 sets of coefficients are stored, that is, 8-order coefficients of 0-16 phases. Each register address contains two 10bit coefficients, so the 8th order coefficient of a phase requires four 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xD000ÿ0xD10C	VHDHLCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	hlcoefn2	reserved	hlcoefn1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access Name		Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	hlcoefn2	Horizontal luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the second-order coefficient; when the register address bit[3:0] is 0x4, it means the fourth-order coefficient; when the register address bit[3:0] is 0x8 , indicating the sixth-order coefficient; when the register address bit[3:0] is 0xC, it indicates the eighth-order coefficient.
[15:10]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xD000ÿ0xD10C	VHDHLCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	hlcoefn2	reserved	hlcoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[9:0]	RW	hlcoefn1	Horizontal luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the first-order coefficient; when the register address bit[3:0] is 0x4, it means the third-order coefficient; when the register address bit[3:0] is 0x8 , indicating the fifth-order coefficient; when the register address bit[3:0] is 0xC, it indicates the seventh-order coefficient.

VHDHCCOEF

VHDHCCOEF is the VHD horizontal chroma scaling filter coefficient register. The storage format refers to VHDHLCOEF.

The VHD horizontal chroma scaling filter is 4th order and 32 phases. Because of the symmetry, 17 groups of coefficients are stored in total, that is, the 4th order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, so the 4th order coefficient of a phase requires two 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xD200ÿ0xD284	VHDHCCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	hccoefn2	reserved	hccoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	hccoefn2	Horizontal chroma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the second-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the fourth-order coefficient.
[15:10]	RO	reserved	reserve.
[9:0]	RW	hccoefn1	Horizontal chroma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the first-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the third-order coefficient.

VHDVLCOEF

VHDVLCOEF is the VHD vertical brightness scaling filter coefficient register. The storage format refers to VHDHLCOEF.

VHD vertical luminance scaling filter is 6-order 32-phase, because of the symmetry relationship, a total of 17 sets of coefficients are stored, that is, 4th-order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, and a phase 6-order coefficient requires four 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xD400ÿ0xD50C	VHDVLCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vlcoefn2	reserved	vlcoefn1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	vlcoefn2	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the second-order coefficient; when the register address bit[3:0] is 0x4, it means the fourth-order coefficient; when the register address bit[3:0] is 0x8 , indicating the sixth-order coefficient; when the register address bit[3:0] is 0xC, it is a reserved bit.
[15:10]	RO	reserved	reserve.
[9:0]	RW	vlcoefn1	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the first-order coefficient; when the register address bit[3:0] is 0x4, it means the third-order coefficient; when the register address bit[3:0] is 0x8 , indicating the fifth-order coefficient; when the register address bit[3:0] is 0xC, it is a reserved bit.

VHDVCCOEF

VHDVCCOEF is the VHD vertical chroma scaling filter coefficient register. The storage format refers to VHDHLCOEF.

The VHD vertical chroma scaling filter is 4th order 32 phases. Because of the symmetry relationship, 17 groups of coefficients are stored in total, that is, the 4th order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, so the 4th order coefficient of a phase requires two 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xD600ÿ0xD684	VHDVCCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	vccoefn2	reserved	vccoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	vccoefn2	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the second-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the fourth-order coefficient.
[15:10]	RO	reserved	reserve.
[9:0]	RW	vccoefn1	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the first-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the third-order coefficient.

WBCHLCOEF

WBCHLCOEF is the WBC horizontal luminance scaling filter coefficient register.

Each filter coefficient is 10bit, composed of a sign bit and a decimal place, the highest bit is the sign bit, and the lower 9 bits are the absolute value of the decimal place. Since the coefficients are stored in the on-chip memory, the default value is indeterminate.

The WBC horizontal luminance scaling filter is 8-order 32-phase. Due to the symmetrical relationship, 17 sets of coefficients are stored in total, that is, the 8-order coefficients of 0-16 phases. Each register address contains two 10bit coefficients, so the 8th order coefficient of a phase requires four 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xE000ÿ0xE10C	WBCHLCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	hlcoefn2	reserved	hlcoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xE000ÿ0xE10C	WBCHLCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hlcoefn2	reserved	hlcoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[25:16]	RW	hlcoefn2	Horizontal luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the second-order coefficient; when the register address bit[3:0] is 0x4, it means the fourth-order coefficient; when the register address bit[3:0] is 0x8 , indicating the sixth-order coefficient; when the register address bit[3:0] is 0xC, it indicates the eighth-order coefficient.
[15:10]	RO	reserved	reserve.
[9:0]	RW	hlcoefn1	Horizontal luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the first-order coefficient; when the register address bit[3:0] is 0x4, it means the third-order coefficient; when the register address bit[3:0] is 0x8 , indicating the fifth-order coefficient; when the register address bit[3:0] is 0xC, it indicates the seventh-order coefficient.

WBCHCCOEF

WBCHCCOEF is the WBC horizontal chroma scaling filter coefficient register. The storage format refers to WBCHLCOEF. The VHD horizontal chroma scaling filter is 4th order 32 phases. Because of the symmetry, 17 groups of coefficients are stored, namely 4th order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, so the 4th order coefficient of a phase requires two 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xE200ÿ0xE284	WBCHCCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hccoefn2	reserved	hccoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	hccoefn2	Horizontal chroma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the second-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the fourth-order coefficient.

Offset Address	Register Name	Total Reset Value
0xE200ÿ0xE284	WBCHCCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	hccoefn2	reserved	hccoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:10]	RO	reserved	reserve.
[9:0]	RW	hccoefn1	Horizontal chroma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the first-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the third-order coefficient.

WBCVLCOEEF

WBCVLCOEF is the WBC vertical brightness scaling filter coefficient register. The storage format refers to WBCHLCOEF. VHD vertical luminance scaling filter is 6-order 32-phase, because of the symmetry relationship, a total of 17 sets of coefficients are stored, that is, 4th-order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, and a phase 6-order coefficient requires four 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xE400ÿ0xE50C	WBCVLCOEEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	vlcoefn2	reserved	vlcoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	vlcoefn2	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the second-order coefficient; when the register address bit[3:0] is 0x4, it means the fourth-order coefficient; when the register address bit[3:0] is 0x8 , indicating the sixth-order coefficient; when the register address bit[3:0] is 0xC, it is a reserved bit.
[15:10]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0xE400ÿ0xE50C	WBCVLCOEEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	vlcoefn2	reserved	vlcoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[9:0]	RW	vlcoefn1	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0, it means the first-order coefficient; when the register address bit[3:0] is 0x4, it means the third-order coefficient; when the register address bit[3:0] is 0x8 , indicating the fifth-order coefficient; when the register address bit[3:0] is 0xC, it is a reserved bit.

WBCVCCOEF

WBCVCCOEF is the WBC vertical chroma scaling filter coefficient register. The storage format refers to WBCHLCOEF.

The VHD vertical chroma scaling filter is 4th order 32 phases. Because of the symmetry relationship, 17 groups of coefficients are stored in total, that is, the 4th order coefficients of 0~16 phases. Each register address contains two 10bit coefficients, so the 4th order coefficient of a phase requires two 32bit register addresses.

Offset Address	Register Name	Total Reset Value
0xE600ÿ0xE684	WBCVCCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	vccoefn2	reserved	vccoefn1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	vccoefn2	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the second-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the fourth-order coefficient.
[15:10]	RO	reserved	reserve.
[9:0]	RW	vccoefn1	Vertical luma scaling filter coefficient. When the register address bit[3:0] is 0x0 or 0x8, it indicates the first-order coefficient; when the register address bit[3:0] is 0x4 or 0xC, it indicates the third-order coefficient.

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12 audio encoding

12.1 Overview

Voice hardware acceleration (VOIE, VoiceEngine) module realizes 16bit linear PCM (pulse code modulation, pulse code modulation) audio data encoding and compression output, supports 8/16/32/48KHz sampling frequency input, G726, G711A/U, ADPCM (adaptive difference pulse code modulation, adaptive differential pulse code modulation) three kinds of speech coding protocol coding output.

12.2 Features

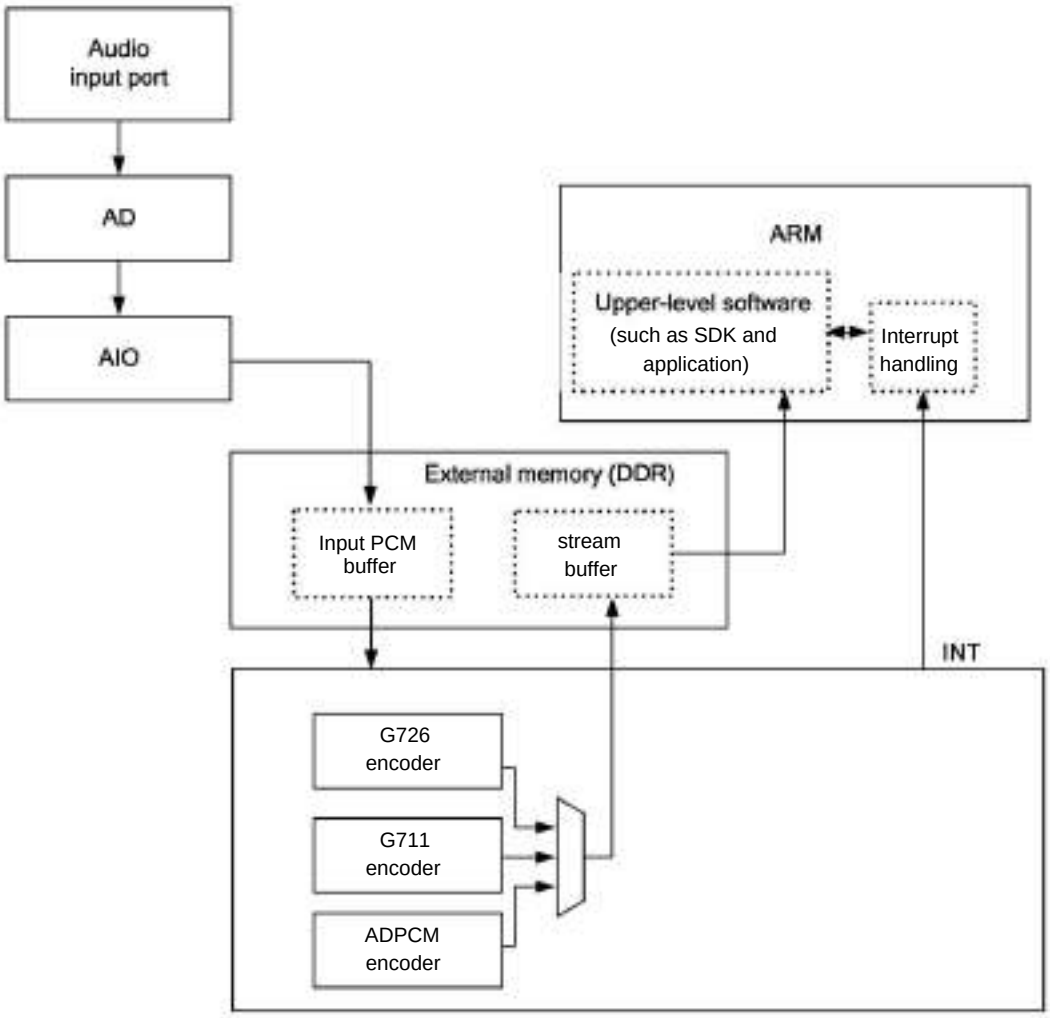
The VOIE module has the following features:

- The input audio sample format supports 16bits linear PCM, little endian mode input. The sampling frequency supports 8/16/32/48KHz. Audio frame frame length supports 10/20/30/40/50/60ms.
- The number of input audio channels per frame is configurable, and supports a maximum of 17 channels of audio input per frame (including 16 channels of encoded output and 1 channel of intercom). The number of input samples per frame is supported from 80 to 2880 (integer multiples of 80). Support ITU-G.726 protocol 40, 32, 24, 16 kbit/s four encoding compression rates. Support ITU-G.711A/U protocol encoding output. Support ADPCM_DVI4, ADPCM_ORG_DVI4 two encapsulation formats ADPCM encoding output. Encoding output supports HiSilicon frame header. Support to check the input frame, discard the wrong frame and report the interrupt. Supports checking the input frame length and encoding mode, discarding frames that do not meet the configuration specifications and reporting interruptions. Support multi-frame continuous encoding.

12.3 Functional description

The functional block diagram of VOIE is shown in Figure 12-1 .

Figure 12-1 VOIE functional block diagram



VOIE consists of three encoder modules: G726 Encoder, G711 Enocder and ADPCM Enocder. According to the configuration encoding mode, select the corresponding encoder to work.

Before a frame encoding starts, the voice data is input through AD, and then input into the voice data buffer buffer by the audio interface (AIO) (see AIO work instructions for details), and then store the data in DDR through DMA for VOIE to start hardware encoding. The start of a frame encoding is configured by the software. After the encoding is completed, VOIE stores the code stream in the corresponding buffer area of DDR; and reports an interruption to complete the encoding of a frame of voice data.

For the corresponding configuration values of various encoding modes, please refer to "12.6 Register Description".

12.4 Working method

VOIE first reads a frame linked list and voice frame data from DDR, and writes the code stream into DDR after passing through the encoder.

Before starting VOIE for voice encoding, the software needs to allocate the following three types of buffers in the external memory (DDR SDRAM):

Input voice data buffer: VOIE

will read the voice data to be encoded from this buffer during encoding. This buffer is written by DMA.

Encoding configuration linked list

buffer: After VOIE is started and before encoding starts, it reads the configuration information of the current channel from the buffer, including data source address, destination address, channel variable address, next channel linked list address and encoding

control configuration

information . Channel variable buffer: VOIE will read the channel variable and verification information of the current channel from this buffer during encoding (G711 protocol encoding does not need such information), and refresh it

after encoding is completed. For the configuration structure of the linked list and channel variables, please refer to "12.7 Linked List Structure Description (Attachment)". G726_check in the table is all (total 11) 32-bit channel variable registers in G.726 coding

mode to perform non-carry accumulation; ADPCM_check is consistent with the value of 32-bit channel variable registers configured in ADPCM coding mode.

Note: Since **ADPCM_ORG_DVI4** does not transmit predicted values, it may cause abnormalities when network packets are lost. Therefore, in the application of audio stream network transmission, it is not recommended to use this protocol encoding.

12.5 Register overview

The VOIE register overview is shown in Table 12-1 .

Table 12-1 VOIE register overview (base address is 0x2064_0000)

offset address name		describe	page number
0x0000	VOIE_INTSTAT interrupt status register		12-4
0x0004 VOIE_INTMASK interrupt mask register			12-5
0x0008 VOIE_RAWINT Status register before masking			12-6
0x000C PATH_INTCLR		Interrupt Clear Register	12-7
0x0010	VIOE_START	Encoding start signal register	12-8
0x0014	VOIE_OUTSTDING outstanding configuration register		12-9
0x0020 PATH_MODE		VOIE working mode register	12-9
0x0028	PATH_CFG	The first linked list address register	12-10
0x0030	PATH_LLICFG0	Linked list member register (SrcPhyAddr)	12-11
0x0034	PATH_LLICFG1	Linked list member register (DstPhyAddr)	12-11
0x0038	PATH_LLICFG2	Linked list member register (StatePhyAddr)	12-11
0x003C	PATH_LLICFG3	Linked list member register (NextLLiAddr)	12-12
0x0040	PATH_LLICFG4	Linked list member register (StCtrl, encoding control) 12-12	
0x0050	VOIE_LISTATE0	G726 encoding channel variable register 0	12-14

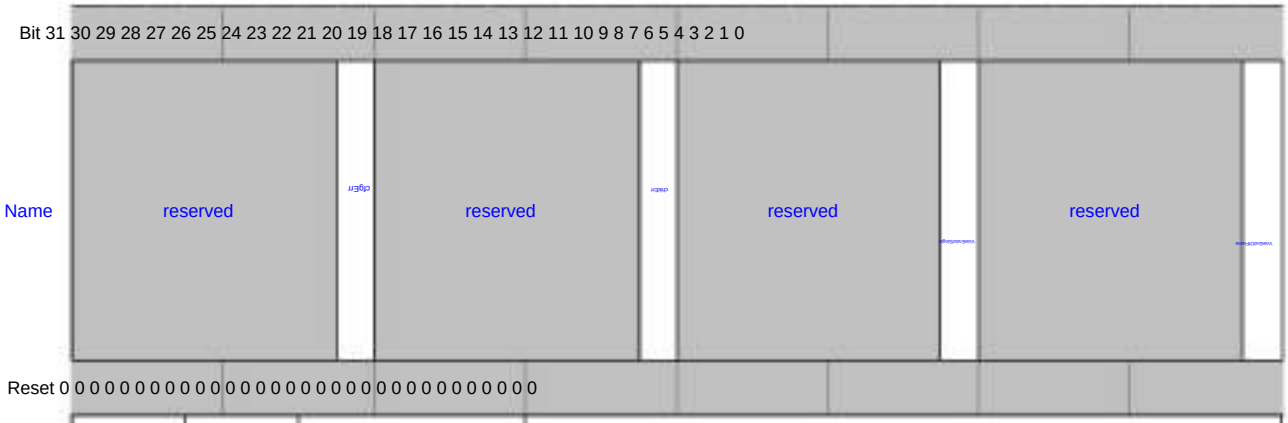
offset address name		describe	page number
0x0054	VOIE_LISTATE1	G726 encoding channel variable register 1	12-14
0x0058	VOIE_LISTATE2	G726 encoding channel variable register 2	12-15
0x005C VOIE_LLISTATE3		G726 encoding channel variable register 3	12-15
0x0060	VOIE_LISTATE4	G726 encoding channel variable register 4	12-16
0x0064	VOIE_LISTATE5	G726 encoding channel variable register 5	12-16
0x0068	VOIE_LISTATE6	G726 encoding channel variable register 6	12-17
0x006C VOIE_LLISTATE7		G726 encoding channel variable register 7	12-17
0x0070	VOIE_LISTATE8	G726 encoding channel variable register 8	12-18
0x0074	VOIE_LISTATE9	G726 encoding channel variable register 9	12-19
0x0078	VOIE_LISTATE10	G726 encoding channel variable register 10	12-19
0x007C VOIE_STATE_CHK0 G726 channel variable check register			12-20
0x0080	VOIE_LLISTATE11 ADPCM encoding channel variable register 11		12-20
0x0084	VOIE_STATE_CHK1 ADPCM channel variable check register		12-20

12.6 Register Description

PATH_INTSTAT

VOIE_INTSTAT is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	PATH_INTSTAT	0x0000_0000

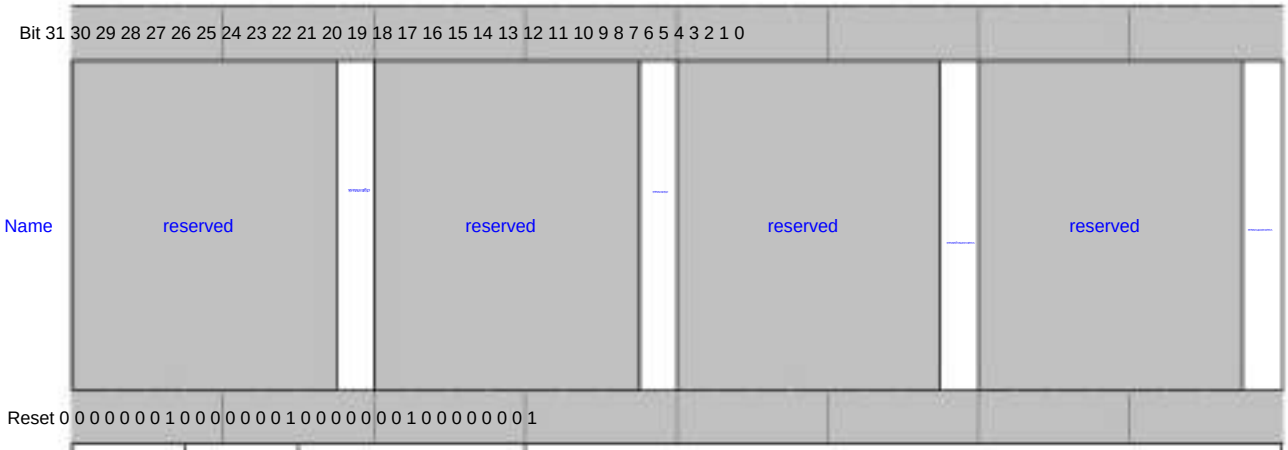


Bits	Access Name		Description
[31:25] RO		reserved	reserve.
[24] RO		cfgErr	Configuration error flag. 0: The configuration is correct; 1: Configuration error.
[23:17] RO		reserved	reserve.
[16] RO		chkErr	Check for error flags. 0: channel variable verification is correct; 1: channel variable verification error.
[15:9] RO		reserved	reserve.
[8]	RO	VoieEndofSingle	Single-pass encoding end flag. 0: Single-channel encoding has not ended; 1: End of single-channel encoding.
[7:1] RO		reserved	reserve.
[0]	RO	VoieEndOfFrame	Frame encoding end flag. 0: The encoding of the current frame has not ended; 1: Encoding of the current frame ends.

PATH_INTMASK

VOIE_INTMASK is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0004	PATH_INTMASK	0x0101_0101

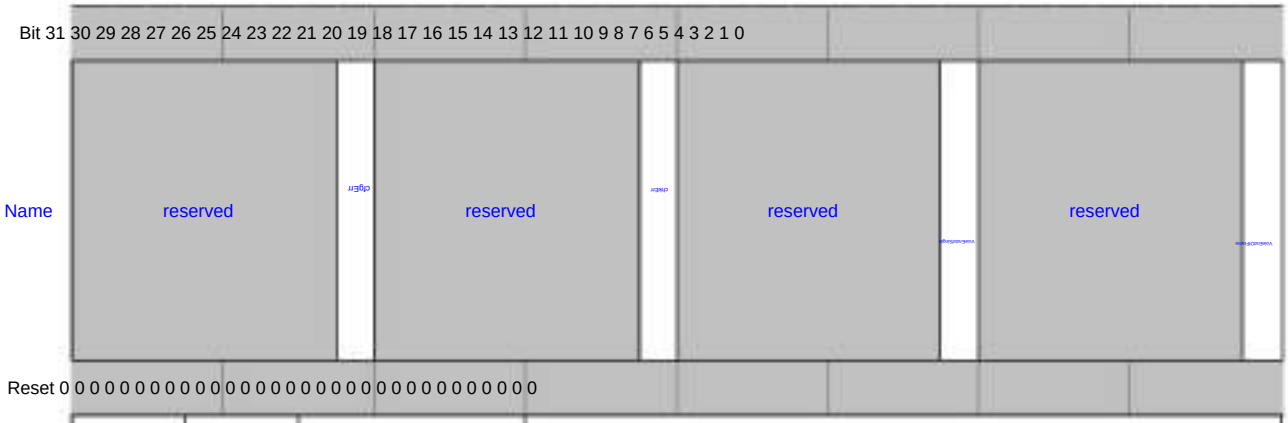


Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	cfgErrMask	Configuration error flag mask enable. 0: interrupt mask enable; 1: Interrupt masking off.
[23:17]	RO	reserved	reserve.
[16]	RW	chkErrMask	Check error flag mask enable. 0: interrupt mask enable; 1: Interrupt masking off.
[15:9]	RO	reserved	reserve.
[8]	RW	VoieEndofSingleM	Single-channel encoding end mask enable. 0: interrupt mask enable; ask 1: Interrupt masking off.
[7:1]	RO	reserved	reserve.
[0]	RW	VoieEndOfPicMas	Frame encoding end mask enable. 0: interrupt mask enable; k 1: Interrupt masking off.

PATH_RAWINT

VOIE_RAWINT is the status register before masking.

Offset Address	Register Name	Total Reset Value
0x0008	PATH_RAWINT	0x0000_0000

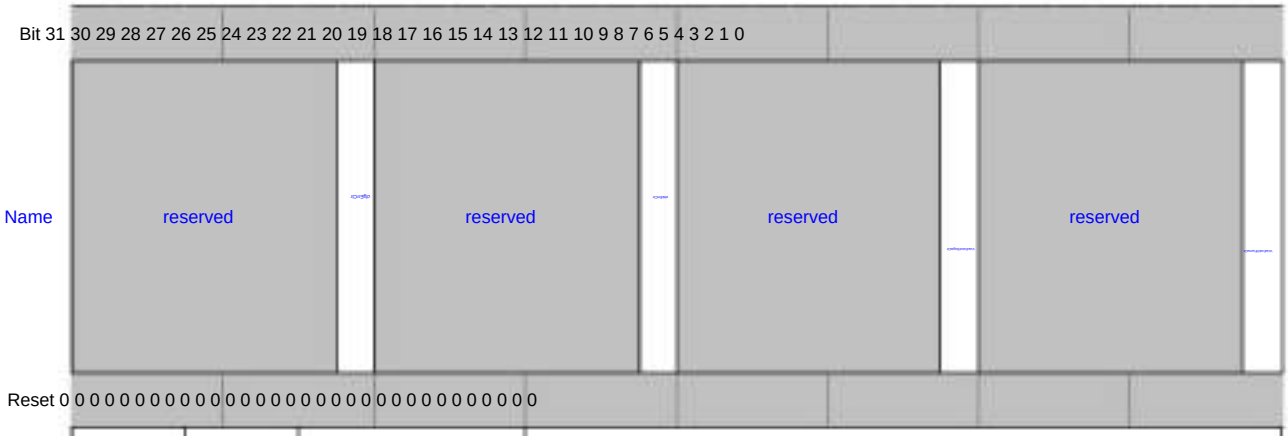


Bits	Access Name		Description
[31:25] RO		reserved	reserve.
[24] RO		cfgErr	Configuration error flag. 0: The configuration is correct; 1: Configuration error.
[23:17] RO		reserved	reserve.
[16] RO		chkErr	Check for error flags. 0: channel variable verification is correct; 1: channel variable verification error.
[15:9] RO		reserved	reserve.
[8]	RO	VoieEndofSingle	Single-pass encoding end flag. 0: Single-channel encoding is the end; 1: The encoding of the current channel is finished.
[7:1] RO		reserved	reserve.
[0]	RO	VoieEndOfFrame	Frame encoding end flag. 0: The encoding of the current frame has not ended; 1: Encoding of the current frame ends.

PATH_INTCLR

VOIE_INTCLR is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x000C	PATH_INTCLR	0x0000_0000



Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	WC	cfgErrClr	Configure error source interrupt clear. write 1 clear
[23:17]	RO	reserved	reserve.
[16]	WC	chkErrClr	Channel variable check error flag source interrupt clear. write 1 clear
[15:9]	RO	reserved	reserve.
[8]	WC	VoieEndofSingleClr	Single-channel encoding end source interrupt clear. write 1 clear
[7:1]	RO	reserved	reserve.
[0]	WC	VoieEndOfFrameClr	The source interrupt is cleared at the end of frame encoding. write 1 clear

VIOE_START

VIOE_START is the encoding start signal register.

Offset Address	Register Name	Total Reset Value
0x0010	VIOE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:1] RO	reserved	reserve.
[0] WO Start		Encode start signal. 0: encoding not started 1: Encoding start

PATH_OUTSTDING

VOIE_OUTSTDING is the outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	PATH_OUTSTDING	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														voieoutstd	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access Name	Description
[31:4] RO	reserved	reserve.
[3:0] RW	voieoutstd	Configure the outstanding depth of the AXI interface (supports 0 to 7 configurations).

PATH_MODE

VOIE_MODE is the VOIE working mode register.

Offset Address	Register Name	Total Reset Value
0x0020	PATH_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RW	memClkGateEn	Memory clock gating enable. Note: This function is not open, no configuration is required, and it is invalid.
[17:16]	RW	clkGateEn	Clock gating enable. Note: No configuration is required and invalid.
[15:9]	RO	reserved	reserve.
[8]	RW	accesslockEn	Internal configuration lock enable. Note: No configuration is required and invalid.
[7:2]	RO	reserved	reserve.
[1:0]	RW	timeEn	Timeout detection is enabled. Note: No configuration is required and invalid.

PATH_CFG

VOIE_CFG is the first linked list address register.

Offset Address	Register Name	Total Reset Value
0x0028	PATH_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AddrOfFirstLLI																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	AddrOfFirstLLI	Store the address of the first linked list of the current speech frame. Note: **128bit** alignment is required for configuration before encoding starts .

PATH_LLICFG0

VOIE_LLICFG0 is the linked list member register (SrcPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0030	PATH_LLICFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SrcPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	SrcPhyAddr	The starting physical address of the speech frame to be encoded stored in DDR requires 128bit address alignment. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.

PATH_LLICFG1

VOIE_LLICFG1 is a linked list member register (DstPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0034	PATH_LLICFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DstPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	DstPhyAddr	The encoded code stream is output to the physical address of DDR, and the 128bit address is aligned. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.

PATH_LLICFG2

VOIE_LLICFG2 is a linked list member register (StatePhyAddr).

Offset Address	Register Name	Total Reset Value
0x0038	PATH_LLICFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	StatePhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	StatePhyAddr	The physical address of the channel variable stored in DDR during encoding requires 128bit address alignment. It must be configured during G726 and ADPCM encoding; channel variables are not used during G711 encoding, so it is not necessary to configure. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.

PATH_LLICFG3

VOIE_LLICFG3 is the linked list member register (NextLLiAddr).

Offset Address	Register Name	Total Reset Value
0x003C	PATH_LLICFG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NextLLiAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	NextLLiAddr	The storage address of the next channel linked list, 128bit address alignment. If the current channel is the last channel of this frame, configure the address of the next linked list as 0x00000000; otherwise, it is not allowed to configure as 0. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.

PATH_LLICFG4

VOIE_LLICFG4 is the linked list member register (StCtrl, encoding control).

Offset Address	Register Name	Total Reset Value
0x0040	PATH_LLICFG4	0x0000_0081

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	SamplesPerFrame	Codec	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	SamplesPerFrame	The number of audio samples contained in the current speech frame: 80-2880 (and an integer multiple of 80). It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.
[15:8]	RO	Codec	Encoding type configuration. 0x01ÿG711 Alawÿ 0x02ÿG711 Shameÿ 0x03ÿADPCM_DIV4ÿ 0x04ÿG726_16kbpsÿ 0x05ÿ G726_24kbpsÿ 0x06ÿG726_32kbpsÿ 0x07ÿG726_40kbpsÿ 0x24ÿMEDIA_G726_16kbpsÿ 0x25ÿMEDIA_G726_24kbpsÿ 0x26ÿ MEDIA_G726_32kbpsÿ 0x27ÿMEDIA_G726_40kbpsÿ 0x43: ADPCM_ORG_DIV4; Others: illegal configuration, if VOIE receives other configurations, it will report a configuration error and interrupt. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.

Offset Address	Register Name	Total Reset Value
0x0040	PATH_LLICFG4	0x0000_0081

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SamplesPerFrame																Codec														reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Access Name		Description
[7]	RW	hisi_head	The output code stream Hisilicon frame header is enabled. 0: Does not contain HiSilicon frame header; 1: The code stream contains the HiSilicon frame header. The default configuration is 0x1. It is written into the corresponding linked list DDR address by software before encoding starts, and loaded by AXI bus after encoding starts. Note: This is only for reading back when debugging.
[6:0]	RO	reserved	Keep the extension.

VOIE_LISTATE0

VOIE_LLISTATE0 is channel variable register 0 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0050	VOIE_LISTATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A1																A2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	A1	G726 Encoded channel variable, second order pole predictor coefficient 1.
[15:0]	RO	A2	G726 Encoded channel variable, second order pole predictor coefficient 2.

VOIE_LISTATE1

VOIE_LLISTATE1 is the channel variable register 1 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0054	VOIE_LISTATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AP																reserved												PK1	PK2	reserved			TD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:22]	RO	AP	G726 encoding channel variable, delay speed control parameter.
[21:16]	RO	reserved	reserve.
[15]	RO	PK1	G726 coded channel variable, delay is 1 DQ+SEZ sign bit.
[14]	RO	PK2	G726 coded channel variable, delay is 2 DQ+SEZ sign bit.
[13:1]	RO	reserved	reserve.
[0]	RO	TD	G726 encoding channel variable, single tone detection signal.

VOIE_LISTATE2

VOIE_LLISTATE2 is channel variable register 2 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0058	VOIE_LISTATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B1																B2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	B1	G726 coded channel variable, sixth order zero predictor coefficient 1.
[15:0]	RO	B2	G726 coded channel variable, sixth order zero predictor coefficient 2.

VOIE_LISTATE3

VOIE_LLISTATE3 is G726 encoding channel variable register 3.

Offset Address	Register Name	Total Reset Value
0x005C	VOIE_LISTATE3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	B3	B4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	B3	G726 coded channel variable, sixth order zero predictor coefficient 3.
[15:0]	RO	B4	G726 code channel variable, sixth order zero predictor coefficient 4.

VOIE_LISTATE4

VOIE_LLISTATE4 is channel variable register 4 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0060	VOIE_LISTATE4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	B5	B6
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	B5	G726 coded channel variable, sixth order zero predictor coefficient 5.
[15:0]	RO	B6	G726 coded channel variable, sixth order zero predictor coefficient 6.

VOIE_LISTATE5

VOIE_LLISTATE5 is channel variable register 5 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0064	VOIE_LISTATE5	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	DML	— DMS	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	DML	G726 Encoded channel variable, long-term average of F(I) over time.

Offset Address	Register Name	Total Reset Value
0x0064	VOIE_LISTATE5	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Name	DML	—	DMS	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[17:16]	RO	reserved	reserve.
[15:4]	RO	DMS	G726 Encoded channel variable, F(I) short-term mean of time delay.
[3:0]	RO	reserved	reserve.

VOIE_LISTATE6

VOIE_LLISTATE6 is G726 encoding channel variable register 6.

Offset Address	Register Name	Total Reset Value
0x0068	VOIE_LISTATE6	0x0400_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	DQ1	reserved	DQ2	reserved
Reset	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	DQ1	G726 Encoding channel variable, quantized difference signal with a delay of 1. Default value: 0x20.
[20:16]	RO	reserved	reserve. Default value: 0.
[15:5]	RO	DQ2	G726 encoding channel variable, quantized difference signal with a delay of 2. Default value: 0x20.
[4:0]	RO	reserved	reserve. Default value: 0.

VOIE_LISTATE7

VOIE_LLISTATE7 is G726 encoding channel variable register 7.

Offset Address	Register Name	Total Reset Value
0x006C	VOIE_LISTATE7	0x0400_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	DQ3	reserved	DQ4	reserved
Reset	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:21]	RO	DQ3	G726 encodes the channel variable, and the quantized difference signal with a delay of 3. Default value: 0x20.
[20:16]	RO	reserved	reserve. Default value: 0.
[15:5]	RO	DQ4	G726 encodes the channel variable, and the quantized difference signal with a delay of 4. Default value: 0x20.
[4:0]	RO	reserved	reserve. Default value: 0.

VOIE_LISTATE8

VOIE_LLISTATE8 is G726 encoding channel variable register 8.

Offset Address	Register Name	Total Reset Value
0x0070	VOIE_LISTATE8	0x0400_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	DQ5	reserved	DQ6	reserved
Reset	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:21]	RO	DQ5	G726 encoding channel variable, quantized difference signal with a delay of 5. Default value: 0x20.
[20:16]	RO	reserved	reserve. Default value: 0.
[15:5]	RO	DQ6	G726 encodes the channel variable, and the quantized difference signal with a delay of 6. Default value: 0x20.
[4:0]	RO	reserved	reserve. Default value: 0.

VOIE_LISTATE9

VOIE_LLISTATE9 is channel variable register 9 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0074	VOIE_LISTATE9	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SR1																reserved				SR2											reserved	
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	SR1	G726 coded channel variable, reconstructed signal with a delay of 1. Default value: 0x20.
[20:16]	RO	reserved	reserve. Default value: 0.
[15:5]	RO	SR2	G726 Coded channel variable, reconstructed signal with a delay of 2. Default value: 0x20.
[4:0]	RO	reserved	reserve. Default value: 0.

VOIE_LISTATE10

VOIE_LLISTATE10 is channel variable register 10 of G726 encoding.

Offset Address	Register Name	Total Reset Value
0x0078	VOIE_LISTATE10	0x1100_0220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YL																														YU	
Reset	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	YL	G726 Encoded channel variant, slow quantization scale factor. Default value: 0x8800.
[12:0]	RO	YU	G726 encodes channel variables, fast quantization scale factors. Default value: 0x220.

VOIE_STATE_CHK0

VOIE_STATE_CHK0 is the G726 channel variable check register.

Offset Address	Register Name	Total Reset Value
0x007C	VOIE_STATE_CHK0	0x2100_1220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	g726_check																															
Reset	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	g726_check	G726 channel variable verification result.

VOIE_LLISTATE11

VOIE_LLISTATE11 is ADPCM code channel variable register 11.

Offset Address	Register Name	Total Reset Value
0x0080	VOIE_LLISTATE11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	valprev																reserved								index							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	valprev	ADPCM encoding channel variable, reconstructed value of the last audio point.
[15:8]	RO	reserved	reserve.
[7:0]	RO	index	ADPCM encoding channel variable, index value of quantization table.

VOIE_STATE_CHK1

VOIE_STATE_CHK1 is the ADPCM channel variable check register.

Offset Address	Register Name	Total Reset Value
0x0084	VOIE_STATE_CHK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adpcm_check																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	adpcm_check ADPCM channel variable check result.

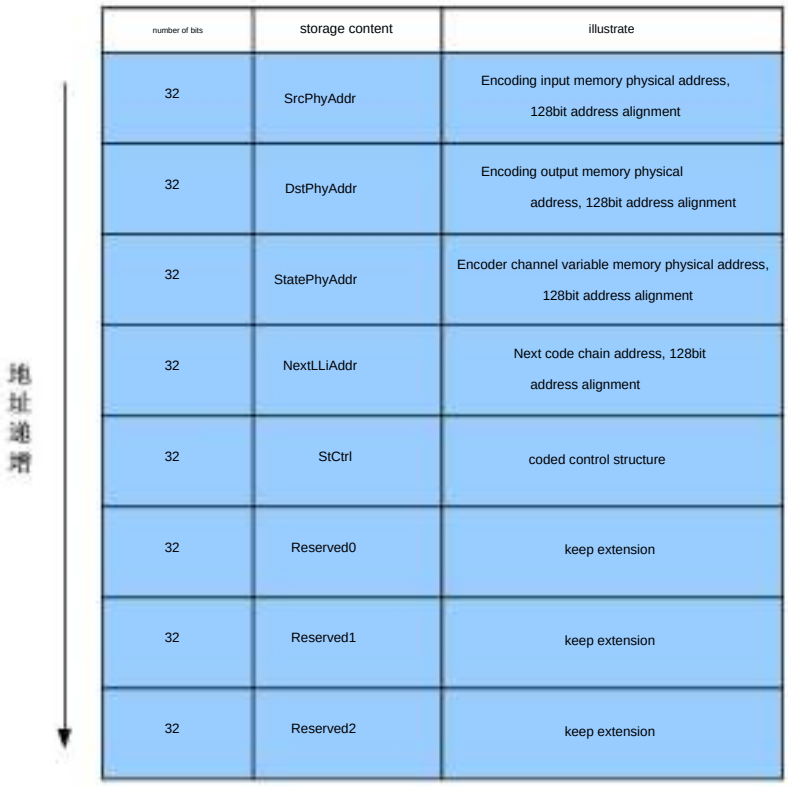
12.7 Description of linked list structure (attached)

Figure 12-2 shows the linked list structure and its arrangement in DDR. It is necessary to write the linked list into DDR, and configure the address of the first linked list to the VOIE_CFG register (address: 0x2064_0028) through the register.

Linked list structure:

```
typedef struct hiVOICE_ENGINE_LLI_STATE
{
    HI_U32              u32SrcPhyAddr;
    HI_U32              u32DstPhyAddr;
    HI_U32              u32StatePhyAddr;
    HI_U32              u32NextLLiAddr;
    VOICE_ENGINE_Ctrl stCtrl;
    HI_U32              u32Reserved0;
    HI_U32              u32Reserved1;
    HI_U32              u32Reserved2;
} VOICE_ENGINE_LLI_STATE;
```

Figure 12-2 Corresponding linked list structure



number of bits	storage content	illustrate
32	SrcPhyAddr	Encoding input memory physical address, 128bit address alignment
32	DstPhyAddr	Encoding output memory physical address, 128bit address alignment
32	StatePhyAddr	Encoder channel variable memory physical address, 128bit address alignment
32	NextLLiAddr	Next code chain address, 128bit address alignment
32	StCtrl	coded control structure
32	Reserved0	keep extension
32	Reserved1	keep extension
32	Reserved2	keep extension

Figure 12-3 Storage structure of StCrtl

内容	Reserved	hisi_head	Codec	SamplesPerFrame
Bit分配	6:0	7	15:8	31:16

Figure 12-4 G726 channel variable structure

Reserved as 0

number of bits	storage content	illustrate
32	A1[15:0] A2[15:0]	[31:16] [15:0]
32	AP[9:0] PK1 PK2 TD	[31:22] [15] [14] [0]
32	B1[15:0] B2[15:0]	[31:16] [15:0]
32	B3[15:0] B4[15:0]	[31:16] [15:0]
32	B5[15:0] B6[15:0]	[31:16] [15:0]
32	DML[13:0] DMS[11:0]	[31:18] [15:4]
32	DQ1[10:0] DQ2[10:0]	[31:21] [15:5]
32	DQ3[10:0] DQ4[10:0]	[31:21] [15:5]
32	DQ5[10:0] DQ6[10:0]	[31:21] [15:5]
32	SR1[10:0] SR2[10:0]	[31:21] [15:5]
32	YL[18:0] YU[12:0]	[31:13] [12:0]
32	G726_check	[31:0]

地址递增

Figure 12-5 ADPCM channel variable structure

保留位均为0

Bit数	存储内容	说明
32	valprev[15:0] index[7:0]	[31:16] [7:0]
32	adpcm_check	[31:0]

地址递增

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13 audio port

13.1 Overview

The audio input and output interface AIO (Audio Input/Output) is used to connect with the off-chip Audio CODEC chip to complete the input and output of audio data to realize functions such as recording, intercom, and playback. Hi3520D integrates 1 AIO, including 1 AIP (Audio Input Port) and 2 AOPs (Audio Output Port), of which AIP supports 2/4/8/16 audio inputs, and AOP0 supports 2/4/8/16 channels Audio output, AOP1 connects with HDMI inside the chip through I. ^{2}S interface implementation

13.2 Features

The AIO interface supports ^{2} S and PCM (Pulse Code Modulation) and two modes, using DMA access I data.

PCM interface

The PCM interface has the following characteristics:

- Support master mode and slave mode.
- Support mono 8bit or 16bit linear PCM coded transmission and reception.
- Support multiple reception of 2/4/8/16 channels of 8/16 bit data.
- Support bit clock and frame synchronization signal generated inside the chip, also support external bit clock and frame synchronization signal.
- PCM interface frame synchronization signal only supports short pulse synchronization signal (the duration of the synchronization signal is 1 clock cycle), and supports standard and custom modes. Receive
- (AIP) and transmit (AOP0/AOP1) are independent of each other and can be enabled or disabled individually. Both receiving
- (AIP) and sending (AOP0/AOP1) adopt DMA operation, access data through the circular buffer opened by software, and the size and waterline of the circular buffer are adjustable.

I2S interface

I ^{2} The S interface has the following characteristics:

- Support master mode and slave mode.

Support left and right channel 8/16/24/32bit data sending and receiving. Support

multiple reception of 2/4/8/16 channels of 8/16bit data.

Support 8kHzÿ192kHz sampling rate.

Receive (AIP) and transmit (AOP0/AOP1) are independent of each other and can be enabled or disabled individually. Both

receiving (AIP) and sending (AOP0/AOP1) adopt DMA operation, access data through the circular buffer opened by software, and the size and waterline of the circular buffer are adjustable.

13.3 Functional description

typical application

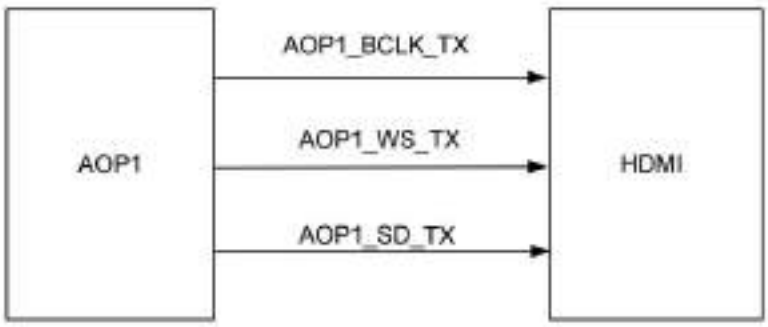
Hi3520D integrates 1 AIP and 2 AOPs, among which:

AIP supports multi-channel receiving function, that is, it supports receiving input 2/4/8/16 channels, and the data bit width is 8/16bit.

AOP0 is used for playback of typical 2-channel 16bits audio data.

AOP1 realizes docking with HDMI inside the chip, and the docking mode only supports I HDMI docking ^{2} S Master mode. AOP1 and diagram as shown in Figure 13-1 .

Figure 13-1 Connection diagram of AOP1 and HDMI



Both AIP and AOP0 support the master-slave mode, and the master-slave mode will be explained ^{2} Typical connection of S/PCM interface below.

In master mode, I ^{2} Typical connections of the S/PCM interface are shown in Figure 13-2 and Figure 13-3 .

说明

In Figure 13-2 , the I2S interface of the AudioCodec chip connected to AIP and AOP0 is 6-wire mode (TX and RX have their own BCLK and WS)

In Figure 13-3 , the I2S interface of the AudioCodec chip connected by AIP and AOP0 is 4-wire mode (TX and RX share BCLK and WS)

In the main mode, the bit stream clock and left and right channel selection signals (synchronous signals in PCM mode) are sent from AIO to AUDIO CODECÿ

Figure 13-2 I 2 S/PCM interface master mode connection diagram 1

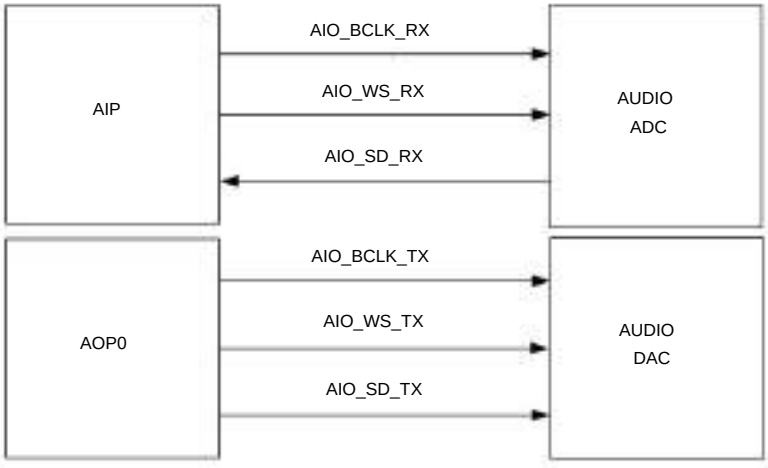
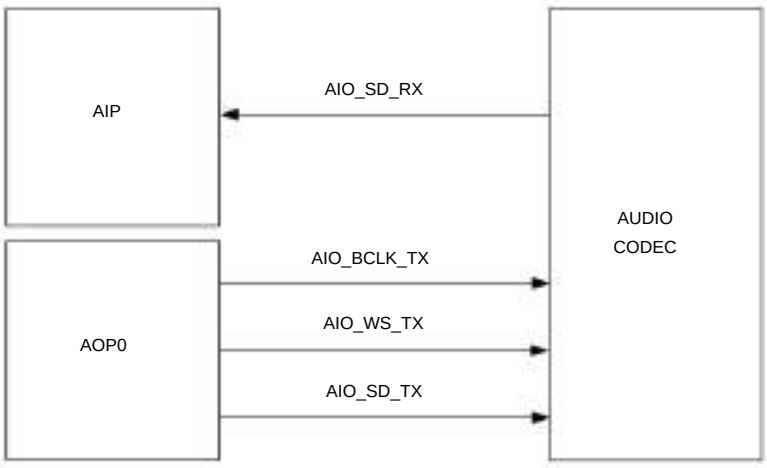


Figure 13-3 I 2 S/PCM interface main mode connection schematic diagram 2



In slave mode, I 2 Typical connections of the S/PCM interface are shown in Figure 13-4 and Figure 13-5 .

说明

In Figure 13-4 , the I2S interface of the AudioCodec chip connected to AIP and AOP0 is in 6-wire mode (TX and RX have their own BCLK and WS)

In Figure 13-5 , the I2S interface of the AudioCodec chip connected by AIP and AOP0 is 4-wire mode (TX and RX share BCLK and WS)

In the slave mode, the bit stream clock and left and right channel selection signals (synchronous signals in PCM mode) are sent to AIO by AUDIO CODEC; the main working clock of AUDIO CODEC is provided by the clock AIO_MCLK output by Hi3520D or an external crystal oscillator.

Figure 13-4 I^{2}S/PCM interface slave mode connection diagram 1

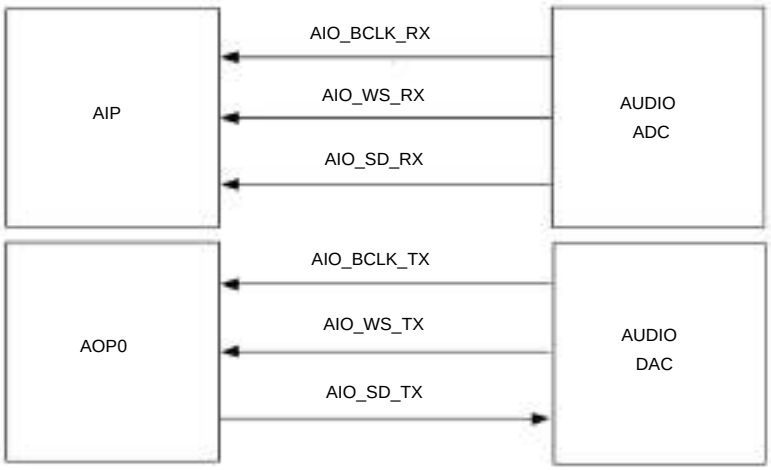
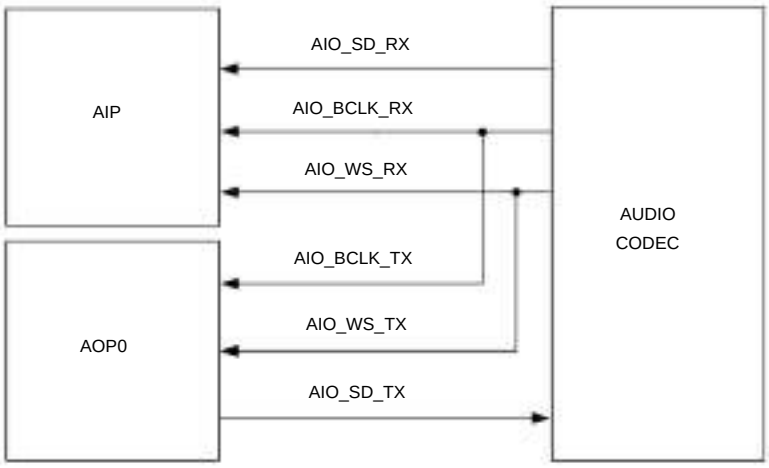


Figure 13-5 I^{2}S/PCM interface slave mode connection diagram 2



Functional principle

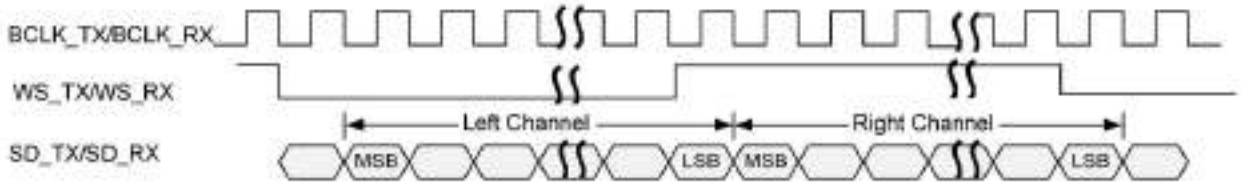
AIP through I^2 The S or PCM interface receives the audio data converted by AD (Analog-to-Digital) from the AUDIO CODEC, stores them in the circular buffer created for the AIP, and then takes them away and stores them by the CPU to complete the recording function.

AOP0 reads the audio data from the circular buffer, and then transmits the audio data to the docked AUDIO CODEC through the IPCM interface I^2S or according to the set sampling rate, and the AUDIO CODEC performs DA (Digital-to-Analog) conversion for sound playback.

I^2S The data transmitted by the S interface is divided into left and right channels, which are distinguished according to the high and low levels of the WS_TX (WS_RX) signal. As shown in Figure 13-6 . According to the protocol, the data is sampled with the rising edge of the BCLK_TX/BCLK_RX clock, and the MSB is valid in the next clock cycle after the change of WS_TX/WS_RX. Always transmit MSB first, then LSBÿ

I^2S The timing sequence of the S interface is shown in Figure 13-6 .

Figure 13-6 I^2S interface timing



The data transmitted by the PCM interface is mono data, WS_TX/WS_RX identifies the starting position of the data, the most significant bit MSB is sent (received) first, and the data is sampled using the falling edge of the clock. In the standard mode timing, the MSB data is valid one cycle after the WS_TX/WS_RX high-level pulse; in the custom mode timing, the position of the MSB is aligned with the high-level pulse of WS_TX/WS_RX.

The timing sequence in PCM interface standard mode is shown in Figure 13-7 .

Figure 13-7 Timing sequence of PCM interface standard mode

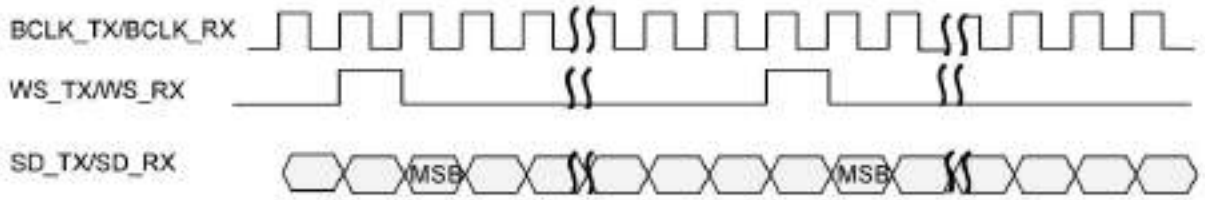
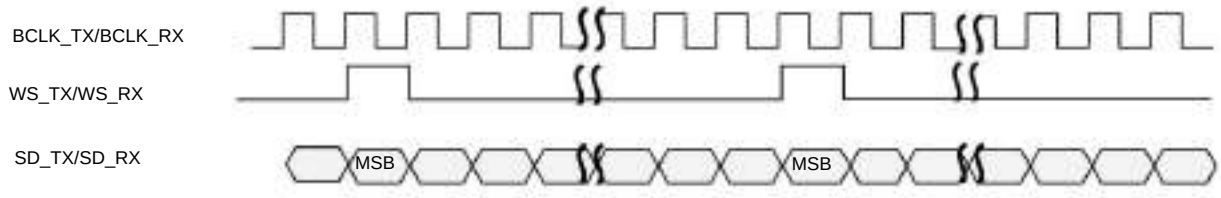


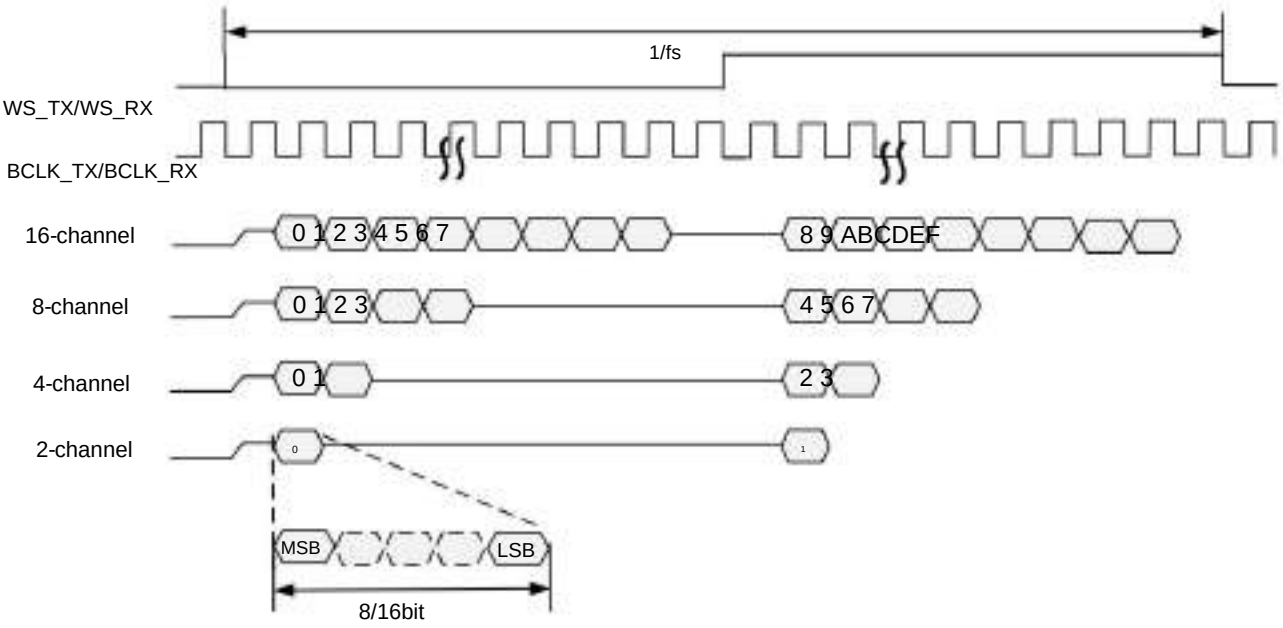
Figure 13-8 shows the timing sequence in PCM interface custom mode .

Figure 13-8 Timing sequence of PCM interface custom mode



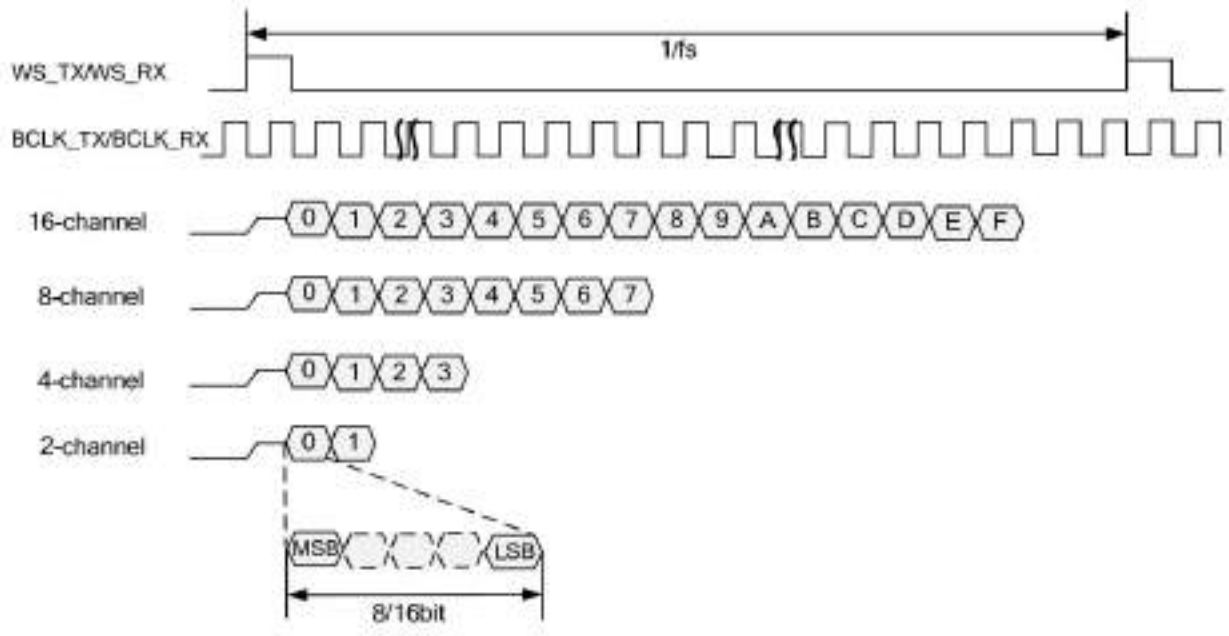
I^2S When performing multi-channel (2/4/8/16-channel 8/16bit) reception, the data are placed in the I^2S The left and right channels of S timing, as shown in the figure 13-9 .

picture 13-9 I ^{2} S 2/4/8/16 channels receiving



Multi-channel reception in PCM mode, as shown in Figure 13-10 . Support PCM standard and custom two modes, AIO can choose data sampling time (rising edge or falling edge) to receive. Figure 13-10 takes the rising edge as an example.

Figure 13-10 PCM 2/4/8/16 channels receiving



13.4 Working method

Clock gating and clock configuration

When enabling AIO for recording or playback, the clock gate of the corresponding channel (AIP/AOP0/AOP1) in AIO must be turned on first. Specific steps are as follows:

说明

AOP1 is connected with HDMI audio, which requires AOP1 to work in master mode, that is, PERI_CRG34 and PERI_CRG38 must be configured, regardless of the use of Audio Codec.

1. Confirm whether the AIO is connected to an independent Audio Codec or an Audio Codec integrated with the video AD chip.

   If the video AD chip integrates Audio Codec, and the required working clock needs to be provided by the Hi3520D main chip (via the pin VI_ADC_CLK), you need to configure CRG to generate the working clock required by the video AD chip. That is to configure the register PERI_CRG11[vi_adc_cksel] to ensure that the main chip outputs the correct video AD working clock.

   If a separate Audio Codec is connected, and the working clock needs to be provided by the Hi3520D main chip (through the pin AIO_MCLK), it is necessary to configure the CRG to generate the working clock required by the Audio Codec. That is to configure the registers PERI_CRG32/PERI_CRG33/PERI_CRG34 to generate the frequency division source clock MCLK of AIP/AOP0/AOP1.

2. Configuration registers PERI_CRG36/PERI_CRG37/ PERI_CRG38 aip_bclk_sel/aop0_bclk_sel/aop1_bclk_sel, select the master-slave mode of the AIO interface. If the AIO works in master mode, go to step 3; if the AIO works in slave mode, go to step 4.

3. If the I of the AudioCodec chip connected to AIP and AOP0 ^{2}S interface is 4-wire mode (TX and RX share BCLK and WS), configure PERI_CRG32[aip_clk_sel] as 0x0, otherwise configure as 0x1.

4. Configure the register PERI_CRG35[aio_hcken] as 0x1 to enable the main switch of the AIO clock.

5. Configure registers PERI_CRG36/PERI_CRG37/PERI_CRG38 to generate bit stream clock (BCLK) and left and right channel selection signal (WS) required by AIP/AOP0/AOP1. Configure the registers PERI_CRG36[aip_cken], PERI_CRG37[aop0_cken] and PERI_CRG38[aop1_cken] separately to enable the clock of the specified channel (AIP/AOP0/AOP1), and aip_cken is also used to enable the working clock of the external Audio Codec (AIO_MCLK).

----Finish

soft reset

The three channels (AIP, AOP0 and AOP1) inside the AIO have independent soft resets, which can be soft reset separately by configuring the corresponding registers.

Take AIP as an example, through the configuration register PERI_CRG36, the individual soft reset of AIP can be realized. After reset, the values of each configuration register of AIP are reset to the default value, so these registers need to be initialized and configured again after reset.

注意

Before performing a soft reset on the AIP, it must be ensured that the AIP is in the stop state, that is, AIP_STOP [aip_enable] is 0x0 and AIP_STOP [aip_stop_done] is 0x1; the same requirements apply to AOP0 and AOP1. It is not necessary to perform a separate soft reset on the AIO after the normal system reset is complete.

recording workflow

The initialization steps are as follows:

1. Configure AIP-related clocks;
2. Set AIP_INF_ATTRI [aip_mode], select I ^{2} S or PCM mode;
3. Set AIP_INF_ATTRI [aip_samp_precision] to select the sampling precision;
4. Set AIP_INF_ATTRI [aip_clk_edge_sel] to set the clock sampling time;
5. Set AIP_INF_ATTRI [aip_timedivision_sel], choose whether to use multi-channel reception;
6. If multi-path reception is used, set AIP_INF_ATTRI[aip_routes_sel];
7. If the sampling precision is 8bit, set AIP_CTRL [aip_shift8_en];
8. ÿÿ AIP_BUF_SADDR [aip_buf_saddr]ÿAIP_BUF_SIZE [aip_buf_size]ÿ AIP_TRANS_SIZE [aip_trans_size]ÿ
9. Write 0 to AIP_BUF_WPTR [aip_buf_wptr] and AIP_BUF_RPTR [aip_buf_rptr];
10. Set AIO_INT_ENA and AIP_INT_ENA according to the need of interrupt masking.

----Finish

The recording steps are as follows:

1. Set AIP_STOP [aip_enable] to 1 to start AIP;
2. By reading the values of AIP_BUF_WPTR [aip_buf_wptr] and AIP_BUF_RPTR [aip_buf_rptr], judge the empty/full status of the circular buffer and the amount of valid data; ensure that the data is taken away before the circular buffer is full, and the updated circular buffer Write the area read address into AIP_BUF_RPTR [aip_buf_rptr], otherwise the circular buffer may overflow and the sound will be discontinuous.
3. After the recording is completed, write 0 to AIP_STOP [aip_enable] to stop AIP;
4. Poll AIP_STOP until AIP_STOP [aip_stop_done] becomes 1.

----Finish

注意

Before starting AIP, the configuration of AIP clock must be completed to ensure that AIO_BCLK_RX and AIO_WS_RX are normal.

playback workflow

The workflow of AOP0 and AOP1 is the same, and the following uses AOP0 as an example to illustrate.

The initialization steps are as follows:

1. Configure AOP0-related clocks;
2. Set AOP0_INF_ATTRI [aop0_mode], select I ^{2} S or PCM mode;
3. Set AOP0_INF_ATTRI [aop0_samp_precision] to select the precision of sending data;
4. Set AOP0_INF_ATTRI [aop0_clk_edge_sel] to select the clock polarity of sending data;
5. Set AOP0_INF_ATTRI [aop0_timedivision_sel], choose whether to use multiplex transmission;
6. If multiplex is used, set AOP0_INF_ATTRI [aop0_routes_sel];
7. Set AOP0_BUF_SADDR [aop0_buf_saddr], AOP0_BUF_SIZE [aop0_buf_size] and AOP0_TRANS_SIZE [aop0_trans_size];
8. Write at least 128bytes of data to the circular buffer of AOP0;
9. Write 0 to AOP0_BUF_RPTR [aop0_buf_rptr], and update AOP0_BUF_WPTR [aop0_buf_wptr] according to the amount of valid data in the circular buffer ;
10. Set AIO_INT_ENA and AOP0_INT_ENA according to the need of interrupt masking.

----Finish

The playback steps are as follows:

1. Set AOP0_STOP[aop0_enable] to 1 to start AOP0;
2. By reading the values of AOP0_BUF_WPTR [aop0_buf_wptr] and AOP0_BUF_RPTR [aop0_buf_rptr], judge the empty/full status of the circular buffer and the amount of available data; ensure that new data is added before the circular buffer is empty, and the updated circular buffer Write the area write address into AOP0_BUF_WPTR [aop0_buf_wptr], otherwise the sound may be discontinuous.
3. After the playback is completed, write 0 to AOP0_STOP [aop0_enable] to stop AOP0;
4. Poll AOP0_STOP until AOP0_STOP [aop0_stop_done] becomes 1.

----Finish

注意

Before starting AOP0, the clock configuration of AOP0 must be completed to ensure that AIO_BCLK_TX and AIO_WS_TX are normal, and AOP1 has the same requirements.

When writing data to the circular buffer of AOP0 and updating AOP0_BUF_WPTR [aop0_buf_wptr], it must be ensured that the free space of the circular buffer of AOP0 is not less than 32 bytes, and there is the same requirement for AOP1.

13.5 Register overview

An overview of the AIO registers is shown in Table 13-1 .

Table 13-1 AIO register overview (base address is 0x2065_0000)

offset address name		describe	page number
0x0000	AIO_INT_ENA	AIO Global Interrupt Enable Register	13-12
0x0004	AIO_INT_STATUS AIO global interrupt status register		13-13
0x0008	AIO_INT_RAW	AIO Global Raw Interrupt Register	13-14
0x1000	AIP_INF_ATTRI	AIP interface attribute setting register	13-15
0x1004	AIP_CTRL	AIP Control Register	13-17
0x1008	AIP_BUF_SADDR AIP circular buffer start address register 13-17		
0x100C	AIP_BUF_SIZE	AIP circular buffer size register	13-18
0x1010	AIP_BUF_WPTR	AIP circular buffer write address register	13-18
0x1014	AIP_BUF_RPTR	AIP circular buffer read address register	13-19
0x1018	AIP_BUF_AFULL_TH	AIP's Circular Buffer Almost Full Threshold Register 13-19	
0x101C AIP_TRANS_SIZE AIP data transfer length register			13-20
0x1020	AIP_INT_ENA	AIP Interrupt Enable Register	13-20
0x1024	AIP_INT_RAW	AIP Raw Interrupt Register	13-21
0x1028	AIP_INT_STATUS AIP interrupt status register		13-22
0x102C	AIP_INT_CLR	AIP Interrupt Clear Register	13-23
0x1030	AIP_BUF_WPTR_TMP	AIP circular buffer write address latch register 13-24	
0x1034	AIP_BUF_RPTR_TMP	AIP Circular Buffer Read Address Latch Register 13-25	
0x1038	AIP_STOP	AIP start/stop register	13-25

offset address	name	describe	page number
0x2000	AOP0_INF_ATTRI	AOP0 interface attribute setting register	13-26
0x2004	AOP0_CTRL	AOP0 Control Register	13-27
0x2008	AOP0_BUF_SADDR	AOP0 circular buffer start address register 13-28	
0x200C	AOP0_BUF_SIZE	Circular Buffer Size Register for AOP0	13-28
0x2010	AOP0_BUF_WPTR	AOP0 circular buffer write address register	13-29
0x2014	AOP0_BUF_RPTR	AOP0 circular buffer read address register	13-29
0x2018	AOP0_BUF_AEMPTY_TH	Circular Buffer Almost Empty Threshold Register 13-30 for AOP0	
0x201C	AOP0_TRANS_SIZE	AOP0 data transfer length register	13-30
0x2020	AOP0_INT_ENA	AOP0 Interrupt Enable Register	13-31
0x2024	AOP0_INT_RAW	AOP0 Raw Interrupt Register	13-32
0x2028	AOP0_INT_STATUS	AOP0 interrupt status register	13-33
0x202C	AOP0_INT_CLR	AOP0 Interrupt Clear Register	13-34
0x2030	AOP0_BUF_WPTR_TMP	AOP0 Circular Buffer Write Address Latch Register 13-35	
0x2034	AOP0_BUF_RPTR_TMP	AOP0 Circular Buffer Read Address Latch Register 13-35	
0x2038	AOP0_STOP	AOP0 Start/Stop Register	13-36
0x2100	AOP1_INF_ATTRI	AOP1 interface attribute setting register	13-37
0x2104	AOP1_CTRL	AOP1 Control Register	13-38
0x2108	AOP1_BUF_SADDR	AOP1 circular buffer start address register 13-38	
0x210C	AOP1_BUF_SIZE	Circular buffer size register for AOP1	13-39
0x2110	AOP1_BUF_WPTR	AOP1 circular buffer write address register	13-39
0x2114	AOP1_BUF_RPTR	AOP1 circular buffer read address register	13-40
0x2118	AOP1_BUF_AEMPTY_TH	AOP1's Circular Buffer Almost Empty Threshold Register 13-40	
0x211C	AOP1_TRANS_SIZE	AOP1 data transfer length register	13-41
0x2120	AOP1_INT_ENA	AOP1 Interrupt Enable Register	13-41
0x2124	AOP1_INT_RAW	AOP1 Raw Interrupt Register	13-42
0x2128	AOP1_INT_STATUS	AOP1 interrupt status register	13-43
0x212C	AOP1_INT_CLR	AOP1 Interrupt Clear Register	13-44

offset address	name	describe	page number
0x2130	AOP1_BUF_WPTR_TMP	AOP1 Circular Buffer Write Address Latch Register	13-45
0x2134	AOP1_BUF_RPTR_TMP	AOP1 Circular Buffer Read Address Latch Register	13-46
0x2138	AOP1_STOP	AOP1 Start/Stop Register	13-46

13.6 Register Description

AIO_INT_ENA

AIO_INT_ENA is AIO global interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0000	AIO_INT_ENA	0x0000_0000

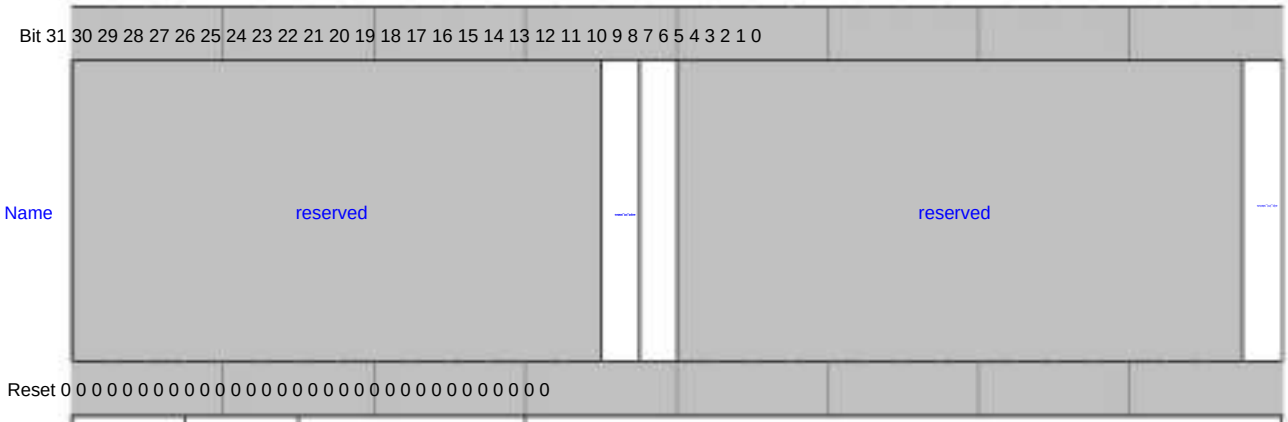
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RW	aop1_int_ena	AOP1 interrupt enable. 0: disable; 1: enable.
[16]	RW	aop0_int_ena	AOP0 interrupt enable. 0: disable; 1: enable.
[15:1]	RO	reserved	reserve.
[0]	RW	aip_int_ena	AIP interrupt enable. 0: disable; 1: enable.

AIO_INT_STATUS

AIO_INT_STATUS is AIO global interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	AIO_INT_STATUS	0x0000_0000

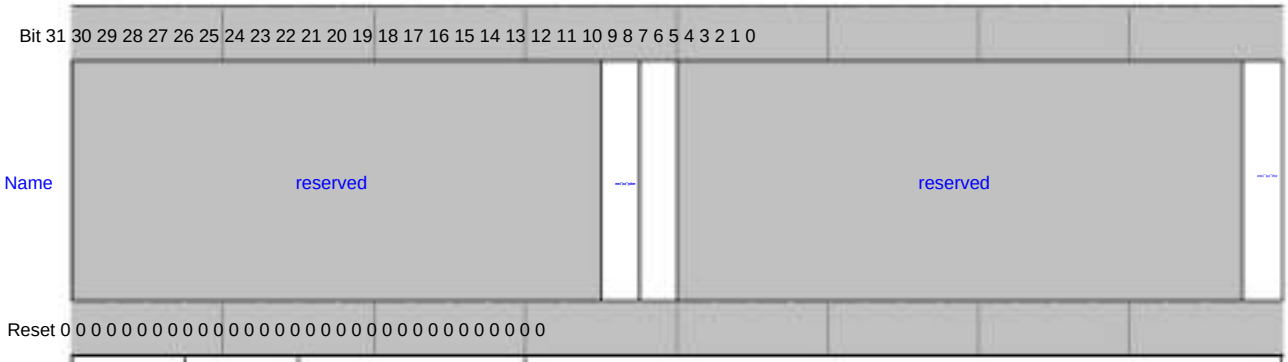


Bits	Access Name		Description
[31:18] RO		reserved	reserve.
[17] RO		aop1_int_status	AOP1 interrupt status. 0: no interrupt status; 1: There is an interrupt status.
[16] RO		aop0_int_status	AOP0 interrupt status. 0: no interrupt status; 1: interrupt status.
[15:1] RO		reserved	reserve.
[0]	RO	aip_int_status	AIP outage status. 0: no interrupt status; 1: There is an interrupt status.

AIO_INT_RAW

AIO_INT_RAW is AIO global raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	AIO_INT_RAW	0x0000_0000

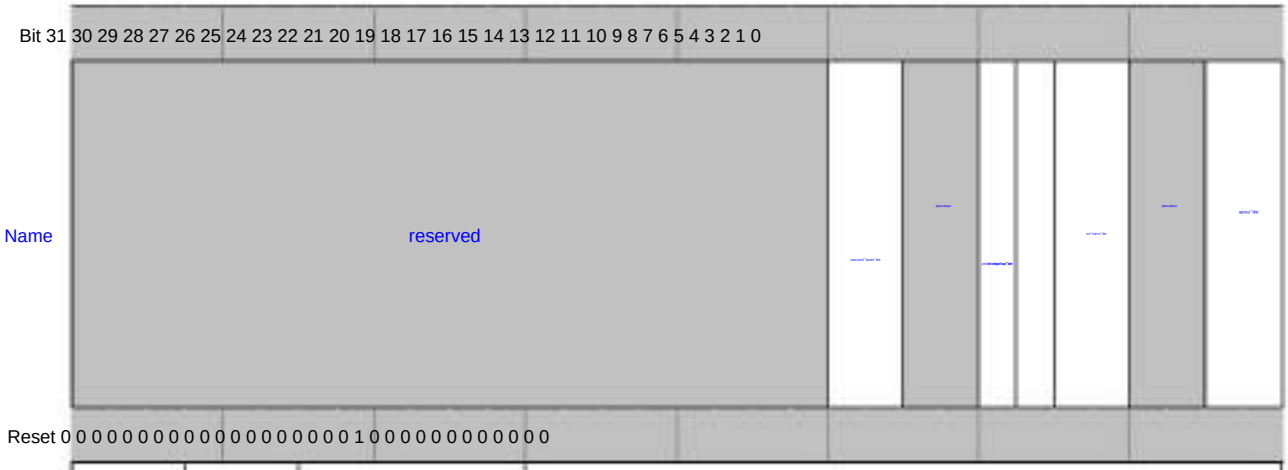


Bits	Access Name		Description
[31:18]	RO	reserved	reserve.
[17]	RO	aop1_int_raw	AOP1 interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[16]	RO	aop0_int_raw	AOP0 interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[15:1]	RO	reserved	reserve.
[0]	RO	aip_int_raw	AIP outage status. 0: no original interrupt; 1: There is a raw interrupt.

AIP_INF_ATTRI

AIP_INF_ATTRI Sets register for AIP interface attributes.

Offset Address	Register Name	Total Reset Value
0x1000	AIP_INF_ATTRI	0x0000_1000



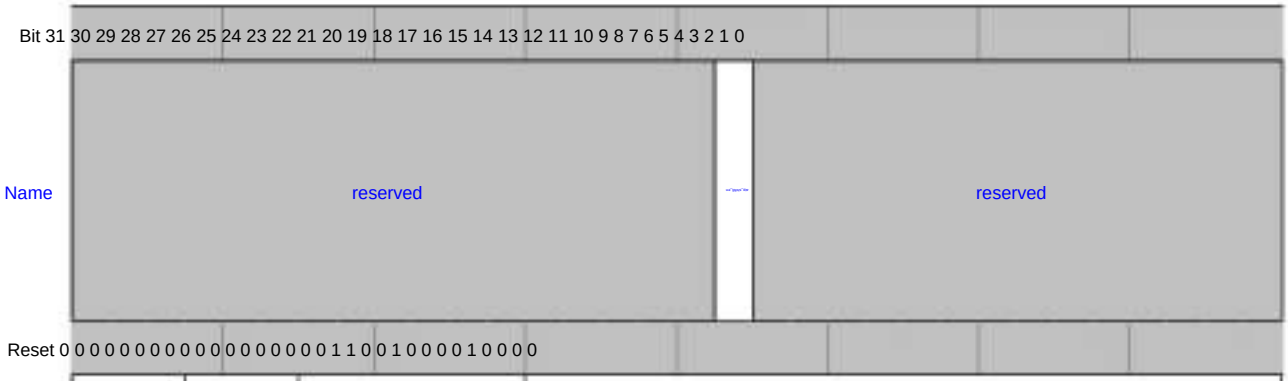
Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved, must be configured as 0x1.
[11:10]	RW	aip_samp_precision	Sampling accuracy configuration of AIP received data. 00ÿ8bitÿ 01ÿ16bitÿ 10ÿ24bitÿ 11ÿ32bitÿ If multi-channel reception is enabled, only 8/16bit is supported; If multi-channel reception is not enabled, 8/16/24/32bit is supported in I2S mode, and 8/16bit is supported in PCM standard mode and PCM custom mode.
[9:8]	RO	reserved	reserve.
[7]	RW	aip_clk_edge_sel	AIP data sampling time selection. 0: Data is sampled on the rising edge of the clock; 1: Data is sampled on the falling edge of the clock.
[6]	RW	enable. aip_timedivision_s reception; el	AIP multiplex receive 0: Disable multi-channel 1: Enable multi-channel reception.
[5:4]	RW	aip_routes_sel	Channel number selection in AIP multi-channel receiving mode. 00: 2 channels; 01: 4 channels; 10:8 way; 11:16 Road.
[3:2]	RO	reserved	reserve.

[1:0] RW	aip_mode		AIP mode selection. 00: I2S mode; 01: PCM standard mode; 10: PCM custom mode; 11: reserved.

AIP_CTRL

AIP_CTRL is the AIP control register.

Offset Address	Register Name	Total Reset Value
0x1004	AIP_CTRL	0x0000_3210



Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved, must be configured as 0x0.
[14]	RW	aip_shift8_en	AIP data shift storage enable (only valid when the sampling precision of received data is 8bit). 0: Do not shift, directly store according to 8bit; 1: shift, shift each received sampling data to the left by 8 bits, add 0 to the lower 8 bits, and store in 16 bits.
[13:0]	RW	reserved	Reserved, must be configured as 0x3210.

AIP_BUF_SADDR

AIP_BUF_SADDR is the start address register of AIP circular buffer.

Offset Address	Register Name	Total Reset Value
0x1008	AIP_BUF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aip_buf_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW aip_buf_saddr	AIP's circular buffer start address. Note: It must be configured as an integer multiple of **128 .**

AIP_BUF_SIZE

AIP_BUF_SIZE is the circular buffer size register of AIP.

Offset Address	Register Name	Total Reset Value
0x100C	AIP_BUF_SIZE	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aip_buf_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:0]	RW aip_buf_size	AIP's circular buffer size in bytes. Note: It must be configured as an integer multiple of **128 .**

AIP_BUF_WPTR

AIP_BUF_WPTR is the write address register for AIP circular buffer.

Offset Address	Register Name	Total Reset Value
0x1010	AIP_BUF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aip_buf_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.

[23:0]	RW	aip_buf_wptr	AIP's circular buffer write address, in bytes. Note 1: The write address is the offset address relative to the start address of the circular buffer of **AIP .** Note 2: It must be configured as an integer multiple of **128 .**

AIP_BUF_RPTR

AIP_BUF_RPTR is the AIP circular buffer read address register.

Offset Address	Register Name	Total Reset Value
0x1014	AIP_BUF_RPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aip_buf_rptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aip_buf_rptr	AIP's circular buffer read address, in bytes. Note 1: The read address is the offset address relative to the start address of the circular buffer of **AIP .** Note 2: It must be configured as an integer multiple of **16 .**

AIP_BUF_AFULL_TH

AIP_BUF_AFULL_TH is the circular buffer almost full threshold register for the AIP.

Offset Address	Register Name	Total Reset Value
0x1018	AIP_BUF_AFULL_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aip_buf_afull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:0]	RW	aip_buf_afull_th	AIP's circular buffer almost full threshold, in bytes. When the free space of the AIP circular buffer is less than the threshold, an AIP circular buffer is almost full interrupt is generated. Note: If **aip_buf_afull_int** interrupt is used, the threshold must be configured as an integer multiple of **16** and greater than or equal to **0xA0.**

AIP_TRANS_SIZE

AIP_TRANS_SIZE is the AIP data transfer length register.

Offset Address	Register Name	Total Reset Value
0x101C	AIP_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aip_trans_size
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aip_trans_size	AIP data transfer length. When AIP finishes receiving audio data of aip_trans_size length (in bytes), an aip_trans_int interrupt is generated. Note: If **aip_trans_int is used, it must be configured to a value greater than or equal to 128 .**

AIP_INT_ENA

AIP_INT_ENA is the AIP interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1020	AIP_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	aip_stop_int_en	AIP stop complete interrupt enable. 0: disable; 1: enable.
[3]	RW	aip_fifo_full_int_en	AIP's FIFO full interrupt enable. 0: disable; 1: enable.
[2]	RW	aip_buf_afull_int_en	The AIP's circular buffer almost full interrupt is enabled. 0: disable; 1: enable.
[1]	RW	aip_buf_full_int_en	AIP circular buffer full interrupt enable. 0: disable; 1: enable.
[0]	RW	aip_trans_int_en	AIP transfer complete interrupt enable. 0: disable; 1: enable.

AIP_INT_RAW

AIP_INT_RAW is the AIP raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x1024	AIP_INT_RAW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	aip_stop_int_raw	The stop of the AIP completes the original interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[3]	RO	aip_fifo_full_int_ra 0: no raw In	AIP's FIFO full raw interrupt. interrupt; 1: There is a raw interrupt.
[2]	RO	aip_buf_afull_int_r 0: no raw well	AIP's circular buffer is almost full of raw interrupts. interrupt; 1: There is a raw interrupt.
[1]	RO	aip_buf_full_int_ra 0: no raw In	The AIP's circular buffer is full of raw interrupts. interrupt; 1: There is a raw interrupt.
[0]	RO	aip_trans_int_raw	The AIP's transfer completes the original interrupt. 0: no original interrupt; 1: There is a raw interrupt.

AIP_INT_STATUS

AIP_INT_STATUS is the AIP interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1028	AIP_INT_STATUS	0x0000_0000

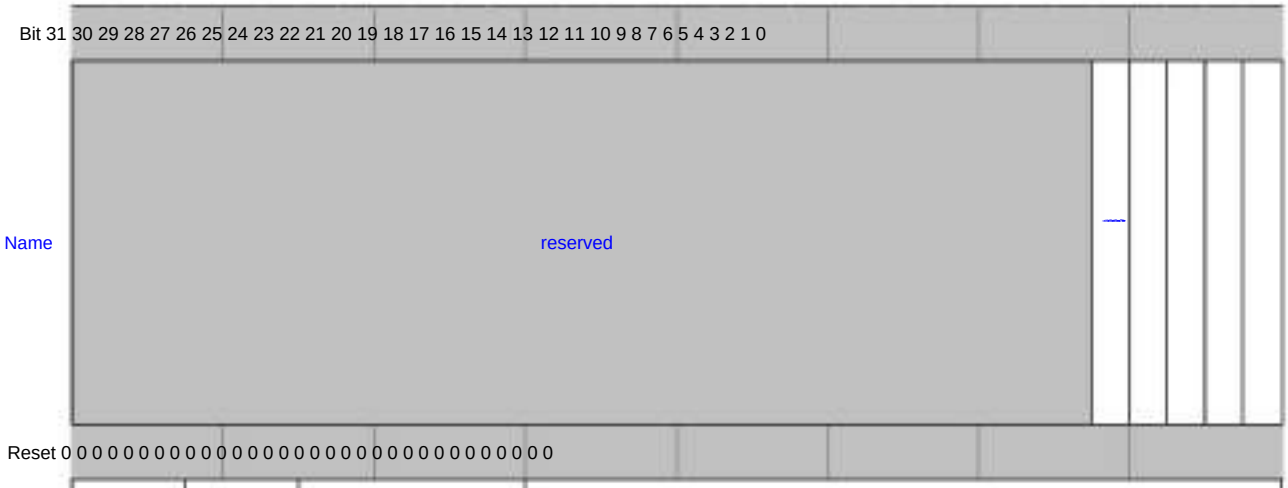
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	aip_stop_int_status	Stop complete interrupt status for AIP. 0: no interrupt status; 1: There is an interrupt status.
[3]	RO	aip_fifo_full_int_st 0: no interrupt status; atus	FIFO full interrupt status of AIP. 1: There is an interrupt status.
[2]	RO	aip_buf_afull_int_s 0: no interrupt status.	AIP's circular buffer is almost full interrupt status. tatus 1:
[1]	RO	aip_buf_full_int_st 0: no hundred interrupt status;	AIP's circular buffer full interrupt status. 1: There is an interrupt status.
[0]	RO	aip_trans_int_status	AIP's transfer complete interrupt status. 0: no interrupt status; 1: There is an interrupt status.

AIP_INT_CLR

AIP_INT_CLR is the AIP interrupt clear register. Reading this register is always 0, meaningless.

Offset Address	Register Name	Total Reset Value
0x102C	AIP_INT_CLR	0x0000_0000



Bits	Access Name	Description
[31:5] RO	reserved	reserve.
[4] RW	aip_stop_int_clr	A stop of the AIP completes the interrupt clear. Write 0: do not clear; Write 1: Clear.
[3] RW	aip_fifo_full_int_clr write r	AIP's FIFO full interrupt is cleared. 0: not clear; Write 1: Clear.
[2] RW	aip_buf_afull_int_c write 0: not clearing.	The AIP's circular buffer is almost full interrupt clear; lr write 1: clear.
[1] RW	aip_buf_full_int_cl write r	AIP circular buffer full interrupt clear. 0: not clear; Write 1: Clear.
[0] RW	aip_trans_int_clr	The AIP's transfer complete interrupt is cleared. Write 0: do not clear; Write 1: Clear.

AIP_BUF_WPTR_TMP

AIP_BUF_WPTR_TMP is the write address latch register for AIP circular buffer.

Offset Address	Register Name	Total Reset Value
0x1030	AIP_BUF_WPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aip_buf_wptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	saved to aip_buf_wptr_tmp	When AIP transfer complete interrupt occurs, the value of aip_buf_wptr is aip_buf_wptr_tmp until AIP transfer complete interrupt occurs again.

AIP_BUF_RPTR_TMP

AIP_BUF_RPTR_TMP is the read address latch register of AIP circular buffer.

Offset Address	Register Name	Total Reset Value
0x1034	AIP_BUF_RPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aip_buf_rptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	aip_buf_rptr_tmp	When an AIP transfer complete interrupt occurs, the value of aip_buf_rptr is saved to aip_buf_rptr_tmp until another AIP transfer complete interrupt occurs.

AIP_STOP

AIP_STOP is the AIP start/stop register.

Offset Address	Register Name	Total Reset Value
0x1038	AIP_STOP	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	aip_stop_done	AIP data reception stop complete status. 0: not completed; 1: Done.
[0]	RW	aip_enable	AIP data reception start/stop control. 0: stop; 1: start.

AOP0_INF_ATTRI

AOP0_INF_ATTRI Set register for AOP0 interface attributes.

Offset Address	Register Name	Total Reset Value
0x2000	AOP0_INF_ATTRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:12]	RO	reserved	reserve.

[11:10] RW		aop0_samp_precise on	The precision configuration of AOP0 sending data. 00ÿ8bitÿ 01ÿ16bitÿ 10ÿ24bitÿ 11ÿ32bitÿ If multiplexing is enabled, only 8/16bit is supported; if multiplexing is not enabled, 8/16/24/32bit is supported in I2S mode, and 8/16bit is supported in PCM standard mode and PCM custom mode.
[9:8] RW reserved			Reserved, must be configured as 0x0.
of the clock;	[7] RW	aop0_clk_edge_sel	Clock polarity selection for AOP0 transmit data. 0: The sent data is valid on the rising edge 1: Transmitted data is valid on the falling edge of the clock.
[6] RW		aop0_timedivision_ sel	0: AOP0 multiplex enable. Do not enable multicast; 1: Enable multiplexing.
[5:4] RW	aop0_routes_sel		Channel number selection in AOP0 multiplexing mode. 00: 2 way; 01: 4 roads; 10: 8 roads; 11:16 Road.
[3:2] RO		reserved	reserve.
[1:0] RW	aop0_mode		AOP0 mode selection. 00: I2S mode; 01: PCM standard mode; 10: PCM custom mode; 11: reserved.

AOP0_CTRL

AOP0_CTRL is the AOP0 control register.

Offset Address	Register Name	Total Reset Value
0x2004	AOP0_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RW	reserved	Reserved, must be configured as 0x0.
[15]	RW	aop0_mute	AOP0 transmit mute enable. 0: no mute; 1: Mute.
[14:0]	RO	reserved	reserve.

AOP0_BUF_SADDR

AOP0_BUF_SADDR is the circular buffer start address register of AOP0.

Offset Address	Register Name	Total Reset Value
0x2008	AOP0_BUF_SADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	aop0_buf_saddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	aop0_buf_saddr	The circular buffer start address of AOP0. Note: It must be configured as an integer multiple of **128 .**

AOP0_BUF_SIZE

AOP0_BUF_SIZE is the circular buffer size register of AOP0.

Offset Address	Register Name	Total Reset Value
0x200C	AOP0_BUF_SIZE	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop0_buf_size	AOP0's circular buffer size in bytes. Note: It must be configured as an integer multiple of **128 .**

AOP0_BUF_WPTR

AOP0_BUF_WPTR is the circular buffer write address register of AOP0.

Offset Address	Register Name	Total Reset Value
0x2010	AOP0_BUF_WPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_wptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop0_buf_wptr	The circular buffer write address of AOP0, in bytes. Note 1: The write address is the offset address relative to the start address of the circular buffer of **AOP0 .** Note 2: It must be configured as an integer multiple of **16 .** Note 3: The software must ensure that the free space of the circular buffer of **AOP0** is not less than **32** bytes.

AOP0_BUF_RPTR

AOP0_BUF_RPTR is the circular buffer read address register of AOP0.

Offset Address	Register Name	Total Reset Value
0x2014	AOP0_BUF_RPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_rptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop0_buf_rptr	The circular buffer read address of AOP0, in bytes. Note 1: The read address is the offset address relative to the start address of the circular buffer of **AOP0 .** Note 2: It must be configured as an integer multiple of **128 .**

AOP0_BUF_AEMPTY_TH

AOP0_BUF_AEMPTY_TH is the circular buffer almost empty threshold register for AOP0.

Offset Address	Register Name	Total Reset Value
0x2018	AOP0_BUF_AEMPTY_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_aempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	AOP0 aop0_buf_aempty_t is	AOP0's circular buffer almost empty threshold, in bytes. When the amount of valid data in the circular buffer of AOP0 is less than the threshold, an circular buffer almost empty interrupt generated. h Note: If **aop0_buf_aempty_int** interrupt is used, the threshold must be configured as an integer multiple of **16** and greater than or equal to **0x80.**

AOP0_TRANS_SIZE

AOP0_TRANS_SIZE is the AOP0 data transfer length register.

Offset Address	Register Name	Total Reset Value
0x201C	AOP0_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / aop0_trans_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop0_trans_size	AOP0 data transfer length. When AOP0 finishes sending audio data of aop0_trans_size length (in bytes), an aop0_trans_int interrupt is generated. Note: If **aop0_trans_int is used, it must be configured to a value greater than or equal to 128 .**

AOP0_INT_ENA

AOP0_INT_ENA is AOP0 interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x2020	AOP0_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	aop0_stop_int_en	Stop complete interrupt enable for AOP0. 0: disable; 1: enable.

[3] RW		AOP0. aop0_fifo_empty_int_en	FIFO empty interrupt enable for 0: disable; 1: enable.
[2] RW		aop0_buf_aempty_int_en	AOP0 circular buffer almost empty interrupt enable. 0: disable; 1: enable.
[1] RW		AOP0. aop0_buf_empty_int_en	Circular buffer empty interrupt enable for 0: disable; 1: enable.
[0] RW	aop0_trans_int_en		Transfer complete interrupt enable for AOP0. 0: disable; 1: enable.

AOP0_INT_RAW

AOP0_INT_RAW is the AOP0 raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x2024	AOP0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RO	aop0_stop_int_raw	AOP0's stop completes the raw interrupt. 0: no raw interrupt. 1: There is a raw interrupt.

[3]	RO	aop0_fifo_empty_i 0: no raw	FIFO empty raw interrupt for AOP0. interrupt; nt_raw 1: There is a raw interrupt.
[2]	RO	aop0_buf_aempty_i 0: no raw interrupt.	AOP0's circular buffer is almost empty for raw interrupts. interrupt; nt_raw 1: raw
[1]	RO	aop0_buf_empty_i 0: no raw	AOP0's circular buffer empty raw interrupt. interrupt; nt_raw 1: There is a raw interrupt.
[0]	RO	aop0_trans_int_raw	AOP0's transfer complete raw interrupt. 0: No raw interrupt; 1: There is a raw interrupt.

AOP0_INT_STATUS

AOP0_INT_STATUS is the AOP0 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x2028	AOP0_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	aop0_stop_int_stat 0: no us	Stop complete interrupt status for AOP0. interrupt status; 1: interrupt status.

[3]	RO	aop0_fifo_empty_i 0: no	FIFO empty interrupt status for AOP0. interrupt status; nt_status 1: There is an interrupt status.
[2]	RO	aop0_buf_aempty_i 0: no 1: interrupt status.	AOP0's circular buffer is almost empty interrupt status. interrupt status; nt_status
[1]	RO	aop0_buf_empty_i 0: no	Circular buffer empty interrupt status for AOP0. interrupt status; nt_status 1: There is an interrupt status.
[0]	RO	aop0_trans_int_stat 0: no us	Transfer complete interrupt status for AOP0. interrupt status; 1: There is an interrupt status.

AOP0_INT_CLR

AOP0_INT_CLR is the AOP0 interrupt clear register. Reading this register is always 0, meaningless.

Offset Address	Register Name	Total Reset Value
0x202C	AOP0_INT_CLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	aop0_stop_int_clr	Stop complete interrupt clear of AOP0. Write 0: not clear; write 1: clear.

[3] RW		aop0_fifo_empty_int_clr	AOP0 FIFO empty interrupt clear. write 0: not clear; write 1: clear.
[2] RW		aop0_buf_aempty_int_clr	AOP0 ring buffer almost empty interrupt clear. write 0: not clear; write 1: clear.
[1] RW		aop0_buf_empty_i	The circular buffer empty interrupt of AOP0 is cleared. write 0: not clear; nt_clr write 1: clear.
[0] RW	aop0_trans_int_clr		AOP0 transfer complete interrupt clear. Write 0: do not clear; Write 1: Clear.

AOP0_BUF_WPTR_TMP

AOP0_BUF_WPTR_TMP is the circular buffer write address latch register of AOP0.

Offset Address	Register Name	Total Reset Value
0x2030	AOP0_BUF_WPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_wptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	aop0_buf_wptr_tm	When the AOP0 transfer complete interrupt occurs, the value of aop0_buf_wptr is saved to aop0_buf_wptr_tmp until the AOP0 transfer complete interrupt occurs again.

AOP0_BUF_RPTR_TMP

AOP0_BUF_RPTR_TMP is the circular buffer read address latch register of AOP0.

Offset Address	Register Name	Total Reset Value
0x2034	AOP0_BUF_RPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop0_buf_rptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	is saved to aop0_buf_rptr_tmp	When AOP0 transfer complete interrupt occurs, the value of aop_buf_rptr aop0_buf_rptr_tmp until AOP0 transfer complete interrupt occurs again.

AOP0_STOP

AOP0_STOP is the AOP0 start/stop register.

Offset Address	Register Name	Total Reset Value
0x2038	AOP0_STOP	0x0000_0002

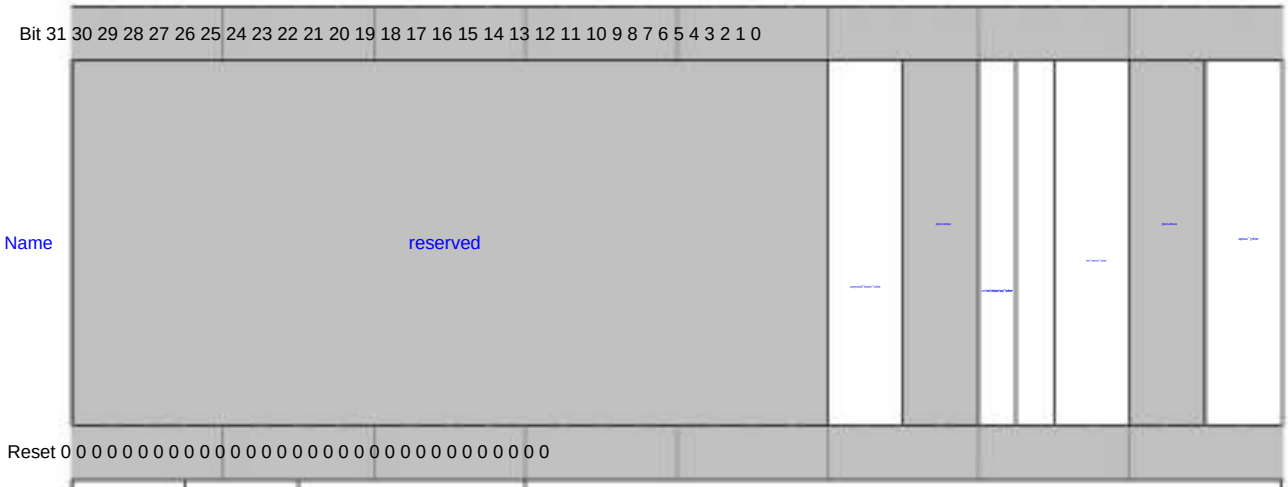
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RO	aop0_stop_done	AOP0 data transmission stop completion status. 0: not completed; 1: Done.
[0]	RW	aop0_enable	AOP0 data transmission start/stop control. 0: stop; 1: start.

AOP1_INF_ATTRI

AOP1_INF_ATTRI Set register for AOP1 interface attributes.

Offset Address	Register Name	Total Reset Value
0x2100	AOP1_INF_ATTRI	0x0000_0000



Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:10]	RW	aop1_samp_precise on	The precision configuration of AOP1 sent data. 00ÿ8bitÿ 01ÿ16bitÿ 10ÿ24bitÿ 11ÿ32bitÿ If multiplexing is enabled, only 8/16bit is supported; if multiplexing is not enabled, 8/16/24/32bit is supported in I2S mode, and 8/16bit is supported in PCM standard mode and PCM custom mode.
[9:8]	RW	reserved	Reserved, must be configured as 0x0.
[7]	RW	aop1_clk_edge_sel	Clock polarity selection for AOP1 transmit the clock; data. 0: The sent data is valid on the rising edge of 1: Transmitted data is valid on the falling edge of the clock.
[6]	RW	aop1_timedivision_ sel	AOP1 Multiplex enable. 0: disable multicast; 1: Enable multiplexing.

[5:4] RW	aop1_routes_sel		Channel number selection in AOP1 multiplexing mode. 00: 2 channels; 01: 4 channels; 10:8 way; 11:16 Road.
[3:2] RO		reserved	reserve.
[1:0] RW	aop1_mode		AOP1 mode selection. 00: I2S mode; 01: PCM standard mode; 10: PCM custom mode; 11: Reserved.

AOP1_CTRL

AOP1_CTRL is the AOP1 control register.

Offset Address	Register Name	Total Reset Value
0x2104	AOP1_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved, must be configured as 0x0.
[15]	RW	aop1_mute	AOP1 transmit mute enable. 0: no mute; 1: Mute.
[14:0]	RO	reserved	reserve.

AOP1_BUF_SADDR

AOP1_BUF_SADDR is the start address register of AOP1 circular buffer.

Offset Address	Register Name	Total Reset Value
0x2108	AOP1_BUF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aop1_buf_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	aop1_buf_saddr	The starting address of the circular buffer for AOP1. Note: It must be configured as an integer multiple of **128 .**

AOP1_BUF_SIZE

AOP1_BUF_SIZE is the circular buffer size register of AOP1.

Offset Address	Register Name	Total Reset Value
0x210C	AOP1_BUF_SIZE	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aop1_buf_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop1_buf_size	AOP1 circular buffer size in bytes. Note: It must be configured as an integer multiple of **128 .**

AOP1_BUF_WPTR

AOP1_BUF_WPTR is the write address register for AOP1 circular buffer.

Offset Address	Register Name	Total Reset Value
0x2110	AOP1_BUF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aop1_buf_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:0]	RW	aop1_buf_wptr	AOP1 circular buffer write address, in bytes. Note 1: The write address is the offset address relative to the start address of the circular buffer of **AOP1 .** Note 2: It must be configured as an integer multiple of **16 .** Note 3: The software must ensure that the free space of the circular buffer of **AOP1** is not less than **32** bytes.

AOP1_BUF_RPTR

AOP1_BUF_RPTR is the AOP1 circular buffer read address register.

Offset Address	Register Name	Total Reset Value
0x2114	AOP1_BUF_RPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_buf_rptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop1_buf_rptr	AOP1 circular buffer read address, in bytes. Note 1: The read address is the offset address relative to the start address of the circular buffer of **AOP1 .** Note 2: It must be configured as an integer multiple of **128 .**

AOP1_BUF_AEMPTY_TH

AOP1_BUF_AEMPTY_TH is the circular buffer almost empty threshold register for AOP1.

Offset Address	Register Name	Total Reset Value
0x2118	AOP1_BUF_AEMPTY_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_buf_aempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:0] RW		aop1_buf_aempty_t	AOP1's circular buffer almost empty threshold, in bytes. When the amount of valid data in the AOP1 circular buffer is less than the threshold, an AOP1 circular buffer almost empty interrupt is generated. h Note: If **aop1_buf_aempty_int** interrupt is used, the threshold must be configured as an integer multiple of **16** and greater than or equal to **0x80.**

AOP1_TRANS_SIZE

AOP1_TRANS_SIZE is the AOP1 data transfer length register.

Offset Address	Register Name	Total Reset Value
0x211C	AOP1_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_trans_size
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	aop1_trans_size	AOP1 data transfer length. When AOP1 finishes sending audio data of aop1_trans_size length (in bytes), an aop1_trans_int interrupt is generated. Note: If **aop1_trans_int is used, it must be configured to a value greater than or equal to 128 .**

AOP1_INT_ENA

AOP1_INT_ENA is the AOP1 interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x2120	AOP1_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
Name	reserved				
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	aop1_stop_int_en	Stop complete interrupt enable for AOP1. 0: disable; 1: enable.
[3]	RW	AOP1.int_en aop1_fifo_empty_i	FIFO empty interrupt enable for 0: disable; 1: enable.
[2]	RW	enable. disable; aop1_buf_aempty_int_en	AOP1 circular buffer almost empty interrupt 0: 1: enable.
[1]	RW	AOP1.int_en aop1_buf_empty_i	Circular buffer empty interrupt enable for 0: disable; 1: enable.
[0]	RW	aop1_trans_int_en	Transfer complete interrupt enable for AOP1. 0: disable; 1: enable.

AOP1_INT_RAW

AOP1_INT_RAW is the AOP1 raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x2124	AOP1_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	aop1_stop_int_raw	The stop of AOP1 completes the original interrupt. 0: no raw interrupt; 1: There is a raw interrupt.
[3]	RO	aop1_fifo_empty_i 0: no raw	FIFO empty raw interrupt for AOP1. interrupt; nt_raw 1: There is a raw interrupt.
[2]	RO	aop1_buf_aempty_i 0: no raw	AOP1's circular buffer is almost empty for raw interrupts. interrupt; nt_raw 1: There is a raw interrupt.
[1]	RO	aop1_buf_empty_i 0: no raw	AOP1 circular buffer empty raw interrupt. interrupt; nt_raw 1: There is a raw interrupt.
[0]	RO	aop1_trans_int_raw	AOP1's transfer complete raw interrupt. 0: no raw interrupt; 1: There is a raw interrupt.

AOP1_INT_STATUS

AOP1_INT_STATUS is the AOP1 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x2128	AOP1_INT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4]	RO	aop1_stop_int_stat 0: no interrupt status; 1: interrupt status.	Stop complete interrupt status for AOP1.
[3]	RO	aop1_fifo_empty_i 0: no interrupt status; nt_status 1: There is an interrupt status.	FIFO empty interrupt status for AOP1.
[2]	RO	aop1_buf_aempty_i 0: no interrupt status; nt_status 1: There is an interrupt status.	AOP1's circular buffer is almost empty interrupt state.
[1]	RO	aop1_buf_empty_i 0: no interrupt status; nt_status 1: interrupt status.	Circular buffer empty interrupt status for AOP1.
[0]	RO	aop1_trans_int_stat 0: no interrupt status; 1: There is an interrupt status.	Transfer complete interrupt status for AOP1.

AOP1_INT_CLR

AOP1_INT_CLR is the AOP1 interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x212C	AOP1_INT_CLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	aop1_stop_int_clr	The stop of AOP1 completes the interrupt clear. Write 0: not clear; write 1: clear.
[3]	RW	aop1_fifo_empty_int_clr	FIFO empty interrupt clear for AOP1. Write 0: not clear; write 1: clear.
[2]	RW	aop1_buf_aempty_int_clr	AOP1 ring buffer almost empty interrupt cleared. Write 0: not clear; write 1: clear.
[1]	RW	aop1_buf_empty_int_clr	AOP1's circular buffer empty interrupt is cleared. Write 0: not clear; write 1: clear.
[0]	RW	aop1_trans_int_clr	The AOP1 transfer complete interrupt is cleared. Write 0: not clear; write 1: clear.

AOP1_BUF_WPTR_TMP

AOP1_BUF_WPTR_TMP is the write address latch register for AOP1 circular buffer.

Offset Address	Register Name	Total Reset Value
0x2130	AOP1_BUF_WPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_buf_wptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	aop1_buf_wptr_tmp	When an AOP1 transfer complete interrupt occurs, the value of aop1_buf_wptr is saved to aop1_buf_wptr_tmp until the AOP1 transfer complete interrupt occurs again.

AOP1_BUF_RPTR_TMP

AOP1_BUF_RPTR_TMP is the circular buffer read address latch register of AOP1.

Offset Address	Register Name	Total Reset Value
0x2134	AOP1_BUF_RPTR_TMP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aop1_buf_rptr_tmp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RO	aop1_buf_rptr_tmp	When an AOP1 transfer complete interrupt occurs, the value of aop_buf_rptr is saved to aop1_buf_rptr_tmp until the AOP1 transfer complete interrupt occurs again.

AOP1_STOP

AOP1_STOP is the AOP1 start/stop register.

Offset Address	Register Name	Total Reset Value
0x2138	AOP1_STOP	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	aop1_stop_done	AOP1 data transmission stop completion status. 0: not completed; 1: Done.
[0]	RW	aop1_enable	AOP1 data transmission start/stop control. 0: stop; 1: start.

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14 peripheral equipment

14.1 I2C

14.1.1 Overview

I 2 The C module is a slave device on the APB bus, and it is an I-to-I 2 Master device on the C bus. I 2 The role of the C module is to complete the CPU 2 Data read and write from the device on the C bus. When the CPU writes to the slave device, the CPU passes the APB bus configuration 2 C's configuration registers, then send control information and operands to the I 2 Data communication register of C module; I 2 After the C module parses the command, the data of the data channel register passes through the I 2 The C bus is sent to the slave device, and the final state is fed back to the CPU through an interrupt after the transmission is completed. The process of CPU reading slave device data is similar to writing operation.

14.1.2 Functional Description

I 2 C has the following features:

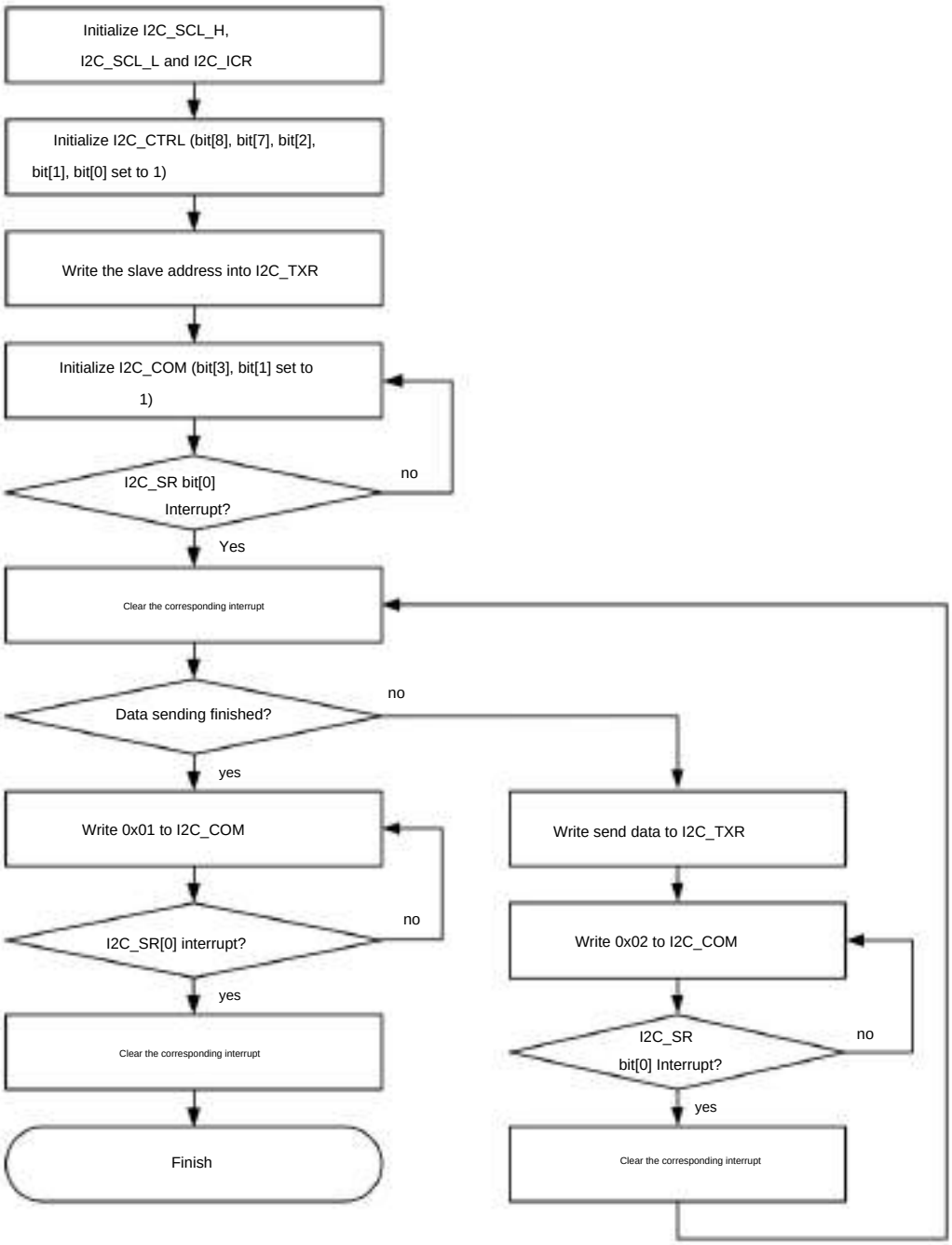
- I of Hi3520D chip 2 C is the Master interface, I 2 The working reference clock of C is 1/4 bus clock.
- Bus arbitration when multi-master is supported.
- Support Clock synchronization and Bit and Byte waiting. Support standard address (7bit) and extended address (10bit). Can work in two speed modes: standard mode (100kbit/s), fast mode (400kbit/s). Support General Call and Start Byte functions. CBUS devices are not supported. Filters the received SDA and SCL signals.

14.1.3 Working method

14.1.3.1 I2C initialization configuration process

The C master can write data to the slave, and can also receive data from the slave. I 2 The process of C host sending data is as follows: 2I as shown in Figure 14-1 .

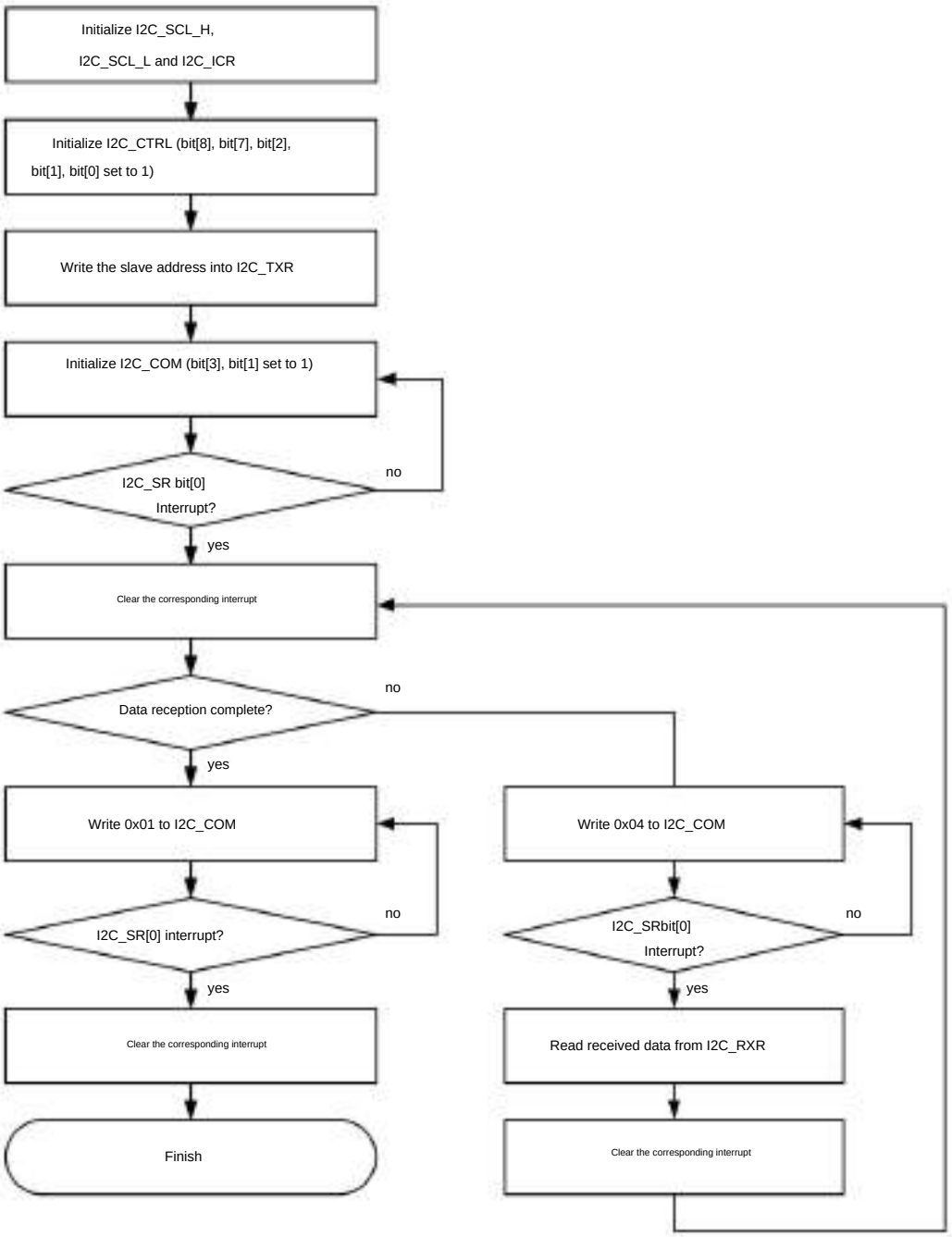
Figure 14-1 Flowchart of host sending data



14.1.3.2 Process of host receiving data

The process of receiving data by the host is shown in Figure 14-2 .

Figure 14-2 Flow chart of host receiving data



14.1.4 Register overview

Hi3520D contains an I ^{2}C module, the register overview is shown in Table 14-1 .

Table 14-1 I²C register overview (base address is 0x200D_0000)

address	name	type	description	page number
0x00	I2C_CTRL	RW	I²C control register	14-4
0x04	I2C_COM	RW	I²C command register	14-5
0x08	I2C_ICR	RW	I²C interrupt clear register	14-6
0x0C	I2C_SR	RO	I²C status register	14-7
0x10	I2C_SCL_H	RW	I²C SCL high level cycle number	14-9
0x14	I2C_SCL_L	RW	I²C SCL low level cycle number	14-10
0x18	I2C_TXR	RW	I²C send data register	14-10
0x1C	I2C_RXR	RO	I²C receive data register	14-11

14.1.5 Register Description

I2C_CTRL

I2C_CTRL is I²C control register. Used to configure I²C Enable and interrupt mask.

Offset Address	Register Name	Total Reset Value
0x00	I2C_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:9]	reserved	reserve.
[8] RW i2c_en		I²C enable. 0: Disable; 1: Enable.
[7] RW int_mask		I²C interrupt total mask. 0: shielded; 1: No shielding.

[6] RW int_start_mask			Master start condition send end interrupt mask. 0: shielded; 1: No shielding.
[5] RW int_stop_mask			Master stop condition sends end interrupt mask. 0: shielded; 1: not shielded.
[4] RW int_tx_mask			Host sends interrupt mask. 0: shielded; 1: No shielding.
[3] RW int_rx_mask			Host receive interrupt mask. 0: shielded; 1: No shielding.
[2] RW int_ack_err_mask			Slave ACK error interrupt mask. 0: shielded; 1: not shielded.
[1] RW int_arb_loss_mask			Bus arbitration loss interrupt mask. 0: shielded; 1: No shielding.
[0] RW int_done_mask			Bus transfer complete interrupt mask. 0: shielded; 1: No shielding.

I2C_COM

I2C_COM is I ^{2} Command register for the C module. Used to configure I ^{2} C module work-time command.

注意

Before configuring or configuring during system initialization, the corresponding interrupt flag needs to be cleared. I2C_COM bit[3:0] will be automatically cleared to 0 after the operation is completed.

Offset Address	Register Name	Total Reset Value
0x04	I2C_COM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]		reserved	reserve.
[4]	RW	op_ack	Whether the host as a receiver sends an ACK. 0: send; 1: Do not send.
[3]	RW	on_start	Produces a start condition operation. 0: operation ended; 1: The operation is valid.
[2]	RW	op_rd	Generate a read operation. 0: operation ended; 1: The operation is valid.
[1]	RW	op_we	Generate a write operation. 0: operation ended; 1: The operation is valid.
[0]	RW	up_stop	Generate stop condition action. 0: operation ended; 1: The operation is valid.

I2C_ICR

I2C_ICR is I ^{2} Interrupt clear register for the C module.

注意

When a new interrupt arrives, the I2C module will automatically clear the corresponding bit of I2C_ICR to 0.

Offset Address	Register Name	Total Reset Value
0x08	I2C_ICR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:7]	reserved	reserve.
[6] WC clr_int_start		Host start condition transmit end interrupt flag is cleared. 0: do not clear; 1: Clear.
[5] WC clr_int_stop		The master stop condition transmits the end of the interrupt flag cleared. 0: do not clear; 1: Clear.
[4] WC clr_int_tx		Master sends interrupt flag cleared. 0: do not clear; 1: Clear.
[3] WC clr_int_rx		Master receive interrupt flag is cleared. 0: do not clear; 1: Clear.
[2] WC clr_int_ack_err		Slave ACK error interrupt flag is cleared. 0: do not clear; 1: Clear.
[1] WC clr_int_arb_loss		The bus arbitration failure interrupt flag is cleared. 0: not clear; 1: clear.
[0] WC clr_int_done		The bus transfer complete interrupt flag is cleared. 0: do not clear; 1: Clear.

I2C_SR

I2C_SR is I ^{2}C module status register. for reading I ^{2}C module working status.

注意

I2C_SR bit[1] indicates I2C bus arbitration failure. When I2C_SR bit[1] is valid, the current operation fails. Before clearing I2C_SR bit[1], you need to clear other interrupt flags, then clear I2C_COM or write a new operation command to I2C_COM, and finally clear I2C_SR bit[1].

Offset Address	Register Name	Total Reset Value
0x0C	I2C_SR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:8]		reserved	reserve.
[7]	RO	bus_busy	The bus is busy. 0: idle; 1: Busy.
[6]	RO	int_start	Host start condition sends end interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.
[5]	RO	int_stop	Master stop condition sends end interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.
[4]	RO	int_tx	Host sends interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.
[3]	RO	int_rx	Host receives interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.
[2]	RO	int_ack_err	Slave ACK error interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.

[1]	RO	int_arb_loss	Bus arbitration failure interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.
[0]	RO	int_done	Bus transfer complete interrupt flag. 0: No interrupt flag generated; 1: Interrupt flag generated.

I2C_SCL_H

I2C_SCL_H is the number[2] C bus SCL signal high cycle number register. Used to configure I[2] SCL when C module works of I high level cycles.

注意

Set I2C_CTRL bit[7]=0 during system initialization or before configuration.

Offset Address	Register Name	Total Reset Value
0x10	I2C_SCL_H	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	scl_h
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	-	reserved	reserve.
[15:0]	RW scl_h		SCL high period count. The actual configuration value is SCL high period number x 2-1.

Let I[2] The working reference clock of C is 108MHz, the value of I2C_SCL_H is m, the high level time of SCL is DelTim, then:

DelTim = (1/108)× (m +1)× 2; (unit: µs)

Assuming that the SCL high level time is expected to be 5µs, the I2C_SCL_H configuration value m is:

m = (5×108)/ 2 ÿ1 = 269 ÿ

I[2] The working reference clock of C is 108MHz, and the maximum time of SCL high level is 606µs.

I2C_SCL_L

I2C_SCL_L is the number[2] C bus SCL signal low cycle number register. Used to configure I[2] SCL when C module works of I low level cycles.

注意

Set I2C_CTRL bit[7]=0 during system initialization or before configuration.

Offset Address	Register Name	Total Reset Value
0x14	I2C_SCL_L	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	scl_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	reserve.
[15:0]	RW	scl_l	SCL low period number %2.

Let I ^{2}C The working reference clock is 108MHz, the value of I2C_SCL_L is m, the low level time of SCL is DelTim, then:

DelTim = (1/108)× (m +1)× 2 (unit: μs)

Assuming that the SCL low level time is expected to be 5μs, the I2C_SCL_H configuration value m is:

m = (5×108)/ 2 ÿ1 = 269

I ^{2}C The working reference clock is 108MHz, and the maximum time of SCL low level is 606μs.

I2C_TXR

I2C_TXR is I ^{2}C Transmit data register. Used to configure I ^{2}C Send data while the C module is working.

注意

After sending, I ^{2}C The module does not modify the I2C_TXR content.

Offset Address	Register Name	Total Reset Value
0x18	I2C_TXR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / i2c_txr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	-	reserved	reserve.
[7:0]	RW	i2c_txr	Host sends data.

I2C_RXR

I2C_RXR is I^{2}C Receive data register. Used by the master to receive data from the slave.

注意

I2C_RXR data is valid when I2C_SR bit[3]=1. Meanwhile the data will be kept until the next read operation.

Offset Address	Register Name	Total Reset Value
0x1C	I2C_RXR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / i2c_rxr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	-	reserved	reserve.
[7:0]	RO	i2c_rxr	Host receives data.

14.2 SPI

14.2.1 Overview

The SPI controller realizes serial-to-parallel and parallel-serial conversion of data, and can be used as a Master to perform synchronous serial communication with external devices. Support MOTOROLA's SPI, TI serial synchronization, and MicroWire three peripheral interface protocols.

14.2.2 Features

注意

Hi3520D has 1 set of SPI interface, supports chip select 0 and chip select 1.

SPI chip select 1 of Hi3520D chip only supports Master interface, and chip select 0 supports both Master and Slave interfaces. The working reference clock is the APB bus clock, and the SPI_CLK output by the SPI supports a maximum of 38.75MHz.

The functional characteristics of SPI are:

The interface clock frequency is programmable.

FIFO with a width of 16bit and a depth of 256 for receiving/transmitting. The serial data frame length is programmable: 4bit ~ 16bit. A loopback test mode is provided internally.

DMA operation is supported.

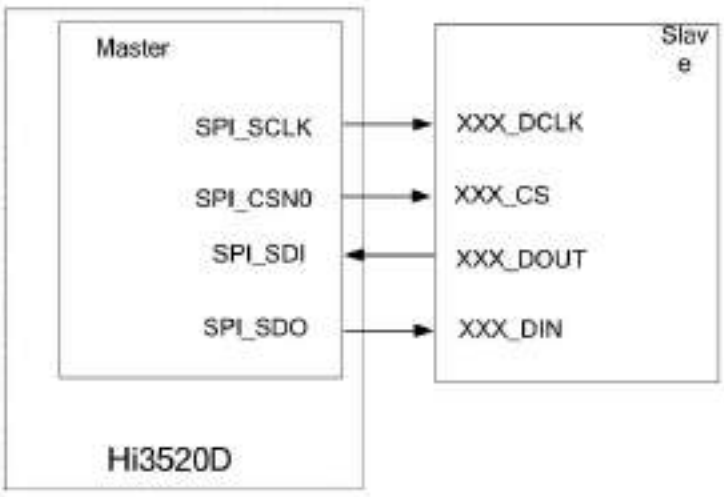
Support SPI, MicroWire, TI synchronous serial interface, support single frame and continuous frame format. Support SPI full-duplex working mode, clock polarity and phase can be configured. Supports MicroWire half-duplex mode of operation. Support TI synchronous serial interface full-duplex working mode.

14.2.3 Functional Description

typical application

The application block diagram when SPI is connected to Slave is shown in Figure 14-3 .

Figure 14-3 Application when SPI is connected to Slave



14.2.4 Three Peripheral Bus Timings

The meanings of the abbreviations in Figure 14-4 to Figure 14-11 are:

MSBÿMost Significant Bit

LSBÿLeast Significant Bit

QÿQ is an undefined signal

SPI interface

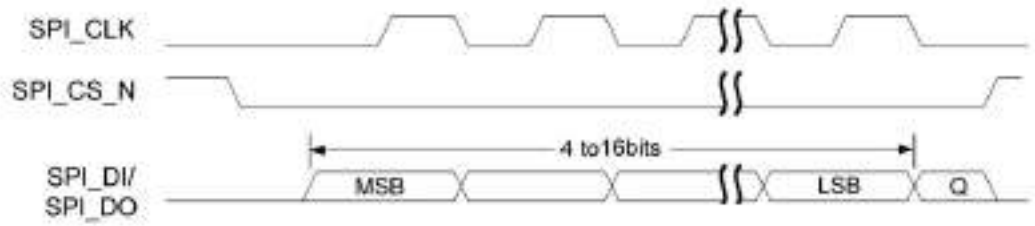
说明

SPO indicates SPICLKOUT polarity and SPH indicates SPICLKOUT phase. They are register SPICR0 bits[7:6].

ÿ1ÿSPO=0ÿSPH=0

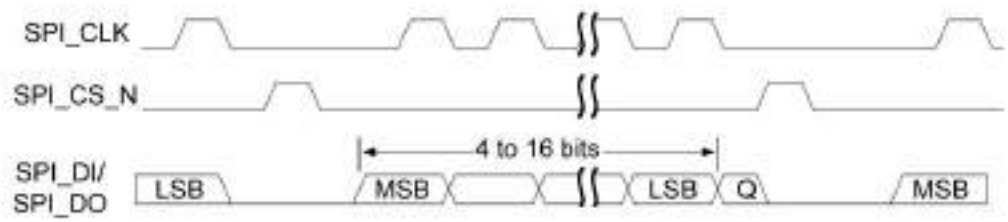
The SPI single frame frame format is shown in Figure 14-4 .

Figure 14-4 SPI single frame frame format (SPO=0, SPH=0)



The frame format of SPI continuous frame is shown in Figure 14-5 .

Figure 14-5 SPI continuous frame frame format (SPO=0, SPH=0)



In this mode, when the SPI is idle:

SPI_CLK signal is set low

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When the SPI is enabled and there is valid data in the send FIFO, set the SPI_CS_N signal to be low, which means start to transmit data. The data from Slave is immediately sent to Master's receiving data line SPI_DI. Valid Master data is transferred to SPI_DO after half a SPI_CLK clock cycle. At this time, the number of Master and Slave

The data are all valid, the SPI_CLK pin goes high after the next half SPI_CLK clock period. Data is captured on the rising edge of the SPI_CLK clock and transferred on the falling edge of the clock.

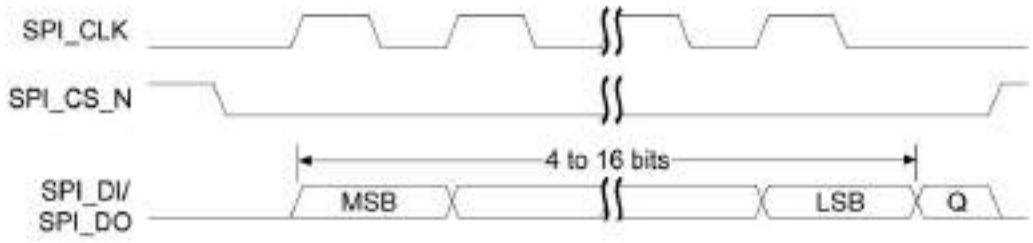
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock cycle.

If it is a continuous transmission, the SPI_CS_N signal must pull the SPI_CLK clock high for one clock cycle between each word transmission. This is because when SPH is 0, the Salve selection pin will fix the data of its internal serial device register so that it will not change. Therefore, during continuous transmission, the master device must pull the SPI_CS_N signal high between each word transmission. At the end of the continuous transmission, SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after the last 1 bit is captured.

ÿ2ÿSPO=0ÿSPH=1

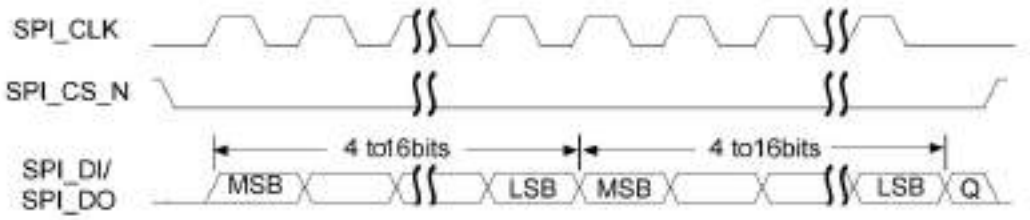
The SPI single frame frame format is shown in Figure 14-6 .

Figure 14-6 SPI single frame frame format (SPO=0, SPH=1)



The frame format of SPI continuous frame is shown in Figure 14-7 .

Figure 14-7 SPI continuous frame frame format (SPO=0, SPH=1)



In this mode, when the SPI is idle:

- SPI_CLK signal is set low
- SPI_CS_N set high transmit
- data line SPI_DO forced low

When the SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N signal to low to start transmitting data. After half a SPI_CLK clock cycle, the valid data of Master and Slave are valid on their respective transmission lines. At the same time, SPI_CLK is valid from the first rising edge. Data is captured on the falling edge of the SPI_CLK clock and transferred on the rising edge of the clock.

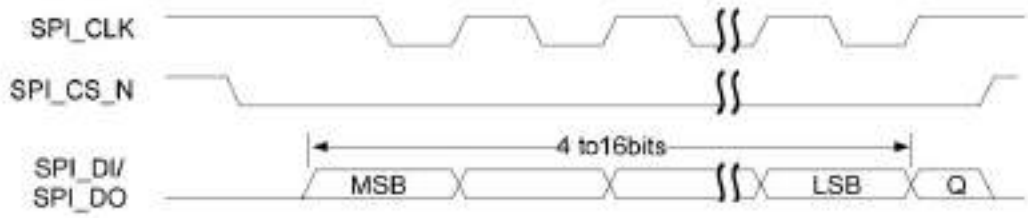
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock.

When transmitting continuously, SPI_CS_N is kept low between transmitted data words. At the end of the continuous transfer, SP_CS_N returns to high level after 1 SPI_CLK clock after the last 1 bit capture.

ÿ3ÿSPO=1ÿSPH=0

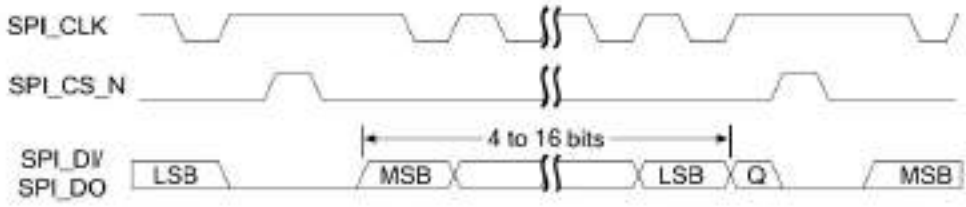
The SPI single frame frame format is shown in Figure 14-8 .

Figure 14-8 SPI single frame frame format (SPO=1, SPH=0)



The frame format of SPI continuous frame is shown in Figure 14-9 .

Figure 14-9 SPI continuous frame frame format (SPO=1, SPH=0)



In this configuration, when the SPI is idle:

SPI_CLK signal is set high

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When the SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N signal to low to start transmitting data. At this time, the data of Slave is sent to the receiving data line SPI_DI of Master immediately. After half a SPI_CLK cycle, the valid data of Master is transferred to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK Master pin is set low. This means that data is captured on the falling edge of the SPI_CLK clock and transferred on the rising edge of the SPI_CLK clock.

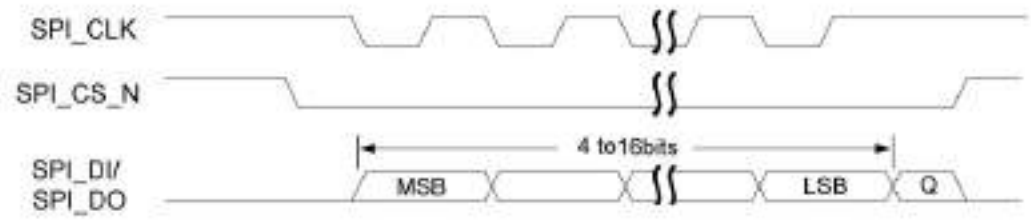
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock.

If it is a continuous transfer, the SPI_CS_N signal must be pulled high between each word transfer. This is because when SPH is 0, the Salve select pin fixes the data of its internal serial device register so that it will not change.
SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after capturing the last 1-bit data.

ÿ4ÿSPO=1ÿSPH=1

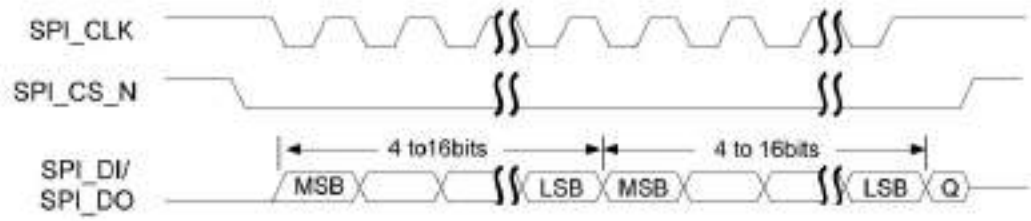
The SPI single frame frame format is shown in Figure 14-10 .

Figure 14-10 SPI single frame frame format (SPO=1, SPH=1)



The frame format of SPI continuous frame is shown in Figure 14-11 .

Figure 14-11 SPI continuous frame frame format (SPO=1, SPH=1)



In this mode, when the SPI is idle:

SPI_CLK signal is set high

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N Master signal to low to start transmitting data. After half a SPI_CLK clock cycle, the Master and Slave data are valid on their respective transmission lines. At the same time, the clock SPI_CLK is valid from 1 falling edge. Data is captured on the rising edge of the SPI_CLK clock and transferred on the falling edge of the clock.

When transmitting a single word, SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after the last 1 bit capture of the transmission.

For continuous transfers, the SPI_CS_N signal is always kept low. SPI_CS_N returns to high state 1 SPI_CLK clock cycle after the last 1 bit is captured. For continuous transfers, SPI_CS_N remains low during the transfer and ends in the same way as a single transfer.

(5) Interface timing

Figure 14-12 SPI interface timing diagram

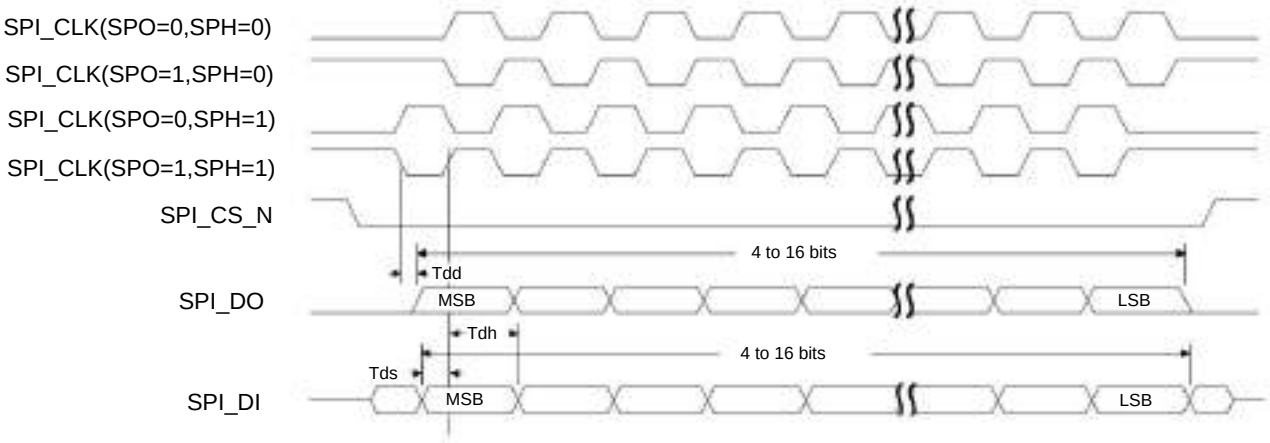


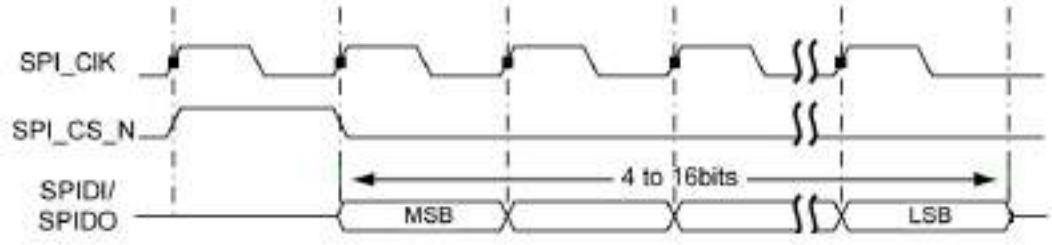
Table 14-2 SPI interface timing parameters

Parameter Description		min max unit		
Tdd output data delay		-3.5	5	ns
Tds	Input control signal setup time	23	-	ns
Tdh input control signal hold time		0	-	ns

TI synchronous serial interface

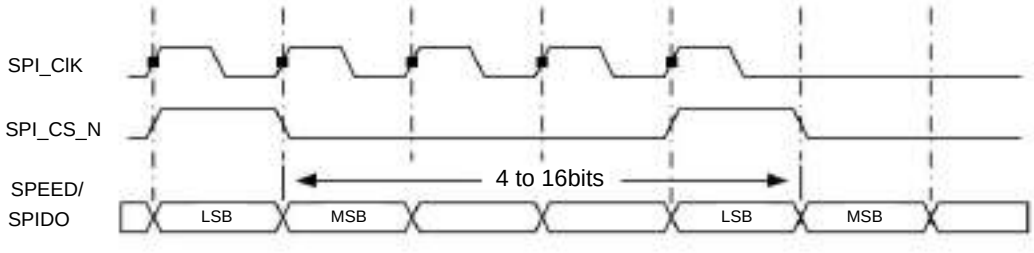
The frame format of TI synchronous serial single frame is shown in Figure 14-13 .

Figure 14-13 TI synchronous serial single frame frame format



The frame format of TI synchronous serial continuous frame is shown in Figure 14-14 .

Figure 14-14 TI synchronous serial continuous frame frame format



In this mode, when the SPI is idle:

SPICK is low.

SPICSN is low. The transmit

data line SPIDO remains high impedance.

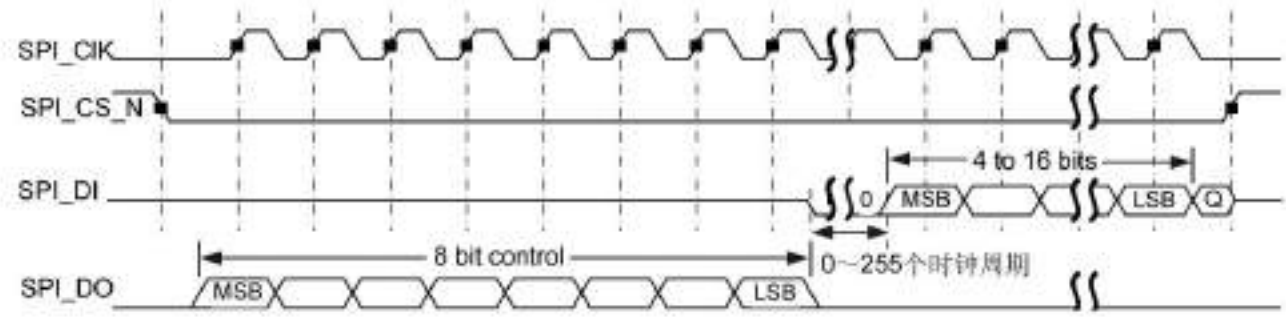
Once there is data in the transmit FIFO, SPICSN will generate a high-level pulse of a SPICK clock cycle, and the data to be transmitted will be transferred from the transmit FIFO to the transmit logic serial shift register. On the next rising edge of the SPICK clock, the MSB of the 4bit~16bit data frame will be shifted out from SPIDO. Likewise, the MSB of data received from an external serial slave device is shifted in from the SPIDI pin.

SPI and off-chip serial devices clock data into the serial shift register on the falling edge of the SPICK clock. The receive serial register sends data to the receive FIFO on the first rising edge of the SPICK clock after receiving the LSB.

National Semiconductor Microwire interface

The National Semiconductor Microwire single frame format is shown in Figure 14-15 .

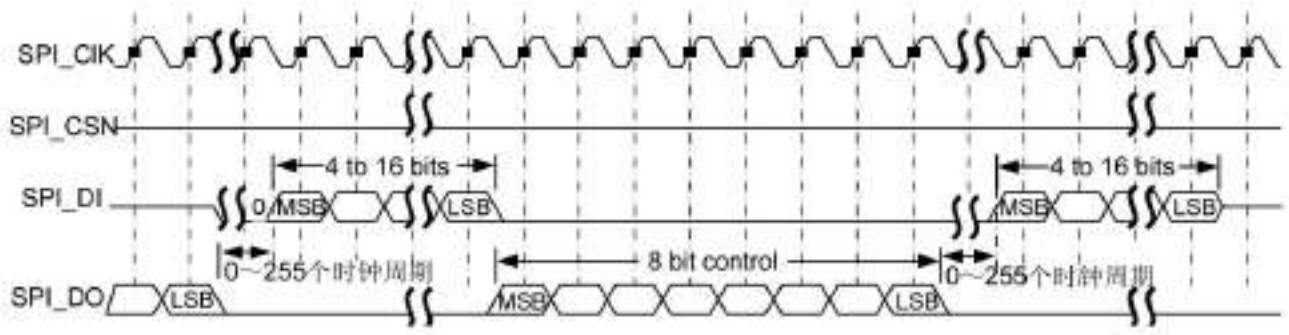
Figure 14-15 National Semiconductor Microwire single frame frame format



There can be a delay between 0 and 255 clock cycles between the end of the SPIDO LSB and the start of the SPIDI MSB.

The National Semiconductor Microwire continuous frame frame format is shown in Figure 14-16 .

Figure 14-16 National Semiconductor Microwire continuous frame frame format



There can be a delay of 0 to 255 clock cycles between the end of the SPI_DO LSB and the start of the SPI_DI MSB.

The format of Microwire is very similar to that of SPI, using master-slave information transmission technology, but SPI is full-duplex communication, while Microwire is half-duplex communication. When SPI sends serial data to external chips, 8-bit control word must be added first. During this process, the SPI does not receive any data. After the transmission is completed, the off-chip chip decodes the received data, and after a clock cycle interval from the 8bit control information, the slave starts to respond to the required data. The length of the returned data is 4bit~16bit, so that the length of the whole frame is 13bit~25bit.

In this mode, when the SPI is idle:

The SPI_CLK signal is set low.

SPI_CS_N is set high. The transmit

data line SPI_DO is forced low.

Writing a control byte internally to the transmit FIFO starts a transfer. The falling edge of SPI_CS_N triggers data transmission, the data in the transmit FIFO is sent to the serial shift register, and the MSB of the 8bit control frame is sent to the transmit pin SPIDO. During frame transmission, SPI_CS_N remains low. SPI_DI remains high impedance during this transfer.

The off-chip serial slave latches data into the serial shift register on every rising edge of the SPI_CLK clock. After the slave device has latched the last bit of data, it starts to decode the received data during the waiting time of the next clock cycle, and then feeds back the data required by the SPI from the device. Every 1 bit is written to SPI_DI on the falling edge of SPICK clock. For a single data transfer, at the end of the frame, SPI_CS_N is pulled high 1 clock cycle after the last bit is written to the receive serial register, thus causing the received data to be transferred to the receive FIFO.

For continuous transfers, the data transfer starts and ends in the same way as a single data transfer. During this transmission process, the signal SPI_CS_N is always kept low, and the transmitted data is also continuous. The control word of the next frame is directly adjacent to the LSB of the previous frame. After the LSB of the frame is latched into the SPI, each received value is taken from the receive shift register on the falling edge of the SPI_CLK clock.

14.2.5 Working method

Operating mode

The working mode of SPI is divided into data transmission in interrupt or query mode and data transmission in DMA mode.

Clock and Reset

The output SPI clock frequency is calculated as follows:

Fsspclkout = Fsspclk/ÿCPSDVRxÿ1+SCRÿÿ

Fsspclk: SPI working reference clock, 1/4 bus clock.

For CPSDVR and SCR, please check the corresponding registers.

SPI in Hi3520D supports independent soft reset, which is controlled by register PERI_CRG57 bit[6:5]. Write "0" to the corresponding bit, SPI exits soft reset; write "1" to the corresponding bit, SPI enters soft reset. The default value is 0 after power-on.

interrupt handling

The SPI has 5 interrupts, the first 4 of which are independent interrupt sources, maskable, active high.

SPIRXINTR

Receive FIFO interrupt request. This interrupt is set when there are 4 or more valid data in the receive FIFO.

SPITCHINTR

Send FIFO interrupt request. This interrupt is set when there are 4 or fewer valid data in the transmit FIFO.

SPIRO INTR

Receive overrun interrupt request. When FIFO is full and new data needs to be written into FIFO, it will cause FIFO overrun and this interrupt will be set. At this point data is written to the receive shift register instead of the FIFO.

SPIRINTTR

Receive time out interrupt request. This interrupt is set when the receive FIFO is not empty and the SPI is in idle state for more than a fixed 32bit period. This indicates

that there is still data to be transmitted in the receive FIFO. This interrupt is deasserted if the receive FIFO is read empty or when new data is received into SPIRXD. The interrupt can also be cleared by writing register SPIICR[RTIC].

SPINTR

Combined interrupt is the result of the above 4 interrupts after "OR" operation. This interrupt is asserted if any of the above 4 individual interrupts is asserted and enabled.

SPI Interrupt SPIINTR Please refer to the Interrupt Handling chapter.

initialization

The initialization steps are as follows:

1. Write "0" to register SPICR1[sse] to disable SPI.
2. Write register SPICR0 to configure parameters such as frame format and transmission data bit width.
3. Configure the register SPICPSR to set the clock frequency division factor.
4. In the interrupt mode, set the register SPIIMSC to enable the corresponding interrupt signal; in the query and DMA mode, the generation of the corresponding interrupt signal should be prohibited.
5. Interrupt or DMA mode, set SPITXFIFOCR and SPIRXFIFOCR.
6. In DMA mode, configure the register SPIDMACR to enable the DMA function of SPI.

----Finish

Data transfer in query mode

Since the transmit/receive FIFO depth is 512, it is generally not necessary to consider FIFO fullness.

Specific steps are as follows:

1. Write "1" to register SPICR1[sse] to enable SPI.
2. Write the data to be sent continuously to the register SPIDR.
3. Poll the register SPISR until [BSY]=0 (indicating that the bus is not busy), [TFE]=1 (indicating that the sending FIFO is empty), [RNE]=1 (indicating that the receiving FIFO is not empty), then go to step 5.
4. To read data, it is necessary to ensure that the receiving FIFO is empty (obtained by querying SPISR[RNE]).

注意

The full-duplex feature of SPI/Microwire, every time a data is sent, a data is received, even if only data is sent, the receiving FIFO needs to be cleared.

5. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

Data transfer in interrupt mode

Specific steps are as follows:

1. Write "1" to register SPICR1[sse] to enable SPI.
2. Write the data to be sent continuously to the register SPIDR.
3. Wait for the interrupt SPIRXINTR to read the data. Loop until all data is read.

注意

The full-duplex feature of SPI/Microwire, every time a data is sent, a data is received, even if only data is sent, the receiving FIFO needs to be cleared.

4. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

Data transfer in DMA mode

Specific steps are as follows:

1. Acquire a DMAC channel.

2. Write "1" to register SPICR1[sse] to enable SPI.

3. Send data

   a. Configure the relevant parameters in the configuration register and control register of the DMAC channel. b. Start the DMAC to respond to the DMA request of the SPI transmit FIFO for data transmission.

   c. Report through DMA interrupt to judge whether the data transmission is completed, and if it is completed, turn off the DMA function of SPI able.

4. Receive data

   a. Configure the relevant parameters in the configuration register and control register of the DMAC channel. b. Start the DMAC to respond to the DMA request of the SPI receive FIFO for data transmission.

   c. Report through the DMA interrupt to judge whether the data is received, and if it is completed, turn off the DMA function of the SPI able.

5. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

14.2.6 Register overview

An overview of the SPI registers is shown in Table 14-3 .

Table 14-3 SPI register overview (base address is 0x200C_0000)

offset address name		describe	page number
0x000	SPICR0	control register 0	14-23
0x004	SPICR1	control register 1	14-24
0x008	SPIDR	data register	14-25
0x00C	SPISR	status register	14-25
0x010	SPICPSR	Clock Divider Register	14-26
0x014	SPIIMSC	interrupt mask register	14-27
0x018	BREATHED	Raw Interrupt Status Register	14-28
0x01C	SPAM	Masked Interrupt Status Register	14-28
0x020	SPIICR	Interrupt Clear Register	14-29
0x024	SPIDMACR	DMA Control Register	14-29
0x028	SPITXFIFOCR Transmit FIFO Control Register		14-30
0x02C	SPIRXFIFOCR Receive FIFO Control Register		14-31

14.2.7 Register Description

SPICR0

SPICR0 is Control Register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12 11 10 9	8	7	6	5	4	3	2	1	0
Name	SCR					SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, the value ranges from 0 to 255. The value of SCR is used to generate the SPI transmit and receive bit rate, the formula is FSPICLK/(CPSDVSRÿ(1+SCR)). CPSDVSR is an even number between 2 and 254, configured by register SPICPSR.
[7]	RW	SPH	SPICLKOUT phase, for specific meaning, please refer to the SPI frame format in "14.2.4 Three Peripheral Bus Timings" .
[6]	RW	SPO	SPICLKOUT polarity, please refer to the SPI frame format in "14.2.4 Three Peripheral Bus Timings" for specific meaning.
[5:4]	RW	FRF	Frame format selection. 00: Motorola SPI frame format; 01: TI synchronous serial frame format; 10: National Microwire frame format; 11: Reserved.

[3:0] RW DSS			Set the data bit width. 0011ÿ4bitÿ 1000ÿ9bitÿ 1101ÿ14bitÿ 0100ÿ5bitÿ 1001ÿ10bitÿ 1110ÿ15bitÿ 0101ÿ6bitÿ 1010ÿ11bitÿ 1111ÿ16bitÿ 0110ÿ7bitÿ 1011ÿ12bitÿ 0111ÿ8bitÿ 1100: 13bit; others: reserved.

SPICR1

SPICR1 is Control Register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14 13 12 11 10 9 8 7	6 5	4	3	2	1	0
Name	WaitEn	WaitVal	reserved	BigEnd	reserved	MS	SSE	LBM
Reset	0	1 1 1 1 1 1 1	1 0 0 0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Waiting to be enabled, it is valid when the FRF of SPICR0 register is configured as National Microwire frame format. 0: disable; 1: enable.
[14:8]	RW	WaitVal	The number of beats to wait between writing and reading in National Microwire frame format. Valid when WaitEn is 1 and the frame format is National Microwire.
[7:5]	RW	reserved	Reserved.

[4]	RW	BigEnd	Set the data size endian mode. 0: end of little endian; 1: Big endian.
[3]	RW	reserved	Reserved.
[2]	RW	MS	Set Master or Slave mode, this bit can only be changed when SPI is disabled. 0: Master mode (default); 1: Reserved.
[1]	RW	SSE	Set SPI enable. 0: disable; 1: enable.
[0]	RW	LBM	Set the loopback mode. 0: Normal serial interface operation enabled; 1: The output of the transmit serial shift register is internally connected to the input of the receive serial shift register.

SPIDR

SPIDR is the data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	Transmit/receive FIFO. Read: Receive FIFO; Write: Transmit FIFO. If the number of data bits is less than 16, it must be right justified. The transmit logic ignores the upper unused bits, and the receive logic automatically right-aligns the data.

SPISR

SPISR is the status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15 14	13 12 11 10 9 8 7 6 5	4	3	2	1	0
Name	reserved		BSY	RFF	RNE	TNF	TFE
Reset 0	0 0	0 0 0 0 0 0 0 0 0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved.
[4]	RW	BSY	SPI busy flag. 0: idle; 1: Busy.
[3]	RW	RFF	Whether the receive FIFO is full. 0: not full; 1: full.
[2]	RW	RNE	Whether the receive FIFO is not empty. 0: empty; 1: not empty.
[1]	RW	TNF	Whether the transmit FIFO is not full. 0: full; 1: not full.
[0]	RW	TFE	Whether the transmit FIFO is empty. 0: not empty; 1: Empty.

SPICPSR

SPICPSR is the clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	reserve.
[7:0]	RW	CPSDVSR	Clock division factor. This value must be an even number between 2 and 254, depending on the frequency of the input clock SPICLK. The lowest bit is read as "0".

SPIIMSC

SPIIMSC is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15 14 13 12 11 10 9	8 7 6 5 4	3	2	1	0
Name	reserved		TXIM	RXIM	RTIM	RORIM
Reset 0	0 0 0 0 0 0 0 0 0		0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved.
[3]	RW	EXCLUSIVE	Transmit FIFO interrupt mask. 0: Interrupts are masked when half-empty or less; 1: Interrupts are not masked when half-empty or less.
[2]	RW	RXIM	Receive FIFO interrupt mask. 0: Interrupts are masked when half-empty or less; 1: Interrupts are not masked when half-empty or less.
[1]	RW	RTIM	Receive timeout interrupt. 0: Receive timeout interrupt mask; 1: Receive timeout interrupt not masked.

[0] RW RORIM			Receive overflow interrupt mask. 0: receive FIFO overflow interrupt mask; 1: receive FIFO overflow interrupt not mask. When the value is "1", the hardware flow control function is enabled, that is, the SPI stops sending data when the receive FIFO is full.

BREATHED

SPIRIS is the raw interrupt status register. A value of "0" means no interruption and a value of "1" means interruption.

Offset Address	Register Name	Total Reset Value
0x018	BREATHED	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXRIS	Raw interrupt status of transmit FIFO interrupt.
[2]	RO	RXRIS	Raw interrupt status for receive FIFO interrupts.
[1]	RO	RTRIS	Raw interrupt status of receive timeout interrupt.
[0]	RO	RORRIS	Raw interrupt status of receive overflow interrupt.

SPAM

SPIMIS is the masked interrupt status register. A value of "0" means no interruption and a value of "1" means interruption.

Offset Address	Register Name	Total Reset Value
0x01C	SPAM	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXMIS	Transmit FIFO interrupt masked status.
[2]	RO	RXMIS	Receive FIFO interrupt masked status.
[1]	RO	RTMIS	Receive timeout interrupt masked state.
[0]	RO	RORMIS	Receive overflow interrupt masked status.

SPIICR

SPIICR is the interrupt clear register. Writing a "1" clears the interrupt, writing a "0" has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved.
[1]	RO	RTIC	Clear receive timeout interrupt.
[0]	RO	RORIC	Clear receive overflow interrupt.

SPIDMACR

SPIDMACR is the DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12 11	10 9 8 7 6 5 4 3 2	1	0
Name	reserved					TXDMAE	RXDMAE
Reset 0	0	0	0	0	0 0 0 0 0 0 0 0 0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved bits.
[1]	WO	TXDMAE	DMA transmit FIFO enable register. 0: forbidden; 1: enable.
[0]	WO	RXDMAE	DMA receive FIFO enable register. 0: forbidden; 1: enable.

SPITXFIFOCR

SPITXFIFOCR is the transmit FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0009

Bit	15 14	13	12	11	10	9	8 7	6	5	4	3	2	1	0
Name	reserved								TXINTSize				DMATXBRSize	
Reset 0	0	0	0	0	0	0	0 0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	reserve.

[5:3]	RW	TXINTSize	Configure the waterline for transmit FIFO request interrupts. That is, send When the number of data in FIFO is less than or equal to the number of words configured by TXINTSize, TXRIS is valid. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ64ÿ 111ÿ64ÿ
[2:0]	RW	DMATXBRSize	Configure the waterline that sends FIFO requests to DMA for burst transfers. That is, when the number of data in the transmit FIFO is less than or equal to the number of words configured by (256-DMATXBRSize), DMATXBREQ is valid, and the word length here is 16 bits. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ128ÿ

SPIRXFIFOCR

SPIRXFIFOCR is the receive FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize		DMARXBRSize			
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name		Description
[15:6]	RW	reserved		reserve.

[5:3]	RW	RXINTSize	Configure the watermark for receive FIFO request interrupts. That is, when the number of data in the receiving FIFO is greater than or equal to the number of words configured by (256-RXINTSize), RXRIS is valid, and the word length here is 16 bits. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ64ÿ 111ÿ64ÿ
[2:0]	RW	DMARXBRSize 010ÿ8ÿ	Configure the waterline for receiving FIFO request DMA for burst transfer. That is, when the number of data in the receive FIFO is greater than or equal to the number of words configured by DMARXBRSize, DMARXBREQ is valid. 000ÿ1ÿ 001ÿ4ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ224ÿ

14.3 Universal Asynchronous Transceiver

14.3.1 Overview

Universal Asynchronous Receiver Transmitter UART (Universal Asynchronous Receiver Transmitter) is an asynchronous serial communication interface. Its main function is to transfer data from peripheral devices to the internal bus after serial-to-parallel conversion, and output the data to the outside after parallel-to-serial conversion. equipment. The main function of UART is to connect with the UART of the external chip, so as to realize the communication between the two chips.

Hi3520D provides 4 UART units:

UART0: 2-wire UART, mainly used for debugging.

UART1: 4-wire UART, mainly used for PTZ control.

UART2: 2-wire UART, mainly used for alarm function, and can also be used for docking with common UART devices.

UART3: 2-wire UART, mainly used for alarm function, and can also be used for docking with common UART devices.

14.3.2 Features

The UART module has the following features:

Support 16 x 8bit transmit FIFO and 16 x 12bit receive FIFO. Support data bit and stop bit width programmable. Data bits can be programmed as 5/6/7/8 bits; stop bits can be programmed as 1bit or 2bit.

Support odd, even parity or no parity.

Support transfer rate programmable.

Support receive FIFO interrupt, send FIFO interrupt, receive timeout interrupt, error interrupt. Supports initial interrupt status query and masked interrupt status query. Support programming to disable UART module or UART transmit/receive function to reduce power consumption.

Supports shutting down the UART clock to save power.

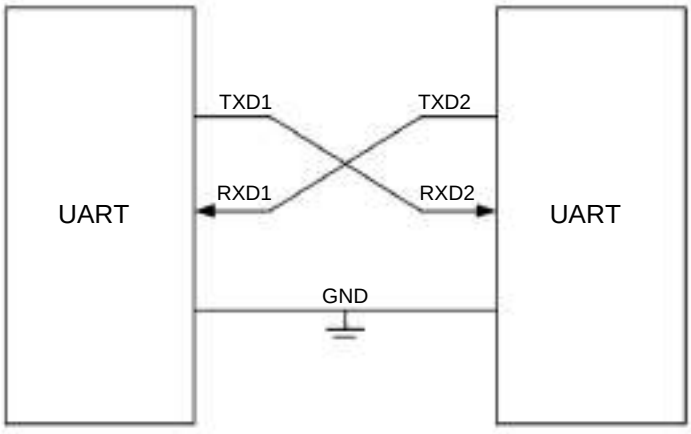
DMA operation is supported.

14.3.3 Functional description

Application Block Diagram

A typical application block diagram of UART is shown in Figure 14-17 .

Figure 14-17 Typical application block diagram of UART



UART is an asynchronous bidirectional serial bus that provides a simple and efficient way of data transmission, requiring only two data lines to be connected to each other.

Functional principle

A frame transmission of UART mainly includes start signal, data, parity bit and end signal, as shown in Figure 14-18 . The data frame is output from the TXD end of one UART and input from the RXD end of another UART.

Figure 14-18 UART frame format

The meanings of start signal, data, parity bit and end signal are as follows:

Start signal (start bit) A sign of the

beginning of a data frame. The UART protocol stipulates that a low level of the TXD signal indicates the beginning of a data frame. When the UART is not transmitting data, it should be kept high. Data signal (data bit)

The data bit width can be adjusted according to different application requirements, and can be configured as 5bit/6bit/7bit/8bit data bit width. Parity bit

(parity bit) The parity bit is a 1-bit

error correction signal. The parity bit of UART includes odd parity, even parity and fixed parity. It also supports the enable and disable of the parity bit. Please refer to See UART_LCR_H register. End signal (stop bit) The end signal is the stop bit of the data

frame, which supports two

configurations of 1-bit stop bit and 2-bit stop bit. The end signal of the data frame is to pull TXD into high level.

14.3.4 Working method

14.3.4.1 Baud Rate Configuration

The baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD . The formula for calculating the baud rate is:

Current baud rate = UART reference clock frequency (1/4 bus clock frequency or 2MHz) / (16 x frequency division factor)

The frequency division coefficient consists of two parts, integer and decimal, which correspond to registers UART_IBRD and UART_FBRD respectively.

For example: UART reference clock frequency is 60MHz, if UART_IBRD is set to 0x1E, UART_FBRD is set to 0x00, according to the baud rate calculation formula, the current baud rate is 60/(16 x 30)=0.125Mbit/s.

Typical values of UART baud rate configuration are: 9,600bit/s, 14,400bit/s, 19,200bit/s, 38,400bit/s, 57,600bit/s, 76,800bit/s, 115,200bit/s, 230,400bit/s, 460,800bit/s.

The calculation of the frequency division coefficient value and the configuration of the frequency division coefficient register are as follows:

If the required baud rate is 230400bit/s, and the UART reference clock frequency is 100MHz, then the frequency division factor is (100 x 106)/(16 x 230400) = 27.1267, so IBRD (integer part) is 27, FBRD (fractional part) is 0.1267.

Calculate the value in the 6bit UART_FBRD register: According to m=integer (FBRDx2n +0.5) (n= the width of the UART_FBRD register), calculate m=integer (0.1267x26 +0.5)=8, configure 0x001B in the UART_IBRD register, and configure 0x001B in the UART_FBRD register Configure 0x08.

When the fractional part of the frequency division factor is configured as 8, the actual value of the baud rate divisor is 27+8/64=27.125, and the resulting baud rate is (100 x 106) /(16 x 27.125)=230414.75, and the error rate is (230414.75–230400) /230400x100=0.006%ÿ

Using the 6bit UART_FBRD register, the maximum error rate is 1/64 x 100=1.56%, which occurs when m=1, and the error rate accumulates over 64 clock cycles.

14.3.4.2 Soft Reset

A separate soft reset for the UART controller can be achieved by configuring the CRG register.

By configuring the CRG register PERI_CRG57[7] to be 1, the individual soft reset of the UART0 controller can be realized.

By configuring the CRG register PERI_CRG57[8] to be 1, the individual soft reset of the UART1 controller can be realized. By

configuring the CRG register PERI_CRG57[9] to be 1, the individual soft reset of the UART2 controller can be realized. By configuring the

CRG register PERI_CRG57[10] to be 1, the individual soft reset of the UART3 controller can be realized.

The value of each configuration register is the default value after reset, so these registers need to be initialized and configured again after reset.

14.3.4.3 Data transfer in interrupt or query mode

initialization

The initialization steps are as follows:

1. Write 0 to UART_CR bit[0] to disable UART.
2. Write corresponding configuration values to the UART_IBRD and UART_FBRD registers to configure the transmission rate.
3. Configure UART_CR, UART_LCR_H, and set the corresponding UART working mode.
4. Configure UART_IFLS to set the corresponding transmit and receive FIFO thresholds.
5. If the driver uses the interrupt method, it is necessary to set UART_IMSC to enable the corresponding interrupt signal; use the query method

   The generation of the corresponding interrupt signal should be prohibited during the mode.
6. Write 1 to UART_CR bit[0] to enable UART and complete the initial configuration.

----Finish

data transmission

The data sending steps are as follows:

1. Write the sending data into UART_DR to start data sending.

2. In the query mode, the TX_FIFO status is detected by reading the UART_FR bit[5] during continuous data transmission.
   The state of TX_FIFO determines whether to send data to TX_FIFO; in interrupt mode, it detects according to the corresponding interrupt status bit; decides whether to send data to TX_FIFO.
3. By checking whether the UART_FR bit[7] is 1, judge whether the UART has finished sending all the data.

----Finish

data reception

Data reception is handled as follows:

In the query mode, when receiving data, check the RX_FIFO status by reading UART_FR[rxfe], according to
The state of RX_FIFO determines whether to read the data in RX_FIFO. In the interrupt
mode, it is determined whether to read the data in RX_FIFO according to the detection of the corresponding interrupt status bit.

14.3.4.4 Data transfer in DMA mode

initialization

The initialization steps are as follows:

1. Write 0 to UART_CR[uarten] to disable UART.
2. Write corresponding configuration values to the UART_IBRD and UART_FBRD registers to configure the transmission rate.
3. Configure UART_CR, UART_LCR_H, and set the corresponding UART working mode.
4. Configure UART_IFLS to set the corresponding transmit and receive FIFO thresholds.
5. If the driver uses the interrupt method, it is necessary to set UART_IMSC to enable the corresponding interrupt signal; use the query method
   The generation of the corresponding interrupt signal should be prohibited during the mode.
6. Write 1 to UART_CR[uarten] to enable UART and complete the initial configuration.

----Finish

data transmission

The steps of data transmission (taking DMA mode as an example) are as follows:

1. Configure the DMA data channel, including data transfer source and destination address, data transfer number, transfer type and other parameters number. For specific configuration, please refer to the related description of "Direct Memory Access Controller".
2. Configure UART_DMACR as 0x2 to enable the DMA transmission function of UART.
3. Through the DMA interrupt report, judge whether the data transmission is completed, and if it is completed, turn off the DMA transmission of UART Function.

----Finish

data reception

Data receiving (taking DMA mode as an example) steps are as follows:

1. Configure the DMA data channel, including data transmission source and destination address, data receiving area address, data transmission Number, transmission type and other parameters.
2. Configure UART_DMACR as 0x1 to enable the DMA receiving function of UART.
3. Through the DMA status query, judge whether the data reception is completed, and if it is completed, close the DMA reception of UART Function.

----Finish

14.3.5 Register overview

Hi3520D provides 4 base addresses of UART units as follows:

The UART0 register base address is 0x2008_0000.

The UART1 register base address is 0x2009_0000.

The UART2 register base address is 0x200A_0000.

The UART3 register base address is 0x200B_0000.

An overview of the UART registers is shown in Table 14-4 .

Table 14-4 UART Register Overview

offset address	name	describe	page number
0x000	UART_DR data register		14-38
0x004	UART_RSR Receive Status Register/Error Clear Register 14-38		
0x008ÿ0x014 RESERVED Reserved			-
0x018	UART_FR Flag Register		14-39
0x01Cÿ0x020 RESERVED Reserved			-
0x024	UART_IBRD Integer Baud Rate Register		14-41
0x028	UART_FBRD Fractional Baud Rate Register		14-41
0x02C	UART_LCR_H line control register		14-42
0x030	UART_CR Control Register		14-43
0x034	UART_IFLS Interrupt FIFO Threshold Select Register		14-45
0x038	UART_IMSC Interrupt Mask Register		14-46
0x03C	UART_RIS Raw Interrupt Status Register		14-47
0x040	UART_MIS Masked Interrupt Status Register		14-48
0x044	UART_ICR Interrupt Clear Register		14-49
0x048	UART_DMACR DMA Control Register		14-50

14.3.6 Register Description

UART_DR

UART_DR is a UART data register, which stores received data and sent data, and can read the receiving status from this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			you are		fe	data							
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[15:12] -		reserved	reserve.
[11] RO		are you	Overflow error. 0: no overflow error; 1: There is an overflow error, the receive FIFO is full and a data has been received.
[10] RO		be	Break Error. 0: no break error; 1: There is a break error, that is, the input of the received data remains low for longer than a full-word transfer (including start, data, parity, and stop bit).
[9] RO		on	Validation error. 0: No check error; 1: Check error.
[8] RO		fe	Framing error. 0: no frame error; 1: Framing error (wrong stop bit).
[7:0] RW	data		Receive data and send data.

UART_RSR

UART_RSR is the receive status register/error clear register.

The register reads as a receive status register. When

the register is written, it acts as an error clear register.

Receive status can also be read from UART_DR . The state information of break, frame, and parity read from UART_DR has higher priority than the information read from UART_RSR (that is, the state changes in UART_DR are faster than UART_RSR).

Any write operation to the UART_RSR register will reset the UART_RSR register.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				are you	be	on	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:4]	reserved	reserve.
[3] RW you		Overflow error. 0: no overflow error; 1: Overflow error. When the FIFO is full, the content in the FIFO remains valid, because there will be no next data written to the FIFO, but the shift register will overflow. The CPU must immediately read the data to empty the FIFO.
[2] RW be		Break Error. 0: no break error; 1: break error. Condition of Break: The input to receive data remains low for longer than a full word transfer (start, data, parity, stop bit are defined).
[1] RW or		Validation error. 0: No parity error; 1: The checksum of received data is wrong. In FIFO mode, this error is associated with the data at the top of the FIFO.
[0] RW fe		Framing error. 0: No frame error; 1: The stop bit of the received data is wrong (valid stop bit is 1).

UART_FR

UART_FR is the UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12 11	10 9	8	7	6	5	4	3	2	1	0
Name	reserved						txfe	rxff	txff	rxfe	busy	reserved		
Reset 0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved.
[7]	RO	txfe	The meaning of this bit is determined by the state of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is 1 when the sending holding register is empty; if UART_LCR_H[fen] is 1, this bit is 1 when the sending FIFO is empty.
[6]	RO	rxff	The meaning of this bit is determined by the state of UART_LCR_H[FEN]. If UART_LCR_H[fen] is 0, this bit is 1 when the receiving holding register is full; if UART_LCR_H[fen] is 1, this bit is 1 when the receiving FIFO is full.
[5]	RO	txff	The meaning of this bit is determined by the state of UART_LCR_H[FEN]. If UART_LCR_H[fen] is 0, this bit is 1 when the sending holding register is full; if UART_LCR_H[fen] is 1, this bit is 1 when the sending FIFO is full.
[4]	RO	rxfe	The meaning of this bit is determined by the state of UART_LCR_H[FEN]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the receiving holding register is empty; if UART_LCR_H[fen] is 1, this bit is set to 1 when the receiving FIFO is empty.
[3]	RO	busy	UART busy status bit. 0: UART is idle or finished sending data; 1: UART is busy sending data. Once this bit is set, it remains in this state until the entire byte (including all stop bits) has been completely sent out of the shift register. This bit is set whenever the transmit FIFO is not empty, regardless of whether the UART is enabled or not.
[2:0]	-	reserved	Reserved.

UART_IBRD

UART_IBRD is an integer baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud became															
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[15:0]	RW	baud divint	Integer baud rate divider value. All cleared to 0 at reset.

UART_FBRD

UART_FBRD is the fractional baud rate register.

注意

The value of the integer baud rate register and the fractional baud rate register must wait until the current data is sent and received

before being updated. The minimum division value is 1, and the maximum division value is 65535 (216–1). That is, UART_IBRD=0 is invalid, and UART_FBRD will be ignored at this time. Similarly, if UART_IBRD=65535 (0xFFFF), UART_FBRD can only be 0, if it is greater than 0, it will cause the failure of sending and receiving.

Suppose UART_FBRD=0x1E, UART_IBRD=0x01, which means that the integer part of the frequency division coefficient is 30, the fractional part is 0.015625, and the entire frequency division coefficient is 30.015625.

UART baud rate = internal bus frequency / (16 x frequency division factor) = internal bus frequency / (16 x 30.015625).

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:6]	-	reserved	reserve.
[5:0]	RW	baud divfrac	Fractional baud rate divider value. All cleared to 0 at reset.

UART_LCR_H

UART_LCR_H is the transmission mode control register, and UART_LCR_H, UART_IBRD, and UART_FBRD form a 30bit wide register. If updating the contents of UART_IBRD and UART_FBRD , UART_LCR_H must be updated at the same time .

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12 11 10 9	8	7	6	5	4	3	2	1	0
Name	reserved					sps	wlen		fen	stp2	eps	pen	brk
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	reserve.
[7]	RW	sps	Check selection. When bit[1], bit[2], bit[7] of this register are set, the parity bit will be sent and detected as 0; when bit[1], bit[7] of this register are set , when bit[2] is 0, the parity bit will be sent and detected as 1. When bit[1], bit[2] and bit[7] are all cleared to 0, stick parity is disabled.
[6:5]	RW	wlen	Indicates the number of data bits sent and received in a frame. 00ÿ5bitÿ 01ÿ6bitÿ 10ÿ7bitÿ 11ÿ8bitÿ
[4]	RW	fen	Transmit and receive FIFO enable control. 0: Transmit and receive FIFO disabled; 1: Transmit and receive FIFO enabled.
[3]	RW	stp2	2-bit stop bit judgment at the end of the sent frame. 0: There is no 2-bit stop bit at the end of the transmitted frame; 1: There is a 2-bit stop bit at the end of the transmitted frame. The receive logic does not check the 2-bit stop bit when receiving.
[2]	RW	eps	Parity selection during transmit and receive. 0: Generate odd parity or check odd parity during sending and receiving; 1: Generate even parity or check even parity during sending and receiving. When UART_LCR_H[fen] is 0, this bit has no effect.

[1] RW pen			Check select bit. 0: No check; 1: Check is generated in the sending direction, and check is performed in the receiving direction.
[0] RW brk			Send a break. 0: Invalid; 1: After sending the current data, UTXD will output low level continuously. Note: To execute the **break** command correctly , software must set this bit to **1** for more than **2** complete frames; in normal use, this bit must be cleared to 0.

UART_CR

UART_CR is the UART control register.

To configure UART_CR follow these steps:

1. Write 0 to UART_CR[uarten] to disable UART.
2. Wait for the current data sending or receiving to end.
3. Clear UART_LCR_H[fen] to 0.
4. Configure UART_CR.
5. Write 1 to UART_CR[uarten] to enable UART.

----Finish

Offset Address: 0x030 | Register Name: UART_CR | Total Reset Value: 0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved	rts	dtr	rxe	txe	lbe	reserved							types
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable. 0: Disable CTS hardware flow control; 1: Enable CTS hardware flow control, only send data when nUARTCTS signal is valid.

[14] RW rtsen			RTS hardware flow control enable. 0: Disable RTS hardware flow control; 1: Enable RTS hardware flow control, request to receive data only when there is space in the receive FIFO.
[13:12] -		reserved	reserve.
[11] RW rts			request to send. This bit is the inversion of UART modem status output signal nUARTRTS. 0: The output signal remains unchanged; 1: That is, if the bit is configured as 1, the output signal is 0.
[10] RW dtr			Data sending preparation. This bit is the inversion of the UART modem status output signal nUARTDTR. 0: The output signal remains unchanged; 1: That is, if the bit is configured as 1, the output signal is 0.
[9] RW rxe			UART receive enable. 0: forbidden; 1: enable. If the UART is disabled during reception, the reception of the current data will end before normal stop.
[8] RW house			UART transmit enable. 0: forbidden; 1: enable. If the UART is disabled during transmission, the current data transmission will end before normal stop.
[7] RW lbe			Loopback enabled. 0: forbidden; 1: UARTTXD output loops back to UARTRXD.
[6:1]		reserved	reserve.
[0] RW uarten			UARTs are enabled. 0: forbidden; 1: enable. If the UART is disabled during transmission and reception, the current data transmission ends before a normal stop.

UART_IFLS

UART_IFLS is the interrupt FIFO threshold selection register, which is used to set the FIFO interrupt (UART_TXINTR or UART_RXINTR) trigger line.

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rxiflsel			txiflsel		
Reset 0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	-	reserved	reserve.
[5:3]	RW	rxiflsel	Threshold selection of receive interrupt FIFO, the trigger point of receive interrupt is as follows. 000: Receive FIFOÿ1/8full; 001: Receive FIFOÿ1/4full; 010: Receive FIFOÿ1/2full; 011: Receive FIFOÿ3/4full; 100: Receive FIFOÿ7/8full; 101ÿ111: Reserved .
[2:0]	RW	txiflsel	Threshold selection of transmit interrupt FIFO, the trigger point of transmit interrupt is as follows. 000: Send FIFOÿ1/8full; 001: Send FIFOÿ1/4full; 011: Transmit FIFOÿ3/4full; 010: Transmit FIFOÿ1/2full; 100: send FIFOÿ7/8full; 101~111: Reserved.

UART_IMSC

UART_IMSC is an interrupt mask register, which is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit 15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		oeim	beim	peim	feim	rtim	txim	rxim				reserved
Reset 0	0	0 0 0	0	0	0	0	0	0	0	0	0	0	0 0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RW	oeim	Mask status of the overflow error interrupt. 0: mask the interrupt; 1: do not mask the interrupt.
[9]	RW	at	break Mask state of error interrupt. 0: Mask the interrupt; 1: Do not mask the interrupt.
[8]	RW	peim	Verify the masking status of interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[7]	RW	feim	Mask status of the framing error interrupt. 0: Mask the interrupt; 1: Do not mask the interrupt.
[6]	RW	rtim	Mask status of receive timeout interrupt. 0: Mask the interrupt; 1: Do not mask the interrupt.
[5]	RW	guilty	Mask status for transmit interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[4]	RW	rxim	Mask status of receive interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[3:0]	-	reserved	Reserved.

UART_RIS

UART_RIS is the raw interrupt status register and its content is not affected by the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0002

Bit 15	14	13 12 11 10	9	8	7	6	5	4	3	2	1	0
Name	reserved		oeris	beris	peris	feris	rtris	txris	rxris			reserved
Reset 0	0	0 0 0 0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	reserve.
[10]	RO	oeris	Raw overflow error interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[9]	RO	beris	Raw break Error break state. 0: Interrupt not generated; 1: Interrupt generated.
[8]	RO	peris	Raw parity interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[7]	RO		Raw error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[6]	RO	rtris	Raw receive timeout interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[5]	RO	txris	Raw send interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[4]	RO	rxris	Raw receive interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[3:0]	-	reserved	reserve.

UART_MIS

UART_MIS is the masked interrupt status register, and its content is the result of the "AND" operation between the original interrupt status and the interrupt mask.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13 12 11 10	9	8	7	6	5	4	3 2 1	0
Name	reserved			oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved
Reset 0	0	0	0 0	0	0	0	0	0	0	0 0 0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RO	oemis	Masked overflow error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[9]	RO	bemis	Masked break Error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[8]	RO	pemis	Masked verification interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[7]	RO	femis	Masked error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[6]	RO	rtmis	Masked receive timeout interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[5]	RO	txmis	Masked transmit interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[4]	RO	rxmis	Masked receive interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[3:0]	-	reserved	Reserved.

UART_ICR

UART_ICR is an interrupt clear register, when writing 1, the corresponding interrupt is cleared, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						oeic	beic	peic	see	rtic	txic	rxic			reserved
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	WO	oec	Clear overflow error interrupt. 0: invalid; 1: Clear interrupt.
[9]	WO	bicycle	Clear break Error interrupt. 0: invalid; 1: Clear interrupt.
[8]	WO	pic	Clear verify interrupt. 0: invalid; 1: Clear interrupt.
[7]	WO	feic	Clear the error interrupt. 0: invalid; 1: Clear interrupt.
[6]	WO	rtic	Clear receive timeout interrupt. 0: invalid; 1: clear interrupt.
[5]	WO	txic	Clear transmit interrupt. 0: invalid; 1: Clear interrupt.
[4]	WO	rxic	Clear receive interrupt. 0: invalid; 1: Clear interrupt.
[3:0]	-	reserved	Reserved.

UART_DMACR

UART_DMACR is the DMA control register, which is used to configure the DMA enable of transmit FIFO and receive FIFO.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	-	reserved	Reserved.
[2]	RW	dmaonerr	Receive channel DMA enable control when UART error interrupt (UARTEINTR) occurs. 0: When the UART error interrupt (UARTEINTR) is valid, the request output of the receiving channel DMA (UARTRXDMASREQ or UARRTXDMABREQ) is valid; 1: When the UART error interrupt (UARTEINTR) is valid, the request output of the receiving channel DMA (UARTRXDMASREQ or UARRTXDMABREQ) is invalid.
[1]	RW	txdmae	DMA enable control for transmit FIFO. 0: forbidden; 1: enable.
[0]	RW	rxdmae	DMA enable control for receive FIFO. 0: forbidden; 1: enable.

14.4 Infrared interface

14.4.1 Overview

The infrared remote control receiving unit IR (Infrared Remoter) receives infrared data through the infrared interface.

14.4.2 Features

The IR module has the following features:

- The software can be configured to close the infrared
  remote control receiver
  module. Supports 2 working modes: ÿMode 0: supports decoding of four data formats of NEC with simple repeat code, NEC with full repeat code, SONY and TC9012, and functions such as receiving data error detection and infrared remote control wake-up.

ÿMode 1: Support symbol level width detection in any data format. In mode 0, it supports received data frame overflow interrupt, received data frame format error interrupt, received data frame interrupt, button release interrupt, and combined interrupts composed of various interrupts.

In mode 1, it supports received symbol overflow interrupt, received symbol interrupt, symbol timeout interrupt, and combined interrupts composed of various interrupts.

Supports initial interrupt status query and masked interrupt status query.

Interrupt clear and mask (write clear) are supported.

Support infrared remote control wake-up.

Support reference clock frequency 1MHzÿ128MHz optional, software programmable control frequency division factor to prescale the working clock to 1MHz.

14.4.3 Functional Description

When the IR module receives the infrared signal emitted by the infrared remote control, it decodes it and sends it to the ARM system. The ARM system performs corresponding operations according to the received codes to realize the expected functions. The IR module is connected to the APB bus in the ARM subsystem. When the chip is in a low power consumption state (the CPU is in low frequency mode), the IR module will generate an interrupt signal to the CPU after receiving a complete frame of data to realize infrared remote control. Wake up function.

By analyzing the signals sent by various infrared remote controllers, it is found that in the infrared commands sent by different remote controllers, the guide codes are different, and the subsequent control commands are also quite different, even the digits of the command codes are different. , this is because the design of these infrared remote controls does not follow the unified infrared remote control standard. Although the standards followed are different, the basic coding ideas are the same, and pulses with different periods and different duty cycles are used to represent 0 and 1 respectively. The duty cycle of different remote controllers may be different, and the pulse period is also different. According to these differences, some infrared data with similar code types are classified: NEC with simple repeat code data format, NEC with full repeat code data format, TC9012 data format and SONY data format.

Table 14-5 to Table 14-7 show the statistics of infrared received data code patterns .

Table 14-5 Statistical Table of Infrared Received Data Patterns (NEC with simple repeat code)

Data Format		NEC with simple repeat code			
		uPD6121G D6121/BU5777/D1913 LC7461M-C13 AEHA			
Lead code (10ÿs) LEAD_S		900	900	900	337.6
	LEAD_E	450	450	450	168.8
bit0ÿ10ÿsÿ	B0_L	56	56	56	42.2
	B0_FUL	56	56	56	42.2
bit1ÿ10ÿsÿ	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
simple repeat code ÿ10ÿsÿ	SLEAD_S 900		900	900	337.6
	SLEAD_E 225		225	225	337.6
burstÿ10ÿsÿ		55	55	55	42.2

Data Format	NEC with simple repeat code			
	uPD6121G D6121/BU5777/D1913 LC7461M-C13 AEHA			
Frame length (10ÿs)	10800	10800	10800	8777.6ÿ 12828.8
valid data bits	32	32	42	48

Table 14-6 Statistical Table of Infrared Received Data Patterns (NEC with full repeat code)

Data Format		NEC with full repeat code						
		uPD6121G LC7461	M-C13	MN602 4-C5D6	MN6014 -C6D6	MATNEW MN6030 LORD		SONIC
boot code ÿ10ÿsÿ	LEAD_S 900		900	337.6	349.2	348.8	349	352
	LEAD_E 450		450	337.6	349.2	374.4	349	352
bit0 ÿ10ÿsÿ	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_FUL	56	56	84.4	87.3	43.6	87.3	88
bit1 ÿ10ÿsÿ	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
simple repeat code ÿ10ÿsÿ	SLEAD_S None		no no no			none	none	none
	SLEAD_E							
burstÿ10ÿsÿ		55	55	84.4	87.3	43.6	87.3	88
Frame length (10ÿs)		10800	10800	10130	10470	12413.6ÿ 16594.4	10500	10400
valid data bits		32	42	22	24	48	22	22

Table 14-7 Statistical table of infrared received data code types (TC9012 and SONY codes)

Data Format		TC9012	SONY			
		TC9012F/9243 SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13	
boot code ÿ10ÿsÿ	LEAD_S 450		240	240	240	240
	LEAD_E 450		60	60	60	60
bit0 ÿ10ÿsÿ	B0_L	56	60	60	60	60
	B0_FUL	56	60	60	60	60

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
bit1 ÿ10ÿsÿ	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
simple repeat code ÿ10ÿsÿ	SLEAD_S None		none	none	none	none
	SLEAD_E					
burstÿ10ÿsÿ		56	none	none	none	none
Frame length (10ÿs)		10800	4500	4500	4500	4500
valid data bits		32	12	13	15	20

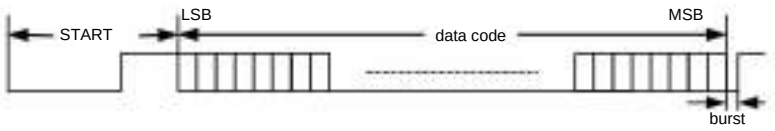
14.4.3.1 NEC with simple repeat code data format

frame format

The data format of NEC with simple repeat code is composed of three parts: START (boot code), data code and burst, among which START is composed of a start code (low level) and an end code (high level); The effective number of digits and the meaning of a certain bit depend on the specific code pattern, which is received in the order of LSB first; the burst signal is used to receive the last data code bit.

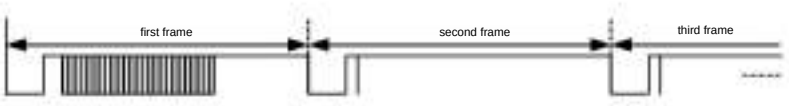
The frame format for sending a single NEC with simple repeat code is shown in Figure 14-19 .

Figure 14-19 Frame format for sending a single NEC with simple repeat code



If the key press lasts longer than one frame, after receiving the complete data frame, the next received data frame only consists of simplified preamble code and burst signal. The boot code is also composed of a start code (low level) and an end code (high level). The frame format of continuously sending the NEC with simple repeat code code is shown in Figure 14-20 .

Figure 14-20 The frame format of continuously sending NEC with simple repeat code by pressing the key



code format

The definition of bit0 or bit1 of NEC with simple repeat code is shown in Figure 14-21 .

Figure 14-21 Definition of bit0 and bit1 of NEC with simple repeat code

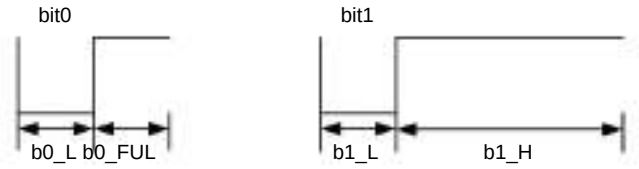


Figure 14-22 and Figure 14-23 show the single-issue code format and continuous-issue code format of NEC simple repeat code respectively .

Figure 14-22 NEC with simple repeat code single-issue code format

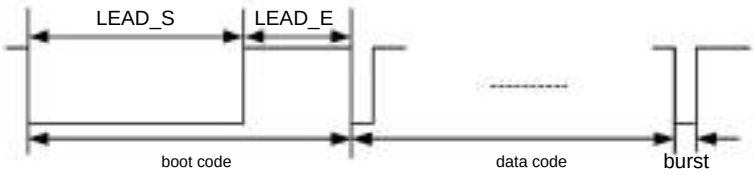
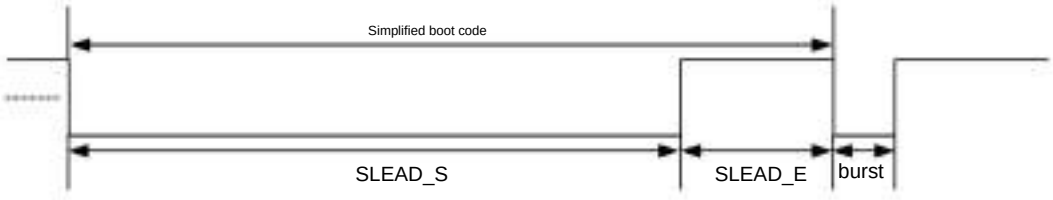


Figure 14-23 NEC with simple repeat code code format



Note 1: The width of the high and low level pulse width and the frame length in the figure are determined by each specific code pattern, please refer to Table 14-5~Table 14-7. Note

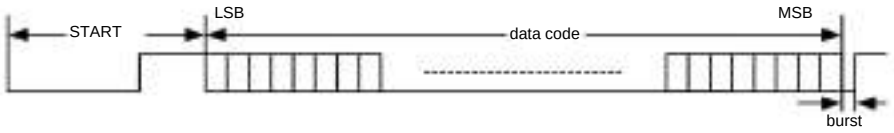
2: The frame length cannot be greater than 160ms, otherwise the simplified boot code cannot be recognized.

14.4.3.2 NEC with full repeat code data format

frame format

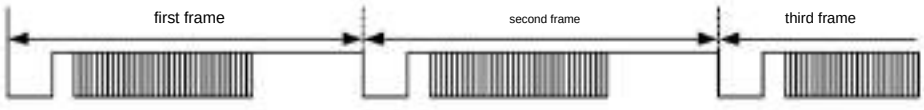
The data format of NEC with full repeat code is composed of three parts: START (boot code), data code and burst. START is composed of a start code (low level) and an end code (high level); the effective number of digits of the data code and the meaning of a certain bit are determined by the specific code pattern, which is in the order of LSB first Received; the burst signal is used to receive the last data bit. The frame format for sending a single NEC with full repeat code is shown in Figure 14-24 .

Figure 14-24 Frame format for sending a single NEC with full repeat code



If the key press lasts for more than one frame, after receiving the complete data frame (the first frame), the next received data frame is still a complete data frame format (that is, the first frame of data is sent repeatedly according to the frame interval) , keep pressing the key to continuously send the NEC with full repeat code frame format as shown in Figure 14-25 .

Figure 14-25 The frame format of continuously sending NEC with full repeat code by pressing the button continuously

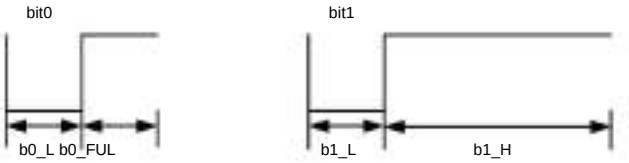


From Figure 14-24 and Figure 14-25, it can be seen that the only difference between NEC with simple repeat code and NEC with full repeat code is the format of the repeated frame. NEC with simple repeat code sends a simplified boot code, while NEC With full repeat code sends the full frame format, the first frame is exactly the same as the repeated frame.

code format

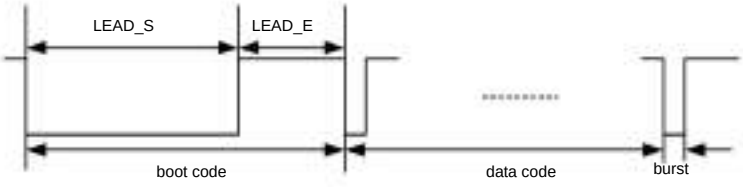
The definition of bit0 or bit1 of NEC with full repeat code is shown in Figure 14-26 .

Figure 14-26 Definition of bit0 and bit1 of NEC with full repeat code



The single-issue code format of NEC with full repeat code is shown in Figure 14-27 .

Figure 14-27 NEC with full repeat code single-issue code format



Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern, please refer to Table 14-5 to Table 14-7.

14.4.3.3 TC9012 Data Format

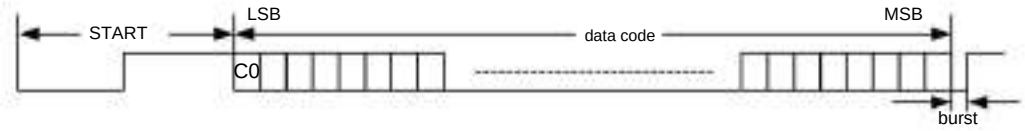
frame format

注意

According to the data format characteristics of TC9012 code, the first bit of all key codes must be all 1 or all 0, otherwise unnecessary continuous key frames will be generated.

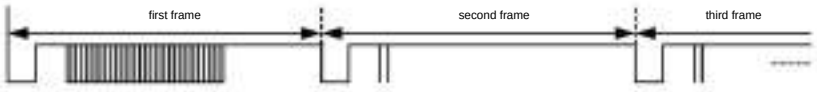
The data format of TC9012 is composed of three parts: START (boot code), data code and burst, among which START is composed of a start code (low level) and an end code (high level); the effective number of data codes And the meaning of a certain bit depends on the specific code pattern, which is received in the order of LSB first; the burst signal is used to receive the last data code bit. The frame format for sending a single TC9012 code is shown in Figure 14-28 .

Figure 14-28 Frame format for sending a single TC9012 code



If the pressing time lasts longer than one frame, after receiving the complete data frame, the next received data frame consists of three parts: the pilot code, a data bit and the burst signal. The leading code is also composed of a start code (low level) and an end code (high level); this data bit is the inverse code of the first data bit (C0) received in the previous frame. The frame format for sending continuous TC9012 codes is shown in Figure 14-29 .

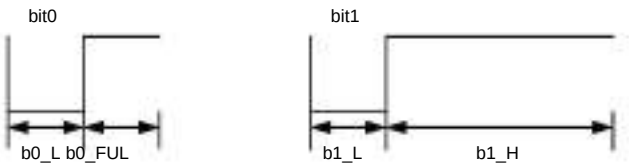
Figure 14-29 The frame format of continuously sending TC9012 codes by continuously pressing the key



code format

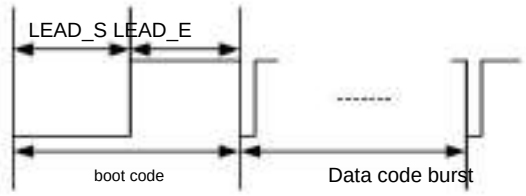
The definition of TC9012 code bit0 or bit1 is shown in Figure 14-30 .

Figure 14-30 Definition of bit0 and bit1 of TC9012 code



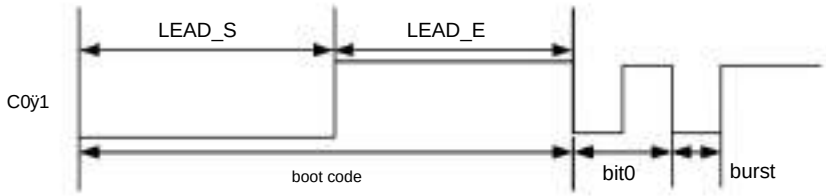
The single-issue code format of TC9012 code is shown in Figure 14-31 .

Figure 14-31 TC9012 single-issue code format



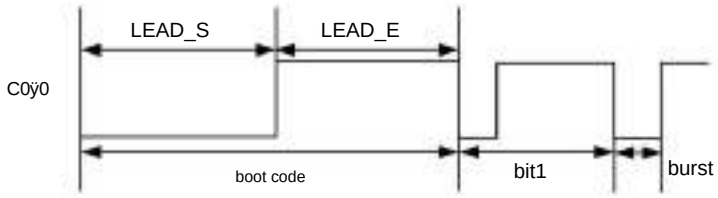
When C0=1, the TC9012 code burst code format is shown in Figure 14-32 .

Figure 14-32 TC9012 code format for continuous sending (C0ÿ1)



When C0=0, the code format of TC9012 code burst is shown in Figure 14-33 .

Figure 14-33 TC9012 code format for continuous sending (C0ÿ0)



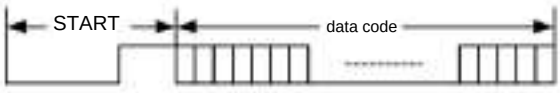
Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern. Please refer to Table 14-5 to Table 14-7. It is also worth noting that the frame length cannot be greater than 160ms, otherwise repeated frames cannot be identified.

14.4.3.4 SONY data format

frame format

The SONY code data format is composed of two parts: START (boot code) and data code. Among them, START is composed of a start code (low level) and an end code (high level); the effective number of digits of the data code and the meaning of a certain bit are determined by the specific code pattern, which is in the order of LSB first Received. The format of sending a single SONY code frame is shown in Figure 14-34 .

Figure 14-34 Send a single SONY frame format



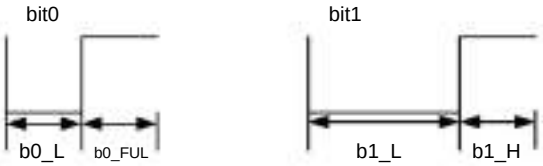
If the pressing time lasts longer than one frame, after receiving the complete data frame, the next received data frame is still in a complete data frame format. Press and hold the key to continuously send the SONY code frame format as shown in Figure 14-35 .

Figure 14-35 Continue to send SONY code frame format continuously by pressing the key

code format

The definition of SONY code bit0 or bit1 is shown in Figure 14-36 .

Figure 14-36 Definition of bit0 and bit1



Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern. Please refer to Table 14-5 to Table 14-7.

14.4.4 Working method

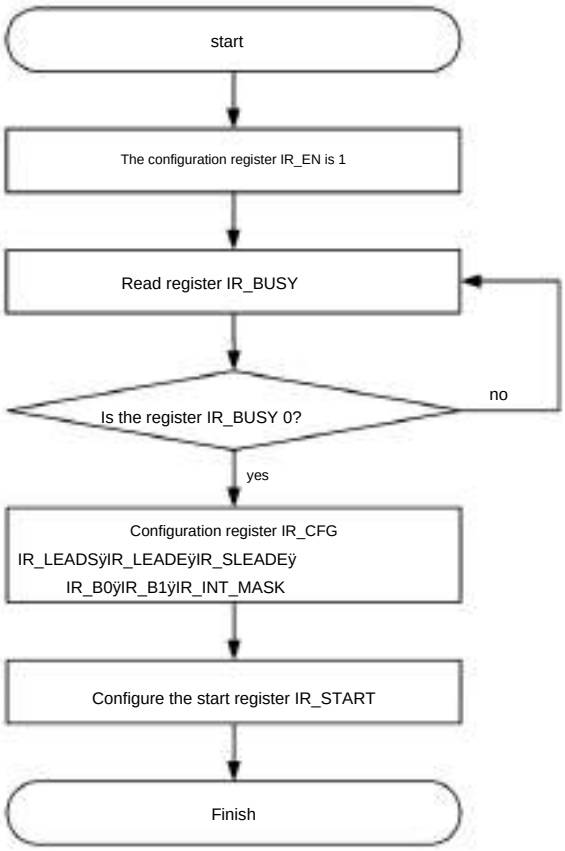
soft reset

Configure the CRG register CRG_PERCTRL57[ir_srst_req] as 1, and soft reset the IR module separately. After reset, the values of each configuration register are reset to default values, so these registers need to be initialized and configured again after reset.

Register Configuration Example

Figure 14-37 shows the operation flow of IR module initialization .

Figure 14-37 IR module initialization operation flow



The IR module initialization operation flow is as follows:

1. Select the IR module address space and start the IR initialization configuration operation.

2. Set IR_EN bit[0] to 1 to enable the IR receiving module.

3. Read IR_BUSY to determine the current status of the IR module configuration.

   If the read value is 1, it means that the IR module is in the configuration busy state, then continue to query IR_BUSY (note : the software should not configure other control registers of the **IR** module at this time, otherwise the configuration will be invalid).

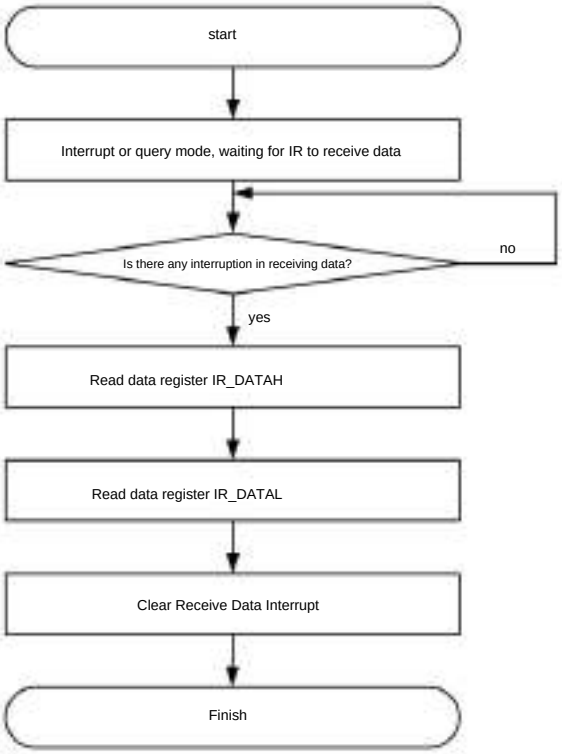
   If the read value is 0, it means that the IR module is in the configured idle state, then go to 4.

4. ConfigurationIR_CFG ÿIR_LEADSÿIR_LEADEÿIR_SLEADEÿIR_B0ÿIR_B1ÿ
   IR_INT_MASK. Note: Users can update the corresponding registers as needed, if not, the registers will keep the original value.

5. Configure IR_START. You must wait for all the IR control registers to be configured before configuring
   IR_START, because it is used to generate a start signal, as long as it is configured, the IR module will receive infrared data according to the value of the control register.

   ----Finish

Figure 14-38 Operation flow of reading decoded data



The operation flow of reading decoded data is as follows:

1. Check the IR module address space.
2. Wait for receiving data frames in interrupt or query mode.

   In the interrupt mode, when the CPU receives the interrupt request signal from the IR module, query the value of IR_INT_STATUS[intms_rcv]. If the read value is 1, it means that the IR module has received a data frame, execute 3; if the read value is 0, execute 2 again, and continue to wait for the interrupt. In the query mode, the software reads the value of IR_INT_STATUS[intrs_rcv] continuously (or at regular intervals) . If the read value is 1, it means that the IR module has received a data frame, and execute 3; if the read value is 0, , indicating that the IR module has not received the data frame, re-execute 2, and continue to query.
3. Read the data register IR_DATAH. (If the number of data bits in a frame is not greater than 32 bits, this step can be omitted step)
4. Read the data register IR_DATAL.
5. Clear the receive data interrupt.

----Finish

14.4.5 Register Overview

An overview of the IR registers is shown in Table 14-8 .

Table 14-8 IR register overview (base address is 0x2007_0000)

offset address	name	describe	page number
0x000	GO	IR Receive Enable Control Register	14-62
0x004	IR_CFG	IR configuration register	14-62
0x008	IR_LEADS	Boot code start bit margin configuration register	14-64
0x00C	IR_LEADE	Boot code end bit margin configuration register	14-65
0x010	AND_SLEADE	Simplified Preamble End Bit Margin Configuration Register 14-66	
0x014	IR_B0	Data 0 Judgment Level Margin Configuration Register 14-67	
0x018	IR_B1	Data 1 Judgment Level Margin Configuration Register 14-68	
0x01C	AND_BUSY	Configure Busy Flag Register	14-69
0x020	IR_DATAH	IR Receives high 16-bit register of decoded data (when IR_CFG[ir_mode]=0) or symbol number register in symbol FIFO (when When IR_CFG[ir_mode]=1)	14-70
0x024	IR_DATAL	IR Receives the low 32-bit register of decoded data (when IR_CFG[ir_mode]=0) or the symbol width register received by the IR module (when When IR_CFG[ir_mode]=1)	14-70
0x028	IR_INT_MASK	IR Interrupt Mask Register	14-71
0x02C	IR_INT_STATUS	IR Interrupt Status Register	14-73
0x030	IR_INT_CLR	IR Interrupt Clear Register	14-75
0x034	IS_START	IR Boot Configuration Register	14-77

14.4.6 Register Description

GO

IR_EN is the IR receive enable control register.

The software must configure the register IR_EN[ir_en]=1 before configuring other registers, otherwise the configuration is invalid.

When the register IR_EN[ir_en]=0, other registers can only be read but not written, and the read value is the reset value of the register.

Offset Address	Register Name	Total Reset Value
0x000	GO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	go
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access Name		Description
[31:1]		reserved	reserve.
[0] RW go_in			Enable of the IR receiver module. 0: Turn off the IR receiving module; 1: Turn on the IR receiving module.

IR_CFG

IR_CFG is the IR configuration register.

注意

This register must be configured when IR_BUSY[ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value.

The reference clock frequency supported by IR is 1MHz~128MHz, and its corresponding relationship with the frequency division factor ir_freq is:

When the reference clock frequency is 1MHz, the frequency division factor ir_freq needs to be configured as 0x00. When the reference clock frequency is 128MHz, the frequency division factor ir_freq needs to be configured as 0x7F.

When the IR reference clock is a non-integer multiple frequency within 1MHz ~ 128MHz, choose the corresponding frequency division factor by rounding off. Example: The reference clock is 12.1MHz, and the selected frequency division factor is 0x0B; the reference clock is 12.8MHz, the selected frequency division factor is 0x0C.

For the relationship between frequency deviation and counting deviation: base frequency f, frequency change Df, then frequency deviation ratio=Df/f; counter counting Deviation Dcnt; judging level width s (ÿs as unit), then counting deviation: $Dcnt = ÿ\ ÿ\ 0.1\times s \times ratio$. Therefore, when there is a frequency offset, the effective range of the parameter value must be shifted. If the frequency increases, the corresponding margin value should be changed to: [min+Dcnt, max+Dcnt], where min and max are no offset When the margin value; if the frequency drops, the corresponding margin value should be changed to: [min-Dcnt, max-Dcnt]. Take the starting bit margin of the pilot code as an example: If the base frequency is 100MHz, and the frequency drifts up by 0.1MHz, then ratio=0.1/100=0.001, and s=9000ÿs, then Dcnt = ÿ0.1× *9000* × 0.001ÿ = 1, the margin value of ir_leads should be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	ir_max_level_width	is_format / ir_bits	is_fashion / ir_freq
Reset	0 0 1 1 1 1 0 1 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1	0 0 0 1 0 1 1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	When IR_CFG[ir_mode]=0, it is invalid; When IR_CFG[ir_mode]=1, it indicates the maximum level width of symbol (unit 10ÿs), which is used to determine the end of a symbol stream.
[15:14]	RW	ir_format	When IR_CFG[ir_mode]=0, it means data pattern. 00: NEC with simple repeat code data format; 01: TC9012 data format; 10: NEC with full repeat code data format; 11: SONY data format. Please refer to Table 14-5 to Table 14-7 for details about which code family the specific code pattern belongs to . When IR_CFG[ir_mode]=1, it means symbol format. bit[15]: Reserved; the meaning of bit[14] is as follows: 0: The format of the symbol is low first and then high, and the symbol stream ends at high level; 1: The format of the symbol is high first and then low, and the symbol stream ends at low level.
[13:8]	RW	ir_bits	When IR_CFG[ir_mode]=0, it indicates the number of data bits in one frame. 0x00ÿ0x2F: correspond to 1ÿ48 data bits in one frame respectively; 0x30~0x3F: Reserved. If the software configures this field with a value in the range of 0x30~0x3F, the configuration will be invalid, and the original value of ir_bits will remain unchanged. When IR_CFG[ir_mode]=1, it means the interrupt watermark of symbol is received. bit[13]: Reserved; bit[12:8]: 0x0~0x1F: corresponding to at least 1~32 symbols in the FIFO reporting interrupt.
[7]	RW	ir_mode	IR working mode. 0: Output the complete data frame after decoding; 1: Only output the symbol width.
[6:0]	RW	ir_freq	Working clock frequency division factor. 0x00~0x7F correspond to the working clock frequency division factor 1~128 respectively.

IR_LEADS

IR_LEADS is the boot code start bit margin configuration register (only used when IR_CFG[ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

In order to accurately judge the start bit of the leading code, a certain margin needs to be considered around the typical value of the specific code type. For the typical value of the specific code type, please refer to the value of LEAD_S in Table 14-5 to Table 14-7 .

For pulse widths with a typical value not less than 400 (its accuracy is 10ÿs), it is recommended that the margin range be set to 8% of the typical value. For example: D6121 pattern, the typical value of LEAD_S is 900, then the corresponding cnt_leads_min=900 x 92%=828=0x33C, cnt_leads_max=900 x 108%=972=0x3CC. For pulse widths with a typical value less than 400 (with an accuracy of 10 ÿs), it is recommended that the margin range be set to 20% of the typical value. For example: SONY-D7C5 pattern, its typical value of LEAD_S is 240, then the corresponding cnt_leads_min=240 x 80%=192=0xC0, cnt_leads_max=240 x 120%=288=0x120.

Basic configuration principle: cnt_leads_max is not less than cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	cnt_leads_min	reserved	cnt_leads_max
Reset	0 0 0 0 0 0 1 1	0 0 1 1	0 0 0 0 0 0	0 0 1 1

Bits	Access	Name	Description
[31:26]	-	reserved	reserve.
[25:16]	RW	cnt_leads_min	The minimum pulse width of the start bit of the boot code. 0x000~0x007: Reserved.
[15:10]	-	reserved	reserve.
[9:0]	RW	cnt_leads_max	The maximum pulse width of the start bit of the boot code. 0x000~0x007: Reserved.

IR_LEADE

IR_LEADE is the configuration register for the end bit margin of the boot code (only used when IR_CFG[ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged. For the code family of NEC with simple repeat code, the margin range of cnt_sleade and the margin range setting of cnt_leade cannot overlap. Otherwise, when the actual count value falls within the coincident range, the simplified guide code cannot be recognized, which will cause a frame format error.

In order to accurately judge the end bit of the pilot code, it is necessary to consider a certain margin around the typical value of the specific code pattern, and the margin range is about 8% of the typical value. For the typical values of specific code types, see the values of LEAD_E in Table 14-5 to Table 14-7 .

For a pulse width with a typical value not less than 400 (its accuracy is 10ÿs), it is recommended that the margin range be set at 8% of the typical value. For example: D6121 pattern, the typical value of LEAD_E is 450, then the corresponding cnt_leade_min=450 x 92%=414=0x19E, cnt_leade_max=450 x 108%=486=0x1E6. For pulse widths with a typical value less than 400 (with an accuracy of 10 ÿs), it is recommended that the margin range be set to 20% of the typical value. For example: SONY-D7C5 pattern, its typical value of LEAD_E is 60, then the corresponding cnt_leade_min=60 x 80%=48=0x030, cnt_leade_max=60 x 120%=72=0x048.

The basic configuration principle is: cnt_leade_max is not less than the value of cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt_leade_min	reserved	cnt_leade_max
Reset	0 0 0 0 0 0 0 1	1 0 0	0 0 0 0 0 1 1 1	1 0 0 1 1 0

Bits	Access	Name	Description
[31:25]	-	reserved	reserve.
[24:16]	RW	cnt_leade_min	The minimum pulse width of the boot code end bit. 0x000~0x007: Reserved.
[15:9]	-	reserved	reserve.
[8:0]	RW	cnt_leade_max	The maximum pulse width of the end bit of the boot code. 0x000~0x007: Reserved.

AND_SLEADE

IR_SLEADE is the configuration register for the end bit margin of the simplified boot code (only used when IR_CFG[ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged. For the code family of NEC with simple repeat code, the margin range of cnt_sleade and the margin range setting of cnt_leade cannot overlap, otherwise when the actual count value falls within the coincident range, the simplified guide code cannot be recognized and the frame

format error will result. For the data format of NEC with simple repeat code, this register needs to be configured; for other formats, this register does not need to be configured.

In order to accurately judge the end bit of the simplified pilot code, it is necessary to consider a certain margin around the typical value of the specific code pattern. For the typical values of specific code types, please refer to the values of SLEAD_E in Table 14-5 to Table 14-7 .

For pulse widths with a typical value not less than 225 (its accuracy is 10ÿs), it is recommended that the margin range be set to 8% of the typical value. For example: D6121 pattern, the typical value of SLEAD_E is 225, then the corresponding cnt_sleade_min=225 x 92%=207=0xCF, cnt_sleade_max=225ÿ x 108%=243=0xF3. For pulse widths with a typical value less than 225 (its accuracy is 10ÿs), it is recommended that the margin range be set to 20% of the typical value. For example: For example, the typical value of SLEAD_E of a certain pattern is 60, then the corresponding cnt_sleade_min=60ÿ x 80%ÿ48ÿ0x30, cnt_sleade_max=60ÿ x 120%=72=0x48.

The basic configuration principle is: cnt_sleade_max is not less than the value of cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	AND_SLEADE	0x00CF_00F3

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt_sleade_min	reserved	cnt_sleade_max
Reset	0 0 0 0 0 0 0 1	1 0 0 1 1	1	0 0 0 0 0 0 0 0 1 1 1 1 0 0 1 1

Bits	Access	Name	Description
[31:25]	-	reserved	reserve.
[24:16]	RW	cnt_sleade_min	The minimum pulse width of the end bit of simplified preamble code. 0x000~0x007: Reserved.
[15:9]	-	reserved	reserve.
[8:0]	RW	cnt_sleade_max	Simplifies the maximum pulse width of the start bit of the preamble. 0x000~0x007: Reserved.

IR_B0

IR_B0 is the judgment level margin configuration register for data 0 (only used when IR_CFG[ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

For the four code types, the bit0 judgment level margin range and the bit1 judgment level range setting cannot overlap, otherwise when the actual count value falls within the overlapping range, bit1 cannot be recognized and bit0 can only be misunderstood.

In order to accurately judge bit0, it is necessary to consider a certain margin around the typical value of the specific pattern, and the margin range is about 20% of the typical value.

For the three code types of NEC with simple repeat code, NEC with full repeat code and TC9012, please refer to the value of B0_H in Table 14-5 to Table 14-7 for the typical values of the specific code types included. For example: D6121 pattern, the typical value of B0_H is 56 (its precision is 10ÿs), then the corresponding cnt0_b_min=56 x 80%=45=0x2D, cnt0_b_max=56 x 120%=67=0x43. For the SONY data format, please refer to the value of B0_L in Table 14-5 to Table 14-7 for the typical values of the specific code patterns it contains. For example: SONY-D7C5 pattern, the typical value of B0_L is 60 (its precision is 10ÿs), then the corresponding cnt0_b_min=60 x 80%=48=0x30, cnt0_b_max=60 x 120%=72=0x48.

The basic configuration principle is: cnt0_b_max is not less than the value of cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt0_b_min								reserved						cnt0_b_max	
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	reserve.
[24:16]	RW	cnt0_b_min	bit0 determines the minimum pulse width of the level. 0x000~0x007: Reserved.
[15:9]		reserved	reserve.
[8:0]	RW	cnt0_b_max	bit0 judges the maximum pulse width of the level. 0x000~0x007: Reserved.

IR_B1

IR_B1 is the judgment level margin configuration register for data 1 (only used when IR_CFG[ir_mode]=0).

注意

This register must be configured when IR_BUSY [0]=0 and IR_EN[0]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the configuration of the reserved value of the register is invalid and the original value remains unchanged. For the four code types, the bit0 judgment level margin range and the bit1 judgment level range setting cannot overlap, otherwise when the actual count value falls within the overlapping range, bit1 cannot be recognized and bit0 can only be misunderstood.

In order to accurately judge bit1, a certain margin needs to be considered around the typical value of the specific pattern, and the margin range is about 20% of the typical value.

For the three code families of NEC with simple repeat code, NEC with full repeat code and TC9012, please refer to the values of B1_H in Table 14-5 to Table 14-7 for the typical values of the specific code types included. For example: D6121 pattern, the typical value of B1_H is 169 (its precision is 10ÿs), then the corresponding cnt1_b_min=169ÿ x 80%ÿ 135ÿ0x87, cnt1_b_max=169 x 120%=203=0xCB. For the SONY data format, please refer to the value of B1_L in Table 14-5 to Table 14-7 for the typical values of the specific code patterns it contains. For example: SONY-D7C5 pattern, the typical value of B1_L is 120 (its precision is 10ÿs), then the corresponding cnt1_b_min=120 x 80%=96=0x60, cnt1_b_max=120 x 120%=144=0x90.

The basic configuration principle is: cnt1_b_max is not less than the value of cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt1_b_min	reserved	cnt1_b_max
Reset	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 1	1 0 0 1	0 1 1 1

Bits	Access	Name	Description
[31:25]	-	reserved	reserve.
[24:16]	RW	cnt1_b_min	bit1 The minimum pulse width for judging the level. 0x000~0x007: Reserved.
[15:9]		reserved	reserve.
[8:0]	RW	cnt1_b_max	Bit1 judges the maximum pulse width of the level. 0x000~0x007: Reserved.

AND_BUSY

IR_BUSY is the configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	AND_BUSY	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	and_will be
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access Name		Description
[31:1]		reserved	reserve.
[0]	RO and_busy		Busy flag. 0: idle state, software can configure data; 1: In busy state, the software cannot configure data.

IR_DATAH

IR_DATAH is the high 16-bit register of IR receiving and decoding data (when IR_CFG[ir_mode]=0) or the symbol number register in symbol FIFO (when IR_CFG[ir_mode]=1).

IR_DATAH is the upper 16 bits of the received decoded data , and IR_DATAL is the lower 32 bits of the received decoded data. Which data bits are valid depends on the number of valid data bits contained in one frame of the specific pattern, please refer to the valid data bits in Table 14-5 to Table 14-7 .

Data storage principle: stored in IR_DATAH and IR_DATAL in order from high to low (MSB... LSB), store IR_DATAL first, and then store IR_DATAH, the unused high bits are reserved bits. The order in which the software reads data must be: first read IR_DATAH, then read IR_DATAL.

For the specific meaning of each data bit, the hardware does not make judgments, but is only responsible for receiving all the data bits, and finally the software handles it uniformly.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	is_datah
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:16] -		reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	is_datah
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RO	is_datah	When IR_CFG[ir_mode]=0, it means the upper 16 bits of the received decoded data. When IR_CFG[ir_mode]=1, it indicates the number of symbols in the symbol FIFO. bit[15:6]: reserved; bit[5:0]: the number of symbols in the symbol FIFO.

IR_DATAL

IR_DATAL is the low 32-bit register of the decoded data received by IR (when IR_CFG[ir_mode]=0) or the symbol width register received by the IR module (when IR_CFG[ir_mode]=1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	ir_data	When IR_CFG[ir_mode]=0, it means the low 32-bit data of the received decoded data. When IR_CFG[ir_mode]=1, it indicates the symbol width received by the IR module. The meaning of bit[31:16] is as follows: When the format of symbol is low first and then high, it means the high level width of the received symbol (unit is 10ÿs); when the format of symbol is high first and then low, it means the width of the received symbol The low level width of symbol (unit is 10ÿs). The meaning of bit[15:0] is as follows: When the format of symbol is low first and then high, it indicates the low level width of the received symbol (unit is 10ÿs); when the format of symbol is high first and then low, it indicates the received symbol The high level width of symbol (unit is 10ÿs).

IR_INT_MASK

IR_INT_MASK is the IR interrupt mask register.

注意

This register can only be configured when IR_EN[ir_en]=1 is ensured , otherwise the configuration is invalid and the register keeps the original value. If all interrupts are shielded, the infrared remote control wake-up function cannot be supported.

When IR_CFG[ir_mode]=0, IR_INT_MASK bit[3:0] is valid; when IR_CFG[ir_mode]=1, IR_INT_MASK bit[18:16] is valid.

The interrupts involved are defined as follows:

Receive data overflow interrupt

If the CPU does not respond in time to take away the data of the current frame and the data of the next frame has been received, the data of the next frame will overwrite the data of the current frame, and at the same time, an interrupt request for receiving data overflow error before masking will be reported. Receive data frame format error interrupt

If the received data frame is incomplete and the data pulse width does not meet the margin range, the received frame format error interrupt request before masking will be reported.

Data frame received interrupt

When a complete frame of data is received, it will report a data frame interrupt request received before masking.

Support the detection interrupt of

key release For the data format of NEC with simple repeat code and TC9012 code family, within 160ms after detecting a valid start synchronization code, if the start synchronization code is not detected again, or a non-simplified boot is detected When the code is a valid data frame, it will report the remote control key release interrupt before shielding. For NEC with full repeat code and SONY two code systems do not support key release

interrupt. Receive symbol

overflow interrupt If the CPU does not respond in time to take away the data, resulting in the symbol FIFO being full, but the next symbol has been received, it will report a received symbol

overflow error interrupt

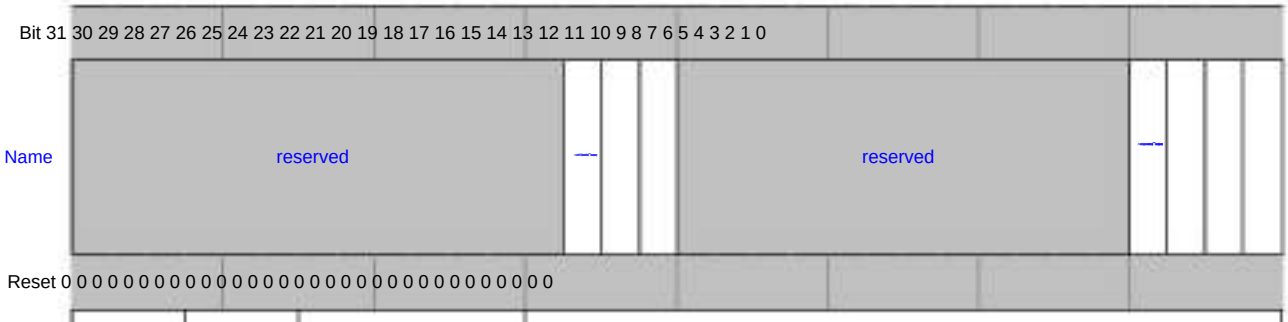
request before masking. Receive symbol interrupt When a complete symbol is received, and the number of symbols in the symbol FIFO exceeds the waterline set by IR_CFG[ir_bits], it will report a

symbol interrupt request

received before masking. Symbol timeout interrupt After receiving a valid symbol , if no new symbol interrupt request is received within the time set by IR_CFG[ir_max_level_width], it will report the symbol timeout interrupt request before masking.

The hardware does not have interrupt priority arbitration, and any one or more masked interrupt sources are valid, and an interrupt will be generated.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000



Bits	Access Name		Description
[31:19]	-	reserved	reserve.
[18]	RW intm_overrun		When IR_CFG[ir_mode]=1, symbol overflow interrupt mask. 0: Not shielded; 1: Shielded.
[17]	RW intm_time_out		When IR_CFG[ir_mode]=1, symbol timeout interrupt mask. 0: no shielding; 1: Shielded.

[16] RW	intm_symb_rcv		When IR_CFG[ir_mode]=1, receive N symbol interrupt mask. 0: no shielding; 1: Shielded.
[15:4]		reserved	reserve.
[3] RW	intm_release		When IR_CFG[ir_mode]=0, key release interrupt mask. 0: no shielding; 1: Shielded.
[2] RW	intm_overflow		When IR_CFG[ir_mode]=0, receive data overflow interrupt mask. 0: no shielding; 1: Shielded.
[1] RW	intm_framerr		When IR_CFG[ir_mode]=0, receive data frame format error interrupt mask. 0: no shielding; 1: Shielded.
[0] RW	intm_rcv		When IR_CFG[ir_mode]=0, received data frame interrupt mask. 0: no shielding; 1: Shielded.

IR_INT_STATUS

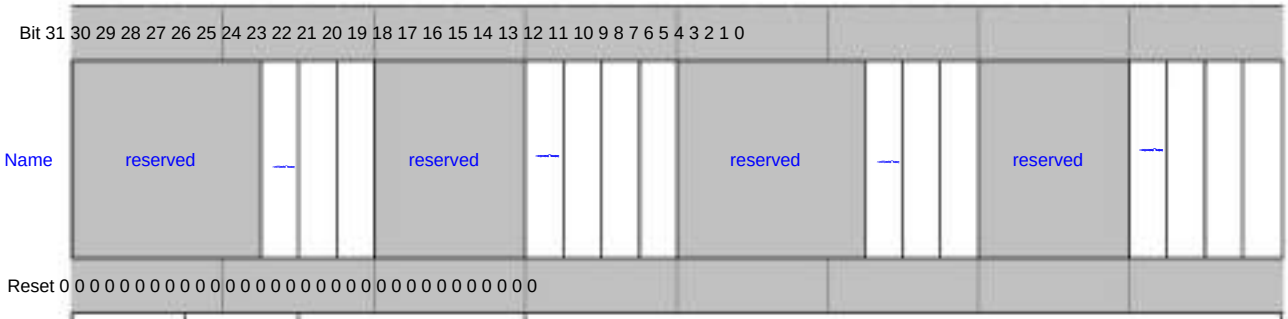
IR_INT_STATUS is the IR interrupt status register.

注意

When IR_CFG[ir_mode]=0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid;

When IR_CFG[ir_mode]=1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000



Bits	Access	Name	Description
[31:27]	-	reserved	reserve.
[26]	RO	intms_overrun	When IR_CFG[ir_mode]=1, the masked symbol overflow interrupt status. 0: no interrupt; 1: There is an interrupt.
[25]	RO	intms_time_out	When IR_CFG[ir_mode]=1, the masked symbol timeout interrupt status. 0: no interrupt; 1: interrupt.
[24]	RO	intms_symb_rcv	When IR_CFG[ir_mode]=1, masked received symbol interrupt status. 0: no interrupt; 1: There is an interrupt.
[23:20]	-	reserved	reserve.
[19]	RO	intms_release	When IR_CFG[ir_mode]=0, the shielded key release interrupt status. 0: no interrupt; 1: There is an interrupt.
[18]	RO	intms_overflow	When IR_CFG[ir_mode]=0, the masked received data overflows the interrupt status. 0: no interrupt; 1: There is an interrupt.
[17]	RO	intms_framerr	When IR_CFG[ir_mode]=0, the masked received data frame format error interrupt status. 0: no interrupt; 1: There is an interrupt.

[16] RO		intms_rcv	When IR_CFG[ir_mode]=0, masked received data frame interrupt status. 0: no interrupt; 1: There is an interrupt.
[15:11] -		reserved	reserve.
[10] RO		intrs_overrun	When IR_CFG[ir_mode]=1, symbol overflow interrupt status before masking. 0: no interrupt; 1: There is an interrupt.
[9]	RO	intrs_time_out	When IR_CFG[ir_mode]=1, the symbol timeout interrupt status before masking. 0: no interrupt; 1: interrupt.
[8]	RO	intrs_symb_rcv	When IR_CFG[ir_mode]=1, the interrupt status of received symbol before masking. 0: no interrupt; 1: interrupt.
[7:4]		reserved	reserve.
[3]	RO	intrs_release	When IR_CFG[ir_mode]=0, the interrupt status of key release before masking. 0: no interrupt; 1: There is an interrupt.
[2]	RO	intrs_overflow	When IR_CFG[ir_mode]=0, the received data before masking overflows the interrupt state. 0: no interrupt; 1: There is an interrupt.
[1]	RO	intrs_framerr	When IR_CFG[ir_mode]=0, the received data frame format error interrupt status before masking. 0: no interrupt; 1: There is an interrupt.
[0]	RO	intrs_rcv	When IR_CFG[ir_mode]=0, the received data frame interrupt status before masking. 0: no interrupt; 1: There is an interrupt.

IR_INT_CLR

IR_INT_CLR is the IR interrupt clear register.

注意

When IR_CFG[ir_mode]=0, IR_INT_CLR bit[3:0] is valid; when IR_CFG[ir_mode]=1, IR_INT_CLR bit[18:16] is valid.

Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:19]	-	reserved	reserve.
[18]	WC intc_overrun		When IR_CFG[ir_mode]=1, clear symbol overflow interrupt request. 0: No effect; 1: Clear.
[17]	WC intc_time_out		When IR_CFG[ir_mode]=1, clear symbol timeout interrupt request. 0: no effect; 1: Clear.
[16]	WC intc_symb_rcv		When IR_CFG[ir_mode]=1, clear the received symbol interrupt request. 0: no effect; 1: Clear.
[15:4]	-	reserved	reserve.
[3]	WC intc_release		When IR_CFG[ir_mode]=0, clear the remote control button release interrupt request. 0: no effect; 1: Clear.
[2]	WC intc_overflow		When IR_CFG[ir_mode]=0, clear the receive data overflow error interrupt request. 0: no effect; 1: Clear.
[1]	WC intc_framerr		When IR_CFG[ir_mode]=0, clear the received data frame format error interrupt request. 0: no effect; 1: Clear.

[0] WC intc_rcv			When IR_CFG[ir_mode]=0, clear the received data frame interrupt request. 0: no effect; 1: Clear. If the software does not read the data in IR_DATAL and directly writes 1 to this bit after receiving the data frame interrupt request , the interrupt request cannot be cleared.

IS_START

IR_START is the IR start configuration register.

After the value configuration of other registers is completed, when starting the IR module, only one write operation to this address (the write operand can be any value) can start the configuration register.

Offset Address	Register Name	Total Reset Value
0x034	IS_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	is_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	reserve.
[0]	WO	ir_start	IR Boot Configuration Register.

14.5 GPIO

14.5.1 Overview

注意

For details on the number of GPIO pins and the multiplexing of pins and other pins, please refer to "02 Hardware". For related controls, please refer to "2.3 Pin Multiplexing Control Register".

For the GPIO multiplexed on the pins that are output signals by default, please note that the pins connected to the chip and device must be output enter.

Hi3520D supports 9 groups of GPIO (General Purpose Input/Output), and each group of GPIO provides 8 programmable input and output pins. Each pin can be configured as input or output. These pins are used to generate application-specific output signals or to acquire application-specific input signals. When used as an input pin, GPIO can be used as an interrupt source; when used as an output pin, each GPIO can be independently cleared or set to 1.

14.5.2 Features

The GPIO module has the following features:

Each GPIO pin can be configured as input or output. ÿWhen used as

an input pin, it can be used as an interrupt source, and each GPIO pin has independent interrupt control. ÿWhen used as an output pin,

each GPIO pin can be cleared or set to 1 independently.

GPIO interrupts are controlled by 7 registers such as GPIO_IS . The interrupt source, polarity and edge characteristics can be selected through these registers. For the interrupt register corresponding to GPIO, please refer to "3.3 Interrupt System".

ÿWhen multiple interrupts occur at the same time, they will be aggregated into one interrupt for reporting. For the interrupt mapping relationship of GPIO, please refer to "3.3 Interrupt System".

ÿ The three registers GPIO_IS, GPIO_IBE, and GPIO_IEV jointly determine the characteristics of the interrupt source and the interrupt trigger category.

Read the original state and masked state of the interrupt through GPIO_RIS and GPIO_MIS respectively. The final reporting of interrupts can be controlled through GPIO_IE. In addition, a separate GPIO_IC is provided for clearing control of interrupt status.

14.5.3 Functional description

Each GPIO group provides 8 programmable input and output pins. Each pin can be configured as input or output. These pins are used to generate or capture application-specific output or input signals.

GPIOs can generate maskable interrupts based on level or transition values. The GPIOINTR (General Purpose Input Output Interrupt) signal gives an indication to the interrupt controller that an interrupt has occurred.

14.5.4 Working method

interface reset

At power-on reset, all registers are cleared to 0, so the pin defaults to input.

When the reset signal is valid, GPIO has the following states:

Disable the interrupt by clearing the corresponding bit in GPIO_IE . All registers are

cleared to 0. All pins are configured

as inputs. Raw interrupt registers are all cleared to

0.

Interrupts are set as edge-triggered interrupts.

GPIO

Each pin can be configured as input or output, the specific steps are as follows:

1. Refer to the corresponding bits of the "Pin Multiplexing Control Register" to configure the pins, and enable the functions of the GPIO pins to be used.
2. Configure the register GPIO_DIR to select whether GPIO is used as input or output.

   GPIO is used for input: external signals are sent in through GPIO pins, and the input signal value can be viewed through the GPIO_DATA register. Note: The input signal

   will be sent to the pin that is multiplexed with **GPIO** at the same time.

   GPIO is used for output: first write the corresponding value to the GPIO_DATA register, and then write the value through GPIO output. Note: If **the**

   GPIO interrupt function is enabled at this time , when the output signal meets the trigger condition, an interrupt will also be generated.

----Finish

interrupt operation

If you want to generate an interrupt and avoid false interrupts, you must follow the following initialization sequence:

1. Configure GPIO_IS, select edge trigger or level trigger.
2. Configure GPIO_IEV, select falling edge/rising edge trigger and high level/low level trigger.
3. If edge trigger is selected, GPIO_IBE needs to be configured to select single-edge or double-edge trigger mode.
4. Ensure that the GPIO data line remains stable during the above operations.
5. Write 0xFF to the register GPIO_IC to clear the interrupt.
6. Set GPIO_IE to 1 to enable interrupts.

----Finish

The interrupt setting of GPIO is controlled by 7 registers. When one or more GPIO pins generate an interrupt, a combined interrupt output is sent to the interrupt controller. Edge trigger and level trigger have the following differences:

Edge Triggered Interrupt: Software must clear this interrupt to enable deeper interrupts.

Level-triggered interrupt: The external interrupt source should maintain this level until the processor recognizes the interrupt.

14.5.5 Register overview

The base addresses of the nine groups of GPIO registers are shown in Table 14-9 .

Table 14-9 Base addresses corresponding to 9 groups of GPIO registers

register	base address
GPIO8	0x201D_0000
GPIO7	0x201C_0000
GPIO6	0x201B_0000
GPIO5	0x201A_0000

register	base address
GPIO4	0x2019_0000
GPIO3	0x2018_0000
GPIO2	0x2017_0000
GPIO1	0x2016_0000
GPIO0	0x2015_0000

Table 14-10 is the offset address and definition of a single group of GPIO internal registers. GPIO0~GPIO8 have the same register group.

说明

The register address corresponding to GPIOn is: GPIOn base address + offset address of this register. The value range of n: [0, 8]

Table 14-10 GPIO Register Overview

offset address	name	describe	page number
0x000ÿ 0x3FC	GPIO_DATA	GPIO data register	14-80
0x400	GPIO_DIR	GPIO direction control register	14-81
0x404	GPIO_IS	GPIO interrupt trigger register	14-82
0x408	GPIO_IBE	GPIO double-edge trigger interrupt register	14-82
0x40C	GPIO_IEV	GPIO trigger interrupt condition register	14-82
0x410	GPIO_IE	GPIO Interrupt Mask Register	14-83
0x414	GPIO_RIS	GPIO Raw Interrupt Status Register	14-83
0x418	GPIO_MIS	GPIO Mask Status Interrupt Register	14-84
0x41C	GPIO_IC	GPIO Interrupt Clear Register	14-84

14.5.6 Register Description

GPIO_DATA

GPIO_DATA is the GPIO data register. Used to cache input or output data.

When the corresponding bit in GPIO_DIR is configured as an output, the value written to the GPIO_DATA register will be output to the corresponding pin (note that the correct pin multiplexing needs to be configured); if it is configured as an input, the corresponding input pin will be read value.

注意

When the corresponding bit of GPIO_DIR is configured as an input, the valid read result will return the value of the pin; when configured as an output, the valid read result will return the written value.

The GPIO_DATA register uses PADDR[9:2] to realize the masking operation of reading and writing register bits. This register corresponds to 256 address spaces. PADDR[9:2] correspond to GPIO_DATA[7:0] respectively. When the corresponding bit is high, the corresponding bit can be read and written; otherwise, if the corresponding bit is low, the operation cannot be performed. For example:

If the address is 0x3FC (0b11_1111_1100), all 8-bit operations of GPIO_DATA[7:0] are valid. If the address is 0x200 (0b10_0000_0000), it is only valid for the operation of GPIO_DATA[7].

Offset Address	Register Name	Total Reset Value
0x000ÿ0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	When GPIO is configured as input mode, it is input data for GPIO; when GPIO is configured as output mode, it is output data. Each bit can be controlled independently. Works with GPIO_DIR .

GPIO_DIR

GPIO_DIR is the GPIO direction control register. Used to configure the direction of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit can be controlled independently. 0: input; 1: output.

GPIO_IS

GPIO_IS is the GPIO interrupt trigger register. It is used to configure the trigger level mode of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: Edge triggered interrupt; 1: Level triggered interrupt.

GPIO_IBE

GPIO_IBE is the GPIO double edge trigger interrupt register. Used to configure GPIO pin edge trigger mode.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge trigger control register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: single-edge trigger interrupt, specifically rising or falling edge trigger is controlled by GPIO_IEV ; 1: bilateral trigger interrupt.

GPIO_IEV

GPIO_IEV is the GPIO trigger interrupt condition register. Used to configure GPIO pins to trigger interrupt conditions.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO trigger interrupt condition register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: Falling edge or low level trigger interrupt; 1: Rising edge or high level trigger interrupt.

GPIO_IE

GPIO_IE is the GPIO interrupt mask register. Used to mask GPIO pin interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: mask interrupt; 1: Do not mask interrupts.

GPIO_RIS

GPIO_RIS is the GPIO raw interrupt status register. Used to query the original interrupt status of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, indicating unmasked interrupt status. This state is not controlled by the GPIO_IE register mask. 0: Interrupt has occurred; 1: Interrupt has not occurred.

GPIO_MIS

GPIO_MIS is the GPIO mask status interrupt register. Used to query the interrupt status of the GPIO pins masked.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, indicating the masked interrupt status. This state is controlled by the GPIO_IE register mask. 0: Interrupt is invalid; 1: Interrupt is valid.

GPIO_IC

GPIO_IC is the GPIO interrupt clear register. It is used to clear the interrupt generated by GPIO pin, and clear the GPIO_RIS register and GPIO_MIS register at the same time.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit can be controlled independently. 0: no effect; 1: Clear interrupt.

14.6 USB 2.0 Host

14.6.1 Overview

USB 2.0 Host controller supports High-speed (480Mbit/s), Full-speed (12Mbit/s) and Low speed (1.5Mbit/s) three kinds of data transmission. The USB 2.0 Host Controller supports USB 2.0, OHCI Rev 1.0a and EHCI Rev 1.0 protocols. The USB 2.0 Host controller contains a Root Hub (a part of the USB system, through which the USB interface can be extended). The features of the USB 2.0 Host controller are as follows:

Complete the control and processing of

transmission, analyze and package

data packets, encode and decode USB transmission

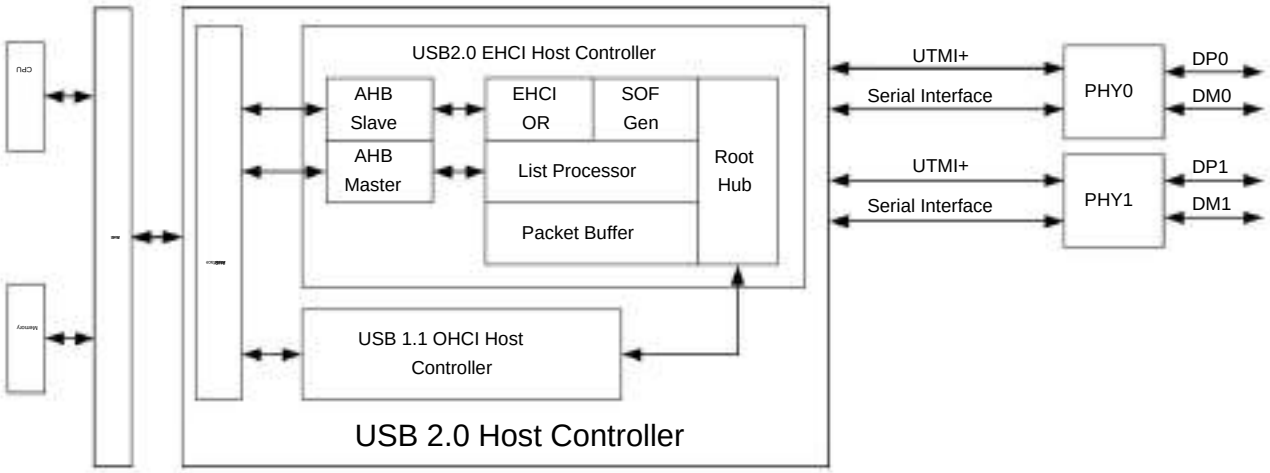
signals, and provide interfaces such as interrupt vectors for drivers

14.6.2 Functional Description

Logic block diagram

The logic block diagram of USB 2.0 Host is shown in Figure 14-39 .

Figure 14-39 USB 2.0 Host logic block diagram



UTMIÿUSB2.0 Transceiver Macrocell Interface

EHCIÿEnhanced Host Controller Interface

OHCIÿOpen Host Controller Interface

typical application

The reference design of USB 2.0 Host is shown in Figure 14-40 .

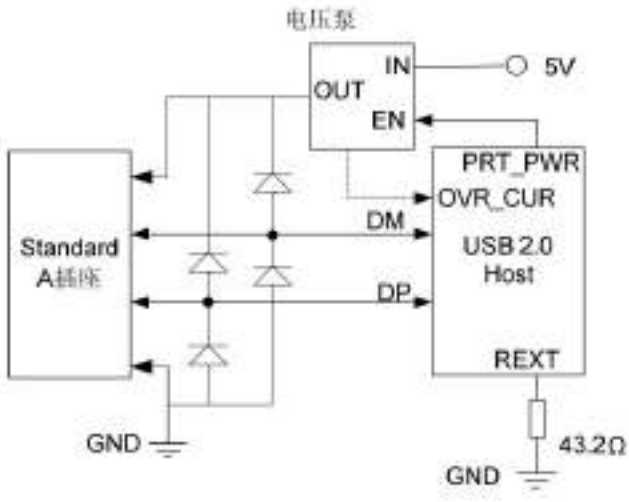
注意

The single-ended impedance of DP and DM is 45ÿ±1%, so DP and DM do not need any external matching resistors.

The accuracy of the REXT resistor is ±1%.

Need to use high-speed ESD devices, the recommended capacitance value is about 1pF.

Figure 14-40 USB 2.0 Host Reference Design



Features

USB 2.0 Host has the following features:

- Fully compatible with USB 2.0.
- Fully compliant with OHCI Rev 1.0a, EHCI Rev 1.0. Can support
- High-speed, Full-speed, Low-speed three devices. Supports low power solutions. Supports
- four basic data transfer types: Control
- Transfer, Bulk Transfer, Isochronous Transfer, and Interrupt Transfer. Up to 127 devices can be connected by connecting the USB Hub.

working principle

USB 2.0 Host supports the following four standard transmission methods:

- Control Transfer (control transfer) is mainly
- used for the transfer between USB Host and USB Device endpoint 0, and the control transfer of certain types of USB devices may use other endpoints. Control transmission is two-way transmission, the amount of data is usually small, and can transmit 8byte, 16byte, 32byte or 64byte data, depending on the device and transmission speed.
- Bulk Transfer (bulk transfer) is mainly
- used to send and receive a large amount of data without bandwidth and interval time requirements. This type of device is suitable for very slow transmission and a large number of delayed transmissions. It can wait until all other types of data Send and receive data after the transfer is complete. Its characteristic is to ensure that the data of USB Host and USB Device is sent without error by means of error detection and retransmission.
- Isochronous Transfer (synchronous transfer) is
- mainly used for streaming data transmission with strict time and strong fault tolerance, or for real-time applications with constant data transmission rate. Isochronous transmission provides deterministic bandwidth and interval time.

Interrupt Transfer (interrupt transfer) is mainly

used for the transmission of small amount, scattered and unpredictable data. In the interrupt transmission mode, periodically check whether the device has interrupt data to send. The structure of the endpoint mode device of the device determines its query frequency is 1ms ~ 255ms. Typical interrupt mode transmission is unidirectional, and there is only input mode for USB Host.

14.6.3 Working method

Pin Polarity Control

You can set USB0_PWREN,
The effective polarity of USB1_PWREN; set the effective polarity of USB0_OVRCUR and USB1_OVRCUR by setting the system control register PERIPHCTRL20 [usbovr_p_ctrl].

clock gating

When the USB 2.0 Host is not in use, the clock of the USB 2.0 Host can be turned off to reduce power consumption.

The procedure for shutting down the clock is as follows:

1. To PERI_CRG46 [usbphy_port0_treq], PERI_CRG46[usbphy_port1_treq], PERI_CRG46[usbphy_req]ÿPERI_CRG46[usb_ctrl_utmi0_req]ÿ PERI_CRG46[usb_ctrl_utmi1_req]ÿPERI_CRG46[usb_ctrl_hub_req]ÿ Write 1 to PERI_CRG46[usb_ahb_srst_req] to reset the USB controller and PHY.
2. Set the system register PERI_CRG46 [usb_cken] to 0, and turn off the clock related to USB 2.0 Host.

----Finish

The steps to turn on the clock are as follows:

1. Set the PERI_CRG46 [usb_cken] of the system controller to 1, and turn on the clock related to the USB 2.0 Host.
2. Undo the reset of the USB controller and PHY, see "Undoing Reset" for details.

----Finish

undo reset

The USB controller and PHY are in the reset state by default after power-on, and the steps to cancel the reset are as follows:

1. Delay at least 10us.
2. Write 0 to PERI_CRG46[usbphy_port0_treq] to cancel the port soft reset of USB PHY port0; write 0 to PERI_CRG46[usbphy_port1_treq] to cancel the port soft reset of USB PHY port1.
3. Write 0 to PERI_CRG46[usbphy_req] to cancel the general reset of USB PHY;
4. After a delay of 250us, write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to cancel the soft reset of the port0 interface of the USB controller; write 0 to PERI_CRG46[usb_ctrl_utmi1_req] to cancel the soft reset of the port1 interface of the USB controller; write 0 to PERI_CRG46[usb_ctrl_hub_req] , to undo the hub soft reset of the USB controller.
5. Write 0 to PERI_CRG46[usb_ahb_srst_req] to cancel the USB bus side soft reset.

----Finish

Reset port0 or port1 individually during work

The steps to reset port0 individually during work are as follows:

1. Write 1 to PERI_CRG46[usb_ctrl_utmi0_req] to soft reset port0 of USB controller.
2. Write 1 to PERI_CRG46[usbphy_port0_treq] to soft reset the USB PHY port0 port.
3. After a delay of 200us, write 0 to PERI_CRG46[usbphy_port0_treq] to cancel port0 port of USB PHY Mouth reset.
4. Write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to cancel port0 reset of USB controller.

----Finish

The steps to reset port1 individually during work are as follows:

1. Write 1 to PERI_CRG46[usb_ctrl_utmi1_req] to soft reset the port1 interface of the USB controller.
2. Write 1 to PERI_CRG46[usbphy_port1_treq] to soft reset the USB PHY port1 port.
3. After a delay of 200us, write 0 to PERI_CRG46[usbphy_port1_treq] to cancel the port1 port of USB PHY Mouth reset.
4. Write 0 to PERI_CRG46[usb_ctrl_utmi1_req] to cancel port1 reset of USB controller.

----Finish

suspend and restart

Suspend port0 (ie SUSPEND): After the software sets the suspend mode through the EHCI/OHCI register, port0 enters the suspend mode.

Restart port0 (ie RESUME): After the software exits SUSPEND mode through the EHCI/OHCI register setting, if PERIPHCTRL21 [commononn] is 1, the software can initiate a USB operation after a delay of at least 225us; if PERIPHCTRL21 [commononn] is 0, it needs at least After a delay of 5us, the software can initiate the USB operation.

说明

The operation of suspending port1 is similar to that of suspending port0, and the operation of restarting port1 is similar to that of restarting port0.

USB TX signal quality adjustment

If the test finds that the USB eye diagram on the board cannot pass the mask, you can adjust the signal quality of the USB TX through the following steps.

Take USB port0 as an example.

1. Write 1 to PERIPHCTRL21[phy0_txpreemphasistune] to enable the pre-emphasis function of USB port0.
2. Write 1 to PERIPHCTRL21[phy0_txrisetune] to reduce the rise/fall time of the high speed signal.
3. Write 0xF to PERIPHCTRL21[phy0_txverftune] to increase the DC level.

---Finish

说明

If it is found that the USB eye diagram cannot pass the mask, please confirm that the above registers have been configured.

14.6.4 Register Overview

说明

Since the USB module is a standard USB 2.0 Host, the internal registers are also standard EHCI and OHCI registers, which are described in detail in the EHCI protocol and OHCI protocol, please refer to the protocol. Only the specially defined registers are described below.

An overview of the USB registers is shown in Table 14-11 .

Table 14-11 USB register overview (base address: 0x100B_0000)

offset address	name	describe	page number
0x90	INTNREG00	Configure Microframe Length Register	14-90
0x94	RESERVED	reserve	.
0x98	RESERVED	reserve	.
0x9C	RESERVED	reserve	.
0xA0	INTNREG04	DEBUG register	14-91
0xA4	INTNREG05	Control and Status Registers	14-92
0xA8	INTNREG06	AHB Error Status Register	14-93
0xAC	INTNREG07	AHB Error Address Register	14-93

Note: The base address of the EHCI register is 0x100B_0000, the base address of the OHCI register is 0x100A_0000, and the base address of the register in Table 14-11 is the base address of the EHCI register.

14.6.5 Register Description

INTNREG00

INTNREG00 is the configuration microframe length register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													val		in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:14]	- reserved	reserve.
[13:1]	RW val	Microframe counter value. This register is for emulation only. During normal operation, the microframe length is 125ÿs specified in the protocol; during simulation, in order to shorten the simulation time, this register can be configured to change the microframe length as required.
[0]	RW and	Enable this register. 0: forbidden; 1: enable.

INTNREG04

INTNREG04 is the DEBUG register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:6]	reserved	reserve.
[5]	RW auto_en	Auto specification enabled. 0: enable (the suspend signal is valid when the software resets run/stop, but the hchalted bit is not set); 1: Disabled (that is, the port does not hang when software clears the run/stop bit). The default is 0.

[4] RW	nak_reldfix_en		NAK reload enable. 0: enable; 1: Prohibited.
[3]		reserved	reserve.
[2] RW		time. scaledwn_enum_ti me	Reduce port enumeration 0: disabled; 1: enable.
[1] RW	hccparam_en		HCCPARAMS register writable enable. 0: forbidden; 1: enable.
[0] RW	hcsparam_en		HCSPARAMS register writable enable. 0: forbidden; 1: enable.

INTNREG05

INTNREG05 is the control and status register. Used to read and write PHY registers.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vbusy vport vcontrol_loadm vcontrol	vstatus
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	-	reserved	reserve.
[17]	RO	vbusy	"1" indicates that the hardware is currently performing a data write operation, and only when the process ends, the bit is cleared.
[16:13]	RW	vport	The port number, which cannot exceed the number of supported ports.
[12]	RW	vcontrol_loadm	Load enable. 0: enable; 1: Prohibited.
[11:8]	RW	vcontrol	port control signal.

[7:0] RO	vstatus		Port status signal.

INTNREG06

INTNREG06 is the AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	err_capture	reserved		hbusrt_err	num_beat_err num_beat_ok
Reset	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31]	RW	err_capture	An AHB error has occurred.
[30:12]		reserved	reserve.
[11:9]	RO	hbusrt_err	Controls the hburst value of the transfer phase when an AHB error occurs.
[8:4]	RO	num_beat_err	The number of beats for this burst transfer when an AHB error occurs. The maximum number of beats is 16ÿ 0x00~0x10: valid; 0x11~0x1F: Reserved.
[3:0]	RO	num_beat_ok	The number of beats that have been successfully completed in this burst transfer when an AHB error occurs.

INTNREG07

INTNREG07 is the AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address of the control transfer phase when an AHB error occurs.

14.7 HOURS

14.7.1 Overview

SATA is based on the AMBA 2.0 AHB bus interface, which facilitates the rapid implementation of integrated applications in SOC systems; provides drivers developed based on the Linux operating system to help software personnel quickly complete the custom development of SOC subsystem drivers; Hi3520D/Hi3515A supports up to 2 SATA Port, Hi3515C supports one SATA port; in addition, it also provides support at the controller level for the latest features such as NCQ, hot swap, Port Multiplier, and eSATA.

14.7.2 Features

The SATA interface of Hi3520D has the following characteristics:

Provide ARM AHB system bus Slave interface, the related standard is AMBA Spec 2.0. Only 32bit access mode is supported. Provide ARM AHB

system bus Master interface, the related standard is AMBA Spec 2.0. Only 32bit access mode is supported. Provide standard interface signals connected

with PHY. Support SATA2.5 and AHCI1.2 protocols.

Support PIO, Legacy DMA, NCQ, ATAPI operations.

Supports power management features. Support Port Multiplier feature.

Supports up to 2 SATA ports.

(Hi3515C supports 1 SATA port)

Support auto-negotiation of 1.5Gbps and 3.0Gbps rate. Support

interrupt reporting mechanism.

14.7.3 Signal description

SATA interface signals are shown in Table 14-12 .

Table 14-12 SATA interface signal description

Signal Name Direction Description			Corresponding pin
SREFCKM I		Negative differential clock input for SATA.	SREFCKM
SREFCKP	I	Non-inverting differential clock input for SATA.	SREFCKP
SRESREF	I/O SATA expansion resistance pin, external expansion resistance. SRESREF		
SRXM0	I	Negative phase differential data input for SATA port 0.	SRXM0
SRXM1	I	Negative phase differential data input for SATA port 1.	SRXM1

Signal Name	Direction	Description	Corresponding pin
SRXP0	I	Non-inverting differential data input for SATA port 0.	SRXP0
SRXP1	I	Non-inverting differential data input for SATA port 1.	SRXP1
STXM0	O	Negative phase differential data output for SATA port 0.	STXM0
STXM1	O	Negative differential data output for SATA port 1.	STXM1
STXP0	O	Non-inverting differential data output for SATA port 0.	STXP0
STXP1	O	Non-inverting differential data output for SATA port 1.	STXP1

SRXM1, SRXP1, STXM1 and STXP1 pins in Hi3515C are NA.

14.7.4 Functional description

typical application

Typical SATA application modes are shown in Figure 14-41, Figure 14-42, and Figure 14-43 .

Figure 14-41 Typical application mode 1

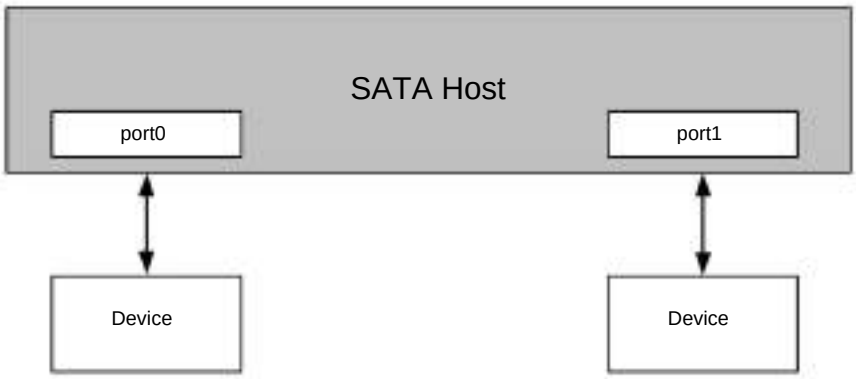


Figure 14-42 Typical application mode 2

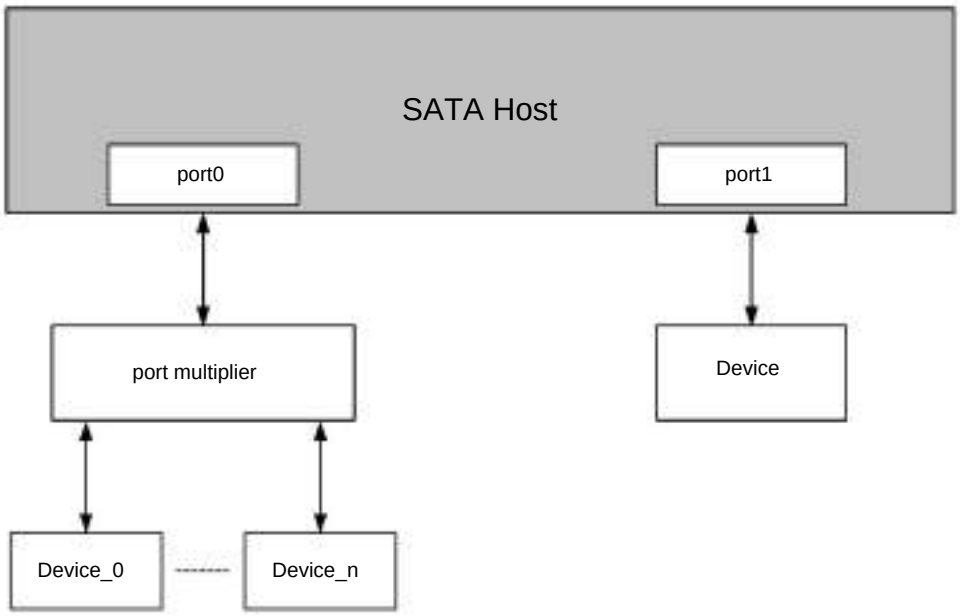
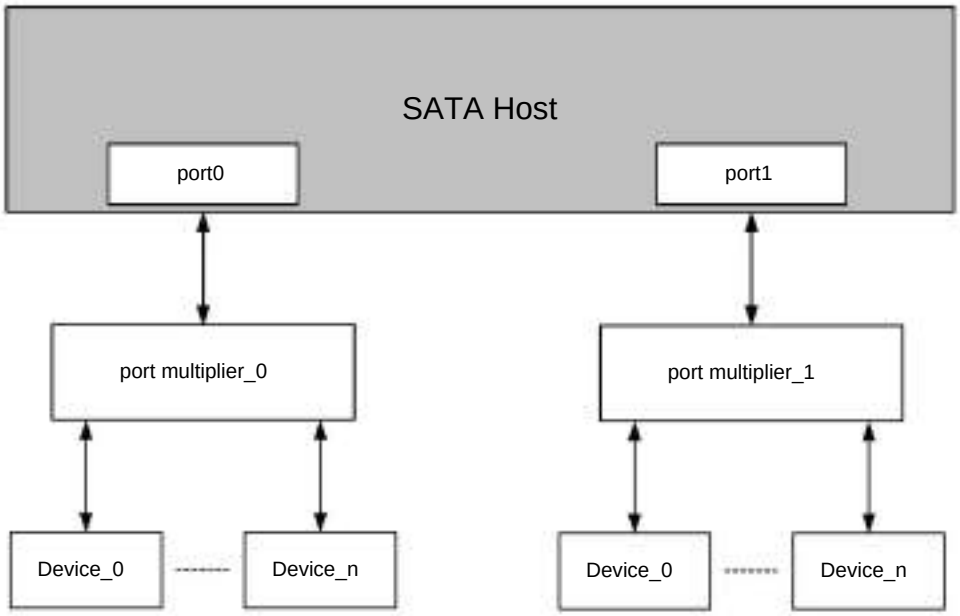


Figure 14-43 Typical application mode 3



注意

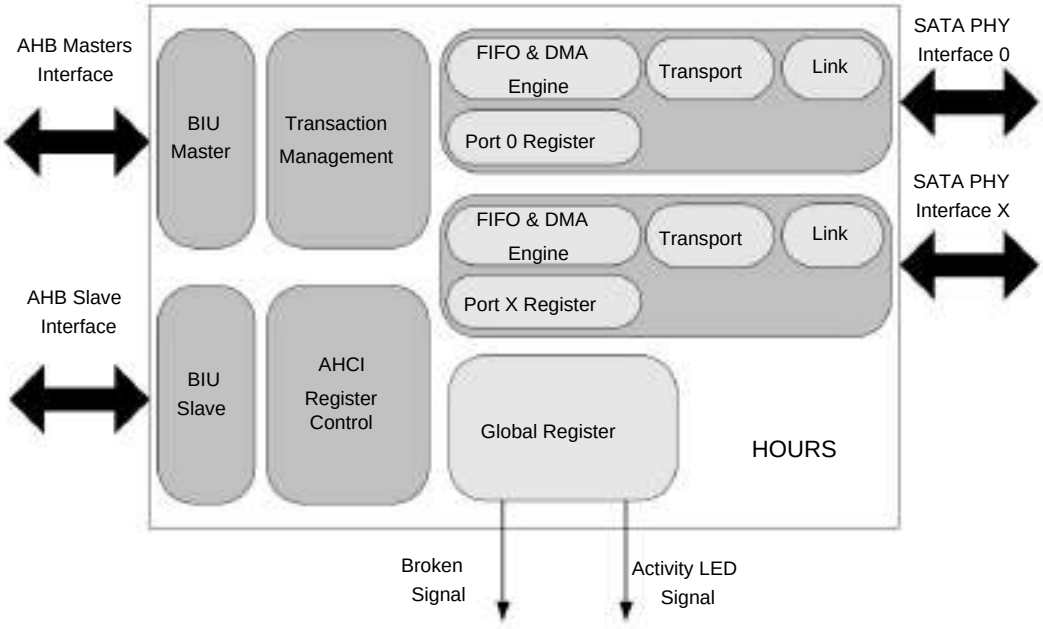
Hi3515C only has PORT0 available.

SATA Host provides support for direct connection with devices such as hard disks and optical drives, and can support two devices at the same time. At the same time, it also supports any port to expand the Port Multiplier, and the Port Multiplier can connect multiple Devices according to its own external expansion capabilities.

Functional principle

The Hi3520D SATA module architecture is shown in Figure 14-44 .

Figure 14-44 Hi3520D SATA module architecture



The AHB Master and AHB Slave interfaces are connected to the AHB based on ARM AMBA2.0 system bus. There should also be ARM CPU and System Memory Controller on the system bus. The software configures SATA through the AHB Slave interface, and the AHB Master interface can actively access System Memory The DRAM controlled by the Controller completes command read operations and data read and write operations.

SATA Host supports PIO, Legacy DMA, Native Commad Queue, ATAPI operations.

The interrupt signal is connected to the system interrupt controller.

Inside the chip, the SATA PHY interface is connected to the SATA PHY; outside the chip, the SATA PHY can be connected to a hard disk or optical drive that supports SATA; the SATA PHY can also be connected to the SATA Port Multiplier to expand to multiple ports.

In addition, the Activity LED display signal can be directly connected to the chip, and this function can be selected according to the actual application.

14.7.5 Working method

14.7.5.1 Clock gating

Configure the system controller PERI_CRG45[sata0_cken] and PERI_CRG45[sata1_cken] as 1 to enable the clock of the SATA module; configure the system controller PERI_CRG45[sata0_cken] and PERI_CRG45[sata1_cken] as 0 to disable the clock of the SATA module.

14.7.5.2 Clock configuration

By configuring the SATA Host internal control register SATA_PHY0_CTLH bit[13] to select the reference clock source for SATA PHY, you can control whether the SATA PHY clock is generated on-chip or input from an external clock source:

When SATA_PHY0_CTLH bit[13] is 1, SREFCKM and SREFCKP are generated on-chip. When SATA_PHY0_CTLH bit[13] is 0, SREFCKM and SREFCKP are input by external clock source.

The reference clock supported by SATA PHY ranges from 25MHz to 156.25MHz. Since the input clock range supported by the MPLL inside the PHY is 50MHz to 78.125MHz, when the provided reference clock changes, it is necessary to configure the SATA_PHY0_CTLL bit[31:30] of the control register inside the SATA Host to satisfy the clock of the MPLL inside the PHY . Require. Please refer to the description of SATA_PHY0_CTLL bit[31:30] for details.

14.7.5.3 Soft Reset

SATA Host has multiple soft reset controls, which are described as follows:

By configuring the system controller PERI_CRG45 bit[7] to be 1, a separate soft reset for the sata_alive clock domain can be realized. By

configuring the PERI_CRG45 bit[6] of the system controller to be 1, the independent soft reset of the sata_rx clock domain of port1 can be realized. (Hi3515C does not need this configuration) By

configuring the system controller PERI_CRG45 bit[5] to be 1, the independent soft reset of the sata_rx clock domain of port0 can be realized. By

configuring the PERI_CRG45 bit[4] of the system controller to be 1, the independent soft reset of the sata_tx clock domain of port1 can be realized. (Hi3515C does not need this configuration) By

configuring the system controller PERI_CRG45 bit[3] to be 1, the independent soft reset of the sata_tx clock domain of port0 can be realized. By

configuring the system controller PERI_CRG45 bit[0] to be 1, the individual soft reset of the PHY can be realized. By

configuring the system controller PERI_CRG45 bit[1] to be 1, the HCLK clock domain can be individually soft reset. By configuring the

system controller PERI_CRG45 bit[2] to be 1, the SATA Host can be soft reset.

In addition, two synchronous reset strategies are provided in the SATA Host controller:

Configure SATA Host controller When the internal SATA_GHC_GHC bit[0] is 1, the SATA Host enters the reset state, and the logic of all internal modules returns to the initial value. SATA_GHC_GHC bit[0] is automatically cleared to 0 after reset is completed. When the

SATA_PORT_CMD bit[0] in Port0 or Port1 is configured from 1 to 0, the corresponding Port0 or Port1 of the SATA Host enters the reset state.

14.7.5.4 Working mode configuration

Before the SATA Host works, it must first complete the initial configuration of the PHY, so that the PHY can work normally; at the same time, complete the initial negotiation with the Device.

Initialize PHY

Taking the reference clock of PHY 150MHz and coming from the chip as an example, the steps to initialize and configure port0 with 1.5Gbps speed are as follows:

1. Set PERI_CRG45 bit [11] to 0, select CRG to output 150MHz reference clock.
2. Set PERI_CRG45 bit [1] to 0 to cancel the soft reset of the SATA controller bus.
3. Set PERI_CRG45 bit [0] to 0 to cancel SATA PHY soft reset.
4. Set SATA_PHY0_CTLH bit[12] to 1, and turn off the reference clock provided to PHY.
5. Configure the SATA_PHY0_CTLL register to 0x880E_C788 (if SATA works in 3G mode, configure this register The register is 0x880E_C888).
6. Configure the SATA_PHY0_CTLH register to 0x2121.
7. Configure the SATA_OOB_CTL register to 0x8406_0C15.
8. Configure the SATA_PORT_PHYCTL register as 0x0E26_2709 (if SATA works in 3G mode, configure this register as 0x0E66_2709).
9. Set PERI_CRG45 bit[0] to 1, soft reset SATA PHY.
10. Set PERI_CRG45 bit [0] to 0 to cancel SATA PHY soft reset.
11. Set PERI_CRG45 bit [2] to 0 to cancel the soft reset of the SATA controller interface.
12. Set PERI_CRG45 bit [3] to 0 to cancel the soft reset of the SATA controller tx0 clock domain.
13. Set PERI_CRG45 bit [5] to 0 to cancel the soft reset of the SATA controller rx0 clock domain.
14. Set PERI_CRG45 bit [7] to 0 to cancel the SATA controller alive clock domain soft reset.

----Finish

initial negotiation

Wait for the PLL of the PHY to work normally, and the Host starts to complete the initial negotiation with the Device.

1. Set SATA_PORT_CMD[cmd_sud] to 1.
2. Wait for the indication signal phyrdy given by PHY to be valid, and check whether the port is normal by checking whether SATA_PORT_SSTS[pxssts_det] is equal to 3. If SATA_PORT_SSTS[pxssts_det] is equal to 3, it means the initialization is successful.

----Finish

Operating business

After the initial negotiation is completed, start business operations through the following steps:

1. Clear the interrupt (it is not necessary to perform this operation after starting the work for the first time, or after reset), and configure in sequence SATA_PORT_SERR, SATA_PORT_IS and SATA_GHC_IS registers, configuration values are 0xFFFFFFFFÿ

2. Configure the interrupt mask register SATA_PORT_IE to mask out the interrupts that do not need to be reported.

3. Enable the global interrupt, configure the SATA_GHC_GHC register to 0x80000002.

4. Create a linked list according to the format of the SATA command linked list in Appendix A.

5. Set the base address of the port command list in the memory, configure the register bit SATA_PORT_CLB[port_clb] (the configuration value is the base address of the memory allocated for the command list), and notify the location to send the DMAC read command and data.

6. Set the base address of the memory where the port receives the frame. The configuration register bit SATA_PORT_FB[port_fb] (the configuration value is the base address of the memory allocated for the received frame) informs the receiving DMAC of the location where the FIS is saved.

7. Set SATA_PORT_CMD[cmd_fre] to 1, enable sending DMAC, receive FIS and write to system memory; configure SATA_PORT_CMD [st] to 1, enable sending DMAC, and send commands and data.

8. Configure the port command sending control register SATA_PORT_CI to indicate which command is currently ready to be sent.

9. Perform command sending and data transmission.

10. The software judges whether the current command is completed or not through the interrupt bit and command execution status. When an interrupt is received, if For PIO/DMA operation, check whether the CI bits are all cleared to 0; for NCQ operation, check whether the corresponding bits of CI and SACT are both cleared to 0.

11. To start the next transmission, repeat 1-10.

----Finish

说明

Legacy DMA operation, PIO operation, and ATAPI operation are all operated according to the above steps, the difference lies in the established linked list (different command codes, flag bits, etc.). In addition

to establishing a different linked list, the NCQ operation also needs to configure the register SATA_PORT_SACT, which indicates the number of commands executed by the NCQ operation. After the step 7 above, add the step of "configuring the register SATA_PORT_SACT". It is necessary to ensure that the command position of the SATA_PORT_SACT configuration and the SATA_PORT_CI Corresponds to the position of the command in .

14.7.6 Register overview

Table 14-13 shows the value range and meaning of the variables in the register offset address .

Table 14-13 Register offset address variable table

variable name	Description of value range	
n	0ÿ1	2 ports of the controller (Hi3515C has 1 port)

SATA Register Overview

The SATA register overview is shown in Table 14-14 .

Table 14-14 SATA register overview (base address is 0x1008_0000)

offset address	name	describe	page number
0x0000	SATA_GHC_CAP1	Feature Support Register 1	14-103
0x0004	SATA_GHC_GHC	global control register	14-104
0x0008	SATA_GHC_IS	Interrupt Status Register	14-105
0x000C	SATA_GHC_PI	port implementation register	14-105
0x0010	SATA_GHC_VS	AHCI Version Identification Register	14-106
0x0014	SATA_GHC_CCC_CTL	CCC Control Register	14-106
0x0018	SATA_GHC_CCC_PORTS	CCC Port Enable Register	14-107
0x0024	SATA_GHC_CAP2	feature support register 2	14-108
0x0028	SATA_GHC_BOHC	BIOS/OS Handover Control Register	14-108
0x0050	SATA_GHC_TM	TM Test Status Register	14-109
0x0054	SATA_PHY0_CTLL	PHY0 Global Control Low Register	14-110
0x0058	SATA_PHY0_CTLH	PHY0 global control high register	14-111
0x005C	SATA_PHY0_STS	PHY0 global status register	14-112
0x006C	SATA_OOB_CTL	PHY OOB control register	14-113

SATA_PORT_CFG Register Overview

The SATA_PORT_CFG register overview is shown in Table 14-15 .

Table 14-15 SATA_PORT_CFG register overview (base address is 0x1008_0100)

offset address	name	describe	page number
0x000+nx 0x80	SATA_PORT_CLB	command list base address register	14-113
0x008+nx 0x80	SATA_PORT_FB	Receive FIS base address register	14-114
0x010+nx 0x80	SATA_PORT_IS	Port Interrupt Status Register	14-114

offset address	name	describe	page number
0x014+nx0x80	SATA_PORT_IE	Port Interrupt Mask Register	14-116
0x018+nx0x80	SATA_PORT_CMD	port command and status register	14-118
0x20+nx0x80	SATA_PORT_TFD	port task file register	14-121
0x24+nx0x80	SATA_PORT_SIG	port signature register	14-121
0x028+nx0x80	SATA_PORT_SSTS	interface status register	14-122
0x02C+nx0x80	SATA_PORT_SCTL	interface control register	14-123
0x30+nx0x80	SATA_PORT_SERR	Error Diagnostic Status Register	14-124
0x034+nx0x80	SATA_PORT_SACT	NCQ Command Identification Control Register	14-126
0x38+nx0x80	SATA_PORT_CI	command sending control register	14-126
0x3C+nx0x80	SATA_PORT_SNTF	asynchronous notification event indication register	14-127
0x044+nx0x80	SATA_PORT_FIFOTH	Receive FIFO Watermark Register	14-128
0x050+nx0x80	SATA_PORT_HBA	HBA Test Status Register	14-128
0x054+nx0x80	SATA_PORT_LINK	Link Test Status Register	14-129
0x058+nx0x80	SATA_PORT_DMA 1	DMAC Test Status Register 1	14-130
0x05C+nx0x80	SATA_PORT_DMA 2	DMAC Test Status Register 2	14-131
0x060+nx0x80	SATA_PORT_DMA 3	DMAC Test Status Register 3	14-132
0x064+nx0x80	SATA_PORT_DMA 4	DMAC Test Status Register 4	14-132
0x068+nx0x80	SATA_PORT_DMA 5	DMAC Test Status Register 5	14-132
0x6C+nx0x80	SATA_PORT_DMA 6	DMAC Test Status Register 6	14-133

offset address	name	describe	page number
0x070+nx 0x80	SATA_PORT_DMA 7	DMAC Test Status Register 7	14-133
0x074+nx 0x80	SATA_PORT_PHYC TL	PHY Control Registers	14-135
0x078+nx 0x80	SATA_PORT_PHYS TS	PHY Test Status Register	14-137

14.7.7 Register Description

SATA_GHC_CAP1

SATA_GHC_CAP1 is feature support register 1.

Offset Address	Register Name	Total Reset Value
0x0000	SATA_GHC_CAP1	0x6F26_FFA1

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name	s64a	sncq	ssntf	smps	sss	salp	shall	sclo	iss	reserved	himself	pm	fbss	pmd	ssc	psc	ncs	cccs	ems	sxs	e.g.
Reset	0	1	1	0	1	1	1	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	1

Bits	Access	Name	Description
[31]	RO	s64a	It is fixed at 0, which means it does not support 64-bit data structure access.
[30]	RO	sncq	It is fixed at 1, indicating that NCQ is supported.
[29]	RO	ssntf	Fixed to 1, which means port SNTF register is supported.
[28]	RO	smps	It is fixed at 0, indicating that mechanical hot swap is not supported.
[27]	RO	sss	Fixed to 1, which means staggered spin-up is supported.
[26]	RO	salp	It is fixed to 1, indicating that it supports power management.
[25]	RO	shall	Fixed to 1, indicating that the lighting pin is supported.
[24]	RO	sclo	It is fixed to 1, indicating that it supports the command linked list overwriting.
[23:20]	RO	iss	It is fixed at 0x2, which means it can support a maximum rate of 3Gbps.
[19]	RO	reserved	reserve.
[18]	RO	himself	Fixed to 1, means only AHCI mode is supported.
[17]	RO	pm	It is fixed to 1, indicating that Port Multiplier is supported.
[16]	RO	fbss	It is fixed at 0, indicating that FIS-based Switching is not supported.

[15] RO		pmd	Fixed to 1, but PIO mode does not support the transfer of multiple DRQ blocks.
[14] RO		ssc	It is fixed at 1, indicating that it supports entering the Slumber state.
[13] RO		psc	It is fixed at 1, indicating that it supports entering the Partial state.
[12:8] RO		ncs	It is fixed at 0x1F, indicating that it supports 32 command slots.
[7]	RO	cccs	It is fixed at 1, indicating that it supports the CCC (Command Completion Coalescing) function.
[6]	RO	ems	It is fixed at 0, indicating that Enclose Management is not supported.
[5]	RO	sxs	Fixed to 1, which means External SATA is supported.
[4:0] RO		e.g.	It is fixed to 0x01, which means it supports 2 ports.

SATA_GHC_GHC

SATA_GHC_GHC is the global control register.

Offset Address	Register Name	Total Reset Value
0x0004	SATA_GHC_GHC	0x8000_0000

Bit	31	30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	[illegible]	reserved
Reset	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31] RO		ahci_en	It is fixed as 1, which means that the software can only interact with the controller through the AHCI mechanism.
[30:2] RO		reserved	reserve.
[1] RW	int_enable		Controller interrupt enable. 0: forbidden; 1: enable.
[0] RW	hba_rst		Controller soft reset control. 0: no reset; 1: Reset. Write 1 to reset the controller, and it will be automatically cleared to 0 after the reset is completed; writing 0 has no effect on the controller. Reset does not affect SATA_GHC_BOHC, SATA_PORT_FB, SATA_PORT_CLB register.

SATA_GHC_IS

SATA_GHC_IS is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	SATA_GHC_IS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved	[illegible]	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WC	ips_ccc	CCC interrupt status. 0: No CCC interrupt is generated; 1: A CCC interrupt has been generated.
[30:2]	RO	reserved	reserve.
[1]	WC	ips_port1	Port 1 interrupt status. 0: report without interruption; 1: An interrupt is reported.
[0]	WC	ips_port0	Port 0 interrupt status. 0: no interrupt reporting; 1: interrupt reporting.

SATA_GHC_PI

SATA_GHC_PI is a port implementation register.

Offset Address	Register Name	Total Reset Value
0x000C	SATA_GHC_PI	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	[illegible]	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x000C	SATA_GHC_PI	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access Name		Description
[1:0] RO		port_imp	Port valid indication, when the value is 0x3, it means 2 ports 0~1 are valid, bit[1]~bit[0] correspond to port 1~port 0 respectively. 0: The port is invalid; 1: The port is valid.

SATA_GHC_VS

SATA_GHC_VS is the AHCI version identification register.

Offset Address	Register Name	Total Reset Value
0x0010	SATA_GHC_VS	0x0001_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	achi_vs																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0] RO		achi_vs	Indicates that the supported AHCI version is V1.2.

SATA_GHC_CCC_CTL

SATA_GHC_CCC_CTL is the CCC control register.

Offset Address	Register Name	Total Reset Value
0x0014	SATA_GHC_CCC_CTL	0x0001_01F8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ccc_tv																ccc_cc								ccc_int							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ccc_tv	CCC timeout parameter, the unit is ms. When the CCC function is enabled, the timeout counter is loaded with this parameter value. When the port participating in the CCC function has a command being executed, the counter is decremented by 1 every 1ms until it is decremented to 0 and a CCC interrupt is generated. After the CCC interrupt is generated, the counter is reloaded with this parameter value. parameter for the next round of counting. This bit cannot be written to 0.
[15:8]	RW	ccc_cc	The CCC command completes the upper limit value. When the CCC function is enabled, the command completion counter is cleared to 0, and the number of command completions of each port participating in the CCC function starts to accumulate. If the counter is accumulated to be greater than or equal to this parameter, a CCC interrupt is generated. After the CCC interrupt is generated, the counter is cleared to 0 and restarts. Cumulative count for the next round. If writing 0 to this bit, the command complete interrupt will be disabled, and the CCC interrupt can only be generated due to timeout.
[7:3]	RO	ccc_int	CCC interrupt vector number, its value is 0x1F (31), which means that SATA_GHC_IS bit[31] is the CCC interrupt status.
[2:1]	RO	reserved	reserve.
[0]	RW	ccc_en	The CCC function is enabled. 0: forbidden; 1: enable. Note: When **the CCC** function is enabled , **the ccc_tv** and **ccc_cc** parameter values cannot be changed.

SATA_GHC_CCC_PORTS

SATA_GHC_CCC_PORTS is the CCC port enable register.

Offset Address	Register Name	Total Reset Value
0x0018	SATA_GHC_CCC_PORTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ccc_prt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	ccc_prt	Specifies the ports participating in the CCC function. Bit[1]~bit[0] represent ports 1~0 respectively. If the corresponding bit is 1, it means that the port participates in CCC counting, and if it is 0, it means that the port does not participate in CCC counting. This register can be changed at any time and take effect.

SATA_GHC_CAP2

SATA_GHC_CAP2 is feature support register 2.

Offset Address	Register Name	Total Reset Value
0x0024	SATA_GHC_CAP2	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	cap_boh	It is fixed at 1, indicating that it supports BIOS/OS handover management control.

SATA_GHC_BOHC

SATA_GHC_BOHC is the BIOS/OS handover control register.

Offset Address	Register Name	Total Reset Value
0x0028	SATA_GHC_BOHC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	bohc_bb	BIOS busy status indication. 0: BIOS is not busy; 1: BIOS is busy completing related operations and preparing to transfer control to OS.
[3]	WC	bohc_ooc	When the bohc_oos signal transitions from 0 to 1, this bit is locked to 1; writing 1 to this bit clears it to 0, writing 0 has no effect.
[2]	RW	bohc_sooe	Message interrupt enable. 0: Do not generate a message interrupt; 1: When the bohc_ooc bit is set to 1, a message interrupt will be generated.
[1]	RW	bohc_oos	Operating system controller request. 0: The OS has not applied for the control right of the controller; 1: The OS has applied for the control right of the controller. If bohc_oos is 1 and bios_bos is 0, it means that the operating system has taken control of the SATA controller. This bit is not affected when the controller is reset using the SATA_GHC_GHC[hab_rst] bit.
[0]	RW	bohc_bos	The BIOS has a controller control flag. 0: BIOS does not have control over the controller; 1: BIOS has established control of the controller. The BIOS will clear this bit if the operating system requests control of the controller. This bit is not affected when the controller is reset using the SATA_GHC_GHC[hab_rst] bit.

SATA_GHC_TM

SATA_GHC_TM is the TM test status register.

Offset Address	Register Name	Total Reset Value
0x0050	SATA_GHC_TM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RO	req_sel	The DMAC that currently obtains the right to use the AHB master. 0x0: Port 0 sends DMAC to obtain channel; 0x1; Port 0 receives DMAC to obtain channel; 0x2: Port 1 sends DMAC to obtain the channel; 0x3: Port 1 receives DMAC to obtain the channel; Others: Reserved.

SATA_PHY0_CTLL

SATA_PHY0_CTLL is PHY0 global control low register.

Offset Address	Register Name	Total Reset Value
0x0054	SATA_PHY0_CTLL	0x8D0E_C88A

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0									
Name		mpll_ncy				tx_lvl	los_lvl	acjt_lvl		
Reset	1 0 0 0 1	1 0 1 0 0 0 0 1 1				1 0 1 1 0 0 1 0 0 0 1 0 0 0 1 0 1 0				

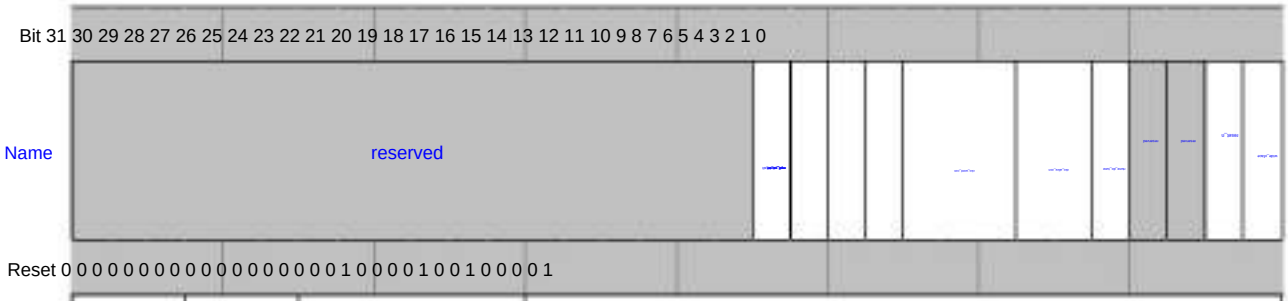
Bits	Access	Name	Description
[31:30]	RW	mpll_prescale	When the reference clock changes, this value needs to change accordingly. 00: Use ref_clk directly; 01: Double the frequency of ref_clk; 10: Divide the frequency of ref_clk by two; 11: Reserved.
[29:25]	RW	mpll_ncy	The PHY internal MPLL working parameters need to be used in conjunction with mpll_ncy5, indicating the multiplier value used.

[24:23] RW	mpll_ncy5		The PHY internal MPLL working parameters need to be used in conjunction with mpll_ncy to indicate the multiplier value used.
[22:20] RW	mpll_int_ctl		MPLL internal bandwidth control selection signal, must be configured as 0b000.
[19:17] RW	mpll_prop_ctl		MPLL internal bandwidth proportional control signal, must be configured as 0b111, and this value can only be changed when reset or MPLL is invalid.
[16:12] RW	tx_lvl		Send level parameter, related to the selected SATA protocol, must be set to 0b01100.
[11:7] RW	los_lvl		LOS signal detection level control, must be set to 0b10001.
[6:2] RW	acjt_lvl		ACJTAG Receive compare level control, must be set to 0b00010.
[1] RW	fast_tech		Indicates that this IP is processed under a fast process variable and must be set to 0.
[0] RW	pddq_h		IDDQ test signal, to perform IDDQ test, all Lane and support modules must be powered off before pddq_h is valid; in normal mode, it must be set to 0.

SATA_PHY0_CTLH

SATA_PHY0_CTLH is the PHY0 global control high register.

Offset Address	Register Name	Total Reset Value
0x0058	SATA_PHY0_CTLH	0x0000_2121



Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13]	RW	use_refclk_alt	PHY reference clock selection signal. 0: use refclk this group of differential signals; 1: Use the refclk_alt group of differential signals.

[12] RW mpll_ck_off			MPLL power-on control signal. The control of this signal needs to follow the following principles: 1. When providing refclk to MPLL, mpll_ck_off must be set to 0; 2. Before setting this signal to 0, mpll_ncy, mpll_ncy5 and mpll_prescale must be set to appropriate values; 3. If refclk is suspended or switched, or if mpll_ncy, mpll_ncy5 and mpll_prescale need to be changed, mpll_ck_off should be set to 1 first.
[11] RW mpll_pwron			Powers the MPLL. 0: cko_word clock will be invalid; 1: internal MPLL is reset and will generate cko_word clock signal based on the frequency of refclk. Before turning off **MPLL , tx_en** must be in **OFF** or **CM** state, and **rx_en** and **rx_pll_pwron** must be set to 0.
[10] RW mpll_ss_en			Spread spectrum function enable signal. 0: forbidden; 1: enable. If refclk has been spread-spectrum processed, it must be set to 0 here.
[9:7] RW cko_word_con			cko_word output selection signal.
[6:5] RW cko_alive_con			cko_alive output signal selection. 00: Invalid; 01: Keep the frequency output of the prescaler; 10: Output low frequency, which is prescaler/ 16; 11: Reserved.
[4] RW rtune_do_tune			Resistor adjustment enable signal. 0: no calibration; 1: Recalibrate the resistance.
[3]	RO	reserved	reserve.
[2]	RO	reserved	reserve.
[1] RW reset_n			The reset signal needs to be kept for at least 5ns.
[0] RW wide_xface			Interface bit width control. 0: The interface is 10bit; 1: The interface is 20bit.

SATA_PHY0_STS

SATA_PHY0_STS is the PHY0 global status register.

Offset Address	Register Name	Total Reset Value
0x005C	SATA_PHY0_STS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_sts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	phy0_sts	SATA PHY0 common part status register.

SATA_OOB_CTL

SATA_OOB_CTL is the PHY OOB control register.

Offset Address	Register Name	Total Reset Value
0x006C	SATA_OOB_CTL	0x8406_0C15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	oob_ctrl_valid							min_comiwake							max_comwake								min_cominit								max_cominit			
Reset	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1		1	0	0	0	0	0	1		1	0	0	0	0	0	1	0	1	0	1

Bits	Access Name		Description
[31]	RW	oob_ctrl_valid	OOB detection parameter configuration bit, when it is high level, select the parameter configuration of this register.
[30:24]	RW	min_comiwake	The minimum space count value required for COMWAKE space detection.
[23:16]	RW	max_comwake	The maximum space count value required for COMWAKE space detection.
[15:8]	RW	min_cominit	The minimum space count value required for COMINIT space detection.
[7:0]	RW	max_cominit	The maximum space count value required by COMINIT space detection.

SATA_PORT_CLB

SATA_PORT_CLB is the command list base address register.

Offset Address	Register Name	Total Reset Value
0x000+n x 0x80	SATA_PORT_CLB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	port_clb / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:10]	RW	port_clb	Sets the base address of the port command list in memory. This register value is not affected when the controller is reset using the SATA_GHC_GHC[hab_rst] bit.
[9:0]	RO	reserved	reserve.

SATA_PORT_FB

SATA_PORT_FB is the receiving FIS base address register.

Offset Address	Register Name	Total Reset Value
0x008+n x 0x80	SATA_PORT_FB	0x0000_0000

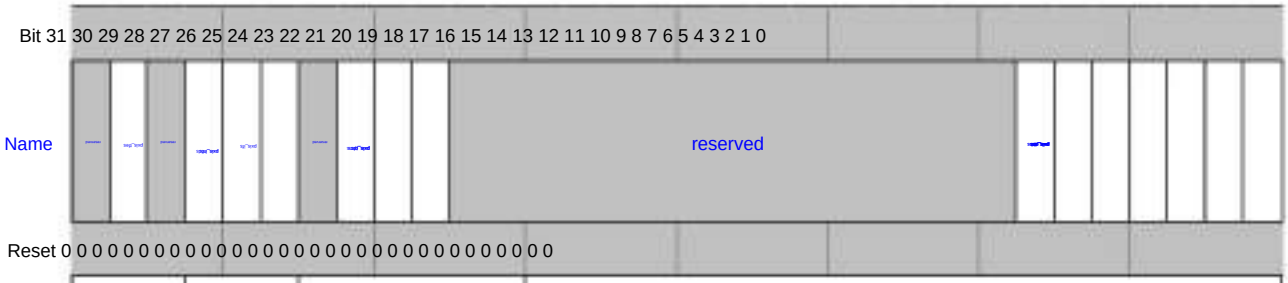
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	port_fb / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:8]	RW	port_fb	Set the base address in the memory where the port receives frames. This register value is not affected when the controller is reset using the SATA_GHC_GHC[hab_rst] bit.
[7:0]	RO	reserved	reserve.

SATA_PORT_IS

SATA_PORT_IS is the port interrupt status register.

Offset Address	Register Name	Total Reset Value
0x010+n x 0x80	SATA_PORT_IS	0x0000_0000



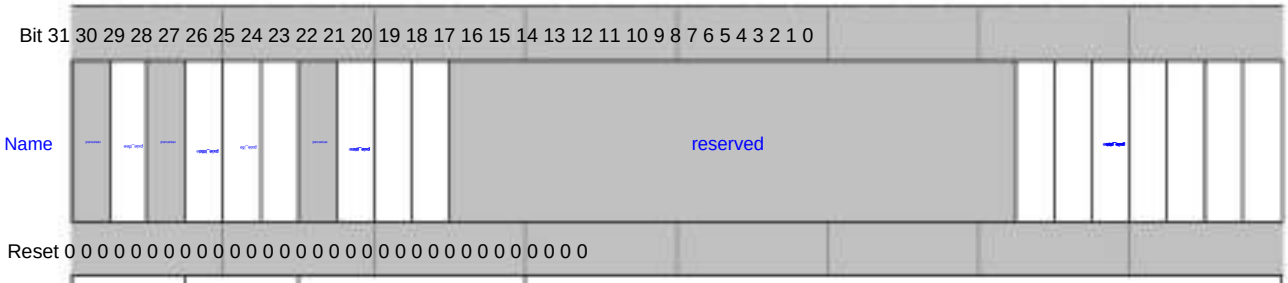
Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	WC	pxis_tfes	TFD error interrupt status. 0: SATA_PORT_TFD bit[0] is not detected to be 1; 1: SATA_PORT_TFD bit[0] is detected to be 1.
[29]	RO	reserved	reserve.
[28]	WC	pxis_hbds	Internal bus error interrupt. 0: DMAC accesses memory normally; 1: DMAC error occurred while accessing memory.
[27]	WC	pxis_ifs	Fatal error interrupt status. 0: No error occurs during data frame transmission; 1: An error occurred during data frame transmission.
[26]	WC	pxis_infs	Non-fatal error interrupt status. 0: No error occurs during non-data frame transmission; 1: Error occurs during non-data frame transmission.
[25]	RO	reserved	reserve.
[24]	WC	pxis_ofs	Data transfer overflow interrupt status. 0: No overflow situation detected; 1: During data frame transmission, if it is detected that the data memory space occupied by the command is less than the actual amount of data to be transmitted, an interruption will be reported at the end of the data transmission.
[23]	WC	pxis_ipms	PM port error interrupt status. 0: PM port number error of received frame not detected; 1: A PM port number error was detected while receiving a frame.
[22]	RO	pxis_prcs	PHY state change interrupt status. 0: No change in phyrdy signal detected; 1: Change in phyrdy signal detected. This bit directly reflects the SATA_PORT_SERR[diag_n] bit.

[21:7] RO		reserved	reserve.
[6]	RO	pxis_pcs	Port connection changes interrupt state. 0: The COMINIT signal sent by the device is not detected; 1: COMINIT signal sent by the device is detected. This bit directly mirrors the SATA_PORT_SERR[diag.x] bit.
[5] WC pxis_dps			The linked list ends the interrupted state. 0: No PRD "I" bit is 1, the data transmission of the linked list is completed; 1: PRD "I" bit is 1, the linked list data has been transmitted normally.
[4]	RO	pxis_ufs	Unknown FIS interrupt status. 0: Unknown FIS not received; 1: Received an Unknown FIS.
[3] WC pxis_sdbs			Set Device Bits FIS interrupt status. 0: no effect; 1: Received a Set Device Bits FIS and the I bit is 1.
[2] WC pxis_dss			DMA Setup FIS interrupt status. 0: meaningless; 1: A DMA Setup FIS was received and the I bit is 1.
[1] WC pxis_pss			PIO Setup FIS interrupt status. 0: meaningless; 1: A PIO Setup FIS was received and the I bit is 1.
[0] WC pxis_drhs			D2H Register FIS interrupt status. 0: meaningless; 1: received a D2H Register FIS, and the I bit is 1.

SATA_PORT_IE

SATA_PORT_IE is the port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x014+n x 0x80	SATA_PORT_IE	0x0000_0000



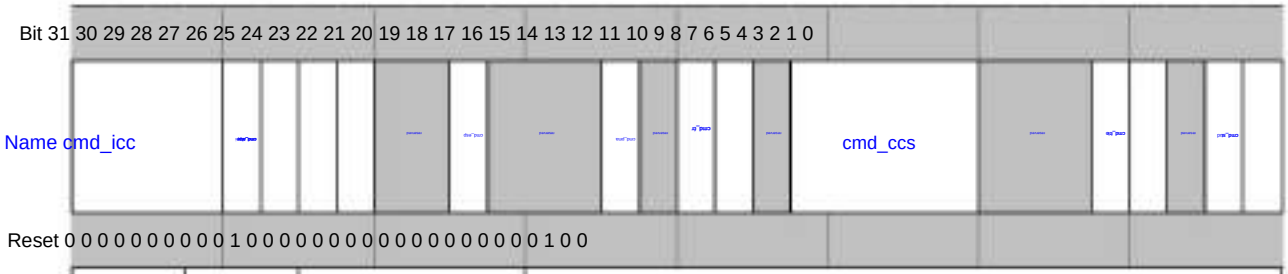
Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	pxie_tfee	TFD error interrupt mask. 0: shielded; 1: No shielding.
[29]	RO	reserved	reserve.
[28]	RW	pxie_hbde	Internal bus error interrupt mask. 0: shielded; 1: No shielding.
[27]	RW	pxie_ife	Fatal errors interrupt masking. 0: shielded; 1: No shielding.
[26]	RW	pxie_infe	Non-fatal error interrupt masking. 0: shielded; 1: No shielding.
[25]	RO	reserved	reserve.
[24]	RW	pxie_ofe	Data transfer overflow interrupt mask. 0: shielded; 1: No shielding.
[23]	RW	pxie_ipme	PM port error interrupt mask. 0: shielded; 1: No shielding.
[22]	RW	pxie_prce	PHY state change interrupt mask. 0: shielded; 1: not shielded.
[21:7]	RO	reserved	reserve.

[6] RW pxie_pce			Port connection change interrupt mask. 0: shielded; 1: No shielding.
[5] RW pxie_dpe			Linked list end interrupt mask. 0: shielded; 1: not shielded.
[4] RW pxie_ufe			Unknown FIS interrupt mask. 0: shielded; 1: No shielding.
[3] RW pxie_sdbe			Set Device Bits FIS interrupt mask. 0: shielded; 1: No shielding.
[2] RW pxie_dse			DMA Setup FIS interrupt mask. 0: shielded; 1: not shielded.
[1] RW pxie_pse			PIO Setup FIS interrupt mask. 0: shielded; 1: No shielding.
[0] RW pxie_drhe			D2H Register FIS interrupt mask. 0: shielded; 1: No shielding.

SATA_PORT_CMD

SATA_PORT_CMD is port command and status register.

Offset Address	Register Name	Total Reset Value
0x018+n x 0x80	SATA_PORT_CMD	0x0020_0004



Bits	Access	Name	Description
[31:28]	RW	cmd_icc	Interface communication control signal. 0x0: No operation, indicating that the next interface status request can be made; 0x1: Request the interface to enter the active state; 0x2: Request the interface to enter the partial state; 0x6: Request the interface to enter the slumber state; Others: Reserved. When the software writes the above non-retained value, the controller will clear cmd_icc to 0 after performing the corresponding operation; when the software requests the interface to enter the state already in, the controller will directly clear cmd_icc to 0; if the software requests the interface to change from a low power consumption mode To enter another low-power mode, such as from partial to slumber, the software should first request the interface to enter the active state from the partial state, and then request the interface to enter the slumber state from the active state.
[27]	RW	cmd_asp	Actively enter the power management Slumber/Partial state selection. 0: Actively enter the partial state; 1: Actively enter the slumber state.
[26]	RW	cmd_alpe	Automatic power management is enabled. 0: forbidden; 1: enable. Once SATA_PORT_CI and SATA_PORT_SACT are cleared to 0, the controller automatically enters the power management state. If cmd_asp is 1, it enters the partial state, and if cmd_asp is 0, it enters the slumber state.
[25]	RW	cmd_dlae	LED driver enable in ATAPI mode. 0: When cmd_atapi is 0, and there is a command being executed, the driving LED pin is valid; 1: As long as there is a command being executed, the driving LED pin is valid.
[24]	RW	cmd_atapi	ATAPI device indication. 0: The current device is a non-ATAPI device; 1: The current device is an ATAPI device.
[23:22]	RO	reserved	reserve.
[21]	RO	cmd_esp	It is always 1, which means it supports External SATA devices.

[20:18] RO		reserved	reserve.
[17] RW	cmd_pma		Port Multipiler device identification indication. 0: The port is not connected to the Port Multipiler device; 1: The port is connected to the Port Multipiler device.
[16] RO		reserved	reserve.
[15] RO		cmd_cr	The command list handles the indication signal. 0: No command is being executed; 1: A command is being executed.
[14] RO		cmd_fr	FIS reception processing indication signal, 0: no FIS reception; 1: Receiving at FIS is in progress.
[13] RO		reserved	reserve.
[12:8] RO		cmd_ccs	Current command slot number. This bit is valid when cmd_st is 1, and cleared to 0 when cmd_st is 0.
[7:5] RO		reserved	reserve.
[4] RW	cmd_fre		FIS receive enable control signal. 0: Disable writing received FIS into system memory; 1: Enable receiving FIS and writing into system memory. The software should set the receiving FIS base address SATA_PORT_FB before enabling this bit to receive FIS; when cmd_st is 1, this bit must be 1.
[3] RW	cmd_clo		Busy/Drq clear control, the software can force clear BSY and DRQ through this bit, and send commands to the device. 0: No effect; 1: Clear the BSY and DRQ bits of the SATA_PORT_TFD[tfd_sts] register, and the bits will be automatically cleared to 0 after BSY and DRQ are 0. This bit can only be written to 1 immediately before cmd_st is set to 1 by 0, and software should ensure that cmd_st is written to 1 after this bit is cleared to 0.
[2]	RO	reserved	reserve.
[1] RW	cmd_sud		Spin-up device control. 0: When SATA_PORT_SCTL[det] is 0, the controller enters the listen mode; 1: After the system is powered on or the HBA is reset, the boot controller sends COMRESET sequence to initialize the hard disk device.

[0] RW	cmd_st		Command list processing enable. 0: Controller enters idle state. 1: The controller starts from slot 0 and processes the commands identified by the SATA_PORT_CI register as valid slots. **cmd_st** can only be set to **1** after **cmd_fre** is 1.

SATA_PORT_TFD

SATA_PORT_TFD is the port task file register.

Offset Address	Register Name	Total Reset Value
0x20+n x 0x80	SATA_PORT_TFD	0x0000_007F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	tfd_err	tfd_sts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RO	tfd_err	task file error register value. The controller updates this register bit when receiving D2H register/PIO setup/ SDB FIS.
[7:0]	RO	tfd_sts	task file status register value. bit[7]: BSY bit, indicating that the device is busy; bit[6:4]: different commands represent different meanings; bit[3]: DRQ bit, indicating that the device has data to be transmitted; bit[2:1]: different The commands have different meanings; bit[0]: ERR bit, indicating that the device made an error during transmission. The controller updates this register bit when receiving D2H register/ PIO setup/SDB FIS.

SATA_PORT_SIG

SATA_PORT_SIG is the port signature register.

Offset Address	Register Name	Total Reset Value
0x24+n x 0x80	SATA_PORT_SIG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	signature																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	signature	LBA address and sector addressing. The specific allocation relationship is as follows: bit[31:24]: LBA high address; bit[23:16]: LBA middle address; bit[15:8]: LBA low address; bit[7:0]: number of sectors. The first D2H register FIS after the hard disk device is reset updates this register.

SATA_PORT_SSTS

SATA_PORT_SSTS is the interface status register.

Offset Address	Register Name	Total Reset Value
0x028+n x 0x80	SATA_PORT_SSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												pxssts_ipm		pxssts_spd		pxssts_it	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RO	pxssts_ipm	Current interface status. 0x0: No device or communication not established; 0x1: in Active state; 0x2: in Partial state; 0x6: in Slumber state; Others: reserved.

[7:4] RO		pxssts_spd	The interface negotiates the speed state. 0x0: No device or communication not established; 0x1: Negotiation uses rate 1 for communication; 0x2: Negotiation uses rate 2 for communication; 0x3: Negotiation uses rate 3 for communication; Others: Reserved.
[3:0] RO		pxssts_it	Device detection and PHY status. 0x0: No device detected and PHY communication not established; 0x1: Device detected but PHY communication not established; 0x3: Device detected and PHY communication established; 0x4: PHY is offline or in BIST state; Others: reserved.

SATA_PORT_SCTL

SATA_PORT_SCTL is the interface control register.

Offset Address	Register Name	Total Reset Value
0x02C+n x 0x80	SATA_PORT_SCTL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	pxsctl_ipm	pxsctl_spd	pxsctl_it
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

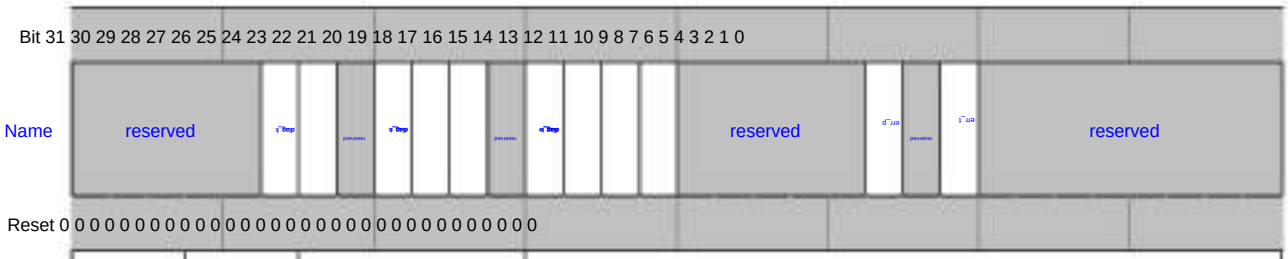
Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	pxsctl_ipm	Interface power management state control. 0x0: No special requirements; 0x1: Forbid to enter Partial state; 0x2: Forbid to enter Slumber state; 0x3: Forbid to enter Partial state or Slumber state; Others: reserved.

[7:4] RW pxsctl_spd			Interface communication speed control. 0x0: No special requirements; 0x1: Speed limit to speed 1 for communication; 0x2: Speed limit to speed 2 for communication; 0x3: Speed limit to speed 3 for communication; Others: Reserved.
[3:0] RW pxsctl_det			Device detection and interface initialization control. 0x0: No device detection or initialization request; 0x1: Request the interface to reset the initialization sequence COMRESET; 0x4: Force the interface to go offline; Others: reserved. When pxsctl_det is set to 1, the controller will send a COMRESET sequence to the device, software should keep this bit as 1 for at least 1ms to ensure that the device receives the COMRESET sequence.

SATA_PORT_SERR

SATA_PORT_SERR is the error diagnosis status register.

Offset Address	Register Name	Total Reset Value
0x30+n x 0x80	SATA_PORT_SERR	0x0000_0000



Bits	Access	Name	Description
[31:27] RO		reserved	reserve.
[26] WC		diag_x	Device detection status. 0: The COMINIT signal sent by the device is not detected; 1: A COMINIT signal from the device is detected.
[25] WC		diag_f	Unknown FIS detection status. 0: Unkonwn FIS not received; 1: Set to 1 when Unkonwn FIS is received and the CRC check is correct.
[24] RO		reserved	reserve.

[23] WC diag_s			Link Link layer error status. 0: There is no state transition error in the link layer; 1: A state transition error occurs at the link layer.
[22] WC diag_h			Handshake error state. 0: No R_ERR primitives from the device are received; 1: One or more R_ERR primitives from the device are received.
[21] WC diag_c			CRC error status. 0: There is no CRC check error in receiving FIS; 1: Receive FIS CRC check error.
[20] RO		reserved	reserve.
[19] WC diag_b			Decoding error status. 0: No 10B to 8B decoding error detected; 1: 10B to 8B decoding error detected.
[18] WC diag_w			COMWAKE state. 0: The COMWAKE signal sent by the device is not detected; 1: A COMWAKE signal from the device is detected.
[17] WC diag_i			PHY internal error status. 0: No PHY internal error detected; 1: A PHY internal error has been detected.
[16] WC diag_n			PhyRdy signal changes state. 0: PhyRdy signal has not changed; 1: PhyRdy signal has changed. Set when the PhyRdy signal changes from 1 to 0 or from 0 to 1.
[15:11] RO		reserved	reserve.
[10] WC err_p			SATA protocol violation error state. 0: The device behavior violates the SATA protocol is not detected; 1: The device behavior violates the SATA protocol is detected.
[9]	RO	reserved	reserve.
[8] WC err_t			Data integrity error status. 0: no data integrity error detected; 1: A data integrity error has been detected.
[7:0] RO		reserved	reserve.

SATA_PORT_SACT

SATA_PORT_SACT identifies the control register for the NCQ command.

Offset Address	Register Name	Total Reset Value
0x034+n x 0x80	SATA_PORT_SACT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_sact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_sact	The NCQ command identifies the control register. Each bit of this register corresponds to a tag number and an NCQ command in the memory, and bit[31:0] corresponds to the command of slot31~0 and tag31~0 respectively. Take bit[3] as an example, the specific meaning of each bit: 0: the slot3 command is a non-NCQ command; 1: the slot3 command is an NCQ command. The software should set bit[3] of this register before setting bit SATA_PORT_CI[3]. After the command data transmission is completed, the device will send a SDB FIS, and the controller will clear bit[3] according to SActive in FIS. Software can only set this register when cmd_st is 1, and clear all 0 when cmd_st is 0.

SATA_PORT_CI

SATA_PORT_CI is the command sending control register.

Offset Address	Register Name	Total Reset Value
0x38+n%0x80	SATA_PORT_CI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_ci																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	port_ci	Command pending send control. Each bit of this register represents a command in the memory, and bit[31:0] corresponds to the commands of slot31~0 respectively. Take bit[3] as an example, the specific meaning of each bit: 0: slot3 has no command waiting to be sent and executed; 1: The slot3 command has been established in the memory, and the controller can send this command; when the controller finishes executing the command, receives the corresponding FIS and clears the BSY, DRQ, and ERR bits of the SATA_PORT_TFD register, the bit will also be cleared at the same time [3]. Each bit of this register can only be set when cmd_st is 1, and all cleared to 0 when cmd_st is 0.

SATA_PORT_SNTF

SATA_PORT_SNTF is an asynchronous notification event indication register.

Offset Address	Register Name	Total Reset Value
0x3C+n x 0x80	SATA_PORT_SNTF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														pxsntf_pmn	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	WC	pxsntf_pmn	Asynchronous notification event status. If the controller receives the SDB FIS of the device on the PM, and the "N" bit of the FIS is 1, it will set the corresponding register bit position of the PM port number of the device to 1. Take bit[3] as an example, the specific meaning of each bit: 0: No asynchronous notification event occurs on the device with PM port number 3; 1: The device with PM port number 3 has an asynchronous notification event.

SATA_PORT_FIFOTH

SATA_PORT_FIFOTH is the receive FIFO watermark register.

Offset Address	Register Name	Total Reset Value
0x044+n x 0x80	SATA_PORT_FIFOTH	0x0000_0F24

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dmac_rxfifo_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 0 0 1 0 0

Bits	Access	Name	Description
[31:9]	RW	reserved	reserve.
[8:4]	RW	dmac_rxfifo_th	DMAC receive FIFO flow control pipeline. When receiving data, if the amount of DMAC FIFO data exceeds this value, the controller starts flow control.
[3]	RW	rxfifo_th_sel	Flow control FIFO selection. 0: link receive FIFO flow control is valid; 1: DMAC receive FIFO flow control is valid.
[2:0]	RW	link_rxfifo_th	link Receive FIFO flow control pipeline. When receiving data, if the amount of DMAC FIFO data exceeds this value, the controller starts flow control.

SATA_PORT_HBA

SATA_PORT_HBA is the HBA test status register.

Offset Address	Register Name	Total Reset Value
0x050+n x 0x80	SATA_PORT_HBA	0x0100_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved p_curr_st ndr_curr_st cfis_curr_st
Reset	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

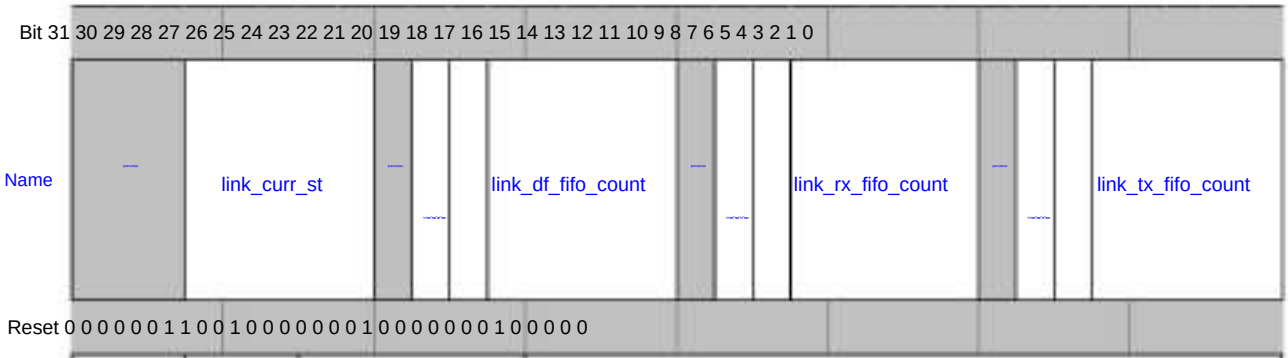
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27:24] RO		p_curr_st	HBA_PINIT_STATE The current state of the state machine.
[23:21] RO		reserved	reserve.
[20:16] RO		ndr_curr_st	HBA_NDR_STATE The current state of the state machine.
[15:12] RO		cfis_curr_st	HBA_CFIS_STATE The current state of the state machine.
[11] RO		reserved	reserve.
[10:8] RO		pio_curr_st	HBA_PIO_STATE The current state of the state machine.
[7]	RO	reserved	reserve.
[6:4] RO		pm_curr_st	HBA_PM_STATE The current state of the state machine.
[3]	RO	reserved	reserve.
[2:0] RO		err_curr_st	HBA_ERR_STATE The current state of the state machine.

SATA_PORT_LINK

SATA_PORT_LINK is Link test status register.

Offset Address	Register Name	Total Reset Value
0x054+n x 0x80	SATA_PORT_LINK	0x0020_2020



Bits	Access	Name	Description
[31:29] RO		reserved	reserve.
[28:24] RO		link_curr_st	LINK_CTL_STATE The current state of the state machine.
[23] RO		reserved	reserve.
[22] RO		link_df_fifo_full	Link Suppression FIFO full flag. 0: FIFO is not full; 1: FIFO is full.

[21] RO		empty; link_df_fifo_empty	Link Suppression FIFO empty flag. 0: FIFO is not 1: FIFO empty.
[20:16] RO		link_df_fifo_count	Link frequency elimination FIFO data volume.
[15] RO		reserved	reserve.
[14] RO		link_rx_fifo_full	Link receive FIFO full flag. 0: FIFO is not full; 1: FIFO is full.
[13] RO		link_rx_fifo_empty	Link receive FIFO empty flag. 0: FIFO non-empty; 1: FIFO empty.
[12:8] RO		link_rx_fifo_count	Link receive FIFO data amount.
[7]	RO	reserved	reserve.
[6]	RO	link_tx_fifo_full	Link sends FIFO full flag. 0: FIFO is not full; 1: FIFO is full.
[5]	RO	link_tx_fifo_empty	Link sends FIFO empty flag. 0: FIFO non-empty; 1: FIFO empty.
[4:0] RO		link_tx_fifo_count	Link transmit FIFO data volume.

SATA_PORT_DMA1

SATA_PORT_DMA1 is DMAC test status register 1.

Offset Address	Register Name	Total Reset Value
0x058+n x 0x80	SATA_PORT_DMA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_entry_dbc_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RO	txdmac_cur_state	SATA_TX_DMAC state machine current state.
[23]	RO	txdmac_prd_i	The "I" bit in the entry of the PRD linked list in SATA_TX_DAMC.
[22:0]	RO	tx_entry_dbc_cnt	The decrement counter in SATA_TX_DMAC is the number of data bytes in the currently used Entry.

SATA_PORT_DMA2

SATA_PORT_DMA2 is DMAC test status register 2.

Offset Address	Register Name	Total Reset Value
0x05C+n x 0x80	SATA_PORT_DMA2	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_data_fis_cnt								tx_cmdh_prdtl							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:8]	RO	tx_data_fis_cnt	The decrement counter in SATA_TX_DMAC indicates the number of Data FIS bytes during PIO, Legacy DMA, and First Party DMA operations. During PIO operation, its initial value is transcount in PIO Setup; during Legacy DMA or First Party DMA operation, its initial value is 16'h2000 (2048DWORD).
[7:0]	RO	tx_cmdh_prdtl	The decrement counter in SATA_TX_DMAC and the parameter in Command Header indicate how many Entries there are in PRDT.

SATA_PORT_DMA3

SATA_PORT_DMA3 is DMAC test status register 3.

Offset Address	Register Name	Total Reset Value
0x060+n x 0x80	SATA_PORT_DMA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_fpdma_tran_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	tx_fpdma_tran_cnt in DMA setup	The decrement counter in SATA_TX_DMAC indicates the number of Data FIS bytes during First Party DMA operation. Its initial value is transcountÿ

SATA_PORT_DMA4

SATA_PORT_DMA4 is DMAC test status register 4.

Offset Address	Register Name	Total Reset Value
0x064+n x 0x80	SATA_PORT_DMA4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rxdmac_cur_state				rxdmac_prd_i	rx_entry_dbc_cnt																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:28] RO	reserved	reserve.
[27:24] RO	rxdmac_cur_state	SATA_RX_DMAC current state machine signal.
[23] RO	rxdmac_prd_i	The "I" bit in the entry of the PRD linked list in SATA_RX_DAMC.
[22:0] RO	rx_entry_dbc_cnt	The decrement counter in SATA_RX_DMAC is the number of data bytes in the currently used Entry.

SATA_PORT_DMA5

SATA_PORT_DMA5 is DMAC test status register 5.

Offset Address	Register Name	Total Reset Value
0x068+n x 0x80	SATA_PORT_DMA5	0x0020_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	rx_data_fis_cnt	rx_cmdh_prdtl
Reset	0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:8]	RO	rx_data_fis_cnt	The decrement counter in SATA_RX_DMAC indicates the number of Data FIS bytes during PIO, Legacy DMA, and First Party DMA operations. During PIO operation, its initial value is transcount in PIO Setup; during Legacy DMA or First Party DMA operation, its initial value is 0x2000 (2048DWORD).
[7:0]	RO	rx_cmdh_prdtl	The decrement counter in SATA_RX_DMAC, the parameter in Command Header, indicates how many Entries there are in PRDT.

SATA_PORT_DMA6

SATA_PORT_DMA6 is DMAC test status register 6.

Offset Address	Register Name	Total Reset Value
0x6C+n x 0x80	SATA_PORT_DMA6	0x0000_0000

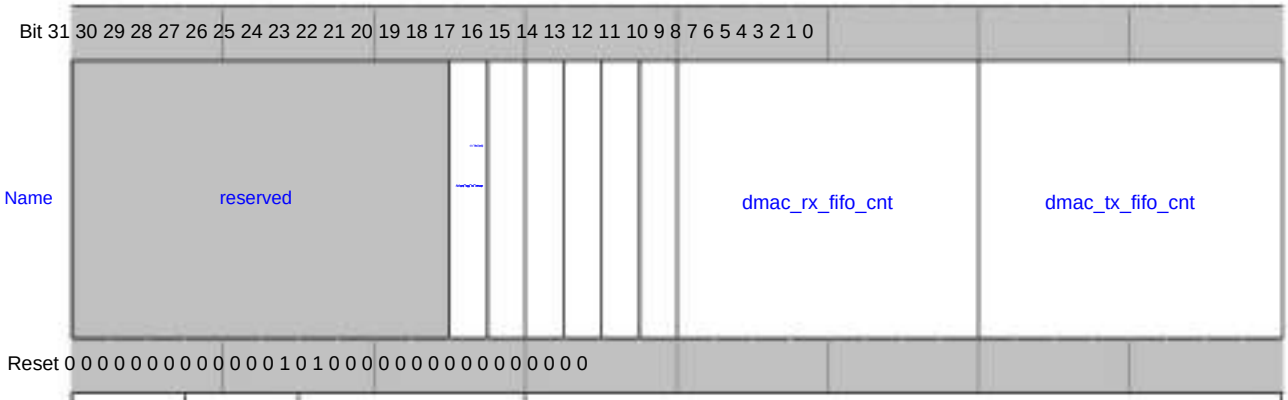
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_fpdma_tran_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rx_fpdma_tran_cnt	The decrement counter in SATA_RX_DMAC indicates the number of Data FIS bytes during First Party DMA operation. Its initial value is the value of transcount in DMA Setup.

SATA_PORT_DMA7

SATA_PORT_DMA7 is DMAC test status register 7.

Offset Address	Register Name	Total Reset Value
0x070+n x 0x80	SATA_PORT_DMA7	0x0005_0000

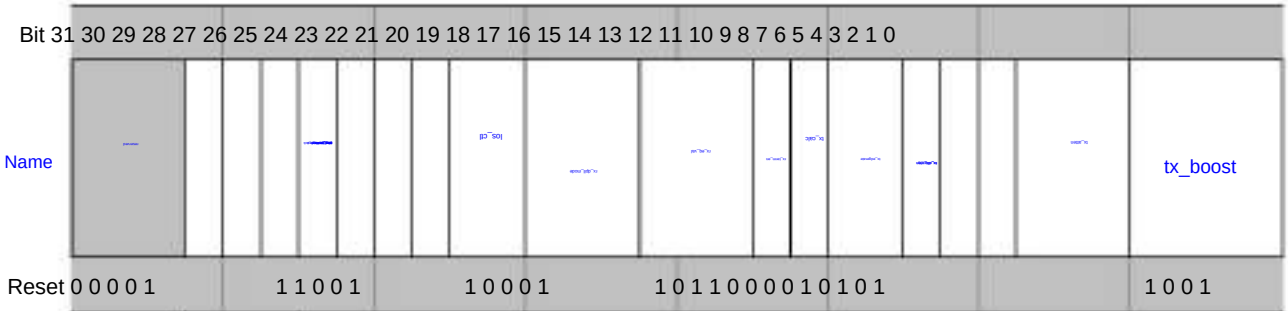


Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RO	pio_op	PIO operation instructions. 0: The current command is not a PIO operation; 1: The current command is a PIO operation.
[20]	RO	fpdma_op	First Party DMA operation instruction. 0: The current command is not a First Party DMA operation; 1: The current command is a First Party DMA operation.
[19]	RO	dmac_rx_fifo_full	SATA_DMAC_RX_FIFO full status. 0: FIFO is not full; 1: FIFO is full.
[18]	RO	dmac_rx_fifo_empty	SATA_DMAC_RX_FIFO empty status. 0: FIFO is not empty; 1: FIFO empty.
[17]	RO	dmac_tx_fifo_full	SATA_DMAC_TX_FIFO full status. 0: FIFO is not full; 1: FIFO is full.
[16]	RO	dmac_tx_fifo_empty	SATA_DMAC_TX_FIFO empty status. 0: FIFO is not empty; 1: FIFO empty.
[15:8]	RO	dmac_rx_fifo_cnt	The number of data in SATA_DMAC_RX_FIFO, the unit is DWORD.
[7:0]	RO	dmac_tx_fifo_cnt	The number of data in SATA_DMAC_TX_FIFO, the unit is DWORD.

SATA_PORT_PHYCTL

SATA_PORT_PHYCTL is the PHY control register.

Offset Address	Register Name	Total Reset Value
0x074+n x 0x80	SATA_PORT_PHYCTL	0x0E63_6159



Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28]	RW	phy_disable	Whether to use PHY. 0: use PHY; 1: PHY is not used.
[27]	RW	phy_calibrated	Whether to calibrate the PHY. 0: no calibration; 1: Calibration.
[26]	RW	spd_change_ack	Whether rate switching is allowed. 0: Speed switching is not allowed; 1: Allow speed switching.
[25]	RW	dp_rdy	Whether the PHY is ready to send data. 0: not ready; 1: ready.
[24]	RW	bis_tx_fspd	BIST mode forces the transmit clock frequency. 0: no force; 1: Forced.
[23]	RW	neg_mode_b	Negotiation mode B is selected. 0: Not supported; 1: Supported.
[22]	RW	gen2_en	Send control signal, whether to allow 3G mode. 0: Does not support 3G mode; 1: Support 3G mode.

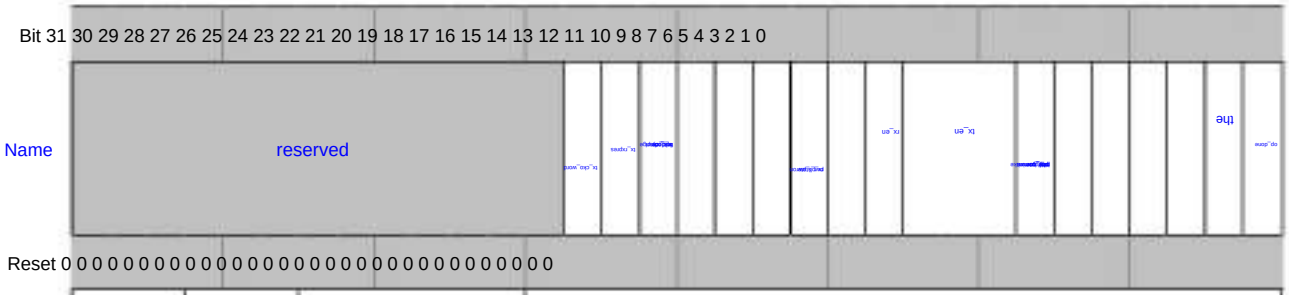
[21:20]	RW	los_ctl	LOS detection control. 00: LOS detection off; 01: Reserved; 10: OOB signal detection; 11: Reserved.
[19:17]	RW	rx_dpll_mode	Receive dpll control mode. 000: indicates that PHUG is 1 and FRUG is 1; 001: indicates that PHUG is 2 and FRUG is 2; 010: means PHUG is 1, FRUG is 4; 011: means PHUG is 2, FRUG is 4; Other: reserved.
[16:14]	RW	rx_eq_val	Receive equalization control. Indicates that the internal equilibrium value is ~(rx_eq_val + 1)x 0.5dBÿ
[13]	RW	rx_term_en	Receive Terminate enable. 0: forbidden; 1: enable.
[12]	RW	tx_calc	This bit is not used and is forced to 0.
[11:10]	RW	tx_edgerate	Transmit signal edge control. The default is 0x0.
[9]	RW	tx_cko_en	tx_cko_clk Clock enable. 0: forbidden; 1: enable.
[8]	RW	rx_align_en	Receive data alignment. 0: Does not support receive data alignment; 1: Support receive data alignment.
[7]	RW	tx_clk_align	Transmit clock alignment. 0: not aligned; 1: align.
[6:4]	RW	tx_atten	Send attenuation control. 000ÿ16/16ÿ 001ÿ14/16ÿ 010ÿ12/16ÿ 011ÿ10/16ÿ 100ÿ9/16ÿ 101ÿ8/16ÿ 11X: reserved.

[3:0]	RW	tx_boost	Send boost control. The value is -20log(1-(tx_boost[3:0]+0.5)/32) dBÿ

SATA_PORT_PHYSTS

SATA_PORT_PHYSTS is the PHY test status register.

Offset Address	Register Name	Total Reset Value
0x078+n x 0x80	SATA_PORT_PHYSTS	0x0000_0000



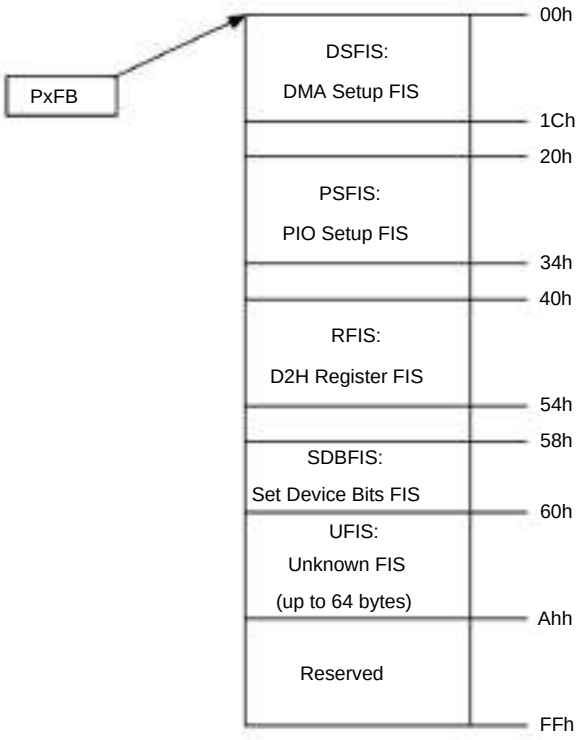
Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RW	tx_cko_word	Receive word clock of each lane, not used for now.
[17]	RW	tx_rxpres	Acceptance test, not used for now.
[16]	RW	tx_done	The operation of sending part of the request has been completed, high effective, and not used for now.
[15]	RW	spd_change	Required change rate, high effective.
[14]	RW	link_rdy	When high indicates that enough D10.2 is sent.
[13]	When RW	init_compl	is high, it means that a non-ALIGN primitive is received and the initialization is completed.
[12]	RW	pwr_state	If it is 1, it means it is in low power consumption mode (partial or slumber), otherwise it means it is in Active state.
[11]	RW	rx_pll_pwron	Receive PLL power-on control signal.
[10]	RW	rx_en	The rx_en signal controls the state.
[9:7]	RW	tx_en	The tx_en signal controls the state.
[6]	RW	mpll_pwron	MPLL power-on control signal.
[5]	RW	phy_comwake	PHY detects COMWAKE, active high.
[4]	RW	phy_cominit	PHY detects COMINIT, active high.
[3]	RW	half_rate	When it is 1, it only supports 1.5G rate.
[2]	RW	phyrdy	The PHY has been initialized and can communicate with the LINK layer, high effective.
[1]	RW	los	Loss of Signal Output, active high.

[0] RW op_done			The operation requested by the MPLL has completed, active high.

14.7.8 Appendix A SATA command list format

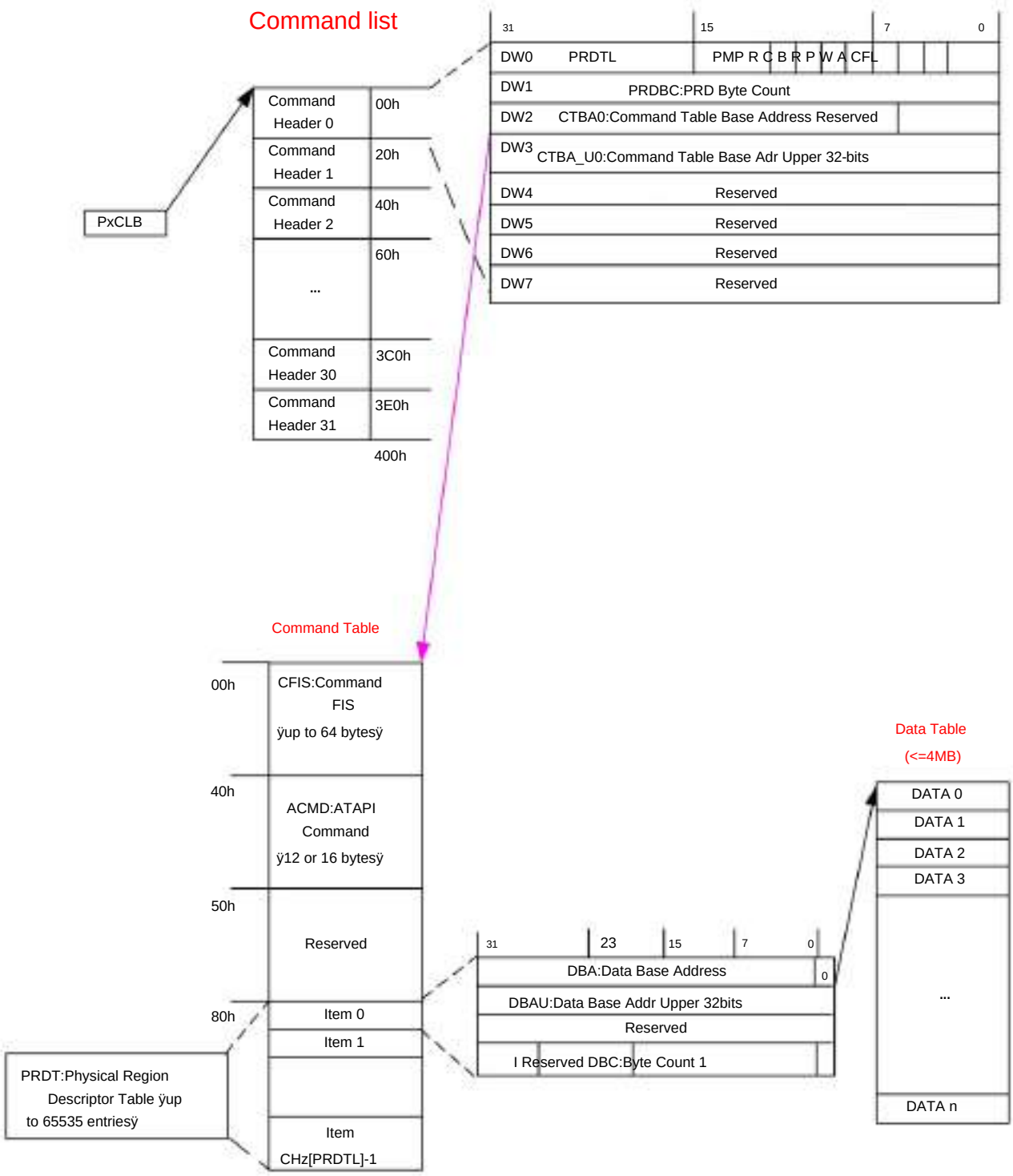
The structure of the FIS linked list is shown in Figure 14-45 . This linked list is a section of space created by the software in the system memory. The base address of the linked list is stored in the PxFB and PxFBU registers in the AHCI register group. The DMAC uses this base address as the destination address to receive The different frames received are moved to different memory spaces.

Figure 14-45 Linked list structure



The structure of the command and data linked list is shown in Figure 14-46 . This linked list is a space opened by the software in the system memory. The Command list includes at most 32 commands. The base address of the Command list is specified by the PxCLB and PxCLBU registers in AHCI. Each command includes a Command Header, in which the content of CTBA0 specifies the base address of the Command Table, which includes the command to be read and the data space linked list for reading and writing.

Figure 14-46 Command and data linked list structure



Each time before the command is executed, the above two linked lists need to be established in the memory. For the specific meaning of the linked list, please refer to the AHCI1.2 protocol. The CFIS area is the H2D Register FIS, and the specific content refers to the SATA2.5 protocol. The ACMD area is the command content of the ATAPI operation. For details, refer to the SSF (Small Form Factor Committee) protocol description for DVD Devices and CD-ROMs.

14.8 PWM

14.8.1 Overview

Hi3520D provides 1 independent PWM signal output.

14.8.2 Features

For each PWM output:

3MHz and 24MHz clock sources are selectable.

Internal 26bit counter, output cycle can be configured. Support up to 12MHz (24MHz/2) output, minimum about 0.045Hz (3MHz/67108863) output. The number of high

levels is configurable in 26 bits.

Internal 10bit counter, the number of output pulses (up to 1023) can be configured. Can support unlimited pulse output.

14.8.3 Working method

The PWM works internally at 3MHz or 24MHz, and the PWM output configuration process is as follows:

1. Select an appropriate clock source, and obtain the required number of cycles and high levels by calculation.
2. Write the corresponding data into the PWM0_CFG0, PWM0_CFG1, PWM0_CFG2 registers.
3. Write 1 to PWM0_CTRL bit[0] to enable PWM output.

----Finish

For example: It is necessary to output a waveform with a frequency of 3KHz, a high level of 72.5% (that is, a duty cycle), and a pulse number of 10.

Select the 3MHz clock as the clock source, and configure the number of cycles as 3MHz /1KHz=1000, which is 1000 after rounding, and the hexadecimal value is 0x00003E8. The number of high levels is configured as 1000 (number of cycles) x 72.5% (duty cycle) = 725, which is 725 after rounding, and the hexadecimal value is 0x00002D5.

Follow the steps below to operate the registers to output the required waveform:

1. Write 0x2 to PERI_CRG14, select the PWM clock source as 3MHz, and turn on the PWM clock.
2. Read PWM0_STATE2 bit[10], and wait for bit[10] to be 0 (indicating PWM is idle and can output square wave)
3. Write 0x0000_03E8 to PWM0_CFG0 .
4. Write 0x0000_02D5 to PWM0_CFG1 .
5. Write 0x0000_000a to PWM0_CFG2 .
6. Write 0x1 to PWM0_CTRL . (The following steps can be omitted, just to verify whether the square wave being output output by configuration)
7. Read PWM0_STATE2 bit[10], wait for bit10 to be 1 (indicating that PWM is outputting square wave)
8. Read PWM0_STATE0 and 0x0000_03E8 for verification.

9. Read PWM0_STATE1 and 0x0000_02D5 for verification.
10. Read PWM0_STATE2 bit[9:0] and 0x0A for verification (when bit[10] is 1, it means that PWM is outputting a square wave, when this bit is 0, it means that the set number of square waves has been output).

----Finish

14.8.4 Register overview

An overview of the PWM registers is shown in Table 14-16 .

Table 14-16 PWM register overview (base address is 0x2012_0000)

offset address name	describe	page number
0x0000 PWM0_CFG0	Configuration 0 Register for PWM0	14-141
0x0004 PWM0_CFG1	Configuration 1 Register for PWM0	14-142
0x0008 PWM0_CFG2	Configuration 2 Register for PWM0	14-142
0x000C PWM0_CTRL	Control register for PWM0	14-142
0x0010 PWM0_STATE0	Status 0 Register for PWM0	14-143
0x0014 PWM0_STATE1	Status 1 Register for PWM0	14-144
0x0018 PWM0_STATE2	Status 2 Register for PWM0	14-144

14.8.5 Register Description

PWM0_CFG0

PWM0_CFG0 is the configuration 0 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	pwm0_period
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 0 0 0 1 1 1

Bits	Access	Name	Description
[31:26]	-	reserved	reserve.
[25:0]	RW	pwm0_period	The period number of PWM0. Cannot be configured as 0 and 1, when it is 0 or 1, it will output high level.

PWM0_CFG1

PWM0_CFG1 is the configuration 1 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / pwm0_duty
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 1 1

Bits	Access	Name	Description
[31:26]	-	reserved	reserve.
[25:0]	RW	pwm0_duty	If the number of high-level beats of PWM0 is greater than or equal to the number of cycles, the output will always be high-level.

PWM0_CFG2

PWM0_CFG2 is the configuration 2 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / pwm0_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	-	reserved	reserve.
[9:0]	RW	pwm0_num	The number of square waves output by PWM0.

PWM0_CTRL

PWM0_CTRL is the control register of PWM0.

Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:3]		reserved	reserve.
[2]	RW	pwm0_keep	PWM output mode. 0: PWM0 outputs a fixed number of square waves; 1: PWM0 outputs square wave all the time.
[1]	RW	pwm0_inv	PWM output positive and negative phase control. 0: PWM0 outputs square wave normally; 1: PWM0 inverts and outputs a square wave.
[0]	RW	pwm0_enable	PWM enable control. 0: PWM0 module is off; 1: PWM0 module is enabled.

PWM0_STATE0

PWM0_STATE0 is the state 0 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						pwm0_period_st																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:26]	-	reserved	reserve.
[25:0]	RO	pwm0_period_st	The number of counting periods used by the internal modules of PWM0.

PWM0_STATE1

PWM0_STATE1 is the state 1 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / pwm0_duty_st
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:26]	-	reserved	reserve.
[25:0]	RO	pwm0_duty_st	The number of high-level pulses used by internal modules of PWM0.

PWM0_STATE2

PWM0_STATE2 is the state 2 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / pwm0_cnt_st / pwm0_keep_st / pwm0_busy / pwm0_period_st
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:22]	-	reserved	reserve.
[21:12]	RO	pwm0_cnt_st	The PWM0 module also needs to output the number of square waves. Only meaningful when pwm0_busy==1, pwm0_keep_st==0.
[11]	RO	pwm0_keep_st	The internal module of PWM0 adopts the output square wave mode. 0: output a fixed number of square waves; 1: Output square wave all the time.
[10]	RO	pwm0_busy	Working status of PWM0 module. 0: idle, output completed; 1: A square wave is being output.

[9:0] RO		pwm0_period_st The number of output square waves used by internal modules of PWM0.	

A Acronym

A

ABR	Average Bit Rate	average bit rate
ACD	Auto Command Done	Auto stop command completed
BUT	Auto Exposure	automatic exposure
AES	Advanced Encryption Standard	Advanced Encryption Standard
OF	Auto Focus	auto focus
AHB	Advanced High-performance Bus	-
BROAD	Advanced Microcontroller Bus Architecture Advanced Microprocessor Bus Architecture	
ARM	ARM	ARM's RISC Core
ATF	Adaptive Temporal Filter	adaptive temporal filtering
AWB	Auto White Balance	auto white balance

B

BTF	Brute Force Temporal Filter	forced temporal filtering
BVACT	Bottom Vertical Active Area	Effective area of bottom field vertical activities
BVBB	Bottom Vertical Back Blank	Blanking after bottom field vertical
BVFB	Bottom Vertical Front Blank	Bottom field vertical pre-blanking

C

CBC	Cipher Block Chaining	cipher block chaining
CBR	Constants Bit Rate	fixed bit rate
CCITT	International Telegraph and Telephone Consultative Committee	International Telegraph and Telephone Consultative Committee

CD	Command Done	command completed
CFB	Cipher Feedback	password feedback
CL	CAS Latency	read latency
CPU	Central Processing Unit	central processing unit
CRC	Cyclic Redundancy Check	Cyclic Redundancy Check
CRG	Clock Reset Generation	Clock reset generation module
CTR	Counter	counter
CVBS	Composite Video Broadcast Signal	composite video broadcast signal
D		
DCRC	Data CRC Error	Data CRC error
DDR	Double Data-Rate	double data rate
OF THE	De-Interlace	Deinterlacing/Deinterlacing
OF THE	Data Encryption Standard	Data Encryption Standard
DFT	Design For Test	Design for Testability
DIS	Digital Image Stabilization	digital image stabilization
DLL	Delay Locked Loop	delay locked loop
DMA	Direct Memory Access	direct memory access
DMAC	Direct Memory Access Controller	direct memory access controller
DNR	Digital Noise Reduction	digital denoising
DQS	Data Strobe	data strobe
DRC	Dynamic Range Compression	dynamic range compression
VINE	Data Read Timeout	data read timeout
DTO	Data Transfer Over	data transfer complete
DVR	Digital Video Recorder	digital video recorder
AND		
WHERE	End-bit error	end bit error
FAMILY	External Bus Interface	External bus interface
ECB	Electronic Codebook	electronic password book
EOF	End Of Frame	end of frame

EOP	End Of Packet	end of package
ETH	Ethernet MAC	Ethernet interface
F		
FIFO	First In First Out	first in first out
FIQ	Fast Interrupt Request	fast interrupt request
MRS	FIFO Underrun/Overrun Error	FIFO overflow error
G		
GPIO	General Purpose Input/Output	General purpose input/output
H		
HACT	Horizontal Active Area	Horizontal active area
HBB	Horizontal Back Blank	Blanking after level
HCCA	Host Controller Communication Area Host Controller Communication Area	
HFB	Horizontal Front Blank	Blanking before horizontal
PLEASE	Hardware Locked Error	hardware lock error
HPW	Horizontal Pulse Width	Horizontal pulse width
HTO	Data starvation-by-host timeout	Controller read and write data timeout
I		
2C	Inter-Integrated Circuit	A serial bus protocol standard
I2S	Inter-IC Sound	I2S audio input and output interface
IE	Image Enhancement	image enhancement
IEC	International Electrotechnical Commission International Electrotechnical Commission	
IEEE	Institute of Electrical and Electronics Engineers	Institute of Electrical and Electronics Engineers
IPVS	IP Video Surveillance	Network Video Surveillance System
AND	Infrared Remoter	Infrared remote control interface
IRQ	Interrupt Request	interrupt request
ISO	International Standard Organization	International Organization for Standardization
ISP	Image Signal Processing	Image Signal Processing

ISR	Interrupt Service Routine	interrupt service routine
ITCM	Instruction TCM	Instruction Tightly Coupled Memory
IT-T	International Telecommunication Union - Telecommunication Standardization Sector	International Telecommunication Union - Telecommunication Standards Sector
IV	Initialization Vector	initial vector
J		
JTAG	Joint Test Action Group	Joint Test Action Team
L		
LSB	Least Significant Bit	end bit
ACCESS	Lookup Table	lookup table
M		
MAC	Media Access Control	media access control
MCU	Micro Controller Unit	micro control unit
MEDIUM	Management Data Input/Output	Control data input and output interface
THOUSAND	Media Independent Interface	media independent interface
MMC	Multi-media Card	multimedia card
MSB	Most Significant Bit	start bit
N		
NTSC	National Television Systems Committee National Television System	Committee (a TV broadcasting transmission system based on the principle of "quadrature balanced amplitude modulation")
NVR	Net Video Recorder	network video recorder
O		
OFB	Output Feedback	output feedback
OHCI	Open Host Controller Interface	Expose the host controller interface
OSD	On Screen Display	Screen video control system
OTG	On-The-Go	-

P

PAL	Phase Alternating Line	Progressive phase inversion (it is a TV broadcast transmission system whose principle is "progressive phase inversion quadrature balanced amplitude modulation system")
PCB	Printed Circuit Board	A printed circuit board
PCI	Peripheral Component Interconnect	A common local bus
PCM	Pulse Code Modulation	pulse code modulation
PID	Packet ID	Package ID
PIP	Picture In Picture	picture in picture
PSRAM	Pseudo Static Random Access Memory Pseudo-static random access memory	

Q

QXGA	Quantum Extended Graphics Array	Quantum Extended Graphics Array (is a standard format for displaying computer graphics)

R

RAM	Random-Access Memory	random access memory
RCRC	Response CRC error	Response to CRC errors
RE	Response error	response error
ROM	Read Only Memory	ROM
ROP	Raster Operation	raster operations
RTO	Response Timeout	response timeout
RXDR	Receive FIFO data request	Receive FIFO data request

s

SAD	Sum Of Absolute Difference	Image Absolute Error and
SBE	Start-bit Error	start bit error
SCL	Serial Clock	serial clock
SCR	System Clock Reference	System Clock Reference
SD	Secure Digital	safe numbers
SDA	Serial Data	serial data
SDIO	secure digital Input/Output	Safe digital input and output interface
SDRAM	Synchronous Dynamic Random Access Synchronous Dynamic Random Access Memory	

	Memory	
SF	Spacial Filter	spatial filtering
SFD	Start of Frame Delimiter	frame preamble
AND	Specific Information	specific information
NOT	Sonic Input/Output	Audio input and output interface
SMI	Static Memory Interface	static memory interface
SOF	Start Of Frame	start frame
SPI	Synchronous Peripheral Interface	Synchronous Peripheral Interface
SRAM	Static Random Access Memory	SRAM
SSP	Synchronous Serial Port	Synchronous serial port
T		
TCM	Tightly-Coupled Memory	tightly coupled memory
TDE	Two Dimension Engine	2D engine
TVACT	Top Vertical Active Area	Effective area of vertical activities in the top field
TVBB	Top Vertical Back Blank	Top Field Vertical Back Blanking
TVFB	Top Vertical Front Blank	Front vertical front consumption
TXDR	Transmit FIFO Data Request	Send FIFO data request
IN		
UART	Universal Asynchronous Receiver Transmitter	Universal Asynchronous Transceiver
USB	Universal Serial Bus	Universal Serial Bus
IN		
VACT	Vertical Active Area	Effective vertical area
VBB	Vertical Back Blank	Blanking after vertical
VBI	Vertical Blanking Interval	vertical blanking interval
VBR	Variable Bit Rate	dynamic bit rate
OURS	Video Encode Unit	video coding unit
VFB	Vertical Front Blank	Vertical front consumption
VGA	Video Graphics Array	Video Graphics Array

IT SAW	Video Input Unit	video input unit
VLC	Variable Length Coding	variable length encoding
I GO	Video Output Unit	video output unit
VPP	Video Pre-processing	Video pre-processing
VPW	Vertical Pulse Width	vertical pulse width

B Ordering Information

The Hi3520D chip identification is shown in Figure B-1 . The Hi3515A chip identification is shown in Figure B-2 .

Figure B-1 Hi3520D chip identification

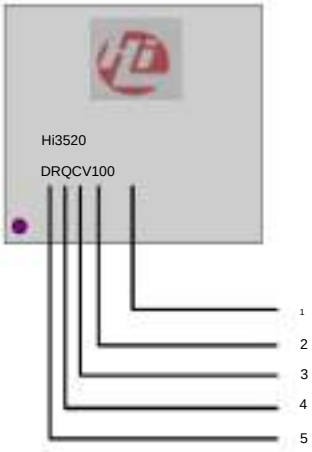
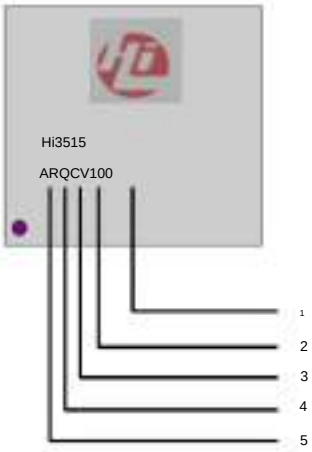


Figure B-2 Hi3515A chip identification



The Hi3520D and Hi3515A chip identification definitions are shown in Table B-1 .

Table B-1 Hi3520D chip identification definition

ID number		meaning
1 version number		Chip version number
2 temperature marking		C: Commercial (commercial supplies)
3 Package marking		QÿQFP
4 Environmental label		RÿRoHS
5 product classification		The last digit of the chip product name is the product area digit. This bit is optional, if this bit is empty, the content on the right will be shifted to the left.