Yayi Technology—[Embedded Smart Connected Device] software and hardware solution provider. Focus on [remote network video surveillance system] R & D and design. For more information, visit: http://www.travellinux.com.

Hi3519V100 Professional HD IP Camera Soc

user guide

Document version 00B07

Release date 2016-06-30

Trademark Statement

, HiSilicon and other HiSilicon trademarks are trademarks of Shenzhen HiSilicon Semiconductor Co., Ltd.

All other trademarks or registered trademarks mentioned in this document are owned by their respective owners.

Note

that the products, services or features you purchase shall be subject to HiSilicon's commercial contracts and terms, and all or part of the products, services or features described in this document may not be within the scope of your purchase or use. Unless otherwise agreed in the contract, HiSilicon does not make any express or implied representations or guarantees for the contents of this document.

Due to product version upgrades or other reasons, the content of this document will be updated from time to time. Unless otherwise agreed, this document is only used as a guide, and all statements, information and suggestions in this document do not constitute any express or implied guarantee.

Shenzhen Hisilicon Semiconductor Co., Ltd.

address:	Huawei Electrical Production Center, Huawei Base, Bantian, Longgang District, Shenzhen Postcode: 518129
URL:	http://www.hisilicon.com
customer service number:	+86-755-28788858
Customer Service Fax:	+86-755-28357515
Customer Service Email:	support@hisilicon.com

Table of contents

foreword

overview

This document introduces the characteristics and logical structure of the Hi3519V100 chip, describes in detail the functions, working methods, and definitions of related registers of each module, gives the interface timing relationship and related parameters in the form of diagrams, and describes in detail the chip's pin definitions and Uses and chip performance parameters and package sizes.

product version

The product versions corresponding to this document are as follows.

product name	product version
Hi3519	V100

Readers

This document is primarily intended for the following engineers:

Electronic product design and maintenance personnel

Electronic product component market salesperson

convention symbol convention

The following symbols may appear in this document, and their meanings are as follows.

symbol	illustrate
 危险	Text beginning with this symbol indicates a hazard with a high level of potential which, if not avoided, will result in death or serious injury.

symbol	illustrate
警告	Text beginning with this symbol indicates a hazard with a medium or low level of potential which, if not avoided, may result in minor or moderate injury.
注意	Text beginning with this symbol indicates potential hazards, which, if ignored, may result in equipment or component damage, data loss, reduced equipment performance, or unpredictable results.
窍门	Text beginning with this symbol can help you solve a problem or save you time.
说明	The text starting with this symbol is the additional information of the main text, and it is the emphasis and supplement to the main text.

General formatting conventions

Format	illustrate
Times New Roman	The text is expressed in Song font.
black body	Level 1, level 2, and level 3 headings are in bold.
italics	Warnings, prompts and other content are all in italics, and lines are added before and after the content to separate them from the main text.
"Terminal Display" format The "Terminal Display" format represents screen output information. In addition, the information input by the user from the terminal mixed with the screen output information is indicated in bold font.	

Form content agreement

content	illustrate
.	A contentless cell in a table.
*	The content in the table can be configured by the user as required.

Register Access Type Conventions

type description		type description	
RO is read-only, not writable.		W0C can be read, write 0 to clear, write 1 to keep unchanged.	
WO write only.		W1S can be read, write 1 to set, write 0 to keep unchanged.	

type description	type description		
RW can read and write.		W0S can be read, write 0 to set, write 1 to keep unchanged.	
RC reads to clear.		OR	Readable, after writing 1, the chip will be self-cleared, that is, a pulse will be generated.
W1C can be read, write 1 to clear, write 0 to keep unchanged.			

Numerical unit convention

The expressions of data capacity, frequency, data rate, etc. are explained below.

category	symbol	corresponding value
Data capacity (such as RAM capacity)	1K	1024
	1M	1,048,576
	1G	1,073,741,824
frequency, data rate, etc.	1 k	1000
	1M	1,000,000
	1G	1,000,000,000

The address and data expressions are described below.

symbol	example	illustrate
0x	0xFE04ÿ0x18	Data value and address value expressed in hexadecimal.
0b	0b000, 0b00 00000000 represent binary data values and binary sequences (except in register descriptions).	

revision history

A revision record accumulates descriptions of each documentation update. The latest version of the documentation contains updates from all previous versions of the documentation.

Revision Date Version	Revision Description
2016-06-30	00B07 7th interim release Chapter 2 Hardware Subsection 2.3.2, Table 2-3 involves revisions Subsection 2.5.1.3, Tables 2-25 and Table 2-26 involve revisions.

Revision Date	Version	Revision Description
		Chapter 9 Video Interface In Section 9.3.6, the 24bit bits in PHY_MODE_LINK0, PHY_MODE_LINK1 and PHY_MODE_LINK2 involve modification. Chapter 14 Difference between Hi3519V100 and Hi3519V101 Chapter 14, Table 14-1 involves modification.
2016-05-10	00B06	6th interim release Chapter 2 Hardware Sections 2.3.7, 2.3.8, 2.5.11 refer to refreshing Chapter 3 System Section 3.2.7, PERI_CRG15, PERI_CRG19 involves refreshing Chapter 7 video and graphics processing Section 7.4.1 deals with modifications Chapter 12 Peripherals Section 12.8 involves revisions and subsections 12.11.2 and 12.11.3 involve revisions
2016-02-25	00B05	5th interim release Chapter 1 Product Overview Subsection 1.3.1, Figure 1-2 involves modification Section 1.3.15 deals with modifications. Sections 2.3.1, 2.3.2, 2.3.3, and 2.3.4 of Chapter 2 Hardware involve modifying Section 2.3.6 and Table 2-13. Subsection 2.3.8, add Table 2-24. Subsection 2.5.6, revised Table 2-36, Table 2-37 Section 3.2.7 of Chapter 3 System, PERI_CRG 19, PERI_CRG51 involves modification. In Section 3.5.5.2, MISC_CTRL1 bit[15] involves updating the internal temperature detection of the chip in Section 3.11.2. Section 12.9.2 of Chapter 12 Peripherals deals with modifications. Chapter 14 Difference between Hi3519V100 and Hi3519V101 Chapter 14, Table 14-1 deals with revisions.
2015-11-20	00B04	4th interim release Chapter 1 Overview Section 1.4, Table 1-1 involves modification Chapter 2 Hardware

Revision Date Version	Revision Notes
	Section 2.2.3, Table 2-4, Table 2-5 and Table 2-6 involve revisions. Section 2.5.6 involves revisions. Subsection 2.5.9 deals with modifications. Chapter 3 System In Section 3.2.7, modify registers PERI_CRG43 and PERI_CRG44. In Section 3.5.6, modify bit[30] of MISC_CTRL1 register. Subsection 3.11.2 deals with modifications. In section 3.11.4, modify registers PERI_PMC77 and PERI_PMC79, and delete registers PERI_PMC80 to PERI_PMC88. Chapter 9 Video Interface 9.16 Delete registers LINE_BUF_ADAPTER_CFG and CH_ADAPTER_CFG. 9.3.3.2 Deleted LVDS wide dynamic mode 4 and deleted Figure 9-33. 9.3.6 Delete register LVDS0_DOLSCD_HBLK, LVDS0_WDR involves modification. Chapter 10, subsection ISP 10.2, deals with modifications. Section 10.4 deals with modifications. Section 10.5.2, ISPFE_MAX_ADDR_iridix1 is replaced by ISPFE_MAX_ADDR_NR1ÿISPFE_MAX_ADDR_iridix2 ÿÿÿISPFE_MAX_ADDR_NR2 10.5.2 ÿÿÿÿÿÿÿÿDRC_STRENGTH_INROIÿ DRC_STRENGTH_OUTROIÿ DRC_ROI_HOR_START_ENDÿ DRC_ROI_VER_ENDÿ DRC_FILTER_MUXÿ DRC_DARK_ENHÿ FRAME_STATS_STATS_RESETÿ FRAME_STATS_STATS_HOLDÿ
2015-10-20	00B03 3rd interim release. Section 1.3.11 of Chapter 1 Product Overview deals with modifications. Chapter 8 Intelligent Acceleration Engine Section 8.1.3.2, add SAD. 02-A Order Notice Added Hi3519V100 order information.
2015-09-20	00B02 2nd interim release. Chapter 2 Hardware Section 2.1.1, Figure 2-1 and Figure 2-2 deal with refreshing. Section 2.5.4.2, Table 2-33, Table 2-34, and Table 2-35 deals with refreshing.

Revision Date Version	Revision Description
	Chapter 3 System Section 3.2.3, refresh Figure 3-3. Chapter 11 Audio Interface Subsection 11.1.5 Table 11-1 deals with refreshing. Section 11.1 deals with updates
2015-08-20	00B01 First interim release.

Table of contents

illustration catalog

table of contents

1 product description

1.1 Overview

Hi3519V100, as a new generation of industry-specific HD IP camera SoC, integrates a new generation of ISP, adopts the latest H.265 video compression encoder in the industry, and adopts advanced low-power technology and low-power architecture design. It continues to lead the industry in terms of high rate, high image quality and low power consumption. The innovative hardware supports 90-degree/270-degree rotation function and lens geometry correction function, which can meet the needs of various scenarios of surveillance applications.

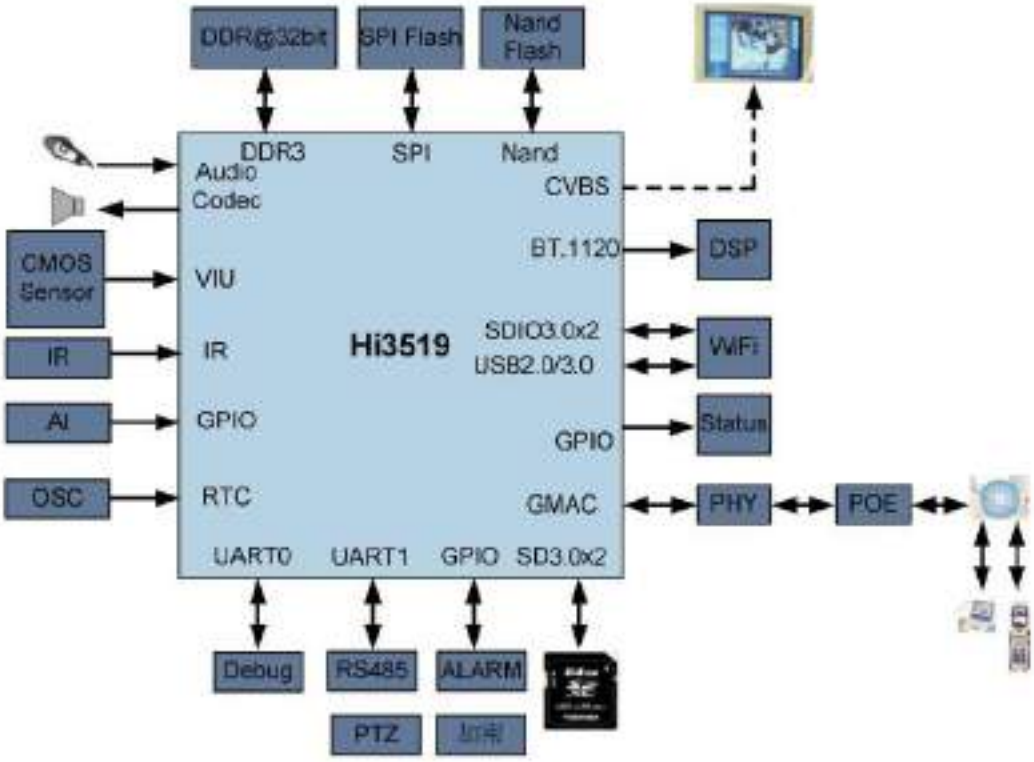
Hi3519V100 supports 3A algorithm, based on which users can design various models including all-in-one machine core. Integrating POR, RTC, Audio Codec, and supporting multiple sensor levels and various clock outputs will greatly reduce the EBOM cost of HD IP cameras based on Hi3519V100. With HiSilicon's stable and easy-to-use SDK design, it can support customers' rapid mass production of products and realize the system layout of DVR/NVR and IP cameras.

1.2 Application scenarios

1.2.1 Hi3519V100HD IP Camera Solution

Typical application scenarios of the Hi3519V100 are shown in Figure 1-1 .

Figure 1-1 Hi3519V100 application block diagram

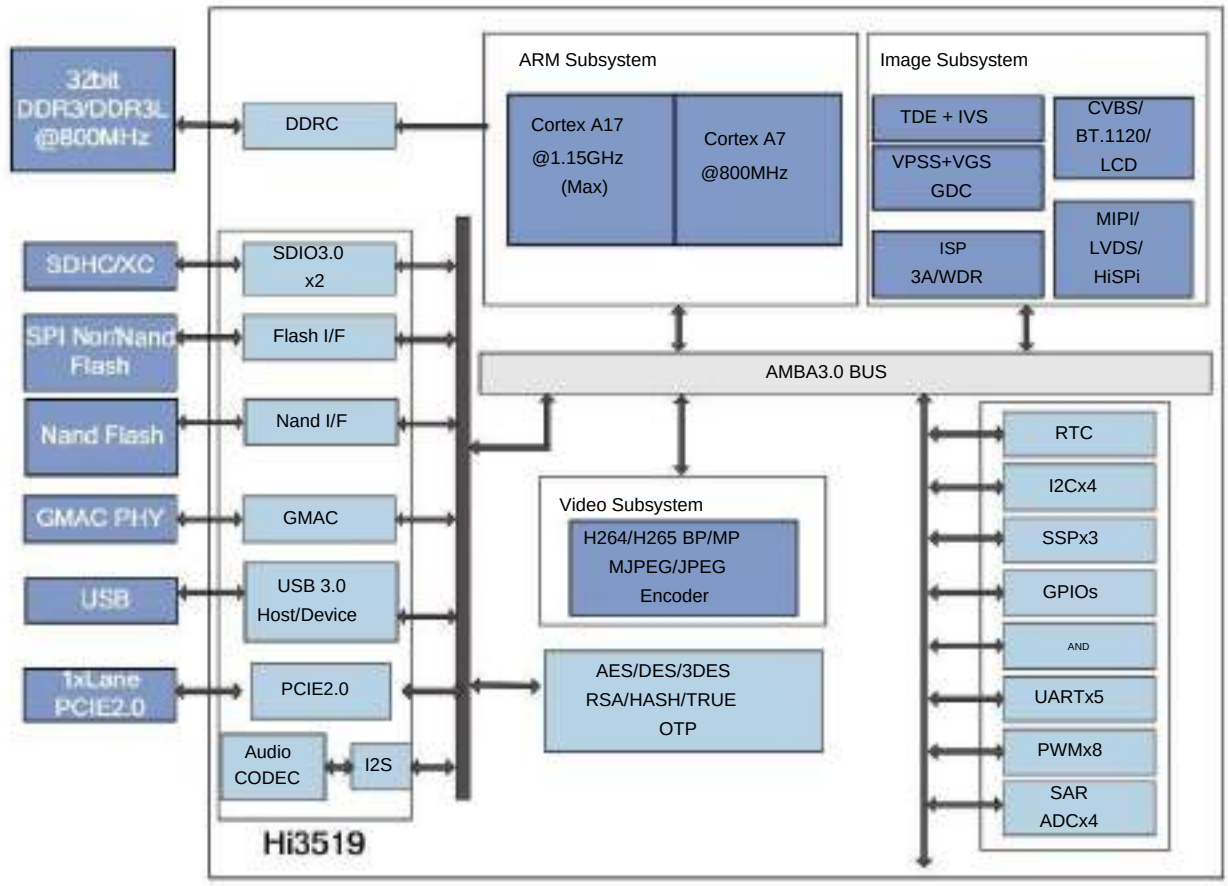


1.3 Architecture

1.3.1 Overview

The logical block diagram of the Hi3519V100 chip is shown in Figure 1-2 .

Figure 1-2 Logic block diagram of Hi3519V100 chip



1.3.2 Processor Core

A7@ 800MHz, 32KB I-Cache, 32KB D-Cache /128KB L2 cache A17@ 1.15GHz (Max),

32KB I-Cache, 32KB D-Cache /256KB L2 cache Support Neon acceleration, integrated FPU processing unit supports ARM® big .LITTLE size core architecture

1.3.3 Video Coding

H.264 BP/MP/HP

H.265 Main Profile

H.264/H265 support I/P/frame

support MJPEG/JPEG Baseline encoding

1.3.4 Video encoding processing performance

H.264/H.265 encoding can support a maximum resolution of 16M Pixel

H.264/H.265 multi-stream real-time encoding capability:

ÿ 4K2K@30fps+720P@30fps

ÿ 16M@2fps

supports JPEG capture 8M @30fps

CBR/VBR code rate control, 2kbpsÿ100Mbps encoding frame rate

supports 1/16ÿ240fps Supports 8 regions of

interest (ROI) encoding

1.3.5 Intelligent Video Analysis

Integrated intelligent analysis acceleration engine, supporting various intelligent analysis applications such as intelligent motion detection, perimeter prevention, video diagnosis, etc.

1.3.6 Video and Graphics Processing

Support 3D denoising, image enhancement, dynamic contrast enhancement processing functions

Support video and graphic output anti-flicker processing

Support video 1/15~16x zoom function

Support graphics 1/2 ~ 2x zoom function

8 zones of pre-encoding OSD overlay

2 layers (video layer, graphics layer) video graphics overlay

1.3.7 ISP

Support 3A (AE/AWB/AF) function, 3A control user can adjust Support fixed pattern noise (FPN)

function Strong light suppression, backlight compensation,

gamma, color enhancement Support dead point correction, denoising, digital

image stabilization Support deshake Fog support fisheye

correction

support image 90°/270°

rotation support image mirror, flip support digital

WDR, 4F/3F/2F - Frame base/Line

base WDR and Tone mapping provide PC-side ISP tuning tools

1.3.8 Audio Codec

Realize multi-protocol voice codec protocol through software

Support G.711, ADPCM, G.726 Support audio 3A (AEC/ANR/

ALC) processing

1.3.9 Security Engine

Hardware implementation of AES/DES/3DES three encryption and decryption

algorithms Hardware implementation of RSA1024/2048/4096 signature verification algorithm

Hardware implements HASH anti-tampering algorithm, supports HASH-SHA1/256, HMAC_SHA1/256 algorithm, internally integrates 512Bit OTP storage space and hardware random number generator

1.3.10 Video interface

Input

ÿ Support 8/10/12/14 bit RGB Bayer DC timing video input, clock frequency up to 150MHz ÿ Support BT.601, BT.656, BT.1120 video input interface

ÿSupports 8Lane MIPI D-PHY interface, 12lane LVDS/sub-LVDS/HiSPi interface ÿSupports docking with mainstream high-definition CMOS sensors such as SONY, Aptina, OmniVision, Panasonic, etc. ÿCompatible with multiple sensor parallel/differential interface electrical characteristics

ÿProvides programmable sensor Clock output

output

ÿ Supports 1 PAL/NTSC output, supports automatic load detection ÿ Provides 1 BT.1120/BT.656 video output interface for external expansion of HDMI or SDI interface, supports maximum 1080P@60fps output, supports LCD output

1.3.11 Audio interface

Integrated Audio codec, support 16bit voice input and output

Support I2S interface, support docking with external Audio codec

Support dual-channel mic differential input to reduce noise floor

1.3.12 Peripheral Interface

Support POR

Integrated high-precision RTC Integrated 4-channel SAR-ADC 5 UART interfaces

IR interface, I2C interface, SSP master interface, GPIO interface

8 PWM interfaces (4 independent, 4 shared with other pins)

2 SD3.0/SDIO3.0 interfaces, support SDXC

1 USB3.0/2.0 HOST/Device interface

1 PCIe2.0 master/slave mode

Support RGMII and RMII mode; support 10/100 Mbps full-duplex or half-duplex mode, support 1000 Mbps full duplex mode; support TSO network acceleration

1.3.13 External memory interface

DDR3/DDR3L interface ÿ One 32bit DDR3/3L up to 800MHz (1.6Gbps) ÿThe maximum capacity of a single 16bit DDR particle supports 1024 MB

ÿThe maximum capacity of two 16bit DDR particles supports 2048 MB

SPI Nor Flash interface

ÿSupport 1, 2, 4 wire mode

ÿSupport 3Byte, 4Byte address mode ÿThe

maximum capacity supports 32MB

SPI Nand Flash interface

ÿThe maximum capacity supports 512 MB

Support eMMC5.0 interface

ÿThe maximum capacity supports 64 GB

NAND Flash interface

ÿ 8bit data width

ÿSupport SLC, MLC

ÿ 4ÿ8ÿ24ÿ40ÿ64bit ECC

ÿSupport devices with a capacity

above 8GB can choose to boot from SPI NOR Flash, SPI Nand Flash or NAND Flash

Support booting from eMMC

1.3.14 SDK

Provide a high-performance PC/iOS/

Android decoding library for H.264/H.265 based on the Linux-3.18 SDK package

1.3.15 Chip physical specifications

Power

consumption ÿ 4K*2K, 1.6W typical power

consumption ÿ support multi-level power

saving mode working voltage

ÿ Core voltage is 0.9V

ÿ IO voltage is 3.3V, tolerance voltage is 3.8V ÿ

DDR3/3L SDRAM interface voltage is 1.5/1.35 V

encapsulation

ÿ RoHSÿTFBGA

ÿ 15mm x 15mm package size

ÿPin pitch: 0.65mm

1.4 Start mode

Hi3519V100 supports the following 5 startup methods:

Boot from BOOT ROM storage space Boot from

off-chip SPI Flash storage space

Boot from off-chip NAND Flash storage space

Boot from off-chip eMMC storage

PCIe Slave Boot

When the chip is powered on and reset, the boot mode is determined by the value of the BOOTROM_SEL/BOOT_SEL0/ BOOT_SEL1 signal, as shown in Table 1-1 .

Table 1-1 Startup modes

BOOTROM_SEL	BOOT_SEL1	BOOT_SEL0	SFC_EMMC_BOOT_MONOF	SFC_DEVICE_MODE	SPI_NAND_SEL	UPDATE_FROM_SDIO	boot mode
1	x	x	x	x	x	x	from BOOTROM start
0	0	0	0	0	x	x	from off-chip SPI NOR Flash (3byte address mode) start
0	0	0	1	0	x	x	from off-chip SPI NOR Flash (4byte address mode) start
0	0	0	0	1	0	x	from off-chip SPI NAND Flash (1-line mode, Plane address bit is not enabled) start
0	0	0	1	1	0	x	from off-chip SPI NAND Flash (4-wire mode, Plane address bit is not enabled) start
0	0	0	0	1	1	X	from off-chip SPI NAND Flash (1-line mode, Plane address bit enable) start

BOOTROM_SEL	BOOT_SEL1	BOOT_SEL0	SFC_EMMC_BOOT_MONOF	SFC_DEVICE_MODE	SPI_NAND_SEL	UPDATE_FROM_SDIO	boot mode
0	0	0	1	1	1	x	from off-chip SPI NAND Flash (4-wire mode, Plane address bit enable) start
0	0	1	x	x	x	x	off-chip NAND Flash start
0	1	0	0	x	x	x	Boot from off-chip eMMC (4-wire)
0	1	0	1	x	x	x	Boot from off-chip eMMC (8-wire)
0	1	1	x	x	x	X	PCIe Slave Boot

Illustrate

The BOOTROM_SEL signal is multiplexed with the external pin VO_DAT2 of the chip;

BOOT_SEL0 signal is multiplexed with chip external pin VO_DAT0.

BOOT_SEL1 signal is multiplexed with chip external pin VO_DAT1.

SFC_EMMC_BOOT_MODE is multiplexed with chip external pin VO_DAT3.

SFC_DEVICE_MODE is multiplexed with chip external pin VO_DAT4.

SPI_NAND_SEL is multiplexed with chip external pin EPHY_RSTN.

UPDATE_FROM_SDIO is multiplexed with chip external pin VO_DAT6.

When the startup mode is booting from BOOTROM, the serial communication mechanism will be started, and the communication with the corresponding software on the PC will be established through the serial port, and the startup will be completed after downloading the boot program (please refer to the "HiBurn Tool User Guide"); If the serial communication timeout does not respond, it will turn to judge the pull-down level of BOOT_SEL1 and BOOT_SEL0. When BOOT_SEL1=0, BOOT_SEL0=0, turn to start from off-chip SPI Flash; when BOOT_SEL1=0, BOOT_SEL0=1, turn to off-chip NAND Flash boot; when BOOT_SEL1=1, BOOT_SEL0=0, turn to boot from off-chip eMMC Flash.

When the boot mode is configured as PCIe slave boot mode, the CPU will not start after the chip power-on reset is cancelled, and the master chip loads the boot program into the slave chip DDR through the PCIe interface, and then the master chip cancels the reset of the slave chip CPU through the PCIe interface , load the boot program from the chip from the DDR.

1.5 Address Space Mapping

Address space mapping is shown in Table 1-2 .

Table 1-2 Address space mapping table

start address end address	Function	size description
0x0000_0000 0x03FF_FFFF	Address remaps selected memory. Point to on-chip RAM after remapping is cancelled.	When remapping 64MB: {BOOTROM_SELÿ BOOT_SEL1, BOOT_SEL0} 3'b000: SPI FLASH MEMORY space; 3'b001: Nand FLASH MEMORY space; 3'b011ÿ BOOTRAMÿ other: BOOTROMÿ After remapping is cancelled: point to on-chip RAM.
0x0400_0000 0x0400_FFFF	BOOTROM address space	64KB The actual size is 16KB.
0x0401_0000 0x0401_FFFF	BOOTRAM address space	64KB The actual size is 28KB.
0x0402_0000 0x0406_FFFF reserved		320KB
0x0407_0000 0x0FFF_FFFF Reserved		
0x1000_0000 0x1000_FFFF	FMC register	64KB
0x1001_0000 0x1001_FFFF reserved		64KB
0x1002_0000 0x1002_FFFF reserved		64KB
0x1003_0000 0x1003_FFFF DMAC Register		64KB
0x1004_0000 0x1004_FFFF reserved		64KB
0x1005_0000 0x1005_FFFF	GSF register	64KB
0x1006_0000 0x1006_FFFF reserved		64KB
0x1007_0000 0x1007_FFFF reserved		64KB
0x1008_0000 0x1008_FFFF	CIPHER register	64KB
0x1009_0000 0x1009_FFFF	HASH register	64KB
0x100A_0000 0x100A_FFFF Reserved		64KB

start address end address	Function	size description
0x100B_0000 0x100B_FFFF reserved		64KB
0x100C_0000 0x100C_FFFF	SDIO0 register	64KB
0x100D_0000 0x100D_FFFF	SDIO1 register	64KB
0x100E_0000 0x100E_FFFF EMMC register		64KB
0x100F_0000 0x100F_FFFF Reserved		64KB
0x1010_0000 0x1010_FFFF reserved		64KB
0x1011_0000 0x1011_FFFF	USB2.0 HOST OHCI register 64KB	
0x1012_0000 0x1012_FFFF	USB2.0 HOST EHCI register 64KB	
0x1013_0000 0x1013_FFFF	USB2.0 DEVICE Register	64KB
0x1014_0000 0x1014_FFFF reserved		64KB
0x1015_0000 0x1015_FFFF reserved		64KB
0x1016_0000 0x1016_FFFF reserved		64KB
0x1017_0000 0x1017_FFFF reserved		64KB
0x1018_0000 0x1018_FFFF	USB3.0 registers	64KB
0x1019_0000 0x1019_FFFF reserved		
0x101A_0000 0x101A_FFFF Reserved		64KB
0x101B_0000 0x101B_FFFF reserved		64KB
0x101C_0000 0x101D_FFFF reserved		128KB
0x101E_0000 0x101F_FFFF reserved		128KB
0x1020_0000 0x1020_FFFF reserved		64KB
0x1021_0000 0x102F_FFFF reserved		
0x1030_0000 0x1030_FFFF	GIC register	64KB
0x1031_0000 0x103F_FFFF reserved		64KB
0x1040_0000 0x1051_FFFF reserved		1088KB
0x1060_0000 0x106F_FFFF reserved		
0x1070_0000 0x1070_FFFF reserved		64KB
0x1071_0000 0x10FF_FFFF reserved		
0x1100_0000 0x1100_FFFF	VDP register	64KB
0x1101_0000 0x1101_FFFF reserved		64KB

start address end address	Function	size description
0x1102_0000 0x1102_FFFF reserved		64KB
0x1103_0000 0x1103_FFFF reserved		64KB
0x1104_0000 0x1104_FFFF	IVE register	64KB
0x1105_0000 0x1105_FFFF reserved		64KB
0x1107_0000 0x1107_FFFF reserved		64KB
0x1108_0000 0x1108_FFFF	AIAO Register	64KB
0x1109_0000 0x1109_FFFF reserved		64KB
0x110A_0000 0x110A_FFFF Reserved		64KB
0x110B_0000 0x110B_FFFF reserved		64KB
0x110C_0000 0x110C_FFFF	GZIP register	64KB
0x110D_0000 0x110F_FFFF reserved		
0x1110_0000 0x1110_FFFF	TDE register	64KB
0x1111_0000 0x1111_FFFF	GDC register	64KB
0x1112_0000 0x1112_FFFF	VGS register	64KB
0x1113_0000 0x1117_FFFF reserved		
0x1118_0000 0x1118_FFFF	VPSS Register	64KB
0x1119_0000 0x1119_FFFF reserved		64KB
0x111A_0000 0x111A_FFFF Reserved		64KB
0x111B_0000 0x111B_FFFF reserved		64KB
0x111C_0000 0x111F_FFFF reserved		
0x1120_0000 0x1120_FFFF	JPGE register	64KB
0x1121_0000 0x1121_FFFF reserved		64KB
0x1122_0000 0x1123_FFFF reserved		
0x1124_0000 0x1124_FFFF reserved		64KB
0x1125_0000 0x1125_FFFF Reserved		64KB
0x1126_0000 0x1126_FFFF reserved		64KB
0x1127_0000 0x1127_FFFF reserved		64KB
0x1128_0000 0x1128_FFFF	VEDU register	64KB
0x1129_0000 0x1129_FFFF reserved		64KB

start address end address	Function	size description
0x112A_0000 0x112A_FFFF Reserved		64KB
0x112B_0000 0x112B_FFFF reserved		64KB
0x112C_0000 0x112F_FFFF reserved		64KB
0x1130_0000 0x1130_FFFF	MIPI registers	64KB
0x1131_0000 0x1137_FFFF reserved		
0x1138_0000 0x113E_FFFF	VICAP register	448KB
0x113F_0000 0x1147_FFFF reserved		
0x1148_0000 0x114E_FFFF reserved		448KB
0x114F_0000 0x11FF_FFFF reserved		
0x1200_0000 0x1200_0FFF	TIMER0/TIMER1 REGISTERS	4KB
0x1200_1000 0x1200_1FFF	TIMER2/TIMER3 Registers	4KB
0x1200_2000 0x1200_2FFF	TIMER4/TIMER5 Registers	4KB
0x1200_3000 0x1200_3FFF Reserved		4KB
0x1200_4000 0x1200_FFFF reserved		48KB
0x1201_0000 0x1201_FFFF	CRG register	64KB
0x1202_0000 0x1202_FFFF	SYSCTRL register	64KB
0x1203_0000 0x1203_FFFF	MISC register	64KB
0x1204_0000 0x1204_07FF	IO MUX config register	2KB multiplexing relationship
0x1204_0800 0x1204_FFFF	IO CTRL config register	62KB drive current
0x1205_0000 0x1205_0FFF	DDRT register	4KB
0x1205_1000 0x1205_1FFF Reserved		60KB
0x1206_0000 0x1206_FFFF	MDDRC/DDRPHY register 64KB	
0x1207_0000 0x1207_07FF reserved		2KB
0x1207_0800 0x1207_FFFF	cipher_hash_key_ctrl register 62KB	
0x1208_0000 0x1208_FFFF WDG register		64KB
0x1209_0000 0x1209_FFFF	RTC register	64KB
0x120A_0000 0x120A_FFFF	PMC register	64KB
0x120B_0000 0x120B_FFFF	RSA register	64KB
0x120C_0000 0x120C_FFFF	TRNG register	64KB

start address end address	Function	size description	
0x120D_0000 0x120D_FFFF	SYSCNT register	64KB	
0x120E_0000 0x120E_FFFF	SAR_ADC Register	64KB	
0x120F_0000 0x120F_FFFF	IR register	64KB	
0x1210_0000 0x1210_0FFF	UART0 register	4KB	
0x1210_1000 0x1210_1FFF	UART1 register	4KB	
0x1210_2000 0x1210_2FFF	UART2 registers	4KB	
0x1210_3000 0x1210_3FFF	UART3 registers	4KB	
0x1210_4000 0x1210_4FFF	UART4 registers	4KB	
0x1210_5000 0x1210_FFFF reserved		44KB	
0x1211_0000 0x1211_0FFF	I2C0 register	4KB	
0x1211_1000 0x1211_1FFF	I2C1 registers	4KB	
0x1211_2000 0x1211_2FFF	I2C2 registers	4KB	
0x1211_3000 0x1211_3FFF	I2C3 registers	4KB	
0x1211_4000 0x1211_4FFF reserved		4KB	
0x1211_5000 0x1211_FFFF reserved		44KB	
0x1212_0000 0x1212_0FFF	SSP0 register	4KB	
0x1212_1000 0x1212_1FFF	SSP1 Register	4KB	
0x1212_2000 0x1212_2FFF	SSP2 Register	4KB	
0x1212_3000 0x1212_3FFF reserved		4KB	
0x1212_4000 0x1212_4FFF	spi_3wire register	4KB	
0x1212_5000 0x1212_5FFF Reserved		4KB	
0x1212_6000 0x1212_FFFF reserved		40KB	
0x1213_0000 0x1213_FFFF PWM Register		64KB	
0x1214_0000 0x1214_0FFF	GPIO0 register	4KB	
0x1214_1000 0x1214_1FFF	GPIO1 register	4KB	
0x1214_2000 0x1214_2FFF	GPIO2 Register	4KB	
0x1214_3000 0x1214_3FFF	GPIO3 register	4KB	
0x1214_4000 0x1214_4FFF	GPIO4 register	4KB	
0x1214_5000 0x1214_5FFF	GPIO5 Register	4KB	

start address end address	Function	size description	
0x1214_6000 0x1214_6FFF	GPIO6 register	4KB	
0x1214_7000 0x1214_7FFF	GPIO7 register	4KB	
0x1214_8000 0x1214_8FFF	GPIO8 register	4KB	
0x1214_9000 0x1214_9FFF	GPIO9 register	4KB	
0x1214_A000 0x1214_AFFF	GPIO10 Register	4KB	
0x1214_B000 0x1214_BFFF	GPIO11 register	4KB	
0x1214_C000 0x1214_CFFF	GPIO12 Register	4KB	
0x1214_D000 0x1214_DFFF	GPIO13 register	4KB	
0x1214_E000 0x1214_EFFF Reserved		4KB	
0x1214_F000 0x1214_FFFF Reserved		4KB	
0x1215_0000 0x1215_FFFF reserved		64KB	
0x1216_0000 0x1216_FFFF	PCIE register space	64KB	
0x1217_0000 0x1217_FFFF reserved		64KB	
0x1218_0000 0x12FF_FFFF reserved			
0x1300_0000 0x13FF_FFFF reserved			
0x1400_0000 0x14FF_FFFF	FMC storage address space	16MB	
0x1500_0000 0x1EFF_FFFF reserved			
0x1F00_0000 0x1FFF_FFFF	CCI register	1MB	
0x2000_0000 0x27FF_FFFF	PCIE configuration space	128MB	
0x2800_0000 0x2FFF_FFFF	PCIE MEMORY space	128MB	
0x3000_0000 0x37FF_FFFF reserved		128MB	
0x3800_0000 0x3FFF_FFFF Reserved		128MB	
0x8000_0000 0xFFFF_FFFF DDR address space		2GB	

Table of contents

illustration catalog

table of contents

2 hardware features

2.1 Package and Pin Distribution

2.1.1 Packaging

The Hi3519V100 chip is packaged in TFBGA, the package size is 15mm x 15mm, the pin pitch is 0.65mm, and the total number of pins is 389. Please refer to Figure 2-1 to Figure 2-4 for detailed packaging, and please refer to Figure 2-4 for package size parameters 2-5ÿ

Figure 2-1 Top view of chip package

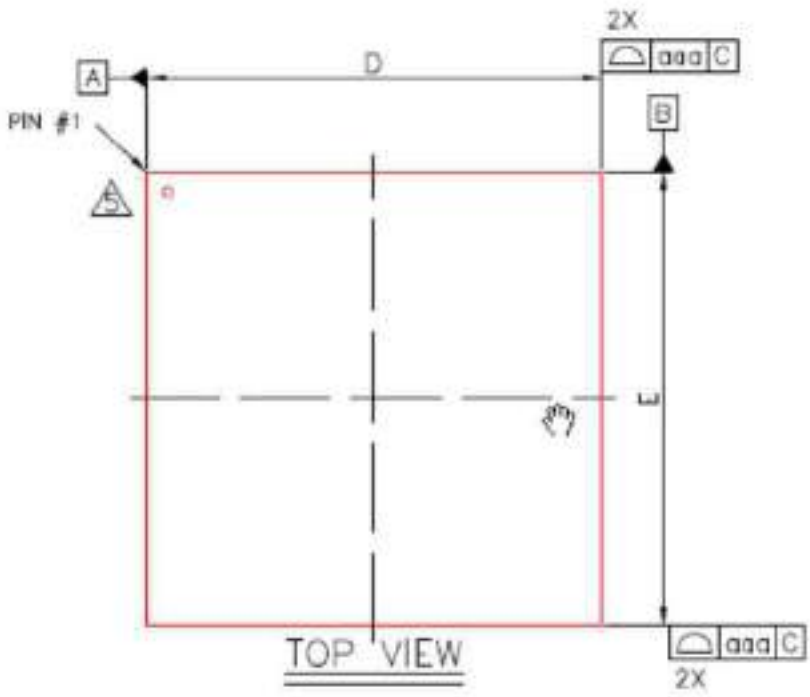


Figure 2-2 Chip package bottom view

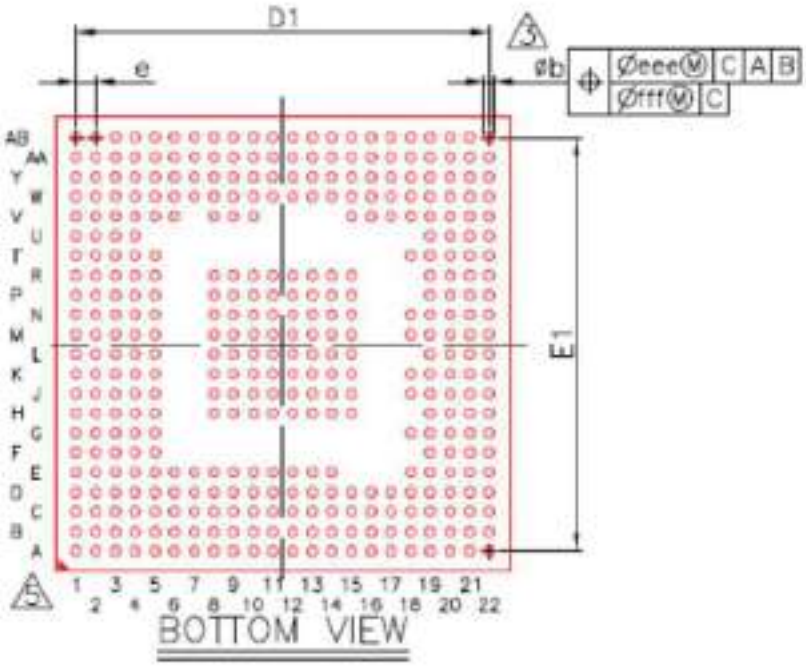


Figure 2-3 Side view of chip package

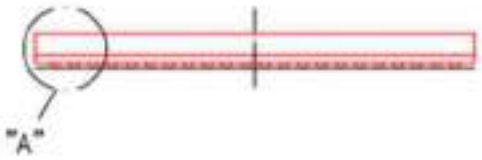


Figure 2-4 Enlarged view of Detail A

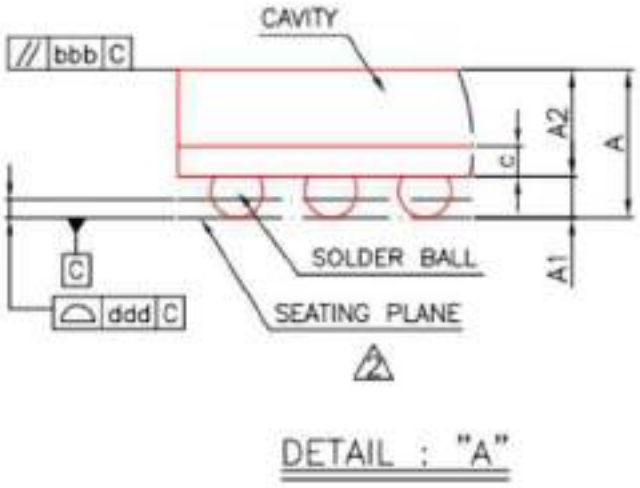


Figure 2-5 Package parameter description

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	13.65	---	---	0.537	---
E1	---	13.65	---	---	0.537	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		22/22				

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

2.1.2 Pin distribution

The Hi3519V100 has 389 pins, and the pin number statistics are shown in Table 2-1 .

Table 2-1 Statistics of Hi3519V100 pin numbers

Pin category	quantity
I/O	240
digital power	44
digitally	66
Other/Analog Power	14
Other/analog ground	25
DDR Reference Supply (VREF)	0
total	389

2.2 Pin information description

For chip pin information description and digital pin default status, please refer to the document:

"HI3519V100_PINOUT_CN".xls.

2.3 Electrical performance parameters

2.3.1 Power Consumption Parameters

The power consumption parameters of Hi3519V100 are shown in Table 2-2 .

注意

The power consumption parameter is based on the typical working scene of the chip

Single-board power supply design must refer to the hardware design guide

Table 2-2 Hi3519V100 power consumption parameters

symbol	parameter	Typical Value Maximum Unit		
VDD	VDD core supply ~160		~251	mW
VDD_DDR	DDR core power ~129		~173	mW
VDD_CPU	CPU core power ~0		~236	mW
VDD_MEDIA MEDIA core power ~715			~1010	mW
VDDIO_DDR DDR IO power supply		~269	~362	mW
3.3V power supply	3.3V I/O power supply	~337	~349	mW

说明

Typical scenario:

8M@30fps input linear mode single P (reference frame) online;

Specific configuration:

A7: 800MHz; 2 DDR3 4Gb particles (16bit bit width); MIPI-VICAP-ISP 300MHz;

VGSÿ400MHzÿVPSSÿ300MHzÿVEDUÿH.265ÿÿ500MHzÿGDCÿ475MHzÿ

Audio codec on, CVBS off, USB off, SDIO off.

Business description:

MIPI -> VICAP (ISP) -> VPSS (one input and three outputs) -> VEDU (1 channel 8M@30fps stream + 1 channel 720p@30fps stream) -> IVE motion detection (720P@5fps);

3A Algorithm + Audio Input -> AENC -> Network + Network -> ADEC -> Audio Output + 8-way network on-demand large stream 64Mbpsÿ

Compression and decompression are used for the entire channel of the data stream, and the scene is a sports scene (the big TV plays the sports scene for IPC collection).

2.3.2 Temperature and thermal resistance parameters

The temperature and thermal resistance parameters are shown in Table 2-3, Table 2-4 and Table 2-5 .

說明

The thermal resistance is given based on the JEDEC JESD51 series standards. The system design and environment of the application may be different from the JEDEC JESD51 series standards, and it needs to be analyzed according to the application conditions.

ýJA Please refer to JESD 51-2 standard

ýJB Please refer to JESD 51-8 standard

ýJC Please refer to:

(1) MIL-STD 883 1012.1 (2) SEMI G30-88

The junction temperature of the chip is directly proportional to the power consumption of the chip. It is necessary to consider controlling the junction temperature of the chip within a reasonable range to match the power supply Specification.

The product is stored in vacuum in a sealed bag, and it can last up to 12 months when the temperature is less than 40°C and the relative humidity is less than 90%.

After the packaging bag is opened, the component will be used in the reflow process or other high temperature process must meet:

a. Complete within 168 hours and the factory environment is ÿ30ý/60% RH. b. Store at <10% RH.

The soldering temperature profile is based on the J-STD-020E standard.

警告

Exceeding the limit value of the working environment parameters may cause physical damage to the chip.

注意

The maximum limit junction temperature of Hi3519V100 is 125°, and the junction temperature of the chip cannot exceed this number under any conditions. value. May cause physical damage to the chip.

The maximum long-term working junction temperature of Hi3519V100 is 105°C, and the junction temperature of the chip under normal working conditions should be lower than at that value.

Under short-term working conditions (according to the GR-63-CORE standard, short-term working conditions are defined as a duration of no more than 96 hours each time, and the accumulative time does not exceed 15 days per year), Hi3519V100 can tolerate over 105°, while less than 125° High temperature, but working for a long time at a junction temperature exceeding 105° will result in reduced chip life or work unstable.

Table 2-3 Working environment parameters

parameter	symbol min max unit			
ambient temperature	FACING	0	70	ÿ

Hi3519V100 junction temperature parameters are shown in Table 2-4 .

Table 2-4 Hi3519V100 junction temperature parameters

Package type maximum power consumption (IN)	Normal operating junction temperature lower limit ÿÿÿ	Long-term working maximum junction temperature ÿÿÿ	Short-Term Operating Upper Junction Temperature ÿÿÿ	Destructive Maximum Junction Temperature ÿÿÿ	Life cycle definition (Year)
TFBGA 2.3W	-20	105	125	125	5

Hi3519V100 thermal resistance parameters are shown in Table 2-5 .

Table 2-5 Thermal resistance parameters

parameter	Symbol	Min	Typ	Max	Unit
Junction-to-ambient thermal resistance ÿJA			24		ÿ/W
Junction-to-board thermal resistance	ÿJB		12.2		ÿ/W
Junction-to-case thermal resistance	ÿJC		6.2	-	ÿ/W

2.3.3 Working conditions

The working conditions of Hi3519V100 are shown in Table 2-6 and Table 2-7 .

注意

When using SVB technology, the prerequisite for the core power supply voltage range is: the customer board must use the SVB circuit, and the resistance and capacitance parameters of the SVB circuit must completely copy the relevant RC parameters in the "Hi3519V100 Hardware Design User Guide".

Table 2-6 SVB related power working conditions

symbol	describe	SVB voltage range			unit
		Min	Typ	Max	
VDD	core power	0.89	0.93	0.97	IN
VDD_DDR	DDR Core Power 0.86		-	0.91	IN

symbol	describe	SVB voltage range			unit
		Min Typ Max			
VDD_CPU	CPU core power 0.67			1.0	IN
VDD_MEDIA	MEDIA Core Power 0.83			0.95	IN
AVDD_PLL	PLL core analog power 0.89		0.93	0.97	IN
AVDD _U3_PCIE USB3.0 and PCIE core analog power supply		0.89	0.93	0.97	IN

Table 2-7 Normal voltage power supply working conditions

symbol	describe	Min Typ Max Unit			
DVDD33	I/O power supply	2.97	3.3	3.63 V	
DVDD33_SENS0 SENSOR0ÿSPI0ÿ GPIO1 I/O Power		2.97	3.3	3.63 V	
DVDD33_UART1 UART1 I/O power supply 2.97			3.3	3.63 V	
DVDD3318_EMMC	NAND FLASH/eMMC I/O Power	2.97/1.62 3.3/1.8		3.63/1.98	IN
DVDD18_SDIO	SDIO1.8V I/O power supply 1.62		1.8	1.98 V	
DVDDIO_RGMII RGMII I/O Power 2.97/1.62 3.3/1.8				3.63/1.98	IN
VDDIO_DDR	DDR3/DDR3L interface power supply	1.425/1.323	1.5/1.35	1.575/1.425	IN
VDDIO_CK_DDR DDR3/DDR3L clock interface power supply		1.425/1.323	1.5/1.35	1.575/1.425	IN
AVDD_DDRPLL1 AVDD_DDRPLL2	DDR3/DDR3L PLL 3.3V analog power supply	3.125	3.3	3.6	IN
AVDD33_PLL	PLL 3.3V Analog Power 2.97		3.3	3.63 V	
AVDD33_USB2	USB2.0 3.3V analog power supply	3.0	3.3	3.6	IN
AVDD_EFUSE	EFUSE 1v8 Analog Power 1.71		1.8	1.89 V	
AVDD3318_MIPI MIPI Analog Power Supply		1.71	1.8	1.89 V	

symbol	describe	Min Typ Max Unit			
	3.3V supply when MIPI is multiplexed as a single-ended digital signal	2.97	3.3	3.63 V	
	1.8V supply when MIPI is multiplexed as a single-ended digital signal	1.62	1.8	1.98 V	
AVDD33_U3_PCIE USB3.0 and PCIE 3.3V analog power supply		3.0	3.3	3.6	IN
AVDD33_AC	AudioCodec 3.3V Analog Power Supply	3	3.3	3.6	IN
AVDD33_VDAC VDAC 3.3V analog power supply		2.97	3.3	3.63 V	
AVDD_BAT	RTC battery power	1.6	3.3	3.6	IN
AVDD33_RTC	RTC Analog Power 2.97		3.3	3.63 V	

2.3.4 Power on and off sequence

Please refer to chapter 1.2.5 of "Hi3519V100 Hardware User Guide" for the power on and off sequence.

2.3.5 DC/AC electrical parameters

Hi3519V100 DC electrical parameters are listed in Table 2-8 .

Table 2-8 DC electrical parameter table (DVDD33_SENS0/ DVDD33_UART1/ DVDD3318_EMMC/ DVDDIO_RGMII/DVDD33ÿ 3.3V)

symbol	parameter	Minimum value	Typical value	Maximum value	Unit	description
DVDD33 interface voltage 2.97			3.3	3.63	IN	
HIV	High level input voltage	2.0		DVDD33+0.3 V is not compatible with 5V input		
WILL	Low level input voltage	–0.3		0.8	IN	
THE	Input Leakage Current-			±10	µA	
IOZ	Three-state output leakage current			±10	µA	
VOH	High level output voltage	2.4			IN	
VOL	Low level output voltage			0.4	IN	-

symbol	parameter	Minimum value	Typical value	Maximum value	Unit	description
RPU1	Internal pull-up resistor 30		33	36	kÿ	·
RPD1	Internal pull-down resistor 30		33	36	kÿ	·
RPU2	Internal pull-up resistor 38		42	46	kÿ	·
RPD2	Internal pull-down resistor 38		42	46	kÿ	·
RPU3	Internal pull-up resistor 18		20	22	kÿ	·
RPD3	Internal pull-down resistor 56		62	68	kÿ	·
RPU4	Internal pull-up resistor 20		22	24	kÿ	·
RPD4	Internal pull-down resistor 22		25	28	kÿ	·
RPU5	Internal pull-up resistor 17		19	21	kÿ	·
RPD5	Internal pull-down resistor 22.5		25	27.5	kÿ	·
RPU8k	8kohm pull-up resistor	6.7	8.54	10.54	kÿ	
RPD8k	8kohm pull-down resistor	6.53	8.32	10.38	kÿ	

Table 2-9 DC Electrical Parameters ((DVDD3318_EMMC/ DVDD18_SDIO/ DVDDIO_RGMII =1.8V)

symbol	parameter	Minimum value	Typical value	Maximum value	Unit	description
DVDD18 interface voltage		1.62	1.8	1.98	IN	·
HIV	High level input voltage 1.17		·	DVDD18+0.3V		
WILL	Low level input voltage – 0.3		·	0.63	IN	·
THE	Input Leakage Current-		·	±10	µA -	
IOZ	Three-State Output Leakage Current-		·	±10	µA -	
VOH	High level output voltage 1.35		·	·	IN	·
VOL	Low Level Output Voltage -		·	0.45	IN	·
RPU1	Internal pull-up resistor 35		38	41	kÿ -	
RPD1	Internal pull-down resistor 29		32	35	kÿ -	
RPU2	Internal pull-up resistor 54		60	66	kÿ -	
RPD2	Internal pull-down resistor 50		56	61	kÿ -	
RPU3	Internal pull-up resistor 38		42	46	kÿ -	

symbol	parameter	Minimum value	Typical value	Maximum value	Unit	description
RPD3	Internal pull-down resistor 160		176	200	kÿ	-
RPU4	Internal pull-up resistor 54		60	66	kÿ	-
RPD4	Internal pull-down resistor 50		56	61	kÿ	-
RPU5	Internal pull-up resistor 38		42	46	kÿ	-
RPD5	Internal pull-down resistor 50.4		56	61.6	kÿ	-
RPU8k	8kohm pull-up resistor 6.7		8.54	10.54	kÿ	-
RPD8k	8kohm pull-down resistor 6.53		8.32	10.38	kÿ	-

In DDR3 mode, the DC electrical parameters are shown in Table 2-10 .

Table 2-10 DC electrical parameter table (VDDIO_DDR =1.5V, DDR3 mode)

symbol	parameter	Minimum value	Typical value	Maximum value	Unit	description
VDDIO_DDR	interface voltage	1.425	1.5	1.575	IN	·
Vref	reference voltage	0.49 * VDDIO_ DDR	0.5 * VDDIO_DD R	0.51 * VDDIO_DD R	·	ÿ0.49~0.51ÿ* VDDIO_DDR
VIH(DC) high level input voltage		Vref+0.1	-	VDDIO_DD R +0.3	IN	·
VIL(DC) low level input voltage		– 0.3	·	Vref–0.1	IN	·
VOH	High level output voltage	0.8* VDDIO_ DDR	·	(1+0.1) VDDIO_DD R	V	drive configurable
VOL	Low level output voltage	0	·	0.2*VDDIO_ DDR	V	drive configurable
John	High level output current-		10.50	10.83	mA	DDR drive impedance 34ÿ, When RTT=60
IOL	Low level output current-		10.50	10.83	mA	DDR drive impedance 34ÿ, When RTT=60
Output Impedance-		34	·	80	Oh	·

In DDR3 mode, AC electrical parameters are shown in Table 2-11 .

Table 2-11 AC electrical parameter table (VDDIO_DDR =1.5V, DDR3 mode)

Symbolic parameters	minimum value	maximum value	unit description
VIH(AC) high level input voltage Vref + 0.15		VDDIO_DDR+0.3	IN -
VIL(AC) low level input voltage-		Vref–0.15	IN -

In DDR3L mode, the DC electrical parameters are shown in Table 2-12 .

Table 2-12 DC Electrical Parameters (VDDIO_DDR =1.35V)

symbol	parameter	minimum value	Typical Value	Maximum	Unit	Description
VDDIO_DDR interface voltage		1.283	1.35	1.45	IN	
VREF	DDR interface reference voltage	0.49* VDDIO_DDR	0.5* VDDIO_DD R	0.51* VDDIO_DD R	IN	
HIV(DC)	High level input voltage 0.49*	VDDIO_DDR +0.125		VDDIO_DD R +0.3	IN	
WILL(DC)	Low level input voltage – 0.3			0.51* VDDIO_DD R -0.125	IN	
VOH	High level output voltage VDDIO_DDR -0.28				IN	
VOL	Low Level Output Voltage -			VDDIO_DD R +0.28	IN	
John	High level output current-		9.42	9.85	mA	DDR drive impedance 34ÿ, When RTT=60
IOL	Low level output current-		9.42	9.85	mA	DDR drive impedance 34ÿÿ When RTT=60

In DDR3L mode, AC electrical parameters are shown in Table 2-13 .

Table 2-13 AC Electrical Parameters (VDDIO_DDR =1.35V)

Symbolic parameters		533ÿ1600 Mbps		unit description	
		minimum value	maximum value		
VIH(AC)	AC high level input voltage 0.49* VDDIO_DDR + 0.25			IN	
WILL(AC)	AC low level input voltage-		0.51* VDDIO_DDR–0.25	IN	-

2.3.6 MIPI/LVDS Rx electrical parameters

LVDS differential DC electrical parameters are shown in Table 2-14 .

Table 2-14 LVDS differential DC electrical parameter table

symbol	parameter		Min	Typ	Max	Unit
VIDTH(SL)	Differential Input Threshold Voltage (VPÿ VM)	Sub-LVDS -70			70	mV
VIDTH(HS)		HiSPi(SLVS) -70			70	
VIDTH(HiVCM)		HiSPi(HiVCM)	-100		100	
VIDTH(DP)		D-PHY HS -70			70	
VIDTH(LV)		LVDS	-100		100	
VIDTH(ML)		Mini-LVDS -100			100	
VCM(SL)	Common Mode Voltage Range (VP+VM)/2	Sub-LVDS 0.5		0.9	1.3	IN
VCM(HS)		HiSPi(SLVS) 0.07		0.2	0.35	
VCM(HiVCM)		HiSPi(HiVCM)	0.66	0.90	1.17	
VCM(DP)		D-PHY HS 0.07		0.2	0.33	
VCM(LV)		LVDS	0.925	1.2	1.475	
VCM(ML)		Mini-LVDS 1.025		1.2	1.375	
VISVR (SL)	Single-ended Input Voltage Range VP,VM	Sub-LVDS 0.4			1.4	IN
VCM(HS)		HiSPi(SLVS) -0.04			0.49	
VCM(HiVCM)		HiSPi(HiVCM)	0.55		1.35	
VCM(DP)		D-PHY HS -0.04			0.46	
VCM(LV)		LVDS	0		1.8	

symbol	parameter		Min Typ Max Unit			
VCM(ML)		Mini-LVDS 0.825			1.575	
WALL (SL)	Internal Termination Resist Value	Sub-LVDS	80	100	120	Oh
ZID(HS)		HiSPi(SLVS)			125	
WALL (HiVCM)		HiSPi(HiVCM)			125	
WALL (LV)		LVDS			120	
ZID(ML)		Mini-LVDS			120	
ZID(DP)		D-PHY HS			125	

The MIPI parameters are shown in Table 2-15, Table 2-16 and Table 2-17 .

Table 2-15 MIPI HS (High Speed) DC parameter list

symbol	parameter	Min Typ Max Unit			
VTERM-EN Single-ended threshold for HS termination enable		·	·	450 mV	

Table 2-16 MIPI HS (High Speed) AC parameter list

symbol	parameter	Min Typ Max Unit			
ÿVCMRX(HF) Common-mode interface beyond 450MHz		·	·	100	·
ÿVCMRX(LF) Common-mode interface	50MHz-450MHz	-50	·	50	mV
CCM	Common-mode termination	·	·	60	pF

Table 2-17 MIPI LP (Low Power) DC parameter table

Symbolic parameters		Min Typ Max Unit			
VIHLP	Logic 1 input voltage	880	·	·	
VILLP	Logic 0 input voltage	·	·	550 mV	
VHYST Input hysteresis		25	·	-	

2.3.7 SDIO electrical parameters

The SDIO electrical performance parameter table (3.3V) is shown in Table 2-18 .

Table 2-18 SDIO electrical performance parameter table 3.3V

Symbolic parameters		Minimum value	Typical value	Maximum value	Unit	description
VDDIO	Supply voltage 2.97		3.3	3.6	IN	
VOH output high level 2.4					IN	
VOL output low level-				0.4	IN	
VIH input high level 2.0				VDD IO+ 0.3	IN	
VIL input low level -0.3				0.8	IN	
- Power-on time-				250	ms 0V to	VDDIO

The SDIO electrical performance parameter table (1.8V) is shown in Table 2-19 .

Table 2-19 SDIO electrical performance parameter table 1.8V

Symbolic parameters		Minimum value	Typical value	Maximum value	Unit	description
VDDIO	Supply voltage 1.62		1.8	1.98	IN	
VOH output high level 1.35					IN	
VOL output low level-				0.45	IN	
VIH input high level 1.17				VDDIO+0.3 V		
VIL input low level -0.3				0.63	IN	
- Power-on time-			-	250	ms 0V to	VDDIO

2.3.8 AUDIO CODEC electrical parameters

Audio Code electrical performance parameters are shown in Table 2-20, Table 2-21, Table 2-22, Table 2-23 and Table 2-24 .

Table 2-20 Overall index table

parameter	Minimum value	Typical value	Maximum value	Unit	description
Analog Circuit Power DEPARTMENT	3	3.3	3.6	V	with respect to AGND
VREF	·	AVDD/2	·	V	with respect to AGND

Table 2-21 DAC main indicators table

parameter	Minimum value	Typical value	Maximum value	Unit	description
Full scale output amplitude -		0.875	·	Vrms	maximum output signal swing

Table 2-22 ADC main indicators table

parameter	Minimum value	Typical value	Maximum value	Unit	description
Maximum input amplitude -		1	·	Vrms	ADC maximum input signal swing

Table 2-23 MICBIAS main indicators table

parameter	Minimum value	Typical value	Maximum value	Unit	description
Bias voltage -		2.1×AVDD/3 .3	·	V	Microphone bias voltage
Maximum output current-		·	3	mA	-

Table 2-24 MICPGA main indicators

parameter	Minimum value	Typical value	Maximum value	Unit	description
Input voltage range-		1	·	Vrms	maximum input signal swing
input resistance-		10	12	kÿ	Input impedance of MICPGA

2.4 PCB Design Recommendations

For details on PCB design, please refer to the "Hi3519V100 Hardware Design User Guide".

2.5 Interface Timing

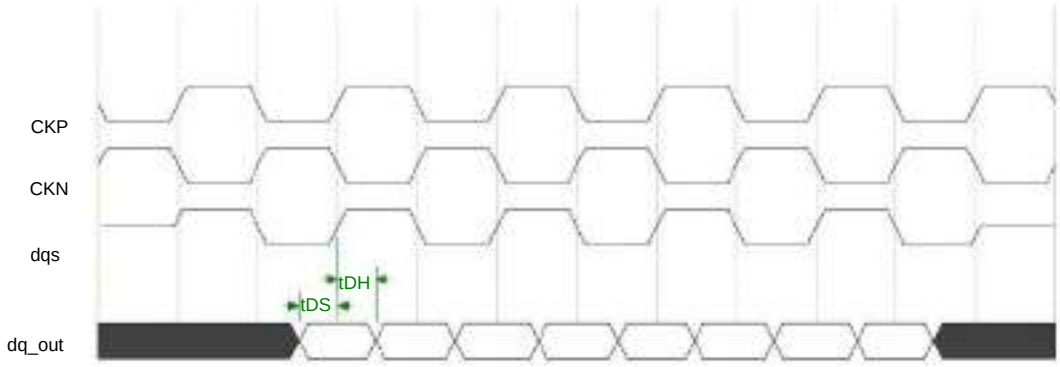
2.5.1 DDR interface timing

2.5.1.1 Write Operation Timing

Write operation timing of dqs_out relative to dq_out

The main timing parameters for the write timing of dqs_out relative to dq_out are tDS and tDH.

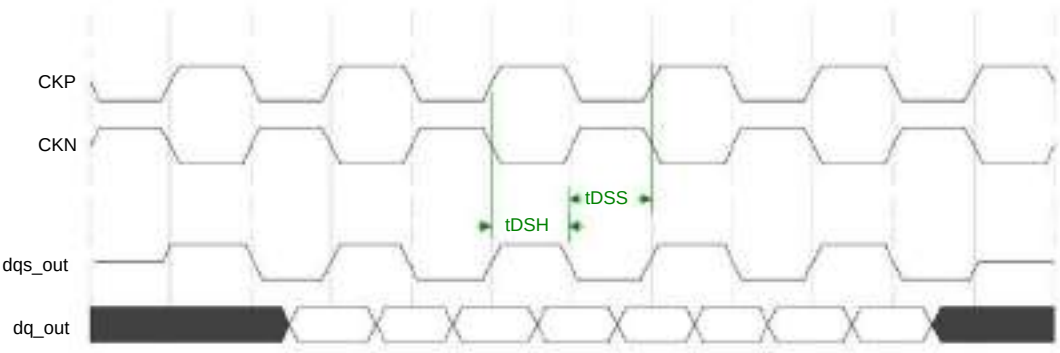
Figure 2-6 The write operation timing diagram of dqs_out relative to dq_out in DDR3



The write operation timing of dqs_out relative to ck

The write operation timing of dqs_out relative to ck. The timing sequence of DDR3 is shown in Figure 2-7 .

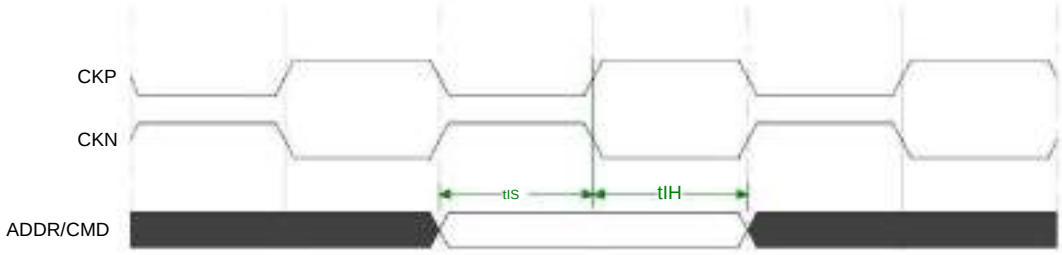
Figure 2-7 The timing diagram of the write operation of dqs_out relative to ck in DDR3



Command and address write timing relative to ck

The write operation timing of commands and addresses relative to ck is shown in Figure 2-8 .

Figure 2-8 Timing diagram of write operation of command and address relative to ck



2.5.1.2 Read Operation Timing

Command and address read timing relative to ck

"Command and address read operation timing relative to ck" is the same as "command and address write operation timing relative to ck " .

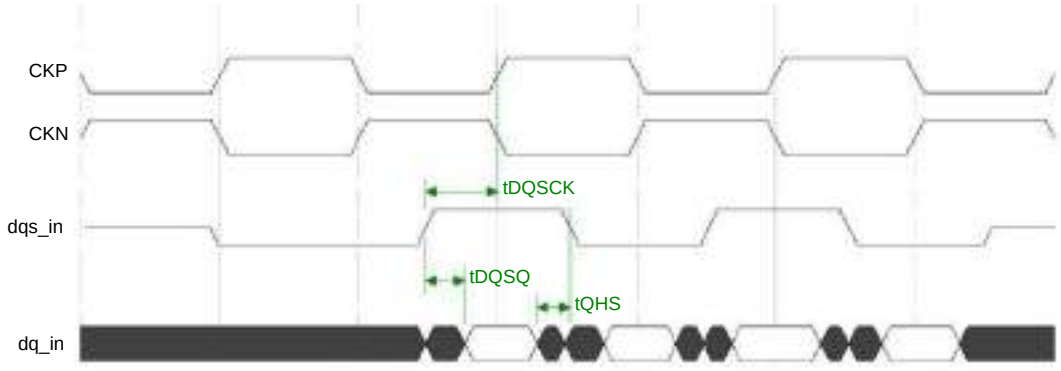
Read operation timing of dqs_in relative to dq_in

The read operation timing of dqs_in relative to dq_in is divided into DDRn SDRAM output timing and DDRPHY terminal dqs_in and dq_in timing.

For DDR SDRAM output timing, ideally, DQS and ck are in the same phase, but in reality, DQS has a skew of tDQSCK relative to CK. tDQSCK is 0.35ns. tDQSQ is the jitter between dq and dqs, it is the jitter of the latest effective dq relative to dqs, the value is 0.2ns, tQHS is the jitter of the earliest effective dq relative to dqs, its value is 0.3ns.

DDR3 SDRAM output timing is shown in Figure 2-9 .

Figure 2-9 DDR3 SDRAM output timing diagram



2.5.1.3 Timing parameters

The timing of the DDR interface meets the standard protocol of JEDEC (JESD79-2E and JESD79-3B). The timing described in this article is the timing of the output of the DDR PHY side.

DDR3-1600 SDRAM clock parameters are shown in Table 2-25 and Table 2-26 .

Table 2-25 DDR3 Clock Parameters

parameter	typical value	unit
memory clock frequency	800.00	MHz
PLL Jitter	0.140	ns
PLL duty cycle	47.000	%
clock skew	0.070	ns

Table 2-26 DDR3 SDRAM memory parameter list (DDR3-1600)

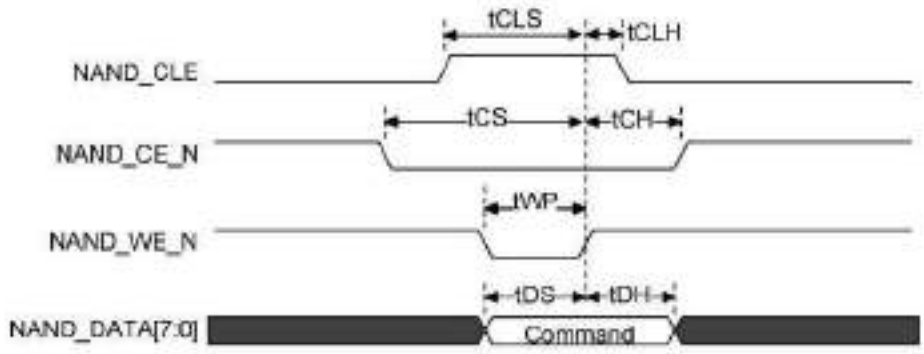
parameter	Symbol Typical	Value Unit	
DQS falling edge relative to DDR clock setup time	tDSS	0.18	TCK
DQS falling edge hold time relative to DDR clock	tDSH	0.18	TCK
DQ/DM setup time relative to DQS	tDS	0.010	ns
DQ/DM hold time relative to DQS	tDH	0.045	ns
Skew of DQS and DQ	tDQSQ 0.100		ns
Address and command setup time relative to DDR clock	tIS	0.170	ns
Address and command hold time relative to DDR clock	tIH	0.120	ns
Skew relative to DDR clock at DQS output	tDQSCK 0.225		ns

2.5.2 NANDC Interface Timing

2.5.2.1 Command Cycle Timing

The timing of NANDC command cycle is shown in Figure 2-10 .

Figure 2-10 NANDC command cycle timing diagram



说明

The high-level width and low-level width of NAND_WE_N and NAND_RE_N can be set through the NF_PULSE_WIDTH register of the NAND Flash controller. Therefore, some parameters in the timing diagram of the NANDC interface will change with the setting of this register. In the parameter table in this section, it is uniformly expressed as "configurable".

The timing parameters of the NANDC command cycle are shown in Table 2-27 .

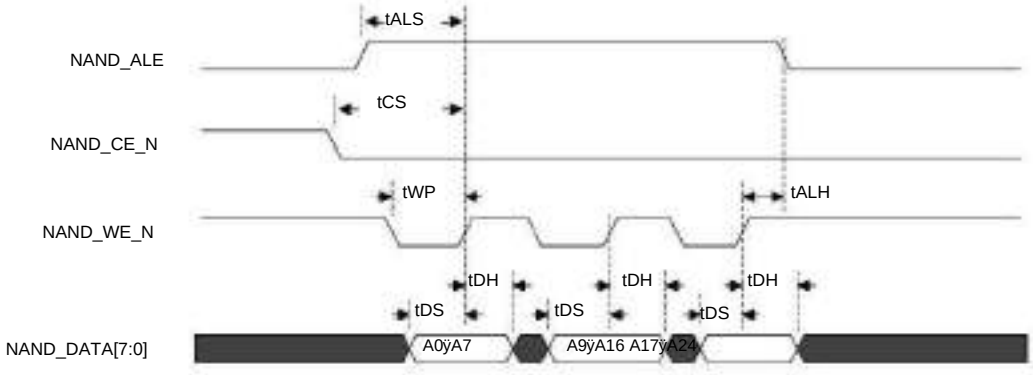
Table 2-27 NANDC command cycle timing parameter list

parameter	Symbol Min Max Max Unit Explanation				
NAND_CLE setup time tCLS		15		ns	
NAND_CLE hold time tCLH 10				ns	
NAND_CE_N setup time tCS		15		ns can be configured	
NAND_CE_N hold time tCH		10		ns can be configured	
NAND_WE_N pulse width tWP		15		ns can be configured	
data creation time	tDS	10		ns can be configured	
data hold time	tDH	10	-	ns can be configured	

2.5.2.2 Address Cycle Timing

The NANDC address cycle timing is shown in Figure 2-11 .

Figure 2-11 Timing Diagram of NANDC Address Cycle



The timing parameters of the NANDC address cycle are shown in Table 2-28 .

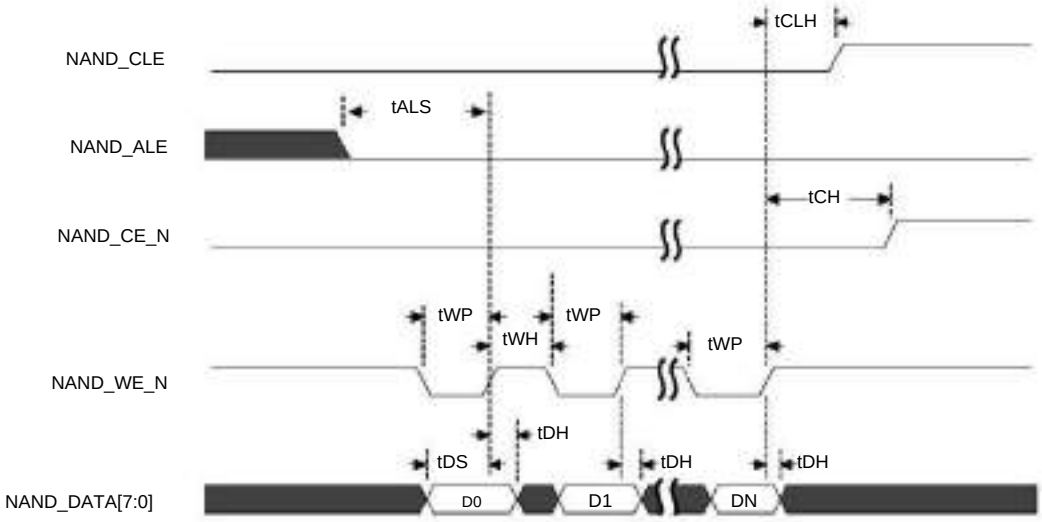
Table 2-28 NANDC Address Cycle Timing Parameters

parameter	Symbol Min	Max	Max	Unit	Explanation
NAND_CE_N setup time tCS		15		ns	can be configured
NAND_WE_N pulse width tWP 15				ns	can be configured
NAND_ALE setup time tALS 15				ns	
NAND_ALE hold time tALH 10				ns	
data creation time	tDS 10			ns	can be configured
data hold time	tDH 10		-	ns	can be configured

2.5.2.3 Write data timing

The timing of writing data in NANDC is shown in Figure 2-12 .

Figure 2-12 NANDC write data timing diagram



The timing parameters for writing data in NANDC are shown in Table 2-29 .

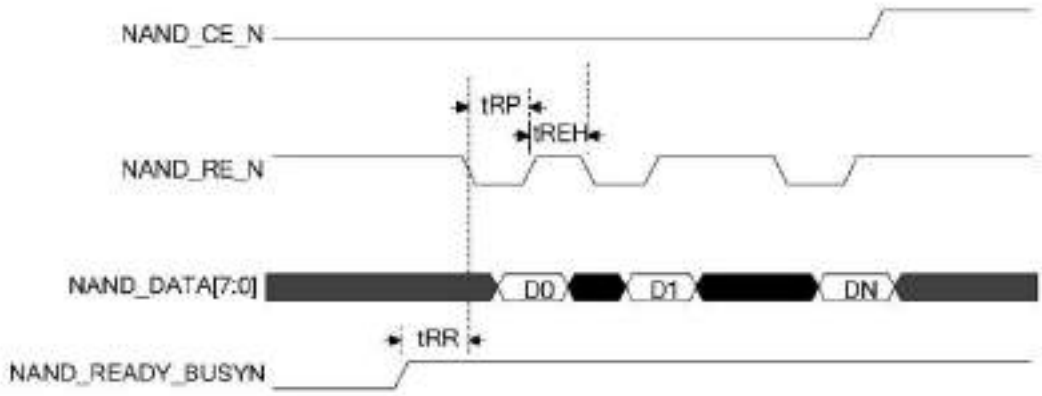
Table 2-29 NANDC Write Data Timing Parameters

parameter	Symbol	Min	Max	Unit	Explanation
NAND_CE_N hold time tCH		10		ns	can be configured
NAND_WE_N pulse width tWP		15		ns	can be configured
NAND_ALE setup time tALS		15		ns	can be configured
data creation time	tDS	10		ns	can be configured
data hold time	tDH	10		ns	can be configured
NAND_WE_N high level hold time	tWH	15	-	ns	can be configured

2.5.2.4 Read data timing

The timing sequence of NANDC read data is shown in Figure 2-13 .

Figure 2-13 NANDC read data timing diagram



The timing parameters of NANDC read data are shown in Table 2-30 .

Table 2-30 NANDC Read Data Timing Parameters

parameter	Symbol Min Max Max Unit Explanation				
NAND_RE_N becomes low waiting time tRR		15		ns can be configured	
NAND_RE_N pulse width	tRP	15		ns can be configured	
NAND_RE_N high level width tREH 15			-	ns can be configured	

Note: tRR delay is configurable.

2.5.3 SFC Interface Timing

The timing sequence of SFC input direction is shown in Figure 2-14 and Figure 2-15 .

Figure 2-14 Timing Diagram of SFC Input Direction - SDR Mode

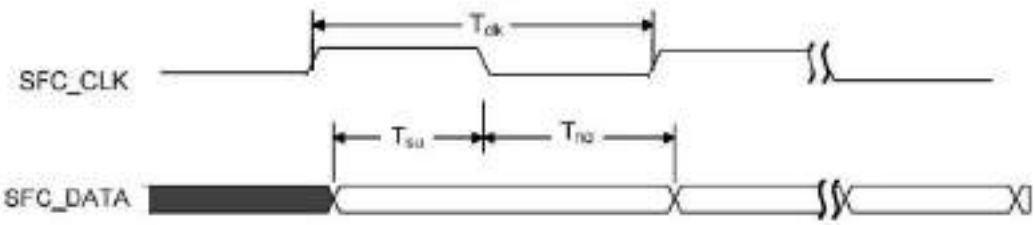
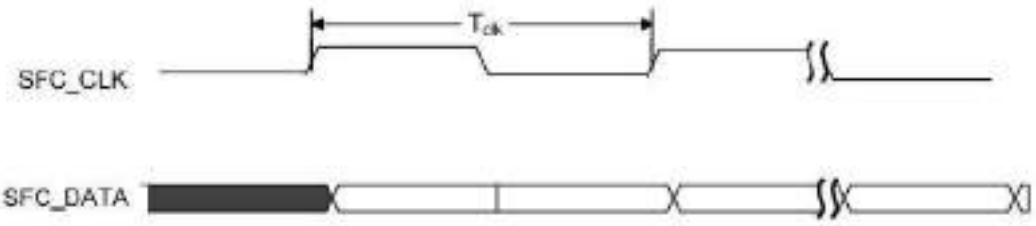


Figure 2-15 SFC input direction timing diagram - DDR mode



The timing parameters of the SFC input direction are shown in Table 2-31 .

Table 2-31 SFC Input Direction Timing Parameters

parameter	Symbol	Min	Typ	Max	Unit
SFC_CLK clock period (SDR)	Tclk	8		83.2	ns
SFC_CLK clock period ÿDDRÿ	Tclk	10		83.2	ns
Input signal settling time requirement Tsu		2			ns
Input signal hold time requirement Thd		0.5			ns

The timing sequence of SFC output direction is shown in Figure 2-16 and Figure 2-17 .

Figure 2-16 SFC output direction timing diagram - SDR mode

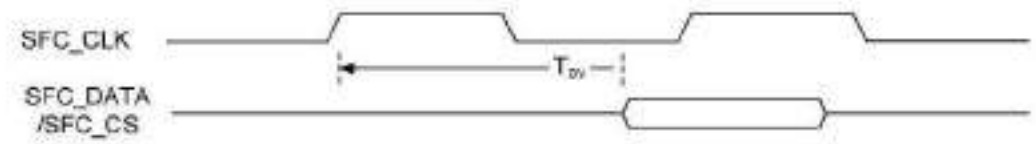
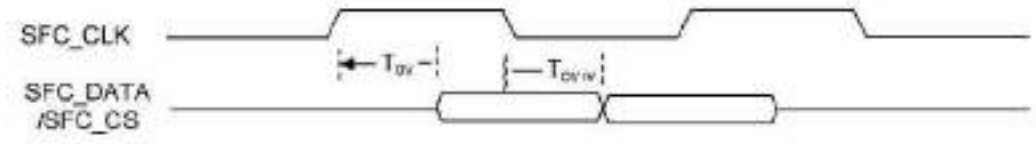


Figure 2-17 SFC output direction timing diagram - DDR mode



The timing parameters of the SFC output direction are shown in Table 2-32 .

Table 2-32 SFC output direction timing parameter list

parameter	Symbol	Min	Typ	Max	Unit
SFCCLK clock period (SDR)	T	8		83.2	ns
SFCCLK clock period ÿDDRÿ	T	10		83.2	ns
Output data signal delay	Mix	5		T-5	ns
Output chip select signal delay	Mix	5	-	T-5	ns

2.5.4 Ethernet MAC Interface Timing

2.5.4.1 RMII Interface Timing

Figure 2-18 shows the 100Mbit/s receiving timing of the RMII interface .

Figure 2-18 RMII interface 100Mbit/s receiving timing

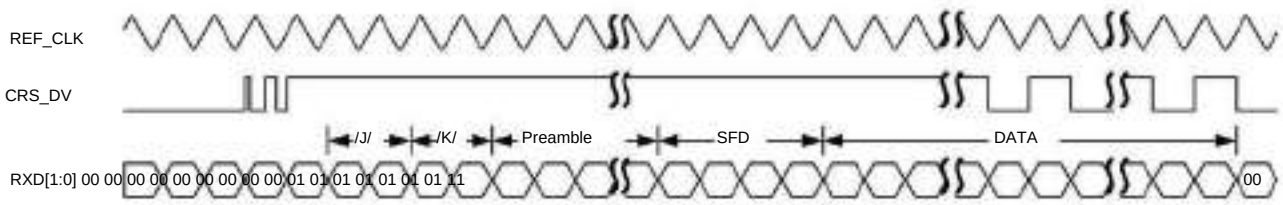


Figure 2-19 shows the 100Mbit/s sending timing of the RMII interface .

Figure 2-19 RMII interface 100Mbit/s sending timing

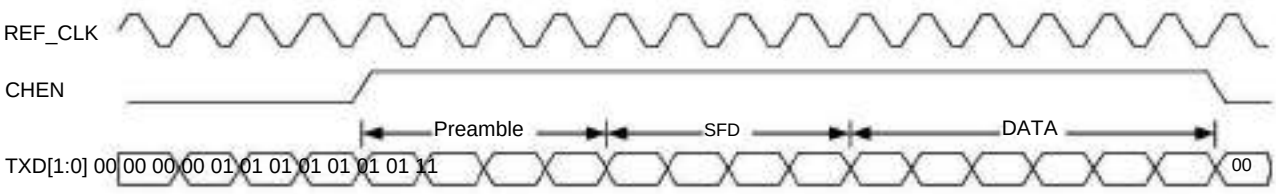


Figure 2-20 shows the 10Mbit/s receiving timing of the RMII interface .

Figure 2-20 RMII interface 10Mbit/s receiving timing

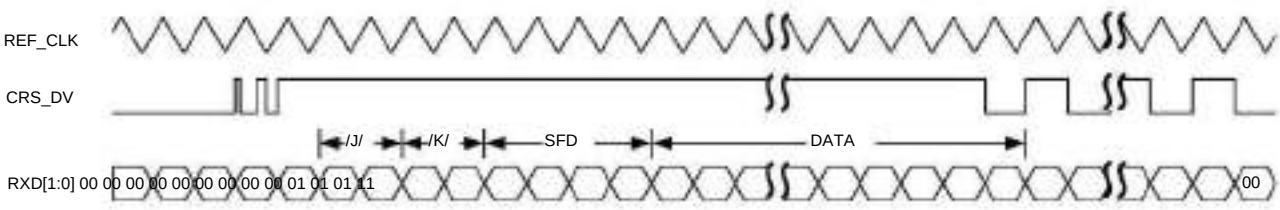
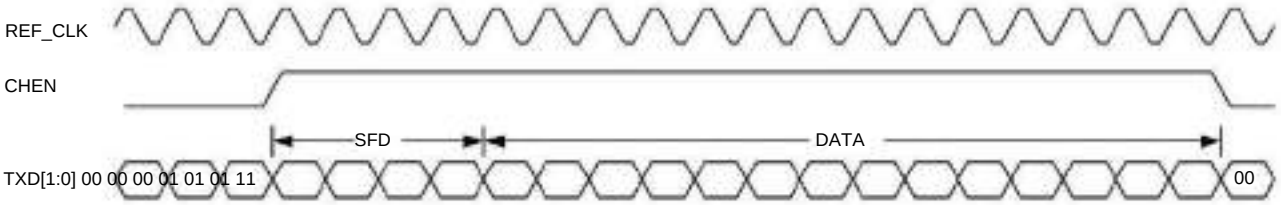


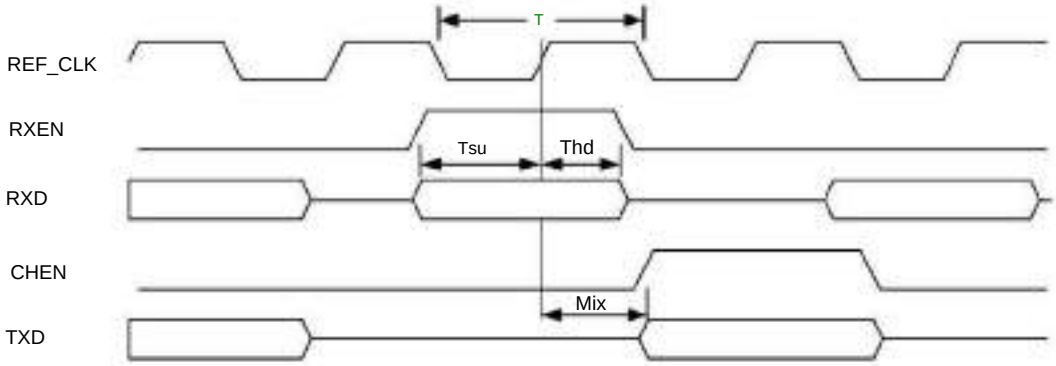
Figure 2-21 shows the 10Mbit/s transmission timing of the RMII interface .

Figure 2-21 RMII interface 10Mbit/s sending timing



The timing parameters of the RMII interface are shown in Figure 2-22 .

Figure 2-22 RMII interface timing parameters



The timing parameters of the RMII interface are described in Table 2-33 .

Table 2-33 RMII interface timing parameter description

parameter	symbol	Signal	min max unit		
RMII clock period T		REF_CLK	20	20	ns
RMII signal setup time Tsu(RX)		CRS_DV/RXD[1:0] 4			ns
RMII signal hold time Thd (RX)		CRS_DV/RXD[1:0] 2			ns
RMII output signal delay Tov (TX)		TXEN/TXD[1:0]	3	16	ns

2.5.4.2 RGMII Interface Timing

Figure 2-23 shows the 1000Mbit/s receiving timing of the RGMII interface .

Figure 2-23 RGMII interface 1000Mbit/s receiving timing

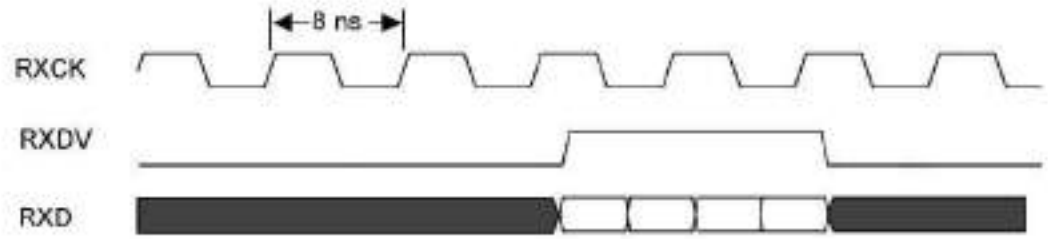
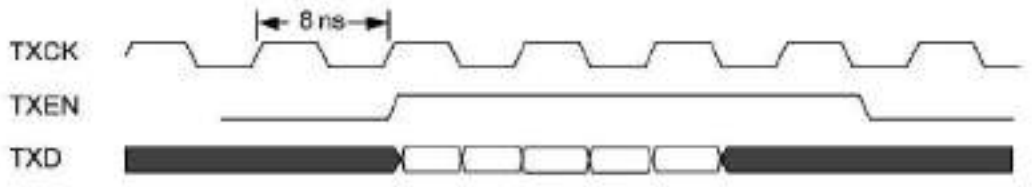


Figure 2-24 shows the 1000Mbit/s sending timing of the RGMII interface .

Figure 2-24 RGMII interface 1000Mbit/s sending timing



The timing parameters of the RGMII interface are described in Table 2-34 .

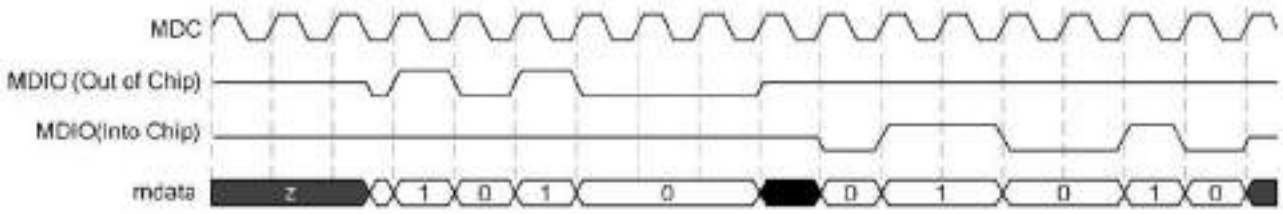
Table 2-34 RGMII interface timing parameter description

parameter	symbol	Signal	min max unit		
RGMII clock period T		RXCKÿTXCK	8	8	ns
RGMII signal setup time	TsuÿRXÿ RXERÿRXDVÿ RXD[3:0]		1		ns
RGMII signal hold time	ThdÿRXÿ RXERÿRXDVÿ RXD[3:0]		1		ns
RGMII output signal delay	Answer (TX) TXD[3:0]ÿ	TXEN -0.5		0.5	ns

2.5.4.3 MDIO Interface Timing

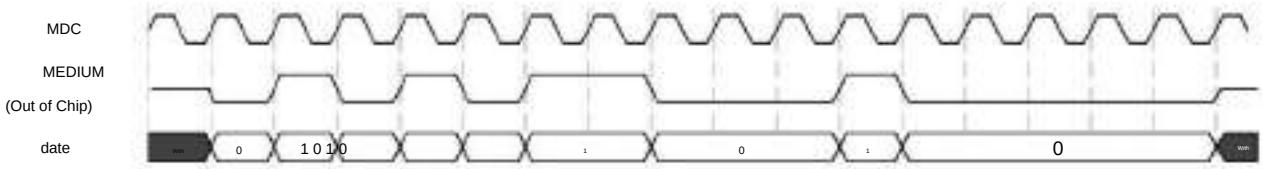
The MDIO interface read timing is shown in Figure 2-25 .

Figure 2-25 MDIO interface read timing



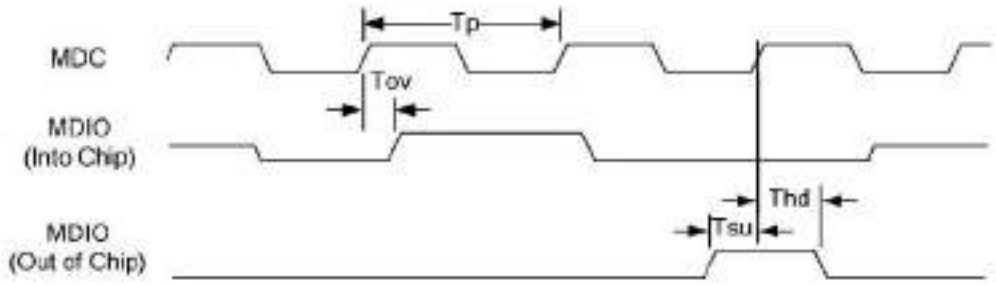
The write sequence of MDIO interface is shown in Figure 2-26 .

Figure 2-26 MDIO interface write timing



The timing parameters of the MDIO interface are shown in Figure 2-27 .

Figure 2-27 MDIO interface receiving timing parameters



The timing parameters of the MDIO interface are described in Table 2-35 .

Table 2-35 MDIO interface timing parameters

parameter	Symbol Signal Min Max Unit				
MDIO receive data delay time Tov MDIO			0	300	ns
MDIO clock cycle	Tp MDCK 400			666	ns
MDIO send data setup time Tsu MDIO			10		ns
MDIO send data hold time Thd MDIO			10	-	ns

2.5.5 VI Interface Timing

Figure 2-28 shows the timing sequence of the VI interface in CMOS mode .

Figure 2-28 Timing diagram of VI interface

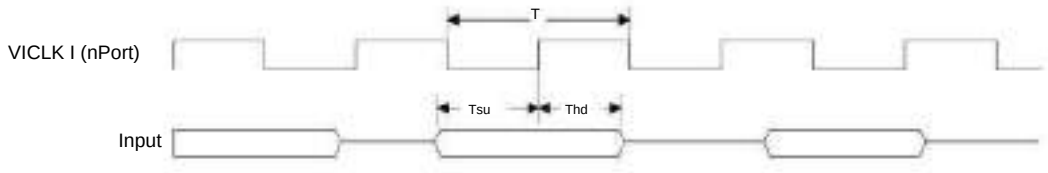


Table 2-36 lists the timing parameters of the VI interface .

Table 2-36 Timing parameter list of VI interface

parameter	Symbol	Min	Typ	Max	Unit
VICLK clock period	T		6.73		ns
Input Signal Settling Time Requirements	Tsu	2.5			ns
Input Signal Hold Time Requirements	Thd	2.0		-	ns

2.5.6 VO Interface Timing

The timing sequence of the BT.656 interface is shown in Figure 2-29 .

Figure 2-29 BT.656 interface timing

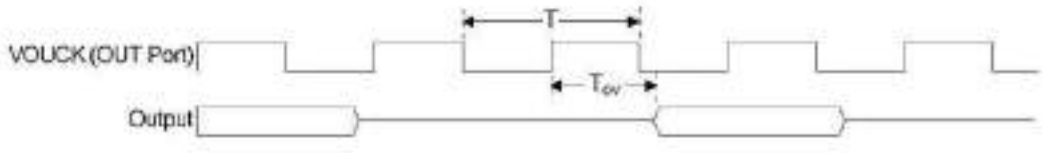


Table 2-37 lists the timing parameters of the BT.656 interface.

Table 2-37 BT.656 interface timing parameter table

parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock period	T		37		ns
output signal delay	Mix	T/2-1.5	-	T/2+1.5	ns

The timing sequence of the BT.1120 interface is shown in Figure 2-30 .

Figure 2-30 BT.1120 interface timing

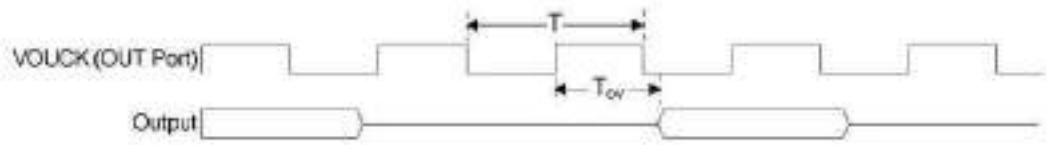


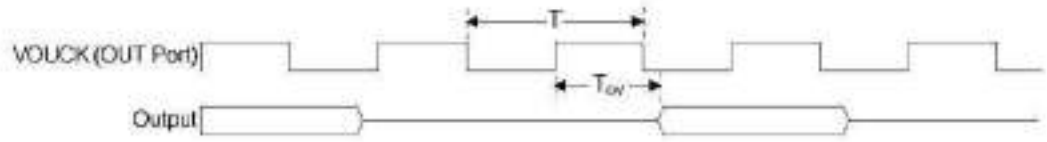
Table 2-38 lists the timing parameters of the BT.1120 interface .

Table 2-38 BT.1120 interface timing parameter list

parameter	Symbol Min Typ Max Unit				
VOUCLK clock period	T	6.734		13.46	ns
output signal delay	Mix	T/2-1.5		T/2+1.5	ns

The timing sequence of the LCD interface is shown in Figure 2-31 .

Figure 2-31 LCD interface timing



The timing parameters of the LCD interface are shown in Table 2-39 .

Table 2-39 LCD interface timing parameter list

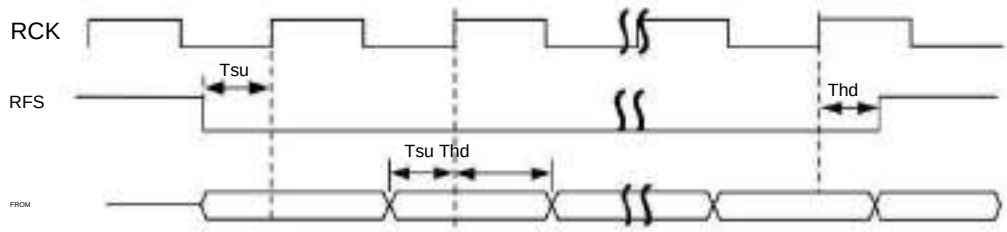
parameter	Symbol Min Typ Max Unit				
VOUCLK clock period	T	37		500	ns
output signal delay	Mix	T/2-1.5 -		T/2+1.5	ns

2.5.7 AIAO Interface Timing

2.5.7.1 I2S interface timing

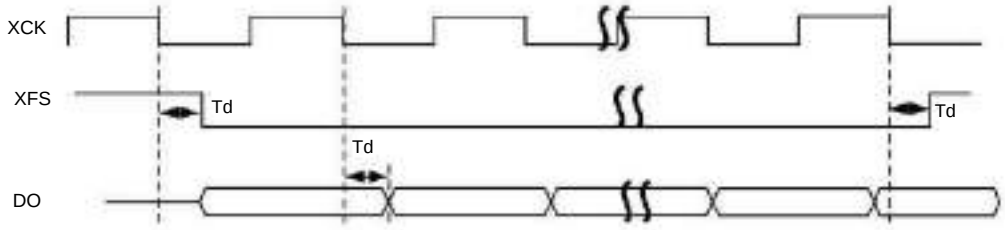
I ^{2} The receiving sequence of the S interface is shown in Figure 2-32 .

Figure 2-32 I 2 S interface receiving timing diagram



I 2 Figure 2-33 shows the sending sequence of the S interface.

Figure 2-33 I 2 S interface sending timing diagram



I 2 Table 2-40 lists the timing parameters of the S interface .

Table 2-40I 2 S interface timing parameter table

parameter	Symbol	Min	Typ	Max	Unit
Input signal settling time	Tsu	10			ns
Input signal hold time	Thd	10			ns
output signal delay	Td	0	-	8	ns

2.5.7.2 PCM Mode Interface Timing

Figure 2-34 shows the receiving timing of the PCM interface.

Figure 2-34 PCM interface receiving timing diagram

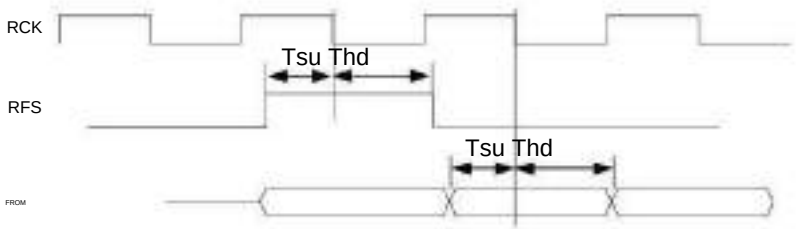


Figure 2-35 shows the sending sequence of the PCM interface.

Figure 2-35 PCM interface sending timing diagram

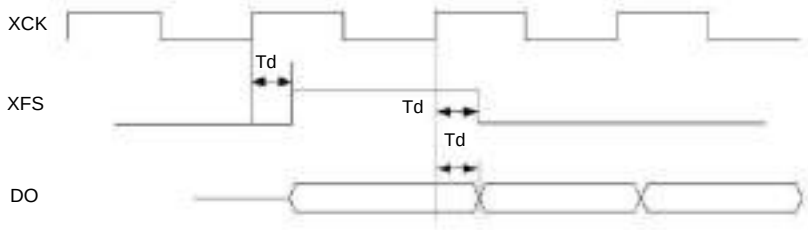


Table 2-41 lists the timing parameters of the PCM interface .

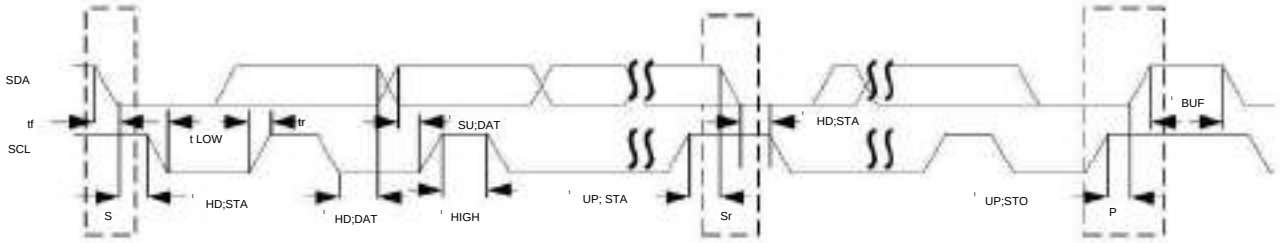
Table 2-41 PCM interface timing parameter list

parameter	Symbol	Min	Typ	Max	Unit
Input signal settling time	Tsu	10			ns
Input signal hold time	Thd	10			ns
output signal delay	Td	0	-	8	ns

2.5.8 I2C Timing

I 2 C The transmission timing is shown in Figure 2-36 .

Figure 2-36 I 2 C Transmission Timing Diagram



I 2 The timing parameters of the C interface are shown in Table 2-42 .

Table 2-42I 2 C interface timing parameter table

parameter	symbol	standard mode		fast mode		unit
		min	max	min	max	
SCL clock frequency	fSCL	0	100	0	400	kHz
Start hold time	tHD;STA	4.0		0.6	-	ÿs

parameter	symbol	standard mode		fast mode		unit
		min max	min max			
SCL low period	tLOW 4.7		·	1.3	·	ÿs
SCL high level period	tHIGH 4.0		·	0.6	·	ÿs
boot build time	tSU;ST A	4.7	·	0.6	·	ÿs
data hold time	tHD;DA T	0	3.45	0	0.9	ÿs
data creation time	tSU;DA T	250	·	100	·	ns
SDA, SCL rise time tr		·	1000	20+0.1C b	300	ns
SDA, SCL fall time tf		·	300	20+0.1C b	300	ns
end build time	tSU;ST O	4.0	·	0.6	·	ÿs
Bus release time between start and end	tBUF	4.7	·	1.3	·	ÿs
bus load	Cb	·	400	·	400	pF
Low level noise margin	VnL	0.1VDD -		0.1VDD -		IN
High level noise margin	VnH	0.2VDD -		0.2VDD -		IN

2.5.9 SPI Interface Timing

说明

In Figure 2-37 to Figure 2-39 , the meanings of the following abbreviations or letters remain unchanged:

MSB:Most Significant Bit

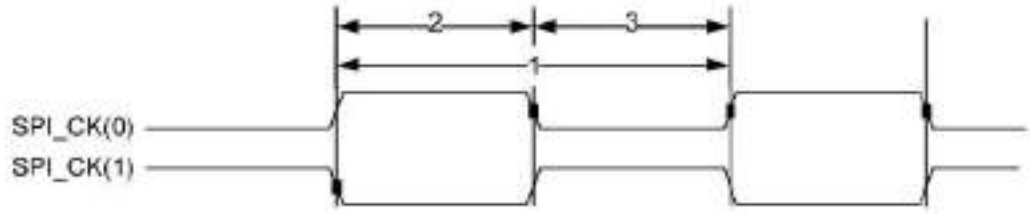
LSB:Least Significant Bit

SPI_CK(0):spo=0

SPI_CK(1):spo=1

SPI interface clock timing is shown in Figure 2-37 .

Figure 2-37 SPICK Timing



The interface timing in SPI master mode is shown in Figure 2-38 and Figure 2-39 respectively .

Figure 2-38 Interface Timing in SPI Master Mode (sph=1)

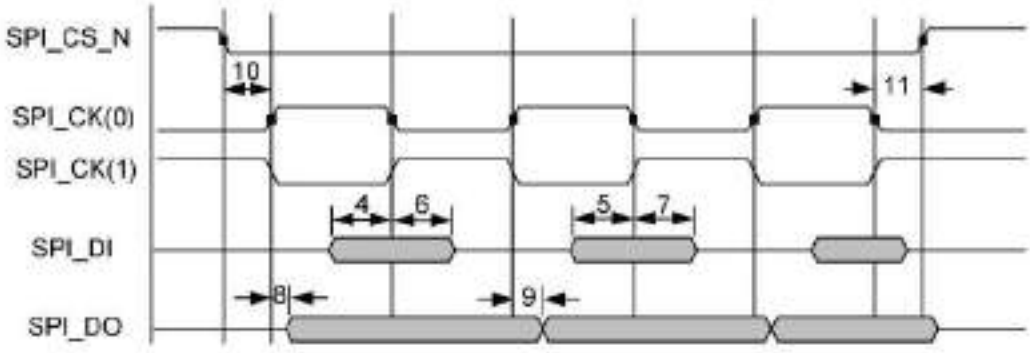
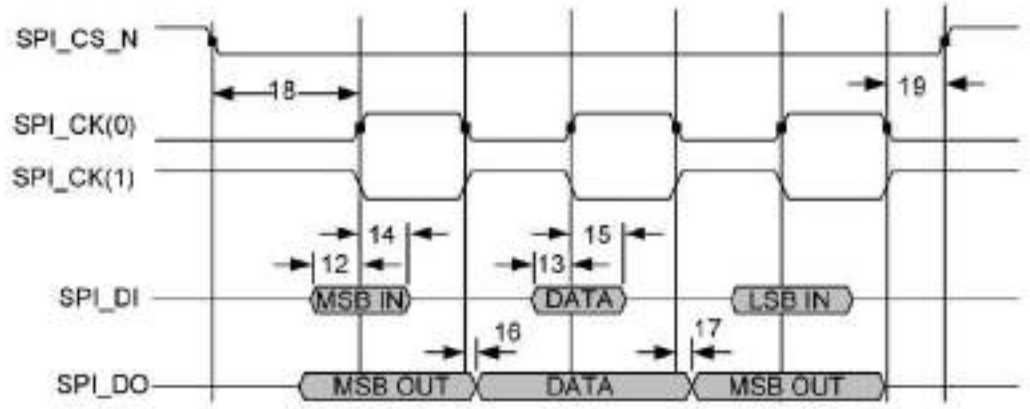


Figure 2-39 Interface Timing in SPI Master Mode (sph=0)



The timing parameters of the SPI interface are shown in Table 2-43 .

Table 2-43 SPI interface timing parameters

No number		Symbol	Min	Typ	Max	Unit	Remarks
1	Cycle time, SPI_CK	tc	2000/Fss pclk	-	65024000/ Fsspclk	ns	Fsspclk to in MHz

No number		Symbol	Min	Typ	Max	Unit	Remarks
2	Pulse duration, SPI_CK high (All Master Modes)	tw1	·	1/2 tc	·	ns	
3	Pulse duration. SPI_CK low (All Master Modes)	tw2	·	1/2 tc	·	ns	
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	·	1/2 tc	·	ns	
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	·	1/2 tc	·	ns	
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	·	1/2 tc	·	ns	
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	·	1/2 tc	·	ns	
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	0	·	·	ns	
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	0	·	·	ns	
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	·	tc	·	ns	
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	·	1/2 tc	·	ns	
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	·	1/2 tc	·	ns	
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	·	1/2 tc	·	ns	
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	·	1/2 tc	·	ns	
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	·	1/2 tc	-	ns	

No number		Symbol Min Typ Max Unit Remarks					
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	0	·	·	ns	
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	0	·	·	ns	
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	·	1/2 tc	·	ns	
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	·	tc	-	ns	

2.5.10 MIPI Rx Interface Timing

The MIPI Rx timing parameters are shown in Table 2-44 .

Table 2-44 MIPI Rx Timing Parameters

symbol	parameter	Min Typ Max Unit			
FMAX	data rate	·	·	1.5G	bps
TPERIOD differential clock period		1.33	T	·	ns
TDUTY differential clock duty cycle 0.45T			·	0.55T	ns
TSET	Differential clock setup time 0.15*UI		·	·	ns
THD	Differential clock hold time 0.15*UI		·	·	ns
THREE	Differential Clock Rise Time (20-80%)	0.15	·	·	ns
TFALL	Differential Clock Fall Time (20-80%)	0.15	·	0.3*UI	ns

说明

UI is equal to T/2.

2.5.11 SDIO/MMC Interface Timing

Figure 2-40 shows the timing sequence of data input and output on a single edge .

Figure 2-40 Timing diagram of data input and output directions on a single edge

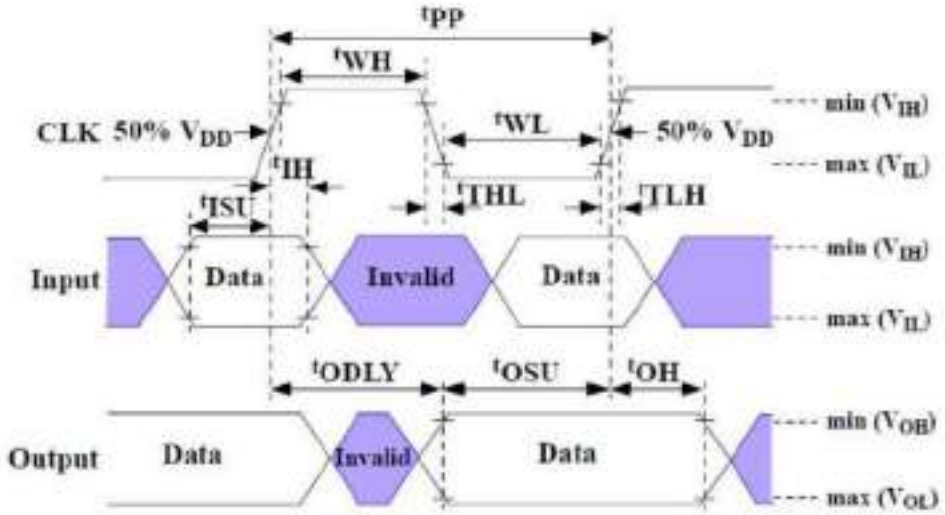
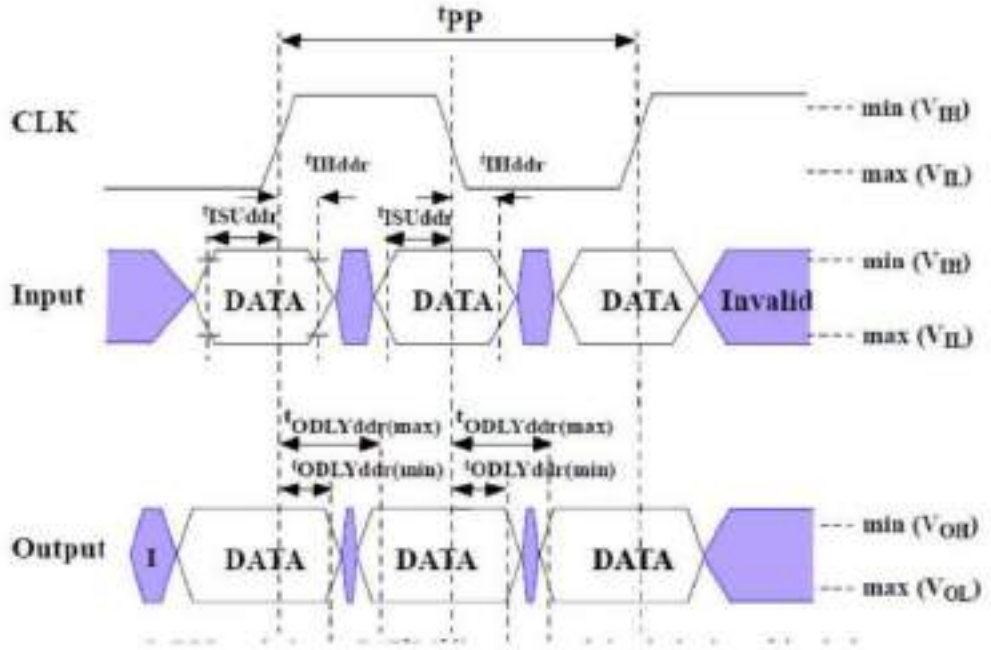


Figure 2-41 shows the timing sequence of data input and output on both edges .

Figure 2-41 Timing diagram of data input and output directions on both edges



The SDIO/MMC timing parameter list is shown in Table 2-45 .

Table 2-45 SDIO/MMC Timing Parameters

speed mode	maximum frequency (MHz)/cycle (ns)	minimum hold time	minimum settling time	The maximum value of the card output delay	Card clock high time
MMC_HS400	100MHz 10ns 0.4ns		0.4ns	_	(0.45~0.55) clock cycle
MMC_HS200	100MHz 10ns 0.8ns		1.4ns	_	
MMC DDR ÿCMD lineÿ	50MHz 20ns 3.0ns		3.0ns	13.7ns	
MMC DDR ÿDAT lineÿ	50MHz 20ns 2.5ns		2.5ns	7.0ns	
MMC_HS	50MHz 20ns 3.0ns		3.0ns	13.7ns	
SD_SDR104	100MHz 10ns 0.8ns		1.4ns	10.0ns	
SD_SDR50	100MHz 10ns 0.8ns		3.0ns	7.5ns	
SD_DDR50 ÿCMD lineÿ	50MHz 20ns 0.8ns		6.0ns	13.7ns	
SD_DDR50 ÿDAT lineÿ	50MHz 20ns 0.8ns		3.0ns	7ns	
SD_SDR25	50MHz 20ns 2.0ns		6.0ns	14ns	
SD_SDR12	25MHz 40ns 5.0ns		5.0ns	14ns	
SD_HS	50MHz 20ns 2.0ns		6.0ns	14ns	
SD_DS	25MHz 40ns 5.0ns		5.0ns	14ns	
Identification Mode	400KHz 2.5us 5.0ns		5.0ns	50ns	

Table of contents

illustration catalog

table of contents

3 system

3.1 Reset

3.1.1 Overview

The reset management module performs unified management on the reset of the entire chip and the reset of each functional module, including:

Management and control of power-on reset

System soft reset, function module independent soft reset control reset signal

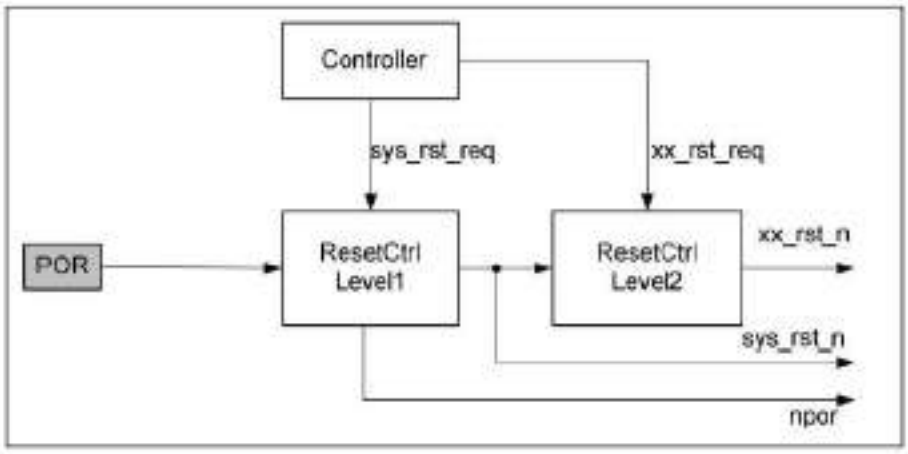
is synchronized to the corresponding clock domain of each module

The reset management module generates reset signals for each functional module inside the chip

3.1.2 Reset Control

The reset signal control is shown in Figure 3-1 .

Figure 3-1 Reset signal control diagram



BY	Chip internal power-on reset (Power-On-Reset) module.
system	Global soft reset request signal originating from the
xx_rst_req	controller. sys_rst_req Sub-module independent soft reset request signal, derived from CRG control register.
xx_rst_n, sys_rst_n, npor	Reset signal.

The classification of reset signals is shown in Table 3-1 .

Table 3-1 Reset signal classification table

Reset signal type generation method		use
Global hard reset npor from internal power-on reset POR module		Perform a global reset on the entire chip.
Global soft reset sys_rst_n	Software configures the global soft reset register of the system controller	Reset all modules in the chip, except the clock reset circuit, test circuit and some registers that will not be soft reset.
Submodule reset xx_rst_n	Software configuration of the submodule reset control register of the CRG control register	Individual reset of each sub-module of the chip.

3.1.3 Reset configuration

3.1.3.1 Power-on reset

To complete the power-on reset process, the following conditions must be met at the same time:

The internal POR module generates a low-level pulse; and the low-level maintenance time is greater than 12 XIN crystal oscillator clock cycles.

The clock input from the crystal oscillator clock input pin XIN is stable.

3.1.3.2 System reset

There are two ways to implement a system reset:

Power-on reset.

Global soft reset, controlled by the system controller.

3.1.3.3 Soft reset

Soft reset control is realized by configuring the corresponding CRG controller. For specific configuration, please refer to the description of the reset register of each module.

注意

After the system soft reset request is issued, the circuit must wait for at least 360 system clock cycles to complete the reset cancellation. During these 360 system clock cycles, the system soft reset request cannot be sent again, otherwise the system state is chaotic and there may be no cannot complete the reset operation.

Each module's individual soft reset will not be canceled automatically. For example, when the reset of a module is configured as 1, the module is in the reset state. It must be configured as 0 again to cancel the reset of the module.

3.2 Clock

3.2.1 Overview

The clock management module performs unified management on chip clock input, clock generation and control, including:

Management and control of clock input Clock

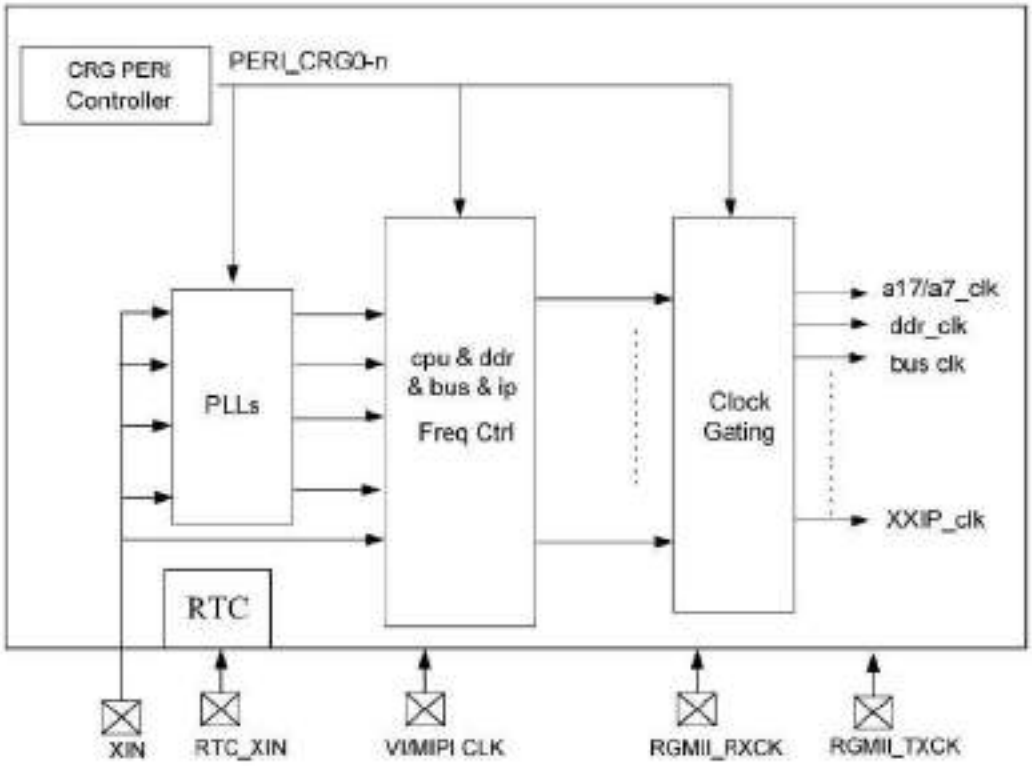
frequency division and control to

generate working clocks for each module

3.2.2 Functional block diagram

Figure 3-2 shows the functional block diagram of the clock management module .

Figure 3-2 Functional block diagram of the clock management module

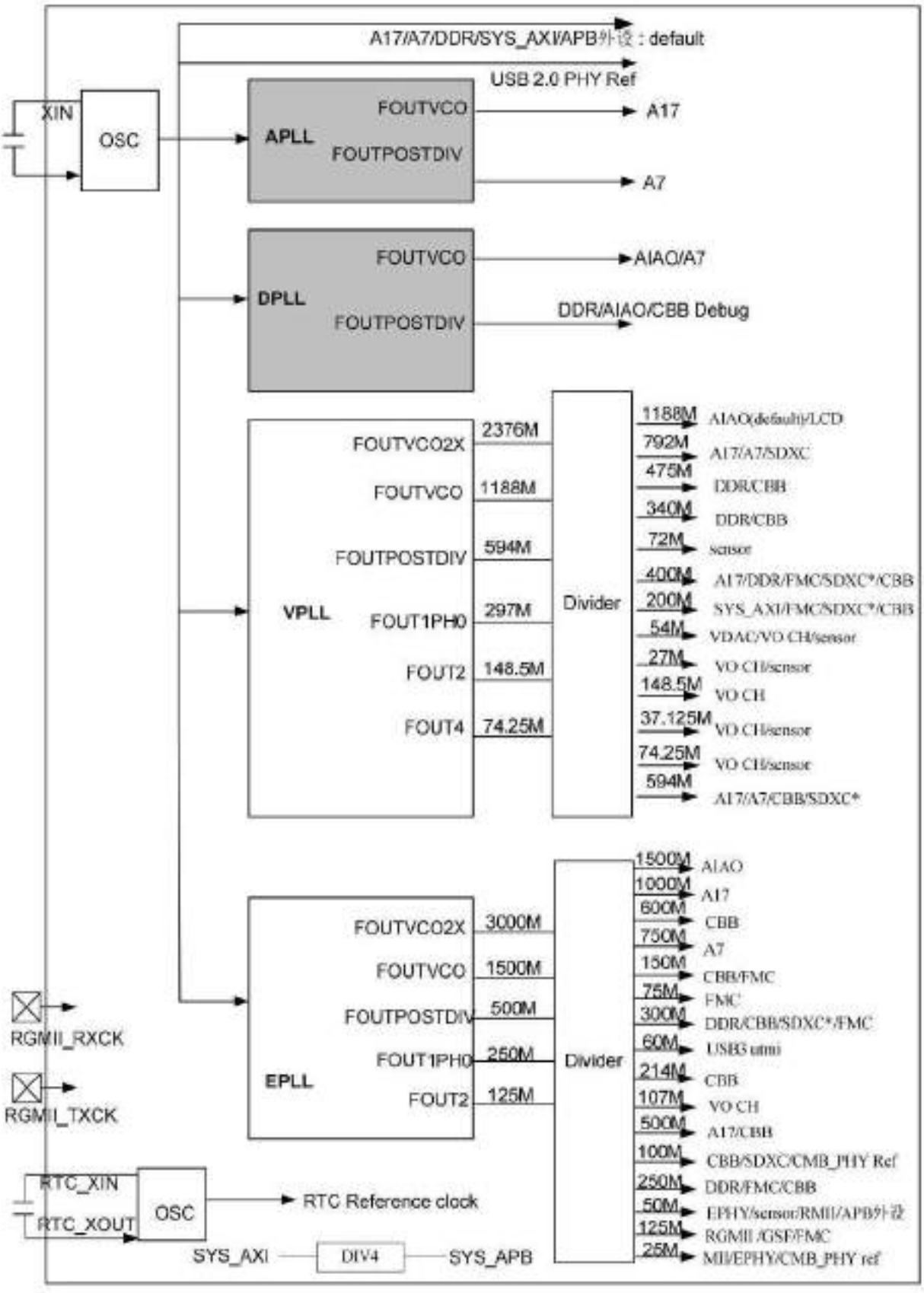


Note: XIN in the figure is the PLL input clock, which is fixedly connected to a 24MHz crystal; RTC_XIN is the RTC input clock, and is fixedly connected to a 32.768KHz crystal.

3.2.3 Clock resource distribution

The clock management module configures, controls and manages the input clock from the chip pins and the internal PLL, and generates the clock resources required by each module. The specific distribution is shown in Figure 3-3 .

Figure 3-3 Block diagram of clock resource distribution



Note: The gray APLL and DPLL in the figure are user-programmable configurations; other PLLs are fixed configurations. When there are multiple clock sources to choose from for some modules, default means the default branch. CBB is other media business modules except CPU, DDR, BUS and peripherals.

3.2.4 PLL configuration

Hi3519V100 uses 4 PLLs internally, and each PLL uses two sets of configuration registers, the corresponding relationship is shown in Table 3-2 .

Table 3-2 Configuration registers corresponding to Hi3519V100 PLL

PLL	Configuration Register 0	Configuration Register 1
APLL	PERI_CRG_PLL0	PERI_CRG_PLL1
DPLL	PERI_CRG_PLL4	PERI_CRG_PLL5
VPLL	PERI_CRG_PLL6	PERI_CRG_PLL7
EPLL	PERI_CRG_PLL8	PERI_CRG_PLL9

All PLLs use the crystal oscillator clock input from pin XIN as the input clock, and the PLL output frequency configuration method is shown in Table 3-3 .

Table 3-3 Hi3519V100 PLL frequency calculation method

PLL Pin	Calculation method description	Precautions
FREF	PLL input reference clock	Hi3519V100 requires fixed input 24MHz
FOUTVCO	FREF x (fbdiv + frac/2^24) / refdiv	PLL operating frequency, required to be greater than or equal to 800MHz, and less than or equal to 2.3GHz
FOUTVCO2X FOUTVCO * 2		.
FOUTPOSTDIV FOUTVCO / (pstdiv1 x pstdiv2)		.
ERROR1PH0	FOUTVCO / (pstdiv1 x pstdiv2 x 2)	.
foot2	FOUTVCO / (pstdiv1 x pstdiv2 x 4)	.
foot3	FOUTVCO / (pstdiv1 x pstdiv2 x 6)	.
FOUT4	FOUTVCO / (pstdiv1 x pstdiv2 x 8)	.
Remarks: fbdiv: integer multiplication coefficient; frac: fractional multiplication coefficient; refdiv: reference clock frequency division coefficient; pstdiv1: first stage output frequency division coefficient; pstdiv2: second stage output frequency division coefficient. For the configuration coefficients of each PLL, please refer to the corresponding bit of the corresponding configuration register in Table 3-1 .		

Take configuring APLL as an example, APLL outputs FOUTVCO to A17 CPU module, the frequency is 1200MHz, calculate the value of the configuration register as follows:

Take postdiv2=2, postdiv1=1, according to FOUTVCO= FREF / (pstdiv1 x pstdiv2) =1200MHz.

Take refdiv=1, then 24 x (fbdiv + frac/2^24)/1=1200MHz.

It is deduced from the above conditions: fbdiv=50, frac=000000.

3.2.5 Frequency configuration

3.2.5.1 CPU/DDR_BUS frequency configuration

The CPU/DDR/BUS frequency clock configuration method is shown in Table 3-4 .

Table 3-4 CPU/DDR/BUS frequency configuration

Signal name	configuration register
cpu_a7_cksel	PERI_CRG13 bit[9:7]ÿ
a7clk_loaden	PERI_CRG11 bit[17]ÿ
a7clk_skipcfg	PERI_CRG11 bit[16:12]ÿ
ddr_sc_sel	PERI_CRG13 bit[2:0]ÿ
bus_sc_sel	PERI_CRG13 bit[13:12]ÿ

3.2.5.2 Module clock frequency configuration

Table 3-5 shows the clock frequency configuration of each module .

Table 3-5 Clock frequency configuration of each module

Signal name	configuration register
VDP clock configuration	
vo_out_cksel	PERI_CRG17 bit[16:14]ÿ
hd_div_mode	PERI_CRG17 bit[13:12]ÿ
vdac_pctrl	PERI_CRG17 bit[3]ÿ
vo_out_pctrl	PERI_CRG17 bit[2]ÿ
lcd_mclk_div	PERI_CRG18 bit[26:0]
VI_MIPI Clock Configuration	
sensor_cksel	PERI_CRG16 bit[3:0]ÿ

Signal name	configuration register
vimipi0_cksel	PERI_CRG19 bit[2:0]ÿ
vi_pctrl	PERI_CRG15 bit[9]ÿ
vi_isp_ckdiv	PERI_CRG15 bit[11:10]
VEDU clock configuration	
vedu_cksel	PERI_CRG19 bit[12:10]
veduclk_loaden	PERI_CRG20 bit[9]ÿ
veduclk_skipcfg	PERI_CRG20 bit[8:4]ÿ
VPSS clock configuration	
vpss0_cksel	PERI_CRG19 bit[7:5]ÿ
vpssclk_loaden	PERI_CRG22 bit[9]ÿ
vpssclk_skipcfg	PERI_CRG22 bit[8:4]ÿ
TDE clock configuration	
tdeclk_loaden	PERI_CRG25 bit[9]ÿ
tdeclk_skipcfg	PERI_CRG25 bit[8:4]ÿ
VGS clock configuration	
vgs_cksel	PERI_CRG19 bit[15:13]ÿ
vgsclk_loaden	PERI_CRG23 bit[9]ÿ
vgsclk_skipcfg	PERI_CRG23 bit[8:4]ÿ
JPGE clock configuration	
jpgeclk_load	PERI_CRG24 bit[9]ÿ
jpgeclk_skipcfg	PERI_CRG24 bit[8:4]ÿ
IVE clock configuration	
ive_cksel	PERI_CRG19 bit[21:19]ÿ
GDC clock configuration	
gdc_cksel	PERI_CRG19 bit[18:16]ÿ
gdcclk_loaden	PERI_CRG29 bit[9]ÿ
gdcclk_skipcfg	PERI_CRG29 bit[8:4]ÿ
FMC clock configuration	
fmc_cksel	PERI_CRG48 bit[4:2]ÿ

Signal name	configuration register
SDIO clock configuration	
emmc_clk_mode	PERI_CRG49 bit[21]ÿ
emmc_cksel	PERI_CRG49 bit[20:18]ÿ
sdxc0_clk_mode	PERI_CRG49 bit[13]ÿ
sdxc0_cksel	PERI_CRG49 bit[12:10]ÿ
sdxc1_clk_mode	PERI_CRG49 bit[5]ÿ
CIPHER clock configuration	
ca_cksel	PERI_CRG31 bit[6]ÿ
PWM/I2C/UART Clock Configuration	
pwm_cksel	PERI_CRG55 bit[3:2]ÿ
i2c_cksel	PERI_CRG57 bit[26]ÿ
uart_cksel	PERI_CRG57 bit[25]ÿ
GSF/GMAC clock configuration	
mac_speed	PERI_CRG59 bit[1]ÿ
port_select	PERI_CRG59 bit[0]ÿ
ext_fephy_cksel	PERI_CRG51 bit[6]ÿ
rmii_cksel	PERI_CRG51 bit[4]ÿ
AIAO clock frequency configuration	
ai0_cksel	PERI_CRG32 bit[3:2]ÿ
COMB PHY Clock Frequency Configuration	
combphy_refclk_sel	PERI_CRG43 bit[9]ÿ
usb3_utmi_cksel	PERI_CRG46 bit[13]ÿ

3.2.5.3 Precautions

The clock configuration needs to pay attention to the following items:

When the PLL changes the frequency configuration, it needs to wait for 0.1ms to output a stable clock. Please switch the target clock to non-PLL clock mode before changing the PLL frequency configuration.

You can judge whether the PLL is stable or not by observing the PLL LOCK indicator bit. The PLL LOCK indicator bit can be obtained by reading the status of PERI_CRG58 bit[3:0].

3.2.6 CRG register overview

An overview of the CRG register is shown in Table 3-6 .

Table 3-6 CRG register overview (base address is 0x1201_0000)

offset address name		describe	page number
0x0000	PERI_CRG_PLL0	APLL Configuration Register 0	3-11
0x0004	PERI_CRG_PLL1	APLL Configuration Register 1	3-12
0x0010	PERI_CRG_PLL4	DPLL Configuration Register 0	3-13
0x0014	PERI_CRG_PLL5	DPLL Configuration Register 1	3-14
0x0018	PERI_CRG_PLL6	VPLL Configuration Register 0	3-15
0x001C	PERI_CRG_PLL7	VPLL Configuration Register 1	3-16
0x0020	PERI_CRG_PLL8	EPLL Configuration Register 0	3-17
0x0024	PERI_CRG_PLL9	EPLL Configuration Register 1	3-18
0x0028	PERI_CRG10	CORESIGHT & A17 Clock Reset Configuration Register	3-19
0x002C	PERI_CRG11	A7 Clock Reset Configuration Register	3-20
0x0030	PERI_CRG12	DDR Clock Configuration Register	3-22
0x0034	PERI_CRG13	SOC Frequency Profile Configuration Register	3-23
0x003C	PERI_CRG15	VI-MIPI Clock Reset Configuration Register	3-24
0x0040	PERI_CRG16	Sensor Clock Configuration Register	3-25
0x0044	PERI_CRG17	VOU Clock and Reset Control Register	3-27
0x0048	PERI_CRG18	LCD Clock Configuration Register	3-28
0x004C	PERI_CRG19	Media CBB Frequency Profile Configuration Register 3-29	
0x0050	PERI_CRG20	VEDU clock and soft reset control register	3-31
0x0058	PERI_CRG22	VPSS Clock and Soft Reset Control Register	3-31
0x005C	PERI_CRG23	VGS Clock and Soft Reset Control Register	3-32
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-33
0x0064	PERI_CRG25	TDE Clock and Soft Reset Control Register	3-33
0x006C	PERI_CRG27	IVE Clock and Soft Reset Control Register	3-34
0x0074	PERI_CRG29	GDC clock and soft reset control register	3-35

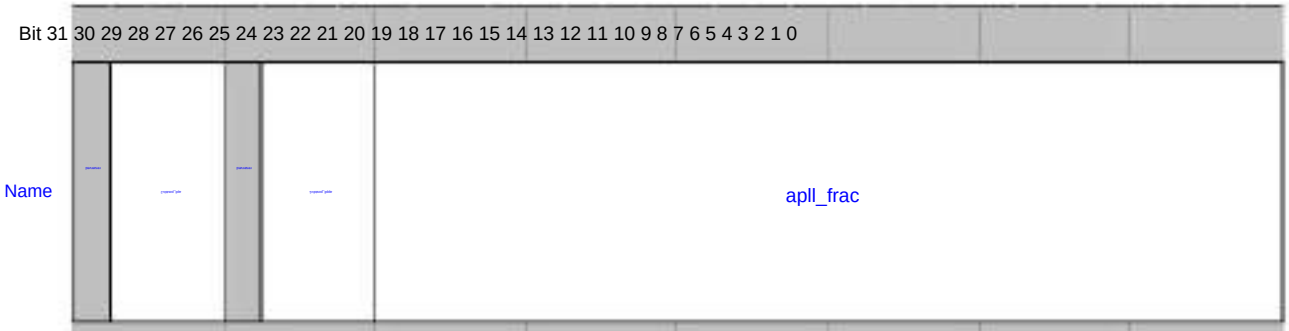
offset address name		describe	page number
0x007C	PERI_CRG31	HASH/LSADC/CIPHER related clock and soft reset control register	3-35
0x0080	PERI_CRG32	AIAO Clock Reset Control Register	3-37
0x0084	PERI_CRG33	GZIP related clock and soft reset control register 3-37	
0x00AC PERI_CRG43		COMB PHY Related Clock Reset Control Register 3-38	
0x00B0 PERI_CRG44		PCIE CTRL related clock and soft reset control register	3-39
0x00B4	PERI_CRG45	USB2 related clock and soft reset control register 3-40	
0x00B8 PERI_CRG46		USB3 CTRL Clock and Soft Reset Control Register 3-42	
0x00C0	PERI_CRG48	FMC related clock and soft reset control register 3-43	
0x00C4 PERI_CRG49		SDIO0/1/eMMC related clock and soft reset control register	3-44
0x00CC PERI_CRG51		Clock and soft reset control registers related to GSF and GMAC interfaces	3-46
0x00D8 PERI_CRG54		DDRT related clock and soft reset control register 3-47	
0x00DC PERI_CRG55		PWM Clock and Reset Control Register	3-48
0x00E0	PERI_CRG56	RSA/TRNG/DMA and other related clock and soft reset control registers	3-49
0x00E4	PERI_CRG57	Other APB module clock soft reset control register 3-50	
0x00E8	PERI_CRG58	CRG status register	3-53
0x00EC PERI_CRG59		GMAC Interface Control Register	3-54
0x00F0	PERI_CRG60	GMAC Interface Status Register	3-56
0x013C PERI_CRG79		SOC Frequency Profile Status Register	3-56

3.2.7 CRG register description

PERI_CRG_PLL0

PERI_CRG_PLL0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG_PLL0	0x1200_0000

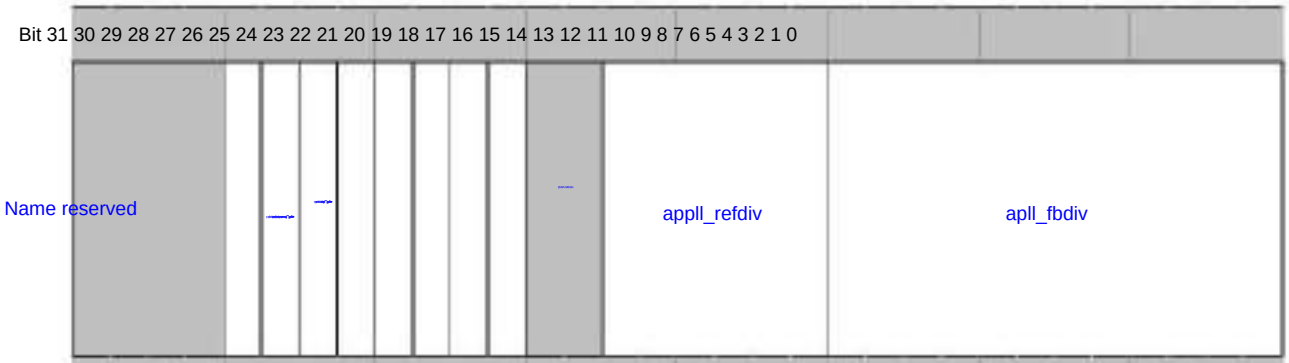


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	apll_postdiv2	The second stage of APLL outputs the frequency division factor.
[27]	RO	reserved	reserve.
[26:24]	RW	apll_postdiv1	APLL first-stage output frequency division coefficient.
[23:0]	RW	apll_frac	APLL Fractional division factor.

PERI_CRG_PLL1

PERI_CRG_PLL1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG_PLL1	0x0910_1032



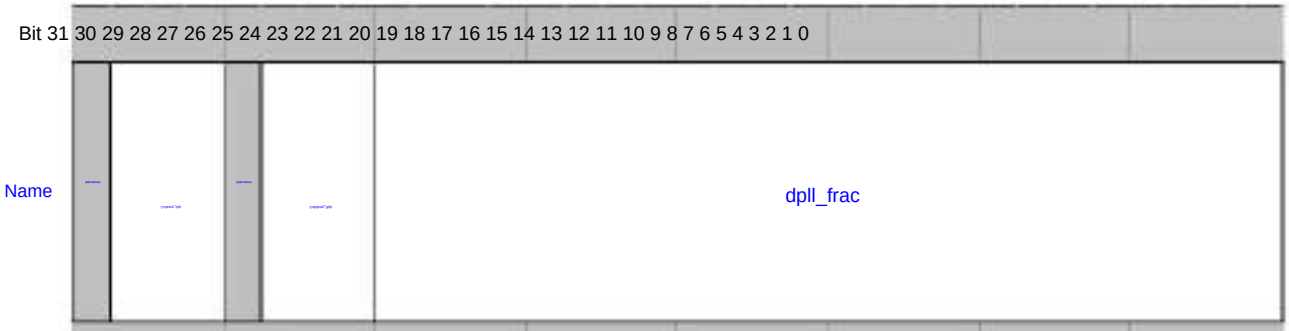
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27] RW	apll_foutvco2xpd		APLL VCO2X output Power Down control. 1: no clock output; 0: Normal output clock.
[26] RW	apll_bypass		APLL clock frequency division bypass (bypass) control. 0: no bypass; 1: Bypass.
[25] RW	apll_dacpd		APLL test signal control. 0: normal working state; 1: power down working state.
[24] RW	apll_dsmpd		APLL Fractional divider control. 0: decimal mode; 1: Integer mode.
[23] RW	apll_pd		APLL Power Down control. 0: normal working state; 1: power down working state.
[22] RW	apll_foutvcopd		APLL VCO output Power Down control. 0: Normal output clock; 1: Do not output clock.
[21] RW	apll_postdivpd		APLL POSTDIV Output Power Down control. 0: Normal output clock; 1: Do not output clock.
[20] RW	apll_fout4phasepd		APLL FOUT output Power Down control. 0: Normal output clock; 1: Do not output clock.
[19:18] RO		reserved	reserve.
[17:12] RW	apll_refdiv		APLL reference clock division factor.
[11:0] RW	apll_fbdiv		APLL integer multiplication factor.

PERI_CRG_PLL4

PERI_CRG_PLL4 Configuration Register 0 for DPLL.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG_PLL4	0x1200_0000

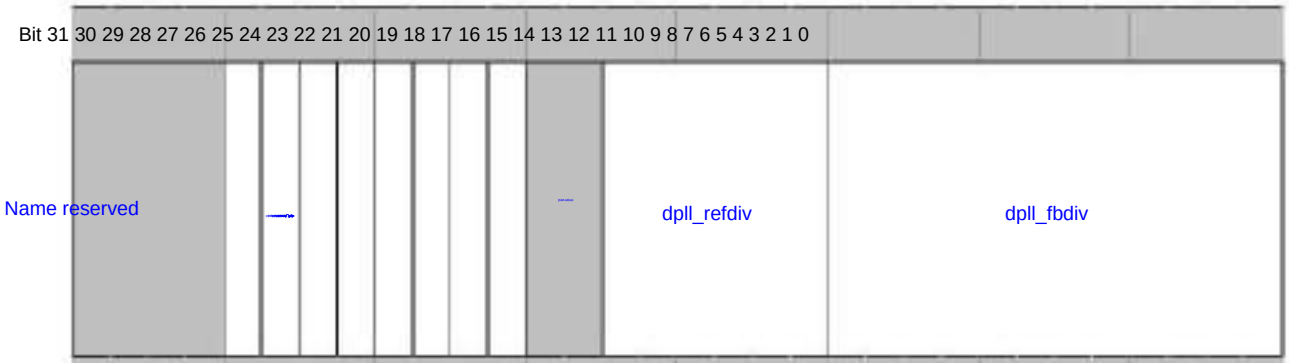


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	dpll_postdiv2	The second stage of DPLL outputs the frequency division factor.
[27]	RO	reserved	reserve.
[26:24]	RW	dpll_postdiv1	The first stage of DPLL outputs the frequency division factor.
[23:0]	RW	dpll_frac	DPLL fractional division factor.

PERI_CRG_PLL5

PERI_CRG_PLL5 Configuration Register 1 for DPLL.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG_PLL5	0x0910_60E9



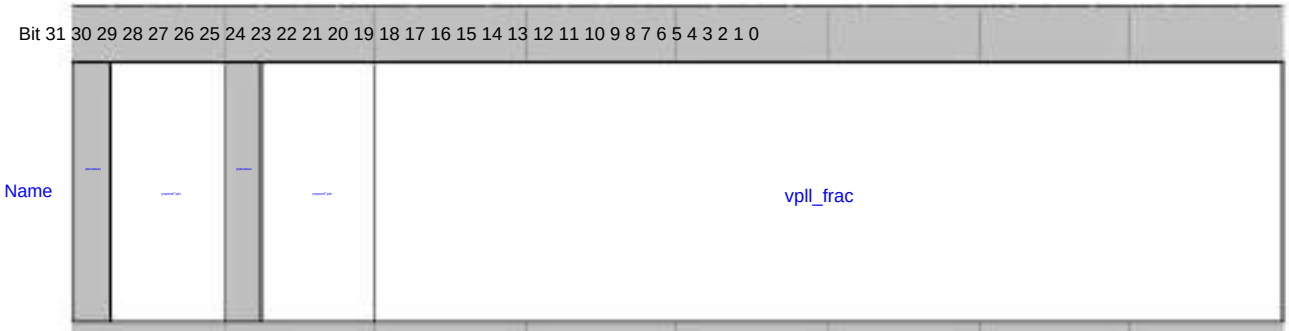
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27] RW	dpll_foutvco2xpd		DPLL VCO2X output Power Down control. 1: no clock output; 0: Normal output clock.
[26] RW	dpll_bypass		DPLL clock divider bypass (bypass) control. 0: no bypass; 1: Bypass.
[25] RW	dpll_dacpd		DPLL test signal control. 0: normal working state; 1: power down working state.
[24] RW	dpll_dsmpd		DPLL fractional divider control. 0: decimal mode; 1: Integer mode.
[23] RW	dpll_pd		DPLL Power Down Control. 0: normal working state; 1: power down working state.
[22] RW	dpll_foutvcopd		DPLL VCO output Power Down control. 0: Normal output clock; 1: Do not output clock.
[21] RW	dpll_postdivpd		DPLL POSTDIV Output Power Down control. 0: Normal output clock; 1: Do not output clock.
[20] RW	dpll_fout4phasepd		DPLL FOUT output Power Down control. 0: Normal output clock; 1: Do not output clock.
[19:18] RO		reserved	reserve.
[17:12] RW	dpll_refdiv		DPLL reference clock division factor.
[11:0] RW	dpll_fbdiv		DPLL integer multiplication factor.

PERI_CRG_PLL6

PERI_CRG_PLL6 Configuration register 0 for VPLL.

Offset Address	Register Name	Total Reset Value
0x0018	PERI_CRG_PLL6	0x1200_0000

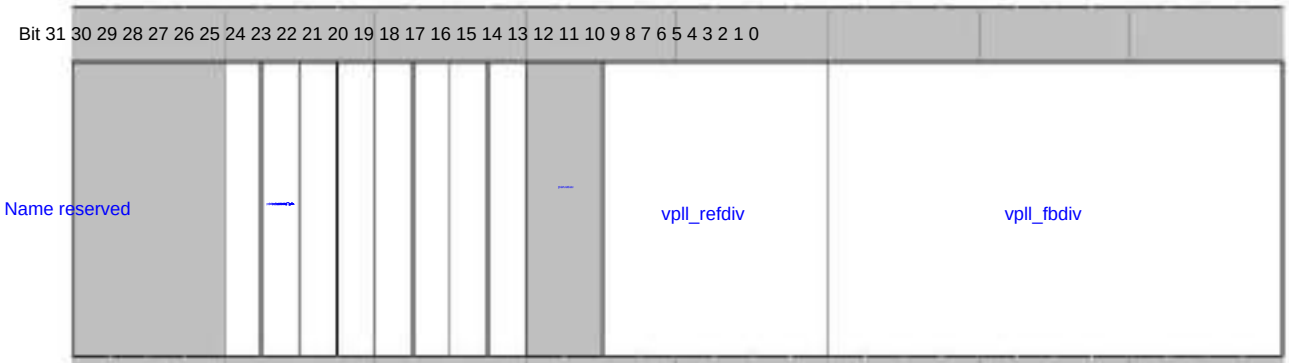


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	vpll_postdiv2	The second stage of VPLL outputs the frequency division factor.
[27]	RO	reserved	reserve.
[26:24]	RW	vpll_postdiv1	VPLL first-stage output frequency division coefficient.
[23:0]	RW	vpll_frac	VPLL fractional division factor.

PERI_CRG_PLL7

PERI_CRG_PLL7 Configuration register 1 for VPLL.

Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG_PLL7	0x0100_2063



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

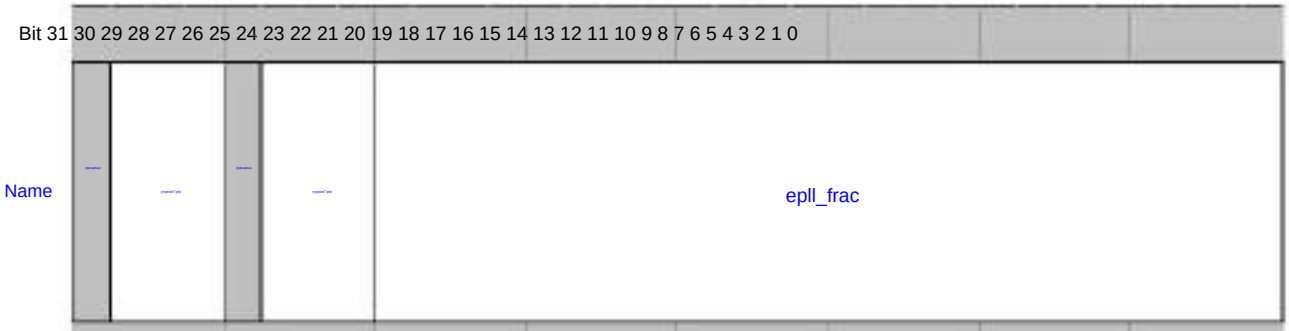
Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG_PLL7	0x0100_2063

[27] RW vpll_foutvco2xpd		VPLL VCO2X output Power Down control. 0: Normal output clock; 1: Do not output clock.
[26] RW vpll_bypass		VPLL clock frequency division bypass (bypass) control. 0: no bypass; 1: Bypass.
[25] RW vpll_dacpd		VPLL test signal control. 0: normal working state; 1: power down working state.
[24] RW vpll_dsmpd		VPLL fractional divider control. 0: decimal mode; 1: Integer mode.
[23] RW vpll_pd		VPLL Power Down Control. 0: normal working state; 1: power down working state.
[22] RW vpll_foutvcopd		VPLL VCO output Power Down control. 0: Normal output clock; 1: Do not output clock.
[21] RW vpll_postdivpd		VPLL POSTDIV Output Power Down control. 0: Normal output clock; 1: Do not output clock.
[20] RW vpll_fout4phasepd		VPLL FOUT output Power Down control. 0: Normal output clock; 1: Do not output clock.
[19:18] RO	reserved	reserve.
[17:12] RW vpll_refdiv		VPLL reference clock division factor.
[11:0] RW vpll_fbdiv		VPLL integer multiplication factor.

PERI_CRG_PLL8

PERI_CRG_PLL8 Configuration register 0 for EPLL.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG_PLL8	0x1300_0000

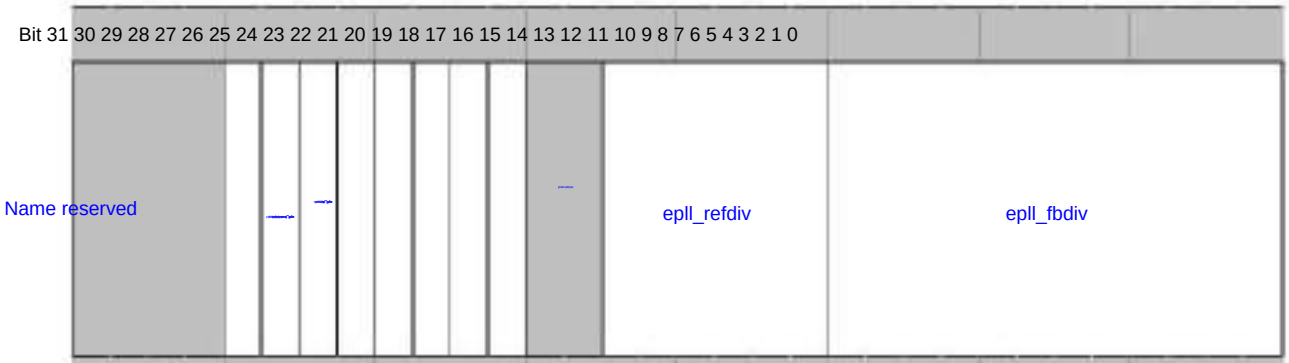


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	epll_postdiv2	The second stage of EPLL outputs the frequency division factor.
[27]	RO	reserved	reserve.
[26:24]	RW	epll_postdiv1	The first stage of EPLL outputs the frequency division factor.
[23:0]	RW	epll_frac	EPLL Fractional division factor.

PERI_CRG_PLL9

PERI_CRG_PLL9 Configuration register 1 for EPLL.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG_PLL9	0x0100_207D



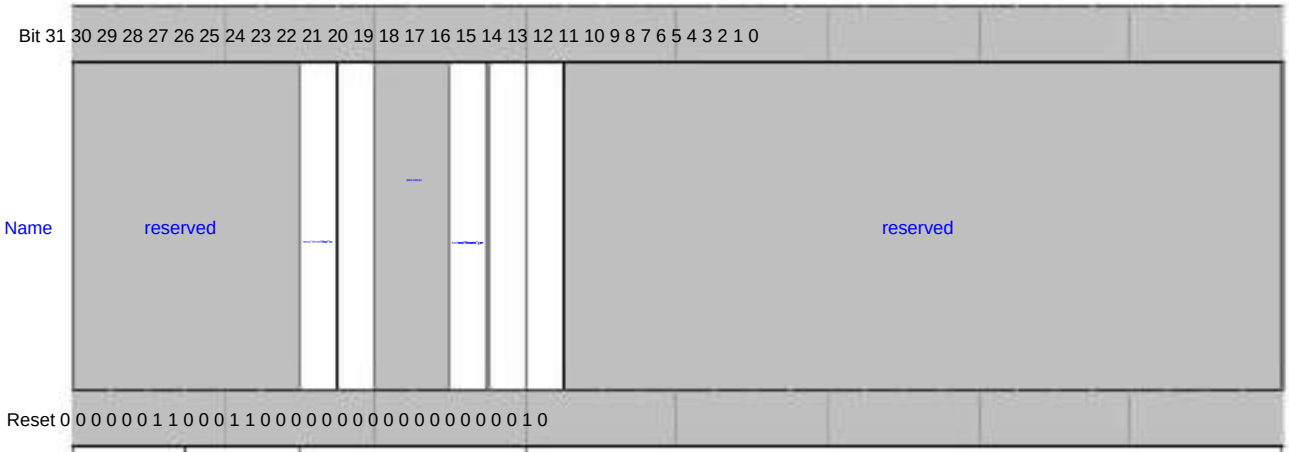
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27] RW	epll_foutvco2xpd		EPLL VCO2X output Power Down control. 0: Normal output clock; 1: Do not output clock.
[26] RW	epll_bypass		EPLL clock divider bypass (bypass) control. 0: no bypass; 1: Bypass.
[25] RW	epll_dacpd		EPLL test signal control. 1: power down working state; 0: normal working state.
[24] RW	epll_dsmpd		EPLL Fractional divider control. 0: decimal mode; 1: Integer mode.
[23] RW	epll_pd		EPLL Power Down control. 1: power down working state; 0: normal working state.
[22] RW	epll_foutvcopd		EPLLVCO output Power Down control. 0: Normal output clock; 1: Do not output clock.
[21] RW	epll_postdivpd		EPLL POSTDIV Output Power Down control. 0: Normal output clock; 1: Do not output clock.
[20] RW	epll_fout4phasepd		EPLLFOUT Output Power Down control. 0: Normal output clock; 1: Do not output clock.
[19:18] RO		reserved	reserve.
[17:12] RW	epll_refdiv		EPLL reference clock division factor.
[11:0] RW	epll_fbdiv		EPLL integer multiplication factor.

PERI_CRG10

PERI_CRG10 is the configuration register for CORESIGHT & A17 clock reset.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0318_0002

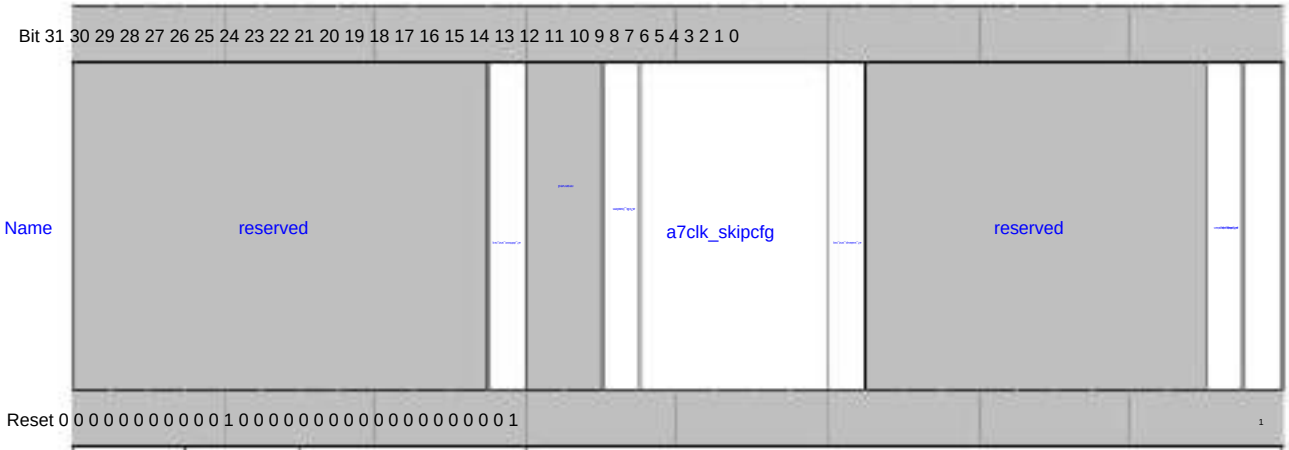


Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RW	cs_cken	CORESIGHT TOP Clock gating configuration register (valid only in manual mode). 0: turn off the clock; 1: Turn on the clock.
[24]	RW	cs_dbg_pwrup_mo	CORESIGHT TOP PwrUp mode. 0: auto mode; de 1: Manual mode.
[23:22]	RO	reserved	reserve
[21]	RW	a17_wakeup_cken	A17 Subsystem Global Clock Gating Register. 0: turn off the clock; 1: Turn on the clock.
[20]	RW	a17_topdbg_cken	PCLKDBG Clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[19]	RW	a17_wakeup_srst_r	A17 Subsystem global soft reset. 0: undo reset; eq 1: Reset.
[18:0]	RO	reserved	reserve.

PERI_CRG11

PERI_CRG11 is A7 clock reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0010_0003

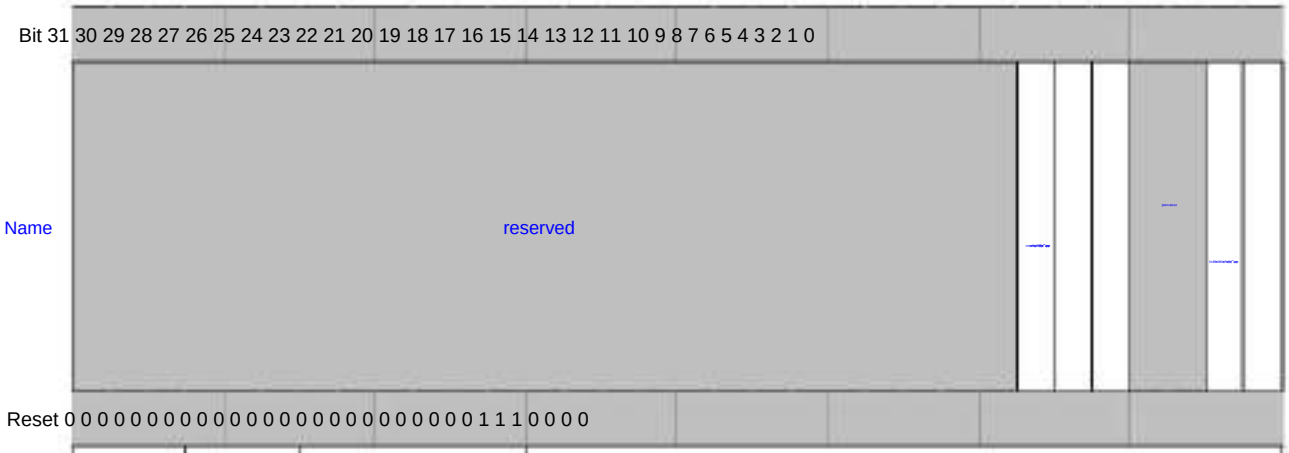


Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20]	RW	a7_ddrboot_srst_re q	A7 Global soft reset, only valid in PCIe slave boot mode. 0: deactivate reset; 1: Reset.
[19:18]	RO	reserved	reserve.
[17]	RW	a7clk_loaden	CPU clock Skip configuration is enabled. Every time you change the skip configuration, divide the following three steps: 1. Write the new skip configuration value 2. Then write loaden as 0 3. Then write loaden as 1
[16:12]	RW	a7clk_skipcfg	CPU clock Skip configuration. N: Turn off the N beat clock in every 32 beats of the CPU clock.
[11]	RW	a7_wakeup_srst_re q	A7 Global soft reset, only valid in non-PCIe slave boot mode. 0: undo reset; 1: Reset.
[10:2]	RO	reserved	reserve.
[1]	RW	a7_wakeup_cken	A7 Global clock gating. 0: clock off; 1: Clock is on.
[0]	RW	pclkdbg_cken	A7 PCLKDBG Clock Gating. 0: clock off; 1: Clock is on.

PERI_CRG12

PERI_CRG12 is the DDR clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0070

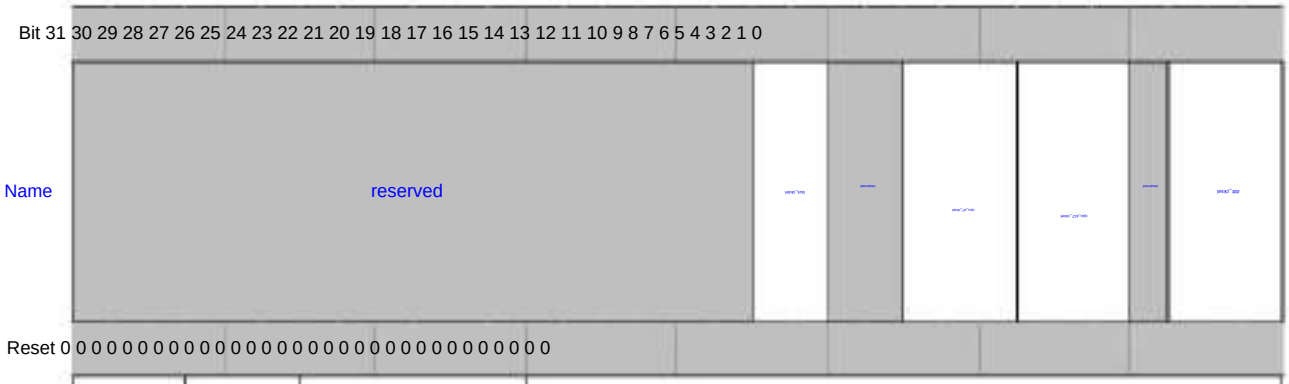


Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	ddr_apb_cken	DDR APB Gate Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[5]	RW	ddr_hipack_cken	DDR HiPACK gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[4]	RW	ddr_cfg_cken	DDR CFG Gate Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[3:2]	RO	reserved	reserve.
[1]	RW	ddr_apb_srst_req	DDR APB soft reset request. 0: cancel reset; 1: Reset.
[0]	RW	ddr_hipack_srst_re q	DDR HiPACK soft reset request. 0: undo reset; 1: Reset.

PERI_CRG13

PERI_CRG13 is the SOC frequency profile configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0000



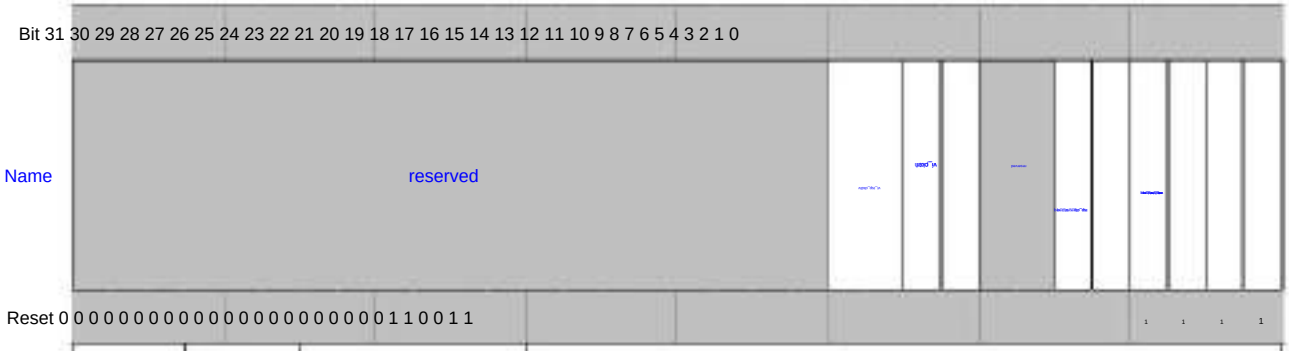
Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:12]	RW	bus_cksel	BUS clock profile configuration. x0: XTAL clock; x1: 200MHz clock.
[11:10]	RO	reserved	reserve.
[9:7]	RW	cpu_a7_cksel	A7 CPU Profile configuration. 000: XTAL clock; 001ÿDPLL VCOÿ 010ÿAPLL POSTDIV 011ÿ792MHzÿ 100ÿ750MHzÿ 101ÿ594MHzÿ Others: reserved.
[6:4]	RW	cpu_a17_cksel	A17 CPU clock profile configuration: 000: XTAL clock; 001ÿAPLL VCOÿ 010ÿDPLL VCOÿ 011ÿ1000MHzÿ 100ÿ792MHzÿ 101ÿ594MHzÿ 110ÿ500MHzÿ 111ÿ400MHzÿ

[3]	RO	reserved	reserve.
[2:0] RW	ddr_cksel		DDR clock profile configuration. 000: XTAL clock; 001ÿDPLL POSTDIVÿ 011ÿ396MHzÿ 100ÿ346MHzÿ 101ÿ300MHzÿ 110ÿ250MHzÿ Others: reserved.

PERI_CRG15

PERI_CRG15 is VI-MIPI clock reset configuration register.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_CRG15	0x0000_033F



Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:10]	RW	vi_isp_ckdiv	ISP CLK frequency division factor configuration. 00: divide by 2; 01: divide by 4; 1X: no frequency division. Note: ISP CLK supports up to 300MHz, and its clock source comes from PERI_CRG19[2:0]. Please choose a reasonable frequency division configuration according to the clock source.
[9]	RW	vi_pctrl	VI interface clock phase control. 0: clock forward; 1: Reverse clock.

[8] RW vi_cken			VI clock gating. 0: clock off; 1: Clock is on.
[7:6] RO		reserved	reserve
[5] RW isp_cfg_srst_req			ISP CFG soft reset request. 0: cancel reset; 1: Reset.
[4] RW isp_core_srst_req			ISP Core soft reset request. 0: cancel reset; 1: reset.
[3] RW mipi_hrst_req			MIPI Ctrl bus soft reset request. 0: cancel reset; 1: Reset.
[2] RW mipi_srst_req			MIPI Ctrl CH0 Partial soft reset request. 0: cancel reset; 1: Reset.
[1] RW vi_hrst_req			VI bus soft reset request. 0: cancel reset; 1: reset.
[0] RW vi_srst_req			VI Soft reset request. 0: cancel reset; 1: Reset.

PERI_CRG16

PERI_CRG16 is the Sensor clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Name	reserved	---	sensor0_cksel
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	sensor0_ctrl_srst_req	Sensor0 slave mode control module soft reset 0: undo reset; 1: Reset.
[5]	RW	sensor0_srst_req	Sensor0 soft reset request. 0: cancel reset; 1: Reset.
[4]	RW	sensor0_cken	Sensor0 CLKOUT clock gating. 0: clock off; 1: Clock is on.
[3:0]	RW	sensor0_cksel	Sensor0 CLKOUT clock configuration register. 0000ÿ74.25MHzÿ 0001ÿ72MHzÿ 0010ÿ54MHzÿ 0011ÿ50MHzÿ 01xxÿ24MHzÿ 1000ÿ37.125MHzÿ 1001ÿ36MHzÿ 1010ÿ27MHzÿ 1011ÿ25MHzÿ 11xxÿ12MHzÿ

PERI_CRG17

PERI_CRG17 is the VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0044	PERI_CRG17	0x0000_0005

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1

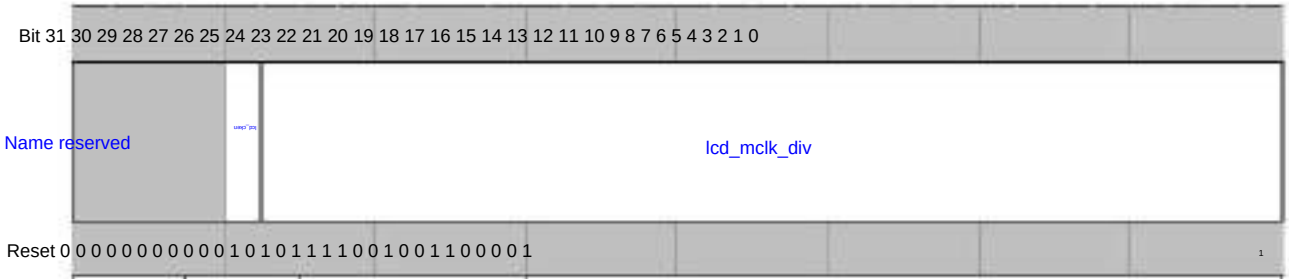
Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:14]	RW	vo_out_cksel	VO_OUT_CLK frequency selection. 000ÿ148.5MHzÿ 001ÿ74.25MHzÿ 010ÿ37.125MHzÿ 011ÿ107MHz ÿ 100ÿ54M Hzÿ 101ÿ27M Hzÿ 110: LCD frequency divider clock; 111: Reserved.
[13:12]	RW	hd_div_mode	VO_OUT_CLK and DHD channel clock division ratio configuration. 00: no frequency division; 01: divide by 2; 10: 3 frequency division; 11: 4 frequency division.
[11]	RW	vdac_cken	VDACH Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[10]	RW	vou_sd_cken	VOU SD Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.

[9] RW vou_hd_cken			VOU HD Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[8] RW vo_out_cken			VO_CLKOUT Clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[7] RW vou_acken			VOU AXI bus clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[6] RW vou_pcken			VOU APB Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[5] RW vou_ppc_cken			VOU PPC Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[4] RW vou_cfg_cken			VOU CFG (Internal Configuration) Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[3] RW vdac_pctrl			VDAC clock phase control. 0: clock forward; 1: Reverse clock.
[2] RW vo_out_pctrl			VOU HD output is controlled with channel clock phase. Default reverse 0: forward clock; 1: Reverse clock.
[1]	RO	reserved	reserve.
[0] RW vo_srst_req			VOU Soft reset request. 0: cancel reset; 1: Reset.

PERI_CRG18

PERI_CRG18 is LCD clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0015_E4C3

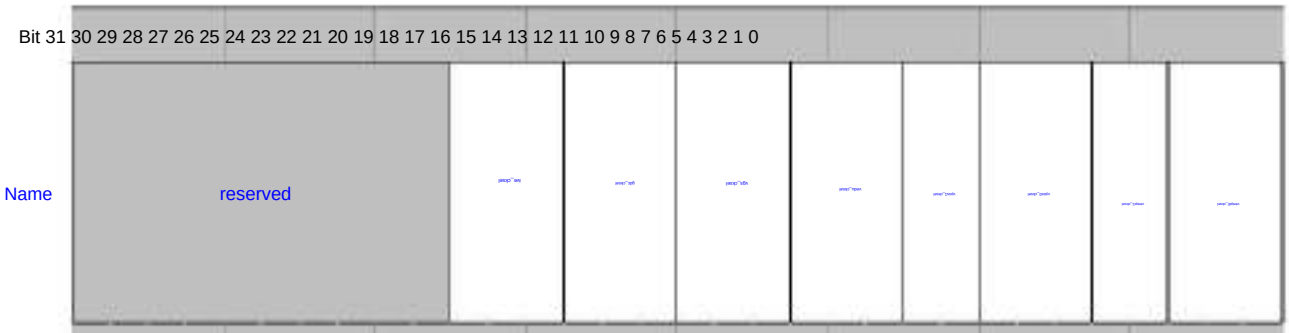


Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	lcd_cken	LCD divider clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[26:0]	RW	lcd_mclk_div	LCD frequency division clock, configurable. Assuming the target frequency is X(MHZ), then lcd_mclk_div = (X/1188) * 2^27.

PERI_CRG19

PERI_CRG19 is the media CBB frequency profile configuration register.

Offset Address	Register Name	Total Reset Value
0x004C	PERI_CRG19	0x0000_0000



Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:19]	RW	ive_cksel	IVE frequency configuration. 000ÿ200MHzÿ 001ÿ300MHzÿ 010ÿ400MHzÿ Others: reserved.

[18:16] RW	gdc_cksel		GDC frequency configuration. 000ÿ200MHzÿ 001ÿ300MHzÿ 010ÿ400MHzÿ 100ÿ340MHzÿ 101ÿ475MHzÿ Others: reserved.
[15:13] RW	vgs_cksel		VGS frequency configuration. 000ÿ150MHzÿ 001ÿ250MHzÿ 010ÿ300MHzÿ 100ÿ400MHzÿ Others: reserved.
[12:10] RW	vedu_cksel		VEDU frequency configuration. 000ÿ200MHzÿ 001ÿ250MHzÿ 010ÿ300MHzÿ 011ÿ500MHzÿ Others: reserved.
[9:8] RO		reserved	reserve.
[7:5] RW	vpss0_cksel		VPSS0 frequency configuration. 000ÿ100MHzÿ 001ÿ150MHzÿ 010ÿ214MHzÿ 011ÿ300MHzÿ Others: reserved.
[4:3] RO		reserved	reserve.

[2:0] RW	vimipi0_cksel		VIMIPI0 frequency configuration. 000ÿ100MHzÿ 001ÿ150MHzÿ 010ÿ214MHzÿ 011ÿ300MHzÿ 100ÿ340MHzÿ 101ÿ398MHzÿ 110ÿ500MHzÿ 111ÿ600MHzÿ Note: This register field is the clock source of PERI_CRG15[11:10].

PERI_CRG20

PERI_CRG20 is the VEDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0050	PERI_CRG20	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	wedu_cken	VEDU Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	vedu_srst_req	Soft reset request for VEDU. 0: cancel reset; 1: Reset.

PERI_CRG22

PERI_CRG22 is the VPSS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	vps0_cken	VPSS0 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	vps0_srst_req	Soft reset request for VPSS0. 0: cancel reset; 1: Reset.

PERI_CRG23

PERI_CRG23 is VGS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_CRG23	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

[1] RW	vgs_cken		VGS Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0] RW	vgs_srst_req		Soft reset request for VGS. 0: cancel reset; 1: Reset.

PERI_CRG24

PERI_CRG24 is JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	jpge_cken	JPGE Clock Gating Configuration Register, 0: turn off the clock; 1: Turn on the clock.
[0]	RW	jpge_srst_req	Soft reset request for JPGE. 0: cancel reset; 1: Reset.

PERI_CRG25

PERI_CRG25 is the TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_CRG25	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RW	tde_cken	TDE Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	tde_srst_req	Soft reset request for TDE. 0: cancel reset; 1: Reset.

PERI_CRG27

PERI_CRG27 is the IVE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RW	ive_cken	IVE Clock Gating Configuration Register. 0: turn off the clock;

			1: Turn on the clock.
[0]	RW	ive_srst_req	IVE soft reset request. 0: cancel reset; 1: Reset.

PERI_CRG29

PERI_CRG29 is the GDC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_CRG29	0x0000_0003

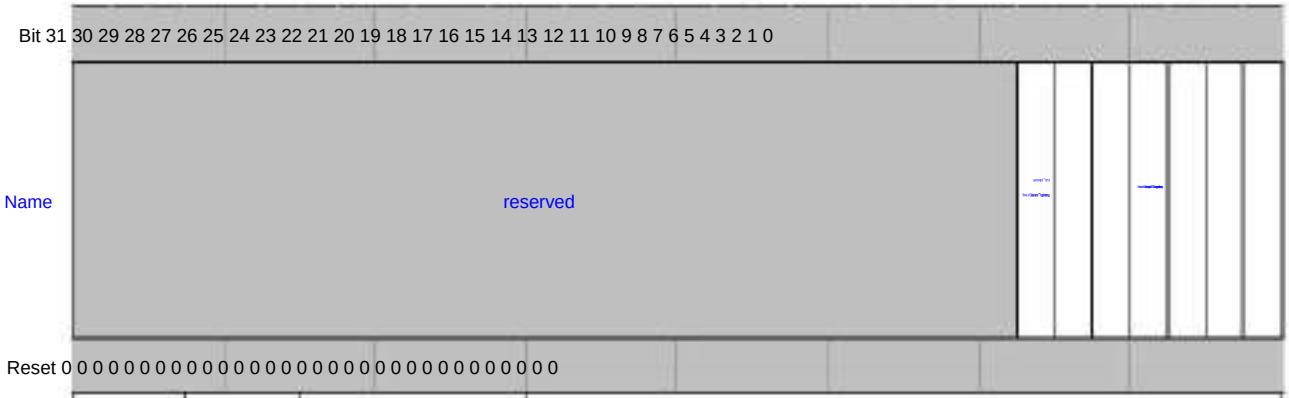
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	gdc_cken	GDC Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	gdc_srst_req	Soft reset request from GDC. 0: cancel reset; 1: reset.

PERI_CRG31

PERI_CRG31 is the clock and soft reset control register related to HASH/LSADC/CIPHER.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000



Bits	Access Name	Description
[31:7] RO	reserved	reserve.
[6] RW ca_cksel		CIPHER clock selection. 0ÿ200MHzÿ 1ÿ250MHzÿ
[5] RW hash_cken		HASH clock gating configuration register, 0: turn off the clock; 1: Turn on the clock.
[4] RW hash_srst_req		Soft reset request for HASH. 0: cancel reset; 1: Reset.
[3] RW lsadc_cken		LSADC Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[2] RW lsadc_srst_req		Soft reset request for LSADC. 0: cancel reset; 1: Reset.
[1] RW cipher_cken		CIPHER Clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0] RW cipher_srst_req		Soft reset request for CIPHER. 0: cancel reset; 1: reset.

PERI_CRG32

PERI_CRG32 is AIAO clock reset control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:2]	RW	science_cksel	AIAO MCLK PLL source selection. 00ÿ1188MHzÿ 01ÿ1500MHzÿ 10ÿDPLL FOUTVCO 11ÿDPLL FOUTPOSTDIVÿ
[1]	RW	science_cken	AIAO bus clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	aiao_srst_req	AIAO bus side soft reset request. 0: cancel reset; 1: reset.

PERI_CRG33

PERI_CRG33 is the clock and soft reset control register related to GZIP.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_CRG33	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	gzip_cken	GZIP clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	gzip_srst_req	Soft reset request for GZIP. 0: cancel reset; 1: Reset.

PERI_CRG43

PERI_CRG43 is the COMB PHY related clock reset control register.

Offset Address	Register Name	Total Reset Value
0x00AC	PERI_CRG43	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.

[9] RW		selection. combphy_refclk_se	COMBPHY Reference clock Internal mode clock source 0: 100MHz; 1ÿ25MHzÿ
[8] RW	combphy_ref_cken		COMBPHY reference clock gating. In PCIE mode: 0: reserved; 1: Turn on the clock. In USB mode: 0: turn off the clock; 1: Turn on the clock.
[7:2] RO		reserved	reserve.
[1] RW		combphy_srst_req_ PCIE controlled by PCIE CTRL;	COMBPHY lower port soft reset mode. In USB3.0 mode: directly controlled by PERI_CRG43[0]. mode: sel 0: 1: Controlled by PERI_CRG43[0].
[0] RW	combphy_srst_req		COMBPHY Port soft reset request. 0: cancel reset; 1: reset.

PERI_CRG44

PERI_CRG44 is the clock and soft reset control register related to PCIE CTRL.

Offset Address	Register Name	Total Reset Value
0x00B0	PERI_CRG44	0x0000_00F0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0

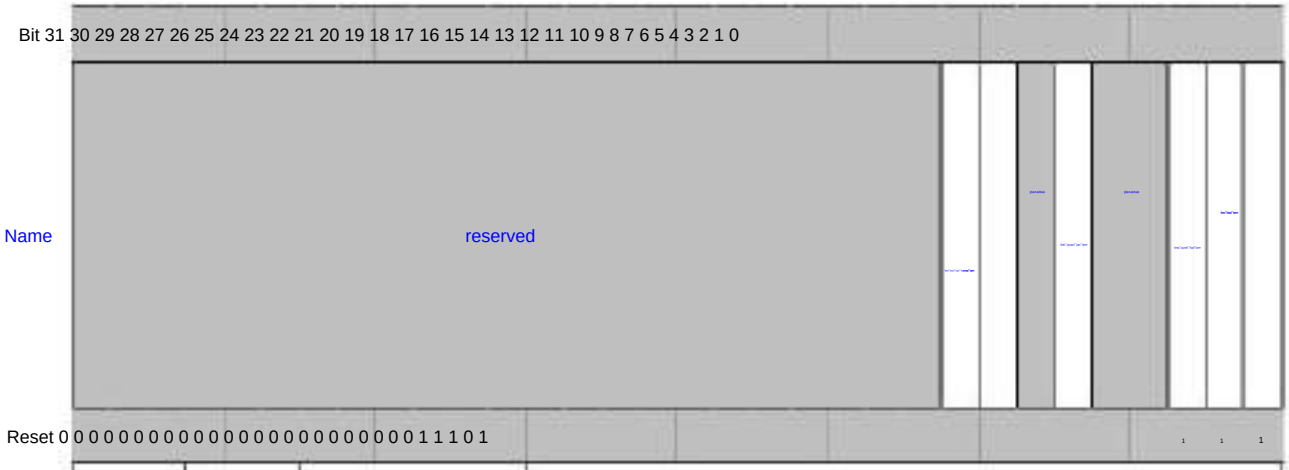
Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.

[10:8] RW	wifi_clk_ctrl		PCIE output differential clock PAD OE control mode 000: Force open; 001: forced shutdown; 101: controlled by PERI_CRG43[8] ; others: reserved.
[7] RW	pcie_aux_cken		PCIE CTRL AUX clock gating. 0: turn off the clock; 1: Turn on the clock.
[6] RW	pcie_pipe_cken		PCIE CTRL PIPE Clock gating. 0: turn off the clock; 1: Turn on the clock.
[5] RW	pcie_sys_cken		PCIE CTRL SYS clock gating. 0: turn off the clock; 1: Turn on the clock.
[4] RW	pcie_bus_cken		PCIECTRL bus clock gating. 0: turn off the clock; 1: Turn on the clock.
[3]	RO	reserved	reserve.
[2] RW	pcie_srst_req		PCIE CTRL Soft reset request. 0: cancel reset; 1: Reset.
[1] RW	pcie_sys_srst_req		PCIECTRL SYS Soft reset request. 0: cancel reset; 1: Reset.
[0] RW	pcie_bus_srst_req		PCIECTRL Bus Soft Reset Request. 0: cancel reset; 1: reset.

PERI_CRG45

PERI_CRG45 is the clock and soft reset control register related to USB2.0.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_CRG45	0x0000_00EF

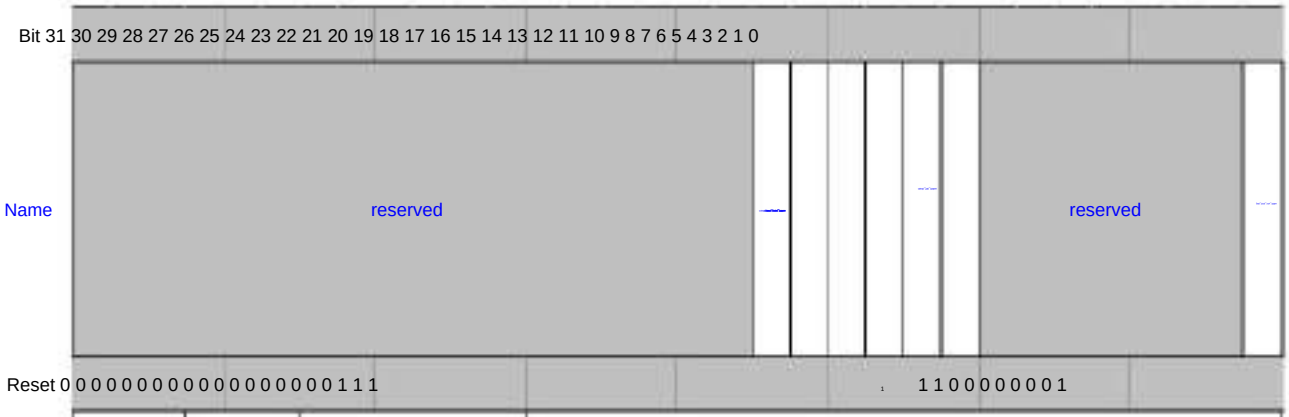


Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	usb_device_ctrl_srs	Soft reset request for USB2.0 device controller. 0: cancel reset; t_req 1: reset.
[7]	RW	usb_cken	USB2.0 PHY Reference Clock Gating 0: off; 1: open.
[6]	RO	reserved	reserve.
[5]	RW	usb_ctrl_utmi0_req	Soft reset request for USB2.0 controller port0. 0: cancel reset; 1: Reset.
[4:3]	RO	reserved	reserve.
[2]	RW	usb_phy_port0_tre	Soft reset request for USB2.0 PHY PORT0. 0: reset reset; q 1: reset.
[1]	RW	usb_phy_req	Soft reset request for USB2.0 PHY. 0: cancel reset; 1: Reset.
[0]	RW	usb_hrst_req	USB2.0 controller bus soft reset request. 0: cancel reset; 1: reset.

PERI_CRG46

PERI_CRG46 is the USB3.0 CTRL clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_3F01



Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13]	RW	usb3_utmi_cksel	USB3.0 UTMI clock source selection. 0: Select USB2.0 PHY clock; 1: Select internal 60MHz clock.
[12]	RW	usb3_utmi_cken	USB3.0 CTRL UTMI clock gating. 0: turn off the clock; 1: Turn on the clock.
[11]	RW	usb3_pipe_cken	USB3.0 CTRL PIPE clock gating. 0: turn off the clock; 1: Turn on the clock.
[10]	RW	usb3_suspend_cken	USB3.0 CTRL SUSPEND Clock gating. 0: turn off the clock; 1: Turn on the clock.
[9]	RW	usb3_ref_cken	USB3.0 CTRL REF clock gating. 0: turn off the clock; 1: Turn on the clock.
[8]	RW	usb3_bus_cken	USB3.0 CTRL bus clock gating. 0: turn off the clock; 1: Turn on the clock.
[7:1]	RO	reserved	reserve.

[0] RW	usb3_vcc_srst_req		USB3.0 CTRL VCC Soft reset request. 0: cancel reset; 1: Reset.

PERI_CRG48

PERI_CRG48 is the clock and soft reset control register related to FMC.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

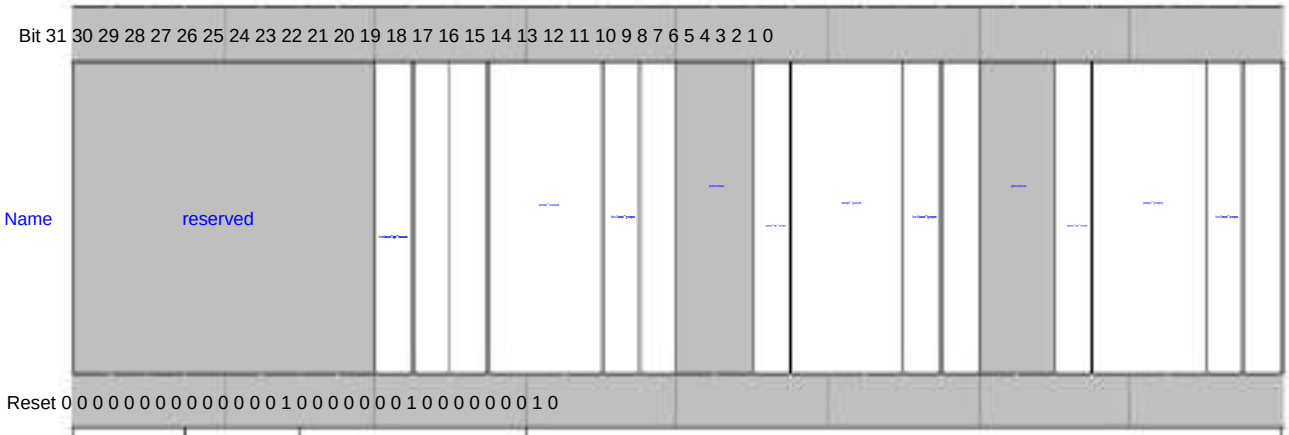
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:2]	RW	fmc_cksel	FMC clock source selection. (In SDR mode, PHY_CLK_OUT is divided by 2 of the original clock; in DDR mode, it is divided by 4 of the original clock) 000: 24MHz clock; 001: 75MHz clock; 010: 125MHz clock; 011: 150MHz clock; 100: 200MHz clock; 101: 250MHz clock (only available in DDR mode); 110: 300MHz clock (only available in DDR mode); 111: 400MHz clock (only available in DDR mode).
[1]	RW	fmc_cken	FMC clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	fmc_srst_req	Soft reset request for FMC. 0: cancel reset; 1: Reset.

PERI_CRG49

PERI_CRG49 is the clock and soft reset control register related to SDIO0/1/eMMC.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0002_0202



Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23]	RW	emmc_dll_srst_req	Soft reset request for eMMC DLL. 0: cancel reset; 1: Reset.
[22]	RW	emmc_dll_cken	eMMC DLL clock gating configuration. 0: off; 1: open.
[21]	RW	emmc_clk_mode	eMMC clock divider mode. 0: reserved; 1: 8 frequency division (corresponding to 16-Phase Tuning).
[20:18]	RW	emmc_cksel	eMMC clock source selection. The actual working clock is obtained after frequency division (controlled by emmc_clk_mode) of this clock. 000ÿ100MHzÿ 001ÿ200MHzÿ 010ÿ300MHzÿ 011ÿ400MHzÿ 100ÿ594MHzÿ 101ÿ792MHzÿ 110: reserved; 111: reserved.

[17] RW	emmc_cken		eMMC clock gating configuration. 0: off; 1: open.
[16] RW	emmc_srst_req		Soft reset request for eMMC. 0: cancel reset; 1: Reset.
[15:14] RO		reserved	reserve.
[13] RW	sdxc0_clk_mode		SDIO0 clock divider mode. 0: reserved; 1: divided by 8 (corresponding to 16-Phase Tuning).
[12:10] RW	sdxc0_cksel		SDIO0 clock source selection. 000ÿ100MHzÿ 001ÿ200MHzÿ 010ÿ300MHzÿ 011ÿ400MHzÿ 100ÿ594MHzÿ 101ÿ792MHzÿ 110: reserved; 111: reserved.
[9] RW	sdxc0_cken		SDIO0 clock gating configuration. 0: off; 1: open.
[8] RW	sdxc0_srst_req		Soft reset request for SDIO0. 0: cancel reset; 1: Reset.
[7:6] RO		reserved	reserve.
[5] RW	sdxc1_clk_mode		SDIO1 clock divider mode. 0: reserved; 1: 8 frequency division (corresponding to 16-Phase Tuning).

[4:2] RW	sdxc1_cksel		SDIO1 clock source selection. 000ÿ100MHzÿ 001ÿ200MHzÿ 010ÿ300MHzÿ 011ÿ400MHzÿ 100ÿ594MHzÿ 101ÿ792MHzÿ 110: reserved; 111: reserved.
[1] RW	sdxc1_cken		SDIO1 clock gating configuration. 0: off; 1: open.
[0] RW	sdxc1_srst_req		Soft reset request for SDIO1. 0: cancel reset; 1: Reset.

PERI_CRG51

PERI_CRG51 is the clock and soft reset control register related to GSF and GMAC interface.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_000A

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0

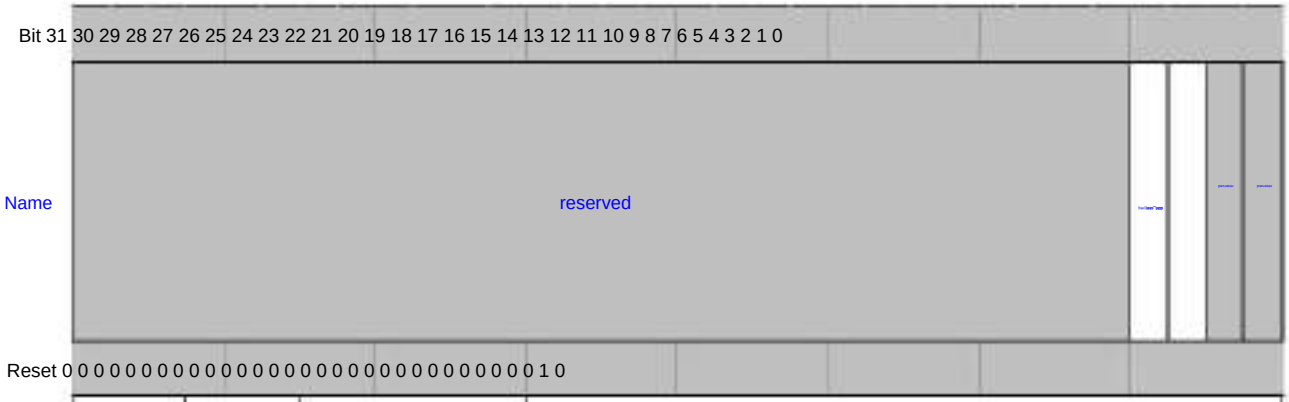
Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	ext_fephy_srst_req	Soft reset request of external FEPHY. 1: Reset. 0: Cancel reset;

[6] RW ext_fephy_cksel			External FEPHY clock selection. 0ÿ25MHzÿ 1ÿ50MHzÿ
[5]	RO	reserved	reserve.
[4] RW rmii_cksel			RMII clock selection. 0: select CRG clock; 1: Select PAD input.
[3] RW gmac_if_cken			MAC_IF Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[2] RW gmac_if_srst_req			Soft reset request for MAC_IF. 0: cancel reset; 1: Reset.
[1] RW gsf_cken			GSF Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[0] RW gsf_srst_req			Soft reset request for GSF. 0: cancel reset; 1: reset.

PERI_CRG54

PERI_CRG54 is the clock and soft reset control register related to DDRT.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002



Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	RW	ddrt_cken	DDRT Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[2]	RW	ddrt_srst_req	Soft reset request for DDRT. 0: cancel reset; 1: Reset.
[1]	RO	reserved	reserve.
[0]	RO	reserved	reserve.

PERI_CRG55

PERI_CRG55 is the PWM clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x00DC	PERI_CRG55	0x0000_0000

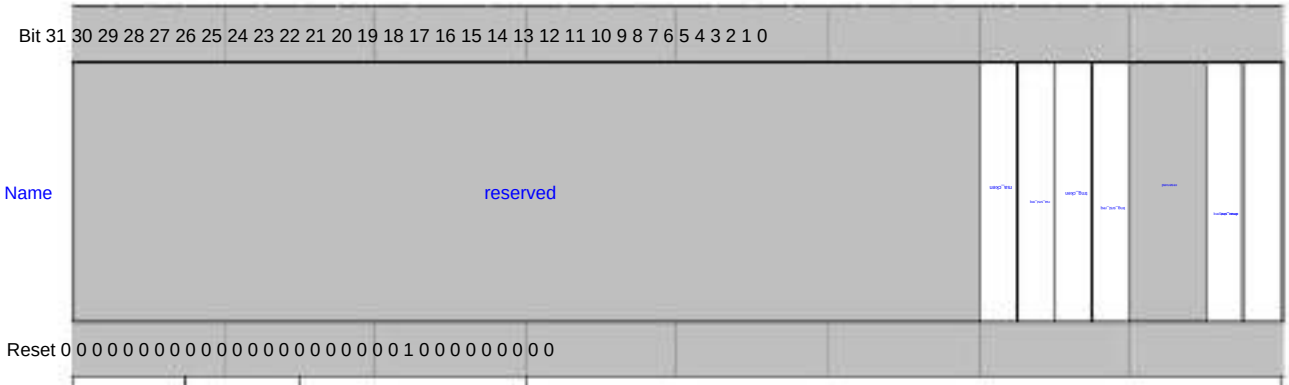
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:2]	RW	pwm_cksel	PWM clock selection. 00ÿ3MHzÿ 01ÿ50MHzÿ 1Xÿ24MHzÿ
[1]	RW	pwm_cken	PWM clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	pwm_srst_req	Soft reset request for PWM. 0: cancel reset; 1: Reset.

PERI_CRG56

PERI_CRG56 is RSA/TRNG/DMA related clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00E0	PERI_CRG56	0x0000_0200

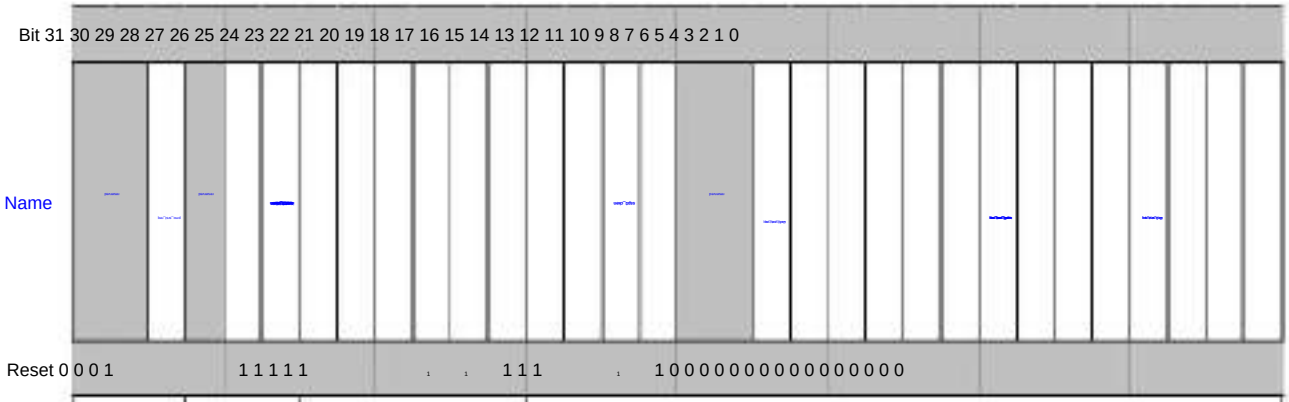


Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	rsa_cken	RSA clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[6]	RW	rsa_srst_req	Soft reset request for RSA. 0: cancel reset; 1: Reset.
[5]	RW	trng_cken	TRNG Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[4]	RW	trng_srst_req	Soft reset request for TRNG. 0: cancel reset; 1: Reset.
[3:2]	RO	reserved	reserve.
[1]	RW	dmac_cken	DMA clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	dmac_srst_req	Soft reset request for DMA. 0: cancel reset; 1: Reset.

PERI_CRG57

PERI_CRG57 is the clock soft reset control register for other APB modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x1FFF_0000



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RW	pmc_srst_req	Soft reset request for PMC. 0: cancel reset; 1: Reset.
[28]	RO	reserved	reserve.
[27]	RW	test_clk_en	Test clock enable register. 0: all test clocks are off; 1: All test clocks are on.
[26]	RW	i2c_cksel	I2C clock selection. 0: reserved; 1: Select 50MHz clock.
[25]	RW	uart_cksel	UART clock selection. 0: reserved; 1: Select 24MHz clock.
[24]	RW	uart4_cken	UART4 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[23]	RW	uart3_cken	UART3 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[22]	RW	uart2_cken	UART2 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.

[21] RW	uart1_cken		UART1 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[20] RW	uart0_cken		UART0 clock gating configuration register. 0: turn off the clock; 1: Turn on the clock.
[19] RW	ir_cken		IR Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[18] RW	ssp2_cken		SSP2 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[17] RW	ssp1_cken		SSP1 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[16] RW	ssp0_cken		SSP0 Clock Gating Configuration Register. 0: turn off the clock; 1: Turn on the clock.
[15] RO		reserved	reserve.
[14] RO		reserved	reserve.
[13] RW	i2c3_srst_req		Soft reset request for I2C3. 0: cancel reset; 1: Reset.
[12] RW	uart4_srst_req		Soft reset request for UART4. 0: cancel reset; 1: reset.
[11] RW	uart3_srst_req		Soft reset request for UART3. 0: cancel reset; 1: Reset.
[10] RW	uart2_srst_req		Soft reset request for UART2. 0: cancel reset; 1: Reset.

[9] RW	uart1_srst_req		Soft reset request for UART1. 0: cancel reset; 1: Reset.
[8] RW	uart0_srst_req		Soft reset request for UART0. 0: cancel reset; 1: Reset.
[7] RW	ir_srst_req		Soft reset request for IR. 0: cancel reset; 1: reset.
[6] RW	ssp2_srst_req		Soft reset request for SSP2. 0: cancel reset; 1: Reset.
[5] RW	ssp1_srst_req		Soft reset request for SSP1. 0: cancel reset; 1: Reset.
[4] RW	ssp0_srst_req		Soft reset request for SSP0. 0: cancel reset; 1: reset.
[3] RW	rtc_srst_req		Soft reset request for T_CAP. 0: cancel reset; 1: Reset.
[2] RW	i2c2_srst_req		Soft reset request for I2C2. 0: cancel reset; 1: Reset.
[1] RW	i2c1_srst_req		Soft reset request for I2C1. 0: cancel reset; 1: reset.
[0] RW	i2c0_srst_req		Soft reset request for I2C0. 0: cancel reset; 1: Reset.

PERI_CRG58

PERI_CRG58 is the CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

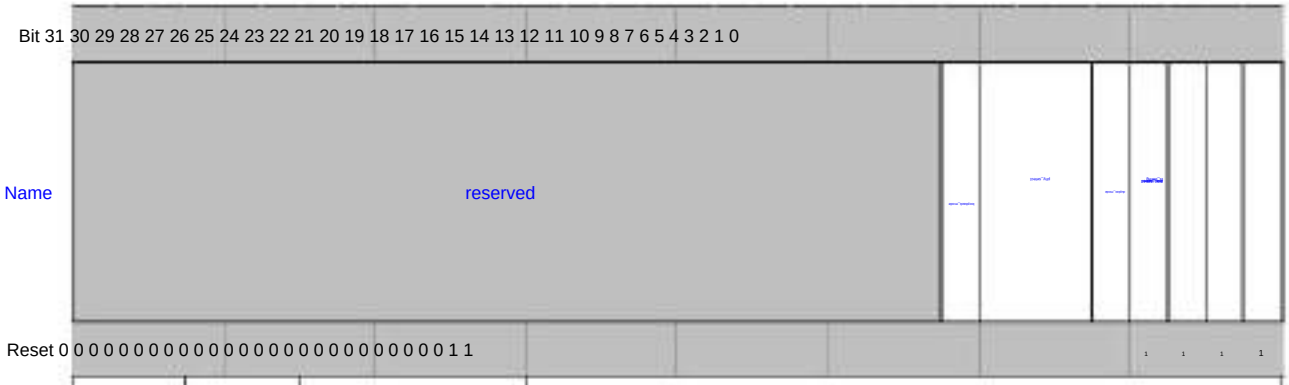
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:9]	RO	reserved	reserve.
[8]	RO	gzip_rst_ok	GZIP reset state. 0: non-reset state; 1: Reset state.
[7:5]	RO	reserved	reserve.
[4]	RO	epll_lock	EPLL LOCK status. 0ÿUnlockÿ 1ÿLockedÿ
[3]	RO	vpll_lock	VPLL LOCK state. 0ÿUnlockÿ 1ÿLockedÿ
[2]	RO	dpll_lock	DPLL LOCK status. 0ÿUnlockÿ 1ÿLockedÿ
[1]	RO	reserved	reserve.
[0]	RO	apll_lock	APLL LOCK status. 0ÿUnlockÿ 1ÿLockedÿ

PERI_CRG59

PERI_CRG59 is the GMAC interface control register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_CRG59	0x0000_003F



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	loopback_mode	Loopback mode enable signal. 0: disable; 1: enable.
[7:5]	RW	phy_select	PHY interface mode. 000: reserved; 001: RGMII mode; 100: RMII mode; Other: reserved.
[4]	RW	duplex_mode	PHY duplex mode. 0: half-duplex mode; 1: Full duplex mode.
[3]	RW	tx_config	Send configuration enable signal. 0: disable; 1: enable.
[2]	RW	link_status	PHY link state control. 0ÿLink Downÿ 1ÿLink Upÿ
[1]	RW	mac_speed	10/100Mbps mode. 0ÿ10Mbpsÿ 1ÿ100Mbpsÿ
[0]	RW	port_select	Network port selection mode. 0ÿ1000Mbpsÿ 1ÿ10/100Mbpsÿ

PERI_CRG60

PERI_CRG60 is the GMAC interface status register.

Offset Address	Register Name	Total Reset Value
0x00F0	PERI_CRG60	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / gmac_if_sys_stat
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RO	link_status	The connection status when both rxdv and rxer are 0 in RGMII mode. 0ÿlink downÿ 1ÿlink upÿ
[2:1]	RO	link_speed	The rate status when both rxdv and rxer are 0 in RGMII mode. 0:2.5MHzÿ 01ÿ25MHzÿ 10ÿ125MHzÿ 11: Reserved.
[0]	RO	link_mode	The mode state when both rxdv and rxer are 0 in RGMII mode. 0ÿhalf-duplexÿ 1ÿfull-duplexÿ

PERI_CRG79

PERI_CRG79 is the SOC frequency profile status register.

Offset Address	Register Name	Total Reset Value
0x013C	PERI_CRG79	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:10]	RO reserved	reserve.
[9]	RO bus_sc_seled	Bus clock switch complete indication signal. 0: switch to crystal oscillator clock; 1: switch to 200MHz.
[8:6]	RO ddr_sc_seled	DDR clock switch complete indication signal. 000: switch to crystal oscillator clock; 001: switch to DPLL FOUTPOSTDIV clock; 010: switch to 476MHz; 011: switch to 396MHz; 100: switch to 346MHz; 101: switch to 300MHz; 110: switch to 250MHz; others: reserved.
[5:3]	RO a17_sc_seled	A17 Clock switching completion indication signal. 000: switch to crystal oscillator clock; 001: switch to APLL FOUTVCOV clock; 010: switch to DPLL FOUTVCO clock; 011: switch to 1000MHz; 100: switch to 792MHz; 101: switch to 594MHz; 110: switch to 500MHz; 111: Switch to 400MHz.

[2:0] RO a7_sc_seled			A7 Clock switching completion indication signal. 000: switch to crystal oscillator clock; 001: switch to DPLL FOUTVCO clock; 010: switch to APLL FOUTPOSTDIV clock; 011: switch to 792MHz; 100: switch to 750MHz; 101: switch to 594MHz; Others: reserved.

3.3 Processor Subsystem

Hi3519V100 adopts ARM Cortex-A17UP single-core processor and Cortex-A7UP single-core processor, both of which are HMP (asymmetric multi-core) architecture.

Among them, Cortex-A17UP has the following characteristics:

- The highest operating frequency of the processor is 1150MHz, supports DVFS, and supports AVS.
- 32KB L1 Instruction Cache and 32KB L1 Data Cache.
- 256KB L2 cacheÿ
- 3.3 DMIPS/MHzÿ
- Contains MMU (Memory Management Unit). Integrated NEON
- (including FPU hardware floating-point coprocessor).

Cortex-A7UP has the following features:

- The highest operating frequency of the processor is 800MHz and supports DFS.
- 32KB L1 Instruction Cache and 32KB L1 Data Cache.
- 128KB L2 cacheÿ
- 1.9 DMIPS/MHzÿ
- Contains MMU (Memory Management Unit). Integrated NEON
- (including FPU hardware floating-point coprocessor).

The HMP (asymmetric multi-core) architecture has the following characteristics:

- Support A7, A17 Big-little architecture Support
- A17 dynamic switch core
- Support unified interrupt handling

3.4 Interrupt System

Hi3519V100 supports 128 interrupt sources, and the corresponding interrupt mapping is shown in Table 3-7 .

Table 3-7 Interrupt source allocation table

interrupt bit interrupt source		interrupt bit	interrupt source
0~31	CPU internal interrupt	67	VGS
32	WatchDog	68	AIAO
33	RTC/TEM_CAP	69	OURS
34	reserve	70	JPGE
35	reserve	71	IVE
36	UART0	72	reserve
37	UART1	73	GZIP
38	UART2	74	Software int
39	UART3	75	GPIO0~7
40	UART4	76	GPIO8~13
41	SSP0/I2C0	77	A7_PMU
42	SSP1/I2C1	78	A17_PMU
43	SSP2/I2C2	79	CCI
44	I2C3	80	GDC
45	eMMC	81	A17_COMMRX
46	reserve	82	A17_COMMTX
47	AND	83	A7_COMMRX
48	LSADC	84	A7_COMMTX
49	DMAC	85	reserve
50	FMC	86	PCIE_CFG_LINK_AUTO _Mr
51	USB2_EHCI	87	PCIE_CFG_BW_MGT
52	USB2_OHCI	88	PCIE_PM
53	USB2_DEV	89	PCIE_INT
54	USB3	90	PCIE_INTB
55	SDIO0	91	PCIE_INTC
56	SDIO1	92	PCIE_INTD

interrupt bit interrupt source		interrupt bit	interrupt source
57	GSF	93	PCIE_EDMA
58	Cipher	94	PCIE_MSI
59	VDP	95	PCIE_LINK_DOWN
60	MIPI	96	Timer0
61	reserve	97	Timer1
62	VICAP	98	Timer2
63	reserve	99	Timer3
64	VPSS	100	Timer4
65	reserve	101	Timer5
66	TDE	102~127 reserved	

3.5 System Controller

3.5.1 Overview

The system controller manages important functions in the system and completes the configuration of some functions of the peripherals.

3.5.2 Features

The system controller has the following characteristics:

Provides control and status monitoring of system address remapping

Provides general-purpose peripheral registers

Provides the write protection function for key registers

Provides the identification register of the chip

3.5.3 Functional description

3.5.3.1 Soft Reset Control

The system controller supports soft reset for the global and local modules of the chip:

After configuring the global soft reset register SC_SYSRES , the system controller will initiate a request to the on-chip reset module, and the chip will be reset.

3.5.3.2 System Address Remapping Control

Please refer to chapter "1.5 Address Space Mapping".

3.5.3.3 Write protection of key registers

In order to prevent the misoperation of the software on the system controller from seriously affecting the entire system, the system controller provides a write protection function for some key configuration registers, including the system control register and the system soft reset register (SC_CTRL and SC_SYSRES) . Before writing to these key registers, the register SC_LOCKEN must be configured to open the write permission. After the operation is completed, configure the register SC_LOCKEN, close the write permission, and protect these key registers from being rewritten by software.

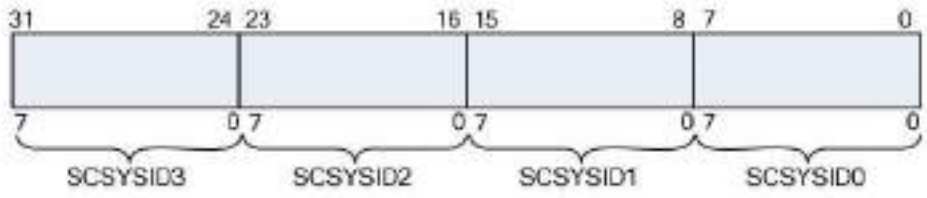
说明

By default, the system does not write-protect these key registers after reset. In order to enable this function, it is recommended to use the register SC_LOCKEN to write-protect these key registers at system startup .

3.5.3.4 Chip identification register

The system controller provides the chip identification (ID) register SC_SYSID. This identification register is a 32-bit identification read-only register, which actually consists of four 8-bit identification registers: SCSYSID3, SCSYSID2, SCSYSID1, SCSYSID0. Read out the values of these 4 registers, and obtain the value 0x3519_0100 of the chip's 32-bit identification read-only register through combination. The combination method is shown in Figure 3-4 .

Figure 3-4 Chip ID register bit allocation diagram



3.5.4 System Controller Registers

3.5.4.1 System Controller Register Overview

An overview of the system controller registers is shown in Table 3-8 .

Table 3-8 Overview of system controller registers (base address is 0x1202_0000)

offset address	name	describe	page number
0x000	SC_CTRL	System Control Register	3-62
0x004	SC_SYSRES	System Soft Reset Register	3-63
0x001C	SOFT_INT	softirq register	3-64
0x0044	SC_LOCK	Lock Register for Critical System Control Registers 3-64	
0x008C	SYSSTAT	System Status Register	3-65
0xEE0	SCSYSID0	Chip ID Register 0	3-68

offset address	name	describe	page number
0xEE4	SCSYSID1	Chip ID Register 1	3-68
0xEE8	SCSYSID2	Chip ID Register 2	3-68
0xEEC	SCSYSID3	Chip ID Register 3	3-69

3.5.4.2 System Controller Register Description

SC_CTRL

SC_CTRL is the system control register. Used to specify actions that require the system to complete.

注意

This register can be write-protected by the register SC_LOCKEN , only when the write protection mode is not used, this register The write operation is valid.

Offset Address: 0x000 | Register Name: SC_CTRL | Total Reset Value: 0x0000_0202

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved | ... | reserved | ... | reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	RW	timeren5ov	Timer5 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[25]	RO	reserved	reserve.
[24]	RW	timeren4ov	Timer4 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[23]	RO	reserved	reserve.

[22] RW	timer3ov		Timer3 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[21] RO		reserved	reserve.
[20] RW	timer2ov		Timer2 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[19] RO		reserved	reserve.
[18] RW	timeren1ov		Timer1 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[17] RO		reserved	reserve.
[16] RW	timeren0ov		Timer0 count clock selection. 0: use 3MHz clock for counting; 1: Count by bus clock.
[15] RO		reserved	reserve.
[14:10] RO		reserved	reserve. Returns 0 on read, no effect on write.
[9]	RO	remapstat	Status of address remapping. 0: no address remapping; 1: Perform address remapping. The Flash address space connected to Bootrom or FMC CS0 is remapped to address 0.
[8] RW	remapclear		Address remapping clears the selection. 0: Keep Remap status. 1: Clear Remap. For the address mapping relationship before and after Clear Remap, please refer to Address Allocation (1 Product Overview/1.4 Boot Mode/1.5 Address Space Mapping).
[7:0] RO		reserved	reserve.

SC_SYSRES

SC_SYSRES is the system soft reset register. Writing any value to this register will cause the system controller to send a system soft reset request to the reset module, and the reset module will perform a system soft reset.

注意

This register can be write-protected by the register SC_LOCKEN , and the write operation to this register is valid only when the write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access Name		Description
[31:0]	WO softresreq		Any write operation to this register will cause a soft reset of the system.

SOFT_INT

SOFT_INT is the soft interrupt register.

Offset Address	Register Name	Total Reset Value
0x001C	SOFT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW software_int		Software interrupt. 0: no interrupt is generated; 1: Generate an interrupt.

SC_LOCKEN

SC_LOCKEN is the lock register for key system control registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lock	Lock register for key system control registers. The registers involved include SC_CTRL and SYSSTAT. Write 0x1ACC_E551 to this register to open the write permission of all registers, and write other values to close the write permission. Reading this register returns the status of the lock rather than the value written to this register. 0x0000_0000: Allows write access (unlocked) to critical system control registers. 0x0000_0001: Disable write access to critical system control registers (locked).

SYSSTAT

SYSSTAT is the system status register.

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	bootrom_sel	Indicates whether to boot from bootrom. 0: Do not start from bootrom; 1: Start from bootrom.

[30] RO	a17_standbywfil2		A17 L2 WFI status indicator bit. 0: not in WFI state; 1: In WFI state.
[29] RO	a17_standbywfe		A17 WFE status indicator bit. 0: not in WFE state; 1: In WFE state.
[28] RO		a17_standbybywfi	A17 WFI status indicator bit. 0: not in WFI state; 1: In WFI state.
[27] RO	a7_standbywfil2		A7 L2 WFI status indicator bit. 0: not in WFI state; 1: In WFI state.
[26] RO	a7_standbywfe		A7 WFE status indicator bit. 0: not in WFE state; 1: In WFE state.
[25] RO		a7_standbybywfi	A7 WFI status indicator bit. 0: not in WFI state; 1: In WFI state.
[24] RO	reserved		reserve.
upgrade; [23] RO	update_from_sdio0 1:		Indicates whether to upgrade from SDIO0 card. 0: No Upgrade. Refer to the description of the boot_mode register.
[22] RO	pcie_ref_clk_sel		Indicates the PCIe PHY reference clock selection. 0: Internal CRG clock; 1: External clock input.
[21] RO		combo phy. PCIe; sel combo_phy_	Indicates the mode of the mode_0: 1ÿUSB3.0ÿ
[20:8] RO	reserved		reserve.

[7]	RO		When boot_mode=2'b00 and sfc_device_mode=0, it means: SPI Nor Flash boot address mode selection. 0ÿ3byteÿ 1: 4byte. When boot_mode=2'b00 and sfc_device_mode=1, it means: SPI Nand Flash boot mode selection. sfc_emmc_boot_mode 0: 1 wire boot; 1: 4-wire boot. When boot_mode=2'b10 means: eMMC boot mode selection. 0: 4-wire boot; 1: 8-wire boot.
[6]	RO reserved		reserve.
[5:4]	RO boot_mode		Chip start mode. When bootrom_sel=0: 00: SPI Flash starts; 01: Nand Flash start; 10: eMMC boot; 11: PCIe slave boot. When bootrom_sel=1 and update_from_sdio0=0: 00: Enter FastBoot, jump to SPI Flash boot after timeout; 01: Enter FastBoot, jump to Nand Flash boot after timeout; 10: Enter FastBoot, jump to eMMC boot after timeout ; 11: reserved. When bootrom_sel=1 and update_from_sdio0=1: 00: upgrade from SDIO0 to SPI Flash; 01: upgrade from SDIO0 to Nand Flash; 10: Upgrade from SDIO0 to eMMC; 11: Reserved.
[3]	RO	sfc_device_mode	SPI FLASH device selection. 0: SPI NOR FLASH device; 1: SPI NAND FLASH device.
[2]	RO	spi_nand_sel	SPI Nand Flash device timing selection. 0: Plane address bit is disabled; 1: Plane address bit is enabled.
[1:0]	RO reserved		reserve.

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	chipid	reserved	sysid0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:24]	RO	chipid	Chip version information.
[23:8]	RO	reserved	reserve.
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0x01

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[7:0]	RO	sysid1	Reading this register returns 0x01.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x19

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	0	1	1	0	0	1

Bits	Access Name		Description
[7:0]	RO	sysid2	Reading this register returns 0x19.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access Name		Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5.5 Peripheral Control Registers

3.5.5.1 Peripheral Control Register Overview

An overview of the peripheral control registers is shown in Table 3-9 .

Table 3-9 Overview of peripheral control registers (base address is 0x1203_0000)

offset address	name	describe	page number
0x0000	MISC_CTRL0	VICAP&VPSS&MIPI PHY Control Register 3-71	
0x0004	MISC_CTRL1	Peripheral Function Select Register 0	3-72
0x0008	MISC_CTRL2	PCIe read current limit control register	3-74
0x000C	MISC_CTRL3	POWERSWITCH CONTROL REGISTER	3-75
0x0010	MISC_CTRL4	RET1N Control Register	3-77
0x0014	MISC_CTRL5	System Bus Arbitration Control Register 0	3-78

offset address	name	describe	page number
0x0018	MISC_CTRL6	System Bus Arbitration Control Register 1	3-78
0x001C	MISC_CTRL7	System Bus Arbitration Control Register 2	3-79
0x0020	MISC_CTRL8	System Bus Priority Control Register 0	3-80
0x0024	MISC_CTRL9	System Bus Priority Control Register 1	3-81
0x002C	MISC_CTRL11	MEDIA0 bus arbitration control register 0	3-82
0x0030	MISC_CTRL12	MEDIA0 bus arbitration control register 1	3-83
0x0038	MISC_CTRL14	MEDIA0 Bus Priority Control Register	3-84
0x003C	MISC_CTRL15	MEDIA1 bus arbitration control register 0	3-85
0x0040	MISC_CTRL16	MEDIA1 bus arbitration control register 1	3-86
0x0048	MISC_CTRL18	MEDIA1 Bus Priority Control Register	3-87
0x0054	MISC_CTRL21	DDR QOS Control Register 0	3-88
0x0058	MISC_CTRL22	DDR QOS Control Register 1	3-89
0x005C	MISC_CTRL23	DDR QOS Control Register 2	3-89
0x0060	MISC_CTRL24	DDR QOS Control Register 3	3-90
0x0074	MISC_CTRL29	USB3.0 Control Register	3-91
0x0078	MISC_CTRL30	USB2.0 Control Register 0	3-93
0x007C	MISC_CTRL31	TEST clock & USB2.0PHY access test path selection register	3-95
0x0080	MISC_CTRL32	USB2.0PHY Test Path Registers	3-96
0x0084	MISC_CTRL33	COMB PHY Test Path Registers	3-96
0x0088	MISC_CTRL34	PCIe&USB3.0 PHY Control Register	3-97
0x00B4	MISC_CTRL45	Audio Codec ANA register 0 (will not be soft reset)	3-99
0x00B8	MISC_CTRL46	Audio Codec ANA register 1 (will not be soft reset)	3-101
0x00BC	MISC_CTRL47	Audio Codec ANA register 2 (will not be soft reset)	3-103
0x00C0	MISC_CTRL48	Audio Codec ANA register 3 (will not be soft reset)	3-104
0x00CC	MISC_CTRL51	Audio Codec DIG control register 0 (will not be soft reset)	3-105

offset address name		describe	page number
0x00D0 MISC_CTRL52		Audio Codec DIG control register 1 (will not be soft reset)	3-107
0x00D4 MISC_CTRL53		Audio Codec DIG control register 2 (will not be soft reset)	3-108
0x00D8 MISC_CTRL54		Audio Codec DIG control register 3 (will not be soft reset)	3-109
0x00E0	MISC_CTRL56	I2S channel selection control register (will not be soft reset)	3-111
0x0140	MISC_CTRL80	eMMC Interface DLL Control Register 0	3-112
0x0144	MISC_CTRL81	eMMC Interface DLL Control Register 1	3-113
0x0154	MISC_CTRL85	PERI Bus Arbitration Control Register 0	3-114
0x0158	MISC_CTRL86	PERI Bus Arbitration Control Register 1	3-115
0x0160	MISC_CTRL88	PERI Bus Priority Control Register 0	3-115
0x0164	MISC_CTRL89	PERI Bus Priority Control Register 1	3-116
0x0174	MISC_CTRL93	VDP_AIAO Bus arbitration control register.	3-117
0x0178	MISC_CTRL94	VDP_AIAO Bus priority control register. 3-118	

3.5.5.2 Peripheral Control Register Description

MISC_CTRL0

MISC_CTRL0 is VICAP&VPSS&MIPI PHY control register.

Offset Address	Register Name	Total Reset Value
0x0000	MISC_CTRL0	0x0000_0054

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep000																														reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0

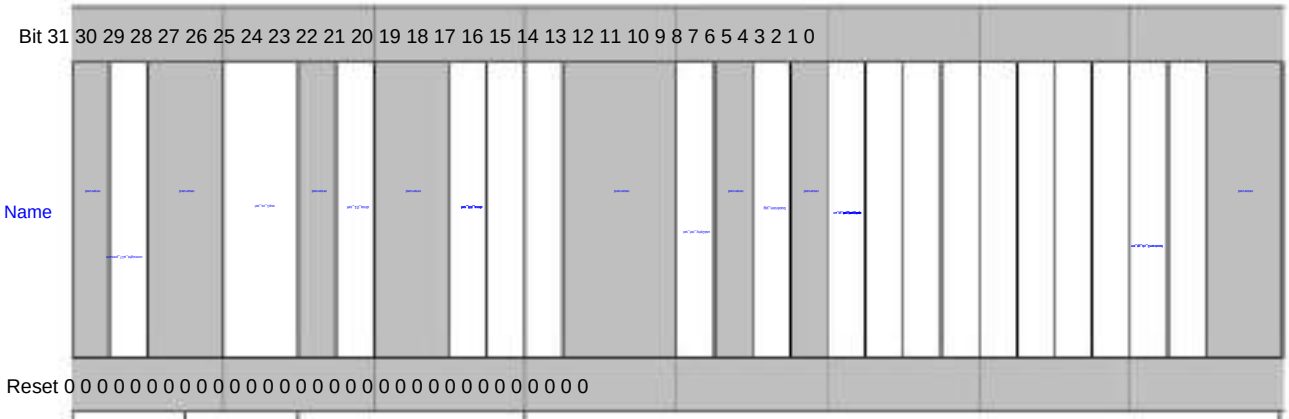
Bits	Access	Name	Description
[31:10]	RO	reserved_keep000	Reserved.

[9] RW		vicap0_vpss0_onlin 0:	Whether VICAP0 and VPSS0 are in online mode. offline mode; 1: Online mode.
[8]	RO	reserved	reserve.
[7:6] RW	mipi0_work_mode		MIPI 0 mode selection. 00: MIPI mode; 01: LVDS mode; 10: CMOS mode; 11: Reserved.
[5:0] RO		reserved	reserve.

MISC_CTRL1

MISC_CTRL1 is peripheral function selection register 0.

Offset Address	Register Name	Total Reset Value
0x0004	MISC_CTRL1	0x0000_0000



Bits	Access	Name	Description
[31] RO		reserved	reserve.
[30] RW		coresight_a17_pres 0:	A17 coresight function switch control. off; ent 1: open.
[29:28] RO		reserved	reserve.
[27:26] RW	ssp1_cs_sel		SSP1 output chip select select. 00: chip selection 0; 01: chip selection 1; 1X: reserved.

[25] RO		reserved	reserve.
[24] RW dma_01_sel			DMA hardware request line 0, 1 connection selection. 0: UART0 is connected to it; 1: UART4 is connected to it.
[23:22] RO		reserved	reserve.
[21] RW dma_89_sel			DMA hardware request line 8, 9 connection selection. 0ÿI2C0ÿ 1ÿSSP0ÿ
[20] RW dma_ab_sel			DMA hardware request line 10, 11 connection selection. 0ÿI2C1ÿ 1ÿSSP1ÿ
[19] RW dma_cd_sel			DMA hardware request line 12, 13 connection selection. 0ÿI2C2ÿ 1ÿSSP2ÿ
[18:16] RO		reserved	reserve.
[15] RW usb2phy_ctrl_sel			USB2.0 PHY control source selection. 0ÿUSB2.0 Ctrlÿ 1ÿUSB3.0 Ctrlÿ
[14] RO		reserved	reserve.
[13] RW bootrom_pg			BOOTROM low power mode control. 0: normal mode; 1: low power mode.
[12] RO		reserved	reserve.
[11] RW spi2_cs0_ctrl			spi2_cs0 signal inversion control. 0: no negation; 1: Reversal.
[10] RW spi1_cs1_ctrl			spi1_cs1 signal inversion control. 0: no negation; 1: Reversal.
[9] RW spi1_cs0_ctrl			spi1_cs0 signal inversion control. 0: no negation; 1: Reversal.

[8] RW spi0_cs0_ctrl			spi0_cs0 signal inversion control. 0: no negation; 1: Reversal.
[7] RW uart1_rts_ctrl			uart1_rts signal inversion control. 0: no negation; 1: Reversal.
[6] RW uart2_rts_ctrl			Uart2_rts signal inversion control. 0: no negation; 1: Reversal.
[5] RW bootram3_ck_gt_en			BOOTRAM3 clock enable control. 0: clock enable; 1: Turn off the clock.
RW bootram2_ck_gt_en			BOOTRAM2 clock enable control. 0: clock enable; [4] 1: Turn off the clock.
RW bootram1_ck_gt_en		1: Disable clock.	BOOTRAM1 clock enable control. 0: Enable clock; [3]
[2] RW bootram0_ck_gt_en			BOOTRAM0 clock enable control. 0: clock enable; 1: Turn off the clock.
[1:0] RO		reserved	reserve.

MISC_CTRL2

MISC_CTRL2 is the PCIe read current limit control register.

Offset Address	Register Name	Total Reset Value
0x0008	MISC_CTRL2	0x0000_0104

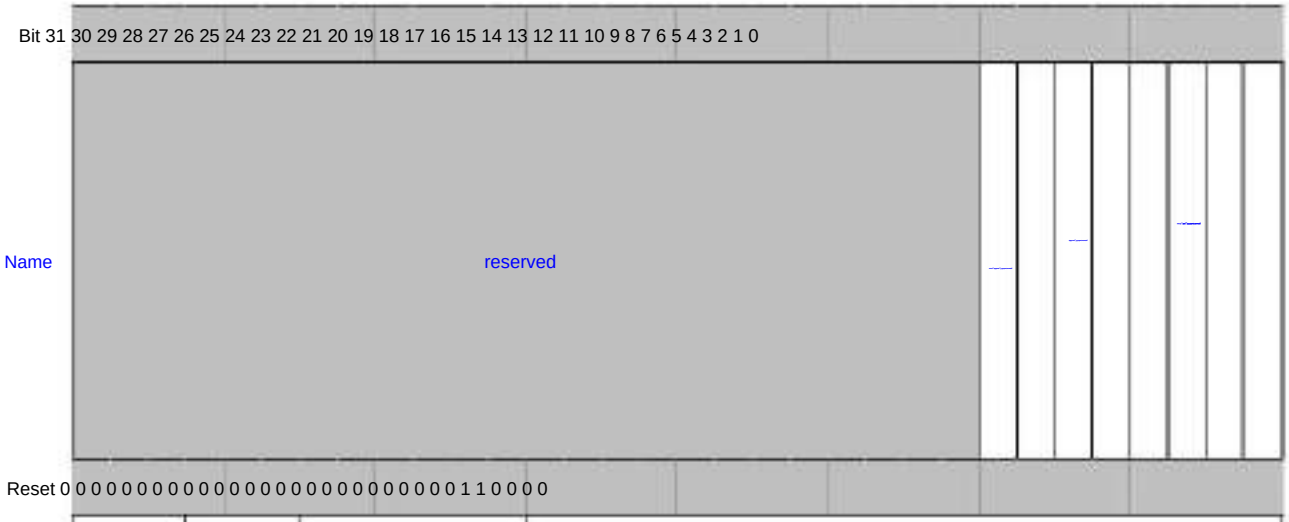
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved_keep001	----	pcie_m_from_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved_keep001	Reserved.
[8]	RW	pcie_m_od_bypass	PCIE MASTER read outstanding limit enable control. 0: open; 1: Off.
[7:0]	RW	pcie_m_od_max	PCIE MASTER read outstanding number. 0 cannot be written. The actual effective value is the configuration value plus 1.

MISC_CTRL3

MISC_CTRL3 is the POWERSWITCH control register.

Offset Address	Register Name	Total Reset Value
0x000C	MISC_CTRL3	0x0000_0030



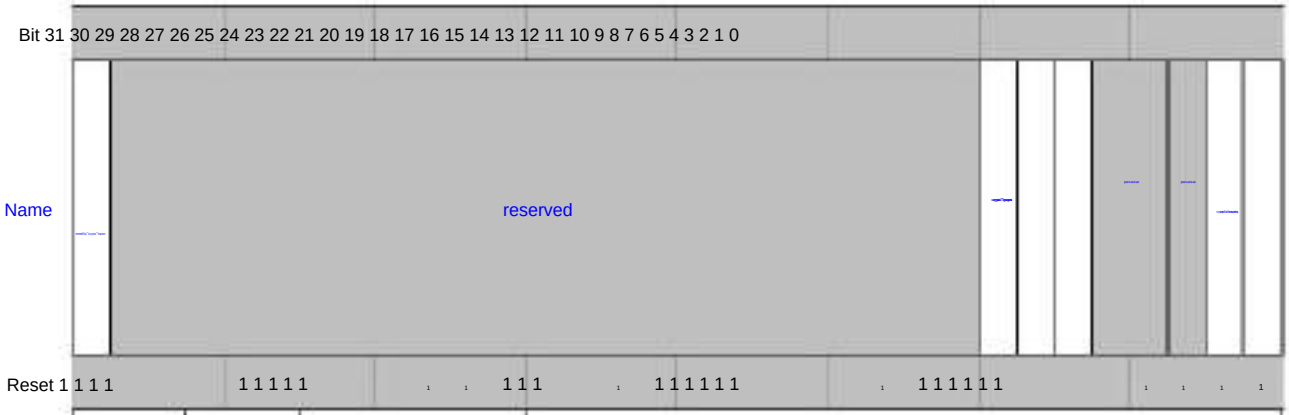
Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	powerswitch1_enab	powerswitch1 enable select source select signal. 0: from SDIO1 controller; le_mux 1: From register powerswitch1_enable.
[6]	RW	powerswitch0_enab	powerswitch0 enable select source select signal. 0: from SDIO0 controller; le_mux 1: From register powerswitch0_enable.
[5]	RW	powerswitch1_enable	powerswitch1 switch enable signal (only valid when _mux is 1). powerswitch1_enable 1: enable; 0: off.
[4]	RW	powerswitch0_enable	powerswitch0 switch enable signal (only valid when _mux is 1). powerswitch0_enable 1: enable; 0: off.
[3]	RW	powerswitch1_sel_	The powerswitch1 switch selects the source selection signal. 0: from SDIO1 controller; mux 1: From register powerswitch1_sel.
[2]	RW	powerswitch1_sel	powerswitch1 switch selection signal (only valid when powerswitch1_sel_mux is 1). 1: powerswitch1 outputs 1.8V; 0: powerswitch1 outputs 3.3V.

[1] RW		selection signal. mux	The powerswitch0 switch selects the source powerswitch0_sel_0: from SDIO0 controller; 1: From register powerswitch0_sel.
[0] RW	powerswitch0_sel		powerswitch0 switch selection signal (only valid when powerswitch0_sel_mux is 1). 1: powerswitch0 outputs 1.8V; 0: powerswitch0 outputs 3.3V.

MISC_CTRL4

MISC_CTRL4 is the RET1N control register.

Offset Address	Register Name	Total Reset Value
0x0010	MISC_CTRL4	0xFFFF_FFFF



Bits	Access	Name	Description
[31]	RW	vedu_ret1n_bypass	1: bypass; 0: enable. The VEDU module automatically selects the mem ret1n function bypass.
[30:8]	RO	reserved	reserve.
[7]	RW	emmc_ret1n	For the RET1N signal of MEM in eMMC CTRL, please set 1 when eMMC CTRL is enabled, and set 0 when eMMC CTRL is not enabled, to save power consumption of MEM.
[6]	RW	sdio1_ret1n	For the RET1N signal of MEM in SDIO1 CTRL, please set 1 when SDIO1 CTRL is enabled, and set 0 when SDIO1 CTRL is not enabled, to save power consumption of MEM.
[5]	RW	sdio0_ret1n	For the RET1N signal of MEM in SDIO0 CTRL, please set 1 when SDIO0 CTRL is enabled, and set 0 when SDIO0 CTRL is not enabled, to save power consumption of MEM.
[4]	RO	reserved	reserve.
[3]	RO	reserved	reserve.

[2]	RO	reserved	reserve.
[1] RW cipher_ret1n			The RET1N signal of MEM in CIPHER should be set to 1 when CIPHER is enabled, and set to 0 when CIPHER is not enabled to save power consumption of MEM.
[0] RW bootram_ret1n			For the RET1N signal of MEM in BOOTRAM, please set 1 when BOOTRAM is enabled, and set 0 when BOOTRAM is not enabled, to save power consumption of MEM.

MISC_CTRL5

MISC_CTRL5 is the system bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0014	MISC_CTRL5	0x0000_0000

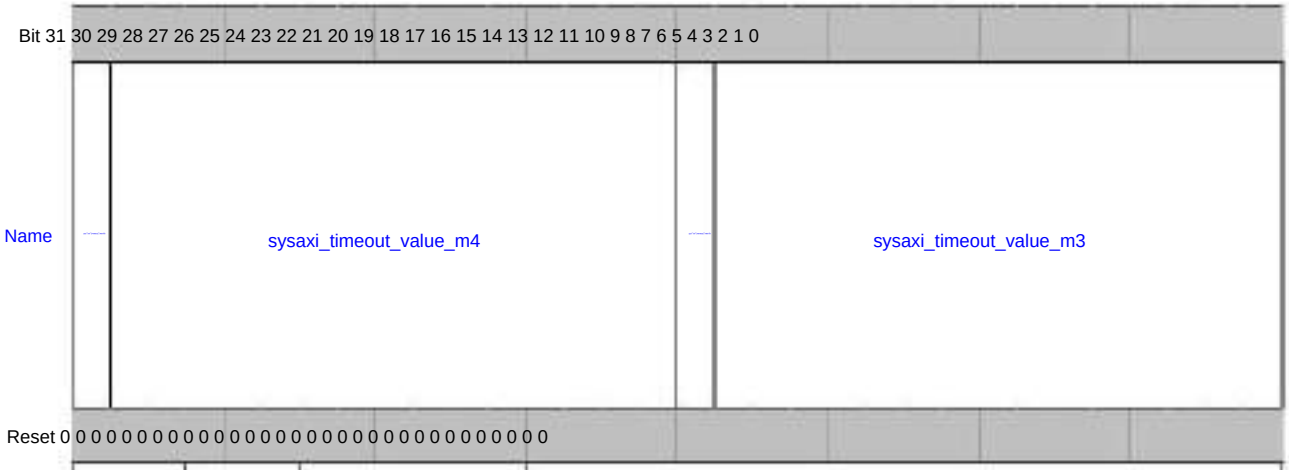
Bit	31	30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	---	sysaxi_timeout_value_m2
	---	sysaxi_timeout_value_m1
Reset	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_ 0:	Timeout count enable for SYS AXI bus port M2(ahb1). disable; m2 1: enable.
[30:16]	RW	sysaxi_timeout_value_m2 count	SYS AXI bus port M2 (ahb1) timeout count value. value=sysaxi_timeout_value_m2×2.
[15]	RW	sysaxi_timeout_en_ 0:	Timeout count enable for SYS AXI bus port M1(ahb0). disable; m1 1: enable.
[14:0]	RW	sysaxi_timeout_value_m1 count	SYS AXI bus port M1(ahb0) timeout count value. value=sysaxi_timeout_value_m1×2.

MISC_CTRL6

MISC_CTRL6 is the system bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0018	MISC_CTRL6	0x0000_0000

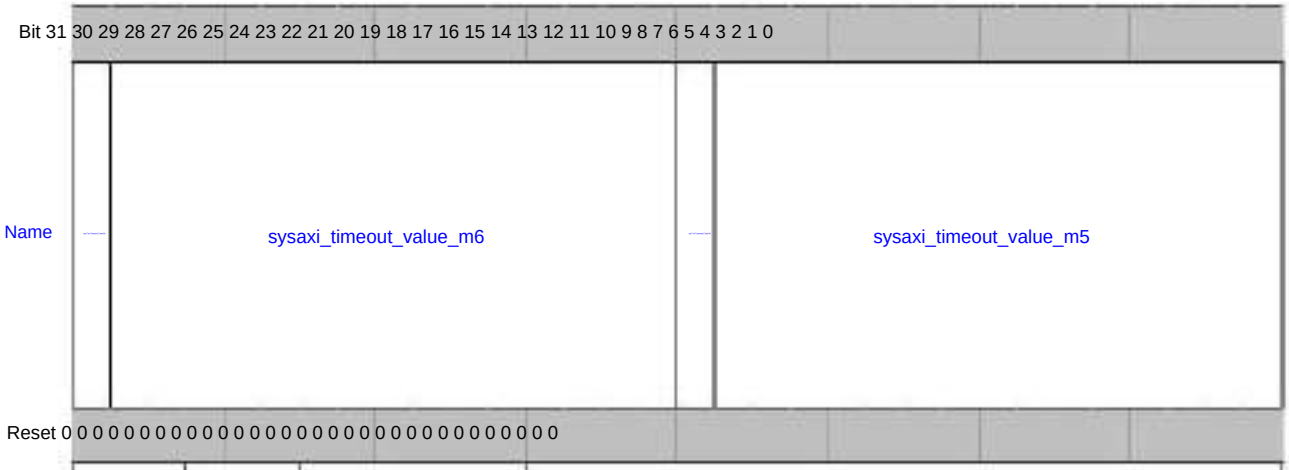


Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_m4	SYS AXI bus port M4 (usb3) timeout count enable. 0: disable; 1: enable.
[30:16]	RW	sysaxi_timeout_value_m4	SYS AXI bus port M4 (usb3) timeout count value. count value=sysaxi_timeout_value_m4×2.
[15]	RW	sysaxi_timeout_en_m3	Timeout count enable for SYS AXI bus port M3(gsf). 0: disable; 1: enable.
[14:0]	RW	sysaxi_timeout_value_m3	SYS AXI bus port M3(gsf) timeout count value. count value=sysaxi_timeout_value_m3×2.

MISC_CTRL7

MISC_CTRL7 is the system bus arbitration control register 2.

Offset Address	Register Name	Total Reset Value
0x001C	MISC_CTRL7	0x0000_0000

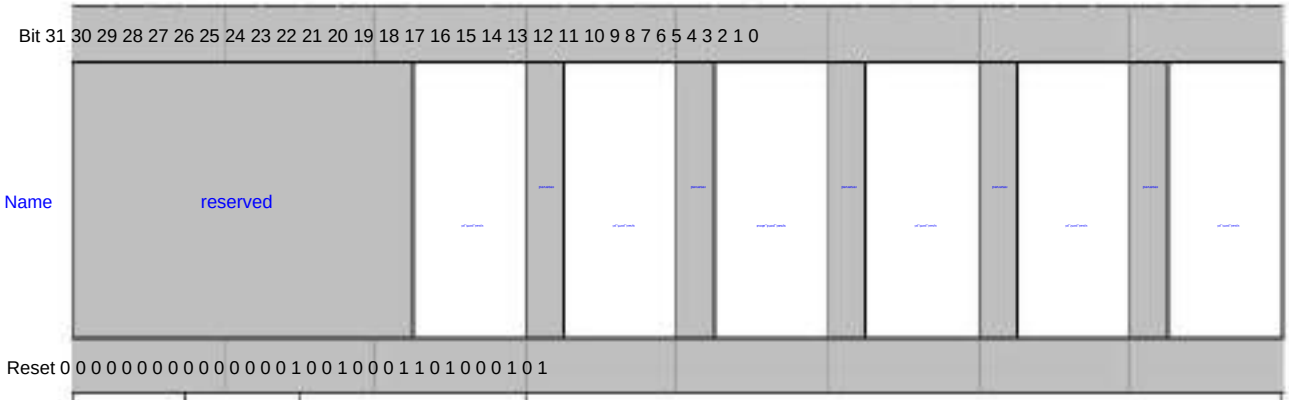


Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_m6	Timeout count enable for SYS AXI bus port M6(ahb2). 0: disabled; 1: enable.
[30:16]	RW	sysaxi_timeout_value_m6	SYS AXI bus port M6 (ahb2) timeout count value. count value=sysaxi_timeout_value_m4×2.
[15]	RW	sysaxi_timeout_en_m5	SYS AXI bus port M5 (pcie) timeout count enable. 0: disable; 1: enable.
[14:0]	RW	sysaxi_timeout_value_m5	SYS AXI bus port M5 (pcie) timeout count value. count value=sysaxi_timeout_value_m5×2.

MISC_CTRL8

MISC_CTRL8 is the system bus priority control register 0.

Offset Address	Register Name	Total Reset Value
0x0020	MISC_CTRL8	0x0001_2345



Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22:20]	RW	sysaxi_port6_pri	SYS AXI bus port M6 (ahb2) priority. 7 is the highest priority.
[19]	RO	reserved	reserve.
[18:16]	RW	sysaxi_port5_pri	SYS AXI bus port M5(pcie) priority. 7 is the highest priority.
[15]	RO	reserved	reserve.
[14:12]	RW	sysaxi_port4_pri	SYS AXI bus port M4 (usb3) priority. 7 is the highest priority.
[11]	RO	reserved	reserve.
[10:8]	RW	sysaxi_port3_pri	SYS AXI bus port M3(gsf) priority. 7 is the highest priority.
[7]	RO	reserved	reserve.
[6:4]	RW	sysaxi_port2_pri	SYS AXI bus port M2 (ahb1) priority. 7 is the highest priority.
[3]	RO	reserved	reserve.
[2:0]	RW	sysaxi_port1_pri	SYS AXI bus port M1 (ahb0) priority. 7 is the highest priority.

MISC_CTRL9

MISC_CTRL9 is the system bus priority control register 1.

Offset Address	Register Name	Total Reset Value
0x0024	MISC_CTRL9	0x0000_0001

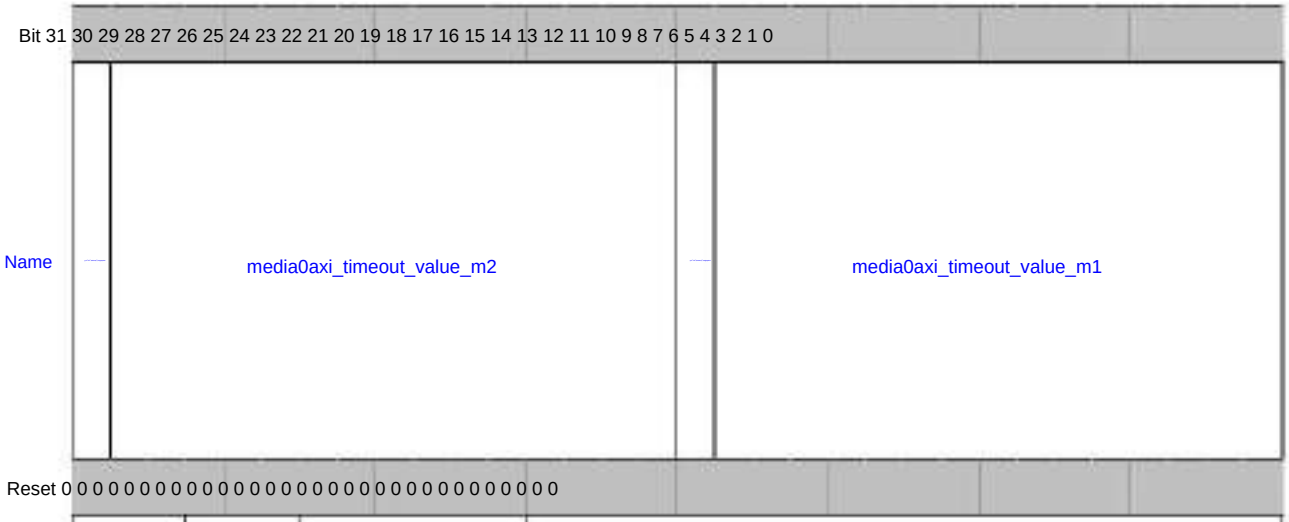
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6:4]	RW	sysaxi_slave_priority_s2	SYS AXI s2 (peri_axi) port bus access priority. 3 is the highest priority.
[3]	RO	reserved	reserve.
[2:0]	RW	sysaxi_slave_priority_s1	SYS AXI s1(mddrc) port bus access priority. 3 is the highest priority.

MISC_CTRL11

MISC_CTRL11 is MEDIA0 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x002C	MISC_CTRL11	0x0000_0000



Bits	Access	Name	Description
[31]	RW	media0axi_timeout_en_m2	MEDIA0 AXI bus port M2 (VGS) timeout count enable. 0: disable; 1: enable.
[30:16]	RW	media0axi_timeout_value_m2	MEDIA0 Timeout count value of AXI bus port M2(VGS). count value=media0axi_timeout_value_m2×2.
[15]	RW	media0axi_timeout_en_m1	MEDIA0 AXI bus port M1 (VEDU) timeout count enable. 0: disable; 1: enable.
[14:0]	RW	media0axi_timeout_value_m1	MEDIA0 Timeout count value of AXI bus port M1(VEDU). count value=media0axi_timeout_value_m1×2.

MISC_CTRL12

MISC_CTRL12 is MEDIA0 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0030	MISC_CTRL12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved_keep0	—	media0axi_timeout_value_m3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved_keep0	Reserved.
[15]	RW	media0axi_timeout_en_m3	MEDIA0 AXI bus port M3 (GDC) timeout count enable. 0: disable; 1: enable.
[14:0]	RW	media0axi_timeout_value_m3	MEDIA0 Timeout count value of AXI bus port M3 (GDC). count value=media0axi_timeout_value_m1×2.

MISC_CTRL14

MISC_CTRL14 is the MEDIA0 bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0038	MISC_CTRL14	0x0000_0012

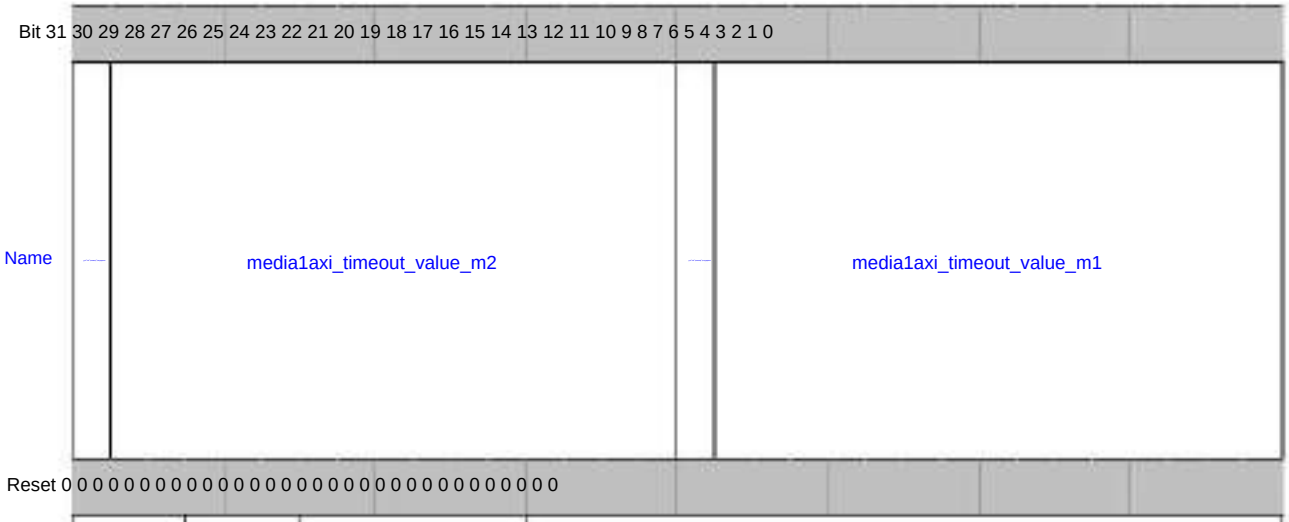
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access Name		Description
[31:11]	RO	reserved	reserve.
[10:8]	RW	3 is the highest priority.	MEDIA0 AXI bus port M3 (GDC) priority. media0axi_port3_pri
[7]	RO	reserved	reserve.
[6:4]	RW	3 is the highest priority.	MEDIA0 AXI bus port M2 (VGS) priority. media0axi_port2_pri
[3]	RO	reserved	reserve.
[2:0]	RW	3 is the highest priority.	MEDIA0 AXI bus port M1 (VEDU) priority. media0axi_port1_pri

MISC_CTRL15

MISC_CTRL15 is MEDIA1 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x003C	MISC_CTRL15	0x0000_0000

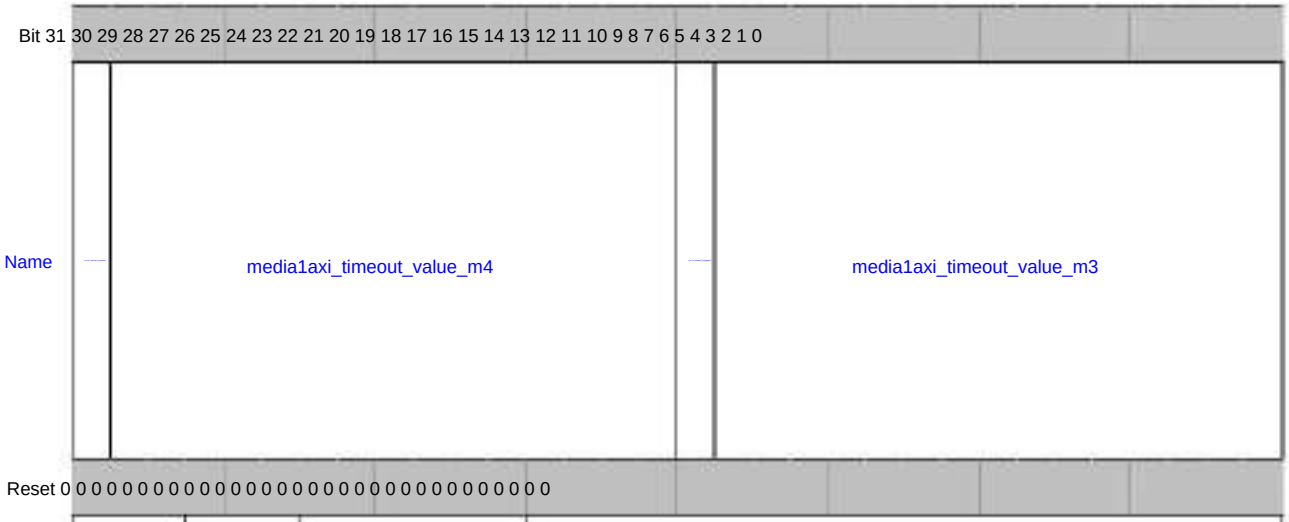


Bits	Access	Name	Description
[31]	RW	media1axi_timeout_en_m2	MEDIA1 AXI bus port M2 (JPGE) timeout count enable. 0: disable; 1: enable.
[30:16]	RW	media1axi_timeout_value_m2	MEDIA1 AXI bus port M2 (JPGE) timeout count value. count value=media1axi_timeout_value_m2×2.
[15]	RW	media1axi_timeout_en_m1	MEDIA1 Timeout count enable for AXI bus port M1(TDE). 0: disable; 1: enable.
[14:0]	RW	media1axi_timeout_value_m1	MEDIA1 Timeout count value of AXI bus port M1(TDE). count value=media1axi_timeout_value_m1×2.

MISC_CTRL16

MISC_CTRL16 is MEDIA1 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0040	MISC_CTRL16	0x0000_0000



Bits	Access	Name	Description
[31]	RW	media1axi_timeout_en_m4	MEDIA1 AXI bus port M4 (GZIP) timeout count enable. 0: disable; 1: enable.
[30:16]	RW	media1axi_timeout_value_m4	MEDIA1 AXI bus port M4 (GZIP) timeout count value. count value=media1axi_timeout_value_m4×2.
[15]	RW	media1axi_timeout_en_m3	MEDIA1 AXI bus port M3(IVE) timeout count enable. 0: disable; 1: enable.
[14:0]	RW	media1axi_timeout_value_m3	MEDIA1 Timeout count value of AXI bus port M3(IVE). count value=media1axi_timeout_value_m3×2.

MISC_CTRL18

MISC_CTRL18 is the MEDIA1 bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0048	MISC_CTRL18	0x0001_2345

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	1

Bits	Access Name		Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	media1axi_port4_pri 7 is the highest priority.	MEDIA1 AXI bus port M4 (GZIP) priority.
[11]	RO	reserved	reserve.
[10:8]	RW	media1axi_port3_pri 7 is the highest priority.	MEDIA1 AXI bus port M3(IVE) priority.
[7]	RO	reserved	reserve.
[6:4]	RW	media1axi_port2_pri 7 is the highest priority.	MEDIA1 AXI bus port M2(JPGE) priority.
[3]	RO	reserved	reserve.
[2:0]	RW	media1axi_port1_pri 7 is the highest priority.	MEDIA1 AXI bus port M1 (TDE) priority.

MISC_CTRL21

MISC_CTRL21 is DDR QOS control register 0.

Offset Address	Register Name	Total Reset Value
0x0054	MISC_CTRL21	0x0004_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep4																				gzip_qosmap				reserved				pcie_qosmap		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved_keep4	Reserved.
[11:8]	RW	gzip_qosmap	The QOS value of GZIP in MDDRC.
[7:4]	RO	reserved	reserve.
[3:0]	RW	pcie_qosmap	The QOS value of PCIE in MDDRC.

MISC_CTRL22

MISC_CTRL22 is DDR QOS control register 1.

Offset Address	Register Name	Total Reset Value
0x0058	MISC_CTRL22	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hash_qosmap				ive_qosmap				aio_qosmap				jpge_qosmap								tde_ddrt_qosmap				vicap0_qosmap				vdp_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	hash_qosmap	The QOS value of HASH in MDDRC.
[23:20]	RW	ive_qosmap	IVE QOS value in MDDRC.
[19:16]	RW	aio_qosmap	AIAO's QOS value in MDDRC.
[15:12]	RW	jpge_qosmap	The QOS value of JPGE in MDDRC.
[11:8]	RW	tde_ddrt_qosmap	TDE QOS value in MDDRC.
[7:4]	RW	vicap0_qosmap	VICAP QOS value in MDDRC.
[3:0]	RW	vdp_qosmap	The QOS value of VDP in MDDRC.

MISC_CTRL23

MISC_CTRL23 is DDR QOS control register 2.

Offset Address	Register Name	Total Reset Value
0x005C	MISC_CTRL23	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emmc_qosmap				reserved				fmc_qosmap				sdio1_qosmap				sdio0_qosmap				cpu_qosmap				vpss0_qosmap				vgs_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	emmc_qosmap	QOS value of EMMC in MDDRC.
[27:24]	RO	reserved	reserve.
[23:20]	RW	fmc_qosmap	The QOS value of FMC in MDDRC.
[19:16]	RW	sdio1_qosmap	The QOS value of SDIO1 in MDDRC.
[15:12]	RW	sdio0_qosmap	The QOS value of SDIO0 in MDDRC.
[11:8]	RW	cpu_qosmap	The QOS value of CPU in MDDRC.
[7:4]	RW	vpss0_qosmap	QOS value of VPSS in MDDRC.
[3:0]	RW	vgs_qosmap	The QOS value of VGS in MDDRC.

MISC_CTRL24

MISC_CTRL24 is DDR QOS control register 3.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gdc_qosmap				usb3_qosmap				vedu_qosmap				usb2_qosmap				cipher_qosmap				dma2_qosmap				dma1_qosmap				gsf_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	gdc_qosmap	The QOS value of GDC in MDDRC.
[27:24]	RW	usb3_qosmap	The QOS value of USB3.0 in MDDRC.
[23:20]	RW	vedu_qosmap	QOS value of VEDU in MDDRC.
[19:16]	RW	usb2_qosmap	QOS value of USB2 in MDDRC.
[15:12]	RW	cipher_qosmap	CIPHER's QOS value in MDDRC.
[11:8]	RW	dma2_qosmap	DMA2 QOS value in MDDRC.
[7:4]	RW	dma1_qosmap	DMA1 QOS value in MDDRC.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gdc_qosmap				usb3_qosmap				vedu_qosmap				usb2_qosmap				cipher_qosmap				dma2_qosmap				dma1_qosmap				gsf_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[3:0]	RW	gsf_qosmap	The QOS value of GSF in MDDRC.

MISC_CTRL29

MISC_CTRL29 is the USB3.0 control register.

Offset Address	Register Name	Total Reset Value
0x0074	MISC_CTRL29	0x0004_0FD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		usb3_fladj_30mhz_reg						usb3_bus_filter_bypass							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0	1	0	0

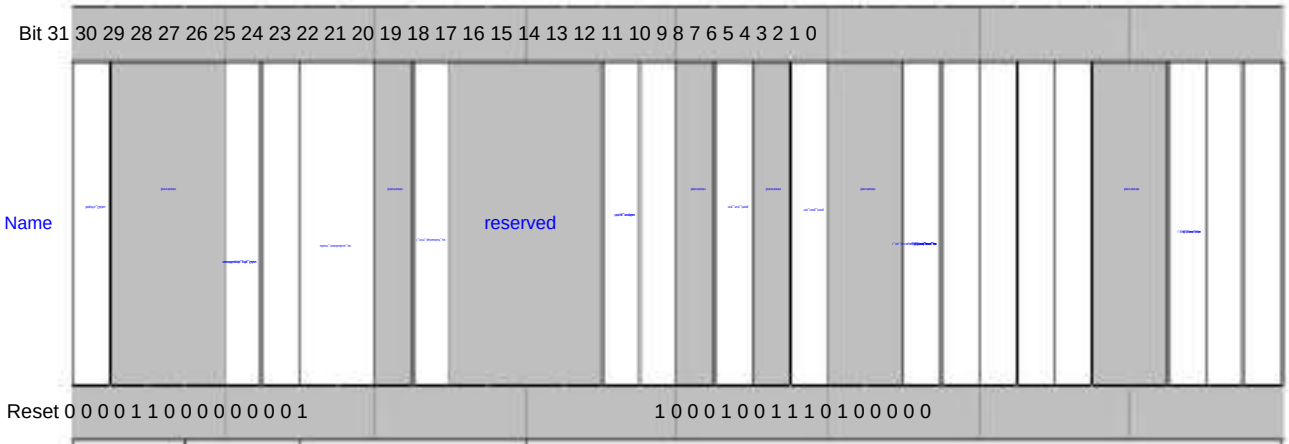
Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RW	usb3_host_port_po wer; wer_control_present	Indicates whether the USB3.0 port has power control. 0: The port has no power control switch, and the USB device always supplies power. 1: The port has a power control switch to control the power supply of the USB device.

[18:13] RW		usb3_fladj_30mhz_ reg	HS clock jitter control. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 µs duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro frame is counted for 123933ns. The value needs to be programmed in terms of high speed bit times in a 30 MHz cycle.
[12] RW		usb3_host_msi_ena	Control whether the USB3.0 port interrupt signal is pulse type or level type. 0: level type; ble 1: Pulse type.
[11:8] RW		usb3_bus_filter_bypass	USB 3.0 bus filter bypass. This register must be set to 4'b1111.
[7] RW		usb3_port_ovrcur_ pol	USB3.0 port overcurrent protection polarity control. 0: active low; pol 1: Active high.
[6] RW		usb3_port_pwren_p ol	USB3.0 port power enable polarity control. 0: active low; ol 1: Active high.
[5] RW		usb3_port_ovrcur_ ctrl_en	USB3.0 port overcurrent protection is enabled. 0: USB3.0 port overcurrent protection is disabled; 1: USB3.0 port overcurrent protection is enabled.
[4] RW		usb3_port_pwr_en	USB3.0 port power supply enable. 0: USB3.0 port power control is disabled; 1: USB3.0 port power supply enable is output by USB3.0 controller.
[3] RW		usb3_host_u3_disable	The USB3.0(SS) port is turned off. 0: USB3.0 port enable. 1: USB3.0 port is disabled.
[2] RW		usb3_host_u2_disable	The USB2.0(HS) port is turned off. 0: USB2.0 port enable. 1: USB2.0 port is disabled.
[1:0] RW		usb3_hub_port_perm_attach	Indicates whether the downstream port device is always on. 0: USB 3.0 port devices are not permanently attached; 1: The USB 3.0 port device is permanently attached.

MISC_CTRL30

MISC_CTRL30 is USB2.0 control register 0.

Offset Address	Register Name	Total Reset Value
0x0078	MISC_CTRL30	0x0C03_13A0



Bits	Access	Name	Description
[31]	RW	usb2_chipid	USB2.0 HOST and DEV switching control signal. 0ÿHOSTÿ 1ÿDEVÿ
[30:28]	RO	reserved	reserve.
[27]	RW	control. usb2_phy_dmpulldown	D- Pull-down resistor enable 0: disable; 1: enable.
[26]	RW	control. usb2_phy_dppulldown	D+ pull-down resistor enable 0: disable; 1: enable.
[25:24]	RW	mode; It is	Scale-Down mode. 00: disable all scale-down, the actual timing value will be used; 01: enable scale-down all timing ss_scaledown_mod except suspend and resume in Device 10: Only enable the timing of scale-down suspend and resume in Device mode; 11: Enable bit0 and bit1 scale-down timing values.
[23]	RO	reserved	reserve.
[22]	RW	ss_hubsetup_min_i	Set the idle period after the leading packet at full speed. 0: There are 5 full-speed idle cycles after the full-speed leading packet; 1: There are 4 full-speed idle cycles after the full-speed preamble.
[21:18]	RO	reserved	reserve.

[17] RW usbovr_p_ctrl			Polarity control for overcurrent protection. 0: Low level active; 1: Active high.
[16] RW usbpwr_pctrl			USB PHY power shutdown polarity control. 0: Low level active; 1: Active high.
[15] RO		reserved	reserve.
[14] RW port_ovr_en			USB PHY overcurrent protection shutdown control. 0: close the overcurrent protection; 1: Enable overcurrent protection.
[13] RO		reserved	reserve.
[12] RW port_pwr_en			USB PHY power off. 0: Turn off the power; 1: Enable the power output of the controller.
[11:10] RO		reserved	reserve.
[9] RW ss_ena_incr16_i			AHB burst16 enable signal. 0: disable; 1: Enabled (default).
[8] RW ss_ena_incr8_i			AHB burst8 enable signal. 0: disable; 1: Enabled (default).
[7] RW ss_ena_incr4_i			AHB burst4 enable signal. 0: disable; 1: Enabled (default).
[6] RW ss_ena_incr_align_i			burst alignment enable signal. 0: disable (default); 1: enable.
[5] RW		when over-current occurs. disable; rcur_en_i	Automatically shut down the port power supply ss_autoppd_on_ove 0: 1: Enabled (default).
[4:3] RO		reserved	reserve.
[2] RW app_start_clk_i			OHCI clock control signal. 0: OHCI works normally (default); 1: Turn on OHCI clock in Suspend mode.

[1] RW	ohci_susp_lgcy_i		OHCI suspend strap input signal.
[0] RW	ss_word_if_i		UTMI interface data width selection signal. 0: 8bit (default); 1ÿ16bitÿ

MISC_CTRL31

MISC_CTRL31 is the TEST clock & USB2.0PHY access test path selection register.

Offset Address	Register Name	Total Reset Value
0x007C	MISC_CTRL31	0x3323_8A00

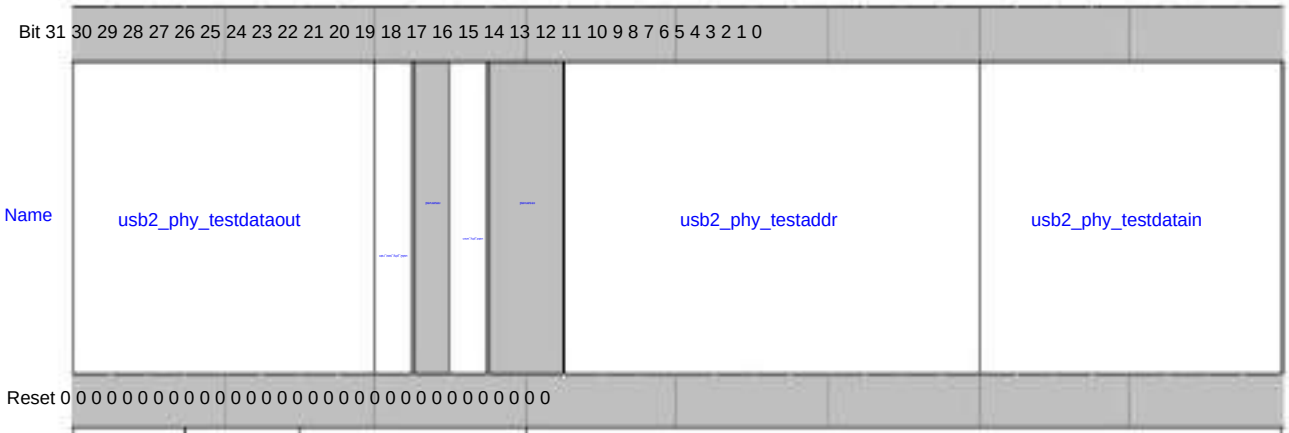
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved_keep7	test_clk_sel
Reset	0 0 1 1 0 0 1 1 0 0 1 0 0 0 1	1 1 0 0 0 1 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved_keep7	Reserved.
[3:0]	RW	test_clk_sel	Test clock selection. 0x0ÿpll_test_out[0]ÿ 0x1ÿpll_test_out[1]ÿ 0x2ÿpll_test_out[2]ÿ 0x3ÿpll_test_out[3]ÿ 0x4ÿpll_test_out[4]ÿ 0x5ÿclk_test_out[0]ÿ 0x6ÿclk_test_out[1]ÿ 0x7ÿclk_test_out[2]ÿ 0x8ÿclk_24mÿ 0x9ÿclk_rtc_outÿ 0xAÿrtc_isoÿ 0xB: audio_codec_mclk; others: reserved.

MISC_CTRL32

MISC_CTRL32 is the USB2.0PHY test channel register.

Offset Address	Register Name	Total Reset Value
0x0080	MISC_CTRL32	0x0000_0000



Bits	Access	Name	Description
[31:24]	RO	usb2_phy_testdatao	USB2.0 PHY read test data bus. out
[23]	RW	usb2_phy_test_rstn	USB2.0 PHY read test interface reset. 0: reset; 1: Do not reset.
[22]	RO	reserved	reserve.
[21]	RW	usb2_phy_wren	USB2.0 PHY test interface register read and write control signal, changing from 0 to 1 means writing, and 0 means reading.
[20:19]	RO	reserved	reserve.
[18:8]	RW	usb2_phy_testaddr	USB2.0 PHY test interface register address.
[7:0]	RW	usb2_phy_testdatain	USB2.0 PHY write test data bus.

MISC_CTRL33

MISC_CTRL33 is the COMB PHY test channel register.

Offset Address	Register Name	Total Reset Value
0x0084	MISC_CTRL33	0x0000_0000

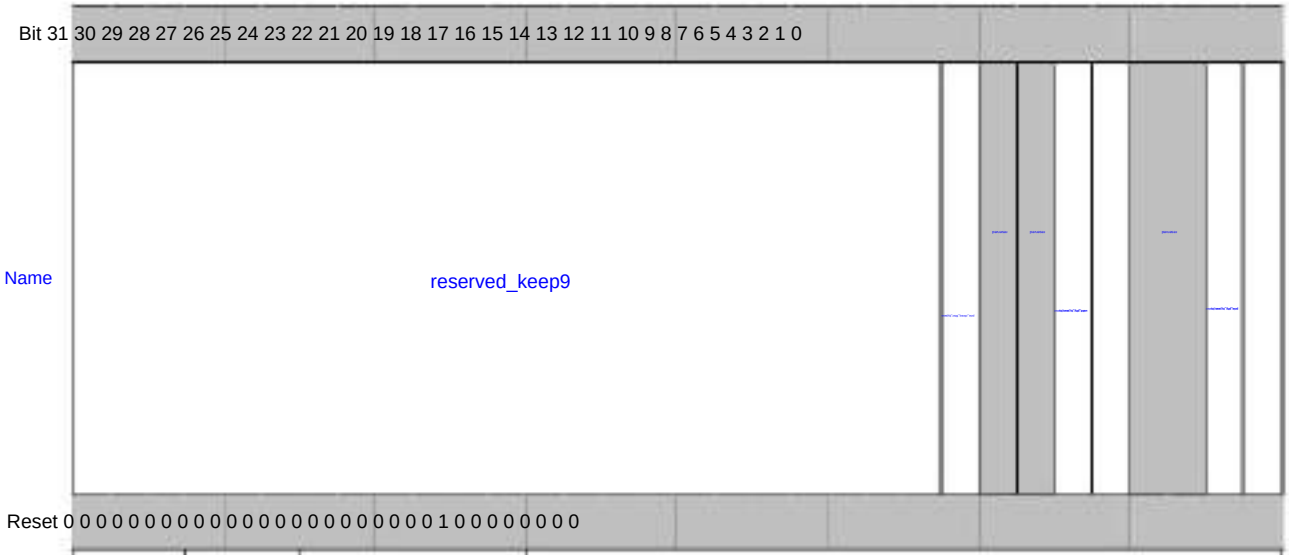
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep8																								comb_phy_test_ad				comb_phy_test _O				comb_phy_test dr		_i	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved_keep8	Reserved.
[16]	RW	comb_phy_test_ control. enable; te	COMB PHY test register read and write wri 0: read 1: Write enable.
[15:13]	RO	reserved	reserve.
[12:8]	RW	comb_phy_test_ad	COMB PHY test register address. dr
[7:4]	RO	comb_phy_test_o	COMB PHY test register read data.
[3:0]	RW	comb_phy_test_i	COMB PHY test register write data.

MISC_CTRL34

MISC_CTRL34 is the PCIe&USB3.0 PHY control register.

Offset Address	Register Name	Total Reset Value
0x0088	MISC_CTRL34	0x0000_0100

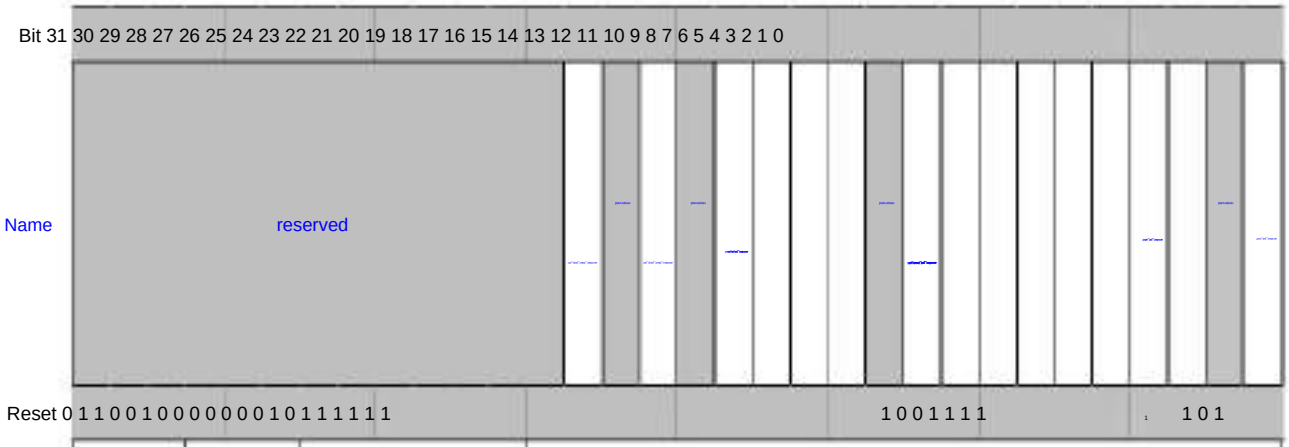


Bits	Access	Name	Description
[31:9]	RO	reserved_keep9	Reserved.
[8]	RW	pcie_clkreq_filter_ control. enable; bypass	pcie_clk_req Input filter processing 0: 1: Off.
[7]	RO	reserved	reserve.
[6]	RO	reserved	reserve.
[5]	RW	usb3_phy_rx_stand 0:	Controls whether the USB3.0 PHY RX is active. PHY RX active status; by 1: PHY RX standby state.
[4]	RW	usb3_phy_bypass_ 0: codec	USB3.0 PHY BYPASS_CODEC control. 8b/10b codec function is executed normally. 1: 8b/10b codec is bypassed.
[3:2]	RO	reserved	reserve.
[1]	RW	pcie_phy_rx_stand 0:	Controls whether the PCIe PHY RX is active in P0/P0s mode. PHY RX active status; by 1: PHY RX standby state.
[0]	RW	pcie_phy_bypass_c 0: normally. odec	PCIE PHY BYPASS_CODEC control. 8b/10b codec function is executed 1: 8b/10b codec is bypassed.

MISC_CTRL45

MISC_CTRL45 is Audio Codec ANA register 0 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B4	MISC_CTRL45	0x6405_FCFD



Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RW	acodec_dacl_pop_en	The left channel POP circuit is enabled. 0: The function of removing POP sound is off; 1: Enable the function of removing POP sound. Note: acodec_dacl_pop_en is only configured as 1 as required during power-on and power-off suppression of the POP process, and acodec_dacl_pop_en must be configured as 0 during the normal operation of the DAC channel.
[17]	RO	reserved	reserve.
[16]	RW	acodec_dacr_pop_en	The right channel POP circuit is enabled. 0: The function of removing POP sound is off; 1: Enable the function of removing POP sound. Note: acodec_dacr_pop_en is only configured as 1 as required during the process of power-on and power-off to suppress the POP process, and acodec_dacr_pop_en must be configured as 0 during the normal operation of the DAC channel.
[15]	RO	reserved	reserve.
[14]	RW	acodec_mute_dacr	Right channel DAC mute control. 0: Right channel DAC works normally; 1: Right channel DAC mute.
[13]	RW	acodec_mute_dacl	Left channel DAC mute control. 0: left channel DAC works normally; 1: left channel DAC mute.

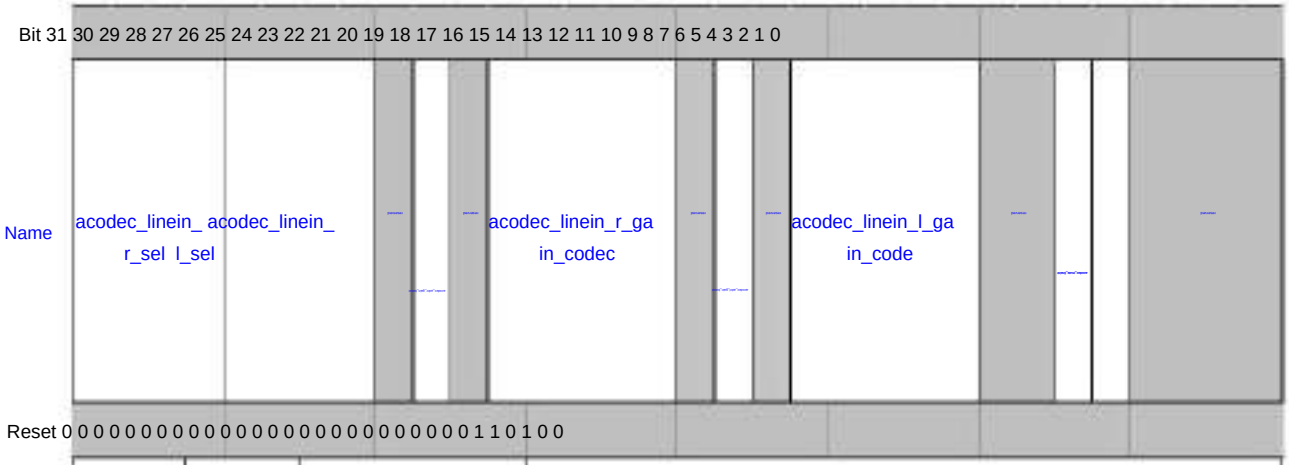
[12] RW	acodec_pd_dacr		Right channel DAC power down control signal. 0: DACR simulation works normally; 1: DACR simulates power down.
[11] RW	acodec_pd_dacl		Left channel DAC power down control signal. 0: DACL simulation works normally; 1: DACL simulates power down.
[10] RO		reserved	reserve.
[9] RW		signal. acodec_pd_dacr_df	Right channel DACR D flip-flop power-down control 0: DACR D flip-flop works normally; f 1: DACR D trigger power down.
[8] RW		signal. acodec_pd_dacl_df	Left channel DACLD flip-flop power-down control 0: DACL D flip-flop works normally; f 1: DACL D trigger power down.
[7] RW		signal. 2 acodec_pd_micbias	MICBIAS2 power down control 0: MICBIAS works normally; 1ÿMICBIAS power downÿ
[6] RW		signal. 1 acodec_pd_micbias	MICBIAS1 power down control 0: MICBIAS works normally; 1ÿMICBIAS power downÿ
[5] RW	acodec_pd_linein_r		LINEIN_R Power-down control signal. 0: Linein works normally; 1ÿLinein power downÿ
[4] RW	acodec_pd_linein_l		LINEIN_L Power-down control signal. 0: Linein works normally; 1ÿLinein power downÿ
[3] RW	acodec_pd_adcr		Right channel ADC power down control signal. 0: ADCR digital analog works normally; 1: ADCR digital analog power down.
[2] RW	acodec_pd_adcl		Left channel ADC power down control signal. 0: ADCL digital analog works normally; 1: ADCL digital analog power down.
[1] RW	reserved		To work properly, it needs to be configured as 1.

[0] RW	acodec_pd_vref		Reference voltage power-down control signal. 0: The reference voltage works normally; 1: Reference voltage power down.

MISC_CTRL46

MISC_CTRL46 is Audio Codec ANA register 1 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B8	MISC_CTRL46	0x0000_0034



Bits	Access	Name	Description
[31:28]	RW	acodec_linein_r_sel	LINEIN Right channel input signal selection. 0x0: IN0R (positive terminal)/IN0L (negative terminal)/differential input; 0x1: IN0R single-ended input; 0x2: IN0R (positive terminal)/IN1R (negative terminal) differential input; 0x3: IN1R single-ended input; 0x4: IN1R (positive terminal) / IN1L (negative terminal) differential input; Other: reserved.
[27:24]	RW	acodec_linein_l_sel	LINEIN Left channel input signal selection. 0x0: IN0L (positive terminal) / IN0R (negative terminal) differential input; 0x1: IN0L single-ended input; 0x2: IN0L (positive terminal) / IN1L (negative terminal) differential input; 0x3: IN1L single-ended input; 0x4: IN1L (positive terminal) / IN1R (negative terminal) differential input; Other: reserved.
[23]	RO	reserved	reserve.

[22] RW		acodec_adcr_gain_0:	ADCR gain boost control. 0db gain; boost 1: 20db gain.
[21] RO		reserved	reserve.
[20:16] RW		acodec_linein_r_gain_codec	LINEINR Input gain control. 0x00ÿ0dbÿ 0x01ÿ2dbÿ 0x02ÿ4dbÿ 0x03ÿ6dbÿ 0x04ÿ8dbÿ 0x05ÿ10dbÿ 0x06ÿ12dbÿ 0x07ÿ14dbÿ 0x08ÿ16dbÿ 0x09ÿ18dbÿ 0x0Aÿ20dbÿ 0x0Bÿ22dbÿ 0x0Cÿ24dbÿ 0x0Dÿ26dbÿ 0x0Eÿ28dbÿ 0x0Fÿ30dbÿ 0x10ÿ-1.5dbÿ Other: reserved.
[15] RO		reserved	reserve.
[14] RW		acodec_adcl_gain_0:	ADCL gain boost control. 0db gain; boost 1: 20db gain.
[13] RO		reserved	reserve.
[12:8] RW		acodec_linein_l_gain_code	LINEINL Input gain control. 0x00ÿ0dbÿ 0x01ÿ2dbÿ 0x02ÿ4dbÿ 0x03ÿ6dbÿ 0x04ÿ8dbÿ 0x05ÿ10dbÿ 0x06ÿ12dbÿ

			0x07ÿ14dbÿ 0x08ÿ16dbÿ 0x09ÿ18dbÿ 0x0Aÿ20dbÿ 0x0Bÿ22dbÿ 0x0Cÿ24dbÿ 0x0Dÿ26dbÿ 0x0Eÿ28dbÿ 0x0Fÿ30dbÿ 0x10ÿ-1.5dbÿ Other: reserved.
[7:6] RO		reserved	reserve.
[5] RW		acodec_mute_linein 0: r	Right channel LINEINR mute control. the right channel LINEINR works normally; 1: Right channel LINEINRmute.
[4] RW		acodec_mute_linein 0: l	Left channel LINEINL mute control. the left channel LINEINL works normally; 1: left channel LINEINL mute.
[3:0] RO		reserved	reserve.

MISC_CTRL47

MISC_CTRL47 is Audio Codec ANA register 2 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00BC	MISC_CTRL47	0x4018_008D

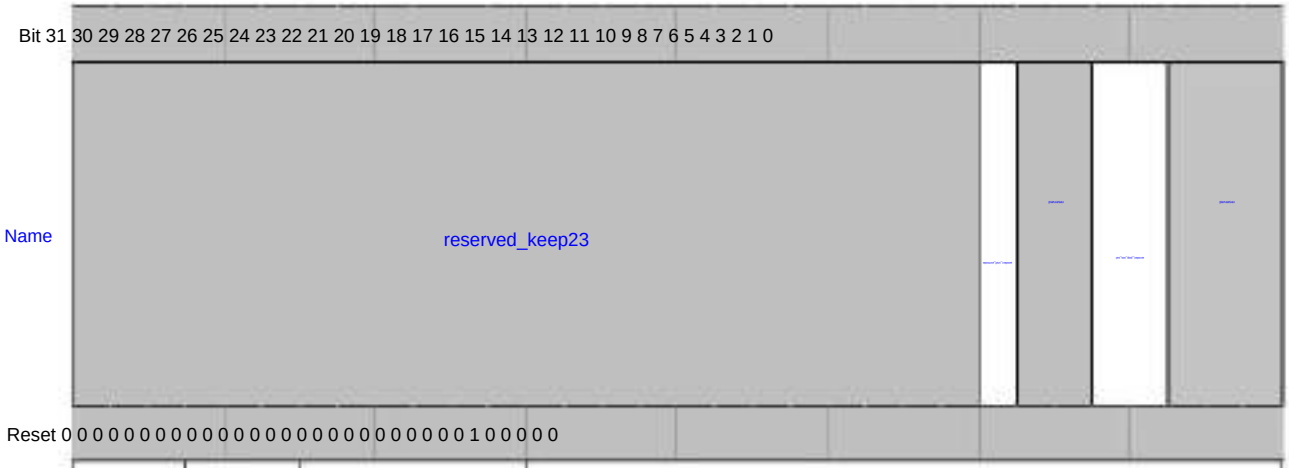
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																		reserved														
Reset	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	reserved	For normal operation, configure to 0.
[29:24]	RO	reserved	reserve.
[23]	RW	acodec_rst	Analog partial reset signal. 0: cancel reset; 1: Reset.
[22:0]	RO	reserved	reserve.

MISC_CTRL48

MISC_CTRL48 is Audio Codec ANA register 3 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00C0	MISC_CTRL48	0x0000_0020

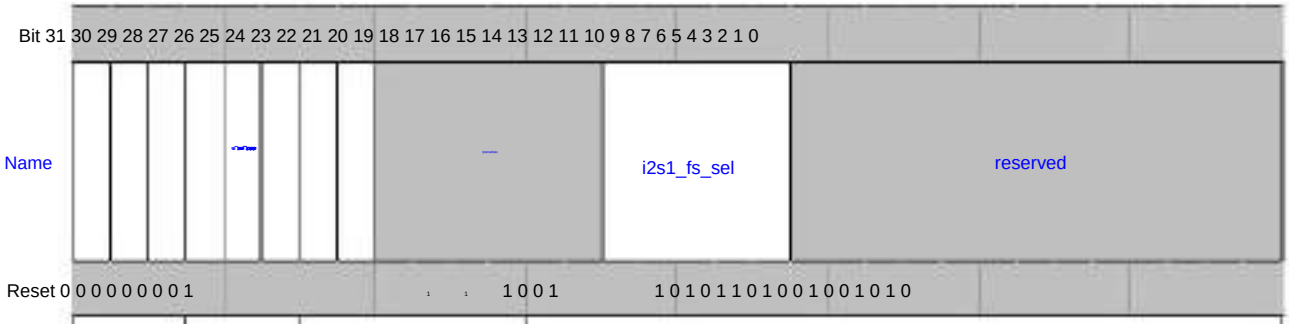


Bits	Access	Name	Description
[31:8]	RO	reserved_keep23	Reserved.
[7]	RW	acodec_vref_exmode	When VREF PD. 0: with pulldown, normal PD; 1: No pull-down, VREF can be added.
[6:5]	RO	reserved	reserve.
[4:3]	RW	acodec_pop_res_sel	Spacer resistor between popfree circuit and main output. 00ÿ100ÿÿ 01ÿ1Kÿÿ 10ÿ10Kÿÿ 11ÿ100Kÿÿ
[2:0]	RO	reserved	reserve.

MISC_CTRL51

MISC_CTRL51 is Audio Codec DIG control register 0 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00CC	MISC_CTRL51	0x00F3_5A4A



Bits	Access	Name	Description
[31]	RW	dacl_rst_n	DACL reset signal. 0: reset is valid; 1: Reset is invalid.
[30]	RW	dacr_rst_n	DACR reset signal. 0: reset is valid; 1: Reset is invalid.
[29]	RW	adcl_rst_n	ADCL reset signal. 0: reset is valid; 1: Reset is invalid.
[28]	RW	adcr_rst_n	ADCR reset signal. 0: reset is valid; 1: Reset is invalid.
[27]	RW	dacl_en	DACL enable signal. 0: disable; 1: enable.
[26]	RW	dacr_en	DACR enable signal. 0: disable; 1: enable.
[25]	RW	adcl_en	ADCL enable signal. 0: disable; 1: enable.
[24]	RW	adcr_en	ADCR enable signal. 0: disable; 1: enable.
[23:18]	RO	reserved	reserve.

[17:13]	RW	i2s1_fs_sel	I2S channel sampling rate selection. 11000ÿmclk/512/2ÿ 11001ÿmclk/256/2ÿ 11010ÿmclk/128/2ÿ 11011ÿmclk/64/2ÿ 111xxÿmclk/32/2ÿ
[12:0]	RO	reserved	reserve.

MISC_CTRL52

MISC_CTRL52 is Audio Codec DIG control register 1 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D0	MISC_CTRL52	0x0000_0001

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31]	RW	smutel	DACL soft-mute control bit. 0: Disable soft-mute; 1: Enable soft-mute.
[30]	RW	smuter	DACR soft-mute control bit. 0: Disable soft-mute; 1: Enable soft-mute.
[29]	RW	sunmutel	DACL soft-unmute control bit. 0: Disable soft-unmute; 1: Enable soft-unmute.
[28]	RW	sunmuter	DACR soft-unmute control bit. 0: Disable soft-unmute; 1: Enable soft-unmute.

[27] RW	dacvu		DAC volume update control bit. 0: Do not update the volume; 1: Update volume.
[26:25] RW	mutel_rate		DACL soft-mute rate control bit. 00ÿfs/2ÿ 01ÿfs/8ÿ 10ÿfs/32ÿ 11ÿfs/64ÿ
[24:23] RW	play_rate		DACR soft-mute rate control bit. 00ÿfs/2ÿ 01ÿfs/8ÿ 10ÿfs/32ÿ 11ÿfs/64ÿ
[22:0] RO		reserved	reserve.

MISC_CTRL53

MISC_CTRL53 is Audio Codec DIG control register 2 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D4	MISC_CTRL53	0x0606_2424

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	tackle_vol										-	-	dacr_vol								reserved									
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

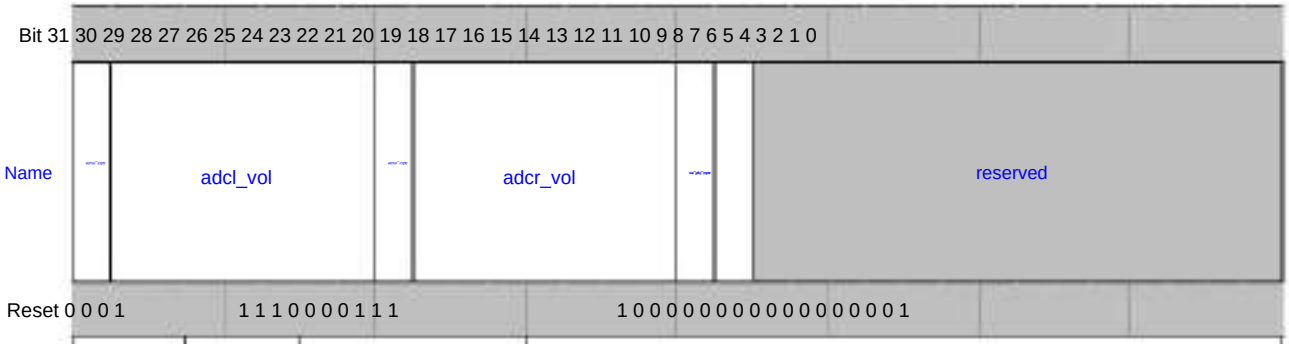
Bits	Access	Name	Description
[31]	RW	dacl_mute	DACL Digital Mute Control. 0: normal work; 1: Mute.

[30:24] RW	tackle_vol		DACL Digital volume control. The calculation formula is: (6- dacl_vol*1)db. When dacl_vol is 0x7F, DACL digits are muted. 0x00ÿ6dB 0x01ÿ5dB 0x02ÿ 4dB … 0x7Eÿ -120dB 0x7Fÿ mute
[23] RW	dacr_mute		DACR Digital Mute Control. 0: normal work; 1: Mute.
[22:16] RW	dacr_vol		DACR Digital volume control. The calculation formula is: (6- dacr_vol*1)db. When dacr_vol is 0x7F, DACR digits are muted. 0x00ÿ6dB 0x01ÿ5dB 0x02ÿ4dB … 0x7Eÿ-120dB 0x7Fÿmute
[15:0] RO		reserved	reserve.

MISC_CTRL54

MISC_CTRL54 is Audio Codec DIG control register 3 (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D8	MISC_CTRL54	0x1E1E_0001



Bits	Access	Name	Description
[31]	RW	adcl_mute	ADCL Digital mute control bit. 0ÿADCL unmuteÿ 1ÿADCL muteÿ
[30:24]	RW	adcl_vol	ADCL volume control bit calculation formula: (30-adcl_vol*1)db. 0x00ÿ30dB 0x01ÿ29dB 0x02ÿ28dB … 0x7Eÿ-96dB 0x7Fÿ-97dB
[23]	RW	adcr_mute	ADCR Digital mute control bit. 0: ADCR is not muted; 1: ADCR muted.
[22:16]	RW	adcr_vol	ADCR volume control bit. Calculation formula: (30-adcr_vol*1)db. 0x00ÿ30dB 0x01ÿ29dB 0x02ÿ28dB … 0x7Eÿ-96dB 0x7Fÿ-97dB
[15]	RW	adcl_hpf_en	ADCL high-pass filter enable control. 0: Turn off the high-pass filter; 1: High-pass filter enabled.

[14] RW	adcr_hpf_en		ADCR high pass filter enable control. 0: Turn off the high-pass filter; 1: High-pass filter enabled.
[13:0] RO		reserved	reserve.

MISC_CTRL56

MISC_CTRL56 selects the control register for the I2S channel (will not be soft reset).

Offset Address	Register Name	Total Reset Value
0x00E0	MISC_CTRL56	0x0000_0000

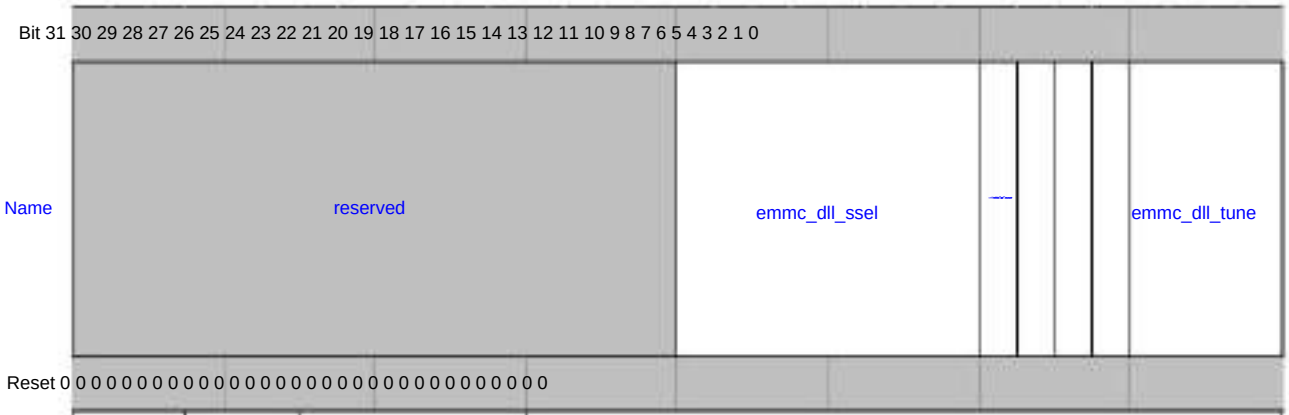
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	reserve.
[1]	RW	i2s_pad_enable	Enable control of chip I2S interface and AIAO channel. 0: Close the channel between the chip I2S interface and AIAO, and the chip I2S interface has no output; 1: Open the channel between the I2S interface of the chip and AIAO, and connect the I2S interface of the chip with the I2S of AIAO. Note: i2s_pad_enable and audio_enable can only be configured as 1 at the same time, and cannot be configured as 1 at the same time.
[0]	RW	audio_enable	Enable control of I2S interface of audicodec and AIAO channel inside the chip. 0: Close the I2S interface of the audicodec inside the chip and the channel of AIAO, and the i2s interface of the audicodec inside the chip has no output; 1: Open the I2S interface of the audicodec inside the chip and the channel of AIAO, and connect the I2S interface of the audicodec inside the chip to the I2S of AIAO. Note: i2s_pad_enable and audio_enable can only be configured as 1 at the same time, and cannot be configured as 1 at the same time.

MISC_CTRL80

MISC_CTRL80 is eMMC interface DLL control register 0.

Offset Address	Register Name	Total Reset Value
0x0140	MISC_CTRL80	0x0000_0000



Bits	Access Name	Description
[31:16]	RO reserved	reserve.
[15:8]	RW emmc_dll_ssel	eMMC port DLL ssel signal. DLL SLAVE LINE delay Initial level selection.
[7]	RW emmc_dll_mode	eMMC port DLL mode signal. 0: normal mode; 1: SLAVE LINE is controlled by dll_dllssel.
[6]	RW emmc_dll_stop	eMMC port DLL stop signal. 0: enable clock detection; 1: Disable clock detection.
[5]	RW emmc_dll_bypass	eMMC port DLL bypass signal. 0: Normal mode, the phase shift of the output clock relative to the input clock is 90°; 1: slave line bypass, the phase shift of the output clock is not.
[4]	RW emmc_dll_slave_en	eMMC port DLL slave_en signal. 0: slave stops working; 1: slave starts working

[3:0]	RW	emmc_dll_tune	eMMC port DLL tune signal. 0x0: no calibration; 0x1: increase 1 level of delay; 0x2: increase 2 levels of delay; 0x3: increase 3 levels of delay; ... 0x7: Add 7 levels of delay; 0x8: No calibration; 0x9: reduce the delay by 1 level; 0xA: reduce the delay by 2 levels; 0xB: reduce the delay by 3 levels; ... 0xF: Decrease 7 levels of delay.

MISC_CTRL81

MISC_CTRL81 is eMMC interface DLL control register 1.

Offset Address	Register Name	Total Reset Value
0x0144	MISC_CTRL81	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	emmc_dll_mdly_tap
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

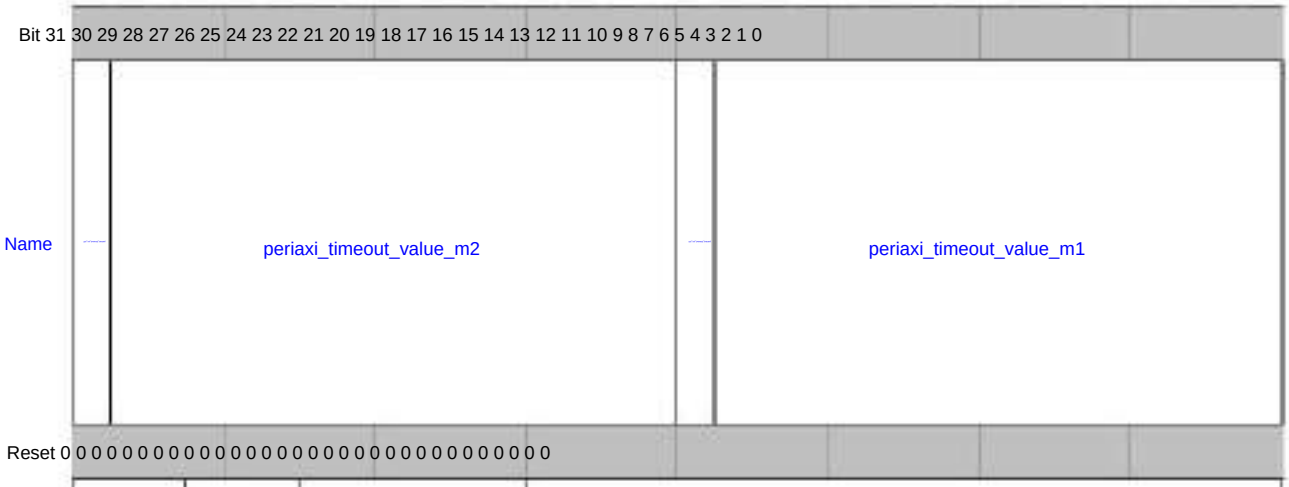
Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10]	RO	emmc_dll_lock	eMMC port DLL lock signal. 0ÿDLL MASTER unlockÿ 1ÿDLL MASTER lockedÿ
[9]	RO	emmc_dll_ready	eMMC port DLL ready signal. 0ÿDLL SLAVE not readyÿ 1ÿDLL SLAVE readyÿ

[8]	RO	emmc_dll_overflo In	eMMC port DLL overflow signal. 0ÿDLL MASTER unoverflowÿ 1ÿDLL MASTER overflowÿ
[7:0] RO		emmc_dll_mdly_ta	eMMC port DLL mdly_tap signal. DLL MASTER LINE tap value. p

MISC_CTRL85

MISC_CTRL85 is PERI bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0154	MISC_CTRL85	0x0000_0000

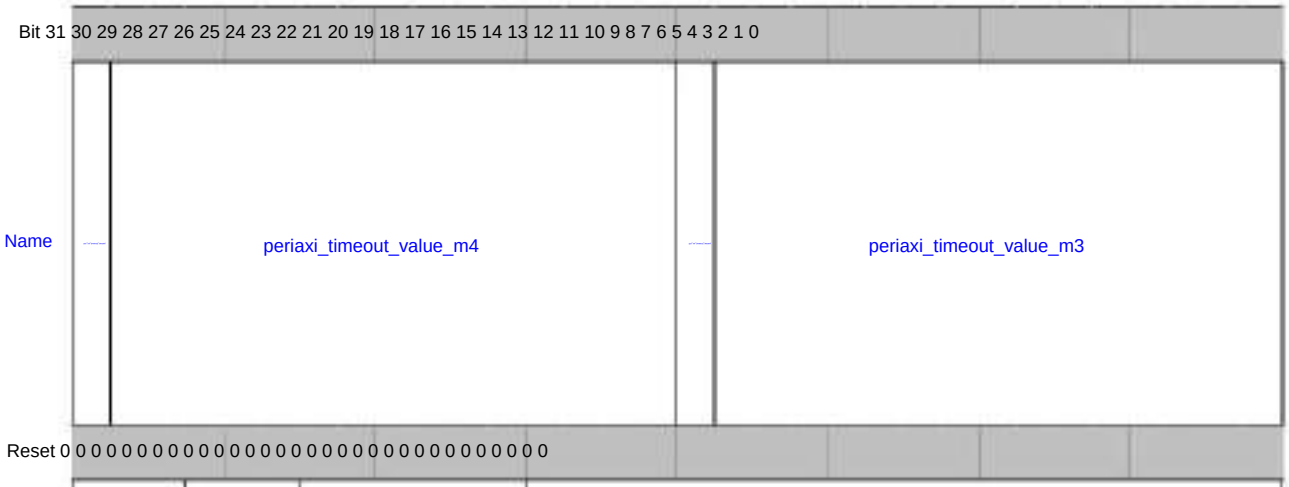


Bits	Access	Name	Description
[31]	RW	periaxi_timeout_en_m2	Timeout count enable for PERI AXI bus port M2 (SYSAXI_S2). 0: disable; 1: enable.
[30:16]	RW	periaxi_timeout_value_m2	The timeout count value of PERI AXI bus port M2 (SYSAXI_S2). count value=periaxi_timeout_value_m2×2.
[15]	RW	periaxi_timeout_en_m1	Timeout count enable for PERI AXI bus port M1 (CCI_M0). 0: disable; 1: enable.
[14:0]	RW	periaxi_timeout_value_m1	The timeout count value of PERI AXI bus port M1 (CCI_M0). count value=periaxi_timeout_value_m1×2.

MISC_CTRL86

MISC_CTRL86 is PERI bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0158	MISC_CTRL86	0x0000_0000

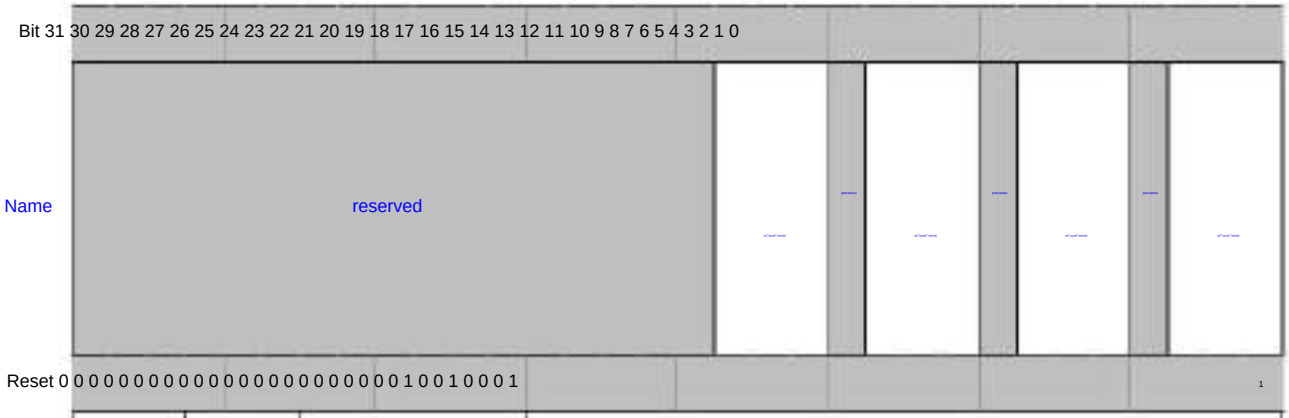


Bits	Access	Name	Description
[31]	RW	periaxi_timeout_en_m4	Timeout count enable for PERI AXI bus port M4(j2c). 0: disable; 1: enable.
[30:16]	RW	periaxi_timeout_value_m4	Timeout count value of PERI AXI bus port M4(j2c). count value = periaxi_timeout_value_m4×2.
[15]	RW	periaxi_timeout_en_m3	The timeout count of PERI AXI bus port M3 (debug_axi) is enabled. 0: disable; 1: enable.
[14:0]	RW	periaxi_timeout_value_m3	The timeout count value of PERI AXI bus port M3 (debug_axi). count value=periaxi_timeout_value_m3×2.

MISC_CTRL88

MISC_CTRL88 is PERI bus priority control register 0.

Offset Address	Register Name	Total Reset Value
0x0160	MISC_CTRL88	0x0000_0123

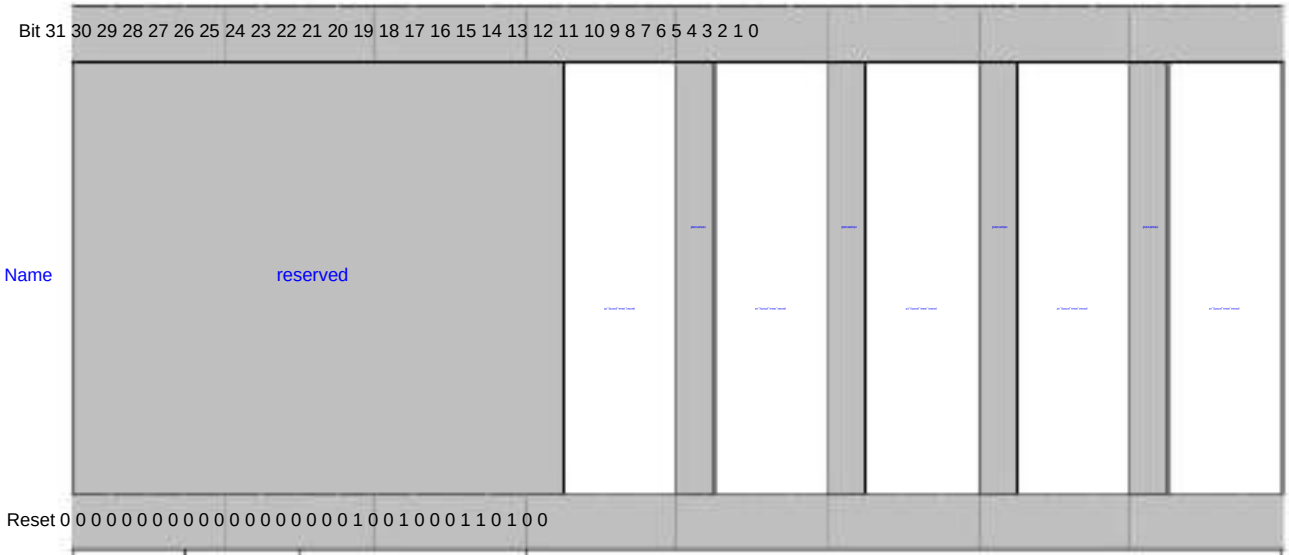


Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	periaxi_port4_pri	PERI AXI bus port M4(j2c) priority. 3 is the highest priority.
[11]	RO	reserved	reserve.
[10:8]	RW	periaxi_port3_pri	PERI AXI bus port M3 (debug_axi) priority. 3 is the highest priority.
[7]	RO	reserved	reserve.
[6:4]	RW	periax_port2_pri	PERI AXI bus port M2 (SYSAXI_S2) priority. 3 is the highest priority.
[3]	RO	reserved	reserve.
[2:0]	RW	periax_port1_pri	PERI AXI bus port M1 (CCI_M0) priority. 3 is the highest priority.

MISC_CTRL89

MISC_CTRL89 is PERI bus priority control register 1.

Offset Address	Register Name	Total Reset Value
0x0164	MISC_CTRL89	0x0000_1234

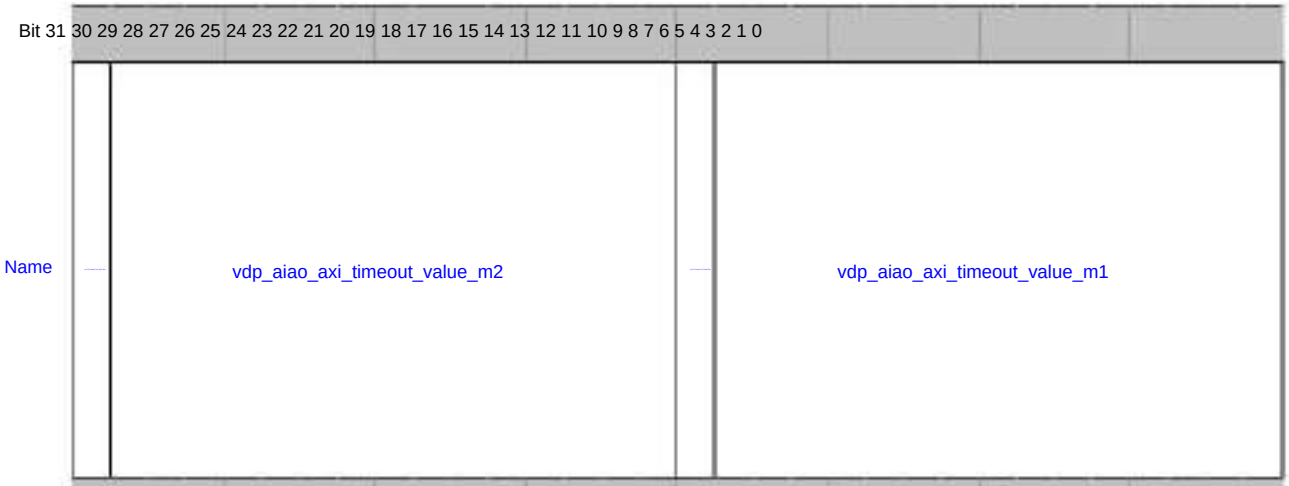


Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:16]	RW	periaxi_slave_priority_s5	PERI AXI S5 (pcie_slave) port bus access priority. 7 is the highest priority.
[15]	RO	reserved	reserve.
[14:12]	RW	periaxi_slave_priority_s4	PERI AXI S4(GIC) port bus access priority. 7 is the highest priority.
[11]	RO	reserved	reserve.
[10:8]	RW	periaxi_slave_priority_s3	PERI AXI S3 (ahb_cfg) port bus access priority. 7 is the highest priority.
[7]	RO	reserved	reserve.
[6:4]	RW	periaxi_slave_priority_s2	PERI AXI S2 (media_apb) port bus access priority. 7 is the highest priority.
[3]	RO	reserved	reserve.
[2:0]	RW	periaxi_slave_priority_s1	PERI AXI S1 (sys_apb) port bus access priority. 7 is the highest priority.

MISC_CTRL93

MISC_CTRL93 is the VDP_AIAO bus arbitration control register.

Offset Address	Register Name	Total Reset Value
0x0174	MISC_CTRL93	0x0000_0000



Bits	Access	Name	Description
[31]	RW	vdp_aiao_axi_timeout_en_m2	VDP_AIAO AXI bus port M2 (AIAO) timeout count enable. 0: disable; 1: enable.
[30:16]	RW	vdp_aiao_axi_timeout_value_m2	VDP_AIAO Timeout count value of AXI bus port M2(AIAO). count value=vpssaxi_timeout_value_m2×2.
[15]	RW	vdp_aiao_axi_timeout_en_m1	VDP_AIAO AXI bus port M1 (VDP) timeout count enable. 0: disable; 1: enable.
[14:0]	RW	vdp_aiao_axi_timeout_value_m1	VDP_AIAO AXI bus port M1 (VDP) timeout count value. count value=vpssaxi_timeout_value_m1×2.

MISC_CTRL94

MISC_CTRL94 is the VDP_AIAO bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0178	MISC_CTRL94	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:7]	RO	reserved	reserve.
[6:4]	RW	_pri 1 is the highest priority.	VDP_AIAO AXI bus port M2 (AIAO) priority. vdp_aiao_axi_port2
[3]	RO	reserved	reserve.
[2:0]	RW	_pri 1 is the highest priority.	VDP_AIAO AXI bus port M1 (VDP) priority. vdp_aiao_axi_port1

3.6 DMA Controller

3.6.1 Overview

DMA (Direct Memory Access) is a high-speed data transfer operation that allows direct reading and writing of data between external devices and memory without going through the CPU. The DMA Controller (DMAC) performs data transfers directly between memory and peripherals, peripherals and peripherals, and memory and memory, avoiding CPU intervention and reducing CPU interrupt handling overhead.

3.6.2 Features

The DMAC in Hi3519V100 has the following features:

- Support 8bit, 16bit, 32bit data bit width mode transmission.
- Four DMA channels are provided, each configurable for a unidirectional transfer.
- Provide 2 Master bus interfaces with a bus width of 32bit for data transmission. Supports software controlled DMA requests.
- Support to determine DMA BURST length by programming.

The source and destination addresses can be individually configured to auto-increment or not during DMA transfers. Support linked list DMA transfer.

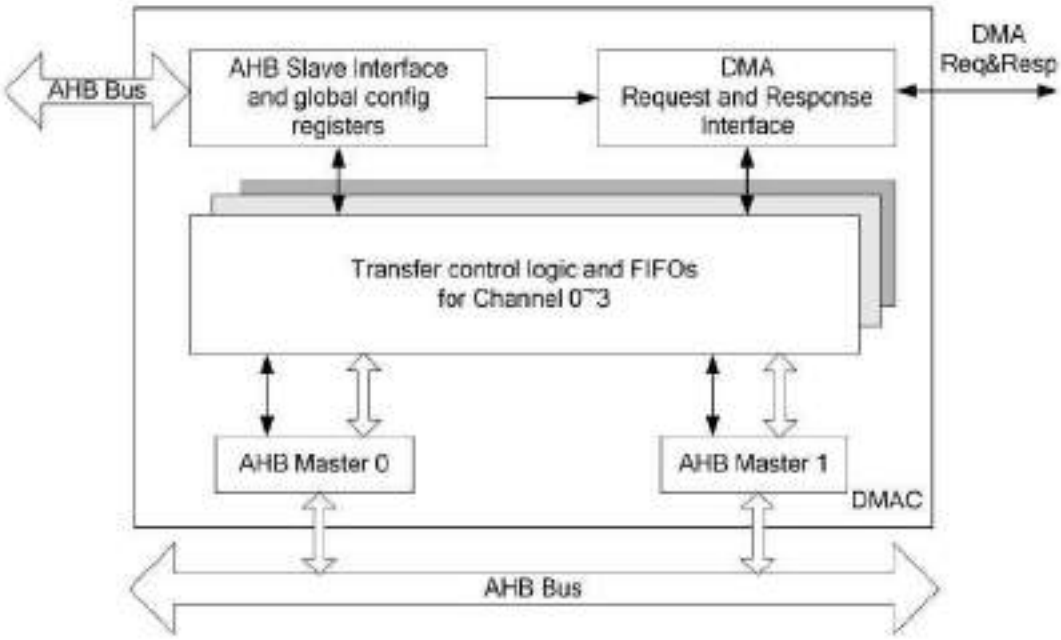
Support DMAC flow control.

3.6.3 Functional description

Functional block diagram

The functional block diagram of the DMAC is shown in Figure 3-5 .

Figure 3-5 DMAC functional block diagram



说明

The priority of the DMA channel is fixed, and the channel numbers corresponding to the priority from high to low are 0~3. When DMA requests from 2 peripherals are active at the same time, the channel with higher priority starts to transfer first.

Each of DMA channels 0~1 contains a 4x32bit FIFO, and each of DMAC channels 2~3 contains one 16x32bit FIFO.

Each channel of the DMAC contains a set of transfer control logic and a FIFO. The transfer control logic automatically completes the following processes:

Step 1. Read data from the source address location specified by the software.

Step 2. Buffer into the FIFO included in the channel.

Step 3. Fetch data from channel FIFO.

Step 4. Write to the destination address specified by the software.

----Finish

work process

The basic workflow of DMAC is as follows:

Step 1. The software selects a channel of DMAC for DMA transmission, and configures the channel's source address, destination address, link list head pointer, number of data to be transferred, DMAC request line numbers corresponding to source and destination devices, source device and destination The master used by the device, and start the channel. Once a channel is enabled, the DMAC hardware begins to detect activity on the DMA request lines of the source and destination peripherals connected to the channel.

Step 2. The source device initiates a DMA request to the DMAC (if the source device is a memory device, the DMAC always valid).

Step 3. The DMAC channel responds to the DMA request of the source device, reads data from the source device and stores it in the FIFO inside the channel.

Step 4. The destination device initiates a DMA request to the DMAC (if the destination device is a memory, the DMAC defaults that its DMA request is always valid).

Step 5. The DMAC channel responds to the DMA request of the destination device, takes out the data from the FIFO inside the channel and writes it into the destination device. prepare.

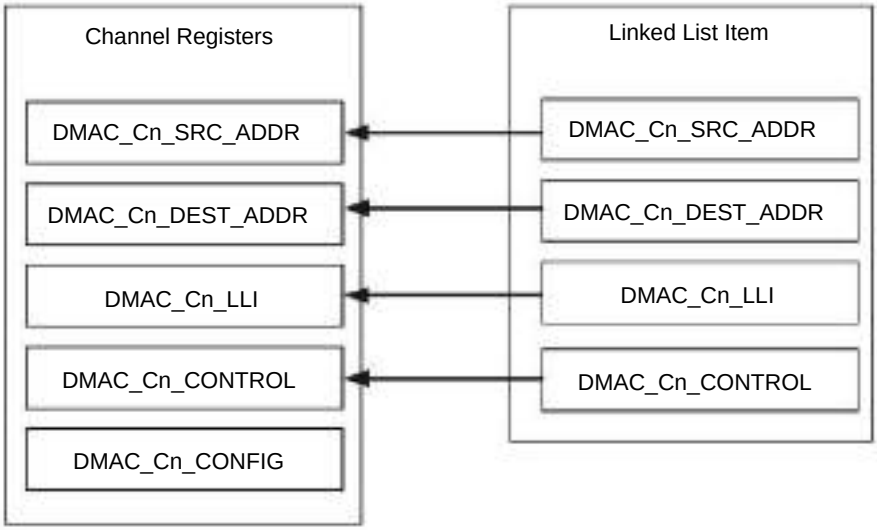
Step 6. Steps 2, 3 and 4, 5 may be performed concurrently, because the source device and the destination device may send DMAC initiates DMA request. When the DMA channel FIFO is full and the destination device is too late to read, or the DMA channel FIFO is read to be empty but the source device is too late to write, the DMAC will automatically block the DMA request of the source or destination device until the corresponding FIFO full state is released until. During the multiple interactions between the DMAC and the source device and the destination device, steps 2 to 5 are executed repeatedly until the data transfer specified by the software is completed, and a transfer completion interrupt is issued (the interrupt can be masked). If the register DMAC_Cn_LLI is not 0, read the linked list node with the value of the register as the address, and load the read value into DMAC_Cn_SRC_ADDR,

The four registers DMAC_Cn_DEST_ADDR, DMAC_Cn_LLI and DMAC_Cn_CONTROL (as shown in Figure 3-5), and then return to step 2. If the value of the register DMAC_Cn_LLI is 0, the current DMA transmission is stopped, the channel is automatically closed, and the transmission process ends.

----Finish

The LLI update channel register is shown in Figure 3-6 .

Figure 3-6 Schematic diagram of LLI updating channel registers



Connection relationship between DMA and peripherals

Peripherals use DMA request signals to request data transfers from the DMAC.

DMAC provides two DMA request signals for each peripheral, namely:

DMACBREQ burst

transfer request signal. This signal triggers a burst transmission, and the burst length is a preset value.

DMACSREQ Single

transfer request signal. This signal initiates a single transfer where the DMAC reads a data from or writes a data to a peripheral.

DMAC provides a request clear signal DMACLR:

The DMA request clear signal sent by the DMAC to each peripheral is used to respond to the DMA request signal of the peripheral.

DMAC request line

Table 3-10 shows the correspondence between DMAC hardware requests and corresponding devices .

Table 3-10 DMA peripheral request allocation definition

DMAC controller hardware request line number	Corresponding equipment
0	UART0 RX channel DMA request/UART4 RX channel DMA request (please refer to dma_01_sel in MISC_CTRL1 register for selection configuration)
1	UART0 TX channel DMA request/UART4 TX channel DMA request (please refer to dma_01_sel in MISC_CTRL1 register for selection configuration)

DMAC controller hardware request line number	Corresponding equipment
2	UART1 RX channel DMA request
3	UART1 TX channel DMA request
4	UART2 RX channel DMA request
5	UART2 TX channel DMA request
6	UART3 RX channel DMA request
7	UART3 TX channel DMA request
8	I2C 0 RX channel DMA request/SSP0 RX channel DMA request (please refer to dma_89_sel in MISC_CTRL1 register for selection configuration)
9	I2C 0 TX channel DMA request/SSP0 TX channel DMA request (please refer to dma_89_sel in MISC_CTRL1 register for selection configuration)
10	I2C 1 RX channel DMA request/SSP1 RX channel DMA request (please refer to dma_ab_sel in MISC_CTRL1 register for selection configuration)
11	I2C 1 TX channel DMA request/SSP1 TX channel DMA request (please refer to dma_ab_sel in MISC_CTRL1 register for selection configuration)
12	I2C 2 RX channel DMA request/SSP2 RX channel DMA request (please refer to dma_cd_sel in MISC_CTRL1 register for selection configuration)
13	I2C 2 TX channel DMA request/SSP2 TX channel DMA request (refer to dma_cd_sel in MISC_CTRL1 register for selection configuration)
14	I2C 3 RX channel DMA request
15	I2C 3 TX channel DMA request

The source and destination requests corresponding to the DMA channel are configured by software. For example, DMA request number 4 is the receive channel request of UART2, if you want to use channel 3 to transmit the received data of UART2, you should configure DMA request number 4 as the source request of channel 3.

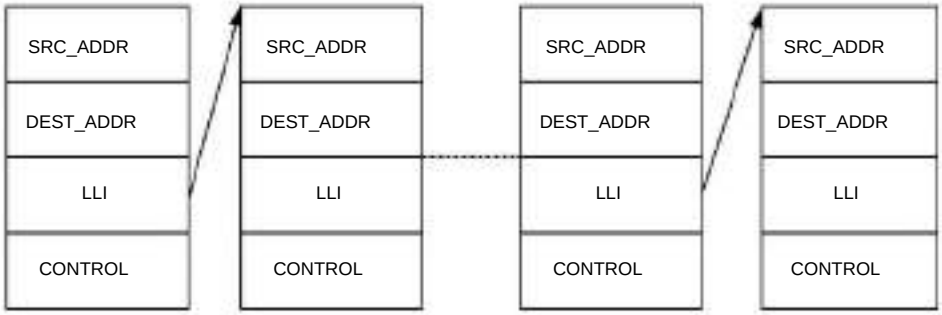
The memory does not have a DMA request line. When the DMA transfer party is the memory, the DMAC defaults that its DMA request is always valid. Due to the transmission on channels 2 and 3 of the DMAC, after each bus operation, an IDLE cycle will be inserted for the Master of the high-priority channel to occupy the bus for transmission; therefore, it is recommended to configure memory-to-memory transfers to channels 2 and 3 for , so that other channels on the bus cannot occupy the bus for a long time.

DMA linked list

The linked list node data structure of DMAC is:

The channel register DMAC_Cn_SRC_ADDR sets the first address of the source device. The channel register DMAC_Cn_DEST_ADDR sets the first address of the destination device. The channel register DMAC_Cn_LLI sets the address of the next node. The channel register DMAC_Cn_CONTROL sets parameters such as the Master used to access the source/destination device, the bit width of the source/destination device, burst size, address increment, and transfer size.

Figure 3-7 Example of DMAC linked list structure



注意

The LLI field of the linked list should not specify a number greater than 0xFFFF_FFF0. Otherwise, a 4-word burst transfer will cause the address to wrap around to 0x0000_0000, resulting in that the linked list node data structure cannot be stored in a continuous address area.

If the value of LLI is 0, it means that the current node is the end of the linked list, and the channel will be closed when all the data blocks corresponding to this node are transmitted.

3.6.4 Working method

clock gating

When the following situations occur, the DMAC can be turned off by software, and the DMAC clock can be turned off to reduce power consumption:

Each channel of the DMAC is idle and there are no DMA transfer requests

DMAC_Cn_CONFIG[ch_en]=0, all channels of DMAC are closed

The steps to turn off the DMAC clock are as follows:

Step 1. Write 0 to DMAC_Cn_CONFIG[ch_en] to close the DMAC channel.

Step 2. Write 0 to DMAC_CONFIG [dmac_enable] to disable DMAC.

Step 3. Write 0 to the CRG register PERI_CRG56 [dmac_cken] to turn off the bus clock gating of the DMA module and finally turn off the DMAC clock.

Step 4. When the DMAC needs to be used for data transfer, turn the clock back on and start the DMAC.

----Finish

initialization

The steps to initialize the DMAC are as follows:

Step 1. Write register DMAC_CONFIG, set the byte order of Master1 and Master2 of DMAC, write 1 to DMAC_CONFIG[dmac_enable], start DMAC.

Step 2. Write all bits of registers DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to 1, clear all off state.

Step 3. Write the corresponding bit of the register DMAC_SYNC to 0, and set the DMA request signal group that needs to be synchronized.

Step 4. Configure and close each channel in turn. Write 0 to DMAC_Cn_CONFIG[ch_en] of each channel to close the channel road.

----Finish

start channel

After the DMAC initialization is completed, the DMAC channel needs to be configured and started before the DMAC can be used for data transmission. The configuration and startup steps of the channel are as follows:

Step 1. Read the DMAC_ENABLED_CHNS register to find out the channels in the non-transmitting state, and select one channel for configuration.

Step 2. Write 1 to the corresponding bits in registers DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3. Write the channel register DMAC_Cn_SRC_ADDR to set the first access address of the source device.

Step 4. Write the channel register DMAC_Cn_DEST_ADDR to set the first access address of the destination device.

Step 5. Write the channel register DMAC_Cn_LLI to set the link list information. If the channel is configured for single-block data transmission, configure the channel register DMAC_Cn_LLI as 0; if the channel is configured for linked list data transmission, configure the channel register DMAC_Cn_LLI as the head pointer of the linked list .

Step 6. Write the channel register DMAC_Cn_CONTROL to set the Master used to access the source/destination device, the bit width of the source/destination device, BURST length, address increment, and trans_size and other parameters.

Step 7. Write the channel register DMAC_Cn_CONFIG to set the DMA request signal, flow control mode and interrupt of this channel shield.

Step 8. Write channel register DMAC_Cn_CONFIG[ch_en] to 1 to start the channel.

----Finish

DMAC_Cn_CONTROL Instructions for use

The channel control register DMAC_Cn_CONTROL contains DMA channel control information, such as transfer length, burst length, transfer bit width, etc.

Each register must be programmed directly by software before the corresponding channel is enabled. When the channel is started, the value of this register is updated when loading from the linked list node after transmitting a complete data block.

When the channel is active, no valid information can be obtained by reading this register. This is because when the software gets the read register value, the value of the register has changed along with the channel transmission. This register can be read when the channel stops transmitting.

The values of dbsize and sbsize of DMAC_Cn_CONTROL register and the corresponding BURST length are shown in Table 3-11 .

Table 3-11 dbsize and sbsize values and their corresponding burst lengths

The value of dbsize or sbsize	BURST length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

The values of dwidth and swidth of the DMAC_Cn_CONTROL register and their corresponding transmission bit widths are shown in Table 3-12 .

Table 3-12 dwidth and swidth values and their corresponding transmission bit widths

the value of swidth or dwidth	Transmission bit width
000	Byteÿ8bitÿ
001	Halfwordÿ16bitÿ
010	Wordÿ32bitÿ
011	reserved
100	reserved
101	reserved
110	reserved

the value of swidth or dwidth	Transmission bit width
111	reserved

Note when configuring the register DMAC_Cn_CONTROL :

When the transfer width of the source device is smaller than the transfer width of the destination device, the product of the transfer width of the source device and trans_size should be an integer multiple of the transfer width of the destination device, otherwise the data in the FIFO will be stranded and lost.

The swidth and dwidth fields cannot be set to an undefined bit width.

If the trans_size field is written as 0 and the DMAC is the flow controller, the DMAC will not perform any transmission action. It is the programmer's responsibility to turn off this DMA channel and reprogram this channel.

Ordinary write/read tests should not be performed on the DMAC_Cn_CONTROL register. Since the trans_size field is not an ordinary register field that can be written and read back with the same value. When written, this field is like a control register, because it determines how much data the DMAC should transfer; when read back, this field is equivalent to a status register, because it returns the remaining number of data to be transferred (in source device bit width).

When the setting value of the trans_size field is greater than the depth of the FIFO in the source device or the destination device (the FIFO of the peripheral, not the FIFO of the DMAC), the source address or destination address of the DMAC must be set to the non-increment mode, otherwise it may cause The peripheral's FIFO overflowed.

Bus access information is provided by master interface signals to source or destination devices when a transfer occurs. These access information are DMAC_Cn_CONTROL[prot_stat] and DMAC_Cn_CONFIG[ch_lock] bits set by programming the channel register . Table 3-13 gives the meaning of the 3 protection bits using prot.

Table 3-13 DMAC_Cn_CONTROL register prot_stat segment attribute and definition

bit description		Purpose
[2]	Cacheable or noncacheable	Indicates whether the access is cacheable or not cacheable. 0: not cacheable; 1: Can be cached. For example, this bit can be used to tell an AMBA bridge that when it sees the first read operation of a burst read of 8 numbers, the bridge can directly initiate a burst read of 8 numbers on the target bus without the source Read operations on the bus are transferred to the target bus one at a time. This bit controls the output of the bus signal HPROT[3].
[1]	Bufferable or nonbufferable	Indicates whether the access is bufferable or non-bufferable. 0: not bufferable; 1: Bufferable. For example, this bit can be used to tell an AMBA bridge that a write operation on the source bus can be completed with zero wait states, without waiting for the bridge to arbitrate the operation to the destination bus, and without waiting for the slave to finish receiving the data. This bit controls the output of the bus signal HPROT[2].

bit description		Purpose
[0]	Privileged or User	Indicates whether the access is user mode or privileged mode. 0: user mode; 1: Privileged mode. This bit controls the output of the bus signal HPROT[1].

ÿÿAMBAÿAdvanced Microcontroller Bus Architectureÿ

DMAC_Cn_CONFIG instructions

Table 3-14 describes the flow control and transfer types corresponding to the flow_ctrl field of the DMAC_Cn_CONFIG register.

Table 3-14 Flow controller and transmission type bit definition

bit value transfer type	controller
000 memory to memory	DMAC
001 memory to peripheral	DMAC
010 Peripherals to memory	DMAC
011 Source device to destination device	DMAC
100 source device to destination device	destination device
101 Memory to Peripherals	destination device
110 Peripherals to Memory	source device
111 Source device to destination device	source device

interrupt handling

After the DMAC channel configuration startup transfer is completed or an error occurs during the transfer process, an interrupt will be reported to the interrupt controller.

The processing steps of the interrupt program are as follows:

Step 1. Read the interrupt status register DMAC_INT_STAT to find out the channel that issued the interrupt request. When multiple channels send

When an interrupt request is issued, the interrupt with the highest priority is serviced first.

Step 2. Read the register DMAC_INT_TC_STAT, and compare whether the selected bit is 1, so as to determine that the interrupt sent by the corresponding channel is the transmission completion interrupt. If yes, go to step 4 to execute; otherwise, go to step 3 to continue execution.

Step 3. Read the register DMAC_INT_ERR_STAT, and compare whether the selected bit is 1, so as to determine that the interrupt sent by the corresponding channel is an error interrupt. If so, go to step 5 for execution; otherwise, exit the interrupt processing.

Step 4. Transfer complete interrupt processing. It can be divided into the following sub-steps:

a. Write the register DMAC_INT_TC_CLR, write 1 to the selected bit , and clear the interrupt status of the corresponding channel.

b. Take away or use the data in the buffer in the memory, and reconfigure and start the channel if necessary (for example, a new buffer needs to be opened in the memory).

c. Exit interrupt processing.

Step 5. Error interrupt handling. It can be divided into the following sub-steps:

a. Write register DMAC_INT_ERR_CLR, write 1 to the selected bit , clear the interrupt status of the corresponding channel state.

b. Give an error message, reconfigure and start the channel if necessary.

c. Exit interrupt processing.

----Finish

3.6.5 DMAC register overview

An overview of the DMAC registers is shown in Table 3-15 .

Table 3-15 DMAC register overview (base address is 0x1003_0000)

offset address	name	describe	page number
0x0000	DMAC_INT_STAT	DMAC Interrupt Status Register	3-130
0x0004	DMAC_INT_TC_STAT	DMAC Transfer Complete Interrupt Status Register	3-131
0x0008	DMAC_INT_TC_CLR	DMAC transfer complete interrupt clear register	3-132
0x000C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-133
0x0010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-133
0x0014	DMAC_RAW_INT_TC_STAT	DMAC Raw Transfer Complete Interrupt Register	3-134
0x0018	DMAC_RAW_INT_ERR_STAT	DMAC Raw Error Interrupt Register	3-135
0x001C	DMAC_ENABLED_CHNS	DMAC Channel Enable Status Register	3-136
0x0020	DMAC_SOFT_BREQ	DMAC Software BURST Transfer Request Register	3-137
0x0024	DMAC_SOFT_SREQ	DMAC Software SINGLE Transfer Request Register	3-138
0x0028	DMAC_SOFT_LBREQ	DMAC software last BURST request register	3-139
0x002C	DMAC_SOFT_LSREQ	DMAC software last SINGLE request register	3-139
0x0030	DMAC_CONFIG	DMAC configuration register	3-140

offset address name		describe	page number
0x0034 DMAC_SYNC		DMAC Request Line Synchronization Enable Register	3-141
0x0100ÿ n×0x20	DMAC_Cn_SRC_ADDR	DMA channel n (n=0,1,2,3) source address register	3-141
0x0104ÿ n×0x20	DMAC_Cn_DEST_ADDR	DMA channel n (n=0,1,2,3) destination address register	3-142
0x0108ÿ n×0x20	DMAC_Cn_LLI	DMA channel n (n=0,1,2,3) linked list information register	3-142
0x010Cÿ n×0x20	DMAC_Cn_CONTROL	DMA channel n (n=0,1,2,3) control register	3-143
0x110ÿn ×0x20	DMAC_Cn_CONFIG	DMA Channel n (n=0,1,2,3) Configuration Register	3-145

The value range and meaning of the variables in the DMAC register offset address are shown in Table 3-16 .

Table 3-16 DMAC register offset address variable table

variable name	Ranges	describe
n	0ÿ3	Corresponding to DMA channel 0~3

3.6.6 DMAC register description

DMAC_INT_STAT

DMAC_INT_STAT is the DMAC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	DMAC_INT_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.

[3]	RO	ch3_int_stat	Masked interrupt status of channel 3. 0: no interrupt is generated; 1: An interrupt has been generated (transmission error or transmission complete).
[2]	RO	ch2_int_stat	Masked interrupt status of channel 2. 0: no interrupt is generated; 1: An interrupt has been generated (transmission error or transmission complete)
[1]	RO	ch1_int_stat	Channel 1 masked interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated (transmission error or transmission complete)
[0]	RO	ch0_int_stat	Channel 0 masked interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated (transmission error or transmission complete)

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is the DMAC transfer complete interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	RO	ch3_int_tc_stat	Channel 3 Masked transfer complete interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[2]	RO	ch2_int_tc_stat	Channel 2 masked transfer complete interrupt status. 0: Interrupt not generated; 1: Interrupt generated.

[1]	RO	ch1_int_tc_stat	Channel 1 masked transfer complete interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[0]	RO	ch0_int_tc_stat	Channel 0 masked transfer complete interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is the DMAC transfer complete interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	WO	ch3_int_tc_clr	Clear channel 3 transfer complete interrupt. 0: do not clear; 1: Clear.
[2]	WO	ch2_int_tc_clr	Clear channel 2 transfer complete interrupt. 0: do not clear; 1: Clear.
[1]	WO	ch1_int_tc_clr	Clear channel 1 transfer complete interrupt. 0: do not clear; 1: Clear.
[0]	WO	ch0_int_tc_clr	Clears the channel 0 transfer complete interrupt. 0: do not clear; 1: Clear.

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is the DMAC error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_stat	ch2_int_err_stat	ch1_int_err_stat	ch0_int_err_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	RO	ch3_int_err_stat	Masked error interrupt status for channel 3. 0: no interrupt is generated; 1: An interrupt has been generated.
[2]	RO	ch2_int_err_stat	Channel 2 masked error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[1]	RO	ch1_int_err_stat	Channel 1 masked error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[0]	RO	ch0_int_err_stat	Channel 0 masked error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is the DMAC error interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	WO	ch3_int_err_clr	Clear channel 3 error interrupt. 0: do not clear; 1: Clear.
[2]	WO	ch2_int_err_clr	Clear channel 2 error interrupt. 0: do not clear; 1: Clear.
[1]	WO	ch1_int_err_clr	Clear channel 1 error interrupt. 0: do not clear; 1: Clear.
[0]	WO	ch0_int_err_clr	Clear channel 0 error interrupt. 0: do not clear; 1: Clear.

DMAC_RAW_INT_TC_STAT

DMAC_RAW_INT_TC_STAT is the DMAC raw transfer complete interrupt register.

Offset Address	Register Name	Total Reset Value
0x0014	DMAC_RAW_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_tc	ch2_raw_int_tc	ch1_raw_int_tc	ch0_raw_int_tc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	RO	ch3_raw_int_tc	Channel 3 Raw transfer complete interrupt status. 0: No transfer completion interrupt generated; 1: Generate a transfer complete interrupt.
[2]	RO	ch2_raw_int_tc	Channel 2 Raw transfer complete interrupt status. 0: No transfer completion interrupt generated; 1: Generate a transfer complete interrupt.
[1]	RO	ch1_raw_int_tc	Channel 1 Raw transfer complete interrupt status. 0: No transfer complete interrupt generated; 1: Transfer complete interrupt generated.
[0]	RO	ch0_raw_int_tc	Channel 0 raw transfer complete interrupt status. 0: No transfer completion interrupt generated; 1: Generate a transfer complete interrupt.

DMAC_RAW_INT_ERR_STAT

DMAC_RAW_INT_ERR_STAT is the DMAC raw error interrupt register.

Offset Address	Register Name	Total Reset Value
0x0018	DMAC_RAW_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												~~~			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:4] RO		reserved	reserve.
[3]	RO	ch3_raw_int_err	Channel 3 raw error interrupt status. 0: no error interrupt is generated; 1: An error interrupt is generated.
[2]	RO	ch2_raw_int_err	Channel 2 raw error interrupt status. 0: no error interrupt is generated; 1: An error interrupt is generated.
[1]	RO	ch1_raw_int_err	Channel 1 raw error interrupt status. 0: no error interrupt is generated; 1: An error interrupt is generated.
[0]	RO	ch0_raw_int_err	Channel 0 raw error interrupt status. 0: No error interrupt generated; 1: Error interrupt generated.

DMAC_ENABLED_CHNS

DMAC_ENABLED_CHNS is the DMAC channel enable status register.

Offset Address	Register Name	Total Reset Value
0x001C	DMAC_ENABLED_CHNS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3]	RO	ch3_enabled	Channel 3 enable status. 0: forbidden; 1: enable.
[2]	RO	ch2_enabled	Channel 2 enable status. 0: forbidden; 1: enable.
[1]	RO	ch1_enabled	Channel 1 enable status. 0: forbidden; 1: enable.
[0]	RO	ch0_enabled	Channel 0 enable status. 0: disable; 1: enable.

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is the DMAC software BURST transfer request register. used for software control to generate DMA BURST transfer request.

Read this register to know the device that is currently requesting DMA BURST transfer. Both the peripheral and this register can generate a DMA request.

Offset Address	Register Name	Total Reset Value
0x0020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	soft_breq
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	soft_breq	It is used for software control to generate DMA BURST transfer request. Please refer to the corresponding relationship between DMAC hardware request and corresponding device for the corresponding request of each bit. When writing to this register: 0: no effect; 1: A DMA BURST transfer request is generated, and the corresponding bit in this register is cleared when the transfer is completed. When reading this register: 0: The peripheral corresponding to the request line DMACBREQ[15:0] has not issued a DMA BURST request; 1: The peripheral corresponding to the request line DMACBREQ[15:0] is requesting a DMA BURST transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is the DMAC software SINGLE transfer request register. used for software control to generate DMA SINGLE transfer request.

If you read this register, you can know the device that is currently requesting DMA SINGLE transfer. Each of the 16 DMA request input signals of the DMAC and this register can generate a DMA request.

Offset Address	Register Name	Total Reset Value
0x0024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	soft_sreq
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0]	RW	soft_sreq	It is used for software control to generate DMA SINGLE transfer request. Please refer to the corresponding relationship between DMAC hardware request and corresponding device for the corresponding request of each bit. When writing to this register: 0: no effect; 1: A DMA SINGLE transfer request is generated, and the corresponding bit in this register is cleared when the transfer is completed. When reading this register: 0: The peripheral corresponding to the request line DMACSREQ[15:0] has not issued DMA SINGLE request; 1: The peripheral corresponding to the request line DMACSREQ[15:0] is requesting a DMA SINGLE transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is the last BURST request register of DMAC software. It is used for software control to generate DMA last burst transfer request.

Offset Address	Register Name	Total Reset Value
0x0028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	soft_lbreq
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	soft_lbreq	The last burst request is initiated by the software. 0: no effect; 1: A DMA last burst transfer request is generated, and the corresponding bit in this register is cleared when the transfer ends.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is the last SINGLE request register of DMAC software. It is used for software control to generate DMA last single transfer request.

Offset Address	Register Name	Total Reset Value
0x002C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	soft_lsreq
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	soft_lsreq	The last single transfer request is initiated by the software. 0: no effect; 1: A DMA last single transfer request is generated, and the corresponding bit in this register is cleared when the transfer ends.

DMAC_CONFIG

DMAC_CONFIG is the DMAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	DMAC_CONFIG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	—
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	m2_endianness	Master 2 byte order configuration. 0: little endian format; 1: Big endian format.
[1]	RW	m1_endianness	Master 1 byte order configuration. 0: little endian format; 1: Big endian format.

[0] RW dmac_enable			DMA controller is enabled. 0: disable DMA controller; 1: Enable DMA controller.

DMAC_SYNC

DMAC_SYNC is the DMAC request line synchronization enable register.

Offset Address	Register Name	Total Reset Value
0x0034	DMAC_SYNC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dmac_sync
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15:0] RW dmac_sync			Control whether the request line needs to be synchronized, and each bit corresponds to the request, please refer to The correspondence between DMAC hardware requests and corresponding devices. 0: Enable the DMA request signal synchronization logic of the corresponding peripheral; 1: Disable the DMA request signal synchronization logic of the corresponding peripheral.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is the source address register of DMA channel n (n=0,1,2,3).

The offset address of the register is 0x100+n*0x20. Among them, the value of n is 0~3, corresponding to DMA channel 0~ 3ÿ

Each register must be programmed directly by software before the corresponding channel is enabled. When a channel is enabled, this register is updated in the following cases:

when the source address is incremented.

When a complete data block is passed, it is loaded from the linked list node.

When the channel is active, no valid information can be obtained by reading this register. This is because when the software gets the read register value, the value of the register has changed along with the channel transmission. The read operation of this register is generally used when the channel stops transmitting. At this time, the read value shows the source address when the DMAC reads the last item.

Offset Address	Register Name	Total Reset Value
0x0100ÿn×0x20 (n = 0ÿ3)	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	src_addr	DMA source address.

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is the destination address register of DMA channel n (n=0,1,2,3).

The offset address is: 0x104+nx 0x20. Among them, the value of n is 0~3, corresponding to DMA channel 0~3 respectively.

The channel destination address register DMAC_Cn_DEST_ADDR contains the destination address of the current data to be transmitted. Each register must be programmed directly by software before the corresponding channel is enabled. When a channel is enabled, this register is updated in the following cases:

The destination address is incremented.

After passing a complete data block, load it from the linked list node.

When the channel is active, no valid information can be obtained by reading this register. This is because when the software gets the read register value, the value of the register has changed along with the channel transmission. When the channel stops transmitting, read this register, and the read value at this time shows the destination address when the DMAC writes the last item.

Offset Address	Register Name	Total Reset Value
0x0104ÿn×0x20 (n = 0ÿ3)	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dest_addr	DMA destination address.

DMAC_Cn_LLI

DMAC_Cn_LLI is the linked list information register of DMA channel n (n=0,1,2,3).

The offset address is: 0x108+nx 0x20. Among them, the value of n is 0~3, corresponding to DMA channel 0~DMA channel 3 respectively. Please refer to the "DMA Linked List" section for details.

Offset Address	Register Name	Total Reset Value
0x0108ÿn×0x20 (n = 0ÿ3)	DMAC_Cn_LLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ll_item																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:2]	RW ll_item	Bits [31:2] of the address of the next linked list node, address bits [1:0] are 0. The linked list address is required to be 4-byte aligned.
[1]	RW reserved	Reserved, 0 must be written when writing, and this bit should be masked when reading.
[0]	RW ll_master	Master for loading the next linked list node. 0ÿMaster 1ÿ 1ÿMaster 2ÿ

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is the control register for DMA channel n (n=0,1,2,3).

The offset address is: 0x10C+nx 0x20. Among them, the value of n is 0~3, corresponding to DMA channel 0~DMA channel 3 respectively.

Offset Address	Register Name	Total Reset Value
0x010Cÿn×0x20 (n = 0ÿ3)	DMAC_Cn_CONTROL	0x0000_0000

Bits	Access Name		Description
[31] RW int_tc_enable			Transfer complete interrupt enable bit. This bit is used to determine whether the current linked list node triggers the transmission completion interrupt. 0: The current linked list node does not trigger the transmission completion interrupt; 1: The current linked list node triggers the transmission completion interrupt.
[30:28] RW prot_stat			The access protection HPROT[2:0] signal issued by the master.
[27] RW dest_incr			The destination address is incremented. 0: The destination address is not incremented; 1: The destination address is incremented every time a number is passed. When the destination device is a peripheral, the destination address does not increase; when the destination device is a memory, the destination address increases.
[26] RW src_incr			The source address is incremented. 0: The source address is not incremented; 1: The source address is incremented every time a number is passed. When the source device is a peripheral, the source address does not increase; when the source device is a memory, the source address increases.
[25] RW dest_select			Set the master of the access target device. 0: use master1 to access; 1: use master2 to access.
[24] RW src_select			Set the master for accessing the source device. 0: use master1 to access; 1: Use master2 to access.
[23:21] RW dwidth			The transmission bit width of the destination device. A transfer bit width wider than the master bit width is illegal. The bit width of the destination device and the source device can be different, and the hardware automatically packs and unpacks the data.

			See Table 3-12 for the value of DWidth and the corresponding relationship between specific bit widths .
[20:18] RW swidth			Source device transmission bit width. A transfer bit width wider than the master bit width is illegal. The bit width of the destination device and the source device can be different, and the hardware automatically packs and unpacks the data. See Table 3-12 for the value of SWidth and the corresponding relationship between specific bit widths .
[17:15] RW dbsize			The burst length of the destination device. Indicates the number of data to be transmitted for one burst transmission of the destination device, that is, the number of data to be transmitted when DMACCnBREQ is valid. This value must be set to the burst size supported by the destination device, or if the destination device is a memory, to the size of the memory area to the memory address boundary. For the corresponding relationship between the value of DBSize and the specific transmission length, see Table 3-11.
[14:12] RW sbsize			Source device burst length. Indicates the number of data to be transmitted for one source device burst transmission, that is, the number of data to be transmitted when DMACCnBREQ is valid. This value must be set to the burst size supported by the source device, or if the source device is a memory, to the size of the memory area to the memory address boundary. For the corresponding relationship between the value of SBSize and the specific transmission length, see Table 3-11.
[11:0] RW trans_size			Writing to this register sets the length of the DMA transfer if the DMAC is the flow controller. Here transfer size represents the number of data to be transferred by the source device. Read this register to get the number of data sent out on the bus connected to the destination device. When the channel is active, no valid information can be obtained by reading this register. This is because when the software gets the read register value, the value of the register has changed along with the channel transmission. The read operation of this register is generally used when the channel is started and then stopped transmitting.

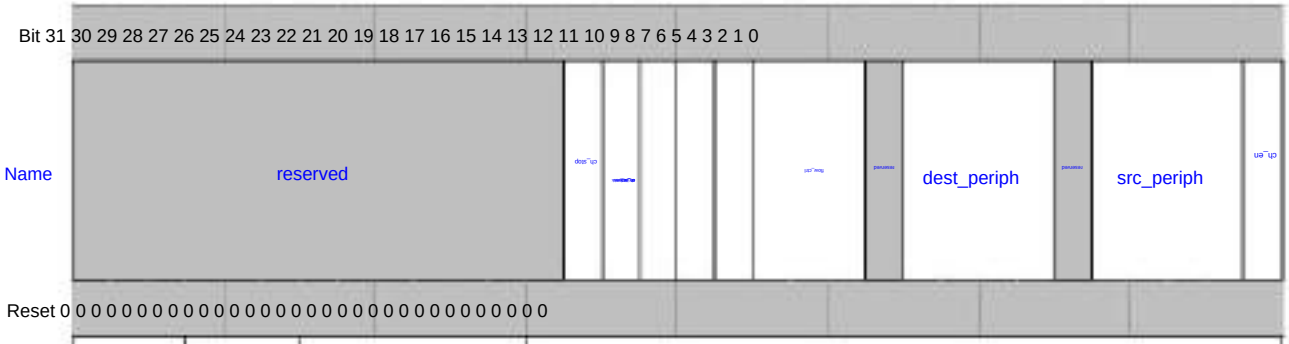
DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is the configuration register for DMA channel n (n=0,1,2,3).

The offset address is: 0x110+n*0x20. Among them, the value of n is 0~3, corresponding to DMA channel 0~DMA channel 3 respectively.

This register is not updated when new linked list nodes are loaded.

Offset Address	Register Name	Total Reset Value
0x110ÿyn×0x20 (n = 0ÿ3)	DMAC_Cn_CONFIG	0x0000_0000



Bits	Access	Name	Description
[31:19]	RW	reserved	reserve. Must write 0 when writing, and should be masked when reading.
[18]	RW	ch_halt	stop ÿÿ 0: Allow DMA request; 1: Ignore subsequent DMA request, all contents in the channel FIFO have been transferred. This bit can be used in conjunction with the Active bit and the Channel Enable bit to turn off a DMA channel without data loss.
[17]	RW	ch_active	Active bit. 0: There is no data in the channel FIFO; 1: There is data in the channel FIFO. This bit can be used in conjunction with the Halt bit and the Channel Enable bit to shut down a DMA channel without data loss.
[16]	RW	ch_lock	Lock bit. 0: Disable lock transmission on the bus; 1: Enables lock transfers on the bus.
[15]	RW	tc_int_msk	Transfer complete interrupt mask bit. 0: Shield the transmission completion interrupt of this channel. 1: Do not shield the transmission completion interrupt of this channel.
[14]	RW	err_int_msk	Error interrupt mask bit. 0: Mask the error interrupt of this channel. 1: Do not mask the error interrupt of this channel.
[13:11]	RW	flow_ctrl	Flow control and transport type fields. This field is used to specify the flow controller and transport type. Flow controllers can be DMACs, source devices, and destination devices. The transfer type can be memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral, memory-to-memory. For details, see Table 3-14 .

[10] RW reserved			reserve. Must write 0 when writing, and should be masked when reading.
[9:6] RW dest_periph			destination device. This field is used to select a peripheral request signal as the request signal of the DMA destination device of this channel. This field is ignored if the destination device of the DMA transfer is memory.
[5] RW reserved			reserve. Must write 0 when writing, and should be masked when reading.
[4:1] RW src_periph			source device. This field is used to select a peripheral request signal as the request signal of the DMA source device of this channel. This field is ignored if the source device for the DMA transfer is memory.
[0] RW ch_en			Channel enable bit. Read this register to know what state the channel is currently in (it can also be obtained by reading the register DMAC_ENABLED_CHNS). 0: close the channel; 1: Enable channel. Channels can be turned off by clearing them. When this bit is cleared, the current bus transfer will continue until complete. Then the channel is closed, and all remaining data in the FIFO is lost; when the last LLI is completed or an error occurs during transmission, the channel will also be closed, and this bit will be cleared; if the channel is to be closed without making the channel FIFO If the data is lost, the Halt bit must also be set at the same time, so that the channel ignores subsequent DMA requests. The active bit must then be polled until its value becomes 0, indicating that there is no more data left in the channel FIFO. Only then can the enable bit be cleared. Starting a channel by setting a bit must first reinitialize the channel before starting the channel again; simply starting a channel by setting a bit will cause unpredictable consequences. When a channel is closed by writing the DMAC_Cn_CONFIG [ch_en] bit, the DMAC_Cn_CONFIG [ch_en] bit must be reset after the corresponding bit in the register DMAC_ENABLED_CHNS is polled to be 0. This is because the actual closing of the channel does not take effect immediately after clearing ch_en. The runtime delay of the bus burst must also be considered.

3.7 Timers

3.7.1 Overview

The Timer module mainly implements the timing and counting functions, which can be used as the system clock by the operating system, and can also be used by the application program as timing and counting. Hi3519V100 provides 6 Timers.

3.7.2 Features

Timers have the following characteristics:

32bit/16bit down timer/counter with programmable 8-bit prescaler.

The counting clock is configurable, and the counting clock of Timer can be selected as bus clock (49.5MHz) or 3MHz clock.

Three counting modes are supported: free-running mode, periodic mode and one-shot counting mode.

There are 2 methods to load the initial value of the count, which are realized through the TIMERx_LOAD and TIMERx_BGLOAD registers respectively.

The current count value can be read at any time.

An interrupt is generated when the count reaches zero.

3.7.3 Functional description

Timer is based on a 32bit/16bit (configurable) down counter. The value of the counter is decremented by 1 at each rising edge of the count clock. When the count value decrements to zero, the Timer will generate an interrupt.

Timer has the following 3 counting modes:

free run mode

The timer keeps counting, and when the count value decreases to 0, it automatically turns back to its maximum value and continues counting. When the count length is 32bit, the maximum value is 0xFFFF_FFFF. When the count length is 16bit, the maximum value is 0xFFFF. In free mode, it is also possible to load the count value and immediately count down from the loaded value, but wrap around to its maximum value when

it reaches 0.

The periodic mode timer keeps counting, when the count value decreases to 0, reload the initial value from the TIMERx_BGLOAD register and continue counting.

one-shot mode

Load the counting initial value into the timer. When the count value of the timer decreases to 0, it stops counting, and does not start counting again until it is reloaded with a new value and the timer is enabled.

Each Timer has a prescaler (prescaler), which can divide its working clock by 1, 16 or 256 again inside the Timer. Further improve the selection flexibility of counting clock frequency.

The method of loading the counting initial value to the timer is as follows:

By writing the TIMERx_LOAD register, the timer can be loaded with the counting initial value. When the timer is in the working state, if you write a value to the TIMERx_LOAD register, it will cause the timer to restart counting from the new value immediately. Applies to all counting modes. The counting period of

the period counting mode can be set by writing the TIMERx_BGLOAD register. Writing this register will not affect the current count of the timer immediately, and the timer will continue to count until the count value decreases to 0. Then the new value loaded into the TIMERx_BGLOAD register starts counting.

3.7.4 Working method

initialization

The Timer should be initialized when the system is initialized. When initializing TimerX ("X" in TimerX is 0, 1, 2, 3, 4, 5), it should be configured according to the following steps:

Step 1. Write the TIMERx_LOAD register to load the initial count value for the Timer.

Step 2. When the Timer needs to work in the period counting mode and the counting period is different from the initial count value loaded into the Timer, write to the TIMERx_BGLOAD register to set the counting period of the Timer.

Step 3. Configure the SC_CTRL register to set the reference clock of the clock enable signal of the Timer.

Step 4. Configure the TIMERx_CONTROL register to set the counting mode, counter length, and prescaler factor of the Timer And interrupt mask, and start Timer counting at the same time.

----Finish

interrupt handling

Timer is mainly used to generate interrupts regularly, so the interrupt processing of Timer is mainly to activate the process waiting for timing interrupts. The operation steps are as follows:

Step 1. Configure the TIMERx_INTCLR register to clear the Timer interrupt.

Step 2. Activate the process waiting for the interrupt to continue execution.

Step 3. When all the processes waiting for the interrupt are completed or execute again to the dormant state waiting for the interrupt, resume the interrupted site and continue to execute the currently interrupted program.

----Finish

clock selection

Timer0, Timer1, Timer2, Timer3, Timer4, and Timer5 all have 2 kinds of counting clocks to choose from. Taking Timer0 as an example, the clock selection configuration process is as follows:

The steps to select the bus clock for counting are as follows:

Step 1. Configure SC_CTRL[timeren0ov]=1 for the system controller.

Step 2. Initialize the Timer and start counting.

----Finish

The steps to select a 3MHz clock for counting are as follows:

Step 1. Configure SC_CTRL[timeren0ov]=0 for the system controller.

Step 2. Initialize the Timer and start counting.

----Finish

3.7.5 Timer register overview

Each of the 6 timers in the Timer module has a set of registers, and these 6 sets of registers have the same characteristics except the base address. in:

Timer0 base address: 0x1200_0000.

Timer1 base address: 0x1200_0020.

Timer2 base address: 0x1200_1000.

Timer3 base address: 0x1200_1020.

Timer4 base address: 0x1200_2000.

Timer5 base address: 0x1200_2020.

说明

"x" in TIMERx takes values 0, 1, 2, 3, 4, 5. Among them, the registers of Timer0~Timer5 are the same, and the descriptions of the registers are described using Timer0 as an example.

Table 3-17 Timer register overview

offset address name		describe	page number
0x000	TIMERx_LOAD count initial value register		3-150
0x004	TIMERx_VALUE Current count value register		3-151
0x008	TIMERx_CONTROL Timer Control Register		3-151
0x00C	TIMERx_INTCLR Interrupt Clear Register		3-153
0x010	TIMERx_RIS	raw interrupt register	3-153
0x014	TIMERx_MIS	Masked Interrupt Register	3-154
0x018	TIMERx_BGLOAD period mode count initial value register		3-154

3.7.6 Timer register description

TIMERx_LOAD

TIMERx_LOAD is the counting initial value register. It is used to configure the counting initial value of the timer. Each of Timer0~Timer5 has a counting initial value register.

说明

The minimum valid value to write to the TIMERx_LOAD register is 1.

When writing 0 to TIMERx_LOAD, Dual-Timer will generate an interrupt immediately.

The difference between TIMERx_LOAD and TIMERx_BGLOAD :

If the value is written to both the TIMERx_BGLOAD register and the TIMERx_LOAD register before the rising edge of the TIMCLK enabled by TIMCLKENx arrives , the TIMCLK enabled by TIMCLKENx will

A rising edge current count value is first updated as the written value of TIMERx_LOAD . When writing a value to the TIMERx_LOAD register, the value of TIMERx_BGLOAD will also be overwritten, so when reading TIMERx_BGLOAD, the returned value is the value of the latest written register among TIMERx_LOAD and TTIMERx_BGLOAD . When the timer is in periodic mode and the count value decreases to 0, it will reload the initial value from the TIMERx_BGLOAD register and continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0_load
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	timer0_load	The initial count value of Timer0.

TIMERx_VALUE

TIMERx_VALUE is the current count value register. Used to give the current value of a counter that is being decremented. Each of Timer0~Timer5 has a current count value register.

When the write operation to the TIMERx_LOAD register occurs, TIMERx_VALUE immediately reflects the new load value of the counter in the PCLK clock domain, without waiting for the next TIMCLK clock edge enabled by TIMCLKENx to arrive.

说明

When the timer is in 16bit mode, the upper 16bits of the 32bit TIMERx_VALUE register are not automatically set to 0. If the timer was in 32bit mode before and TIMERx_LOAD has never been written since entering 16bit mode , the upper 16 bits of the TIMERx_VALUE register may have a non-zero value.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0_value
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access Name		Description
[31:0]	RO	timer0_value	Current value of Timer0 being decremented.

TIMERx_CONTROL

TIMERx_CONTROL is the TIMER control register. Each of Timer0~5 has a control register.

说明

When you choose to count in period mode, you need to set TIMERx_CONTROL[timermode] to 1, TIMERx_CONTROL[oneshot] is set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	timer	The timer is enabled. 0: Disable Timer; 1: Timer enabled.
[6]	RW	timer mode	The counting mode of the timer. 0: Free-running mode; 1: Periodic mode.
[5]	RW	Untenable	TIMERx_RIS interrupt mask. 0: Mask the interrupt; 1: Do not mask the interrupt.
[4]	RO	reserved	reserve.
[3:2]	RW	timerpre	This field is used to set the prescale factor of Timer. 00: No prescaler, the clock frequency is divided by 1; 01: 4-level prescaler, the Timer clock frequency is divided by 16; 10: 8-level prescaler, divide the Timer clock frequency by 256; 11: Undefined, if set to this value, it is equivalent to 8-level prescaler, divide the Timer clock frequency by 256.
[1]	RW	timersize	Select 16bit/32bit counter operation mode. 0: 16bit counter; 1: 32bit counter.
[0]	RW	oneshot	Select the count mode as one-shot count mode or period count mode. 0: Period counting mode or free running mode; 1: One-shot counting mode.

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. Any write to this register will clear the interrupt status of the corresponding counter. Each of Timer0~Timer5 has an interrupt clear register.

注意

This register is a write-only register, if any value is written in, it will cause the timer to be cleared and interrupted, and the written value is not memorized internally, and there is no reset value.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timer0_intclr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	WO	timer0_intclr	Write this register to clear the interrupt output of Timer0.

TIMERx_RIS

TIMERx_RIS is the raw interrupt register. Each of Timer0~Timer5 has a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve. Writing is invalid and returns 0 when reading.
[0]	RO	timer0ris	Raw interrupt status of Timer0. 0: no interrupt is generated; 1: An interrupt has been generated.

TIMERx_MIS

TIMERx_MIS is the masked interrupt register. Timer0~Timer5 each have a masked interrupt register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	—
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	timer0mis	Masked interrupt status of Timer0. 0: Interrupt is invalid; 1: Interrupt is active.

TIMERx_BGLOAD

TIMERx_BGLOAD is the counting initial value register in period mode. Each of Timer0~Timer5 has a period mode count initial value register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload the initial count value when the count value of the timer is decremented to 0 in periodic mode.

This register provides an alternate method of accessing the TIMERx_LOAD register. The difference is that writing a value to the TIMERx_BGLOAD register does not cause the timer to immediately start counting from the newly written value.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	timer0bgload	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:0]	RW	timer0bgload	The initial count value of Timer0. Note: It is different from the TIMERX_LOAD register, please refer to Description of the TIMERx_LOAD register.

3.8 Watchdog

3.8.1 Overview

The watchdog WatchDog is used to send a reset signal within a certain period of time to reset the entire system when the system is abnormal.

3.8.2 Features

WatchDog has the following features:

- There is a 32bit down counter inside, and the counting clock source can be configured.
- It supports configurable timeout interval (that is, the initial count value).
- Support register lock to prevent registers from being changed by mistake.
- Support timeout interrupt generation.
- Support reset signal generation.
- Debug mode is supported.

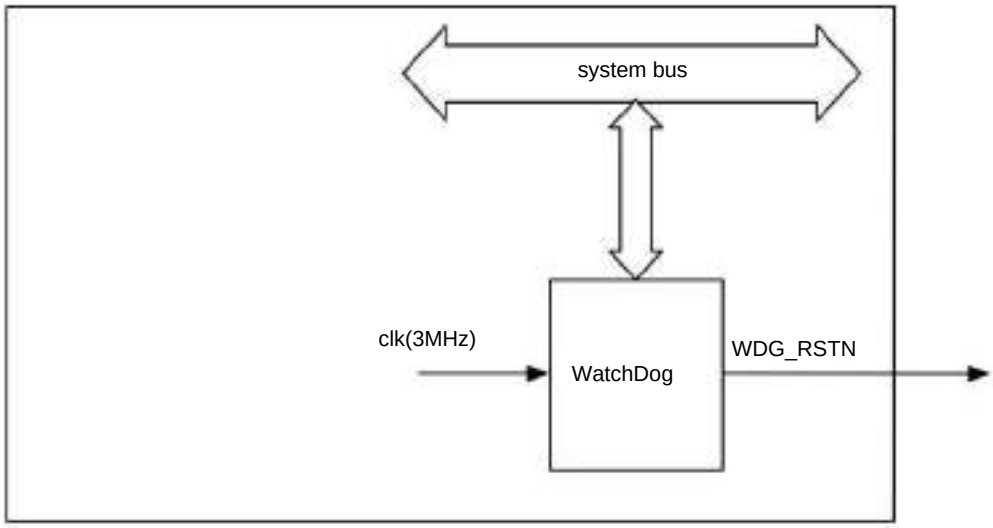
3.8.3 Functional description

Application Block Diagram

The system configures register parameter values for WatchDog through the system bus. WatchDog sends interrupt requests to the system regularly, and when the system does not respond to the interrupt (such as: crash), it sends a WDG_RSTN reset signal to reset the system to achieve the purpose of monitoring system operation.

The block diagram of the WatchDog application is shown in Figure 3-8 .

Figure 3-8 WatchDog application block diagram



Functional principle

The operation of WatchDog is based on a 32bit down counter, and the initial counting value is loaded by the register WDG_LOAD . When the WatchDog clock is enabled, the count value is decremented by 1 at each rising edge of the count clock. When the count value decrements to 0, WatchDog will generate an interrupt. Then at the rising edge of the next counting clock, the counter reloads the counting initial value from the register WDG_LOAD and starts counting down.

If the count value of the counter counts down to 0 for the second time, but the CPU has not cleared the WatchDog interrupt, the WatchDog will send a reset signal WDG_RSTN, and the counter will stop counting.

According to actual application needs, you can enable or disable WatchDog to generate interrupt and reset signals by configuring WDG_CONTROL :

When interrupt generation is disabled, the counter will stop

counting. When interrupts are turned back on, WatchDog will start counting from the value set by WDG_LOAD instead of the value it was at when the counter was last stopped. Before the interrupt arrives, the initial value can be reloaded.

The counting clock of WatchDog can choose crystal oscillator clock or bus clock, which is convenient for choosing different counting time ranges.

By configuring the WDG_LOCK register, you can prohibit writing to the WatchDog internal registers:

Write 0x1ACC_E551 to WDG_LOCK to open the write permission of all WatchDog registers. Writing any other value to the WDG_LOCK register disables write access to all WatchDog registers except the WDG_LOCK register.

This feature protects WatchDog's registers from being incorrectly modified by software, so that under abnormal conditions, WatchDog will not be wrongly terminated by software.

In debug mode, WatchDog is automatically turned off to prevent interference with normal debug operations.

3.8.4 Working method

Count Clock Frequency Configuration

WatchDog count clock is 3MHz clock.

WatchDog counts time as TWDG:

$$T_{WDG} = Value_{WDG\_LOAD} \times \left(\frac{1}{f_{clk}}\right)$$

说明

In the above formula, the meanings of each parameter are:

TWDG means WatchDog counting time;

ValueWDG_LOAD represents the initial value of the WatchDog count;

fclk represents WatchDog counting clock frequency.

The counting time range of WatchDog is 0s~1400s.

System initialization configuration

After the system is powered on and reset, the WatchDog counter is in the stop counting state. During the system initialization process, the WatchDog needs to be initialized and started to run. The initialization process of WatchDog is as follows:

Step 1. Write the register WDG_LOAD to set the counting initial value.

Step 2. Write register WDG_CONTROL to enable interrupt mask and start WatchDog counting.

Step 3. Write the register WDG_LOCK to lock the WatchDog to prevent the software from modifying the WatchDog configuration by mistake.

----Finish

interrupt handling

After receiving the interrupt from WatchDog, the interrupt status should be cleared in time, and it should be loaded with the initial counting value to start counting again. The process of WatchDog interrupt handling is as follows:

Step 1. Write 0x1ACC_E551 to WDG_LOCK to unlock the WatchDog.

Step 2. Write register WDG_INTCLR, clear the interrupt status of WatchDog, and also make WatchDog automatically load
The initial counting value restarts counting.

Step 3. Write any value other than 0x1ACC_E551 to the register WDG_LOCK to lock the WatchDog.

----Finish

close watchdog

Write 0 or 1 to the register WDG_CONTROL[inten] control bit to control the status of WatchDog:

0: Turn off WatchDog; 1:

Turn on WatchDog.

3.8.5 WDG register overview

An overview of the WatchDog registers is shown in Table 3-18 .

Table 3-18 WatchDog register overview (base address is 0x1208_0000)

offset address	name	describe	page number
0x0000	WDG_LOAD	Count initial value register	3-158
0x0004	WDG_VALUE	Counter Current Value Register	3-158
0x0008	WDG_CONTROL	Control Register	3-158
0x000C	WDG_INTCLR	Interrupt Clear Register	3-159
0x0010	WDG_RIS	raw interrupt register	3-159
0x0014	WDG_MIS	Masked Interrupt Register	3-160

offset address	name	describe	page number
0x0C00	WDG_LOCK	LOCK register	3-160

3.8.6 WDG register description

WDG_LOAD

WDG_LOAD is the counting initial value register. It is used to configure the counting initial value of WatchDog's internal counter.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	etc_load
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:0]	RW	etc_load	Count initial value.

WDG_VALUE

WDG_VALUE is the counter current value register. It is used to read the current count value of WatchDog's internal counter.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wdogvalue
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	WatchDog counter current value.

WDG_CONTROL

WDG_CONTROL is the control register. Used to control the On/Off, Interrupt and Reset functions of the WatchDog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RW reset		WatchDog reset signal output enable. 0: forbidden; 1: enable.
[0]	RW inten		WatchDog interrupt signal output enable. 0: The counter stops counting, the count value keeps the current value unchanged, and the WatchDog is turned off; 1: Both start counter and enable interrupt, WatchDog is started.

WDG_INTCLR

WDG_INTCLR is the interrupt clear register. It is used to clear the WatchDog interrupt and make WatchDog reload the initial value for counting. This register is a write-only register, if any value is written in, it will cause the WatchDog to be cleared and interrupted, and the written value is not memorized internally, and there is no reset value.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wdg_intclr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	WO etc_intclr		Writing any value to this register can clear the WatchDog interrupt and make WatchDog reload the initial count from the register WDG_LOAD .

WDG_RIS

WDG_RIS is the raw interrupt register. Used to reflect the WatchDog raw interrupt status.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	wdogris	WatchDog raw interrupt status, this bit is set to 1 when the count value of the counter is decremented to 0. 0: no interrupt is generated; 1: An interrupt has been generated.

WDG_MIS

WDG_MIS is the masked interrupt register. Used to reflect the shielded WatchDog interrupt status.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	wdogmis	Interrupt state after WatchDog masking. 0: No interrupt is generated or the interrupt is masked; 1: An interrupt has been generated.

WDG_LOCK

WDG_LOCK is the LOCK register. Used to control the read and write permissions of WatchDog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	wdg_lock	Write 0x1ACC_E551 to this register to open the write permission of all registers; Writing other values to this register disables write access. Reading this register returns the status of the lock rather than the value written to this register: 0x0000_0000: write access allowed (unlocked); 0x0000_0001: write access disabled (locked).

3.9 Real Time Clock

3.9.1 Overview

The real time clock RTC (Real Time Clock) is used to realize time display and timing alarm function.

3.9.2 Features

RTC has the following characteristics:

It has a 16bit day counter, 5bit hour counter, 6bit minute counter, 6bit second counter and 7bit 10ms counter inside.

Counting clock 100Hz

Counting initial value is

configurable Counting comparison

value is configurable Support timeout

interrupt generation Support soft reset

Support frequency division parameters to be configurable

64bit user registers provide user save data

Battery low voltage

detection 128bit DDR standby information register

3.9.3 Functional description

The operation of RTC is based on a common 40bit (day, hour, minute, second, 10ms) addition counter .

RTC_LR_D_H is loaded. When the count value is added to the register and RTC_MR_10MS, RTC_MR_S,
When the RTC_MR_M, RTC_MR_H, RTC_MR_D_L, RTC_MR_D_H register values are equal, the RTC will generate an interrupt, and then the counter will continue to count up on the next rising edge of the counting clock.

According to actual application needs, RTC can be enabled or disabled to generate interrupt signals by configuring RTC_IMSC . At this point, there are the following two situations:

When the interrupt is disabled, the RTC counter continues to count up, and no external interrupt will be generated. The status of the masked interrupt is displayed in RTC_MSC_INT , and the original interrupt status is displayed in RTC_RAW_INT .

When the interrupt is restarted, the RTC counter still continues to count up. When the count value is added to the RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H,
The RTC will generate an interrupt when the RTC_MR_D_H register values are equal.

The counting clock of RTC adopts 100Hz clock, and provides 16bit day counting at the same time, which is convenient to convert the day counting value into specific year, month and day.

3.9.4 Working method

3.9.4.1 Count clock frequency

The RTC uses a 100Hz clock to count, and the maximum counting time is:

$$T_{RTC} = 65536 \text{ (days)}$$

说明

TRTC represents RTC count time.

3.9.4.2 Soft reset

By configuring the RTC reset register RTC_POR_N, an individual soft reset of the RTC can be realized. After the soft reset, the values of each RTC configuration register are restored to the default values, so these registers need to be initialized and configured again after the soft reset.

The soft reset steps are as follows:

Step 1. Write 0 to RTC_POR_N to soft reset RTC.

Step 2. Wait for 30ms.

----Finish

3.9.4.3 RTC initialization

When the RTC is powered on for the first time, the system needs to initialize the RTC. The initialization process of RTC is as follows:

Step 1. Configure RTC_POR_N, reset RTC.

Step 2. Wait for 30ms.

Step 3. Configure RTC_IMSC, set the RTC interrupt mask bit.

Step 4. Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, RTC_MR_D_H, set the RTC comparison value.

Step 5. Configure RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, RTC_LR_D_H, set the initial value of RTC count.

Step 6. Configure RTC_LORD as 1, so that the initial value of the RTC count is loaded into the RTC counter.

Step 7. Wait for 5ms.

Step 8. The RTC counts from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, The values in RTC_LR_H, RTC_LR_D_L, RTC_LR_D_H start counting, when counting to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, When the value in RTC_MR_D_H , it will determine whether to generate an interrupt according to the setting of RTC_IMSC.

----Finish

3.9.4.4 Interrupt Handling

After the system receives the interrupt from the RTC, it means that the time is up, and the user can perform the corresponding user-defined operation, and the RTC counter still keeps counting up. The process of RTC interrupt processing is as follows:

Step 1. Set RTC_INT_CLR to 1 to clear the RTC interrupt status.

Step 2. If you need to continue to set the timing time, write to the registers RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, RTC_MR_D_H write new comparison values.

----Finish

3.9.4.5 RTC register access

The RTC registers are inside the RTC module and not on the bus. The RTC registers on the bus just provide access to the RTC internal registers.

The steps to write RTC internal registers are as follows:

Step 1. Configure SPI_CLK_DIV; if the bus clock is 50MHz and the expected SPI clock is 5MHz, then spi_clk_div should be configured as (50MHz/5MHz)/2 -1 =4=0x04. (This step can be omitted if it is already configured and you do not want to change the clock frequency of the SPI).

Step 2. Read SPI_RW until SPI_RW [31]=0.

Step 3. Configure SPI_RW; if you want to write 0x10 to RTC_MR_10MS , the internal address of this register in RTC is 0x06, so SPI_RW should be configured as 0x01060010 (spi_start=1, spi_rw=0, spi_add=0x06, spi_wdata=0x10).

----Finish

The steps to read RTC internal registers are as follows:

Step 1. Configure SPI_CLK_DIV; if the bus clock is 50MHz and the expected SPI clock is 5MHz, then spi_clk_div should be configured as (50MHz/5MHz)/2 -1 =4=0x04. (This step can be omitted if it has already been configured and you do not want to change the clock frequency of the spi).

Step 2. Read SPI_RW until SPI_RW [31]=0.

Step 3. Configure SPI_RW; if you want to read RTC_MR_10MS, the address of this register in RTC is 0x06, so SPI_RW should be configured as 0x01860000 (spi_start=1, spi_rw=1, spi_add=0x06).

Step 4. Read SPI_RW until SPI_RW [31]=0. Then SPI_RW [15:8] is the readback of RTC_MR_10MS value.

----Finish

3.9.5 RTC register overview

An overview of the RTC registers is shown in Table 3-19 .

Table 3-19 RTC register overview (base address is 0x1209_0000)

offset address	name	describe	page number
0x0000	SPI_CLK_DIV	Clock Rate Value Register for SPI Interface	3-167
0x0004	SPI_RW	SPI interface read and write operation register	3-167
0x0080	CONVER_T	External temperature sensor DS1820 (DS18B20) acquisition control register	3-168
0x0084	CRC_EN	External temperature sensor DS1820 (DS18B20) acquisition CRC check enable control register	3-169
0x0088	INT_MASK	External temperature sensor DS1820 (DS18B20) acquisition interrupt mask register	3-169
0x008C	INT_CLEAR	External temperature sensor DS1820 (DS18B20) acquisition interrupt clear register	3-170
0x0090	BUSY	External temperature sensor DS1820 (DS18B20) acquisition status register	3-170
0x0094	INT_RAW	External temperature sensor DS1820 (DS18B20) collects raw interrupt status register	3-171
0x0098	INT_TCAP	External temperature sensor DS1820 (DS18B20) acquisition interrupt status register	3-171
0x009C	T_VALUE	External temperature sensor DS1820 (DS18B20) acquisition result register	3-172
0x00A0	FILTER_NUM	Glitch filter width configuration register	3-172

Table 3-20 RTC internal register overview (base address is 0x00)

offset address	name	describe	page number
0x00	RTC_10MS_COUNT	RTC 10ms count value register	3-173

offset address	name	describe	page number
0x01	RTC_S_COUNT	RTC Second Count Value Register	3-173
0x02	RTC_M_COUNT	RTC minute counter value register	3-174
0x03	RTC_H_COUNT	RTC Time Count Value Register	3-174
0x04	RTC_D_COUNT_L	Low 8-bit register of RTC day count value	3-175
0x05	RTC_D_COUNT_H	RTC day count value high 8-bit register	3-175
0x06	RTC_MR_10MS	RTC 10ms timer value register	3-176
0x07	RTC_MR_S	RTC Second Timing Value Register	3-176
0x08	RTC_MR_M	RTC minute timer value register	3-177
0x09	RTC_MR_H	RTC Timer Value Register	3-177
0x0A	RTC_MR_D_L	Low 8-bit register of RTC daily value	3-178
0x0B	RTC_MR_D_H	High 8-bit register of RTC day time value	3-178
0x0C	RTC_LR_10MS	RTC 10ms set value register	3-179
0x0D	RTC_LR_S	RTC Second Setting Value Register	3-179
0x0E	RTC_LR_M	RTC minute setting value register	3-180
0x0F	RTC_LR_H	RTC Time Set Value Register	3-180
0x10	RTC_LR_D_L	Low 8-bit register of RTC day setting value	3-181
0x11	RTC_LR_D_H	High 8-bit register of RTC day setting value	3-181
0x12	RTC_LORD	RTC setting value enable load register	3-182
0x13	RTC_IMSC	RTC Interrupt Enable Register	3-183
0x14	RTC_INT_CLR	RTC Interrupt Clear Register	3-183
0x15	RTC_MSC_INT	RTC mask interrupt status register	3-184
0x16	RTC_RAW_INT	RTC Raw Interrupt Status Register	3-185
0x17	RTC_CLK	RTC output clock selection register	3-185
0x18	RTC_POR_N	RTC Reset Control Register	3-186
0x1A	RTC_UV_CTRL	RTC internal low voltage detection control register	3-186
0x51	SDM_COEF_OUSIDE_H	High 4-bit register of external frequency division factor	3-187
0x52	SDM_COEF_OUSIDE_L	Low 8-bit register of external frequency division factor	3-188
0x53	USER_REGISTER1	64bit user use register 1	3-188

offset address	name	describe	page number
0x54	USER_REGISTER2 64bit user	use register 2	3-189
0x55	USER_REGISTER3 64bit user	use register 3	3-189
0x56	USER_REGISTER4 64bit user	use register 4	3-189
0x57	USER_REGISTER5 64bit user	use register 5	3-190
0x58	USER_REGISTER6 64bit user	use register 6	3-190
0x59	USER_REGISTER7 64bit user	register 7	3-190
0x5A	USER_REGISTER8 64bit user	register 8	3-191
0x5F	DDR_SB_CTRL	DDR standby control register	3-191
0x60	DDR_SB_REGISTE R0	128bit DDR standby information register 0	3-192
0x61	DDR_SB_REGISTE R1	128bit DDR standby information register 1	3-192
0x62	DDR_SB_REGISTE R2	128bit DDR standby information register 2	3-192
0x63	DDR_SB_REGISTE R3	128bit DDR standby information register 3	3-193
0x64	DDR_SB_REGISTE R4	128bit DDR standby information register 4	3-193
0x65	DDR_SB_REGISTE R5	128bit DDR standby information register 5	3-193
0x66	DDR_SB_REGISTE R6	128bit DDR standby information register 6	3-194
0x67	DDR_SB_REGISTE R7	128bit DDR standby information register 7	3-194
0x68	DDR_SB_REGISTE R8	128bit DDR standby information register 8	3-194
0x69	DDR_SB_REGISTE R9	128bit DDR standby information register 9	3-195
0x6A	DDR_SB_REGISTE R1	128bit DDR standby information register 10	3-195
0x6B	DDR_SB_REGISTE R11	128bit DDR standby information register 11	3-195
0x6C	DDR_SB_REGISTE R12	128bit DDR standby information register 12	3-196
0x6D	DDR_SB_REGISTE R13	128bit DDR standby information register 13	3-196

offset address	name	describe	page number
0x6E	DDR_SB_REGISTER14	128bit DDR standby information register 14	3-196
0x6F	DDR_SB_REGISTER15	128bit DDR standby information register 15	3-197

3.9.6 RTC register description

SPI_CLK_DIV

SPI_CLK_DIV is the clock rate value register of SPI interface.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	spi_clk_div
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1 1 0 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	spi_clk_div	The clock division factor of the SPI interface. The SPI clock must not exceed 5MHz, and it is recommended to configure it as 5MHz. The value range is 1 to 255. The value of spi_clk_div is used to calculate the clock frequency of SPI transmission and reception, the formula is FSPICLK=FAPBCLK/(2x(spi_clk_div+1)). Where FAPBCLK is the clock frequency of the bus. For example, the bus clock is 50MHz, and the expected SPI clock is 5MHz, then spi_clk_div should be configured as (50MHz/5MHz)/2 -1 =4

SPI_RW

SPI_RW reads and writes registers for the SPI interface.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved												spi_add											spi_rdata								spi_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RO	spi_busy	SPI interface read and write busy status indicator. 0: idle, can start a new SPI read and write operation; 1: Read and write operations are being performed on the SPI interface, and new SPI read and write operations cannot be initiated.
[30:25]	RO	reserved	reserve.
[24]	W1_PULSE	spi_start	Initiates an SPI read and write operation. Write 1 to auto-clear. Writing is invalid when spi_busy is 1. That is, a new SPI operation will not be started until the last read and write operation is completed. If it is started, the hardware will ignore this start request.
[23]	RW	spi_rw	Type of SPI operation. 0: write operation; 1: Read operation.
[22:16]	RW	spi_add	Address for SPI operations. The value range is 0~127.
[15:8]	RO	spi_rdata	The data read back by the SPI interface.
[7:0]	RW	spi_wdata	Data to be written to the SPI interface.

CONVER_T

CONVER_T is the acquisition control register for the external temperature sensor DS1820 (DS18B20).

Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	conver_t	External temperature sensor DS1820 (DS18B20) acquisition control register start. Must be set to 1. 1: start, the hardware will automatically reset to zero when the interrupt is cleared.

CRC_EN

CRC_EN is the external temperature sensor DS1820 (DS18B20) acquisition CRC check enable control register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	crc_en	The external temperature sensor DS1820 (DS18B20) collects the CRC check enable control register. 0: forbidden; 1: enable.

INT_MASK

INT_MASK is the acquisition interrupt mask register for the external temperature sensor DS1820 (DS18B20).

Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	int_mask	External temperature sensor DS1820 (DS18B20) acquisition interrupt mask register. 0: no shielding; 1: Shielded.

INT_CLEAR

INT_CLEAR is the external temperature sensor DS1820 (DS18B20) acquisition interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	int_clear	External temperature sensor DS1820 (DS18B20) acquisition interrupt clear register. Write 1 to clear interrupt. Hardware will automatically reset to zero after the interrupt is cleared.

BUSY

BUSY is the acquisition status register of the external temperature sensor DS1820 (DS18B20).

Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1] RO		reserved	reserve
[0]	RO	busy	The external temperature sensor DS1820 (DS18B20) collects the status. 0ÿreadyÿ 1ÿbusyÿ

INT_RAW

INT_RAW collects the raw interrupt status register for the external temperature sensor DS1820 (DS18B20).

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2] RO		reserved	reserve.
[1]	RO	int_err	Error interrupt register.
[0]	RO	get_tmprt_int The external temperature sensor DS1820 (DS18B20) is interrupted when the acquisition is completed.	

INT_TCAP

INT_TCAP is the external temperature sensor DS1820 (DS18B20) acquisition interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_tcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1] RO		reserved	reserve.
[0]	RO	int_tcap	Masked interrupt status. 0: no interrupt; 1: There is an interrupt.

T_VALUE

T_VALUE is the acquisition result register of the external temperature sensor DS1820 (DS18B20).

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														t_value	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:12] RO		reserved	reserve.
[11:0] RO		t_value	The external temperature sensor DS1820 (DS18B20) collects the results.

FILTER_NUM

FILTER_NUM Filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														filter_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	filter_num	Select the input glitch width to filter out N+1 APB clock width glitches.

3.9.7 RTC internal register description

RTC_10MS_COUNT

RTC_10MS_COUNT is the RTC 10ms count value register.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	—	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7]	RO	reserved	reserve
[6:0]	RO	rtc_10ms_count	RTC 10ms counter value, indicating the number of 10ms time currently counted. The value range is 0-99.

RTC_S_COUNT

RTC_S_COUNT is the RTC second count value register.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	—			rtc_s_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5:0]	RO	rtc_s_count	RTC second counter value, indicating the number of seconds currently counted. The value range is 0-59.

RTC_M_COUNT

RTC_M_COUNT is the RTC minute counter value register.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	—			rtc_m_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5:0]	RO	rtc_m_count	RTC minute counter value, indicating the number of minute time currently counted. Take the range of 0ÿ59ÿ

RTC_H_COUNT

RTC_H_COUNT is the RTC hour counter value register.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	-----			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	reserve
[4:0]	RO	rtc_h_count	RTC hour counter value, indicating the number of hours currently counted. The range is 0-23.

RTC_D_COUNT_L

RTC_D_COUNT_L is the low 8-bit register of the RTC day count value.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	The lower 8 bits of the RTC day counter value cooperate with RTC_D_COUNT_H to indicate the number of days currently counted, and the value range is 0 to 65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is the high 8-bit register of the RTC day count value.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RO	rtc_d_count_h	The upper 8 bits of the RTC day counter value cooperate with RTC_D_COUNT_L to indicate the number of days currently counted, and the value range is 0 to 65535.

RTC_MR_10MS

RTC_MR_10MS is RTC 10ms timer value register.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access Name		Description
[7]	RW	reserved	reserve.
[6:0]	RW	rtc_mr_10ms	RTC 10ms timing value, indicating the timing value of 10ms. The value range is 0~99.

RTC_MR_S

RTC_MR_S is RTC second timing value register.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	—		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5:0]	RW	rtc_mr_s	RTC second timing value, which indicates the timing second time value. The value range is 0-59.

RTC_MR_M

RTC_MR_M is RTC minute value register.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	—		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve
[5:0]	RW	rtc_mr_m	RTC sub-timer value, indicating the sub-time value of timing. The value range is 0-59.

RTC_MR_H

RTC_MR_H is the timer value register for RTC.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	-----			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RO	reserved	reserve
[4:0]	RW	rtc_mr_h	RTC hourly timer value, indicating the hourly time value of the timer. The value range is 0~23.

RTC_MR_D_L

RTC_MR_D_L is the lower 8-bit register of RTC daily value.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	The lower 8 bits of the RTC day timer value, cooperate with RTC_MR_D_H to indicate the timer day time value, and the value range is 0~65535.

RTC_MR_D_H

RTC_MR_D_H is the high 8-bit register of RTC daily value.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access Name		Description
[7:0]	RW	rtc_mr_d_h	The high 8 bits of the RTC day value, cooperate with RTC_MR_D_L, to indicate the time value of the day, and the value range is 0~65535.

RTC_LR_10MS

RTC_LR_10MS Set value register for RTC 10ms.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	-----	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7]	RO	reserved	reserve.
[6:0]	RW	rtc_lr_10ms	RTC 10ms setting value, indicating the set 10ms time value. The value range is 0-99.

RTC_LR_S

RTC_LR_S Set value register for RTC seconds.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	—			rtc_lr_s				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve
[5:0]	RW	rtc_lr_s	RTC second setting value, indicating the set second time value. The value range is 0-59.

RTC_LR_M

RTC_LR_M is the RTC minute set value register.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	—			rtc_lr_m				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5:0]	RW	rtc_lr_m	RTC minute setting value, indicating the set minute time value. The value range is 0-59.

RTC_LR_H

RTC_LR_H Set value register for RTC.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	-----			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:5]	RO reserved	reserve.
[4:0]	RW rtc_lr_h	RTC hour setting value, indicating the set hour time value. The value range is 0-23.

RTC_LR_D_L

RTC_LR_D_L is the lower 8-bit register of RTC day setting value.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW rtc_lr_d_l	The lower 8 bits of the RTC day setting value, cooperate with RTC_LR_D_H to indicate the set day time, and the value range is 0~65535.

RTC_LR_D_H

RTC_LR_D_H is the high 8-bit register of RTC day setting value.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW rtc_lr_d_h	The high 8 digits of the RTC day setting value, cooperate with RTC_LR_D_L to indicate the set day time, and the value range is 0~65535.

RTC_LORD

RTC_LORD Enable load register for RTC setting value.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:3]	RO reserved	reserve
[2]	RW rtc_lock_bypass	RTC time latch enable signal. 0: Enable, the RTC count value (0x00~0x05) will only be updated after the latch is successful. 1: Disabled, the RTC count value (0x00~0x05) is updated in real time.
[1]	RW rtc_lock	RTC time latch signal. After the software writes 1, the hardware will automatically clear it to 0 after the latch is successful. Note: This register is only valid when rtc_lock_bypass is 0.
[0]	RW rtc_load	Enable signal to write the RTC time configuration value into the RTC accumulator. After the software writes 1, the hardware will automatically clear to 0 after the loading is successful.

RTC_IMSC

RTC_IMSC is the RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:3]	RO reserved	reserve.
[2]	RW rtc_imsc	RTC total interrupt output enable bit. 0: no output interrupt; 1: Output interrupted.
[1]	RW rtc_imsc_uv	Battery low voltage detection interrupt output enable bit. 0: Do not output interrupt; 1: Output interrupt.
[0]	RW rtc_imsc_time	RTC timing interrupt output enable bit. 0: no output interrupt; 1: Output interrupted.

RTC_INT_CLR

RTC_INT_CLR is the RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:1]	RO	reserved	reserve.
[0]	WO	rtc_int_clr	RTC interrupt clear register, software can write any value to clear the interrupt, reading back is meaningless.

RTC_MSC_INT

RTC_MSC_INT is RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:2]	RO	reserved	reserve.
[1]	RO	mask_int_uv	Masked low battery detection interrupt status register. 0: no interrupt; 1: There is an interrupt.
[0]	RO	mask_int_time	Masked RTC timer interrupt status register. 0: no interrupt; 1: There is an interrupt.

RTC_RAW_INT

RTC_RAW_INT is RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						---	---
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:2]	RO	reserved	reserve.
[1]	RO	raw_int_uv	Low battery detection raw interrupt status register. 0: no interrupt; 1: There is an interrupt.
[0]	RO	raw_int_time	RTC timing raw interrupt status register. 0: no interrupt; 1: There is an interrupt.

RTC_CLK

RTC_CLK is the RTC output clock selection register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	reserve.
[1:0]	RW	clk_out_sel	Test clock selection for RTC output. 00: Output crystal oscillator clock; 01: output corrected 100Hz clock; 1X: Output 1Hz clock.

RTC_POR_N

RTC_POR_N is the RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	RO	reserved	reserve.
[0]	RW	rtc_por_n	Reset signal for RTC module. Set to 1 automatically after successful reset. 0: Reset.

RTC_UV_CTRL

RTC_UV_CTRL is RTC internal low voltage detection control register.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_UV_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name								
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5]	RW	bat_uv_ctrl_en	Low voltage detection enable control. 0: off; 1: open.
[4]	RW	bat_uv_ctrl_sel	Low voltage detection source selection. 0: No filter processing; 1: Filtered.
[3:2]	RO	reserved	reserve.
[1:0]	RW	sample_time	Low voltage detection cycle. 00: 1 second; 01: 1 minute; 10: 10 minutes; 11:30 minutes.

SDM_COEF_OUSIDE_H

SDM_COEF_OUSIDE_H is the high 4-bit register of the external frequency division coefficient.

Offset Address	Register Name	Total Reset Value
0x51	SDM_COEF_OUSIDE_H	0x08

Bit	7	6	5	4	3	2	1	0
Name	reserved				sdm_coef_ouside_h			
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	reserve.
[3:0]	RW	sdm_coef_ouside_h	Higher 4 bits of frequency division coefficient in fixed frequency division mode.

SDM_COEF_OUSIDE_L

SDM_COEF_OUSIDE_L is the lower 8-bit register of the external frequency division coefficient.

Offset Address	Register Name	Total Reset Value
0x52	SDM_COEF_OUSIDE_L	0x1B

Bit	7	6	5	4	3	2	1	0
Name	sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	sdm_coef_ouside_l	The lower 8 bits of the frequency division factor in the fixed frequency division mode. Note: When reading/writing the frequency division coefficient registers (0x51, 0x52), you should first read/write the high 4 bits and then read/write the low 8 bits, and the continuous operation from the high bit to the low bit is required. Complete read/write operation. The calculation formula of this register is (f 32700)*30.52 (32700=<f<=32799, f is the oscillation frequency of the external crystal).

USER_REGISTER1

USER_REGISTER1 uses register 1 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x53	USER_REGISTER1	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register1	64bit users use register 1, which corresponds to bit[7:0].

USER_REGISTER2

USER_REGISTER2 uses register 2 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x54	USER_REGISTER2	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register2	64bit users use register 2, which corresponds to bit[15:8].

USER_REGISTER3

USER_REGISTER3 uses register 3 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x55	USER_REGISTER3	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register3	64bit users use register 3, which corresponds to bit[23:16].

USER_REGISTER4

USER_REGISTER4 uses register 4 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x56	USER_REGISTER4	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register4	64bit users use register 4, which corresponds to bit[31:24].

USER_REGISTER5

USER_REGISTER5 Use register 5 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x57	USER_REGISTER5	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register5	64bit users use register 5, which corresponds to bit[39:32].

USER_REGISTER6

USER_REGISTER6 Use register 6 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x58	USER_REGISTER6	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register6	64bit users use register 6, which corresponds to bit[47:40].

USER_REGISTER7

USER_REGISTER7 Use register 7 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x59	USER_REGISTER7	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	user_register7	64bit users use register 7, which corresponds to bit[55:48].

USER_REGISTER8

USER_REGISTER8 Use register 8 for 64bit users.

Offset Address	Register Name	Total Reset Value
0x5A	USER_REGISTER8	0x00

Bit	7	6	5	4	3	2	1	0
Name	user_register8							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW user_register8	64bit users use register 8, which corresponds to bit[63:56].

DDR_SB_CTRL

DDR_SB_CTRL is the DDR standby control register.

Offset Address	Register Name	Total Reset Value
0x5F	DDR_SB_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:2]	RO reserved	reserve.
[1]	RW ddr_ioctrl_lhen	ddr io latch enable control. 0: disable; 1: enable.
[0]	RW ddrc_ctrl_iso	ddrc System reset isolation control. 0: Can be reset; 1: Cannot be reset.

DDR_SB_REGISTER0

DDR_SB_REGISTER0 is 128bit DDR standby information register 0.

Offset Address	Register Name	Total Reset Value
0x60	DDR_SB_REGISTER0	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register0							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register0	128bitDDR standby information register 0, corresponding to bit[7:0].

DDR_SB_REGISTER1

DDR_SB_REGISTER1 is 128bit DDR standby information register 1.

Offset Address	Register Name	Total Reset Value
0x61	DDR_SB_REGISTER1	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register1	128bitDDR standby information register 1, corresponding to bit[15:8].

DDR_SB_REGISTER2

DDR_SB_REGISTER2 is 128bit DDR standby information register 2.

Offset Address	Register Name	Total Reset Value
0x62	DDR_SB_REGISTER2	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register2	128bitDDR standby information register 2, corresponding to bit[23:16].

DDR_SB_REGISTER3

DDR_SB_REGISTER3 is 128bit DDR standby information register 3.

Offset Address	Register Name	Total Reset Value
0x63	DDR_SB_REGISTER3	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register3 128bitDDR standby information register 3, corresponding to bit[31:24].

DDR_SB_REGISTER4

DDR_SB_REGISTER4 is 128bit DDR standby information register 4.

Offset Address	Register Name	Total Reset Value
0x64	DDR_SB_REGISTER4	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register4 128bitDDR standby information register 4, corresponding to bit[39:32].

DDR_SB_REGISTER5

DDR_SB_REGISTER5 is 128bit DDR standby information register 5.

Offset Address	Register Name	Total Reset Value
0x65	DDR_SB_REGISTER5	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register5 128bitDDR standby information register 5, corresponding to bit[47:40].

DDR_SB_REGISTER6

DDR_SB_REGISTER6 is 128bit DDR standby information register 6.

Offset Address	Register Name	Total Reset Value
0x66	DDR_SB_REGISTER6	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register6	128bitDDR standby information register 6, corresponding to bit[55:48].

DDR_SB_REGISTER7

DDR_SB_REGISTER7 is 128bit DDR standby information register 7.

Offset Address	Register Name	Total Reset Value
0x67	DDR_SB_REGISTER7	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register7	128bitDDR standby information register 7, corresponding to bit[63:56].

DDR_SB_REGISTER8

DDR_SB_REGISTER8 is 128bit DDR standby information register 8.

Offset Address	Register Name	Total Reset Value
0x68	DDR_SB_REGISTER8	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register8							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register8	128bitDDR standby information register 8, corresponding to bit[71:64].

DDR_SB_REGISTER9

DDR_SB_REGISTER9 is 128bit DDR standby information register 9.

Offset Address	Register Name	Total Reset Value
0x69	DDR_SB_REGISTER9	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register9							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register9 128bitDDR standby information register 9, corresponding to bit[79:72].

DDR_SB_REGISTER10

DDR_SB_REGISTER10 is 128bit DDR standby information register 10.

Offset Address	Register Name	Total Reset Value
0x6A	DDR_SB_REGISTER10	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register10							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register10 128bitDDR standby information register 10, corresponding to bit[87:80].

DDR_SB_REGISTER11

DDR_SB_REGISTER11 is 128bit DDR standby information register 11.

Offset Address	Register Name	Total Reset Value
0x6B	DDR_SB_REGISTER11	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register11							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW	ddr_sb_register11 128bitDDR standby information register 11, corresponding to bit[95:88].

DDR_SB_REGISTER12

DDR_SB_REGISTER12 is 128bit DDR standby information register 12.

Offset Address	Register Name	Total Reset Value
0x6C	DDR_SB_REGISTER12	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register12							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register12	128bitDDR standby information register 12, corresponding to bit[103:96].

DDR_SB_REGISTER13

DDR_SB_REGISTER13 is 128bit DDR standby information register 13.

Offset Address	Register Name	Total Reset Value
0x6D	DDR_SB_REGISTER13	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register13							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register13	128bitDDR standby information register 13, corresponding to bit[111:104].

DDR_SB_REGISTER14

DDR_SB_REGISTER14 is 128bit DDR standby information register 14.

Offset Address	Register Name	Total Reset Value
0x6E	DDR_SB_REGISTER14	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register14							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:0]	RW ddr_sb_register14	128bitDDR standby information register 14, corresponding to bit[119:112].

DDR_SB_REGISTER15

DDR_SB_REGISTER15 is 128bit DDR standby information register 15.

Offset Address	Register Name	Total Reset Value
0x6F	DDR_SB_REGISTER15	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register15							
Reset	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[7:0]	RW	ddr_sb_register15 128bit	DDR standby information register 15, corresponding to bit[127:120].

3.10 Power Management and Low Power Mode Control

3.10.1 Overview

The low power consumption mode of the chip is used to effectively reduce the power consumption of the chip. The chip provides a variety of low power consumption controls to dynamically reduce the power consumption of the chip.

Clock gating and clock frequency adjustment

provide a clock shutdown function, which can shut down unnecessary clocks and reduce power consumption of the chip. The clock frequency of the system can be adjusted, and the clock frequency can be adjusted to reduce the power consumption of the chip when the function is satisfied. Module-level low-power

control provides module-level low-power control. When a module is not working, turn off the module or put the module in a low-power state to reduce chip power consumption.

DDR Low Power Control

The DDR controller and related pins have a dynamic power consumption control function. You can choose to enable this function to reduce chip power consumption, and you can also enable the DDR self-refresh mode to reduce the power consumption of the entire product.

DVFS (Dynamic Frequency and Voltage Regulation) function based on A17 CPU load monitoring.

3.10.2 Clock Gating and Clock Frequency Adjustment

The system provides the clock gating function of each module. When the module is idle, the corresponding clock can be turned off to reduce the power consumption of the chip. For the operation process, please refer to the clock gating part of each module.

The system can reduce chip power consumption by adjusting the operating frequency, as follows:

Close the service module so that it does not access DDR.

The system switches to run in on-chip memory.

Configure DDRC_CTRL_SREF[sref_seq] as a valid value, DDRC will control DDRn SDRAM to enter self-refresh mode.

Step 1. Configure PERI_CRG13 to select the clock source of system bus, DDRC and CPU.

Step 2. According to the configuration requirements of DDRC, after waiting for a certain period of time, configure DDRC_CTRL_SREF to exit self-refresh new, for normal operation.

Step 3. The program jumps to run in DDR.

----Finish

In addition to the adjustment of the system operating frequency, the operating frequency of some modules can also be adjusted independently. Adjusting the operating frequency of these modules can also further reduce the power consumption of the system. For details, refer to the section on clock source selection for each module in "3.2.3 Clock Resource Distribution" .

3.10.3 Module level low power consumption control

PHY modules such as USB 2.0 Host/Device, USB 3.0 Host/Device, PCIe, Video DAC, and PLL in the chip can provide low-power working modes. (Refer to the register description of the system controller, clock, etc.)

Low power consumption control of USB 2.0 Host/Device module If

the USB2.0 function is not used, the PERI_CRG45 bit[7] can be configured as 0, and the clock of the USB 2.0 PHY can be turned off.

Low power consumption control of USB 3.0 Host/Device & PCIe module If the

USB3.0 function is not used, the corresponding clock gating signal of PERI_CRG46 can be configured to turn off the corresponding clock of USB3.0 CTRL. If the PCIe function is

not used, the corresponding clock gating signal of PERI_CRG44 can be configured to turn off the corresponding clock of PCIe CTRL.

If the USB3.0 and PCIe functions are not used at the same time, the corresponding clock gating signal of PERI_CRG43 can be configured to turn off the corresponding clock of COMB PHY.

Video DAC Low Power Control

If the Video DAC function is not used, the CVBS channel can be turned off to reduce power consumption. For details, refer to the VDP chapter.

The PLL provides the function of low power consumption. If the PLL is not used, the PLL can be turned off to make the system in a low power consumption state. Please refer to the description of the PERI_CRG_PLL0~PLL9 Power Down control bits in the CRG register.

3.10.4 DDR Low Power Control

For details about DDRC low power consumption control, please refer to "Low Power Consumption Configuration" in "DDRC Working Mode".

3.10.5 DVFS and AVS function description

DVFS (Dynamic voltage and frequency scaling) dynamically sets different frequencies and voltage levels according to different operating scenarios to meet the timing and performance requirements of the current circuit. The system can set the operating frequency and operating voltage of the CPU according to the application scenario.

AVS (Added voltage scaling) is based on DVFS, according to the chip process, temperature, circuit timing, real-time dynamic adjustment of voltage to further reduce power consumption. The system can obtain the PVT information of the chip through the PMC module

information, and automatically adjust the voltage through the PWM output signal in the PMC, please refer to chapter 3.11 “PMC” for details.

3.11 PMC

3.11.1 Functional description

PMC (Power manage control) provides basic information and control of chip power management, mainly including the following items.

PWM output

PMC contains a programmable PWM module, and the peripheral PWM voltage regulation circuit can adjust the power supply voltage of the chip through the PWM output of the chip. Hi3519V100 provides 4 PWM outputs.

The HPM control

obtains the PVT comprehensive information of the current chip through the HPM, and generates decision-making references for chip power supply voltage adjustment based on the information.

Hardware AVS Control

After the hardware AVS is enabled, the chip acquires the HPM value regularly, and adjusts the duty cycle of the PWM output according to the configured relevant strategies to realize the self-adaptive power supply voltage adjustment of the chip.

Chip internal temperature detection

The chip integrates a temperature sensor, which is used to obtain the internal temperature of the chip, and provides temperature information for the temperature protection processing of the chip.

CPU A17 power on and off control Provide

CPU A17 power switch control registers and related logic for A17 power on and off control.

3.11.2 Working method

PWM output

The working clock of the PWM module in the PMC is 24MHz, and the period and duty ratio counters are 16bits. by configuration
The PWM-related registers in the PMC can realize PWM output with specified period and duty cycle.

The steps to configure PWM output are:

Step 1. According to the required PWM output frequency and duty cycle, calculate the corresponding number of PWM counting cycles and high level counting value.

The formula for calculating the number of counting cycles is:

pwm_ period = (24000000/ Freq) ÿ1

The formula for calculating the high level count value is:

pwm_ duty = (24000000/ Freq)*duty ÿ1

Step 2. Configure the PWM count period and high level count value registers.

Step 3. Enable the PWM output.

----Finish

For example, the voltage regulation control of the chip CORE power supply is controlled by the PWM0 signal, if the PWM0 output frequency is required to be 200KHz, the duty cycle is 75%, the configuration steps are as follows:

Step 1. Calculate the required number of calculation cycles and high count value:

pwm_period=(24000000/200000)-1 = 119

pwm_duty=(24000000/200000)*0.75-1=89

Step 2. Set CORE PWM parameters: set PERI_PMC0[15:0]=0x77, PERI_PMC0[31:16]=0x59;

Step 3. Enable the corresponding PWM of CORE: Set PERI_PMC4[0]=1.

----Finish

HPM control

Only 4 HPMs are placed in the chip to obtain PVT information of CORE, MDDRC, CPU A17 and MEDIA modules.

The reference clock source clock of HPM is 200MHz (the HPM working clock of A17 is the working clock of A17), in order to make the value of HPM more accurate, it is recommended to configure core_hpm_div as 0x3, so that the reference clock of HPM is close to 50MHz ÿ

Taking obtaining the CORE HPM monitoring value as an example, the HPM monitoring enabling configuration process is as follows:

Step 1. Set the HPM acquisition mode.

There are two modes of HPM acquisition: single acquisition mode and loop acquisition mode. Please refer to the description in the PERI_PMC10 register.

In the cyclic collection mode, the collection period needs to be set, and the collection period is: T = (N*2048+M*16)/1000 ms (N= PERI_PMC13 [31:24], M= PERI_PMC31[7:0]).

Step 2. Configure core_hpm_div as 0x3, cancel reset, and start HPM acquisition.

First configure PERI_PMC10 to 0x04000003, and then configure PERI_PMC10 to 0x05000003. Start the HPM cycle acquisition mode.

Step 3. After waiting for core_hpm_pc_valid to be 1, the software reads the monitoring value of HPM.

Step 4. In single-shot acquisition mode, only HPM raw pattern 0 recorded in PERI_PMC11[9:0] is valid.

In cyclic acquisition mode, PERI_PMC11 [9:0], PERI_PMC11 [21:12], PERI_PMC12 [9:0] and PERI_PMC12 [21:12] record the last four HPM original code patterns 0~3, the latest recorded value is HPM original pattern 0.

----Finish

Hardware AVS

Through the hardware AVS function in the PMC, the chip can automatically adjust the PWM output duty cycle according to the HPM monitoring value, thereby realizing automatic power supply voltage adjustment.

The chip supports HPM hardware AVS of CORE, MDDRC, CPU A17 and MEDIA. Taking CORE as an example, the hardware AVS startup process is as follows:

Step 1. Configure PERI_PMC5 [2:1] to set the calculation mode of hardware AVS.

Step 2. Configure PERI_PMC5 [31:16] to set the buck-boost step of hardware AVS.

Step 3. Set PERI_PMC5 [0] to 1 to enable hardware AVS.

----Finish

Chip internal temperature detection

The temperature sensor is integrated inside the chip, and the temperature detection range is -40~125°C. The process of enabling temperature sensor data collection is as follows:

Step 1. Set Tsensor acquisition mode.

There are two modes for Tsensor acquisition temperature: single acquisition mode and cyclic acquisition mode. Please refer to the description in the PERI_PMC68 register.

In the cyclic acquisition mode, the acquisition period needs to be set, and the acquisition period is (tsensor_monitor_period*2) ms.

Step 2. Enable Tsensor and start temperature collection.

Step 3. The software reads the temperature code collected by Tsensor.

In single acquisition mode, only temperature record code 0 recorded in PERI_PMC70 [9:0] is valid.

In the cyclic collection mode, PERI_PMC70~PERI_PMC73 have recorded the last eight temperature record codes 0~7, and the latest temperature record value is temperature record code 0.

Step 4. Calculate the corresponding temperature value according to the temperature record code.

Calculation formula: T = [(tsensor_temp_code -125)/806]*165-40 (°C).

Note: tsensor_temp_code value range: [125,931]

----Finish

CPU A17 power on and off control

A17 power off process:

Step 1. Set mode_onoff in PERI_PMC79 to 0x2 to enable manual A17 power on and off mode. configuration

When MISC_CTRL1 [30] is 0, the coresight debugging function of A17 is turned off.

Step 2. Read PERI_PMC77 [8:7] as 0x3, wait for the STANDBYWFI and STANDBYWFIL2 output of A17

Both signals are valid (active high).

Step 3. Read PERI_PMC77[4:3] as 0x0, wait for the idle indication signal cactives/cactivem output signal of A17 ADB asynchronous bridge to be valid (active low).

Step 4. Configure PERI_PMC77 [5] to 0 to make A17 ADB bridge enter low power consumption mode.

Step 5. Read PERI_PMC77 [6] as 0, wait for A17 ADB bridge to enter low power mode.

Step 6. Set PERI_PMC77 [0] to 1 to enable A17 output isolation.

Step 7. Set the CRG register PERI_CRG10[19] to 1 to make the global soft reset of A17 take effect.

Step 8. Set the CRG register PERI_CRG10[21] to 0, and turn off A17 and A17 ADB MST clock.

Step 9. Set PERI_PMC77[1] to 1 to enable A17 MTCMOS to be powered off.

Step 10. Read PERI_PMC77[2] as 1, and wait for power-off to complete.

----Finish

A17 power-on process:

Step 11. Set MISC_CTRL1 [30] to 1 to enable the coresight debugging function of A17.

Step 12. Configure the mode_onoff in PERI_PMC79 to 0x2, and enable the A17 power on and off mode.

Step 13. Set the CRG register PERI_CRG10[21] to 1, and output the clock to A17.

Step 14. Set PERI_PMC77[1] to 0 to enable A17 MTCMOS to power on.

Step 15. Read PERI_PMC77[2] as 0, and wait for the power-on to complete.

Step 16. Set PERI_PMC77 [0] to 0 to release A17 output isolation.

Step 17. Set the CRG register PERI_CRG10[19] to 0 to release the overall reset of A17 (except A17 core).

Step 18. Configure PERI_PMC77 [5] to 1 to make A17 ADB bridge exit low power mode.

Step 19. Read PERI_PMC77 [6] as 1, wait for A17 ADB bridge to exit low power mode.

Configure the CRG register PERI_CRG10[1] as 0 to release the A17 core reset.

----Finish

3.11.3 PMC register overview

An overview of the PMC registers is shown in Table 3-21 .

Table 3-21 PMC register overview (base address is 0x120A_0000)

offset address	name	describe	page number
0x0000	PERI_PMC0	PERI_PMC0 Register	3-204
0x0004	PERI_PMC1	PERI_PMC1 Register	3-204
0x0008	PERI_PMC2	PERI_PMC2 Register	3-205
0x000c	PERI_PMC3	PERI_PMC3 Register	3-205
0x0010	PERI_PMC4	PERI_PMC4 Register	3-205
0x0014	PERI_PMC5	PERI_PMC5 Register	3-207
0x0018	PERI_PMC6	PERI_PMC6 Register	3-208

offset address	name	describe	page number
0x001c	PERI_PMC7	PERI_PMC7 Register	3-209
0x0020	PERI_PMC8	PERI_PMC8 Register	3-210
0x0028	PERI_PMC10	CORE HPM Control Register 0	3-211
0x002C	PERI_PMC11	CORE HPM Status Register 1	3-212
0x0030	PERI_PMC12	CORE HPM Status Register 2	3-213
0x0034	PERI_PMC13	CORE HPM Control Register 3	3-214
0x0038	PERI_PMC14	A17 HPM Control Register 0	3-215
0x003C	PERI_PMC15	A17 HPM status register 1	3-216
0x0040	PERI_PMC16	A17 HPM status register 2	3-216
0x0044	PERI_PMC17	A17 HPM Control Register 3	3-217
0x0048	PERI_PMC18	DDR HPM Control Register 0	3-218
0x004C	PERI_PMC19	DDR HPM Status Register 1	3-219
0x0050	PERI_PMC20	DDR HPM Status Register 2	3-219
0x0054	PERI_PMC21	DDR HPM Control Register 3	3-220
0x0058	PERI_PMC22	MDA0 HPM Control Register 0	3-221
0x005C	PERI_PMC23	MDA0 HPM Status Register 1	3-222
0x0060	PERI_PMC24	MDA0 HPM Status Register 2	3-223
0x0064	PERI_PMC25	MDA0 HPM Control Register 3	3-223
0x0078	PERI_PMC30	HPM Loop Monitor Trim Control Register 1	3-224
0x007C	PERI_PMC31	HPM Loop Monitor Trim Control Register 2	3-224
0x110	PERI_PMC68	PERI_PMC68 Register	3-225
0x0114	PERI_PMC69	PERI_PMC69 Register	3-225
0x0118	PERI_PMC70	PERI_PMC70 Register	3-226
0x011C	PERI_PMC71	PERI_PMC71 Register	3-226
0x0120	PERI_PMC72	PERI_PMC72 Register	3-227
0x0124	PERI_PMC73	PERI_PMC73 Register	3-227
0x0128	PERI_PMC74	PERI_PMC74 Register	3-228
0x0134	PERI_PMC77	PERI_PMC77 Register	3-229
0x0138	PERI_PMC78	PERI_PMC78 Register	3-230

offset address	name	describe	page number
0x013C	PERI_PMC79	PERI_PMC79 Register	3-232

3.11.4 PMC register description

PERI_PMC0

PERI_PMC0 is the PERI_PMC0 register.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_PMC0	0x0012_0078

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	core_pwm_duty	core_pwm_period
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0

Bits	Access	Name	Description
[31:16]	RW	core_pwm_duty	If the high-level pulse number of PWM output by CORE AVS is greater than or equal to the cycle number, the output will always be high-level. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.
[15:0]	RW	core_pwm_period	The number of PWM cycles for CORE AVS output. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.

PERI_PMC1

PERI_PMC1 is the PERI_PMC1 register.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_PMC1	0x0012_0078

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	a17_pwm_duty	a17_pwm_period
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0

Bits	Access	Name	Description
[31:16]	RW	a17_pwm_duty	A17 The high-level pulse number of PWM output by AVS, if it is greater than or equal to the cycle number, the output will always be high-level. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.
[15:0]	RW	a17_pwm_period	A17 AVS output PWM period. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.

PERI_PMC2

PERI_PMC2 is the PERI_PMC2 register.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_PMC2	0x0012_0078

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ddr_pwm_duty	ddr_pwm_period
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0

Bits	Access	Name	Description
[31:16]	RW	ddr_pwm_duty	If the high-level pulse number of PWM output by DDR AVS is greater than or equal to the cycle number, the output will always be high-level. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.
[15:0]	RW	ddr_pwm_period	DDR AVS output PWM period. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.

PERI_PMC3

PERI_PMC3 is the PERI_PMC3 register.

Offset Address	Register Name	Total Reset Value
0x000c	PERI_PMC3	0x0012_0078

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mda0_pwm_duty	mda0_pwm_period
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0

Bits	Access	Name	Description
[31:16]	RW	mda0_pwm_duty	MDA0 AVS output PWM high-level beats, if greater than or equal to the number of cycles, the output is always high. Cannot be configured as 0, when configured as 0, the actual effective value is 1. That is, the effective value is the configuration value plus 1.
[15:0]	RW	mda0_pwm_period	When mda0_pwm_period is 0, the MDA0 AVS output PWM period. Cannot be configured as 0, when configuring effective value is 1. That is, the effective value is the configuration value plus 1.

PERI_PMC4

PERI_PMC4 is the PERI_PMC4 register.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_PMC4	0x0000_E400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve
[15:14]	RW	pwm3_reuse_cfg	AVS output PWM3 source selection. 00ÿCOREÿ 01ÿA17ÿ 10ÿDDRÿ 11ÿMDA0ÿ
[13:12]	RW	pwm2_reuse_cfg	AVS output PWM2 source selection. 00ÿCOREÿ 01ÿA17ÿ 10ÿDDRÿ 11ÿMDA0ÿ
[11:10]	RW	pwm1_reuse_cfg	AVS output PWM1 source selection. 00ÿCOREÿ 01ÿA17ÿ 10ÿDDRÿ 11ÿMDA0ÿ
[9:8]	RW	pwm0_reuse_cfg	AVS output PWM0 source selection. 00ÿCOREÿ 01ÿA17ÿ 10ÿDDRÿ 11ÿMDA0ÿ
[7]	RW	mda0_pwm_inv	PWM positive and negative phase control of MDA0 AVS output. 0: normal output; 1: Inverted output.

[6] RW mda0_pwm_enable	PWM enable control for MDA0 AVS output. 0: off; 1: open.
[5] RW ddr_pwm_inv	PWM positive and negative phase control of DDR AVS output. 0: normal output; 1: Inverted output.
[4] RW ddr_pwm_enable	PWM enable control for DDR AVS output. 0: off; 1: open.
[3] RW a17_pwm_inv	A17 AVS output PWM positive and negative phase control. 0: normal output; 1: Inverted output.
[2] RW a17_pwm_enable	A17 PWM enable control for AVS output. 0: off; 1: open.
[1] RW core_pwm_inv	PWM positive and negative phase control of CORE AVS output. 0: normal output; 1: Inverted output.
[0] RW core_pwm_enable	PWM enable control for CORE AVS output. 0: off; 1: open.

PERI_PMC5

PERI_PMC5 is the PERI_PMC5 register.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_PMC5	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	core_avs_fsm_inc_pwm_step	core_avs_fsm_dec_pwm_step	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	core_avs_fsm_inc_pwm_step	CORE AVS FSM PWM self-increasing stepping.
[23:16]	RW	core_avs_fsm_dec_pwm_step	CORE AVS FSM PWM auto-decrement step.
[15:3]	RO	reserved	reserve
[2:1]	RW	core_avs_hpm_fsm_samples_calc_mode	CORE AVS HPM FSM calculation mode. 00: average of 4 samples; 01: average of 8 samples; 10: average of 16 samples; 11: average of 32 samples.
[0]	RW	core_hpm_fsm_en	CORE AVS HPM FSM enable control. 0: off; 1: open.

PERI_PMC6

PERI_PMC6 is the PERI_PMC6 register.

Offset Address	Register Name	Total Reset Value
0x0018	PERI_PMC6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_avs_fsm_inc_pwm_step								a17_avs_fsm_dec_pwm_step								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	a17_avs_fsm_inc_pwm_step	A17 AVS FSM PWM self-increasing stepping.
[23:16]	RW	a17_avs_fsm_dec_pwm_step	A17 AVS FSM PWM auto-decrement step.
[15:3]	RO	reserved	reserve
[2:1]	RW	a17_avs_hpm_fsm_calc_mode	A17 AVS HPM FSM calculation mode. 00: average of 4 01: average of 8 10: average of 16 samples; 11: average of 32 samples.
[0]	RW	a17_hpm_fsm_en	A17 AVS HPM FSM enable control. 0: off; 1: open.

PERI_PMC7

PERI_PMC7 is the PERI_PMC7 register.

Offset Address	Register Name	Total Reset Value
0x001c	PERI_PMC7	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ddr_avs_fsm_inc_pwm_step	ddr_avs_fsm_dec_pwm_step	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	ddr_avs_fsm_inc_pwm_step	DDR AVS FSM PWM self-increasing stepping.
[23:16]	RW	ddr_avs_fsm_dec_pwm_step	DDR AVS FSM PWM Decrement step.
[15:3]	RO	reserved	reserve
[2:1]	RW	ddr_avs_hpm_fsm_samples; samples; calc_mode	DDR AVS HPM FSM calculation mode. 00: average of 4 01: average of 8 10: average of 16 samples; 11: average of 32 samples.
[0]	RW	ddr_hpm_fsm_en	DDR AVS HPM FSM enable control. 0: off; 1: open.

PERI_PMC8

PERI_PMC8 is the PERI_PMC8 register.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_PMC8	0x0000_0000

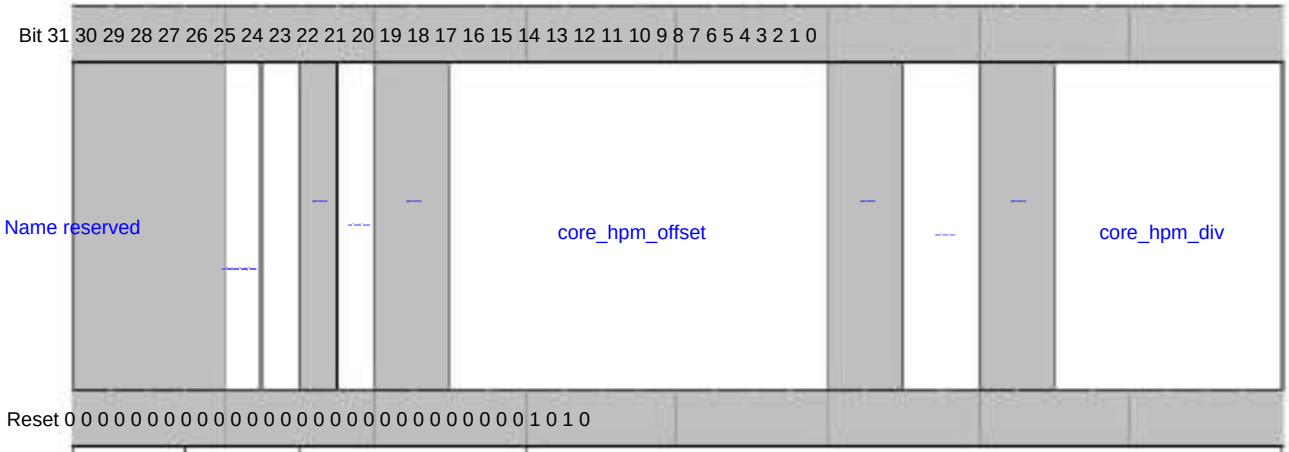
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0_avs_fsm_inc_pwm_step								mda0_avs_fsm_dec_pwm_step								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	mda0_avs_fsm_inc_pwm_step	MDA0 AVS FSM PWM self-increasing stepping.
[23:16]	RW	mda0_avs_fsm_dec_pwm_step	MDA0 AVS FSM PWM auto-decrement step.
[15:3]	RO	reserved	reserve
[2:1]	RW	mda0_avs_hpm_fsm_calc_mode	MDA0 AVS HPM FSM calculation mode. 00: average of 4 samples; 01: average of 8 samples; 10: average of 16 samples; 11: average of 32 samples.
[0]	RW	mda0_hpm_fsm_en	MDA0 AVS HPM FSM enable control. 0: off; 1: open.

PERI_PMC10

PERI_PMC10 is the CORE HPM control register 0

Offset Address	Register Name	Total Reset Value
0x0028	PERI_PMC10	0x0000_000A



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	core_hpm_srst_req	CORE HPM reset request, active high. 0: cancel reset; 1: Reset.
[26]	RW	core_hpm_monitor_en	CORE HPM loop monitoring enabled. 0: single monitoring; 1: Cyclic monitoring.
[25]	RO	reserved	reserve.
[24]	RW	core_hpm_en	Enables a CORE HPM measurement process. 0: Before starting a process, this value needs to be kept at 0; 1: Start a FM process.
[23:22]	RO	reserved	reserve.
[21:12]	RW	core_hpm_offset	CORE HPM OFFSET value.
[11:10]	RO	reserved	reserve.
[9:8]	RW	core_hpm_shift	CORE HPM SHIFT value.
[7:6]	RO	reserved	reserve.
[5:0]	RW	core_hpm_div	CORE HPM reference clock divider configuration. n : n+1 frequency division (n must be configured greater than 0).

PERI_PMC11

PERI_PMC11 is the CORE HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_PMC11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	core_hpm_pc_record1	core_hpm_pc_record0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RO	core_hpm_up_warning	CORE HPM overflow warning. High effective.
[24]	RO	core_hpm_low_warning	CORE HPM underflow warning. High effective.
[23:22]	RO	reserved	reserve.
[21:12]	RO	core_hpm_pc_recor	CORE HPM raw pattern 1. d1
[11]	RO	reserved	reserve.
[10]	RO	0: invalid; core_hpm_pc_valid	The CORE HPM outputs a valid indication. 1: Valid.
[9:0]	RO	core_hpm_pc_recor	CORE HPM raw pattern 0. d0

PERI_PMC12

PERI_PMC12 is CORE HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_PMC12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	---				core_hpm_rcc				---												core_hpm_pc_record3								---								core_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve
[28:24]	RO	core_hpm_rcc	CORE HPM output has RCC code.
[23:22]	RO	reserved	reserve.
[21:12]	RO	core_hpm_pc_recor	CORE HPM raw pattern 3. d3
[11:10]	RO	reserved	reserve.
[9:0]	RO	core_hpm_pc_recor	CORE HPM raw pattern 2. d2

PERI_PMC13

PERI_PMC13 is CORE HPM control register 3

Offset Address	Register Name	Total Reset Value
0x0034	PERI_PMC13	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_monitor_period								---												core_hpm_lowlimit								---								core_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

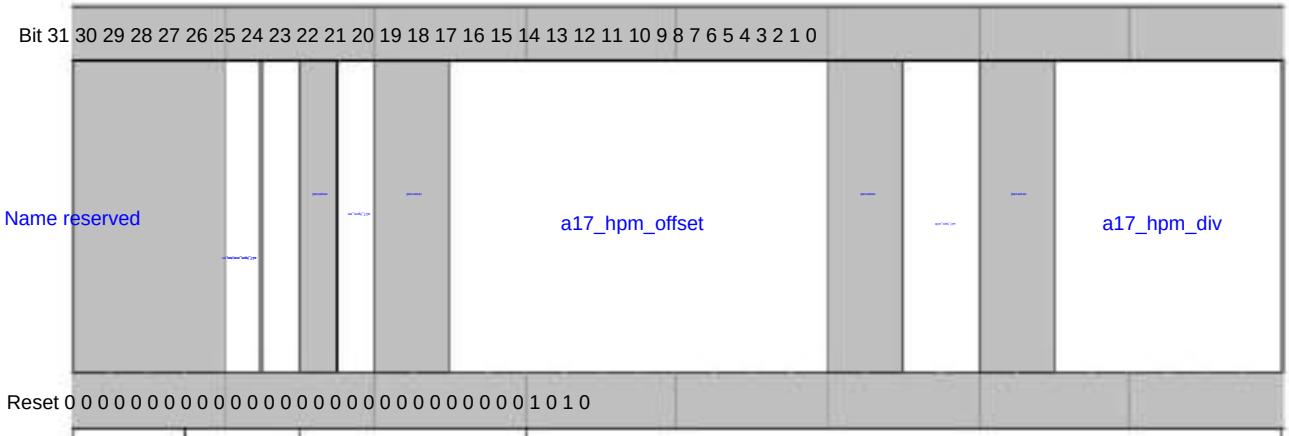
Bits	Access Name		Description
[31:24]	RW	period is: core_hpm_monitor_period T = N*2048/1000 ms	CORE HPM loop monitoring period. If the configuration value is N, the monitoring interval is 522ms, and the minimum interval is 2msÿ
[23:22]	RO	reserved	reserve.
[21:12]	RW	core_hpm_lowlimit	CORE HPM lower limit value.

[11:10] RO		reserved	reserve.
[9:0] RW	core_hpm_uplimit		CORE HPM upper limit value.

PERI_PMC14

PERI_PMC14 is A17 HPM control register 0

Offset Address	Register Name	Total Reset Value
0x0038	PERI_PMC14	0x0000_000A



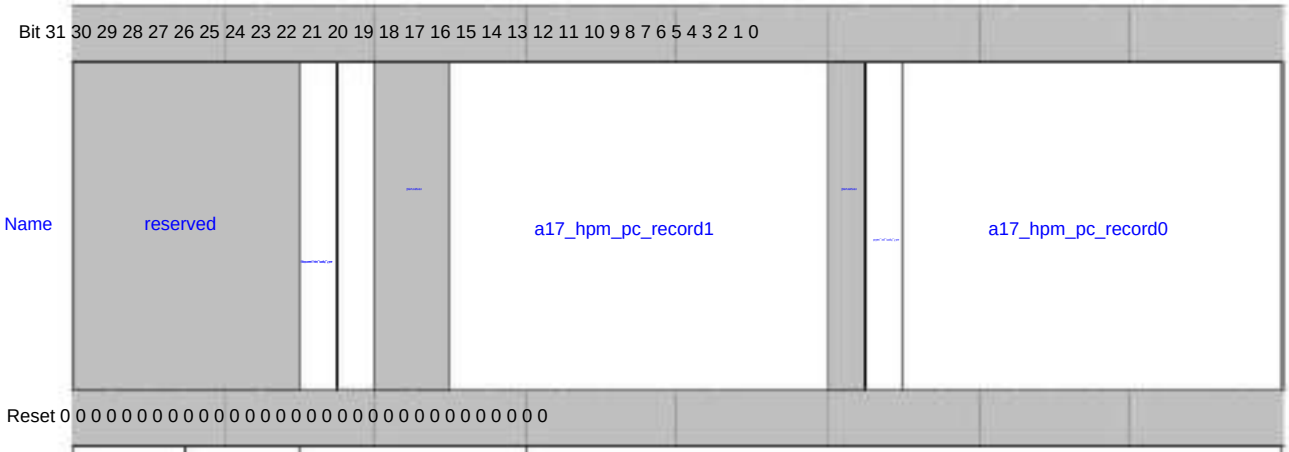
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	a17_hpm_srst_req	A17 HPM reset request, active high. 0: cancel reset; 1: Reset.
[26]	RW	enable. a17_hpm_monitor_in	A17 HPM cycle monitoring 0: single monitoring; 1: Cyclic monitoring.
[25]	RO	reserved	reserve.
[24]	RW	a17_hpm_en	Enable an A17 HPM measurement process. 0: Before starting a process, this value needs to be kept at 0; 1: Start a FM process.
[23:22]	RO	reserved	reserve.
[21:12]	RW	a17_hpm_offset	A17 HPM OFFSET value.
[11:10]	RO	reserved	reserve.
[9:8]	RW	a17_hpm_shift	A17 HPM SHIFT value.
[7:6]	RO	reserved	reserve.

[5:0] RW	a17_hpm_div		A17 HPM clock divider configuration. n : n+1 frequency division (n must be configured greater than 0).

PERI_PMC15

PERI_PMC15 is A17 HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_PMC15	0x0000_0000



Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RO	a17_hpm_up_warning	A17 HPM overflow warning, high effective.
[24]	RO	a17_hpm_low_warning	A17 HPM underflow warning, high effective.
[23:22]	RO	reserved	reserve.
[21:12]	RO	a17_hpm_pc_record1	A17 HPM raw pattern 1. d1
[11]	RO	reserved	reserve.
[10]	RO	a17_hpm_pc_valid	A17 HPM output valid indication. 0: invalid; 1: Valid.
[9:0]	RO	a17_hpm_pc_record0	A17 HPM raw pattern 0. d0

PERI_PMC16

PERI_PMC16 is A17 HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_PMC16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	---				a17_hpm_rcc				---				a17_hpm_pc_record3								---				a17_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:24]	RO	a17_hpm_rcc	A17 HPM output has RCC code.
[23:22]	RO	reserved	reserve.
[21:12]	RO	a17_hpm_pc_recor	A17 HPM raw pattern 3. d3
[11:10]	RO	reserved	reserve.
[9:0]	RO	a17_hpm_pc_recor	A17 HPM raw pattern 2. d2

PERI_PMC17

PERI_PMC17 is A17 HPM control register 3

Offset Address	Register Name	Total Reset Value
0x0044	PERI_PMC17	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_hpm_monitor_period								---				a17_hpm_lowlimit								---				a17_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

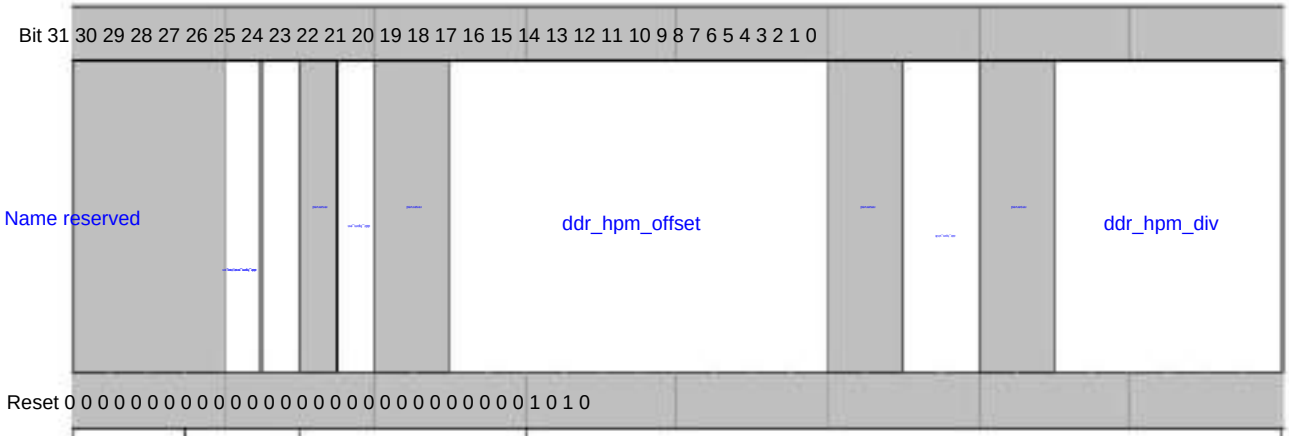
Bits	Access Name		Description
[31:24]	RW	is: a17_hpm_monitor_ period T = N*2048/1000 ms	A17 HPM cycle monitoring period. If the configuration value is N, the monitoring period is. The maximum monitoring interval is 522ms, and the minimum interval is 2msÿ
[23:22]	RO	reserved	reserve.
[21:12]	RW	a17_hpm_lowlimit	A17 HPM lower limit value.

[11:10] RO		reserved	reserve.
[9:0] RW	a17_hpm_uplimit	A17 HPM upper limit value.	

PERI_PMC18

PERI_PMC18 is DDR HPM control register 0

Offset Address	Register Name	Total Reset Value
0x0048	PERI_PMC18	0x0000_000A



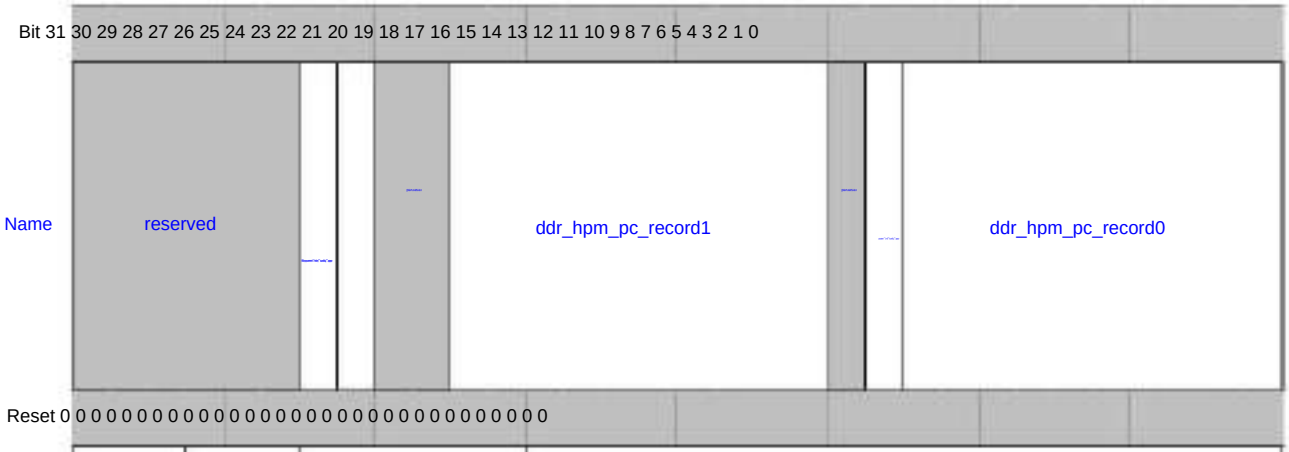
Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	ddr_hpm_srst_req	DDR HPM reset request, active high. 0: cancel reset; 1: Reset.
[26]	RW	enable. ddr_hpm_monitor_in	DDR HPM cycle monitoring 0: single monitoring; 1: Cyclic monitoring.
[25]	RO	reserved	reserve.
[24]	RW	ddr_hpm_en	Enable a DDR HPM measurement process 0: Before starting a process, this value needs to be kept at 0; 1: Start a FM process.
[23:22]	RO	reserved	reserve.
[21:12]	RW	ddr_hpm_offset	DDR HPM OFFSET ÿÿ
[11:10]	RO	reserved	reserve.
[9:8]	RW	ddr_hpm_shift	DDR HPM SHIFT ÿÿ
[7:6]	RO	reserved	reserve.

[5:0] RW	ddr_hpm_div		DDR HPM clock divider configuration. n : n+1 frequency division (n must be configured greater than 0).

PERI_PMC19

PERI_PMC19 is DDR HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x004C	PERI_PMC19	0x0000_0000



Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RO	ddr_hpm_up_warning	DDR HPM overflow warning, active high.
[24]	RO	ddr_hpm_low_warning	DDR HPM underflow warning, active high.
[23:22]	RO	reserved	reserve.
[21:12]	RO	ddr_hpm_pc_recor	DDR HPM raw pattern1. d1
[11]	RO	reserved	reserve.
[10]	RO	ddr_hpm_pc_valid	DDR HPM output valid indication. 0: invalid; 1: Valid.
[9:0]	RO	ddr_hpm_pc_recor	DDR HPM raw pattern 0. d0

PERI_PMC20

PERI_PMC20 is DDR HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0050	PERI_PMC20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	---				ddr_hpm_rcc				---												ddr_hpm_pc_record3								---								ddr_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:24]	RO	ddr_hpm_rcc	DDR HPM output has RCC code.
[23:22]	RO	reserved	reserve.
[21:12]	RO	ddr_hpm_pc_recor	DDR HPM raw pattern 3. d3
[11:10]	RO	reserved	reserve.
[9:0]	RO	ddr_hpm_pc_recor	DDR HPM raw pattern 2. d2

PERI_PMC21

PERI_PMC21 is DDR HPM control register 3

Offset Address	Register Name	Total Reset Value
0x0054	PERI_PMC21	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddr_hpm_monitor_period								---												ddr_hpm_lowlimit								---								ddr_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

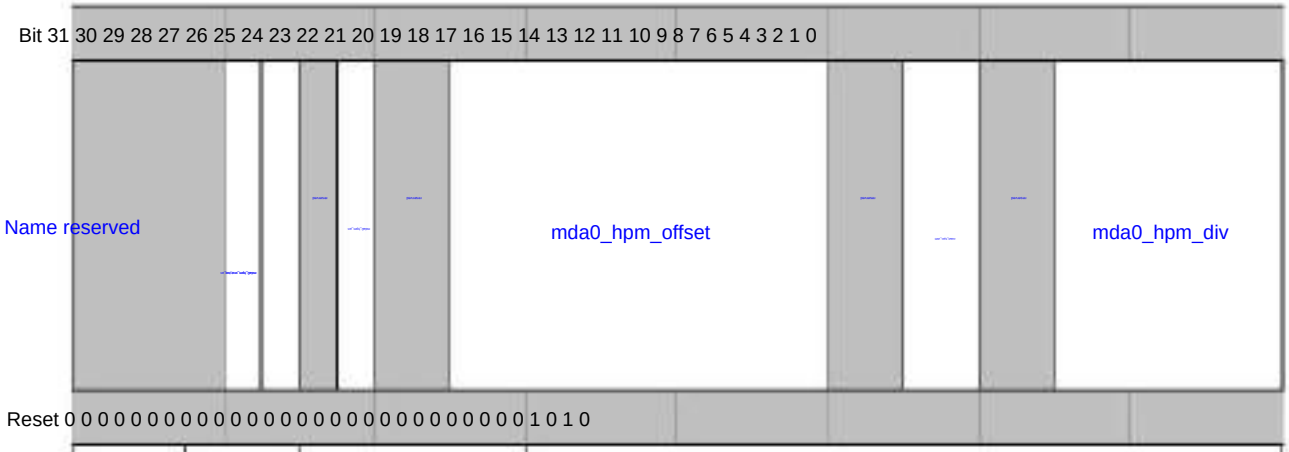
Bits	Access Name		Description
[31:24]	RW	period is: ddr_hpm_monitor_period T = N*2048/1000 ms	DDR HPM cycle monitoring period. If the configuration value is N, the monitoring . The maximum monitoring interval is 522ms, and the minimum interval is 2msÿ
[23:22]	RO	reserved	reserve.
[21:12]	RW	ddr_hpm_lowlimit	DDR HPM lower limit value.

[11:10] RO		reserved	reserve.
[9:0] RW	ddr_hpm_uplimit	DDR HPM upper limit value.	

PERI_PMC22

PERI_PMC22 is MDA0 HPM control register 0

Offset Address	Register Name	Total Reset Value
0x0058	PERI_PMC22	0x0000_000A



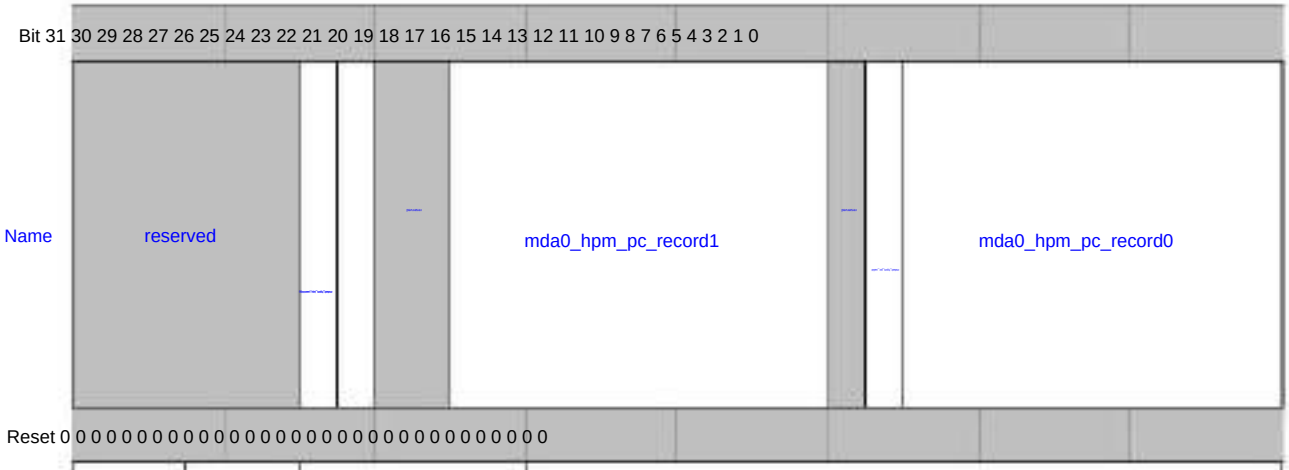
Bits	Access	Name	Description
[31:28] RO		reserved	reserve.
[27] RW		mda0_hpm_srst_re	MDA0 HPM reset request, active high. 0: cancel reset; q 1: reset.
[26] RW		mda0_hpm_monito	MDA0 HPM loop monitoring enable. 0: single monitor; r_en 1: Cyclic monitoring.
[25] RO		reserved	reserve.
[24] RW	mda0_hpm_en		Enable an MDA0 HPM measurement process. 0: Before starting a process, this value needs to be kept at 0; 1: Start a FM process.
[23:22] RO		reserved	reserve.
[21:12] RW	mda0_hpm_offset	MDA0 HPM OFFSET value.	
[11:10] RO		reserved	reserve.
[9:8] RW	mda0_hpm_shift	MDA0 HPM SHIFT value.	

[7:6]	RW	reserved	reserve.
[5:0]	RW	mda0_hpm_div	MDA0 HPM clock divider configuration. n : n+1 frequency division (n must be configured greater than 0).

PERI_PMC23

PERI_PMC23 is MDA0 HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_PMC23	0x0000_0000



Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25]	RO	mda0_hpm_up_warning	MDA0 HPM overflow warning, high effective.
[24]	RO	mda0_hpm_low_warning	MDA0 HPM underflow warning, active high.
[23:22]	RO	reserved	reserve.
[21:12]	RO	mda0_hpm_pc_rec	MDA0 HPM raw pattern 1. ord1
[11]	RO	reserved	reserve.
[10]	RO	mda0_hpm_pc_vali	MDA0 HPM output valid indication. 0: invalid; d 1: Valid.
[9:0]	RO	mda0_hpm_pc_rec	MDA0 HPM raw pattern 0. ord0

PERI_PMC24

PERI_PMC24 is MDA0 HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_PMC24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—				mda0_hpm_rcc				—								mda0_hpm_pc_record3								—								mda0_hpm_pc_record2			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:24]	RO	mda0_hpm_rcc	MDA0 HPM output has RCC code.
[23:22]	RO	reserved	reserve.
[21:12]	RO	mda0_hpm_pc_rec	MDA0 HPM raw pattern 3. ord3
[11:10]	RO	reserved	reserve.
[9:0]	RO	mda0_hpm_pc_rec	MDA0 HPM raw pattern 2. ord2

PERI_PMC25

PERI_PMC25 is MDA0 HPM control register 3

Offset Address	Register Name	Total Reset Value
0x0064	PERI_PMC25	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0_hpm_monitor_period								—								mda0_hpm_lowlimit								—								mda0_hpm_uplimit			
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:24]	RW	period is: mda0_hpm_monitor_period T	MDA0 HPM cycle monitoring period. If the configuration value is N, the monitoring = N*2048/1000 ms. The maximum monitoring interval is 522ms, and the minimum interval is 2ms.

[23:22] RO		reserved	reserve.
[21:12] RW		mda0_hpm_lowlim	MDA0 HPM lower limit value. it
[11:10] RO		reserved	reserve.
[9:0] RW	mda0_hpm_up	limit	MDA0 HPM upper limit value.

PERI_PMC30

PERI_PMC30 is the HPM loop monitor trimming control register 1.

Offset Address	Register Name	Total Reset Value
0x0078	PERI_PMC30	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	a17_hpm_monitor_period_fine	ddr_hpm_monitor_period_fine	mda0_hpm_monitor_period_fi it is	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	a17_hpm_monitor_ period_fine	A17 HPM cycle monitor period trimming parameter.
[23:16]	RW	ddr_hpm_monitor_ period_fine	DDR HPM cycle monitor cycle trimming parameter.
[15:8]	RW	mda0_hpm_monito r_period_fine	MDA0 HPM cycle monitor cycle fine-tuning parameter.
[7:0]	RO	reserved	reserve.

PERI_PMC31

PERI_PMC31 is the HPM loop monitor trimming control register 2.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_PMC31	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			core_hpm_monitor_period_fin it is
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

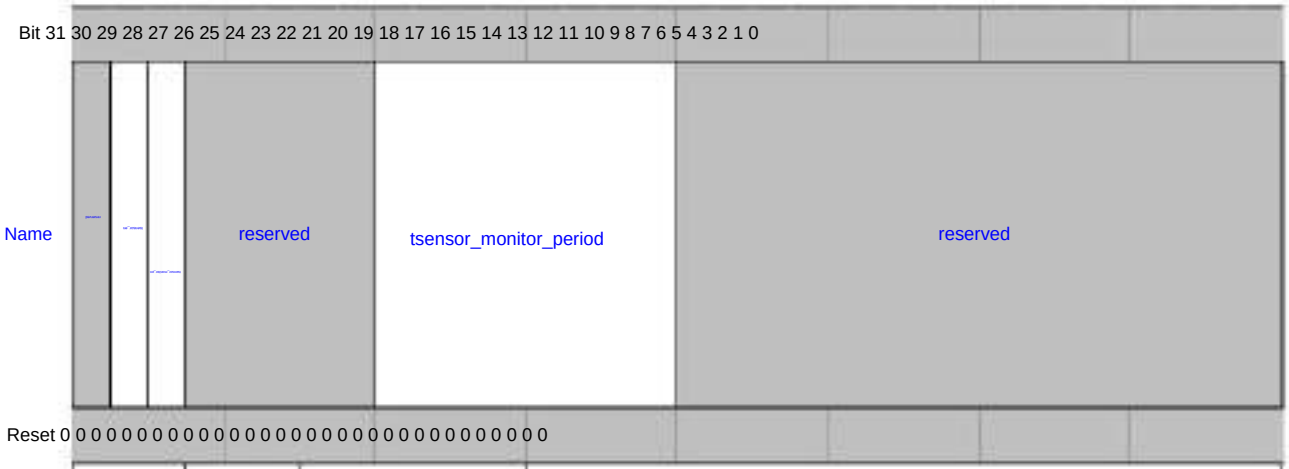
Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.

[7:0] RW		core_hpm_monitor_period_fine	CORE HPM loop monitor cycle fine-tuning parameter.

PERI_PMC68

PERI_PMC68 is the PERI_PMC68 register.

Offset Address	Register Name	Total Reset Value
0x110	PERI_PMC68	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	tsensor_en	TSENSOR enable control. 0: off; 1: enable.
[29]	RW	tsensor_monitor_en	Temperature cycling monitoring is enabled. 0: off; 1: enable.
[28:24]	RO	reserved	reserve.
[23:16]	RW	tsensor_monitor_period	Temperature cycle monitoring cycle, timing base is 2ms.
[15:0]	RO	reserved	reserve.

PERI_PMC69

PERI_PMC69 is the PERI_PMC69 register.

Offset Address	Register Name	Total Reset Value
0x0114	PERI_PMC69	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tsensor_temp_uplimit	reserved	tsensor_temp_lowlimit
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	tsensor_temp_uplimit	temperature overflow value.
[15:10]	RO	reserved	reserve.
[9:0]	RW	tsensor_temp_lowlimit	temperature underflow value.

PERI_PMC70

PERI_PMC70 is the PERI_PMC70 register.

Offset Address	Register Name	Total Reset Value
0x0118	PERI_PMC70	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tsensor_temp_code1	reserved	tsensor_temp_code0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	tsensor_temp_code	Temperature record value 1. 1
[15:10]	RO	reserved	reserve.
[9:0]	RO	tsensor_temp_code	temperature record value 0. 0

PERI_PMC71

PERI_PMC71 is the PERI_PMC71 register.

Offset Address	Register Name	Total Reset Value
0x011C	PERI_PMC71	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tsensor_temp_code3								reserved							tsensor_temp_code2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	tsensor_temp_code	temperature record value 3. 3
[15:10]	RO	reserved	reserve.
[9:0]	RO	tsensor_temp_code	temperature record value 2. 2

PERI_PMC72

PERI_PMC72 is the PERI_PMC72 register.

Offset Address	Register Name	Total Reset Value
0x0120	PERI_PMC72	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tsensor_temp_code5								reserved							tsensor_temp_code4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	tsensor_temp_code	temperature record value 5. 5
[15:10]	RO	reserved	reserve.
[9:0]	RO	tsensor_temp_code	temperature record value 4. 4

PERI_PMC73

PERI_PMC73 is the PERI_PMC73 register.

Offset Address	Register Name	Total Reset Value
0x0124	PERI_PMC73	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	tsensor_temp_code7	reserved	tsensor_temp_code6
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	tsensor_temp_code	temperature record value 7. 7
[15:10]	RO	reserved	reserve.
[9:0]	RO	tsensor_temp_code	temperature record value 6. 6

PERI_PMC74

PERI_PMC74 is the PERI_PMC74 register.

Offset Address	Register Name	Total Reset Value
0x0128	PERI_PMC74	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RO	tsensor_low_warning	Temperature underflow warning flag. High effective.
[0]	RO	tsensor_up_warnin	temperature overflow warning flag. High effective. g

PERI_PMC77

PERI_PMC77 is the PERI_PMC77 register.

Offset Address	Register Name	Total Reset Value
0x0134	PERI_PMC77	0x011F_EC01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	1	0	0	0	1	1	1							1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:12] RO		reserved	reserve.
[11] RO		a17_irq_n	A17 Rapid interrupt indication signal. 0: Interrupt is valid; 1: Interrupts are disabled.
[10] RO		a17_fiq_n	A17 General interrupt indication signal. 0: Interrupt is valid; 1: Interrupts are disabled.
[9]	RO	a17_standbywfe	A17 Core WFE indication signal. 0: WFE is disabled. 1: WFE is valid;
[8]	RO	a17_standbywfil2	A17 non-CPU WFI indicator signal. 0: WFI is disabled. 1: WFI is valid;
[7]	RO	a17_standbywfi	A17 Core WFI indication signal. 0: WFI is disabled. 1: WFI is valid;
[6]	RO	a17_bus_pwrdn_ac 0: 1: Complete the power-on request;	A17_CPU_SUBSYS Bus power down handshake indication signal. complete power off request. k_n

[5] RW		a17_bus_pwrdn_re 0: Power	A17_CPU_SUBSYS Bus power down handshake control signal. down request. q_n_cfg 1: power-on request;
[4]	RO	a17_bus_cactives	A17 Asynchronous bridge active indication signal (slave end). 0: asynchronous bridge idle; 1: The asynchronous bridge is busy.
[3]	RO	idle; a17_bus_cactivem	A17 Asynchronous bridge active indication signal (master end). 0: asynchronous bridge 1: The asynchronous bridge is busy.
[2]	RO	a17_pwrdn_ack	A17 Power supply status indicator. 0: power supply; 1: Power down.
[1] RW		request. a17_pwrdn_req_cf g	A17 Power down 0: power supply; 1: Power down.
[0] RW a17_pwrdn_iso_cfg 0:		no isolation;	A17 Signal isolation control (signal isolation must be performed before power-off, and the bus must be in idle state when isolation is started). 1: Quarantine.

PERI_PMC78

PERI_PMC78 is the PERI_PMC78 register.

Offset Address	Register Name	Total Reset Value
0x0138	PERI_PMC78	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	cci_arch_clkgate_en	CCI arch automatic gate switch. 0: off; nable 1: open.
[11]	RW	use_cs_pr	coresight power requestor component switch. 0: off; 1: open.
[10]	RW	lp_mode_en	A17 L2 retention Low power mode switch. 0: disable; 1: enable.
[9]	RW	wfi_ret_en	A17 Wi-Fi signal triggers low power mode enable switch. 0: off; 1: open.
0cycle; [8]	RW	pgen_pulse_width	pgen signal stretching control. 0: increase 1: increase 2cycle.
widened. 0: increase 0cycle; [7]	RW	pgenf2retnr_timing	The time interval from the falling edge of the pgen signal to the rising edge of the ret1n signal is 1: increase 2cycle.

0: increase 0cycle; [6] RW		retnf2pgenr_timing	Time interval widening control from falling edge of ret1n signal to rising edge of pgen signal. 1: increase 2cycle.
[5:4] RW		mode; a17_l2_ram_lp_mo	Low power mode selection for A17 L2 RAM. 00: normal 01: enable precharge mode; de 10: reserved; 11: RET mode enabled.
[3] RW		cci_sf_ram_lp_mod 0: e_update	cci_sf_ram_lp_mode update enable. do not update to logic; 1: Update to logic.
[2:0] RW		cci_sf_ram_lp_mod 1x:	Low power mode selection for CCI snoop filter ram. 00: CCI snoop filter RAM remains in normal operating state; 01: Allow CCI snoop filter RAM to enter retention dynamically; power off. Note: Flush to logic only when cci_sf_ram_lp_mode_update is 1.

PERI_PMC79

PERI_PMC79 is the PERI_PMC79 register.

Offset Address	Register Name	Total Reset Value
0x013C	PERI_PMC79	0x00FF_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.

[8] RW	a17_ac_inactive		A17 ACE bus AC channel deactivation control signal. 0: Do not shield the AC channel; 1: Shield the AC channel.
[7:2] RO		reserved	reserve.
[1:0] RW	mode_onoff		A17 Power on and off control mode. 00: reserved; 01: reserved; 1X: Software manual mode.

Table of contents

illustration catalog

table of contents

4 memory interface

4.1 DDR Controller

4.1.1 Overview

DDRC (DDR SDRAM Controller) realizes the access control to the dynamic memory DDR3 SDRAM.

4.1.2 Features

Features of DDRC:

DDRC supports a single channel and only provides one chip select space; the corresponding DDR SDRAM data bus bit width of each channel is 32bit, that is, it supports DDR with a maximum bit width of 32bit, and also supports DDR with a bit width of 16bit, but it is limited to the use of

low Two bytes. The maximum supported

storage space is: 2GByte. Support DDR3 SDRAM bus operating frequency is 800MHz, support data rate

1600Mbps. Support low power consumption modes such as Power Down and Self Refresh of DDR SDRAM.

The burst8 transfer mode of DDR SDRAM supports INCR and WRAP commands, but does not support FIXED.

4.1.3 Functional description

4.1.3.1 Application Block Diagram

DDRC realizes the data access of external memory DDR3 SDRAM from CPU and other main devices in the SoC system. The timing parameter register of DDRC can be configured by CPU to support DDR3 SDRAM devices conforming to JEDEC standard. Table 4-1 lists the DDR3 SDRAMs of several mainstream DRAM manufacturers supported by DDRC. This table describes the operating frequency of DDR3 SDRAM without considering the limitations of capacity and other factors.

Table 4-1 List of DDR3 SDRAM supported by DDRC

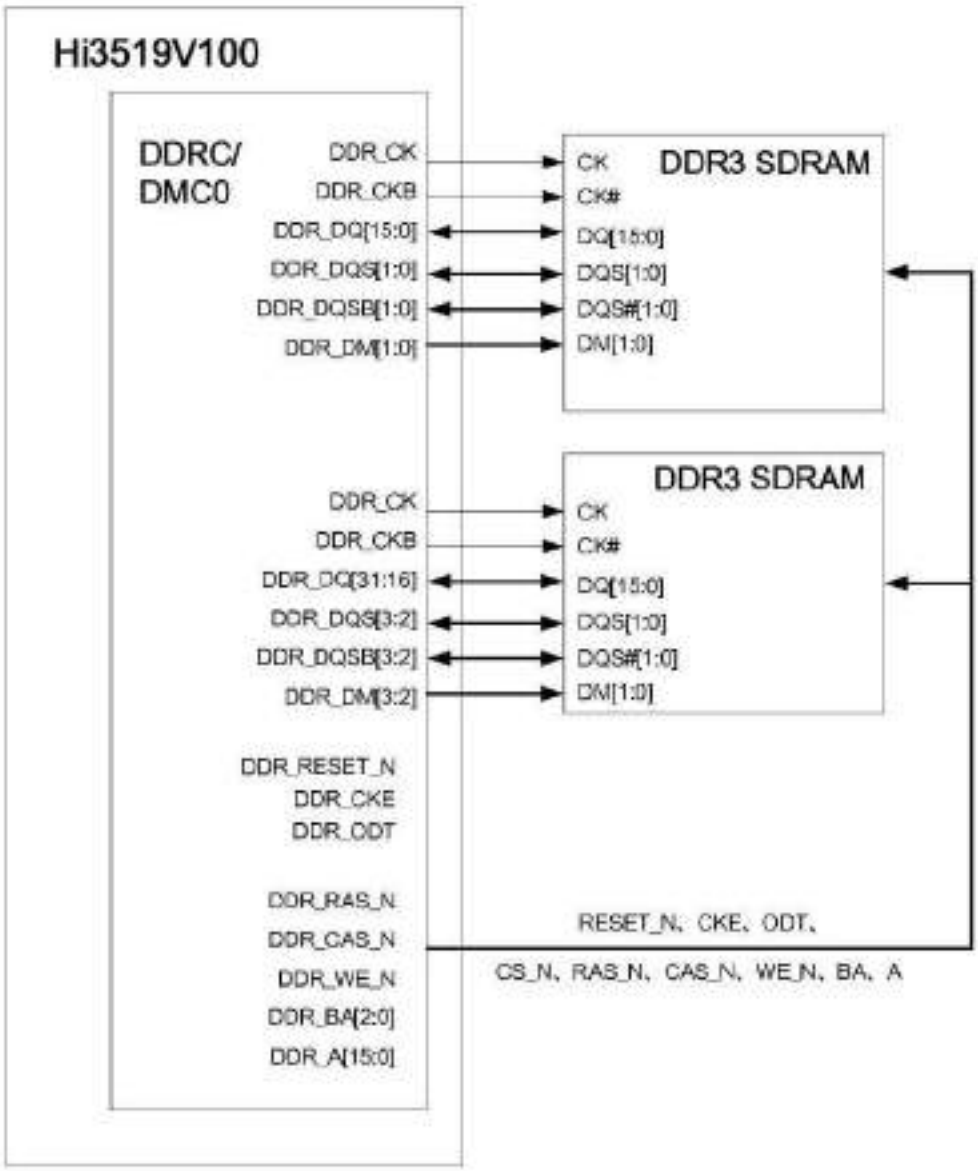
manufacturers	800MHz	933MHz
Samsung	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133

manufacturers	800MHz	933MHz
lanya	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133
Hynix	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133

Note: The specific supported device types are based on the JEDEC standard and the device DATASHEET.

In DDRC single-channel mode, each channel supports 32bit interconnection mode, as shown in Figure 4-1 and Figure 4-2 .

Figure 4-1 In DDRC single-channel mode, the interconnection diagram between each channel and two 16-bit DDR3 SDRAMs

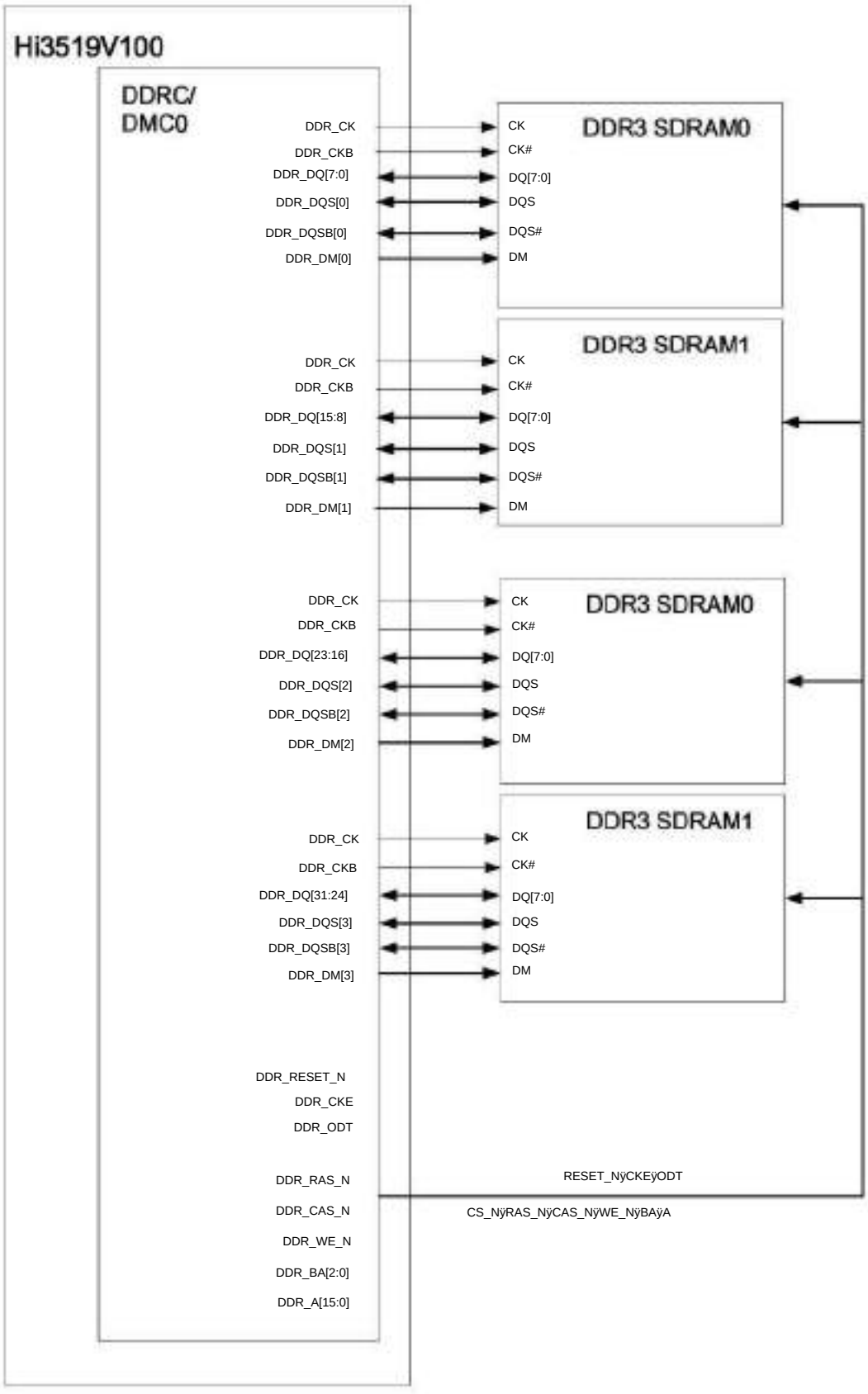


Connection

instructions: DDRC is connected to 32bit DDR3 SDRAM, which consists of two storage devices with a data bus width of 16bit.

Command control signals corresponding to DDRC/DMC0: DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[15:0], DDR_ODT are connected to the command control signal of DDR3 SDRAMx, and the command control bus of DDRC is a 1 drive 2 connection mode.

Figure 4-2 In DDRC single-channel mode, the interconnection diagram of each channel and four pieces of 8-bit DDR3 SDRAM



Connection

instructions: DDRC is connected to 32bit DDR3 SDRAM, which is composed of 4 memory devices with a data bus width of 8bit. DDRC command control signals: DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[15:0] are connected to the command control signal of DDR3 SDRAMx at the same time, that is, the command control bus of DDRC is a connection mode of 1 drive 4.

4.1.3.2 Functional principle

The DDRC interface timing meets the JESD standard, and completes the data access and state control of the DDR3 SDRAM by sending the command word of the DDR3 SDRAM. Including DDR3 SDRAM read and write access, automatic refresh, low power consumption control and other functions.

command truth table

DDRC supports the read, write and control command words of DDR3 SDRAM. The command truth table of DDRC is shown in Table 4-2 . Please refer to the JEDEC standard and device handbook for more detailed information.

Table 4-2 DDR3 command truth table

FUNCTION	DDR3 _CKE	DDR3 _CSN	DDR3_ Rasna	DDR3_ CASN	DDR3 _WEN	DDR3_ADR			DDR 3_NO
						15:11 AP(10) 9:0			
DESELECT	H	H	X	X	X	X	X	X X	
ACTIVE	H	L	L	H	H	IN	IN	V V	
READ	H	L	H	L	H	IN	IN	V V	
WRITE	H	L	H	L	L	IN	IN	V V	
PRECHARGE	H	L	L	H	L	IN	L	VBA	
PRECHARGE ALL H		L	L	H	L	IN	H	V V	
AUTO REFRESH	H	L	L	L	H	IN	IN	V V	
SELF REFRESH ENTRY	H->L L		L	L	H	IN	IN	V V	
SELF REFRESH EXIT L->H L			H	H	H	IN	IN	V V	
MODE REGISTER SET H		L	L	L	L	IN	IN	V V	
ZQCL	H	L	H	H	L	X	H	X X	
ZQCS	H	L	H	H	L	X	L	X X	

H: Indicates high level; L: Indicates low level; V: Indicates valid; X: Indicates don't care.

ZQCL (ZQ Calibration Long): It is used to start the ZQ Calibration operation of DDR3 when DDR3 SDRAM is powered on and initialized.

ZQCS (ZQ Calibration Short): It is used to start the ZQ Calibration operation of DDR3 when the environmental conditions of the chip change.

Auto Refresh

When DDRC_CFG_TIMING2[taref] is configured as a non-zero value, DDRC automatically generates periodic AUTO REFRESH commands to complete the refresh operation on DDR SDRAM. At room temperature, DDR3 SDRAM requires 8,192 auto-refresh operations to be completed within 64ms, that is, the cycle of auto-refresh operations is 7.8us, and the actual value is subject to the device manual. DDRC_CFG_TIMING2[taref] configuration value (taref) and automatic refresh period (T=7.8us) relationship is:

Tÿtaref*(16*DDR clock period)

When DDRC_CFG_TIMING2[taref] is configured , the counter inside DDRC will automatically load the taref value to count down. When the counter value is 0, DDRC initiates an automatic refresh operation and reloads the taref value to count .

Low Power Management

DDRC supports low-power management in two modes: normal low-power mode and self-refresh low-power mode.

When configuring DDRC_CFG_PD[pd_en]=1 and enabling SDRAM automatic low power consumption, when the system is in an idle state (the DDRC bus interface has no read/write DDR access for a certain period of time), it will automatically control DDR3 SDRAM to enter normal low power consumption mode.

When the system needs to enter the standby mode, the DDR3 SDRAM can be controlled to enter the self-refresh low-power mode by configuring the register DDRC_CTRL_SREF[sref_req]=1 . In this mode, the power consumption of DDR3 SDRAM can be reduced to a minimum, while maintaining the data in DDR3 SDRAM, but at this time the system cannot access DDR3 SDRAMÿ

arbitration mechanism

DDRC mainly schedules each command through the priority scheduling algorithm. In addition, DDRC also implements two scheduling auxiliary methods, flow control and timeout control (these two control methods can be enabled according to business needs, and can be enabled at the same time or separately) to control command requests.

1. Priority scheduling

The priority level is: 0~7. Priority configuration is independent for each AXI port.

Priority configuration method for each AXI port command:

Step 1. Select the priority mapping method by configuring AXI_QOS_MAP[pri_map_mode], if AXI_QOS_MAP
If [pri_map_mode] is set to 1, the system bus associated signal of the command is used to get the index; if AXI_QOS_MAP [pri_map_mode] is set to 0, the value of AXI_QOS_MAP [id_map_idx] needs to be configured to select any 3 bits in the command id signal to get the index number.

Step 2. Configure the AXI_QOS_WRPRIn and AXI_QOS_RDPRIn registers.

Step 3. DDRC queries AXI_QOS_WRPRIn or
One of the 8 preset values in the AXI_QOS_RDPRIn register, and add this value to the read and write commands of the bus as a priority. The DDRC internal arbitrator is scheduled according to the priority attribute of the command that initiates the arbitration request, so as to realize high-efficiency access to DDR SDRAM.

----Finish

Supports priority adaptation. By configuring AXI_QOS_ADPTn, enable the priority adaptive function of each port to help low-priority commands pass through all levels of arbitration: every time the priority increment cycle arrives, the command priority will be automatically increased by one level until the priority is raised to Second highest; the range of priority increment period is adpt_prd*16

The read and write commands of the same port will be aggregated into one path, and two optional arbitration rules are supported:

Read and write commands are arbitrated on a first-come, first-served basis, and when they arrive at the same time, read first and then write.

Arbitrate according to the priority of read and write commands.

Commands with different priorities: Arbitration is given to the command with the highest priority.

Commands with the same priority: Arbitrate to the command that has not been arbitrated for the longest time.

2. Flow control

Configure QOSB_FLUX_EN [flux_en], and group according to the id of the command according to the needs of flow control, and DDRC will distribute the flow of each group to ensure the bandwidth of each port when DDRC access is busy.

3. timeout control

Configure QOSB_TIMEOUT_MODE[timeout_mode] to select the timeout attribute mapping mode of the command. Similar to the priority mapping, the timeout mapping method: in the configured mapping mode, query one of the 16 preset timeout values, and add this value to the command as the timeout value (a value of 0 means prohibiting timeout) . Inside DDRC, the commands with timeout attribute will forcibly shield other commands without timeout attribute from initiating arbitration requests to the arbitrator when the waiting time is up, and initiate arbitration requests immediately.

Traffic statistics and command latency statistics function

DDRC supports traffic statistics function: It can count interface read and write traffic to collect current traffic information to decide whether to perform DFS (Dynamical Frequency Scaling), that is, to increase or decrease the frequency of DDRC. You can count the read/write traffic of the specified ID separately. Statistics on overall read/write traffic can be made. It supports DDR interface utilization statistics. The statistical counter supports continuous statistics and single statistics. When it is continuous statistics, the counter is a non-saturated counter. The counter value is read out before winding. When it is a single statistics, the statistics counter will stop statistics after the statistics time is up, the system can use this function to count the instantaneous traffic and latency.

DDRC supports the command latency statistics function: it supports the maximum latency statistics of the specified ID access read and write, and the cumulative latency statistics.

The statistics function operates as follows:

Step 1. Use DDRC_CFG_PERF [perf_mode] to configure whether the statistical mode is continuous trigger or single trigger, such as
For a single trigger, you also need to configure the perf_prd field to configure the statistics period.

Step 2. Configure the desired statistical ID through DDRC_CFG_STAID .

Step 3. Set the Mask value of the ID through DDRC_CFG_STAIDMSK , and DDRC will determine whether to include the current visit in the statistics according to whether sta_idmask& cmd_id is equal to DDRC_CFG_STAID . Using this method can count the statistical values of multiple IDs.

Step 4. Configure DDRC_CTRL_PERF[perf_en] to enable statistics. For single statistics, when perf_en returns to 0, it means the statistics are completed. For continuous statistics, the software needs to write 0 to DDRC_CTRL_PERF[perf_en] to stop the statistics.

Step 5. Through DDRC_HIS_FLUX_WR, DDRC_HIS_FLUX_RD, DDRC_HIS_FLUX_WCMD, DDRC_HIS_FLUX_RCMDÿDDRC_HIS_FLUXID_WRÿDDRC_HIS_FLUXID_RDÿ

DDRC_HIS_FLUXID_WCMDÿDDRC_HIS_FLUXID_RCMDÿ
DDRC_HIS_WLATCNT0ÿDDRC_HIS_WLATCNT1ÿDDRC_HIS_RLATCNT0ÿ
DDRC_HIS_RLATCNT1, DDRC_HIS_INHERE_RLAT_CNT to observe the statistical results.

----Finish

address mapping method

DDRC realizes the conversion of the access address of the system bus to the access address of DDR SDRAM.
RRBC(Rank_row_bank_col),
RRBC(Row_rank_bank_col)ÿRRCBC(Rank_row_col_bank_col)ÿ
RRCBC (Row_rank_col_bank_col) four mapping methods. Configure the SDRAM row address and column address bit width through the DDRC_CFG_RNKVOL[mem_row] and DDRC_CFG_RNKVOL[mem_col] registers . DDRC converts system bus addresses to DDR SDRAM addresses according to the address mapping algorithm.

The following uses the RRCBC (Rank_row_col_bank_col) mode as an example to illustrate the mapping algorithm of the system bus address and the DDR SDRAM address. Suppose the system bus address is BUSADR[31:0], the effective address is BUSADR[m-1:0], and the address of DDR3 SDRAM is DDRADR[15:0]. When DDRADR[15:0] is used as a row address, its effective address is DDRROW[x-1:0], when it is used as a column address, its effective address is DDRCOL[y-1:0], and the BANK address of DDR is DDRBA[z-1:0], the storage data bus width of DDRC is DW, at this time AXI_REGION_ATTRIB[ch_mode]=2'b01 (AXI_REGION_ATTRIB[ch_mode]=2'b11 will not be introduced temporarily), then the address mapping relationship is:

AXI_REGION_ATTRIB[bnk_mod] selects the granularity of bank interleaving, assuming that the configuration is 3b101 (docking 32bit wide devices), that is, the granularity of interleaving is 256B:

BUSADR[m-1:0] = {DDRROW[x-1:0],DDRCOL[y-1:6],DDRBA[z 1:0],DDRCOL[5:0],2{b0}}

Table 4-3 below illustrates the address mapping methods of DDR3 respectively.

Table 4-3 DDRC DDR3 32bit mode address mapping table

memory type			DDR BA				DDR ADR													
Mbit×bw	row address width	Column address width	2	1	0	row address column address	14	13	12	11	10/ AP	9	8	7	6	5	4	3	2	1 0
512Mbit 8bank																				
32×16	12	10	10	9	8	Row -	- 26 25 24 23 22 21 [20:15]													
						Col	·	·	·	- AP 14 13 12 11											[7:2]
1024Mbit 8bank																				
64×16	13	10	10	9	8	Row -	- 27 26 24 24 23 22 21 [20:15]													
						Col	·	·	·	- AP 14 13 12 11											[7:2]
2048Mbit 8bank																				
128×16	13	10	10	9	8	Row - 28 27 26 25 24 23 22 21 [20:15]														
						Col	·	·	-	- AP 14 13 12 11											[7:2]

memory type			DDR BA				DDR ADR													
Mbit×bw	row address width	Column address width	2	1	0	row address column address	14	13	12	11	10/ AP	9	8	7	6	[5	0]			
4096Mbit 8bank																				
256×16	14	10	10	9	8	Row 29 28 27 26 25 24 23 22 21 [20:15]														
						Col	·	·	-	-	AP	14	13	12	11				[7:2]	

4.1.4 Working method

4.1.4.1 Soft Reset

DDRC cannot perform a single reset operation. DDRC can only be reset during global soft reset. After reset, you need to re-initialize DDR3 SDRAM according to the initialization process.

4.1.4.2 DDR initial configuration process

After the system is powered on, the initialization of DDR SDRAM must be completed before the system can access DDR SDRAM. The following points need to be noted before initialization:

When powering on DDR SDRAM, the JEDEC standard needs to be followed. This initialization process needs to be carried out after the system enters NORMAL mode.

The DDR SDRAM connected by DDRC has a capacity of 8Gbit, which can be composed of two pieces of DDR SDRAM with a capacity of 4Gbit and a data bus width of 16bit or four pieces of DDR SDRAM with a capacity of 2Gbit and a data width of 8bit; the working frequency of DDRC and DDR In ratio 1:2 mode, the initialization steps of the entire DDR subsystem are as follows:

Step 1. Configure DMC0 register DDRC_CFG_SREF=0x0 to exit self-refresh (this step is required for DDR3 mode).

Step 2. The software queries the DMC0 register DDRC_CURR_FUNC[0]=1'b0 , and then executes.

Configure the working mode, clock frequency, and timing parameters of DMC0, involving registers DDRC_CFG_WORKMODEÿDDRC_CFG_RNKVOLÿ

ÿÿ 3. DDRC_CFG_TIMING0ÿDDRC_CFG_TIMING1ÿDDRC_CFG_TIMING2ÿ
DDRC_CFG_TIMING3ÿDDRC_CFG_TIMING4ÿDDRC_CFG_TIMING5ÿ
DDRC_CFG_TIMING6ÿDDRC_CFG_PDÿDDRC_CFG_DDRPHYÿ
DDRC_CFG_ODTÿ

Step 4. Configure the register DDRC_CFG_DDRMODE of DMC0 to select the type of external DDR.

Step 5. Configure the working mode of DDRPHY connected to DMC0, time parameters, DDRPHY IO driver and ODT impedance, and delay parameters of the read and write command path. The registers involved are: PHYTIMER0, PHYTIMER1ÿPLLTIMERÿDLYMEASCTRLÿDRAMCFG ÿACPHYCTL4ÿ
DRAMTIMER0ÿDRAMTIMER1ÿDRAMTIMER2ÿDRAMTIMER3ÿ
DRAMTIMER4ÿDRAMTIMER5ÿIOCTL(Static_reg)ÿMISCÿMODEREG01ÿ
MODEREG23ÿMODEREG45ÿMODEREG67ÿPHYCTRL0ÿACPHYBOUNDÿ

Step 6. Configure the registers RNK2RNK, DMSEL, DQSSEL(Static_reg) of DDRPHY0, select ADDR/CMD signal swap mode and DQ/DQS signal swap mode.

Step 7. Configure the register PHYINITCTRL of the DDRPHY docked with DMC0, and start DDRPHY0 for initialization change.

Step 8. Wait for the PHYINITCTRL of DDRPHY0 to be 0, that is, the initialization of DDR PHY0 is completed.

Step 9. Configure DDRC_CFG_TIMING2[10:0] of DMC0 to enable the auto refresh command sending function.

Step 10. Configure the AXI_REGION_MAP of AXI , and configure the address region mapping of DDR.

Step 11. Configure the AXI_REGION_ATTRIB of AXI , and configure the address region attribute of DDR.

Step 12. Configure DMC0 register DDRC_CFG_SREF=0x2 to decompress.

----Finish

After completing the above steps, DDR3 SDRAM can work normally.

Note: For different DDR granules, the values of the configured registers may be partially different, but the configuration process needs to be carried out according to the above steps.

4.1.5 AXI registers

4.1.5.1 AXI register overview

An overview of the AXI registers is shown in Table 4-4 .

Table 4-4 AXI register overview (base address is 0x1206_0000)

offset address name		describe	page number
0x004	AXI_CFG_LOCK register lock control		4-11
0x008	AXI_CKG	Module Clock Gating	4-12
0x020	AXI_ACTION	AXI Interface Operating Mode Register	4-13
0x100ÿ0x10 ×regions	AXI_REGION_MAP address region mapping		4-14
0x104ÿ0x10 ×regions	AXI_REGION_ATT RIB	Address Area Properties	4-15
0x108ÿ0x10 ×regions	AXI_REGION_SCR MBL	Address area address scrambling mode	4-18
0x200ÿ0x10 ×ports	AXI_QOS_MAP command priority mapping method		4-19
0x204ÿ0x10 ×ports	AXI_QOS_WRPRIn write command priority mapping table		4-20

offset address name		describe	page number
0x208ÿ0x10 ×ports	AXI_QOS_RDPRIn Read command priority mapping table		4-22
0x20Cÿ0x10 ×ports	AXI_QOS_ADPTn priority adaptive period mapping table		4-24
0x300ÿ0x10 ×ports	Command OSTD Limitations for AXI_OSTD_PRTn Ports		4-25
0x304ÿ0x10 ×ports	AXI_OSTD_PRT_S Tn	Command OSTD statistics for ports	4-26
0x400ÿ0x10 ×groups	AXI_OSTD_GROU Pn	Port Grouping Command OSTD	4-26
0x404ÿ0x10 ×groups	AXI_OSTD_PRI0 Priority-based	Command OSTD	4-27
0x408ÿ0x10 ×groups	AXI_OSTD_PRI1 Priority-based	Command OSTD	4-29
0x40Cÿ0x10 ×groups	AXI_OSTD_GROU P_STn	Command OSTD Statistics for Port Grouping	4-30
0x600	AXI_STATUS The working status of each port		4-30
0x610	AXI_INT_STATUS interrupt status		4-31

The value range and meaning of the variables in the AXI register offset address are shown in Table 4-5 .

Table 4-5 AXI register offset address variable table

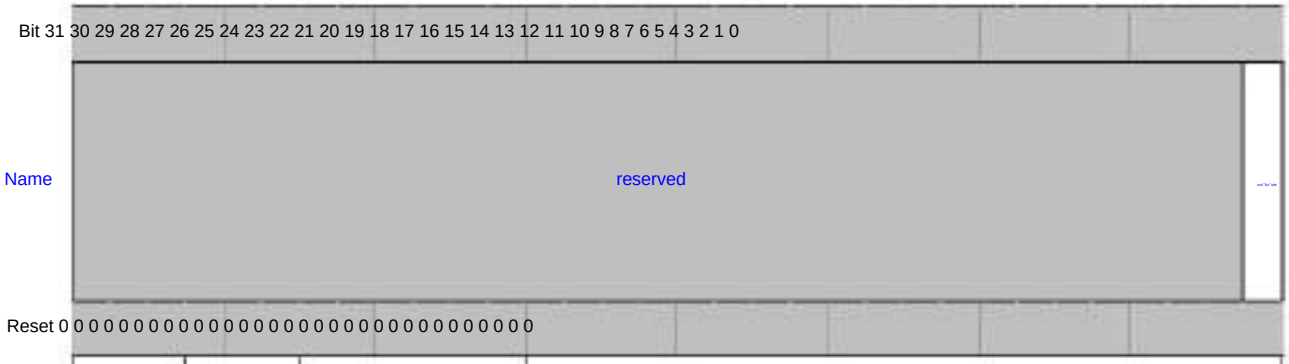
variable name	Ranges	describe
regions	0~16	The number of address areas.
ports	0ÿ8	Number of AXI ports.
groups	0~4	Port outstanding Statistics group number.

4.1.5.2 AXI register description

AXI_CFG_LOCK

AXI_CFG_LOCK is the register lock control.

Offset Address	Register Name	Total Reset Value
0x004	AXI_CFG_LOCK	0x0000_0000

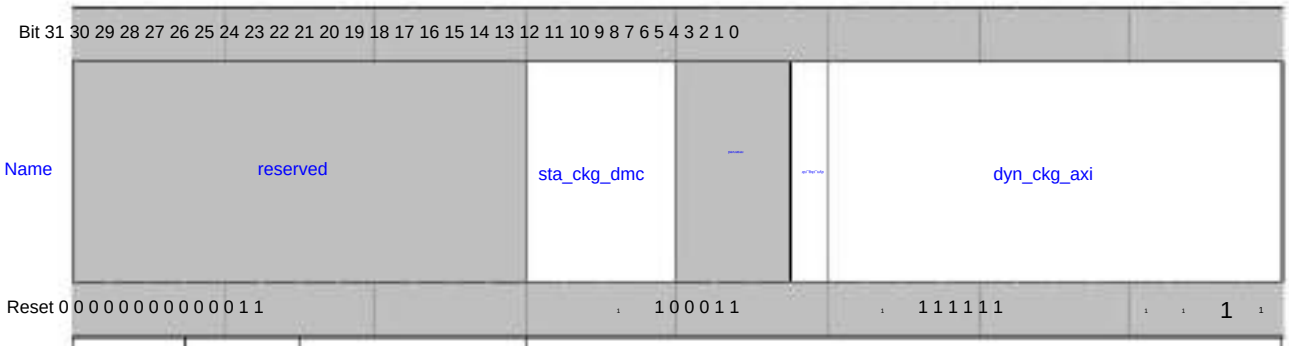


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	apb_cfg_lock	Lock all register configuration blocks (AXI_IF/SEC/ DMC/PUB) in MDDRC. 0: Not locked; 1: Locked (all AXI_IF configuration registers except this register are inaccessible to reduce power consumption).

AXI_CKG

AXI_CKG is the clock gating for the module.

Offset Address	Register Name	Total Reset Value
0x008	AXI_CKG	0x000F_1FFF



Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:16]	RW	sta_ckg_dmc	Static clock gating for each DMC. sta_ckg_dmc[n]=0: close DMCn and corresponding pub clock; sta_ckg_dmc[n]=1: open DMCn and corresponding pub clock. Note: The cases of n = 2 and n = 3 are reserved.

[15:13] RO		reserved	reserve.
[12] RW	dyn_ckg_rdr		Dynamic clock gating for the REORDER block. 0: The clock is always on; 1: When the module is idle, the clock is automatically turned off.
[11:0] RW	dyn_ckg_axi		Dynamic clock gating for individual AXI ports. dyn_ckg_axi[n]=0: the clock of AXI port n is always on; dyn_ckg_axi[n]=1: when the internal modules of AXI port n are idle, the clock is automatically turned off.

AXI_ACTION

AXI_ACTION is the AXI interface working mode register.

Offset Address	Register Name	Total Reset Value
0x020	AXI_ACTION	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Name	reserved	wr_rcv_mode	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:8]	RW	wr_rcv_mode	Anti-deadlock mode is enabled. wr_rcv_mode[n]=0: the anti-deadlock mode of port n is disabled; wr_rcv_mode[n]=1: the anti-deadlock mode of port n is enabled. Note: 1. Whether the anti-deadlock mode is enabled or not depends on the requirements of the bus architecture; 2. After the anti-deadlock mode is enabled, the write command outstanding for the AXI port is limited to 1.
[7:2]	RO	reserved	reserve.
[1]	RW	rd_wrap_split_en	wrap Read command splitting enable. 0: No splitting, wrap address wrapping is done by DMC; 1: Splitting.

[0] RW exclusive_en			The exclusive command is enabled. 0: forbidden; 1: enable.

AXI_REGION_MAP

AXI_REGION_MAP is the address region mapping.

Offset Address	Register Name	Total Reset Value
0x100ÿ0x10×regions (regions = 0ÿ15)	AXI_REGION_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgn_base_addr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	rgn_en	Enable the current address area. 0: forbidden; 1: enable.
[11]	RO	reserved	reserve.
[10:8]	RW	rgn_size	The size of the current address area. 000ÿ16MBÿ 001: 32MB; at this time rgn_base_addr/ch_offset[0] must be set to zero; 010: 64MB; at this time rgn_base_addr/ ch_offset[1:0] must be configured as zero; 011: 128MB; at this time rgn_base_addr/ ch_offset[2:0] must be configured as zero; 100: 256MB; at this time rgn_base_addr/ ch_offset[3:0] must be set to zero; 101: 512MB; at this time rgn_base_addr/ ch _offset[4:0] must be set to zero; 110: 1GB; at this time rgn_base_addr/ ch _offset[5:0] must be configured as zero; 111: 2GB; at this time rgn_base_addr/ ch _offset[6:0] must be configured as zero.

			Notice: 1. The above configuration takes a 32bits address as an example. If the address bit width is different, the meaning of the configuration will be different. For example: For 40bits address: 0x3: 32GB; at this time rgn_base_addr[2:0] must be configured as zero; 2. When two-channel interleaving, rgn_size cannot be configured as 0; when four-channel interleaving, rgn_size cannot be configured as 0 or 1.
[7:0] RW	rgn_base_addr		The base address (higher eight bits) of the current address area. Notice: Since only the upper eight bits of the address can be set, the granularity of the area address alignment varies with the address bit width. For example: For a 32bits address, the lower 24 bits of the base address of the address area are zero, and the area address is aligned by 16MB; for a 40bits address, the lower 32 bits of the base address of the address area are zero, and the area address is aligned by 4GB. The current version only supports 32bit address width.

AXI_REGION_ATTRIB

AXI_REGION_ATTRIB is the address region attribute.

Offset Address	Register Name	Total Reset Value
0x104ÿ0x10×regions (regions = 0ÿ15)	AXI_REGION_ATTRIB	0x0001_0004

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved | ch_offset

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.

[30:28]	RW	bnk_mod	BANK interleave granularity in the channel of the current address area (the interleave granularity varies with different devices). 8Byte*2^n (8bit device); 16Byte*2^n (16bit device); 32Byte*2^n (32bit device); 64Byte*2^n (64bit device); where n=0~7. Note: The bank interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).
[27:26]	RO	reserved	reserve.
[25:24]	RW	rnk_mod	Intra-lane RANK interleaving mode for the current address region. 00: use DMC internal configuration; 01: Single RANK address is independent; 10: Double RANK addresses are interleaved; 11: Four RANK addresses are interleaved. The current version has only one channel and only supports single-channel mode, and this channel only supports one rank.
[23:19]	RO	reserved	reserve.
[18:16]	RW	addr_aligned	The address boundary alignment granularity of the current address region. 000: 8Byte (this item can only be selected when the DMC data bit width is 64bit); 001ÿ16Byteÿ 010ÿ32Byteÿ 011ÿ64Byteÿ 100ÿ128Byteÿ 101ÿ256Byteÿ 110ÿ512Byteÿ 111: 1KByte; Note: 1. Commands that cross this address alignment boundary will be split; 2. The address alignment granularity must be less than or equal to the bank interleaving granularity (bnk_mod); 3. When address interleaving, the address alignment granularity must be less than or equal to the address interleaving granularity (ch_intlv); 4. When the address is independent, the address alignment granularity must be smaller than or equal to the PAGE size of the DDR device.

[15:8] RW ch_offset			The offset address (higher eight bits) of the current address area in the channel. Note: This address is used to replace the upper eight bits of the address in the channel to realize the offset of the mapped address in the channel, which will be different due to the different address bit width. For example: For a 32bits address, you can replace the address after channel mapping [31:24]; For a 40bits address, you can replace the address after channel mapping [39:32]; The current version only supports 32bit address width.
[7:6] RO		reserved	reserve.
[5:4] RW ch_intlv			The address interleaving granularity of the current address area (in single channel address independent mode, this configuration is invalid). 00ÿ128Byteÿ 01ÿ256Byteÿ 10ÿ512Byteÿ 11: 1KByte; Note: 1. Commands are distributed to multiple channels alternately with this granularity as the boundary; 2. When channels are interleaved, the address interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).
[3:2] RW ch_mode			Channel mapping mode for the current address region. 00: no mapping; 01: Mapped to a single channel, the address is independent; 10: Mapping to dual channels, address interleaving; 11: Mapping to four channels, address interleaving. Note: A command that attempts to access an unmapped address area will be treated as an error command: report an interrupt, record command information, and the AXI bus returns a SLVERR response. The current version has only one channel and only supports single-channel mode.

[1:0] RW	ch_start		The mapping start channel of the current address area. 00: channel 0; 01: channel 1; 10: channel 2; 11: Channel 3. Note: When the mapping mode is single channel, the mapping start channel can be any channel; when the mapping mode is dual channel, the mapping starting channel must be channel 0 (0/1 channel interleaving) or channel 2 (2/3 channel address interleaving); when the mapping mode is four channels, the mapping start channel must be channel 0 (0/1/2/3 channel address interleaving). The current version has only one channel and only supports single-channel mode.

AXI_REGION_SCRMBL

AXI_REGION_SCRMBL is the address scrambling mode of the address region.

Offset Address	Register Name	Total Reset Value
0x108ÿ0x10×regions (regions = 0ÿ15)	AXI_REGION_SCRMBL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	bnk_scrmbl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve. Need to be fixed at 0.
[3:0]	RW	bnk_scrmbl	BANK address scrambling mode. 0x0: no scrambling code; When single channel: 0x1ÿaddr[14:12] = addr[14:12] xor addr[19:17]ÿ 0x2ÿaddr[14:12] = addr[14:12] xor addr[20:18]ÿ 0x3ÿaddr[14:12] = addr[14:12] xor addr[21:19]ÿ 0x4ÿaddr[14:12] = addr[14:12] xor addr[22:20]ÿ 0x5ÿaddr[14:12] = addr[14:12] xor addr[23:21]ÿ 0x6ÿaddr[14:12] = addr[14:12] xor addr[24:22]ÿ 0x7: addr[14:12] = addr[14:12] xor addr[25:23]; Others: reserved. In case of dual channel (on the basis of ch_scrmbl address exchange, perform

			bnk_scrmblÿÿ 0x1ÿaddr[15:13] = addr[15:13] xor addr[20:18]ÿ 0x2ÿaddr[15:13] = addr[15:13] xor addr[21:19]ÿ 0x3ÿaddr[15:13] = addr[15:13] xor addr[22:20]ÿ 0x4ÿaddr[15:13] = addr[15:13] xor addr[23:21]ÿ 0x5ÿaddr[15:13] = addr[15:13] xor addr[24:22]ÿ 0x6ÿaddr[15:13] = addr[15:13] xor addr[25:23]ÿ 0x7: addr[15:13] = addr[15:13] xor addr[26:24]; Others: reserved. Note: addr is the bus address.

AXI_QOS_MAP

AXI_QOS_MAP is the command priority mapping method.

Offset Address	Register Name	Total Reset Value
0x200ÿ0x10×ports (ports = 0ÿ8)	AXI_QOS_MAP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	~~	~~	reserved	~~	id_map_idx
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

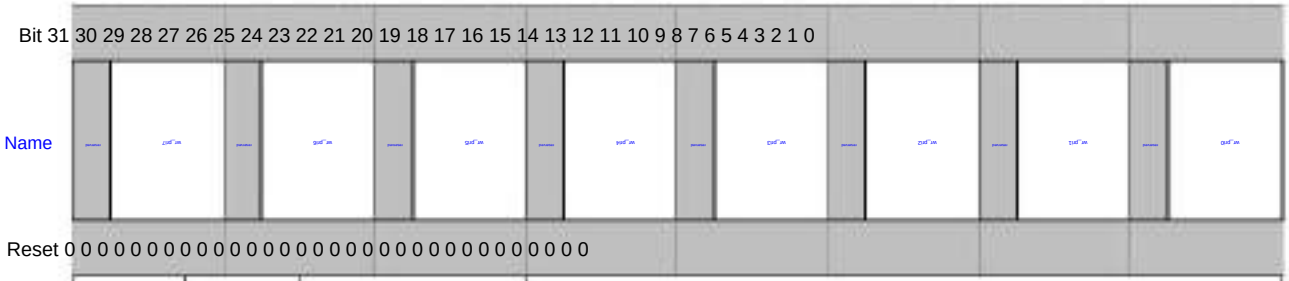
Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21]	RW	qos_rever	QoS inversion enable (for priority arbitration of read and write commands within the same port). 0: When axqos=0, it is the lowest priority; 1: When axqos=0, it is the highest priority. Notice: This register is valid when rw_arb_mode==1.

[20] RW rw_arb_mode			Arbitration mode for read and write commands within the same port. 0: Based on command read and write type: a. First-come-first-arbitration; b. When arriving at the same time (or being back-pressed at the same time), the order of the first read command and then the write command will be arbitrated in turn; 1: Based on command priority: a. First-come-first-served arbitration; b. When arriving at the same time (or being back-pressed at the same time), it will be arbitrated according to the order priority judgment; c. If the priorities are the same, the arbitration will be based on the LRU principle Arbitration Order.
[19:13] RO		reserved	reserve.
[12] RW pri_map_mode			Read and write command priority mapping mode. 0: 3-bit channel-associated signal mapping index using read and write commands; 1: Use any 3bits mapping index in the lower 16 bits of the command ID. Description: Use one of the above two methods to get the mapped index, and then look up the table from the priority (the lookup table here refers to AXI_QOS_WRPRI or AXI_QOS_RDPRI register content) maps out the command priority
[11:0] RW id_map_idx			When mapping priority by command ID, this register configures the 3 selection bits of the command ID: id_map_idx[11:8]: select any 1 bit of the lower 16 bits of the command ID as idx[2]; id_map_idx[7:4]: select any 1 bit of the lower 16 bits of the command ID as idx[1]; id_map_idx[3:0]: Select any 1 bit in the lower 16 bits of the command ID as idx[0]. For example: id_map_idx is configured as 0x3A0, then {ID[3],ID[10],ID[0]} of the command ID will be combined into an index idx[2:0], which is used to look up the table from the priority (the lookup table here refers to The command priority is mapped in the AXI_QOS_WRPRI or AXI_QOS_RDPRI register content). Note: The command ID here is the original ID of the command.

AXI_QOS_WRPRIn

AXI_QOS_WRPRIn is the write command priority mapping table.

Offset Address	Register Name	Total Reset Value
0x204ÿ0x10×ports (ports = 0ÿ8)	AXI_QOS_WRPRI	0x0000_0000



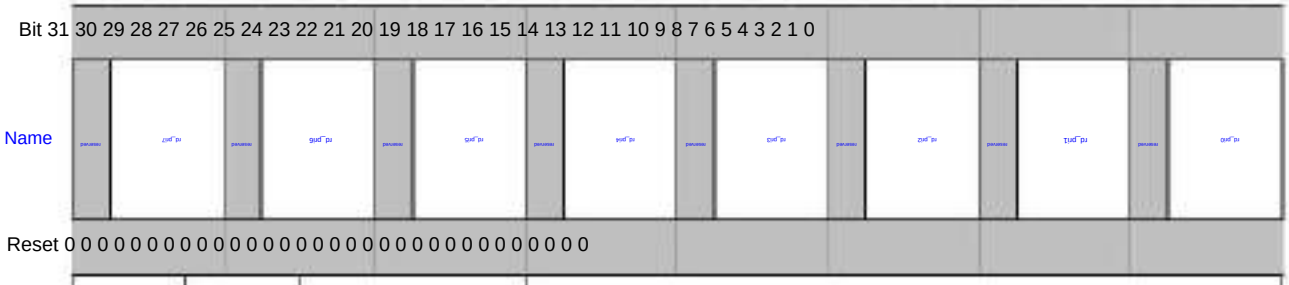
Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	wr_pri7	The priority configuration when the write command is mapped to 7. 0x0: the highest priority; …… 0x7: lowest priority.
[27]	RO	reserved	reserve.
[26:24]	RW	wr_pri6	The priority configuration when the write command is mapped to 6. 0x0: the highest priority; …… 0x7: lowest priority.
[23]	RO	reserved	reserve.
[22:20]	RW	wr_pri5	The priority configuration when the write command is mapped to 5. 0x0: the highest priority; …… 0x7: lowest priority.
[19]	RO	reserved	reserve.
[18:16]	RW	wr_pri4	The priority configuration when the write command is mapped to 4. 0x0: the highest priority; …… 0x7: lowest priority.
[15]	RO	reserved	reserve.
[14:12]	RW	wr_pri3	The priority configuration when the write command is mapped to 3. 0x0: the highest priority; …… 0x7: lowest priority.

[11] RO		reserved	reserve.
[10:8] RW	wr_pri2		The priority configuration when the write command is mapped to 2. 0x0: the highest priority; …… 0x7: lowest priority.
[7]	RO	reserved	reserve.
[6:4] RW	wr_pri1		The priority configuration when the write command is mapped to 1. 0x0: the highest priority; …… 0x7: lowest priority.
[3]	RO	reserved	reserve.
[2:0] RW	wr_pri0		The priority configuration when the write command is mapped to 0. 0x0: the highest priority; …… 0x7: lowest priority.

AXI_QOS_RDPRIn

AXI_QOS_RDPRIn is the priority mapping table for read commands.

Offset Address	Register Name	Total Reset Value
0x208ÿ0x10×ports (ports = 0ÿ8)	AXI_QOS_RDPRIn	0x0000_0000



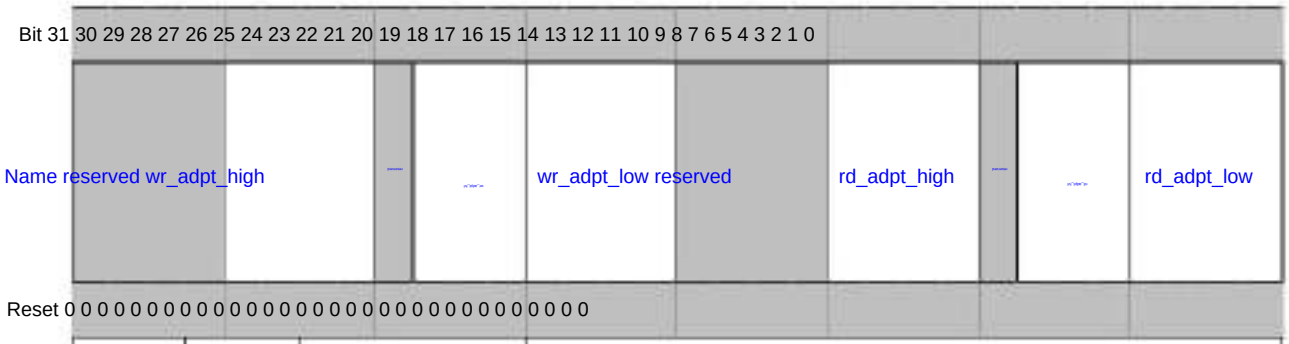
Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	rd_pri7	The priority configuration when the read command is mapped to 7. 0x0: the highest priority; …… 0x7: lowest priority.
[27]	RO	reserved	reserve.

[26:24] RW	rd_pri6		The priority configuration when the read command is mapped to 6. 0x0: the highest priority; …… 0x7: lowest priority.
[23] RO		reserved	reserve.
[22:20] RW	rd_pri5		The priority configuration when the read command is mapped to 5. 0x0: the highest priority; …… 0x7: lowest priority.
[19] RO		reserved	reserve.
[18:16] RW	rd_pri4		The priority configuration when the read command is mapped to 4. 0x0: the highest priority; …… 0x7: lowest priority.
[15] RO		reserved	reserve.
[14:12] RW	rd_pri3		The priority configuration when the read command is mapped to 3. 0x0: the highest priority; …… 0x7: lowest priority.
[11] RO		reserved	reserve.
[10:8] RW	rd_pri2		The priority configuration when the read command is mapped to 2. 0x0: the highest priority; …… 0x7: lowest priority.
[7]	RO	reserved	reserve.
[6:4] RW	rd_pri1		The priority configuration when the read command is mapped to 1. 0x0: the highest priority; …… 0x7: lowest priority.
[3]	RO	reserved	reserve.
[2:0] RW	rd_pri0		The priority configuration when the read command map is 0. 0x0: the highest priority; …… 0x7: lowest priority.

AXI_QOS_ADPTn

AXI_QOS_ADPTn is the priority adaptive period mapping table.

Offset Address	Register Name	Total Reset Value
0x20Cÿ0x10×ports (ports = 0ÿ8)	AXI_QOS_ADPTn	0x0000_0000



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	wr_adpt_high	Write command priority adaptive cycle configuration (high bit). 0x0: disable the priority adaptive function; 0x1~0xF: N*16 clock cycles. Note: Whenever the self-adaptation period arrives, the command priority will be automatically increased by one level, and the highest priority can be increased to the second highest priority.
[23]	RO	reserved	reserve.
[22:20]	RW	wr_adpt_lvl	Write command priority adaptive cycle configuration watermark. 0x0~0x1: Reserved; 0x2ÿ0x7: When the command priority is higher than or equal to this waterline, use the high-level configuration, otherwise use the low-level configuration. Example: 0x5: Write commands with priority 2~5 use wr_adpt_high, and write commands with priority 6~7 use wr_adpt_low.
[19:16]	RW	wr_adpt_low	Write command priority adaptive cycle configuration (low gear). 0x0: disable the priority adaptive function; 0x1~0xF: N*16 clock cycles. illustrate: Whenever the adaptive cycle arrives, the priority of the command is automatically raised by one level, and the highest priority can be raised to the second highest priority.
[15:12]	RO	reserved	reserve.

[11:8]	RW	rd_adpt_high	Read command priority adaptive cycle configuration (high bit). 0x0: disable the priority adaptive function; 0x1~0xF: N*16 clock cycles. Note: Whenever the self-adaptation period arrives, the command priority will be automatically increased by one level, and the highest priority can be increased to the second highest priority.
[7]	RO	reserved	reserve.
[6:4]	RW	rd_adpt_lvl	Read command priority adaptive cycle configuration watermark. 0x0ÿ0x1: Reserved; 0x2ÿ0x7: When the command priority is higher than or equal to this waterline, use the high-level configuration, otherwise use the low-level configuration. Example: 0x5: Use rd_adpt_high for read commands with priority 2~5, and use rd_adpt_low for read commands with priority 6~7.
[3:0]	RW	rd_adpt_low	Read command priority adaptive cycle configuration (low gear). 0x0: disable the priority adaptive function; 0x1~0xF: N*16 clock cycles. Note: Whenever the self-adaptation period arrives, the command priority will be automatically increased by one level, and the highest priority can be increased to the second highest priority.

AXI_OSTD_PRTn

AXI_OSTD_PRTn is the command OSTD limit for the port.

Offset Address	Register Name	Total Reset Value
0x300ÿ0x10×ports (ports = 0ÿ8)	AXI_OSTD_PRTn	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	prt_ostd_lvl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x300ÿ0x10×ports (ports = 0ÿ8)	AXI_OSTD_PRTn	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / prt_ostd_lvl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[6:0]	RW prt_ostd_lvl	Port's command OSTD watermark. 0x00: Do not limit the number of command OSTDs of this port; 0x01~0x7F: The maximum command OSTD number allowed by the current port. Notice: 1. The number of OSTD here is essentially the number of commands in the subsequent module QOSBUF (the same below); 2. The waterline setting cannot be greater than the command queue depth of the QOSBUF configured by the parameters (the same below).

AXI_OSTD_PRT_STn

AXI_OSTD_PRT_STn is the command OSTD statistics value of the port.

Offset Address	Register Name	Total Reset Value
0x304ÿ0x10×ports (ports = 0ÿ8)	AXI_OSTD_PRT_STn	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / prt_ostd_st
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:7]	RO	reserved	reserve.
[6:0]	RO	Command OSTD statistics	for the prt_ostd_st port.

AXI_OSTD_GROUPn

AXI_OSTD_GROUPn is the command OSTD for port grouping.

Offset Address	Register Name	Total Reset Value
0x400ÿ0x10×groups (groups = 0ÿ3)	AXI_OSTD_GROUP	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7	6 5 4 3 2 1 0
Name	reserved	group_ostd_sel	reserved	group_ostd_lvl
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	group_ostd_sel	Group port selection: group_ostd_sel[n]=0: port n is not selected; group_ostd_sel[n]=1: port n is selected. Notice: Only the selected port will participate in the OSTD statistics of the group.
[15:7]	RO	reserved	reserve.
[6:0]	RW	group_ostd_lvl	Grouped commands OSTD waterline. 0x00: No limit to the number of command OSTDs in this group; 0x01~0x7F: The maximum cumulative number of command OSTDs allowed in the current group. Notice: 1. The group command OSTD is the sum of the command OSTD of the port selected by the current group; 2. After the watermark is exceeded, all ports in the group will be blocked.

AXI_OSTD_PRI0

AXI_OSTD_PRI0 is the priority-based command OSTD within each port group.

Offset Address	Register Name	Total Reset Value
0x404ÿ0x10×groups (groups = 0ÿ3)	AXI_OSTD_PRI0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	pri3_ostd_lvl															—	pri2_ostd_lvl													—	pri1_ostd_lvl															reserved																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:24]	RW	pri3_ostd_lvl	Priority 3 command OSTD watermark. 0x00: Do not limit the number of accumulated command OSTD of the selected group; 0x01ÿ0x7F: When the number of accumulated command OSTD of the selected group reaches this waterline, only the commands with priority higher than 1 are allowed to pass. Note: 1. The statistics and limitation of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, the low priority commands may no longer be blocked because the priority is raised.
[23]	RO	reserved	reserve.
[22:16]	RW	pri2_ostd_lvl	Priority 2 command OSTD watermark. 0x00: Do not limit the number of accumulated command OSTD of the selected group; 0x01ÿ0x7F: When the number of accumulated command OSTD of the selected group reaches this waterline, only the commands with priority higher than 1 are allowed to pass. Notice: 1. The statistics and limitation of command OSTD are based on port grouping; 2. If the priority transfer function is enabled, low priority commands may no longer be blocked because the priority is raised.
[15]	RO	reserved	reserve.
[14:8]	RW	pri1_ostd_lvl	Priority 1 command OSTD watermark. 0x00: Do not limit the number of accumulated command OSTD of the selected group; 0x01ÿ0x7F: When the number of accumulated command OSTD of the selected group reaches this waterline, only the commands with priority higher than 1 are allowed to pass. Note: 1. The statistics and limitation of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, the low priority commands may no longer be blocked because the priority is raised.

[7:0] RO		reserved	reserve.

AXI_OSTD_PRI1

AXI_OSTD_PRI1 is the priority-based command OSTD within each port group.

Offset Address	Register Name	Total Reset Value
0x408ÿ0x10×groups (groups = 0ÿ3)	AXI_OSTD_PRI1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	pri7_ostd_lvl							—	pri6_ostd_lvl							—	pri5_ostd_lvl							—	pri4_ostd_lvl						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:24]	RW	pri7_ostd_lvl	OSTD waterline of priority 7 commands: 0x00: no limit to the number of cumulative command OSTDs of the selected group; 0x01~0x7F: when the number of cumulative command OSTDs of the selected group reaches this watermark, only those with priority higher than 1 are allowed The order passed. Note: 1. The statistics and limitation of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, the low priority commands may no longer be blocked because the priority is raised.
[23]	RO	reserved	reserve.
[22:16]	RW	pri6_ostd_lvl	Command OSTD waterline of priority 6: 0x00: no limit to the number of cumulative command OSTDs of the selected group; 0x01~0x7F: when the number of cumulative command OSTDs of the selected group reaches this watermark, only the number of priority higher than 1 is allowed The order passed. Note: 1. The statistics and limitation of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, the low priority commands may no longer be blocked because the priority is raised.
[15]	RO	reserved	reserve.

[14:8] RW	pri5_ostd_lvl		Command OSTD waterline for priority 5: 0x00: Do not limit the cumulative command OSTD number of the selected group; 0x01~0x7F: When the cumulative number of OSTD commands of the selected group reaches this watermark, only the commands with priority higher than 1 are allowed to pass. Note: 1. The statistics and limits of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, low priority commands may no longer be blocked because the priority is raised.
[7]	RO	reserved	reserve.
[6:0] RW	pri4_ostd_lvl		Command OSTD waterline for priority 4: 0x00: Do not limit the number of accumulated command OSTD of the selected group; 0x01ÿ0x7F: When the number of accumulated command OSTD of the selected group reaches this waterline, only the commands with priority higher than 1 are allowed to pass. Note: 1. The statistics and limitation of the command OSTD are based on port grouping; 2. If the priority transfer function is enabled, the low priority commands may no longer be blocked because the priority is raised.

AXI_OSTD_GROUP_STn

AXI_OSTD_GROUP_STn is the command OSTD statistics value of the port group.

Offset Address	Register Name	Total Reset Value
0x40Cÿ0x10×groups (groups = 0ÿ3)	AXI_OSTD_GROUP_ST	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / group_ostd_st
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6:0]	RO	group_ostd_st	Command OSTD statistics for port groups.

AXI_STATUS

AXI_STATUS is the working status of each port.

Offset Address	Register Name	Total Reset Value
0x600	AXI_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	axi_if_busy
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RO	axi_if_busy	The working status of each AXI port. axi_prt_busy[n]=0: AXI port n is idle; axi_prt_busy[n]=1: AXI port n is processing commands or data.

AXI_INT_STATUS

AXI_INT_STATUS is the interrupt status.

Offset Address	Register Name	Total Reset Value
0x610	AXI_INT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	int_ports
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RO	int_ports	Interrupt source indication. interrupt_ports[n]=1: Interrupts come from port n. Notice: When the command fails the security permission check and the interrupt is enabled, the corresponding port will generate an interrupt.

4.1.6 QOSBUF Register

4.1.6.1 QOSBUF register overview

The QOSBUF register overview is shown in Table 4-6

Table 4-6 QOSBUF register overview (base address is 0x1206_4000)

offset address	name	describe	page number
0x000	QOSB_PUSH_CTRL	Configure the register of QosBuf Push function	4-35
0x004	QOSB_ADPT_CTRL	configures the adpt function of QosBuf	4-35
0x008ÿ 0x4×fids	QOSB_FLUX_ID	Traffic match ID of QosBuf	4-36
0x024ÿ 0x4×fids	QOSB_FLUX_ID_MASK	Mask register of ID of QosBuf traffic statistics	4-36
0x040	QOSB_FLUX_PRD	QosBuf traffic statistics cycle register	4-37
0x044ÿ 0x4×fgps	QOSB_FLUX_LVL	Flow statistics waterline of QosBuf	4-37
0x064	QOSB_FLUX_EN	QosBuf traffic statistics function enable register	4-38
0x068ÿ 0x4× chance	QOSB_BANK_CTRL	QosBuf's bank rotating control register	4-38
0x078ÿ 0x4× chance	QOSB_GREEN_CTRL	Green Channel Control Register for QosBuf	4-39
0x088	QOSB_BUF_BYP	QosBuf bypass function control register	4-40
0x08Cÿ 0x4× chance	QOSB_WBUF_CTRL	QosBuf Write Command Priority Adjustment Control Register	4-40
0x09C	QOSB_WRTOUT0	QosBuf write command timeout configuration register 0	4-41
0x0A0	QOSB_WRTOUT1	QosBuf write command timeout configuration register 1	4-42
0x0A4	QOSB_WRTOUT2	QosBuf write command timeout configuration register 2	4-43
0x0A8	QOSB_WRTOUT3	QosBuf write command timeout configuration register 3	4-43
0x0AC	QOSB_RDTOUT0	QosBuf read command timeout configuration register 0	4-45
0x0B0	QOSB_RDTOUT1	QosBuf read command timeout configuration register 1	4-45
0x0B4	QOSB_RDTOUT2	QosBuf read command timeout configuration register 2	4-46
0x0B8	QOSB_RDTOUT3	QosBuf read command timeout configuration register 3	4-47
0x0BC	QOSB_WRTOUT_MAP	QosBuf write command timeout mapping control register	4-48
0x0D0	QOSB_RDTOUT_MAP	QosBuf read command timeout mapping control register	4-49

offset address name		describe	page number
0x0D4	QOSB_WRAGE0	QosBuf write command aging configuration register 0	4-50
0x0D8	QOSB_WRAGE1	QosBuf write command aging configuration register 1	4-51
0x0DC	QOSB_RDAGE0	QosBuf read command aging configuration register 0	4-52
0x0E0	QOSB_RDAGE1	QosBuf read command aging configuration register 1	4-53
0x0E4	QOSB_WRAGE_MA P	QosBuf write command aging mapping control register 4-54	
0x0E8	QOSB_RDAGE_MA P	QosBuf read command aging mapping control register 4-55	
0x0EC	QOSB_ROWHIT_PR ILVL	QosBuf's row hit priority watermark register 4-56	
0x0F0	QOSB_ROWHIT_PR I	QosBuf row hit priority control register 4-58	
0x0F4	QOSB_ROWHIT_CT RL	Enable control of row hit of QosBuf	4-59
0x108	QOSB_CKG_CFG Clock control register for QosBuf		4-60
0x10Cÿ 0x4× chance	QOSB_DMC_LVL QosBuf's waterline control register for commands entering the DMC		4-60
0x120	QOSB_CFG_PERF QosBuf performance statistics mode configuration register 4-61		
0x124	QOSB_CMD_SUM Cumulative register for QosBuf command count		4-62
0x128	QOSB_SLOT_STAT 0	QosBuf's queue status register 0	4-62
0x12C	QOSB_SLOT_STAT 1	QosBuf's queue status register 1	4-63
0x130	QOSB_SLOT_STAT 2	QosBuf's queue status register 2	4-63
0x134	QOSB_SLOT_STAT 3	QosBuf's queue status register 3	4-64
0x140ÿ 0x4× chans	QOSB_WBUF_STA T0	Write buf status register 0 of QosBuf	4-64
0x150ÿ 0x4× chans	QOSB_WBUF_STA T1	Write buf status register 1 of QosBuf	4-64
0x160ÿ 0x4× chance	QOSB_RDRBUF_ST AT	buf status register of the Reorder module	4-65

offset address	name	describe	page number
0x170	QOSB_INTMSK	QosBuf interrupt mask register	4-65
0x174	QOSB_RINT	QosBuf raw interrupt register	4-66
0x178	QOSB_INTSTS	QOSBUF Interrupt Status Register	4-67
0x180	QOSB_CMD_CNT	Statistical register of how many commands are currently in QOSBUF device	4-67
0x190ÿ 0x4× chance	QOSB_RNK_CNT	The statistics register of how many commands are currently in each rank in QOSBUF	4-67
0x1A0ÿ 0x4× chance	QOSB_BNK_CNT0	Statistics register 0 of how many commands are currently in each Bank in QOSBUF	4-68
0x1B0ÿ 0x4× chance	QOSB_BNK_CNT1	Statistical register 1 of how many commands each Bank currently has in QOSBUF	4-68
0x1C0ÿ 0x4× chance	QOSB_BNK_CNT2	Statistics register 2 of how many commands are currently in each Bank in QOSBUF	4-69
0x1D0ÿ 0x4× chance	QOSB_BNK_CNT3	Statistical register 3 of how many commands each Bank currently has in QOSBUF	4-69
0x1E0	QOSB_OSTD_CNT	How many channels are currently in QOSBUF Statistics Registers for Oustanding Commands	4-70
0x1E4	QOSB_WR_CMD_SONE	QosBuf Accumulation register for write command count	4-70
0x1E8	QOSB_RD_CMD_SONE	Accumulation register for QosBuf read command count	4-71
0x1F0	QOSB_TIMEOUT_MODE	Timeout Mode Selection Register 4-71 in QOSBUF	
0x1F4	QOSB_WBUF_PRI_CTRL	Write wbuf priority adjustment control register in QOSBUF	4-72
0x1F8	QOSB_RHIT_CTRL	rowhit priority adjustment control register in QOSBUF device	4-72

The value range and meaning of variables in the QOSBUF register offset address are shown in Table 4-7 .

Table 4-7 QOSBUF register offset address variable table

variable name	Ranges	describe
chance	0ÿ1	Number of channels
fgps	0ÿ7	Number of groups for traffic statistics
fids	0ÿ6	The number of traffic statistics matching id

4.1.6.2 QOSBUF register description

QOSB_PUSH_CTRL

QOSB_PUSH_CTRL is the register for configuring the QosBuf Push function.

Offset Address	Register Name	Total Reset Value
0x000	QOSB_PUSH_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2]	RW	mid_push_en	Push enable for commands with the same MID. 0: push function is disabled; 1: push function is enabled.
[1]	RW	addr_push_en	Push enable for commands with the same address. 0: push function is disabled; 1: push function is enabled.
[0]	RW	id_push_en	Push enable for commands with the same ID. 0: push function is disabled; 1: push function is enabled.

QOSB_ADPT_CTRL

QOSB_ADPT_CTRL is to configure the adpt function of QosBuf.

Offset Address	Register Name	Total Reset Value
0x004	QOSB_ADPT_CTRL	0x0000_0FF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																adpt_share_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name	Description
[31:20]	RO reserved	reserve.
[19:4]	RW adpt_share_cnt	Low shared counter for the Adapt function. When the counter is decremented to 0, the high-bit counter corresponding to each cmd is decremented by 1.
[3:1]	RO reserved	reserve.
[0]	RW adpt_en	Adapt function enable control. 0: Adapt function is off; 1: Adapt function is on.

QOSB_FLUX_ID

QOSB_FLUX_ID is the flow matching ID of QosBuf.

Offset Address	Register Name	Total Reset Value
0x008ÿ0x4×fids (fids = 0ÿ6)	QOSB_FLUX_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW flux_id	The matching ID used for traffic statistics has 0~6 IDs in total, and each ID corresponds to a statistical group; if it is different from these 7 IDs, the traffic will be classified into the default group.

QOSB_FLUX_ID_MASK

QOSB_FLUX_ID_MASK is the Mask register of the ID of QosBuf's traffic statistics.

Offset Address	Register Name	Total Reset Value
0x024ÿ0x4×fids (fids = 0ÿ6)	QOSB_FLUX_ID_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	flux_id_mask	Corresponding to the QOSB_FLUX_ID register, it is used for ID MASK. 0: Indicates that the bit of the corresponding ID is ignored; 1: Indicates that the bit of the corresponding ID participates in the comparison.

QOSB_FLOW_PRD

QOSB_FLUX_PRD is the flow statistics period register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x040	QOSB_FLOW_PRD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stream_prod															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	flux_prd	Traffic statistics cycle.

QOSB_FLUX_LVL

QOSB_FLUX_LVL is the flow statistics waterline of QosBuf.

Offset Address	Register Name	Total Reset Value
0x044ÿ0x4×fgps (fgps = 0ÿ7)	QOSB_FLUX_LVL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved flux_lvl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	flux_lvl	Watermark settings for traffic statistics. During the statistical period, when the traffic is higher than the watermark, the priority of the command will be reduced to the lowest.

QOSB_FLOW_EN

QOSB_FLUX_EN is the enable register for the traffic statistics function of QosBuf.

Offset Address	Register Name	Total Reset Value
0x064	QOSB_FLOW_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	flux_en	The traffic statistics function is enabled. 0: indicates that the traffic statistics function is disabled; 1: Indicates that the traffic statistics function is enabled.

QOSB_BANK_CTRL

QOSB_BANK_CTRL is the bank rotating control register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x068ÿ0x4×chans (chance = 0ÿ1)	QOSB_BANK_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved		ba_cnt_lvl	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	ba_cnt_lvl	Bank conflict waterline configuration, when the number of commands with the same bank address is higher than the waterline, it is considered that there is a bank conflict. Otherwise, it is considered that there is no bank conflict.
[3:1]	RO	reserved	reserve.
[0]	RW	ba_intleave_en	Bank rotating enable control of QosBuf. 0: Bank rotating function is disabled; 1: Bank rotating function is enabled.

QOSB_GREEN_CTRL

QOSB_GREEN_CTRL is the green channel control register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x078ÿ0x4×chans (chance = 0ÿ1)	QOSB_GREEN_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved		green_lvl	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.

[7:4] RW green_lvl			Green Channel Waterline. That is, the vacancy above the waterline is reserved for the green channel. If the queue of dmc is 12 and the waterline is set to 9, then 10 and 11 are reserved for the green channel. Note: Due to the pipeline problem, when the configuration is N, the number of actually passed commands is N+1. In addition, this register cannot be dynamically configured during access.
[3:1] RO		reserved	reserve.
[0] RW green_en			The green channel function is enabled. (Note that the channel is not controlled separately here, and needs to be optimized in the future) 0: Indicates that the function is turned off; 1: Indicates that the function is enabled.

QOSB_BUF_BYP

QOSB_BUF_BYP is the bypass function control register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x088	QOSB_BUF_BYP	0x0000_0000

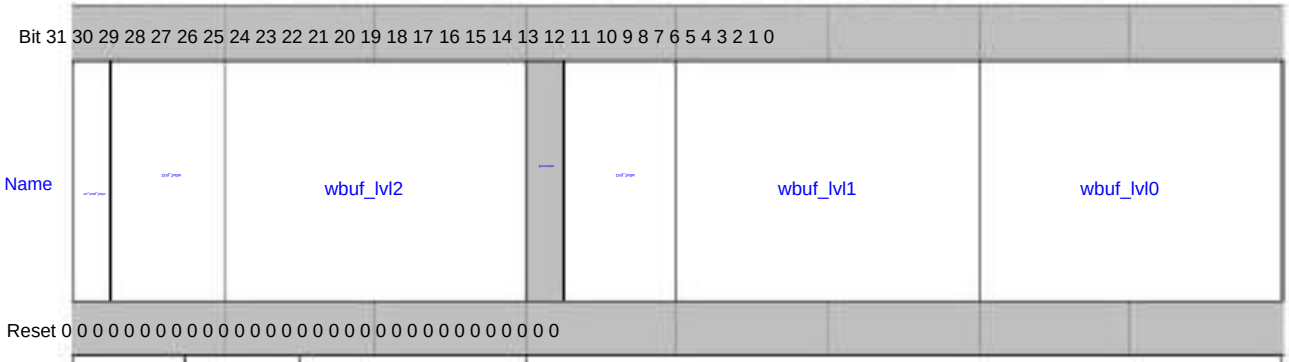
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2] RO		reserved	reserve.
[1:0] RW		qos_buf_byp	Bypass control of Qos buf. X0: indicates mandatory non-bypass, that is, when it is set to 00 or 10, all commands must enter qosbuf; 01: indicates whether to bypass automatically according to the status of the queue in dmc; 11: indicates mandatory bypass, and all commands will not enter qosbuf (Note: These modes need to be configured before the visit begins, and cannot be dynamically configured during the visit)

QOSB_WBUF_CTRL

QOSB_WBUF_CTRL is the write command priority adjustment control register for QosBuf.

Offset Address	Register Name	Total Reset Value
0x08Cÿ0x4×chans (chance = 0ÿ1)	QOSB_WBUF_CTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	wbuf_ptun_en	Write tuning level adjustment enable. 0: Indicates that the function is off; 1: Indicates that the function is enabled.
[30:28]	RW	wbuf_pri2	The priority corresponding to watermark 2 of wbuf.
[27:20]	RW	wbuf_lvl2	Waterline 2 of wbuf. When the number of commands passes through the waterline from bottom to top, if the priority of all write commands is lower than wbuf_pri2, it will be configured as wbuf_pri2; if it is higher than wbuf_pri2, the priority will be restored. (Note, this waterline cannot be dynamically configured, otherwise it may cause the write buf adaptive function to fail)
[19]	RO	reserved	reserve.
[18:16]	RW	wbuf_pri1	The priority corresponding to watermark 1 of wbuf.
[15:8]	RW	wbuf_lvl1	Waterline 1 of wbuf. When the number of commands crosses the waterline from bottom to top, or from top to bottom, if the priority of all write commands is lower than wbuf_pri1, configure it as wbuf_pri1; if it is higher than wbuf_pri1, Then the priority will be restored. (Note that this waterline cannot be dynamically configured, otherwise it may cause the write buf adaptive function to fail)
[7:0]	RW	wbuf_lvl0	The waterline of wbuf is 0. When the number of commands crosses the waterline from top to bottom, the priority of all write commands will be reduced to the lowest. (Note that this waterline cannot be dynamically configured, otherwise it may cause the write buf adaptive function to fail)

QOSB_WRTOUT0

QOSB_WRTOUT0 configures register 0 for the write command timeout of QosBuf.

Offset Address	Register Name	Total Reset Value
0x09C	QOSB_WRTOUT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout3								wr_tout2								wr_tout1								wr_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout3	Write command timeout configuration (gear 3). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[23:16]	RW	wr_tout2	Write command timeout configuration (gear 2). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[15:8]	RW	wr_tout1	Write command timeout configuration (gear 1). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[7:0]	RW	wr_tout0	Write command timeout configuration (gear 0). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: timeout is configured as 8bits, but the actual count is 10bits, that is, the lower two bits are fixed as zero.

QOSB_WRTOUT1

QOSB_WRTOUT1 is QosBuf write command timeout configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0A0	QOSB_WRTOUT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wr_tout7	wr_tout6	wr_tout5	wr_tout4
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout7	Write command timeout configuration (gear 7). 0x0: disable timeout function; 0x1~0xFF: n*4 clock cycles. Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[23:16]	RW	wr_tout6	Write command timeout configuration (gear 6). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[15:8]	RW	wr_tout5	Write command timeout configuration (gear 5). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[7:0]	RW	wr_tout4	Write command timeout configuration (gear 4). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: timeout is configured as 8bits, but the actual count is 10bits, that is, the lower two bits are fixed as zero.

QOSB_WRTOUT2

QOSB_WRTOUT2 is the configuration register 2 for the write command timeout of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0A4	QOSB_WRTOUT2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wr_tout11	wr_tout10	wr_tout9	wr_tout8
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout11	Write command timeout configuration (gear 11). The configuration method is the same as wr_tout0.
[23:16]	RW	wr_tout10	Write command timeout configuration (gear 10). The configuration method is the same as wr_tout0.
[15:8]	RW	wr_tout9	Write command timeout configuration (gear 9). The configuration method is the same as wr_tout0.
[7:0]	RW	wr_tout8	Write command timeout configuration (gear 8). The configuration method is the same as wr_tout0.

QOSB_WRTOUT3

QOSB_WRTOUT3 is the timeout configuration register 3 of QosBuf write command.

Offset Address	Register Name	Total Reset Value
0x0A8	QOSB_WRTOUT3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wr_tout15	wr_tout14	wr_tout13	wr_tout12
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout15	Write command timeout configuration (gear 15). The configuration method is the same as wr_tout0.
[23:16]	RW	wr_tout14	Write command timeout configuration (gear 14). The configuration method is the same as wr_tout0.
[15:8]	RW	wr_tout13	Write command timeout configuration (gear 13). The configuration method is the same as wr_tout0.
[7:0]	RW	wr_tout12	Write command timeout configuration (gear 12). The configuration method is the same as wr_tout0.

QOSB_RDTOUT0

QOSB_RDTOUT0 is the read command timeout configuration register 0 of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0AC	QOSB_RDTOUT0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	rd_tout3	rd_tout2	rd_tout1	rd_tout0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout3	Read command timeout configuration (level 3). The configuration method is the same as rd_tout0.
[23:16]	RW	rd_tout2	Read command timeout configuration (level 2). The configuration method is the same as rd_tout0.
[15:8]	RW	rd_tout1	Read command timeout configuration (level 1). The configuration method is the same as rd_tout0.
[7:0]	RW	rd_tout0	Read command timeout configuration (position 0). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.

QOSB_RDTOUT1

QOSB_RDTOUT1 is QosBuf read command timeout configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0B0	QOSB_RDTOUT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	rd_tout7	rd_tout6	rd_tout5	rd_tout4
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout7	Read command timeout configuration (level 7). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[23:16]	RW	rd_tout6	Read command timeout configuration (level 6). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[15:8]	RW	rd_tout5	Read command timeout configuration (gear 5). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[7:0]	RW	rd_tout4	Read command timeout configuration (level 4). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: timeout is configured as 8bits, but the actual count is 10bits, that is, the lower two bits are fixed as zero.

QOSB_RDTOUT2

QOSB_RDTOUT2 is the configuration register 2 for the read command timeout of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0B4	QOSB_RDTOUT2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	rd_tout11	rd_tout10	rd_tout9	rd_tout8
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout11	Read command timeout configuration (gear 11). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[23:16]	RW	rd_tout10	Read command timeout configuration (gear 10). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[15:8]	RW	rd_tout9	Read command timeout configuration (gear 9). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[7:0]	RW	rd_tout8	Read command timeout configuration (gear 8). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: timeout is configured as 8bits, but the actual count is 10bits, that is, the lower two bits are fixed as zero.

QOSB_RDTOUT3

QOSB_RDTOUT3 is the timeout configuration register 3 of QosBuf read command.

Offset Address	Register Name	Total Reset Value
0x0B8	QOSB_RDTOUT3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	rd_tout15	rd_tout14	rd_tout13	rd_tout12
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout15	Read command timeout configuration (gear 15). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Notice: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[23:16]	RW	rd_tout14	Read command timeout configuration (gear 14). 0x0: Disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[15:8]	RW	rd_tout13	Read command timeout configuration (gear 13). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: The timeout configuration is 8bits, but the actual count is 10bits, that is, the lower two bits are fixed to zero.
[7:0]	RW	rd_tout12	Read command timeout configuration (gear 12). 0x0: disable timeout function; 0x1ÿ0xFF: n*4 clock cycles; Note: timeout is configured as 8bits, but the actual count is 10bits, that is, the lower two bits are fixed as zero.

QOSB_WRTOUT_MAP

QOSB_WRTOUT_MAP is the write command timeout mapping control register for QosBuf.

Offset Address	Register Name	Total Reset Value
0x0BC	QOSB_WRTOUT_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	----					wrtout_map3			----					wrtout_map2			----					wrtout_map1			----					wrtout_map0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	wrtout_map3	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. wrtout_map3 indicates the position of bit3 to be selected in the entire ID.
[23:21]	RO	reserved	reserve.
[20:16]	RW	wrtout_map2	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. wrtout_map2 indicates the position of bit2 to be selected in the entire ID.
[15:13]	RO	reserved	reserve.
[12:8]	RW	wrtout_map1	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. wrtout_map1 indicates the position of bit1 to be selected in the entire ID.
[7:5]	RO	reserved	reserve.
[4:0]	RW	wrtout_map0	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. wrtout_map0 indicates the position of bit0 to be selected in the entire ID.

QOSB_RDTOUT_MAP

QOSB_RDTOUT_MAP is the QosBuf read command timeout mapping control register.

Offset Address	Register Name	Total Reset Value
0x0D0	QOSB_RDTOUT_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	----			rdtout_map3					----			rdtout_map2					----			rdtout_map1					----			rdtout_map0				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	rdtout_map3	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdtout_map3 indicates the position of bit3 to be selected in the entire ID.
[23:21]	RO	reserved	reserve.
[20:16]	RW	rdtout_map2	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdtout_map2 indicates the position of bit2 to be selected in the entire ID.
[15:13]	RO	reserved	reserve.
[12:8]	RW	rdtout_map1	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdtout_map1 indicates the position of bit1 to be selected in the entire ID.
[7:5]	RO	reserved	reserve.
[4:0]	RW	rdtout_map0	The timeout is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdtout_map0 indicates the position of bit0 to be selected in the entire ID.

QOSB_WRAGE0

QOSB_WRAGE0 configures register 0 for writing command aging of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0D4	QOSB_WRAGE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_age_prd7				wr_age_prd6				wr_age_prd5				wr_age_prd4				wr_age_prd3				wr_age_prd2				wr_age_prd1				wr_age_prd0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd7	Write command aging time configuration (level 7). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[27:24]	RW	wr_age_prd6	Write command aging time configuration (level 6). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[23:20]	RW	wr_age_prd5	Write command aging time configuration (gear 5). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[19:16]	RW	wr_age_prd4	Write command aging time configuration (Gear 4). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[15:12]	RW	wr_age_prd3	Write command aging time configuration (Gear 3). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[11:8]	RW	wr_age_prd2	Write command aging time configuration (gear 2). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[7:4]	RW	wr_age_prd1	Write command aging time configuration (level 1). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[3:0]	RW	wr_age_prd0	Write command aging time configuration (gear 0). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.

QOSB_WRAGE1

QOSB_WRAGE1 is the aging configuration register 1 for the writing command of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0D8	QOSB_WRAGE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_age_prd15				wr_age_prd14				wr_age_prd13				wr_age_prd12				wr_age_prd11				wr_age_prd10				wr_age_prd9				wr_age_prd8			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd15	Write command aging time configuration (gear 15). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[27:24]	RW	wr_age_prd14	Write command aging time configuration (gear 14). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[23:20]	RW	wr_age_prd13	Write command aging time configuration (gear 13). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[19:16]	RW	wr_age_prd12	Write command aging time configuration (gear 12). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[15:12]	RW	wr_age_prd11	Write command aging time configuration (gear 11). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[11:8]	RW	wr_age_prd10	Write command aging time configuration (Gear 10). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[7:4]	RW	wr_age_prd9	Write command aging time configuration (gear 9). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[3:0]	RW	wr_age_prd8	Write command aging time configuration (gear 8). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.

QOSB_RDAGE0

QOSB_RDAGE0 is the aging configuration register 0 for the read command of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0DC	QOSB_RDAGE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_age_prd7				rd_age_prd6				rd_age_prd5				rd_age_prd4				rd_age_prd3				rd_age_prd2				rd_age_prd1				rd_age_prd0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd7	Read command aging time configuration (level 7). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[27:24]	RW	rd_age_prd6	Read command aging time configuration (level 6). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[23:20]	RW	rd_age_prd5	Read command aging time configuration (gear 5). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[19:16]	RW	rd_age_prd4	Read command aging time configuration (level 4). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[15:12]	RW	rd_age_prd3	Read command aging time configuration (level 3). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[11:8]	RW	rd_age_prd2	Read command aging time configuration (level 2). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[7:4]	RW	rd_age_prd1	Read command aging time configuration (level 1). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[3:0]	RW	rd_age_prd0	Read command aging time configuration (gear 0). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.

QOSB_RDAGE1

QOSB_RDAGE1 is the aging configuration register 1 for the read command of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0E0	QOSB_RDAGE1	0x0000_0000

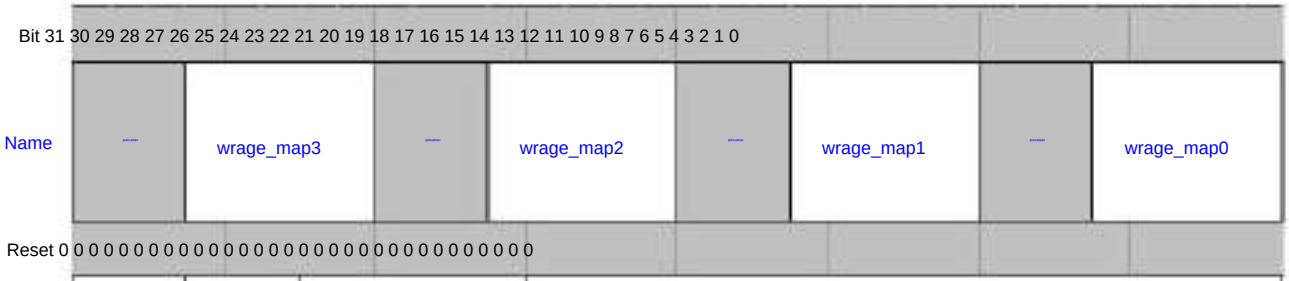
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_age_prd15				rd_age_prd14				rd_age_prd13				rd_age_prd12				rd_age_prd11				rd_age_prd10				rd_age_prd9				rd_age_prd8			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd15	Read command aging time configuration (gear 15). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[27:24]	RW	rd_age_prd14	Read command aging time configuration (position 14). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[23:20]	RW	rd_age_prd13	Read command aging time configuration (position 13). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[19:16]	RW	rd_age_prd12	Read command aging time configuration (level 12). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[15:12]	RW	rd_age_prd11	Read command aging time configuration (position 11). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[11:8]	RW	rd_age_prd10	Read command aging time configuration (level 10). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[7:4]	RW	rd_age_prd9	Read command aging time configuration (gear 9). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.
[3:0]	RW	rd_age_prd8	Read command aging time configuration (gear 8). 0x0: Aging function disabled; 0x1~0xF: N×16 clock cycles.

QOSB_WRAGE_MAP

QOSB_WRAGE_MAP is the write command aging mapping control register for QosBuf.

Offset Address	Register Name	Total Reset Value
0x0E4	QOSB_WRAGE_MAP	0x0000_0000



Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	wrage_map3	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. wrap_map3 indicates the position of bit3 to be selected in the entire ID.
[23:21]	RO	reserved	reserve.
[20:16]	RW	wrage_map2	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. Wrage_map2 indicates the position of bit2 to be selected in the entire ID.
[15:13]	RO	reserved	reserve.
[12:8]	RW	wrage_map1	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. Wrage_map1 indicates the position of bit1 to be selected in the entire ID.
[7:5]	RO	reserved	reserve.
[4:0]	RW	wrage_map0	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. Wrage_map0 indicates the position of bit0 to be selected in the entire ID.

QOSB_RDAGE_MAP

QOSB_RDAGE_MAP is the aging map control register for reading commands of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0E8	QOSB_RDAGE_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	----			rdage_map3				----			rdage_map2				----			rdage_map1				----			rdage_map0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	rdage_map3	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdage_map3 indicates the position of bit3 to be selected in the entire ID.
[23:21]	RO	reserved	reserve.
[20:16]	RW	rdage_map2	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdage_map2 indicates the position of bit2 to be selected in the entire ID.
[15:13]	RO	reserved	reserve.
[12:8]	RW	rdage_map1	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdage_map1 indicates the position of bit1 to be selected in the entire ID.
[7:5]	RO	reserved	reserve.
[4:0]	RW	rdage_map0	Aging is divided into 16 gears. The mapping method is to select 4 bits from the ID, and select the corresponding gear according to the value of the 4 bits. rdage_map0 indicates the position of bit0 to be selected in the entire ID.

QOSB_ROWHIT_PRILVL

QOSB_ROWHIT_PRILVL is the row hit priority watermark register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0EC	QOSB_ROWHIT_PRILVL	0x0000_0000

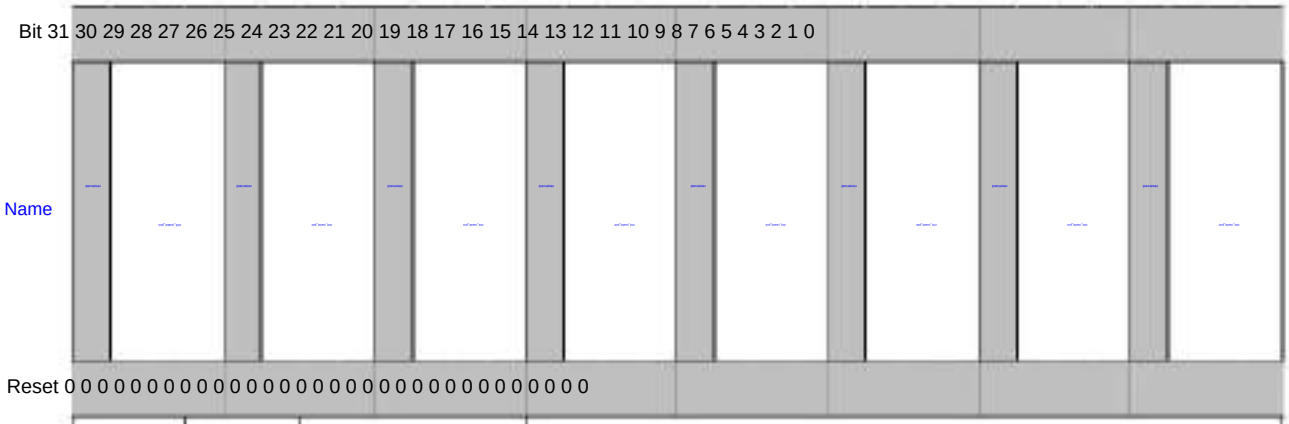
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	ch3_rowhit_pri_lvl	Channel 3 priority watermark. When the current priority is lower than ch3_rohit_pri_lvl, raise the priority to ch3_rowhit_pri1; When the current priority is higher than ch3_rohit_pri_lvl, raise the priority to ch3_rowhit_pri0;
[11]	RO	reserved	reserve.
[10:8]	RW	ch2_rowhit_pri_lvl	Channel 2 priority watermark. When the current priority is lower than ch2_rohit_pri_lvl, raise the priority to ch2_rowhit_pri1; When the current priority is higher than ch2_rohit_pri_lvl, raise the priority to ch2_rowhit_pri0;
[7]	RO	reserved	reserve.
[6:4]	RW	ch1_rowhit_pri_lvl	Channel 1 priority watermark. When the current priority is lower than ch1_rohit_pri_lvl, raise the priority to ch1_rowhit_pri1; When the current priority is higher than ch1_rohit_pri_lvl, raise the priority to ch1_rowhit_pri0;
[3]	RO	reserved	reserve.
[2:0]	RW	ch0_rowhit_pri_lvl	Channel 0 priority watermark. When the current priority is lower than ch0_rohit_pri_lvl, raise the priority to [2:0] ch0_rowhit_pri1; when the current priority is higher than ch0_rohit_pri_lvl, raise the priority to ch0_rowhit_pri0;

QOSB_ROWHIT_PRI

QOSB_ROWHIT_PRI is the row hit priority control register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0F0	QOSB_ROWHIT_PRI	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	ch3_rowhit_pri1	See description of ch3_rowhit_pri_lvl.
[27]	RO	reserved	reserve.
[26:24]	RW	ch3_rowhit_pri0	See description of ch3_rowhit_pri_lvl.
[23]	RO	reserved	reserve.
[22:20]	RW	ch2_rowhit_pri1	See description of ch2_rowhit_pri_lvl.
[19]	RO	reserved	reserve.
[18:16]	RW	ch2_rowhit_pri0	See description of ch2_rowhit_pri_lvl.
[15]	RO	reserved	reserve.
[14:12]	RW	ch1_rowhit_pri1	See description of ch1_rowhit_pri_lvl.
[11]	RO	reserved	reserve.
[10:8]	RW	ch1_rowhit_pri0	See description of ch1_rowhit_pri_lvl.
[7]	RO	reserved	reserve.
[6:4]	RW	ch0_rowhit_pri1	See description of ch0_rowhit_pri_lvl.
[3]	RO	reserved	reserve.
[2:0]	RW	ch0_rowhit_pri0	See description of ch0_rowhit_pri_lvl.

QOSB_ROWHIT_CTRL

QOSB_ROWHIT_CTRL is the enable control of row hit of QosBuf.

Offset Address	Register Name	Total Reset Value
0x0F4	QOSB_ROWHIT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	ch3_dual_flow_en	Dual stream enable control of row hit of channel3: 0: Dual stream function off; 1: The dual-stream function is enabled.
[6]	RW	ch2_dual_flow_en	Dual stream enable control of row hit of channel2: 0: Dual stream function off; 1: The dual-stream function is enabled.
[5]	RW	ch1_dual_flow_en	Dual stream enable control of row hit of channel1: 0: Dual stream function off; 1: The dual-stream function is enabled.
[4]	RW	ch0_dual_flow_en	Dual-stream enable control of row hit of channel0: 0: dual-stream function disabled; 1: The dual-stream function is enabled.
[3]	RW	ch3_row_hit_en	channel3 row hit enable control: 0: rowhit function off; 1: rowhit function on;
[2]	RW	ch2_row_hit_en	channel2 row hit enable control: 0: rowhit function is off; 1: The rowhit function is enabled;

[1] RW	ch1_row_hit_en		channel1 row hit enable control. 0: rowhit function is off; 1: The rowhit function is enabled;
[0] RW	ch0_row_hit_en		channel0 row hit enable control. 0: rowhit function is off; 1: The rowhit function is enabled;

QOSB_CKG_CFG

QOSB_CKG_CFG is the clock control register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x108	QOSB_CKG_CFG	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	dyn_ck_gate	Dynamic clock gating for the Qosbuf module. 0: The clock is always on; 1: When the module is idle, the clock is automatically gated.

QOSB_DMC_LVL

QOSB_DMC_LVL is the line control register for the command of QosBuf entering DMC.

Offset Address	Register Name	Total Reset Value
0x10Cÿ0x4×chans (chance = 0ÿ1)	QOSB_DMC_LVL	0x0000_000F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dmc_cmd_full_lvl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:0]	RW	dmc_cmd_full_lvl	QOS BUF is the number of commands entering dmc. When this watermark is reached, it means that the queue of dmc is full. Note: Due to the pipeline problem, when the configuration is N, the number of actually passed commands is N+1. In addition, this register cannot be dynamically configured during access.

QOSB_CFG_PERF

QOSB_CFG_PERF is the mode configuration register for QosBuf performance statistics.

Offset Address	Register Name	Total Reset Value
0x120	QOSB_CFG_PERF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	— perf_prd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RW	perf_en	Performance statistics enable register. 1: Enable; 0: Disable. Note: When perf_mode=0, enabling this bit means that the performance statistics register will start counting in circles. When perf_mode=1, this bit is automatically cleared after a statistics is completed.

[28] RW perf_mode			performance statistics mode. 0: Continuous trigger mode. Counters related to performance statistics count continuously. It can guarantee that in the continuous statistics mode, the statistics will not overflow within 1s. 1: Single trigger mode. After the performance statistics time expires perf_prd, the statistics results will be kept and the statistics will stop. Note: The maximum stat value is maintained when overflow occurs.
[27:0] RW perf_prd			Performance statistics cycle. 0x0: invalid configuration. 0x1~0xFFFFFFF: statistics period. The actual statistical period is perf_prd*16*tclk (Tclk is the DDRC bus clock period). Note: This configuration is only valid when perf_mode=1. When the continuous statistics mode of perf_mode=0, the counters related to performance statistics will keep counting.

QOSB_CMD_SUM

QOSB_CMD_SUM is the accumulative register of QosBuf command count.

Offset Address	Register Name	Total Reset Value
0x124	QOSB_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_cmd_sum	The value of the current QosBuf buffer command is accumulated periodically, overflowed and wound.

QOSB_SLOT_STAT0

QOSB_SLOT_STAT0 is the status register 0 of the queue of QosBuf.

Offset Address	Register Name	Total Reset Value
0x128	QOSB_SLOT_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_l	The state of the cmd queue in QosBuf is from 0 to 31, and the corresponding bit is 1, indicating that there is a command in the slot, otherwise it is empty.

QOSB_SLOT_STAT1

QOSB_SLOT_STAT1 is the status register 1 of the queue of QosBuf.

Offset Address	Register Name	Total Reset Value
0x12C	QOSB_SLOT_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	that there is a command in the	The state of the cmd queue in QosBuf is from 32 to 63, and the corresponding bit is 1, indicating grp_cmd_valid_m0 slot, otherwise it is empty.

QOSB_SLOT_STAT2

QOSB_SLOT_STAT2 is the status register 2 of the queue of QosBuf.

Offset Address	Register Name	Total Reset Value
0x130	QOSB_SLOT_STAT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	that there is a command in the	The state of the cmd queue in QosBuf is from 64 to 95, and the corresponding bit is 1, indicating grp_cmd_valid_m1 slot, otherwise it is empty.

QOSB_SLOT_STAT3

QOSB_SLOT_STAT3 is the status register 3 of the queue of QosBuf.

Offset Address	Register Name	Total Reset Value
0x134	QOSB_SLOT_STAT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	grp_cmd_valid_h	The state of the cmd queue in QosBuf is from 96 to 127, and the corresponding bit is 1, indicating that there is a command in the slot, otherwise it is empty.

QOSB_WBUF_STAT0

QOSB_WBUF_STAT0 is the write buf status register 0 of QosBuf.

Offset Address	Register Name	Total Reset Value
0x140ÿ0x4×chans (chance = 0ÿ1)	QOSB_WBUF_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	buf_ldata_valid_l	Write the state of buf from 0 to 31 in QosBuf, and the corresponding bit is 1, which means there is a burst of data stored in this buf, otherwise the data is less than a burst or empty.

QOSB_WBUF_STAT1

QOSB_WBUF_STAT1 is the write buf status register 1 of QosBuf.

Offset Address	Register Name	Total Reset Value
0x150ÿ0x4×chans (chance = 0ÿ1)	QOSB_WBUF_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	buf_ldata_valid_h	Write the state of buf from 32 to 63 in QosBuf, the corresponding bit is 1, which means there is a burst of data stored in this buf, otherwise the data is less than a burst or empty.

QOSB_RDRBUF_STAT

QOSB_RDRBUF_STAT is the buf status register of the Reorder module.

Offset Address	Register Name	Total Reset Value
0x160ÿ0x4×chans (chance = 0ÿ1)	QOSB_RDRBUF_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	e_vld																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	e_vld	The state of reorder buf in Reorder is from 0 to 31, and the corresponding bit is 1, indicating that there is a burst of data stored in the buf, otherwise the data is less than a burst or empty.

QOSB_INTMSK

QOSB_INTMSK is the QosBuf interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x170	QOSB_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	qos_stat_int_mask	QOS Buf command statistics interrupt mask enable. 1: mask interrupt; 0: enable interrupt.

QOSB_RINT

QOSB_RINT is the original interrupt register of QosBuf.

Offset Address	Register Name	Total Reset Value
0x174	QOSB_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	INT_WC	qos_stat_rint	QOS Buf command statistics interrupt. Write 1 to clear the interrupt.

QOSB_INTSTS

QOSB_INTSTS is the QOSBUF interrupt status register.

Offset Address	Register Name	Total Reset Value
0x178	QOSB_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	INT	qos_stat_intsts	QOS Buf command statistics interrupt.

QOSB_CMD_CNT

QOSB_CMD_CNT is the statistics register of how many commands are currently in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x180	QOSB_CMD_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														qos_cmd_cnt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:8]	RO	reserved	reserve.
[7:0]	INT	qos_cmd_cnt	QosBuf The number of current commands, including commands on the pipeline.

QOSB_RNK_CNT

QOSB_RNK_CNT is the statistics register of how many commands are currently in each rank in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x190ÿ0x4×chans (chance = 0ÿ1)	QOSB_RNK_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	rnk3_cmd_cnt		rnk0_cmd_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7:0] RO		rnk0_cmd_cnt	The number of commands in the current channel belonging to rank0 in QosBuf.

QOSB_BNK_CNT0

QOSB_BNK_CNT0 is the statistics register 0 of how many commands each Bank currently has in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1A0ÿ0x4×chance (chance = 0ÿ1)	QOSB_BNK_CNT0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	bnk3_cmd_cnt	bnk2_cmd_cnt	bnk1_cmd_cnt	bnk0_cmd_cnt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24] RO		bnk3_cmd_cnt	counts the number of commands belonging to bank3 in the current channel in DMC.
[23:16] RO		bnk2_cmd_cnt	counts the number of commands belonging to bank2 in the current channel in DMC.
[15:8] RO		bnk1_cmd_cnt	counts the number of commands belonging to bank1 in the current channel in DMC.
[7:0] RO		bnk0_cmd_cnt	counts the number of commands belonging to bank0 in the current channel in DMC.

QOSB_BNK_CNT1

QOSB_BNK_CNT1 is the statistics register 1 of how many commands each Bank currently has in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1B0ÿ0x4×chans (chance = 0ÿ1)	QOSB_BNK_CNT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	bnk7_cmd_cnt	bnk6_cmd_cnt	bnk5_cmd_cnt	bnk4_cmd_cnt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO	bnk7_cmd_cnt counts the number of commands belonging to bank7 in the current channel in DMC.
[23:16]	RO	bnk6_cmd_cnt counts the number of commands belonging to bank6 in the current channel in DMC.
[15:8]	RO	bnk5_cmd_cnt counts the number of commands belonging to bank5 in the current channel in DMC.
[7:0]	RO	bnk4_cmd_cnt counts the number of commands belonging to bank4 in the current channel in DMC.

QOSB_BNK_CNT2

QOSB_BNK_CNT2 is the statistics register 2 of how many commands each Bank currently has in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1C0ÿ0x4×chans (chance = 0ÿ1)	QOSB_BNK_CNT2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	bnk11_cmd_cnt	bnk10_cmd_cnt	bnk9_cmd_cnt	bnk8_cmd_cnt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO	bnk11_cmd_cnt counts the number of commands belonging to bank11 in the current channel in DMC.
[23:16]	RO	bnk10_cmd_cnt counts the number of commands belonging to bank10 in the current channel in DMC.
[15:8]	RO	bnk9_cmd_cnt counts the number of commands belonging to bank9 in the current channel in DMC.
[7:0]	RO	bnk8_cmd_cnt counts the number of commands belonging to bank8 in the current channel in DMC.

QOSB_BNK_CNT3

QOSB_BNK_CNT3 is the statistics register 3 of how many commands each Bank currently has in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1D0ÿ0x4×chance (chance = 0ÿ1)	QOSB_BNK_CNT3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	bnk15_cmd_cnt	bnk14_cmd_cnt	bnk13_cmd_cnt	bnk12_cmd_cnt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO		bnk15_cmd_cnt counts the number of commands belonging to bank15 in the current channel in DMC.
[23:16]	RO		bnk14_cmd_cnt counts the number of commands belonging to bank14 in the current channel in DMC.
[15:8]	RO		bnk13_cmd_cnt counts the number of commands belonging to bank13 in the current channel in DMC.
[7:0]	RO		bnk12_cmd_cnt counts the number of commands belonging to bank12 in the current channel in DMC.

QOSB_OSTD_CNT

QOSB_OSTD_CNT is the statistical register of how many Oustanding commands each channel currently has in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1E0	QOSB_OSTD_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		ch1_cmd_ostd	ch0_cmd_ostd
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RO	ch1_cmd_ostd	The number of Outanding commands that the current channel belongs to channel1 in QosBuf.
[7:0]	RO	ch0_cmd_ostd	The number of outanding commands that the current channel belongs to channel0 in QosBuf.

QOSB_WR_CMD_SUM

QOSB_WR_CMD_SUM is the accumulation register of QosBuf write command count.

Offset Address	Register Name	Total Reset Value
0x1E4	QOSB_WR_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_wr_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	qos_wr_cmd_sum	The value of the current QosBuf temporary storage write command is accumulated by cycle, overflowed and wound.

QOSB_RD_CMD_SUM

QOSB_RD_CMD_SUM is the accumulative register of QosBuf read command count.

Offset Address	Register Name	Total Reset Value
0x1E8	QOSB_RD_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_rd_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	qos_rd_cmd_sum	The value of the current QosBuf temporary storage read command is accumulated by cycle, overflowed and wound.

QOSB_TIMEOUT_MODE

QOSB_TIMEOUT_MODE is the timeout mode selection register in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1F0	QOSB_TIMEOUT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.

[0]	RW	timeout_mode	Timeout Mapping Mode Selection Register for Read and Write Commands. 0: Mapping by ID, 16 levels in total (each level is defined in QOSB_WRTOUT0~ QOSB_WRTOUT3 or QOSB_RDTOUT0~ QOSB_RDTOUT3); 1: Mapping by priority, 8 levels in total. The mapping table is the same as the lower 8 levels of the ID mapping table.

QOSB_WBUF_PRI_CTRL

QOSB_WBUF_PRI_CTRL is the write wbuf priority adjustment control register in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1F4	QOSB_WBUF_PRI_CTRL	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbuf_hcnt																wbuf_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wbuf_hcnt	When the number of write commands to write wbuf reaches the QOSB_WBUF_CTRL[wbuf_lvl2] watermark, the internal counter will use this value. Indicates that once the number of write commands of wbuf reaches wbuf_lvl2, the internal counting starts, and in the time zone before the count value reaches wbuf_hcnt, the priority of write commands for writing buf is adjusted to pri2. Note: pri2 here refers to the corresponding priority of wbuf above wbuf_lvl2, see QOSB_WBUF_CTRL[wbuf_pri2].
[15:0]	RW	wbuf_lcnt	When the number of write commands to write wbuf reaches the QOSB_WBUF_CTRL[wbuf_lvl2] watermark, and the internal counter has reached wbuf_hcnt, this value will be used. Indicates that after the internal counter reaches wbuf_hcnt, it restarts counting internally. In the time zone before the count value reaches wbuf_lcnt, writing buf will adjust the priority of the write command to pri1. If the counter is 0, it means that the priority of pri2 will always be used class. Note: pri1 here refers to the corresponding priority of wbuf above wbug_lvl1, see QOSB_WBUF_CTRL[wbuf_pri1].

QOSB_RHIT_CTRL

QOSB_RHIT_CTRL is the rowhit priority adjustment control register in QOSBUF.

Offset Address	Register Name	Total Reset Value
0x1F8	QOSB_RHIT_CTRL	0x00FF_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	virtual_hcnt																rhit_lcnt															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:16]	RW	rhit_hcnt	The time allowed for the rowhit command stream to persist. Note: When the rowhit command flow maintenance time reaches the rhit_hcnt value configured by this register, it will be forcibly disconnected. Then the internal counter counts again, and the rowhit command stream is allowed to initiate an arbitration request after the calculated value reaches rhit_lcnt.
[15:0]	RW	rhit_lcnt	The time at which the rowhit command flow was disconnected. Note: When the rowhit command flow maintenance time reaches the rhit_hcnt value configured by this register, it will be forcibly disconnected. Then the internal counter counts again, and the rowhit command stream is allowed to initiate an arbitration request after the calculated value reaches rhit_lcnt.

4.1.7 DMC module registers in DDRC

4.1.7.1 DMC register overview

An overview of the DMC registers is shown in Table 4-8 .

Table 4-8 Overview of DMC registers (base address: 0x1206_8000)

offset address	name	describe	page number
0x000	DDRC_CTRL_SREF	DDRC self-refresh control register	4-77
0x00C	DDRC_CTRL_SFC	DDRC Software Configuration DDR Command Start Register 4-77	
0x010	DDRC_CTRL_PERF	DDRC performance statistics enable register	4-78
0x020	DDRC_CRG_SREF	DDR self-refresh configuration register	4-79
0x024	DDRC_CFG_INIT	DDR initialization configuration register	4-80
0x028	DDRC_CFG_PD	DDR Low Power PowerDown Status Configuration Register	4-80
0x02C	DDRC_CFG_AREF	DDRC auto refresh mode configuration register	4-82
0x040	DDRC_CFG_WORK MODE	DDRC Operating Mode Configuration Register	4-83

offset address	name	describe	page number
0x044	DDRC_CFG_WORK FASHION2	DDRC Operating Mode Configuration Register	4-85
0x050	DDRC_DDRMODE	DDR operating mode configuration register	4-85
0x058	DDRC_CFG_SCRA MB	DDR Data Scrambling Configuration Register	4-89
0x060	DDRC_CFG_RNKV OL	DDR capacity configuration register for each RANK controlled by DDRC	4-90
0x0A0	DDRC_CFG_ODT	ODT feature configuration register	4-91
0x0F0	DDRC_CFG_EMRS0 1	DDR mode register 0 and mode register 1 configuration register	4-92
0x0F4	DDRC_CFG_EMRS2 3	Configuration registers of mode register 2 and mode register 3 of DDR	4-93
0x100	DDRC_CFG_TIMIN G0	Timing parameter register 0 of DDRC	4-93
0x104	DDRC_CFG_TIMIN G1	Timing parameter register 1 of DDRC	4-94
0x108	DDRC_CFG_TIMIN G2	Timing parameter register 2 of DDRC	4-95
0x10C	DDRC_CFG_TIMIN G3	Timing parameter register 3 of DDRC	4-96
0x110	DDRC_CFG_TIMIN G4	Timing parameter register 4 of DDRC	4-97
0x114	DDRC_CFG_TIMIN G5	Timing parameter register 5 of DDRC	4-98
0x118	DDRC_CFG_TIMIN G6	DDRC Timing Parameter Register 6	4-99
0x11C	DDRC_CFG_TIMIN G7	Timing parameter register 7 of DDRC	4-100
0x140	DDRC_CFG_BLDA FACING	DDRC write data pre-receive write data configuration register	4-100
0x144	DDRC_CFG_DMCL VL	DDR Controller Command Queue Depth Watermark Configuration Register	4-101
0x200	DDRC_CFG_DDRP HE	DDR IO configuration register	4-101
0x20C	DDRC_CFG_SFC_TI M	DDRC software configures the timing register of the DDR command	4-102
0x210	DDRC_CFG_SFC	DDRC software configuration DDR command property command	4-103

offset address name		describe	page number
0x214	DDRC_CFG_SFC_ADDR0	SFC read and write memory address configuration register 0	4-104
0x218	DDRC_CFG_SFC_ADDR1	SFC read and write memory address configuration register 1	4-105
0x21C	DDRC_CFG_SFC_WDATE0	SFC write data configuration register 0	4-105
0x220	DDRC_CFG_SFC_WDATA1	SFC write data configuration register 1	4-105
0x224	DDRC_CFG_SFC_WDATA2	SFC write data configuration register 2	4-106
0x228	DDRC_CFG_SFC_WDATA3	SFC write data configuration register 3	4-106
0x254	DDRC_CFG_STADAT	DDRC data statistics enable register	4-106
0x258	DDRC_CFG_DATMIN	Minimum Threshold Register for DMC Data Count	4-108
0x25C	DDRC_CFG_DATMAX	DMC Data Count Maximum Threshold Register	4-108
0x260	DDRC_CFG_STACMD	Mode configuration register for DDR performance statistics	4-108
0x264	DDRC_CFG_CMDMIN	Minimum Threshold Register for DMC Command Count	4-109
0x268	DDRC_CFG_CMDMAX	DMC Command Count Maximum Threshold Register	4-110
0x270	DDRC_CFG_PERF	DDR performance statistics mode configuration register	4-110
0x274	DDRC_CFG_STAID	Command ID for DDR Performance Statistics Configuration Register 4-111	
0x278	DDRC_CFG_STAIDCEC	Command ID MASK configuration register for DDR performance statistics	4-112
0x280	DDRC_INTMSK	DDRC Interrupt Mask Register	4-112
0x284	DDRC_RINT	DDRC Raw Interrupt Register	4-114
0x288	DDRC_INTSTS	DDRC Interrupt Status Register	4-115
0x290	DDRC_CURR_STAYOU	DDRC Status Register	4-116
0x294	DDRC_CURR_FUNC	DDRC FUNC module status register	4-117
0x298	DDRC_CURR_FUNC2	DDRC FUNC2 module status register	4-118

offset address	name	describe	page number
0x2A0	DDRC_CURR_EXECST	DDRC command state machine state	4-118
0x2A4	DDRC_CURR_WGFIFOST	DDRC write FIFO empty full status register	4-119
0x380	DDRC_HIS_FLUX_WR	DDRC All Write Command Traffic Statistics Register 4-119	
0x384	DDRC_HIS_FLUX_RD	DDRC All read command traffic statistics register 4-120	
0x0388	DDRC_HIS_FLUX_WCMD	DDRC The number of all write commands	4-120
0x038C	DDRC_HIS_FLUX_RCMD	DDRC The number of all read commands	4-121
0x390	DDRC_HIS_FLOWSD_WR	DDRC specified ID write traffic statistics register	4-121
0x394	DDRC_HIS_FLOWSD_RD	DDRC specified ID read traffic statistics register 4-122	
0x0398	DDRC_HIS_FLOWSD_WCMD	DDRC The number of all write commands	4-122
0x039C	DDRC_HIS_FLOWSD_RCMD	DDRC The number of all read commands	4-123
0x3A0	DDRC_HIS_WLATCNT0	DDRC Write Command Latency Statistical Register 0 Specified by ID	4-123
0x3A4	DDRC_HIS_WLATCNT1	DDRC Specifies the write command ID Latency statistics register 1	4-124
0x3A8	DDRC_HIS_RLATCNT0	DDRC Specified ID read command Latency statistics register 0	4-124
0x3AC	DDRC_HIS_RLATCNT1	DDRC Specified ID read command Latency statistics register 1	4-125
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	Read Channel Intrinsic Delay Register	4-125
0x3B4	DDRC_STAT_RPT	DMC Command Counter Accumulation Register Read Pointer Needle	4-126
0x3B8	DDRC_HIS_CMD_SONE	Cumulative Register for DMC Command Count	4-126
0x3BC	DDRC_HIS_DAT_SONE	Accumulation register for DMC data count	4-127
0x4A8	DDRC_HIS_SFC_RDATE0	SFC read data register 0	4-127

offset address name		describe	page number
0x4AC	DDRC_HIS_SFC_R DATA1	SFC read data register 1	4-127
0x4B0	DDRC_HIS_SFC_R DATA2	SFC read data register 2	4-128
0x4B4	DDRC_HIS_SFC_R DATA3	SFC read data register 3	4-128

4.1.7.2 DMC Register Description

DDRC_CTRL_SREF

DDRC_CTRL_SREF is the DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_CTRL_SREF	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	sref_done	The DDRPHY self-refresh operation is complete. 0: normal working state; 1: The transition from 0 to 1 indicates that DDRPHY completes all necessary operations after exiting from self-refresh, and DMC can accept new requests.
[0]	RW	sref_req	SDRAM self-refresh request. 0: Exit the self-refresh state; 1: Enter self-refresh state.

DDRC_CTRL_SFC

DDRC_CTRL_SFC configures the DDR command enable register for DDRC software.

Offset Address	Register Name	Total Reset Value
0x00C	DDRC_CTRL_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	cmd_req	The controller configuration command executes the request. 1: Request to execute the command; 0: Do not execute the command or automatically clear the parameter to zero after the command is executed. At this time, after writing again, the operation will take effect

DDRC_CTRL_PERF

DDRC_CTRL_PERF is the DDRC performance statistics enable register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL_PERF	0x0000_0000

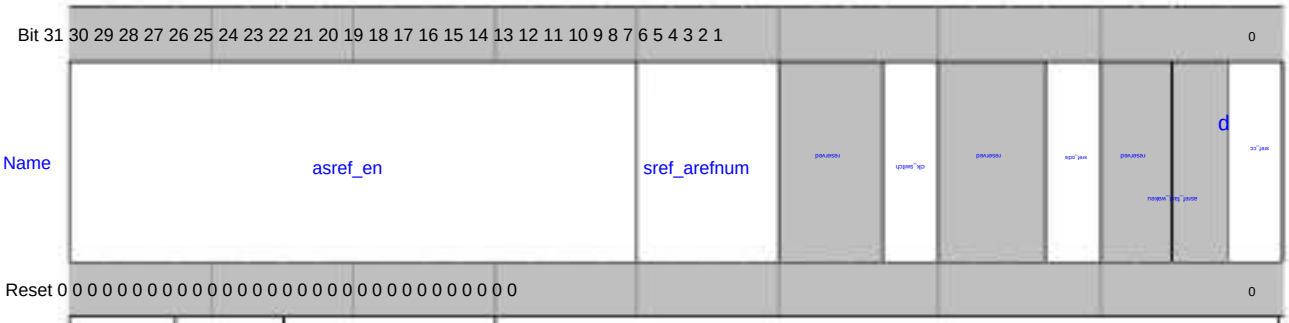
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	perf_en	Enable performance statistics. 0: forbidden; 1: enable. Note: When perf_mode=0, enabling this bit means that the performance statistics register will start counting in circles. When perf_mode=1, after completing a statistics, this bit is automatically cleared

DDRC_CFG_SREF

DDRC_CFG_SREF is the DDR self-refresh configuration register.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CFG_SREF	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	asref_en	SDRAM automatically enters SELF REFRESH enable. 1: enable; 0: Disabled. Note that each RANK corresponds to a control bit. When DDRC_CFG_PD[PD_EN] is valid and the corresponding asref_en of RANK is valid, this RANK can automatically enter SELF REFRESH. The current version does not support this feature.
[15:12]	RW	sref_arefnum	DDR3 SDRAM The number of auto-refresh operations issued after exiting self-refresh during the DFS process. 0x0: Do not send auto refresh operation. 0x1~0xF: n times.
[11:9]	RO	reserved	reserve.
[8]	RW	clk_switch	DDRC Low Power Clock Switching Control. Whether DDRC enters the low power consumption state (DDR Self Refresh) state and backpressures the AXI interface command. 0: back pressure interface command, and execute the original command at the same time; 1: Back pressure interface command, after the clock switching is completed, continue to execute the original command.
[7:5]	RO	reserved	reserve.
[4]	RW	sref_odis	Self-refresh mode, output shutdown configuration for DDR command and data IO. 0: Do not turn off the pin output; 1: Turn off the pin output. Note: This configuration is a static configuration. It is suggested that after configuring DDR to enter self_refresh, it can be configured as 1 to turn off the output of DDR command and data IO. in configuration Before DDR exits self_refresh, configure it as 0 to enable the output of DDR command and data IO.
[3:2]	RO	reserved	reserve.

[1] RW	asref_fast_wakeup		AUTO SELFREFRESH Fast wakeup enable. 0: forbidden; 1: enable.
[0] RW	sref_cc		Self-refresh mode, SDRAM clock control. 0: Do not turn off the SDRAM clock; 1: Disable SDRAM clock.

DDRC_CFG_INIT

DDRC_CFG_INIT initializes configuration registers for DDR.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CFG_INIT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / init_arefnum
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	init_arefnum	The number of auto-refresh operations issued during DDR3 SDRAM initialization. 0x0~0x2: 2 times; 0x3~0xF: n times.

DDRC_CFG_PD

DDRC_CFG_PD is the DDR low-power PowerDown state configuration register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CFG_PD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	asref_prd / t_clk_cke / pd_prd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

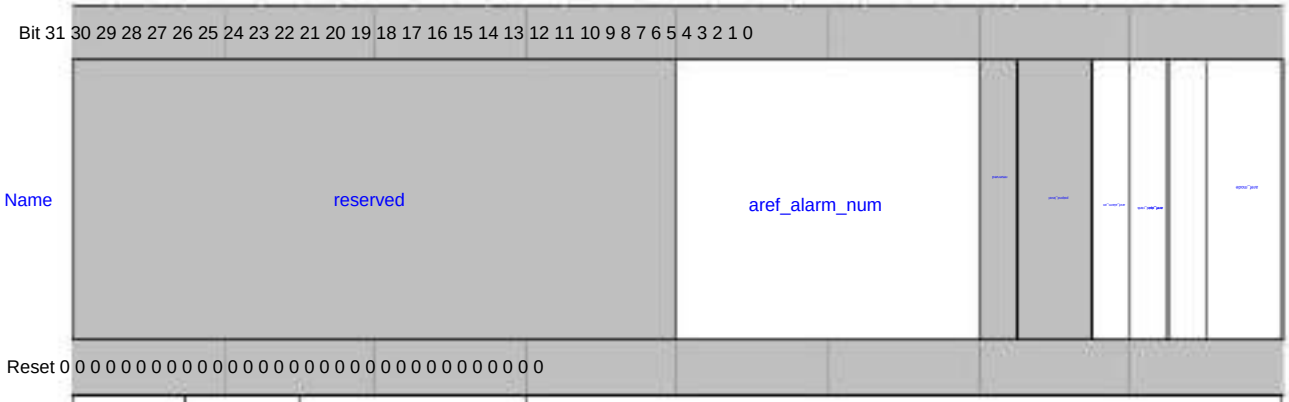
Bits	Access	Name	Description
[31:20]	RO	asref_prd	SDRAM low power consumption (Self-refresh) cycle configuration. When DDRC does not receive a command in consecutive asref_prd cycles, it controls SDRAM to enter the self-refresh state, and when a new command arrives, it controls SDRAM to exit the self-refresh state. 0x0~0xFFF: n*16 clock cycles. Note: This parameter is only valid when asref_en is 1.
[19:16]	RW	t_clk_cke	CLK and CKE relationship settings. 0x0~0x7: DDRPHY closes the delay of DDR3 granular clock relative to CKE, which is related to the specific DDRPHY. In the current version, when the clock is turned off, it can be configured as 0.
[15:4]	RW	pd_prd	SDRAM low power consumption (Power Down) cycle configuration. When DDRC does not receive a command in consecutive pd_prd cycles, it controls SDRAM to enter a low power consumption state, and when a new command arrives, it controls SDRAM to exit a low power consumption state. 0x00: Do not enter the power down state; 0x01~0xFFF: n clock cycles. Note: This parameter is only valid when pd_en is 1.
[3]	RO	reserved	reserve
[2]	RW	pd_cc	Low power mode (powerdown), SDRAM clock control. 1: Turn off the SDRAM clock; 0: Do not turn off SDRAM clock. Note: This function cannot be used in DDR3 mode.
[1]	RW	pd_ac	Low power mode (PowerDown), SDRAM address command dynamic shutdown control. 1: Turn off the pin output; 0: Do not turn off the pin output. Note: It is valid when pd_en is enabled, and the control pins do not include CKE, ODT, CSN and RESET_N.

[0] RW pd_en			SDRAM automatic low power enable. 1: enable; 0: Disabled.

DDRC_CFG_AREF

DDRC_CFG_AREF is the DDRC auto refresh mode configuration register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_CFG_AREF	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15 : 8]	RW	aref_alarm_num	Configure to issue the self refresh command forcibly after several auto refresh commands cannot be issued. 0x0~0xFF: lack of n+1 auto refresh. (Note, but when n=255, since the counter is 8 bits, the high bit will be lost after the carry, which is equivalent to 1) When it is optimized mode, set aref_opt=1, and when the number of posted commands is greater than or equal to 15, it will alarm.
[7]	RO	reserved	reserve.
[6:5]	RW	pstpnd_level	Optimize the waterline configuration of the automatic refresh mode. 11: Postponed command waterline is 8; 10: Postponed command waterline is 4; 01: Postponed command waterline is 2; 00: Postponed command waterline is 1;
[4]	RW	aref_alarm_en	Enable the alarm enable of auto refresh in AREF function: 1: Enable; 0: Disable.

[3] RW aref_dual_rank			AREF Module sends REF command mode selection. 0: Only send REF command to one rank at a time 1: Send REF command to two ranks each time.
[2] RW aref_opt			auto refresh optimization enabled. 1: Enable automatic refresh optimization; 0: Disable automatic refresh optimization. When this function is enabled, it is recommended to configure aref_mode as 00. DMC will dynamically detect whether the DDR is idle every time it is auto refresh, and if it is idle, it will send AREF command, otherwise it will wait until the AREF cycle accumulates to 9 AREF cycles, forcefully terminate the DDR access, and insert the AREF command.
[1:0] RW aref_mode			Non-optimized auto-refresh mode selection. 11: Perform 8 automatic refresh operations every 9 tREFI cycles; 10: 4 auto-refresh operations every 5 tREFI cycles 01: Perform 3 auto-refresh operations every 4 tREFI cycles 00: Execute an automatic refresh operation every tREFI period. Optimize the automatic refresh mode. 11: Postponed command waterline is 8; 10: Postponed command waterline is 4; 01: Postponed command waterline is 2; 00: Postponed command waterline is 1;

DDRC_CFG_WORKMODE

DDRC_CFG_WORKMODE is the DDRC working mode configuration register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_CFG_WORKMODE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:14] RO		reserved	reserve

[13] RW hdr_mode			DFI interface mode selection. 0: SDR mode; 1: HDR mode. The current version only supports HDR mode.
[12] RW read_mode			Controller read mode selection. 0: read along with the road mode; 1: Delayed read mode. The read-associated mode means that the controller completes data sampling according to the data valid signal sent by the PHY. Delayed read mode refers to the internal delay of the controller to wait for the completion of sampling the data sent by the PHY.
[11:10] RW addr_mode			DDR address line toggle mode selection. 00: In IDLE, all command addresses are set to 1; 01: In IDLE, keep the state of the previous command; 10: Reverse the previous state during IDLE; 11: Reserved.
[9] RW intlv_en			DMC BURST burst enable. 0: forbidden; 1: enable. It is recommended to set it to 0.
[8] RW wrap_en			WRAP command optimized processing enabled. 0: disable; 1: enable.
[7:5] RO		reserved	reserve.
[4] RW after_en			Auto Precharge function enable: 0: disabled; 1: enable.
[3] RW func_clkon			Function module clock switch. 0: internal automatic control clock; 1: Forcibly open the clock.
[2] RW data_clkon			Data lane clock switch. 0: internal automatic control clock; 1: Forcibly open the clock.
[1] RW cmd_clkon			Command channel clock switch. 0: internal automatic control clock; 1: Forcibly open the clock.

[0] RW clk_ratio			Controller working mode. 1: The frequency ratio between DDRC and PHY is 1:2; 0: The frequency ratio between DDRC and PHY is 1:1. Note: The current version needs to be fixed at 1.

DDRC_CFG_WORKMODE2

DDRC_CFG_WORKMODE2 is the DDRC working mode configuration register.

Offset Address	Register Name	Total Reset Value
0x044	DDRC_CFG_WORKMODE2	0x0000_0000

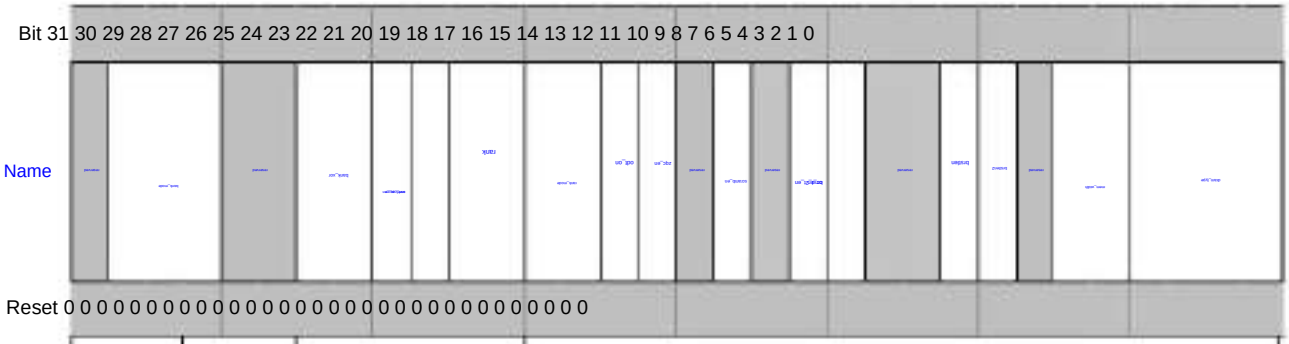
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—		openpage_time																		rank_disable											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:16]	RW	openpage_time	OPEN PAGE delay control: 0x0~0x1: Disable OPEN PAGE function; 0x2~0x3fff: OPEN PAGE delay time. Note: When DDRC_CFG_WORKMODE.apre_en is enabled, the OPEN PAGE function is invalid
[15:0]	RW	rank_disable	RANK disable switch. 0: normal working mode; 1: Disable the AUTO REFRESH/POWER DOWN/SELFRESH function of a certain RANK.

DDRC_CFG_DDRMODE

DDRC_CFG_DDRMODE is the DDRC working mode configuration register.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_CFG_DDRMODE	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	bank_mode	BANK interleave mode. When the memory bus width is 8bit: 000: 8byte interleaving; 001: 16byte interleaving; … 111: 1kbyte interleaving. When the storage bus bit width is 16bit: 000: 16byte interleaving; 001: 32byte interleaving; … 111: 2kbyte interleaving. When the memory bus width is 32bit: 000: 32byte interleaving; 001: 64byte interleaving; … 111: 4kbyte interleaving. When the memory bus width is 64bit: 000: 64byte interleaving; 001: 128byte interleaving; … 111: 8kbyte interleaving. Note: When the configuration of AXI is non-zero, this field must be configured as 000 to work in AXI configuration mode. When AXI configuration is 000, it works in DMC configuration mode.
[27:26]	RO	reserved	reserve.

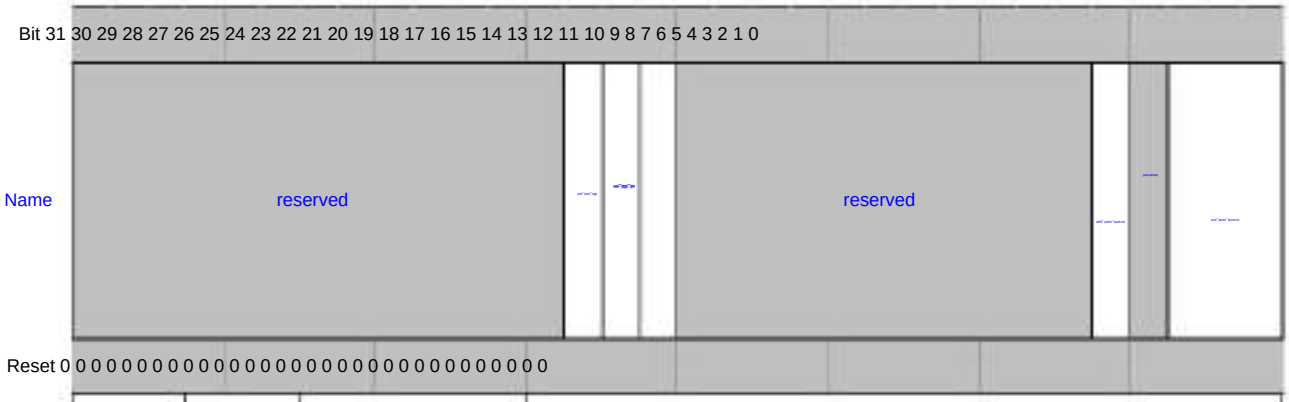
[25:24] RW	bank_xor		BANK address and ROW address scramble enable. 0: forbidden; 1: BANK and offset address 0 are scrambled; 2: BANK and offset address 1 are scrambled; 3: scramble BANK and offset address 2;
[23] RW	asref_zqc_en		SDRAM ZQ enable on ASREF exit. 0: forbidden; 1: enable.
[22] RW	sref_zqc_en		SDRAM ZQ enable on SREF exit. 0: forbidden; 1: enable. Note: Only valid for DDR3 SDRAM, the default configuration is 0. Also note that this configuration bit does not allow dynamic changes during exit self-refresh.
[21:20] RW	rank		Controller RANK configuration. 00: 1 RANK; 01: 2 RANKs; 10: 3 RANKs; 11: 4 RANKs. Note: When the external DDR device is greater than 4 RANKs, this control bit is used for the control of 0-3, 4-7, 8-11, 12-16 four groups of RANK at the same time
[19:18] RW	rank_mode		RANK interleave mode. 00: Single RANK mode; 01: Single RANK mode; 10: Double RANK interleaving; 11: Four RANKs are interleaved. Note: Multi-RANK interleaving can only be used when the RANK configurations are identical. Otherwise, unpredictable errors will occur.
[17] RW	odt_on		The ODT signal output to SDRAM is a fixed value. 0: automatically controlled by DDRC; 1: The fixed output is the wodt configuration of rank0.
[16] RW	zqc_en		Aref module ZQ command enable. 0: forbidden; 1: enable.
[15] RO		reserved	reserve.

[14] RW scramb_en			Data scrambling enabled (use address as seed to generate scrambled code, then XOR with data to reduce sync flipping). 0: forbidden; 1: enable.
[13] RO		reserved	reserve.
[12] RW bc_en			DDR3 Burst Chop mode enabled. 0: forbidden; 1: enable.
[11] RO		reserved	reserve. Must remain 1'b0.
[10:9] RO		reserved	reserve.
[8] RW brushes			Controller Burst Length configuration. When brstlen2 is configured as 0, 1ÿBL8ÿ 0ÿBL4ÿ When brstlen2 is configured as 1, 1ÿBL32ÿ 0ÿBL16ÿ DDR3 can only be configured as Burst8 mode. Note: The burst len here is related to the clk ratio of dmc and phy. Its configuration value should be BLx/n (where x represents 4/8/16/32 burst types, and n represents the clock relationship between dmc and phy is 1:n). Take clk ratio=1:2 as an example, if To configure ddr bl32, you only need to configure brstlen=0;brstlen2=1.
[7] RW brstlen2			Controller Burst Length2 configuration. 1: extended mode; 0: basic mode. Works with brstlen.
[6]	RO	reserved	reserve.
[5:4] RW mem_width			Store data bus width. 00ÿ8bitÿ 01ÿ16bitÿ 10ÿ32bitÿ 11ÿ64bitÿ
[3:0] RW dram_type			External memory type. 110ÿDDR3ÿ Other: reserved.

DDRC_CFG_SCRAMB

DDRC_CFG_SCRAMB is the DDR data scrambling configuration register.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_CFG_SCRAMB	0x0000_0000



Bits	Access Name		Description
[31:19] RO		reserved	reserve.
[18] RW dbi_	ow_act		DBI active level. 0: high effective; 1: Active low.
[17] RW rd_d	bi_en		Read direction DBI enable. 0: forbidden; 1: enable.
[16] RW wr_d	bi_en		Write direction DBI enable. 0: forbidden; 1: enable.
[15:5] RO		reserved	reserve.
[4] RW scram	b_seed_type		Address pattern used for scrambling. 0: use chip select and BA to scramble; 1: Use chip select, BA, and low-order column address to scramble.
[3]	RO	reserved	reserve.

[2:0]	RW	scramb_seed_sort	The address arrangement used for scrambling. 000: CS_BA_COL alignment; 001: CS_COL_BA alignment; 010: COL_CS_BA alignment; 011: COL_BA_CS alignment; 100: BA_CS_COL alignment; 101: BA_COL_CS alignment; Others: reserved.

DDRC_CFG_RNKVOL

DDRC_CFG_RNKVOL is the DDR capacity configuration register for each RANK controlled by DDRC.

Offset Address	Register Name	Total Reset Value
0x060	DDRC_CFG_RNKVOL	0x0000_0022

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	mem_x4	The external device is 4bit device splicing mode. 0: External is composed of 8/16/32bit devices; 1: External is composed of 4bit device splicing.
[15:14]	RO	reserved	reserve.

[13:12] RW	mem_map		SDRAM address decoding mode. 00ÿ{Rank,Row,Ba,Col,DW}= AXI_Addressÿ 01ÿ{Rank,Ba,Row,Col,DW}= AXI_Addressÿ 10ÿ{Rank,Row,Ba,Col,cs,Col,DW}= AXI_Addressÿ 11: {Rank, Ba, Row, Col, cs, Col, DW} = AXI_Address. This parameter can only be configured as 'b10 or 'b11 when DDRC_CONFIG1[dual_ch] is valid. When there are multiple ranks, each rank must use the same configuration. The current version only supports 00 configuration.
[11:10] RO		reserved	reserve.
[9:8] RW	mem_bank		Single chip SDRAM Bank number. 00ÿ4 Bankÿ 01ÿ8 Bankÿ 10ÿ16 Bankÿ 11: Reserved.
[7]	RO	reserved	reserve.
[6:4] RW	mem_row		Single-chip SDRAM row address bit width configuration. 000ÿ11 bitÿ 001ÿ12 bitÿ 010ÿ13 bitÿ 011ÿ14 bitÿ 100ÿ15 bitÿ 101ÿ16 bitÿ Others: reserved.
[3]	RO	reserved	reserve.
[2:0] RW	mem_col		Single-chip SDRAM column address bit width configuration. 000ÿ8 bitÿ 001ÿ9 bitÿ 010ÿ10 bitÿ 011ÿ11 bitÿ 100ÿ12 bitÿ Others: reserved.

DDRC_CFG_ODT

DDRC_CFG_ODT is the ODT feature configuration register of DDR.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_CFG_ODT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	guess	wodt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rodt	ODT configuration of other RANKs when the current RANK sends a read command. 1: enable reading ODT; 0: Disable ODT reading.
[15:0]	RW	wodt	When the current RANK sends a write command, the ODT configuration of other RANKs. 1: enable write ODT; 0: Disable writing to ODT.

DDRC_CFG_EMRS01

DDRC_CFG_EMRS01 is the configuration register of mode register 0 and mode register 1 of DDR.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_CFG_EMRS01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	emrs1	mrs
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDR3 SDRAM Extended Mode Register 1. Corresponding to Mode Register 1 (MR1) effective bits in DDR3 SDRAM manual: [13:0]. Among them, MR1[15:14] of most ddr devices is not used, then DDRC_CFG_EMRS01 [31:30] is reserved and set to 2'b00. Note: For the specific explanation of MR1, please refer to the manual of the DDR3 SDRAM used.
[15:0]	RW	mrs	DDR3 SDRAM mode register. Corresponding to Mode Register 0 (MR0) effective bits in DDR3 SDRAM manual: [13:0]. Among them, MR0[15:14] of most ddr devices is not used, so DDRC_CFG_EMRS01 [15:14] is reserved and set to 2'b00. Note: For the specific explanation of MR0, please refer to the manual of the DDR3 SDRAM used.

DDRC_CFG_EMRS23

DDRC_CFG_EMRS23 is the configuration register of mode register 2 and mode register 3 of DDR.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_CFG_EMRS23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	emrs3	emrs2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDR3 SDRAM Extended Mode Register 3. Corresponding to Mode Register 3 (MR3) effective bits in DDR3 SDRAM manual: [13:0]. Among them, MR3[15:14] of most ddr devices is not used, so DDRC_CFG_EMRS23 [31:30] is reserved and set to 2'b00. Note: For the specific explanation of MR3, please refer to the manual of the DDR3 SDRAM used.
[15:0]	RW	emrs2	DDR3 SDRAM Extended Mode Register 2. Corresponding to Mode Register 2 (MR2) effective bits in DDR3 SDRAM manual: [13:0]. Among them, MR2[15:14] of most ddr devices is not used, and DDRC_CFG_EMRS23 [15:14] is reserved and set to 2'b00. Note: For the specific explanation of MR2, please refer to the manual of the DDR3 SDRAM used.

DDRC_CFG_TIMING0

DDRC_CFG_TIMING0 is the timing parameter register 0 of DDRC.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_CFG_TIMING0	0xFFFF_FF3F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tmrd				trrd				trp					trcd					trc					-----				after				
Reset	1	1	1	1	1	1	1	1	1					1	1	1			1	1	1	1	1	1			1	1	0	0	1	1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Wait period for the Load Mode Register (LMR) command (configured as tMRD for DDR3). 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[27:24]	RW	trrd	Waiting period from opening BANK A to opening BANK B (ACT bank a to ACT bank b). 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[23:19]	RW	trp	Turn off (PRE period) command waiting period. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[18:14]	RW	trcd	Same as BANK activation to read or write (ACT to READ or WRITE) command wait period. 0x0~0x3: 3 clock cycles; 0x4~0xF: n clock cycle.
[13:8]	RW	trc	It is the same as the wait period from active a bank to active a bank of BANK. 0x00~0x01: 1 clock cycle; 0x02~0x3F: n clock cycles.
[7:6]	RO	reserved	reserve.
[5:0]	RW	tras	It is the same as the wait period from the activation command to the close command (ACT to PRE) of BANK. This product supports a maximum configuration of 0xF. 0x00~0x01: 1 clock cycle; 0x02~0x0F: n clock cycles.

DDRC_CFG_TIMING1

DDRC_CFG_TIMING1 is the timing parameter register 1 of DDRC.

Offset Address	Register Name	Total Reset Value
0x104	DDRC_CFG_TIMING1	0xFF22_15FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trtw				twl				tcl				—				trfc							
Reset	1	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Exit the wait cycle from Self-Refresh to read command. 0x0: reserved; 0x01~0xFF: n×4 clock cycles. For DDR3 SDRAM, this value configures the maximum value of tXSDLL and tXS.
[23:20]	RW	trtw	Latency from last read data to first write data. 0x0~0x1: 1 clock cycle; 0x2~0xF: n+1 clock cycles. Note: In DDR3 mode, the trtw parameter mainly considers the delay of the board, package and IO.
[19:15]	RW	stupid	Wait period from write command to write data. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles. For example: 0x3: 3 clock cycles. Note: The clock cycle is DDR3 clock cycle.
[14:10]	RW	tcl	The delay from DDR read command to read data (CAS Latency). 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles. Note: The clock cycle is DDR3 clock cycle.
[9]	RO	reserved	reserve.
[8:0]	RW	trfc	Auto refresh command period and auto refresh to active (AREF period or AREF to ACT) command waiting period. This register chooses to configure a large value of max{trfc,tzqcs}. 0x00: reserved; 0x01~0x1FF: n clock cycles.

DDRC_CFG_TIMING2

DDRC_CFG_TIMING2 is the timing parameter register 2 of DDRC.

Offset Address	Register Name	Total Reset Value
0x108	DDRC_CFG_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved								wow				---	tariff										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	The minimum time to maintain a low power state. 0x0: reserved; 0x1~0xF: n clock cycles. This value needs to configure the maximum value among several values of tCKESR, tCKSRE, tCKSRX, tCKE and tCPDED.
[27:24]	RW	twtr	The last write operation wait cycle from write data to read command (write to read). 0x0~0x1: 1 clock cycle; 0x2~0xf: n clock cycles. Such as 0x3: 3 clock cycles.
[23:18]	RO	reserved	reserve.
[17:12]	RW	tfaw	4 consecutive active command cycles. 0x00ÿ0x3F: n clock cycles; eg: 0x14: 20 clock cycles.
[11]	RO	reserved	reserve.
[10:0]	RW	taref	Automatic refresh cycle. 0x000: Auto-refresh disabled; 0x001~0x7FF: SDRAM refresh cycle time is 16×n clock cycles. Such as 0x008: 128 clock cycles (16×8). Configure the interval time as tREFI = 7800/16/tclk. Tclk is twice the operating cycle of DDR.

DDRC_CFG_TIMING3

DDRC_CFG_TIMING3 is the timing parameter register 3 of DDRC.

Offset Address	Register Name	Total Reset Value
0x10C	DDRC_CFG_TIMING3	0xFFFF_E0F2

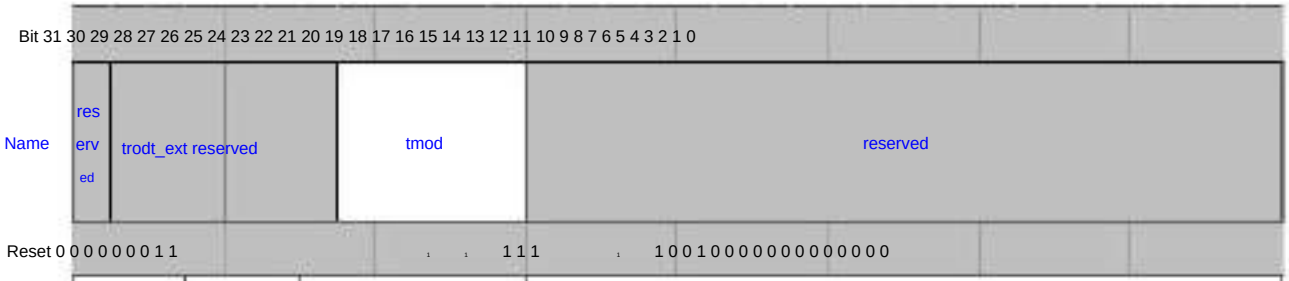
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd											tzzinit										year			bad			trtp				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	ZQCS command cycle. 0x000: ZQCS command disabled; 0x001ÿ0x3FF: n×128 AREF cycles. The ZQCS command cycle time is n×128 taref clock cycles.
[21:13]	RW	tzqinit	ZQ initialization delay period. 0x0~0x1ff: nx4 clock cycles. This value configures the maximum value of tZQINIT, tDLLK.
[12:8]	RW	taond	ODT (On-die termination) open and close cycle. In DDR3 mode, the value is configured as tWL-2 (tWL is DDRC_CFG_TIMING1[twl]).
[7:4]	RW	xard	Exit DDR low-power state wait cycle. 0x0ÿ0xF: n clock cycles, n represents a decimal number; eg: 0x7: 7 clock cycles. Take the maximum value among {tXP,tXARD,tXARDS,tXS}. In DDR3 mode, take (tXP, the maximum value of tCKE).
[3:0]	RW	trtp	Wait delay from read command to close command. 0x0~0x2: 2 clock cycles; 0x3~0xF: n clock cycles. The calculation formula of Trtp is AL+BL/2+Max(trtp,2)-2.

DDRC_CFG_TIMING4

DDRC_CFG_TIMING4 is the timing parameter register 4 of DDRC.

Offset Address	Register Name	Total Reset Value
0x110	DDRC_CFG_TIMING4	0x01FF_2000

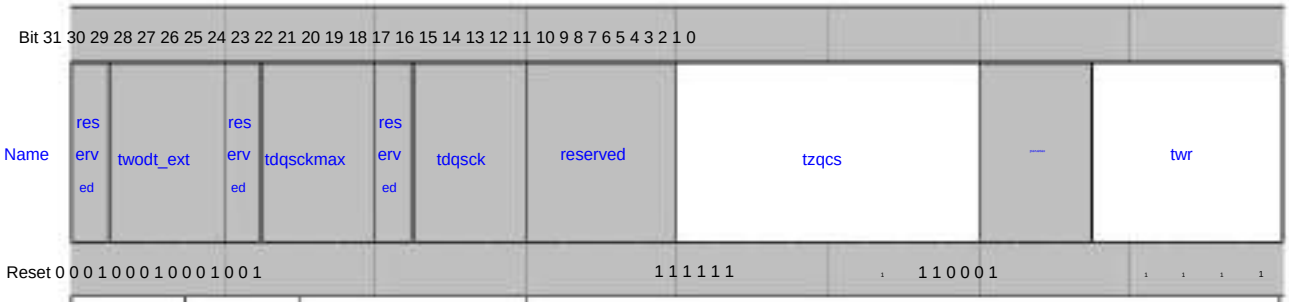


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	trodt_ext	reserve.
[27:25]	RO	reserved	reserve
[24:20]	RW	tmod	Valid delay parameters from MRS command to ODT and ZQCL. 0x0~0x1: 1 clock cycle; 02~0x1F: n clock cycles.
[19:0]	RO	reserved	reserve.

DDRC_CFG_TIMING5

DDRC_CFG_TIMING5 is the timing parameter register 5 of DDRC.

Offset Address	Register Name	Total Reset Value
0x114	DDRC_CFG_TIMING5	0x1113_FF1F



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	twodt_ext	reserve.
[27]	RO	reserved	reserve.
[26:24]	RW	tdqsckmax	The maximum output access time of DQS relative to CK, this parameter does not need to be concerned in DDR3 mode.

[23] RO		reserved	reserve.
[22:20] RW	tdqsck		The output access time of DQS relative to CK, this parameter does not need to be concerned in DDR3 mode, keep the default value.
[19:16] RO		reserved	reserve
[15:8] RW	tzqcs		ZQCS calibration delay period. 0x0~0xff: n*2 clock cycles. Due to the design of dmc, this value needs to be constrained to be greater than or equal to 10
[7:5] RO		reserved	reserve.
[4:0] RW	tower		Write recovery wait period. 0x0~0x1: 1 clock cycle; 0x2~0x1f: n clock cycles. Note: When DFS is required, the tWR parameter needs to be configured according to the highest possible frequency of the chip in DFS. And the configuration of tWR cannot be modified with the frequency change of DDR.

DDRC_CFG_TIMING6

DDRC_CFG_TIMING6 is the timing parameter register 6 of DDRC.

Offset Address	Register Name	Total Reset Value
0x118	DDRC_CFG_TIMING6	0x0000_00FF

Bit	31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	trrd_l	twtr_l	tccd_l	reseverd	tcksrx	thank you
Reset	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	trrd_l	trrd wait period between Bank Groups. 0x0~0x1: 1 clock cycle 0x2~0xf: n clock cycles.
[19:16]	RW	twtr_l	twtr wait period between Bank Groups. 0x0~0x1: 1 clock cycle 0x2~0xf: n clock cycles.
[15:12]	RW	tccd_l	tccd wait period between Bank Groups. 0x0~0x1: 1 clock cycle 0x2~0xf: n clock cycles.

[11:8] RW	todt_sft		reserve.
[7:4] RW	tcksrx		tCKSRX parameter for DDR3. The effective number of ticks the clock needs to advance before exiting self-refresh. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.
[3:0] RW	tcksre		tCKSRE parameter for DDR3. The number of beats the clock needs to hold after entering self-refresh. 0x0~0x1: 1 clock cycle; 0x2~0xF: n clock cycles.

DDRC_CFG_TIMING7

DDRC_CFG_TIMING7 is the timing parameter register 7 of DDRC.

Offset Address	Register Name	Total Reset Value
0x11c	DDRC_CFG_TIMING7	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10	9 8 7	6 5 4	3 2 1	0
Name	reserved	dim_trtr	dim_twtw	rnk_trtr	rnk_twtw	rnk_trtw	rnk_twtr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	dimm_trtr	The read-to-read switching between DIMMs is based on the additional delay added by rnk_trtr, which is used to match the maximum skew between DIMMs.
[19:16]	RW	dimm_twtw	Write-to-write switching between DIMMs is based on the additional delay added by rnk_twtw, which is used to match the maximum skew between DIMMs.
[15:12]	RW	rnk_trtr	Read-to-read latency between RANKs.
[11:8]	RW	rnk_twtw	Write-to-write delay between RANKs.
[7:4]	RW	rnk_trtw	Read to write delay between RANK.
[3:0]	RW	rnk_twtr	Write-to-read latency between RANKs.

DDRC_CFG_BLDATA

DDRC_CFG_BLDATA is the DDRC write data pre-receive write data configuration register.

Offset Address	Register Name	Total Reset Value
0x140	DDRC_CFG_BLDATA	0x0000_0002

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	bl_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	bl_data	In the current mode, the number of DMC data beats corresponding to each DDR command. 0x0~0xF: n beats.

DDRC_CFG_DMCLVL

DDRC_CFG_DMCLVL is the command queue depth watermark configuration register for DDR controller.

Offset Address	Register Name	Total Reset Value
0x144	DDRC_CFG_DMCLVL	0x0000_0008

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	mbist_que_level	—	which level
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0			

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:8]	RW	mbist_que_level	When the MTEST or MCLR function is used, the number of command BUFFERs started by DMC. 0x0: 1. 0x1~0x10: 1~16, the maximum value is related to the code configuration.
[7:5]	RO	reserved	reserve.
[4:0]	RW	que_level	In DMC, the depth of the command register FIFO. 0x1ÿ0x10: n command depth. Others: reserved.

DDRC_CFG_DDRPHY

DDRC_CFG_DDRPHY is the DDR IO configuration register.

Offset Address	Register Name	Total Reset Value
0x200	DDRC_CFG_DDRPHY	0x001F_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	wr_busy_dly	tired / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 1 1 1	1 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:16]	RW	wr_busy_dly	Used internally by the PHY as a gating signal for data beats. Must be configured greater than WL+2. For scenarios that are not sensitive to power consumption, it can be configured as 0x1F.
[15:13]	RO	reserved	reserve.
[12]	RW	phy_updenn	The controller initiates dfi_phyupd_en in response to DDRPHY. 0: forbidden; 1: enable.
[11:8]	RW	trdlat	DDRPHY inherent latency. 0x0~0xF: n+1 cycles. It needs to be configured as 8 when using synopsys3/2phy.
[7:0]	RO	reserved	reserve.

DDRC_CFG_SFC_TIM

DDRC_CFG_SFC_TIM is the timing register for DDRC software configuration DDR command.

Offset Address	Register Name	Total Reset Value
0x20C	DDRC_CFG_SFC_TIM	0x0000_0000

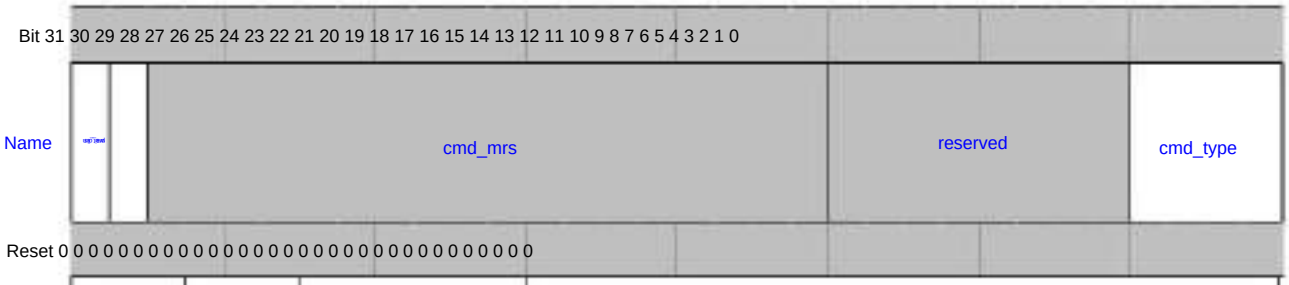
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / wait_time
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	wait_time	The waiting time after executing the DDR command configured by SFC. Valid when DDRC_CFG_SFC[wait_en] is 1.

DDRC_CFG_SFC

DDRC_CFG_SFC Configure DDR command attribute command for DDRC software.

Offset Address	Register Name	Total Reset Value
0x210	DDRC_CFG_SFC	0x0000_0000



Bits	Access	Name	Description
[31]	RW	wait_en	Wait for a while after executing the command before exiting. 0: forbidden; 1: enable. The waiting time is configured by the DDRC_CFG_SFC_TIM register.
[30]	RW	pre_dis	Sending the PRECHARGE command is prohibited. 0: Send precharge before every SFC command; 1: Don't send precharge before every SFC command, send the corresponding command directly.
[29:12]	RW	cmd_mrs	When configuring the LMR command, the DDR mode register configures the value. During RDMRS or RD operation, it is used to select which beat is valid data.
[11:4]	RO	reserved	reserve.

[3:0]	RW	cmd_type	DDR command configuration. 0x0: Deep Power Down enter; 0x1: Deep Power Down exit; 0x2: Load Mode Register (LMR) command; 0x3: ZQCL command; 0x4: WRITE command; 0x5: READ command; 0x6: PRECHARGE ALL command; 0x7: READ MRS command; 0x8: AREF command; 0x9: SELF REFRESH enter; 0xA: SELF REFRESH exit; 0xF: DFI_CTRL_UPD_REQ/ACK handshake, requesting PHY to enter refresh mode (this operation is not supported yet). Other: reserved

DDRC_CFG_SFC_ADDR0

DDRC_CFG_SFC_ADDR0 is SFC read and write memory address configuration register 0.

Offset Address	Register Name	Total Reset Value
0x214	DDRC_CFG_SFC_ADDR0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sfc_row	sfc_col
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	sfc_row	SFC reads and writes access memory row address. The configuration of the maximum address bit width is related to the actual connected device specifications.
[11:0]	RW	sfc_col	SFC reads and writes to access the column address of memory. Note: The access data address of DDRC needs to be aligned with the bit width of the current DMC. For example, the current DMC bit width is 128bit: External 64/72bitDDR. DMC access column address according to {sfc_col[15:1],1'b0} to access external 32 /36bitDDR.DMC Access column address according to {sfc_col[15:2],2'b0}

DDRC_CFG_SFC_ADDR1

DDRC_CFG_SFC_ADDR1 is SFC read and write memory address configuration register 1.

Offset Address	Register Name	Total Reset Value
0x218	DDRC_CFG_SFC_ADDR1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Name	sfc_rank	reserved	sfc_bank
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	sfc_rank	The ddr_rank of the executed command. 0: do not execute; 1: execute. Note: Each bit corresponds to a RANK control
[15:4]	RO	reserved	reserve.
[3:0]	RW	sfc_bank	SFC reads and writes access to the bank address of memory.

DDRC_CFG_SFC_WDATA0

DDRC_CFG_SFC_WDATA0 is the SFC write data configuration register.

Offset Address	Register Name	Total Reset Value
0x21C	DDRC_CFG_SFC_WDATA0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wdata0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	wdata0	SFC write data[31:0].

DDRC_CFG_SFC_WDATA1

DDRC_CFG_SFC_WDATA1 is the SFC write data configuration register.

Offset Address	Register Name	Total Reset Value
0x220	DDRC_CFG_SFC_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW wdata1	SFC write data[63:32].

DDRC_CFG_SFC_WDATA2

DDRC_CFG_SFC_WDATA2 is the SFC write data configuration register.

Offset Address	Register Name	Total Reset Value
0x224	DDRC_CFG_SFC_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW wdata2	SFC write data[95:64].

DDRC_CFG_SFC_WDATA3

DDRC_CFG_SFC_WDATA3 is the SFC write data configuration register.

Offset Address	Register Name	Total Reset Value
0x228	DDRC_CFG_SFC_WDATA3	0x0000_0000

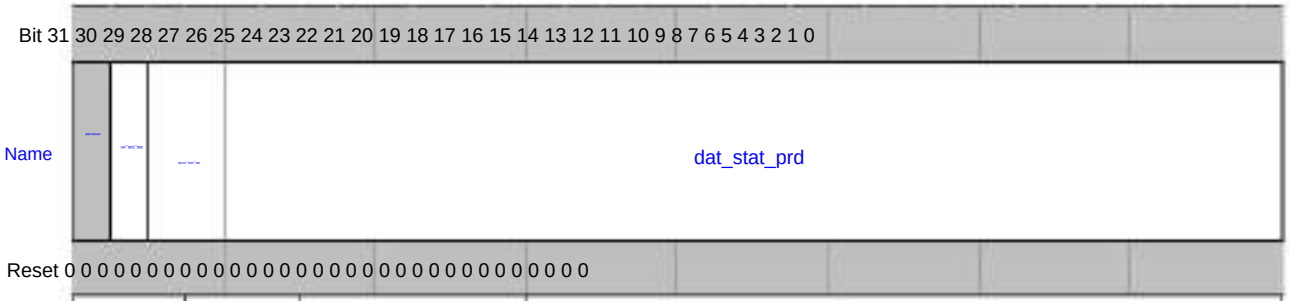
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW wdata3	SFC write data[127:96].

DDRC_CFG_STADAT

DDRC_CFG_ STADAT is the DDRC data statistics enable register.

Offset Address	Register Name	Total Reset Value
0x254	DDRC_CFG_ STADAT	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	dat_stat_en	DDR data statistics enable. 0: forbidden; 1: enable. Note: When dat_stat _mode =0, enabling this bit means that the performance statistics register will start to cycle count. When dat_stat _mode=1, this bit will be cleared to 0 automatically after completing a statistics.
[29:28]	RW	dat_stat _mode	Statistics mode. 00: Continuous trigger mode. Counters related to performance statistics count continuously. It can ensure that in the continuous statistics mode, the statistics will not overflow within 1s. 01: Single trigger mode. After the performance statistics time expires perf_prd, the statistics results will be kept and the statistics will stop. The statistical cycle arrives and reports the interruption. 10: Trigger based on threshold. When the statistics period arrives, if it is within the specified threshold range, no interruption will be reported, and at the same time, the statistics will be restarted until it exceeds the specified threshold range, and an interruption will be reported. Stop counting when the threshold range is exceeded. Other: reserved. Note: When dat_stat_mode is 2'b01 and 2'b10, the statistical value will be kept after overflow; when dat_stat_mode is 2'b00, the statistical value will wrap around after overflow.
[27:0]	RW	dat_stat_prd	Data statistics cycle. 0x0~0x1: invalid configuration. 0x2~0xFFFFFFF: statistics period. The actual statistical cycle is load_stat_prd*16*tclk (Tclk is the DDRC bus clock cycle). Note: This configuration is only valid when load_stat_mode=2'b01 or 2'b10. In the continuous statistics mode of load_stat_mode=0, the counters related to performance statistics will keep counting.

DDRC_CFG_DATMIN

DDRC_CFG_DATMIN is the minimum threshold register for DMC data count.

Offset Address	Register Name	Total Reset Value
0x258	DDRC_CFG_ DATMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / dmc_dat_min
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	dmc_dat_min	Data statistics threshold register, when the data is less than or equal to the threshold, an interrupt is reported. Note: The threshold here is in units of 32, that is, if the configuration is n, the final threshold is n *32.

DDRC_CFG_DATMAX

DDRC_CFG_DATMAX is the maximum threshold register for DMC data count.

Offset Address	Register Name	Total Reset Value
0x25c	DDRC_CFG_ DATMAX	0x0000_0000

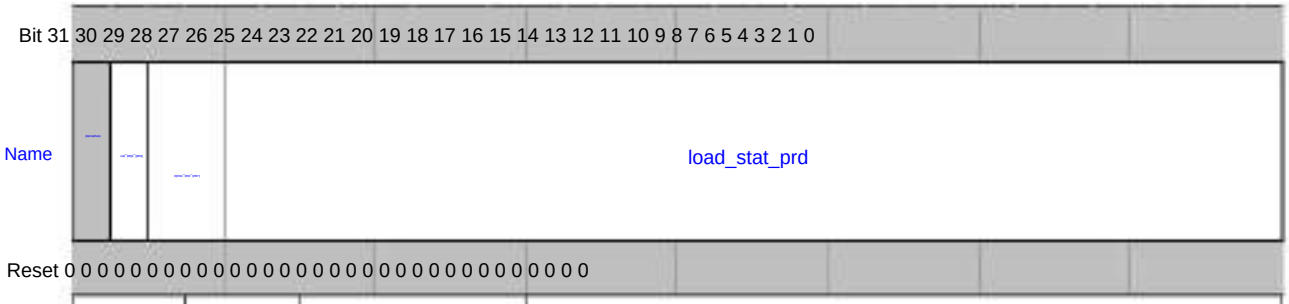
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / dmc_dat_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	dmc_dat_max	Data statistics threshold register, when the data is greater than or equal to the threshold, an interrupt is reported. Note: The threshold here is in units of 32, that is, if the configuration is n, the final threshold is n*32.

DDRC_CFG_STACMD

DDRC_CFG_STACMD is the mode configuration register for DDR performance statistics.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_CFG_ STACMD	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve
[30]	RW	load_stat_en	DDR load statistics enable. 0: forbidden; 1: enable. Note: When dat_stat_mode=0, enabling this bit means that the performance statistics register will start counting in circles. When load_stat_mode=1, after completing a statistics, this bit is automatically cleared
[29:28]	RW	load_stat _mode	Load statistics mode. 00: Continuous trigger mode. Counters related to performance statistics count continuously. It can ensure that in the continuous statistics mode, the statistics will not overflow within 1s. 01: Single trigger mode. After the performance statistics time expires perf_prd, the statistics results will be kept and the statistics will stop. The statistical cycle arrives and reports the interruption. 10: Trigger based on threshold. When the statistical period arrives, if it is within the specified threshold range, no interruption will be reported, and at the same time, the statistics will be restarted until it exceeds the specified threshold range, and an interruption will be reported. Stop counting when the threshold range is exceeded. Other: reserved. Note: If the result of load statistics exceeds the maximum count range, it will wrap around after overflow.
[27:0]	RW	load_stat_prd	Load statistics cycle. 0x0~0x1: invalid configuration. 0x2~0xFFFFFFF: statistics period. The actual statistical period is perf_prd*16*tclk (Tclk is the DDRC bus clock period). Note: This configuration is only valid when perf_mode=1. When the continuous statistics mode of perf_mode=0, the counters related to performance statistics will keep counting.

DDRC_CFG_CMDMIN

DDRC_CFG_CMDMIN is the minimum threshold register for DMC command count.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_CFG_ CMDMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dmc_cmd_min
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	dmc_cmd_min	Command statistics threshold register, when the command is less than or equal to the threshold, an interrupt is reported. Note: The threshold here is in units of 32, that is, if the configuration is n, the final threshold is n*32.

DDRC_CFG_CMDMAX

DDRC_CFG_CMDMAX is the maximum threshold register for DMC command count.

Offset Address	Register Name	Total Reset Value
0x268	DDRC_CFG_ CMDMAX	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dmc_cmd_max
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	dmc_cmd_max	Command statistics threshold register, when the command is greater than or equal to the threshold, an interrupt is reported. Note: The threshold here is in units of 32, that is, if the configuration is n, the final threshold is n*32.

DDRC_CFG_PERF

DDRC_CFG_PERF is the mode configuration register for DDR performance statistics.

Offset Address	Register Name	Total Reset Value
0x270	DDRC_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																															perf_prd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:30]	RO	reserved	reserve.
[29]	RW flux_en		DMC flow monitoring enabled. 0: Flow monitoring is off. 1: Flow monitoring is enabled. When traffic monitoring is enabled, the statistical module will feed back the number of cycles occupied by the DDR interface to each requesting port according to the ID number. Flow control can be performed with the flow setting of the port.
[28]	RW perf_mode		performance statistics mode. 0: Continuous trigger mode. Counters related to performance statistics count continuously. It can guarantee that in the continuous statistics mode, the statistics will not overflow within 1s. 1: Single trigger mode. After the performance statistics time expires perf_prd, the statistics results will be kept and the statistics will stop. Note: Keep when the statistics value overflows.
[27:0]	RW perf_prd		Performance statistics cycle. 0x0~0x1: invalid configuration. 0x2~0xFFFFFFF: statistics period. The actual statistical period is perf_prd*16*tclk (Tclk is the DDRC bus clock period). Note: This configuration is only valid when perf_mode=1. When the continuous statistics mode of perf_mode=0, the counters related to performance statistics will keep counting.

DDRC_CFG_STAID

DDRC_CFG_STAID is the command ID configuration register for DDR performance statistics.

Offset Address	Register Name	Total Reset Value
0x274	DDRC_CFG_STAID	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sta_id
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	sta_id	Configure performance statistics for the specified ID. Used in conjunction with sta_idmask.

DDRC_CFG_STAIDMSK

DDRC_CFG_STAIDMSK is the command ID MASK configuration register for DDR performance statistics.

Offset Address	Register Name	Total Reset Value
0x278	DDRC_CFG_STAIDMSK	0x0000_FFFF

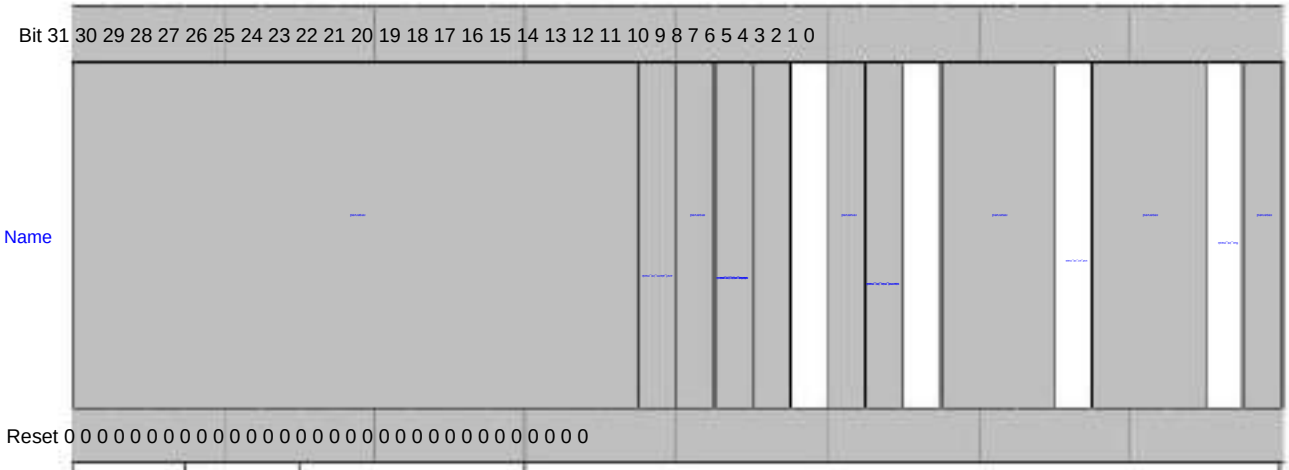
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sta_idmask
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	sta_idmask	Configure to mask the signal for the specified ID. The performance statistics-related registers in DDRC only count the commands with a specific ID. Cmd_id (DDRC internal command ID) & sta_idmask=sta_id.

DDRC_INTMSK

DDRC_INTMSK is the DDRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_INTMSK	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	enable aref_alarm_int_mask	DDR AREF command interrupt mask 1: mask interrupt; 0: enable interrupt.
[15]	RO	reserved	reserve
[14]	RW	enable stadat_max_int_mask	DDR data statistics overflow interrupt mask 1: mask interrupt; 0: Enable interrupts.
[13]	RW	enable stadat_min_int_mask	DDR data statistical cycle arrival or underflow interrupt mask 1: mask interrupt; 0: Enable interrupts.
[12]	RW	enable. rdtimeout_int_mask	DDRPHY Read data timeout interrupt mask interrupt; 0: enable 1: Mask interrupt.
[11]	RO	reserved	reserve.
[10]	RW	enable stacmd_max_int_mask	DDR LOAD statistical overflow interrupt mask 1: mask interrupt; 0: enable interrupt.
[9]	RW	enable. stacmd_min_int_mask	DDR LOAD statistical cycle arrival or underflow interrupt mask 0: enable interrupt; 1: Mask interrupt.
[8:6]	RO	reserved	reserve.

[5] RW	sref_err_int_mask		There is a command access error on the interface during DDR self-refresh. 0: enable interrupt; 1: Mask interrupt.
[4:2] RO		reserved	reserve.
[1] RW	flux_int_mask		DDR FLUX statistical cycle arrival interrupt mask enable 0: enable interrupt; 1: Mask interrupt.
[0]	RO	reserved	reserve.

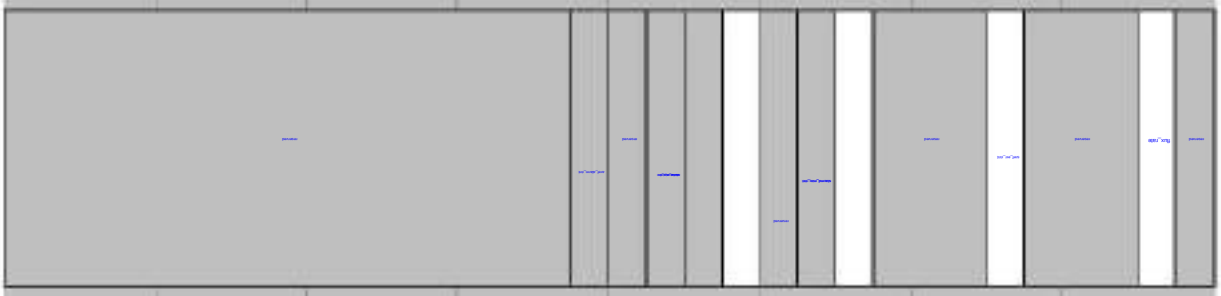
DDRC_RINT

DDRC_RINT is the DDRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_RINT	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name



Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	INT_WC	aref_alarm_rint	DDR AREF command error raw interrupt. Write 1 to clear the interrupt.
[15]	RO	reserved	reserve.
[14]	INT_WC	stadat_max_rint	DDR data statistics exceed the upper threshold interrupt, write 1 to clear the interrupt.
[13]	INT_WC	stadat_min_rint	DDR data statistical period reaches or falls below the lower threshold interrupt, write 1 to clear the interrupt.
[12]	INT_WC	rdtimeout_rint	DDRPHY Read data timeout raw interrupt. Write 1 to clear the interrupt.
[11]	RO	reserved	reserve.
[10]	INT_WC	stacmd_max_rint	DDR LOAD Statistics exceed the upper threshold interrupt, write 1 to clear the interrupt.
[9]	INT_WC	stacmd_min_rint	The DDR LOAD statistical period reaches or falls below the lower threshold and is interrupted. Write 1 to clear the interrupt.

[8:6] RO		reserved	reserve.
[5]	INT_WC sref_err_rint		Self-refresh interface command access interrupt. Write 1 to clear the interrupt.
[4ÿ2] RO		reserved	reserve.
[1] RW flux_rint			DDR FLUX statistical cycle arrival interrupt. Write 1 to clear the interrupt.
[0]	RO	reserved	reserve.

DDRC_INTSTS

DDRC_INTSTS is the DDRC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_INTSTS	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:17] RO		reserved	reserve.
[16]	INT	aref_alarm_intsts	DDR AREF command error interrupt. 0: no interrupt; 1: There is an interrupt.
[15] RO		reserved	reserve.
[14]	INT	stadata_max_intsts	DDR data statistics overflow interrupt. 0: no interrupt; 1: There is an interrupt.
[13]	INT	stadata_min_intsts	DDR data statistics cycle arrival or underflow interrupt. 0: no interrupt; 1: There is an interrupt.

[12]	INT	rdtimeout_intsts	DDRPHY Read data timeout interrupt. 0: no interrupt; 1: There is an interrupt.
[11] RO		reserved	reserve.
[10]	INT	stacmd_max_intsts	DDR LOAD statistics overflow interrupt. 0: no interrupts; 1: There is an interrupt.
[9]	INT	stacmd_min_intsts	DDR LOAD statistical cycle arrival or underflow interrupt. 0: no interrupts; 1: There is an interrupt.
[8:6] RO		reserved	reserve.
[5]	INT	sref_err_intsts	The self-refresh interface has interrupts for command access. 0: no interrupt; 1: interrupt.
[4:2] RO		reserved	reserve.
[1]	INT	flux_intsts	DDR FLUX statistical cycle arrival interrupt. 0: no interrupt; 1: There is an interrupt.
[0]	RO	reserved	reserve.

DDRC_CURR_STATUS

DDRC_CURR_STATUS is the DDRC status register.

Offset Address	Register Name	Total Reset Value
0x290	DDRC_CURR_STATUS	0x0000_0101

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved, busy_func, reserved, busy_dmc, reserved, busy

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1

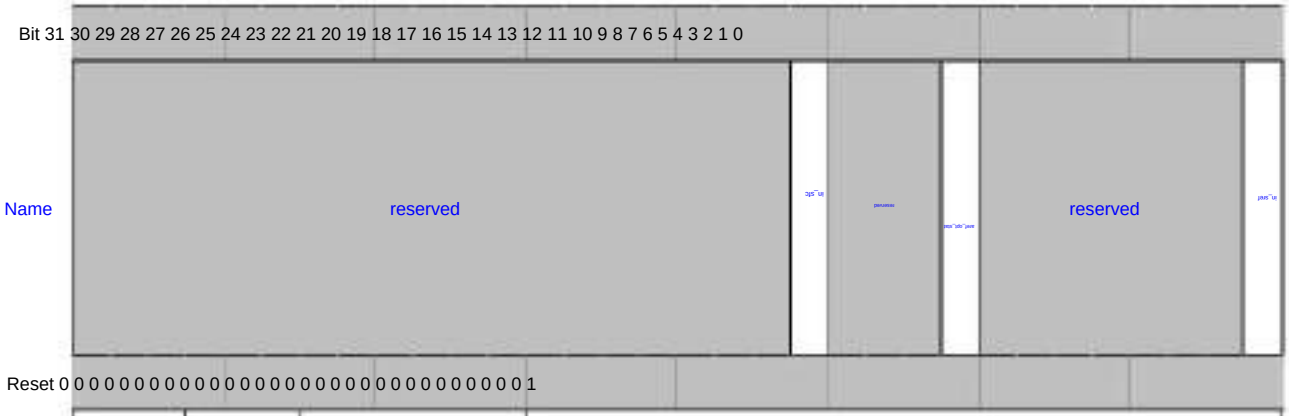
Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.

[8]	RO	busy_func	Busy status register for the DDRC FUNC module. (Reset is in sref state). 0: idle; 1: Command processing.
[7:5] RO		reserved	reserve.
[4]	RO	busy_dmc	Busy status register for the DDRC DMC module. 0: idle; 1: Command processing.
[3:1] RO		reserved	reserve.
[0]	RO	busy	DDRC Overall Busy Status Register. 0: idle; 1: Command processing.

DDRC_CURR_FUNC

DDRC_CURR_FUNC is the status register of DDRC FUNC module.

Offset Address	Register Name	Total Reset Value
0x294	DDRC_CURR_FUNC	0x0000_0001



Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RO		in_sfc	DDRC SFC Status Register. 0: idle; 1: SFC command processing.
[11:9] RO		reserved	reserve.
[8]	RO	aref_opt_stat	Automatically refreshes the optimization mode status indication. 1: Indicates that it is in optimization mode; 0: Indicates that it has exited optimization mode.

			Note: Before software configuration or requesting to enter self-refresh through the csysreq interface, it is necessary to ensure that the auto-refresh optimization mode has been exited. Because when in self-refresh optimization mode, there may be postponed commands that were not sent.
[7:1] RO		reserved	reserve.
[0]	RO	in_sref	DDRC self-refresh status. 1: Self-refresh state; 0: Normal state.

DDRC_CURR_FUNC2

DDRC_CURR_FUNC2 is the status register of DDRC FUNC2 module.

Offset Address	Register Name	Total Reset Value
0x298	DDRC_CURR_FUNC2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	in_asref	in_pd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:15] RO		in_asref	DDRC automatic self-refresh status. 1: Automatic self-refresh state; 0: Normal state. Each bit represents a Rank.
[15:0] RO		in_pd	DDRC PowerDown state. 1: PowerDown state; 0: Normal state. Each bit represents a Rank.

DDRC_CURR_EXECST

DDRC_CURR_EXECST is the state of DDRC command state machine.

Offset Address	Register Name	Total Reset Value
0x2A0	DDRC_CURR_EXECST	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dmc_ct	dmc_cv
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	dmc_ct	Controller command type. 0: means read command; 1: Indicates a write command.
[15:0]	RO	dmc_cv	Whether the controller command is valid. 0: Invalid; 1: Indicates valid.

DDRC_CURR_WGFIFOST

DDRC_CURR_WGFIFOST Write FIFO empty full status register for DDRC.

Offset Address	Register Name	Total Reset Value
0x2A4	DDRC_CURR_WGFIFOST	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	wgntfifo_e	WGNT_FIFO is empty and full. Empty means that all write data has been received, and non-empty means that write data has not been received. 1: FIFO empty; 0: FIFO is not empty.

DDRC_HIS_FLUX_WR

DDRC_HIS_FLUX_WR is the flow statistics register of all write commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x380	DDRC_HIS_FLUX_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	flux_wr	MASTER write traffic statistics for all DDRC IDs. Count within the effective statistical period. The unit is DMC bit width. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_FLUX_RD

DDRC_HIS_FLUX_RD is the flow statistics register of all read commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x384	DDRC_HIS_FLUX_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	flux_rd	MASTER read traffic statistics for all DDRC IDs. Count within the effective statistical period. The unit is DMC bit width. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_FLUX_WCMD

DDRC_HIS_FLUX_WCMD is the number of all write commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x0388	DDRC_HIS_FLUX_WCMD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flux_wr_cmd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	flux_wr_cmd	Statistics of the number of MASTER write commands for all DDRC IDs. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_FLUX_RCMD

DDRC_HIS_FLUX_RCMD is the number of all read commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x038C	DDRC_HIS_FLUX_RCMD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flux_rd_cmd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	flux_rd_cmd	Statistics of the number of MASTER read commands of all IDs in DDRC. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_FLUXID_WR

DDRC_HIS_FLUXID_WR specifies ID for DDRC to write flow statistics register.

Offset Address	Register Name	Total Reset Value
0x390	DDRC_HIS_FLUXID_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	fluxid_wr	DDRC MASTER write traffic statistics for the specified ID. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero. Note: The unit is DMC data bit width (128bit).

DDRC_HIS_FLUXID_RD

DDRC_HIS_FLUXID_RD specifies ID for DDRC to read flow statistics register.

Offset Address	Register Name	Total Reset Value
0x394	DDRC_HIS_FLUXID_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	fluxid_rd	DDRC MASTER read traffic statistics of the specified ID. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero. Note: The unit is DMC data bit width (128bit).

DDRC_HIS_FLUXID_WCMD

DDRC_HIS_FLUXID_WCMD is the number of all write commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x0398	DDRC_HIS_FLUXID_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	fluxid_wr_cmd	DDRC Counts the number of MASTER write commands with the specified ID. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_FLUXID_RCMD

DDRC_HIS_FLUXID_RCMD is the number of all read commands of DDRC.

Offset Address	Register Name	Total Reset Value
0x039C	DDRC_HIS_FLUXID_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	fluxid_rd_cmd	DDRC Counts the number of MASTER read commands with the specified ID. Count within the effective statistical period. Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_WLATCNT0

DDRC_HIS_WLATCNT0 specifies the write command latency statistics register 0 of ID for DDRC.

Offset Address	Register Name	Total Reset Value
0x3A0	DDRC_HIS_WLATCNT0	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wlatcnt_max	wlatcnt_min
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access Name	Description
[31:16]	RO wlatcnt_max	DDRC The maximum latency statistics of the write command with the specified ID. When the next statistics starts, it will be cleared to zero.
[15:0]	RO wlatcnt_min	DDRC specifies the minimum latency statistics of write commands with ID. If overflow maintains the maximum value. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_WLATCNT1

DDRC_HIS_WLATCNT1 is the Latency statistics register 1 of the write command ID specified by DDRC.

Offset Address	Register Name	Total Reset Value
0x3A4	DDRC_HIS_WLATCNT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wlatcnt_all
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RO wlatcnt_all	In the statistical period, the Latency accumulation value of the write command with the specified ID (ignore the result of the lower 4 bits). Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. When the next statistics starts, it will be cleared to zero. Note: The software can use (wlatcnt_all)/fluxid_wr_cmd to get the average latency of the write command with the specified ID.

DDRC_HIS_RLATCNT0

DDRC_HIS_RLATCNT0 is the read command latency statistics register 0 of the specified ID for DDRC.

Offset Address	Register Name	Total Reset Value
0x3A8	DDRC_HIS_RLATCNT0	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rlatcnt_max	rlatcnt_min
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access Name	Description
[31:16]	RO rlatcnt_max	DDRC The maximum latency statistics of the read command with the specified ID. The actual read maximum delay is rlatcnt_max+ inhere_rlatcnt. If overflow maintains the maximum value. When the next statistics starts, it will be cleared to zero.
[15:0]	RO rlatcnt_min	DDRC specifies the minimum latency statistics of the read command of the ID. Note: The real read minimum delay is rlatcnt_min+ inhere_rlatcnt. If overflow maintains the maximum value. When the next statistics starts, it will be cleared to zero.

DDRC_HIS_RLATCNT1

DDRC_HIS_RLATCNT1 is the read command latency statistics register 1 of the specified ID for DDRC.

Offset Address	Register Name	Total Reset Value
0x3AC	DDRC_HIS_RLATCNT1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rlatcnt_all	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RO rlatcnt_all	In the statistical period, the Latency accumulation value of the read command with the specified ID (ignore the result of the lower 4 bits). Maintained after overflow when perf_mode=1. Wrap after overflow when perf_mode=0. It will be cleared to zero when the next statistics start. Note: The software can use (rlatcnt_all/fluxid_rd_cmd+inhere_rlatcnt) to get the average latency of the read command with the specified ID.

DDRC_HIS_INHERE_RLAT_CNT

DDRC_HIS_INHERE_RLAT_CNT is the read channel intrinsic delay register.

Offset Address	Register Name	Total Reset Value
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	inhere_rlatcnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	inhere_rlatcnt	Indicates the inherent delay of DDRC and PHY on the read data channel; this register should be used in conjunction with rlatcnt_min, rlatcnt_max, rlatcnt_all, fluxid_rd_cmd to get the real latency.

DDRC_STAT_RPT

DDRC_STAT_RPT is the read pointer of the accumulation register for DMC command count.

Offset Address	Register Name	Total Reset Value
0x3B4	DDRC_STAT_RPT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	stacmd_rpt	When the statistics is in the threshold-based statistics mode, the latest 8 statistics results will be saved. This pointer is used to indicate the number of statistics results that the read result of DDRC_HIS_CMD_SUM or DDRC_HIS_DAT_SUM points to. 000: the latest statistics result; 001: the second latest statistics result; ... 111: The latest 7th statistical result.

DDRC_HIS_CMD_SUM

DDRC_HIS_CMD_SUM is the accumulation register of DMC command count.

Offset Address	Register Name	Total Reset Value
0x3B8	DDRC_HIS_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	dmc_cmd_sum	The value of the current DMC buffer command is accumulated cycle by cycle, overflow wrapping.

DDRC_HIS_DAT_SUM

DDRC_HIS_DAT_SUM is the accumulation register of DMC data count.

Offset Address	Register Name	Total Reset Value
0x3BC	DDRC_HIS_DAT_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_dat_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	dmc_dat_sum	The value of the current DMC temporary storage data is accumulated periodically and overflowed.

DDRC_HIS_SFC_RDATA0

DDRC_HIS_SFC_RDATA0 is SFC read data register 0.

Offset Address	Register Name	Total Reset Value
0x4A8	DDRC_HIS_SFC_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdate0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	rdate0	SFC read data[31:0];

DDRC_HIS_SFC_RDATA1

DDRC_HIS_SFC_RDATA1 is the SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4AC	DDRC_HIS_SFC_RDATA1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rdata1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rdata1	SFC read data[63:32].

DDRC_HIS_SFC_RDATA2

DDRC_HIS_SFC_RDATA2 is the SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B0	DDRC_HIS_SFC_RDATA2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rdata2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rdata2	SFC read data[95:64].

DDRC_HIS_SFC_RDATA3

DDRC_HIS_SFC_RDATA3 is the SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B4	DDRC_HIS_SFC_RDATA3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rdata3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rdata3	SFC read data[127:96].

4.2 Flash Memory Controller

4.2.1 Overview

FMC (Flash Memory Controller) provides a memory controller interface to connect off-chip SPI NAND Flash, SPI NOR Flash, and NAND Flash to complete data access.

4.2.2 Features

The main features of FMC are as follows:

Provide a 9KB (8192Byte+1024Byte) on-chip cache to improve reading speed. Support external 2

chip selects (SPI NAND Flash or SPI NOR Flash).

Support external 1 chip select (NAND Flash).

Support SPI NOR Flash, SPI NAND Flash, NAND Flash three types of devices. Support five SPI interface

types: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual I/O SPI, Quad I/O SPI. Supports reading data in DDR STR mode. Support various specifications of SPI

NAND Flash devices. ÿSupport 2K, 4K Page-

size devices. ÿ Devices that support 64 Pages/Block.

Support NAND Flash devices of various specifications;

ÿSupport 2K, 4K, 8K, 16K Page-size devices.

ÿDevices that support 64, 128, 256, 512 Pages/Block.

ÿ Devices that support 8-bit data interface bit width. ÿSupport legacy

asynchronous interface devices. Support the BOOT function of SPI NOR

Flash, SPI NAND Flash, and CS0 of NAND Flash;

ÿSupport 1MB Boot space. ÿIn Boot

mode, the controller automatically sends the reset command of the device before reading data (only in SPI NAND

Flash and NAND Flash mode, the reset

command is sent). ÿSupports the function of automatically skipping bad blocks (SPI NAND Flash and NAND Flash), and can skip up to 4 consecutive blocks

bad block.

ÿSupport adaptive Boot function (SPI NAND Flash and NAND Flash), the controller automatically finds the correct Correct Page-size, ECC type, Block-size configuration. ÿSupport

dual Boot images (SPI NAND Flash and NAND Flash). ÿSupport 1-wire and 4-wire Boot

for SPI NAND Flash; only support 1-wire for SPI NOR Flash Bootÿ

ÿSupports Boot of 3byte address devices and 4byte address devices for SPI NOR Flash. Support SPI

NOR Flash, SPI NAND Flash, DMA read and write functions of NAND Flash;

ÿSupport built-in DMA mode read and write operations for SPI NAND Flash and NAND Flash. Write operations are performed in units of the entire page; read operations support reading the entire page, read-only control information (read-only OOBÿÿ

ÿSupports DMA read and write operations for SPI NOR Flash, and the read and write length is configurable.

Supports manual configuration command combinations to complete various commands. (Only supports manual configuration operation in ECC0 mode).

Support ECC function (only for SPI NAND Flash and NAND Flash); ÿSupport 8bit/1KB, 16bit/

1KB, 24bit/1KB, 28bit/1KB, 40bit/1KB, 64bit/1KB BCH code ECC checksum and error correction (1KB Refers to 1KB order of magnitude, not strictly 1024Byte).

ÿSupport the enabling and disabling of ECC check code generation, and the enabling and disabling of ECC function.

ÿSupport data read and write operations in ECC0 (transparent transmission)

mode. ÿWhen reading a blank page (all data is 0xFF) is supported, the ECC uncorrectable error will not be falsely

reported. Support Randomizer function. It is only effective in the non-ECC0 mode of 8K Page-size and 16K Page-size, and it is closed inside the controller in other modes. Support 7 kinds of interrupts:

operation complete, programming operation failure, ECC check error correctable, ECC check alarm, ECC parity uncorrectable error, AHB operation error, DMA transfer error. Support low power

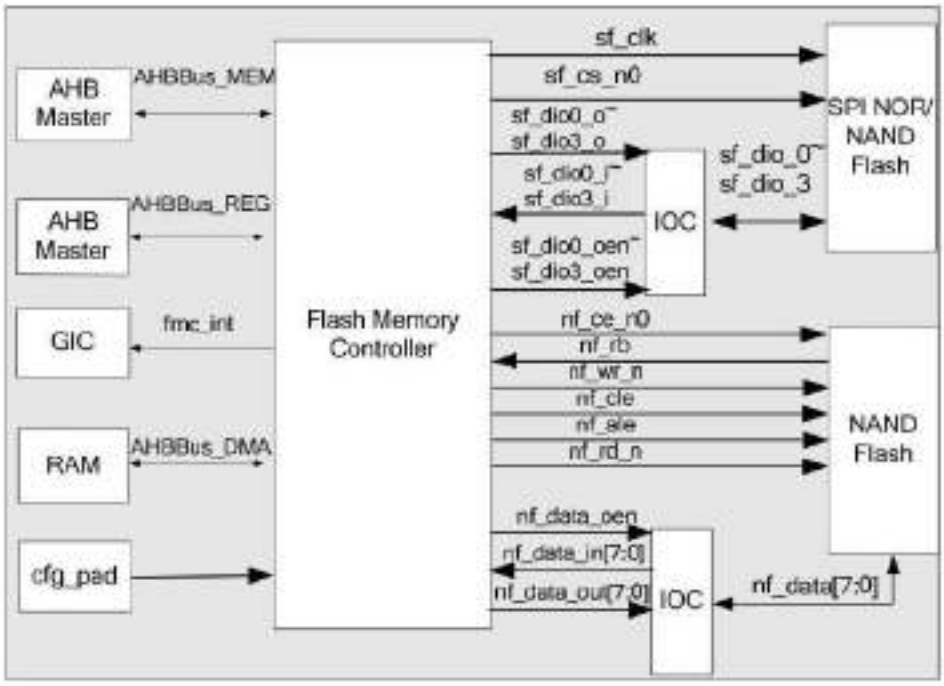
mode, you can turn off unused modules.

4.2.3 Functional description

4.2.3.1 Interface Block Diagram

FMC is used for AHB bus to interact with external Flash storage devices. Its interface block diagram is shown in Figure 4-3 .

Figure 4-3 FMC interface block diagram



In Figure 4-3 , names such as sf_clk are internal pin names of the controller, and their pin names outside the chip correspond to internal names as shown in Table 4-9. In the subsequent chapters, all the interface descriptions are the names of the controller pins.

Table 4-9 Correspondence between controller pins and chip pins

Controller pin	Chip pin name
sf_clk	NF_DQ1
sf_god_0	NF_DQ3
sf_god_1	NF_REN
sf_god_2	NF_RDY
sf_god_3	NF_DQ0
sf_cs_n0	NF_CSN
sf_cs_n1	NF_DQ7
nf_ce_n0	NF_CSN
nf_wr_b	NF_RDY
nf_wr_n	NF_WEN
nf_cle	NF_CLE
nf_but	NF_ALE
nf_rd_n	NF_REN
nf_data[0]~nf_data[7]	NF_DQ0~NF_DQ7

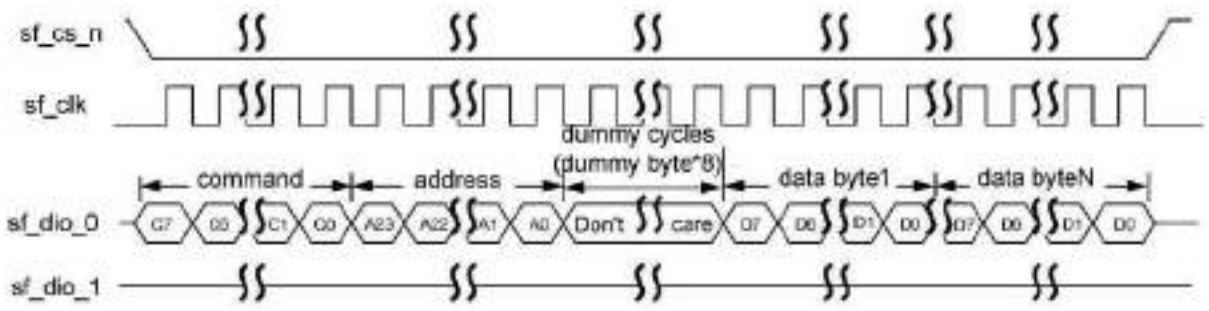
4.2.3.2 Interface description

FMC can support five SPI interface types, the five types are Standard SPI, Dual-Output/Dual Input SPI, Quad-Output/Quad-Input SPI, Dual I/O SPI, Quad I/O SPI type, Standard SPI, Dual I/O SPI, Quad I/O SPI types support SDR, DTR, DDR modes.

Standard SPI mode

Standard SPI interface mode has 1bit data input line and 1bit data output line. Figure 4-4 is the timing diagram of writing operation in Standard SPI interface mode.

Figure 4-4 Standard SPI Interface Mode Write Operation Sequence Diagram

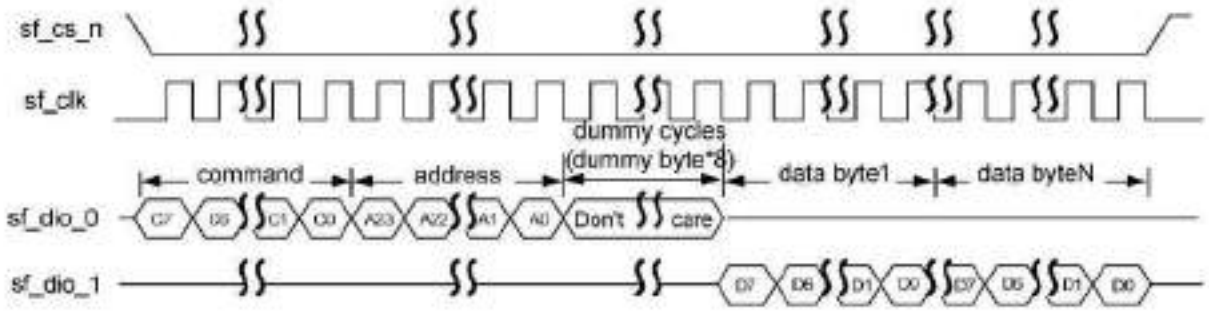


Timing description:

command/address/dummy cycles are output on the sf_dio_0 line in single-bit serial mode; Data are output on the sf_dio_0 line in single-bit serial mode.

Figure 4-5 is the timing diagram of the read operation in Standard SPI interface mode.

Figure 4-5 Standard SPI interface mode read operation timing diagram.



Timing description:

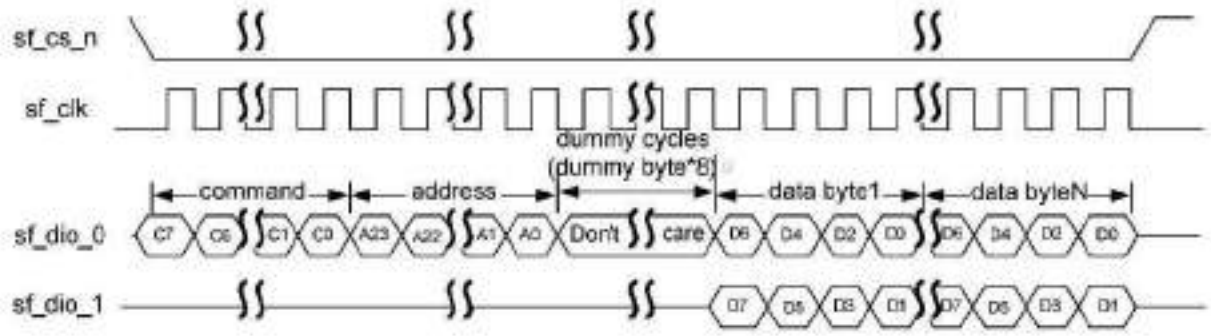
command/address/dummy cycles are output on the sf_dio_0 line in single-bit serial mode.

Data is input on the sf_dio_1 line in single-bit serial mode.

Dual-Output /Dual-Input SPI ÿÿ

The timing sequence of Dual-Output /Dual-Input SPI interface is shown in Figure 4-6 .

Figure 4-6 Dual-Output/Dual-Input SPI interface timing diagram



Timing description:

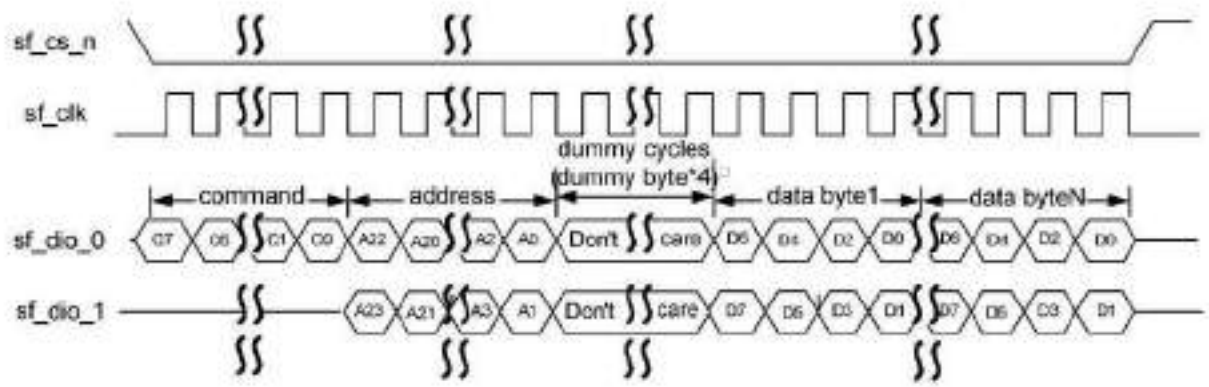
command/address/dummy cycles are output on the sf_dio_0 line in single-bit serial mode.

Data is output (write) or input (read) on the sf_dio_0/sf_dio_1 line in 2 Bits mode.

Dual I/O SPI mode

Dual I/O timing diagrams are shown in Figure 4-7 and Figure 4-8 .

Figure 4-7 Dual I/O SPI mode SDR timing diagram

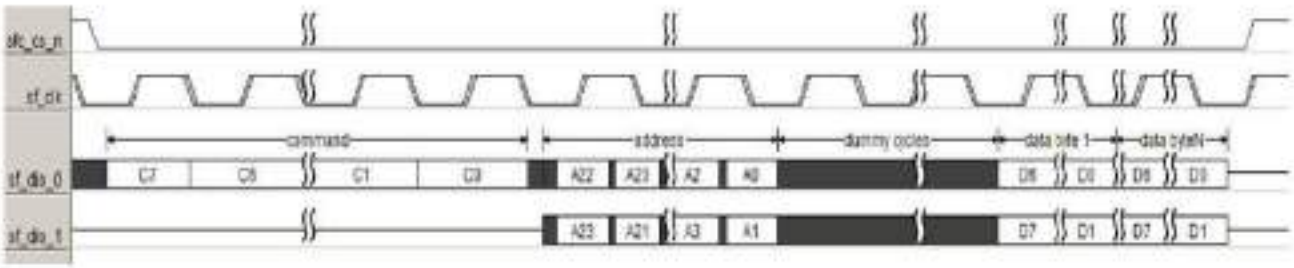


Timing description:

The command is output on the sf_dio_0 line in single-bit serial mode. The address/dummy cycles are output on the sf_dio_0/sf_dio_1 line in 2 Bits mode.

Data is output (write) or input (read) on the sf_dio_0/sf_dio_1 line in 2 Bits mode.

Figure 4-8 Dual I/O SPI mode DDR/DTR timing diagram



Timing description:

The command is output on the sf_dio_0 line in single-bit serial mode. The address/dummy cycles are output on the sf_dio_0/sf_dio_1 line in a 2 Bits double-edge effective manner.

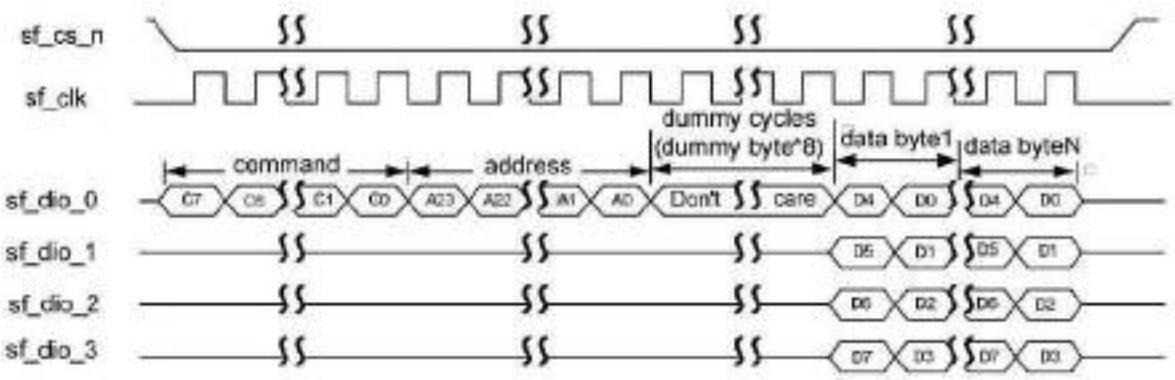
Data is input (read) on the sf_dio_0/sf_dio_1 line in 2 Bits double-edge valid mode.

DDR/DTR mode only supports reading.

Quad-Output /Quad-Input SPI

The Quad-Output / Quad-Input SPI timing diagram is shown in Figure 4-9 .

Figure 4-9 Quad-Output/Quad-Input SPI mode timing diagram



Timing description:

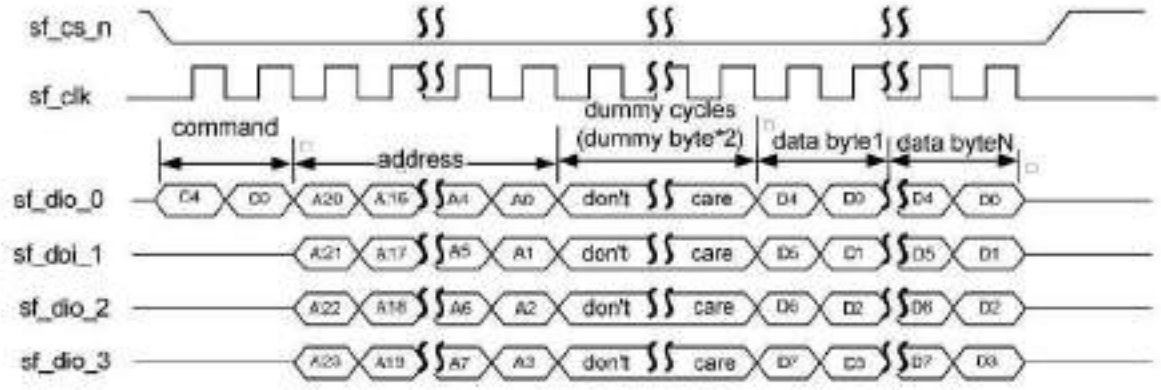
command/address/dummy cycles are output on the sf_dio_0 line in single-bit serial mode.

Data is output (write) or input (read) on the sf_dio_0/sf_dio_1/sf_dio_2/sf_dio_3 lines in the form of 4 Bits.

Quad I/O SPI mode

The timing diagram of Quad I/O SPI mode is shown in Figure 4-10 and Figure 4-11 .

Figure 4-10 Quad-I/O SPI mode interface timing diagram



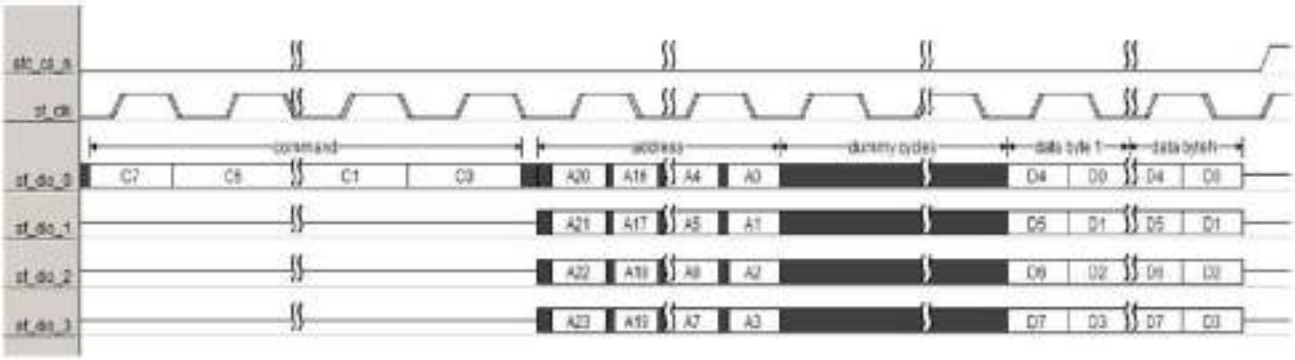
Timing description:

The command is output on the sf_dio_0 line in single-bit serial mode. Address/

dummy cycles are output on sf_dio_0/sf_dio_1/sf_dio_2/sf_dio_3 lines in 4 Bits mode.

Data is output (write) or input (read) on the sf_dio_0/sf_dio_1/sf_dio_2/sf_dio_3 lines in the form of 4 Bits.

Figure 4-11 Quad-I/O SPI mode DDR/DTR interface timing diagram



Timing description:

The command is output on the sf_dio_0 line in a single-bit single-edge data serial

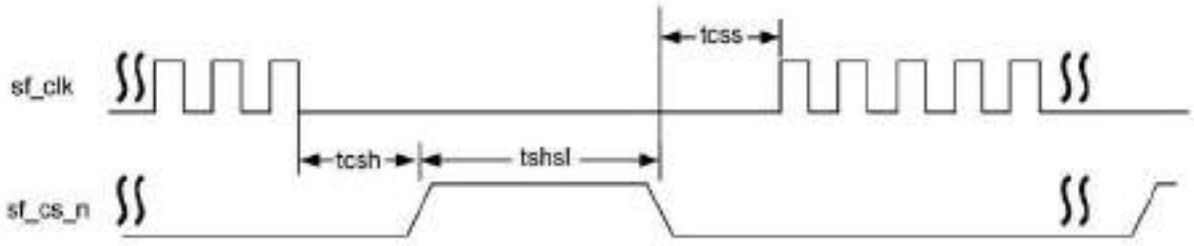
mode. The address/dummy cycles are output on the sf_dio_0/sf_dio_1/sf_dio_2/sf_dio_3 line in a 4 Bits double-edge manner.

Data is input on the sf_dio_0/sf_dio_1/sf_dio_2/sf_dio_3 line in the way of 4 Bits double edge acquisition.

4.2.3.3 SPI Interface Timing Description

The timing sequence and parameter description of the SPI interface are shown in Figure 4-12 .

Figure 4-12 SPI output timing diagram



Note: The timing configuration corresponds to the TIMING_SPI_CFG register.

tcshÿCS hold timeÿ tcssÿ

CS setup timeÿ tshslÿÿÿ

deselect timeÿ

4.2.3.4 SPI NAND FALSH Address Description

For SPI NAND Flash device address, see Table 4-10. Among them, 1st byte and 2nd byte are column addresses, 3rd byte, 4th byte and 5th byte are row addresses.

Table 4-10 FLASH address allocation table

number of bytes	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
1st byte	A0	A1	A2	A3	A4	A5	A6	A7

number of bytes Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
2nd byte A8	A9	A10 A11		A12*	A13* 0		0
3rd byte A12 A13		A14 A15		A16	A17 A18		A19
4th byte A20 A21		A22 A23		A24	A25	A26	A27
5th byte* A28* A29* 0			0	0	0	0	0

说明

A0-A11 bits are configured as effective column addresses for 2KB pagesize, and A0-A12 are configured as effective column addresses for 4KB pagesize.

A12 bits (2KB pagesize), A13 bits (4KB pagesize), for Micron devices, they are plane addresses, but for other manufacturers, there is no concept of plane addresses.

The A28 and A29 bits need to be checked according to the specific device, if not, the output is 0.

When issuing the read and write operations of SPI NAND Flash, the row and column addresses are issued according to the specific operation during the operation.

The write operation configures the column address during the LOAD operation, and configures the row address during the PROGRAM operation; the read operation configures the row address during the PAGE READ TO CACHE operation, and configures the column address during the READ operation;

Built-in DMA operation, address delivery is completed by the controller, the software needs to configure FMC_ADDRL and FMC_ADDRH according to the operation address. The FMC_ADDRL configuration value is 1st byte-4th byte, and the FMC_ADDRH configuration value is 5th byte.

说明

For 2KB pagesize configuration, the A12 bit is regarded as the plane address, which does not support A12 has other meanings and affects the read and write results device.

For 4KB pagesize configuration, the A13 bit is regarded as the plane address, and it does not support devices where A13 has other meanings and affects the read and write results.

4.2.3.5 Boot function

The FMC is in the Boot mode by default, which can support reading data directly from the FLASH to start. The CPU can directly read data in the address range from 0x00_0000 to 0x0F_FFFF, and the entire space is 1MB.

Boot function of SPI NOR Flash

Since the address space of SPI NOR Flash is continuous, 1MB of Boot data is directly mapped to the address space 0x00_0000~0x0F_FFFF of SPI NOR Flash.

SPI NAND Flash and Boot function of NAND Flash

For SPI NAND Flash and NAND Flash, due to the discontinuous address space and the possibility of bad blocks, the 1M Boot data cannot be directly mapped to Flash, and Boot also needs ECC_TYPE, PAGE_SIZE, BLOCK_SIZE information for address decoding.

FMC supports adaptive Boot function, which can automatically adapt the ECC_TYPE, PAGE_SIZE, BLOCK_SIZE information. The controller requires that physical Block0 must be a good block, and other blocks can be automatically skipped if they are bad blocks.

When FMC encounters bad blocks during Boot, it can automatically skip bad blocks to find good blocks and read Boot information. A maximum of 4 bad blocks can be skipped continuously during each bad block jumping process. If 5 physical bad blocks appear continuously during a bad block jumping process, the Boot will fail. There may be several times of skipping bad blocks in the whole Boot process. When a good block is encountered, the bad block skipping process ends. If a bad block is encountered again, a new bad block skipping process will start.

In Boot mode, SPI NAND Flash and NAND Flash support different specifications. For specific modes, refer to Table 4-11ÿ

Table 4-11 List of adaptive boot modes

ECCa(bit)	Page_sizec (KB)	Block_sizeb(Pages/Block)	SPI NAND	NAND
8	2	64(SPI NAND) 64/128/256(NAND)	support	support
	4		support	support
24	2		support	support
	4		support	support
	8	64/128/256/512(NAND)	/	support
40	8		/	support
	16		/	support
64	8		/	support
	16		/	support

a: SPI NAND Flash only supports 8bit and 24bit ECC modes during Boot.

b: SPI NAND Flash only supports Block_size of 64 during Boot.

c: During Boot, the Randomizer function is enabled for both 8K and 16K configurations.

Dual mirror function

For SPI NAND Flash and NAND Flash, if an uncorrectable error is encountered during Boot, the controller will automatically trigger the dual mirror function: jump to the same Page of the next backup mirror to read Boot data.

注意

The dual-mirror function requires mirror 0 and mirror 1 to be stored in two consecutive good blocks (there can be no more than 4 bad blocks between these two good blocks).

4.2.3.6 Register mode operation

The software configures operation-related registers, such as operation commands, addresses, etc., and finally configures the FMC_OP register to issue operations, and the controller issues operations to the device according to the software configuration values. If data needs to be transferred to the device, the internal buffer will be used to transfer the data.

Read id, set feature, erase and other operations are issued in this way.

The register operation mode can combine all device operations, and can issue instructions, addresses, transfer data, etc. separately.

4.2.3.7 Built-in DMA operation mode

FMC supports read and write operations using built-in DMA mode to increase access speed. In this way, FMC can directly access DDR through the bus.

DMA write operation: SPI NOR Flash supports transferring data of any length from any address of DDR to any address of the device. For SPI NAND Flash and NAND Flash, only page-based write operations are supported.

DMA read operation: Same as write operation, SPI NOR Flash supports any address of the slave device to transfer data of any length to any address of DDR. For SPI NAND Flash and NAND Flash, it supports whole page read and read-only OOB operations. Read-only OOB operation:

When the software only needs software management information (such as bad block marks, empty block marks, etc.), it does not need to read the data of the entire page, but only needs to read the control information part, using the read-only OOB method Complete this purpose.

4.2.3.8 ECC verification function

For SPI NAND Flash, FMC supports ECC check error correction function. There are four kinds of maximum error correction capabilities supported: 8bit /1KB, 16bit /1KB, 24bit /1KB and 28bit /1KB. Taking 8bit ECC as an example, it means that 1KB (about) data can correct up to 8bit errors.

For NAND Flash, FMC supports six error correction modes: 8bit/1KB, 16bit/1KB, 24bit/1KB, 28bit/1KB, 40bit/1KB, 64bit/1KB. Among them, different error correction modes support different PAGE_SIZE, please refer to the data structure for details.

ECC protection data plus OOB information plus ECC code, the error correction algorithm is calculated according to the error correction unit (1KB). It can be considered that DATA+OOB is the data for calculating ECC. For 2KB pagesize, the data of each error correction unit is (DATA+OOB)/2, and for 4KB it is (DATA+OOB)/4.

OOB is the part of software management information, see the data structure description for details.

DATA is real data, 2KB PAGE_SIZE is 2048Byte, 4KB PAGE_SIZE is 4096Byteÿ

When BOOT starts, SPI NAND Flash only supports 8bit and 24bit ECC, and the corresponding device requirements are 4bit/512B and 8bit/512B (512byte is the error correction unit described in the device manual). In NORMAL mode, it also supports 16bit ECC and 28bit ECC. If the spare area of the device is enough to store the check code, the 16bit/1KB ECC mode can be used for the device required by 4bit/512B to improve reliability. For NAND Flash, it supports 8bit/1KB, 24bit/1KB, 40bit/1KB, 64bit/1KB in Boot, and supports 16bit/1KB, 28bit/1KB in NORMAL mode.

When the maximum error correction capability is exceeded, an uncorrectable error interrupt can be reported. FMC provides an alarm interrupt, when the number of error bits in an error correction process is equal to or greater than the configured error threshold (FMC_ERR_THD[fmc_err_thd]), an error will be reported

False alarm, prompting the software that the number of error digits in this operation has reached the preset value. If one or more error correction units have error bits, and the number of error bits of all error correction units does not reach the error threshold and uncorrectable value, the error correctable interrupt flag FMC_INT[err_val_int] will become 1.

When reading a page data, if there is an uncorrectable error in one of the error correction units, the uncorrectable interrupt status will be reported; otherwise, if there is an error alarm error correction unit, the error correction alarm status will be reported; if If there is error correction, but the number of error correction bits does not reach the error threshold, the error correctable interrupt status can be reported.

When working in SPI NOR Flash mode, the ECC check function is not enabled. When FMC_CFG[ecc_type] is set to zero, the SPI NAND Flash works in the mode without ECC check function, and the controller transfers the data directly without processing the data structure, and directly transfers the flash data.

4.2.3.9 Randomizer check function

For large-capacity MLC NAND devices, in order to improve the stability of data storage, FMC provides the Randomizer function to randomize data.

After the Randomizer function is enabled, the controller will perform Randomizer processing on the data written into the Flash during the write operation, and then write it into the Flash; during the read operation, the controller will first perform De Randomizer processing on the data read back from the Restore and then write to Buffer.

注意

In ECC0 mode or SPI NOR mode, regardless of the value of GLOBAL_CFG[randomizer_en], the Randomizer function will be disabled inside the FMC.

Under the 2K/4K Page-size configuration, the Randomizer function will also be turned off internally.

After the Randomizer is turned on, reading the data in the block just erased will cause uncorrectable errors, because all the data in the Page is 0xFF, and after the De-Randomizer is performed, the data will be uncorrectable.

4.2.3.10 TIMEOUT function

FMC provides a TIMEOUT mechanism for DMA write operations. While waiting for the DMA write operation to end, the controller will continuously send GET FEATURE operations to check whether the write operation is over; for SPI NOR Flash, the controller will wait for the device to send RDSR operations to query Whether the operation is over; for NAND Flash, the controller waits for RB to be pulled high. If the waiting time of FMC exceeds the configuration value of register FMC_TIMEOUT_WR[timeout_wr], it will end the DMA write operation and report FMC_INT[op_fail] interrupt.

For NAND Flash, in the DMA write operation, even if RB is pulled high before the TIMEOUT time, the controller will automatically send a read status register operation, and store the read value in FM_STATUS[fm_status], if its bit0 is 1, It means that the DMA write operation failed, and the controller will also report FMC_INT[op_fail] interrupt.

4.2.4 Workflow

4.2.4.1 Initialization process

The initialization process is as follows:

Step 1. (If you need to adjust Timing parameters) According to the device configuration register TIMING_SPI_CFG (SPI NAND Flash or SPI NOR Flash), register PND_PWIDTH_CFG (NAND Flash).

Step 2. According to the interfaced FLASH device manual, configure the FMC configuration register (FMC_CFG). The main configuration has File interface type, ecc_type, pagesize, etc.

Step 3. For SPI NOR Flash, if the device is a 4byte address device and the default is 3byte address mode, refer to 4.2.4.4 SPI NOR Flash address mode switching process to complete the 4byte address mode switching.

Step 4. After the initialization is completed, the operation can be issued according to the specific operation configuration register.

----Finish

4.2.4.2 FMC_OP operation flow (register operation mode)

Register operations on the device (such as reading ID or configuring device registers) are completed by configuring the FMC_OP delivery operation. The operation steps are as follows:

Step 1. Configure ecc_type of FMC_CFG as 0.

Step 2. If it is a register write operation (such as configuring the FLASH configuration register), first write the desired operation data from the Buffer access start address.

Step 3. According to the device operation needs, configure the operation command FMC_CMD, device operation address FMC_ADDRL, read and write data Data number FMC_DATA_NUM and other operation registers.

Step 4. According to the issued device operation, match the FMC_OP configuration FMC_OP_CFG register.

Step 5. Configure the delivery operation of the FMC_OP register. For specific configuration values, refer to the description of the FMC_OP register.

Step 6. If you use the query method, check that the FMC_OP [0] bit is 1, which means the operation is completed; if you use the interrupt method, check to FMC_INT [op_done_init], indicating that the operation is complete.

Step 7. For the read register operation (such as read ID operation), the read register is stored in the buffer after step 6 is completed, Software can read device register values from it.

----Finish

4.2.4.3 Read device status register operation

If you want to read the status register of the device, there is an easy way to do it. details as follows:

Step 1. Configure FMC_OP register delivery operation (configure FMC_OP [read_status_en] and FMC_OP [reg_op_start] is 1).

Step 2. The read status register is stored in the FMC_FLASH_INFO register.

----Finish

4.2.4.4 SPI NOR Flash address mode switching process

For SPI NOR Flash devices, it supports 3Bytes and 4Bytes Flash address modes. The initial default address mode can be selected by pulling the pin up and down, or the address mode can be dynamically switched through the configuration register after the chip starts up.

If the default is 3byte mode startup, but the device is a 4byte address mode device, switch after the chip starts up
The steps of flash address mode are as follows:

Step 1. No flash operation or ensure that the previous flash operation is completed.

Step 2. According to the requirements of the device, use the register operation mode to configure the relevant registers of the device and send specific commands to configure Flash to enter 4B mode.

Step 3. Configure the FMC_CFG[spi_nor_addr_mode] of the FMC as 4B mode, complete the 3byte mode to 4byte mode mode switching.

----Finish

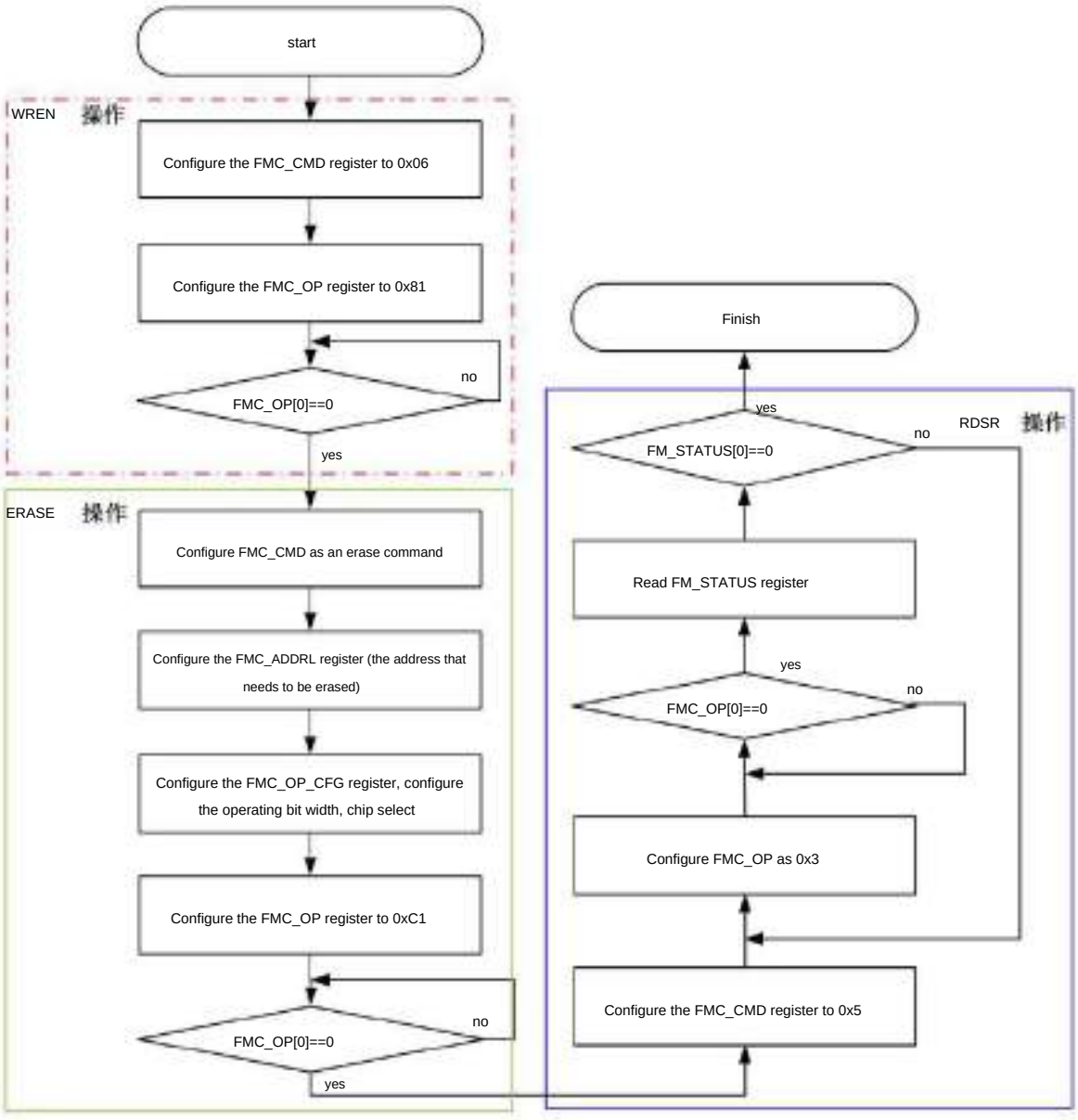
说明

For specific SPI NOR Flash address mode switching commands, please find the relevant device manual.

4.2.4.5 Erase operation process (SPI NAND Flash and SPI NOR Flash)

For flash operation, erase must be performed before programming operation, and WREN operation must be completed before erasing operation. The erase operation reference flow (query method) is shown in Figure 4-13.

Figure 4-13 Erase operation flow chart



说明

The above figure is the query mode. If the interrupt mode is used, the query FMC_OP[0] operation becomes an interrupt processing mode, and FMC_INT[op_done_init] is detected, indicating that the operation is completed.

During the ERASE operation, the configured erase command and operating address need to be configured according to the specific device manual.

4.2.4.6 FMC_OP Erase (NAND Flash)

In NAND Flash mode, the operation process of erasing CS0 in NFC_OP mode is as follows:

Step 1. Configure the register FMC_CFG [op_mode] as 1 to ensure that the controller is in NORMAL mode.

Step 2. Write the configuration register FMC_ADDRL to erase the Block address, and write the erase command 0xD060 to the register FMC_CMD.

Step 3. Write 0x30 into the configuration register FMC_OP_CFG, and configure it as CS0, indicating that the 3Byte address needs to be sent.

Step 4. Write 0xDB into the configuration register FMC_OP to start the erase operation of CS0 (additional automatic read status register operation do).

Step 5. In query mode, check FMC_OP[reg_op_start], if it is 0, it means the operation is over; if using interrupt mode, check FMC_INT[op_done_int], if it is 1, it means the operation is over. Otherwise, loop in this step.

Step 6. Read the status value of FM_STATUS[fm_status] to judge whether the erasing is successful.

----Finish

4.2.4.7 Built-in DMA read operation process (FMC_OP_CTRL read operation)

The operation process of using the built-in DMA method to read data is as follows:

Step 1. Configure the register FMC_CFG [op_mode] as 1 to ensure that the controller is in NORMAL mode.

Step 2. Configure FMC_ADDRL and FMC_ADDRH to configure the device operating address. For SPI NOR Flash, only FMC_ADDRL needs to be configured.

注意

For SPI NOR Flash, the number of address cycles during DMA operation is determined by FMC_CFG[spi_nor_addr_mode]: 3Byte address mode and 4Byte address mode selection are supported. For SPI NAND Flash and NAND Flash, the controller defaults to 5Byte address mode, which is not configurable.

Step 3. Configure the FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB registers, and configure the starting address for storing data in DDR.

For SPI NOR FLASH, it is not necessary to configure the FMC_DMA_SADDR_OOB register; for the read-only OOB operation of SPI Nand Flash and NAND Flash, only need to configure FMC_DMA_SADDR_OOB register.

注意

For SPI NAND Flash and NAND Flash, 4byte address alignment is required when configuring DDR address.

For SPI NAND Flash and ECC0 mode of NAND Flash, FMC_DMA_LEN needs 4byte align.

Step 4. Configure the FMC_DMA_LEN register. In SPI NOR Flash mode, you need to configure FMC_DMA_LEN as the length of the read data; in SPI NAND Flash and NAND Flash ECC0 mode, you need to configure the spare area data length; other operations do not need to configure this register.

Step 5. Configure the FMC_OP_CFG register, and configure according to the issued read operation requirements.

For SPI NAND Flash and SPI NOR Flash, configure FMC_OP_CFG [dummy_num] and FMC_OP_CFG [mem_if_type] according to the number of dummy cycles in the device read operation sequence and the type of SPI interface . Configure FMC_OP_CFG [fm_cs],

select operation chip select.

Step 6. Configure the FMC_OP_CTRL register, set FMC_OP_CTRL [0] to 1, and issue the FMC read FLASH operation do.

Configure FMC_OP_CTRL [rw_op] to be zero, which means DMA read operation. For

SPI NAND Flash and read-only OOB operation of NAND Flash, FMC_OP_CTRL [rd_op_sel] needs to be configured. For SPI NAND Flash and

SPI NOR Flash, you need to configure FMC_OP_CTRL [rd_opcode], and configure it according to the device READ operation command.

Step 7. Use the query method to detect that FMC_OP_CTRL [0] has become low, indicating that the read operation has been completed and the data has been written into the DDR; use the interrupt method to detect that FMC_INT [op_done_int] has become high, indicating that the read operation has been completed and the data has been written. Write to DDR.

----Finish

4.2.4.8 Built-in DMA write operation process (FMC_OP_CTRL read operation)

Use the built-in DMA method to write FLASH, the process is as follows:

Step 1. Configure the register FMC_CFG [op_mode] as 1 to ensure that the controller is in NORMAL mode.

Step 2. Configure FMC_ADDRL and FMC_ADDRH to configure the device operating address. For SPI NOR FLASH, only FMC_ADDRL needs to be configured.

For SPI NOR Flash, the number of address cycles during DMA operation is determined by FMC_CFG[spi_nor_addr_mode]: 3Byte address mode and 4Byte address mode selection are supported. For SPI NAND Flash and NAND Flash, the controller defaults to 5Byte address mode, which is not configurable.

Step 3. Configure the FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB registers to configure the starting address for transferring data from DDR. For SPI NOR Flash, it is not necessary to configure the FMC_DMA_SADDR_OOB register.

注意

For SPI NAND Flash and NAND Flash, 4byte address alignment is required when configuring DDR address.

For SPI NAND Flash and ECC0 mode of NAND Flash, FMC_DMA_LEN needs 4byte alignment.

Step 4. Configure the FMC_DMA_LEN register. In SPI NOR Flash mode, you need to configure FMC_DMA_LEN as the length of the read data; in SPI NAND Flash and NAND Flash ECC0 mode, you need to configure the spare area data length; other operations do not need to configure this register.

Step 5. Configure the FMC_OP_CFG register and configure it according to the issued write operation requirements

For SPI NAND Flash and SPI NOR Flash, select and configure according to the required write operation SPI interface FMC_OP_CFG [mem_if_type]ÿ

FMC_OP_CFG [fm_cs], select operation chip select.

Step 6. Configure the FMC_OP_CTRL register delivery operation,

Configure the rw_op information as write (configure as 1), which means DMA write

operation. For SPI NAND Flash and SPI NOR Flash, you need to configure FMC_OP_CTRL [wr_opcode], and configure it according to the device PROGRAM operation instruction.

Step 7. Use the query method to detect that FMC_OP_CTRL [0] has become low, indicating that a DMA write operation has been completed and the data has been written into FLASH; use the interrupt method to detect that FMC_INT [op_done_int] has become high, indicating that the data has been written to FLASH middle.

----Finish

4.2.4.9 Other Notes

Other precautions are as follows:

For SPI NAND Flash and NAND Flash devices, the Reset operation of the device must be performed before use or after abnormal reset. When

FMC_OP_CTRL[dma_op_ready] or FMC_OP[reg_op_start] is 1 (the controller is in operation), do not configure the relevant operation registers, otherwise it may cause abnormal operation. The software configuration needs to be carried out

under the principle of correctness and rationality, otherwise the random configuration of the registers may cause the FMC to hang up. For example, NAND Flash does not support dummy_en. In the FMC_OP operation of NAND Flash, if this enable is configured and FMC_OP_CFG[dmmy_num] is not 0, the controller will hang.

4.2.5 Data structure (NAND Flash/SPI NAND Flash)

The data structure of FMC is divided into two types, one is user's original data, and the other is the data structure stored in NAND Flash after conversion by FMC in non-ECC0 mode. In non-ECC0 mode, both the original user data and the data transformed by FMC have a fixed data structure, and the length and position of each data member are strictly fixed. In ECC0 mode, the user data is written/read intact, and the FMC does not make any changes to the user data.

For ECC0 mode, FMC performs transparent transmission processing on data: when writing, the controller directly writes the data in the Buffer to Flash without processing; during reading, the controller directly writes the data read from Flash to the Buffer.

In non-ECC0 mode, when writing to Flash, FMC processes user data twice: generate ECC code and reassemble. The controller performs ECC encoding in the internal Buffer and generates ECC codes, and then reassembles the data in the Buffer before writing it into Flash. When performing a read operation on Flash, FMC also needs to perform two processes: reorganizing Flash data and ECC error correction. FMC reassembles the data read from Flash and writes it into the internal Buffer, and then performs ECC error correction on the data in the Buffer.

In non-ECC0 mode, the data in Buffer and the data in Flash are divided into different structures. For different configurations, refer to Table 4-12 for the length of each data segment.

Table 4-12 Non-ECC0 mode data structure length

ECCa(bit)	ecc_lenb(byte)	Page_size(byte)	oob_lenc(byte)	sec_lend(byte)
4/512B (8/1K)	14	2048	30+2	1040
		4096		1032
8/512B (16/1K)	28	2048	6+2	1028
		4096	14+2	
24/1K	42	2048	30+2	1040
		4096		1032
		8192		1028
40/1K	70	8192	30+2	1028
		16384		1026
64/1 Que	112	8192	30+2	1028
		16384		1026

a: 4bit/512B is equivalent to 8bit/1K, and 8bit/512B is equivalent to 16bit/1K.

b: ecc_len indicates the length of the ECC code generated by each error correction unit.

c: oob_len indicates the length of the redundant area visible to the upper layer software, composed of CTRL+BB.

d: sec_len indicates the data area length of each error correction unit, sec_len=1024+(oob_len*1024)/Page_size

e: Each error correction unit of ECC is 1K, here 1K is not strictly 1024byte, but refers to the length of 1K. For example, the error correction unit length sec_len in the table varies from 1026 to 1040, collectively referred to as 1K.

The following describes the composition of each data segment in combination with the process of the write operation.

When FMC writes data into Flash, it will be stored alternately and continuously in the format of DATA+ECC, but the data in the OOB area needs special processing:

The BB logo needs to be placed in the page_size of the Flash page, that is, for configurations of 2K, 4K, 8K, and 16K, the BB data will be placed in two bytes beginning with 2048, 4096, 8192, and 16384 Byte. This will break the original DATA or ECC data.

The CTRL data needs to be placed at the end of the valid data, so the storage form of the last data segment in Flash is: DATA (excluding BB and CTRL)+ECC+CTRL.

EB is used as a mark bit to mark an empty block, and is fixedly placed in the last 2Byte of CTRL.

4.2.5.2 4bit ECC mode (error correction 8bit/1KB)

2KB Page-size

For the configuration of 2KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-14 .

Figure 4-14 Data structure of 2K Page-size in 4bit ECC mode

4KB Page-size

For the configuration of 4KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-15 .

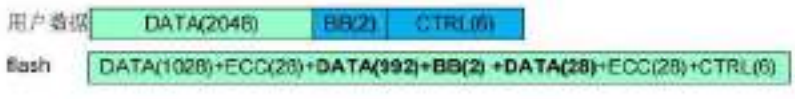
Figure 4-15 Data structure of 4K Page-size in 4bit ECC mode

4.2.5.3 8bit ECC mode (error correction 16bit/1KB)

2KB Page-size

For the configuration of 2KB Page-size, the redundant area available to the software is 8 bytes. The structure of data in Buffer and Flash is shown in Figure 4-16 .

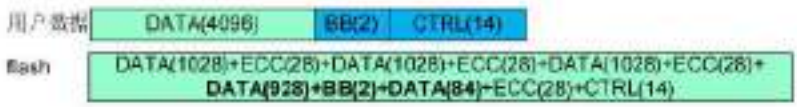
Figure 4-16 Data structure of 2K Page-size in 8bit ECC mode



4KB Page-size

For the configuration of 4KB Page-size, the size of redundant area available to the software is 16byte. The structure of data in Buffer and Flash is shown in Figure 4-17 .

Figure 4-17 Data structure of 4K Page-size in 8bit ECC mode

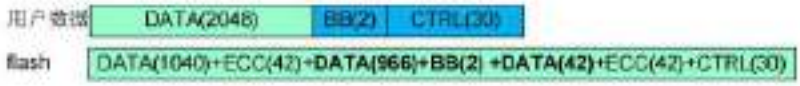


4.2.5.4 24bit ECC mode (error correction 24bit/1KB)

2KB Page-size

For the configuration of 2KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-18 .

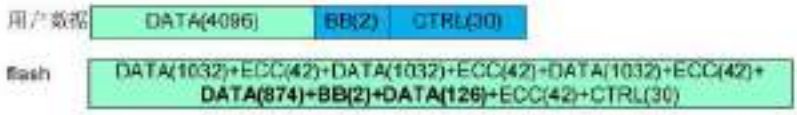
Figure 4-18 Data structure of 2K Page-size in 24bit ECC mode



4KB Page-size

For the configuration of 4KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-19 .

Figure 4-19 Data structure of 4K Page-size in 24bit ECC mode



8KB Page-size

For the configuration of 8KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-20 .

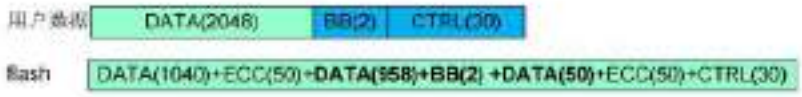
Figure 4-20 Data structure of 8K Page-size in 24bit ECC mode

4.2.5.5 28bit ECC mode (error correction 28bit/1KB)

2KB Page-size

For the configuration of 2KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-21 .

Figure 4-21 Data structure of 2K Page-size in 28bit ECC mode



4KB Page-size

For the configuration of 4KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-22 .

Figure 4-22 Data structure of 4K Page-size in 28bit ECC mode

8KB Page-size

For the configuration of 8KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-23 .

Figure 4-23 Data structure of 8K Page-size in 28bit ECC mode

4.2.5.6 40bit ECC mode (error correction 40bit/1KB)

8KB Page-size

For the configuration of 8KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-24 .

Figure 4-24 Data structure of 8K Page-size in 40bit ECC mode

16KB Page-size

For the configuration of 16KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-25 .

Figure 4-25 Data structure of 16K Page-size in 40bit ECC mode

4.2.5.7 64bit ECC mode (error correction 40bit/1KB)

8KB Page-size

For the configuration of 8KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-26 .

Figure 4-26 Data structure of 8K Page-size in 64bit ECC mode

16KB Page-size

For the configuration of 16KB Page-size, the size of redundant area available to the software is 32byte. The structure of data in Buffer and Flash is shown in Figure 4-27 .

Figure 4-27 Data structure of 16K Page-size in 64bit ECC mode

4.2.6 ECC Mode Selection Instructions

Because the "ECC error correction IP" used by the controller processes data "based on 1KB data block", so when describing the ECC error correction performance of the controller, it is written as follows: 8bit/1KByte, 24bit/1KByte, etc. . In order to use the device reliably, the device datasheet often gives the recommended ECC error correction performance, such as 1bit/512Byte, 4bit/512Byte, 8bit/512Byte, etc. The error correction performance described by 8bit/1KByte and 4bit/512Byte is actually the same. When using the controller, the ECC mode selection should follow the following 2 guidelines:

ECC error correction performance of the controller >= device recommended ECC error correction performance

For example, if the device recommends 1bit/512Byte or 4bit/512Byte, then the controller can choose the ECC mode of 8bit/1Kbyte error correction performance. Page

size of device >= memory size required for controller ECC mode

For example, if the page size of the device is 2K+64Byte, then the controller cannot select the ECC mode with 24bit/1Kbyte error correction performance, because the storage size required by this ECC mode is 2K+116Byte, and the storage size required by the ECC mode is please Refer to the chapter "4.2.5 Data Storage Structure".

4.2.7 FMC register overview

An overview of the FMC registers is shown in Table 4-13 .

Table 4-13 FMC register overview (base address is 0x1000_0000)

offset address name	describe	page number
0x0000 FMC_CFG	Device Configuration Register	4-154
0x0004 GLOBAL_CFG Global configuration register		4-156
0x0008 TIMING_SPI_CFG SPI Timing Configuration Register		4-158
0x000C PND_PWIDTH_CFG Read and write pulse width configuration register		4-158
0x0010 PND_OPIDLE_CFG Operation Interval Configuration Register		4-159
0x0018 FMC_INT	Interrupt Status Register	4-159
0x001C FMC_INT_EN	interrupt enable register	4-161
0x0020 FMC_INT_CLR interrupt clear register		4-163
0x0024 FMC_CMD	Command Word Configuration Register	4-164
0x0028 FMC_ADDRH device address configuration register high byte		4-164

offset address name	describe	page number
0x002C FMC_ADDRL	Device address configuration register low 4byte	4-165
0x0030 FMC_OP_CFG operation configuration register		4-165
0x0034 SPI_OP_ADDR Operation Address Configuration Register		4-166
0x0038 FMC_DATA_NUM data length register		4-167
0x003C FMC_OP	operation register	4-167
0x0040 FMC_DMA_LEN DMA operation length register		4-169
0x0048 FMC_DMA_AHB_CTRL	DMA AHB Bus Control Register	4-169
0x004C FMC_DMA_SADDR_D0	DMA operation DDR start address register 0	4-170
0x0050 FMC_DMA_SADDR_D1	DMA operation DDR start address register 1	4-171
0x0054 FMC_DMA_SADDR_D2	DMA operation DDR start address register 2	4-171
0x0058 FMC_DMA_SADDR_D3	DMA operation DDR start address register 3	4-171
0x005C FMC_DMA_SADDR_OOB	DMA operation DDR stores OOB information start address register	4-172
0x0068 FMC_OP_CTRL operation control register		4-172
0x006C FMC_TIMEOUT_WR	Write operation TIMEOUT time register	4-173
0x0070 FMC_OP_PARA	OP Operation parameter selection register	4-174
0x0074 FMC_BOOT_SET boot setting register		4-175
0x0078 FMC_LP_CTRL Low Power Control Register		4-175
0x007C FMC_LOCK	Lock Address Configuration Register	4-176
0x0080 FMC_LOCK_SA0 Lock start address 0 configuration register		4-177
0x0084 FMC_LOCK_EA0 Lock end address 0 configuration register		4-177
0x0088 FMC_LOCK_SA1 Lock start address 1 configuration register		4-178
0x008C FMC_LOCK_EA1 Lock end address 1 configuration register		4-178
0x0090 FMC_LOCK_SA2 Lock start address 2 configuration register		4-178
0x0094 FMC_LOCK_EA2 Lock end address 2 configuration register		4-179
0x0098 FMC_LOCK_SA3 Lock start address 3 configuration register		4-179

offset address name	describe	page number
0x009C FMC_LOCK_EA3 Lock end address 3 configuration register		4-180
0x00A0 FMC_EXPCMD Extended page command register		4-180
0x00A4 FMC_EXBCMD extended block command register		4-180
0x00A8 FMC_ERR_THD	ECC Warning Threshold Register	4-181
0x00AC FMC_FLASH_INFO device status register value		4-181
0x00B8 FMC_OP_CNT The number of operations sent by the controller register		4-182
0x00BC FMC_VERSION version register		4-182
0x00C0 FMC_ERR_NUM0_ BUF0	SPI NAND FLASH and NAND FLASH first buffer error correction information 0 statistics register	4-183
0x00C4 FMC_ERR_NUM1_ BUF0	NAND FLASH first buffer error correction information 1 statistics register	4-183
0x00C8 FMC_ERR_NUM0_ BUF1	NAND FLASH second buffer error correction statistics register 0	4-184
0x00CC FMC_ERR_NUM1_ BUF1	NAND FLASH second BUFFER error correction statistics register 1	4-184
0x00D0 FMC_ERR_ALARM _ADDRH	ECC alarm flash address high byte register 4-185	
0x00D4 FMC_ERR_ALARM _ADDRL	ECC alarm flash address low byte register 4-185	
0x00D8 FMC_ECC_INVALI D_ADDRH	ECC uncorrectable address high byte register	4-186
0x00DC FMC_ECC_INVALI D_ADDRL	ECC uncorrectable address low 4byte register 4-186	
0x0E0	FMC_READ_TIMIN G_TUNE	Asynchronous NAND read sampling point adjustment register	4-187
0x100	FMC_EXP_OP_CTR L	Extended Operation Control Register	4-187
0x104	FMC_EXP_ADDRH extended operation device address configuration register high byte		4-188
0x108	FMC_EXP_ADDRL extended operation device address configuration register lower 4byte		4-189
0x10C	FMC_EXP_DMA_S ADDR_D0	Extended DMA operation DDR start address register 0 4-189	
0x110	FMC_EXP_DMA_S ADDR_D1	Extended DMA operation DDR start address register 1 4-190	
0x114	FMC_EXP_DMA_S ADDR_D2	Extended DMA operation DDR start address register 2 4-190	

offset address	name	describe	page number
0x118	FMC_EXP_DMA_S ADDR_D3	Extended DMA operation DDR start address register 3	4-190
0x11C	FMC_EXP_DMA_S ADDR_OOB	Extended DMA operation DDR storage OOB information start address register	4-191
0x120	FMC_EXP_INT	Extended operation interrupt status register	4-191
0x124	FMC_EXP_INT_EN	extended operation interrupt enable register	4-193
0x128	FMC_EXP_INT_CL R	Extended operation interrupt clear register	4-195
0x12C	FMC_EXP_ERR_NO M0_BUF0	Extended operation first buffer error correction information 0 statistics register	4-195
0x130	FMC_EXP_ERR_NO M1_BUF0	Extended operation first buffer error correction information 1 statistics register	4-196
0x13C	FMC_EXP_ERR_NO M0_BUF1	Extended operation second buffer error correction statistics register 0	4-196
0x140	FMC_EXP_ERR_NO M1_BUF1	Extended operation second buffer error correction statistics register 1	4-197

4.2.8 FMC register description

FMC_CFG

FMC_CFG is the device configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	FMC_CFG	0x0000_1820

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.

[12:11] RW	spi_nand_sel		Select the spi nand device manufacturer. (Only valid for SPI NAND using device internal ECC) 01ÿwinbondÿ 10: esmtÿ 11ÿmicronÿ Other: other devices.
RW	spi_nor_addr_mode	1: 4Bytes address mode. The reset value is determined by the pin SFC_EMMC_BOOT_MODE.	SPI address mode (only valid for SPI NOR) 0: 3Bytes address mode (default); [10]
[9:8] RW	block_size		Block size of NAND Flash. 00ÿ64 pageÿ 01ÿ128pageÿ 10ÿ256 pageÿ 11ÿ512 pageÿ
[7:5] RW	ecc_type		Configure the ecc type of the controller. 000: no ECC; 001ÿ8bit ECCÿ 010ÿ16bit ECCÿ 011ÿ24bit ECCÿ 100ÿ28bit ECCÿ 101ÿ40bit ECCÿ 110ÿ64bit ECCÿ 111: Reserved.
[4:3] RW	page_size		Page size of SPI NAND/NAND Flash. 00ÿ2KB pagesizeÿ 01ÿ4KB pagesizeÿ 10ÿ8KB pagesizeÿ 11ÿ16KB pagesizeÿ
[2:1] RW	flash_sel		Flash type selection. 00ÿSPI NOR FLASHÿ 01ÿSPI NAND FLASHÿ 10ÿNAND FLASHÿ 11: Reserved. The reset value is determined by the pin BOOT_SEL0/ BOOT_SEL1/ SFC_DEVICE_MOD.

[0] RW op_mode			FMC operation mode selection. 0: boot mode; 1: normal mode.

GLOBAL_CFG

GLOBAL_CFG is the global configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	GLOBAL_CFG	0x0000_00C4

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved sample_point

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 0 0

Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15:12] RW	sample_point		In DDR mode, the sampling point is selected according to different delay parameters of different devices. The sampling clock frequency is 4 times the interface read and write clock. 0x0 is the minimum delay, 0xB is the maximum delay. 0x0: The sampling point is 2 sampling clock cycles after the valid edge. 0x1: The sampling point is 2.5 sampling clock cycles after the valid edge. 0x2: The sampling point is 3 sampling clock periods after the valid edge. 0x3: The sampling point is 3.5 sampling clock cycles after the valid edge. 0x4: The sampling point is 4 sampling clock cycles after the valid edge. 0x5: The sampling point is 4.5 sampling clock cycles after the valid edge. 0x6: The sampling point is 5 sampling clock cycles after the valid edge. 0x7: The sampling point is 5.5 sampling clock cycles after the valid edge. 0x8: The sampling point is 6 sampling clock periods after the valid edge. 0x9: The sampling point is 6.5 sampling clock cycles after the valid edge. 0xA: The sampling point is 7 sampling clock periods after the valid edge. 0xB: The sampling point is 7.5 sampling clock periods after the valid edge. Other: reserved.

[11] RW ddr_mode			DDR mode enable control. 0: normal SDR mode; 1: DDR mode.
[10] RO		reserved	reserve.
[9] RW edo_mode			Whether to use EDO mode for NAND device read data operation, if the device switches to EDO mode, the controller needs to be configured as EDO mode. 0: non-EDO mode; 1: EDO mode.
[8] RW rb_sel			It is valid when multiple NAND Flash devices (multiple chip selects) are connected externally. 0: NAND Flash devices share the same ready/busy signal; 1: NAND Flash devices use independent ready/busy signals. When only one NAND Flash device is connected, only chip select signals ce0 and ready_busy0 are used.
[7] RW cs_ctrl			Chip select control. 0: Always keep CS valid; 1: When the RB signal is pulled low and the device is working, cs is pulled high. (The spi interface has no rb signal, which is invalid for the spi interface configuration).
[6] RW wp_en			Write protection enable (WP pin). When enabled, the output of the chip to the WP pin is 0ÿ 0: disable; 1: enable.
[5:3] RW rd_delay			SPI read data delay cycle number. (in SDR mode) 000: read data delay 0 clock cycle; (default) 001: read data delay 0.5 device working clock cycle; 010: Read data is delayed by 1 device working clock cycle; 011: Read data is delayed by 1.5 device operating clock cycles. 100: Read data is delayed by 2 device working clock cycles; 101: Read data is delayed by 2.5 device working clock cycles; 110: Read data is delayed by 3 device working clock cycles; 111: Read data is delayed by 3.5 device working clock cycles.
[2] RW randomizer_en			The randomizer function is enabled. The default value is 1, but in the 2K/4K Page-size configuration, the logic automatically turns off the randomizer function. When enabled, scramble and descramble the data written and read to flash. 0: disable; 1: enable.
[1:0] RO		reserved	reserve.

TIMING_SPI_CFG

TIMING_SPI_CFG is the SPI Timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	TIMING_SPI_CFG	0x0000_006F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	tcss	tshsl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1	1 1	1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	tcss	CS setup time. 0x0~0x7: n+1 interface clock cycles. n is 0, 1, 2, . . . , 7.
[3:0]	RW	tshsl	Set the Deselect time of chip selection, which is equivalent to the time interval between two Flash operations. 0x0~0xF: n+1 interface clock cycles. n is 0, 1, 2, ..., 15.

PND_PWIDTH_CFG

PND_PWIDTH_CFG is the read and write pulse width configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	PND_PWIDTH_CFG	0x0000_0333

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	rw_hcnt	r_lcnt	w_lcnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 1 0 0 1			1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	rw_hcnt	NAND Flash read/write signal high level width. 0x1~0xF: 2~16 interface clock cycles.
[7:4]	RW	r_lcnt	NAND Flash read signal low level width. 0x1~0xF: 2~16 interface clock cycles.
[3:0]	RW	w_lcnt	NAND Flash write signal low level width. 0x1~0xF: 2~16 interface clock cycles.

PND_OPIDLE_CFG

PND_OPIDLE_CFG is the operation interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	PND_OPIDLE_CFG	0x0008_8880

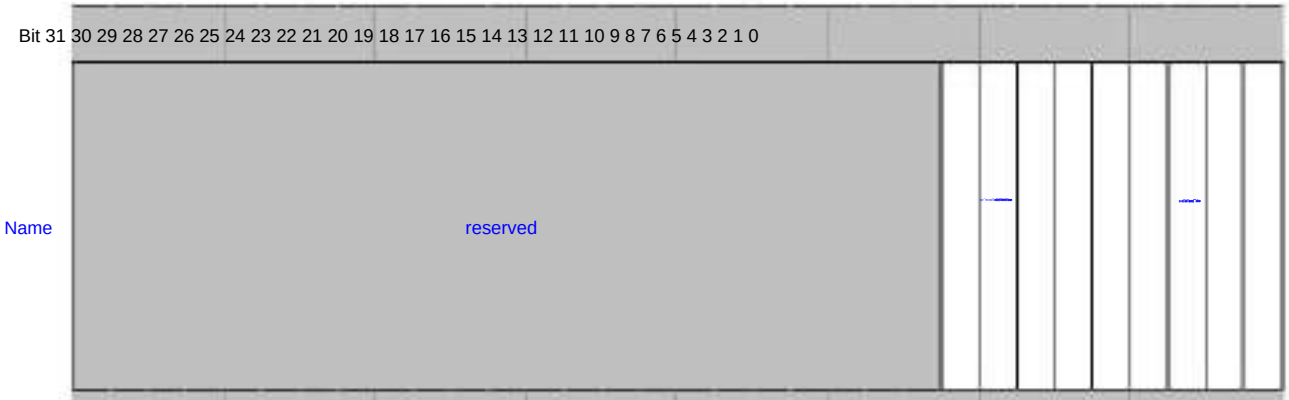
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				frb_wait				cmd1_wait				addr_wait				cmd2_wait				wait_ready_wa it			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:16]	RW	frb_wait	After sending the read and write command, delay for a period of time, and then check whether the ready signal becomes high level. The number of clock cycles of the delayed interface is: frb_wait*8.
[15:12]	RW	cmd1_wait	Number of cycles to wait after sending command1. The number of clock cycles of the delayed interface is: cmd1_wait*8.
[11:8]	RW	addr_wait	Number of cycles to wait after sending address. 0x0~0xF: configuration value. The number of interface clock cycles for delay is: addr_wait*8.
[7:4]	RW	cmd2_wait	Number of cycles to wait after sending command2. The number of clock cycles of the delayed interface is: cmd2_wait*8.
[3:0]	RW	wait_ready_wait	After the ready signal of NAND Flash becomes high, there will be a delay for a period of time before the read signal can be sent to read data. The number of cycles of delay is: frb_idle*2.

FMC_INT

FMC_INT is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	FMC_INT	0x0000_0000



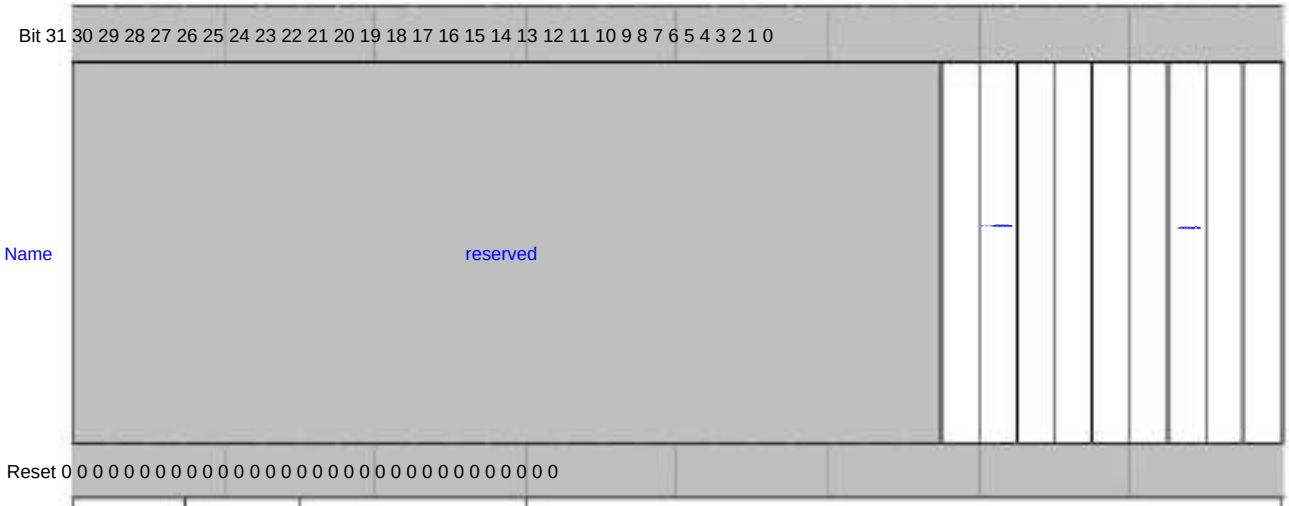
Bits	Access Name		Description
[31:9] RO		reserved	reserve.
[8]	RO	0: no interruption; nt	When FMC performs cache operation on NAND FLASH, an interrupt will be generated every time the data of a page is read. cache_page_done_i 1: There is an interrupt.
[7]	RO	ahb_op_int	When FMC performs data operation on FLASH, CPU reads and writes internal buffer. 0: no interrupt; 1: There is an interrupt.
[6]	RO	wr_lock_int	Write operation to lock address. 0: no interrupt; 1: There is an interrupt.
[5]	RO	dma_err_int	DMA transfer bus error interrupt. 0: no interrupt; 1: There is an interrupt.
[4]	RO	err_alarm_int	ECC verification warning interrupt. When the wrong bit reaches the set threshold, an interrupt is generated. 0: no interrupt; 1: There is an interrupt.
[3]	RO	err_inval_int	ECC checks for uncorrectable errors. In 8bit error correction mode, if more than 8bit errors occur in the 1024byte data, an interrupt will be generated. In 16bit error correction mode, if more than 16bit errors occur in the 1024byte data, an interrupt will be generated. In 24bit error correction mode, check if there are more than 24bit errors in the 1024byte data

			error, an interrupt is generated. In 28bit error correction mode, if more than 28bit errors occur in the 1024byte data, an interrupt will be generated. In 40bit error correction mode, if more than 40bit errors occur in the 1024byte data, an interrupt will be generated. In 64bit error correction mode, if more than 64bit errors occur in the 1024byte data, an interrupt will be generated. 0: no interrupt; 1: There is an interrupt.
[2]	RO	err_val_int	ECC checks correctable errors. In 8bit error correction mode, if 1-8bit errors occur in the 1024byte data, an interrupt will be generated. In 16bit error correction mode, if 1-16bit errors occur in the 1024byte data, an interrupt will be generated. In 24bit error correction mode, if 1-24bit errors occur in the 1024byte data, an interrupt will be generated. In the 28bit error correction mode, if there are 1-28bit errors in the 1024byte data, an interrupt will be generated. In the 40bit error correction mode, if there are 1-40bit errors in the 1024byte data, an interrupt will be generated. In the 64bit error correction mode, if there are 1-64bit errors in the 1024byte data, an interrupt will be generated. 0: no interrupt; 1: There is an interrupt.
[1]	RO	op_fail_int	The programming operation fails and an interrupt is reported. 0: no interrupt; 1: There is an interrupt.
[0]	RO	op_done_int	The controller is interrupted at the end of this operation. This flag is automatically cleared after writing to the operation register. 0: no interrupt; 1: There is an interrupt.

FMC_INT_EN

FMC_INT_EN is the interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x001C	FMC_INT_EN	0x0000_0000



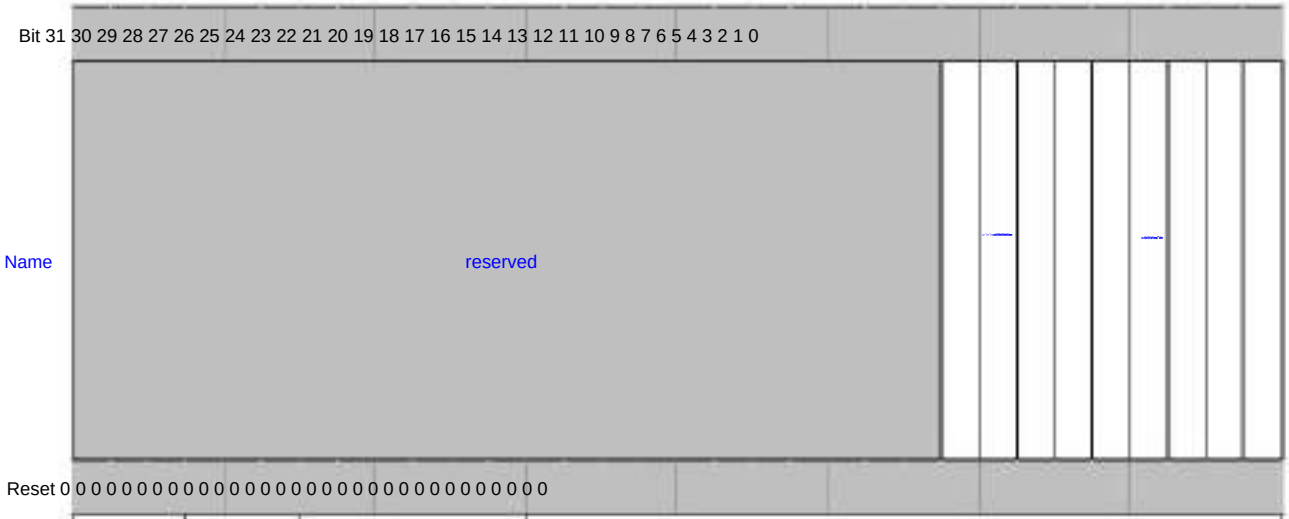
Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	cache_page_done_int_en	When FMC performs cache operation on NAND FLASH, it will generate an interrupt enable after completing the data reading of a page. 0: disable; nt_en 1: enable.
[7]	RW	ahb_op_int_en	When FMC reads and writes flash data, CPU reads and writes internal buffer error interrupt enable. 0: disable; 1: enable.
[6]	RW	wr_lock_int_en	Write to lock address error interrupt enable. 0: forbidden; 1: enable.
[5]	RW	dma_err_int_en	DMA transfer bus error interrupt enable. 0: forbidden; 1: enable.
[4]	RW	err_alarm_int_en	ECC verification warning interrupt. When the wrong bit reaches the set threshold, an interrupt is generated. 0: forbidden; 1: enable.
[3]	RW	err_inval_int_en	ECC parity uncorrectable error, an interrupt is generated. 0: disable; 1: enable.

[2] RW	err_val_int_en		ECC checks correctable errors and generates an interrupt. 0: forbidden; 1: enable.
[1] RW	op_fail_int_en		Program operation failed interrupt enable. 0: forbidden; 1: enable.
[0] RW	op_done_int_en		FMC is interrupted when this operation is finished. 0: forbidden; 1: enable.

FMC_INT_CLR

FMC_INT_CLR is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0020	FMC_INT_CLR	0x0000_0000



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	WHERE	cache_page_done_int_clr	Clear cache_page_done interrupt, write 1 to clear.
[7]	WO	ahb_op_int_clr	Clear ahb_op_err interrupt, write 1 to clear.
[6]	WO	wr_lock_int_clr	Clear wr_lock_err interrupt, write 1 to clear.
[5]	WO	dma_err_int_clr	Clear dma transfer bus error interrupt, write 1 to clear.
[4]	WO	err_alarm_int_clr	Clear err_alarm interrupt, write 1 to clear.
[3]	WO	err_inval_int_clr	Clear err_invalid interrupt, write 1 to clear.

Offset Address	Register Name	Total Reset Value
0x0020	FMC_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2]	WO	err_val_int_clr	Clear err_valid interrupt, write 1 to clear.
[1]	WO	op_fail_int_clr	Clear op_fail interrupt, write 1 to clear.
[0]	WO	op_done_int_clr	Clear op_done interrupt, write 1 to clear.

FMC_CMD

FMC_CMD is the command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	FMC_CMD	0x0000_3000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cmd2								cmd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	cmd2	The second command sent by Controller to NAND FLASH.
[7:0]	RW	cmd1	The first command sent by Controller to NAND FLASH, or the operation command sent to SPI NOR/NAND FLASH.

FMC_ADDRH

FMC_ADDRH is the high byte of the device address configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	FMC_ADDRH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	addrh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	addrh	For SPI NAND FLASH, configure the operating high byte address of the flash device.

FMC_ADDRL

FMC_ADDRL is the lower 4 bytes of the device address configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	FMC_ADDRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	addrl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	addrl	Configure the lower 4 bytes of the operating address of the flash device. For spi norflash, configure the device address.

FMC_OP_CFG

FMC_OP_CFG is the operation configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	FMC_OP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													dummy_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:12]	RO reserved	reserve.
[11]	RW fm_cs	Select the Flash device to operate on. 0ÿCS0ÿ 1ÿCS1ÿ
[10]	RW force_cs_en	CS chip select forced low enable. 0: disable; 1: enable.
[9:7]	RW mem_if_type	Read operation, SPI FLASH interface type selection. 000: Standard SPI interface type 001ÿDual-Input/Dual-Output SPI 010ÿDual-I/O SPI 011ÿQuad-Input/Dual-Output SPI 100: Quad-I/O SPI 101-111: Reserved.
[6:4]	RW addr_num	Address Byte number sent to Flash.
[3:0]	RW dummy_num	For dummy_en operation Byte number. (1Byte=4 wires 2 clock cycles or 2 wires 4 clock cycles or 1 wire 8 clock cycles)

SPI_OP_ADDR

SPI_OP_ADDR is the operation address configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	SPI_OP_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_op_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	spi_op_addr	Configure the operation address of SPI NOR/NAND FLASH. The operating address of the device is issued for each operation. Different from FMC_ADDRL and FMC_ADDRH.

FMC_DATA_NUM

FMC_DATA_NUM is the data length register.

Offset Address	Register Name	Total Reset Value
0x0038	FMC_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												op_data_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	op_data_num	The length of data to be processed in one operation. It needs to be configured when there is data transfer operation, and it does not need to be configured for DMA operation or AHB bus direct access. Valid only for ECC0.

FMC_OP

FMC_OP is the operation register.

Offset Address	Register Name	Total Reset Value
0x003C	FMC_OP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	dummy_en	After address operation, transfer dummy byte operation is enabled. 0: forbidden; 1: enable.
[7]	RW	cmd1_en	Send command1 command to FLASH to enable. 0: forbidden; 1: enable.
[6]	RW	addr_en	Write operation address enable to FLASH. 0: forbidden; 1: enable.
[5]	RW	write_data	Write data to FLASH enable. read_data_en and write_data_en cannot be 1 at the same time. 0: forbidden; 1: enable.
[4]	RW	cmd2_en	Send command2 command to NAND FLASH to enable. 0: forbidden; 1: enable.
[3]	RW	wait_ready_en	For NAND FLASH, wait for the ready/busy signal to become high to enable it. 0: forbidden; 1: enable.
[2]	RW	read_data_en	Enable to read data from Flash. read_data_en and write_data_en cannot be 1 at the same time. 0: forbidden; 1: enable.

[1]	RW	read_status_en	Read device status register enable. When the value is set to 1, send the 0x70 command to read status to NAND, and read the status data from NAND Flash, and write the returned data into the fm_status field of the NANDC status register (not into the internal buffer). 0: forbidden; 1: enable.
[0]	RWSC	reg_op_start	Send the status of the OP operation controller. 0: The controller is ready; (during software delivery operation, this bit field can only be configured as 1 to enable logic) 1: The controller is busy. (After the controller operation is completed, this bit will be automatically set to 0, indicating that the logic is completed)

FMC_DMA_LEN

FMC_DMA_LEN is the DMA operation length register.

Offset Address	Register Name	Total Reset Value
0x0040	FMC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dma_len															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:0]	RW	dma_len	DMA operation data transfer length, in byte. When used for SPI NAND FLASH ecc0 and NAND FLASH ecc0, it is configured as the data length of the spare area. When used for DMA read and write operations of SPI NORFLASH, it is configured as the data length required by DMA.

FMC_DMA_AHB_CTRL

FMC_DMA_AHB_CTRL is the DMA AHB bus control register.

Offset Address	Register Name	Total Reset Value
0x0048	FMC_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2]	RW	burst16_en	BURST16 is enabled. 0: forbidden; 1: enable.
[1]	RW	burst8_en	BURST8 is enabled. 0: forbidden; 1: enable.
[0]	RW	burst4_en	BURST4 is enabled. 0: forbidden; 1: enable.

FMC_DMA_SADDR_D0

FMC_DMA_SADDR_D0 is DDR start address register 0 for DMA operation.

Offset Address	Register Name	Total Reset Value
0x004C	FMC_DMA_SADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_mem_saddr_d.	For SPI NOR FLASH, instruct DMA to operate DDR start address register For SPI NAND FLASH, indicating DMA operation, DDR operand 0 data base address.

FMC_DMA_SADDR_D1

FMC_DMA_SADDR_D1 is DDR start address register 1 for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0050	FMC_DMA_SADDR_D1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_mem_saddr_d1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	dma_mem_saddr_d 1 1, it is useless for 2KB and	For NAND FLASH, it indicates DMA operation, DDR operation data base address 4KB pagesize configuration.

FMC_DMA_SADDR_D2

FMC_DMA_SADDR_D2 is DDR start address register 2 for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0054	FMC_DMA_SADDR_D2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_mem_saddr_d2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	dma_mem_saddr_d 2 2, only useful for 16KB	For NAND FLASH, indicate DMA operation, DDR operation data base address pagesize.

FMC_DMA_SADDR_D3

FMC_DMA_SADDR_D3 is DDR start address register 3 for DMA operation.

Offset Address	Register Name	Total Reset Value
0x0058	FMC_DMA_SADDR_D3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_mem_saddr_d 3	For NAND FLASH, indicate DMA operation, DDR operation data base address 3, only useful for 16KB pagesize.

FMC_DMA_SADDR_OOB

FMC_DMA_SADDR_OOB is the start address register for DMA operation DDR storing OOB information.

Offset Address	Register Name	Total Reset Value
0x005C	FMC_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_mem_saddr_o DDR ob	base address for reading and writing OOB data.

FMC_OP_CTRL

FMC_OP_CTRL is the operation control register.

Offset Address	Register Name	Total Reset Value
0x0068	FMC_OP_CTRL	0x0003_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rd_opcode								wr_opcode							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	rd_opcode	SPI NAND/NOR FLASH, non-bus mode, DMA read operation command. (FAST_READ/READ/DUAL_READ)
[15:8]	RW	wr_opcode	For SPI NAND/NOR FLASH, non-bus mode, DMA write operation command.
[7:6]	RO	reserved	reserve.
[5:4]	RW	rd_op_sel	During read operation, read data area selection. 00: read the whole page; 01: read only OOB operation; 1x: reserved.
[3:2]	RO	reserved	reserve.
[1]	RW	rw_op	DMA read and write mode selection. 0: DMA read; 1: DMA write.
[0]	RWSC	dma_op_ready	Send the status of the operation controller. 0: The controller is ready; (software can only be configured as 1, enabling logic) 1: The controller is busy. (The logic can only be configured as 0, indicating that the logic is completed)

FMC_TIMEOUT_WR

FMC_TIMEOUT_WR is the write operation TIMEOUT time register.

Offset Address	Register Name	Total Reset Value
0x006C	FMC_TIMEOUT_WR	0x00FF_FFFF

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	timeout_wr
Reset	0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	timeout_wr	The length of timeout during the waiting period of the programming operation busy. (Device Response Timeout Time) The unit is 1 interface clock cycle. (NAND/SPI NAND/SPI NOR FLASH)

FMC_OP_PARA

FMC_OP_PARA is OP operation parameter selection register.

Offset Address	Register Name	Total Reset Value
0x0070	FMC_OP_PARA	0x0000_0000

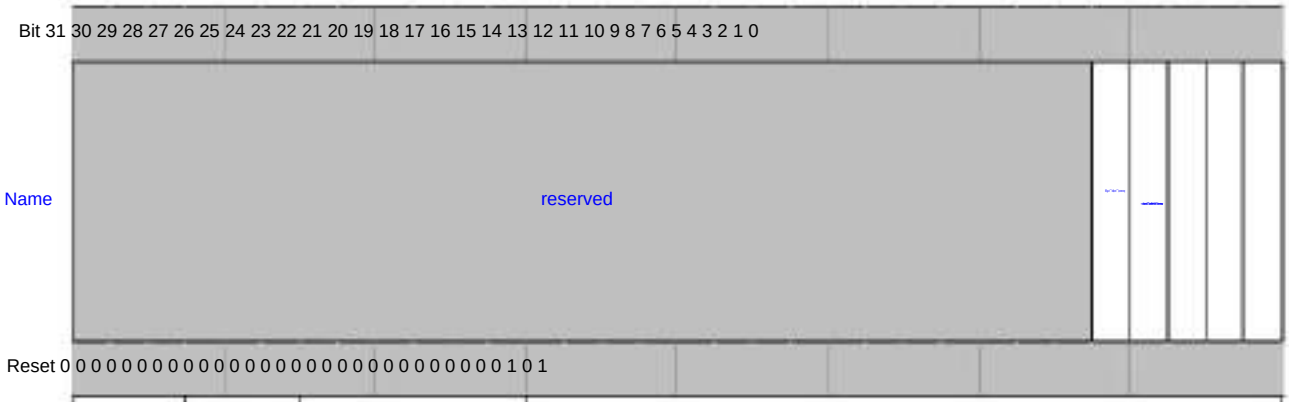
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	rd_oob_only	When the OP issues a register read flash operation, only the OOB-related sectors are read. 0: read page; 1: read only OOB.
[0]	RW	last_segment	Since the internal buffer only operates 8K at a time, for devices with a page size larger than 8K (16K, etc.), this register is used to indicate whether to transfer to the last 8KB of data. (Used for 16K OP operation, DMA does not need to be configured) 0: The current operation data is not the last 8K data segment; 1: The current operation data is the last 8K data segment.

FMC_BOOT_SET

FMC_BOOT_SET is set register for boot.

Offset Address	Register Name	Total Reset Value
0x0074	FMC_BOOT_SET	0x0000_0005



Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	boot_otp_cfg	Device configuration information, using OTP to directly configure the fmc_cfg register. 0: Use adaptive Boot mode; 1: Use OTP mode.
[3]	RW	device_ecc_sel	For SPI NAND FLASH, configure whether to use the internal ECC of the device. 0: not used; 1: use.
[2]	RW	two_image_boot	For NAND FLASH boot, whether to use dual mirror boot. 0: not used; 1: use.
[1]	RW	boot_quad_mode	For SPI NAND FLASH, whether BOOT uses four-wire mode to start. The reset value is determined by the pin SFC_EMMC_BOOT_MODE. 0: Not used, use single-wire mode to start; 1: use.
[0]	RW	boot_page0_cfg	NAND FLASH /SPI NAND FLASH data format conversion enable. 0: No data format conversion, no traversal operation during BOOT; 1: Adaptive data format conversion, traversal operation during BOOT.

FMC_LP_CTRL

FMC_LP_CTRL is the low power control register.

Offset Address	Register Name	Total Reset Value
0x0078	FMC_LP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	clk_gate_en	Clock gating selection. Turn on this function, use low power consumption design, and logic select to turn off the working clock of the module. 0: All clocks are enabled; 1: According to low power consumption design, turn off the clock.

FMC_LOCK

FMC_LOCK is the lock address configuration register.

Offset Address	Register Name	Total Reset Value
0x007C	FMC_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	lock_excmd_en	For extended write commands (new commands that may be added to new devices), write protection is enabled for the protected address. 0: forbidden; 1: enable.

[2] RW	lock_en		Flash lock enabled. 0: forbidden; 1: enable.
[1] RW	global_lock_en		Flash global lock enabled. 0: forbidden; 1: enable.
[0] RW	lock_down		Flash lock mode. 0: lock mode; 1: lock-down mode, write 1 at one time, only hardware reset can write 0 to this bit.

FMC_LOCK_SA0

FMC_LOCK_SA0 is the lock start address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x0080	FMC_LOCK_SA0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_saddr0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_saddr0	Latch start address 0, corresponding to page address.

FMC_LOCK_EA0

FMC_LOCK_EA0 is the lock end address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x0084	FMC_LOCK_EA0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_eaddr0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:0]	RW	flash_lock_eaddr	0 Latch end address 0, corresponding to page address.

FMC_LOCK_SA1

FMC_LOCK_SA1 is the lock start address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x0088	FMC_LOCK_SA1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_saddr1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_saddr	1 Latch start address 1, corresponding to page address.

FMC_LOCK_EA1

FMC_LOCK_EA1 is the lock end address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x008C	FMC_LOCK_EA1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_eaddr1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_eaddr	1 Latch end address 1, corresponding to page address.

FMC_LOCK_SA2

FMC_LOCK_SA2 is the lock start address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x0090	FMC_LOCK_SA2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_saddr2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_saddr2	Latch start address 2, corresponding to page address.

FMC_LOCK_EA2

FMC_LOCK_EA2 is the lock end address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	FMC_LOCK_EA2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_eaddr2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_eaddr2	Latch end address 2, corresponding to page address.

FMC_LOCK_SA3

FMC_LOCK_SA3 is the lock start address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x0098	FMC_LOCK_SA3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_saddr3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_saddr3	Latch start address 3, corresponding to page address.

FMC_LOCK_EA3

FMC_LOCK_EA3 is the lock end address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x009C	FMC_LOCK_EA3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flash_lock_eaddr3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	flash_lock_eaddr3	Latch end address 3, corresponding to page address.

FMC_EXPCMD

FMC_EXPCMD is the extended page command register.

Offset Address	Register Name	Total Reset Value
0x00A0	FMC_EXPCMD	0x8080_8080

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	ex_pcmd3	ex_pcmd2	ex_pcmd1	ex_pcmd0
Reset	1 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	ex_pcmd3	Flash extended page write operation command 3
[23:16]	RW	ex_pcmd2	Flash extended page write operation command 2.
[15:8]	RW	ex_pcmd1	Flash extended page write operation command 1.
[7:0]	RW	ex_pcmd0	Flash extended page write operation command 0.

FMC_EXBCMD

FMC_EXBCMD is the extended block command register.

Offset Address	Register Name	Total Reset Value
0x00A4	FMC_EXBCMD	0x0000_6060

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	ex_bcmd1	ex_bcmd0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0	1 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	ex_bcmd1	Flash extended block write operation command 1.
[7:0]	RW	ex_bcmd0	Flash extended block write operation command 0.

FMC_ERR_THD

FMC_ERR_THD is the ECC alarm threshold register.

Offset Address	Register Name	Total Reset Value
0x00A8	FMC_ERR_THD	0x0000_00FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		fmc_err_thd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	fmc_err_thd	ECC parity warning threshold configuration register. When the error bit reaches this threshold, the ECC verification alarm interrupt is triggered. Note: 1. When the error cannot be corrected, no matter what the value of this register is, it will be reported as an uncorrectable interrupt; 2. Set it to be equivalent to 0 and 1, that is, as long as there is an error, it will be reported as an alarm interrupt; 3. When the setting value is greater than the error-correctable range, no matter how many bit errors occur, the alarm interrupt will not be reported, and only error-correctable and uncorrectable error interrupts will be generated.

FMC_FLASH_INFO

FMC_FLASH_INFO is the device status register value.

Offset Address	Register Name	Total Reset Value
0x00AC	FMC_FLASH_INFO	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	exp_bb_flag	bb_flag	exp_flash_status	flash_status
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	exp_bb_flag	Uncorrected data corresponding to the bad block flag of the current page when the read-only OOB issued by the extended operation or when the page is read.
[23:16]	RO	bb_flag	When only reading OOB or reading page, the uncorrected data corresponding to the bad block flag of the current page
[15:8]	RO	exp_flash_status	In extended operation, the value of the status register read by the controller from the device.
[7:0]	RO	flash_status	In normal operation, the controller reads the value of the status register from the device. (For the meaning of the bit, please refer to the manual of each flash device)

FMC_OP_CNT

FMC_OP_CNT is the register for the number of operations issued by the controller.

Offset Address	Register Name	Total Reset Value
0x00B8	FMC_OP_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			op_cnt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	op_cnt	For the device operation count register, configure the OP register counter to add one, and keep it when it reaches the maximum value, and read it to clear it. For debugging only.

FMC_VERSION

FMC_VERSION is the version register.

Offset Address	Register Name	Total Reset Value
0x00BC	FMC_VERSION	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	FMC version V100.

FMC_ERR_NUM0_BUF0

FMC_ERR_NUM0_BUF0 is the statistical register of error correction information 0 of the first buffer of SPINAND FLASH and NAND FLASH.

Offset Address	Register Name	Total Reset Value
0x00C0	FMC_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf0	For the first buffer operation of 2KB, 4KB, 8KB and 16KB pagesize, the first 4KB data error statistics register. bit[31:24]: Fourth KB data error correction, error data statistics register. bit[23:16]: Third KB data error correction, error data statistics register. bit[15:8]: Second KB data error correction, error data statistics register. bit[7:0]: First KB data error correction, error data statistics register.

FMC_ERR_NUM1_BUF0

FMC_ERR_NUM1_BUF0 is the first buffer error correction information 1 statistical register of NANDFLASH.

Offset Address	Register Name	Total Reset Value
0x00C4	FMC_ERR_NUM1_BUF0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_num1_buf0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf0	For the first buffer operation of 8KB and 16KB pagesize, the last 4KB data error statistics register. bit[31:24]: Eighth KB data error correction, error data statistics register. bit[23:16]: Seventh KB data error correction, error data statistics register. bit[15:8]: Sixth KB data error correction, error data statistics register. bit[7:0]: Fifth KB data error correction, error data statistics register.

FMC_ERR_NUM0_BUF1

FMC_ERR_NUM0_BUF1 is the second buffer error correction statistics register 0 of NAND FLASH.

Offset Address	Register Name	Total Reset Value
0x00C8	FMC_ERR_NUM0_BUF1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_num0_buf1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf1	For 16KB pagesize, for the second buffer operation, the error statistics register is 0. bit[31:24]: Fourth KB data error correction, error data statistics register. bit[23:16]: Third KB data error correction, error data statistics register. bit[15:8]: Second KB data error correction, error data statistics register. bit[7:0]: First KB data error correction, error data statistics register.

FMC_ERR_NUM1_BUF1

FMC_ERR_NUM1_BUF1 is the second buffer error correction statistics register 1 of NANDFLASH.

Offset Address	Register Name	Total Reset Value
0x00CC	FMC_ERR_NUM1_BUF1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_num1_buf1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf1	For 16KB pagesize, the second buffer operation, error statistics register 1ÿ bit[31:24]: Eighth KB data error correction, error data statistics register. bit[23:16]: Seventh KB data error correction, error data statistics register. bit[15:8]: Sixth KB data error correction, error data statistics register. bit[7:0]: Fifth KB data error correction, error data statistics register.

FMC_ERR_ALARM_ADDRH

FMC_ERR_ALARM_ADDRH is the high byte register of ECC alarm flash address.

Offset Address	Register Name	Total Reset Value
0x00D0	FMC_ERR_ALARM_ADDRH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fmc_err_alarm_addrh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RO	interrupt is the high byte rh	When an ECC alarm interrupt occurs, the address of the last flash operation that triggered the register of fmc_err_alarm_add.

FMC_ERR_ALARM_ADDRL

FMC_ERR_ALARM_ADDRL is the low byte register of ECC alarm flash address.

Offset Address	Register Name	Total Reset Value
0x00D4	FMC_ERR_ALARM_ADDRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fmc_err_alarm_addrl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO		When an ECC alarm interrupt occurs, the last flash operation address fmc_err_alarm_add rl that triggered the interrupt is the lower 4-byte register.

FMC_ECC_INVALID_ADDRH

FMC_ECC_INVALID_ADDRH is the high byte register of ECC uncorrectable address.

Offset Address	Register Name	Total Reset Value
0x00D8	FMC_ECC_INVALID_ADDRH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved fmc_ecc_invalid_addrh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RO	interrupt last time is fmc_ecc_invalid_addrh high byte register.	When an ECC uncorrectable error occurs, the address of the flash operation that triggered the

FMC_ECC_INVALID_ADDRL

FMC_ECC_INVALID_ADDRL is the lower 4byte register of ECC uncorrectable address.

Offset Address	Register Name	Total Reset Value
0x00DC	FMC_ECC_INVALID_ADDRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fmc_ecc_invalid_addrl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	ddrl that triggers an interrupt is the lower 4-byte register.	When an ECC uncorrectable error occurs, the last flash operation address fmc_ecc_invalid_a

FMC_READ_TIMING_TUNE

FMC_READ_TIMING_TUNE is an asynchronous NAND read sampling point adjustment register.

Offset Address	Register Name	Total Reset Value
0x0E0	FMC_READ_TIMING_TUNE	0x0000_0000

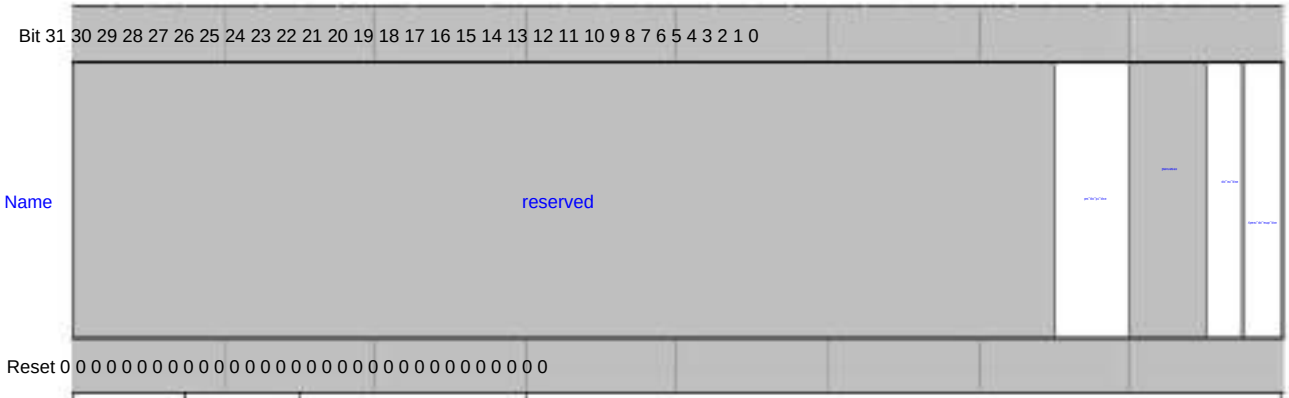
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	reserve.
[2:0]	RW	read_timing_tune	Asynchronous nand read operation, sample read data software adjustment register. When asynchronous nand reads flash data, the sampling point delay clock number selection is determined according to the current interface frequency and chip internal delay. 000: No delay, data is sampled at the rising edge of the rd signal. 001: The rising edge of the rd signal is delayed by 1 interface clock cycle to sample data. 010: The rising edge of the rd signal is delayed by 2 interface clock cycles to sample data. 011: The rising edge of the rd signal is delayed by 3 interface clock cycles to sample data. 100: The rising edge of the rd signal is delayed by 4 interface clock cycles to sample data. 101: The rising edge of the rd signal is delayed by 5 interface clock cycles to sample data. 110: The rising edge of the rd signal is delayed by 6 interface clock cycles to sample data. 111: The rising edge of the rd signal is delayed by 7 interface clock cycles to sample data.

FMC_EXP_OP_CTRL

FMC_EXP_OP_CTRL is the extended operation control register.

Offset Address	Register Name	Total Reset Value
0x100	FMC_EXP_OP_CTRL	0x0000_0000



Bits	Access Name		Description
[31:6]	RO	reserved	reserve.
[5:4]	RW exp_rd_op_sel		Extended operation, read operation, read data area selection. 00: read the whole page; 01: read only OOB operation; 1x: reserved.
[3:2]	RO	reserved	reserve.
[1]	RW exp_rw_op		Extended operation, the operation read and write type of the issued device: 0: DMA read; 1: DMA write.
[0]	RWSC exp_dma_op_ready	1: The controller is	The logical operation sends the enable register. 0: The controller is ready; (the controller is automatically cleared to 0) busy. (Configured to 1 by software) When the software sends the operation, it is configured as 1, and it will be automatically cleared after the controller operation is completed. The software can only configure 1, not 0.

FMC_EXP_ADDRH

FMC_EXP_ADDRH is the high byte of the extended operation device address configuration register.

Offset Address	Register Name	Total Reset Value
0x104	FMC_EXP_ADDRH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	exp_addrh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	exp_addrh	extended operation, configure the high byte address of flash operation.

FMC_EXP_ADDRL

FMC_EXP_ADDRL is the lower 4 bytes of the extended operation device address configuration register. For internal reference only

Offset Address	Register Name	Total Reset Value
0x108	FMC_EXP_ADDRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_addrl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	exp_addrl	Extended operation, configure the lower 4 bytes of the operation address of the flash device.

FMC_EXP_DMA_SADDR_D0

FMC_EXP_DMA_SADDR_D0 is DDR start address register 0 for extended DMA operation. For internal reference only

Offset Address	Register Name	Total Reset Value
0x10C	FMC_EXP_DMA_SADDR_D0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_dma_mem_saddr_d0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d0	Extended operation, for SPI NAND FLASH, indicates DMA operation, DDR address. operates data base

FMC_EXP_DMA_SADDR_D1

FMC_EXP_DMA_SADDR_D1 is the DDR start address register 1 for extended DMA operation.

Offset Address	Register Name	Total Reset Value
0x110	FMC_EXP_DMA_SADDR_D1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	exp_dma_mem_saddr_d1	For NAND FLASH, extended operation, indicating DMA operation, DDR operation data base address 1, useless for 2KB and 4KB pagesize configuration.

FMC_EXP_DMA_SADDR_D2

FMC_EXP_DMA_SADDR_D2 is the extended DMA operation DDR start address register 2. For internal reference only

Offset Address	Register Name	Total Reset Value
0x114	FMC_EXP_DMA_SADDR_D2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	exp_dma_mem_saddr_d2	For NAND FLASH, extended operation, indicating DMA operation, DDR operation data base address 2, only useful for 16KB pagesize.

FMC_EXP_DMA_SADDR_D3

FMC_EXP_DMA_SADDR_D3 is the DDR start address register 3 for extended DMA operation.

Offset Address	Register Name	Total Reset Value
0x118	FMC_EXP_DMA_SADDR_D3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_dma_mem_saddr_d3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d3	For NAND FLASH, extended operation, indicating DMA operation, DDR operation data base address 3, only useful for 16KB pagesize.

FMC_EXP_DMA_SADDR_OOB

FMC_EXP_DMA_SADDR_OOB is the start address register for storing OOB information for extended DMA operation DDR.

For internal reference only

Offset Address	Register Name	Total Reset Value
0x11C	FMC_EXP_DMA_SADDR_OOB	0x0000_0000

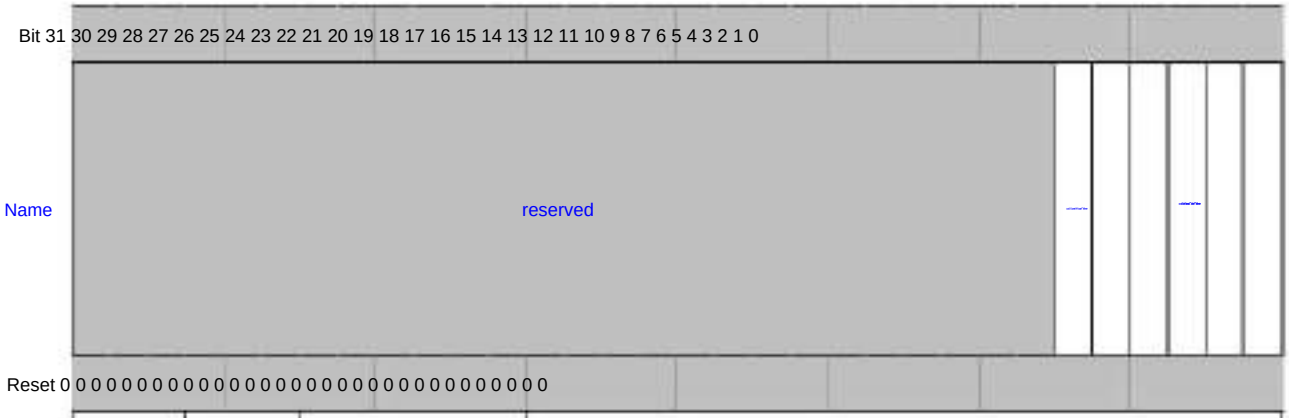
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_dma_mem_saddr_oob
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_oob	Extended operation, read and write DDR base address of OOB area data. dr_oob

FMC_EXP_INT

FMC_EXP_INT is the extended operation interrupt status register.

Offset Address	Register Name	Total Reset Value
0x120	FMC_EXP_INT	0x0000_0000



Bits	Access Name		Description
[31:6] RO		reserved	reserve.
[5]	RO	exp_dma_err_int	DMA transfer bus error interrupt. 0: no interrupt; 1: There is an interrupt.
[4]	RO	exp_err_alarm_int	ECC verification warning interrupt. When the wrong bit reaches the set threshold, an interrupt is generated. 0: no interrupt; 1: There is an interrupt.
[3]	RO	exp_err_inval_int	ECC checks for uncorrectable errors. In 8bit error correction mode, if more than 8bit errors occur in the 1024byte data, an interrupt will be generated. In 16bit error correction mode, if more than 16bit errors occur in the 1024byte data, an interrupt will be generated. In 24bit error correction mode, if more than 24bit errors occur in the 1024byte data, an interrupt will be generated. In 28bit error correction mode, if more than 28bit errors occur in the 1024byte data, an interrupt will be generated. In 40bit error correction mode, if more than 40bit errors occur in the 1024byte data, an interrupt will be generated. In 64bit error correction mode, if more than 64bit errors occur in the 1024byte data, an interrupt will be generated. 0: no interrupt; 1: There is an interrupt.

[2]	RO	exp_err_val_int	ECC checks correctable errors. In 8bit error correction mode, if 1-8bit errors occur in the 1024byte data, an interrupt will be generated. In 16bit error correction mode, if 1-16bit errors occur in the 1024byte data, an interrupt will be generated. In 24bit error correction mode, if 1-24bit errors occur in the 1024byte data, an interrupt will be generated. In the 28bit error correction mode, if there are 1-28bit errors in the 1024byte data, an interrupt will be generated. In the 40bit error correction mode, if there are 1-40bit errors in the 1024byte data, an interrupt will be generated. In the 64bit error correction mode, if there are 1-64bit errors in the 1024byte data, an interrupt will be generated. 0: no interrupt; 1: There is an interrupt.
[1]	RO	exp_op_fail_int	The programming operation fails and an interrupt is reported. 0: no interrupt; 1: There is an interrupt.
[0]	RO	exp_op_done_int	The controller is interrupted when the extension operation ends. This flag is automatically cleared after writing to the operation register. 0: no interrupt; 1: There is an interrupt.

FMC_EXP_INT_EN

FMC_EXP_INT_EN is the extended operation interrupt enable register. For internal reference only

Offset Address	Register Name	Total Reset Value
0x124	FMC_EXP_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	exp_dma_err_int_en	DMA transfer bus error interrupt enable. 0: disable; 1: enable.
[4]	RW	exp_err_alarm_int_in	ECC verification warning interrupt. When the wrong bit reaches the set threshold, an interrupt is generated. 0: disabled; 1: enable.
[3]	RW	exp_err_inval_int_in	ECC parity uncorrectable error, an interrupt is generated. 0: forbidden; 1: enable.
[2]	RW	exp_err_val_int_en	ECC checks correctable errors and generates an interrupt. 0: forbidden; 1: enable.
[1]	RW	exp_op_fail_int_en	Program operation failed interrupt enable. 0: forbidden; 1: enable.
[0]	RW	exp_op_done_int_en	The FMC is interrupted when the extended operation ends. 0: disable; 1: enable.

FMC_EXP_INT_CLR

FMC_EXP_INT_CLR is the extended operation interrupt clear register. For internal reference only

Offset Address	Register Name	Total Reset Value
0x128	FMC_EXP_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	WHERE	exp_dma_err_int_c	Clear DMA transfer bus error interrupt, write 1 to clear. lr
[4]	WHERE	exp_err_alarm_int_	Clear exp_err_alarm interrupt, write 1 to clear. clr
[3]	WHERE	exp_err_inval_int_	Clear exp_err_invalid interrupt, write 1 to clear. clr
[2]	WO	exp_err_val_int_clr	Clear exp_err_valid interrupt, write 1 to clear.
[1]	WO	exp_op_fail_int_clr	Clear exp_op_fail interrupt, write 1 to clear.
[0]	WHERE	exp_op_done_int_c	Clear exp_op_done interrupt, write 1 to clear. lr

FMC_EXP_ERR_NUM0_BUF0

FMC_EXP_ERR_NUM0_BUF0 is the first buffer error correction information 0 statistical register of the extended operation.

Offset Address	Register Name	Total Reset Value
0x12C	FMC_EXP_ERR_NUM0_BUF0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_err_num0_buf0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	exp_err_num0_buf 0	For the first buffer operation of 2KB, 4KB, 8KB and 16KB pagesize, the first 4KB data error statistics register. bit[31:24]: Fourth KB data error correction, error data statistics register. bit[23:16]: Third KB data error correction, error data statistics register. bit[15:8]: Second KB data error correction, error data statistics register. bit[7:0]: First KB data error correction, error data statistics register.

FMC_EXP_ERR_NUM1_BUF0

FMC_EXP_ERR_NUM1_BUF0 is the first buffer error correction information 1 statistics register of the extended operation.

Offset Address	Register Name	Total Reset Value
0x130	FMC_EXP_ERR_NUM1_BUF0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	exp_err_num1_buf0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	exp_err_num1_buf	For the first buffer operation of 8KB and 16KB pagesize, the last 4KB data error statistics register. bit[31:24]: Eighth KB data error correction, error data statistics register. bit[23:16]: Seventh KB data error correction, error data statistics register. 0 bit[15:8]: Sixth KB data error correction, error data statistics register. bit[7:0]: Fifth KB data error correction, error data statistics register.

FMC_EXP_ERR_NUM0_BUF1

FMC_EXP_ERR_NUM0_BUF1 is the second buffer error correction statistics register 0 of the extended operation.

Offset Address	Register Name	Total Reset Value
0x13C	FMC_EXP_ERR_NUM0_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num0_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	exp_err_num0_buf 1 For 16KB pagesize, the second buffer operation, error statistics register 0ÿ bit[31:24]: Fourth KB data error correction, error data statistics register. bit[23:16]: Third KB data error correction, error data statistics register. bit[15:8]: Second KB data error correction, error data statistics register. bit[7:0]: First KB data error correction, error data statistics register.

FMC_EXP_ERR_NUM1_BUF1

FMC_EXP_ERR_NUM1_BUF1 is the second buffer error correction statistics register 1 of the extended operation.

Offset Address	Register Name	Total Reset Value
0x140	FMC_EXP_ERR_NUM1_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num1_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	exp_err_num1_buf For 16KB pagesize, the second buffer operation, error count register 1. bit[31:24]: Eighth KB data error correction, error data statistics register. bit[23:16]: Seventh KB data error correction, error data statistics register. 1 bit[15:8]: Sixth KB data error correction, error data statistics register. bit[7:0]: Fifth KB data error correction, error data statistics register.

Table of contents

illustration catalog

5 GSF

5.1 Overview

GSF (Gigabit Switch Fabric) Gigabit Ethernet switching interface realizes the receiving and sending of network interface data, supports 10/100/1000Mbit/s working mode configurable, and supports full-duplex and half-duplex working modes. The network port can realize data communication with the CPU port. In addition, the network port supports EEE (Engery Efficient Ethernet) and WoL (Wake_on_LAN) network wake-up functions.

5.2 Functional description

The Ethernet switching module has the following features:

Support 10/100/1000Mbit/s rate. Support full-duplex or half-duplex working mode. Support RMII/RGMII (Reduced Gigabit Media Independent Interface) interface. Provide MDIO interface.

Supports frame length validity detection, and discards ultra-long frames and ultra-short frames.

Supports CRC check for input frames, and can discard frames with check errors. Support adding CRC check to the output frame.

Support short frame filling function.

Supports external loopback (that is, line-side loopback) in port full-duplex mode. Supports statistical counting of received and sent frames. Support broadcast frame, multicast frame and unicast frame filtering. Support control packet, IP packet, broadcast or multicast packet speed limit processing function is configurable.

Support packet filtering function.

Supports two interrupt modes: enqueue interrupt and timeout interrupt.

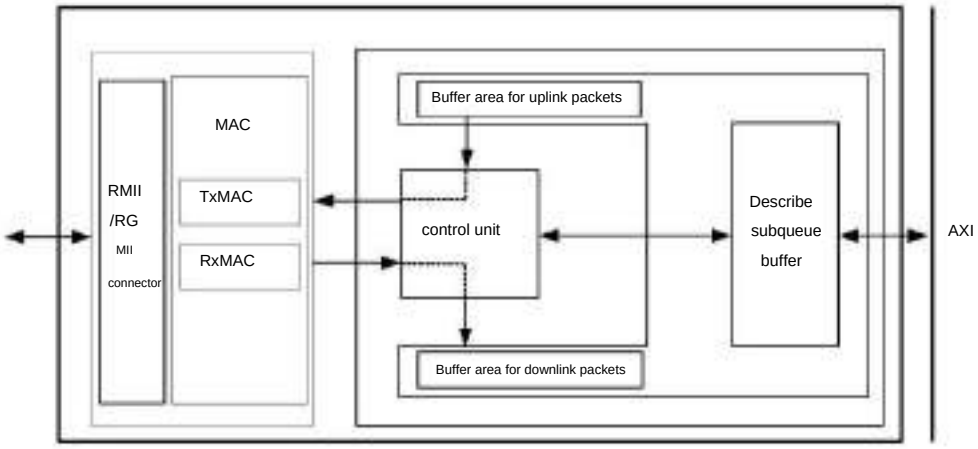
Support sending and receiving packet buffering. Support EEE Energy Efficient Ethernet function. Support WoL wake-on-lan function. Support SG (Scatter Gather) dispersion aggregation function.

Both receiving and sending directions support COE (Checksum Offload Engine) checksum offload engine function. Support TSO (TCP Segment Offload) TCP segment offload function. Support UFO (UDP Fragment Offload) UDP fragment offload function.

5.3 Overall data flow

Figure 5-1 shows the overall data flow of the GSF (Gigabit Switch Fabric) Gigabit Ethernet switching interface .

Figure 5-1 GSF overall data flow



5.4 Network port function configuration description

5.4.1 Ethernet transceiver frame management function

The CPU manages the sending and receiving frame addresses of the Ethernet by configuring the description sub-queue buffer area:

When receiving, Ethernet distinguishes various data packets received from the external network, and according to the message cache information configured by the CPU, including the start address of the message cache, the depth of the message cache, etc., stores the received legal packets to the in DDR.

When sending, Ethernet carries the message stored in DDR through the bus according to the message cache information configured by the CPU, including the start address of the message cache, the length of the message, and other message information, and assembles it into a packet by itself. Then send it to the network interface.

5.4.2 Send and receive DDR buffer description sub-queue configuration

When sending, the CPU needs to configure 2 buffer queues stored in DDR. When receiving, the CPU configures another 2 buffer queues. The starting addresses of the buffer queues are all word addresses, and one descriptor contains 4 words. The subword represents a packet cache information, and the first two words of the sending and receiving buffer descriptor are shown in Table 5-1 .

Table 5-1 Data structure of the first two words of the transceiver buffer descriptor

name	Bit width (bit) Description	
DataBudSAddr 32		The starting address of the packet buffer, supporting byte addresses.
DescVld	1	Descriptor effective identifier, 1 is valid, 0 is invalid.
DataLen	11	The amount of valid data in the message buffer, in byte.
BufLen	11	The writable depth of the message cache, in bytes.

说明

In the receiving direction, since the maximum frame length is 1.6KB, the storage space allocated to each frame is larger than 1.6KB. It is recommended to be 1600B+128B, the software needs to ensure that the address space of this size is the available access space for storing packet data in the network.

Table 5-2 Data structure of the first two words of the send buffer descriptor

Signal Name Bit Bit	Name Description		
desc_word1 [31:0]		DataBufSAddr 1) If the current descriptor is a non-SG descriptor, it identifies the starting address of the message buffer; 2) If the current descriptor is an SG descriptor, identify the starting address of the secondary linked list.	
desc_word2 [31]		hw_own	Identify the ownership of the current descriptor 0: the descriptor software uses; 1: This descriptor logic is used.
	[30]	sg_flag	Whether to support SG. 0: Does not support SG; 1: Supports SG. Note that when sg_flag is 0, tso_flag must be 0.
	[29]	coe_flag	Whether to perform checksum offload. 0: Do not execute checksum offload; 1: Execute checksum offload.
	[28]	leave_flag	Whether to perform TSO operation. 0: Do not perform TSO operation; 1: Perform TSO operation.
	[27]	reserved	reserve.
	[26:16]	data_len	1. When sg_flag is 1, this field indicates the mss size of the sliced message; 2. When sg_flag is 0, it indicates the length of the entire message Every time.

Signal Name Bit	Bit	Name	Description
	[15:11]	nfrags_num	nfrags contained in the SKB indicated by the current descriptor The maximum number is 17.
	[10]	vlan_flag	Whether the current packet has a VLAN tag. 0: The current packet has no VLAN ID; 1: The current packet has no VLAN ID.
	[9]	ip_version	Current packet IP protocol version. 0ÿIPv4ÿ 1ÿIPv6ÿ
	[8]	protocol_type	The current packet transport layer protocol type. 0ÿTCPÿ 1ÿUDPÿ
	[7:4]	ip_hdr_len	IP header length of the current packet, in word (4 bytes) as the unit. If the current message is an IPv4 message, its length is 5~15 words; if the current message is an IPv6 message, its length is 10 words.
	[3:0]	protocol_hdr_le n	If the current message is a TCP message, it indicates the length of its TCP header, in word (4 bytes), and the value is 5 to 15 words; if the current message is a UDP message, it indicates the length of its UDP header, in word (4 bytes) as the unit, and the value is 2word.

5.4.3 Ethernet packet receiving interrupt management function

interrupt generated

Configure the receiving direction enqueue interrupt enable and report enqueue interrupt waterline, when the number of descriptors written back into DDR reaches the configured waterline, a receive enqueue interrupt will be generated:

Configure ENA_PMU_INT (PMU module original interrupt register) bit[17]rx_bq enqueue interrupt enable; configure IN_QUEUE_TH (rx_bq, tx_rq enqueue interrupt watermark register) bit[7:0]. Configure the timeout interrupt enable and timeout watermark in the receiving direction. When the logic writes back a descriptor, the timeout count is started. If the timeout count reaches the configured timeout time under the condition that the receiving enqueuing interrupt is not met, a receive timeout will be generated. interruption. If the conditions for reporting two interrupts are met at the same time, only the receiving enqueuing interrupt is reported:

Configure ENA_PMU_INT (PMU module original interrupt register) bit[28]rx_bq to enable queue timeout interrupt;

Configure RX_BQ_IN_TIMEOUT_TH (rx_bq enqueue timeout raw interrupt watermark register).

interrupt clear

After the CPU receives the receive queue interrupt or receive timeout interrupt, write 1 to clear the receive queue interrupt and receive timeout interrupt.

5.4.4 Ethernet packet sending interrupt management function

interrupt generated

Configure the enqueue interrupt enable of the sending direction and the waterline for reporting the enqueue interrupt. When the number of descriptors written back into the DDR reaches the configured waterline, a send enqueue interrupt will be generated:

Configure ENA_PMU_INT (PMU module original interrupt register) bit[19] tx_rq enqueue interrupt enable; configure IN_QUEUE_TH (rx_bq, tx_rq enqueue interrupt watermark register) bit[23:16]. Configure the send timeout interrupt enable and timeout watermark. When the logic writes back a descriptor, start the timeout count. If the timeout count reaches the configured timeout time under the condition that the send queue interrupt is not met, a send timeout interrupt will be generated. . If the conditions for reporting two kinds of interrupts are met at the same time, only the queue-entry interrupt will be reported: Configure ENA_PMU_INT (PMU module original interrupt register) bit[29]tx_rq to enable the enqueue timeout interrupt; configure TX_RQ_IN_TIMEOUT_TH (tx_rq enqueue timeout original interrupt watermark register).

interrupt clear

After the CPU receives the send queue interrupt or send timeout interrupt, write 1 to clear the send queue interrupt and send timeout interrupt.

5.4.5 Configure PHY Chip Working Status

The Ethernet switch module provides MDIO interface to manage the PHY chip. MDIO is divided into read operation and write operation, and the operation steps of the two are introduced respectively below.

The configuration steps for the read operation are as follows:

The CPU writes the PHY chip address to bit[12:8] of MDIO_SINGLE_CMD (MDIO single operation register), writes the PHY internal register address to bit[4:0], and configures bit[20] of MDIO_SINGLE_CMD to be 1 at the same time. bit[17:16] is 2'b10, start MDIO read operation; MDIO writes the data read back from the external PHY chip to bit[31:16] of MDIO_SINGLE_DATA (MDIO read and write data register), and simultaneously writes MDIO_SINGLE_CMD (MDIO The bit[20] of the single operation register) is configured as 0; the CPU queries the bit[31:16] of MDIO_SINGLE_DATA (MDIO read and write data register) to get the data read back by MDIO from the external PHY chip.

The configuration steps for writing operations are as follows:

The CPU writes the data sent to the external PHY chip to bit[15:0] of MDIO_SINGLE_DATA (MDIO read and write data register);

Write the PHY chip address to bit[9:8] of MDIO_SINGLE_CMD (MDIO single operation register), write the PHY internal register address to bit[4:0], and configure bit[20] to 1, and configure bit[17: 16] is 1, start MDIO write operation;

MDIO writes the value of bit[15:0] of MDIO_SINGLE_DATA (MDIO read and write data register) into the corresponding PHY internal register, completes the MDIO write operation, and automatically configures MDIO_SINGLE_CMD (MDIO single operation register) bit[20] is 0x0.

5.4.6 Working Mode Switching

The working mode supported by the Ethernet switching module: RMII (10M/100M) RGMII (10M/100M/1000M), and supports switching between modes. The operation steps are described below.

Step 1. Configure the corresponding PERI_CRG51 (GSF CRG clock reset controller 0x120100CC) to 0xe to reset,

Then configure PERI_CRG59 (GMAC interface control register) [8:0], and finally configure PERI_CRG51 as 0xa to cancel the reset and make the configured working mode take effect;

Step 2. Configure and enable the MODE_CHANGE_EN register; then configure the register PORT_MODE (MAC port rate mode register), and then cancel the enable of the register MODE_CHANGE_EN;

说明

This configuration cannot be performed when the chip is working normally, and it is recommended to configure it during initialization.

----Finish

5.5 Typical applications

5.5.1 Ethernet speed limit function

The Ethernet switching module has the function of limiting the rate of received packets, that is, within a certain period of time, when the number of passing packets exceeds the set maximum number, subsequent packets will be discarded.

The Ethernet switch module divides the packet rate limit into the following three types:

Rate limit for control packets

Rate limit for service packets

Rate limiting for broadcast or multicast packets

Limiting the rate of control packets

There are two types of speed limit for control packets:

Within a speed limit time T, only the control packets whose number is less than or equal to the speed limit packet are allowed to pass, and the control packets exceeding this number will be discarded. The speed limit time T is counted in units of 125μs, and when the count is equal to the number of configured speed limit times, it is a speed limit time unit T.

If the number of receiving addresses in the configuration FIFO of the receiving direction is less than the number of speed-limiting addresses, all received control packets will pass through first. At this time, IP packets will be filtered and discarded, regardless of whether there are IP packets at this time. The speed limit of the file or whether there is traffic reaching the IP speed limit.

To limit the rate of control packets, the following configurations are required:

Configure bit[20] of CONTROL_WORD (control register) to 1 Configure bit[15:0] of FLOW_CTRL_PKG_THRSLD (number of speed limit packets register) Configure bit[7:0] of CRF_FLOW_TIME_THRSLD (number of speed limit time register) Configure CRF_RX_LEFT_NUM (Speed limit receiving address number register)

Rate limit for service packets

This rate limiting function is the same as the first condition of the control packet rate limit. When the second condition of the control packet rate limit is established, all IP packets will be discarded.

When limiting the rate of service packets (such as IP packets), the following configurations are required:

Configure bit[21] of CONTROL_WORD (control register) to 1 Configure bit[31:16] of FLOW_CTRL_PKG_THRSLD (number of speed limit packets register) Configure bit[7:0] of CRF_FLOW_TIME_THRSLD (speed limit time register)

Rate limiting for broadcast or multicast packets

The rate limit time of broadcast or multicast packets is counted in units of 1µs. During the rate limit time, when the number of passing packets reaches the rate limit, subsequent packets will be discarded.

When limiting the rate of broadcast or multicast packets, the following configurations are required:

Configure bit[16] of CONTROL_WORD (control register) to 1. Configure CRF_BM_PKT_THRSLD (number of packets processed by the rate limit for broadcast and multicast messages) Configure CRF_BM_TIME_THRSLD (count register for rate limit time for broadcast and multicast messages)

5.5.2 Wol Wake on LAN

Wake on LAN supports receiving wake-up frame and magic packet wakeup.

Wake_up frame Wake up

Configure filter templates. There are 4 sets of filter templates. Take template 1 as an example.

Configure FILTER_0_BYTE_MASK (the first set of effective byte selection registers). Configure FILTER_COMMAND (the first set of filter template enable registers). Configure FILTER_OFFSET (position offset register for calculating CRC). Configure FILTER0_1_CRC (software expected CRC value register). Configure PMT_CTRL_STAUTS (PMT Control and Status Register) bit[0]=1 to enter power_down mode.

Configure PMT_CTRL_STAUTS (PMT Control and Status Register) bit[2]=1 to enable wake_up frame reception. Exit power_down mode: ÿ If you need to exit power_dowm mode locally, just reset PMT_CTRL_STAUTS (PMT control and status register) bit[0]=0;

ÿWhen receiving a wake-up frame, it will automatically exit the power_down mode, and the network port will be automatically opened at this time

At the same time, the software needs to read the original interrupt register.

Magic packet wake up

To receive Magic packet, configure as follows:

Configure PMT_CTRL_STAUTS (PMT control and status register) bit[0]=1, enter power_down mode; bit[1]=1, enable magic packet reception; exit power_down mode: ÿ If the local needs to

exit power_dowm mode, directly

reset PMT_CTRL_STAUTS (PMT control and status register) bit[0]=0; ÿWhen a magic packet is received, it will automatically exit the power_down mode, and the network port

will automatically open at this time

At the same time, the software needs to read the original interrupt register.

5.6 GSF Register Overview

An overview of the GSF registers is shown in Table 5-3 .

Table 5-3 GSF register overview (base address is 0x1005_0000)

offset address name		describe	page number
0x00000000 STATION_ADDR_LOW Local MAC address register			5-16
0x00000004 STATION_ADDR_HIG H		Local MAC address register	5-16
0x00000008 DUPLEX_SEL_RGMII Half-duplex selection register			5-16
0x0000000C FD_FC_TYPE		Flow Control Frame Type Field Register	5-17
0x00000014 COL_DISTANCE		Single retransmission packet length watermark register	5-17
0x0000001C FC_TX_TIMER		Flow Control Time Parameter Register	5-18
0x00000020 FD_FC_ADDR_LOW flow control frame destination address low 32-bit register 5-18			
0x00000024 FD_FC_ADDR_HIGH Flow control frame destination address high 16-bit register 5-19			
0x00000030 IPG_TX_TIMER		Transmit Interframe Gap Register	5-19
0x00000038 PAUSE_THR		Transmit Flow Control Interframe Gap Register	5-19
0x0000003C MAX_FRM_SIZE		Maximum frame length register	5-20
0x00000040 PORT_MODE		Port Status Register	5-20
0x00000044 PORT_EN		Channel Enable Register	5-21
0x00000048 PAUSE_EN		Flow Control Enable Register	5-22
0x00000050 SHORT_RUNTS_THR Short frame limit register			5-22

offset address name		describe	page number
0x00000054 DROP_UNK_CTL_FRM Unknown Control Frame Drop Enable Register 5-23			
0x00000060 TRANSMIT_CONTROL common configuration register			5-23
0x00000064 REC_FILT_CONTROL Receive frame filter control register			5-24
0x00000068 PORT_MC_ADDR_LO	IN	multicast address register	5-25
0x0000006C PORT_MC_ADDR_HIG	H	multicast address register	5-25
0x00000070 MAC_CLR		MAC Clear Register	5-25
0x00000080 RX_OCTETS_OK_CNT RX_OCTETS_TOTAL_OK for receiving		Byte Statistics Register for Valid Frames	5-26
0x00000084 RX_OCTETS_BAD_CN	T	RX_OCTETS_BAD is the receive error frame byte statistics register	5-27
0x00000088 RX_UC_PKTS		MAC Received Unicast Frame Statistics Register 5-27	
0x0000008C RX_MC_PKTS		Receive multicast frame statistics register	5-27
0x00000090 RX_BC_PKTS		Received Broadcast Frame Statistics Register 5-28	
0x00000094 RX_PKTS_64OCTETS Statistics of the number of frames received with a frame length of 64 bytes		register	5-28
0x00000098 RX_PKTS_65TO127OC	TETS	Received frame number statistics register with frame length of 65~127byte	5-28
0x0000009C RX_PKTS_128TO255O	CTETS	Received frame number statistics register with frame length of 128~255byte	5-29
0x000000A0 RX_PKTS_255TO511O	CTETS	Received frame number statistics register with frame length of 256~511byte	5-29
0x000000A4 RX_PKTS_512TO1023O	CTETS	Received frame number statistics register with frame length of 512~1023byte	5-29
0x000000A8 RX_PKTS_1024TO1518	OCTETS	Frame statistics register with received frame length of 1024~1518byte	5-30
0x000000AC RX_PKTS_1519TOMA	XOCTETS	Received frame number statistics register with a frame length of 1519 to the maximum byte	5-30
0x000000B0 RX_FCS_ERRORS Received CRC check error frame number statistics sent		memory	5-30
0x000000B4 RX_TAGGED		Receive TAG Frame Statistics Register 5-31	
0x000000B8 RX_DATA_ERR		Receive Data Error Frame Statistics Register 5-31	

offset address name		describe	page number
0x000000BC RX_ALIGN_ERRORS		Receive data non-byte alignment error frame statistics register	5-31
0x000000C0 RX_LONG_ERRORS		Received frame number statistics register whose frame length is greater than the allowed maximum length	5-32
0x000000C4 RX_JABBER_ERRORS		Receive frame number statistics register whose frame length is greater than the allowed maximum length	5-32
0x000000C8 RX_PAUSE_MACCON	TROL_FRAMCOUNTE R	Received flow control frame number statistics register	5-33
0x000000CC RX_UNKNOWN_MAC	CONTROL_FRAMCOU NTER	Statistic register of the number of non-flow control control frames received by MAC	5-33
0x000000D0 RX_VERY_LONG_ERR	_CNT	received jumbo frame statistics register	5-33
0x000000D4 RX_RUNT_ERR_CNT		Received frame count register with frame length less than 64byte but greater than or equal to 12byte	5-34
0x000000D8 RX_SHORT_ERR_CNT		The statistics of the number of frames received with a frame length less than 96 bits memory	5-34
0x00000100 OCTETS_TRANSMITT	ED_OK	Statistical Register of Bytes of Good Packets Sent Successfully	5-34
0x00000104 OCTETS_TRANSMITT	ED_BAD	Statistical Register of Bytes of Bad Packets Sent Successfully	5-35
0x00000108 TX_UC_PKTS		Sent unicast frame statistics register 5-35	
0x0000010C TX_MC_PKTS		Sent Multicast Frame Statistics Register 5-36	
0x00000110 TX_BC_PKTS		Sent Broadcast Frame Statistics Register 5-36	
0x00000114 TX_PKTS_64OCTETS		64byte sending frame statistics memory	5-36
0x00000118 TX_PKTS_65TO127OC	TETS	Frame statistics register with sending frame length of 65~127byte	5-37
0x0000011C TX_PKTS_128TO255O	CTETS	Frame statistics register with sending frame length of 128~255byte	5-37
0x00000120 TX_PKTS_255TO511O	CTETS	Frame statistics register with sending frame length of 256~511byte	5-37
0x00000124 TX_PKTS_512TO1023O	CTETS	Send frame number statistics register with a frame length of 512-1023 bytes	5-38

offset address name	describe	page number
0x00000128 TX_PKTS_1024TO1518 OCTETS	Frame statistics register with sending frame length of 1024~1518byte	5-38
0x0000012C TX_PKTS_1519TOMAX OCTETS	Send frame number statistics register with frame length greater than 1519byte	5-38
0x00000144 TX_EXC_COL_ERR_C NT	TX_EXC_COL_ERR_CNT The packet counter that reached the maximum number of retransmissions	5-39
0x0000014C TX_EXCESSIVE_LENG TH_DROP	Statistics register for the number of sending failures caused by exceeding the set maximum frame length	5-39
0x00000150 TX_UNDERRUN	Statistics register for the number of failed transmissions due to internal errors during frame transmission	5-40
0x00000154 TX_TAGGED	Sent VLAN frame statistics register 5-40	
0x00000158 TX_CRC_ERROR	Send frame length correct CRC wrong frame count register	5-40
0x0000015C TX_PAUSE_FRAMES Transmitting PAUSE frame statistics register 5-41		
0x000001A8 LINE_LOOP_BACK MAC line side loopback register		5-41
0x000001B0 CF_CRC_STRIP	CRC Stripping Enable Register	5-41
0x000001B4 MODE_CHANGE_EN Port mode change enable register		5-42
0x000001C0 COL_SLOT_TIME Half-duplex collision retransmission interval time counter register		5-43
0x000001DC LOOP_REG	Loopback Supplementary Register	5-43
0x000001E0 RECV_CONTROL Receive control register		5-44
0x000001E8 VLAN_CODE	VLAN Code Register	5-44
0x000001EC RX_OVERRUN_CNT FIFO overflow statistics register		5-45
0x000001F4 RX_LENGTHFIELD_E RR_CNT	Contains PAD frame statistics register	5-45
0x000001F8 RX_FAIL_COMMA_CN T	Byte Delimited COMMA Statistics Register 5-45	
0x00000200 MAC_SA_ADDR_L Source MAC address register		5-46
0x00000204 MAC_SA_ADDR_H Source MAC address register		5-46
0x00000208 MAC_DA_ADDR_L destination MAC address register		5-46
0x0000020C MAC_DA_ADDR_H destination MAC address register		5-47
0x00000210 CRF_MIN_PACKET minimum filter packet length register		5-47

offset address name		describe	page number
0x00000214 CONTROL_WORD Control Register			5-48
0x00000218 FLOW_CTRL_PKG_TH RSLD		Speed limit packet number register	5-49
0x0000021C CRF_FLOW_TIME_TH RSLD		Speed limit time register	5-50
0x00000220+ 4*m	FILTER_LISTm(m=0~1 5)	filter list register	5-50
0x00000260 CRF_UDP_NO		UDP port number register	5-51
0x00000264 CRF_TX_FIFO_THRSL D		Transmit FIFO watermark register	5-52
0x00000268 CRF_RX_FIFO_THRSL D		Receive FIFO Watermark Register	5-52
0x00000280 ERR_GIVEN_PKG_CN T		Statistical counter of packets dropped due to MAC tagging wrong end of frame	5-53
0x00000284 SHORT_ERR_PKT_CN T		Short Error Packet Counter Register	5-53
0x00000288 ERR_FRM_TYPE_CNT Statistics counter register of packets discarded because the frame type is not in the filtering list			5-54
0x0000028C ERR_IP_TYPE_CNT Statistics counter register of packets discarded because the IP type is not in the filtering list			5-54
0x00000290 ERR_UDP_CNT		Filtered packet statistics counter register because UDP port number is not within the set range	5-54
0x00000294 OVER_FLOW_CNT Statistics counter register for packets dropped due to receive FIFO full			5-55
0x00000298 OVER_LENGTH_CNT Statistics counter register for dropped packets due to exceeding the maximum length of the PMU			5-55
0x000002A4 RX_PAUSE_EN		rx direction flow control frame enable register	5-55
0x000002A8 CRF_CFF_DATA_NUM Configure FIFO data number register			5-56
0x000002AC FLOW_OUT_IP_CNT Statistical counter of packets discarded by IP packet rate limit register			5-57
0x000002B0 FLOW_OUT_CTRL_CN T		Packet statistics counter register for control packet rate limit discarding	5-57
0x00000340 CRF_TX_PAUSE		Transmit flow control register	5-57
0x00000344 CRF_RX_LEFT_NUM CRF_RX_ADDR_NUM is the speed limit receiving address number register			5-58

offset address name		describe	page number
0x00000348 CRF_CTRL_0_TYPE Control message type 0 register			5-58
0x0000034C CRF_CTRL_1_TYPE Control message type 1 register			5-59
0x00000350 CRF_CTRL_2_TYPE Control message type 2 register			5-59
0x00000354 CRF_CTRL_3_TYPE Control message type 3 register			5-60
0x00000358 CRF_BM_PKT_THRSL	D	Rate limit processing packet count register for broadcast and multicast packets	5-60
0x0000035C CRF_BM_TIME_THRS	LD	Rate Limit Time Count Register for Broadcast and Multicast Messages	5-60
0x000003C0 MDIO_SINGLE_CMD MDIO single operation register			5-61
0x000003C4 MDIO_SINGLE_DATA MDIO read and write data register			5-62
0x000003CC MDIO_CTL		MDIO Control Register	5-62
0x000003D0 MDIO_RDATA_STATUS	S	MDIO read data status register	5-63
0x00000500 RX_FQ_START_ADDR Free description subqueue start address register 5-63			
0x00000504 RX_FQ_DEPTH		Idle Descriptor Queue Depth Register	5-64
0x00000508 RX_FQ_WR_ADDR Idle Descriptor Subqueue Write Address Register 5-64			
0x0000050C RX_FQ_RD_ADDR Free descriptor subqueue read address register 5-65			
0x00000510 RX_FQ_VLDDESC_CN	T	Idle Descriptor Queue Valid Descriptor Number Register	5-65
0x00000514 RX_FQ_ALRMPTY_TH The idle descriptor queue is almost empty and the waterline is registered		device	5-66
0x00000518 RX_FQ_REG_EN		Enable registers associated with receive direction idle descriptor subqueues	5-66
0x0000051C RX_FQ_ALFULL_TH The idle descriptor queue is almost full and the waterline is registered		device	5-67
0x00000520 RX_BQ_START_ADDR rx_buff describes subqueue start address registration		device	5-67
0x00000524 RX_BQ_DEPTH		rx_buff describes the subqueue depth register 5-68	
0x00000528 RX_BQ_WR_ADDR		rx_buff describes subqueue write address register 5-68	
0x0000052C RX_BQ_RD_ADDR		rx_buff describes subqueue read address register 5-68	

offset address name		describe	page number
0x00000530 RX_BQ_	FREE_DESC_C NT	rx_buff Descriptor number register that can be written by the subqueue	5-69
0x00000534 RX_BQ_	ALEMPTY_TH	The rx_buff description subqueue is almost empty memory	5-69
0x00000538 RX_BQ_	REG_EN	The enable register related to the buff description subqueue in the receiving direction	5-70
0x0000053C RX_BQ_	ALFULL_TH	The rx_buff description subqueue is almost full memory	5-70
0x00000580 TX_BQ_	START_ADDR	tx_buff describes the subqueue start address register device	5-71
0x00000584 TX_BQ_	DEPTH	tx_buff Descriptor Subqueue Depth Register 5-71	
0x00000588 TX_BQ_	WR_ADDR	tx_buff describes subqueue write address register 5-72	
0x0000058C TX_BQ_	RD_ADDR	tx_buff describes subqueue read address register 5-72	
0x00000590 TX_BQ_	VLDDESC_CN T	tx_buff description subqueue effective description sub-number register	5-72
0x00000594 TX_BQ_	ALEMPTY_TH	tx_buff descriptor queue is almost empty memory	5-73
0x00000598 TX_BQ_	REG_EN	The enable register related to the send direction buff description subqueue	5-73
0x0000059C BQ1_	ALFULL_TH	The buff1 descriptor queue is almost full of watermark registers	5-74
0x000005A0 TX_RQ_	START_ADDR	tx_rq Describe subqueue start address register 5-75	
0x000005A4 TX_RQ_	DEPTH	tx_rq Descriptor Subqueue Depth Register 5-75	
0x000005A8 TX_RQ_	WR_ADDR	tx_rq Description Subqueue Write Address Register 5-75	
0x000005AC TX_RQ_	RD_ADDR	tx_rq Descriptor Subqueue Read Address Register 5-76	
0x000005B0 TX_RQ_	FREE_DESC_C NT	tx_rq descriptor number register that can be written by the descriptor queue	5-76
0x000005B4 TX_RQ_	ALEMPTY_TH	tx_rq descriptor queue almost empty waterline register device	5-77
0x000005B8 TX_RQ_	REG_EN	Enable registers associated with tx_rq descriptor queues	5-77
0x000005BC TX_RQ_	ALFULL_TH	tx_rq descriptor queue is almost full waterline register device	5-78
0x000005C0 RAW_	PMU_INT	PMU Module Raw Interrupt Status Register 5-78	

offset address name	describe	page number
0x000005C4 ENA_PMU_INT	PMU Module Raw Interrupt Enable Register 5-82	
0x000005C8 STATUS_PMU_INT PMU module interrupt status register		5-85
0x000005CC DESC_WR_RD_ENA cff Read and write descriptor enable register		5-89
0x000005D8 IN_QUEUE_TH	rx_bq, tx_rq enqueue interrupt watermark register 5-90	
0x000005DC OUT_QUEUE_TH	rx_fq, tx_bq dequeue interrupt watermark register 5-90	
0x000005E0 RX_BQ_IN_TIMEOUT_TH	rx_bq enqueue timeout raw interrupt watermark register	5-91
0x000005E4 TX_RQ_IN_TIMEOUT_TH	tx_rq enqueue timeout raw interrupt watermark register	5-91
0x000005E8 STOP_CMD	Stop receiving and sending packets control register Register 5-92	
0x000005EC FLUSH_CMD	Recycling Descriptor Enable Register	5-92
0x00000800 U_EEE_INTR_SRC	rx and tx direction lpi status register 5-93	
0x00000804 U_EEE_INTR_EN	rx and tx direction interrupt mask and enable registers	5-94
0x00000808 U_EEE_ENABLE	EEE Module Enable Signal Register	5-96
0x0000080C U_EEE_TIMER	LPI Time Counter Register	5-97
0x00000810 U_EEE_LINK_STATUS EEE status register		5-97
0x00000814 U_EEE_TIME_CLK_CNT	Watch Pulse Count Register	5-98
0x00000A00 PMT_CTRL_STAUTS PMT control and status register		5-98
0x00000A04 FILTER_0_BYTE_MASK	PMT 0th effective byte selection register 5-100	
0x00000A08 FILTER_1_BYTE_MASK	PMT 1st effective byte selection register 5-100	
0x00000A0C FILTER_2_BYTE_MASK	PMT 2nd effective byte selection register 5-100	
0x00000A10 FILTER_3_BYTE_MASK	PMT 3rd effective byte selection register 5-101	
0x00000A14 FILTER_COMMAND PMT Template Selection and Multicast Enable Register 5-101		
0x00000A18 FILTER_OFFSET Calculate CRC position offset register 5-103		
0x00000A1C FILTER0_1_CRC	Software expects CRC values 0 and 1 Register 5-103	
0x00000A20 FILTER2_3_CRC	Software expects CRC values 2 and 3 Register 5-104	

5.7 GSF Register Description

STATION_ADDR_LOW

STATION_ADDR_LOW is the local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000000	STATION_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	station_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	station_addr_low	MAC_CORE MAC source address low 32bit.

STATION_ADDR_HIGH

STATION_ADDR_HIGH is the local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000004	STATION_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																station_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	station_addr_high	MAC_CORE MAC source address high 16bit, can be default.

DUPLEX_SEL_RGMII

DUPLEX_SEL_RGMII is a half-duplex selection register.

Offset Address	Register Name	Total Reset Value
0x00000008	DUPLEX_SEL_RGMII	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	duplex_sel_rgmii	Half-duplex select signal. 0: full duplex; 1: half duplex.

FD_FC_TYPE

FD_FC_TYPE is the field register of flow control frame type.

Offset Address	Register Name	Total Reset Value
0x0000000C	FD_FC_TYPE	0x0000_8808

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fd_fc_type
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	fd_fc_type	TYPE field of flow control frame in full-duplex mode.

COL_DISTANCE

COL_DISTANCE is a single retransmission packet length watermark register.

Offset Address	Register Name	Total Reset Value
0x00000014	COL_DISTANCE	0x0000_0043

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	col_distance
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 0 0 0 1 1

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	col_distance	The length of a single retransmission packet.

FC_TX_TIMER

FC_TX_TIMER is the flow control time parameter register.

Offset Address	Register Name	Total Reset Value
0x0000001C	FC_TX_TIMER	0x0000_00FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fc_tx_timer
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	fc_tx_timer	Send flow control frame time parameter, with 512bit as the time unit. In 100M mode, it is 128 clock cycles; in Gigabit mode, it is 64 clock cycles.

FD_FC_ADDR_LOW

FD_FC_ADDR_LOW is the destination address register of the flow control frame.

Offset Address	Register Name	Total Reset Value
0x00000020	FD_FC_ADDR_LOW	0xC200_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fd_fc_addr_low	
Reset	1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:0]	RW	fd_fc_addr_low	Flow control frame DA address low 32bit.

FD_FC_ADDR_HIGH

FD_FC_ADDR_HIGH is the destination address register of the flow control frame.

Offset Address	Register Name	Total Reset Value
0x00000024	FD_FC_ADDR_HIGH	0x0000_0180

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fd_fc_addr_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	fd_fc_addr_high	Flow control frame DA address high 16bit.

IPG_TX_TIMER

IPG_TX_TIMER is the transmit frame interval register.

Offset Address	Register Name	Total Reset Value
0x00000030	IPG_TX_TIMER	0x0000_0008

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	ipg_tx_timer
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ipg_tx_timer	transmit frame interval, the unit is byte.

PAUSE_THR

PAUSE_THR is the frame gap register for sending flow control.

Offset Address	Register Name	Total Reset Value
0x00000038	PAUSE_THR	0x0000_002F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	pause_thr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	pause_thr	Flow control frame interval time, if the flow control time is greater than the interval time, MAC will automatically send flow control frame. Take 512bit as the time unit. In 100M mode, it is 128 clock cycles; in Gigabit mode, it is 64 clock cycles.

MAX_FRM_SIZE

MAX_FRM_SIZE is the maximum frame length register.

Offset Address	Register Name	Total Reset Value
0x0000003C	MAX_FRM_SIZE	0x0000_05EE

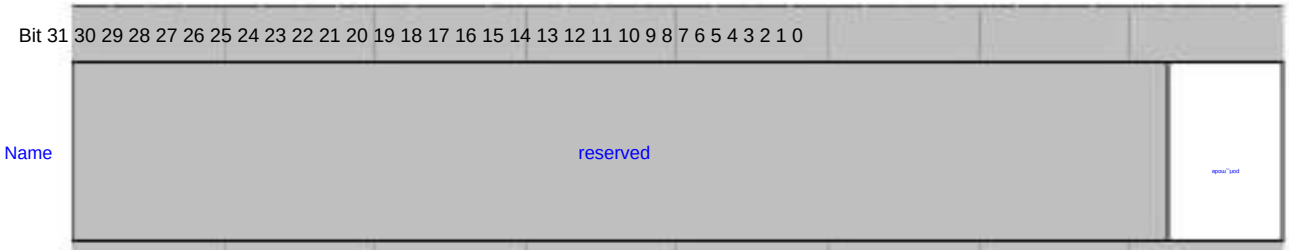
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	max_frm_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	max_frm_size	The maximum frame length allowed in the MAC part. When a frame longer than the frame length is received, the frame is regarded as an oversized error frame; when a frame exceeding the frame length is sent, the sending frame is truncated and sent as an error frame.

PORT_MODE

PORT_MODE is the port status register.

Offset Address	Register Name	Total Reset Value
0x00000040	PORT_MODE	0x0000_0001

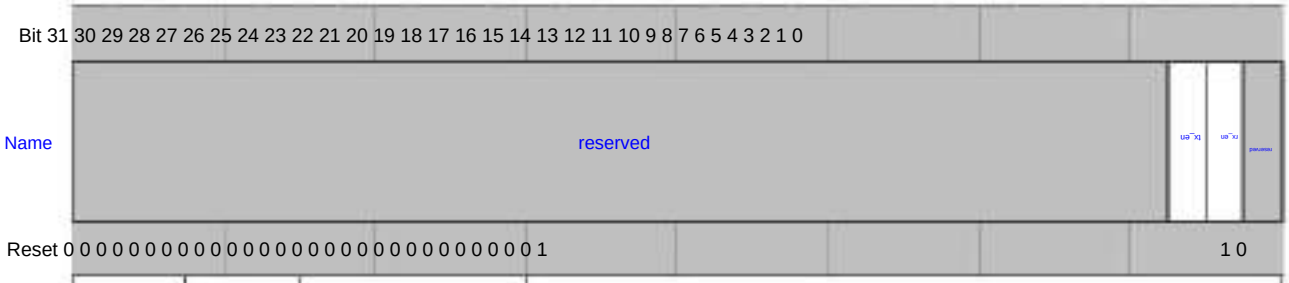


Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	port_mode	Indicates the working mode of the current MAC port. 000ÿ10Mbpsÿ 001ÿ100Mbpsÿ 101: 1000Mbps; Others: Reserved.

PORT_EN

PORT_EN is the channel enable register.

Offset Address	Register Name	Total Reset Value
0x00000044	PORT_EN	0x0000_0006



Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	tx_en	Transmit channel enable bit. 0: disable; 1: enable.
[1]	RW	rx_en	Receive channel enable bit. 0: disable; 1: enable.

[0]	RO	reserved	reserve.

PAUSE_ONE

PAUSE_EN is the flow control enable register.

Offset Address	Register Name	Total Reset Value
0x00000048	PAUSE_ONE	0x0000_0007

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	tx_fdfc	Enable sending flow control frames in full-duplex mode. 0: disable; 1: enable.
[0]	RW	rx_fdfc	Response flow control frame enable in full-duplex mode. 0: Disabled. 1: enable.

SHORT_RUNTS_THR

SHORT_RUNTS_THR is the very short frame limit register.

Offset Address	Register Name	Total Reset Value
0x00000050	SHORT_RUNTS_THR	0x0000_000C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	short_runts_thr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:0]	RW	short_runts_thr	short frame, ultra short frame limit (only for statistics).

DROP_UNK_CTL_FRM

DROP_UNK_CTL_FRM is the unknown control frame drop enable register.

Offset Address	Register Name	Total Reset Value
0x00000054	DROP_UNK_CTL_FRM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	drop_unk_ctl_frm	Unknown control frame processing bit. 0: Forward unknown control frames normally; 1: Discard unknown control frames.

TRANSMIT_CONTROL

TRANSMIT_CONTROL is a common configuration register.

Offset Address	Register Name	Total Reset Value
0x00000060	TRANSMIT_CONTROL	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	pad_enable	Send to add PAD enable. 0: disable; 1: enable.

[6] RW	crc_add		Send Add FCS enable. 0: enable; 1: Disable.
[5:0] RO		reserved	reserve.

REC_FILT_CONTROL

REC_FILT_CONTROL is the receive frame filter control register.

Offset Address	Register Name	Total Reset Value
0x00000064	REC_FILT_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	crc_err_pass	Filter CRC error frame enable. 0: disable; 1: enable.
[4]	RW	pause_frm_pass	Filter flow control frame enable. 0: Disabled, the flow control is enabled only when it is enabled, and it needs to be uploaded to the software; 1: Enable, the flow control is enabled only when it is enabled, and it will not be uploaded to the software.
[3]	RW	vlan_drop_en	Filtering of VLAN frames is enabled. 0: Disable; 1: Enable.
[2]	RW	bc_drop_en	Filter broadcast frames enable. 0: disable; 1: enable.

[1] RW mc_match_en			Filter DA mismatched multicast frames enable. 0: disable; 1: enable.
[0] RW uc_match_en			Filter DA mismatched unicast frames enable. 0: disable; 1: enable.

PORT_MC_ADDR_LOW

PORT_MC_ADDR_LOW is the multicast address register.

Offset Address	Register Name	Total Reset Value
0x00000068	PORT_MC_ADDR_LOW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	port_mc_addr_low
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	port_mc_addr_low	The lower 32 bits of the multicast address, used to judge whether the multicast frame matches.

PORT_MC_ADDR_HIGH

PORT_MC_ADDR_HIGH is the multicast address register.

Offset Address	Register Name	Total Reset Value
0x0000006C	PORT_MC_ADDR_HIGH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / port_mc_addr_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	port_mc_addr_high	Multicast address high 16bit, used to judge whether the multicast frame matches.

MAC_CLR

MAC_CLR is the MAC clear register.

Offset Address	Register Name	Total Reset Value
0x00000070	MAC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	soft_rst_mdio	MDIO clear signal. 0: invalid; 1: Valid.
[2]	RO	reserved	reserve.
[1]	RW	soft_rst_rx	Receive clear signal. 0: invalid; 1: Valid.
[0]	RW	soft_rst_tx	Send a clear signal. 0: invalid; 1: Valid.

RX_OCTETS_OK_CNT

RX_OCTETS_OK_CNT is RX_OCTETS_TOTAL_OK is the byte statistics register for receiving valid frames.

Offset Address	Register Name	Total Reset Value
0x00000080	RX_OCTETS_OK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_ok_cnt	Receive valid frame byte statistics, the range includes DAÿFCS.

RX_OCTETS_BAD_CNT

RX_OCTETS_BAD_CNT is RX_OCTETS_BAD is received error frame byte statistics register.

Offset Address	Register Name	Total Reset Value
0x00000084	RX_OCTETS_BAD_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_octets_bad_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_octets_bad_cnt	receives bad frame byte statistics, including CRC errors, alignment errors, etc.

RX_UC_PKTS

RX_UC_PKTS is the statistics register of MAC received unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000088	RX_UC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_uc_pkts_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_uc_pkts_cnt	Receive statistics of unicast frames (excluding bad frames).

RX_MC_PKTS

RX_MC_PKTS is the statistics register of received multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000008C	RX_MC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_mc_pkts_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_mc_pkts_cnt	received multicast frame statistics (excluding bad frames).

RX_BC_PKTS

RX_BC_PKTS is the statistics register of received broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000090	RX_BC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_bc_pkts_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_bc_pkts_cnt	Receive broadcast frame statistics (excluding bad frames).

RX_PKTS_64OCTETS

RX_PKTS_64OCTETS is the statistics register of the number of received frames with a length of 64 bytes.

Offset Address	Register Name	Total Reset Value
0x00000094	RX_PKTS_64OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pks_64oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pks_64oct_cnt	Receive frame number statistics with a frame length of 64bytes (including bad frames).

RX_PKTS_65TO127OCTETS

RX_PKTS_65TO127OCTETS is the statistics register of the number of received frames with a length of 65 to 127 bytes.

Offset Address	Register Name	Total Reset Value
0x00000098	RX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pks_65to127_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pks_65to127_oc t_cnt	Receive frame number statistics (including bad frames) with a frame length of 65byte to 127byte.

RX_PKTS_128TO255OCTETS

RX_PKTS_128TO255OCTETS is the statistics register of frame number received with frame length of 128~255byte.

Offset Address	Register Name	Total Reset Value
0x0000009C	RX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pkts_128to255_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pkts_128to255_ oct_cnt	Receive frames). frame number statistics with a frame length of 128byte to 255byte (including bad

RX_PKTS_255TO511OCTETS

RX_PKTS_255TO511OCTETS is the statistics register of the number of received frames with a length of 256~511bytes.

Offset Address	Register Name	Total Reset Value
0x000000A0	RX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pkts_256to511_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pkts_256to511_ oct_cnt	Receive frame). frame number statistics with frame length 256byte~511byte (including bad

RX_PKTS_512TO1023OCTETS

RX_PKTS_512TO1023OCTETS is the statistics register of frame number received with frame length of 512~1023byte.

Offset Address	Register Name	Total Reset Value
0x000000A4	RX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pkts_512to1023_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pkts_512to1023 Receive frames). _oct_cnt	frame number statistics with a frame length of 512byte to 1023byte (including bad

RX_PKTS_1024TO1518OCTETS

RX_PKTS_1024TO1518OCTETS is the frame statistics register with the received frame length of 1024~1518byte.

Offset Address	Register Name	Total Reset Value
0x000000A8	RX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pkts_1024to1518_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pkts_1024to151 Receive 1518byte. 8_oct_cnt	frame number statistics (including bad frames) with a frame length of 1024byte to

RX_PKTS_1519TOMAXOCTETS

RX_PKTS_1519TOMAXOCTETS is the statistics register of the number of frames received with frame length from 1519 to the maximum byte.

Offset Address	Register Name	Total Reset Value
0x000000AC	RX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pkts_1519tomax_oct_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pkts_1519tomax frames). _oct_cnt	Receive frame number statistics from 1519byte to maximum byte (including bad

RX_FCS_ERRORS

RX_FCS_ERRORS is the statistics register of received CRC check error frames.

Offset Address	Register Name	Total Reset Value
0x000000B0	RX_FCS_ERRORS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_fcs_errors
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_fcs_errors	CRC detection error frame statistics (excluding short frames).

RX_TAGGED

RX_TAGGED is the statistics register for receiving frame with TAG.

Offset Address	Register Name	Total Reset Value
0x000000B4	RX_TAGGED	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_tagged
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_tagged	Receive frame statistics with TAG.

RX_DATA_ERR

RX_DATA_ERR is the statistical register of received data error frames.

Offset Address	Register Name	Total Reset Value
0x000000B8	RX_DATA_ERR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_data_err
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_data_err	Receive data error frame statistics.

RX_ALIGN_ERRORS

RX_ALIGN_ERRORS is the statistics register for received data non-byte-aligned error frames.

Offset Address	Register Name	Total Reset Value
0x000000BC	RX_ALIGN_ERRORS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_align_errors
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_align_errors	Receive data non-byte alignment error frame statistics.

RX_LONG_ERRORS

RX_LONG_ERRORS is the statistics register for the number of frames whose received frame length is greater than the allowed maximum length.

Offset Address	Register Name	Total Reset Value
0x000000C0	RX_LONG_ERRORS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_long_errors
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_long_errors	The number of frames whose frame length is greater than the allowed maximum length, and the CRC is correct.

RX_JABBER_ERRORS

RX_JABBER_ERRORS is the statistics register of the number of frames whose received frame length is greater than the allowed maximum length.

Offset Address	Register Name	Total Reset Value
0x000000C4	RX_JABBER_ERRORS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_jabber_errors
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_jabber_errors	Statistics of the number of frames whose frame length is greater than the allowed maximum length, CRC error or byte number is not an integer.

RX_PAUSE_MACCONTROL_FRAMECOUNTER

RX_PAUSE_MACCONTROL_FRAMCOUNTER is the statistics register of received flow control frames.

Offset Address	Register Name	Total Reset Value
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_pause_maccontrol_framecounter
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_pause_maccontrol_framecounter	Received flow control frame statistics (when the CRC detection is valid, the CRC must be correct).

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER is the statistical register for the number of non-flow control control frames received by MAC.

Offset Address	Register Name	Total Reset Value
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_unknown_maccontrol_framecounter
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	rx_unknown_maccontrol_framecounter	Statistics of the number of non-flow control control frames received.

RX_VERY_LONG_ERR_CNT

RX_VERY_LONG_ERR_CNT is the statistics register of received very long frame.

Offset Address	Register Name	Total Reset Value
0x000000D0	RX_VERY_LONG_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_very_long_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RC	rx_very_long_err_cnt	Statistics of received very long frames (length greater than twice the maximum frame length).

RX_RUNT_ERR_CNT

RX_RUNT_ERR_CNT is the statistics register of the number of received frames whose length is less than 64byte but greater than or equal to 12byte.

Offset Address	Register Name	Total Reset Value
0x000000D4	RX_RUNT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_runt_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RC	rx_runt_err_cnt	Frame number statistics whose frame length is less than 64byte but greater than or equal to 12byte.

RX_SHORT_ERR_CNT

RX_SHORT_ERR_CNT is the statistics register of the number of received frames whose frame length is less than 96bit.

Offset Address	Register Name	Total Reset Value
0x000000D8	RX_SHORT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_short_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RC	rx_short_err_cnt	Counts the number of frames whose frame length is less than 12byte.

OCTETS_TRANSMITTED_OK

OCTETS_TRANSMITTED_OK is the statistics register of bytes of good packets sent successfully.

Offset Address	Register Name	Total Reset Value
0x00000100	OCTETS_TRANSMITTED_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_ok	The number of bytes of good packets sent successfully (excluding preamble and SFD).

OCTETS_TRANSMITTED_BAD

OCTETS_TRANSMITTED_BAD is the statistics register of bytes of bad packets sent successfully.

Offset Address	Register Name	Total Reset Value
0x00000104	OCTETS_TRANSMITTED_BAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_bad																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_bad	The number of bytes of bad packets sent successfully.

TX_UC_PKTS

TX_UC_PKTS is the statistical register of the number of unicast frames sent.

Offset Address	Register Name	Total Reset Value
0x00000108	TX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_uc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_uc_pkts	Statistics of the number of unicast frames sent (excluding bad packets).

TX_MC_PKTS

TX_MC_PKTS is the statistics register for the number of multicast frames sent.

Offset Address	Register Name	Total Reset Value
0x0000010C	TX_MC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_mc_pkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_mc_pkts	Statistics of the number of multicast frames sent (excluding bad packets).

TX_BC_PKTS

TX_BC_PKTS is the statistics register of broadcast frames sent.

Offset Address	Register Name	Total Reset Value
0x00000110	TX_BC_PKTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_bc_pkts
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_bc_pkts	The number of broadcast frames sent (excluding bad packets).

TX_PKTS_64OCTETS

TX_PKTS_64OCTETS is the statistics register of the number of frames sent with a frame length of 64 bytes.

Offset Address	Register Name	Total Reset Value
0x00000114	TX_PKTS_64OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_64octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_64octets	The number of frames sent with a frame length of 64bytes (including bad packets).

TX_PKTS_65TO127OCTETS

TX_PKTS_65TO127OCTETS is the statistics register of the number of frames sent with a frame length of 65 to 127 bytes.

Offset Address	Register Name	Total Reset Value
0x00000118	TX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_65to127octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	tx_pkts_65to127oct Sendets	frame number statistics (including bad packets) with frame length of 65~127byte.

TX_PKTS_128TO255OCTETS

TX_PKTS_128TO255OCTETS is the statistics register of the number of frames sent with a length of 128 to 255 bytes.

Offset Address	Register Name	Total Reset Value
0x0000011C	TX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_128to255octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	tx_pkts_128to255o Sendctets	frame number statistics (including bad packets) with a frame length of 128-255 bytes.

TX_PKTS_255TO511OCTETS

TX_PKTS_255TO511OCTETS is the statistics register of the number of frames sent with a length of 256 to 511 bytes.

Offset Address	Register Name	Total Reset Value
0x00000120	TX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_256to511octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	tx_pkts_256to511o Sendctets	frame number statistics (including bad packets) with a frame length of 256~511byte.

TX_PKTS_512TO1023OCTETS

TX_PKTS_512TO1023OCTETS is the statistics register of the number of frames sent with a frame length of 512 to 1023 bytes.

Offset Address	Register Name	Total Reset Value
0x00000124	TX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_512to1023octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	tx_pkts_512to1023 Send octets	frame number statistics (including bad packets) with a frame length of 512 to 1023 bytes.

TX_PKTS_1024TO1518OCTETS

TX_PKTS_1024TO1518OCTETS is the statistics register of the number of frames sent with a length of 1024~1518 bytes.

Offset Address	Register Name	Total Reset Value
0x00000128	TX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_1024to1518octets
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	tx_pkts_1024to151 Send 8octets	frame number statistics with a frame length of 1024~1518byte (including bad packets).

TX_PKTS_1519TOMAXOCTETS

TX_PKTS_1519TOMAXOCTETS is the statistical register of the number of frames sent with a frame length greater than 1519 bytes.

Offset Address	Register Name	Total Reset Value
0x0000012C	TX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pkts_1519tomaxoctes
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1519tomax octes	The number of frames (including bad packets) whose frame length is greater than or equal to 1519byte.

TX_EXC_COL_ERR_CNT

TX_EXC_COL_ERR_CNT is the packet counter whose TX_EXC_COL_ERR_CNT reaches the maximum number of retransmissions.

Offset Address	Register Name	Total Reset Value
0x00000144	TX_EXC_COL_ERR_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_exc_col_err_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	tx_exc_col_err_cnt	Counter for packets with maximum number of retransmissions reached.

TX_EXCESSIVE_LENGTH_DROP

TX_EXCESSIVE_LENGTH_DROP is the statistical register for the number of failed transmissions caused by exceeding the set maximum frame length.

Offset Address	Register Name	Total Reset Value
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_excessive_length_drop
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_excessive_length_drop	Counts the number of sending failures due to exceeding the set maximum frame length.

TX_UNDERRUN

TX_UNDERRUN is the statistical register for the number of failed transmissions due to internal errors during frame transmission.

Offset Address	Register Name	Total Reset Value
0x00000150	TX_UNDERRUN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_underrun
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_underrun	counts the number of failed transmissions caused by internal errors during frame transmission.

TX_TAGGED

TX_TAGGED is the statistical register for the number of VLAN frames sent.

Offset Address	Register Name	Total Reset Value
0x00000154	TX_TAGGED	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_tagged
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_tagged	The number of VLAN frames sent, the packets whose Type field is equal to 0x8100.

TX_CRC_ERROR

TX_CRC_ERROR is the counting register of frames with correct CRC error in sending frame length.

Offset Address	Register Name	Total Reset Value
0x00000158	TX_CRC_ERROR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_crc_error
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_crc_error	The statistics of the number of frames with correct frame length and CRC error.

TX_PAUSE_FRAMES

TX_PAUSE_FRAMES is the statistics register of sending PAUSE frames.

Offset Address	Register Name	Total Reset Value
0x0000015C	TX_PAUSE_FRAMES	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_pause_frames
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	tx_pause_frames	The number of pause frames sent.

LINE_LOOP_BACK

LINE_LOOP_BACK is the MAC line side loopback register.

Offset Address	Register Name	Total Reset Value
0x000001A8	LINE_LOOP_BACK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	line_loop_back	MAC line side loopback enable. 0: disable; 1: enable.

CF_CRC_STRIP

CF_CRC_STRIP is the CRC strip enable register.

Offset Address	Register Name	Total Reset Value
0x000001B0	CF_CRC_STRIP	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	cf_crc_strip	MAC stripping receive direction CRC enable. 0: Disabled, the reported packet length includes 4 bytes of CRC; 1: Enable, after stripping, the reported packet length does not include 4 bytes of CRC.

MODE_CHANGE_EN

MODE_CHANGE_EN is the port mode change enable register.

Offset Address	Register Name	Total Reset Value
0x000001B4	MODE_CHANGE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	mode_change_en	port_mode change takes effect enable. 0: disable; 1: enable.

COL_SLOT_TIME

COL_SLOT_TIME is the half-duplex collision retransmission interval counter register.

Offset Address	Register Name	Total Reset Value
0x000001C0	COL_SLOT_TIME	0x0000_40FF

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cf2bc_slottime	cf2bc_random_seed
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:8]	RW	cf2bc_slottime	half-duplex collision retransmission unit interval time.
[7:0]	RW	cf2bc_random_seed	half-duplex collision retransmission random multiple base.

RUN_REG

LOOP_REG is the loopback supplementary register.

Offset Address	Register Name	Total Reset Value
0x000001DC	RUN_REG	0x0000_0002

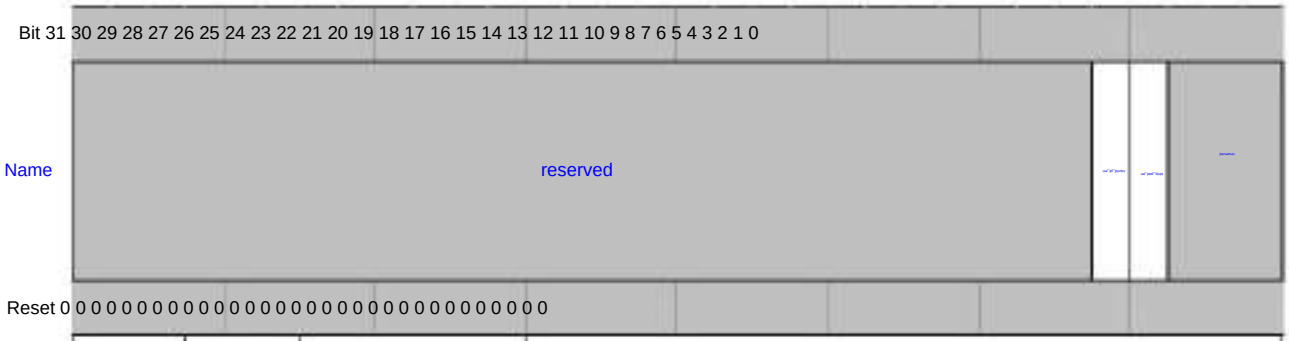
Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	cf_ext_drive_lp	When the line side loops back, the MAC data read and write enable signal is generated. 0: When looping back on the line side, the read and write enable signal of MAC data is generated internally by MAC; 1: When looping back on the line side, the read and write enable signal of MAC data is generated according to the read MAC enable signal of the downlink FIFO.
[0]	RO	reserved	reserve.

RECV_CONTROL

RECV_CONTROL is the receive control register.

Offset Address	Register Name	Total Reset Value
0x000001E0	RECV_CONTROL	0x0000_0000

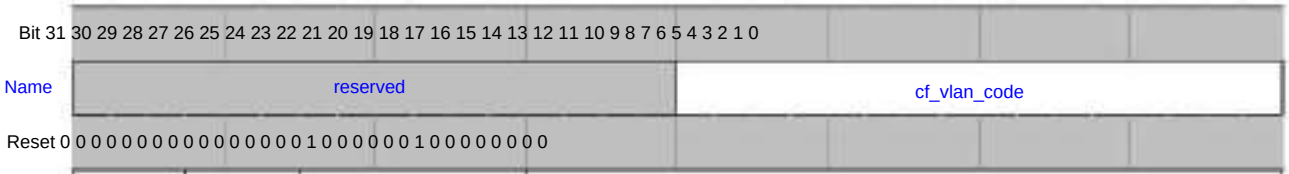


Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	runt_pt_en	Receive ultra-short frame penetration function. 0: Discard, do not upload to the software; 1: Upload to the software.
[3]	RW	strip_path_en	Strips the PAD enable of the received frame. 0: disable; 1: enable.
[2:0]	RO	reserved	reserve.

VLAN_CODE

VLAN_CODE is VLAN Code register.

Offset Address	Register Name	Total Reset Value
0x000001E8	VLAN_CODE	0x0000_8100



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	cf_vlan_code	Ethernet Type domain configuration.

RX_OVERRUN_CNT

RX_OVERRUN_CNT is the FIFO overflow statistics register.

Offset Address	Register Name	Total Reset Value
0x000001EC	RX_OVERRUN_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_overrun_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RC	rx_overrun_cnt MAC application side receive FIFO overflow statistics.

RX_LENGTHFIELD_ERR_CNT

RX_LENGTHFIELD_ERR_CNT is the frame statistics register with PAD.

Offset Address	Register Name	Total Reset Value
0x000001F4	RX_LENGTHFIELD_ERR_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_lengthfield_err_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RC	When MAC stripping PAD is enabled, the frame length of the received frame containing PAD is not equal to the number of 64. cnt rx_lengthfield_err_

RX_FAIL_COMMA_CNT

RX_FAIL_COMMA_CNT is a byte-delimited COMMA statistics register.

Offset Address	Register Name	Total Reset Value
0x000001F8	RX_FAIL_COMMA_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_fail_comma_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RC	The rx_fail_comma_cnt number of two or more comma codes appearing simultaneously during the byte delimitation process.

MAC_SA_ADDR_L

MAC_SA_ADDR_L is the source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000200	MAC_SA_ADDR_L	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mac_sa_addr_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mac_sa_addr_l	The lower 32 bits of the configured local MAC address used by the PMU are used to fill the lower 32 bits of the SA field.

MAC_SA_ADDR_H

MAC_SA_ADDR_H is the source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000204	MAC_SA_ADDR_H	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / mac_sa_addr_h
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	mac_sa_addr_h	High 16 bits of local MAC address used by PMU.

MAC_DA_ADDR_L

MAC_DA_ADDR_L is the destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000208	MAC_DA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_da_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	mac_da_addr_l	The lower 32 bits of the configured destination MAC address used by the PMU are used to fill the lower 32 bits of the DA field.

MAC_DA_ADDR_H

MAC_DA_ADDR_H is the destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x0000020C	MAC_DA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					crf_tx_max_packet											mac_da_addr_h																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	crf_tx_max_packet	The maximum length of normal and sg packets allowed in the PMU.
[15:0]	RW	mac_da_addr_h	The upper 16 bits of the destination MAC address used by the PMU.

CRF_MIN_PACKET

CRF_MIN_PACKET is the minimum filter packet length register.

Offset Address	Register Name	Total Reset Value
0x00000210	CRF_MIN_PACKET	0x0000_0F2A

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	tso_version	reserved	crf_tx_min_packet	crf_rx_min_packet
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	1 1 0 0 1 0 1 0	1 0 1 0

Bits	Access	Name	Description
[31:20]	RO	tso_version	TSO version register: 100: single-byte concatenated version; 200: sg and coe version; 300: tso version. Other: reserved.
[19:14]	RO	reserved	reserve.
[13:8]	RW	crf_tx_min_packet	The minimum sending packet length configured in the sending direction, the default is 15byte.
[7:6]	RO	reserved	reserve.
[5:0]	RW	crf_rx_min_packet	The minimum sending packet length configured in the receiving direction, the default is 42bytes.

CONTROL_WORD

CONTROL_WORD is the control register.

Offset Address	Register Name	Total Reset Value
0x00000214	CONTROL_WORD	0x00C0_0640

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			crf_large_packet
Reset	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	1 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.

[25] RW	crf_tx_standard		The transmit watermark of the transmit FIFO sets the standard. 0: Set by pack and empty waterline. When there is a complete packet in the sending FIFO, or the number of valid data in the sending FIFO is greater than or equal to 4 times the sending waterline, it will send a read request to the MAC; 1: Set by packet; when there is a complete packet in the sending FIFO A read request is sent to the MAC only when the packet is received.
[24:22] RO		reserved	reserve.
[21] RW	crf_ip_flow_ctrl		Enable IP packet rate limit. 0: no speed limit; 1: Speed limit.
[20] RW	crf_ctrl_flow_ctrl		Enable the rate limit of control packets. 0: no speed limit; 1: Speed limit.
[19:18] RO		reserved	reserve.
[17] RW		control. crf_filt_unused_pk filter; g	Filter illegal message 0 do not 1: filter.
[16] RW	crf_bm_flow_ctrl		Control the flow of broadcast or multicast packets. 0: no flow control; 1: flow control.
[15] RW	crf_peel_dsa		Stripped DA/SA controls. 0: no stripping; 1: Peel off.
[14] RW	crf_add_da_sa		Added DA/SA control. 0: do not add; 1: add.
[13:0] RW	crf_large_packet		The maximum packet length configured, the default is 1600byte (the maximum packet length used by the PMU).

FLOW_CTRL_PKG_THRSLD

FLOW_CTRL_PKG_THRSLD is the register for the number of speed limit packets.

Offset Address	Register Name	Total Reset Value
0x00000218	FLOW_CTRL_PKG_THRSLD	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	crf_ip_pkg_thrsld	crf_ctrl_pkg_thrsld
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RW	crf_ip_pkg_thrsld	The upper limit of IP packets, when the number of IP packets received within T time exceeds this number, the rate will be limited, otherwise, the rate will not be limited.
[15:0]	RW	crf_ctrl_pkg_thrsld, the	The packet upper limit of the control message, when the control message received within T time exceeds the number of rate will be limited, otherwise, the rate will not be limited.

CRF_FLOW_TIME_THRSLD

CRF_FLOW_TIME_THRSLD is the speed limit time register.

Offset Address	Register Name	Total Reset Value
0x0000021C	CRF_FLOW_TIME_THRSLD	0x0000_00FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	crf_flow_time_thrsld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	crf_flow_time_thrsl d	The processing time of the speed limit, the unit is 125ÿs. speed limit time T=(crf_flow_time_thrsld+1)(125ÿs)

FILTER_LISTm

FILTER_LISTm (m=0~15) is the filter list register.

Offset Address	Register Name	Total Reset Value
0x00000220+4*m	FILTER_LISTm	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_filt_frm_type0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:18]	RO	reserved	reserve.
[17]	RW crf_filt_cfg_m		Indicates whether the row has been configured. 0: not configured; 1: Configuration. Only when CFG is 1, the content of this table needs to be parsed, otherwise, the content of this table can be ignored.
[16]	RW crf_filt_id_m		Indicates which type TYPE is. 0: MAC frame type; 1: IP type.
[15:0]	RW	crf_filt_frm_type_ When m	The configured filtering type. ID=0, all 16 bits of TYPE are valid; when ID=1, the lower 8 bits of TYPE are valid, and the upper 8 bits are ignored.

CRF_UDP_NO

CRF_UDP_NO is the UDP port number register.

Offset Address	Register Name	Total Reset Value
0x00000260	CRF_UDP_NO	0xFFFF_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	crf_udp_max_no	reserved
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RW crf_udp_max_no		UDP port number maximum.
[15:0]	RO	reserved	reserve.

CRF_TX_FIFO_THRSLD

CRF_TX_FIFO_THRSLD is the transmit FIFO watermark register.

Offset Address	Register Name	Total Reset Value
0x00000264	CRF_TX_FIFO_THRSLD	0x0271_017C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_tx_p_full_th	reserved	crf_tx_p_empty_th
Reset	0 0 0 0 0 0 1 0 0 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0 1 1 1	1 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	crf_tx_p_full_th	High water mark of transmit FIFO. When the number of valid data in the transmit FIFO is 4 (crf_tx_p_full_th), stop transferring packets from SDRAM. After the watermark is set, it is necessary to keep the reserved space in the sending FIFO to allow receiving a packet with a maximum frame length (set in bit[13:0] of the CONTROL_WORD (control register)), that is, it needs to meet CONTROL_WORD[13:0]<(8192–4(crf_tx_p_full_th)ÿ
[15:11]	RO	reserved	reserve.
[10:0]	RW	crf_tx_p_empty_th	The low watermark of the transmit FIFO. When the number of valid data in the transmit FIFO (4(crf_tx_p_empty_th)), allows to read data from the transmit FIFO. It is recommended that this waterline be set to a minimum of 0x14.

CRF_RX_FIFO_THRSLD

CRF_RX_FIFO_THRSLD is the receive FIFO watermark register.

Offset Address	Register Name	Total Reset Value
0x00000268	CRF_RX_FIFO_THRSLD	0x0E10_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_rx_p_full_th	reserved	crf_rx_p_empty_th
Reset	0 0 0 0 1 1 1 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27:16] RW	crf_rx_p_full_th		The high water mark of the receive FIFO. When the number of valid data in the receive FIFO is 4 (crf_rx_p_full_th), it is not allowed to write new packets into the receive FIFO. After the watermark is set, it is necessary to keep the reserved space in the receiving FIFO to allow receiving a packet with a maximum frame length (set in bit[13:0] of the CONTROL_WORD (control register)), that is, it needs to meet CONTROL_WORD[13:0]<(8192–4(crf_rx_p_full_th)ÿ
[15:12] RO		reserved	reserve.
The [11:0] RW	crf_rx_p_empty_th	watermark needs to be set to at least 0x200.	The low water mark of the receive FIFO. When there is valid data in the receive FIFO ((4(crf_rx_p_empty_th), data is allowed to be read from the receive FIFO.

ERR_GIVEN_PKG_CNT

ERR_GIVEN_PKG_CNT is the statistical counter of packets discarded due to MAC marking wrong frame end.

Offset Address	Register Name	Total Reset Value
0x00000280	ERR_GIVEN_PKG_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_given_pkg_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	err_given_pkg_cnt	Statistical count of packets dropped due to MAC tagging wrong end of frame.

SHORT_ERR_PKT_CNT

SHORT_ERR_PKT_CNT is the short error packet counter register.

Offset Address	Register Name	Total Reset Value
0x00000284	SHORT_ERR_PKT_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	short_err_pkt_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	short_err_pkt_cnt	Short error packet count.

ERR_FRM_TYPE_CNT

ERR_FRM_TYPE_CNT is the statistics counter register of packets discarded because the frame type is not in the filtering list.

Offset Address	Register Name	Total Reset Value
0x00000288	ERR_FRM_TYPE_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_frm_type_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	err_frm_type_cnt	Statistical count of packets discarded because the frame type is not in the filtering list.

ERR_IP_TYPE_CNT

ERR_IP_TYPE_CNT is the statistical counter register of packets discarded because the IP type is not in the filtering list.

Offset Address	Register Name	Total Reset Value
0x0000028C	ERR_IP_TYPE_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_ip_type_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	err_ip_type_cnt	Statistics count of packets discarded because the IP type is not in the filter list.

ERR_UDP_CNT

ERR_UDP_CNT is the packet statistics counter register that is filtered because the UDP port number is not within the set range.

Offset Address	Register Name	Total Reset Value
0x00000290	ERR_UDP_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	err_udp_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	err_udp_cnt	Statistical count of packets filtered because the UDP port number is not within the set range.

OVER_FLOW_CNT

OVER_FLOW_CNT is the statistical counter register for packets discarded due to receive FIFO full.

Offset Address	Register Name	Total Reset Value
0x00000294	OVER_FLOW_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	over_flow_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	over_flow_cnt	Statistical count of packets dropped due to receive FIFO full

OVER_LENGTH_CNT

OVER_LENGTH_CNT is the statistical counter register for discarding packets due to exceeding the maximum length of the PMU.

Offset Address	Register Name	Total Reset Value
0x00000298	OVER_LENGTH_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	over_length_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	over_length_cnt	Statistical count of dropped packets due to exceeding the maximum length of the PMU.

RX_PAUSE_EN

RX_PAUSE_EN is the flow control frame enable register in the rx direction.

Offset Address	Register Name	Total Reset Value
0x000002A4	RX_PAUSE_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	rx_fifo_pause_en	Flow control frame enable for rx_fifo. 0: disable; 1: enable.
[1]	RW	rx_bq_pause_en	Flow control frame enable for rx_bq. 0: disable; 1: enable.
[0]	RW	rx_fq_pause_en	Flow control frame enable for rx_fq. 0: Disable; 1: Enable.

CRF_CFF_DATA_NUM

CRF_CFF_DATA_NUM is the register for configuring FIFO data number.

Offset Address	Register Name	Total Reset Value
0x000002A8	CRF_CFF_DATA_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	crf_rx_cfg_num | crf_tx_cfg_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	crf_rx_cfg_num	The number of valid descriptors remaining in the rx_fq FIFO.
[15:0]	RW	crf_tx_cfg_num	tx_bq FIFO remaining valid descriptor number.

FLOW_OUT_IP_CNT

FLOW_OUT_IP_CNT is the packet statistical counter register for IP packets discarded by rate limit.

Offset Address	Register Name	Total Reset Value
0x000002AC	FLOW_OUT_IP_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flow_out_ip_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	flow_out_ip_cnt The statistics	count of packets discarded by IP packet rate limit.

FLOW_OUT_CTRL_CNT

FLOW_OUT_CTRL_CNT is the packet statistics counter register for rate-limit discarding of control packets.

Offset Address	Register Name	Total Reset Value
0x000002B0	FLOW_OUT_CTRL_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	flow_out_ctrl_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RC	flow_out_ctrl_cnt Control	packet rate limit discarded packet statistics.

CRF_TX_PAUSE

CRF_TX_PAUSE is the transmit flow control register.

Offset Address	Register Name	Total Reset Value
0x00000340	CRF_TX_PAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
receiving [0]	RW crf_tx_pause	_auto FIFO of PMU is	Transmit flow control register, which determines the way of MAC transmit flow control. 0: MAC decides whether to send flow control frame according to the actual flow, when the full or nearly full, MAC will automatically send flow control frame; 1: Force MAC to send flow control frame.

CRF_RX_LEFT_NUM

CRF_RX_LEFT_NUM is CRF_RX_ADDR_NUM is the register for the number of speed-limited receiving addresses.

Offset Address	Register Name	Total Reset Value
0x00000344	CRF_RX_LEFT_NUM	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												crf_rx_left_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access Name		Description
[31:8]	RO	reserved	reserve.
[7:0]	RW crf_rx_left_num		When the number of remaining addresses in the downstream configuration FIFO is less than this number, only control packets will be passed, and all data packets will be discarded (the default setting is 0).

CRF_CTRL_0_TYPE

CRF_CTRL_0_TYPE is the control message type 0 register.

Offset Address	Register Name	Total Reset Value
0x00000348	CRF_CTRL_0_TYPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_ctrl_0_type
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	crf_ctrl_0_type	If the configured control packet type is 0, if the frame type of the received packet is the same as it, the packet is considered to be a control packet.

CRF_CTRL_1_TYPE

CRF_CTRL_1_TYPE is the control message type 1 register.

Offset Address	Register Name	Total Reset Value
0x0000034C	CRF_CTRL_1_TYPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_ctrl_1_type
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	crf_ctrl_1_type	If the configured control packet type 1 is the same as the frame type of the received packet, the packet is considered to be a control packet.

CRF_CTRL_2_TYPE

CRF_CTRL_2_TYPE is the control message type 2 register.

Offset Address	Register Name	Total Reset Value
0x00000350	CRF_CTRL_2_TYPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_ctrl_2_type
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RO		crf_ctrl_2_type	If the configured control packet type 2 is the same as the frame type of the received packet, the packet is considered to be a control packet.

CRF_CTRL_3_TYPE

CRF_CTRL_3_TYPE is the control message type 3 register.

Offset Address	Register Name	Total Reset Value
0x00000354	CRF_CTRL_3_TYPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_ctrl_3_type
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	crf_ctrl_3_type	If the configured control packet type 3 is the same as the frame type of the received packet, the packet is considered to be a control packet.

CRF_BM_PKT_THRSLD

CRF_BM_PKT_THRSLD is the rate limit processing packet number register for broadcast and multicast messages.

Offset Address	Register Name	Total Reset Value
0x00000358	CRF_BM_PKT_THRSLD	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_bm_pkt_thrsld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	crf_bm_pkt_thrsld	The packet upper limit of broadcast and multicast messages, when the broadcast or multicast messages received within the rate limit unit time exceeds this number, the rate will be limited, otherwise, the rate will not be limited.

CRF_BM_TIME_THRSLD

CRF_BM_TIME_THRSLD is the rate limit time count register for broadcast and multicast messages.

Offset Address	Register Name	Total Reset Value
0x0000035C	CRF_BM_TIME_THRSLD	0x0000_2710

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	crf_bm_time_thrsld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	crf_bm_time_thrsld	The upper limit of the speed limit time of broadcast and multicast messages is counted in units of 1us. When equal to the count value, it is a speed limit unit time.

MDIO_SINGLE_CMD

MDIO_SINGLE_CMD is the MDIO single operation register.

Offset Address	Register Name	Total Reset Value
0x000003C0	MDIO_SINGLE_CMD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	phy_addr reg_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20]	RW	mdio_cmd	MDIO operation complete indication. 0: MDIO operation completed; 1: Initiate MDIO operation.
[19:18]	RO	reserved	reserve.
[17:16]	RW	op_code	MDIO operation type. 00: reserved; 01: write operation; 10: read operation; 11: Reserved.
[15:13]	RO	reserved	reserve.
[12:8]	RW	phy_addr	Configure 5 bits of the external PHY address.

[7:5] RO		reserved	reserve.
[4:0] RW reg_addr			Register address inside the PHY device.

MDIO_SINGLE_DATA

MDIO_SINGLE_DATA is the MDIO read and write data register.

Offset Address	Register Name	Total Reset Value
0x000003C4	MDIO_SINGLE_DATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mid_rd_data	mid_wr_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16] RO		mdio_rd_data	MDIO data read back from external PHY device.
[15:0] RW	mdio_wr_data	MDIO write data.	

MEDIUM_CTL

MDIO_CTL is the MDIO control register.

Offset Address	Register Name	Total Reset Value
0x000003CC	MEDIUM_CTL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

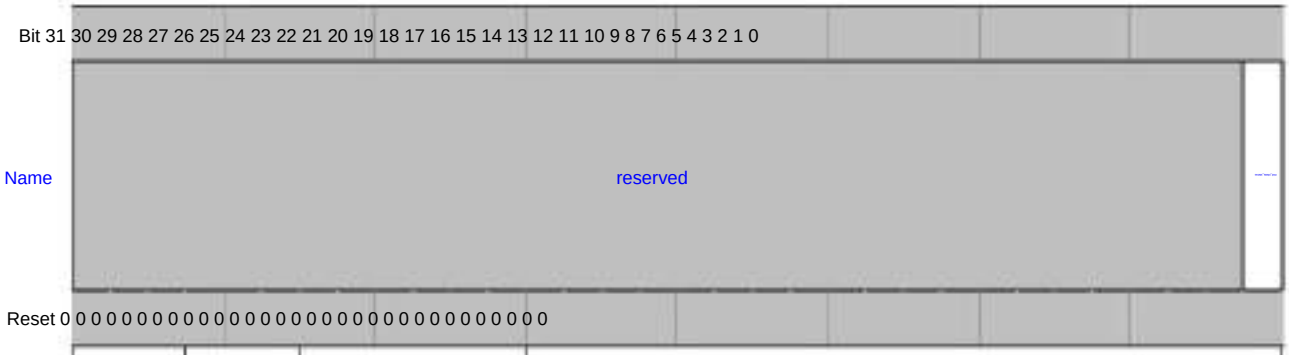
Bits	Access Name		Description
[31:4] RO		reserved	reserve.
[3]	RO	mdio_in_work	MDIO single operation execution flag bit. 0: MDIO single operation is not executed; 1: MDIO single operation is in progress.

[2] RW	mdio_in_work_en		MDIO_IN_WORK bit valid indication. 0: MDIO_IN_WORK bit is invalid; 1: MDIO_IN_WORK bit is valid.
[1] RW	autoscan_en		The auto-detect function is enabled. 0: Disable automatic detection function; 1: Enable auto-detect function. (Controlling the automatic scan enablement of all PHY addresses, currently there is only one PHY, so it can be configured as 1 and unchanged)
[0] RW	mdc_speed		MDIO interface clock frequency configuration. 0: MDIO interface clock frequency is 2.5MHz; 1: MDIO interface clock frequency is 18MHz.

AVERAGE_RDATA_STATUS

MDIO_RDATA_STATUS is the MDIO read data status register.

Offset Address	Register Name	Total Reset Value
0x000003D0	AVERAGE_RDATA_STATUS	0x0000_0000



Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RC	mid_rdata_status	Whether the MDIO read data is valid. 0: MDIO read data is valid; 1: MDIO read data is invalid.

RX_FQ_START_ADDR

RX_FQ_START_ADDR is the start address register of the free description subqueue.

Offset Address	Register Name	Total Reset Value
0x00000500	RX_FQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fq_start_addr	The start address of the idle description subqueue, when the rx_fq_start_addr_en in the RX_FQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and only Word address is supported.

RX_FQ_DEPTH

RX_FQ_DEPTH is the free description sub-queue depth register.

Offset Address	Register Name	Total Reset Value
0x00000504	RX_FQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														fq_depth	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:0]	RW	fq_depth	The depth of the idle descriptor queue in the receiving direction (the number of words, the number of non-descriptors), when the rx_fq_depth_en in the RX_FQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and the depth needs to be set to Integer multiples of 8. It is recommended to configure at least 0x400.

RX_FQ_WR_ADDR

RX_FQ_WR_ADDR is the free descriptor queue write address register.

Offset Address	Register Name	Total Reset Value
0x00000508	RX_FQ_WR_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fq_wr_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	fq_wr_addr	Idle descriptor queue write address in receive direction.

RX_FQ_RD_ADDR

RX_FQ_RD_ADDR is the idle description subqueue read address register.

Offset Address	Register Name	Total Reset Value
0x0000050C	RX_FQ_RD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fq_rd_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	fq_rd_addr	The read address of the idle description subqueue in the receiving direction, when the rx_fq_rd_addr_en in the RX_FQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read.

RX_FQ_VLDDESC_CNT

RX_FQ_VLDDESC_CNT is the valid descriptor number register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000510	RX_FQ_VLDDESC_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fq_vlddesc_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RO		fq_vlddesc_cnt	The number of effective descriptors in the free descriptor queue in the receiving direction.

RX_FQ_ALRMPTY_TH

RX_FQ_ALRMPTY_TH is the almost empty watermark register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000514	RX_FQ_ALRMPTY_TH	0x0010_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fq_pause_low_th	fq_alempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_low_th	rx_fq queue flow control low watermark. When the number of effective descriptors is less than or equal to fq_pause_low_th, an indication signal for sending flow control frames is generated.
[15:0]	RW	fq_alempty_th	The free descriptor queue in the receive direction is almost empty.

RX_FQ_REG_EN

RX_FQ_REG_EN is the enable register related to the idle description subqueue in the receive direction.

Offset Address	Register Name	Total Reset Value
0x00000518	RX_FQ_REG_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	rx_fq_start_addr_en	0: RX_FQ_START_ADDR register, software writable enable. RX_FQ_START_ADDR register is protected, software cannot write; 1: Software can write RX_FQ_START_ADDR.

[1]	RW	rx_fq_depth_en	RX_FQ_DEPTH register, software writable enable. 0: The RX_FQ_DEPTH register is protected and cannot be written by software; 1: The RX_FQ_DEPTH register can be written by software.
[0]	RW	rx_fq_rd_addr_en	RX_FQ Read address register, software writable enable. 0: The read address register of RX_FQ is protected and cannot be written by software; 1: The read address register of RX_FQ can be written by software.

RX_FQ_ALFULL_TH

RX_FQ_ALFULL_TH is the almost full watermark register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000051C	RX_FQ_ALFULL_TH	0x0010_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fq_pause_hi_th	fq_alfull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_hi_th	rx_fq queue flow control high watermark. When the number of valid descriptors is greater than or equal to fq_pause_hi_th, the indication signal for sending flow control frames is set to 0, indicating that the TX direction stops sending flow control frames.
[15:0]	RW	fq_alfull_th	In the receiving direction, the idle descriptor queue is almost full.

RX_BQ_START_ADDR

RX_BQ_START_ADDR describes the subqueue start address register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x00000520	RX_BQ_START_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_bq_start_addr	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	rx_bq_start_addr	The buff in the receiving direction describes the start address of the subqueue. When rx_bq_start_addr_en in the RX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and only Word address is supported.

RX_BQ_DEPTH

RX_BQ_DEPTH Describes the subqueue depth register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x00000524	RX_BQ_DEPTH	0x0000_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_bq_depth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:0]	RW	rx_bq_depth	The buff in the receiving direction describes the depth of the subqueue (the number of words, the number of non-descriptors). When rx_bq_depth_en in the RX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and the depth is set to 8 Integer multiples of . It is recommended to configure at least 0x400.

RX_BQ_WR_ADDR

RX_BQ_WR_ADDR describes the subqueue write address register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x00000528	RX_BQ_WR_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_bq_wr_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	rx_bq_wr_addr	The buff in the receiving direction describes the write address of the subqueue. When rx_bq_wr_addr_en in the RX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read.

RX_BQ_RD_ADDR

RX_BQ_RD_ADDR describes the subqueue read address register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x0000052C	RX_BQ_RD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_bq_rd_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	rx_bq_rd_addr	The buff description subqueue read address in the receiving direction.

RX_BQ_FREE_DESC_CNT

RX_BQ_FREE_DESC_CNT is the writable descriptor number register of the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000530	RX_BQ_FREE_DESC_CNT	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_bq_free_desc_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rx_bq_free_desc_cnt	The number of descriptors that can be written in the buff descriptor queue in the receiving direction.

RX_BQ_ALEMPTY_TH

RX_BQ_ALEMPTY_TH describes the subqueue almost empty watermark register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x00000534	RX_BQ_ALEMPTY_TH	0x0010_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_bq_pause_low_th	rx_bq_alempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_low_th	The number of writable descriptors is less than or equal to rx_bq queue flow control low watermark. When the number of writable descriptors is less than rx_bq_pause_low_th, an indication signal for sending flow control frames is generated.

[15:0] RW	rx_bq_alempty_th	Receive direction buff descriptor subqueue almost empty waterline.	

RX_BQ_REG_EN

RX_BQ_REG_EN is the enable register related to the receiving direction buff description subqueue.

Offset Address	Register Name	Total Reset Value
0x00000538	RX_BQ_REG_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	rx_bq_start_addr_en	RX_BQ_START_ADDR register, software writable enable. 0: The RX_BQ_START_ADDR register is protected and cannot be written by software; 1: The RX_BQ_START_ADDR can be written by software.
[1]	RW	rx_bq_depth_en	RX_BQ_DEPTH register, software writable enable. 0: The RX_BQ_DEPTH register is protected and cannot be written by software; 1: The RX_BQ_DEPTH register can be written by software.
RW	rx_bq_wr_addr_en	1: Software can write RX_BQ	RX_BQ Write address register, software can write enable. 0: RX_BQ write address register is protected, software cannot write; [0] write address register.

RX_BQ_ALFULL_TH

RX_BQ_ALFULL_TH describes the subqueue almost full watermark register for rx_buff.

Offset Address	Register Name	Total Reset Value
0x0000053C	RX_BQ_ALFULL_TH	0x0010_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_bq_pause_hi_th	rx_bq_alfull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_hi_th	rx_bq queue flow control high watermark. When the number of writable descriptors is greater than or equal to bq_pause_hi_th, the indication signal for sending flow control frames is set to 0, indicating that the TX side direction stops sending flow control frames.
[15:0]	RW	rx_bq_alfull_th	Receive direction, the buff descriptor queue is almost full.

TX_BQ_START_ADDR

TX_BQ_START_ADDR describes the subqueue start address register for tx_buff.

Offset Address	Register Name	Total Reset Value
0x00000580	TX_BQ_START_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_bq_start_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	tx_bq_start_addr	The buff in the sending direction describes the start address of the subqueue. When tx_bq_start_addr_en in the TX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and only Word address is supported.

TX_BQ_DEPTH

TX_BQ_DEPTH describes the subqueue depth register for tx_buff.

Offset Address	Register Name	Total Reset Value
0x00000584	TX_BQ_DEPTH	0x0000_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved tx_bq_depth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.

[18:0] RW	tx_bq_depth		The buff in the sending direction describes the depth of the subqueue (the number of words, the number of non- descriptors). When tx_bq_depth_en in the TX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and the depth is set to 8 Integer multiples of . It is recommended to configure at least 0x400.

TX_BQ_WR_ADDR

TX_BQ_WR_ADDR describes subqueue write address register for tx_buff.

Offset Address	Register Name	Total Reset Value
0x00000588	TX_BQ_WR_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_bq_wr_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	tx_bq_wr_addr	buff description subqueue write address in send direction.

TX_BQ_RD_ADDR

TX_BQ_RD_ADDR describes the subqueue read address register for tx_buff.

Offset Address	Register Name	Total Reset Value
0x0000058C	TX_BQ_RD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_bq_rd_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	tx_bq_rd_addr	The buff in the sending direction describes the read address of the subqueue. When tx_bq_rd_addr_en in the TX_BQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read.

TX_BQ_VLDDESC_CNT

TX_BQ_VLDDESC_CNT is the valid descriptor number register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000590	TX_BQ_VLDDESC_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_bq_vlddesc_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	tx_bq_vlddesc_cnt	The effective descriptor number of buff descriptor queue in the sending direction.

TX_BQ_ALEMPTY_TH

TX_BQ_ALEMPTY_TH describes the subqueue almost empty watermark register for tx_buff.

Offset Address	Register Name	Total Reset Value
0x00000594	TX_BQ_ALEMPTY_TH	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_bq_alempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	tx_bq_alempty_th	The buff descriptor subqueue in the send direction is almost empty.

TX_BQ_REG_EN

TX_BQ_REG_EN is the enable register related to the buff description subqueue in the sending direction.

Offset Address	Register Name	Total Reset Value
0x00000598	TX_BQ_REG_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	tx_bq_start_addr_en	0: TX_BQ_START_ADDR register, software writable enable. TX_BQ_START_ADDR register is protected and cannot be written by software; 1: TX_BQ_START_ADDR can be written by software.
[1]	RW	tx_bq_depth_en	TX_BQ_DEPTH register, software writable enable. 0: The TX_BQ_DEPTH register is protected and cannot be written by software; 1: The TX_BQ_DEPTH register can be written by software.
[0]	RW	tx_bq_rd_addr_en	TX_BQ Read address register, software can write enable. 0: The read address register of TX_BQ is protected and cannot be written by software; 1: The read address register of TX_BQ can be written by software.

BQ1_ALFULL_TH

BQ1_ALFULL_TH describes the subqueue almost full watermark register for buff1.

Offset Address	Register Name	Total Reset Value
0x0000059C	BQ1_ALFULL_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved bq1_alfull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	bq1_alfull_th	send direction, buff1 description subqueue is almost full waterline.

TX_RQ_START_ADDR

TX_RQ_START_ADDR describes the subqueue start address register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005A0	TX_RQ_START_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_rq_start_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0]	RW tx_rq_start_addr	The start address of the reclaim description subqueue in the sending direction, when tx_rq_start_addr_en in the TX_RQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read, and only Word address is supported.

TX_RQ_DEPTH

TX_RQ_DEPTH Describes the subqueue depth register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005A4	TX_RQ_DEPTH	0x0000_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / tx_rq_depth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:19]	RO reserved	reserve.
[18:0]	RW tx_rq_depth	The depth of the recovery descriptor queue in the sending direction (the number of words, the number of non-descriptors), when the tx_rq_depth_en in the TX_RQ_REG_EN register is 1, it can be read and written; when the configuration is 0, it can only be read, and the depth is set to 8 Integer multiples of . It is recommended to configure at least 0x400.

TX_RQ_WR_ADDR

TX_RQ_WR_ADDR Describes the subqueue write address register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005A8	TX_RQ_WR_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_wr_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	tx_rq_wr_addr	Recycling description subqueue write address in sending direction, when tx_rq_wr_addr_en in the TX_RQ_REG_EN register is 1, it can be read and written; when it is configured as 0, it can only be read.

TX_RQ_RD_ADDR

TX_RQ_RD_ADDR describes the subqueue read address register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005AC	TX_RQ_RD_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_rd_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:0]	RW	tx_rq_rd_addr	The read address of the reclamation descriptor queue in the sending direction

TX_RQ_FREE_DESC_CNT

TX_RQ_FREE_DESC_CNT is the writable descriptor number register of the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B0	TX_RQ_FREE_DESC_CNT	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_free_desc_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RW		tx_rq_free_desc_cn The number	of descriptors that can be written in the free descriptor queue in the sending direction. t

TX_RQ_ALEMPTY_TH

TX_RQ_ALEMPTY_TH Describes the subqueue almost empty watermark register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005B4	TX_RQ_ALEMPTY_TH	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_alempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15:0] RW	tx_rq_alempty_th	The reclamation descriptor queue for send direction is almost empty.	

TX_RQ_REG_EN

TX_RQ_REG_EN is the enable register related to the tx_rq description subqueue.

Offset Address	Register Name	Total Reset Value
0x000005B8	TX_RQ_REG_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:3] RO		reserved	reserve.
[2] RW		tx_rq_start_addr_e n	0: TX_RQ_START_ADDR register, software writable enable. TX_RQ_START_ADDR register is protected and cannot be written by software; 1: TX_RQ_START_ADDR can be written by software.

[1] RW	tx_rq_depth_en		TX_RQ_DEPTH register, software writable enable. 0: The TX_RQ_DEPTH register is protected and cannot be written by software; 1: The TX_RQ_DEPTH register can be written by software.
RW	tx_rq_wr_addr_en	1: Software can write TX_RQ	TX_RQ Write address register, software can write enable. 0: TX_RQ write address register is protected, software cannot write; [0] write address register.

TX_RQ_ALFULL_TH

TX_RQ_ALFULL_TH Describes the subqueue almost full watermark register for tx_rq.

Offset Address	Register Name	Total Reset Value
0x000005BC	TX_RQ_ALFULL_TH	0x0000_0010

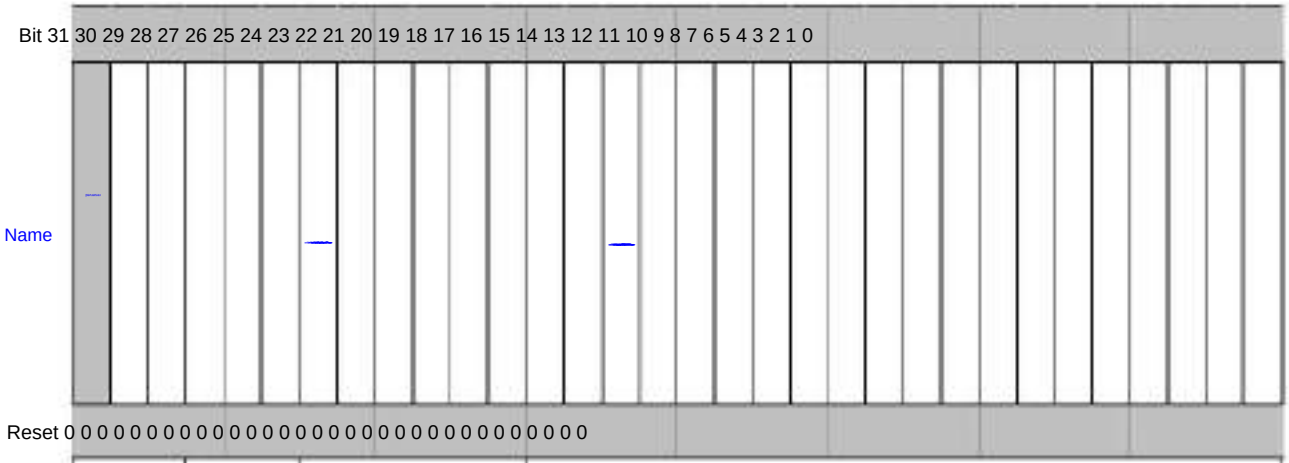
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_alfull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	tx_rq_alfull_th	In the sending direction, the recovery descriptor queue is almost full.

RAW_PMU_INT

RAW_PMU_INT is the raw interrupt status register of the PMU module.

Offset Address	Register Name	Total Reset Value
0x000005C0	RAW_PMU_INT	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	interrupt. raw_mac_fifo_err_i nt	MAC internal FIFO is empty and full error original interrupt status, write 1 to clear 0: No raw interrupt. 1: There is an original interrupt;
[29]	RW	clear the interrupt. raw_tx_rq_in_time interrupt; out_int	The RQ queue descriptor in the sending direction enqueues the timeout original interrupt, write 1 to 1: with raw 0: No raw interrupt.
[28]	RW	clear the interrupt. raw_rx_bq_in_time interrupt; out_int	The BQ queue descriptor in the receiving direction enqueues timeout original interrupt, write 1 to 0: no raw 1: There is a raw interrupt.
[27]	RW	interrupt, raw_txoutcff_full_i nt	Send direction DESC_OUTCFF full raw interrupt, write 1 to clear 0: no raw interrupt; 1: There is a raw interrupt.
[26]	RW	interrupt, raw_txoutcff_empt y_int	Send direction DESC_OUTCFF Empty raw interrupt, write 1 to clear 0: no raw interrupt; 1: There is a raw interrupt.
[25]	RW	raw_txcff_full_int	Send direction DESC_FIFO is full of original interrupt, write 1 to clear interrupt, 0: no original interrupt; 1: There is a raw interrupt.
[24]	RW	interrupt. raw_txcff_empty_i nt	Transmit direction DESC_FIFO empty raw interrupt, write 1 to clear 0: no raw interrupt; 1: There is a raw interrupt.

[23] RW		interrupt. raw_rxoutcff_full_i	Receive direction DESC_OUTCFF full raw interrupt, write 1 to clear 0: no raw interrupt; nt 1: There is a raw interrupt.
[22] RW		interrupt. raw_rxoutcff_empt y_int	Receive direction DESC_OUTCFF Empty raw interrupt, write 1 to clear 0: no raw interrupt; 1: There is a raw interrupt.
[21] RW	raw_rxcff_full_int		Receive direction DESC_FIFO full raw interrupt, write 1 to clear interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[20] RW		interrupt. raw_rxcff_empty_i	Receive direction DESC_FIFO empty raw interrupt, write 1 to clear 0: no raw interrupt; nt 1: There is a raw interrupt.
[19] RW	raw_tx_rq_in_int		Descriptor enqueuing (multiple or single descriptor enqueuing) in the sending direction tx_rq queue is interrupted, write 1 to clear the interrupt. 1: There is an original interrupt; 0: No raw interrupt.
[18] RW	raw_tx_bq_out_int	0: no raw interrupt;	The descriptor of the tx_bq queue in the sending direction is dequeued (multiple or single descriptor dequeue) interrupt, write 1 to clear the interrupt, 1: There is a raw interrupt.
[17] RW	raw_rx_bq_in_int		Descriptors enqueued in the rx_bq queue in the receiving direction (multiple or single descriptors enqueued) are interrupted, write 1 to clear the interrupt, 0: no original interrupt; 1: There is a raw interrupt.
[16] RW	raw_rx_fq_out_int		Dequeue dequeue (multiple or single descriptor dequeue) interrupt in the receiving direction rx_fq, write 1 to clear the interrupt, 1: original interrupt; 0: no original interrupt.
[15] RW		1 to clear interrupt. raw_tx_rq_empty_i 0: no raw interrupt; nt 1: raw interrupt.	Recycling description subqueue empty original interrupt in sending direction, write
[14] RW	raw_tx_rq_full_int		The recycling description subqueue in the sending direction is full of the original interrupt, write 1 to clear the interrupt. 0: no original interrupt; 1: There is a raw interrupt.

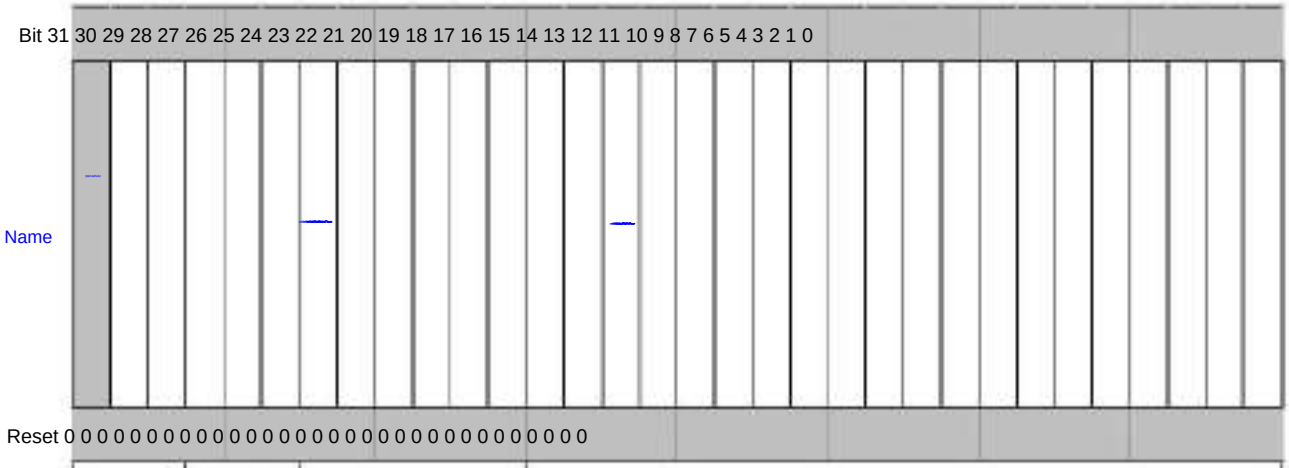
[13] RW		to clear the interrupt. raw_tx_rq_ _int	The recovery descriptor queue in the sending direction is almost empty. The original interrupt, write 1 alempty 0: no raw interrupt; 1: There is a raw interrupt.
[12] RW		clear the interrupts. raw_tx_rq_alfull_in t	The recovery descriptor queue in the sending direction is almost full of original interrupts, write 1 to 0: no raw interrupt; 1: There is a raw interrupt.
[11] RW		1 to clear the interrupt. raw_tx_bq_ int	The buff in the sending direction describes the original interrupt when the subqueue is empty, write empty_ 0: no raw interrupt; 1: There is a raw interrupt.
[10] RW raw_tx_bq_full_int			The buff description sub-queue in the sending direction is full of the original interrupt, write 1 to clear the interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[9] RW		1 to clear the interrupt. raw_tx_bq_ interrupt; _int	The buff description sub-queue in the sending direction is almost empty for the original interrupt, write alempty 0: no raw 1: There is a raw interrupt.
[8] RW		clear the interrupts. raw_tx_bq_alfull_i nt	The buff description sub-queue in the sending direction is almost full of original interrupts, write 1 to 0: no raw interrupt; 1: There is a raw interrupt.
[7] RW		1 to clear the interrupt. raw_rx_bq_ int	The buff in the receiving direction describes the original interrupt when the subqueue is empty, write empty_ 1: have raw interrupt; 0: No raw interrupt.
clear the interrupt. 0: No raw interrupt; [6] RW raw_rx_bq_			The buff description subqueue in the receiving direction is full of the original interrupt, write 1 to full_int 1: There is a raw interrupt.
[5] RW		1 to clear the interrupt. raw_rx_bq_ y_int	The buff description subqueue in the receiving direction is almost empty and the original interrupt, write alempt 0: no raw interrupt; 1: There is a raw interrupt.
[4] RW		clear the interrupts. raw_rx_bq_alfull_i nt	The buff description subqueue in the receiving direction is almost full of original interrupts, write 1 to 1: have raw interrupt; 0: No raw interrupt.
[3] RW		1 to clear the interrupt. raw_rx_fq_ nt	The idle description subqueue of the receiving direction is empty and the original interrupt is written empty_i 0: no raw interrupt; 1: There is a raw interrupt.

[2] RW	raw_rx_fq_full_int		The idle descriptor queue in the receiving direction is full of original interrupt, write 1 to clear the interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[1] RW		clear the interrupts. raw_rx_fq_ interrupt; _int	The idle descriptor queue in the receiving direction is almost empty for raw interrupts, write 1 to alempty 0: no raw 1: There is a raw interrupt.
[0] RW		clear the interrupts. raw_rx_fq_ interrupt; nt	The idle descriptor queue in the receiving direction is almost full of raw interrupts, write 1 to alfull_i 0: no raw 1: There is a raw interrupt.

ENA_PMU_INT

ENA_PMU_INT is the original interrupt enable register of PMU module.

Offset Address	Register Name	Total Reset Value
0x000005C4	ENA_PMU_INT	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	enable. ena_mac_fifo_err_i nt	MAC internal FIFO full and empty error interrupt 0: disable; 1: enable.
[29]	RW	direction. ena_tx_rq_in_time out_int	RQ queue descriptor enqueue timeout interrupt enable in send 0: Disable; 1: Enable.

[28] RW		direction. ena_rx_bq_in_time out_int	BQ queue descriptor enqueue timeout interrupt enable in receive 0: disable; 1: enable.
[27] RW		enable. ena_txoutcff_full_i nt	Transmit direction DESC_OUTCFF full interrupt 0: disable; 1: enable.
[26] RW		enable. ena_txoutcff_empt y_int	Transmit direction DESC_OUTCFF Empty interrupt 0: disable; 1: enable.
[25] RW	ena_txcff_full_int		Transmit direction DESC_FIFO full interrupt enable. 0: disable; 1: enable.
[24] RW		enable. ena_txcff_empty_i	Transmit direction DESC_FIFO empty interrupt 0: disable; nt 1: enable.
[23] RW		enable. ena_rxoutcff_full_i nt	Receive direction DESC_OUTCFF full interrupt 0: disable; 1: enable.
[22] RW		enable. ena_rxoutcff_empt y_int	Receive direction DESC_OUTCFF Empty interrupt 0: disable; 1: enable.
[21] RW	ena_rxcff_full_int		Receive direction DESC_FIFO full interrupt enable. 0: disable; 1: enable.
[20] RW		enable. ena_rxcff_empty_i	Receive direction DESC_FIFO empty interrupt 0: disable; nt 1: enable.
[19] RW	ena_tx_rq_in_int		Descriptor enqueue (multiple or single descriptor enqueue) interrupt enable for tx_rq queue in send direction. 0: disable; 1: enable.
[18] RW	ena_tx_bq_out_int	0: disable;	The descriptor dequeue (multiple or single descriptor dequeue) interrupt enable of the tx_bq queue in the sending direction. 1: enable.

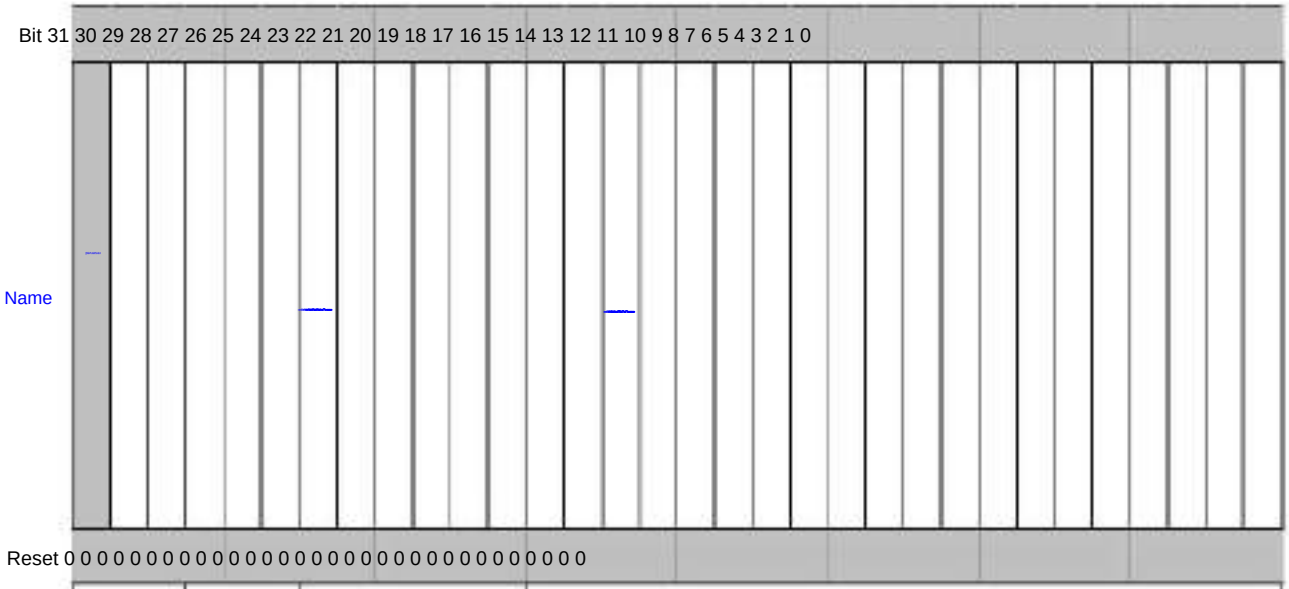
[17] RW	ena_rx_bq_in_int		Descriptor enqueue (multiple or single descriptor enqueue) interrupt enable for rx_bq queue in receive direction. 0: disable; 1: enable.
[16] RW	ena_rx_fq_out_int		The descriptor dequeuing (multiple or single descriptor dequeuing) interrupt enable of the rx_fq queue in the receiving direction. 1: enable; 0: Disabled.
[15] RW	ena_tx_rq_empty_i nt	send direction.	Recycling description subqueue empty interrupt enable in 0: disable;
direction. 0: disable;			1: enable.
[14] RW	ena_tx_rq_full_int		Recycling description subqueue full interrupt enable in sending 1: enable.
[13] RW	ena_tx_rq_alempty _int	direction is enabled. disable;	The reclaim descriptor subqueue almost empty interrupt in the send 0: 1: enable.
[12] RW	ena_tx_rq_alfull_in t	direction is enabled.	The reclaim descriptor subqueue almost full interrupt in the send 0: disable; 1: enable.
[11] RW	ena_tx_bq_empty_i nt	interrupt enable. disable;	The buff in the sending direction describes the subqueue empty 0: 1: enable.
[10] RW	ena_tx_bq_full_int		The buff in the sending direction describes the subqueue full interrupt enable. 0: Disabled. 1: enable;
[9] RW	ena_tx_bq_alempty _int	send direction. disable;	buff description subqueue almost empty interrupt enable for 0: 1: enable.
[8] RW	ena_tx_bq_alfull_i nt	interrupt is enabled.	The buff description subqueue in the send direction is almost full and the 0: disable; 1: enable.
[7] RW	ena_rx_bq_empty_i nt	interrupt enable.	The buff in the receiving direction describes the subqueue empty 0: disable; 1: enable.

[6] RW	ena_rx_bq_full_int		The buff in the receiving direction describes the subqueue full interrupt enable. 0: disable; 1: enable.
[5] RW		receive direction. disable; _int	ena_rx_bq_alempty buff description subqueue almost empty interrupt enable in 0: 1: enable.
[4] RW		interrupt is enabled. nt	ena_rx_bq_alfull_i The buff description subqueue in the receive direction is almost full and the 0: disable; 1: enable.
[3] RW		receive direction. disable; nt	ena_rx_fq_empty_i Idle descriptor subqueue empty interrupt enable for 0: 1: enable.
direction is enabled. 0:		disable;	[2] RW ena_rx_fq_full_int The idle descriptor queue full interrupt in the receive 1: enable.
[1] RW		direction is enabled. disable; _int	ena_rx_fq_alempty The Idle Descriptor Queue Almost Empty interrupt in the receive 0: 1: enable.
[0] RW		direction is enabled. disable; t	ena_rx_fq_alfull_in The idle descriptor queue almost full interrupt in the receive 0: 1: enable.

STATUS_PMU_INT

STATUS_PMU_INT is the interrupt status register of PMU module.

Offset Address	Register Name	Total Reset Value
0x000005C8	STATUS_PMU_INT	0x0000_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	status_mac_fifo_err	MAC internal FIFO full and empty error interrupt status. 0: no interrupt status; _int 1: There is an interrupt status.
[29]	RW	status_tx_rq_in_tim interrupt status. status; eout_int	The RQ queue descriptor in the sending direction enqueues the timeout 0: no interrupt 1: There is an interrupt status.
[28]	RW	status_rx_bq_in_ti direction. status; meout_int	BQ queue descriptor enqueue timeout interrupt status in receive 0: no interrupt 1: There is an interrupt status.
[27]	RW	status. status_txoutcff_full _int 1: interrupt status.	Transmit direction DESC_OUTCFF full interrupt 0: no interrupt status;
[26]	RW	status. status_txoutcff_em pty_int	Transmit direction DESC_OUTCFF Empty interrupt 0: no interrupt status; 1: There is an interrupt status.
[25]	RW	status. status_txcff_full_in t	Transmit direction DESC_FIFO full interrupt 0: no interrupt status; 1: There is an interrupt status.

[24] RW		status. status_txcff_empty_int	Transmit direction DESC_FIFO empty interrupt 0: no interrupt status; 1: There is an interrupt status.
[23] RW		status_rxoutcff_full 0: no interrupt status; _int	Receive direction DESC_OUTCFF full interrupt status. 1: There is an interrupt status.
[22] RW		status. status_rxoutcff_empty_int	Receive direction DESC_OUTCFF Empty interrupt 0: no interrupt status; 1: There is an interrupt status.
[21] RW		status. status_rxcff_full_int	Receive direction DESC_FIFO full interrupt 0: no interrupt status; 1: There is an interrupt status.
[20] RW		status. status_rxcff_empty_int	Receive direction DESC_FIFO empty interrupt 0: no interrupt status; 1: There is an interrupt status.
[19] RW	status_tx_rq_in_int	0: no interrupt status;	Descriptor enqueuing (multiple or single descriptor enqueuing) interrupt status of the tx_rq queue in the sending direction. 1: There is an interrupt status.
[18] RW		sending direction. status_tx_bq_out_i 0: no interrupt status; nt 1: interrupt status.	Dequeue dequeue (multiple or single descriptor dequeue) interrupt status of the tx_bq queue in the
[17] RW	status_rx_bq_in_int	0: no interrupt status;	Descriptor enqueuing (multiple or single descriptor enqueuing) interrupt status of the rx_bq queue in the receiving direction. 1: There is an interrupt status.
[16] RW		receiving direction. status_rx_fq_out_in 0: no interrupt status; 1: interrupt status.	Dequeue dequeue (multiple or single descriptor dequeue) interrupt status of the rx_fq queue in the
[15] RW		interrupt state. status_tx_rq_empty 0: no interrupt status; _int	Recycling in the send direction describes the subqueue empty 1: There is an interrupt status.

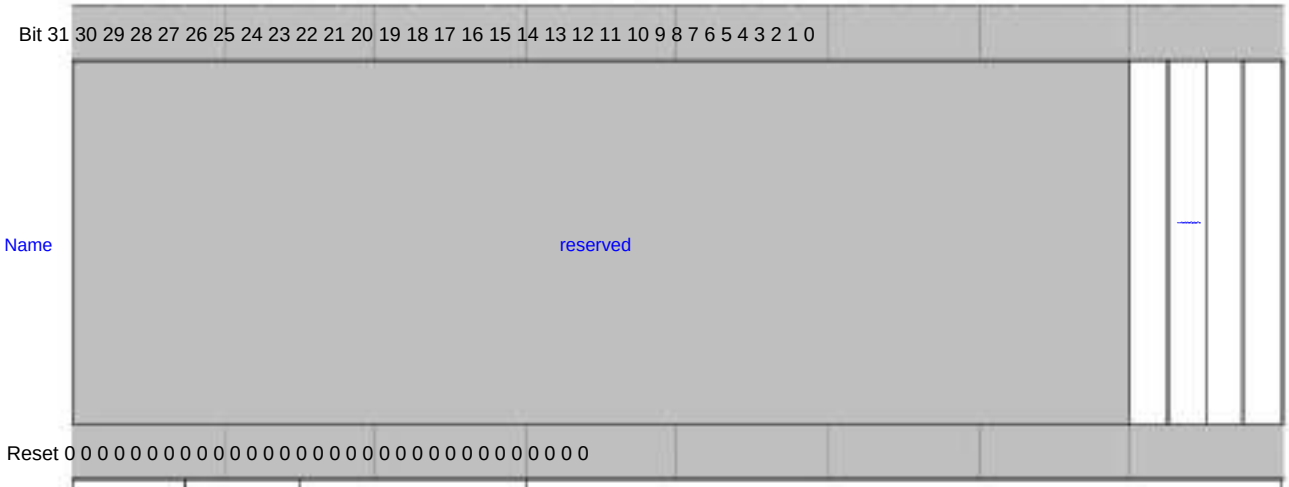
[14] RW		interrupt state. status; nt	status_tx_rq_	Recycling in the send direction describes the subqueue full full_i 0: no interrupt 1: There is an interrupt status.
[13] RW		interrupt state. status; ty_int	status_tx_rq_a	Recycling in the send direction describes the subqueue almost empty lemp 0: no interrupt 1: There is an interrupt status.
[12] RW		interrupt state. status; int	status_tx_rq_a	Recycling in the send direction describes the subqueue almost full lfull_ 0: no interrupt 1: There is an interrupt status.
[11] RW		interrupt status. status; y_int	status_tx_bq_	The buff in the sending direction describes the subqueue empty empt 0: no interrupt 1: There is an interrupt status.
[10] RW		interrupt status. status; nt	status_tx_bq_	The buff in the sending direction describes the subqueue full full_i 0: no interrupt 1: There is an interrupt status.
[9] RW		interrupt state. status; ty_int	status_tx_bq_a	The buff in the send direction describes the subqueue almost empty lemp 0: no interrupt 1: There is an interrupt status.
[8] RW		interrupt state. status; _int	status_tx_bq_	The buff in the send direction describes the subqueue almost full alfull 1: interrupt 0: No interrupt status.
[7] RW		interrupt status. y_int	status_rx_bq_	The buff in the receiving direction describes the subqueue empty empt 1: interrupt status; 0: No interrupt status.
[6] RW		interrupt status. status; nt	status_rx_bq_	The buff in the receiving direction describes the subqueue full full_i 0: no interrupt 1: There is an interrupt status.
[5] RW		interrupt state. status; pty_int	status_rx_bq_a	The buff in the receive direction describes the subqueue almost empty lem 0: no interrupt 1: There is an interrupt status.
[4] RW		interrupt state. status; _int	status_rx_bq_a	The buff in the receive direction describes the subqueue almost full lfull 0: no interrupt 1: There is an interrupt status.

[3] RW		interrupt status. status; _int	status_rx_fq_	Idle in the receive direction describes the subqueue empty empty 0: no interrupt 1: There is an interrupt status.
[2] RW		interrupt status. status; nt	status_rx_fq_	Idle in the receive direction describes the subqueue full full_i 0: no interrupt 1: There is an interrupt status.
[1] RW		interrupt status. status; ty_int	status_rx_fq_	Idle in receive direction describes subqueue almost empty alemp 0: no interrupt 1: There is an interrupt status.
[0] RW		interrupt status. status; _int	status_rx_fq_	The idle descriptor subqueue in the receive direction is almost full alfull 0: no interrupt 1: There is an interrupt status.

DESC_WR_RD_ENA

DESC_WR_RD_ENA is cff read and write descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x000005CC	DESC_WR_RD_ENA	0x0000_0000



Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	rx_outcff_wr_desc 0:	RX_OUTCFF in the receive direction writes desc enable to RX_BQ. disable; _ena 1: enable.

RW	rx_cff_rd_desc_ena		RX_CFF in receive direction Read desc from free descriptor queue enable. 0: Disable; [2] 1: enable.
[1] RW		tx_outcff_wr_desc_ 0: this one	TX_OUTCFF in the sending direction writes desc enable to TX_RQ. disable; 1: enable.
RW	tx_cff_rd_desc_ena	1: Enable.	TX_CFF in transmit direction read desc enable from TX_BQ. 0: Disable; [0]

IN_QUEUE_TH

IN_QUEUE_TH is the rx_bq, tx_rq queue interrupt watermark register.

Offset Address	Register Name	Total Reset Value
0x05D8	IN_QUEUE_TH	0x0001_0001

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	tx_rq_in_th	reserved	rx_bq_in_th
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	tx_rq_in_th	Sending direction, report the waterline of the descriptor enqueuing interrupt, at least set to 1.
[15:8]	RO	reserved	reserve.
[7:0]	RW	rx_bq_in_th	Receive direction, report the waterline of descriptor enqueue interrupt, at least set to 1.

OUT_QUEUE_TH

OUT_QUEUE_TH is the rx_fq, tx_bq dequeuing interrupt watermark register.

Offset Address	Register Name	Total Reset Value
0x05DC	OUT_QUEUE_TH	0x0001_0001

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	tx_bq_out_th	reserved	rx_fq_out_th
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	tx_bq_out_th	send direction, report the waterline of descriptor out of queue interrupt.
[15:8]	RO	reserved	reserve.
[7:0]	RW	rx_fq_out_th	Receive direction, the waterline for reporting descriptor out of queue interrupt.

RX_BQ_IN_TIMEOUT_TH

RX_BQ_IN_TIMEOUT_TH is the original interrupt watermark register for rx_bq enqueue timeout.

Offset Address	Register Name	Total Reset Value
0x05E0	RX_BQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	rx_bq_in_timeout_th		
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	rx_bq_in_timeout_th	rx_bq_in_timeout_t is the BQ queue in the receiving direction, and describes the timeout interrupt waterline of subqueue enqueue.

TX_RQ_IN_TIMEOUT_TH

TX_RQ_IN_TIMEOUT_TH is the tx_rq enqueue timeout raw interrupt watermark register.

Offset Address	Register Name	Total Reset Value
0x05E4	TX_RQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_rq_in_timeout_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_rq_in_timeout_t	is the RQ queue in the sending direction, and describes the queue timeout interrupt waterline. h

STOP_CMD

STOP_CMD is the stop receiving and sending packet control register.

Offset Address	Register Name	Total Reset Value
0x05E8	STOP_CMD	0x0000_0000

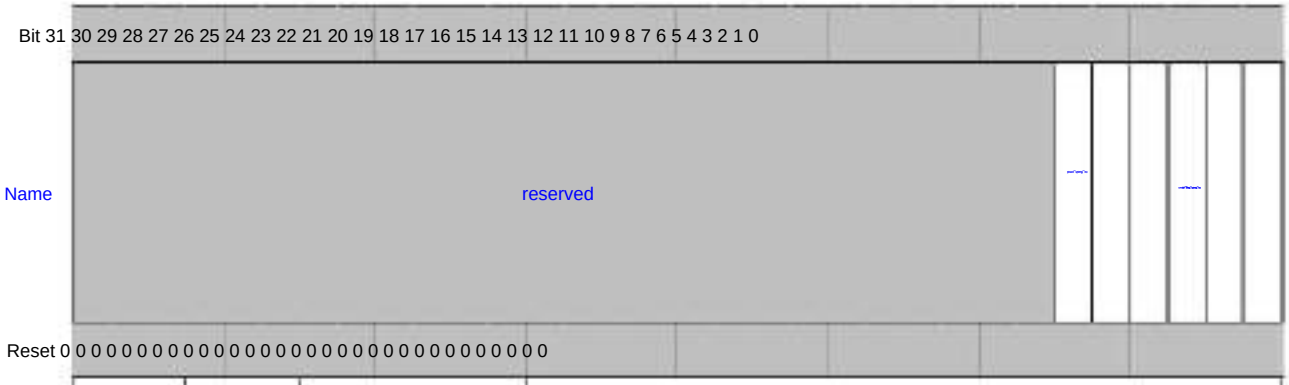
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	tx_stop_en	Enable to stop sending packets in the sending direction. 0: disable; 1: enable.
[0]	RW	rx_stop_en	Enable to stop receiving packets in the receiving direction. 0: disable; 1: enable.

FLUSH_CMD

FLUSH_CMD is the flush descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x05EC	FLUSH_CMD	0x0000_0000



Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	tx_flush_cmd	The recycle descriptor command in the sending direction, the descriptor enters the tx_rq queue. 0: The configuration recovery description subcommand is invalid; 1: Configure the recycling description subcommand to be valid.
[4]	RW	rx_flush_cmd	Recycling descriptor commands in the receiving direction, the descriptors enter the rx_bq queue. 0: The configuration recovery description subcommand is invalid; 1: Configure the recycling description subcommand to be valid.
[3]	RW	tx_flush_flag_down	Indicates the end of the reclaimed descriptor in the sending direction. When the reclaimed descriptor is completed, the logic will set tx_flush_flag to 1, and the software will write 1 to clear it.
[2]	RW	tx_flush_flag_up	The flushing descriptor in the sending direction indicates that when the sending and receiving of packets is stopped, the logic sets tx_flush_flag to 1, indicating that the software can perform the flushing descriptor operation, and the software writes 1 to clear it to zero.
[1]	RW	rx_flush_flag_down	Indicates the end of the recycling descriptor in the receive direction. When the logic completes the descriptor recovery operation, set rx_flush_flag_down to 1, and write 1 to clear it to 0 by software.
[0]	RW	rx_flush_flag_up	Recycling descriptor indication for receive direction. After stopping to receive packets, the logic will set rx_flush_flag_up to 1, indicating that the software can perform the reclaim descriptor operation, and the software writes 1 to clear 0.

U_EEE_INTR_SRC

U_EEE_INTR_SRC is the rx and tx direction lpi status register.

Offset Address	Register Name	Total Reset Value
0x0800	U_EEE_INTR_SRC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	tx_lpi_cond	tx direction lpi state. 0: tx fifo and tx descriptor are not empty; 1: Both tx fifo and tx descriptor are empty.
[3]	RW	rx_leave_lpi	rx direction leaves lpi state 0: not left 1: leave
[2]	RW	rx_entry_lpi	The rx direction enters the lpi state 0: not entered 1: enter
[1]	RW	tx_leave_lpi	The tx direction leaves the lpi state 0: not left 1: leave
[0]	RW	tx_entry_lpi	The tx direction enters the lpi state 0: not entered 1: enter

U_EEE_INTR_EN

U_EEE_INTR_EN is the rx and tx direction interrupt mask and enable register.

Offset Address	Register Name	Total Reset Value
0x0804	U_EEE_INTR_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	tx_lpi_cond_msk	tx direction lpi status interrupt mask register. 0: Disable the interrupt mask function; 1: Enable the interrupt mask function.
[8]	RW	rx_leave_lpi_msk	rx direction leaves lpi state interrupt mask register 0: disable interrupt mask function; 1: Enable the interrupt mask function.
[7]	RW	rx_entry_lpi_msk	The rx direction enters the lpi state interrupt mask register 0: disable the interrupt mask function; 1: enable the interrupt mask function.
[6]	RW	tx_leave_lpi_msk	The tx direction leaves the lpi state interrupt mask register 0: disable the interrupt mask function; 1: Enable the interrupt mask function.
[5]	RW	tx_entry_lpi_msk	The tx direction enters the lpi state interrupt mask register 0: disable the interrupt mask function; 1: Enable the interrupt mask function.
[4]	RW	tx_lpi_cond_en	tx direction lpi status interrupt enable register. 0: disable interrupt enable; 1: Enable interrupt enable.
[3]	RW	rx_leave_lpi_en	rx direction leaves lpi status interrupt enable register 0: disable interrupt enable; 1: Enable interrupt enable.
[2]	RW	rx_entry_lpi_en	rx direction enters lpi state interrupt enable register 0: disable interrupt enable; 1: Enable interrupt enable.

[1] RW	tx_leave_lpi_en		tx direction leaves lpi status interrupt enable register 0: disable interrupt enable; 1: Enable interrupt enable.
[0] RW	tx_entry_lpi_en		The tx direction enters the lpi state interrupt enable register 0: disable the interrupt enable; 1: Enable interrupt enable.

U_EEE_ENABLE

U_EEE_ENABLE is the enable signal register of EEE module.

Offset Address	Register Name	Total Reset Value
0x0808	U_EEE_ENABLE	0x00F4_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eee_ls_timer																															
Reset	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[31:4]	RW	eee_ls_timer		After PHY link=1, the buffering software enables the hardware to enter the buffering time of lpi, and the default is 1s.
[3]	RW	gmii_mode		GMII mode selection. 0: 10M, 100M rate mode; 1: 1000M rate mode.
[2]	RW	cond_intr_keep		Interrupt signal sending frequency configuration 0: The hardware sends the tx_lpi_cond interrupt only once; 1: In the tx direction lpi, the interrupt signal is enabled for each rising edge of the clock.
[1]	RW	tx_lpi_assert		Software configures the hardware to enter the LPI state. 0: do not enter; 1: enter.
[0]	RW	eee_enable		The EEE module is enabled. 0: disable; 1: enable.

U_EEE_TIMER

U_EEE_TIMER is the LPI time counter register.

Offset Address	Register Name	Total Reset Value
0x080C	U_EEE_TIMER	0x001E_000A

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lpi_tw_timer	lpi_cond_timer
Reset	0 0 0 0 0 0 0 0 0 0 0 0 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0

Bits	Access Name	Description
[31:16]	RW lpi_tw_timer	The wake-up time from LPI to normal mode, the default is 30us.
[15:0]	RW lpi_cond_timer	Record the duration of the condition that both TXFIFO and EX_DESC are empty at the same time, when the duration is equal to lpi_cond_timer, you can enter LPI

U_EEE_LINK_STATUS

U_EEE_LINK_STATUS is the EEE status register.

Offset Address	Register Name	Total Reset Value
0x0810	U_EEE_LINK_STATUS	0x0000_3F20

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	in_cnt	version
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 1 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RW intr_cnt		EEE interrupt counter.
[15]	RO	eee_tx_lpi_stay	TX is in LPI state. 0: not in LPI state; 1: In LPI state.
[14]	RO	eee_rx_lpi_stay_ff3	RX is in LPI state. 0: not in LPI state; 1: In LPI state.
[13:4]	RO	version	Logical version number.

[3]	RO	reserved	reserve.
[2] RW eee_auto			Automatic entry and exit EEE switch. 0: To enter and exit EEE with the cooperation of software and logic interrupt; 1: The logic automatically enters and exits EEE without software participation.
[1] RW		packets from TXFIFO	When in LPI state, can eee_hold_txdesc_re take 0: In LPI state, it can fetch packets from TXFIFO; ad 1: Control MAC does not read packets from TXFIFO during LPI.
[0] RW phy_link_sts			PHY connection status. 0ÿlink_downÿ 1ÿlink_upÿ

U_EEE_TIME_CLK_CNT

U_EEE_TIME_CLK_CNT is the timing pulse count register.

Offset Address	Register Name	Total Reset Value
0x0814	U_EEE_TIME_CLK_CNT	0x0000_007D

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	clk_period_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1

Bits	Access Name		Description
[31:0] RW	clk_period_cnt		The counter is used to generate a timing pulse unit of 1us in the hardware, and the clock cycle of 125M is 8ns.

PMT_CTRL_STAUTS

PMT_CTRL_STAUTS is the PMT control and status register.

Offset Address	Register Name	Total Reset Value
0x0A00	PMT_CTRL_STAUTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	wake-up frame frame; cast scr_wkupfrm_glbu	Configure whether the unicast frame of the MAC address is a 0: not considered a wake-up 1: A unicast frame with a matching MAC address is considered a valid wake-up frame.
[8:7]	RO	reserved	reserve
[6]	RW	rcvd_wkup_frm	Whether a wakeup frame was received. 0: No wake_up frame received; 1: Wake_up frame received.
[5]	RW	rcvd_mgk_pkt	Whether to receive magic packet. 0: No magic packet received; 1: Magic packet received.
[4]	RO	reserved	reserve
[3]	RW	scr_intr_en	PMT interrupt enable switch. 0: off; 1: enable enable.
[2]	RW	scr_wkupfrm_en	Receive wake_up frame enable. 0: off; 1: enable enable.
[1]	RW	scr_mgkpkt_en	Magic packet reception enable. 0: off; 1: enable enable.
[0]	RW	scr_power_down	powerdown mode enabled. 0: exit power_down mode; 1: enter power_down mode.

FILTER_0_BYTE_MASK

FILTER_0_BYTE_MASK is the 0th effective byte selection register of PMT.

Offset Address	Register Name	Total Reset Value
0x0A04	FILTER_0_BYTE_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter0bytemsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter0bytemsk	as byte mask. A bit of 1 indicates that the corresponding byte is valid. Bit[31] must be set to low, indicating that the mask is valid, and bit[30:0] is used

FILTER_1_BYTE_MASK

FILTER_1_BYTE_MASK is the first effective byte selection register of PMT.

Offset Address	Register Name	Total Reset Value
0x0A08	FILTER_1_BYTE_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter1bytemsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter1bytemsk	byte mask. bit[31] must be set to low, indicating that the mask is valid, and bit[30:0] is maskÿ

FILTER_2_BYTE_MASK

FILTER_2_BYTE_MASK is the second valid byte selection register of PMT.

Offset Address	Register Name	Total Reset Value
0x0A0C	FILTER_2_BYTE_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter2bytemsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	byte wkupfrm_filter2byte emsk	bit[31] must be set to low, indicating that the mask is valid, and bit[30:0] is maskÿ

FILTER_3_BYTE_MASK

FILTER_3_BYTE_MASK is the third effective byte selection register of PMT.

Offset Address	Register Name	Total Reset Value
0x0A10	FILTER_3_BYTE_MASK	0x0000_0000

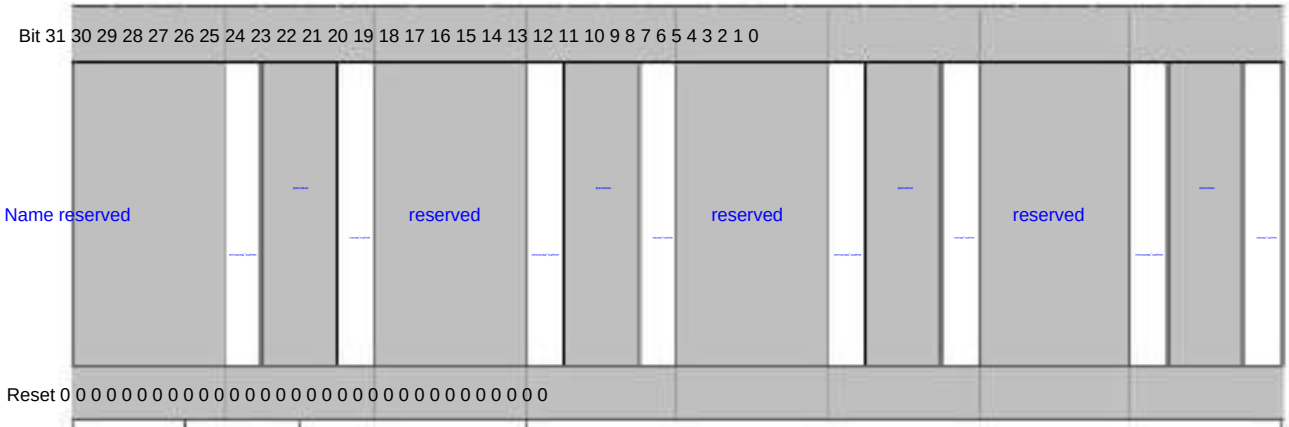
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter3bytemsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	byte wkupfrm_filter3byte emsk	Bit[31] must be set to low, indicating that the mask is valid, and bit[30:0] is mask.

FILTER_COMMAND

FILTER_COMMAND is the PMT template selection and multicast enable register.

Offset Address	Register Name	Total Reset Value
0x0A14	FILTER_COMMAND	0x0000_0000



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	offset address of the corresponding template;	Template 3 specifies the address type. 0: Determine whether the wkupfrm_filter3mc ast is successfully matched according to the effective byte and CRC 1: As long as DA is a valid multicast address, address filtering is successful.
[26:25]	RO	reserved	reserve.
[24]	RW	wkupfrm_filter3en	The third set of filter templates is enabled. 0: disable; 1: enable.
[23:20]	RO	reserved	reserve.
[19]	RW	address of the corresponding ast template;	Template 2 specifies the address type. 0: Judge whether the wkupfrm_filter2mc is successfully matched according to the effective byte and CRC offset 1: As long as DA is a valid multicast address, address filtering is successful.
[18:17]	RO	reserved	reserve
[16]	RW	wkupfrm_filter2en	The second set of filter templates is enabled. 0: disable; 1: enable.
[15:12]	RO	reserved	reserve.
[11]	RW	offset address of the corresponding template;	Template 1 specifies the address type. 0: Determine whether the wkupfrm_filter1mc ast match is successful or not according to the effective byte and CRC 1: As long as DA is a valid multicast address, address filtering is successful.

[10:9] RO		reserved	reserve.
[8] RW	wkupfrm_filter1en		The first set of filter templates is enabled. 0: disable; 1: enable.
[7:4] RO		reserved	reserve.
[3] RW		address of the corresponding ast template	Template 0 specifies the address type. 0: Determine whether the wkupfrm_filter0mc match is successful according to the effective byte and CRC offset 1: As long as DA is a valid multicast address, address filtering is successful.
[2:1] RO		reserved	reserve.
[0] RW	wkupfrm_filter0en		The 0th set of filter templates is enabled. 0: disable; 1: enable.

FILTER_OFFSET

FILTER_OFFSET is the position offset register for calculating CRC.

Offset Address	Register Name	Total Reset Value
0x0A18	FILTER_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wkupfrm_filter3offset	wkupfrm_filter2offset	wkupfrm_filter1offset	wkupfrm_filter0offset
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	There are 4 sets of templates in set	wkupfrm_filter3off, and the third set of templates is used to calculate the position offset of CRC.
[23:16]	RW	There are 4 sets of templates in set	wkupfrm_filter2off, the second set of templates is used to calculate the position offset of CRC.
[15:8]	RW	There are 4 sets of templates set	in wkupfrm_filter1off. The first set of templates calculates the position offset of CRC.
[7:0]	RW	There are 4 sets of templates set	in wkupfrm_filter0off, the 0th set of templates is used to calculate the position offset of CRC.

FILTER0_1_CRC

FILTER0_1_CRC is the software expected CRC value 0 and 1 register.

Offset Address	Register Name	Total Reset Value
0x0A1C	FILTER0_1_CRC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter1crc	wkupfrm_filter0crc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter1crc	There are 4 sets of templates in total, template 1 is the CRC value register expected by the software.
[15:0]	RW	wkupfrm_filter0crc	Template 0 software expected CRC value register.

FILTER2_3_CRC

FILTER2_3_CRC is the software expected CRC value 2 and 3 registers.

Offset Address	Register Name	Total Reset Value
0x0A20	FILTER2_3_CRC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	wkupfrm_filter3crc	wkupfrm_filter2crc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter3crc	Template 3 software expected CRC value register.
[15:0]	RW	wkupfrm_filter2crc	Template 2 software expected CRC value register.

Table of contents

illustration catalog

6 video encoding

6.1 General overview

The video encoder is a multi-protocol encoder that supports H.264/H.265/JPEG/MJPEG, including VEDU and JPGE. Among them, VEDU implements the encoding of H.265 and H.264 protocols, and JPGE implements JPEG/MJPEG Protocol encoding.

6.2 OURS

6.2.1 Overview

VEDU (Video Encode Decode Unit) is a hardware-implemented encoder that supports the H.265/H.264 video standard. VEDU has the advantages of low CPU occupancy, small bus bandwidth occupancy, low latency, and low power consumption.

6.2.2 Features

VEDU encoders have the following features:

Support ITU-T H.265 Main Profile @Level 6.1 Main Tier encoding ÿ Support 1/2, 1/4
pixel precision motion compensation
ÿ Inter prediction supports four PU types: 64x64, 32x32, 16x16, and 8x8 ÿ Intra prediction
supports four PU types: 32x32, 16x16, 8x8, and 4x4 ÿ Supports Merge/SKIP mode with
a maximum candidate number of 2 ÿ Supports 32x32, 16x16, 8x8, 4x4
four TU types
ÿSupport CABAC entropy coding
ÿSupport De-blocking filtering ÿSupport
SAO ÿSupport IPCM
encoding Support ITU-T
H.264 High Profile/Main Profile/Baseline Profile@Level 5 encoding ÿSupport 1/2, 1/4 pixel precision motion
compensation
ÿSupport inter-frame prediction 16x16 and 8x8 sub-block types

ÿSupports all Intra4x4, Intra8x8, Intra16x16 prediction modes ÿSupports Trans4x4,

Trans8x8

ÿSupport CABAC, CAVLC entropy coding

ÿSupport De-blocking filter ÿSupport

IPCM encoding

Supports H.264 SVC Time Domain Layering (SVC-T)

The following input image formats are supported

ÿ Semi-Planar YCbCr4:2:0

H.265 / H.264 multi-stream encoding performance: ÿ 8M

(3840x2160)@30fps + 720P@30fps encoding supports configurable image resolution

ÿ Minimum image resolution: 128x128 (H.265), 192x128 (H.264)

ÿMaximum image resolution: 4608x4608

ÿConfiguration step size of image width/height is 2

Support region of interest

encoding ÿSupport region of interest encoding of up to 8

regions ÿEach region of interest encoding function can be independently

enabled/disabled Support OSD Region Code Protection

OSD area coding protection function can enable/disable support video

front-end OSD overlay processing

ÿ Pre-encode OSD overlay supporting up to 8 regions

ÿSupport OSD overlay at any position and the maximum image size

ÿSupport 129-level alpha overlay

ÿ OSD overlay function can be enabled/

disabled Support color to gray

encoding function Support CBR/VBR/FIXQP three bit rate

control modes Output bit rate range: 2kbpsÿ100Mbps

注意

The area code protection function of VEDU only works on the OSD superimposed on VEDU.

6.2.3 Functional description

The functional block diagram of VEDU is shown in Figure 6-1 .

VEDU coding realizes motion estimation/inter prediction, intra prediction, motion vector prediction, transformation/quantization, inverse quantization/inverse transformation, CABAC coding and code stream generation, de-blocking filtering, SAO and other protocol/algorithm processing (H. 265), the ARM software completes encoding control processing such as bit rate control and interrupt processing.

Before starting VEDU for video encoding, the software needs to allocate the following three types of buffers in the external memory (DDR SDRAM).

input image buffer

VEDU will read the original image to be encoded from this buffer during the encoding process. This buffer is usually written by the video input unit.

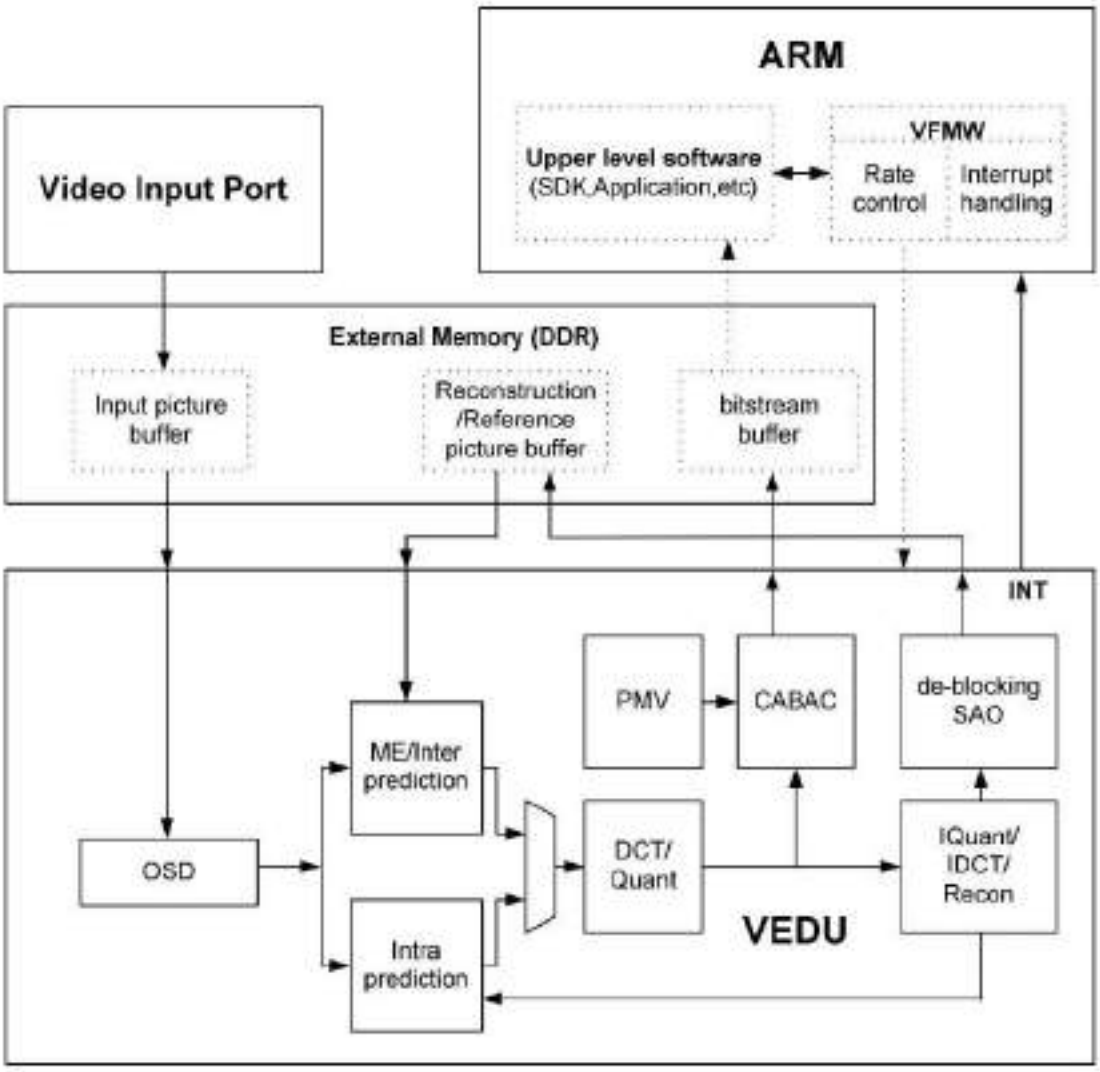
Reconstructed image/reference image buffer

During the encoding process, VEDU will write the reconstructed image into the buffer as the reference image of the subsequent image, and read the reference image from the buffer when encoding the P frame.

Code stream

buffer This buffer is used to store the code stream output by encoding. VEDU will write the code stream into this buffer during the encoding process. This buffer is normally read by software.

Figure 6-1 VEDU coding functional block diagram



6.3 JPGE

6.3.1 Overview

JPGE (JPEG Encoder) is a hardware-implemented high-performance JPEG encoder, which can realize up to 67.1M pixel picture capture or high-definition image MJPEG encoding business.

6.3.2 Features

JPGE has the following characteristics:

Support ISO/IEC 10918-1 (CCITT T.81) Baseline Process (DCT Sequential) encoding Support YCbCr4:2:0, YCbCr4:2:2 image encoding of two chroma sampling formats Support the following input image formats:

ÿ Semi-Planar YCbCr4:2:0

ÿ Semi-Planar YCbCr4:2:2

JPEG encoding performance :

ÿ 8Mÿ3840x2160ÿ@30fps

ÿ 12Mÿ4224x2816ÿ@20fps

ÿ 16M (4608x3456)@15fps supports configurable image resolution

ÿMinimum image resolution: 32x32

ÿMaximum image resolution: 8192x8192 Image width/height is configured in steps of 2

Quantization tables are configurable

ÿ Three components of Y, Cb, and Cr, providing two quantization tables (shared by Cb and Cr) and supporting color-to-gray conversion

6.3.3 Functional description

The JPGE function is shown in Figure 6-2 .

It can be seen from the figure that the JPGE hardware implements protocol processing with a large amount of computation, such as level shift, DCT, quantization, scanning, VLC encoding, and code stream generation, while the ARM software completes encoding control processing such as quantization table configuration and interrupt processing.

Before starting JPGE for video encoding, the software needs to allocate the following two types of buffers in the external memory (DDR SDRAM):

input image buffer

JPGE reads the raw image to be encoded from this buffer during the encoding process. This buffer is usually written by the video input unit.

stream buffer

The buffer is used to store the encoded output code stream. JPGE writes the codestream to this buffer during encoding. This buffer is normally read by software.

Figure 6-2 JPGE functional block diagram

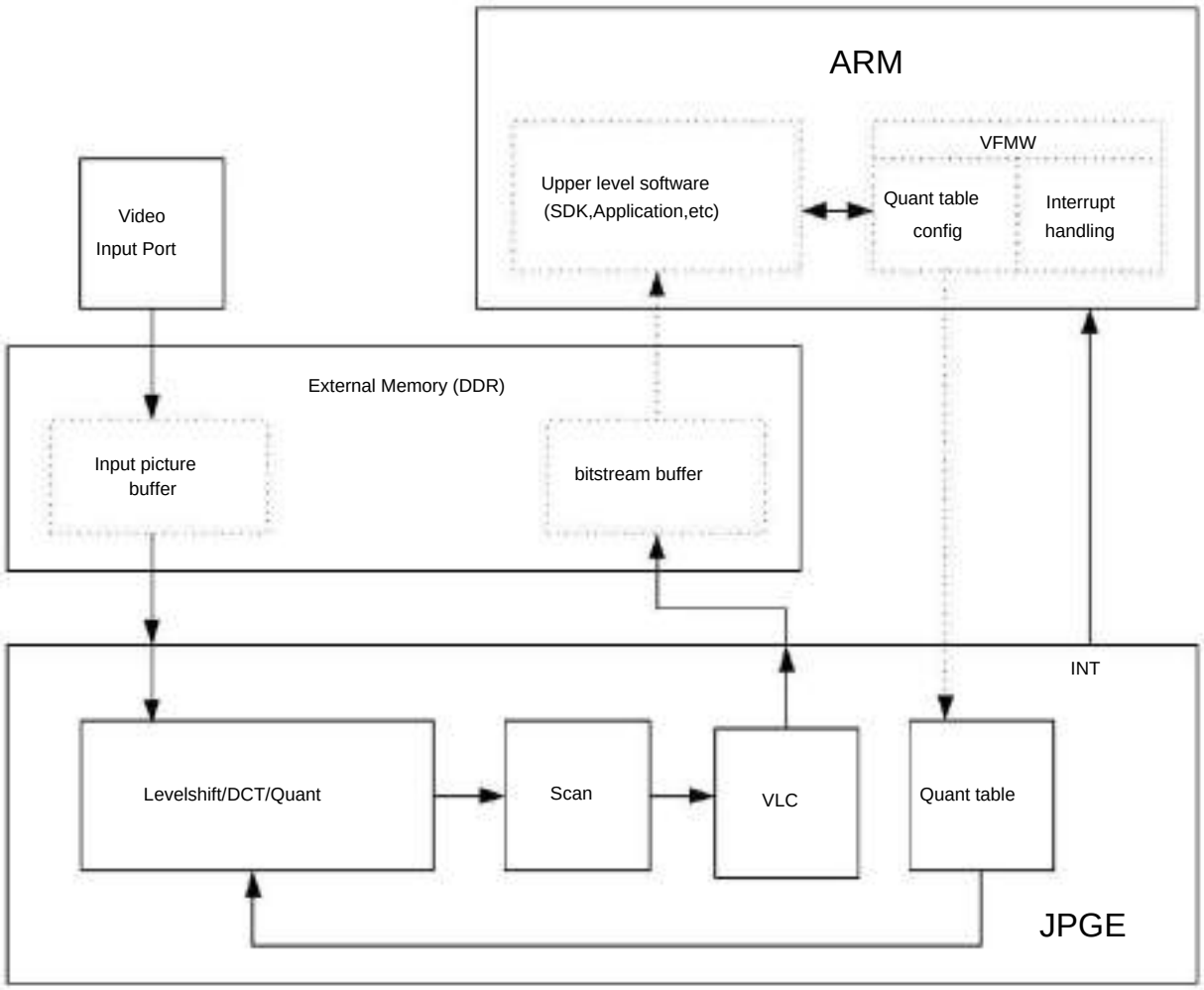


Table of contents

7 Video and Graphics Processing

7.1 TDE

7.1.1 Overview

The 2D graphics acceleration engine TDE (Two Dimensional Engine) uses hardware for graphics rendering, which can greatly reduce the CPU usage and improve the resource utilization of memory bandwidth. TDE reads and writes bitmap data, filter scaling factor, linked list node parameter information, and some linked list information through the AXI Master bus interface; obtains CPU register configuration information through the APB Slave bus interface.

The graphics data interface includes two paths, whose functions are as follows:

Passage 1 completes the functions of direct copy and direct filling during single-source operation.

Channel 2 can complete various complex operations, such as image scaling, etc., when operating with a single source. When pass 1 and pass 2 work together, operations such as color mixing can be completed.

7.1.2 Functional description

The TDE module has the following features:

Channel 1 supports ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, byte, halfword format.

Channel 2 supports ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8 formats. The output image supports ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, byte, halfword format.

Only little-endian systems are supported. Support source bitmap 1, source bitmap 2 and output bitmap formats can be configured separately.

Support Gamma correction, brightness and contrast adjustment.

Direct copy is supported.

Direct filling is supported.

Support 2D-resize operation.

Support clip operation. Support

alpha blending operation. Support colorkey

operation. Support clip mask function.

Support reverse scanning.

Provides a status interrupt.

7.2 VPSS

7.2.1 Overview

The video processing subsystem VPSS (Video Processing Sub System) realizes the video processing function. Contains Gaussian noise 3D adaptive noise reduction, video occlusion, video cropping, scaling, brightness single component processing, mirror, flip functions.

VPSS features are as follows:

Support single-frame online or offline processing of 4096-width video sources.

Support up to four channels of video output, which are three encoding channels and one display channel. The output supports video arbitrary

quadrilateral solid occlusion in 8 regions, among which concave quadrilaterals are processed into triangles.

Support video cropping of three output channels, two encoding channels and one display channel respectively.

Support video data compression. The

offline mode supports the register linked list configuration function, and the online mode supports the APB configuration register function. Support across

4K boundaries. The input and

output data format is Semiplanar 420/422. Support outstanding configuration. Support

clock gate low power consumption mode of

MEM. Support low latency.

Supports luma single-component processing.

7.2.2 Features

Gaussian noise removal function: NR module (noise reduction), which can remove Gaussian noise in the image through parameter configuration, making the image smoother and reducing the encoding bit rate.

Scaling function: Low-frequency filtering processing with different input and output resolutions. In online mode, the large stream channel only supports 1:1, and the other channels support reduction or 1:1, and do not support enlargement. In offline mode, only large stream channels support zoom-in (maximum 16 times zoom-in), and other channels support zoom-out (maximum 15 times zoom-out).

7.3 VGS

7.3.1 Overview

Video graphics system VGS (Video Graphics System) realizes video and graphics processing functions. Contains OSD overlay, zoom, brightness area statistics, video cropping, video occlusion, and rotation functions.

VGS features are as follows:

Support single frame offline processing 4096 wide video source

Support one channel video output

Support 1 area OSD and video overlay

The input format of OSD is ARGB1555/ ARGB4444/ ARGB8888 Support register linked list configuration function

Support across 4K boundaries

Input/output data supports linear storage, supports video data compression, supports 90° or 270° rotation, supports 1-area video occlusion, and the occlusion shape can support solid or hollow arbitrary quadrilaterals, and concave quadrilaterals can be processed into triangles.

Support video clipping

Support outstanding configuration Support MEM clock gate low power mode Support area brightness and statistics

Support luma single component processing

7.3.2 Features

Video occlusion: The shape of video occlusion can be any solid or hollow quadrilateral, and the concave quadrilateral is treated as a triangle.

Scaling function: Low-frequency filtering processing with different input and output resolutions. The zoom factor is 15 times smaller and 16 times larger.

7.4 GDC

7.4.1 Overview

GDC (Geometric Distortion Correction) realizes image distortion correction function.

GDC features are as follows:

Support single-frame offline processing Maximum 16M video source

Maximum single-mode 8M 30fps processing performance

Support YUV semi planer420 format input and output images Support 360/180/normal three

fisheye correction models

Support top-mounted, wall-mounted, table-mounted three installation methods

Support PTZ function under three correction methods of fisheye Support

register linked list configuration function

Support across 4K boundaries

Input/output data supports linear storage

Support video image uncompressed input, support video data compressed output

Support outstanding configuration Support

clock gate low power consumption mode of MEM

7.4.2 Features

Fisheye correction function: When the fisheye function is turned on, an appropriate output resolution can be configured according to the currently selected visible area and correction model to ensure the best effect of the corrected image;

Installation method: 3 installation methods are supported. In actual use, it is necessary to select the appropriate installation method and correction model according to the current needs, so as to achieve the best correction effect;

Table of contents

illustration catalog

table of contents

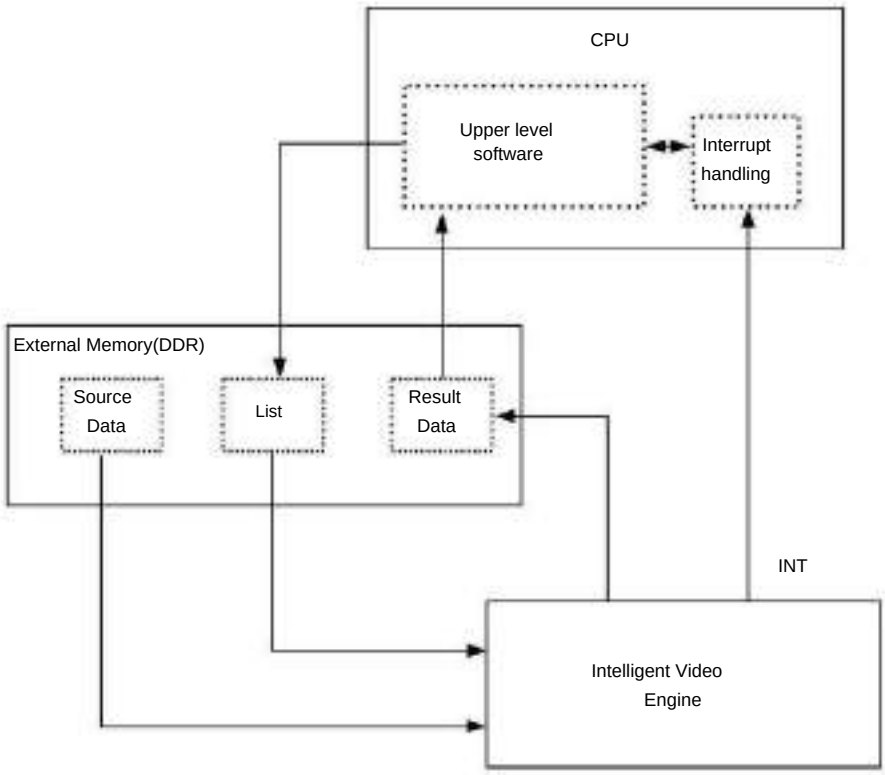
8 Intelligent Acceleration Engine

8.1 IVE

8.1.1 Overview

The IVE (Intelligent Video Engine) module provides a series of basic computing functions used in the intelligent analysis algorithm, as well as some special functions that consume a lot of time. It is a hardware acceleration module in the intelligent analysis system. The position of IVE in the system is shown in Figure 8-1 .

Figure 8-1 Location map of IVE in the system



8.1.2 Functional description

The IVE module supports the following features:

DMA: supports direct copy, interval copy, and memory filling.

Filter: Support 5x5 template filtering.

CSC: Support YUV2RGB, YUV2HSV, YUV2LAB, RGB2YUV color space conversion.

FilterAndCSC: Supports the composite function of 5x5 mask filter and CSC.

Sobel: Support 5x5 template Sobel-like gradient calculation.

MagAndAng\Canny: Support 5x5 template gradient magnitude and argument calculation, Canny edge extraction.

Erode: Support for 5x5 template erosion.

Dilate: Supports 5x5 template dilation.

Thresh\Thresh_S16\Thresh_U16: support image thresholding.

And\Or\Xor: Supports AND, OR, XOR of two images.

Add\Sub: Support weighted addition and subtraction of two images.

Integ: Support integral graph calculation.

Hist: supports histogram statistics.

Map: Supports assigning values to images through 256-level map mapping.

16BitTo8Bit: Support linear conversion from 16bit data to 8bit data.

OrdStatFilter: Supports order statistics filtering: median filtering, maximum filtering, and minimum filtering.

NCC: Supports the calculation of the cross-correlation coefficient of two images of the same size.

CCL: Support for connected region labeling.

GMM: Supports mixed Gaussian background modeling of grayscale images and RGB images.

LBP: Supports simple local binary pattern calculations.

NormGrad: supports normalized gradient calculation.

LKOpticalFlow: supports LK optical flow tracking.

STCorner: Support ShiTomasi corner detection.

GradFg: Support gradient foreground operation.

MatchBgModel\UpdateBgModel: supports background matching and background updating.

ANN_MLP_Predict: ANN_MLP prediction is supported.

SVM_Predict: Supports SVM prediction.

Resize: Support bilinear, area image scaling.

GMM2: Support fast mixed Gaussian background modeling of grayscale and RGB images.

CNN: Supports convolutional neural network calculations.

SAD: Calculate the cumulative sum of the absolute values of the corresponding pixel differences of the two images in blocks. Support for soft reset alone.

Support 128bit AXI bus and 32 bit APB bus.

Support linked list level interrupt, node level interrupt and timeout interrupt.

Support SP 400, SP420 (semi-plannar 420), SP422 (semi-plannar 422), package, planar and other input formats. Support SP 400, SP420, SP422,

package, plannar and other output formats. Some operators support non-16-byte alignment for

read and write addresses.

8.1.3 Working method

8.1.3.1 Input and output data format

Both w and h in Figure 8-2 to Figure 8-12 refer to the width and height of the image in units of pixels. Unless otherwise specified, the data storage order is in the memory storage order of the little endian system (little endian). For the convenience of description, word is used as the storage unit for description. In practical applications, different operators have special requirements for data storage alignment formats. request . The different operator functions described in 8.1.3.2 Supported functions have different corresponding input and output formats.

Figure 8-2 SP422 storage format

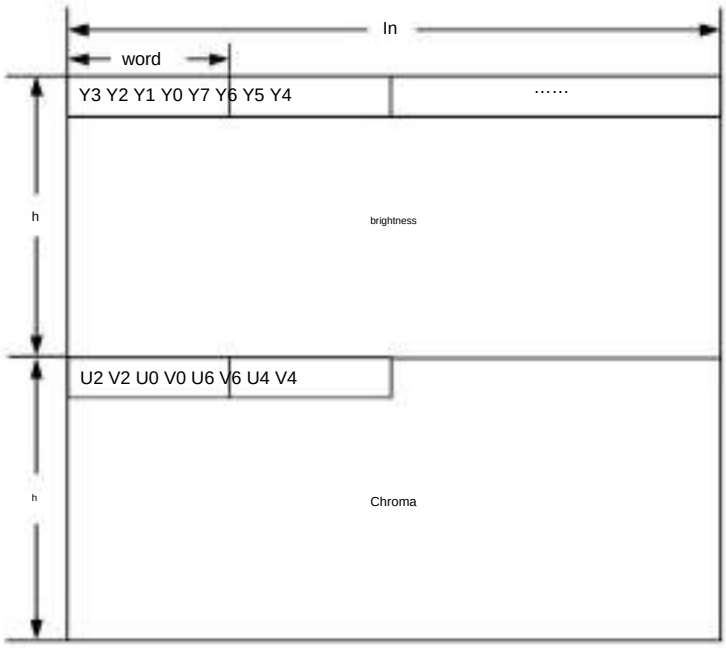


Figure 8-3 SP420 storage format

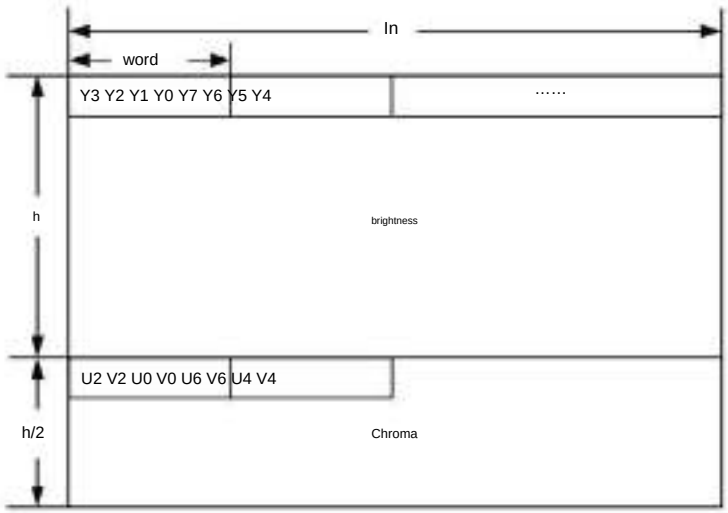


Figure 8-4 Storage of 8bit single component data in Memory

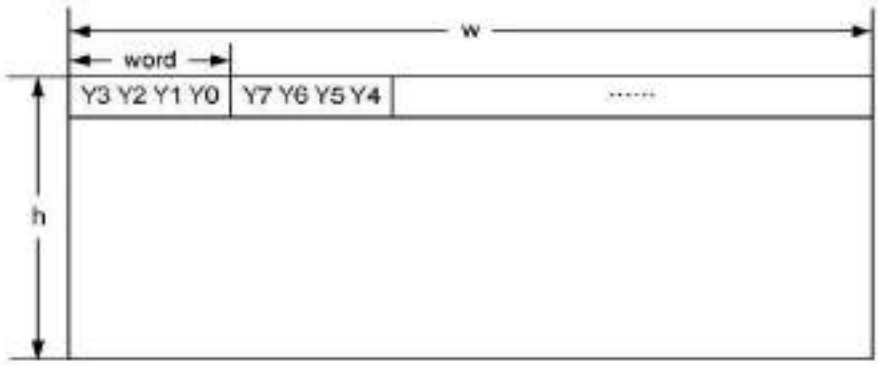


Figure 8-5 Package storage format

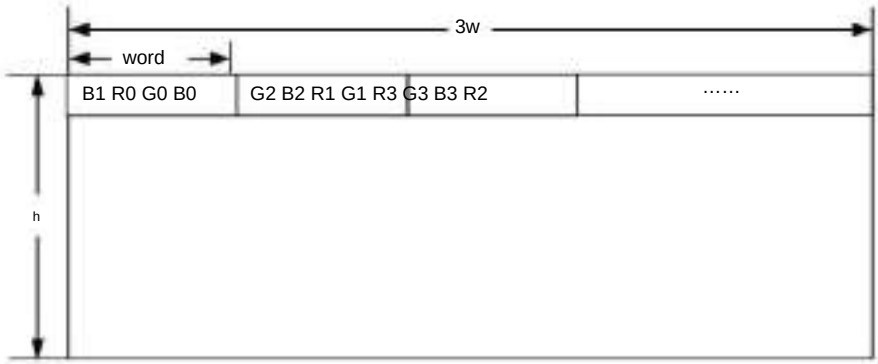


Figure 8-6 Plannar storage format

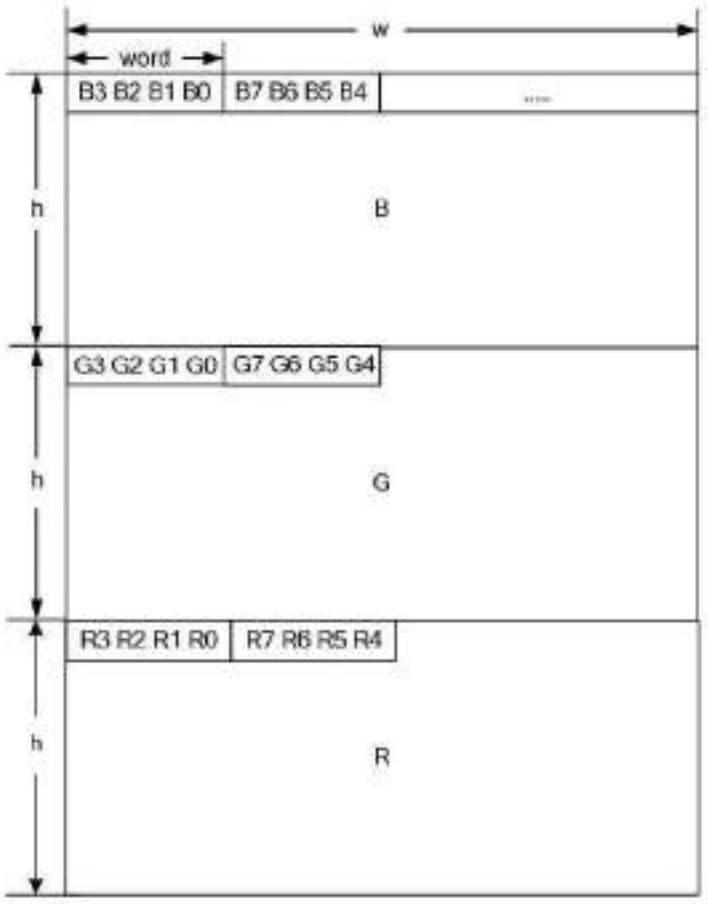


Figure 8-7 Storage of 16bit single component data in Memory

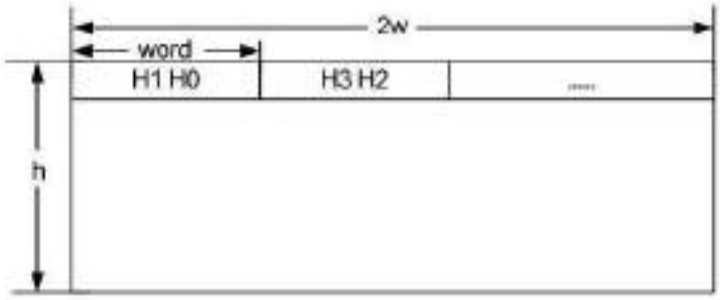


Figure 8-8 Storage of 32bit single component data in Memory

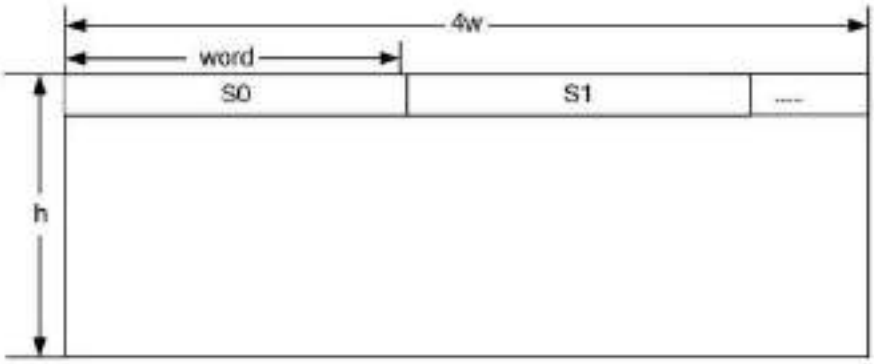


Figure 8-9 Storage of 64bit single component data in Memory

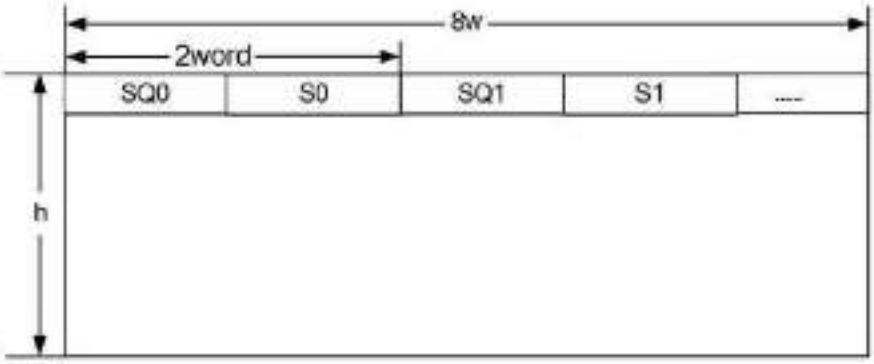


Figure 8-10 Storage of NCC output data in Memory

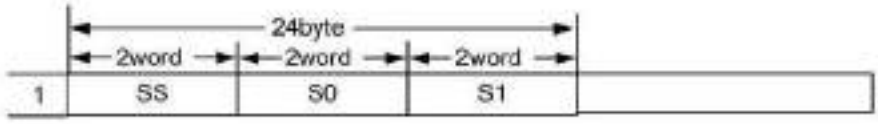


Figure 8-11 Storage of CCL statistics in Memory (sequential storage)

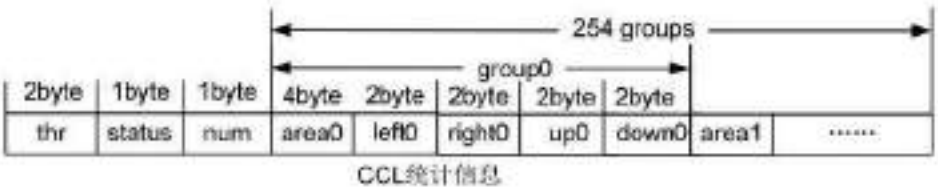
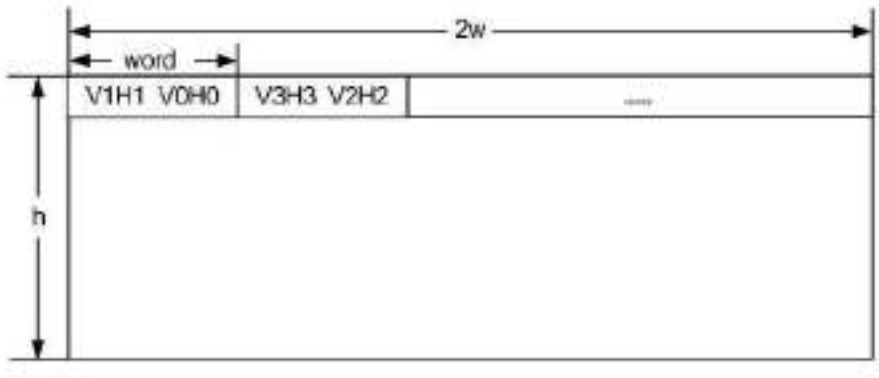


Figure 8-12 Storage of 16bit horizontal and vertical interleaved data in Memory



8.1.3.2 Supported functions

说明

Please refer to the "HiIVE API Reference" for the supported resolutions of each operator described in this chapter.

DMA

(1) Direct copy mode

Realize the fast moving function of the rectangular data area. In this mode, the source data will be directly moved to the target area through the internal fast path of the IVE, and directly overwrite the data in the target area.

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment.

Input and output format: both input and output are 8bit single-component data, as shown in Figure 8-4

(2) Interval copy mode

Realize the function of moving data intervals in rectangular areas. In this mode, the source data will move fixed-size data to the destination area at a given distance in both the horizontal and vertical directions.

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment.

Input and output format: both input and output are 8bit single-component data, as shown in Figure 8-4

Others: source data width width must be an integer multiple of distance

(3) 3-byte memset mode

Realize the memory set function of the rectangular data area, and fill the target area with 3 bytes.

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment.

Input and output format: no input data, output 8bit single-component data, as shown in Figure 8-4

(4) 8-byte memset mode

Realize the memory set function of the rectangular data area, and fill the destination area with 8 bytes as a unit.

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment.

Input and output format: no input data, output 8bit single-component data, as shown in Figure 8-4

Filter

Output the source image after filtering with a 5x5 template.

Address alignment: both input and output addresses and stride require 16-byte alignment, and the output components are configured with the same stride

There are 3 different cases of input and output

formats: ÿInput and output are both 8bit single-component data, as shown in Figure 8-4

ÿInput and output are both SP420 data, as shown in Figure 8-3

ÿ Both input and output are SP422 data, as shown in Figure 8-2

CSC

Color space conversion, support YUV2RGB, YUV2HSV, YUV2LAB, RGB2YUV space conversion.

Address alignment: both input and output addresses and stride require 16-byte alignment, and the configuration of each output component is the same stride

Input and output formats:

ÿ SP420 --> packageÿSP420 --> planar

ÿ SP422 --> packageÿSP422 --> plannar ÿ package-->SP420ÿ

package-->SP422

ÿ plannar-->SP420; plannar-->SP422 SP420 or SP422 format,

as shown in Figure 8-3 and Figure 8-2 . package format, as shown in Figure 8-5 .

In plannar format, as shown in Figure 8-6 .

FilterAndCSC

Filter the YUV SP420/SP422 image with a 5X5 template, and then convert it into YUV2RGB color space and output it.

Address alignment: both input and output addresses and stride require 16-byte alignment, and the configuration of each output component is the same stride

Input and output formats:

ÿ SP420 --> packageÿSP420 --> planar

ÿ SP422 --> packageÿSP422 --> planar

For SP420 or SP422 format, as shown in Figure 8-2 and Figure 8-3 ; for package format, as shown in Figure 8-5 ; for plannar format, as shown in Figure 8-6

Sobel

Do sobel filtering of the 5x5 template for vertical and horizontal directions.

Address alignment: both input and output addresses and stride require 16-byte alignment, and the configuration of each output component is the same stride

Input and output formats:

ÿThe input is an 8-bit single-component image, as shown in Figure 8-4

ÿWhen only H or V is output, as shown in Figure 8-7

ÿ When both H and V are output, as shown in Figure 8-7

MagAndAng

Calculate the magnitude and argument of the image gradient, and support the TO_ZERO thresh operation on the magnitude map.

Address alignment: both input and output addresses and stride require 16-byte alignment, and the configuration of each output component is the same stride

Input and output format: -

Input is 8bit single component graph, as shown in Figure 8-5 - Output is 16bit

single component amplitude graph, as shown in Figure 8-7

ÿThe output is an 8bit single-component argument diagram, as shown in Figure 8-4

Dilate

Binary image 5x5 template dilation.

Address alignment: Both input and output addresses require 16-byte alignment Input and output

format: both input and output are 8bit single-component data, as shown in Figure 8-4

Erode

Binary Image 5x5 Stencil Erosion.

Address alignment: Both input and output addresses require 16-byte alignment Input and output

format: both input and output are 8bit single-component data, as shown in Figure 8-4

Thresh

Threshold the image using a fixed threshold with 8 configurable modes.

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment. Input and output format:

both input and output are 8bit single-component data, as shown in Figure 8-4

And

The source 2 data is ANDed with the source 1 data, and the result is output to the destination area.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: Both input and output addresses require byte alignment, and input and output strides require 16byte alignment. Input and output formats:

ÿInput is source 1 8bit single-

component data ÿ Input is source 2 8bit single-component

data ÿ Output is the result data after operation, which is

8bit single component data, as shown in Figure 8-4

Sub

Source 2 data is subtracted from source 1 data, and the result is output to the destination area.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: both input and output addresses require byte alignment, and input and output strides require 16byte alignment. Input and output formats: ÿ

minuend 8bit single component

ÿSubtrahend 8bit single component

ÿResult data 8bit single component, as shown in Figure 8-4

Or

The OR operation is performed on the data in source image 2 and the data in source image 1, and the result is output to the destination area.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: Both input and output addresses require byte alignment, and input and output strides require 16byte alignment. Input and output formats:

ÿ Both input images are 8bit single-component images

ÿOutput 8bit single component image, as shown in Figure 8-4

Integral

Calculate the integral map, square and integral map of the image, support the separate output of the integral map, the separate output of the square and integral map, and the output of the sum integral map and the square and integral map together (the cumulative sum of the components occupies the lower 28 bits, and the cumulative sum of the squared components occupies the upper 36 bits).

Address alignment: both input and output addresses and stride require 16byte alignment Input and output format: ÿ

Input is 8bit single-component

map, as shown in Figure 8-4

ÿWhen the sum-integral image is output separately, the input is a 32-bit single-component image, as shown in Figure 8-8 ; when the square-and-integral image is output alone or the sum-integral image and the square-and-integral image are output together, the output is a 64-bit single-component image , as shown in Figure 8-9

Histogram

256-level histogram statistics, the input is a single component, and the output is a 256-level histogram statistical value with a bit width of 32bit.

Address alignment method: both input and output addresses and stride require 16byte alignment Input and output

format: ÿInput is 8bit single

component, as shown in Figure 8-4 ÿOutput statistics result is 32bit single

component data, as shown in Figure 8-8

Thresh_S16

Thresholding from Signed 16bit data to 8bit data, supporting 4 comparison modes.

Address alignment: both input and output addresses and stride require 16byte alignment

Input and output format: ÿ

Input 16bit single component data, as shown in Figure 8-7

ÿOutput converted 8bit single-component data, as shown in Figure 8-4

Thresh_U16

Thresholding from unsigned 16bit data to unsigned 8bit data supports 2 comparison modes.

Address alignment: Both input and output addresses and stride require 16byte alignment Input and output

formats:

ÿInput 16-bit single-component data, as shown in Figure 8-7 ÿOutput converted

8-bit single-component data, as shown in Figure 8-4

16BitTo8Bit

16bit data to 8bit linear conversion, support 4 comparison modes.

Address alignment: both input and output addresses and stride require 16byte alignment Input and output

format: ÿ Input 16bit data,

as shown in Figure 8-7 ÿ Output converted 8bit data, as shown

in Figure 8-4

OrdStatFilter

3x3 template order statistics filtering, support median filtering, maximum value, minimum value.

Address alignment: both input and output addresses and stride require 16byte alignment Input and output

format: both input and output are 8bit single-component images, as shown in Figure 8-4

Map

Data mapping assignment, the source data is assigned a new value output through the 256-level unsigned 8bit Map, unsigned 16bit Map or signed 16bit Map table configured by the user.

Address alignment: All input and output addresses and stride require 16byte alignment. Input and output data format:

ÿEnter 8-bit single-component data,

as shown in Figure 8-4 ÿEnter an 8-bit or 16-bit wide mapping table with a

fixed length of 256 entries.

ÿ Output mapped 8bit single component or 16bit data. As shown in Figure 8-4 and Figure 8-7

Add

The weighted sum of two grayscale images can be configured with their own weights.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: both input and output addresses require byte alignment, and both input and output stride require 16byte alignment

Input and output data format: ÿ Input

two 8bit single-component image data, as shown in Figure 8-4

ÿOutput the added 8bit single component image data. As shown in Figure 8-4

Free

The corresponding data of two binary images is XORed.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: both input and output addresses require byte alignment, and both input and output strides require 16byte alignment Input and output data

format: ÿ Input two 8-bit single-

component image data as shown in Figure 8-4 ÿ Output 8-bit single-component image after

XOR Data, as shown in Figure 8-4

NCC

Find the normalized cross-correlation coefficient of two grayscale images with the same resolution.

Image resolution: The resolution of the two input images is required to be the same

Address alignment: the input address requires byte alignment, and the output address and input and output stride both require 16byte alignment. Input and

output data format: ÿ

Input two 8-bit single-component

image data, as shown in Figure 8-4

ÿ There are 3 data to be output, which are the multiplication and accumulation value of two images, the square and accumulation value of image 1 in sequence.

Added value, square and accumulated value of image 2, as shown in Figure 8-10

CCL

8-connected/4-connected region labeling for binary graphs.

Image resolution: widthxheight < 1024x1024 Address alignment: All input

and output addresses and stride require 16byte alignment Input and output data format: ÿInput 8bit single-component image,

as shown in Figure 8-4 , output 16bit

data to indicate the effective connected area of the output

domain minimum area

ÿOutput 8bit data indicating whether the detected connected region exceeds the threshold

ÿ Output the circumscribed rectangle coordinates and areas of each connected region, as shown in Figure 8-11 , and rewrite the original image as an 8-bit single-

component image after the connected region is marked, as shown in Figure 8-4

GMM

GMM background modeling, support GMM background modeling of grayscale image and RGB package image input, the number of Gauss models is 3 or 5.

Address alignment: All input and output addresses and stride require 16byte alignment

Input and output data format: - Input

8bit single component image or RGB package image, as shown in Figure 8-4 and Figure 8-5 - Input model data

ÿOutput 8-bit single-component foreground binary image, as shown in Figure 8-4 ÿOutput

updated model data ÿOutput background data, the

corresponding input is 8-bit single-component image or RGB package image, as shown in Figure 8-4 and Figure 8 -5 shown

CannyHysEdge

The hysteresis thresholding and non-maximum suppression part of Canny edge detection outputs strong and weak edge maps and strong edge coordinate information.

Address alignment: All input and output addresses and stride require 16byte alignment Input and output data format:

ÿInput 8-bit single-component argument diagram, as shown in Figure 8-4 ÿInput

16-bit single-component amplitude diagram, as shown in Figure 8-7

ÿOutput 8bit single-component edge label map, as shown in Figure 8-4

ÿ Output the stack represented by 32bit single-component data, as shown in Figure 8-8 ÿ Output

the stack size, represented by a 32bit data

LBP

LBP local binary mode, which extracts the local texture information of the image.

Address alignment: All input and output addresses and stride require 16byte alignment Input data format: ÿ Input 8bit

single component data ÿ

Output 8bit single component 8bit result data,

as shown in Figure 8-4

NormGrad

Normalized gradient calculation, the gradient components are normalized to 8bit.

Address alignment: All input and output addresses and strides are required to be 16byte aligned, and each output component is required to be configured with the same stride

Input and output data format:

ÿInput 8bit single component data, as shown in Figure 8-4 ÿWhen out_fmt is

0x00, 0x01 or 0x02, the output is 8bit single component data, as shown in Figure 8-4 ; when out_fmt is 0x03, the output is 16bit H and V interleaved data, as shown in Figure 8-12

LKOpticalFlow

LK optical flow motion estimation, supports multi-layer pyramid input, 1~4 layers can be configured, and supports up to 500 corner points.

Address alignment: All input and output addresses and stride require 16byte alignment

Input and output data format: ÿ Input

the 8-bit single-component single/multi-layer pyramid image of the previous frame, and each layer image is shown in Figure 8-4

ÿInput the current frame 8bit single-component single/multi-layer pyramid image, each layer image is shown in Figure 8-4

ÿInput the corner coordinates of the previous frame, and each coordinate is represented by two 32bits, representing horizontal coordinates and vertical coordinates respectively.

Coordinates, effective bits [21:0] - The

corner coordinates of the current frame are used as both input (only when using the initial optical flow) and output - the output mode can be

configured, 0 means only output the corner coordinates of the current frame, and 1 means Output current frame corner coordinates and status

information, 2 is to output the current frame corner coordinates, status information, err information

STBoxFltAndEigCalc

Box filtering in the calculation process of Shi-tamosi-like corner points, calculating the corner point response value and the maximum corner point response value.

Address alignment: All input and output addresses and stride require 16byte alignment Input and output data format:

ÿInput 16-bit horizontal and vertical interleaved data, as shown in Figure 8-12 ÿOutput 16-bit single-component

data, as shown in Figure 8-7 ÿOutput 16-bit maxEig

STCandiCorner

Realize the selection of corner points from Shi-Tomasi-like candidate corner points.

Image resolution: The resolution of the input two images is required to be the same

Address alignment: All input and output addresses require byte alignment, and stride requires 16byte alignment. Input and output data format: ÿ

Input is 8bit single-component image

ÿ Output is 8bit single-component image, as shown

in Figure 8-4

GradFg

Calculate the gradient foreground image based on the gradient information of the background image and the current frame image.

Address alignment: All input and output addresses and stride require 16byte alignment Input and output data format: ÿInput

the background difference foreground

image, as shown in Figure 8-4

ÿ Input current gradient interpolation image

ÿInput background gradient interpolation image, as shown in Figure 8-12 ÿOutput

gradient foreground image, as shown in Figure 8-4

MatchBgModel

CodeBook-based background model matching.

Address alignment: All input and output addresses and strides are required to be 16byte aligned, and each output component is required to be configured with the same stride

Input and output data format: ÿ

Input 8bit single component current grayscale image

ÿInput 8bit single-component foreground state flag image, as shown in Figure 8-4

ÿInput 24byte model data; ÿOutput 8bit single

component background difference foreground image

ÿOutput 8bit single-component inter-frame difference map

ÿOutput 8bit single-component foreground state flag map, as shown in Figure 8-4 ÿOutput 24byte

model data ÿOutput 64bit data statistics

UpdateBgModel

Background model update based on CodeBook.

Address alignment: All input and output addresses and strides are required to be 16byte aligned, and each output component is required to be configured with the same stride

Input and output data format:

ÿInput 8bit single-component foreground state flag image, as shown in Figure 8-4

ÿInput 24byte model data; ÿOutput 8bit single

component foreground state flag image ÿOutput 8bit single component

background grayscale image ÿOutput 8bit single

component grayscale image of changing state

ÿOutput 8bit single component change state foreground image, as shown in Figure 8-4

ÿOutput 16bit single component change status pixel life time, as shown in Figure 8-7 ÿOutput 24byte model

data ÿOutput 64bit data statistics

ANN_MLP_Predict

The ANN_MLP prediction task of a single feature sample supports up to 6 hidden layers, supports up to 64 sample vector inputs, and a maximum of 1024 neurons in the input layer, and no more than 256 neurons in each other layer.

Address alignment: All input and output addresses require 16byte alignment Input and output

data format: ÿ Input 32-bit input

layer feature vector data, as shown in Figure 8-8 ÿ Input 8-bit model data, as shown in Figure 8-4

ÿ Input 16-bit search Table data, as shown in Figure 8-7

ÿOutput 32bit output layer data, as shown in Figure 8-8

SVM_Predict

SVM prediction of a single feature sample supports a maximum of 1024-dimensional input vectors.

Address alignment: All input and output addresses require 16byte alignment

Input and output data format:

ÿInput 32ibt feature vector data, as shown in Figure 8-8

ÿInput support vector, 8bit single component, as shown in Figure 8-4

ÿInput 16bit lookup table data, as shown in Figure 8-7 ÿInput 8bit

decision function, as shown in Figure 8-4

ÿOutput 16bit predicted voting result vector, as shown in Figure 8-7

Resize

Support bilinear interpolation (bilinear) and area interpolation (area) scaling, support up to 64 image inputs, horizontal scaling factor [1, 16], vertical scaling factor [1, 16], but horizontal and vertical scaling factors cannot be at the same time 1.

Address alignment: All input and output addresses and strides require 16byte alignment Input and output

data format: ÿInput 8bit single-

component image or RGB Plannar image, as shown in Figure 8-4 and Figure 8-6 . ÿ Outputs a scaled image,

corresponding to the input image format. Zoom mode:

ÿThe image scaling mode in one task must be the same

GMM2

GMM background modeling supports grayscale image and RGB package image input, and the number of Gauss models supports 1-5.

Address alignment: All input and output addresses and stride require 16byte alignment Input and output

data format:

ÿInput 8-bit single-component image or RGB package image, as shown in Figure 8-4 and Figure 8-5 ÿInput 16-bit pixel

factor map, pixel factor includes high 8-bit update time, low 8-bit sensitivity information, as shown in Figure 8-7 Show

ÿ Input model data

ÿOutput 8bit single-component foreground binary image, as shown in Figure 8-4

ÿ Output updated model data ÿ Output

background image, corresponding to input image type

ÿOutput 8-bit model hit information, as shown in Figure 8-4 , the lower 1 bit indicates whether the model is hit or not, and the upper 7 bits indicate the hit model index

CNN

Convolutional neural network supports array image processing, and each operation supports up to 64 image block inputs.

Address alignment: All input and output addresses and stride require 16byte alignment Input and

output data format:

— Input 8bit image data or RGB_Planar image data, as shown in Figure 8-4 and Figure 8-6 respectively , in the array All image types, resolutions must be the same as the model

— Enter model data

— Output N feature vectors with a maximum dimension of 1024, N is the same as the number of input images, and the feature vectors are used as The input of the CNN fully connected layer.

SAD

The cumulative sum of the absolute values of the corresponding pixel differences of the two images is calculated in blocks.

Image resolution: The width and height are required to be configured as integer multiples of the block size.

Address alignment: All input addresses and stride require byte alignment, and output addresses require byte alignment

Input and output data format:

ÿThe input is 2 frames of 8-bit single-component images with the same resolution, as shown

in Figure 8-4 . ÿThe output result depends on the output mode (out_fmt)

configuration: (1) Composite 16bit SAD output mode, output 16bit SAD value map according to the specified block size, and output binarized 8bit SAD binary map at the same time, as shown in the figure 8-7 and Figure 8-4 .

(2) Composite 8bit SAD output mode, output 8bit SAD value map according to the specified block size, and output 8bit SAD binary map after binarization, as shown in Figure 8-4 .

(3) Single 16bit SAD output mode, output 16bit SAD value map according to the specified block size, as shown in the figure 8-7 shown.

(4) Single 8bit SAD output mode, output 8bit SAD value map according to the specified block size, as shown in Figure 8-4 .

(5) Single binary image SAD output mode, output binarized image according to the specified block size 8bitSAD binary image, as shown in Figure 8-4 .

8.1.4 IVE register overview

An overview of the IVE registers is shown in Table 8-1 .

Table 8-1 IVE register overview (base address is 0x1104_0000)

offset address name		describe
0x0000	IVE_START	IVE boot configuration register
0x0004	INT_EN	IVE Interrupt Enable Register
0x0008	INT_RW	IVE clear interrupt register
0x000C	INT_STATUS	IVE Interrupt Status Register
0x0010	LIST_POINTER	Linked list first address register
0x0014	IVE_STATUS	IVE working status register
0x0018	IVE_TASK_ID	IVE last completed task ID number register
0x0030	NODE_CLK_VALUE cycle number register	consumed by a node
0x0034	CLK_GT_EN	Clock Gating Registers for IVE Internal Blocks

offset address name		describe
0x0040	NODE_DONE_CNT	Completed Node Count Register
0x0044	LIST_DONE_CNT	Completed linked list register
0x0054	AXI_INFO	Read and write outstanding number registers
0x0060	IVE_OVER_TIME_THR timeout interrupt threshold register	
0x0064	IVE_OVER_TIME_CNT Operator working cycle number dynamic counting register	
0x0068	CHAIN_STAT_CLK_VAL UE	The cycle number register consumed by the last linked list
0x006C	CHAIN_CYCLE_CNT Current linked list cycle number real-time counting register	

Table of contents

illustration catalog

table of contents

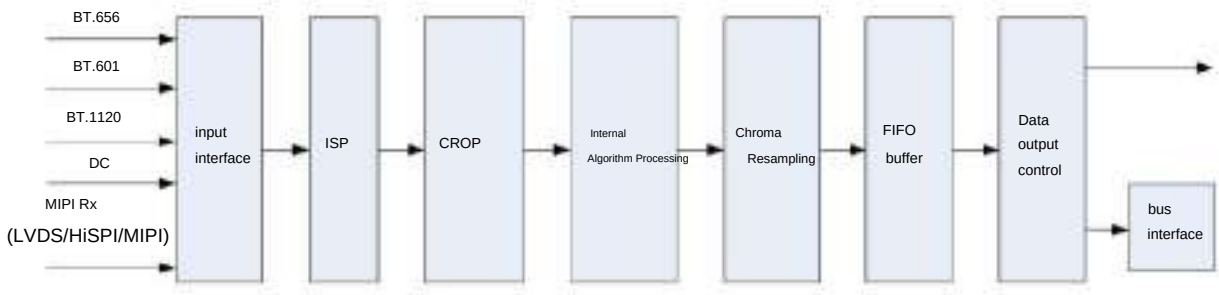
9 video interface

9.1 VICAP

9.1.1 Overview

The video capture unit VICAP (Video capture), can receive video data through BT.656/601, BT.1120 interface and DC (Digital Camera), MIPI Rx (including MIPI, LVDS, HiSPi) interface, and store it in the specified memory area or Send directly to the VPSS module. VICAP supports embedded ISP processing unit and can directly connect to external raw data (BAYER RGB data). The functional block diagram of VICAP is shown in Figure 9-1 .

Figure 9-1 Functional block diagram of VICAP



9.1.2 Features

VICAP has the following features:

- The maximum input resolution is 4608x3456, the
- external support is 1 interface, the maximum data bit width is 16bit, the
- internal support is 1 port and 1 channel video processing, and the channel supports interlaced and progressive input modes
- Support BT.656, BT.601, BT.1120 and DC, MIPI, LVDS, HiSPi and other timing
- Support SMPTE293M/ITU-R BT.1358 timing (480P/576P)
- support flash trigger

Support shutter trigger Support

sensor master-slave mode

Support embedded ISP processing function

Support data acquisition within a specified window

Support offline output data to DDR and online output data to VPSS

The output format supports storage modes:

ÿ SPYCbCr 4:2:2 mode

ÿ SPYCbCr 4:2:0 mode

9.1.3 Functional description

9.1.3.1 Typical applications

VICAP is a video input capture unit that supports multiple timing inputs. It stores the captured video data in DDR or sends it to VPSS online. The system can be configured with different functional modes so that it can flexibly adapt to different external input video interfaces. , supports a variety of external input devices.

VICAP occupies a total of 23 pins, 1 clock, 2 external synchronization signals (with pin multiplexing), 16 data lines, 1 shutter trigger signal (with pin multiplexing), and 1 flash trigger signal (with pin multiplexing). Pin multiplexing), 2 sensor slave mode timing output pins.

VICAP module has 1 port and 1 channel in total. 1 port can analyze the timing of 1 docking chip, and 1 channel can process 1 video signal.

The typical input of VICAP has the following 2 types:

1 way 8M

1 way 2M

9.1.3.2 Functional principle

ITU-R BT.656 YCbCr4:2:2

(1) Horizontal timing

In the ITU-R BT.656 protocol, the synchronization signal is integrated in the data stream, and the special bytes SAV and EAV in the data stream represent the start and end of valid line data respectively. In the video data stream, the terminal of the timing reference codeword composed of FF 00 00 (FF, 00 is the reserved value of image coding data, which is non-image data) marks the next byte as SAV or EAV, ITU-The row data stream format of R BT. 656 is shown in Table 9-1 .

Table 9-1 ITU-R BT.656 YCbCr 4:2:2 row data format

timing reference code	line blanking area	timing reference code	720 effective pixels YCbCr 4:2:2
FF 00 00 EAV 80 10 … 80 10	FF 00 00 SAV Cb0 Y0	Cr0 Y1 … Cr718 Y719	

The difference between SAV and EAV is distinguished by the special bit "H" of SAV/EAV, and SAV/EAV also includes the vertical blanking bit "V" and the field indicator bit "F". The specific description of SAV/EAV is shown in Table 9-2 .

Table 9-2 SAV/EAV format

bit[7]	bit[6](F)	bit[5](V)	bit[4](H)	bit[3:0](P3ÿP0)
Fixed value 1 field indicator bit	1st fieldÿF=0 2nd fieldÿF=1	vertical blanking bit VBIÿV=1 Active videoÿV=0	SAVÿH=0 EAVÿH=1	Check Digit

The ITU-R BT.656 protocol uses 8 effective reserved bits to define effective SAV and EAV, and 4 parity bits can correct 1-bit errors and detect 2-bit errors. Valid SAV/EAV values are shown in Table 9-3 .

Table 9-3 Valid SAV/EAV values

coding	binary value	field number	vertical consumption
SAV	10000000	1	-
EAV extension	10011101	1	-
SAV	10101011	1	yes
EAV extension	10110110	1	yes
SAV	11000111	2	-
EAV extension	11011010	2	-
SAV	11101100	2	yes
EAV extension	11110001	2	yes

The 4 effective reserved bits also play the role of error correction. P0, P1, P2, and P3 are determined by F, V, and H bits, as shown in Table 9-4 .

Table 9-4 ITU-R BT.656 error correction code table

F	IN	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

in:

P0=F^V^H

P1=F^V

P2=F^H

P3=V^H

(2) Vertical timing

The vertical timing is also realized through the "F" and "V" of the timing reference code SAV/EAV. The vertical timing of typical 525-line and 625-line video systems is shown in Figure 9-2 and Figure 9-3 .

Figure 9-2 Vertical timing of 525-line 60 field/second video system

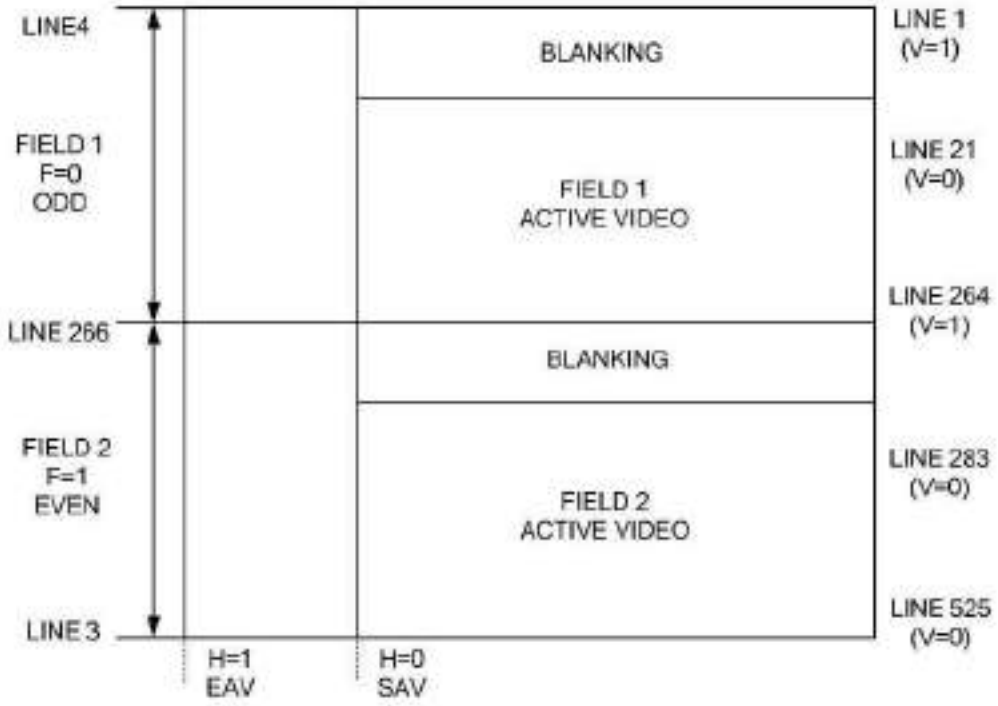
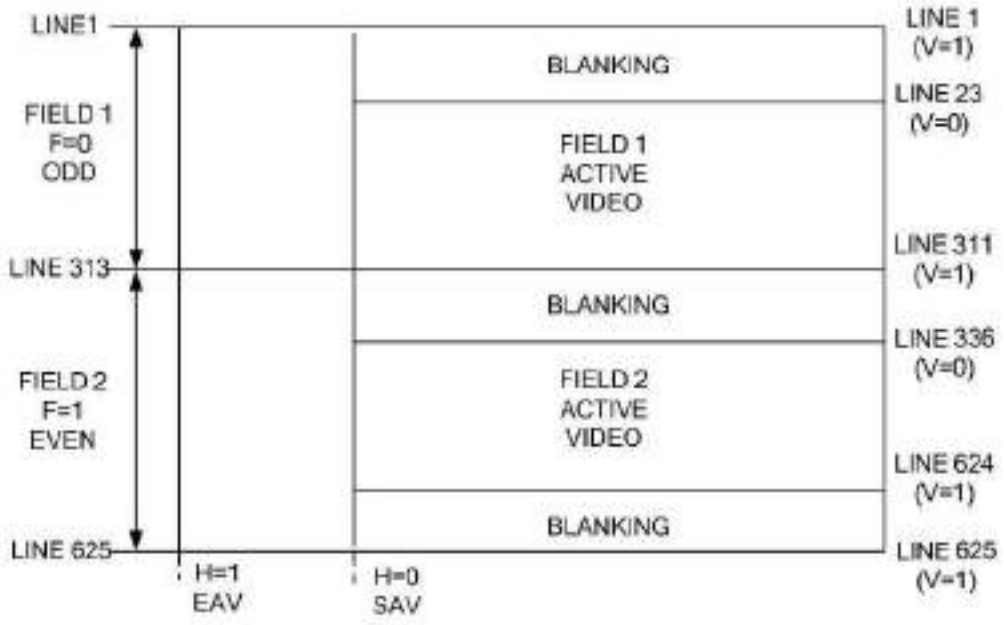


Figure 9-3 Vertical timing of 625-line 50 fields/second video system



Note: VICAP only recognizes vertical timing based on SAV/EAV, and does not limit which row it is in.

BT 1120 (HD) interface timing

VICAP supports high-definition interface timing with Y/C separate input. At this time, two data ports are needed, one port is used to transmit brightness, and the other port is used to transmit chroma, as shown in Figure 9-4 and Figure 9-5 .

Figure 9-4 HD interface input timing horizontal timing

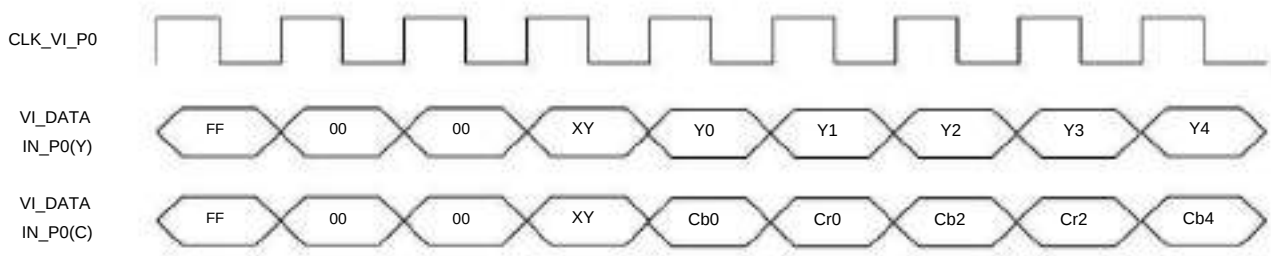
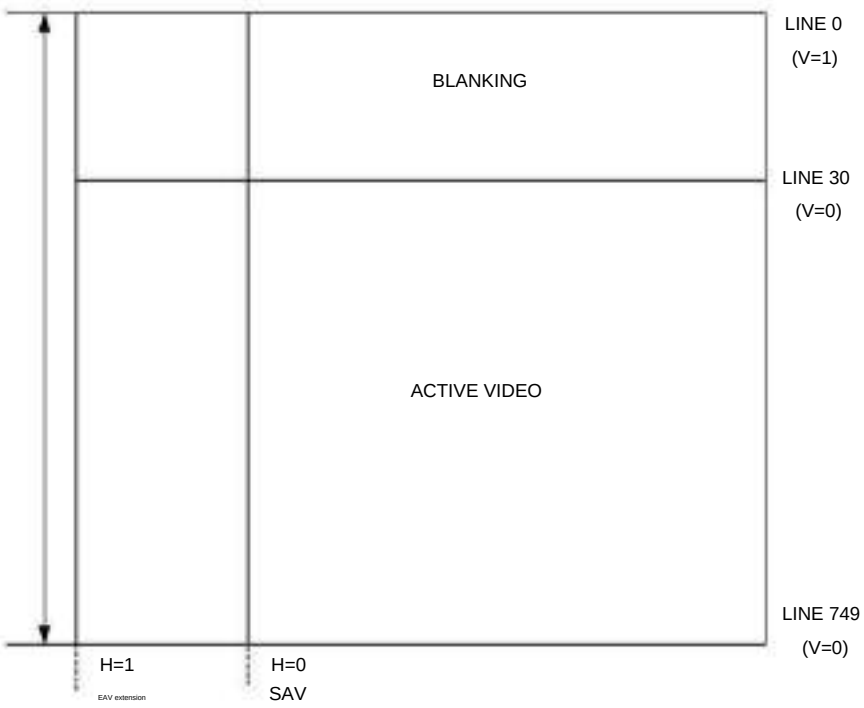


Figure 9-5 HD interface input timing vertical timing

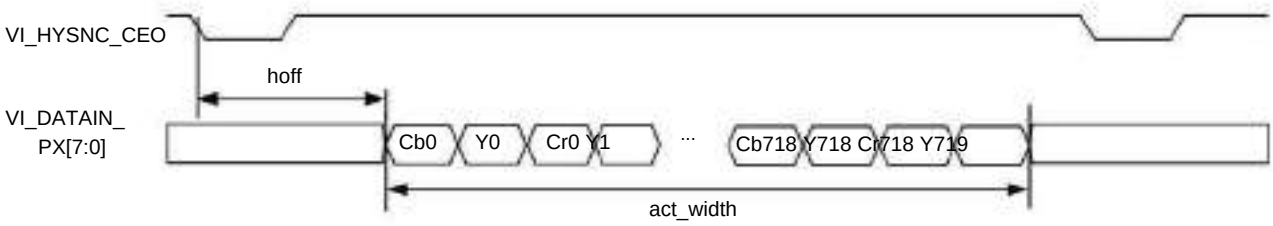


ITU-R BT.601 YCbCr4:2:2

(1) Horizontal timing

A horizontal pulse indicates the start of a new line as shown in Figure 9-6 . After hoff (configurable, the value of NTSC525 line system is 244, the value of the PAL625 line system is 264 clocks), the blanking area before the line ends, and enters the effective data area of the line, and after act_width (configurable, the typical value is 720 or 704) clocks, the effective area of the line ends and enters the line back blanking zone. Horizontal sync polarity is configurable.

Figure 9-6 ITU-R BT.601 horizontal timing diagram

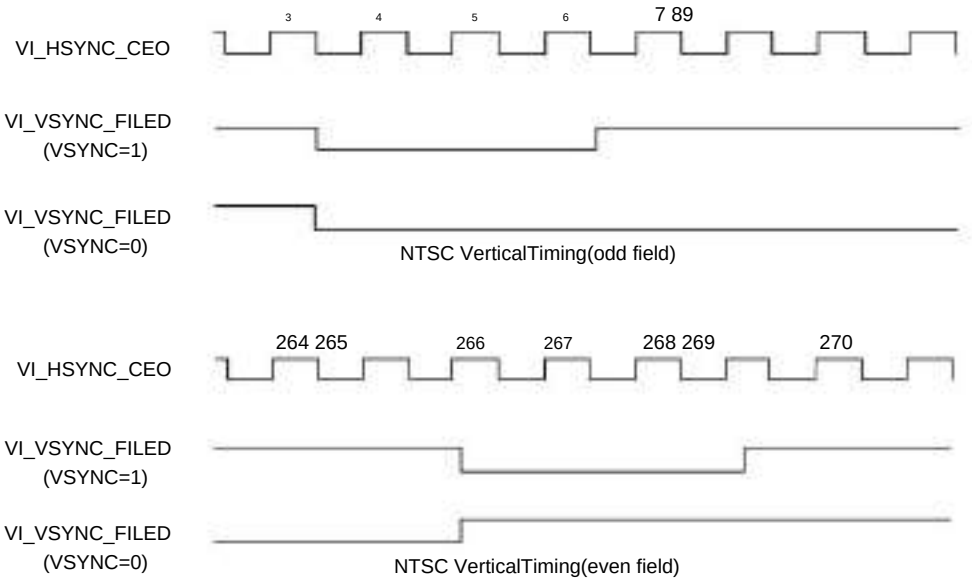


(2) Vertical timing

Recommendation ITU-R BT.601: The signal VSYNC/FIELD is used as the vertical synchronization signal. The pulse of VSYNC or the transition of FIELD marks the beginning of the parity field. VICAP supports the following two vertical synchronization methods.

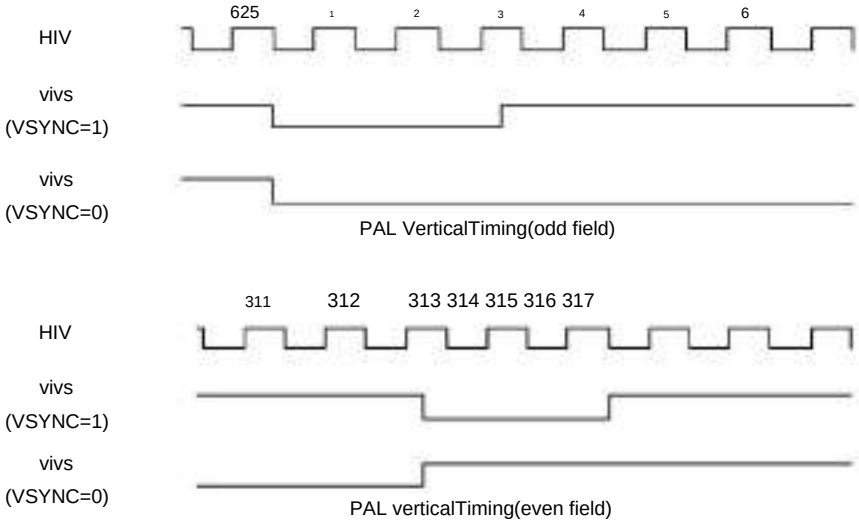
The vertical timing diagrams of VI in NTSC system (525 lines) and PAL system (625 lines) are shown in Figure 9-7 and Figure 9-8 , where VI_HSYNC_VD is the horizontal synchronization pulse, and VI_VSYNC_FIELD is the vertical synchronization pulse when VSYNC=1 ; When VSYNC=0, it is the vertical synchronous signal.

Figure 9-7 NTSC vertical synchronization timing diagram



Under the NTSC interlaced scanning system, the vertical synchronous signal of the first field changes to low level at the beginning of line 4, and after the low level lasts for 3 lines, it changes to high level at the beginning of line 7. VICAP receives 240 lines of data starting at line 22 and ending at line 261. The vertical synchronous signal of the second field becomes low level in the middle of the 266th line, and changes to the high level in the middle of the 269th line after the low level lasts for 3 lines. VICAP receives 240 lines of data starting from line 285 and ending with line 524.

Figure 9-8 PAL system vertical synchronization timing diagram



In the PAL interlaced scanning system, the vertical synchronous signal of the first field changes to low level at the beginning of the first line, and after 2.5 lines of low level, it changes to high level in the middle of the third line. VICAP receives 288 lines of data starting at line 24 and ending at line 310. The vertical sync signal of field 2 becomes low in the middle of line 313,

After 2.5 lines of low level, the starting position of line 316 becomes high level. VICAP receives 288 lines of data starting at line 336 and ending at line 623.

The above two are typical BT.601 vertical timings. VICAP internally supports configurable number of lines between field start and field effective line start, field effective line number, and vertical sync polarity.

Digital Camera Interface Timing

(1) Horizontal timing

When VICAP is connected to a digital camera, VI_HSYNC_VD indicates a valid data signal, and the polarity of the valid data signal can be configured. The horizontal timing is shown in Figure 9-9 .

Figure 9-9 Digital camera horizontal timing sequence

(2) Vertical timing

VICAP supports two vertical timing pulse modes and row effective mode, as shown in Figure 9-10 and Figure 9-11 . Vertical sync polarity is configurable.

Figure 9-10 Digital camera vertical timing pulse mode

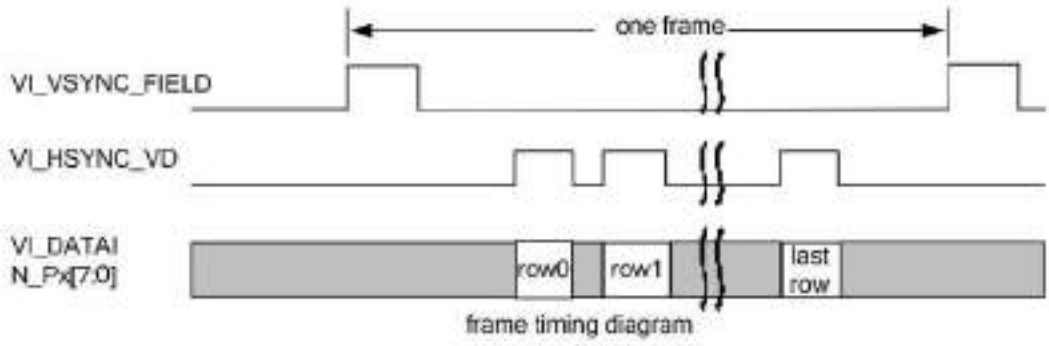
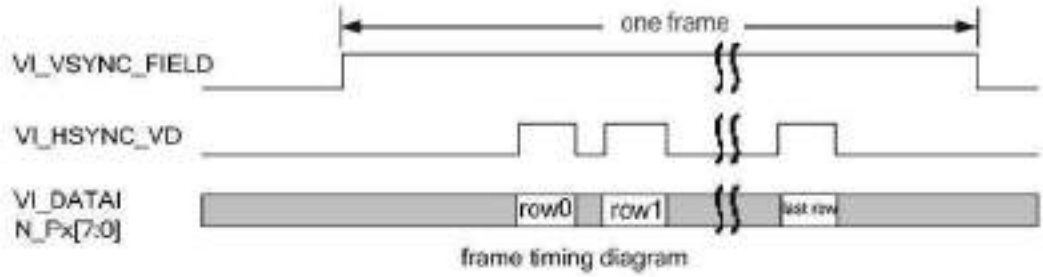


Figure 9-11 Digital camera vertical timing line effective mode

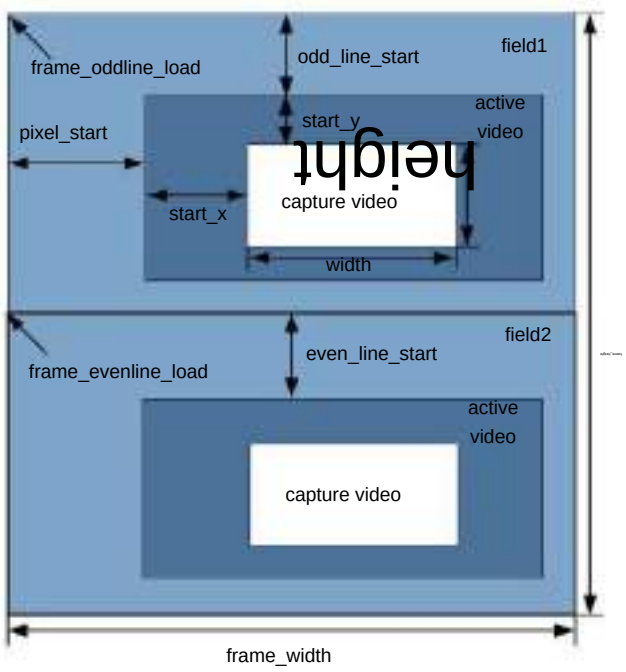


For the internal processing of VICAP, these two timings are the same. VICAP detects a rising edge or falling edge, which is considered as the beginning of a frame, and then detects the data valid signal to determine whether the current data is valid.

9.1.3.3 Image CROP

The effective video range is shown in Figure 9-12 . Starts after horizontal blanking and vertical blanking. However, the actually displayed viewing area is often included within the range of the effective video, and is slightly reduced relative to the boundary of the effective video, in order to avoid edge effects.

Figure 9-12 Relationship between effective image area and horizontal and vertical blanking



9.1.3.4 Image storage mode

Image storage modes include:

1. YUV data storage

Semi-planar YCbCr storage.

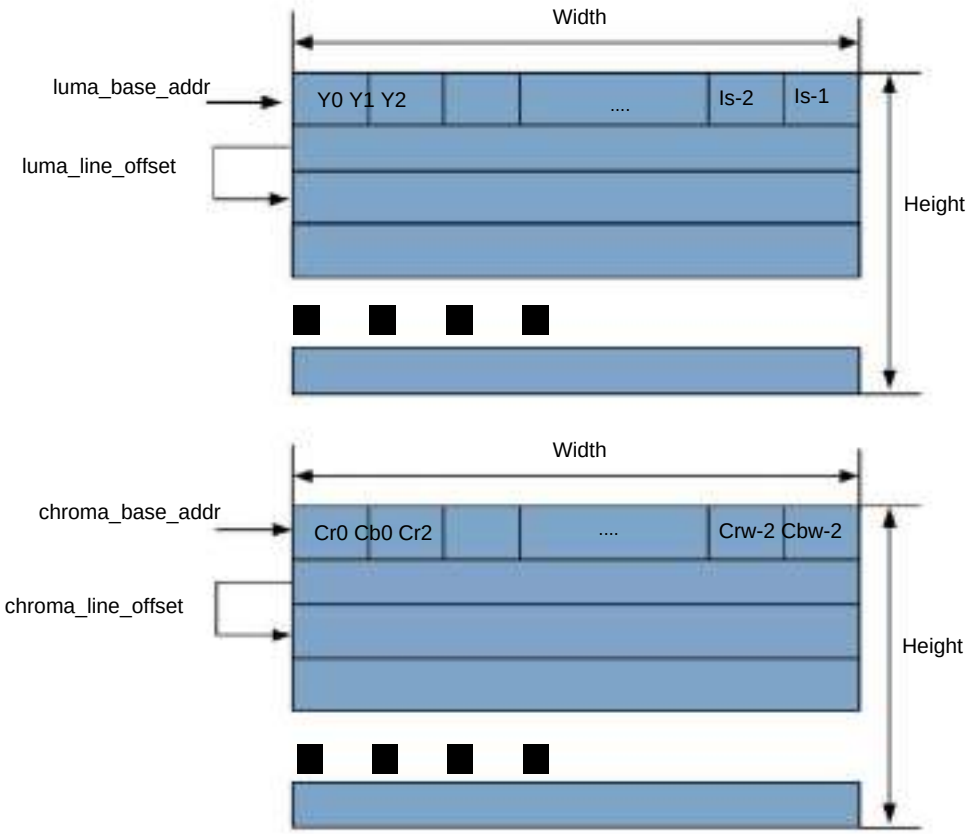
After the system sets the viewing area, the read-in data is stored in a semi-planar manner, that is, the luminance component and chrominance component are stored in the luminance storage space and chrominance storage space in DDR respectively.

In one line, the luma and chrominance components are stored consecutively.

The storage between two consecutive lines can be defined by the system-defined storage interval parameter offset between the beginning of the line and the

beginning of the line. The storage location of luma and chrominance components in DDR is indicated by the starting address base_addr. The storage structure of the YCbCr4:2:2 data captured by the VI is shown in Figure 9-13 .

Figure 9-13 YCbCr4:2:2 storage mode



2. RAW data storage

Stored as a single component.

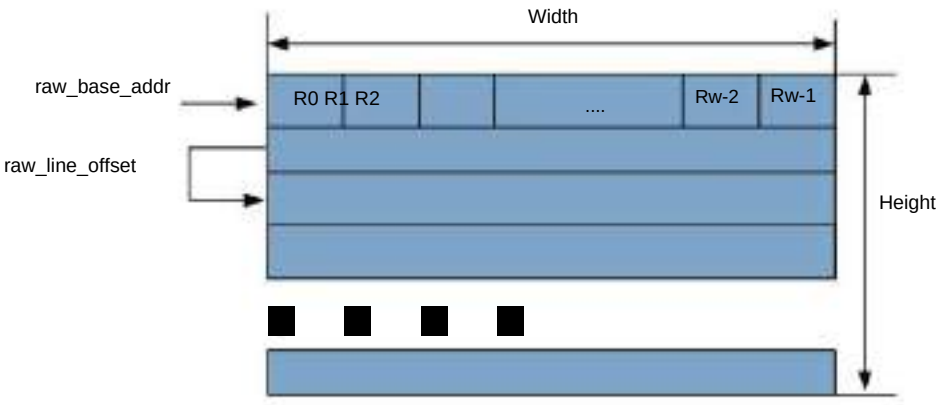
Within 1 row, RAW data is stored consecutively.

The storage between two consecutive lines can be defined by the system-defined storage interval parameter offset between the beginning of the line and the beginning of the line.

The memory location in DDR is indicated by the starting address base_addr.

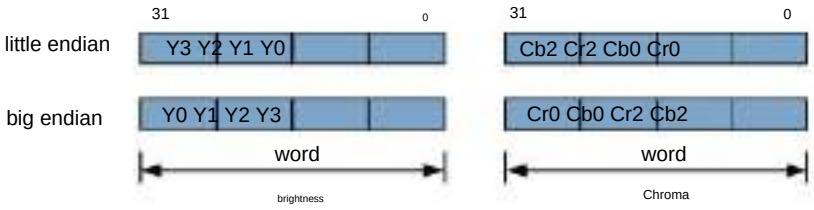
The storage structure of the RAW data captured by the VI is shown in Figure 9-14 .

Figure 9-14 RAW DATA storage mode



In DDR, data storage is in word (32bit) unit. A 32bit word is composed of 4 8bit pixels. When 4 bytes constitute a word, there are two ways: big endian and little endian. Figure 9-15 uses luma and chrominance components as an example to illustrate the storage methods of big endian and little endian.

Figure 9-15 big endian and little endian image storage modes



VICAP only supports little endian way to store data to DDR, and the storage address is 16byte aligned.

9.1.4 Working method

9.1.4.1 reg_newer function of VICAP

Before the software enables a VICAP channel, the software should complete the following operations:

ÿComplete the configuration of VICAP attribute registers.

ÿWrite the reg_newer bit as "1" to inform the VICAP module that the current register is ready. After VICAP is enabled, the VICAP logic starts to work. When a field/frame arrives, there will be: ÿ If reg_newer is 0, VICAP will not receive data, and the hardware state will be set to SNOOZE (based on The following hardware states are used in Figure 9-16), waiting for the arrival of the data of the next field/frame.

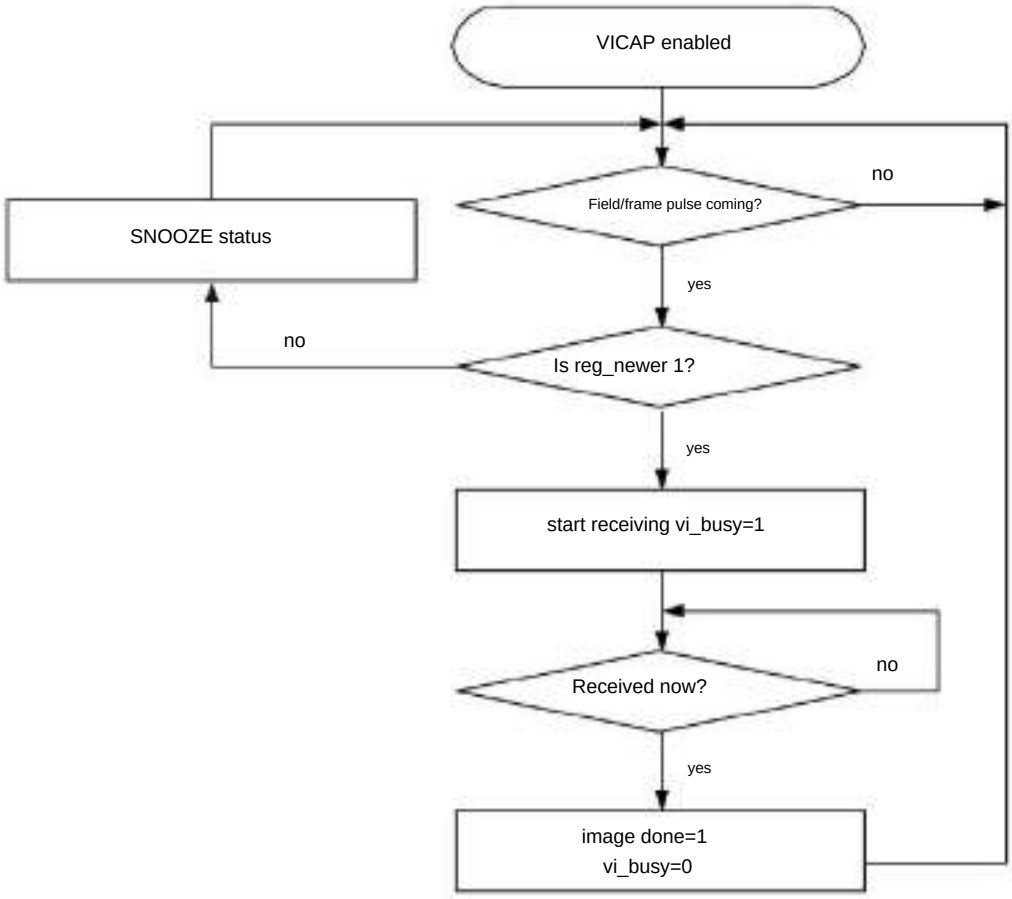
ÿ If reg_newer is 1, start to receive data, give register update interrupt (reg_update_int) at the same time, and set the hardware status to busy.

After receiving the current data, clear the hardware busy state. When the next field/frame arrives, then: ÿ If reg_newer is 0, give up receiving the next field/frame data. ÿIf reg_newer is 1, it can continue to receive the data of the next field/frame following the previous data.

9.1.4.2 Hardware workflow

The hardware workflow of VICAP is shown in Figure 9-16 .

Figure 9-16 VICAP hardware workflow

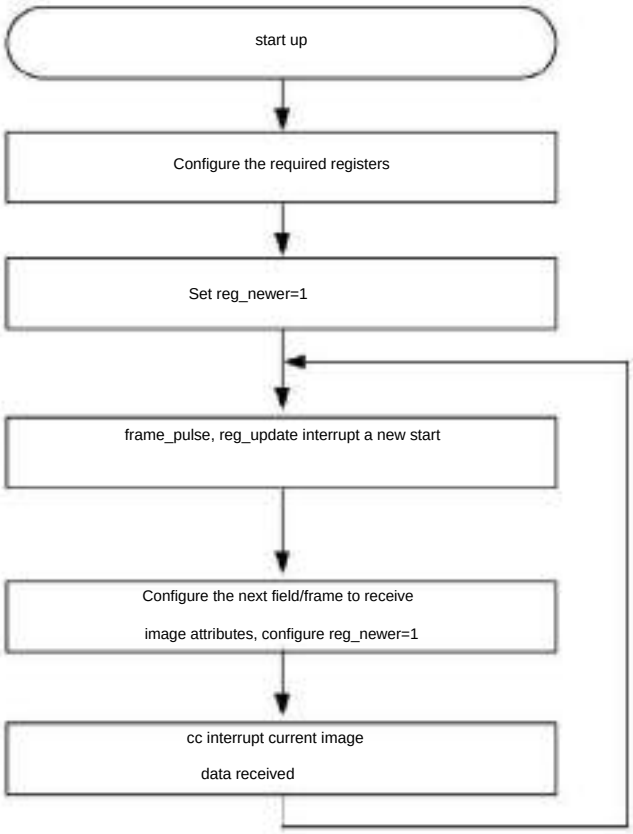


When VICAP is working, VICAP will detect the reg_newer bit when the next field arrives after each field/frame data is received. If the reg_newer bit is 1 (indicating that the software has updated or confirmed the VICAP register), VICAP will automatically load the register value configured by the software to the working register (the working register software cannot be accessed), then clear the reg_newer bit to 0, and start receiving the next field/frame data. Otherwise, start receiving data only when reg_newer is 1 and a new field/frame arrives.

9.1.4.3 Software configuration process

In the interrupt mode, the operation flow of the software is shown in Figure 9-17 .

Figure 9-17 Software operation process



In the case of using BT.656 mode, BT.1120 mode, MIPI Rx and digital camera interface, there is no need to configure the timing register. In BT.601 mode, you also need to configure timing registers, which include vertical synchronization registers and horizontal synchronization registers.

9.1.5 VICAP register overview

An overview of the VICAP registers is shown in Table 9-5 .

Table 9-5 VICAP register overview (base address is 0x1138_0000)

offset address name		describe	page number
0x0000 WK_MODE		Global Working Configuration Register	9-18
0x0010	AXI_CFG	bus configuration register	9-19
0x0014 MAC_CFG		MAC configuration register	9-19
0x0030	CH_SEL	Channel Input Data Select Register	9-20
0x0040	DES_SEL	DES Input Data Select Register	9-21
0x0050	ISP_SEL	ISP Input Data Select Register	9-22

offset address name		describe	page number
0x0230	DES_CROP0_START	0 area CROP start position register	9-53
0x0234	DES_CROP0_SIZE	0 area CROP size setting register	9-54
0x0270	DES_CFG	DES configuration register	9-54
0x0284	DES_SIZE	DES store size register	9-55
0x0290	DES_FADDR	DES storage base address register	9-55
0x0294	DES_STRIDE	DES store line spacing register	9-55
0x029C	DES_BUF_CFG	DES bus BUF control register	9-56
0x02F0	DES_INT	DES Raw Interrupt Register	9-56
0x02F8	DES_MASK	DES Interrupt Mask Register	9-57
0x0500	LINE_BUF_CFG	LINE_BUF Control Register	9-58
0x0504	LINE_BUF_REG_NEWER	LINE_BUF update register	9-59
0x0510	LINE_BUF_ID_CFG	LINE_BUF receive ID selection register	9-60
0x0520	LINE_BUF_CROP_CFG	CROP enable register, immediate register	9-60
0x0530	LINE_BUF_CROP0_START	0 zone CROP start location register, immediate register	9-61
0x0534	LINE_BUF_CROP0_SIZE	0 area CROP size register, immediate register	9-61
0x0550	LINE_BUF_WIDTH	LINE_BUF image width register	9-62
0x0554	LINE_BUF_HEIGHT	LINE_BUF image height register	9-62
0x05F0	LINE_BUF_INT	LINE_BUF Raw Interrupt Register	9-62
0x05F8	LINE_BUF_MASK	LINE_BUF interrupt mask register	9-63
0x0600	SRC_CTRL	SRC Control Register	9-64
0x0604	SRC_REG_NEWER	acquisition control register	9-65
0x0670	SRC_CFG	configuration register	9-66
0x0684	SRC_SIZE	SRC Storage Size Register	9-66
0x0690	SRC_FADDR	SRC storage base address register	9-67
0x0694	SRC_STRIDE	SRC Store Line Spacing Register	9-67
0x069C	SRC_BUF_CFG	SRC Bus BUF Control Register	9-68

offset address name	describe	page number
0x06F0 SRC_INT	SRC Raw Interrupt Register	9-68
0x06F8 SRC_MASK	SRC Interrupt Mask Register	9-69
0x1000 CH_CTRL	Channel Control Register	9-70
0x1004 CH_REG_NEWER acquisition control register		9-71
0x1034 CH_DLY_CFG channel input image start interrupt delay configuration register 9-72		
0x1080 CH_WCH_Y_CFG WCH module Y component configuration register		9-72
0x1084 CH_WCH_Y_SIZE WCH Module Y Component Storage Size Register 9-73		
0x1090 CH_WCH_Y_FADD R	WCH module Y component storage base address register 9-74	
0x1094 CH_WCH_Y_HADD R	WCH module Y component header information storage base address register	9-74
0x1098 CH_WCH_Y_STRID AND	WCH module Y component line offset register	9-75
0x109C CH_WCH_Y_BUF_ CFG	CH_DES bus BUF control register	9-75
0x10A0 CH_WCH_C_CFG WCH module C component configuration register		9-76
0x10A4 CH_WCH_C_SIZE WCH module C component storage size register 9-77		
0x10B0 CH_WCH_C_FADD R	WCH Module C Component Storage Base Address Register 9-77	
0x10B4 CH_WCH_C_HADD R	WCH module C component header information storage base address register	9-78
0x10B8 CH_WCH_C_STRID AND	WCH Module C Component Line Offset Register	9-78
0x10BC CH_WCH_C_BUF_ CFG	CH_WCH bus BUF control register	9-79
0x10E8 CH_Y_OUT_SIZE channel luminance output image size indication register 9-79		
0x10EC CH_C_OUT_SIZE channel chroma output image size indication register 9-79		
0x10F0 CH_INT	Channel Raw Interrupt Register	9-80
0x10F8 CH_INT_MASK channel interrupt mask register		9-81
0x1100 CH_Y_CROP_CFG channel brightness CROP enable register		9-82
0x1110 CH_Y_CROP0_STA RT	Channel Brightness 0 Area CROP Start Position Register 9-82	
0x1114 CH_Y_CROP0_SIZE channel brightness 0 area CROP size register 9-83		

offset address name		describe	page number
0x1120 CH_C_CROP_CFG Channel chroma CROP enable register			9-83
0x1130	CH_C_CROP0_STA RT	Channel Chroma 0 Area CROP Start Position Register 9-84	
0x1134	CH_C_CROP0_SIZE channel chroma 0 area CROP size register 9-84		

9.1.6 VICAP register description

WK_MODE

WK_MODE is the global working configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_DB58

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 0 1 1 0 1 0 1 1 0 0 0

Bits	Access Name		Description
[31:17] RO		reserved	reserve.
[16:14] RW ros_mem_ema		Read-only MEM Q-side speed regulation configuration.	
[13:11] RW rft_mem_emab		Dual-port MEM D-side speed regulation configuration.	
[10:8] RW rft_mem_emaa		Dual-port MEM Q-side speed regulation configuration.	
[7:6] RW rfs_mem_emaw		Single-port MEM D-side speed regulation configuration.	
[5:3] RW rfs_mem_ema		Single-port MEM Q-side speed regulation configuration.	
[2]	RO	reserved	reserve.
[1] RW mem_power_mode			MEM idle power-down mode. 0: MEM idle power-down mode off; 1: MEM idle power-down mode on.

[0] RW	power_mode		clock mode. 0: Low power consumption off; 1: Low power on.

AXI_CFG

AXI_CFG is the bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	r_outstanding	---	w_outstanding	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:12]	RW	r_outstanding	The outstanding number of read requests. The value range of outstanding is [1, 16].
[11:9]	RO	reserved	reserve.
[8:4]	RW	w_outstanding	Outstanding number of write requests. The value range of outstanding is [1, 8].
[3:0]	RO	reserved	reserve.

MAC_CFG

MAC_CFG is the MAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2	1 0
Name	reserved	r_req_prio	w_req_prio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	r_req_prio	w_req_prio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:8]	RW	r_req_prio	Read request arbitration priority. 0: low priority; 1: High priority. bit[8]: SRC0 read request priority; bit[9]: SRC1 read request priority; bit[10]: SRC2 read request priority; bit[11]: SRC3 read request priority; bit[12]: reserved ; bit[13]: reserved; bit[14]: reserved; bit[15]: reserved.
[7:0]	RW	w_req_prio	Write request arbitration priority. 0: low priority; 1: high priority. bit[0]: DES0 write request priority; bit[1]: DES1 write request priority; bit[2]: DES2 write request priority; bit[3]: WCH_Y write request priority; bit[4]: WCH_C Write request priority; bit[5]: reserved; bit[6]: reserved; bit[7]: reserved.

CH_SEL

CH_SEL is the channel input data selection register.

Offset Address	Register Name	Total Reset Value
0x0030	CH_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	ch_sel	Channel input data selection. 000: channel is connected to ISP_BE; 001: channel is connected to PT; (used by DEBUG) 010: channel is connected to LINE_BUF; (used by DEBUG) 011: channel is connected to ISP_FE; (used by DEBUG) Others: reserved.

DES_SEL

DES_SEL is the DES input data selection register.

Offset Address	Register Name	Total Reset Value
0x0040	DES_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														des2_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

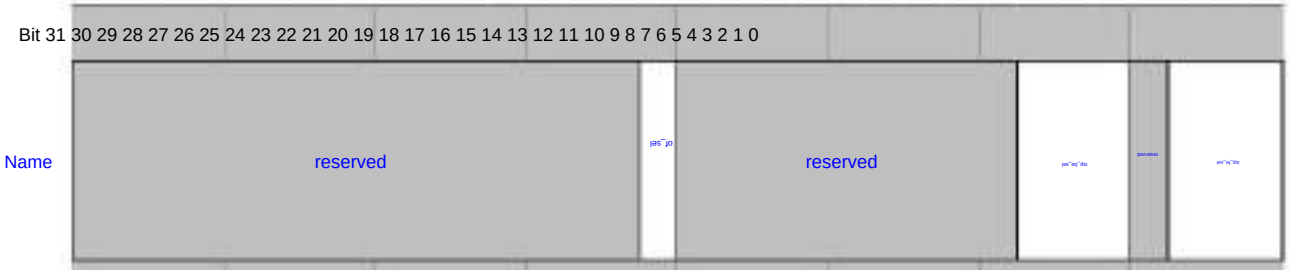
Bits	Access Name		Description
[31:11]	RO	reserved	reserve.
[10:8]	RW	des2_sel	DES2 Input data selection. 000: DES is connected to the port; 001: DES is connected to LINE_BUF; 010: DES is connected to FPN; 011: DES is connected to FSP_FE output. Other: reserved.
[7]	RO	reserved	reserve.

[6:4] RW des1_sel			DES1 Input data selection. 000: DES is connected to the port; 001: DES is connected with LINE_BUF; 010: DES and FPN connection; 011: DES is connected to FSP_FE output. Other: reserved.
[3]	RO	reserved	reserve.
[2:0] RW des0_sel			DES0 Input data selection. 000: DES is connected to port; 001: DES is connected to LINE_BUF; 010: DES is connected to FPN; 011: DES is connected to FSP_FE output. Other: reserved.

ISP_SEL

ISP_SEL is the ISP input data selection register.

Offset Address	Register Name	Total Reset Value
0x0050	ISP_SEL	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	of_sel	AF Input data selection. 0: AF is connected to ISP_FE; 1: AF is connected to ISP_BE; Others: Reserved.
[15:7]	RO	reserved	reserve.

[6:4] RW	isp_be_sel		ISP_BE Input data selection. 000: ISP_BE is connected with ISP_FE (for RAW input); 001: ISP_BE is connected with LINE_BUF (for YUV input); 011: ISP_BE is connected with SRC0 (for DEBUG); 100: ISP_BE is connected with SRC1 (for DEBUG); 101: ISP_BE is connected with SRC2 connection (use by DEBUG); 110: ISP_BE and SRC3 connection (use by DEBUG); Others: reserved.
[3]	RO	reserved	reserve.
[2:0] RW	isp_fe_sel		ISP_FE Input data selection. 000: ISP_FE is connected to LINE_BUF (in RAW input); 001: ISP_FE is connected to SRC0; 010: ISP_FE is connected to SRC1; 011: ISP_FE is connected to SRC2; 100: ISP_FE is connected to SRC3; Others: reserved.

CHN_MODE

CHN_MODE is the bus read and write rate control mode register.

Offset Address	Register Name	Total Reset Value
0x0060	CHN_MODE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved			
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

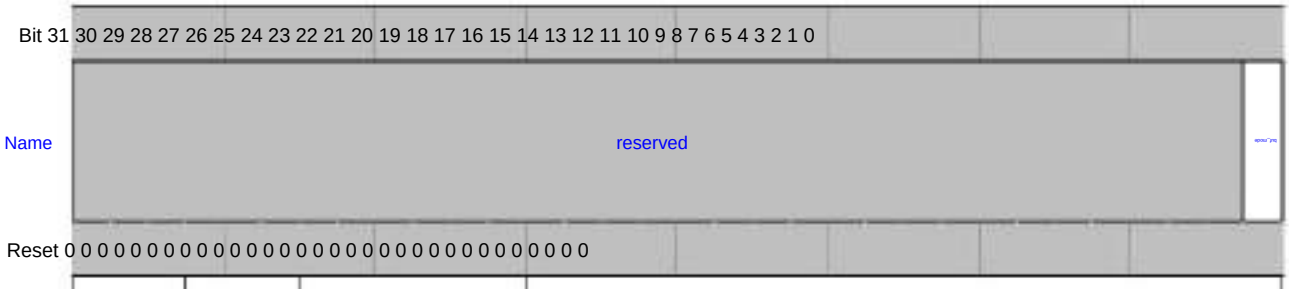
Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.

[5:4] RW	chn2_mode		SRC2/DES2 bus read and write rate control mode register (used when sharing buf). 00: no control; 01: Control the rate of SRC2 so that it cannot catch up with the write rate of DES2 (write first and then read). 10: Control the rate of DES2 so that it cannot catch up with the read rate of SRC2 (read first and then write). 11: Reserved.
[3:2] RW	chn1_mode		SRC1/DES1 bus read and write rate control mode register (used when sharing buf). 00: No control; 01: Control the rate of SRC1 so that it cannot catch up with the write rate of DES1 (write first and then read). 10: Control the rate of DES1 so that it cannot catch up with the read rate of SRC1 (read first and then write). 11: Reserved.
[1:0] RW	chn0_mode		SRC0/DES0 bus read and write rate control mode register (used when sharing buf). 00: No control; 01: Control the rate of SRC0 so that it cannot catch up with the write rate of DES0 (write first and then read). 10: Control the rate of DES0 so that it cannot catch up with the read rate of SRC0 (read first and then write). 11: Reserved.

BUF_MODE

BUF_MODE is the LINE_BUF input data selection register.

Offset Address	Register Name	Total Reset Value
0x0070	BUF_MODE	0x0000_0000



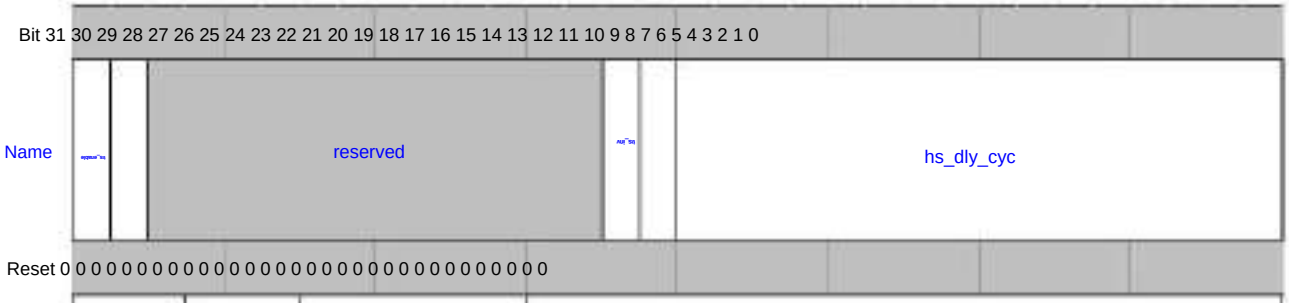
Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.

[0] RW	buf_mode		line_buf input data mode. 0: RAW data; 1ÿYUV422ÿ

SLAVE_MODE_CFG

SLAVE_MODE_CFG is SENSOR slave mode configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	SLAVE_MODE_CFG	0x0000_0000



Bits	Access	Name	Description
[31]	RW	vs_enable	VS output enable. 0: off; 1: enable.
[30]	RW	hs_enable	HS output enable. 0: off; 1: enable.
[29:18]	RO	reserved	reserve.
[17]	RW	vs_inv	VS Output polarity. 0: high effective; 1: Active low.
[16]	RW	hs_inv	HS output polarity. 0: high effective; 1: Active low.
[15:0]	RW	hs_dly_cyc	HS output relative to VS delay cycle configuration (unit: CYC).

SLAVE_MODE_VS_TIME

SLAVE_MODE_VS_TIME is the period configuration register for SENSOR slave mode output VSYNC.

Offset Address	Register Name	Total Reset Value
0x00B0	SLAVE_MODE_VS_TIME	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vs_time																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vs_time	VS output cycle configuration (unit: CYC).

SLAVE_MODE_HS_TIME

SLAVE_MODE_HS_TIME is the cycle configuration register for SENSOR slave mode output HSYNC.

Offset Address	Register Name	Total Reset Value
0x00B4	SLAVE_MODE_HS_TIME	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hs_time																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hs_time	HS output cycle configuration (unit: CYC).

SLAVE_MODE_VS_CYC

SLAVE_MODE_VS_CYC is the configuration register for the valid signal duration of the output VSYNC pulse of SENSOR slave mode.

Offset Address	Register Name	Total Reset Value
0x00B8	SLAVE_MODE_VS_CYC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vs_cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vs_cyc	VS output valid signal duration configuration (unit: CYC).

SLAVE_MODE_HS_CYC

SLAVE_MODE_HS_CYC is the configuration register for the valid signal duration of SENSOR slave mode output HSYNC pulse.

Offset Address	Register Name	Total Reset Value
0x00BC	SLAVE_MODE_HS_CYC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hs_cyc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	hs_cyc	HS output valid signal duration configuration (unit: CYC).

APB_TIMEOUT

APB_TIMEOUT is the APB timeout register.

Offset Address	Register Name	Total Reset Value
0x00E0	APB_TIMEOUT	0x8000_0180

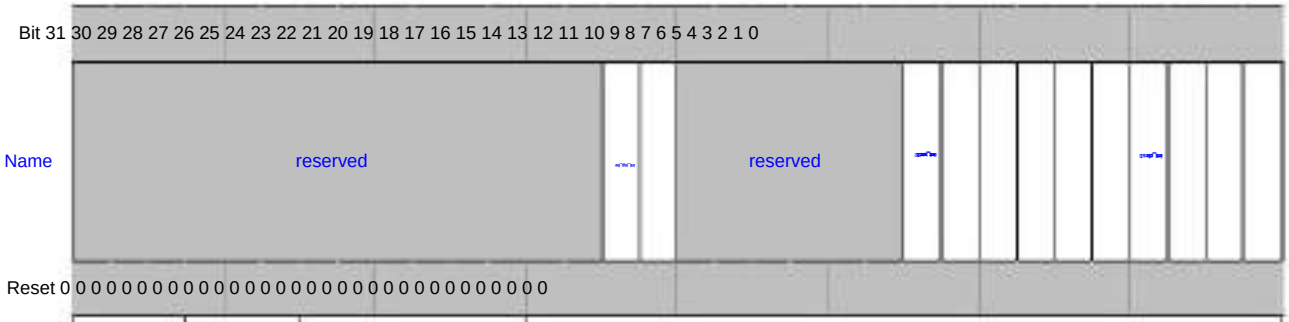
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	enable / reserved / timeout
Reset	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	enable	Timeout enabled. 0: off; 1: enable.
[30:16]	RO	reserved	reserve.
[15:0]	RW	timeout	Timeout threshold, the unit is APB bus clock.

VICAP_INT

VICAP_INT is the interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000



Bits	Access Name		Description
[31:18] RO		reserved	reserve.
[17] RO		int_isp_be	ISP_BE interrupt indication. 0: no interrupt; 1: There is an interrupt.
[16] RO		int_isp_fe	ISP_FE interrupt indication. 0: no interrupt; 1: There is an interrupt.
[15:10] RO		reserved	reserve.
[9]	RO	int_buf	LINE_BUF interrupt indication. 0: no interrupt; 1: There is an interrupt.
[8]	RO	int_src3	SRC3 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[7]	RO	int_src2	SRC2 interrupt indication. 0: no interrupt; 1: interrupt.
[6]	RO	int_src1	SRC1 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[5]	RO	int_src0	SRC0 interrupt indicator. 0: no interrupt; 1: There is an interrupt.

[4]	RO	int_des2	DES2 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[3]	RO	int_des1	DES1 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[2]	RO	int_des0	DES0 interrupt indication. 0: no interrupt; 1: There is an interrupt.
[1]	RO	int_ch	Channel interruption indication. 0: no interrupt; 1: There is an interrupt.
[0]	RO	int_pt	Port interrupt indication. 0: no interrupt; 1: There is an interrupt.

VICAP_INT_MASK

VICAP_INT_MASK is the interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:18]	RO	reserved	reserve.
[17]	RW	int_isp_be	ISP_BE interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

[16] RW int_isp_fe			ISP_FE Interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[15:10] RO		reserved	reserve.
[9] RW int_buf			LINE_BUF interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[8] RW int_src3			SRC3 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[7] RW int_src2			SRC2 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[6] RW int_src1			SRC1 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[5] RW int_src0			SRC0 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[4] RW int_des2			DES2 interrupt enable. 0: mask interrupt; 1: enable interrupt.
[3] RW int_des1			DES1 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[2] RW int_des0			DES0 interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[1] RW int_ch			Channel interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[0] RW int_pt			Port interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

PT_INTF_MOD

PT_INTF_MOD is the interface mode register.

Offset Address	Register Name	Total Reset Value
0x0100	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved	[illegible]
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	enable	The port is enabled. 0: off; 1: enable.
[30:1]	RO	reserved	reserve.
[0]	RW	mode	Timing mode configuration. 0: external synchronization; 1ÿBT.656ÿ

PT_OFFSET0

PT_OFFSET0 is a 0-component offset register.

Offset Address	Register Name	Total Reset Value
0x0110	PT_OFFSET0	0xFFF0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved												offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RW	mask	0 component mask.
[15]	RW	rev	Whether the data line is flipped. 0: no inversion; 1: Reverse.
[14:6]	RO	reserved	reserve.

[5:0] RW	offset		0 component offset.

PT_OFFSET1

PT_OFFSET1 is a 1-component offset register.

Offset Address	Register Name	Total Reset Value
0x0114	PT_OFFSET1	0xFFF0_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved												offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	1 component mask.
[15]	RW	rev	Whether the data line is flipped. 0: no inversion; 1: Reverse.
[14:6]	RO	reserved	reserve.
[5:0]	RW	offset	1 component offset.

PT_OFFSET2

PT_OFFSET2 is a 2-component offset register.

Offset Address	Register Name	Total Reset Value
0x0118	PT_OFFSET2	0xFFF0_0020

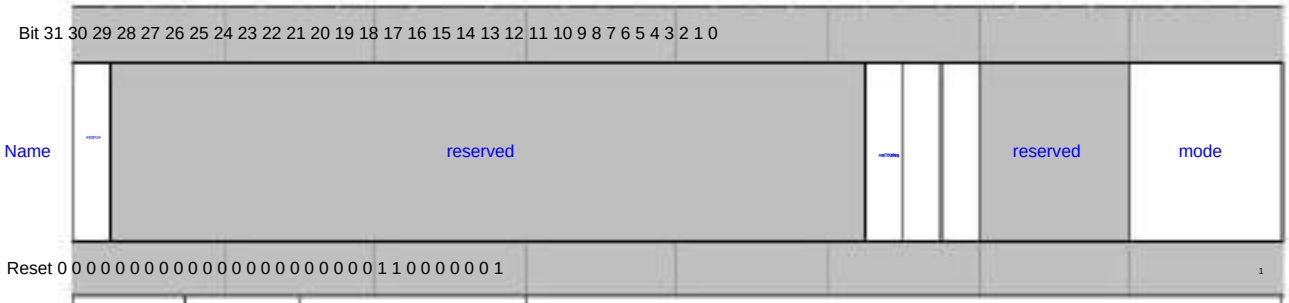
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved												offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	2 component masks.
[15]	RW	rev	Whether the data line is flipped. 0: no inversion; 1: Reverse.
[14:6]	RO	reserved	reserve.
[5:0]	RW	offset	2-component offset.

PT_BT656_CFG

PT_BT656_CFG is the BT656 configuration register.

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303



Bits	Access Name	Description
[31] RW	enable	BT.656 enable register. 0: off; 1: enable.
[30:11] RO	reserved	reserve.
[10] RW	field_inv	field reverse control. 0: no reverse; 1: Reverse.
[9] RW	vsync_inv	vsync reverse control. 0: no reverse; 1: Reverse.
[8] RW	hsync_inv	hsync reverse control. 0: no reverse; 1: Reverse.
[7:4] RO	reserved	reserve.

[3:0] RW	mode		mode select register. mode[0] 0: hsync is not a valid signal; 1: hsync is a valid signal. mode[1] 0: hsync output is active low; 1: hsync output is active high. mode[3:2] 00: analyze 0 component; 01: analyze 1 component; 10: Analyze 2 components; 11: Reserved.

PT_UNIFY_TIMING_CFG

PT_UNIFY_TIMING_CFG is the timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	RW	field_inv	Whether field is reversed (field level 1 processing). 0: no inversion; 1: Inverted.
[25:24]	RW	field_sel	Field source selection (field level 0 processing). 00: input field; 01: input vsync; 10: check according to the relationship between vsync and hsync; 11: always 0.
[23:21]	RO	reserved	reserve.

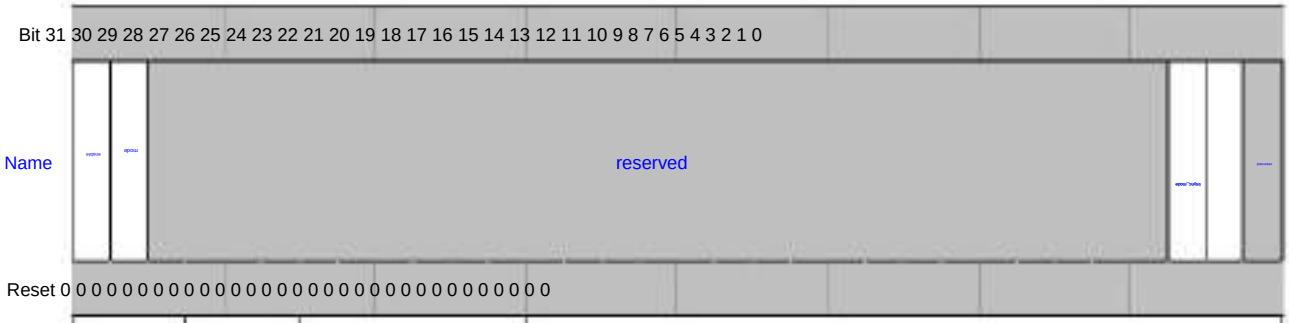
[20:19] RW	vsync_mode		vsync processing mode (vsync level 2 processing). 00: do not process; 01: Take the rising edge; 10: Take rising edge and falling edge; 11: Reserved.
[18] RW	vsync_inv		Whether vsync is inverted (vsync level 1 processing). 0: no inversion; 1: Inverted.
[17:16] RW	vsync_sel		vsync source selection (vsync level 0 processing) 00: input vsync; 01: input field; 10: always 0; 11: Reserved.
[15] RO		reserved	reserve.
[14:13] RW	hsync_mode		hsync processing mode (hsync level 3 processing). 0: do not process; 1: Take the rising edge.
[12:11] RW	hsync_and		Whether hsync operates with the result of vsync level 1 processing (hsync level 2 processing). 00: do not process; 01: Giving; 10: XOR; 11: Reserved.
[10] RW	hsync_inv		Whether hsync is inverted (hsync level 1 processing). 0: no inversion; 1: Inverted.
[9:8] RW	hsync_sel		hsync source selection (hsync level 0 processing). 00: input hsync; 01: input de; 10: always 0; 11: reserved.
[7:3] RO		reserved	reserve.
[2] RW	de_inv		Whether de is inverted (de 1st stage processing). 0: no inversion; 1: Inverted.

[1:0] RW de_sel			de source selection (de level 0 processing). 00: input de; 01: the result of hsync level 2 processing; 10: always 1; 11: always 0.

PT_GEN_TIMING_CFG

PT_GEN_TIMING_CFG is the timing recovery module configuration register.

Offset Address	Register Name	Total Reset Value
0x0134	PT_GEN_TIMING_CFG	0x0000_0000

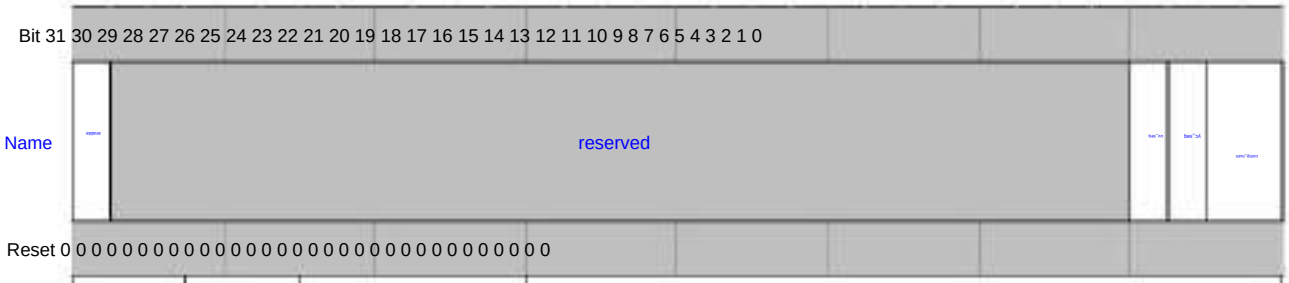


Bits	Access Name		Description
[31] RW enable			Timing recovery is enabled, and the timing is restored according to the timing parameters. 0: off; 1: enable.
[30] RW mode			Timing recovery mode, recover timing according to timing parameters. 0: Rely on the Valid signal input by PT to generate timing; 1: The timing is automatically calculated internally.
[29:3] RO		reserved	reserve.
[2] RW vsync_mode			Whether to restore vsync. 0: no recovery; 1: restore.
[1] RW hsync_mode			Whether to restore hsync. 0: no recovery; 1: restore.
[0]	RO	reserved	reserve.

PT_UNIFY_DATA_CFG

PT_UNIFY_DATA_CFG is the data configuration register.

Offset Address	Register Name	Total Reset Value
0x0140	PT_UNIFY_DATA_CFG	0x0000_0000



Bits	Access	Name	Description
[31]	RW	enable	Data separation is enabled. 0: off; 1: enable.
[30:4]	RO	reserved	reserve.
[3]	RW	uv_seq	CbCr order. 0ÿCbCrÿ 1ÿCrCbÿ
[2]	RW	yc_seq	YC order. 0ÿCYÿ 1ÿYCÿ
[1:0]	RW	comp_num	Data component selection. 00: 1 component; 01: 2 components; 10: 3 servings; 11: reserved.

PT_GEN_DATA_CFG

PT_GEN_DATA_CFG is the data generation module configuration register.

Offset Address	Register Name	Total Reset Value
0x0144	PT_GEN_DATA_CFG	0x0000_00E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1

Bits	Access	Name	Description
[31]	RW	enable	Data generation is enabled, and data is generated according to the data generation parameters. 0: off; 1: enable.
[30:8]	RO	reserved	reserve.
[7]	RW	data0_move	Whether data0 is incremented. 0: no increment; 1: increment.
[6]	RW	data1_move	Whether data1 is incremented. 0: no increment; 1: increment.
[5]	RW	data2_move	Whether data2 is incremented. 0: no increment; 1: increment.
[4]	RW	vsync_reset	Whether the data is reset according to the vsync signal. 0: no reset; 1: Reset.
[3]	RW	hsync_reset	Whether the data is reset according to the hsync signal. 0: no reset; 1: Reset.
[2]	RW	vsync_move	Whether data is incremented according to vsync. 0: no increment; 1: increment.
[1]	RW	hsync_move	Whether data is incremented according to hsync. 0: no increment; 1: increment.

[0]	RW	de_move	Whether data is incremented according to de. 0: no increment; 1: increment.

PT_GEN_DATA_COEF

PT_GEN_DATA_COEF is the data generation module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0148	PT_GEN_DATA_COEF	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inc_frame								step_frame								inc_space								step_space							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	inc_frame	The value is incremented between data frames, and the incremental value is accumulated in the upper 8 bits of the data.
[23:16]	RW	step_frame	Increment interval between data frames. The configuration value is the actual value minus 1, and the configuration is 0, which means incrementing every frame.
[15:8]	RW	inc_space	The value is incremented between data pixels, and the incremental value is accumulated in the upper 10 bits of the data.
[7:0]	RW	step_space	The increasing interval between data pixels, 0 means increasing per pixel.

PT_GEN_DATA_INIT

PT_GEN_DATA_INIT configures the register for the initial value of the data generation module.

Offset Address	Register Name	Total Reset Value
0x014C	PT_GEN_DATA_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								data2								data1								date0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	data2	Initial value of V/B.
[15:8]	RW	data1	Initial value of U/G.
[7:0]	RW	data0	Initial value of Y/R.

PT_YUV444_CFG

PT_YUV444_CFG is YUV444 configuration register.

Offset Address	Register Name	Total Reset Value
0x0150	PT_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable, adjust YUV422 signal to YUV444 signal. 0: off; 1: enable.
[30:0]	RO	reserved	reserve.

PT_FSTART_DLY

PT_FSTART_DLY is the port fstart interrupt delay register.

Offset Address	Register Name	Total Reset Value
0x0160	PT_FSTART_DLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fstart_dly																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fstart_dly	fstart Interrupt delay time, in port clock.

PT_INTF_HFB

PT_INTF_HFB is the horizontal leading blanking width register.

Offset Address	Register Name	Total Reset Value
0x0180	PT_INTF_HFB	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hfb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hfb	Horizontal leading blanking width.

PT_INTF_HACT

PT_INTF_HACT is the horizontal active area width register.

Offset Address	Register Name	Total Reset Value
0x0184	PT_INTF_HACT	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hact
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	hact	Horizontal effective area width (unit: clock cycle).

PT_INTF_HBB

PT_INTF_HBB is the horizontal post-blanking width register.

Offset Address	Register Name	Total Reset Value
0x0188	PT_INTF_HBB	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hbb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hbb	Horizontal back blanking width.

PT_INTF_VFB

PT_INTF_VFB is the vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x018C	PT_INTF_VFB	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vfb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vfb	Vertical leading blanking width.

PT_INTF_VACT

PT_INTF_VACT is the vertical active area width register.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vact
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vact	Vertical active area width.

PT_INTF_VBB

PT_INTF_VBB is the vertical back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0194	PT_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vbb	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	etc	Vertical back blanking width.

PT_INTF_VBFB

PT_INTF_VBFB is the width register of blanking area before vertical bottom field.

Offset Address	Register Name	Total Reset Value
0x0198	PT_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vbfb	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vbfb	The width of the blanking zone before the vertical bottom field.

PT_INTF_VBACT

PT_INTF_VBACT is the vertical bottom field active area width register.

Offset Address	Register Name	Total Reset Value
0x019C	PT_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vbact	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vbact	The width of the effective area of the vertical bottom field.

PT_INTF_VBBB

PT_INTF_VBBB is the width register of blanking area after vertical bottom field.

Offset Address	Register Name	Total Reset Value
0x01A0	PT_INTF_VBBB	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	etc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vbbb	The width of the blanking zone after the vertical bottom field.

PT_ID_CFG

PT_ID_CFG is the ID configuration register.

Offset Address	Register Name	Total Reset Value
0x01A4	PT_ID_CFG	0x0000_0000

Bit	31	30	29	28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Name	enable	mode	reset	reserved	id_it id_max id
Reset	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0

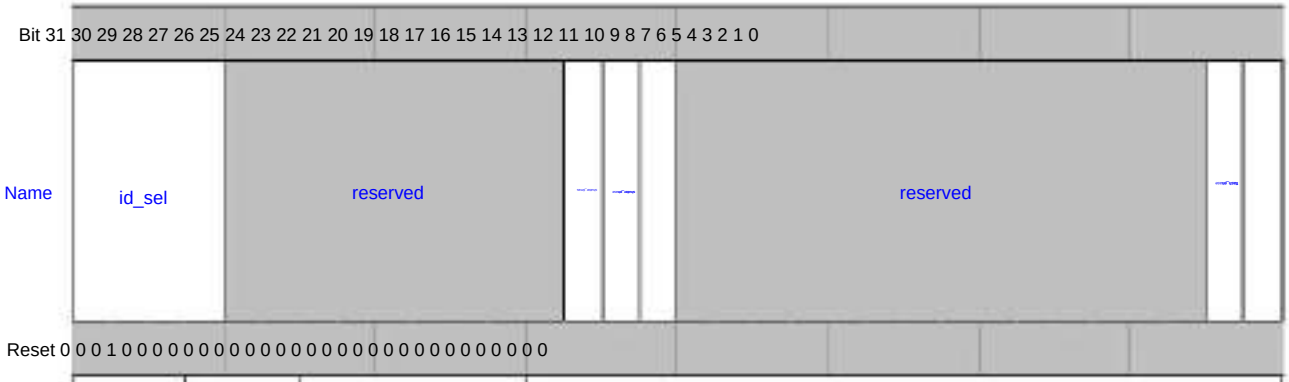
Bits	Access	Name	Description
[31]	RW	enable	Generate ID function enable. 0: disable; 1: enable.
[30]	RW	mode	Generate ID mode selection. 0: Auto mode, ID is automatically increased every frame; 1: Non-automatic mode, the ID is determined by the configuration value.
[29]	WO	reset	In automatic mode, setting the configuration register to 1 can restore the ID of the next frame to the initial value, and it will be automatically cleared to 0 after recovery.
[28:6]	RO	reserved	reserve.
[5:4]	RW	id_it	Width and height detection corresponds to the ID number of the frame.

[3:2] RW	id_max		The maximum value to add to the ID in automatic mode.
[1:0] RW	id		It is the initial ID value in automatic mode, and the generated ID value in non-automatic mode.

PT_FLASH_CFG

PT_FLASH_CFG is the flash configuration register.

Offset Address	Register Name	Total Reset Value
0x01B0	PT_FLASH_CFG	0x1000_0000



Bits	Access	Name	Description
[31:28]	RW	id_sel	Toggles the frame ID select register. 0x1: triggered by the frame start interrupt with ID 0; 0x2: triggered by the frame start interrupt with ID 1; 0x4: triggered by the frame start interrupt with ID 2; 0x8: triggered by the frame start interrupt with ID 3 trigger; Other: reserved.
[27:19]	RO	reserved	reserve.
[18]	RW	shutter_times	The number of shutter pulses. 0: 2 times; 1:1 times.
[17]	RW	shutter_phase	Whether the shutter signal is reversed. 0: no reverse; 1: Reverse.
[16]	WO	shutter_en	Trigger shutter control, auto-zero. 0: off; 1: enable.
[15:2]	RO	reserved	reserve.

[1] RW	flash_phase		Whether the flash signal is reversed. 0: no reverse; 1: Reverse.
[0] WO	flash_on		Trigger flash control, auto clear. 0: off; 1: enable.

PT_FLASH_CYC0

PT_FLASH_CYC0 is the flash timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01C0	PT_FLASH_CYC0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cyc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	cyc	The time of sequence 0 of the flashlight, in the unit of PT clock, the configuration value is minus 1 from the actual value.

PT_FLASH_CYC1

PT_FLASH_CYC1 is the flash timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01C4	PT_FLASH_CYC1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cyc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	cyc	The time of flash timing sequence 1, in the unit of PT clock, the configuration value is minus 1 from the actual value.

PT_SHUTTER_CYC0

PT_SHUTTER_CYC0 is the shutter timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01D0	PT_SHUTTER_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	The time of shutter sequence 0, in the unit of PT clock, the configuration value is the actual value minus 1.

PT_SHUTTER_CYC1

PT_SHUTTER_CYC1 is the shutter timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01D4	PT_SHUTTER_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	The time of shutter sequence 1, in the unit of PT clock, the configuration value is the actual value minus 1.

PT_SHUTTER_CYC2

PT_SHUTTER_CYC2 is the shutter timing 2 width register.

Offset Address	Register Name	Total Reset Value
0x01D8	PT_SHUTTER_CYC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	The time of shutter sequence 2 is in unit of PT clock, and the configuration value is the actual value minus 1.

PT_SHUTTER_CYC3

PT_SHUTTER_CYC3 is the shutter timing 3 width register.

Offset Address	Register Name	Total Reset Value
0x01DC	PT_SHUTTER_CYC3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cyc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	cyc	The time of shutter sequence 3, in the unit of PT clock, the configuration value is the actual value minus 1ÿ

PT_STATUS

PT_STATUS is the port status register.

Offset Address	Register Name	Total Reset Value
0x01E0	PT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved id field negative hsync of
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:6]	RO	reserved	reserve.
[5:4]	RO	id	The id of the port output.
[3]	RO	field	The field output by the port.
[2]	RO	vsync	vsync for port output.
[1]	RO	hsync	hsync for port output.
[0]	RO	of	port output de.

PT_BT656_STATUS

PT_BT656_STATUS is the BT656 status register.

Offset Address	Register Name	Total Reset Value
0x01E4	PT_BT656_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	seav	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:8]	RO	seav	synchronization code.
[7:0]	RO	reserved	reserve.

PT_SIZE

PT_SIZE is the input size indication register.

Offset Address	Register Name	Total Reset Value
0x01EC	PT_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	height	image height.
[15:0]	RO	width	Image width.

PT_INT

PT_INT is the port interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x01F0	PT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	WC	height_err	Image height change interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[1]	WC	width_err	Image width change interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[0]	WC	fstart	Frame/field start interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

PT_INT_MASK

PT_INT_MASK is the port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	PT_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.

[2] RW height_err			Image height change interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[1] RW width_err			Image width change interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[0] RW fstart			Frame/field start interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.

OFF_CTRL

DES_CTRL is the DES control register.

Offset Address	Register Name	Total Reset Value
0x0200	OFF_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	reserved																												bit_width		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	DES enable register. 0: disable; 1: enable. 0x0200~0x02FF: DES0 register address space. 0x0300~0x03FF: DES1 register address space. 0x0400 ÿ0x04FF: DES2 register address space (only available in vicap0).
[30:6]	RO	reserved	reserve.
[5:0]	RW	bit_width	Data bit width. 0x08ÿ8bitÿ 0x0Aÿ10bitÿ 0x0Cÿ12bitÿ 0x0Eÿ14bitÿ 0x10ÿ16bitÿ Other: reserved.

DES_REG_NEWER

DES_REG_NEWER is the acquisition control register.

Offset Address	Register Name	Total Reset Value
0x0204	DES_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	reg_newer	DES update register, cleared to 0 automatically every frame. 0: no update (drop frame); 1: update.

DES_ID_CFG

DES_ID_CFG is the DES receive ID selection register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0210	DES_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														id_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	id_sel	ID selection register. 0: filter the data of this ID; 1: Receive the data of this ID. bit[0]: enable DES to receive data whose ID is 0; bit[1]: enable DES to receive data whose ID is 1; bit[2]: enable DES to receive data whose ID is 2; bit[3]: DES Receive data enable with ID 3.

DES_CROP_CFG

DES_CROP_CFG is the CROP enable register.

Offset Address	Register Name	Total Reset Value
0x0220	DES_CROP_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

DES_CROP0_START

DES_CROP0_START is the CROP start position register for area 0.

Offset Address	Register Name	Total Reset Value
0x0230	DES_CROP0_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start	reserved	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

DES_CROP0_SIZE

DES_CROP0_SIZE is 0 area CROP size setting register.

Offset Address	Register Name	Total Reset Value
0x0234	DES_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

DES_CFG

DES_CFG is the DES configuration register.

Offset Address	Register Name	Total Reset Value
0x0270	DES_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	k_coef_range	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	cmp_en	DES channel frame compression enable register. 0: disable; 1: enable. 0x300~0x3FF: DES1 register address space. 0x400~0x4FF: DES2 register address space.
[30:27]	RW	k_coef_range	DES channel frame compression rate control register. The value range is [7,12], and the typical configuration is that the data bit width is reduced by one. (12 for 14bit width)
[26:0]	RO	reserved	reserve.

DES_SIZE

DES_SIZE is the DES storage size register.

Offset Address	Register Name	Total Reset Value
0x0284	DES_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							height									—								width							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Store the height of the image (in row units), the configuration value is the actual value minus 1.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Stores the width of the image in pixels, the configured value is the actual value minus 1.

DES_FADDR

DES_FADDR Stores the base address register for DES.

Offset Address	Register Name	Total Reset Value
0x0290	DES_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	DES stores the base address.

DES_STRIDE

DES_STRIDE Stores the line spacing register for DES.

Offset Address	Register Name	Total Reset Value
0x0294	DES_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	stride	DES channel frame line spacing.

DES_BUF_CFG

DES_BUF_CFG is the DES bus BUF control register.

Offset Address	Register Name	Total Reset Value
0x029C	DES_BUF_CFG	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	buf_thd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	buf_thd	Depth of bus buf.

DES_INT

DES_INT is DES raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x02F0	DES_INT	0x0000_0000

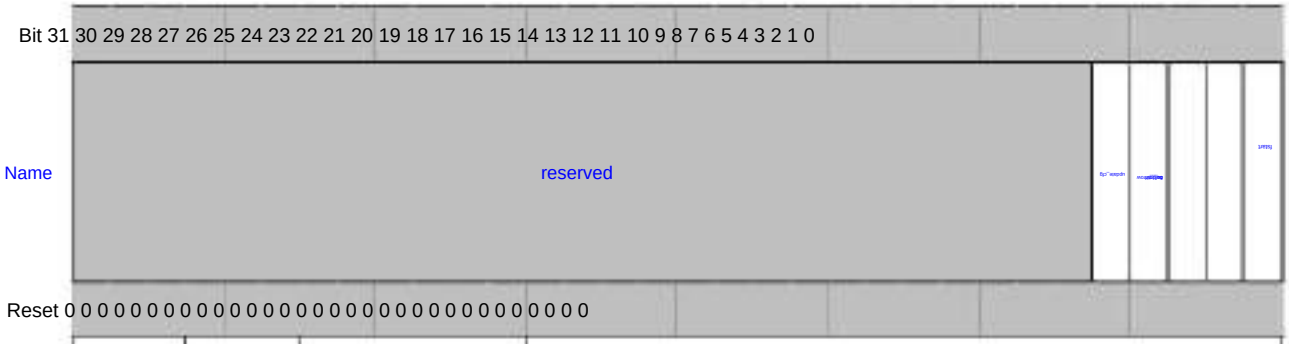
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	WC	update_cfg	Register update interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[3]	WC	field_throw	Field/frame loss interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[2]	WC	buf_ovf	Internal FIFO overflow error interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[1]	WC	cc_int	After obtaining the interrupt status, write 1 to clear it. 0: no interrupt; 1: interrupt.
[0]	WC	fstart	Field/frame start interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

DES_MASK

DES_MASK is the DES interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x02F8	DES_MASK	0x0000_0000



Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	update_cfg	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[3]	RW	field_throw	Field/frame loss interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[1]	RW	cc_int	Get complete interrupt enable. 0: mask interrupt; 1: enable interrupt.
[0]	RW	fstart	Start of field/frame interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

LINE_BUF_CFG

LINE_BUF_CFG is the LINE_BUF control register.

Offset Address	Register Name	Total Reset Value
0x0500	LINE_BUF_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31] RW	enable		LINE_BUF enable register. 0: forbidden; 1: enable.
[30:1] RO		reserved	reserve.
[0] RW	vsync_mode		Drop frame mode control signal. 0: When a frame is lost, data is lost and vsync is lost at the same time. 1: When a frame is lost, only data is lost but not vsync.

LINE_BUF_REG_NEWER

LINE_BUF_REG_NEWER Update register for LINE_BUF.

Offset Address	Register Name	Total Reset Value
0x0504	LINE_BUF_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1] RO		reserved	reserve.
[0] WO	reg_newer		The LINE_BUF update register is automatically cleared to 0 every frame. 0: no update (drop frame); 1: update.

LINE_BUF_ID_CFG

LINE_BUF_ID_CFG is the LINE_BUF receive ID selection register. Instant register.

Offset Address	Register Name	Total Reset Value
0x0510	LINE_BUF_ID_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	id_sel
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	id_sel	ID selection register. 0: filter the data of this ID; 1: Receive the data of this ID. bit[0]: Enable LINE_BUF to receive data with ID 0; bit[1]: Enable LINE_BUF to receive data with ID 1; bit[2]: Enable LINE_BUF to receive data with ID 2; bit[3]: LINE_BUF Receive data enable with ID 3.

LINE_BUF_CROP_CFG

LINE_BUF_CROP_CFG is the CROP enable register, immediate register.

Offset Address	Register Name	Total Reset Value
0x0520	LINE_BUF_CROP_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	n0_en
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

LINE_BUF_CROP0_START

LINE_BUF_CROP0_START is the CROP start position register of area 0, an immediate register.

Offset Address	Register Name	Total Reset Value
0x0530	LINE_BUF_CROP0_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	y_start	—	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

LINE_BUF_CROP0_SIZE

LINE_BUF_CROP0_SIZE is 0 area CROP size setting register, real-time register.

Offset Address	Register Name	Total Reset Value
0x0534	LINE_BUF_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

LINE_BUF_WIDTH

LINE_BUF_WIDTH is the LINE_BUF image width register.

Offset Address	Register Name	Total Reset Value
0x0550	LINE_BUF_WIDTH	0x077F_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							line_buf_thd									—								line_buf_width							
Reset	0	0	0	0	0	1	1	1	0	1				1	1	1				1	0	0	0	0	0	1	1	0	1	1	1	

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	line_buf_thd	LINE_BUF RAM read operation initiation threshold.
[15:13]	RO	reserved	reserve.
[12:0]	RW	line_buf_width	LINE_BUF image width.

LINE_BUF_HEIGHT

LINE_BUF_HEIGHT is the LINE_BUF image height register.

Offset Address	Register Name	Total Reset Value
0x0554	LINE_BUF_HEIGHT	0x0000_0437

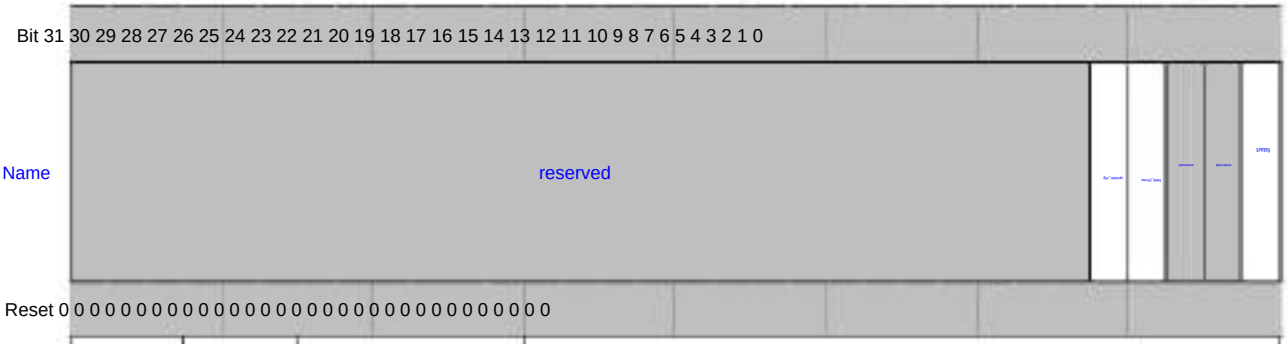
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													line_buf_height		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	line_buf_height	LINE_BUF image height.

LINE_BUF_INT

LINE_BUF_INT is the LINE_BUF raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x05F0	LINE_BUF_INT	0x0000_0000



Bits	Access Name		Description
[31:5] RO		reserved	reserve.
[4] WC update_cfg			Register update interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[3] WC field_throw			Field/frame loss interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[2]	RO	reserved	reserve.
[1]	RO	reserved	reserve.
[0] WC fstart			Field/frame start interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

LINE_BUF_MASK

LINE_BUF_MASK is the LINE_BUF interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x05F8	LINE_BUF_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	update_cfg	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[3]	RW	field_throw	Field/frame loss interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RO	reserved	reserve.
[1]	RO	reserved	reserve.
[0]	RW	fstart	Start of field/frame interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

SRC_CTRL

SRC_CTRL is the SRC control register.

Offset Address	Register Name	Total Reset Value
0x0600	SRC_CTRL	0x0000_0000

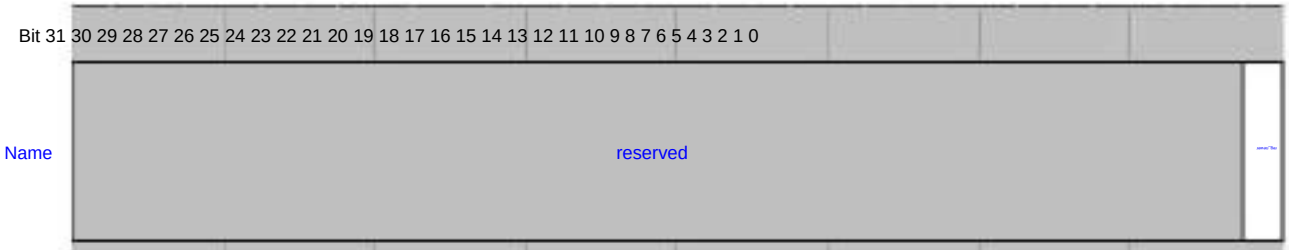
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	reserved																													bit_width	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31] RW enable		SRC enable register. 0: disable; 1: enable. 0x600~0x6FF: SRC0 register address space. 0x700~0x7FF: SRC1 register address space. 0x800~0x8FF: SRC2 register address space. 0x900~0x9FF: SRC3 register address space.
[30:6] RO	reserved	reserve.
[5:0] RW bit_width		SRC read data bit width. 0x08ÿ8bitÿ 0x0Aÿ10bitÿ 0x0Cÿ12bitÿ 0x0Eÿ14bitÿ 0x10ÿ16bitÿ Other: reserved.

SRC_REG_NEWER

SRC_REG_NEWER is the acquisition control register.

Offset Address	Register Name	Total Reset Value
0x0604	SRC_REG_NEWER	0x0000_0000

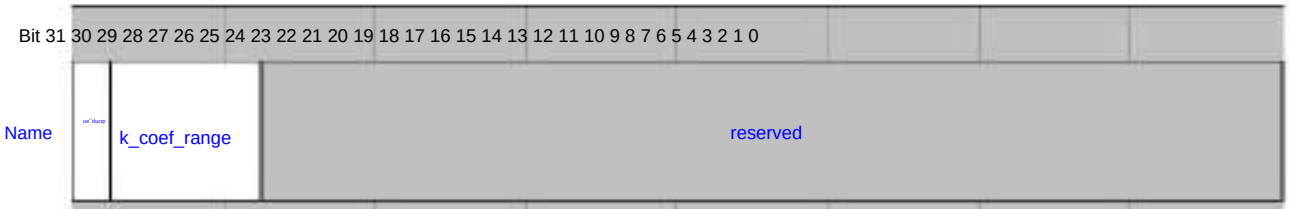


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	reg_newer	SRC update register, cleared to 0 automatically every frame. 0: no update (drop frame); 1: update.

SRC_CFG

SRC_CFG is the configuration register.

Offset Address	Register Name	Total Reset Value
0x0670	SRC_CFG	0x0000_0000



Bits	Access	Name	Description
[31]	RW	dcmp_en	SRC Read Channel Frame Decompression Enable Register. 0: disable; 1: enable.
[30:27]	RW	k_coef_range	SRC channel frame compression rate control register. The value range is [7,12]. It needs to be consistent with the configuration during compression. The typical configuration is the bit width minus one (configure 12 when the bit width is 14bit).
[26:0]	RO	reserved	reserve.

SRC_SIZE

SRC_SIZE is the SRC storage size register.

Offset Address	Register Name	Total Reset Value
0x0684	SRC_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Store the height of the image (in row units), the configuration value is the actual value minus 1.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Stores the width of the image in pixels, the configured value is the actual value minus 1.

SRC_FADDR

SRC_FADDR is the base address register for SRC storage.

Offset Address	Register Name	Total Reset Value
0x0690	SRC_FADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	faddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	faddr	SRC stores the base address.

SRC_STRIDE

SRC_STRIDE Stores the line spacing register for the SRC.

Offset Address	Register Name	Total Reset Value
0x0694	SRC_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	stride	SRC channel frame line spacing.

SRC_BUF_CFG

SRC_BUF_CFG is the SRC bus BUF control register.

Offset Address	Register Name	Total Reset Value
0x069C	SRC_BUF_CFG	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	buf_thd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	buf_thd	Depth of bus buf.

SRC_INT

SRC_INT is the SRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x06F0	SRC_INT	0x0000_0000

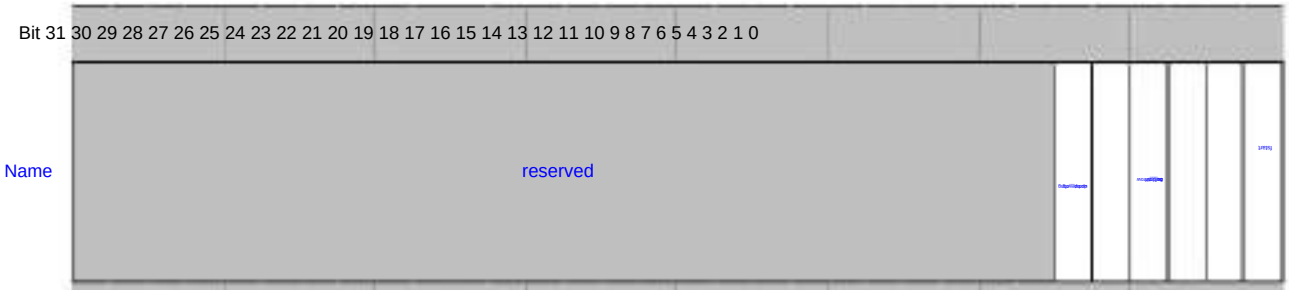
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	WC	dcmp_wrong	Decompression error interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[4]	WC	update_cfg	Register update interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[3]	WC	field_throw	Field/frame loss interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[2]	WC	buf_ovf	Internal FIFO overflow error interrupt status, write 1 to clear. 0: no interrupt; 1: interrupt.
[1]	WC	cc_int	After obtaining the interrupt status, write 1 to clear it. 0: no interrupt; 1: There is an interrupt.
[0]	WC	fstart	Field/frame start interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

SRC_MASK

SRC_MASK is the SRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x06F8	SRC_MASK	0x0000_0000



Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	dcmp_wrong	Decompression error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[4]	RW	update_cfg	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[3]	RW	field_throw	Field/frame loss interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable. 0: mask interrupt; 1: enable interrupt.
[1]	RW	cc_int	Get complete interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[0]	RW	fstart	Start of field/frame interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

CH_CTRL

CH_CTRL is the channel control register.

Offset Address	Register Name	Total Reset Value
0x1000	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved	[illegible]
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable register. 0: disable; 1: enable.
[30:2]	RO	reserved	reserve.
[1:0]	RW	mode	Channel mode register. 00: normal mode; 01: single component (luminance) mode; 10: single component (chroma) mode; others: reserved.

CH_REG_NEWER

CH_REG_NEWER is the acquisition control register.

Offset Address	Register Name	Total Reset Value
0x1004	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	[illegible]
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	reg_newer	Channel update register, cleared to 0 automatically every frame.

CH_DLY_CFG

CH_DLY_CFG is the channel input image start interrupt delay configuration register.

Offset Address	Register Name	Total Reset Value
0x1034	CH_DLY_CFG	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_dly_cfg																								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	v_dly_cfg	Number of vertical lines delay register.
[15:0]	RO	reserved	reserve.

CH_WCH_Y_CFG

CH_WCH_Y_CFG is the WCH module Y component configuration register.

Offset Address	Register Name	Total Reset Value
0x1080	CH_WCH_Y_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																		reserved												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH Write channel enable register. 0: disable; 1: enable.
[30:20]	RO	reserved	reserve.
[19]	RW	interleave	progressively interlaced flag. 0: The output data is progressive, or the output data is interlaced, and there is no need for interleaved frame storage; 1: The output data is interlaced and needs to be interleaved into frames for storage.

[18] RW bfield			The top and bottom field flags are used when the output data is interlaced and needs to be interleaved into frames for storage. 0: top field; 1: Bottom field.
[17:16] RW bit_width			Data bit width. 00ÿ8bitÿ 10ÿ16bitÿ Other: reserved.
[15:5] RO		reserved	reserve.
[4] RW flip			The channel FLIP function is enabled. 0: Disable the flip function; 1: Enable the flip function.
[3] RW mirror			The channel MIRROR function is enabled. 0: Disable the mirror function; 1: Enable the mirror function.
[2] RW head_tword			header information stride option. 0: 128 bits (128bit/line); 1: 256 bits (256bit/line).
[1] RW cmp_mode			Compressed segment length. 0: 128 pixels; 1: 256 pixels.
[0] RW cmp_en			Compression enabled. 0: forbidden; 1: enable.

CH_WCH_Y_SIZE

CH_WCH_Y_SIZE Stores the size register for the WCH module Y component.

Offset Address	Register Name	Total Reset Value
0x1084	CH_WCH_Y_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	---	height	---	width
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Store the height of the image (in row units), the configuration value is the actual value minus 1.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Stores the width of the image in pixels, the configured value is the actual value minus 1.

CH_WCH_Y_FADDR

CH_WCH_Y_FADDR Stores the base address register for the Y component of the WCH module.

Offset Address	Register Name	Total Reset Value
0x1090	CH_WCH_Y_FADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	faddr	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	faddr	The Y component stores the base address.

CH_WCH_Y_HADDR

CH_WCH_Y_HADDR is the base address register for WCH module Y component header information storage.

Offset Address	Register Name	Total Reset Value
0x1094	CH_WCH_Y_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Y component header information storage base address.

CH_WCH_Y_STRIDE

CH_WCH_Y_STRIDE is the WCH module Y component row offset register.

Offset Address	Register Name	Total Reset Value
0x1098	CH_WCH_Y_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												stride			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	stride	The image stores the stride of the Y component, in bytes.

CH_WCH_Y_BUF_CFG

CH_WCH_Y_BUF_CFG is the CH_DES bus BUF control register.

Offset Address	Register Name	Total Reset Value
0x109C	CH_WCH_Y_BUF_CFG	0x0000_0080

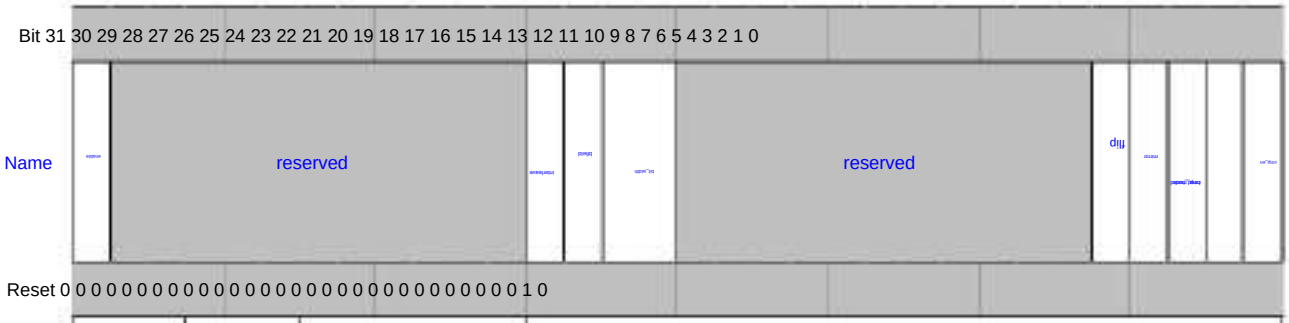
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												buf_thd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	buf_thd	Depth of bus buf.

CH_WCH_C_CFG

CH_WCH_C_CFG is the WCH module C component configuration register.

Offset Address	Register Name	Total Reset Value
0x10A0	CH_WCH_C_CFG	0x0000_0002



Bits	Access	Name	Description
[31]	RW	enable	CH Write channel enable register. 0: disable; 1: enable.
[30:20]	RO	reserved	reserve.
[19]	RW	interleave	progressively interlaced flag. 0: The output data is progressive, or the output data is interlaced, and there is no need for interleaved frame storage; 1: The output data is interlaced and needs to be interleaved into frames for storage.
[18]	RW	bfield	The top and bottom field flags are used when the output data is interlaced and needs to be interleaved into frames for storage. 0: top field; 1: Bottom field.
[17:16]	RW	bit_width	Data bit width. 00ÿ8bitÿ 10: 16bit; Others: Reserved.
[15:5]	RO	reserved	reserve.
[4]	RW	flip	The channel FLIP function is enabled. 0: Turn off the flip function; 1: Turn on the flip function.
[3]	RW	mirror	The channel MIRROR function is enabled. 0: turn off the mirror function; 1: Turn on the mirror function.

[2] RW	head_tword		header information stride option. 0: 128 bits (128bit/line); 1: 256 bits (256bit/line).
[1] RW	cmp_mode		Compressed segment length. 0: 128 pixels; 1: 256 pixels.
[0] RW	cmp_en		Compression enabled. 0: disable; 1: enable.

CH_WCH_C_SIZE

CH_WCH_C_SIZE is the WCH module C component storage size register.

Offset Address	Register Name	Total Reset Value
0x10A4	CH_WCH_C_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height — width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Store the height of the image (in row units), the configuration value is the actual value minus 1.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Stores the width of the image in pixels, the configured value is the actual value minus 1.

CH_WCH_C_FADDR

CH_WCH_C_FADDR Stores the base address register for the C component of the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B0	CH_WCH_C_FADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	faddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	faddr	The C component stores the base address.

CH_WCH_C_HADDR

CH_WCH_C_HADDR Base address register for WCH module C component header information storage.

Offset Address	Register Name	Total Reset Value
0x10B4	CH_WCH_C_HADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	haddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	haddr	C component header information storage base address.

CH_WCH_C_STRIDE

CH_WCH_C_STRIDE is the C component line offset register of WCH module.

Offset Address	Register Name	Total Reset Value
0x10B8	CH_WCH_C_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	stride	The image stores the stride of the C component, in byte.

CH_WCH_C_BUF_CFG

CH_WCH_C_BUF_CFG is the CH_WCH bus BUF control register.

Offset Address	Register Name	Total Reset Value
0x10BC	CH_WCH_C_BUF_CFG	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	buf_thd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	buf_thd	Depth of bus buf.

CH_Y_OUT_SIZE

CH_Y_OUT_SIZE is the channel brightness image output size indication register.

Offset Address	Register Name	Total Reset Value
0x10E8	CH_Y_OUT_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	height	image height.
[15:0]	RO	width	Image width.

CH_C_OUT_SIZE

CH_C_OUT_SIZE is the channel chroma image output size indication register.

Offset Address	Register Name	Total Reset Value
0x10EC	CH_C_OUT_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	height	image height.
[15:0]	RO	width	Image width.

CH_INT

CH_INT is the channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10F0	CH_INT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

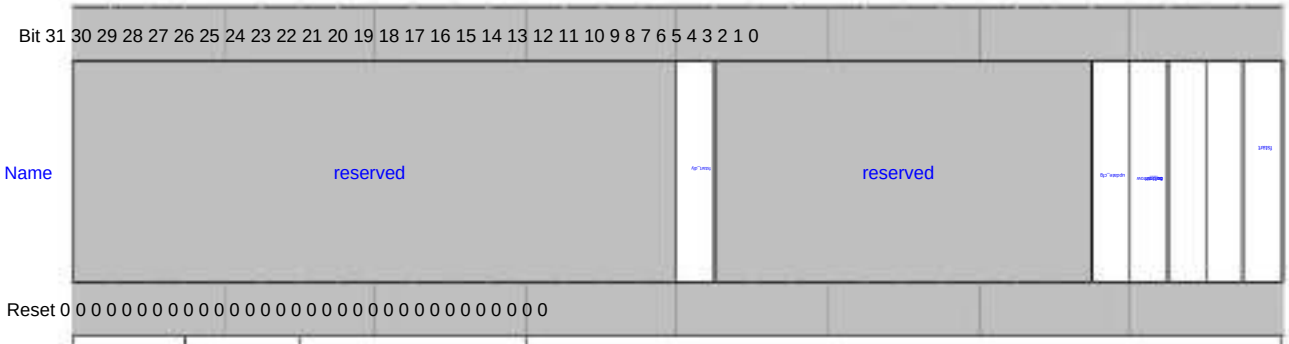
Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	WC	fstart_dly	Field/frame start interrupt status after delay, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[14:5]	RO	reserved	reserve.
[4]	WC	update_cfg	Register update interrupt status, write 1 to clear. 0: no interrupt; 1: interrupt.
[3]	WC	field_throw	Field/frame loss interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

[2] WC buf_ovf			Internal FIFO overflow error interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[1] WC cc_int			After obtaining the interrupt status, write 1 to clear it. 0: no interrupt; 1: There is an interrupt.
[0] WC fstart			Field/frame start interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

CH_INT_MASK

CH_INT_MASK is the channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10F8	CH_INT_MASK	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	fstart_dly	Start of field/frame interrupt enable after delay. 0: no interrupt; 1: There is an interrupt.
[14:5]	RO	reserved	reserve.
[4]	RW	update_cfg	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[3]	RW	field_throw	Field/frame loss interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

[2] RW buf_ovf			Internal FIFO overflow error interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[1] RW cc_int			Get complete interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[0] RW fstart			Start of field/frame interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

CH_Y_CROP_CFG

CH_Y_CROP_CFG is the channel brightness CROP enable register.

Offset Address	Register Name	Total Reset Value
0x1100	CH_Y_CROP_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

CH_Y_CROP0_START

CH_Y_CROP0_START is the CROP start position register of channel brightness 0 area.

Offset Address	Register Name	Total Reset Value
0x1110	CH_Y_CROP0_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	y_start	—	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

CH_Y_CROP0_SIZE

CH_Y_CROP0_SIZE is the CROP size setting register for channel brightness 0 area.

Offset Address	Register Name	Total Reset Value
0x1114	CH_Y_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

CH_C_CROP_CFG

CH_C_CROP_CFG is the channel chroma CROP enable register.

Offset Address	Register Name	Total Reset Value
0x1120	CH_C_CROP_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

CH_C_CROP0_START

CH_C_CROP0_START is the CROP start position register of channel chroma 0 area.

Offset Address	Register Name	Total Reset Value
0x1130	CH_C_CROP0_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	y_start	reserved	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

CH_C_CROP0_SIZE

CH_C_CROP0_SIZE is the CROP size setting register for channel chroma 0 area.

Offset Address	Register Name	Total Reset Value
0x1134	CH_C_CROP0_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

9.2 VDP

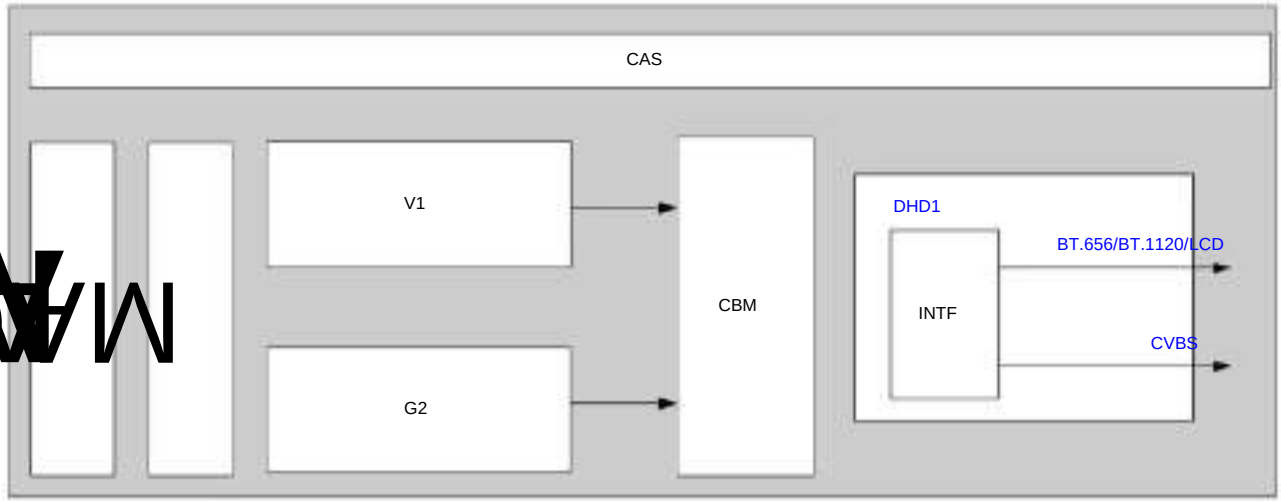
9.2.1 Overview

The VDP (Video Display Processor) module actively reads video and graphics data from the corresponding location in the memory, superimposes the video layer and graphics layer data and sends them out through the display channel.

9.2.2 Architecture Description

The overall block diagram of VDP is shown in Figure 9-17 .

Figure 9-17 Overall block diagram of VDP



Surface: Data path for bus input. Its functions include bus data reading and data processing of a single layer. Surface includes: video layer V1, graphics layer G2.

Display Channel: display channel. Including high-definition display channel DHD1.

CBM (CrossBar and Mixer, strobe overlay): Video layer/graphics layer overlay.

MAC (Memory Access Controller, memory access controller): The bus application arbitration module of each Surface. Each module reads data from the memory through the AXI (Advanced eXtensible Interface) bus, and the module arbitrates the application made by each Surface.

CAS (Control And Status): This module mainly configures the registers through the APB (Advanced Peripheral Bus, Advanced Peripheral Bus) bus, and the status information of each module is reported to the CPU through this module.

VDP registers are mainly allocated according to module global, Surface and Display Channel:

module global registers

Includes bus-related configuration, interrupts, and version registers.

Surface registers include

video layer and graphics layer configuration registers.

Display Channel registers include

DHD1 configuration registers.

The characteristics of VDP are as follows:

Digital output interface: support ITU-R BT.656 output, support LCD16bit parallel/6bit serial/8bit serial output, support ITU-R BT.1120 output.

Video Layer (Video Surface)

Graphics Surface Overlay feature VDP

contains 1

video channel, which has independent vertical timing interrupt, marks the end of the frame/field, and 1 low-bandwidth interrupt.

Analog output interface: support CVBS output.

9.2.3 Working method

9.2.3.1 Clock configuration

There is one configurable clock source for VDP:

Interface output clock source: U_VPLL

For specific registers, refer to the description of PERI_CRG17 and PERI_CRG18 in Section 3.2.7 of Chapter 3 CRG registers.

9.2.3.2 Reset

VDP reset includes 1 hardware reset and 1 software reset.

注意

Before doing an AXI bus reset:

Turn all layers off.

After the next frame/field is interrupted (reaching the update point), configure the bus reset request.

9.2.3.3 Bus related configuration

AXI Master

VDP includes a Master interface to improve bus access efficiency:

VDP supports AXI Master, and the data read and write requests of V1 and G2 layers can be operated on the bus through MASTER.

VDP supports multiple IDs, but cannot be dynamically switched.

APB register configuration

The VDP registers are read and written through the APB interface. In HI3519V100, the base address of VDP is 0x1100_0000, the register addressing space is 64KB, and the corresponding address offset range is: 0x0000ý0xFFFF.

Outstanding configuration

The Outstanding depth of AXI Master can be configured as 0, 1, 2, 3, 4, 5, 6, 7. Among them, when outstanding is 0, AXI Master does not perform any operations on the bus.

9.2.3.4 Digital output interface

VDP supports the following three digital interface outputs: ITU-R BT.656, ITU-R BT.1120, LCD RGB mode

9.2.3.5 Interrupts

VDP interrupts fall into 3 categories:

- Vertical Timing Interrupt Low
- Bandwidth Interrupt
- DAC No Load Interruption

vertical timing interrupt

VDP supports vertical timing interrupts, and the location of interrupt generation can be flexibly configured:

- The VDP contains a vertical timing interrupt, which marks the end of a frame/field.
- Interrupt generation methods are optional: frame interrupt, field interrupt.
- For progressive display, the vertical timing interrupt can only be configured as frame interrupt mode.
- For interlaced display, the vertical timing interrupt can be configured as frame interrupt mode or field interrupt mode (it is recommended that HD generate interrupts according to fields, and SD generate interrupts according to frames).
- Support interrupt mask can be configured.
- Supports configurable vertical timing interrupt threshold. Each interrupt source can be turned on and off independently, write 1 to clear 0.

low bandwidth interrupt

VDP supports the reporting of low bandwidth status in interrupt mode:

- VDP contains a low-bandwidth interrupt, flagging frame/field low-bandwidth information.
- Support interrupt mask can be configured.
- Each interrupt source can be turned on and off independently, write 1 to clear 0.

9.2.4 Functional description

9.2.4.1 Video layer functions

Video Layer Features

Supports non-compressed and lossless compressed data

sources Supported input pixel formats: semi-plannar420, semi-plannar422, semi-plannar400 minimum input resolution 32x32,

maximum input resolution 1920x1080 minimum output resolution 32x32, maximum output

resolution 1920x1080

The horizontal resolution of the input is a multiple of 2

Interlaced 420 Input vertical resolution is a multiple of 4, otherwise it is a multiple of 2 Supports progressive

mode, interlaced mode source start address

can be allocated (sub-luminance, chrominance address), non-compressed data source, address is 2byte alignment; compression Data source, the address is 16byte alignment source stride can be

allocated (sub-brightness, chroma address), 16byte alignment supports vertical chroma

upsampling, copy mode. Support horizontal chroma

upsampling IFIR, copy mode, bilinear interpolation, 16-order half-band filter mode optional.

Support color space conversion, support contrast/hue/saturation adjustment

Support display position configurable: display at any position on the screen

Support global alpha configurable, configuration range 0~255

DCMP: decompress

To reduce bandwidth, the source read by VDP may be compressed data. V1 decompresses the compressed data and restores it to the original YcbCr pixels.

CROP: horizontal cropping

Support for horizontal cropping of the input width.

420-422: vertical chroma upsampling

When the input image data is 420, it is necessary to enlarge the chromaticity by 2 times in the vertical direction and convert the data format to 422. V1 converts the data format to the copy method.

422-444: horizontal chroma upsampling

The main function of the horizontal chroma upsampling is to upsample the chroma in the horizontal direction and convert the 422 data format to 444.

There are 3 ways to achieve chroma level upsampling, which can be configured:

copy

bilinear interpolation

16th-order half-band filtering

CSC: Color Space Conversion

Realize the conversion of YCbCr BT.601, BT.709 and RGB color space, and support adjustment of brightness, hue and saturation.

9.2.4.2 Graphics Layer Functions

Graphics layer features:

Supported input pixel formats: ARGB1555, ARGB4444, ARGB8888 Minimum input resolution 32x32, maximum input resolution 1920x1080 Minimum output resolution 32x32, maximum output resolution 1920x1080

Input horizontal and vertical resolutions are multiples of 2

Support progressive mode, interlaced mode

Support frame update, field update

source start address can be configured, address is 128bit (16byte) alignment source

stride can be configured, is 128bit (16byte) alignment support color space conversion

Support display position configurable: display anywhere on the screen

Support global alpha configurable, configuration range 0~255 pixel alpha

enable configurable, for graphics with pixel alpha value in pixel format ARGB1555, select ALPHA0 or ALPHA1

Support colorkey processing Support premultiplication processing

CSC Functional Description

Support color space conversion, including: mutual conversion between RGB2YCbCr601 and RGB2YCbCr709.

alpha processing

Alpha values for graphics layers can come from two sources:

Pixel Alpha value: Indicates the overlay property of a certain pixel. Global Alpha value: Indicates the overlay property of a certain layer.

There is a special case of the pixel Alpha value. In the ARGB1555 format, the Alpha value has only 1 bit. This bit is not the real Alpha value, but only the index of alpha. The real Alpha value is obtained by selecting the value in the Alpha register according to the index value. When the index value is 0, the value is ALPHA0, otherwise, the value is ALPHA1.

Colorkey function

The key mode is optional, and the pixels outside or within the configuration range are used for key processing.

The bit of Key can be masked.

premultiplied function

Support input data as premultiplied data. When the input is premultiplied data, the Colorkey function must be turned off.

9.2.4.3 Overlay processing

VDP supports the superposition function of V1 and G2 layers.

Overlay feature

Support bottom-to-top overlay mode Overlay

background color

configurable Overlay surface priority configurable

9.2.4.4 Display channels

Video channel characteristics

DHD1 can be used as an output channel of HD and SD. In the

same scene, only one timing can be output. HD and SD timing cannot be output at the same time. The

following typical output timings are supported: 1080p, 1080i, 720p, PAL, NTSC

timing configuration

The output interface of VDP supports the configuration of various typical and atypical timings to adapt to different docking chip interfaces.

注意

When configuring all timing parameters, the interface should be closed, and the interface should be opened after the configuration is completed.

9.2.4.5 HD output interface BT.1120

BT.1120 Features

Support 10bit to 8bit dither Support

YCbCr444 to YCbCr422 horizontal chroma downsampling dfir Support data clamp clip,

according to the interface protocol, Y clamp range 16~235, C clamp range 16~240 Support the following typical output timing: 720p,

1080p and 1080i support bypass mode, and dither and dfir are processed by

truncation and point loss respectively. 16bit data, the default Y is in the high position, C is in the low position,

and the position of YC is interchangeable

9.2.4.6 SD output interface BT.656

BT.656 Features

Support 10bit to 8bit dither

Support YCbCr444 to YCbCr422 horizontal chroma downsampling dfir

Support data clamp clip, according to the interface protocol, Y clamp range 16~235, C clamp range 16~240 Support the following typical output timing: NTSC, PAL

9.2.4.7 SD output interface CVBS

CVBS Features

Support data clamping clip, Y clamping range 64~940, C clamping range 64~960 DATE supporting digital analog processing

DATE supports VDAC auto detection function

supports the following typical output timings: NTSC, PAL

9.2.4.8 LCD output interface RGB

Support 8bit/6bit serial RGB output bit order, reverse order adjustable.

Support 16bit parallel RGB output, default RGB order, BGR order output is optional. Support RGB serial output, output sequence R, G, B, low 8bit output in 16bit. The maximum output clock is 27MHz.

9.2.5 VDP register overview

An overview of the VDP registers is shown in Table 9-6 .

Table 9-6 VDP register overview (base address is 0x1100_0000)

offset address name	describe	page number
0x0000 VOCTRL	VO control register	9-97
0x0004 VOINTSTA	VO interrupt status, read-only register	9-98
0x0008 VOMSKINTSTA	VO passes through Mask's interrupt status register	9-99
0x000C VOINTMSK	VDP Interrupt Mask Register	9-100
0x0010 VDPVERSION1	VDP version 1 registers	9-101
0x0014 VDPVERSION2	VDP version 2 registers	9-101
0x0020 VOMEM_CTRL	VDP MEM Debug Control Register	9-101
0x0034 VOAXICTRL	VO AXI bus configuration register	9-102
0x0100 VO_MUX	VO output interface check register	9-103

offset address name	describe	page number
0x0108 VO_MUX_TESTSY NC	VO output interface test register	9-103
0x010C IN VO_MUX_TEST FACING	VO output interface test data register	9-104
0x0120 VO_DAC_CTRL	VO DAC Control Register	9-105
0x0134 VO_DAC_0_CTRL VO DAC 0 channel control register		9-106
0x0140 VO_DAC_STAT0 VO DAC status 0 register		9-106
0x1000 V1_CTRL	This register can configure the relevant information of the layer, which is a non-immediate register	9-107
0x1004 V1_UPD	v1 channel update enable register	9-109
0x1028 V1_IRESO	Input Resolution Register, for non-immediate registers 9-109	
0x102C V1_ORESO	Output Resolution Register, for non-immediate registers 9-110	
0x1034 V1_DCMP_SGMT_ CROP	The input segment decompresses the crop register, which is a non-immediate register	9-110
0x1038 V1_CBMPARA Overlay related parameters, non-immediate registers		9-110
0x1044 V1_CPOS	The horizontal clipping coordinate register of the source image	9-111
0x1060 V1_DFPOS	Surface at the starting position of the display window (First POSition), non-immediate registers	9-111
0x1064 V1_DLPOS	Surface at the end of the display window (Last POSition), in pixels, non-immediate registers	9-112
0x1080 V1_CSC_IDC	Color space conversion input DC component register, for immediate register	9-112
0x1084 V1_CSC_ODC Color space conversion output DC component register, which is an immediate register		9-113
0x1088 V1_CSC_IODC Color space conversion input/output DC component register	device, the immediate register	9-113
0x108C V1_CSC_P0	Color space conversion parameter 0, for immediate registers 9-114	
0x1090 V1_CSC_P1	Color space conversion parameter 1, for immediate registers 9-114	
0x1094 V1_CSC_P2	Color space conversion parameter 2, for immediate registers 9-115	
0x1098 V1_CSC_P3	Color space conversion parameter 3, for immediate registers 9-116	
0x109C V1_CSC_P4	Color space conversion parameter 4, for immediate registers 9-116	
0x1204 V1_P0LADDR Video layer brightness address register		9-116

offset address name		describe	page number
0x1208 V1_P0CADDR		video layer chroma address register	9-117
0x120C V1_P0STRIDE		video layer stride register	9-117
0x1640 V1_LADDROFFSET		Luminance compressed data address relative to header information address offset register, effective when decompression is enabled, it is a non-immediate register	9-118
0x1644 V1_CADDROFFSET		Chroma compression data address offset register relative to header information address, valid when decompression is enabled, non-immediate register	9-118
0x1720 V1_DCMP_LSTATE	0	Video layer luma channel decompression status register 0	9-118
0x1724 V1_DCMP_LSTATE	1	Video layer luma channel decompression status register 1	9-119
0x1728 V1_DCMP_CSTATE	0	Video layer chroma channel decompression status register 0	9-119
0x172C V1_DCMP_CSTATE	1	Video Layer Chroma Channel Decompression Status Register 1	9-119
0x1730 V1_DCMPERRCLR		Video layer decompression error status clear register 9-120	
0x1734 V1_DCMP_ERR		Video layer decompression error signal register	9-120
0x7000	G2_CTRL	This register can configure the relevant information register 9-121 of the layer	
0x7004 G2_UPD		Graphics layer update enable register	9-122
0x7010 G2_ADDR		graphics layer address register	9-123
0x701C G2_STRIDE		The stride register of the graphics layer	9-123
0x7020	G2_IRESO	Input Resolution Register, for non-immediate registers 9-124	
0x7024	G2_SFPOS	Surface needs to read the starting position of the data in the source bitmap, non-immediate registers	9-124
0x7030 G2_CBMPARA		Overlay related parameters, which are non-immediate registers	9-125
0x7034 G2_CKEYMAX		Color key maximum value, for non-immediate registers 9-126	
0x7038 G2_CKEYMIN		Color key minimum value for non-immediate registers 9-126	
0x703C G2_CMASK		Color key mask value, for non-immediate registers 9-127	
0x7080	G2_DFPOS	Surface at the starting position of the display window (First POSition), in pixels, non-immediate registers	9-127

offset address name		describe	page number
0x7084	G2_DLPOS	Surface at the end of the display window (Last POSition), in pixels, non-immediate registers	9-128
0x70C0 G2_CSC_IDC		Color space conversion input DC component register, for immediate register	9-128
0x70C4 G2_CSC_ODC Color space conversion output DC component register, which is an immediate register			9-129
0x70C8 G2_CSC_IODC Color space conversion input/output DC component register, which is an immediate register			9-130
0x70CC G2_CSC_P0		Color space conversion parameter 0, for immediate registers 9-130	
0x70D0	G2_CSC_P1	Color space conversion parameter 1, for immediate registers 9-131	
0x70D4 G2_CSC_P2		Color space conversion parameter 2, for immediate register 9-131	
0x70D8	G2_CSC_P3	Color space conversion parameter 3, for immediate register 9-132	
0x70DC G2_CSC_P4		Color space conversion parameter 4, for immediate registers 9-132	
0xB420 CBM_BKG2		CBM Mixer2 overlay background color register	9-133
0xB428 CBM_MIX2		CBM Mixer2 Priority Configuration Register	9-133
0xC400 DHD1_CTRL		Displays the overall control register for the channel	9-134
0xC404 DHD1_VSYNC When interlaced output, this register indicates the vertical synchronization timing of the top field; when outputting progressively, this register indicates the vertical synchronization timing of the frame			9-135
0xC408 DHD1_HSYNC1 In the case of interlaced or progressive output, the horizontal synchronization configuration register			9-135
0xC40C DHD1_HSYNC2 In the case of interlaced or progressive output, the horizontal synchronization configuration register is not an immediate register			9-136
0xC410 DHD1_VPLUS When interlaced output, this register indicates the bottom vertical step timing, non-immediate registers			9-136
0xC414 DHD1_PWR		Synchronization Signal Pulse Width, Non-immediate Register 9-137	
0xC418 DHD1_VTTHD3		Vertical Timing Threshold (Vertical Timing Threshold), for the immediate register	9-137
0xC41C DHD1_VTTHD		Vertical Timing Threshold (Vertical Timing Threshold), for the immediate register	9-138
0xC4B0 DHD1_PARATHD PARA coefficient update point threshold register			9-139
0xC4C0 DHD1_START_POS DHD channel start signal start position register 9-139			

offset address name	describe	page number
0xC4F0 DHD1_STATE	DHD1 Status Register	9-139
0xD200 BT_CTRL	BT.656/BT.1120 Control Register	9-140
0xD210 BT_CLIP0_L	BT.656/BT.1120 Clip handles the lowest threshold register, which is an immediate register	9-141
0xD214 BT_CLIP0_H	BT.656/BT.1120 Clip handles the highest threshold value register, which is an immediate register	9-142
0xD280 BT_DITHER0_CTRL	BT.656/BT.1120 Dither Control Register 9-142	
0xD284 BT_DITHER0_COEF0	BT.656/BT.1120 Dither Coefficient 0 Register 9-143	
0xD288 BT_DITHER0_COEF1	BT.656/BT.1120 Dither Coefficient 1 Register 9-144	
0xD400 LCD_CTRL	LCD Control Register	9-144
0xD408 LCD_SYNC_INV	Synchronization signal polarity configuration register when LCD external synchronization timing input	9-145
0xF200 DATE_COEFF0 standard parameter configuration register		9-146
0xF204 DATE_COEFF1 Amplitude Configuration Register		9-149
0xF208 DATE_COEFF2	DATE coefficient 2 register	9-151
0xF20C DATE_COEFF3	DATE coefficient 3 register	9-151
0xF210 DATE_COEFF4	DATE coefficient 4 register	9-151
0xF214 DATE_COEFF5	DATE coefficient 5 register	9-152
0xF218 DATE_COEFF6	DATE coefficient 6 register	9-152
0xF254 DATE_COEFF21 Output Matrix Control Register		9-153
0xF258 DATE_COEFF22	DTO Initial Phase Configuration Register	9-154
0xF25C DATE_COEFF23	VIDEO_OUT Delay Configuration Register	9-154
0xF260 DATE_COEFF24	ColorBurst Home Position Register	9-155
0xF280 DATE_ISRMASK interrupt mask register		9-155
0xF284 DATE_ISRSTATE Interrupt Status Register		9-156
0xF288 DATE_ISR	interrupt register	9-156
0xF294 DATE_COEFF37 Upsampling filter coefficient 1 register		9-157
0xF298 DATE_COEFF38 Upsampling filter coefficient 2 register		9-157

offset address name	describe	page number
0xF29C DATE_COEFF39	Upsampling filter coefficient 3 register	9-158
0xF2A0 DATE_COEFF40	Upsampling filter coefficient 4 register	9-158
0xF2A4 DATE_COEFF41	Upsampling filter coefficient 5 register	9-159
0xF2A8 DATE_COEFF42	Upsampling filter coefficient 6 register	9-159
0xF2C0 DATE_DACDET1	DAC auto detection 1 register	9-160
0xF2C4 DATE_DACDET2	DAC auto detection 2 register	9-160
0xF2C8 DATE_COEFF50	Oversampling filter coefficient 1 register	9-161
0xF2CC DATE_COEFF51	Oversampling filter coefficient 2 register	9-161
0xF2D0 DATE_COEFF52	Oversampling filter coefficient 3 register	9-162
0xF2D4 DATE_COEFF53	Oversampling filter coefficient 4 register	9-162
0xF2D8 DATE_COEFF54	Oversampling filter coefficient 5 register	9-162
0xF2DC DATE_COEFF55	Oversampling filter coefficient 6 register	9-163
0xF2E0 DATE_COEFF56	Oversampling rounding register	9-163
0xF2E4 DATE_COEFF57	CVBS Gain Control Register	9-164
0xF2E8 DATE_COEFF58	Component gain control register	9-165
0xF2EC DATE_COEFF59	clip control bit register	9-165

9.2.6 VDP register description

VOCTRL

VOCTRL is the VO control register. The surface bus applies for arbitration mode.

Offset Address	Register Name	Total Reset Value
0x0000	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																													m0_arb_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31] RW	vo_ck_gt_en		VDP clock gating enable. 0: Clock gating is off; 1: Internal clock gating of VDP is on.
[30:4] RO		reserved	reserve.
[3:0] RW	m0_arb_mode		VO MAC0 internal surface bus data application arbitration mode. 0x0: polling; 0x1: graphic layer priority; Other: reserved.

WELLNESS

VOINTSTA is VO interrupt status, read-only register.

Offset Address	Register Name	Total Reset Value
0x0004	WELLNESS	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

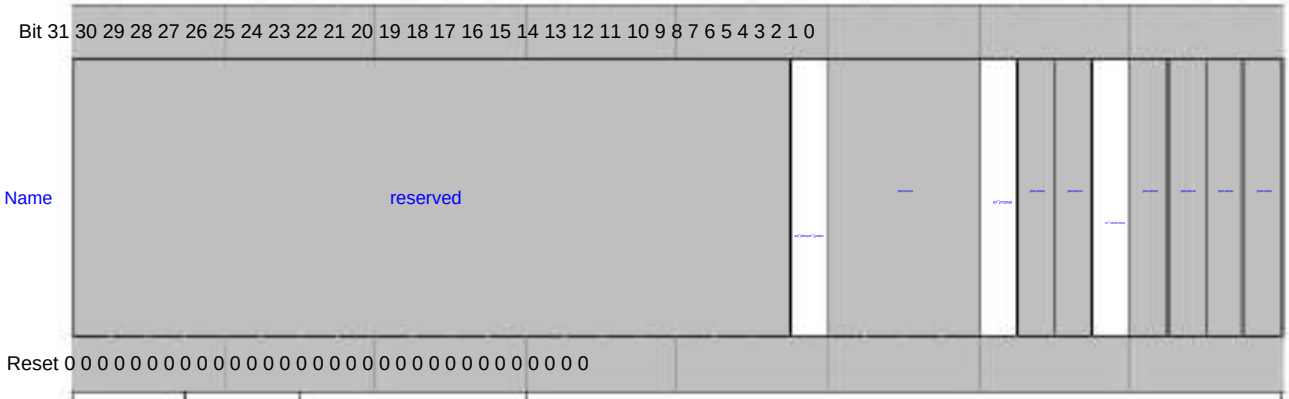
Bits	Access Name		Description
[31:8] RO		reserved	reserve.

[7]	RO	dhd1uf_int	DHD1 channel low bandwidth alarm interrupt. 0: no interrupt; 1: Report interruption.
[6]	RO	reserved	reserve.
[5]	RO	reserved	reserve.
[4]	RO	dhd1vtthd1_int	DHD1 channel vertical timing interrupt 1. 0: no interrupt; 1: Report interruption.
[3:0] RO		reserved	reserve.

VOMSKINTSTA

VOMSKINTSTA is the interrupt status register of VO passing Mask. Write 1 to clear.

Offset Address	Register Name	Total Reset Value
0x0008	VOMSKINTSTA	0x0000_0000



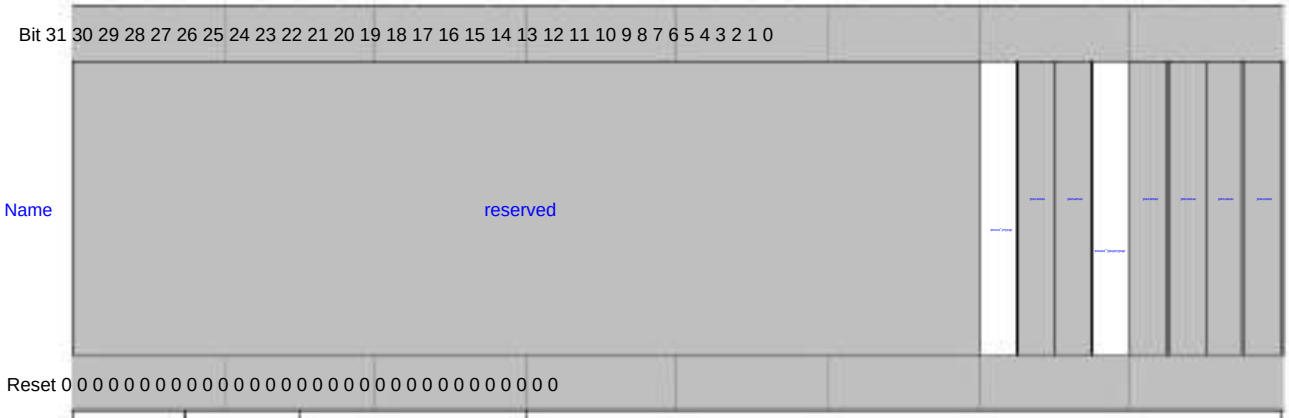
Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] WC	vdac0_unload_int		DAC0 has no load interrupt. 0: no interrupt; 1: Report interruption.
[11:8] RO		reserved	reserve.
[7] WC	dhd1uf_clr		DHD1 channel low bandwidth alarm interrupt. 0: no interrupt; 1: Report interruption.
[6]	RO	reserved	reserve.
[5]	RO	reserved	reserve.

[4] WC dhd1vt	hd1_clr		DHD1 channel vertical timing interrupt 1. 0: no interrupt; 1: Report interruption.
[3]	RO	reserved	reserve.
[2]	RO	reserved	reserve.
[1]	RO	reserved	reserve.
[0]	RO	reserved	reserve.

VOINTMSK

VOINTMSK is the VDP interrupt mask register. Corresponds to VOINTSTA. If the corresponding bit is 1, the interrupt is enabled, and if it is 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0x000C	VOINTMSK	0x0000_0000



Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	dhd1uf_intmsk	DHD1 channel low bandwidth alarm interrupt. 0: interrupt mask; 1: Interrupts are on.
[6]	RO	reserved	reserve.
[5]	RO	reserved	reserve.
[4]	RW	dhd1vt_intmsk	DHD1 channel vertical timing interrupt 1. 0: interrupt mask; 1: Interrupts are on.
[3]	RO	reserved	reserve.

[2]	RO	reserved	reserve.
[1]	RO	reserved	reserve.
[0]	RO	reserved	reserve.

VDPVERSION1

VDPVERSION1 is the VDP version 1 register.

Offset Address	Register Name	Total Reset Value
0x0010	VDPVERSION1	0x7675_6F76

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	vdpversion1			
Reset	0 1 1 1 0 1 1 0	0 1	1 0 1 0 1 0 1 1	0 1 1 0 1 1 1 0

Bits	Access Name		Description
[31:0]	RO	vdpversion1	VDP version register 1.

VDPVERSION2

VDPVERSION2 is the VDP version 2 register.

Offset Address	Register Name	Total Reset Value
0x0014	VDPVERSION2	0x3031_3134

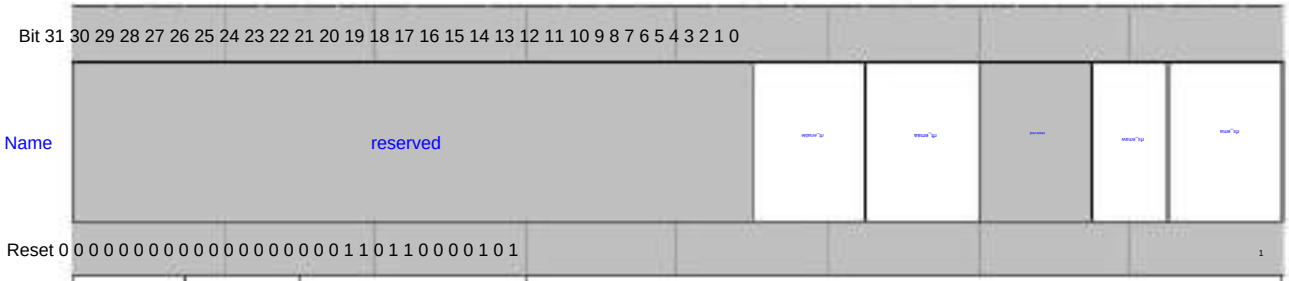
Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	vdpversion2			
Reset	0 0 1 1 0 0 0 0	0 0 1	1 0 0 0 1 0 0 1	1 0 0 0 1 0 0 1 1 0 1 0 0

Bits	Access Name		Description
[31:0]	RO	vdpversion2	VDP version register 2.

VOMEM_CTRL

VOMEM_CTRL is the VDP MEM debug control register.

Offset Address	Register Name	Total Reset Value
0x0024	VOMEM_CTRL	0x0000_1B0B

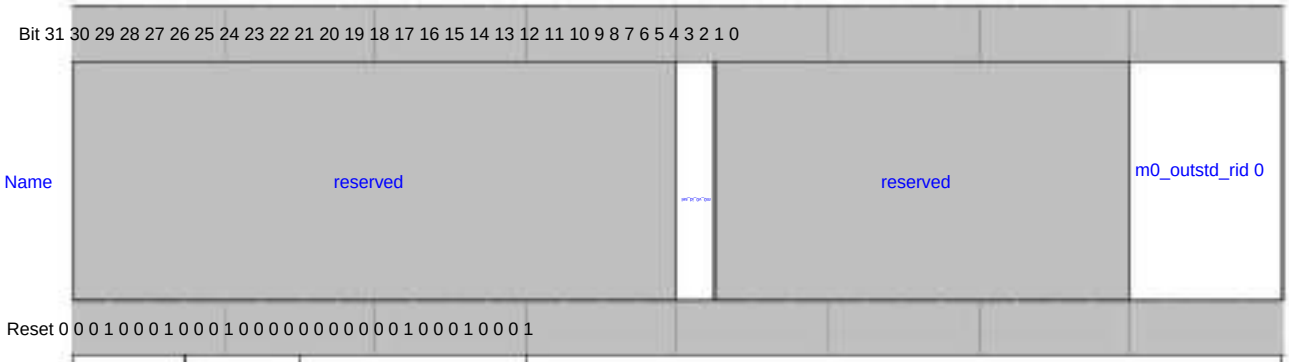


Bits	Access	Name	Description
[31:14]	RO	reserved	reserve
[13:11]	RW	rft_emab	RFT MEM's EMAB speed control register.
[10:8]	RW	rft_emaa	RFT EMAA side speed regulation register of MEM.
[7:5]	RO	reserved	reserve.
[4:3]	RW	rfs_emaw	EMAW side speed regulation register of RFS MEM.
[2:0]	RW	rfs_ema	EMA side speed regulation register of RFS MEM.

VOAXICTRL

VOAXICTRL is the VO AXI bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	VOAXICTRL	0x1110_0111



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	m0_v0_id_sel	m0 Read multiple ID output enable. 0: One ID output; 1: Multiple ID output.
[14:4]	RO	reserved	reserve.

[3:0] RW	m0_outstd_rid0		axi master 0 read ID0 outstanding configuration, the configuration range is 0~7.

VO_MUX

VO_MUX is the multiplex register of VO output interface.

Offset Address	Register Name	Total Reset Value
0x0100	VO_MUX	0x0001_6540

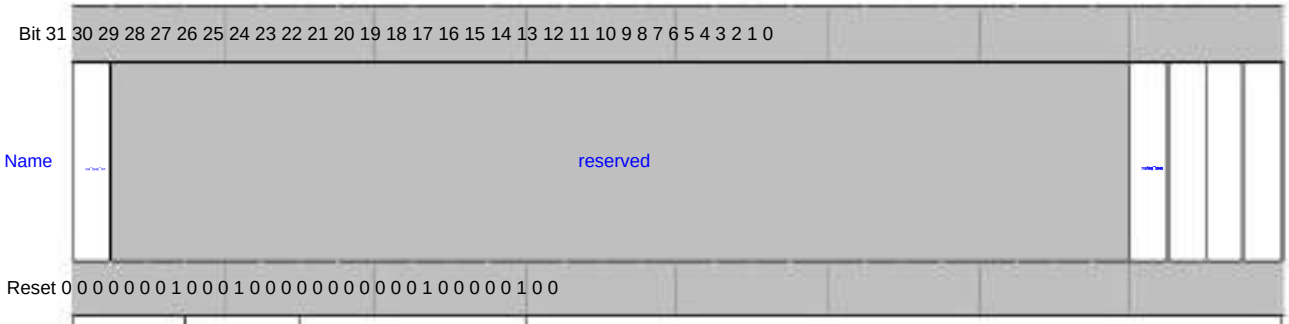
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	digital_sel				reserved																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	digital_sel	Digital port data selection (default 0). 0ÿBT.1120ÿ 1ÿBT.656ÿ 2ÿLCDÿ Other: reserved.
[27:0]	RO	reserved	reserve.

VO_MUX_TESTSYNC

VO_MUX_TESTSYNC is the test register of VO output interface. (VOPINTEST)

Offset Address	Register Name	Total Reset Value
0x0108	VO_MUX_TESTSYNC	0x0110_0104

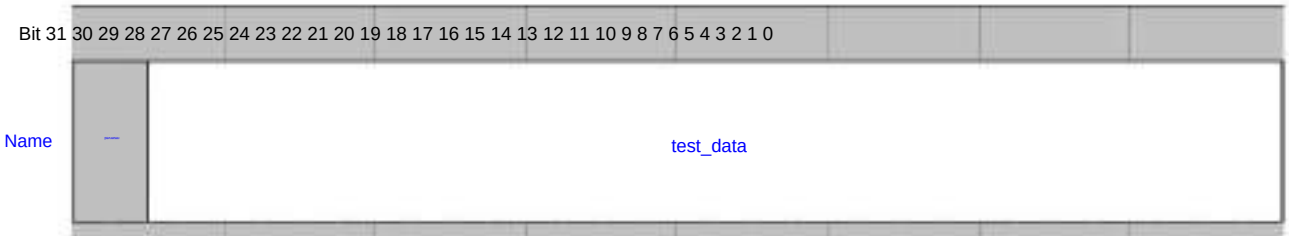


Bits	Access	Name	Description
[31]	RW	vo_test_en	VDP output interface test mode enable. 0: disable; 1: enable.
[30:4]	RO	reserved	reserve.
[3]	RW	test_field	field signal test value.
[2]	RW	test_vsync	vsync signal test value.
[1]	RW	test_hsync	hsync signal test value.
[0]	RW	test_dv	dv signal test value.

VO_MUX_TESTDATA

VO_MUX_TESTDATA is the test data register of VO output interface. (VOPINTEST)

Offset Address	Register Name	Total Reset Value
0x010C	VO_MUX_TESTDATA	0x0000_0000



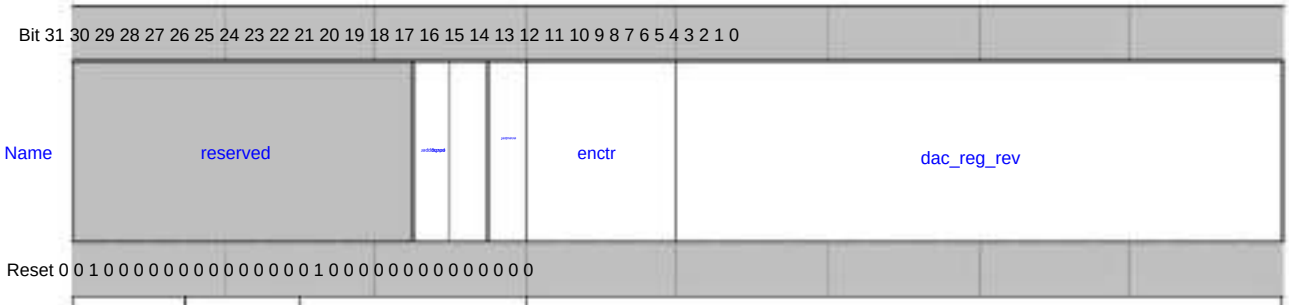
Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.

[29:0]	RW	test_data	Data output value register in test mode. The DAC (CVBS) channel output is the lower 10bit of the register, the BT.1120 channel output is the lower 16bit of the register, the LCD channel output is the {29~22,19~12,9~2}bit of the register, and the output of other channels is the register value , the order from high to low is RGB or YUV.

VO_DAC_CTRL

VO_DAC_CTRL is the VO DAC control register.

Offset Address	Register Name	Total Reset Value
0x0120	VO_DAC_CTRL	0x2000_4000



Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22]	RW	envbg	VBG reference voltage enable. 0: off; 1: open.
[21]	RW	pdchopper	Chopper enable for VBG. 0: enable chopper function; 1: disable chopper function.
[20]	RW	enextref	Output test enable for VBG. 0: Use internal VBG, VBG is not output to the test pin; 1: VBG output to the outside for testing.
[19:16]	RW	enctr	Output test enable for VBG. 0: Use internal VBG, VBG is not output to the test pin; 1: VBG output to the outside for testing.
[15:0]	RW	dac_reg_rev	Reserve test.

VO_DAC_0_CTRL

VO_DAC_0_CTRL is the VO DAC 0 channel control register.

Offset Address	Register Name	Total Reset Value
0x0134	VO_DAC_0_CTRL	0x1000_0000

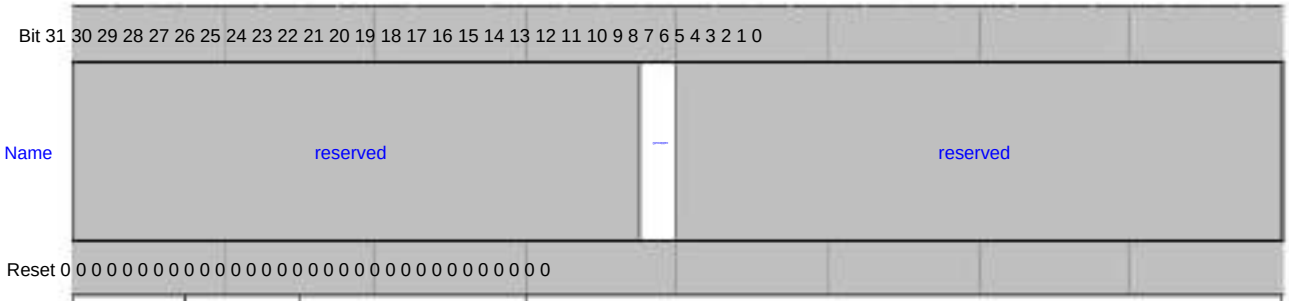
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																				dac0gc										
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31] RW dac0en		DAC enable terminal. 0: disable; 1: enable.
[30:10] RO	reserved	reserve.
[9:4] RW dac0gc		DAC output amplitude control register. The full-scale output voltage range covers 0.52RO1.37V, the output amplitude is divided into 64 levels of adjustment, and the adjustment accuracy is 1%. The calculation formula is Ifs=13.9+GAIN*0.358(m A)ÿ 000000ÿ0.52V ….. 111111:1.37V
[3:2] RO	reserved	reserve.
[1:0] RW cablectr0		VREF_CABLE Reference Voltage Regulation for DAC. 00: default normal; 01ÿ-10%ÿ 10ÿ-20%ÿ 11ÿ+10%ÿ

VO_DAC_STAT0

VO_DAC_STAT0 is the VO DAC status 0 register.

Offset Address	Register Name	Total Reset Value
0x0140	VO_DAC_STAT0	0x0000_0000

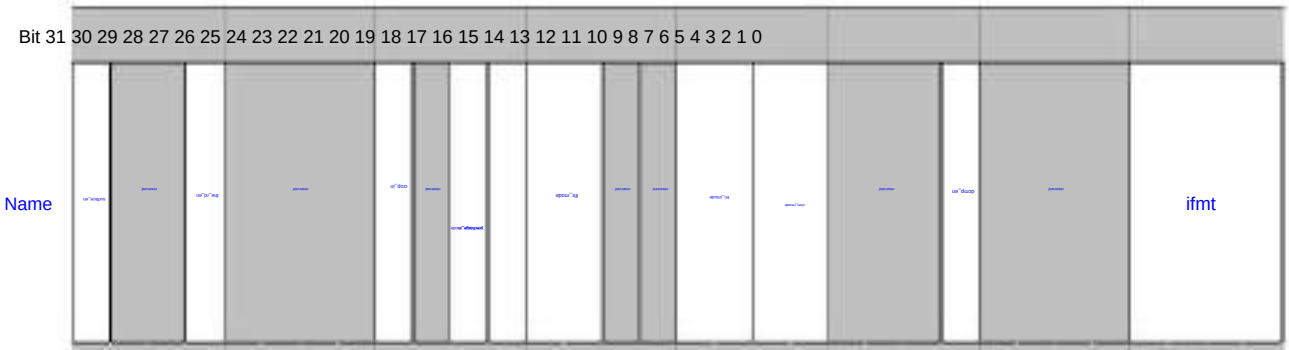


Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RO	cableout0	cableout0 feedback signal
[15:0]	RO	reserved	reserve.

V1_CTRL

V1_CTRL is the relevant information of the layer that can be configured by this register, and it is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x1000	V1_CTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	surface_en	surface is enabled. non-immediate registers. 0: disable; 1: enable.
[30:29]	RO	reserved	reserve.
[28]	RW	die_rd_en	Chroma channel repeat read enable (only input 420 is valid). 0: forbidden; 1: enable.

[27:24] RO		reserved	reserve.
[23] RW crop_en			crop enabled, non-immediate registers. 0: forbidden; 1: enable.
[22] RO		reserved	reserve.
[21] RW precharge_en			The PreCharge state is enabled, and it is valid when the PreCharge mode is 1 (software mode). 0: forbidden; 1: enable.
[20] RW precharge_mode			FDR FIFO PreCharge mode: 0: Hardware mode, the hardware automatically enters the precharge state at the end of the frame; 1: Software mode, enters/leaves the precharge state under software control.
[19:18] RW ifir_mode			Horizontal chroma IFIR mode. 00: reserved; 01: Chroma IFIR copy mode; 10: bilinear interpolation; 11: 16th order half-band filter.
[17] RO		reserved	reserve.
[16] RO		reserved	reserve.
[15:14] RW lm_rmode			Luminance progressive interlaced read mode. 00: The read mode is bound to the interface; 01: Read frame buffer data line by line; 10: When reading interlaced, read into the top field; 11: When reading interlaced, read the bottom field.
[13:12] RW chm_rmode			Chroma progressive interlaced read mode. 00: The read mode is bound to the interface; 01: Read the frame buffer data line by line; 10: When reading interlaced, read into the top field; 11: When reading interlaced, read the bottom field.
[11:9] RO		reserved	reserve.
[8] RW dcmp_en			Decompression enabled. 0: disable; 1: enable.
[7:4] RO		reserved	reserve.

[3:0] RW ifmt			Input data format. 0x1ÿSPYCbCr400ÿ 0x3ÿSPYCbCr420ÿ 0x4ÿSPYCbCr422ÿ Other: reserved.

V1_UPD

V1_UPD is the update enable register for the V1 channel.

Offset Address	Register Name	Total Reset Value
0x1004	V1_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															chnUpd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WC	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

V1_IRESO

V1_IRESO is the input resolution register, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x1028	V1_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								them																				iw			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Take the frame height as the reference, and use the row unit.
[11:0]	RW	iw	Width, in pixels. The actual width is minus 1.

V1_ORESO

V1_ORESO is the output resolution register, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x102C	V1_ORESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved oh ow
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	oh	Height, behavioral unit. The actual height is minus 1. Take the frame height as the reference, and use the row unit.
[11:0]	RW	ow	Width, in pixels. The actual width is minus 1.

V1_DCMP_SGMT_CROP

V1_DCMP_SGMT_CROP decompresses the crop register for the input segment, which is a non-immediate register

Offset Address	Register Name	Total Reset Value
0x1034	V1_DCMP_SGMT_CROP	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dcmp_xlsgmt dcmp_xfsgmt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	dcmp_xlsgmt	segment decompression terminal segment;
[3:0]	RW	dcmp_xfsgmt	segment decompression starting segment;

V1_CBMPARA

V1_CBMPARA is an overlay related parameter, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x1038	V1_CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	galpha	Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

V1_CPOS

V1_CPOS is the horizontal clipping coordinate register of the source image

Offset Address	Register Name	Total Reset Value
0x1044	V1_CPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	src_xlpos	src_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	src_xlpos	The horizontal crop end coordinates of the source image.
[11:0]	RW	src_xfpos	The horizontal crop start coordinates of the source image.

V1_DFPOS

V1_DFPOS is the starting position of Surface in the display window (First POSition), not an immediate register.

Offset Address	Register Name	Total Reset Value
0x1060	V1_DFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	disp_yfpos	disp_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:12] RW	disp_yfpos		display column start coordinates, Take the frame height as the reference, and use the row unit.
[11:0] RW	disp_xfpos		Displays the row start coordinates.

V1_DLPOS

V1_DLPOS is the end position of Surface in the display window (Last POSition), in pixels, not an immediate register.

Offset Address	Register Name	Total Reset Value
0x1064	V1_DLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Displays the column end coordinates. Take the frame height as the reference, and use the row unit.
[11:0]	RW	disp_xlpos	Display line end coordinates.

V1_CSC_IDC

V1_CSC_IDC is the input DC component register for color space conversion, and it is an immediate register.

Offset Address	Register Name	Total Reset Value
0x1080	V1_CSC_IDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscidc1	cscidc0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22]	RW	csc_en	CSC enable control signal. 0: CSC disabled; 1: CSC enabled.

Offset Address	Register Name	Total Reset Value
0x1080	V1_CSC_IDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / cscidc1 / cscidc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[21:11]	RW	cscidc1	Input U/G component DC parameters, MSB is the sign bit. complement representation.
[10:0]	RW	cscidc0	Input the DC parameter of V/B component, MSB is the sign bit. complement representation.

V1_CSC_ODC

V1_CSC_ODC is the color space conversion output DC component register, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x1084	V1_CSC_ODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / cscodc1 / cscodc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22]	RW	csc_sign_mode	CSC output mode control signal. 0: CSC outputs 10bit unsigned number; 1: CSC outputs 12bit signed number.
[21:11]	RW	cscodc1	Output U/G component DC parameters, MSB is the sign bit. complement representation.
[10:0]	RW	cscodc0	Output Y/R component DC parameters, MSB is the sign bit. complement representation.

V1_CSC_IODC

V1_CSC_IODC is the color space conversion input/output DC component register, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x1088	V1_CSC_IODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscidc2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:11]	RW	cscodc2	Output the DC parameter of V/B component, MSB is the sign bit. complement representation.
[10:0]	RW	cscidc2	Input Y/R component DC parameters, MSB is the sign bit. complement representation.

V1_CSC_P0

V1_CSC_P0 is color space conversion parameter 0, which is an instant register.

Offset Address	Register Name	Total Reset Value
0x108C	V1_CSC_P0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	—	cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RW	cscp01	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RW	cscp00	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

V1_CSC_P1

V1_CSC_P1 is color space conversion parameter 1, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x1090	V1_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp10															—	cscp02														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RW	cscp10	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RW	cscp02	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

V1_CSC_P2

V1_CSC_P2 is color space conversion parameter 2, which is an instant register.

Offset Address	Register Name	Total Reset Value
0x1094	V1_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp12															—	cscp11														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RW	cscp12	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RW	cscp11	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

V1_CSC_P3

V1_CSC_P3 is color space conversion parameter 3, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x1098	V1_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp21															—	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RW	cscp21	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RW	cscp20	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

V1_CSC_P4

V1_CSC_P4 is color space conversion parameter 4, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x109C	V1_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													cscp22		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:0]	RW	cscp22	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

V1_P0LADDR

V1_P0LADDR is the video layer luma address register.

Offset Address	Register Name	Total Reset Value
0x1204	V1_P0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Video layer luma first address register.

V1_P0CADDR

V1_P0CADDR is the video layer chroma address register.

Offset Address	Register Name	Total Reset Value
0x1208	V1_P0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Video layer chroma first address register.

V1_P0STRIDE

V1_P0STRIDE is the video layer stride register.

Offset Address	Register Name	Total Reset Value
0x120C	V1_P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	The stride of video layer chroma buffer (useful for semi-planaer format), 128bit alignment.
[15:0]	RW	surface_stride	The stride of the luma buffer of the video layer. (For the semi-planaer format, it refers to the stride of brightness), 128bit alignment.

V1_LADDROFFSET

V1_LADDROFFSET is the brightness compression data address offset register relative to the header information address, it is valid when decompression is enabled, and it is a non-immediate register

Offset Address	Register Name	Total Reset Value
0x1640	V1_LADDROFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	laddr_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	laddr_offset	Luma compressed data address relative to header information address offset.

V1_CADDROFFSET

V1_CADDROFFSET is the chroma compressed data address offset register relative to the header information address, it is valid when decompression is enabled, and it is a non-immediate register

Offset Address	Register Name	Total Reset Value
0x1644	V1_CADDROFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	caddr_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	caddr_offset	The offset of chroma compressed data address relative to header information address.

V1_DCMP_LSTATE0

V1_DCMP_LSTATE0 is the video layer luma channel decompression status register 0.

Offset Address	Register Name	Total Reset Value
0x1720	V1_DCMP_LSTATE0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dcmp_l_state0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	dcmp_l_state0	Video layer luma channel decompression state register 0.

V1_DCMP_LSTATE1

V1_DCMP_LSTATE1 is the video layer luma channel decompression status register 1.

Offset Address	Register Name	Total Reset Value
0x1724	V1_DCMP_LSTATE1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dcmp_l_state1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	dcmp_l_state1	Video layer luma channel decompression state register 1.

V1_DCMP_CSTATE0

V1_DCMP_CSTATE0 is the decompression status register 0 of the video layer chrominance channel.

Offset Address	Register Name	Total Reset Value
0x1728	V1_DCMP_CSTATE0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dcmp_c_state0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	dcmp_c_state0	Video layer chroma channel decompression state register 0.

V1_DCMP_CSTATE1

V1_DCMP_CSTATE1 is the video layer chrominance channel decompression status register 1.

Offset Address	Register Name	Total Reset Value
0x172C	V1_DCMP_CSTATE1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dcmp_c_state1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	dcmp_c_state1	Video layer chroma channel decompression state register 1.

V1_DCMPERRCLR

V1_DCMPERRCLR is the clear register for video layer decompression error status. Write 1 to clear.

Offset Address	Register Name	Total Reset Value
0x1730	V1_DCMPERRCLR	0x0000_0000

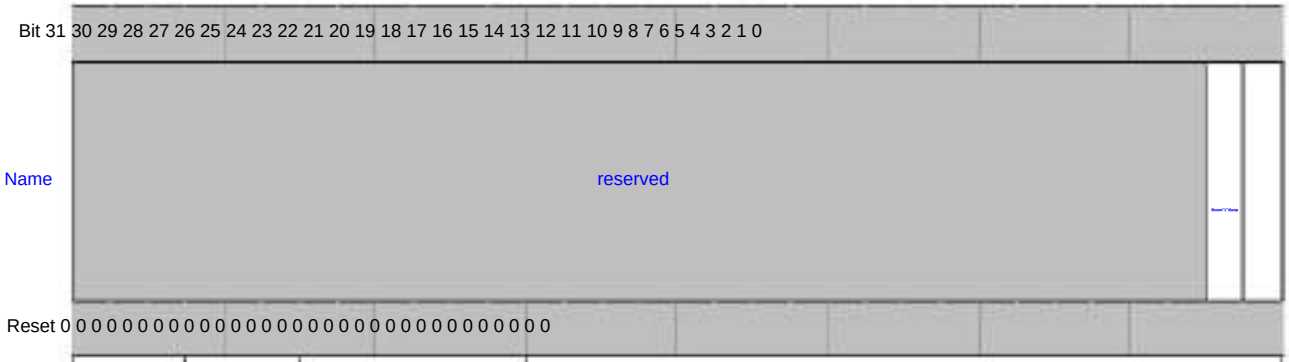
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	WC	dcmp_c_errclr	Chroma channel decompression error status clear register. 0: not cleared; 1: cleared.
[0]	WC	dcmp_l_errclr	Luma channel decompression error status clear register. 0: not cleared; 1: cleared.

V1_DCMP_ERR

V1_DCMP_ERR is the video layer decompression error signal register.

Offset Address	Register Name	Total Reset Value
0x1734	V1_DCMP_ERR	0x0000_0000

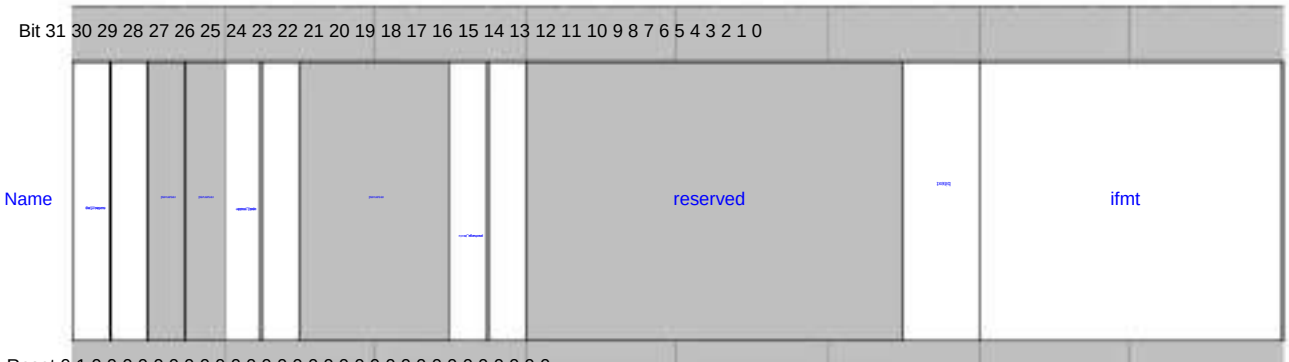


Bits	Access Name		Description
[31:2]	RO	reserved	reserve
[1]	RO	dcmp_c_wrong	Chroma channel decompression error signal. 0: Decompression is correct; 1: Decompression error.
[0]	RO	dcmp_l_wrong	Luma channel decompression error signal. 0: Decompression is correct; 1: Decompression error.

G2_CTRL

G2_CTRL is the relevant information register that can configure the layer for this register. is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x7000	G2_CTRL	0x4000_0000



Bits	Access Name		Description
[31] RW	surface_en		surface is enabled. non-immediate registers. 0: disable; 1: enable.

[30] RW nosec_flag			The bus interface signals the operational safety attributes. 0: security attribute; 1: Non-secure attribute.
[29] RO		reserved	reserve.
[28] RO		reserved	reserve.
[27] RW upd_mode			update mode. 0: frame update; 1: field update.
[26] RW read_mode			Data read mode. 0: Automatically select according to the interface reading mode (read line by line when displaying line by line, read line by line when displaying interlaced); 1: Force to read line by line.
[25:22] RO		reserved	reserve.
[21] RW precharge_en			The PreCharge state is enabled, and it is valid when the PreCharge mode is 1 (software mode). 0: disable; 1: enable.
[20] RW precharge_mode			FDR FIFO PreCharge mode. 0: Hardware mode, the hardware automatically enters the precharge state at the end of the frame; 1: Software mode, the software controls the entry/exit of the precharge state.
[19:10] RO		reserved	reserve.
[9:8] RW bitext			Layer input bitmap Bit Bit extension mode. 00: Low bit extension 0; 10: The lower bit extends the highest bit; 11: The lower bits extend the highest bits.
[7:0] RW ifmt			Input data format. 0x48ÿARGB4444ÿ 0x49ÿARGB1555ÿ Other: reserved.

G2_UPD

G2_UPD is the graphics layer update enable register.

Offset Address	Register Name	Total Reset Value
0x7004	G2_UPD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	regup	The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

G2_ADDR

G2_ADDR is the graphics layer address register. In the case of horizontal pixel offset, refer to the G2SFPOS description for address calculation.

Offset Address	Register Name	Total Reset Value
0x7010	G2_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	surface_addr	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Surface frame buffer address.

G2_STRIDE

G2_STRIDE is the stride register of graphics layer.

Offset Address	Register Name	Total Reset Value
0x701C	G2_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve;

Offset Address	Register Name	Total Reset Value
0x701C	G2_STRIDE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	surface_stride
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[15:0]	RW	surface_stride	The stride of the frame buffer.

G2_IRESO

G2_IRESO is the input resolution register, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x7020	G2_IRESO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	them	iw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	ih	Height, behavioral unit. The actual height is minus 1. Note: For interlaced output, the actual height of the layer must be an even number. There is no such limitation for progressive output.
[11:0]	RW	iw	Width, in pixels. The actual width is minus 1. Note: The actual width of the layer must be an even number.

G2_SFPOS

G2_SFPOS is the starting position of the data that Surface needs to read in the source bitmap, not an immediate register. When the read position is not 128-bit-word aligned, this register indicates the number of pixels required to fill the entire 128-bit-word. Please note: The offset of the starting position cannot exceed a 128-bit-word, and the part beyond the 128-bit-word is indicated by the address.

The specific calculation method is as follows:

Let the initial address of the graphics layer of the original image be addr_ori, the address of the graphics layer allocated to the logic is addr_offset, the offset of the graphics layer is offsetp pixels, and the data format of the graphics layer is bpp (for example, bpp=32 of ARGB8888), then

G2ADDR=addr_offset = addr_ori + int(offsetp*bpp/128)ÿ

G2SFPOS=offset%128ÿ

Among them, int means rounding operation, % means modulo operation.

Offset Address	Register Name	Total Reset Value
0x7024	G2_SFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	src_xfpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6:0]	RW	src_xfpos	The starting X coordinate value of the source, 0 is the first pixel of a line.

G2_CBMPARA

G2_CBMPARA is the overlay related parameter, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x7030	G2_CBMPARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
Name	reserved					reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0						

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RW	key_mode	color key mode. 0: When Keymin <= Pixel <= Keymax is met, it will be treated as key color; 1: When Pixel <= Keymin or Pixel >= Keymax is met, it will be treated as key color.
[14]	RW	key_en	color key enable. 0: forbidden; 1: enable.
[13]	RW	premult_en	The input bitmap is a premultiplied image. 0: non-premultiplied image; 1: Premultiplied map.

[12] RW palpha_en			Pixel alpha enabled. 0: forbidden; 1: enable.
[11:8] RO		reserved	reserve.
[7:0] RW galpha			Overlays the global alpha value. The value range is from 0 to 255, 255 is fully opaque, and 0 is fully transparent.

G2_CKEYMAX

G2_CKEYMAX is the maximum color key value, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x7034	G2_CKEYMAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	wa0	keyr_max	keyg_max	keyb_max
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RW	of 0	alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, replace it with this value.
[23:16]	RW	keyr_max	The maximum value of the colry key R component.
[15:8]	RW	keyg_max	The maximum value of the color key G component.
[7:0]	RW	keyb_max	Color key B component maximum value.

G2_CKEYMIN

G2_CKEYMIN is the minimum value of the color key, which is a non-immediate register.

Offset Address	Register Name	Total Reset Value
0x7038	G2_CKEYMIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	va1	keyr_min	keyg_min	storage_min
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RW	va1	alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, replace it with this value.

[23:16] RW	keyr_min		colry key R component minimum value.
[15:8] RW	keyg_min		The minimum value of the color key G component.
[7:0] RW	keyb_min		Color key B component minimum value.

G2_CMASK

G2_CMASK is the color key mask value, which is a non-immediate register. If the corresponding bit is 1, it means that the corresponding bit of the pixel remains unchanged during the Key comparison process; if the corresponding bit is 0, it means that the corresponding bit of the pixel is forced to be set to 0 no matter it is 0 or 1 during the Key comparison process

Offset Address	Register Name	Total Reset Value
0x703C	G2_CMASK	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	kmsk_r	kmsk_g	kmsk_b
Reset	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	kmsk_r	The R component of the color key mask.
[15:8]	RW	kmsk_g	The G component of the color key mask.
[7:0]	RW	kmsk_b	The B component of the color key mask.

G2_DFPOS

G2_DFPOS is the starting position of Surface in the display window (First POSition), in pixels, not an immediate register.

Offset Address	Register Name	Total Reset Value
0x7080	G2_DFPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	disp_yfpos	disp_xfpos	
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_yfpos	Column start coordinates.
[11:0]	RW	disp_xfpos	Row start coordinates.

G2_DLPOS

G2_DLPOS is the end position of Surface in the display window (Last POSition), in pixels, not an immediate register.

Offset Address	Register Name	Total Reset Value
0x7084	G2_DLPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	disp_ylpos	disp_xlpos
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:12]	RW	disp_ylpos	Column end coordinates.
[11:0]	RW	disp_xlpos	Line end coordinates.

G2_CSC_IDC

G2_CSC_IDC is the input DC component register for color space conversion, and it is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70C0	G2_CSC_IDC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	cscidc1	cscidc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.

[25:23] RW	csc_mode		It is only valid when the CSC coefficient of G2 layer is solidified. 000ÿreservedÿ 001ÿYUV2YUVÿ 010ÿYUV601_RGBÿ 011ÿYUV709_RGBÿ 100ÿYUV2YUV_709_601ÿ 101ÿYUV2YUV_601_709ÿ 110ÿRGB2YUV_601ÿ 111ÿRGB2YUV_709ÿ
[22] RW	csc_en		CSC enable control signal. 0: CSC disabled; 1: CSC enabled.
[21:11] RO		cscidc1	Input U/G component DC parameters, MSB is the sign bit. complement representation.
[10:0] RO		cscidc0	Input the DC parameter of V/B component, MSB is the sign bit. complement representation.

G2_CSC_ODC

G2_CSC_ODC is the color space conversion output DC component register, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70C4	G2_CSC_ODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Name	reserved	cscodc1	cscodc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22]	RO	csc_sign_mode	CSC output mode control signal. 0: CSC output 10bit unsigned number; 1: CSC outputs 12bit signed numbers.
[21:11]	RO	cscodc1	Output U/G component DC parameters, MSB is the sign bit. complement representation.
[10:0]	RO	cscodc0	Output Y/R component DC parameters, MSB is the sign bit. complement representation.

G2_CSC_IODC

G2_CSC_IODC is the color space conversion input/output DC component register, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70C8	G2_CSC_IODC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	cscodc2	cscidc2
Reset	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:22]	RO	reserved	reserve.
[21:11]	RO	cscodc2	Output the DC parameter of V/B component, MSB is the sign bit. complement representation.
[10:0]	RO	cscidc2	Input Y/R component DC parameters, MSB is the sign bit. complement representation.

G2_CSC_P0

G2_CSC_P0 is the color space conversion parameter 0, which is the real-time register.

Offset Address	Register Name	Total Reset Value
0x70CC	G2_CSC_P0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	—	cscp01	— cscp00
Reset	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31]	RO	reserved	reserve.
[30:16]	RO	cscp01	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RO	cscp00	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

G2_CSC_P1

G2_CSC_P1 is color space conversion parameter 1, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70D0	G2_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp10															—	cscp02														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RO	cscp10	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RO	cscp02	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

G2_CSC_P2

G2_CSC_P2 is color space conversion parameter 2, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70D4	G2_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp12															—	cscp11														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:16]	RO	cscp12	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.

[14:0] RO		cscp11	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

G2_CSC_P3

G2_CSC_P3 is color space conversion parameter 3, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70D8	G2_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	cscp21															—	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RO	reserved	reserve.
[30:16]	RO	cscp21	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.
[15]	RO	reserved	reserve.
[14:0]	RO	cscp20	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

G2_CSC_P4

G2_CSC_P4 is color space conversion parameter 4, which is an immediate register.

Offset Address	Register Name	Total Reset Value
0x70DC	G2_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												cscp22			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:15]	RO	reserved	reserve.
[14:0]	RO	cscp22	5.10 Data format: 1bit sign bit, 4bit integer bit, 10bit decimal place. complement representation.

CBM_BKG2

CBM_BKG2 is the overlay background color register for CBM Mixer2.

Offset Address	Register Name	Total Reset Value
0xB420	CBM_BKG2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	—	cbm_bkgy2	cbm_bkgcb2	cbm_bkgcr2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:20]	RW	cbm_bkgy2	CBM Mixer2 overlay background color, Y component.
[19:10]	RW	cbm_bkgcb2	CBM Mixer2 Overlay background color, Cb component.
[9:0]	RW	cbm_bkgcr2	CBM Mixer2 overlay background color, Cr component.

CBM_MIX2

CBM_MIX2 is the CBM Mixer2 priority configuration register. Updates are valid at vsync. mixer_prio_x indicates the configured layer for the xth priority.

This register is an immediate register.

Offset Address	Register Name	Total Reset Value
0xB428	CBM_MIX2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	mixer_prio1 mixer_prio0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

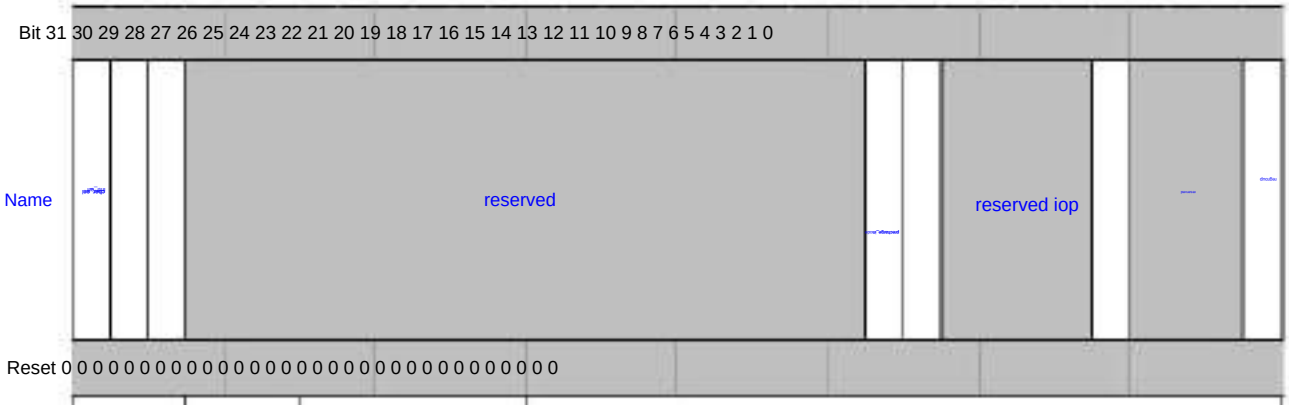
Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	mixer_prio1	CBM Mixer2's overlay priority configuration, representing a priority 1 driver layer. 0x0: means no layer driver; 0x9ÿv1ÿ 0xA: g2; others: reserved.

[3:0] RW	mixer_prio0		CBM Mixer2's overlay priority configuration, representing a priority 0 driver layer. 0x0: means no layer driver; 0x9ÿv1ÿ 0xA: g2; others: reserved.

DHD1_CTRL

DHD1_CTRL is the overall control register of the display channel. The configuration of all bits of this register must be no later than the DHD1_CTRL.intf_en bit, otherwise the configuration will not take effect.

Offset Address	Register Name	Total Reset Value
0xC400	DHD1_CTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	intf_en	Displays whether the interface is enabled. When enabled, the interface will output. is an immediate register. 0: disable; 1: enable.
[30]	RW	cbar_en	color bar enabled. When enabled, the interface outputs color bar. 0: forbidden; 1: enable.
[29]	RW	cbar_sel	Output color bar color space selection signal, instant register. 0ÿVGAÿ 1ÿYPbPrÿ
[28:11]	RO	reserved	reserve.
[10]	RW	precharge_en	The PreCharge state is enabled, and it is valid when the PreCharge mode is 1 (software mode). 0: Disable; 1: Enable.

[9] RW precharge_mode			AFIFO PreCharge mode. 0: Hardware mode, the hardware automatically enters the precharge state in the vertical blanking area; 1: Software mode, enters/leaves the precharge state under software control.
[8:5] RO		reserved	reserve.
[4] RW iop			Progressive or interlaced display, non-immediate register. 0: Interlaced display; 1: Display line by line.
[3:1] RO		reserved	reserve.
[0] WC regup			The surface's registers are updated. After the software configures the registers of this layer, write 1 to update them. After the update is completed, the hardware will automatically clear them.

DHD1_VSYNC

When DHD1_VSYNC is interlaced output, this register indicates the top field vertical synchronization timing; when it is progressive output, this register indicates the frame vertical synchronization timing. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0xC404	DHD1_VSYNC	0x0011_321B

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vfb	vbb	vact
Reset	0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 1 0 0 1 1	0 0 1 0 0 0 0 1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	vfb	For interlaced output: top field vertical blanking front porch; for progressive output: vertical blanking front porch.
[19:12]	RW	etc	For interlaced output: top field vertical blanking back porch; When outputting line by line: the width of the vertical pulse is added to the shoulder after the vertical blanking.
[11:0]	RW	vact	For interlaced output: the height of the active image in the top field; When outputting progressively: the height of the active image of one frame. The value of this register is minus 1 from the actual value.

DHD1_HSYNC1

When DHD1_HSYNC1 is interlaced or progressive output, the horizontal synchronization configuration register. non-immediate registers.

Offset Address	Register Name	Total Reset Value
0xC408	DHD1_HSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	1

Bits	Access Name		Description
[31:16]	RW	hbb	Horizontal blanking back shoulder, in pixels.
[15:0]	RW	hact	The number of horizontal pixels in the active area.

DHD1_HSYNC2

DHD1_HSYNC2 is the horizontal synchronization configuration register in the case of interlaced or progressive output, not an immediate register.

Offset Address	Register Name	Total Reset Value
0xC40C	DHD1_HSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access Name		Description
[31:16]	RW	Hamid	Bottom field vertical sync valid pixel value (valid data area).
[15:0]	RW	hfb	Horizontal blanking front shoulder, in pixels.

DHD1_VPLUS

When DHD1_VPLUS is an interlaced output, this register indicates the vertical synchronization timing of the bottom field, not an immediate register.

Offset Address	Register Name	Total Reset Value
0xC410	DHD1_VPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access Name		Description
[31:28]	RO	reserved	reserve.
[27:20]	RW	bvfb	For interlaced output: Bottom field vertical blanking front porch.

[19:12] RW bvbb			For interlaced output: the width of the vertical pulse of the porch after the vertical blanking of the bottom field.
[11:0] RW bvact			During interlaced output: the height of the active image in the bottom field. The value of this register is minus 1 from the actual value.

DHD1_PWR

DHD1_PWR is the sync signal pulse width, not an immediate register.

Offset Address	Register Name	Total Reset Value
0xC414	DHD1_PWR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vpw / hpw
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	vpw	The vertical pulse width is minus 1.
[15:0]	RW	hpw	Subtract 1 from the horizontal pulse width.

DHD1_VTTHD3

DHD1_VTTHD3 is the vertical timing threshold (Vertical Timing Threshold), which is an instant register. This register contains two threshold configurations, which can generate two interrupts independently.

Offset Address	Register Name	Total Reset Value
0xC418	DHD1_VTTHD3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	vtmgthd4	vtmgthd3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

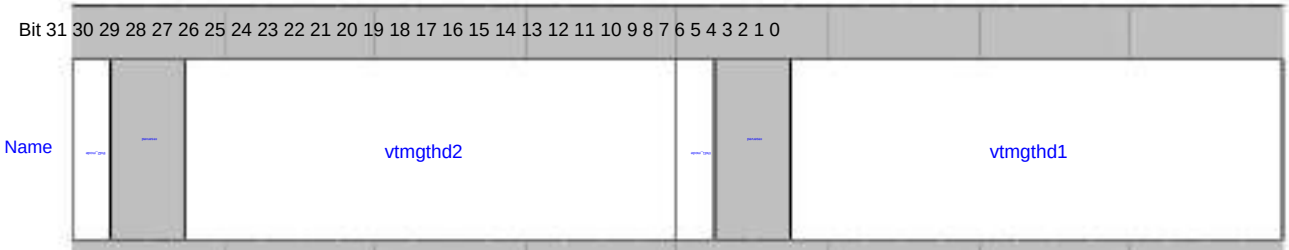
Bits	Access	Name	Description
[31]	RW	thd4_mode	Threshold 4 produces the pattern. 0: Frame mode, threshold counting is done in units of frames; 1: Field mode, the threshold counting is performed in units of field during interlaced display.
[30:29]	RO	reserved	reserve.

[28:16] RW	vtmgthd4		The vertical timing threshold value 4 is used for synchronous triggering of DHD and DSD. The interface timing start of DSD is later than that of DHD, which is equal to the number of rows configured by vtmgthd4.
[15] RW	thd3_mode		Threshold 3 Interrupt Generation Mode: 0: Frame mode, the threshold counting is performed in units of frames; 1: Field mode, the threshold counting is performed in units of fields in interlaced display.
[14:13] RO		reserved	reserve.
[12:0] RW	vtmgthd3		The vertical timing threshold value is 3, when the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd3_int] interrupt is triggered.

DHD1_VTTHD

DHD1_VTTHD is the vertical timing threshold (Vertical Timing Threshold), which is an immediate register. This register contains two threshold configurations, which can generate two interrupts independently.

Offset Address	Register Name	Total Reset Value
0xC41C	DHD1_VTTHD	0x0001_0001



Bits	Access	Name	Description
[31]	RW	thd2_mode	Threshold 2 Interrupt generation mode. 0: Frame mode, threshold counting is done in units of frames; 1: Field mode, the threshold counting is performed in units of field during interlaced display.
[30:29]	RO	reserved	reserve.
[28:16]	RW	vtmgthd2	Vertical timing threshold value 2, when the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd2_int] interrupt is triggered.
[15]	RW	thd1_mode	Threshold 1 Mode for interrupt generation. 0: Frame mode, threshold counting is done in units of frames; 1: Field mode, the threshold counting is performed in units of field during interlaced display.
[14:13]	RO	reserved	reserve.
[12:0]	RW	vtmgthd1	The vertical timing threshold value is 1, when the vertical timing counter reaches the threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHD1_PARATHD

DHD1_PARATHD is the PARA coefficient update point threshold register.

Offset Address	Register Name	Total Reset Value
0xC4B0	DHD1_PARATHD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_en	reserved																													to_thd	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dfs_en	DFS enable control bit. 0: disable; 1: enable.
[30:6]	RO	reserved	reserve.
[5:0]	RW	para_thd	PARA coefficient update point threshold register, indicating which line of the vertical post-blanking line generates the update point (this control bit is only valid after DFS is enabled).

DHD1_START_POS

DHD1_START_POS is the start position register of DHD channel start signal.

Offset Address	Register Name	Total Reset Value
0xC4C0	DHD1_START_POS	0x0000_0805

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																timing_start_pos								start_pos							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	timing_start_pos	The state machine of timing_gen starts working at the first few lines of the active area.
[7:0]	RW	start_pos	In online mode, the start signal is generated in the first few lines of the active area.

DHD1_STATE

DHD1_STATE is the DHD1 status register.

Offset Address	Register Name	Total Reset Value
0xC4F0	DHD1_STATE	0x0000_0006

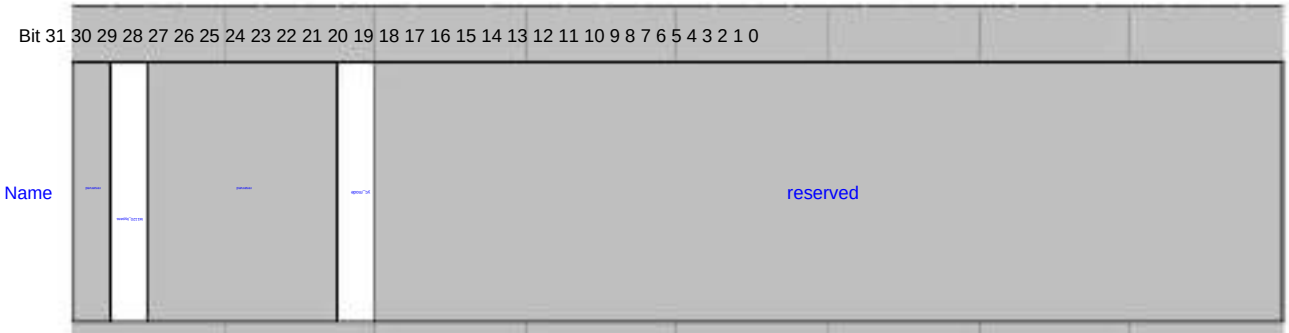
Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3	2	1	0
Name	reserved	count_int	vcnt			
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:16]	RO	count_int	DHD1 interrupt statistics counter. Add 1 each time a vertical timing interrupt is reported.
[15:3]	RO	vcnt	DHD1 Displays the row valid count.
[2]	RO	bottom_field	DHD1 shows top and bottom field logos. 0: top field; 1: Bottom field.
[1]	RO	vblank	DHD1 displays blanking zone identification. 0: effective area; 1: blanking zone.
[0]	RO	vback_blank	DHD1 Blanking logo after display. 0: not the post-blanking zone; 1: It is the rear blanking area.

BT_CTRL

BT_CTRL is the control register of BT656/BT1120.

Offset Address	Register Name	Total Reset Value
0xD200	BT_CTRL	0x0000_0000

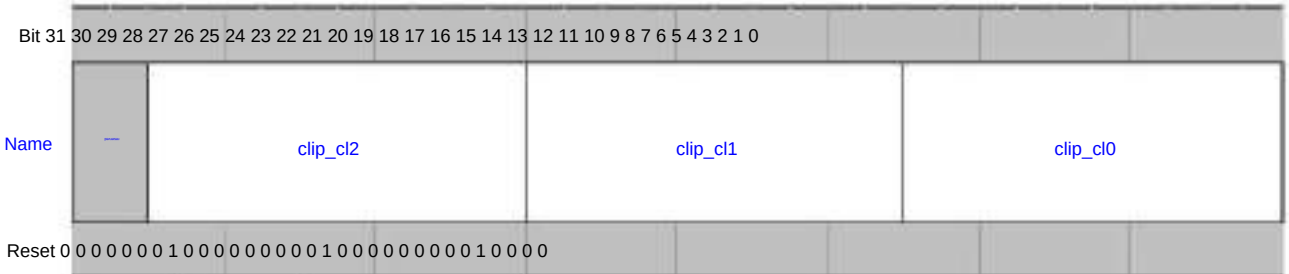


Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RW	bt1120_bypass	BT.1120 bypass mode. 0: forbidden; 1: enable.
[29:25]	RO	reserved	reserve.
[24]	RW	yc_mode	BT.1120 yc Interchange register. 0: Y is in high position, C is in low position; 1: Y is in the low position, C is in the high position.
[23:0]	RO	reserved	reserve.

BT_CLIP0_L

BT_CLIP0_L is the lowest threshold value register for BT.656/BT.1120 Clip processing, and it is an immediate register.

Offset Address	Register Name	Total Reset Value
0xD210	BT_CLIP0_L	0x0100_4010



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:20]	RW	clip_cl2	Component 2 Minimum threshold value Y/R, unsigned integer.

[19:10] RW	clip_cl1		Component 1 is the lowest threshold Cb/G, an unsigned integer.
[9:0] RW	clip_cl0		Component 0 is the lowest threshold Cr/B, an unsigned integer.

BT_CLIP0_H

BT_CLIP0_H is the highest threshold value register for BT656/BT1120 Clip processing, and it is an immediate register.

For example, BT.656 standard output needs to do CLIP processing on the output data.

Offset Address	Register Name	Total Reset Value
0xD214	BT_CLIP0_H	0x0EB3_C0F0

Bit	31 30 29 28	27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	—	clip_ch2	clip_ch1	clip_ch0
Reset	0 0 0 0	1 1 1 0 1 0 1	1 0 0 1	1 1 1 0 0 0 0 0 0 1 1 1 1 0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:20]	RW	clip_ch2	Component 2 The highest threshold Y/R, an unsigned integer.
[19:10]	RW	clip_ch1	Component 1 is the highest threshold Cb/G, an unsigned integer.
[9:0]	RW	clip_ch0	Component 0 is the highest threshold Cr/B, an unsigned integer.

BT_DITHER0_CTRL

BT_DITHER0_CTRL is the BT.656/BT.1120 Dither control register.

Offset Address	Register Name	Total Reset Value
0xD280	BT_DITHER0_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select register. 000: 12bit input, 10bit output, do not do dither, directly truncate; 001: 12bit input, 10bit output, time domain dither; 010: 12bit input, 10bit output, airspace dither; 011: 12bit input, 8bit output, time domain and airspace dither; 100: 12bit input, 10bit output, rounded; 101: 12bit input, 8bit output, rounded. Other: reserved.
[28:0]	RO	reserved	reserve.

BT_DITHER0_COEF0

BT_DITHER0_COEF0 is the BT656/BT1120 Dither Coefficient 0 register.

Offset Address	Register Name	Total Reset Value
0xD284	BT_DITHER0_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 used by dither in time domain mode.
[23:16]	RW	dither_coef2	Coefficient 2 used by dither in time domain mode.
[15:8]	RW	dither_coef1	Coefficient 1 used by time domain mode dither.
[7:0]	RW	dither_coef0	Coefficient 0 used by dither in time domain mode.

BT_DITHER0_COEF1

BT_DITHER0_COEF1 is the BT656/BT1120 Dither Coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xD288	BT_DITHER0_COEF1	0xDD66_4400

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dither_coef7	dither_coef6	dither_coef5	dither_coef4
Reset	1 1 0 1	1 1 0 1 0 1	1 0 0 1	1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 used by dither in time domain mode.
[23:16]	RW	dither_coef6	Coefficient 6 used by dither in time domain mode.
[15:8]	RW	dither_coef5	Coefficient 5 used by time domain mode dither.
[7:0]	RW	dither_coef4	Coefficient 4 used by dither in time domain mode.

LCD_CTRL

LCD_CTRL is the LCD control register.

Offset Address	Register Name	Total Reset Value
0xD400	LCD_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	RO	reserved	reserve.
[29]	RW	lcd_serial_mode	LCD serial mode. 0: parallel; 1: Serial.

[28] RW	lcd_serial_perd		LCD serial output single pixel clock cycle number. 0: 3 cycles; 1: 4 cycles.
[27] RW	lcd_parallel_order		LCD parallel output sequence. 0ÿRGBÿ 1ÿBGRÿ
[26] RW	lcd_data_inv		The LCD output bit is inverted. 0: High bit to low bit 15~0bit/23~0bit; 1: High bit to low bit 0~15bit/0~23bit.
[25] RW	lcd_parallel_mode		LCD parallel output bit width mode. 0ÿRGB565ÿ 1ÿRGB888ÿ
[24] RO		reserved	reserve.
[23:0] RO		reserved	reserve.

LCD_SYNC_INV

When LCD_SYNC_INV is LCD external synchronous timing input, the synchronous signal polarity configuration register. This register takes effect immediately after configuration, and will immediately affect the polarity of the corresponding synchronization signal.

Offset Address	Register Name	Total Reset Value
0xD408	LCD_SYNC_INV	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

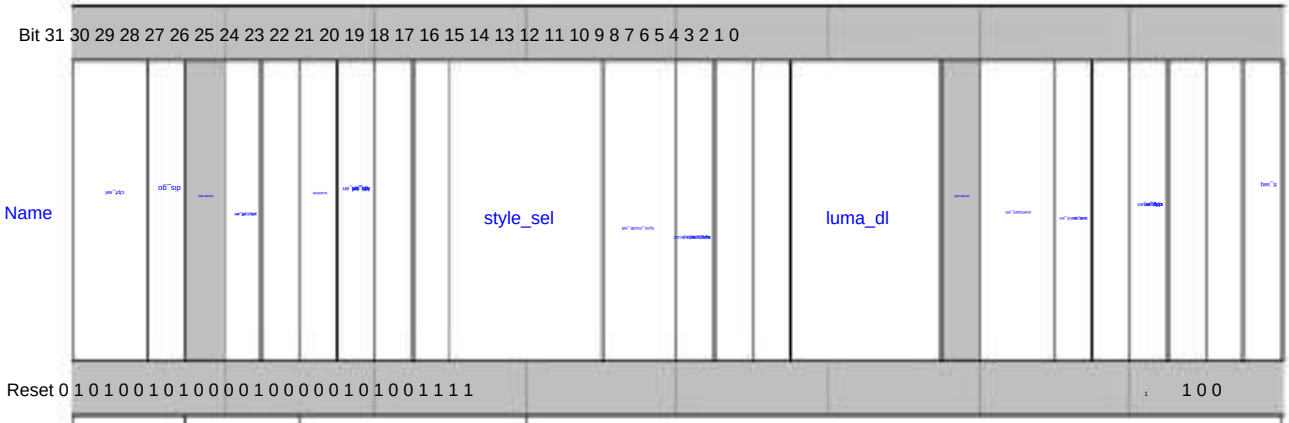
Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	f_inv	Parity field indication signal output inversion enable, instant register. 0: disable; 1: enable.
[2]	RW	vs_inv	Vertical sync pulse output inversion enable, immediate register. 0: forbidden; 1: enable.

[1] RW hs_inv			Horizontal sync pulse output inverting enable, immediate register. 0: forbidden; 1: enable.
[0] RW dv_inv			Data valid signal output inversion enable, instant register. 0: forbidden; 1: enable.

DATE_COEFF0

DATE_COEFF0 is the standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xF200	DATE_COEFF0	0x5284_14FC



Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Chroma low pass filter bandwidth selection. 00: 1.1MHz bandwidth (NTSC); 01: 1.3MHz bandwidth (PAL); 10: 1.6MHz bandwidth (test); 11: Reserved.
[29]	RW	dis_ire	For (M)NTSC and (M,N)PAL, the black level is higher than the blanking level 7.5IRE; for other systems, the black level is equal to the blanking level. This bit controls whether the black level should be 7.5 IRE above the blanking level. 0: The black level is higher than the blanking level by 7.5IRE; 1: The black level is equal to the blanking level.
[28]	RO	reserved	reserve.
[27]	RW	pal_half_en	PAL value half-line clipping enabled. 0: disable; 1: enable.

[26] RW pbpr_lpf_en			Component chroma low pass filtering enable. 0: disable; 1: enable.
[25] RW scanline			Set according to the number of scanning lines contained in each frame under different systems. For (M)NTSC, NTSC-J, (M)PAL, each frame contains 525 lines; for (B, D, J, H, I)PAL, (N)PAL, (Nc)PAL, each frame contains 625 lines. 0: Each frame contains 525 lines; 1: Each frame contains 625 lines.
[24] RW rgb_en			When intf_sel is configured as 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr is selected for component signal; 1: Use RGB for component signals.
[23] RW vbi_lpf_en			Vbi data low pass filter enable control. 0: No filter processing; 1: filter processing.
[22] RW fm_sel			FMsecam FM selection. 0: Secam FM adopts sin; 1: Secam FM adopts cos.
[21:18] RW style_sel			Cooperate with scanline to set the system of CVBS/S-Video output signal. When scanline is 0, that is, each frame contains 525 lines, the meaning is as follows: 0x1: (M)NTSC format; 0x2: NTSC-J format; 0x4: (M)PAL format. Other: reserved. When scanline is 1, that is, each frame contains 625 lines, the meanings are as follows: 0x1: (B, D, G, H, I) PAL system; 0x2: (N) PAL system; 0x4: (Nc) PAL system; 0x8: SECAM format. Other: reserved.

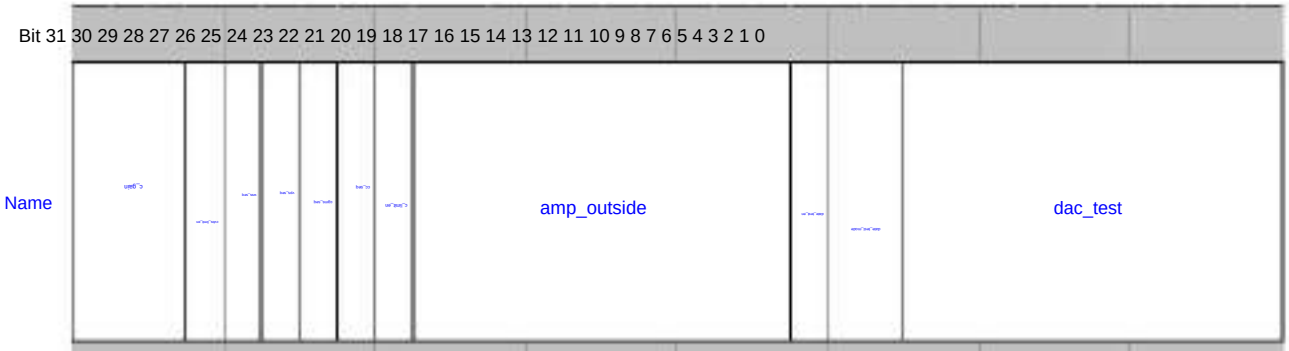
[17:16] RW sync_mode_sel			The high bit indicates whether the component output should include sync signals on all three channels, and this control bit only works when sync_mode_scart is configured as 0. The high bit is only valid when intf_sel is set to 100, that is, there is component output, meaning: 0: when component output, only one channel contains synchronous signal; 1: During component output, sync signals are included on all three channels. When this bit is set to 0, for YPbPr output, the sync channel can only be Y channel; for RGB output, it can only be G channel. The low bits indicate whether the RGB output has a blanking base or not. The low bit is only valid when intf_sel is set to 100 and rgb_en is set to 1, the meanings are: 0: no blanking base in RGB output; 1: There is a blanking base in RGB output.
[15] RW sync_mode_scart			This bit indicates that the 3 channels of the lower component are not superimposed and synchronized. 0: The component synchronization output is configured according to sync_mode_sel[1]; 1: The 3 channels of the component are not superimposed and synchronized.
[14] RW length_sel			Indicates the effective width of the line in pixels that each video line contains. 0: Output according to the line effective pixel width of BT.601 mode; 1: Output according to the line effective pixel width of BT.470 mode. When this bit is 0, the effective width of the row is 720 pixels. When this bit is configured as 1, for the 625-line system, the effective width of the line is 704 pixels; for the 525-line system, the effective width of the line is 712 pixels. The current version does not support dynamic configuration in BT.601 mode and BT.470 mode, and the configuration cannot be changed in the middle of the configuration after reset. It is recommended to set the fixed configuration to BT.601 mode, that is, to use the power-on reset value.
[13] RW agc_amp_sel			AGC pulse selection control bit. 0: Refer to the default value inside the image to generate AGC pulse (recommended); 1: Refer to the configuration outside the image to generate AGC pulse DATE_COEFF1[amp_outside].
[12:9] RW luma_dl			The amount by which the chroma signal leads or lags relative to the luma signal, in units of half a pixel width. The highest bit indicates the direction of displacement of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luma signal; 1: The chroma signal leads the chroma signal. The lower 3 bits represent the absolute value of the displacement of the chrominance signal relative to the luminance signal, expressed in binary, and the value range is from 0 to 7. 000: Chroma and brightness are aligned, no adjustment is made; 001~111: The chrominance signal leads or lags behind the luminance signal by 1~7 units.
[8]	RO	reserved	reserve.

[7:6] RW oversam_en			The first-level oversampling switch control bits include brightness oversampling switch control bits and chroma oversampling switch control bits. The high bit is the brightness oversampling switch control bit. 0: luma oversampling off; 1: luma oversampling on. The low bit is the chroma oversampling switch control bit. 0: chroma oversampling is off; 1: chroma oversampling is on.
[5] RW lunt_en			Brightness notch function switch control bit. 0: Luminance notch function is off; 1: The luma notch function is turned on.
[4] RW oversam2_en			The second-level oversampling switch control bit controls both the luma and chrominance channels. 0: Brightness oversampling is off; 1: Luma oversampling is on.
[3] RW chlp_en			Chroma low-pass filter function switch control bit. 0: Chroma low-pass filter function is off; 1: The chroma low-pass filter function is turned on.
[2] RW sylp_en			Synchronous low-pass filter function switch control bit. 0: Synchronous low-pass filter function is off; 1: The synchronous low-pass filter function is enabled.
[1] RW chgain_en			Chroma gain switch control bit. 0: chroma gain off; 1: Chroma gain is on.
[0] RW tt_seq			Configures the order in which bits in the Teletext data byte are sent. 0: from high to low; 1: From low to high.

DATE_COEFF1

DATE_COEFF1 is the amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xF204	DATE_COEFF1	0x0000_0000



Bits	Access	Name	Description
[31:29]	RW	c_gain	Color burst gain adjustment.
[28]	RW	cvbs_limit_en	CVBS limit switch control bit. 0: unlimited; 1: clipping.
[27]	RW	wss_seq	Configures the order in which bits in the WSS data byte are sent. 0: from high to low; 1: From low to high.
[26]	RW	vps_seq	Configures the order in which bits in the VPS data byte are sent. 0: from high to low; 1: from low to high.
[25]	RW	cgms_seq	Configures the order in which bits in the CGMS data byte are sent. 0: from high to low; 1: From low to high.
[24]	RW	cc_seq	Configure the order in which bits in the Closed Caption data byte are sent. 0: from high to low; 1: From low to high.
[23]	RW	c_limit_en	Chroma clip switch control bit. 0: unlimited; 1: clipping.
[22:13]	RW	amp_outside	External AGC pulse amplitude input.
[12]	RW	date_test_en	Test valid signal.
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE_COEFF2

DATE_COEFF2 is the DATE coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF208	DATE_COEFF2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	coef02
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	coef02	DATE coefficient 2 register.

DATE_COEFF3

DATE_COEFF3 is the DATE coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF20C	DATE_COEFF3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / coef03
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:0]	RW	coef03	DATE coefficient 3 register.

DATE_COEFF4

DATE_COEFF4 is the DATE coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF210	DATE_COEFF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:0]	RW	coef04	DATE coefficient 4 register.

DATE_COEFF5

DATE_COEFF5 is the DATE coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF214	DATE_COEFF5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:0]	RW	coef05	DATE coefficient 5 register.

DATE_COEFF6

DATE_COEFF6 is the DATE coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF218	DATE_COEFF6	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	[illegible]	reserved																									coef06_1						
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	coef06_0	DATE Coefficient 6 Register 0.
[30:23]	RO	reserved	reserve.
[22:0]	RW	coef06_1	DATE Factor 6 Register 1.

DATE_COEFF21

DATE_COEFF21 is the output matrix control register.

Offset Address	Register Name	Total Reset Value
0xF254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													[illegible]		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.

[2:0] RW	dac0_in_sel		DAC0 output mode selection. 000ÿ0ÿ 001ÿcvbsÿ 010ÿG/Yÿ 011ÿB/Pbÿ 100R/Prÿ 101ÿsvideo_yÿ 110ÿsvideo_cÿ 111ÿ0ÿ

DATE_COEFF22

DATE_COEFF22 is the DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xF258	DATE_COEFF22	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / video_phase_delta
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:0]	RW	video_phase_delta	DTO Initial phase configuration register.

DATE_COEFF23

DATE_COEFF23 is the VIDEO_OUT delay configuration register.

Offset Address	Register Name	Total Reset Value
0xF25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	dac0_out_dly	DAC0 output delay period. Take a 54MHz clock cycle as a unit, configure n delay cycles.

DATE_COEFF24

DATE_COEFF24 is the ColorBurst start position register.

Offset Address	Register Name	Total Reset Value
0xF260	DATE_COEFF24	0x0001_2C99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:0]	RW	burst_start	ColorBurst start position register.

DATE_ISRMASK

DATE_ISRMASK is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xF280	DATE_ISRMASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	tt_mask	Teletext interrupt mask bit. 0: Enable Teletext interrupt; 1: Shield Teletext interrupt.

DATE_ISRSTATE

DATE_ISRSTATE is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0xF284	DATE_ISRSTATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WC	tt_status	Teletext interrupt flag. When DATE has read all the Teletext data, the interrupt flag will be pulled high. To clear the interrupt, you need to write 1 to this bit.

DATE_ISR

DATE_ISR is the interrupt register.

Offset Address	Register Name	Total Reset Value
0xF288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RO	tt_int	Teletext interrupt register, tt_status Interrupt status after masked by tt_mask.

DATE_COEFF37

DATE_COEFF37 is the upsampling filter coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF294	DATE_COEFF37	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	for_y1_coeff3								for_y1_coeff2								for_y1_coeff1								for_y1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	fir_y1_coeff3	Luma upsampling filter coefficient 13.
[23:16]	RW	fir_y1_coeff2	Luma upsampling filter coefficient 12.
[15:8]	RW	fir_y1_coeff1	Luma upsampling filter coefficient 11.
[7:0]	RW	fir_y1_coeff0	Luma upsampling filter coefficient 10.

DATE_COEFF38

DATE_COEFF38 is the upsampling filter coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF298	DATE_COEFF38	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	for_y2_coeff1																for_y2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff1	Luma upsampling filter coefficient 21.
[15:0]	RW	fir_y2_coeff0	Luma upsampling filter coefficient 20.

DATE_COEFF39

DATE_COEFF39 is the upsampling filter coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF29C	DATE_COEFF39	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	for_y2_coeff3																for_y2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	1

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff3	Luma upsampling filter coefficient 23.
[15:0]	RW	fir_y2_coeff2	Luma upsampling filter coefficient 22.

DATE_COEFF40

DATE_COEFF40 is the upsampling filter coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	for_c1_coeff3								for_c1_coeff2								for_c1_coeff1								for_c1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	0	1	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	1

Bits	Access	Name	Description
[31:24]	RW	fir_c1_coeff3	Chroma upsampling filter coefficient 13.
[23:16]	RW	fir_c1_coeff2	Chroma upsampling filter coefficient 12.

Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	for_c1_coeff3	for_c1_coeff2	for_c1_coeff1	for_c1_coeff0
Reset	0 0 0 1	1 0 0 1 1	1 0 1 1	1 0 0 0 0 1 1 0 0 1 1 1 1 1 0 0 1

Bits	Access	Name	Description
[15:8]	RW	fir_c1_coeff1	Chroma upsampling filter coefficient 11.
[7:0]	RW	fir_c1_coeff0	Chroma upsampling filter coefficient 10.

DATE_COEFF41

DATE_COEFF41 is the upsampling filter coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2A4	DATE_COEFF41	0x003A_FFDA

Bit	31 30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	for_c2_coeff1	for_c2_coeff0
Reset	0 0 0 0 0 0 0 0 0 0 1	1 1 0 1 0 1 1 1 1 1 1 1 0 1 1 1 1 0 1 1 0 1 0

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff1	Chroma upsampling filter coefficient 21.
[15:0]	RW	fir_c2_coeff0	Chroma upsampling filter coefficient 20.

DATE_COEFF42

DATE_COEFF42 is the upsampling filter coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2A8	DATE_COEFF42	0x0148_FF97

Bit	31 30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	for_c2_coeff3	for_c2_coeff2
Reset	0 0 0 0 0 0 0 1 0 1 0	0 1 0 0 0 1 0 0 0 1 1 1 1 1 1 1 0 0 1 0 1

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff3	Chroma upsampling filter coefficient 23.
[15:0]	RW	fir_c2_coeff2	Chroma upsampling filter coefficient 22.

DATE_DACDET1

DATE_DACDET1 is the DAC auto-detection 1 register.

Offset Address	Register Name	Total Reset Value
0xF2C0	DATE_DACDET1	0x000D_0303

Bit	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	it_line	reserved	vdac_det_high
Reset	0 0 0 0 0 0	0 0 0 0 0 1 1 0 1 0	0 0 0 0 0 0	1 1 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	it_line	The row where the detection level is located.
[15:10]	RO	reserved	reserve.
[9:0]	RW	vdac_det_high	detection level value.

DATE_DACDET2

DATE_DACDET2 is the DAC auto-detection 2 register.

Offset Address	Register Name	Total Reset Value
0xF2C4	DATE_DACDET2	0x0030_0118

Bit	31	30 29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	it_pixel_wid	reserved	it_pixel_sta
Reset	0	0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1	1 0 0 0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC auto-detect enable. 0: disable; 1: enable.
[30:27]	RO	reserved	reserve.
[26:16]	RW	det_pixel_wid	level width.
[15:11]	RO	reserved	reserve.

[10:0] RW	det_pixel_sta	at the beginning of a row.	

DATE_COEFF50

DATE_COEFF50 is the oversampling filter coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF2C8	DATE_COEFF50	0x07FF_07FF

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 1 1 1	1 1 1	1 0 0 0 0 0 1	1 1 1 1 1 1

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 11.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 10.

DATE_COEFF51

DATE_COEFF51 is the oversampling filter coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF2CC	DATE_COEFF51	0x07FF_0204

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 1 1 1	1 1 1	1 0 0 0 0 0 0 1	0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 21.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 20.

DATE_COEFF52

DATE_COEFF52 is the oversampling filter coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF2D0	DATE_COEFF52	0x0000_07FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 31.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 30.

DATE_COEFF53

DATE_COEFF53 is the oversampling filter coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2D4	DATE_COEFF53	0x07BF_000C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 1 1 1 1 0 1	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1	1 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 41.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 40.

DATE_COEFF54

DATE_COEFF54 is the oversampling filter coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2D8	DATE_COEFF54	0x0135_0135

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 0 0 1 0 0 1	1 0 1 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 51.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 50.

DATE_COEFF55

DATE_COEFF55 is the oversampling filter coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2DC	DATE_COEFF55	0x000C_07BF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ovs_coeff1	reserved	ovs_coeff0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0	0 0 0 0 0 0 1 1 1 0 1 1 1 1 1 1

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ovs_coeff1	Luma oversampling filter coefficient 61.
[15:11]	RO	reserved	reserve.
[10:0]	RW	ovs_coeff0	Luma oversampling filter coefficient 60.

DATE_COEFF56

DATE_COEFF56 is the oversampling rounding register.

Offset Address	Register Name	Total Reset Value
0xF2E0	DATE_COEFF56	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	---
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	oversam2_round_e n	Double upsampling rounds. 0: disable; 1: enable.

DATE_COEFF57

DATE_COEFF57 is the CVBS gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E4	DATE_COEFF57	0x0080_8080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
Name	---	reserved	ycvbs_gain	u_gain	v_gain
Reset	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0				

Bits	Access	Name	Description
[31]	RW	cvbs_gain_en	CVBS gain enable. 0: disable; 1: enable.
[30:24]	RO	reserved	reserve.
[23:16]	RW	ycvbs_gain	Luminance Y gain control register.

[15:8] RW	u_gain		Chroma component U gain control register.
[7:0] RW	v_gain		Chroma component V gain control register.

DATE_COEFF58

DATE_COEFF58 is the component gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E8	DATE_COEFF58	0x0080_8080

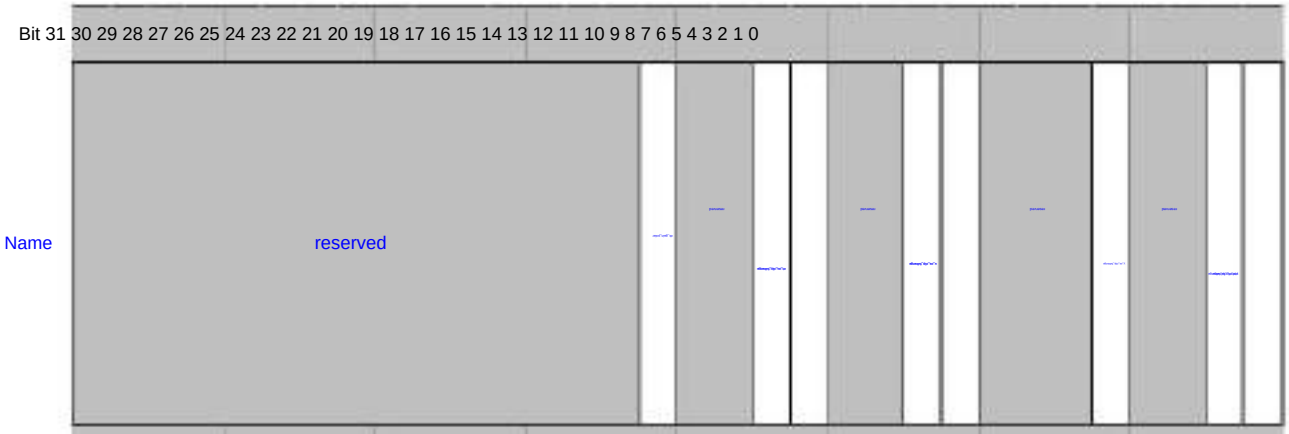
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	comp_gain_en	reserved															ycomp_gain								pb_gain							pr_gain	
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	comp_gain_en	Component gain enable. 0: disable; 1: enable.
[30:24]	RO	reserved	reserve.
[23:16]	RW	ycomp_gain	Luminance Y gain control register.
[15:8]	RW	pb_gain	Chroma component U gain control register.
[7:0]	RW	pr_gain	Chroma component V gain control register.

DATE_COEFF59

DATE_COEFF59 is the clip control bit register.

Offset Address	Register Name	Total Reset Value
0xF2EC	DATE_COEFF59	0x0001_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	cb_gain_polar	Color subcarrier polarity control. 0: Negative gain; 1: Positive gain.
[15:14]	RO	reserved	reserve.
[13]	RW	module clip. It is cr_os_clip_fullrang	The CR component is enabled in the upsampling 0: disable; 1: enable.
[12]	RW	module clip. It is cb_os_clip_fullrang	The CB component is enabled in the upsampling 0: disable; 1: enable.
[11:10]	RO	reserved	reserve.
disable; [9]	RW	v_os_clip_fullrange	V Upsampling module clip enabled. 0: 1: enable.
disable; [8]	RW	u_os_clip_fullrange	U The upsampling module clip is enabled. 0: 1: enable.
[7:5]	RO	reserved	reserve.
Disable; [4]	RW	y_os_clip_fullrange	1: Enable. The Y upsampling module clip is enabled. 0:

[3:2] RO		reserved	reserve.
0: disable; [1] RW clpf_clip_fullrange			The chroma low-pass module clip is enabled. 1: enable.
[0] RW		enabled. ge ynotch_clip_fullran	The luma notch module clip is 0: disable; 1: enable.

9.3 MIPI Rx

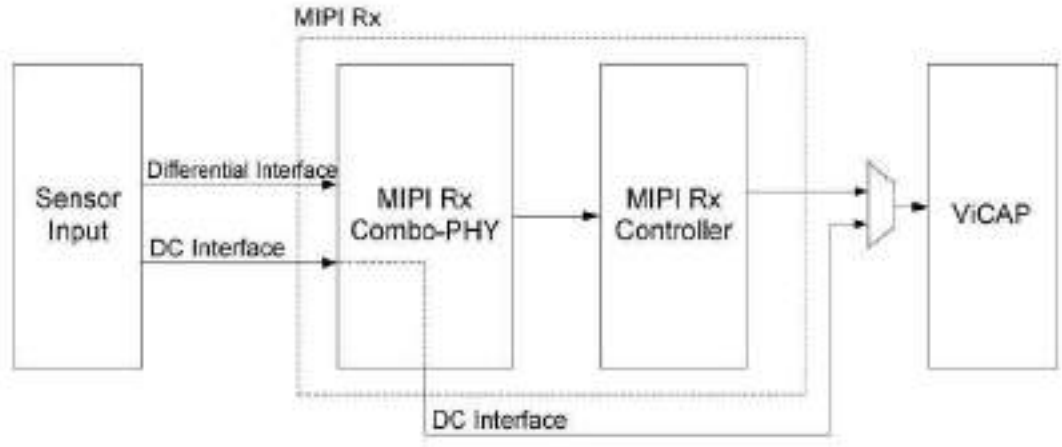
9.3.1 Overview

The mobile industry processor interface MIPI Rx (Mobile Industry Processor Interface Receiver), receives the original video data (BAYER RGB data) through the low-voltage differential signal, and converts it into DC (Digital Camera) timing and then passes it to the next-level module ViCAP (Video Capture).

MIPI Rx supports serial video signal input such as MIPI D-PHY, LVDS (Low-Voltage Differential Signal), HiSPi (High Speed Serial Pixel Interface), etc. The serial video interface can provide higher transmission bandwidth and enhance transmission stability. MIPI Rx is also compatible with DC video interface and supports 3.3V/1.8V DC parallel (Digital Camera) input, which saves the number of chip pins and provides better compatibility.

MIPI Rx includes combo-PHY and Controller. The functional block diagram and its position in the system are shown in Figure 9-18 .

Figure 9-18 MIPI Rx functional block diagram and its position in the system



9.3.2 Features

MIPI Rx has the following features:

Support up to 8-Lane MIPI D-PHY interface, up to 1.5Gbps/Lane Support up

to 12-Lane LVDS/ sub-LVDS /HiSPi interface, up to 1.5Gbps/Lane Support CMOS Parallel

1.8V/3.3V input

Support RAW8/ RAW10/ RAW12/ RAW14/ RAW16 data type analysis

Supports 4 frames of WDR, supports multiple WDR timings

supports LVDS/HiSPi mode pixel/sync code big and small endian configuration

supports channel number and channel order can be configured

9.3.3 Functional description

9.3.3.1 Typical applications

MIPI Rx is an acquisition unit that supports multiple differential video input interfaces, and its main function is the conversion of interface timing. Through different functional configurations, MIPI Rx can receive data from MIPI/LVDS/sub-LVDS/HiSPi/DC interface, and supports transmission requirements of various speeds and resolutions, and is compatible with various image sensors.

MIPI Rx supports up to 2Link/8Lane MIPI input, 3Link/12Lane LVDS/sub-LVDS/HiSPi input, each link can use its own external input clock, link1 and link2 can also choose to use the clock from link0 through register configuration. The above input pins can be multiplexed as single-ended DC/BT.1120 channel input, which can provide better compatibility with fewer chip pins.

The interface types supported by MIPI Rx are shown in Table 9-7 .

Table 9-7 Interface types supported by MIPI Rx

Interface Type Common mode voltage	Differential mode voltage	Maximum clock frequency	Maximum data rate per lane
D-PHY	200mV	200mV	750MHz	1.5Gbps
sub-LVDS	900mV	150mV	750MHz	1.5Gbps
LVDS	1.25V	350mV	750MHz	1.5Gbps
HiSPi(HiVCM) 900mV		280mV	750MHz	1.5Gbps
HiSPi(SLVS)	200mV	200mV	750MHz	1.5Gbps
CMOS Parallel	1.8V	1.8V	150MHz	150Mbps
CMOS Parallel	3.3V	3.3V	150MHz	150Mbps

MIPI Rx only completes the timing conversion of the interface, and does not process the data format of the image. Any resolution and frame rate can be supported under the premise of satisfying the bandwidth. The bandwidth of MIPI Rx is limited by two parts: the interface data rate of the combo-PHY and the internal processing speed. The maximum interface supports 1.5Gbps/Lane, and the maximum internal processing speed is 600Mpixels/s.

說明

The maximum supported bandwidth on the combo-PHY interface is 1.5Gbps*channels, and the maximum internal processing capacity is 600M*pixel bit width. In practice, the maximum operating rate of MIPI Rx is limited by the minimum of the two.

9.3.3.2 Functional principle

MIPI Interface Data Format

The MIPI specification is developed and maintained by different working groups, covering different application requirements and oriented to applications in different fields. MIPI Rx supports D-PHY and CSI-2 (Camera Serial Interface). D-PHY specifies the physical layer transmission specification, and CSI-2 specifies the format and protocol of the Camera output data packet.

D-PHY

D-PHY is a high-speed physical layer standard released by the MIPI Alliance, which specifies the physical characteristics and transmission protocols of the physical layer of the host and peripherals. D-PHY adopts 200mV source synchronous low-voltage differential signaling technology, and the data rate range of each channel is 80~1500Mbps. D-PHY can work at low power consumption (Low Power, LP) and high speed (High Speed, HS) in two modes.

CSI-2

CSI-2 is a data protocol for cameras, which specifies the packet format for communication between the host and peripherals.

CSI-2 can support image applications with different pixel formats, and the minimum granularity of data transmission is bytes. In order to increase the performance of CSI-2, the number of data channels can be selected. The CSI-2 protocol specifies the mechanism for the sender to pack pixel data into bytes, and specifies the way to allocate and manage multiple data channels. Byte data is organized in packets, which are transferred between SoT and EoT. The receiving end parses the corresponding data packets according to the protocol, and restores the original pixel data.

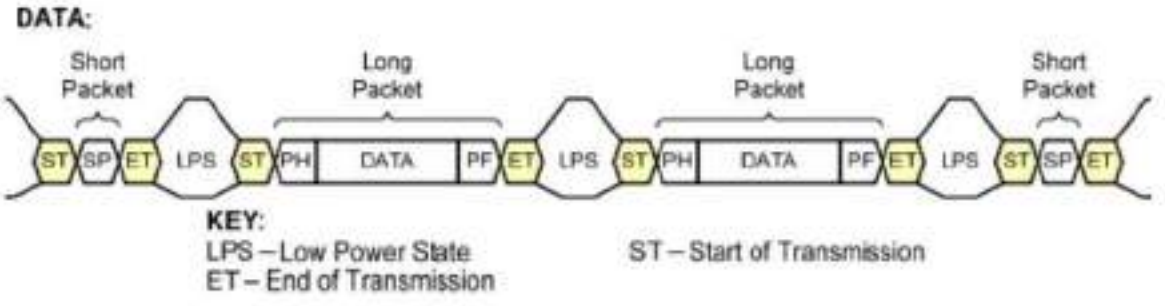
MIPI Rx supports pixel data parsing in RAW8/RAW10/RAW12/RAW14/RAW16 formats.

CSI-2 data packets are divided into two types: long packets and short packets, which contain check codes and can perform error correction and error detection.

Both long and short packets are transmitted between SoT and EoT, and the D-PHY is in LP mode between data transmissions.

The transmission mechanism of CSI-2 data packets is shown in Figure 9-19 . PH and PF represent Packet Header and Packet respectively Footerÿ

Figure 9-19 CSI-2 packet transmission mechanism



The long packet is used to transmit valid pixel data and is divided into five parts: Data ID, Word Count, ECC, PAYLOAD, Checksum.

Data ID includes Virtual Channel and Data Type. Virtual Channel controls the channel used for transmission, and can specify the multiplexing of channels so that different channels can transmit different data. Data Type specifies the type of data.

Word Count indicates the amount of data that the receiver needs to receive.

ECC is an 8-bit error correction code that can correct or detect errors in Data Type and Word Count.

Payload Data is the pixel data that needs to be transmitted.

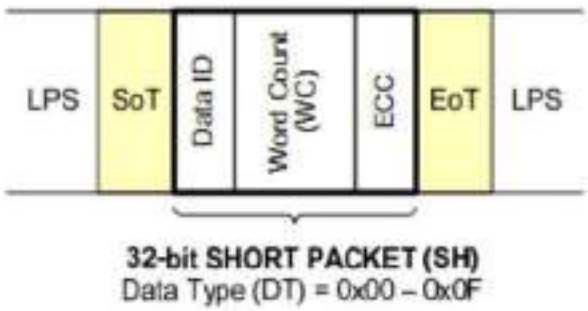
Checksum is a checksum generated by a linear feedback shift register, which is used for Payload data verification.

The structure of the long packet is shown in Figure 9-20 .

Figure 9-20 CSI-2 long packet format

The function of the short packet is to transmit synchronous information, including Data ID, Word Count and ECC. Its format is shown in Figure 9-21 .

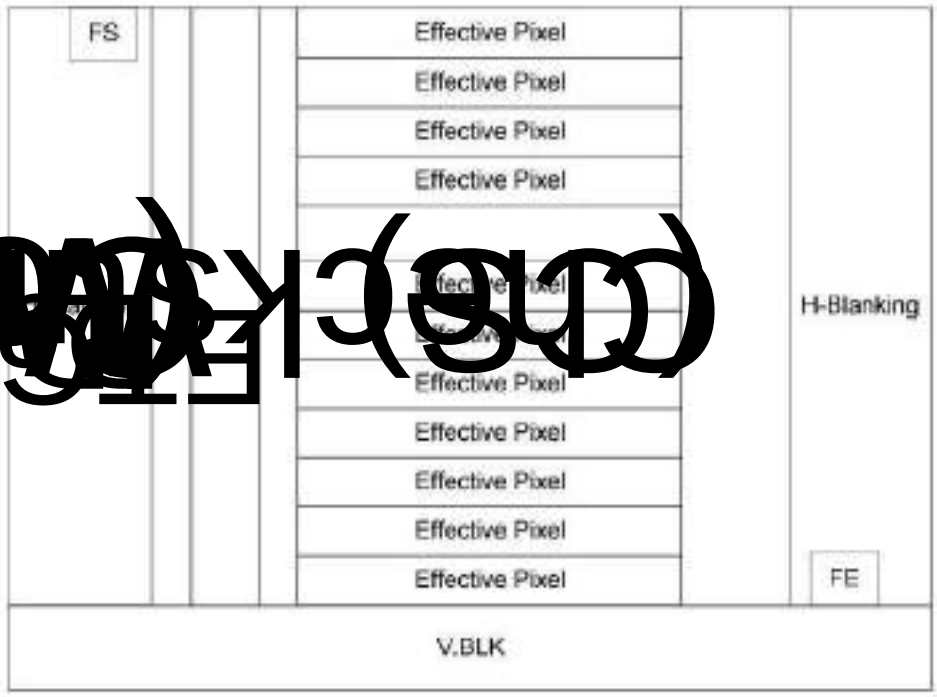
Figure 9-21 CSI-2 short packet format



MIPI Interface Linear Mode

The linear mode video transmission format of the MIPI interface is shown in Figure 9-22 . Frame Start (FS) indicates the start of the frame, and Frame End (FE) indicates the end of the frame. The packet header of each line is 32-bit, which contains information such as the Virtual Channel and Data Type of the current line.

Figure 9-22 MIPI interface image format



MIPI interface wide dynamic mode

MIPI Rx supports 3 wide dynamic (WDR) modes of the MIPI interface, namely:

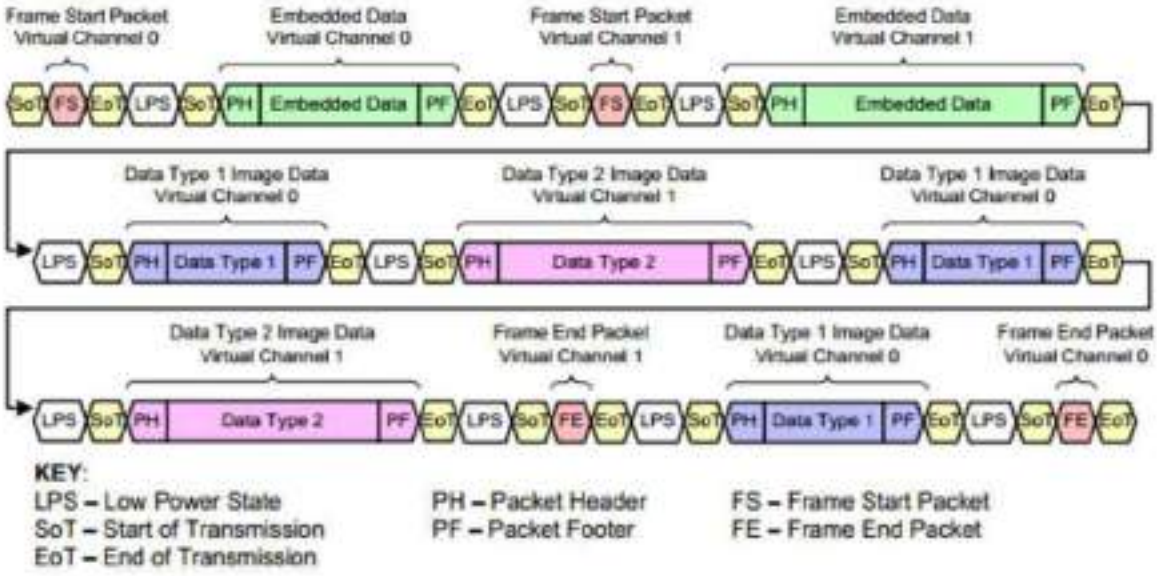
1) MIPI wide dynamic mode 1: use VC (Virtual Channel) to distinguish long/short exposure data.

2) MIPI Wide Dynamic Mode 2: Use DT (Data Type) to distinguish long/short exposure data.

3) MIPI wide dynamic mode 3: DOL wide dynamic transmission format.

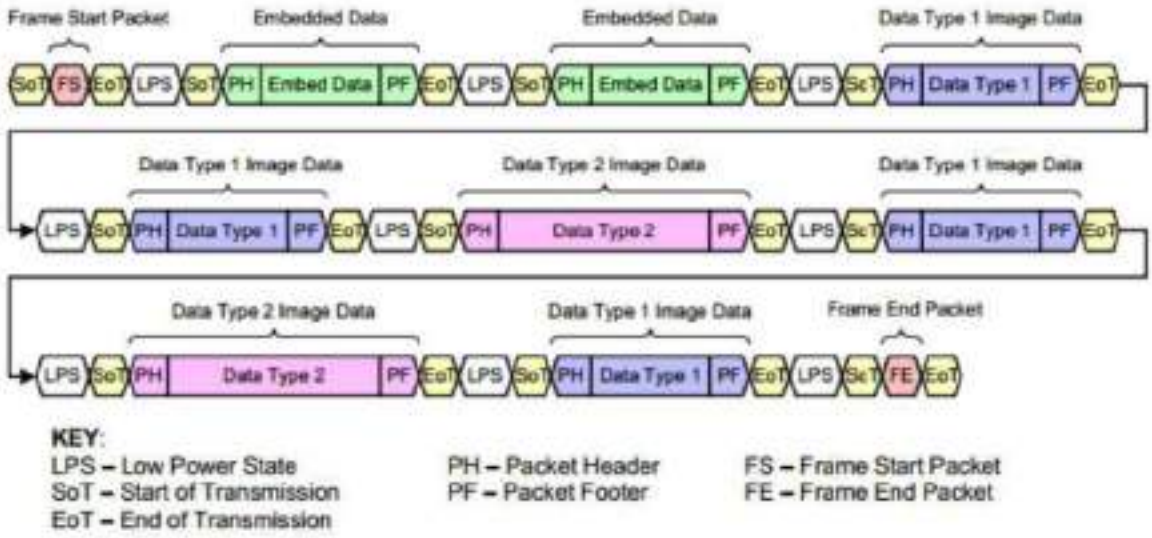
The WDR transmission mode using VC is shown in Figure 9-23 . Both the FS/FE short packet and the long data packet contain VC information. The MIPI Rx controller detects the long/short exposure data according to the VC value in the short packet/long packet, and adds a 2-bit signal mark to each row of data, and outputs it to VICAP with DC timing, and realizes demultiplexing in VICAP .

Figure 9-23 MIPI interface wide dynamic data transmission (using VC)



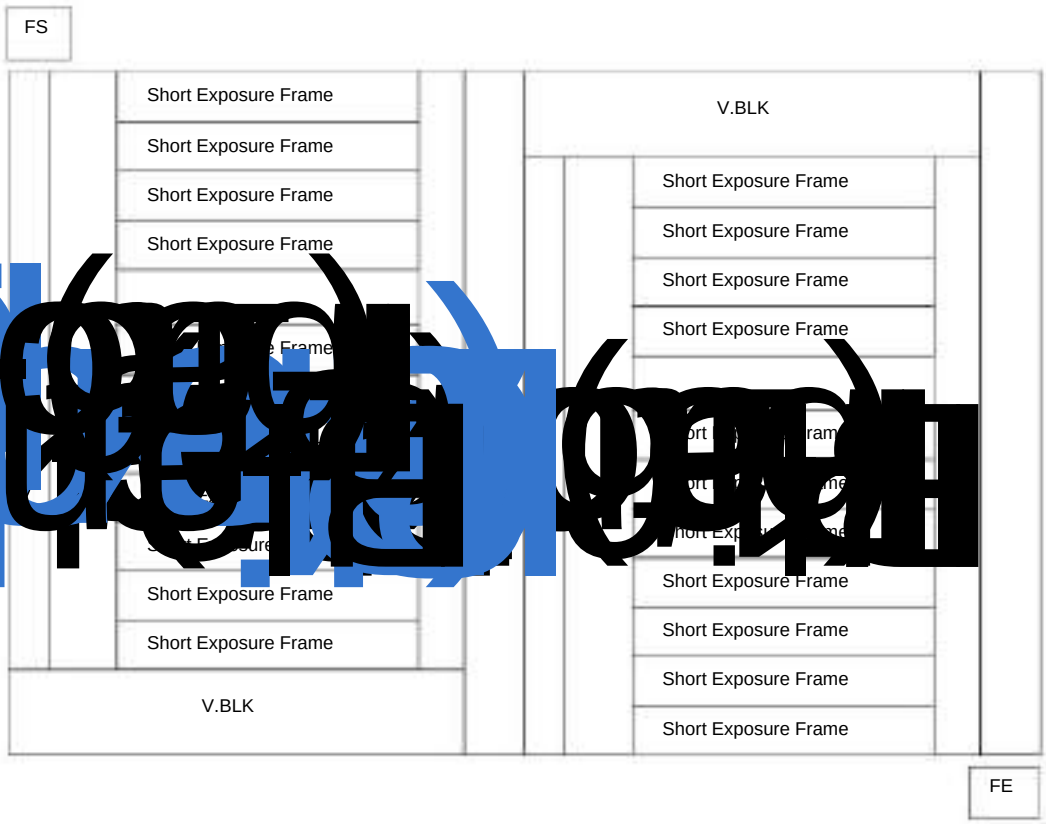
The WDR transmission method using DT is shown in Figure 9-24 . The same frame with different exposure lengths shares a set of FS/FE short packets, and the header of the long packet has DT information. The RAW DATA bit width of DT0 and DT1 can be different. The MIPI Rx controller distinguishes long/short exposure data according to the DT value, and adds a 2-bit signal to each line of data, and outputs it to VICAP with DC timing, and realizes demultiplexing in VICAP.

Figure 9-24 MIPI interface wide dynamic data transmission (using DT)



The MIPI DOL wide dynamic transmission format is shown in Figure 9-25 . Long and short exposure data share a set of FS/FE short packets, and the first 4 pixels of each line are used as Identification Code to distinguish long/short exposure data.

Figure 9-25 MIPI DOL data transmission



说明

The image sensor has two wide dynamic modes, frame interleaved mode and line interleaved mode. The wide dynamic range of the frame mode is the same as that of the linear mode in terms of timing and data format, and the wide dynamic range introduced here is for the line interleaved mode.

LVDS interface data format

Low-voltage differential signal LVDS (Low-Voltage Differential Signal) is commonly used in front-end cameras. The data in the blanking area and the valid area are distinguished by the synchronization code.

说明

LVDS only constrains electrical transmission specifications, and there is no standard agreement on timing and data format. sub-LVDS is a differential signal technology with ultra-low voltage swing. The common mode/differential mode voltage is lower than LVDS, which is more suitable for image sensor applications. Sub LVDS can be regarded as a kind of LVDS, which is collectively referred to as LVDS here.

The combo-PHY of MIPI Rx converts the differential serial data into parallel data, and the MIPI Rx controller splits and splices the parallel data, then extracts the synchronization code and parses out the pixel data.

In LVDS transmission mode, the frame/line synchronization signal is integrated in the data stream, and the special code patterns SOF and EOF in the data stream represent the start and end of the frame respectively, and SOL and EOL represent the start and end of the line respectively. In the data stream, SOF/EOF/SOL/EOL consists of 4 fields, and the bit width of each field is consistent with the pixel data. The first 3 fields are fixed reference codewords, and the frame/ The start or end of the line. The LVDS synchronization code format is shown in Table 9-8 .

Table 9-8 LVDS synchronization code format

Field Bit	Width	Sync code			
		SOL/SAV (Valid line)	EOL/EAV (Valid line)	SOF/SAV (Invalid line)	EOF/EAV (Invalid line)
1st code	8bit	FFh	FFh	FFh	FFh
	10bit	3FFh	3FFh	3FFh	3FFh
	12bit	FFFh	FFFh	FFFh	FFFh
	14bit	3FFFh	3FFFh	3FFFh	3FFFh
	16bit	FFFFh	FFFFh	FFFFh	FFFFh
2nd code	8bit	00h	00h	00h	00h
	10bit	000h	000h	000h	000h
	12bit	000h	000h	000h	000h
	14bit	0000h	0000h	0000h	0000h
	16bit	0000h	0000h	0000h	0000h
3rd code	8bit	00h	00h	00h	00h
	10bit	000h	000h	000h	000h
	12bit	000h	000h	000h	000h
	14bit	0000h	0000h	0000h	0000h
	16bit	0000h	0000h	0000h	0000h
4th code	8bit	20h	20h	20h	20h
	10bit XXXh		XXXh	XXXh	XXXh
	12bit XXXh		XXXh	XXXh	XXXh
	14bit XXXXh		XXXXh	XXXXh	XXXXh
	16bit XXXXh		XXXXh	XXXXh	XXXXh

说明

The first three fields of the synchronization code are fixed, and the fourth field identifies the start or end of the frame/line. The value of the 4th field is determined by the image sensor factory

Determined by the manufacturer, different manufacturers will use different values. Table 9-9 is one of the implementation methods.

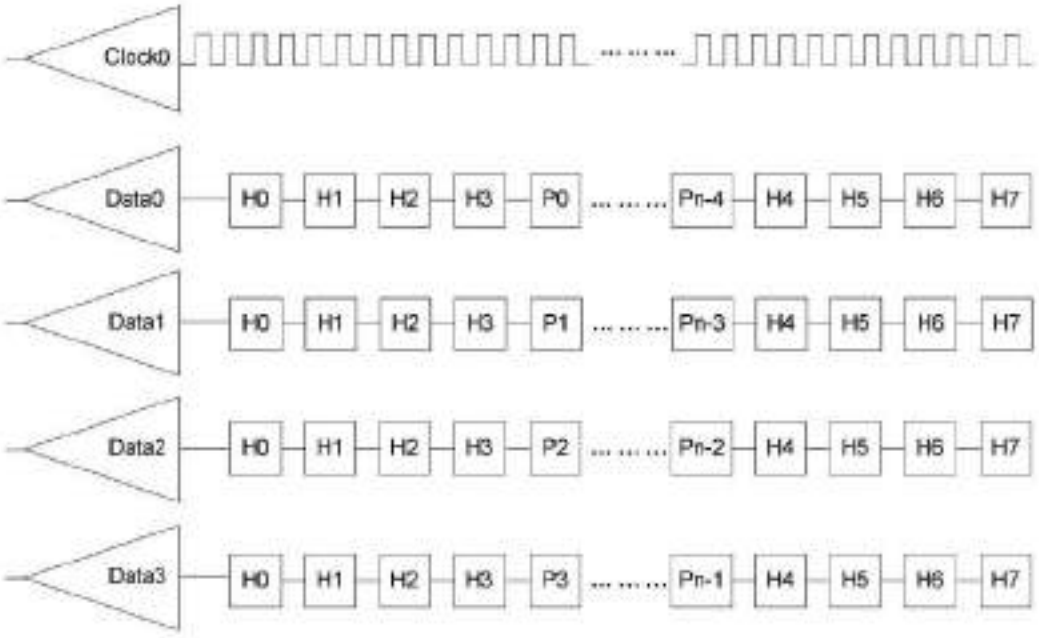
Table 9-9 Example of the fourth field of LVDS synchronization code

Field Bit	Width	Sync code			
		SAV(Valid line)	EAV(Valid line)	SAV(Invalid line)	EAV(Invalid line)

Field Bit	Width	Sync code			
		SAV(Valid line)	EAV(Valid line)	SAV(Invalid line)	EAV(Invalid line)
4th code	8bit	80h	9Dh	ABh	B6h
	10bit	200h	274h	2ACh	2D8h
	12bit	800h	9D0h	AB0h	B60h
	14bit	2000h	2740h	2AC0h	2D80h
	16bit	8000h	9D00h	AB00h	B600h

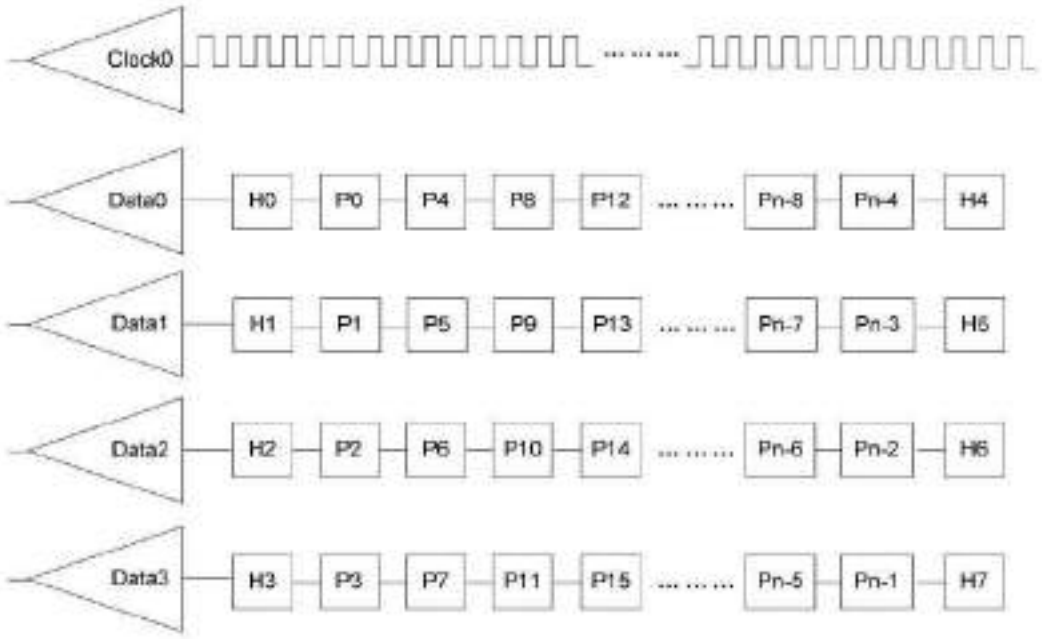
Taking 4 channels as an example, the transmission mode of LVDS synchronization code and pixel data on each channel is shown in Figure 9-26 . In the figure, H represents the synchronization code, P represents the pixel, and the bit width of H and P is the same as that of the image sensor outputting a single pixel. The bit width is the same. Each data channel first transmits a synchronous code with a width of 4 pixels, followed by pixel data, and the distribution of pixel data is related to the number of channels.

Figure 9-26 LVDS synchronization code and image transmission mode 1



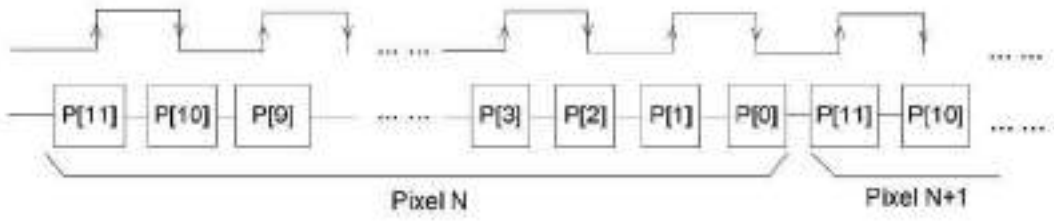
LVDS also has another transmission mode: the transmission in which the synchronization code is assigned to each channel. As shown in Figure 9-27 . H0, H1, H2, and H3 are transmitted simultaneously on four data channels respectively, and the transmission method of pixel data is the same as that in Figure 9-26 .

Figure 9-27 LVDS synchronization code and image transmission mode 2



The transmission of synchronization code and pixel data is serial, and MIPI Rx supports configurable endianness of data. Taking RAW12 and big-endian mode as an example, the timing of the image sensor outputting a single pixel is shown in Figure 9-28 .

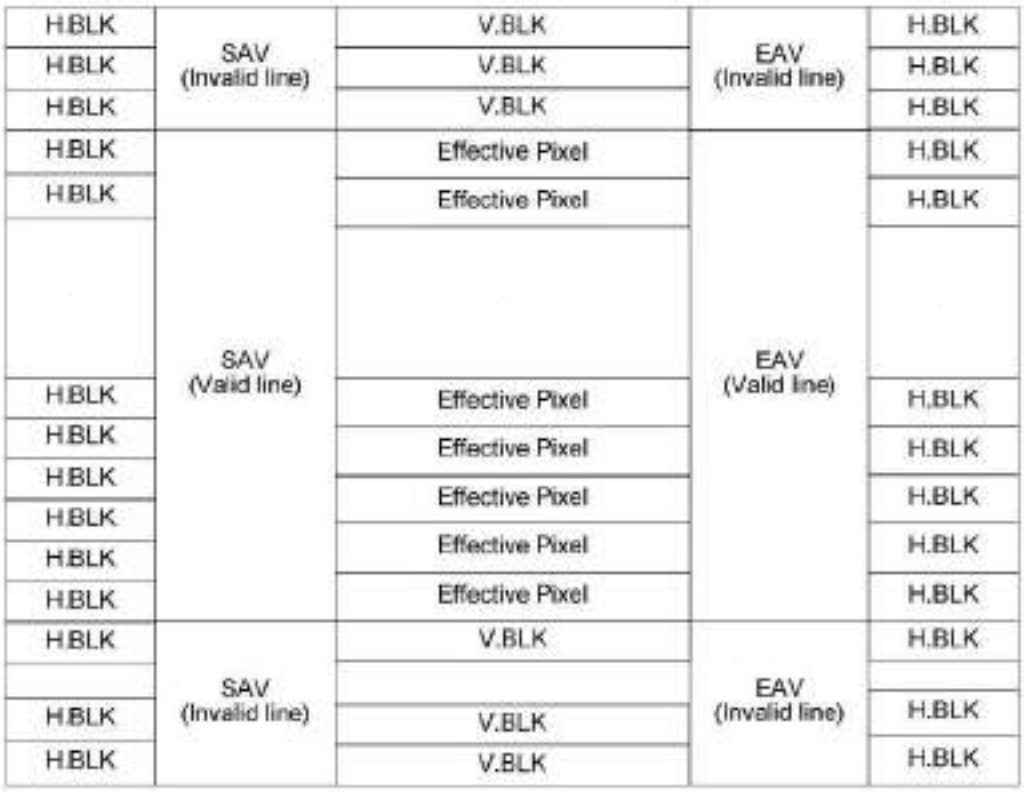
Figure 9-28 LVDS single pixel timing



LVDS Interface Linear Mode

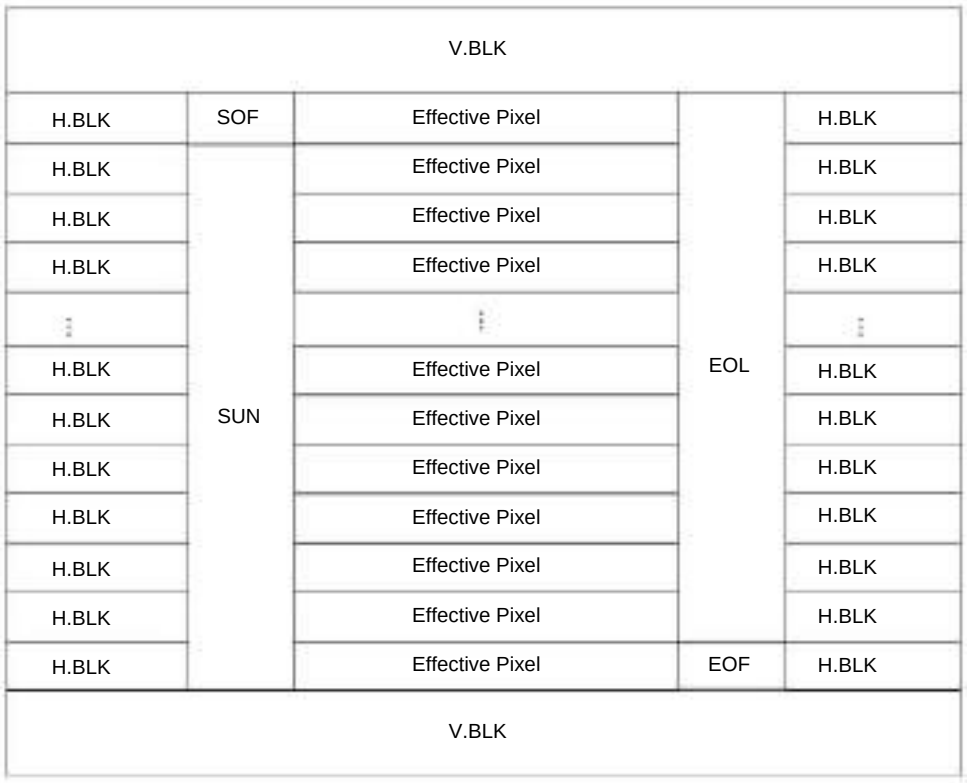
LVDS has two synchronization methods, one of which uses SAV (Invalid) and EAV (Invalid) to identify the invalid data in the blanking area, and uses SAV (Valid) and EAV (Valid) to identify the pixel data in the valid area. This synchronization method is shown in the figure 9-29 .

Figure 9-29 LVDS synchronization mode 1



Another synchronization method uses SOF to mark the start of the first line of the effective area, uses EOF to mark the end of the last line of the effective area, and other effective areas use SOL and EOL as the start and end respectively. This synchronization method is shown in Figure 9-30 shown.

Figure 9-30 LVDS synchronization mode 2



LVDS interface wide dynamic mode

MIPI Rx supports 3 LVDS wide dynamic transmission modes, namely:

1) LVDS wide dynamic mode 1: SOF-EOF logo, long and short exposure frames have independent synchronization codes.

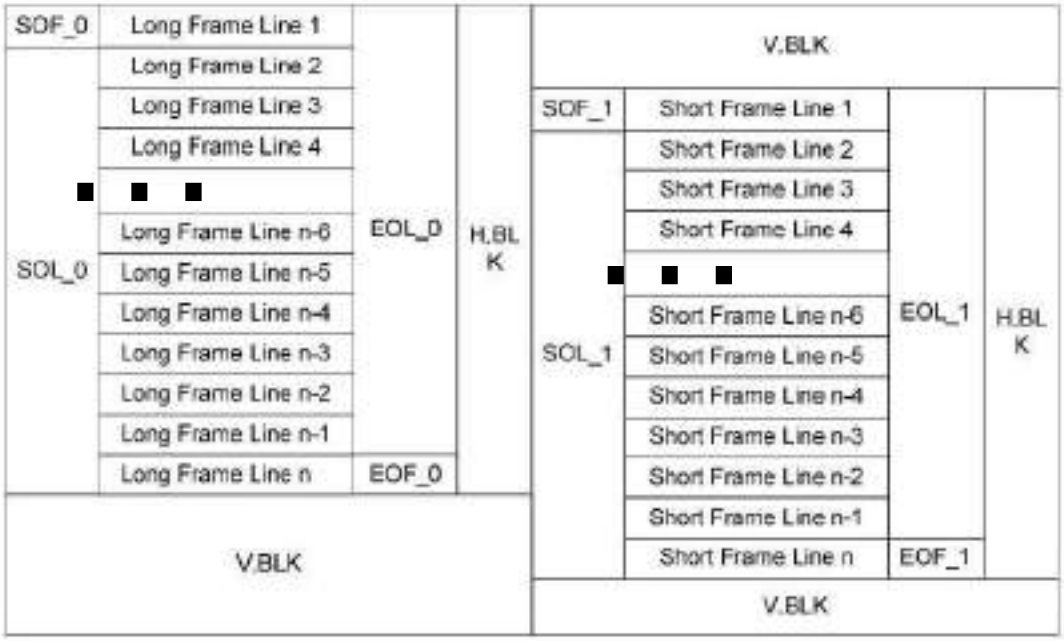
2) LVDS wide dynamic mode 2: SAV-EAV logo, DOL mode, four-field synchronization code, long and short exposure
Frames have independent synchronization codes.

3) LVDS wide dynamic mode 3: SAV-EAV logo, DOL mode, five-field synchronization code, long and short exposure
Frames have independent synchronization codes.

MIPI Rx compares the value of the received synchronization code with the preset value in the register according to different mode configurations, so as to distinguish the received image as long/short exposure and identify it in a specific way. In VICAP Implement demultiplexing within.

LVDS wide dynamic mode 1 is shown in Figure 9-31 . Synchronization codes of long/short exposure video data have different patterns, and the synchronization codes are used to distinguish data of different exposure lengths.

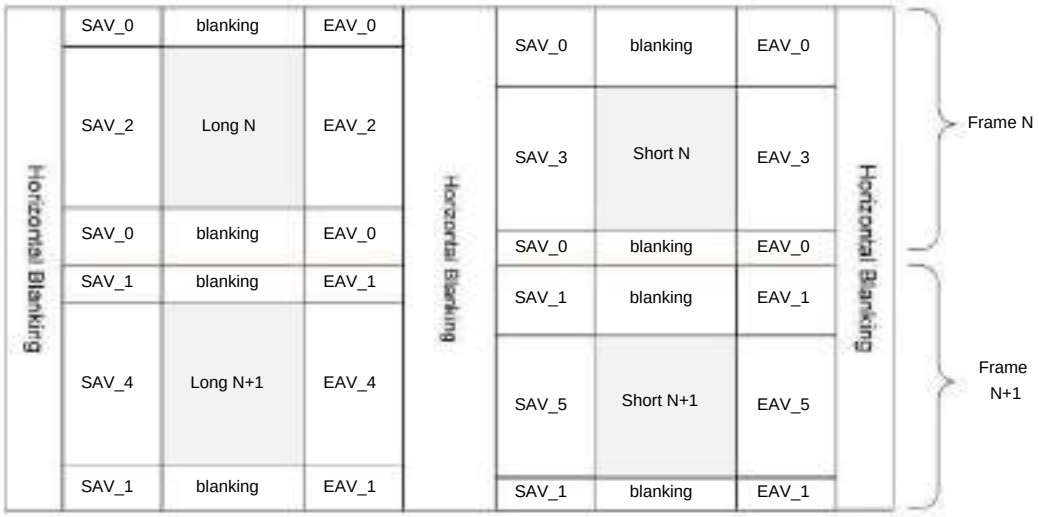
Figure 9-31 LVDS wide dynamic mode 1 (2 frames)



LVDS wide dynamic mode 2 is shown in Figure 9-32 . Using SAV-EAV as the synchronization method, long and short exposures have independent synchronization codes, and the synchronization codes of the Nth frame and the N+1th frame are also different.

LVDS wide dynamic mode 3 is basically the same as mode 2, the only difference is that the synchronization code of mode 3 is 5 fields.

Figure 9-32 LVDS wide dynamic mode 2 (2 frames)



HiSPi interface data format

The High-Speed Serial Pixel (HiSPi) protocol consists of two parts: the HiSPi physical layer protocol and the HiSPi specification.

The electrical characteristics and timing parameters are specified in the HiSPi physical layer protocol, and the data packaging method is specified in the HiSPi specification.

The HiSPi specification contains two physical layer electrical standards and four different data transmission methods. The electrical standards are: HiVCM and SLVS; the data transmission methods are: Packetized-SP, Streaming-SP, Streaming-S and ActiveStart-SP8ÿ

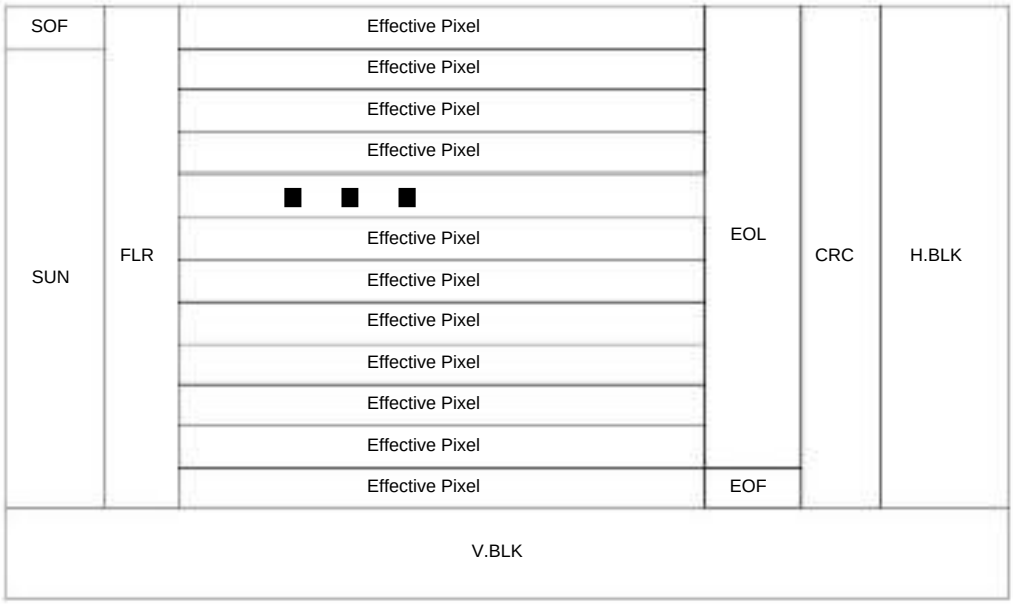
MIPI Rx supports both HiVCM and SLVS electrical standards, and supports Packetized-SP and Streaming-SP data transmission methods.

HiSPi interface linear mode

In Packetized-SP mode, the image sensor uses SOF to mark the start of the first line of the effective area of the image, uses EOF to mark the end of the last line of the effective area, and other effective areas use SOL and EOL as the start and end respectively. This synchronization method is similar to Figure 9-30 , the difference is that CRC and FLR can be added to the packet in Packetized-SP mode. Its data format is shown in Figure 9-33 .

MIPI Rx can check whether the pairing of SOF-EOF and SOL-EOL is normal, but it does not process CRC and FLR data.

Figure 9-33 HiSPi Packetized-SP data format



The transmission methods of the other three modes of HiSPi (Streaming-SP, Streaming-S, ActiveStart-SP8) are similar to Packetized-SP, the difference lies in the calibration method of the synchronization code. The differences between them are shown in Table 9-10 . Among them, SOF and EOF represent the frame start and frame end of the image effective area respectively; SOL and EOL represent the line start and line end of the image effective area respectively; SAV represents the line start of the image blanking area.

Table 9-10 HiSPi transmission mode

sync code	Packetized-SP	Streaming-SP	Streaming-S	ActiveStart SP8
SOF	Required	Required	Unsupported	Required
SUN	Required	Required	Required	Required

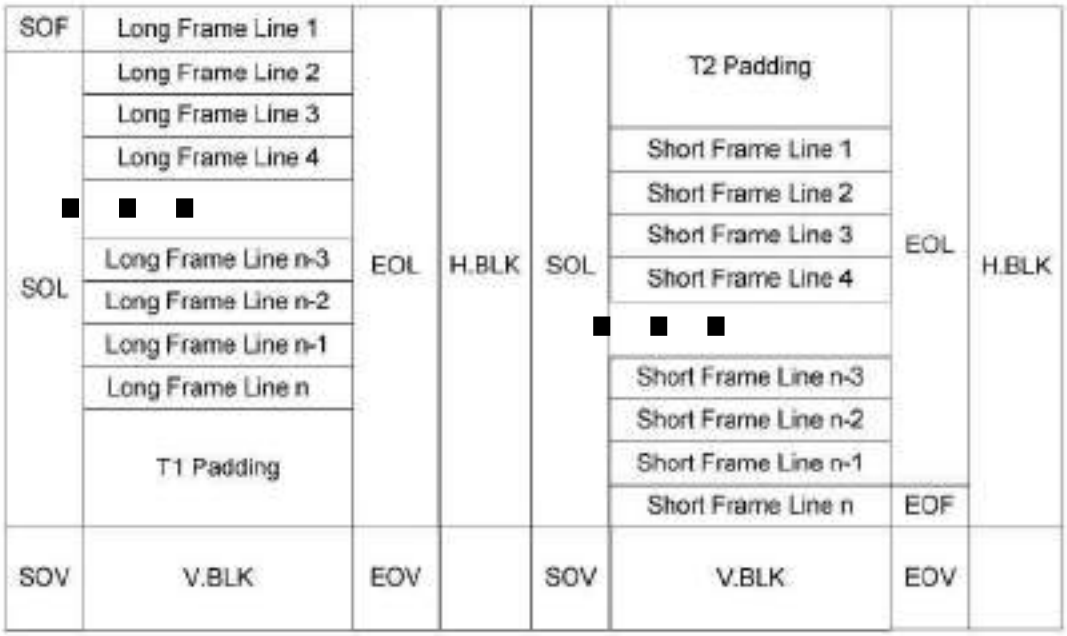
sync code	Packetized-SP Streaming	-SP Streaming-S		ActiveStart SP8
EOF	Required	Unsupported	Unsupported	Unsupported
EOL	Required	Unsupported	Unsupported	Unsupported
SAV	Unsupported	Required	Required	Unsupported

MIPI Rx can support the above 4 modes, and at the same time support all channels to transmit 4-field sync codes or assign sync codes to each channel for transmission (as shown in Figure 9-26 and Figure 9-27).

HiSPi interface wide dynamic mode

The synchronous code of the wide dynamic mode of the HiSPi interface is the same as that of the linear mode, and there is a blanking area between the long exposure and short exposure data. The first few lines of the short exposure are not valid pixel areas, but are filled with fixed values. The timing of the wide dynamic mode of the HiSPi interface is shown.

Figure 9-34 HiSPi wide dynamic mode



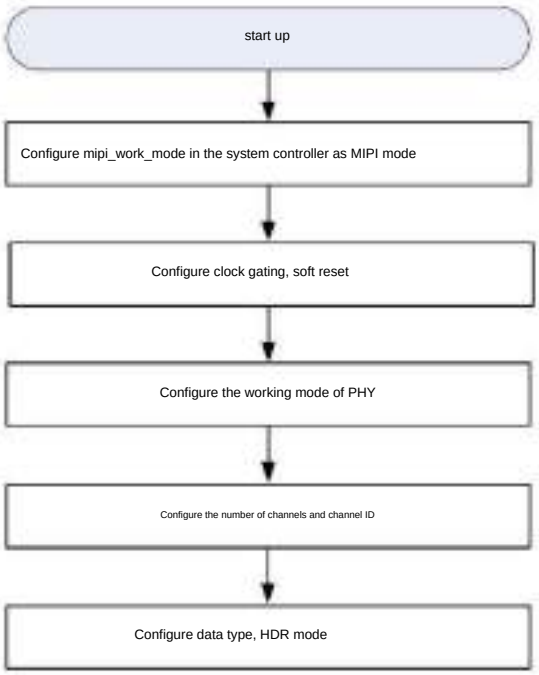
9.3.4 MIPI Rx controller working mode

The MIPI Rx controller supports MIPI, LVDS and HiSPi modes, and the software configuration in each mode consists of two parts: controller and combo-PHY.

9.3.4.1 MIPI mode configuration process

In MIPI mode, you need to configure the PHY working mode, the number of channels used for data transmission, data type and wide dynamic mode. The frame/line synchronization information of MIPI mode is included in the data packet, and the controller completes the analysis of the data packet to restore the pixel data. The MIPI mode software operation flow is shown in Figure 9-35 .

Figure 9-35 MIPI Rx MIPI mode software configuration process

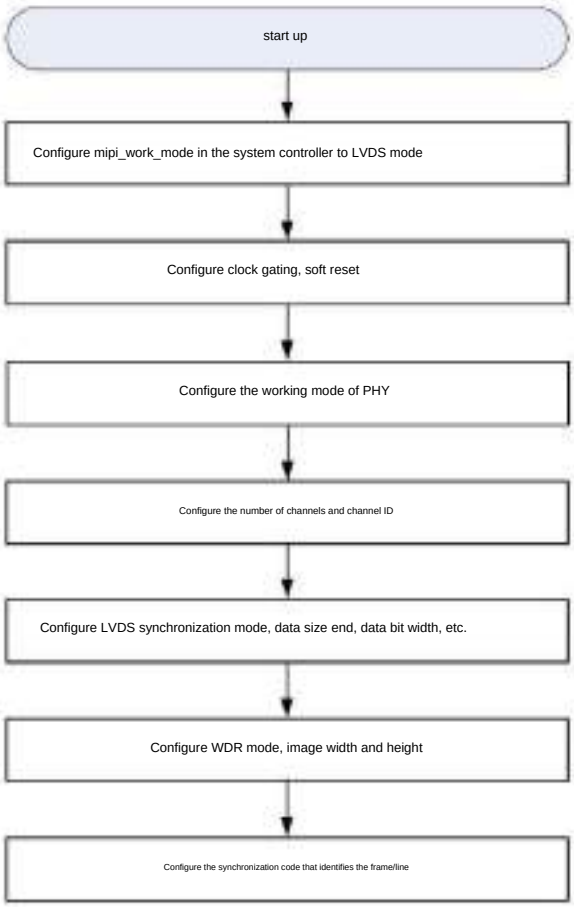


9.3.4.2 LVDS and HiSPi mode configuration process

In LVDS/HiSPi mode, registers such as RAW DATA type, data size end, synchronization mode, WDR type, and image width and height need to be configured. The LVDS mode relies on the synchronization code to identify the frame/row synchronization information. According to the different types of RAW DATA, the synchronization code can be 8/10/12/14/16-bit.

The operating flow of LVDS and HiSPi mode software is shown in Figure 9-36 .

Figure 9-36 MIPI Rx LVDS and HiSPi mode software configuration process



9.3.5 MIPI Rx Register Overview

An overview of the MIPI Rx registers is shown in Table 9-11 .

Table 9-11 MIPI register overview (base address is 0x1130_0000)

offset address	name	describe	page number
0x0000	PHY_MODE_LINK0	Link0 PHY working mode register	9-199
0x0004	PHY_SKEW_LINK0	Link0 PHY channel delay adjustment register	9-200
0x0008	PHY_EN_LINK0	Link0 PHY Channel Enable Register	9-201
0x0018	PHY_DATA_LINK0	Link0 PHY output parallel data register 9-202	
0x001C	PHY_PH_MIPI_LIN K0	Link0 MIPI Packet Header Register	9-203
0x0020	PHY_DATA_MIPI_ LINK0	Link0 MIPI Mode Data Register	9-203

offset address	name	describe	page number
0x0024	PHY_SYNC_DCT_LINK0	Link0 PHY LVDS mode sync header detection control register	9-204
0x0030	PHY_SYNC_CODE0_LINK0	Link0 PHY LVDS Mode Sync Header Register 0	9-205
0x0034	PHY_SYNC_CODE1_LINK0	Link0 PHY LVDS Mode Sync Header Register 1	9-205
0x0038	PHY_SYNC_CODE2_LINK0	Link0 PHY LVDS Mode Sync Header Register 2	9-206
0x003C	PHY_SYNC_CODE3_LINK0	Link0 PHY LVDS Mode Sync Header Register 3	9-206
0x01F0	MIPI_CIL_INT_RAW_LINK0	Link0 MIPI CIL Raw Interrupt Status Register 9-207	
0x01F4	MIPI_CIL_INT_LINK0	Link0 MIPI CIL Interrupt Status Register	9-208
0x01F8	MIPI_CIL_INT_MSK_LINK0	Link0 MIPI CIL interrupt mask register	9-209
0x0200	PHY_MODE_LINK1	Link1 PHY working mode register	9-211
0x0204	PHY_SKEW_LINK1	Link1 PHY lane delay adjustment register	9-212
0x0208	PHY_EN_LINK1	Link1 PHY Channel Enable Register	9-213
0x0218	PHY_DATA_LINK1	Parallel Data Register 9-214 for Link1 PHY output	
0x021C	PHY_PH_MIPI_LINK1	Link1 MIPI Packet Header Register	9-215
0x0220	PHY_DATA_MIPI_LINK1	Link1 MIPI Mode Data Register	9-215
0x0224	PHY_SYNC_DCT_LINK1	Link1 PHY LVDS mode sync header detection control register	9-216
0x0230	PHY_SYNC_CODE0_LINK1	Link1 PHY LVDS Mode Sync Header Register 0	9-217
0x0234	PHY_SYNC_CODE1_LINK1	Link1 PHY LVDS Mode Sync Header Register 1	9-217
0x0238	PHY_SYNC_CODE2_LINK1	Link1 PHY LVDS Mode Sync Header Register 2	9-218
0x023C	PHY_SYNC_CODE3_LINK1	Link1 PHY LVDS Mode Sync Header Register 3	9-218
0x03F0	MIPI_CIL_INT_RAW_LINK1	Link1 MIPI CIL Raw Interrupt Status Register 9-219	

offset address	name	describe	page number
0x03F4	MIPI_CIL_INT_LIN K1	Link1 MIPI CIL Interrupt Status Register	9-220
0x03F8	MIPI_CIL_INT_MS K_LINK1	Link1 MIPI CIL Interrupt Mask Register	9-222
0x0400	PHY_MODE_LINK2	Link2 PHY working mode register	9-223
0x0404	PHY_SKEW_LINK2	Link2 PHY channel delay adjustment register	9-225
0x0408	PHY_EN_LINK2	Link2 PHY Channel Enable Register	9-226
0x0418	PHY_DATA_LINK2	Link2 PHY Output Parallel Data Register 9-227	
0x041C	PHY_PH_MIPI_LIN K2	Link2 MIPI Packet Header Register	9-227
0x0420	PHY_DATA_MIPI_ LINK2	Link2 MIPI Mode Data Register	9-228
0x0424	PHY_SYNC_DCT_L INK2	Link2 PHY LVDS Mode Sync Header Detection Control Register	9-228
0x0430	PHY_SYNC_CODE0 _LINK2	Link2 PHY LVDS Mode Sync Header Register 0	9-229
0x0434	PHY_SYNC_CODE1 _LINK2	Link2 PHY LVDS Mode Sync Header Register 1	9-230
0x0438	PHY_SYNC_CODE2 _LINK2	Link2 PHY LVDS Mode Sync Header Register 2	9-230
0x043C	PHY_SYNC_CODE3 _LINK2	Link2 PHY LVDS Mode Sync Header Register 3	9-231
0x05F0	MIPI_CIL_INT_RA W_LINK2	Link2 MIPI CIL Raw Interrupt Status Register 9-231	
0x05F4	MIPI_CIL_INT_LIN K2	Link2 MIPI CIL Interrupt Status Register	9-232
0x05F8	MIPI_CIL_INT_MS K_LINK2	Link2 MIPI CIL Interrupt Mask Register	9-234
0x0800	PHY_CHN_CTRL	PHY channel control selection register	9-235
0x0804	PHY_LP_SELECT	PHY1 LP Mode Signal Select Register	9-236
0x080C	MIPI_MEM_CTRL	MEMORY control register	9-237
0x0810	LANE_EN	LANE_EN enable register	9-238
0x0814	MIPI_PHYCFG_MO OF	MIPI PHY Configuration Mode Register	9-239
0x0818	MIPI_PHYCFG_EN	MIPI PHY configuration enable register	9-240

offset address name		describe	page number
0x081C	MIPI_CIL_CTRL	MIPI CIL Control Register	9-240
0x0820	MIPI_SRST_CFG	MIPI CORE Soft Reset Register	9-241
0x0EF0	MIPI_CHN0_INT_RAw	MIPI Lane 0 Raw Interrupt Status Register	9-242
0x0EF4	MIPI_CHN0_INT	MIPI Lane 0 Interrupt Status Register	9-243
0x0EF8	MIPI_CHN0_INT_MSK	MIPI Lane 0 Interrupt Mask Register	9-244
0x1004	MIPI0_LANES_NUM	MIPI0 data lane number enable register	9-246
0x100C	MIPI0_MAIN_INT_ST	MIPI0 Total Interrupt Status Register	9-246
0x1010	MIPI0_DI_1	MIPI0 Controller Data ID 1 Register	9-247
0x1014	MIPI0_DI_2	MIPI0 Controller Data ID 2 Register	9-249
0x1060	MIPI0_PKT_INTR_ST	MIPI0 Packet Interrupt Status Register	9-250
0x1064	MIPI0_PKT_INTR_CEC	MIPI0 Packet Interrupt Mask Register	9-251
0x1070	MIPI0_PKT_INTR2_ST	MIPI0 Packet Interrupt Status Register 2	9-252
0x1074	MIPI0_PKT_INTR2_CEC	MIPI0 Packet Interrupt Mask Register 2	9-253
0x1080	MIPI0_FRAME_INTR_ST	MIPI0 Frame Interrupt Status Register	9-255
0x1084	MIPI0_FRAME_INTR_MSK	MIPI0 frame interrupt mask register	9-257
0x1090	MIPI0_LINE_INTR_ST	MIPI0 Line Interrupt Status Register	9-258
0x1094	MIPI0_LINE_INTR_CEC	MIPI0 Line Interrupt Mask Register	9-260
0x1100	MIPI0_USERDEF_DT	The pixel bit width configuration register corresponding to MIPI0 user-defined data type	9-262
0x1104	MIPI0_USER_DEF	MIPI0 user-defined data type type enable configuration register	9-264
0x1108	MIPI0_CTRL_MODE_HS	MIPI0 operating mode enable register	9-265
0x1200	MIPI0_DOL_ID_CODE0	MIPI0 DOL mode frame identification register 0	9-265

offset address name		describe	page number
0x1204	MIPI0_DOL_ID_CODE1	MIPI0 DOL mode frame identification register 1	9-266
0x1208	MIPI0_DOL_ID_CODE2	MIPI0 DOL mode frame identification register 2	9-266
0x1230	MIPI0_CTRL_MODE_PIXEL	MIPI0 Output Operation Mode Enable Register	9-267
0x1240	MIPI0_DUMMY_PIX_REG	MIPI0 dummy row pixel value register	9-268
0x1250	MIPI0_IMGSIZE0_S of the father	MIPI0 VC0 transmitted image width and height register 9-268	
0x1254	MIPI0_IMGSIZE1_S of the father	Image width and height registers transmitted by MIPI0 VC1 9-268	
0x1258	MIPI0_IMGSIZE2_S of the father	MIPI0 VC2 transmitted image width and height register 9-269	
0x125C	MIPI0_IMGSIZE3_S of the father	Image Width and Height Register 9-269 transmitted by MIPI0 VC3	
0x12F0	MIPI0_CTRL_INT_RAW	MIPI0 Read Data Error Raw Interrupt Status Register 9-270	
0x12F4	MIPI0_CTRL_INT MIPI0 Read Data Error Interrupt Status Register 9-271		
0x12F8	MIPI0_CTRL_INT_CEC	MIPI0 Read Data Error Interrupt Mask Register 9-272	
0x1300 LVDS0_WDR		LVDS WDR Control Register	9-273
0x130C LVDS0_IMGSIZE LVDS image width and height register			9-274
0x1310	LVDS0_CTRL	LVDS Control Register	9-274
0x1314	LVDS0_CROP_START	LVDS clipping register	9-275
0x1320	LVDS0_LANE0_SOF_01	In LVDS/HiSPi mode, lane0 frame start synchronization code configuration register	9-276
0x1324	LVDS0_LANE0_SOF_23	In LVDS/HiSPi mode, lane0 frame start synchronization code configuration register	9-276
0x1328	LVDS0_LANE0_EOF_01	In LVDS/HiSPi mode, lane0 frame end synchronization code configuration register	9-277
0x132C LVDS0_LANE0_EOF_23		In LVDS/HiSPi mode, lane0 frame end synchronization code configuration register	9-277
0x1330	LVDS0_LANE0_SOL_01	In LVDS/HiSPi mode, lane0 line start synchronization code configuration register	9-278

offset address name		describe	page number
0x1334	LVDS0_LANE0_SOL_23	In LVDS/HiSPi mode, lane0 line start synchronization code configuration register	9-278
0x1338	LVDS0_LANE0_EOL_01	In LVDS/HiSPi mode, lane0 end-of-line synchronization code configuration register	9-279
0x133C	LVDS0_LANE0_EOL_23	In LVDS/HiSPi mode, lane0 end-of-line synchronization code configuration register	9-279
0x1340	LVDS0_LANE1_SOF_01	In LVDS/HiSPi mode, lane1 frame start synchronization code configuration register	9-280
0x1344	LVDS0_LANE1_SOF_23	In LVDS/HiSPi mode, lane1 frame start synchronization code configuration register	9-280
0x1348	LVDS0_LANE1_EOF_01	In LVDS/HiSPi mode, lane1 frame end synchronization code configuration register	9-281
0x134C	LVDS0_LANE1_EOF_23	In LVDS/HiSPi mode, lane1 frame end synchronization code configuration register	9-281
0x1350	LVDS0_LANE1_SOL_01	In LVDS/HiSPi mode, lane1 line start synchronization code configuration register	9-282
0x1354	LVDS0_LANE1_SOL_23	In LVDS/HiSPi mode, lane1 line start synchronization code configuration register	9-282
0x1358	LVDS0_LANE1_EOL_01	In LVDS/HiSPi mode, lane1 end-of-line synchronization code configuration register	9-283
0x135C	LVDS0_LANE1_EOL_23	In LVDS/HiSPi mode, lane1 end-of-line synchronization code configuration register	9-283
0x1360	LVDS0_LANE2_SOF_01	In LVDS/HiSPi mode, lane2 frame start synchronization code configuration register	9-284
0x1364	LVDS0_LANE2_SOF_23	In LVDS/HiSPi mode, lane2 frame start synchronization code configuration register	9-284
0x1368	LVDS0_LANE2_EOF_01	In LVDS/HiSPi mode, lane2 frame end synchronization code configuration register	9-285
0x136C	LVDS0_LANE2_EOF_23	In LVDS/HiSPi mode, lane2 frame end synchronization code configuration register	9-285
0x1370	LVDS0_LANE2_SOL_01	In LVDS/HiSPi mode, lane2 line start synchronization code configuration register	9-286
0x1374	LVDS0_LANE2_SOL_23	In LVDS/HiSPi mode, lane2 line start synchronization code configuration register	9-286
0x1378	LVDS0_LANE2_EOL_01	In LVDS/HiSPi mode, lane2 end-of-line synchronization code configuration register	9-287

offset address name	describe	page number
0x137C LVDS0_LANE2_EO L_23	In LVDS/HiSPi mode, lane2 end-of-line synchronization code configuration register	9-287
0x1380 LVDS0_LANE3_SO F_01	In LVDS/HiSPi mode, lane3 frame start synchronization code configuration register	9-288
0x1384 LVDS0_LANE3_SO F_23	In LVDS/HiSPi mode, lane3 frame start synchronization code configuration register	9-288
0x1388 LVDS0_LANE3_EO F_01	In LVDS/HiSPi mode, lane3 frame end synchronization code configuration register	9-289
0x138C LVDS0_LANE3_EO F_23	In LVDS/HiSPi mode, lane3 frame end synchronization code configuration register	9-289
0x1390 LVDS0_LANE3_SO L_01	In LVDS/HiSPi mode, lane3 line start synchronization code configuration register	9-290
0x1394 LVDS0_LANE3_SO L_23	In LVDS/HiSPi mode, lane3 line start synchronization code configuration register	9-290
0x1398 LVDS0_LANE3_EO L_01	In LVDS/HiSPi mode, lane3 end-of-line synchronization code configuration register	9-291
0x139C LVDS0_LANE3_EO L_23	In LVDS/HiSPi mode, lane3 end-of-line synchronization code configuration register	9-291
0x13A0 LVDS0_LANE4_SO F_01	In LVDS/HiSPi mode, lane4 frame start synchronization code configuration register	9-292
0x13A4 LVDS0_LANE4_SO F_23	In LVDS/HiSPi mode, lane4 frame start synchronization code configuration register	9-292
0x13A8 LVDS0_LANE4_EO F_01	In LVDS/HiSPi mode, lane4 frame end synchronization code configuration register	9-293
0x13AC LVDS0_LANE4_EO F_23	In LVDS/HiSPi mode, lane4 frame end synchronization code configuration register	9-293
0x13B0 LVDS0_LANE4_SO L_01	In LVDS/HiSPi mode, lane4 line start synchronization code configuration register	9-294
0x13B4 LVDS0_LANE4_SO L_23	In LVDS/HiSPi mode, lane4 line start synchronization code configuration register	9-294
0x13B8 LVDS0_LANE4_EO L_01	In LVDS/HiSPi mode, lane4 end-of-line synchronization code configuration register	9-295
0x13BC LVDS0_LANE4_EO L_23	In LVDS/HiSPi mode, lane4 end-of-line synchronization code configuration register	9-295
0x13C0 LVDS0_LANE5_SO F_01	In LVDS/HiSPi mode, lane5 frame start synchronization code configuration register	9-296

offset address name	describe	page number
0x13C4 LVDS0_LANE5_SOF_23	In LVDS/HiSPi mode, lane5 frame start synchronization code configuration register	9-296
0x13C8 LVDS0_LANE5_EOF_01	In LVDS/HiSPi mode, lane5 frame end synchronization code configuration register	9-297
0x13CC LVDS0_LANE5_EOF_23	In LVDS/HiSPi mode, lane5 frame end synchronization code configuration register	9-297
0x13D0 LVDS0_LANE5_SOL_01	In LVDS/HiSPi mode, lane5 line start synchronization code configuration register	9-298
0x13D4 LVDS0_LANE5_SOL_23	In LVDS/HiSPi mode, lane5 line start synchronization code configuration register	9-298
0x13D8 LVDS0_LANE5_EOL_01	In LVDS/HiSPi mode, lane5 end-of-line synchronization code configuration register	9-299
0x13DC LVDS0_LANE5_EOL_23	In LVDS/HiSPi mode, lane5 end-of-line synchronization code configuration register	9-299
0x13E0 LVDS0_LANE6_SOF_01	In LVDS/HiSPi mode, lane6 frame start synchronization code configuration register	9-300
0x13E4 LVDS0_LANE6_SOF_23	In LVDS/HiSPi mode, lane6 frame start synchronization code configuration register	9-300
0x13E8 LVDS0_LANE6_EOF_01	In LVDS/HiSPi mode, lane6 frame end synchronization code configuration register	9-301
0x13EC LVDS0_LANE6_EOF_23	In LVDS/HiSPi mode, lane6 frame end synchronization code configuration register	9-301
0x13F0 LVDS0_LANE6_SOL_01	In LVDS/HiSPi mode, lane6 line start synchronization code configuration register	9-302
0x13F4 LVDS0_LANE6_SOL_23	In LVDS/HiSPi mode, lane6 line start synchronization code configuration register	9-302
0x13F8 LVDS0_LANE6_EOL_01	In LVDS/HiSPi mode, lane6 end-of-line synchronization code configuration register	9-303
0x13FC LVDS0_LANE6_EOL_23	In LVDS/HiSPi mode, lane6 end-of-line synchronization code configuration register	9-303
0x1400 LVDS0_LANE7_SOF_01	In LVDS/HiSPi mode, lane7 frame start synchronization code configuration register	9-304
0x1404 LVDS0_LANE7_SOF_23	In LVDS/HiSPi mode, lane7 frame start synchronization code configuration register	9-304
0x1408 LVDS0_LANE7_EOF_01	In LVDS/HiSPi mode, lane7 frame end synchronization code configuration register	9-305

offset address name	describe	page number
0x140C LVDS0_LANE7_EOF_23	In LVDS/HiSPi mode, lane7 frame end synchronization code configuration register	9-305
0x1410 LVDS0_LANE7_SOL_01	In LVDS/HiSPi mode, lane7 line start synchronization code configuration register	9-306
0x1414 LVDS0_LANE7_SOL_23	In LVDS/HiSPi mode, lane7 line start synchronization code configuration register	9-306
0x1418 LVDS0_LANE7_EOL_01	In LVDS/HiSPi mode, lane7 end-of-line synchronization code configuration register	9-307
0x141C LVDS0_LANE7_EOL_23	In LVDS/HiSPi mode, lane7 end-of-line synchronization code configuration register	9-307
0x1420 LVDS0_LANE8_SOF_01	In LVDS/HiSPi mode, lane8 frame start synchronization code configuration register	9-308
0x1424 LVDS0_LANE8_SOF_23	In LVDS/HiSPi mode, lane8 frame start synchronization code configuration register	9-308
0x1428 LVDS0_LANE8_EOF_01	In LVDS/HiSPi mode, lane8 end-of-frame synchronization code configuration register	9-309
0x142C LVDS0_LANE8_EOF_23	In LVDS/HiSPi mode, lane8 end-of-frame synchronization code configuration register	9-309
0x1430 LVDS0_LANE8_SOL_01	In LVDS/HiSPi mode, lane8 line start synchronization code configuration register	9-310
0x1434 LVDS0_LANE8_SOL_23	In LVDS/HiSPi mode, lane8 line start synchronization code configuration register	9-310
0x1438 LVDS0_LANE8_EOL_01	In LVDS/HiSPi mode, lane8 end-of-line synchronization code configuration register	9-311
0x143C LVDS0_LANE8_EOL_23	In LVDS/HiSPi mode, lane8 end-of-line synchronization code configuration register	9-311
0x1440 LVDS0_LANE9_SOF_01	In LVDS/HiSPi mode, lane9 frame start synchronization code configuration register	9-312
0x1444 LVDS0_LANE9_SOF_23	In LVDS/HiSPi mode, lane9 frame start synchronization code configuration register	9-312
0x1448 LVDS0_LANE9_EOF_01	In LVDS/HiSPi mode, lane9 frame end synchronization code configuration register	9-313
0x144C LVDS0_LANE9_EOF_23	In LVDS/HiSPi mode, lane9 frame end synchronization code configuration register	9-313
0x1450 LVDS0_LANE9_SOL_01	In LVDS/HiSPi mode, lane9 line start synchronization code configuration register	9-314

offset address name		describe	page number
0x1454	LVDS0_LANE9_SOL_23	In LVDS/HiSPi mode, lane9 line start synchronization code configuration register	9-314
0x1458	LVDS0_LANE9_EOL_01	In LVDS/HiSPi mode, lane9 end-of-line synchronization code configuration register	9-315
0x145C	LVDS0_LANE9_EOL_23	In LVDS/HiSPi mode, lane9 end-of-line synchronization code configuration register	9-315
0x1460	LVDS0_LANE10_SOF_01	In LVDS/HiSPi mode, lane10 frame start synchronization code configuration register	9-316
0x1464	LVDS0_LANE10_SOF_23	In LVDS/HiSPi mode, lane10 frame start synchronization code configuration register	9-316
0x1468	LVDS0_LANE10_EOF_01	In LVDS/HiSPi mode, lane10 frame end synchronization code configuration register	9-317
0x146C	LVDS0_LANE10_EOF_23	In LVDS/HiSPi mode, lane10 frame end synchronization code configuration register	9-317
0x1470	LVDS0_LANE10_SOL_01	In LVDS/HiSPi mode, lane10 line start synchronization code configuration register	9-318
0x1474	LVDS0_LANE10_SOL_23	In LVDS/HiSPi mode, lane10 line start synchronization code configuration register	9-318
0x1478	LVDS0_LANE10_EOL_01	In LVDS/HiSPi mode, lane10 line end synchronization code configuration register	9-319
0x147C	LVDS0_LANE10_EOL_23	In LVDS/HiSPi mode, lane10 line end synchronization code configuration register	9-319
0x1480	LVDS0_LANE11_SOF_01	In LVDS/HiSPi mode, lane11 frame start synchronization code configuration register	9-320
0x1484	LVDS0_LANE11_SOF_23	In LVDS/HiSPi mode, lane11 frame start synchronization code configuration register	9-320
0x1488	LVDS0_LANE11_EOF_01	In LVDS/HiSPi mode, lane11 frame end synchronization code configuration register	9-321
0x148C	LVDS0_LANE11_EOF_23	In LVDS/HiSPi mode, lane11 frame end synchronization code configuration register	9-321
0x1490	LVDS0_LANE11_SOL_01	In LVDS/HiSPi mode, lane11 line start synchronization code configuration register	9-322
0x1494	LVDS0_LANE11_SOL_23	In LVDS/HiSPi mode, lane11 line start synchronization code configuration register	9-322
0x1498	LVDS0_LANE11_EOL_01	In LVDS/HiSPi mode, lane11 end-of-line synchronization code configuration register	9-323

offset address	name	describe	page number
0x149C	LVDS0_LANE11_EOL_23	In LVDS/HiSPi mode, lane11 end-of-line synchronization code configuration register	9-323
0x14A0	LVDS0_LANE0_NXT_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane0 frame start synchronization code configuration register	9-324
0x14A4	LVDS0_LANE0_NXT_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane0 frame start synchronization code configuration register	9-324
0x14A8	LVDS0_LANE0_NXT_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane0 frame end synchronization code configuration register	9-325
0x14AC	LVDS0_LANE0_NXT_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane0 frame end synchronization code configuration register	9-325
0x14B0	LVDS0_LANE0_NXT_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane0 line of frame N+1	9-326
0x14B4	LVDS0_LANE0_NXT_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane0 line of frame N+1	9-326
0x14B8	LVDS0_LANE0_NXT_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 0 of frame N+1	9-327
0x14BC	LVDS0_LANE0_NXT_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 0 of frame N+1	9-327
0x14C0	LVDS0_LANE1_NXT_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane1 frame start synchronization code configuration register	9-328
0x14C4	LVDS0_LANE1_NXT_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane1 frame start synchronization code configuration register	9-328
0x14C8	LVDS0_LANE1_NXT_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane1 frame end synchronization code configuration register	9-329
0x14CC	LVDS0_LANE1_NXT_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane1 frame end synchronization code configuration register	9-329
0x14D0	LVDS0_LANE1_NXT_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane1 line of N+1 frame	9-330
0x14D4	LVDS0_LANE1_NXT_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane1 line of N+1 frame	9-330
0x14D8	LVDS0_LANE1_NXT_EOL_01	In LVDS/HiSPi mode, end synchronization code configuration register of lane1 line of N+1 frame	9-331
0x14DC	LVDS0_LANE1_NXT_EOL_23	In LVDS/HiSPi mode, end synchronization code configuration register of lane1 line of N+1 frame	9-331
0x14E0	LVDS0_LANE2_NXT_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane2 frame start synchronization code configuration register	9-332

offset address	name	describe	page number
0x14E4	LVDS0_LANE2_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane2 frame start synchronization code configuration register	9-332
0x14E8	LVDS0_LANE2_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane2 frame end synchronization code configuration register	9-333
0x14EC	LVDS0_LANE2_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane2 frame end synchronization code configuration register	9-333
0x14F0	LVDS0_LANE2_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane2 line of frame N+1	9-334
0x14F4	LVDS0_LANE2_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane2 line of frame N+1	9-334
0x14F8	LVDS0_LANE2_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 2 of frame N+1	9-335
0x14FC	LVDS0_LANE2_NX T_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 2 of frame N+1	9-335
0x1500	LVDS0_LANE3_NX T_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane3 frame start synchronization code configuration register	9-336
0x1504	LVDS0_LANE3_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane3 frame start synchronization code configuration register	9-336
0x1508	LVDS0_LANE3_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane3 frame end synchronization code configuration register	9-337
0x150C	LVDS0_LANE3_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane3 frame end synchronization code configuration register	9-337
0x1510	LVDS0_LANE3_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane3 line of N+1 frame	9-338
0x1514	LVDS0_LANE3_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane3 line of N+1 frame	9-338
0x1518	LVDS0_LANE3_NX T_EOL_01	In LVDS/HiSPi mode, end synchronization code configuration register of lane3 line of N+1 frame	9-339
0x151C	LVDS0_LANE3_NX T_EOL_23	In LVDS/HiSPi mode, end synchronization code configuration register of lane3 line of N+1 frame	9-339
0x1520	LVDS0_LANE4_NX T_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane4 frame start synchronization code configuration register	9-340
0x1524	LVDS0_LANE4_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane4 frame start synchronization code configuration register	9-340
0x1528	LVDS0_LANE4_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane4 frame end synchronization code configuration register	9-341

offset address	name	describe	page number
0x152C	LVDS0_LANE4_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane4 frame end synchronization code configuration register	9-341
0x1530	LVDS0_LANE4_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane4 line of N+1 frame	9-342
0x1534	LVDS0_LANE4_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane4 line of N+1 frame	9-342
0x1538	LVDS0_LANE4_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 4 of frame N+1	9-343
0x153C	LVDS0_LANE4_NX T_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 4 of frame N+1	9-343
0x1540	LVDS0_LANE5_NX T_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane5 frame start synchronization code configuration register	9-344
0x1544	LVDS0_LANE5_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane5 frame start synchronization code configuration register	9-344
0x1548	LVDS0_LANE5_NX T_EOF_01	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane5 frame	9-345
0x154C	LVDS0_LANE5_NX T_EOF_23	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane5 frame	9-345
0x1550	LVDS0_LANE5_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane5 of frame N+1	9-346
0x1554	LVDS0_LANE5_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane5 of frame N+1	9-346
0x1558	LVDS0_LANE5_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 5 of frame N+1	9-347
0x155C	LVDS0_LANE5_NX T_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 5 of frame N+1	9-347
0x1560	LVDS0_LANE6_NX T_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane6 frame start synchronization code configuration register	9-348
0x1564	LVDS0_LANE6_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane6 frame start synchronization code configuration register	9-348
0x1568	LVDS0_LANE6_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane6 frame end synchronization code configuration register	9-349
0x156C	LVDS0_LANE6_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane6 frame end synchronization code configuration register	9-349
0x1570	LVDS0_LANE6_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane6 line of N+1 frame	9-350

offset address	name	describe	page number
0x1574	LVDS0_LANE6_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane6 line of N+1 frame	9-350
0x1578	LVDS0_LANE6_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 6 of frame N+1	9-351
0x157C	LVDS0_LANE6_NX T_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 6 of frame N+1	9-351
0x1580	LVDS0_LANE7_NX T_SOF_01	In LVDS/HiSPi mode, the N+1 frame lane7 frame start synchronization code configuration register	9-352
0x1584	LVDS0_LANE7_NX T_SOF_23	In LVDS/HiSPi mode, the N+1 frame lane7 frame start synchronization code configuration register	9-352
0x1588	LVDS0_LANE7_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane7 frame end synchronization code configuration register	9-353
0x158C	LVDS0_LANE7_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane7 frame end synchronization code configuration register	9-353
0x1590	LVDS0_LANE7_NX T_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane7 line of frame N+1	9-354
0x1594	LVDS0_LANE7_NX T_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane7 line of frame N+1	9-354
0x1598	LVDS0_LANE7_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 7 of frame N+1	9-355
0x159C	LVDS0_LANE7_NX T_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 7 of frame N+1	9-355
0x15A0	LVDS0_LANE8_NX T_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane8 frame start synchronization code configuration register	9-356
0x15A4	LVDS0_LANE8_NX T_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane8 frame start synchronization code configuration register	9-356
0x15A8	LVDS0_LANE8_NX T_EOF_01	In LVDS/HiSPi mode, the N+1th frame lane8 frame end synchronization code configuration register	9-357
0x15AC	LVDS0_LANE8_NX T_EOF_23	In LVDS/HiSPi mode, the N+1th frame lane8 frame end synchronization code configuration register	9-357
0x15B0	LVDS0_LANE8_NX T_SOL_01	In LVDS/HiSPi mode, the N+1th frame lane8 line start synchronization code configuration register	9-358
0x15B4	LVDS0_LANE8_NX T_SOL_23	In LVDS/HiSPi mode, the N+1th frame lane8 line start synchronization code configuration register	9-358
0x15B8	LVDS0_LANE8_NX T_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 8 of frame N+1	9-359

offset address	name	describe	page number
0x15BC	LVDS0_LANE8_NXT_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 8 of frame N+1	9-359
0x15C0	LVDS0_LANE9_NXT_SOF_01	In LVDS/HiSPi mode, the N+1 frame lane9 frame start synchronization code configuration register	9-360
0x15C4	LVDS0_LANE9_NXT_SOF_23	In LVDS/HiSPi mode, the N+1 frame lane9 frame start synchronization code configuration register	9-360
0x15C8	LVDS0_LANE9_NXT_EOF_01	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane9 frame	9-361
0x15CC	LVDS0_LANE9_NXT_EOF_23	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane9 frame	9-361
0x15D0	LVDS0_LANE9_NXT_SOL_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane9 of frame N+1	9-362
0x15D4	LVDS0_LANE9_NXT_SOL_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane9 of frame N+1	9-362
0x15D8	LVDS0_LANE9_NXT_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 9 of frame N+1	9-363
0x15DC	LVDS0_LANE9_NXT_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 9 of frame N+1	9-363
0x15E0	LVDS0_LANE10_NXT_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane10 frame start synchronization code configuration register	9-364
0x15E4	LVDS0_LANE10_NXT_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane10 frame start synchronization code configuration register	9-364
0x15E8	LVDS0_LANE10_NXT_EOF_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of frame N+1 lane10 frame	9-365
0x15EC	LVDS0_LANE10_NXT_EOF_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of frame N+1 lane10 frame	9-365
0x15F0	LVDS0_LANE10_NXT_SUN_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane10 of frame N+1	9-366
0x15F4	LVDS0_LANE10_NXT_SUN_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane10 of frame N+1	9-366
0x15F8	LVDS0_LANE10_NXT_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 10 of frame N+1	9-367
0x15FC	LVDS0_LANE10_NXT_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 10 of frame N+1	9-367
0x1600	LVDS0_LANE11_NXT_SOF_01	In LVDS/HiSPi mode, the N+1th frame lane11 frame start synchronization code configuration register	9-368

offset address	name	describe	page number
0x1604	LVDS0_LANE11_N XT_SOF_23	In LVDS/HiSPi mode, the N+1th frame lane11 frame start synchronization code configuration register	9-368
0x1608	LVDS0_LANE11_N XT_EOF_01	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane11 frame	9-369
0x160C	LVDS0_LANE11_N XT_EOF_23	In LVDS/HiSPi mode, the synchronization code configuration register of the end of frame N+1 lane11 frame	9-369
0x1610	LVDS0_LANE11_N XT_SUN_01	In LVDS/HiSPi mode, the start synchronization code configuration register of lane11 of frame N+1	9-370
0x1614	LVDS0_LANE11_N XT_SUN_23	In LVDS/HiSPi mode, the start synchronization code configuration register of lane11 of frame N+1	9-370
0x1618	LVDS0_LANE11_N XT_EOL_01	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 11 of frame N+1	9-371
0x161C	LVDS0_LANE11_N XT_EOL_23	In LVDS/HiSPi mode, the synchronization code configuration register at the end of line 11 of frame N+1	9-371
0x1620	LVDS0_LI_WORD0	LVDS DOL mode frame 0 LI register	9-372
0x1624	LVDS0_LI_WORD1	LVDS DOL mode frame 1 LI register	9-372
0x1628	LVDS0_LI_WORD2	LVDS DOL mode frame 2 LI register	9-373
0x162C	LVDS0_LI_WORD3	LVDS DOL mode frame 3 LI register	9-373
0x1680	LVDS0_IMGSIZE0_ STATIS	LVDS LEF image width and height statistics register	9-374
0x1684	LVDS0_IMGSIZE1_ STATIS	LVDS SEF1 image width and height statistics register	9-374
0x1688	LVDS0_IMGSIZE2_ STATIS	LVDS SEF2 image width and height statistics register	9-374
0x168C	LVDS0_IMGSIZE3_ STATIS	LVDS SEF3 image width and height statistics register	9-375
0x16F0	LVDS0_CTRL_INT_ RAW	LVDS Read Data Raw Interrupt Status Register 9-375	
0x16F4	LVDS0_CTRL_INT	LVDS read data interrupt status register	9-378
0x16F8	LVDS0_CTRL_INT_ CEC	LVDS Read Data Interrupt Mask Register	9-381
0x1700	LANE_ID0_CHN0	Link0 Individual LANE Priority Configuration Register 9-384	
0x1704	LANE_ID1_CHN0	Link1 individual LANE priority configuration register 9-385	
0x1708	LANE_ID2_CHN0	Link2 each LANE priority configuration register 9-386	

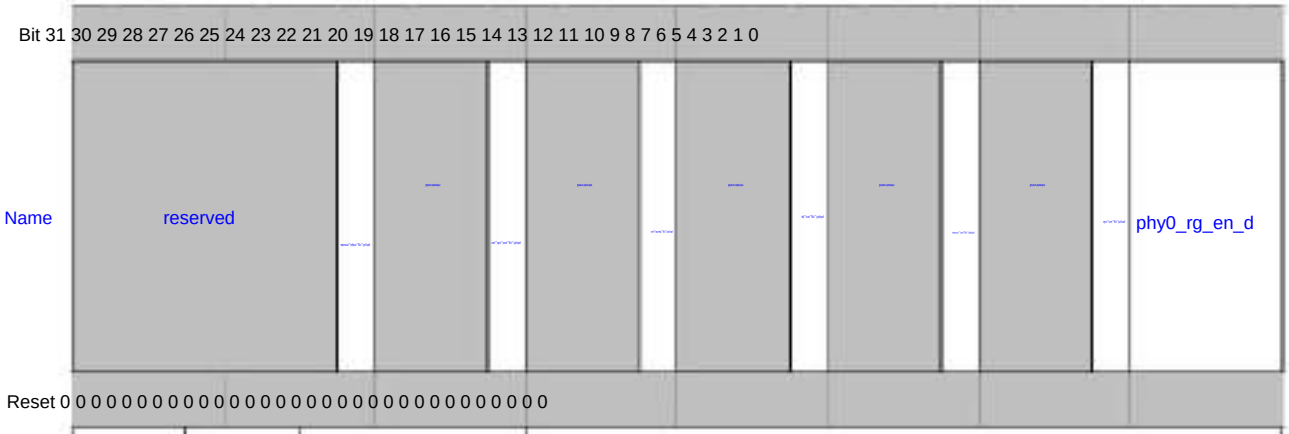
offset address	name	describe	page number
0x17F0	ALIGN0_INT_RAW MIPI_ALIGN	Raw Interrupt Status Register	9-386
0x17F4	ALIGN0_INT	MIPI_ALIGN Interrupt Status Register	9-388
0x17F8	ALIGN0_INT_MSK MIPI_ALIGN	interrupt mask register	9-390

9.3.6 MIPI register description

PHY_MODE_LINK0

PHY_MODE_LINK0 is Link0 PHY working mode register.

Offset Address	Register Name	Total Reset Value
0x0000	PHY_MODE_LINK0	0x0000_0000



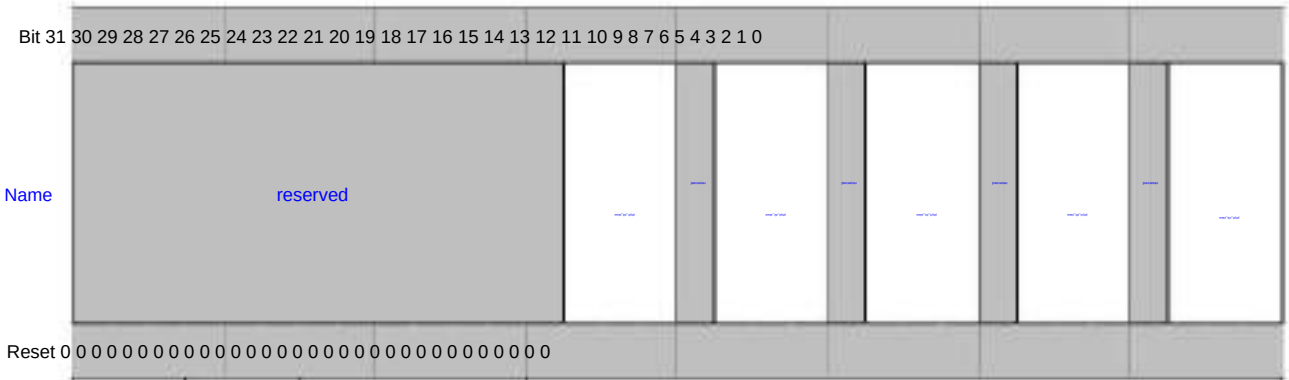
Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	phy0_rg_mipi_mod	MIPI/LVDS input mode selection. Set to 0 when PHY works in LVDS mode and Common voltage is greater than or equal to 1.25V. 0: Common voltage is above 1.25V; 1: Common voltage is 1.25V or below.
[23:21]	RO	reserved	reserve.
[20]	RW	phy0_rg_ext_clk_en	Differential clock source selection. 0: select PAD input differential clock; 1: Select the differential clock of other Link.
[19:17]	RO	reserved	reserve.
[16]	RW	phy0_rg_faclk_en	The associated clock phase of the PHY output data. 0: clock rising edge output data; 1: Output data on the falling edge of the clock.

[15:13] RO		reserved	reserve.
[12] RW	phy0_rg_en_lp		LP mode is enabled. Enabled in MIPI mode, disabled in other modes. 0: Disable the LP mode of PHY; 1: Enable LP mode of the PHY.
[11:9] RO		reserved	reserve.
[8] RW	phy0_rg_en_cmos		CMOS mode enabled. 0: Disable CMOS mode of PHY; 1: Enable CMOS mode of PHY.
[7:5] RO		reserved	reserve.
[4] RW	phy0_rg_en_clk		Clock Lane is enabled. 0: Disable Clock Lane; 1: Enable Clock Lane.
[3:0] RW	phy0_rg_en_d		Data Lane enabled. 0: Disable the corresponding Data Lane; 1: Enable the corresponding Data Lane.

PHY_SKEW_LINK0

PHY_SKEW_LINK0 is Link0 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0004	PHY_SKEW_LINK0	0x0000_0000



Bits	Access	Name	Description
[31:19] RO		reserved	reserve.
[18:16] RW	phy0_d3_skew		Timing delay adjustment for Data lane 3. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[15] RO		reserved	reserve.

[14:12] RW	phy0_d2_skew		Timing delay adjustment for Data lane 2. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[11] RO		reserved	reserve.
[10:8] RW	phy0_d1_skew		Timing delay adjustment for Data lane 1. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[7]	RO	reserved	reserve.
[6:4] RW	phy0_d0_skew		Timing delay adjustment for Data lane 0. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[3]	RO	reserved	reserve.
[2:0] RW	phy0_clk_skew		Timing delay adjustment of Clock Lane. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.

PHY_EN_LINK0

PHY_EN_LINK0 is Link0 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0008	PHY_EN_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
resistor; [8]	RW	phy0_clk_term_en	Clock Lane Termination Impedance Enable. 0: Turn off the internal termination 1: Turn on the internal termination resistor.
[7]	RW	phy0_d3_term_en	Data lane3 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.

[6]	RW	phy0_d2_term_en	Data lane2 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[5]	RW	phy0_d1_term_en	Termination impedance enable for Data lane1. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[4]	RW	phy0_d0_term_en	Termination impedance enable for Data lane0. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[3]	RW	phy0_da_d3_valid	Data lane3 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.
mode off; [2]	RW	phy0_da_d2_valid	Data lane2 high-speed mode enable. 0: high speed 1: High speed mode enabled.
mode off; [1]	RW	phy0_da_d1_valid	Data lane1 high-speed mode enable. 0: high speed 1: High speed mode enabled.
[0]	RW	phy0_da_d0_valid	Data lane0 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.

PHY_DATA_LINK0

PHY_DATA_LINK0 is the parallel data register of Link0 PHY output.

Offset Address	Register Name	Total Reset Value
0x0018	PHY_DATA_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy0_data3_mipi	phy0_data2_mipi	phy0_data1_mipi	phy0_data0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi	Data Lane3 received data.
[23:16]	RO	phy0_data2_mipi	Data Lane2 received data.
[15:8]	RO	phy0_data1_mipi	Data Lane1 received data.

Offset Address	Register Name	Total Reset Value
0x0018	PHY_DATA_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy0_data3_mipi	phy0_data2_mipi	phy0_data1_mipi	phy0_data0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[7:0]	RO	phy0_data0_mipi Data	Lane0 received data.

PHY_PH_MIPI_LINK0

PHY_PH_MIPI_LINK0 is Link0 MIPI packet header register.

Offset Address	Register Name	Total Reset Value
0x001C	PHY_PH_MIPI_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy0_ph3_mipi	phy0_ph2_mipi	phy0_ph1_mipi	phy0_ph0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy0_ph3_mipi Data	Lane3 received packet header.
[23:16]	RO	phy0_ph2_mipi Data	packet header received by Data Lane2.
[15:8]	RO	phy0_ph1_mipi Data	packet header received by Data Lane1.
[7:0]	RO	phy0_ph0_mipi Data	Lane0 Received packet header.

PHY_DATA_MIPI_LINK0

PHY_DATA_MIPI_LINK0 is Link0 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0020	PHY_DATA_MIPI_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy0_data3_mipi_hs	phy0_data2_mipi_hs	phy0_data1_mipi_hs	phy0_data0_mipi_hs
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi_hs	Data Lane3 MIPI formatted data.

Offset Address	Register Name	Total Reset Value
0x0020	PHY_DATA_MIPI_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_data3_mipi_hs																phy0_data2_mipi_hs															
Name	phy0_data1_mipi_hs																phy0_data0_mipi_hs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[23:16]	RO	phy0_data2_mipi_hs Data	Lane2 MIPI formatted data.
[15:8]	RO	phy0_data1_mipi_hs Data	Lane1 MIPI formatted data.
[7:0]	RO	phy0_data0_mipi_hs Data	Lane0 MIPI formatted data.

PHY_SYNC_DCT_LINK0

PHY_SYNC_DCT_LINK0 is the synchronous header detection control register of Link0 PHY LVDS mode.

Offset Address	Register Name	Total Reset Value
0x0024	PHY_SYNC_DCT_LINK0	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:9]	RO	reserved	reserve.
[8]	RW	serial data sequence is an	In LVDS/HiSPi mode, the serial bit transmission order of the transmitted RAW data synchronization code (sync_code). 0: LSB, the lower bit is transmitted first, the actually received sync code (sync_code) bit0, bit1, ... bit11; 1: MSB, the higher bit is transmitted first, the actually received sync code (sync_code) The sequence of serial data is bit11, bit10, ... bit0.
[7]	RO	reserved	reserve.

[6:4] RW	cil0_split_mode		LVDS/HiSPi Sync Code transfer type. 000: Per Lane mode; Other: reserved.
[3]	RO	reserved	reserve.
[2:0] RW	cil0_raw_type		In LVDS/HiSPi mode, the RAW data type transmitted. 001ÿRaw 8bitÿ 010ÿRaw 10bitÿ 011ÿRaw 12bitÿ 100ÿRaw 14bitÿ 101ÿRaw 16bitÿ Other: reserved.

PHY_SYNC_CODE0_LINK0

PHY_SYNC_CODE0_LINK0 is Link0 PHY LVDS mode sync header register 0.

Offset Address	Register Name	Total Reset Value
0x0030	PHY_SYNC_CODE0_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil0_sof1_word4_0	cil0_sof0_word4_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_0	Lane0 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil0_sof0_word4_0	Lane0 frame start synchronization code (N Frame).

PHY_SYNC_CODE1_LINK0

PHY_SYNC_CODE1_LINK0 is Link0 PHY LVDS mode sync header register 1.

Offset Address	Register Name	Total Reset Value
0x0034	PHY_SYNC_CODE1_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil0_sof1_word4_1	cil0_sof0_word4_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_1	Lane1 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil0_sof0_word4_1	Lane1 frame start synchronization code (N Frame).

PHY_SYNC_CODE2_LINK0

PHY_SYNC_CODE2_LINK0 is Link0 PHY LVDS mode sync header register 2.

Offset Address	Register Name	Total Reset Value
0x0038	PHY_SYNC_CODE2_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil0_sof1_word4_2	cil0_sof0_word4_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_2	Lane2 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil0_sof0_word4_2	Lane2 frame start synchronization code (N Frame).

PHY_SYNC_CODE3_LINK0

PHY_SYNC_CODE3_LINK0 is Link0 PHY LVDS mode sync header register 3.

Offset Address	Register Name	Total Reset Value
0x003C	PHY_SYNC_CODE3_LINK0	0x0000_0000

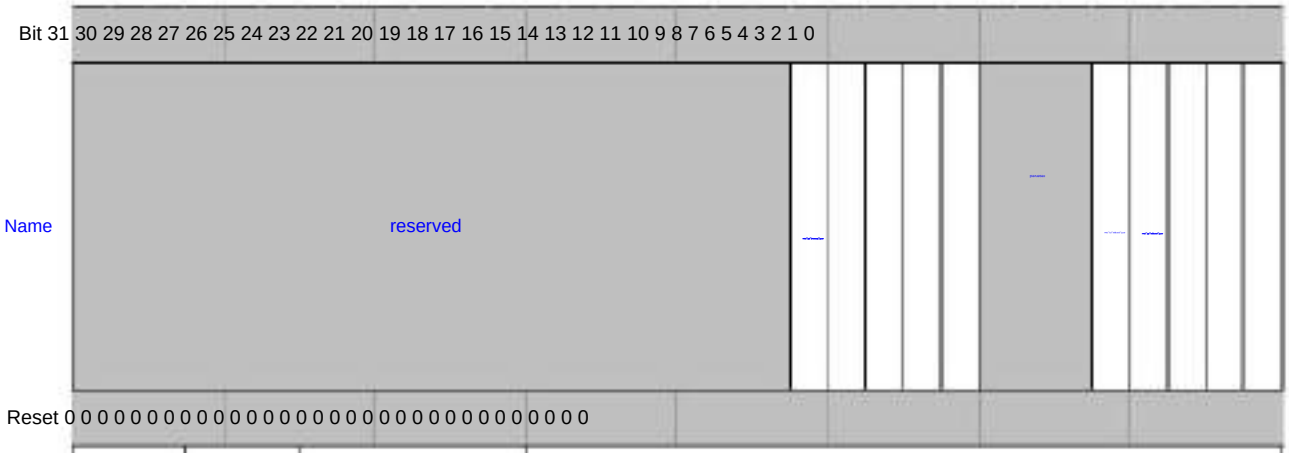
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil0_sof1_word4_3	cil0_sof0_word4_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_3	Lane3 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil0_sof0_word4_3	Lane3 frame start synchronization code (N Frame).

MIPI_CIL_INT_RAW_LINK0

MIPI_CIL_INT_RAW_LINK0 is Link0 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F0	MIPI_CIL_INT_RAW_LINK0	0x0000_0000



Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	WC	err0_timeout_ck_ra 0: In	Clock Lane FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[11]	WC	err0_timeout_d3_ra 0: In	Data Lane3 FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[10]	WC	err0_timeout_d2_ra 0: In	Data Lane2 FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[9]	WC	err0_timeout_d1_ra 0: In	Data Lane1 FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[8]	WC	err0_timeout_d0_ra 0: In	Data Lane0 FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[7:5]	RO	reserved	reserve.

[4] WC		status.In	err0_escape_ck_ra	Clock Lane escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[3] WC		status.In	err0_escape_d3_ra	Data Lane3 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[2] WC		status.In	err0_escape_d2_ra	Data Lane2 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[1] WC		status.In	err0_escape_d1_ra	Data Lane1 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[0] WC		status.In	err0_escape_d0_ra	Data Lane0 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.

MIPI_CIL_INT_LINK0

MIPI_CIL_INT_LINK0 is Link0 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F4	MIPI_CIL_INT_LINK0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

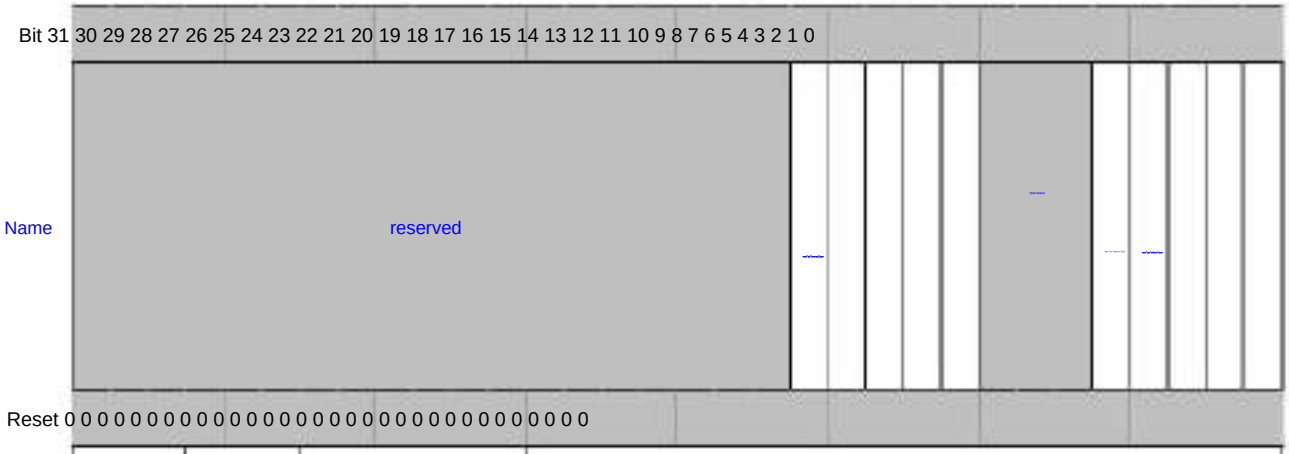
Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RO	err0_timeout_ck_st	Clock Lane FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.

[11] RO		err0_timeout_d3_st	Data Lane3 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[10] RO		err0_timeout_d2_st	Data Lane2 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[9]	RO	err0_timeout_d1_st	Data Lane1 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[8]	RO	err0_timeout_d0_st	Data Lane0 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[7:5] RO		reserved	reserve.
[4]	RO	err0_escape_ck_st	Clock Lane escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	err0_escape_d3_st	Data Lane3 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	err0_escape_d2_st 1: interrupt.	Data Lane2 escape sequence interrupt status. 0: no interrupt;
[1]	RO	err0_escape_d1_st	Data Lane1 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	err0_escape_d0_st	Data Lane0 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.

MIPI_CIL_INT_MSK_LINK0

MIPI_CIL_INT_MSK_LINK0 is Link0 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	MIPI_CIL_INT_MSK_LINK0	0x0000_0000



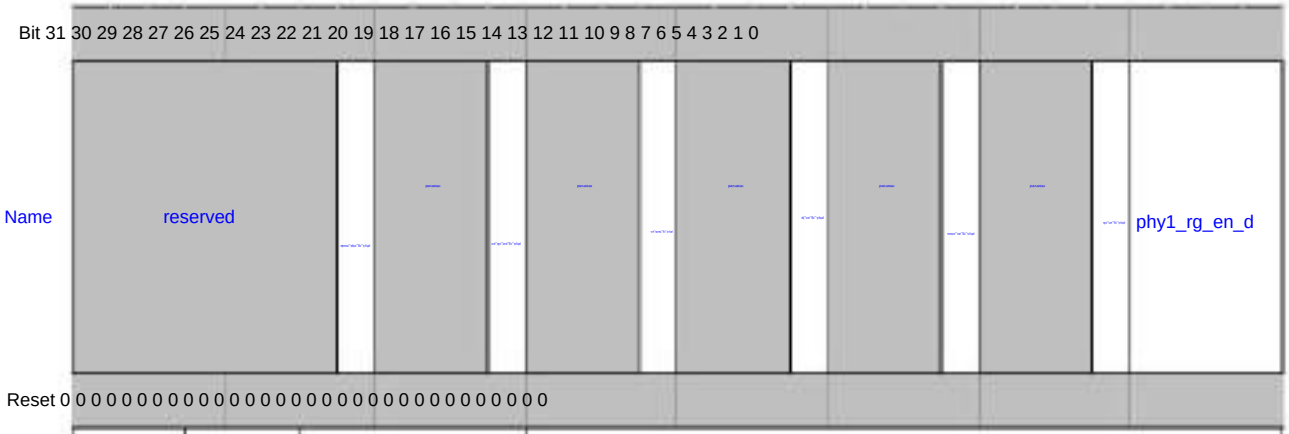
Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	err0_timeout_ck_m	Clock Lane FSM timeout interrupt status enable. 0: mask interrupt; sk 1: Interrupts are enabled.
[11]	RW	err0_timeout_d3_m	Data Lane3 FSM timeout interrupt status enable. 0: mask interrupt; sk 1: Interrupts are enabled.
[10]	RW	err0_timeout_d2_m	Data Lane2 FSM timeout interrupt status enable. 0: mask interrupt; sk 1: Interrupts are enabled.
[9]	RW	err0_timeout_d1_m	Data Lane1 FSM timeout interrupt status enable. 0: mask interrupt; sk 1: enable interrupt.
[8]	RW	err0_timeout_d0_m	Data Lane0 FSM timeout interrupt status enable. 0: mask interrupt; sk 1: Interrupts are enabled.
[7:5]	RO	reserved	reserve.
[4]	RW	err0_escape_ck_m	Clock Lane escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.
[3]	RW	err0_escape_d3_m	Data Lane3 escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.

[2] RW		enable. err0_escape_d2_mask	Data Lane2 escape sequence interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[1] RW		enable. err0_escape_d1_mask	Data Lane1 escape sequence interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[0] RW		enable. err0_escape_d0_mask	Data Lane0 escape sequence interrupt status 0: mask interrupt; 1: Interrupts are enabled.

PHY_MODE_LINK1

PHY_MODE_LINK1 is Link1 PHY working mode register.

Offset Address	Register Name	Total Reset Value
0x0200	PHY_MODE_LINK1	0x0000_0000



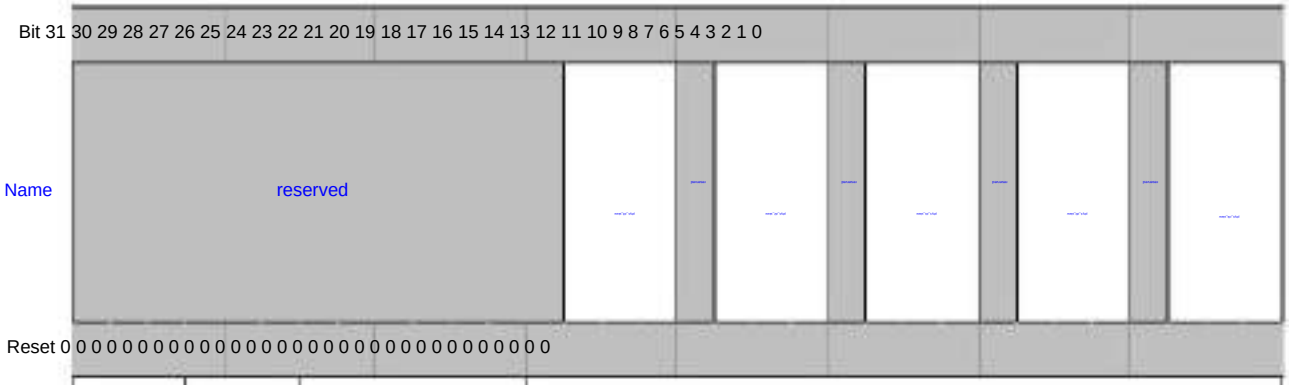
Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	phy1_rg_mipi_mode	MIPI/LVDS input mode selection. Set to 0 when PHY works in LVDS mode and Common voltage is greater than or equal to 1.25V. 0: Common voltage is above 1.25V; 1: Common voltage is 1.25V or below.
[23:21]	RO	reserved	reserve.
[20]	RW	phy1_rg_ext_clk_en	Differential clock source selection. 0: select PAD input differential clock; 1: Select the differential clock of other Link.
[19:17]	RO	reserved	reserve.

[16] RW	phy1_rg_faclk_en		The associated clock phase of the PHY output data. 0: clock rising edge output data; 1: Output data on the falling edge of the clock.
[15:13] RO		reserved	reserve.
[12] RW	phy1_rg_en_lp		LP mode is enabled. Enabled in MIPI mode, disabled in other modes. 0: Disable the LP mode of PHY; 1: Enable LP mode of the PHY.
[11:9] RO		reserved	reserve.
[8] RW	phy1_rg_en_cmos		CMOS mode enabled. 0: Disable CMOS mode of PHY; 1: Enable CMOS mode of PHY.
[7:5] RO		reserved	reserve.
[4] RW	phy1_rg_en_clk		Clock Lane is enabled. 0: Disable Clock Lane; 1: Enable Clock Lane.
[3:0] RW	phy1_rg_en_d		Data Lane enabled. 0: Disable the corresponding Data Lane; 1: Enable the corresponding Data Lane.

PHY_SKEW_LINK1

PHY_SKEW_LINK1 is the Link1 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0204	PHY_SKEW_LINK1	0x0000_0000



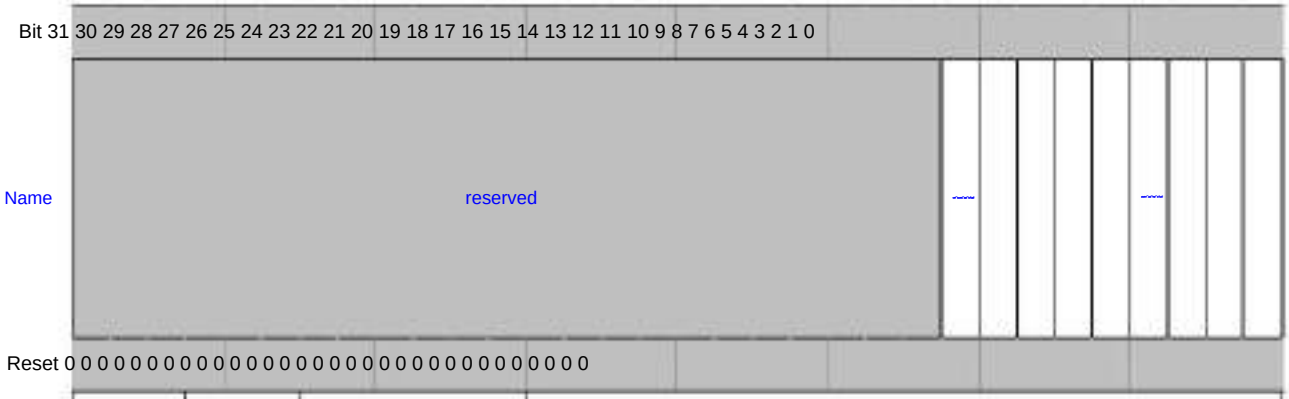
Bits	Access	Name	Description
[31:19] RO		reserved	reserve.

[18:16] RW	phy1_d3_skew		Timing delay adjustment for Data lane 3 . Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[15] RO		reserved	reserve.
[14:12] RW	phy1_d2_skew		Timing delay adjustment for Data lane 2. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[11] RO		reserved	reserve.
[10:8] RW	phy1_d1_skew		Timing delay adjustment for Data lane 1. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[7]	RO	reserved	reserve.
[6:4] RW	phy1_d0_skew		Timing delay adjustment for Data lane 0. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[3]	RO	reserved	reserve.
[2:0] RW	phy1_clk_skew		Timing delay adjustment of Clock Lane. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.

PHY_EN_LINK1

PHY_EN_LINK1 is Link1 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0208	PHY_EN_LINK1	0x0000_0000



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	phy1_clk_term_en	Clock Lane Termination Impedance Enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.

[7] RW	phy1_d3_term_en		Data lane3 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[6] RW	phy1_d2_term_en		Data lane2 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[5] RW	phy1_d1_term_en		Termination impedance enable for Data lane1. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[4] RW	phy1_d0_term_en		Termination impedance enable for Data lane0. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
RW	phy1_da_d3_valid		Data lane3 high-speed mode enable. 0: High speed mode off; [3] 1: High speed mode enabled.
RW	phy1_da_d2_valid		Data lane2 high-speed mode enable. 0: high speed mode off; [2] 1: High speed mode enabled.
[1] RW	phy1_da_d1_valid		Data lane1 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.
RW	phy1_da_d0_valid		Data lane0 high-speed mode enable. 0: High speed mode off; [0] 1: High speed mode enabled.

PHY_DATA_LINK1

PHY_DATA_LINK1 is the parallel data register of Link1 PHY output.

Offset Address	Register Name	Total Reset Value
0x0218	PHY_DATA_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy1_data3_mipi	phy1_data2_mipi	phy1_data1_mipi	phy1_data0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_data3_mipi Data	Lane3 received data.
[23:16]	RO	phy1_data2_mipi Data	Lane2 received data.
[15:8]	RO	phy1_data1_mipi Data	Lane1 received data.
[7:0]	RO	phy1_data0_mipi Data	Lane0 received data.

PHY_PH_MIPI_LINK1

PHY_PH_MIPI_LINK1 is Link1 MIPI packet header register.

Offset Address	Register Name	Total Reset Value
0x021C	PHY_PH_MIPI_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy1_ph3_mipi	phy1_ph2_mipi	phy1_ph1_mipi	phy1_ph0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_ph3_mipi Data	packet header received by Data Lane3.
[23:16]	RO	phy1_ph2_mipi Data	packet header received by Data Lane2.
[15:8]	RO	phy1_ph1_mipi Data	packet header received by Data Lane1.
[7:0]	RO	phy1_ph0_mipi Data	Lane0 Received packet header.

PHY_DATA_MIPI_LINK1

PHY_DATA_MIPI_LINK1 is Link1 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0220	PHY_DATA_MIPI_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy1_data3_mipi_hs	phy1_data2_mipi_hs	phy1_data1_mipi_hs	phy1_data0_mipi_hs
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_data3_mipi_hs	Lane3 MIPI format data.
[23:16]	RO	phy1_data2_mipi_hs	Lane2 MIPI format data.
[15:8]	RO	phy1_data1_mipi_hs	Lane1 MIPI formatted data.
[7:0]	RO	phy1_data0_mipi_hs	Lane0 MIPI formatted data.

PHY_SYNC_DCT_LINK1

PHY_SYNC_DCT_LINK1 is Link1 PHY LVDS mode sync header detection control register.

Offset Address	Register Name	Total Reset Value
0x0224	PHY_SYNC_DCT_LINK1	0x0000_0101

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	(sync_code) serial number cit1_code_big_endian	In LVDS/HiSPi mode, the serial bit transmission order of the transmitted RAW data synchronization code (sync_code). 0: LSB, the lower bit is transmitted first, and the actually received synchronization code data sequence is bit0, bit1, ... bit11; 1: MSB, the high bit is transmitted first, and the serial data sequence of the actually received synchronization code (sync_code) is bit11, bit10, ... bit0.

[7]	RO	reserved	reserve.
[6:4] RW	cil1_split_mode		LVDS/HiSPi Sync Code transfer type. 000: Per Lane mode; Other: reserved.
[3]	RO	reserved	reserve.
[2:0] RW	cil1_raw_type		In LVDS/HiSPi mode, the RAW data type transmitted. 001ÿRaw 8bitÿ 010ÿRaw 10bitÿ 011ÿRaw 12bitÿ 100ÿRaw 14bitÿ 101ÿRaw 16bitÿ Other: reserved.

PHY_SYNC_CODE0_LINK1

PHY_SYNC_CODE0_LINK1 is Link1 PHY LVDS mode sync header register 0.

Offset Address	Register Name	Total Reset Value
0x0230	PHY_SYNC_CODE0_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil1_sof1_word4_0	cil1_sof0_word4_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_0	Lane0 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil1_sof0_word4_0	Lane0 frame start synchronization code (N Frame).

PHY_SYNC_CODE1_LINK1

PHY_SYNC_CODE1_LINK1 is Link1 PHY LVDS mode sync header register 1.

Offset Address	Register Name	Total Reset Value
0x0234	PHY_SYNC_CODE1_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil1_sof1_word4_1	cil1_sof0_word4_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_1	Lane1 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil1_sof0_word4_1	Lane1 frame start synchronization code (N Frame).

PHY_SYNC_CODE2_LINK1

PHY_SYNC_CODE2_LINK1 is Link1 PHY LVDS mode sync header register 2.

Offset Address	Register Name	Total Reset Value
0x0238	PHY_SYNC_CODE2_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil1_sof1_word4_2	cil1_sof0_word4_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_2	Lane2 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil1_sof0_word4_2	Lane2 frame start synchronization code (N Frame).

PHY_SYNC_CODE3_LINK1

PHY_SYNC_CODE3_LINK1 is Link1 PHY LVDS mode sync header register 3.

Offset Address	Register Name	Total Reset Value
0x023C	PHY_SYNC_CODE3_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil1_sof1_word4_3	cil1_sof0_word4_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_3	Lane3 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil1_sof0_word4_3	Lane3 frame start synchronization code (N Frame).

MIPI_CIL_INT_RAW_LINK1

MIPI_CIL_INT_RAW_LINK1 is Link1 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x03F0	MIPI_CIL_INT_RAW_LINK1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

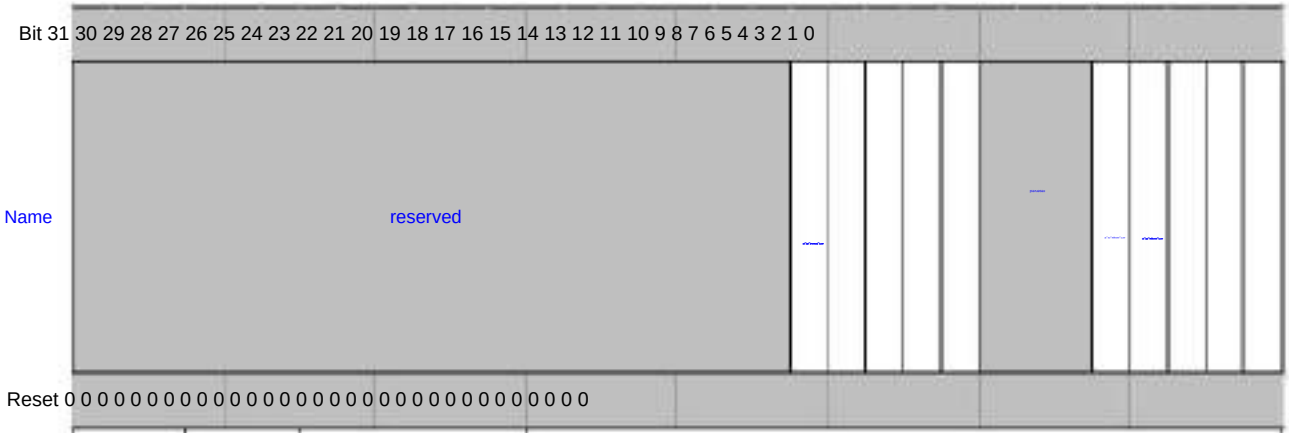
Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	WC	err1_timeout_ck_ra	Clock Lane FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[11]	WC	err1_timeout_d3_ra	Data Lane3 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[10]	WC	err1_timeout_d2_ra	Data Lane2 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[9]	WC	err1_timeout_d1_ra	Data Lane1 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[8]	WC	err1_timeout_d0_ra	Data Lane0 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[7:5]	RO	reserved	reserve.

[4] WC		status.
In err1_escape_ck_	Clock Lane escape sequence raw interrupt
ra 0: no raw interrupt;
1: There is a raw interrupt.
[3] WC		status.
In err1_escape_d3_	Data Lane3 escape sequence raw interrupt
ra 0: no raw interrupt;
1: There is a raw interrupt.
[2] WC		status.
In err1_escape_d2_	Data Lane2 escape sequence raw interrupt
ra 0: no raw interrupt;
1: There is a raw interrupt.
[1] WC		status.
In err1_escape_d1_	Data Lane1 escape sequence raw interrupt
ra 0: no original interrupt;
1: There is a raw interrupt.
[0] WC		status.
In err1_escape_d0_	Data Lane0 escape sequence raw interrupt
ra 0: no raw interrupt;
1: There is a raw interrupt.

MIPI_CIL_INT_LINK1

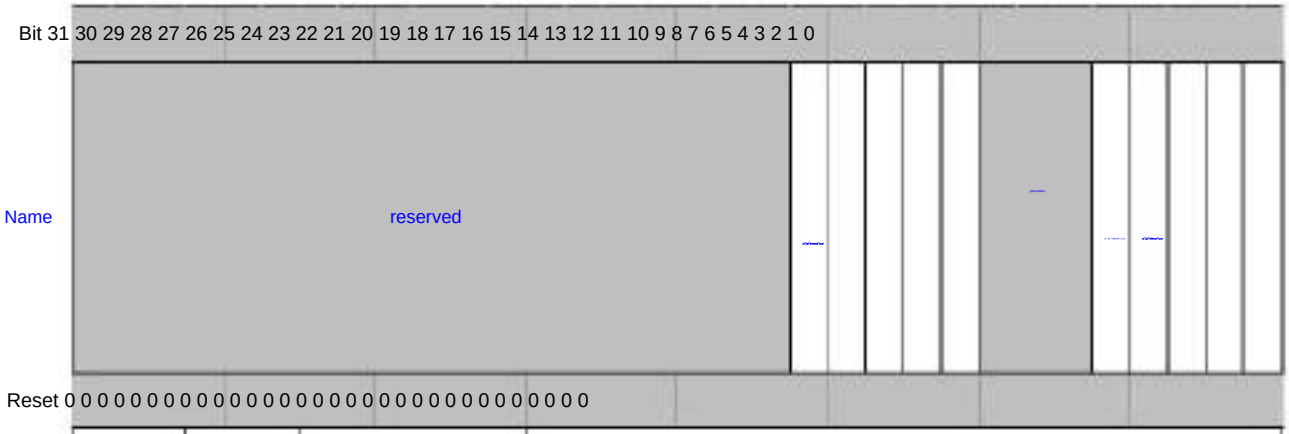
MIPI_CIL_INT_LINK1 is the Link1 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x03F4	MIPI_CIL_INT_LINK1	0x0000_0000



Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RO		err1_timeout_ck_st	Clock Lane FSM timeout interrupt status. 0:
no interrupt;
1: There is an interrupt.

Offset Address	Register Name	Total Reset Value
0x03F4	MIPI_CIL_INT_LINK1	0x0000_0000



Bits	Access Name		Description
[11] RO		err1_timeout_d3_st	Data Lane3 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[10] RO		err1_timeout_d2_st	Data Lane2 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[9]	RO	err1_timeout_d1_st 1:	Data Lane1 FSM timeout interrupt status. 0: no interrupt; interrupted.
[8]	RO	err1_timeout_d0_st	Data Lane0 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[7:5] RO		reserved	reserve.
[4]	RO	err1_escape_ck_st	Clock Lane escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	err1_escape_d3_st	Data Lane3 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	err1_escape_d2_st	Data Lane2 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.

Offset Address	Register Name	Total Reset Value
0x03F4	MIPI_CIL_INT_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[1]	RO	err1_escape_d1_st	Data Lane1 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	err1_escape_d0_st	Data Lane0 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.

MIPI_CIL_INT_MSK_LINK1

MIPI_CIL_INT_MSK_LINK1 is Link1 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x03F8	MIPI_CIL_INT_MSK_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

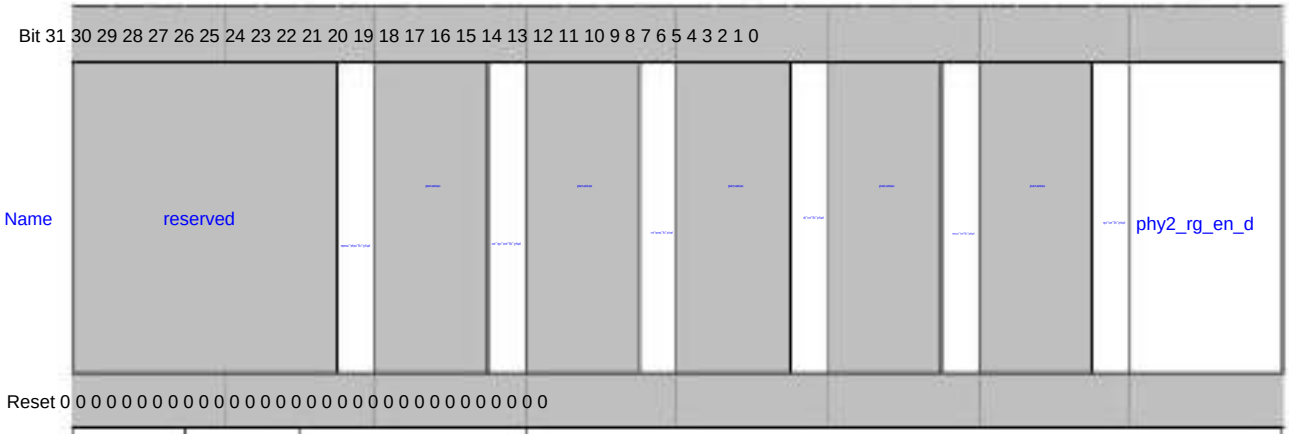
Bits	Access Name		Description
[31:13]	RO	reserved	reserve.

[12] RW		err1_timeout_ck_m 0:	Clock Lane FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[11] RW		err1_timeout_d3_m 0:	Data Lane3 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[10] RW		err1_timeout_d2_m 0:	Data Lane2 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[9] RW		err1_timeout_d1_m 0:	Data Lane1 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[8] RW		err1_timeout_d0_m 0:	Data Lane0 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[7:5] RO		reserved	reserve.
[4] RW		err1_escape_ck_m	Clock Lane escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.
[3] RW		err1_escape_d3_m	Data Lane3 escape sequence interrupt status enable. 0: mask interrupt; k 1: enable interrupt.
[2] RW		err1_escape_d2_m	Data Lane2 escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.
[1] RW		err1_escape_d1_m	Data Lane1 escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.
[0] RW		err1_escape_d0_m	Data Lane0 escape sequence interrupt status enable. 0: mask interrupt; k 1: Interrupts are enabled.

PHY_MODE_LINK2

PHY_MODE_LINK2 is Link2 PHY working mode register.

Offset Address	Register Name	Total Reset Value
0x0400	PHY_MODE_LINK2	0x0000_0000



Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	phy2_rg_mipi_mod	MIPI/LVDS input mode selection. Set to 0 when PHY works in LVDS mode and Common voltage is greater than or equal to 1.25V. 0: Common voltage is above 1.25V; 1: Common voltage is 1.25V or below.
[23:21]	RO	reserved	reserve.
[20]	RW	phy2_rg_ext_clk_en	Differential clock source selection. 0: select PAD input differential clock; 1: Select the differential clock of other Link.
[19:17]	RO	reserved	reserve.
[16]	RW	phy2_rg_faclk_en	The associated clock phase of the PHY output data. 0: output data on the rising edge of the clock; 1: output data on the falling edge of the clock.
[15:13]	RO	reserved	reserve.
[12]	RW	phy2_rg_en_lp	LP mode is enabled. Enabled in MIPI mode, disabled in other modes. 0: Disable the LP mode of PHY; 1: Enable LP mode of the PHY.
[11:9]	RO	reserved	reserve.
[8]	RW	phy2_rg_en_cmos	CMOS mode enabled. 0: Disable CMOS mode of PHY; 1: Enable CMOS mode of PHY.
[7:5]	RO	reserved	reserve.

[4] RW	phy2_rg_en_clk		Clock Lane is enabled. 0: Disable Clock Lane; 1: Enable Clock Lane.
[3:0] RW	phy2_rg_en_d		Data Lane enabled. 0: Disable the corresponding Data Lane; 1: Enable the corresponding Data Lane.

PHY_SKEW_LINK2

PHY_SKEW_LINK2 is the Link2 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0404	PHY_SKEW_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

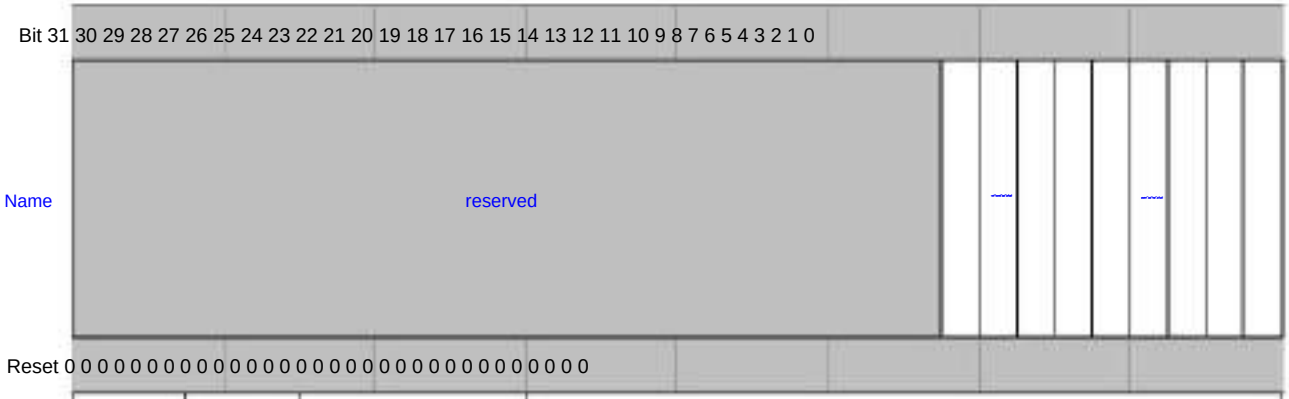
Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:16]	RW	phy2_d3_skew	Timing delay adjustment for Data lane 3. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[15]	RO	reserved	reserve.
[14:12]	RW	phy2_d2_skew	Timing delay adjustment for Data lane 2. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[11]	RO	reserved	reserve.
[10:8]	RW	phy2_d1_skew	Timing delay adjustment for Data lane 1. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[7]	RO	reserved	reserve.
[6:4]	RW	phy2_d0_skew	Timing delay adjustment for Data lane 0. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.
[3]	RO	reserved	reserve.

[2:0] RW	phy2_clk_skew		Timing delay adjustment of Clock Lane. Every time the value of this register is increased by 1, the phase will be delayed by about 62.5ps.

PHY_EN_LINK2

PHY_EN_LINK2 is Link2 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0408	PHY_EN_LINK2	0x0000_0000



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
resistor; [8]	RW	phy2_clk_term_en	Clock Lane Termination Impedance Enable. 0: Turn off the internal matching 1: Turn on the internal matching resistor.
[7]	RW	phy2_d3_term_en	Data lane3 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[6]	RW	phy2_d2_term_en	Data lane2 termination impedance enable. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[5]	RW	phy2_d1_term_en	Termination impedance enable for Data lane1. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.
[4]	RW	phy2_d0_term_en	Termination impedance enable for Data lane0. 0: Turn off the internal matching resistor; 1: Turn on the internal matching resistor.

[3] RW	phy2_da_d3_valid		Data lane3 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.
mode off; [2] RW	phy2_da_d2_valid		Data lane2 high-speed mode enable. 0: high speed 1: High speed mode enabled.
[1] RW	phy2_da_d1_valid		Data lane1 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.
[0] RW	phy2_da_d0_valid		Data lane0 high-speed mode enable. 0: high speed mode off; 1: High speed mode enabled.

PHY_DATA_LINK2

PHY_DATA_LINK2 is the output parallel data register of Link2 PHY.

Offset Address	Register Name	Total Reset Value
0x0418	PHY_DATA_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy2_data3_mipi	phy2_data2_mipi	phy2_data1_mipi	phy2_data0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_data3_mipi	Data Lane3 received data.
[23:16]	RO	phy2_data2_mipi	Data Lane2 received data.
[15:8]	RO	phy2_data1_mipi	Data Lane1 received data.
[7:0]	RO	phy2_data0_mipi	Data Lane0 received data.

PHY_PH_MIPI_LINK2

PHY_PH_MIPI_LINK2 is Link2 MIPI packet header register.

Offset Address	Register Name	Total Reset Value
0x041C	PHY_PH_MIPI_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy2_ph3_mipi	phy2_ph2_mipi	phy2_ph1_mipi	phy2_ph0_mipi
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_ph3_mipi	Data packet header received by Data Lane3.
[23:16]	RO	phy2_ph2_mipi	Data packet header received by Data Lane2.
[15:8]	RO	phy2_ph1_mipi	Data packet header received by Data Lane1.
[7:0]	RO	phy2_ph0_mipi	Data Lane0 Received packet header.

PHY_DATA_MIPI_LINK2

PHY_DATA_MIPI_LINK2 is Link2 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0420	PHY_DATA_MIPI_LINK2	0x0000_0000

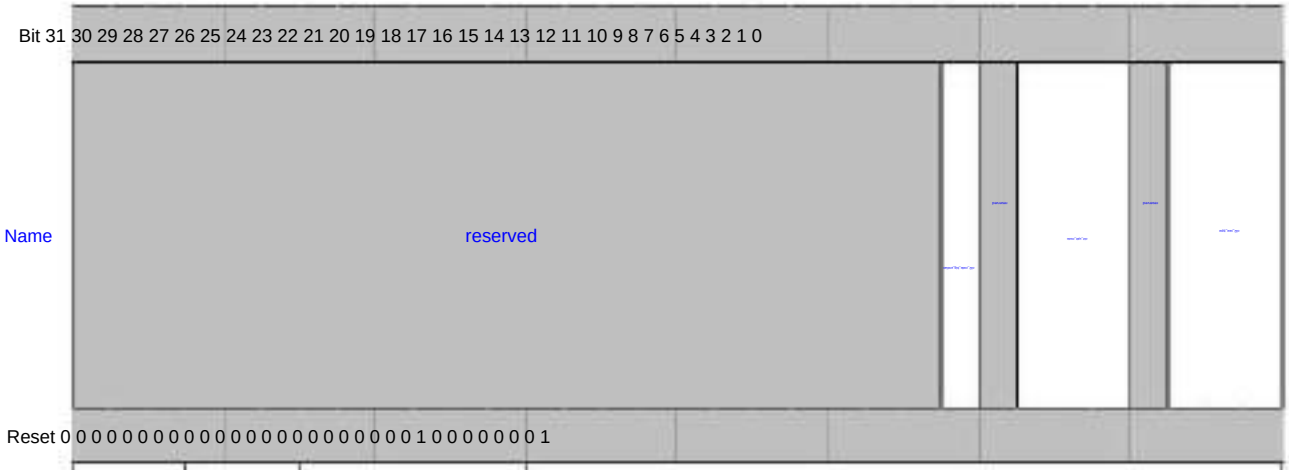
Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	phy2_data3_mipi_hs	phy2_data2_mipi_hs	phy2_data1_mipi_hs	phy2_data0_mipi_hs
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_data3_mipi_hs	Data Lane3 MIPI format data.
[23:16]	RO	phy2_data2_mipi_hs	Data Lane2 MIPI format data.
[15:8]	RO	phy2_data1_mipi_hs	Data Lane1 MIPI format data.
[7:0]	RO	phy2_data0_mipi_hs	Data Lane0 MIPI formatted data.

PHY_SYNC_DCT_LINK2

PHY_SYNC_DCT_LINK2 is the synchronous header detection control register of Link2 PHY LVDS mode.

Offset Address	Register Name	Total Reset Value
0x0424	PHY_SYNC_DCT_LINK2	0x0000_0101



Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	cil2_code_big_endian	In LVDS/HiSPi mode, the serial bit transmission order of the transmitted RAW data synchronization code (sync_code). 0: LSB, the lower bit is transmitted first, and the actually received synchronization code (sync_code) serial number data sequence is bit0, bit1, ... bit11; 1: MSB, the high bit is transmitted first, and the serial data sequence of the actually received synchronization code (sync_code) is bit11, bit10, ... bit0.
[7]	RO	reserved	reserve.
[6:4]	RW	cil2_split_mode	LVDS/HiSPi Sync Code transfer type. 000: Per Lane mode; Other: reserved.
[3]	RO	reserved	reserve.
[2:0]	RW	cil2_raw_type	In LVDS/HiSPi mode, the RAW data type transmitted. 001ÿRaw 8bitÿ 010ÿRaw 10bitÿ 011ÿRaw 12bitÿ 100ÿRaw 14bitÿ 101ÿRaw 16bitÿ Other: reserved.

PHY_SYNC_CODE0_LINK2

PHY_SYNC_CODE0_LINK2 is Link2 PHY LVDS mode sync header register 0.

Offset Address	Register Name	Total Reset Value
0x0430	PHY_SYNC_CODE0_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil2_sof1_word4_0	cil2_sof0_word4_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW	cil2_sof1_word4_0 Lane0 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil2_sof0_word4_0 Lane0 frame start synchronization code (N Frame).

PHY_SYNC_CODE1_LINK2

PHY_SYNC_CODE1_LINK2 is Link2 PHY LVDS mode sync header register 1.

Offset Address	Register Name	Total Reset Value
0x0434	PHY_SYNC_CODE1_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil2_sof1_word4_1	cil2_sof0_word4_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW	cil2_sof1_word4_1 Lane1 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil2_sof0_word4_1 Lane1 frame start synchronization code (N Frame).

PHY_SYNC_CODE2_LINK2

PHY_SYNC_CODE2_LINK2 is Link2 PHY LVDS mode sync header register 2.

Offset Address	Register Name	Total Reset Value
0x0438	PHY_SYNC_CODE2_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil2_sof1_word4_2	cil2_sof0_word4_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW	cil2_sof1_word4_2 Lane2 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil2_sof0_word4_2 Lane2 frame start synchronization code (N Frame).

PHY_SYNC_CODE3_LINK2

PHY_SYNC_CODE3_LINK2 is Link2 PHY LVDS mode sync header register 3.

Offset Address	Register Name	Total Reset Value
0x043C	PHY_SYNC_CODE3_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cil2_sof1_word4_3	cil2_sof0_word4_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	cil2_sof1_word4_3	Lane3 frame start synchronization code (N+1 Frame).
[15:0]	RW	cil2_sof0_word4_3	Lane3 frame start synchronization code (N Frame).

MIPI_CIL_INT_RAW_LINK2

MIPI_CIL_INT_RAW_LINK2 is the Link2 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x05F0	MIPI_CIL_INT_RAW_LINK2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

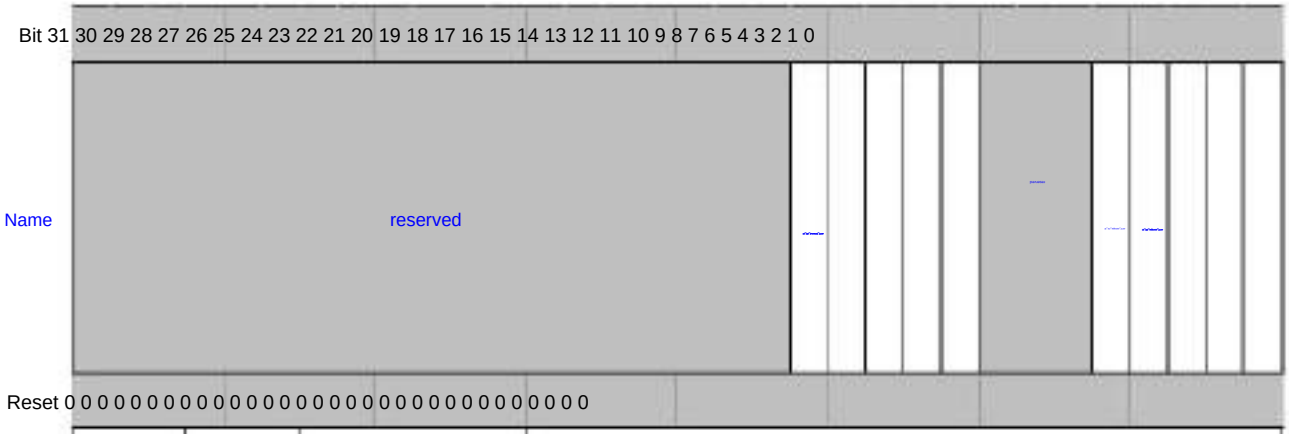
Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	WC	err2_timeout_ck_ra 0: In	Clock Lane FSM timeout raw interrupt status. no raw interrupt; 1: There is a raw interrupt.

[11] WC		err2_timeout_d3_ra In	Data Lane3 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[10] WC		err2_timeout_d2_ra In	Data Lane2 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[9] WC		err2_timeout_d1_ra In	Data Lane1 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[8] WC		err2_timeout_d0_ra In	Data Lane0 FSM timeout raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[7:5] RO		reserved	reserve.
[4] WC		status. In err2_escape_ck_ra	Clock Lane escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[3] WC		status. In err2_escape_d3_ra	Data Lane3 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[2] WC		status. In err2_escape_d2_ra	Data Lane2 escape sequence raw interrupt 0: no original interrupt; 1: original interrupt.
[1] WC		status. In err2_escape_d1_ra	Data Lane1 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[0] WC		status. In err2_escape_d0_ra	Data Lane0 escape sequence raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.

MIPI_CIL_INT_LINK2

MIPI_CIL_INT_LINK2 is the Link2 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x05F4	MIPI_CIL_INT_LINK2	0x0000_0000



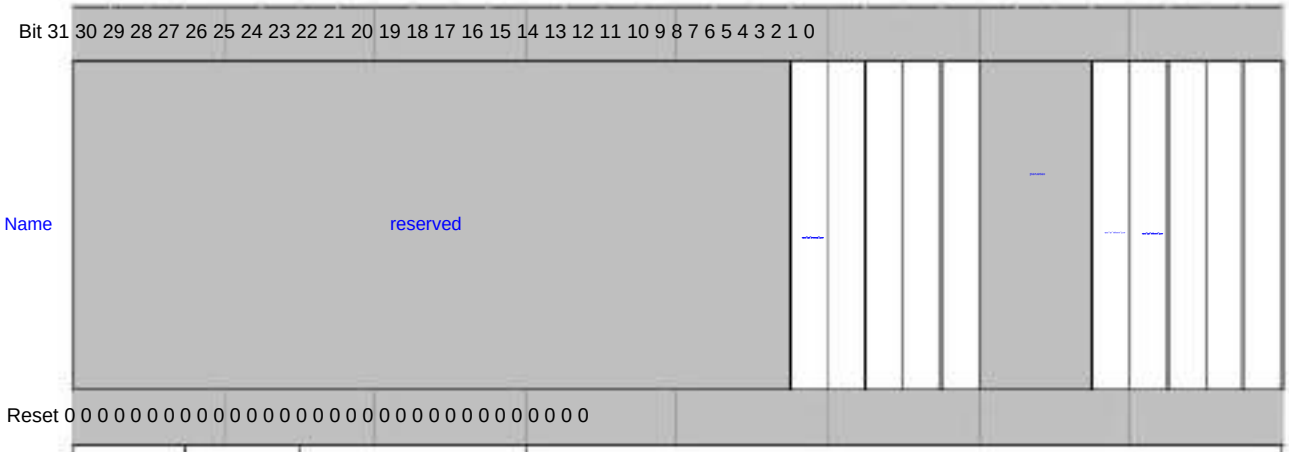
Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RO		err2_timeout_ck_st	Clock Lane FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[11] RO		err2_timeout_d3_st	Data Lane3 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[10] RO		err2_timeout_d2_st	Data Lane2 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[9]	RO	err2_timeout_d1_st	Data Lane1 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[8]	RO	err2_timeout_d0_st	Data Lane0 FSM timeout interrupt status. 0: no interrupt; 1: There is an interrupt.
[7:5] RO		reserved	reserve.
[4]	RO	err2_escape_ck_st	Clock Lane escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	err2_escape_d3_st	Data Lane3 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.

[2]	RO	err2_escape_d2_st	Data Lane2 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[1]	RO	err2_escape_d1_st	Data Lane1 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	err2_escape_d0_st	Data Lane0 escape sequence interrupt status. 0: no interrupt; 1: There is an interrupt.

MIPI_CIL_INT_MSK_LINK2

MIPI_CIL_INT_MSK_LINK2 is the Link2 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x05F8	MIPI_CIL_INT_MSK_LINK2	0x0000_0000



Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RW		err2_timeout_ck_m 0: mask	Clock Lane FSM timeout interrupt status enable. interrupt; sk 1: Interrupts are enabled.
[11] RW		err2_timeout_d3_m 0: mask	Data Lane3 FSM timeout interrupt status enable. interrupt; sk 1: Interrupts are enabled.
[10] RW		err2_timeout_d2_m 0: mask interrupt.	Data Lane2 FSM timeout interrupt status enable. interrupt; sk 1: enable

[9] RW		err2_timeout_d1_m 0:	Data Lane1 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[8] RW		err2_timeout_d0_m 0:	Data Lane0 FSM timeout interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[7:5] RO		reserved	reserve.
[4] RW		enable. interrupt; k err2_escape_ck_	Clock Lane escape sequence interrupt status ms 0: mask 1: Interrupts are enabled.
[3] RW		enable. interrupt; k err2_escape_d3_	Data Lane3 escape sequence interrupt status ms 0: mask 1: Interrupts are enabled.
[2] RW		enable. interrupt; k err2_escape_d2_	Data Lane2 escape sequence interrupt status ms 0: mask 1: Interrupts are enabled.
[1] RW		enable. interrupt; k err2_escape_d1_	Data Lane1 escape sequence interrupt status ms 0: mask 1: Interrupts are enabled.
[0] RW		enable. err2_escape_d0_ interrupt; k 1: enable interrupt.	Data Lane0 escape sequence interrupt status ms 0: mask

PHY_CHN_CTRL

PHY_CHN_CTRL is the PHY channel control selection register.

Offset Address	Register Name	Total Reset Value
0x0800	PHY_CHN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	phy2_en	PHY2 enable control. 0: PHY2 is not enabled; 1: PHY2 operation is enabled.
[1]	RW	phy1_en	PHY1 enable control. 0: PHY1 is not enabled; 1: PHY1 operation is enabled.
[0]	RW	phy0_en	PHY0 enable control. 0: PHY0 is not enabled; 1: PHY0 operation is enabled.

PHY_LP_SELECT

PHY_LP_SELECT is the PHY1 LP mode signal selection register.

Offset Address	Register Name	Total Reset Value
0x0804	PHY_LP_SELECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x0804	PHY_LP_SELECT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[0]	RW	phy1_lp_sel	PHY1 LP mode signal selection. 0: PHY1 LP signal comes from PHY1; 1: PHY1 LP signal comes from PHY0.

MIPI_MEM_CTRL

MIPI_MEM_CTRL is the MEMORY control register.

Offset Address	Register Name	Total Reset Value
0x080C	MIPI_MEM_CTRL	0x0000_0331

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 1 0 0 0 1

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	mem_ck_gt	MIPI memory clock gating configuration register. 0: disable clock gating; 1: Enable clock gating, when MEMORY is not read or written, the clock of MEMORY port will not be reversed.
[11:0]	RO	reserved	reserve.

LANE_EN

LANE_EN is the LANE_EN enable register.

Offset Address	Register Name	Total Reset Value
0x0810	LANE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11]	RW	lane11_en	Lane11 work is enabled. 0: disable; 1: enable.
[10]	RW	lane10_en	Lane10 work is enabled. 0: Disable; 1: Enable.
[9]	RW	lane9_en	Lane9 work is enabled. 0: disable; 1: enable.
[8]	RW	lane8_en	Lane8 work is enabled. 0: disable; 1: enable.
[7]	RW	lane7_en	Lane7 work is enabled. 0: disable; 1: enable.
[6]	RW	lane6_en	Lane6 work is enabled. 0: disable; 1: enable.
[5]	RW	lane5_en	Lane5 work is enabled. 0: disable; 1: enable.

[4] RW	lane4_en		Lane4 work is enabled. 0: disable; 1: enable.
[3] RW	lane3_en		Lane3 work is enabled. 0: disable; 1: enable.
[2] RW	lane2_en		Lane2 work is enabled. 0: disable; 1: enable.
[1] RW	lane1_en		Lane1 work is enabled. 0: disable; 1: enable.
[0] RW	lane0_en		Lane0 work is enabled. 0: disable; 1: enable.

MIPI_PHYCFG_MODE

MIPI_PHYCFG_MODE is the MIPI PHY configuration mode register.

Offset Address	Register Name	Total Reset Value
0x0814	MIPI_PHYCFG_MODE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

[2:0] RW		mipi0_phycfg_mod It is	MIPI0 PHY configuration mode. 000: PHY configuration is controlled by PHYCFG_EN and FSM; 001: PHY configuration is controlled by PHYCFG_EN; 010: PHY configuration is directly controlled by register value; PHY configuration is controlled by register value and FSM. 100: PHY configuration is controlled by PHYCRG_EN and FSM, and clock channel enable is controlled by PHYCFG_EN. Other: reserved.

MIPI_PHYCFG_EN

MIPI_PHYCFG_EN is the MIPI PHY configuration enable register.

Offset Address	Register Name	Total Reset Value
0x0818	MIPI_PHYCFG_EN	0x0000_0000

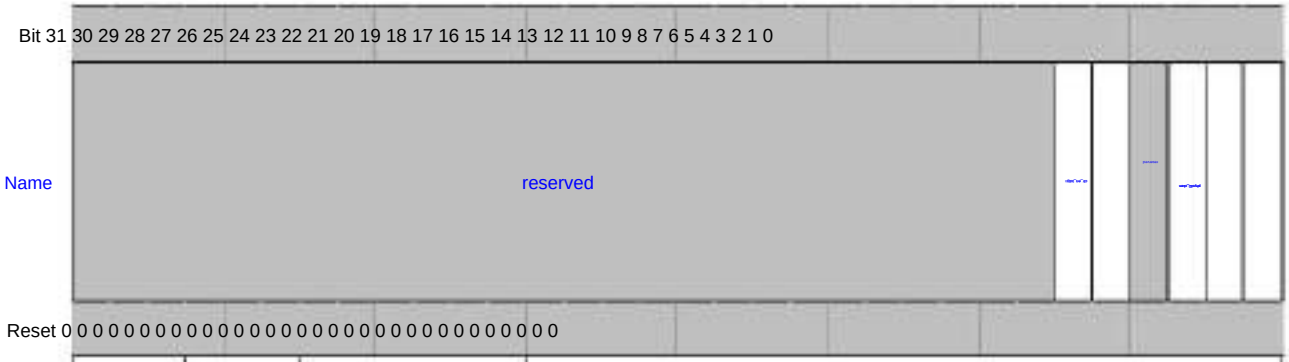
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1] RO		reserved	reserve.
[0] WO	chn0_phycfg_en		MIPI0 PHY configuration enable register. 0: Disable PHY configuration; 1: Enable configuration of the PHY.

MIPI_CIL_CTRL

MIPI_CIL_CTRL is the MIPI CIL control register.

Offset Address	Register Name	Total Reset Value
0x081C	MIPI_CIL_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	clr_en_align	Force assertion control for the LVDS PRE SYNC block. 0: Disable ALIGN set request; 1: Enable ALIGN set request;
[4]	RW	clr_en_lvds	Force assertion control for the LVDS PRE SYNC block. 0: Disable the set request of LVDS CTRL; 1: Enable the set request of LVDS CTRL;
[3]	RO	reserved	reserve.
[2]	RW	phycil2_cken	PHYCIL2 clock gating. 0: turn off the clock; 1: Turn on the clock.
[1]	RW	phycil1_cken	PHYCIL1 clock gating. 0: turn off the clock; 1: Turn on the clock.
[0]	RW	phycil0_cken	PHYCIL0 clock gating. 0: turn off the clock; 1: Turn on the clock.

MIPI_SRST_CFG

MIPI_SRST_CFG is MIPI CORE soft reset register.

Offset Address	Register Name	Total Reset Value
0x0820	MIPI_SRST_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	mipi_srst_aux	MIPI CORE soft reset request. 0: no reset; 1: A soft reset is requested. This reset signal does not affect the value of the register.

MIPI_CHN0_INT_RAW

MIPI_CHN0_INT_RAW is the MIPI channel 0 raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF0	MIPI_CHN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	WC	int_data_align_raw	MIPI ALIGN raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

[5] WC	int_mipi_ctrl_raw		MIPI CTRL raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[4] WC	int_mipi_csi_raw		MIPI CSI2 raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[3] WC	int_lvds_ctrl_raw		LVDS CTRL raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[2] WC	int_phycil2_raw		PHYCIL2 Raw Interrupt Status. 0: no original interrupt; 1: There is a raw interrupt.
[1] WC	int_phycil1_raw		PHYCIL1 Raw Interrupt Status. 0: no original interrupt; 1: There is a raw interrupt.
[0] WC	int_phycil0_raw		PHYCIL0 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

MIPI_CHN0_INT

MIPI_CHN0_INT is MIPI channel 0 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF4	MIPI_CHN0_INT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.

[6]	RO	int_data_align_st	MIPI ALIGN interrupt status. 0: no interrupt; 1: There is an interrupt.
[5]	RO	int_mipi_ctrl_st	MIPI CTRL interrupt status. 0: no interrupt; 1: There is an interrupt.
[4]	RO	int_mipi_csi_st	MIPI CSI2 interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	int_lvds_ctrl_st	LVDS CTRL interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	int_phycil2_st	PHYCIL2 interrupt status. 0: no interrupt; 1: There is an interrupt.
[1]	RO	int_phycil1_st	PHYCIL1 interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	int_phycil0_st	PHYCIL0 interrupt status. 0: no interrupt; 1: There is an interrupt.

MIPI_CHN0_INT_MSK

MIPI_CHN0_INT_MSK is MIPI channel 0 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0EF8	MIPI_CHN0_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	int_data_align_msk	MIPI ALIGN interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[5]	RW	int_mipi_ctrl_msk	MIPI CTRL interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[4]	RW	int_mipi_csi_msk	MIPI CSI2 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[3]	RW	int_lvds_ctrl_msk	LVDS CTRL interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	int_phycil2_msk	PHYCIL2 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[1]	RW	int_phycil1_msk	PHYCIL1 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[0]	RW	int_phycil0_msk	PHYCIL0 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.

MIPI0_LANES_NUM

MIPI0_LANES_NUM is the MIPI0 data lane number enable register.

Offset Address	Register Name	Total Reset Value
0x1004	MIPI0_LANES_NUM	0x0000_0003

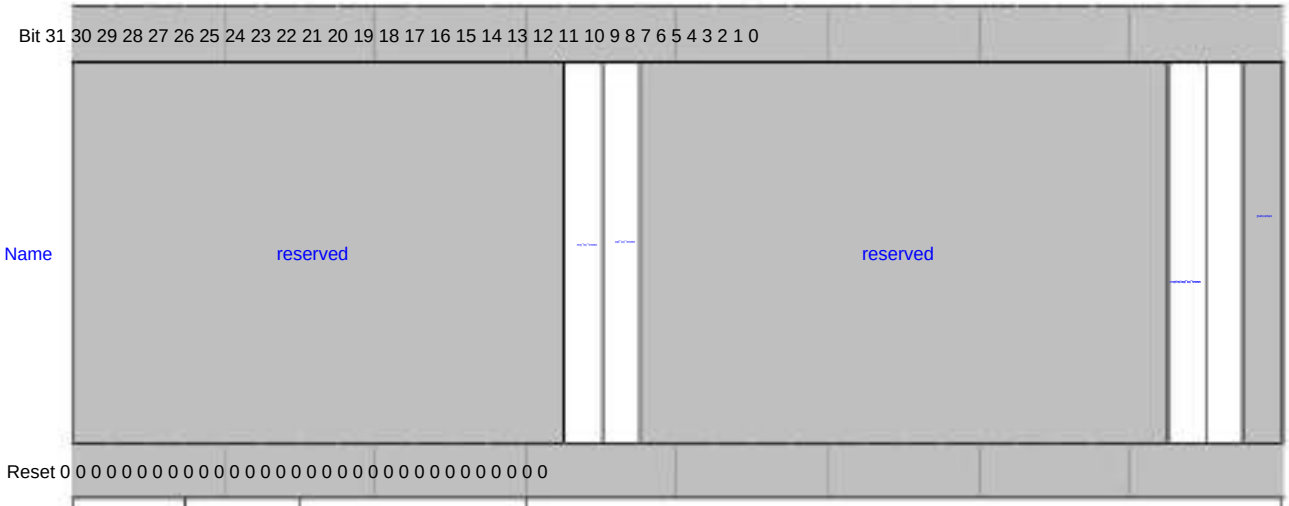
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	lane_num	Number of data channels enabled. 000: The number of data channels is 1; 001: The number of data channels is 2; 010: The number of data channels is 3; 011: The number of data channels is 4. 100: the number of data channels is 5; 101: the number of data channels is 6; 110: the number of data channels is 7; 111: The number of data channels is 8.

MIPI0_MAIN_INT_ST

MIPI0_MAIN_INT_ST is MIPI0 master interrupt status register.

Offset Address	Register Name	Total Reset Value
0x100C	MIPI0_MAIN_INT_ST	0x0000_0000



Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	RC	status_int_line	Line interrupt status register, if any bit of the register MIPI0_LINE_INTR_ST is set to 1, this bit is set to 1, and read to 0. To clear the reported interrupt, this bit and MIPI0_LINE_INTR_ST should be cleared.
[17]	RC	status_int_pkt	Packet interrupt status register, if any bit of the register MIPI0_PKT_INTR2_ST is set to 1, then this bit is set to 1, read as 0. To clear the reported interrupt, this bit and MIPI0_PKT_INTR2_ST should be cleared.
[16:3]	RO	reserved	reserve.
[2]	RC	status_int_frame_fa bit 1, MIPI0_FRAME_INTR_ST.	Frame interrupt status register, if the register MIPI0_FRAME_INTR_ST has any then this bit is 1, read 0. To clear the reported interrupt, tal should clear this bit and
[1]	RC	MIPI0_PKT_INTR_ST	Packet interrupt status register, if any bit of register MIPI0_PKT_INTR_ST is 1, then this bit is 1, read 0. To clear the reported interrupt, the bit status_int_pkt_fatal and should be cleared.
[0]	RO	reserved	reserve.

MIPI0_DI_1

MIPI0_DI_1 is the MIPI0 controller Data ID 1 register.

Offset Address	Register Name	Total Reset Value
0x1010	MIPI0_DI_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	di3_vc	Virtual channel number of Data ID3.
[29:24]	RW	di3_dt	Data type of Data ID3. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[23:22]	RW	di2_vc	Virtual channel number of Data ID2.
[21:16]	RW	di2_dt	Data type of Data ID2. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[15:14]	RW	di1_vc	Virtual channel number of Data ID1.
[13:8]	RW	di1_dt	Data type of Data ID1. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[7:6]	RW	di0_vc	Virtual channel number of Data ID0.

[5:0] RW	di0_dt		Data type of Data ID0. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.

MIPI0_DI_2

MIPI0_DI_2 is the MIPI0 controller Data ID 2 register.

Offset Address	Register Name	Total Reset Value
0x1014	MIPI0_DI_2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	di7_vc / di7_dt	di6_vc / di6_dt	di5_vc / di5_dt	di4_vc / di4_dt
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:30]	RW	di7_vc	Virtual channel number of Data ID7.
[29:24]	RW	di7_dt	Data type of Data ID7. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[23:22]	RW	di6_vc	Virtual channel number of Data ID6.
[21:16]	RW	di6_dt	Data type of Data ID6. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[15:14]	RW	di5_vc	Virtual channel number of Data ID5.

[13:8] RW	di5_dt		The data type of Data ID5. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.
[7:6] RW	di4_vc		Virtual channel number of Data ID4.
[5:0] RW	di4_dt		Data type of Data ID4. 0x2AÿRAW8ÿ 0x2BÿRAW10ÿ 0x2CÿRAW12ÿ 0x2DÿRAW14ÿ Other: reserved.

MIPI0_PKT_INTR_ST

MIPI0_PKT_INTR_ST is MIPI0 packet interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1060	MIPI0_PKT_INTR_ST	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RC	err_ecc_double	Header has at least 2 errors, and ECC cannot correct errors. Read to clear. 0: no ECC error; 1: There is an ECC error.
[15:4]	RO	reserved	reserve.

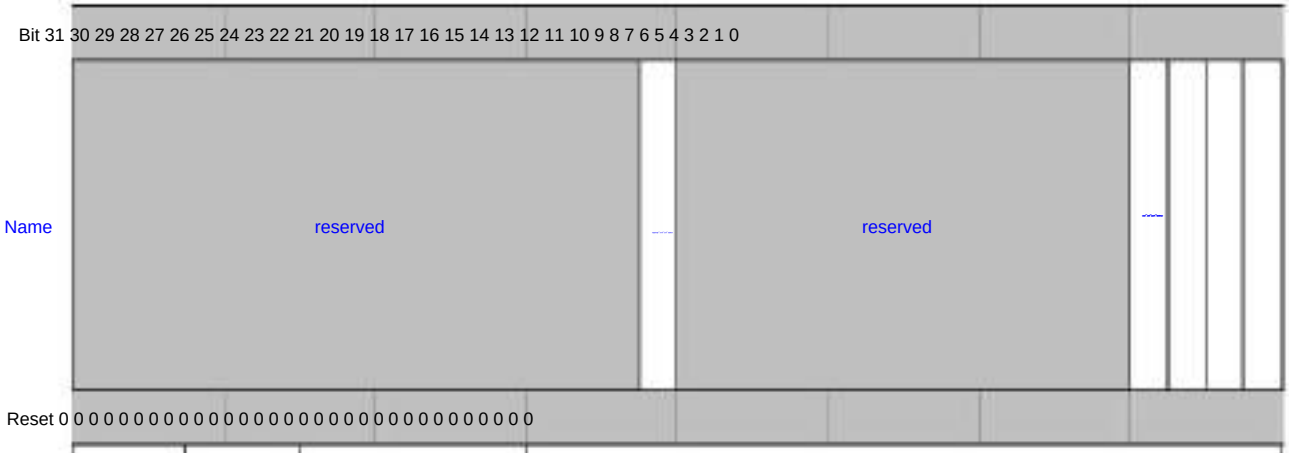
Offset Address	Register Name	Total Reset Value
0x1060	MIPI0_PKT_INTR_ST	0x0000_0000

[3]	RC	vc3_err_crc	VC3 data CRC error. Read to clear. 0: VC3 data has no CRC error; 1: VC3 data has CRC error.
[2]	RC	vc2_err_crc	VC2 data CRC error. Read to clear. 0: VC2 data has no CRC error; 1: VC2 data has CRC error.
[1]	RC	vc1_err_crc	VC1 data CRC error. Read to clear. 0: VC1 data has no CRC error; 1: VC1 data has CRC error.
[0]	RC	vc0_err_crc	VC0 data CRC error. Read to clear. 0: VC0 data has no CRC error; 1: VC0 data has CRC error.

MIPI0_PKT_INTR_MSK

MIPI0_PKT_INTR_MSK is MIPI0 packet interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1064	MIPI0_PKT_INTR_MSK	0x0000_0000



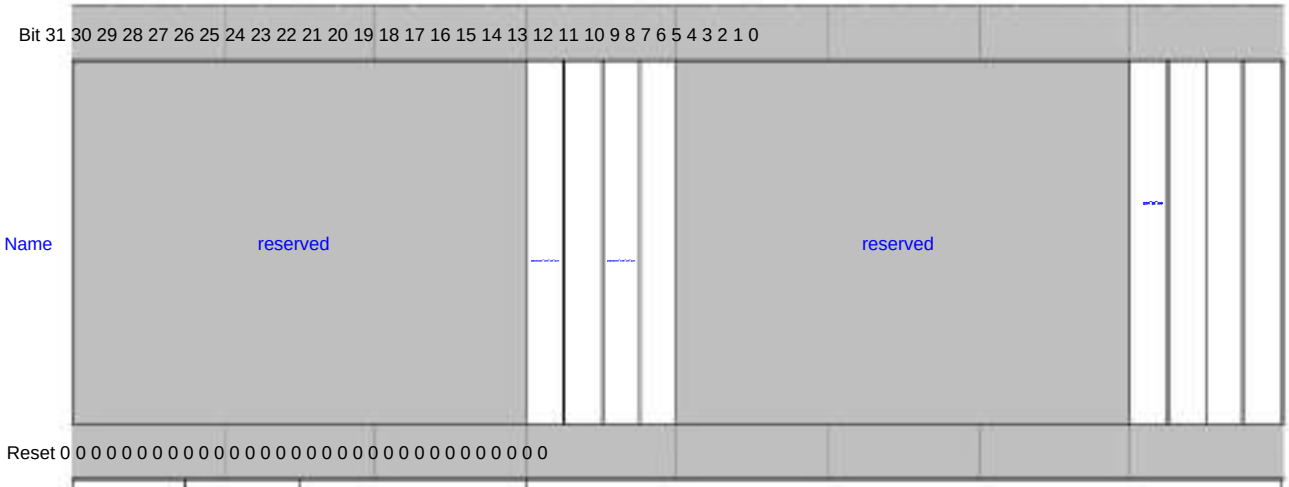
Bits	Access Name		Description
[31:17] RO		reserved	reserve.
[16] RW		mask_err_ecc_doub 0:	err_ecc_double Interrupt mask register. mask interrupt; le 1: Interrupts are enabled.
[15:4] RO		reserved	reserve.

[3]	RW	mask_vc3_err_crc	vc3_err_crc interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	mask_vc2_err_crc	vc2_err_crc interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[1]	RW	mask_vc1_err_crc	vc1_err_crc interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[0]	RW	mask_vc0_err_crc	vc0_err_crc Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.

MIPI0_PKT_INTR2_ST

MIPI0_PKT_INTR2_ST is MIPI0 packet interrupt status register 2.

Offset Address	Register Name	Total Reset Value
0x1070	MIPI0_PKT_INTR2_ST	0x0000_0000



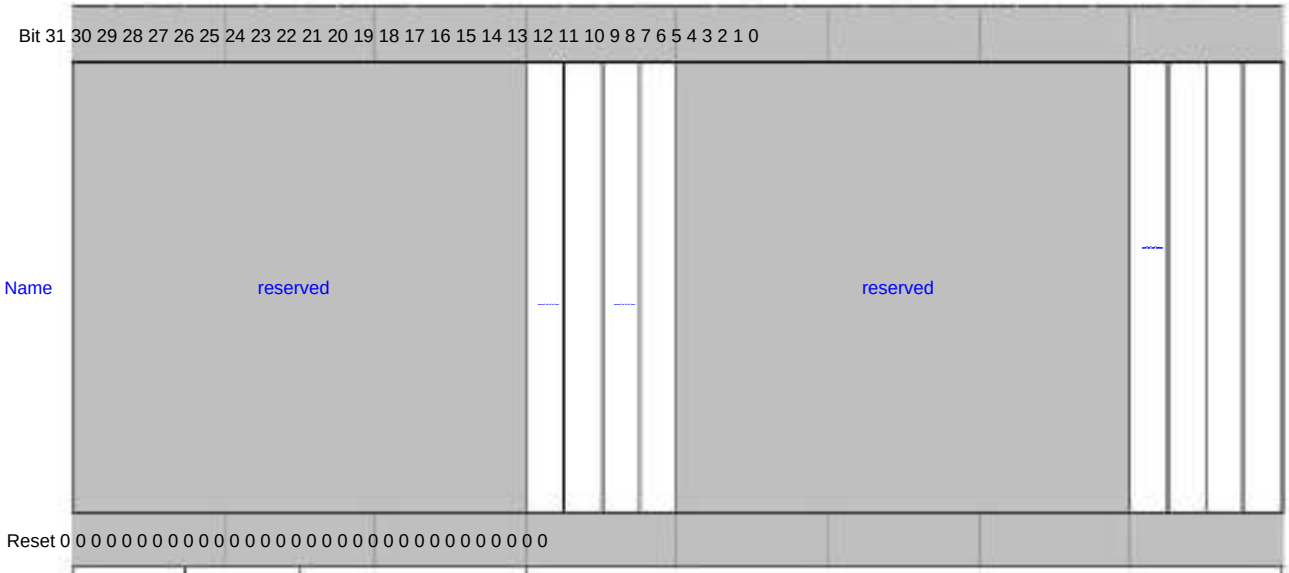
Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RC	clear. vc3_err_ecc_corrected	VC3 channel Header error, ECC has been corrected. Read to 0: VC3 channel Header has no ECC error; 1: VC3 channel Header has ECC error and has been corrected.

[18] RC		vc2_err_ecc_correc 0:	VC2 channel Header error, ECC has been corrected. Read to clear. VC2 channel Header has no ECC error; ted 1: VC2 channel Header has ECC error and has been corrected.
[17] RC		vc1_err_ecc_correc 0:	VC1 channel Header error, ECC has been corrected. Read to clear. VC1 channel Header has no ECC error; ted 1: VC1 channel Header has ECC error and has been corrected.
[16] RC		vc0_err_ecc_correc 0:	VC0 channel Header error, ECC has been corrected. Read to clear. VC0 channel Header has no ECC error; ted 1: VC0 channel Header has ECC error and has been corrected.
[15:4] RO		reserved	reserve.
[3]	RC	err_id_vc3	VC3 channel data type. Read to clear. 0: Supported data types; 1: Unsupported data type.
[2]	RC	err_id_vc2	VC2 channel data type. Read to clear. 0: Supported data types; 1: Unsupported data type.
[1]	RC	err_id_vc1	VC1 channel data type. Read to clear. 0: Supported data types; 1: Unsupported data type.
[0]	RC	err_id_vc0	VC0 channel data type. Read to clear. 0: supported data type; 1: unsupported data type.

MIPI0_PKT_INTR2_MSK

MIPI0_PKT_INTR2_MSK is MIPI0 packet interrupt mask register 2.

Offset Address	Register Name	Total Reset Value
0x1074	MIPI0_PKT_INTR2_MSK	0x0000_0000



Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RW	mask_vc3_err_ecc_corrected	vc3_err_ecc_corrected interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[18]	RW	mask_vc2_err_ecc_corrected	vc2_err_ecc_corrected interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[17]	RW	mask_vc1_err_ecc_corrected	vc1_err_ecc_corrected interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[16]	RW	mask_vc0_err_ecc_corrected	vc0_err_ecc_corrected interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[15:4]	RO	reserved	reserve.
[3]	RW	mask_err_id_vc3	err_id_vc3 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	mask_err_id_vc2	err_id_vc2 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.

[1] RW	mask_err_id_vc1		err_id_vc1 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[0] RW	mask_err_id_vc0		err_id_vc0 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.

MIPI0_FRAME_INTR_ST

MIPI0_FRAME_INTR_ST is MIPI0 frame interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1080	MIPI0_FRAME_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

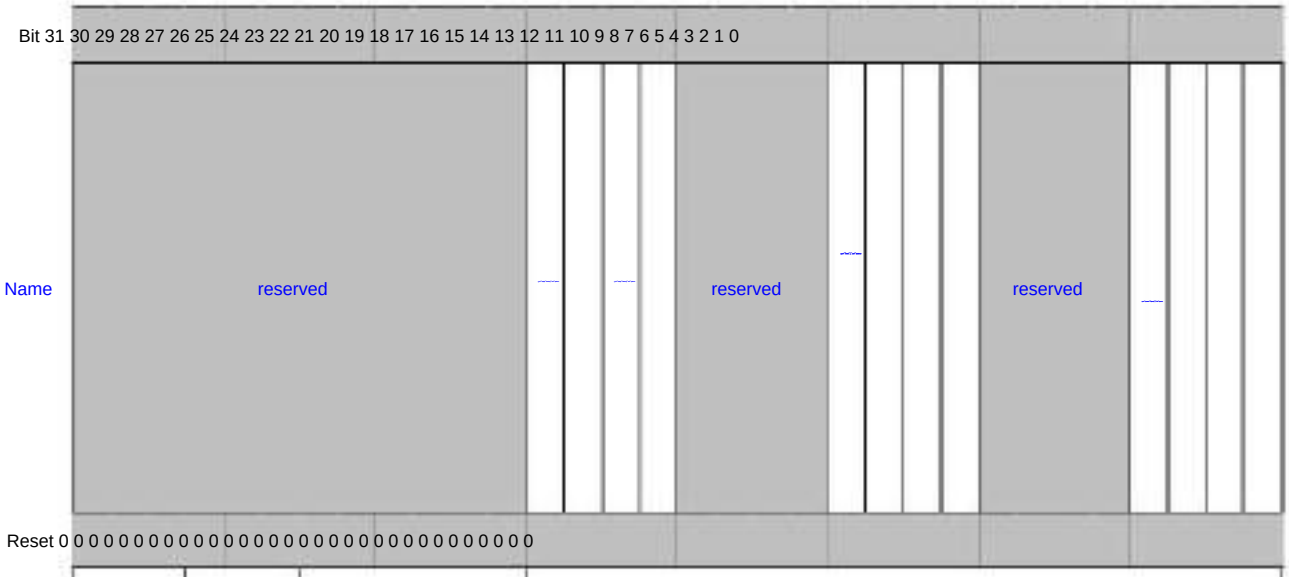
Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RC	err_frame_data_vc3	Read to clear. In the last frame of data, the VC3 channel data has at least one CRC error. 0: no CRC error; 1: There is a CRC error.
[18]	RC	err_frame_data_vc2	Read to clear. In the last frame of data, the VC2 channel data has at least one CRC error. 0: no CRC error; 1: There is a CRC error.

[17] RC		clear. err_frame_data_vc1	In the last frame of data, the VC1 channel data has at least one CRC error. Read to 0: no CRC error; 1: There is a CRC error.
[16] RC		clear. err_frame_data_vc0	In the last frame of data, the VC0 channel data has at least one CRC error. Read to 0: no CRC error; 1: There is a CRC error.
[15:12] RO		reserved	reserve.
[11] RC		err_f_seq_vc3	The frame sequence of VC3 is wrong. Read to clear. 0: The frame sequence is correct; 1: The frame sequence is wrong.
[10] RC		err_f_seq_vc2	The frame sequence of VC2 is wrong. Read to clear. 0: The frame sequence is correct; 1: The frame sequence is wrong.
[9]	RC	err_f_seq_vc1	The frame sequence of VC1 is wrong. Read to clear. 0: The frame sequence is correct; 1: The frame sequence is wrong.
[8]	RC	err_f_seq_vc0	The frame sequence of VC0 is wrong. Read to clear. 0: The frame sequence is correct; 1: The frame sequence is wrong.
[7:4] RO		reserved	reserve.
[3]	RC	err_f_bndry_match	Frame start and frame end mismatch for VC3 channel. Read to clear. 0: frame start and frame end short packets match; _vc3 1: The frame start and frame end short packets do not match.
[2]	RC	err_f_bndry_match	Frame start and frame end mismatch for VC2 channel. Read to clear. 0: frame start and frame end short packets match; _vc2 1: The frame start and frame end short packets do not match.
[1]	RC	err_f_bndry_match	Frame start and frame end mismatch for VC1 channel. Read to clear. 0: frame start and frame end short packets match; _vc1 1: frame start and frame end short packets do not match.
[0]	RC	err_f_bndry_match	Frame start and frame end mismatch for VC0 channel. Read to clear. 0: frame start and frame end short packet match; _vc0 1: The frame start and frame end short packets do not match.

MIPI0_FRAME_INTR_MSK

MIPI0_FRAME_INTR_MSK is MIPI0 frame interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1084	MIPI0_FRAME_INTR_MSK	0x0000_0000



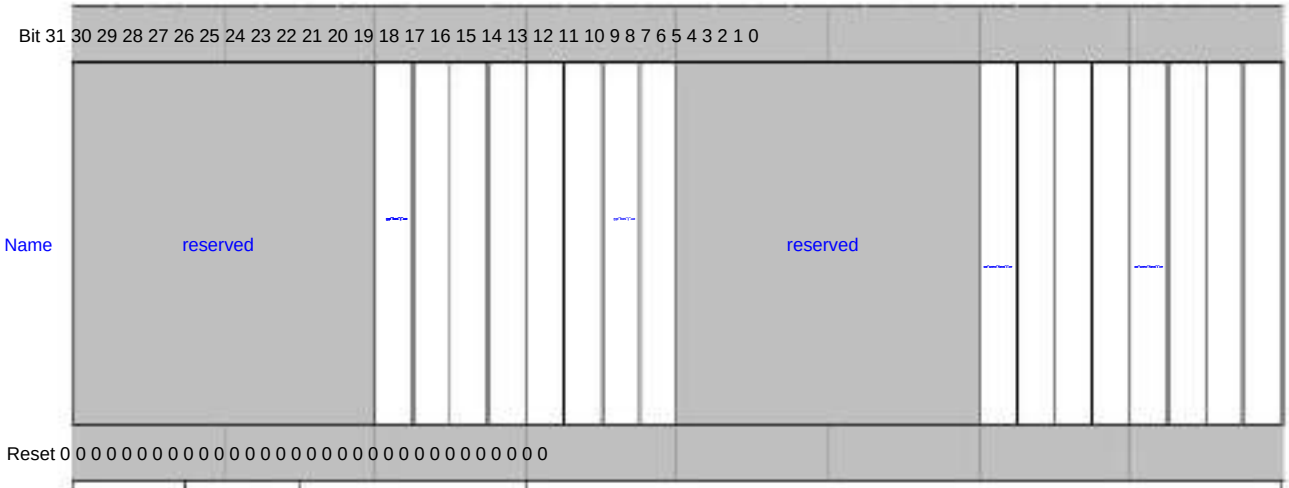
Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19]	RW	mask_err_frame_da ta_vc3	err_frame_data_vc3 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[18]	RW	mask_err_frame_da ta_vc2	err_frame_data_vc2 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[17]	RW	mask_err_frame_da ta_vc1	err_frame_data_vc1 Interrupt mask register. 0: mask interrupt; 1: enable interrupt.
[16]	RW	mask_err_frame_da ta_vc0	err_frame_data_vc0 Interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[15:12]	RO	reserved	reserve.
[11]	RW	mask_err_f_seq_vc 0:	err_f_seq_vc3 Interrupt mask register. mask interrupt; 3 1: Interrupts are enabled.

[10] RW		mask_err_f_seq_vc 0:	err_f_seq_vc2 Interrupt mask register. mask interrupt; 2 1: Interrupts are enabled.
[9] RW		mask_err_f_seq_vc 0:	err_f_seq_vc1 Interrupt mask register. mask interrupt; 1 1: Interrupts are enabled.
[8] RW		mask_err_f_seq_vc 0:	err_f_seq_vc0 Interrupt mask register. mask interrupt; 0 1: Interrupts are enabled.
[7:4] RO		reserved	reserve.
[3] RW		mask_err_f_bndry_ 0: match_vc3	err_f_bndry_match_vc3 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[2] RW		mask_err_f_bndry_ 0: match_vc2	err_f_bndry_match_vc2 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[1] RW		mask_err_f_bndry_ 0: match_vc1	err_f_bndry_match_vc1 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[0] RW		mask_err_f_bndry_ 0: match_vc0	err_f_bndry_match_vc0 Interrupt mask register. mask interrupt; 1: enable interrupt.

MIPI0_LINE_INTR_ST

MIPI0_LINE_INTR_ST is MIPI0 line interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1090	MIPI0_LINE_INTR_ST	0x0000_0000



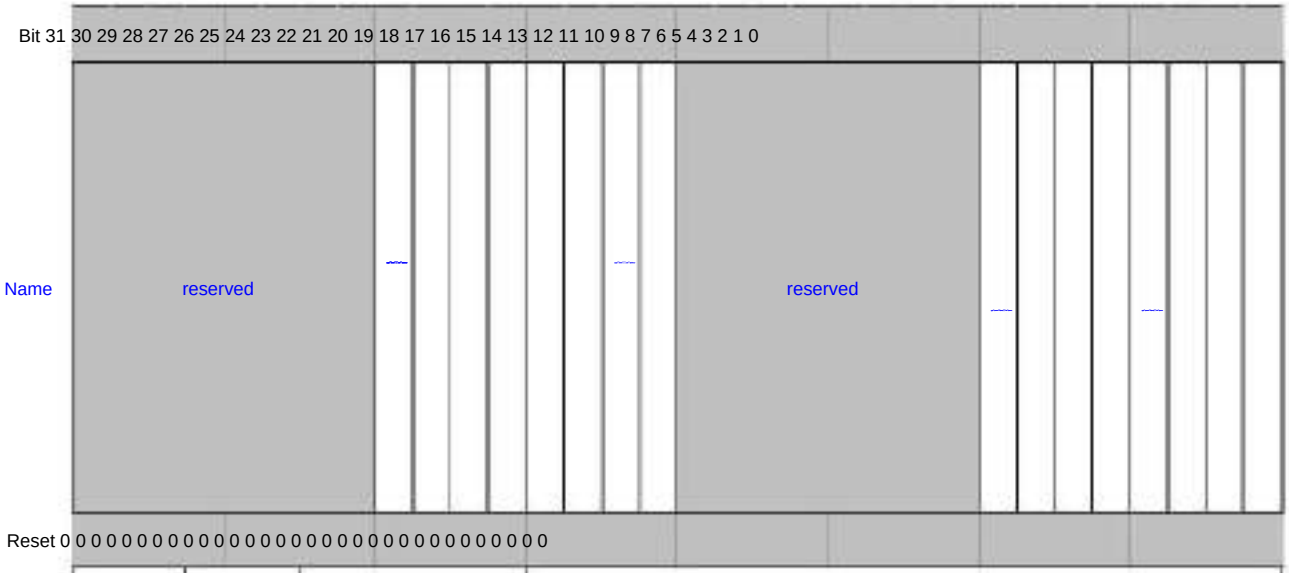
Bits	Access Name		Description
[31:24] RO		reserved	reserve.
[23] RC		err_l_seq_di7	VC7 and DT7 have wrong line order. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[22] RC		err_l_seq_di6	VC6 and DT6 have wrong line order. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[21] RC		err_l_seq_di5	VC5 and DT5 have wrong line order. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[20] RC		err_l_seq_di4	VC4 and DT4 line order is wrong. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[19] RC		err_l_seq_di3	VC3 and DT3 line order is wrong. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[18] RC		err_l_seq_di2	VC2 and DT2 line order error. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[17] RC		err_l_seq_di1	VC1 and DT1 line order error. Read to clear. 0: The line order is normal; 1: The line order is wrong.

[16] RC		err_l_seq_di0	VC0 and DT0 row order is wrong. Read to clear. 0: The line order is normal; 1: The line order is wrong.
[15:8] RO		reserved	reserve.
[7]	RC	err_l_bndry_match 0: line	VC7 and DT7 do not match line start and line end. Read to clear. start and line end short packet match; _di7 1: Line-start and line-end short packets do not match.
[6]	RC	err_l_bndry_match 0: line	VC6 and DT6 do not match line start and line end. Read to clear. start and line end short packet match; _di6 1: Line-start and line-end short packets do not match.
[5]	RC	err_l_bndry_match 0: line	VC5 and DT5 do not match line start and line end. Read to clear. start and line end short packet match; _di5 1: Line-start and line-end short packets do not match.
[4]	RC	err_l_bndry_match 0: line	VC4 and DT4 do not match line start and line end. Read to clear. start and line end short packet match; _di4 1: Line-start and line-end short packets do not match.
[3]	RC	err_l_bndry_match 0: line	VC3 and DT3 do not match line start and line end. Read to clear. start and line end short packet match; _di3 1: Line-start and line-end short packets do not match.
[2]	RC	err_l_bndry_match 0: the line	VC2 and DT2 have mismatched line start and line end. Read to clear. start and line end short packets match; _di2 1: the line start and line end short packets do not match.
[1]	RC	err_l_bndry_match 0: line	Line start and line end mismatch between VC1 and DT1. Read to clear. start and line end short packet match; _di1 1: Line-start and line-end short packets do not match.
[0]	RC	err_l_bndry_match 0: line	Line start and line end mismatch between VC0 and DT0. Read to clear. start and line end short packet match; _di0 1: Line-start and line-end short packets do not match.

MIPI0_LINE_INTR_MSK

MIPI0_LINE_INTR_MSK is MIPI0 line interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1094	MIPI0_LINE_INTR_MSK	0x0000_0000



Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23]	RW	mask_err_l_seq_di 0:	err_l_seq_di7 Interrupt mask register. mask interrupt; 7 1: Interrupts are enabled.
[22]	RW	mask_err_l_seq_di 0:	err_l_seq_di6 Interrupt mask register. mask interrupt; 6 1: Interrupts are enabled.
[21]	RW	mask_err_l_seq_di 0:	err_l_seq_di5 Interrupt mask register. mask interrupt; 5 1: Interrupts are enabled.
[20]	RW	mask_err_l_seq_di 0:	err_l_seq_di4 Interrupt mask register. mask interrupt; 4 1: Interrupts are enabled.
[19]	RW	mask_err_l_seq_di 0:	err_l_seq_di3 Interrupt mask register. mask interrupt; 3 1: Interrupts are enabled.
[18]	RW	mask_err_l_seq_di 0:	err_l_seq_di2 Interrupt mask register. mask interrupt; 2 1: Interrupts are enabled.

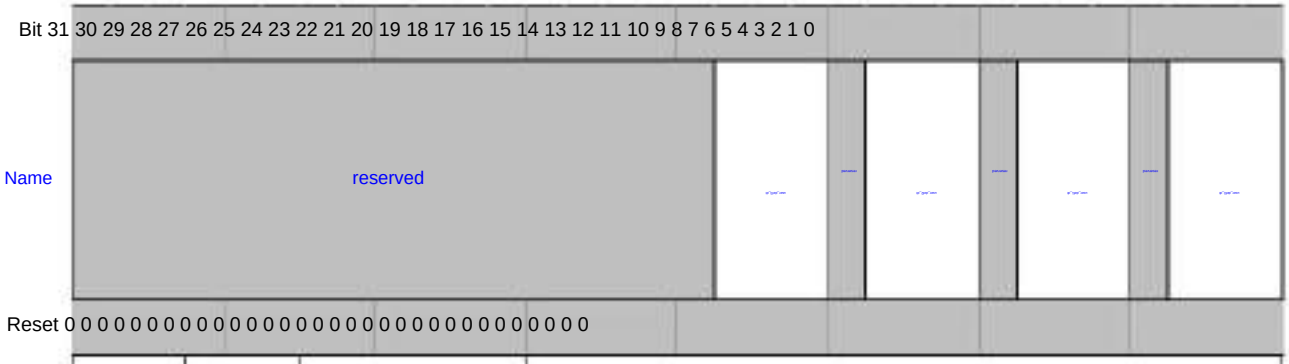
[17] RW		mask_err_l_seq_di 0:	err_l_seq_di1 Interrupt mask register. mask interrupt; 1 1: Interrupts are enabled.
[16] RW		mask_err_l_seq_di 0:	err_l_seq_di0 Interrupt mask register. mask interrupt; 0 1: Interrupts are enabled.
[15:8] RO		reserved	reserve.
[7] RW		mask_err_l_bndry_ 0: match_di7	err_l_bndry_match_di7 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[6] RW		mask_err_l_bndry_ 0: match_di6	err_l_bndry_match_di6 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[5] RW		mask_err_l_bndry_ 0: match_di5	err_l_bndry_match_di5 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[4] RW		mask_err_l_bndry_ 0: match_di4	err_l_bndry_match_di4 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[3] RW		mask_err_l_bndry_ 0: match_di3 1: enable interrupt.	err_l_bndry_match_di3 Interrupt mask register. mask interrupt;
[2] RW		mask_err_l_bndry_ 0: match_di2	err_l_bndry_match_di2 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[1] RW		mask_err_l_bndry_ 0: match_di1	err_l_bndry_match_di1 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.
[0] RW		mask_err_l_bndry_ 0: match_di0	err_l_bndry_match_di0 Interrupt mask register. mask interrupt; 1: Interrupts are enabled.

MIPI0_USERDEF_DT

MIPI0_USERDEF_DT is MIPI0 user-defined data type

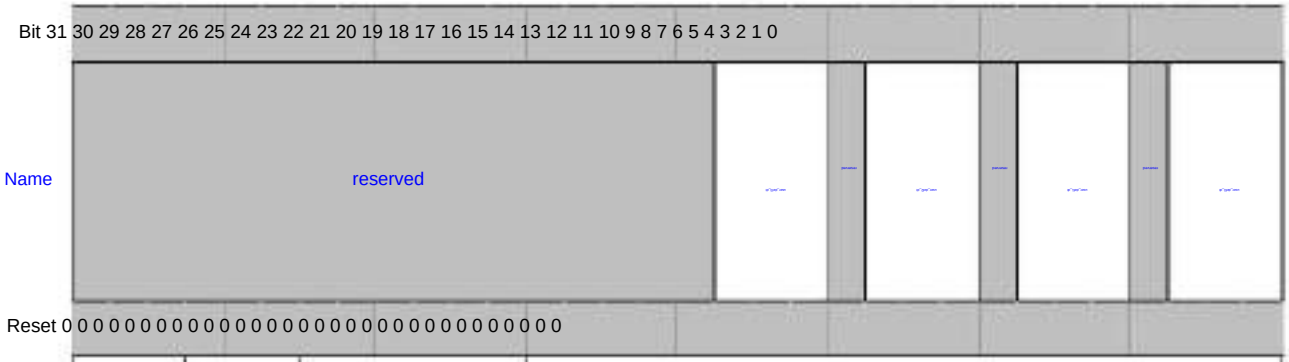
The corresponding pixel width configuration register.

Offset Address	Register Name	Total Reset Value
0x1100	MIPI0_USERDEF_DT	0x0000_0000



Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:12]	RW	user_def3_dt	The pixel bit width transmitted when the data type is user_def3. 000ÿ8bitÿ 001ÿ10bitÿ 010ÿ12bitÿ 011ÿ14bitÿ 100ÿ16bitÿ Other: reserved.
[11]	RO	reserved	reserve
[10:8]	RW	user_def2_dt	The pixel bit width transmitted when the data type is user_def2. 000ÿ8bitÿ 001ÿ10bitÿ 010ÿ12bit 011ÿ14bitÿ 100ÿ16bitÿ Other: reserved.
[7]	RO	reserved	reserve
[6:4]	RW	user_def1_dt	The pixel bit width transmitted when the data type is user_def1. 000ÿ8bitÿ 001ÿ10bitÿ 010ÿ12bitÿ 011ÿ14bitÿ 100ÿ16bitÿ Other: reserved.

Offset Address	Register Name	Total Reset Value
0x1100	MIPI0_USERDEF_DT	0x0000_0000

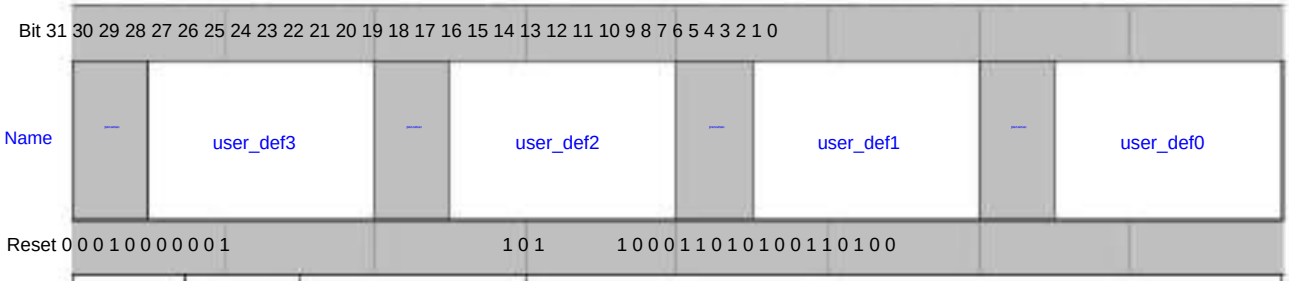


Bits	Access	Name	Description
[3]	RO	reserved	reserve.
[2:0]	RW	user_def0_dt	The pixel bit width transmitted when the data type is user_def0. 000ÿ8bitÿ 001ÿ10bitÿ 010ÿ12bitÿ 011ÿ14bitÿ 100ÿ16bitÿ Other: reserved.

MIPI0_USER_DEF

MIPI0_USER_DEF is the type enable configuration register for MIPI0 user-defined data type.

Offset Address	Register Name	Total Reset Value
0x1104	MIPI0_USER_DEF	0x1036_3534



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:24]	RW	user_def3	User-defined data type 3. The value of this register is used to match the data type of the sensor output and is used in conjunction with MIPI0_USERDEF_DT[user_def3_dt].

[23:22] RO		reserved	reserve.
[21:16] RW	user_def2		User-defined data type 2. The value of this register is used to match the data type of the sensor output and is used in conjunction with MIPI0_USERDEF_DT[user_def2_dt].
[15:14] RO		reserved	reserve.
[13:8] RW	user_def1		User-defined data type 1. The value of this register is used to match the data type of the sensor output and is used in conjunction with MIPI0_USERDEF_DT[user_def1_dt].
[7:6] RO		reserved	reserve.
[5:0] RW	user_def0		User-defined data type 0. The value of this register is used to match the data type of the sensor output, and it is used in conjunction with MIPI0_USERDEF_DT[user_def0_dt].

MIPI0_CTRL_MODE_HS

MIPI0_CTRL_MODE_HS is the MIPI0 working mode enable register.

Offset Address	Register Name	Total Reset Value
0x1108	MIPI0_CTRL_MODE_HS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RW	user_def_en	User Define mode enabled. 0: disable; 1: enable.
[7:0]	RO	reserved	reserve.

MIPI0_DOL_ID_CODE0

MIPI0_DOL_ID_CODE0 is MIPI0 DOL mode frame identification register 0.

Offset Address	Register Name	Total Reset Value
0x1200	MIPI0_DOL_ID_CODE0	0x0242_0241

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg1																id_code_reg0															
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	id_code_reg1	SEF1 frame ID code of frame N in mipi dol mode.
[15:0]	RW	id_code_reg0	LEF frame ID code of frame N in mipi dol mode.

MIPI0_DOL_ID_CODE1

MIPI0_DOL_ID_CODE1 is MIPI0 DOL mode frame identification register 1.

Offset Address	Register Name	Total Reset Value
0x1204	MIPI0_DOL_ID_CODE1	0x0251_0244

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg3																id_code_reg2															
Reset	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg3	LEF frame ID code of frame N+1 in mipi dol mode.
[15:0]	RW	id_code_reg2	SEF2 frame ID code of frame N in mipi dol mode.

MIPI0_DOL_ID_CODE2

MIPI0_DOL_ID_CODE2 is MIPI0 DOL mode frame identification register 2.

Offset Address	Register Name	Total Reset Value
0x1208	MIPI0_DOL_ID_CODE2	0x0254_0252

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg5																id_code_reg4															
Reset	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg5	SEF2 frame ID code of frame N+1 in mipi dol mode.
[15:0]	RW	id_code_reg4	SEF1 frame ID code of frame N+1 in mipi dol mode.

MIPI0_CTRL_MODE_PIXEL

MIPI0_CTRL_MODE_PIXEL is the MIPI0 output mode enable register.

Offset Address	Register Name	Total Reset Value
0x1230	MIPI0_CTRL_MODE_PIXEL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14:13]	RW	stagger_frm_num	STAGGER HDR MODE frame number. 01: Two frames of hdr; 10: Three frames of hdr; 11: four-frame hdr; Other: reserved.
[12]	RW	stagger_hdr_mode	Omnivision Stagger Hdr Mode mode enable. 0: disable; 1: enable.
[11:5]	RO	reserved	reserve.
[4]	RW	mipi_dol_mode	MIPI DOL mode enabled. 0: disable; 1: enable.
[3:1]	RO	reserved	reserve.
[0]	RW	crop_en	Cropping enabled. 0: disable; 1: enable;

MIPI0_DUMMY_PIX_REG

MIPI0_DUMMY_PIX_REG is the pixel value register of MIPI0 dummy row.

Offset Address	Register Name	Total Reset Value
0x1240	MIPI0_DUMMY_PIX_REG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dummy_pix_reg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	dummy_pix_reg	stagger hdr mode dummy line pixel value.

MIPI0_IMGSIZE0_STATIC

MIPI0_IMGSIZE0_STATIS is the image width and height register transmitted by MIPI0 VC0.

Offset Address	Register Name	Total Reset Value
0x1250	MIPI0_IMGSIZE0_STATIC	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	imgheight_statis_vc0	imgwidth_statis_vc0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_v In	MIPI mode, the image height of the last frame transmitted by virtual channel0. c0
[15:0]	RO	imgwidth_statis_vc In	MIPI mode, the last image width transmitted by virtual channel0. 0

MIPI0_IMGSIZE1_STATIS

MIPI0_IMGSIZE1_STATIS is the image width and height register transmitted by MIPI0 VC1.

Offset Address	Register Name	Total Reset Value
0x1254	MIPI0_IMGSIZE1_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	imgheight_static_vc1	imgwidth_static_vc1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	imgheight_statis_v In c1	MIPI mode, the image height of the last frame transmitted by virtual channel1.
[15:0]	RO	imgwidth_statis_vc In	MIPI mode, the last image width transmitted by virtual channel1. 1

MIPI0_IMGSIZE2_STATIS

MIPI0_IMGSIZE2_STATIS is the image width and height register transmitted by MIPI0 VC2.

Offset Address	Register Name	Total Reset Value
0x1258	MIPI0_IMGSIZE2_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	imgheight_statis_vc2	imgwidth_statis_vc2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	imgheight_statis_v In c2	MIPI mode, the image height of the last frame transmitted by virtual channel2.
[15:0]	RO	imgwidth_statis_vc In	MIPI mode, the last image width transmitted by virtual channel2. 2

MIPI0_IMGSIZE3_STATIS

MIPI0_IMGSIZE3_STATIS is the image width and height register transmitted by MIPI0 VC3.

Offset Address	Register Name	Total Reset Value
0x125C	MIPI0_IMGSIZE3_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	imgheight_statis_vc3	imgwidth_statis_vc3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_v c3	In MIPI mode, the image height of the previous frame transmitted by virtual channel3.
[15:0]	RO	imgwidth_statis_vc	In MIPI mode, the last image width transmitted by virtual channel3. 3

MIPI0_CTRL_INT_RAW

MIPI0_CTRL_INT_RAW is MIPI0 read data error raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F0	MIPI0_CTRL_INT_RAW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	WC	int_dfifo_rderr_raw	MIPI CTRL Read data FIFO raw interrupt status. 0: No raw interrupt; 1: There is a raw interrupt.
[16]	WC	int_cfifo_rderr_raw	MIPI CTRL Read command FIFO raw interrupt status. 0: No raw interrupt.
[15:2]	RO	reserved	reserve.

[1] WC		int_dfifo_wrerr_ra In	MIPI CTRL Write data FIFO raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[0] WC		int_cfifo_wrerr_ra In	MIPI CTRL Write command FIFO raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

MIPI0_CTRL_INT

MIPI0_CTRL_INT is MIPI0 read data error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F4	MIPI0_CTRL_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						~~~	reserved								~~~
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:18] RO		reserved	reserve.
[17] RO		int_dfifo_rderr_st	MIPI CTRL Read data FIFO interrupt status. 0: no interrupt; 1: There is an interrupt.
[16] RO		int_cfifo_rderr_st	MIPI CTRL Read command FIFO interrupt status. 0: no interrupt; 1: There is an interrupt.
[15:2] RO		reserved	reserve.
[1]	RO	int_dfifo_wrerr_st	MIPI CTRL Write data FIFO interrupt status. 0: no interrupt; 1: There is an interrupt.

[0]	RO	int_cfifo_wrerr_st	MIPI CTRL Write command FIFO interrupt status. 0: no interrupt; 1: There is an interrupt.

MIPI0_CTRL_INT_MSK

MIPI0_CTRL_INT_MSK is MIPI0 read data error interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x12F8	MIPI0_CTRL_INT_MSK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RW	int_dfifo_rderr_ms	MIPI CTRL Read Data FIFO Interrupt Enable. 0: mask interrupt; k 1: Interrupts are enabled.
[16]	RW	int_cfifo_rderr_ms	MIPI CTRL read command FIFO interrupt enable. 0: mask interrupt; k 1: enable interrupt.
[15:2]	RO	reserved	reserve.
[1]	RW	int_dfifo_wrerr_ms	MIPI CTRL Write Data FIFO Interrupt Enable. 0: mask interrupt; k 1: Interrupts are enabled.
[0]	RW	int_cfifo_wrerr_ms	MIPI CTRL Write command FIFO interrupt enable. 0: mask interrupt; k 1: Interrupts are enabled.

LVDS0_WDR

LVDS0_WDR is the LVDS WDR control register.

Offset Address	Register Name	Total Reset Value
0x1300	LVDS0_WDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														lvds_wdr_mod	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	lvds_wdr_mode	LVDS WDR mode selection. 0x0: WDR marked by SOF-EOF, both long and short exposures have independent synchronization codes. 0x2: WDR mode of HiSPi interface, long and short exposure share a pair of SOF-EOF marks, and the first few lines of short exposure are filled with 0x04. 0x4: SONY DOL mode, 4-field synchronization code, SAV-EAV identification method, long and short exposures have independent synchronization codes. 0x6: SONY DOL mode, 5-field synchronization code, Frame Information Line is not included in the image information. 0xC: SONY DOL mode, 5-field synchronization code, Frame Information Line is not included in the image information.
[7:6]	RO	reserved	reserve.
[5:4]	RW	lvds_wdr_num	WDR mode configuration signal. 00: Reserved; 01: 2-frame WDR; 10: 3-frame WDR; 11: 4-frame WDR.
[3:1]	RO	reserved	reserve.
[0]	RW	lvds_wdr_en	WDR enable signal. 0: Linear mode; 1: WDR mode.

LVDS0_IMGSIZE

LVDS0_IMGSIZE is the LVDS image width and height register.

Offset Address	Register Name	Total Reset Value
0x130C	LVDS0_IMGSIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_imgheight	lvds_imgwidth_lane
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lvds_imgheight	Image height minus 1.
[15:0]	RW	lvds_imgwidth_lan	The image width transmitted by each channel minus 1.

LVDS0_CTRL

LVDS0_CTRL is the LVDS control register.

Offset Address	Register Name	Total Reset Value
0x1310	LVDS0_CTRL	0x0000_0310

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:16]	RW	lvds_split_mode	LVDS/HiSPi Sync Code transfer type. 000: Per Lane mode; Others: Reserved.
[15:13]	RO	reserved	reserve.

[12] RW	lvds_crop_en		LVDS/HiSPi image cropping enable. 0: disable; 1: enable.
[11:10] RO		reserved	reserve.
[9] RW		(sync_code) serial data bit11; ian lvds_code_big_end	In LVDS/HiSPi mode, the serial bit transmission order of the transmitted RAW data synchronization code (sync_code). 0: LSB, the lower bit is transmitted first, and the actually received synchronization code sequence is bit0, bit1, ... 1: MSB, the high bit is transmitted first, and the serial data sequence of the actually received synchronization code (sync_code) is bit11, bit10, ... bit0.
[8] RW		serial data sequence is n	In LVDS/HiSPi mode, the transmitted RAW data is the transmission sequence of the serial bits of the effective pixel pixel. 0: LSB, the lower bit is transmitted first, and the actually received effective pixel bit0, bit1, ... bit11; 1: MSB, the high bit is transmitted first, and the serial data sequence of the actually received effective pixel pixel is bit11, bit10, ... bit0.
[7]	RO	reserved	reserve.
[6:4] RW	lvds_raw_type		In LVDS/HiSPi mode, the RAW data type transmitted. 001ÿRaw 8bitÿ 010ÿRaw 10bitÿ 011ÿRaw 12bitÿ 100ÿRaw 14bitÿ 101ÿRaw 16bitÿ Other: reserved.
[3:1] RO		reserved	reserve.
[0] RW	lvds_sync_mode		In LVDS mode, frame/line synchronous mode. 0: The synchronization mode is SOF/EOF/SOL/EOL mode; SOF marks the start of the first line of the effective area, EOF marks the end of the last line of the effective area, and other effective areas use SOL and EOL as the start and end respectively. 1: The synchronization mode is SAV/EAV mode; use SAV(Invalid) and EAV(Invalid) to identify the invalid data in the blanking area, and use SAV(Valid) and EAV(Valid) to identify the pixel data in the valid area.

LVDS0_CROP_START

LVDS0_CROP_START is the LVDS cropping register.

Offset Address	Register Name	Total Reset Value
0x1314	LVDS0_CROP_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_start_y	lvds_start_x_lane
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lvds_start_y	Clipping start point height.
[15:0]	RW	lvds_start_x_lane	Cropping starting point width. The configuration value is the starting pixel point to be cropped divided by the number of channels.

LVDS0_LANE0_SOF_01

LVDS0_LANE0_SOF_01 is LVDS/HiSPi mode, lane0 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1320	LVDS0_LANE0_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_sof_1	lane0_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane0 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane0 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE0_SOF_23

LVDS0_LANE0_SOF_23 is LVDS/HiSPi mode, lane0 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1324	LVDS0_LANE0_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_sof_3	lane0_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane0 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane0 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_EOF_01

LVDS0_LANE0_EOF_01 is the end-of-frame synchronization code configuration register for lane0 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1328	LVDS0_LANE0_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_eof_1	lane0_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane0 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane0 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE0_EOF_23

LVDS0_LANE0_EOF_23 is the end-of-frame sync code configuration register for lane0 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x132C	LVDS0_LANE0_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_eof_3	lane0_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane0 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane0 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_SOL_01

LVDS0_LANE0_SOL_01 is the LVDS/HiSPi mode, lane0 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1330	LVDS0_LANE0_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_sol_1	lane0_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane0 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane0 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE0_SOL_23

LVDS0_LANE0_SOL_23 is the configuration register for lane0 line start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1334	LVDS0_LANE0_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_sol_3	lane0_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane0_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane0 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane0_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane0 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_EOL_01

LVDS0_LANE0_EOL_01 is the end-of-line synchronous code configuration register for lane0 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1338	LVDS0_LANE0_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_eol_1	lane0_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane0_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane0 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane0_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane0 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE0_EOL_23

LVDS0_LANE0_EOL_23 is the end-of-line synchronous code configuration register for lane0 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x133C	LVDS0_LANE0_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_eol_3	lane0_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane0_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane0 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane0_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane0 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_SOF_01

LVDS0_LANE1_SOF_01 is the LVDS/HiSPi mode, lane1 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1340	LVDS0_LANE1_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_sof_1	lane1_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane1 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane1 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE1_SOF_23

LVDS0_LANE1_SOF_23 is the LVDS/HiSPi mode, lane1 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1344	LVDS0_LANE1_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_sof_3	lane1_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane1 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_sof_2	Frame start synchronization code of frame 2 in LVDS, HiSPi mode, lane1 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_EOF_01

LVDS0_LANE1_EOF_01 is the end-of-frame sync code configuration register for lane1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1348	LVDS0_LANE1_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_eof_1	lane1_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane1 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane1 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE1_EOF_23

LVDS0_LANE1_EOF_23 is the end-of-frame sync code configuration register for lane1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x134C	LVDS0_LANE1_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_eof_3	lane1_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane1 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane1 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_SOL_01

LVDS0_LANE1_SOL_01 is the LVDS/HiSPi mode, lane1 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1350	LVDS0_LANE1_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_sol_1	lane1_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane1 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane1 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE1_SOL_23

LVDS0_LANE1_SOL_23 is the LVDS/HiSPi mode, lane1 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1354	LVDS0_LANE1_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_sol_3	lane1_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane1 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane1 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_EOL_01

LVDS0_LANE1_EOL_01 is the end-of-line synchronous code configuration register for lane1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1358	LVDS0_LANE1_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_eol_1	lane1_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane1 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane1 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE1_EOL_23

LVDS0_LANE1_EOL_23 is the end-of-line synchronous code configuration register for lane1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x135C	LVDS0_LANE1_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_eol_3	lane1_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane1 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane1 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_SOF_01

LVDS0_LANE2_SOF_01 is the configuration register for lane2 start of frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1360	LVDS0_LANE2_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_sof_1	lane2_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane2 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane2 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE2_SOF_23

LVDS0_LANE2_SOF_23 is the configuration register for lane2 start of frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1364	LVDS0_LANE2_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_sof_3	lane2_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane2 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane2 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_EOF_01

LVDS0_LANE2_EOF_01 is the end-of-frame sync code configuration register for lane2 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1368	LVDS0_LANE2_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_eof_1	lane2_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane2 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane2 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE2_EOF_23

LVDS0_LANE2_EOF_23 is the end-of-frame sync code configuration register for lane2 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x136C	LVDS0_LANE2_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_eof_3	lane2_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane2 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane2 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_SOL_01

LVDS0_LANE2_SOL_01 is the LVDS/HiSPi mode, lane2 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1370	LVDS0_LANE2_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_sol_1	lane2_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane2 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane2 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE2_SOL_23

LVDS0_LANE2_SOL_23 is the LVDS/HiSPi mode, lane2 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1374	LVDS0_LANE2_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_sol_3	lane2_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane2 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane2 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_EOL_01

LVDS0_LANE2_EOL_01 is the end-of-line synchronous code configuration register for lane2 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1378	LVDS0_LANE2_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_eol_1	lane2_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane2 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane2 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE2_EOL_23

LVDS0_LANE2_EOL_23 is the end-of-line synchronous code configuration register for lane2 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x137C	LVDS0_LANE2_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_eol_3	lane2_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane2 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane2 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_SOF_01

LVDS0_LANE3_SOF_01 is LVDS/HiSPi mode, lane3 start of frame synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1380	LVDS0_LANE3_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_sof_1	lane3_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane3 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane3 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE3_SOF_23

LVDS0_LANE3_SOF_23 is the configuration register for lane3 start-of-frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1384	LVDS0_LANE3_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_sof_3	lane3_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane3 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane3 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_EOF_01

LVDS0_LANE3_EOF_01 is the end-of-frame sync code configuration register for lane3 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1388	LVDS0_LANE3_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_eof_1	lane3_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane3 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane3 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE3_EOF_23

LVDS0_LANE3_EOF_23 is the end-of-frame synchronization code configuration register for lane3 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x138C	LVDS0_LANE3_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_eof_3	lane3_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane3 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane3 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_SOL_01

LVDS0_LANE3_SOL_01 is the LVDS/HiSPi mode, lane3 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1390	LVDS0_LANE3_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_sol_1	lane3_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane3 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane3 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE3_SOL_23

LVDS0_LANE3_SOL_23 is the LVDS/HiSPi mode, lane3 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1394	LVDS0_LANE3_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_sol_3	lane3_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane3_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane3 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane3_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane3 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_EOL_01

LVDS0_LANE3_EOL_01 is the end-of-line synchronous code configuration register for lane3 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1398	LVDS0_LANE3_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_eol_1	lane3_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane3_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane3 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane3_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi mode, lane3 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE3_EOL_23

LVDS0_LANE3_EOL_23 is the end-of-line synchronous code configuration register for lane3 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x139C	LVDS0_LANE3_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_eol_3	lane3_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane3 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane3 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_SOF_01

LVDS0_LANE4_SOF_01 is the configuration register for lane4 start of frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13A0	LVDS0_LANE4_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_sof_1	lane4_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane4 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane4 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE4_SOF_23

LVDS0_LANE4_SOF_23 is the configuration register for lane4 start of frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13A4	LVDS0_LANE4_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_sof_3	lane4_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane4 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane4 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_EOF_01

LVDS0_LANE4_EOF_01 is the end-of-frame sync code configuration register for lane4 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13A8	LVDS0_LANE4_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_eof_1	lane4_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane4 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane4 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE4_EOF_23

LVDS0_LANE4_EOF_23 is the end-of-frame sync code configuration register for lane4 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13AC	LVDS0_LANE4_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_eof_3	lane4_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane4 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane4 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_SOL_01

LVDS0_LANE4_SOL_01 is the LVDS/HiSPi mode, lane4 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x13B0	LVDS0_LANE4_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_sol_1	lane4_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane4 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane4 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE4_SOL_23

LVDS0_LANE4_SOL_23 is the configuration register for lane4 line start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13B4	LVDS0_LANE4_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_sol_3	lane4_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane4 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane4 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_EOL_01

LVDS0_LANE4_EOL_01 is the end-of-line synchronous code configuration register for lane4 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13B8	LVDS0_LANE4_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_eol_1	lane4_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane4 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane4 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE4_EOL_23

LVDS0_LANE4_EOL_23 is the end-of-line synchronous code configuration register for lane4 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13BC	LVDS0_LANE4_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_eol_3	lane4_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane4 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane4 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_SOF_01

LVDS0_LANE5_SOF_01 is the LVDS/HiSPi mode, lane5 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x13C0	LVDS0_LANE5_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_sof_1	lane5_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane5 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane5 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE5_SOF_23

LVDS0_LANE5_SOF_23 is the configuration register for lane5 start of frame synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13C4	LVDS0_LANE5_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_sof_3	lane5_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane5 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane5 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_EOF_01

LVDS0_LANE5_EOF_01 is the end-of-frame sync code configuration register for lane5 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13C8	LVDS0_LANE5_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_eof_1	lane5_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane5 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane5 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE5_EOF_23

LVDS0_LANE5_EOF_23 is the end-of-frame sync code configuration register for lane5 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13CC	LVDS0_LANE5_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_eof_3	lane5_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane5 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane5 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_SOL_01

LVDS0_LANE5_SOL_01 is the LVDS/HiSPi mode, lane5 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x13D0	LVDS0_LANE5_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_sol_1	lane5_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane5 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane5 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE5_SOL_23

LVDS0_LANE5_SOL_23 is the LVDS/HiSPi mode, lane5 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x13D4	LVDS0_LANE5_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_sol_3	lane5_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane5 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane5 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_EOL_01

LVDS0_LANE5_EOL_01 is the end-of-line synchronous code configuration register for lane5 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13D8	LVDS0_LANE5_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_eol_1	lane5_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane5 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane5 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE5_EOL_23

LVDS0_LANE5_EOL_23 is the end-of-line synchronous code configuration register for lane5 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13DC	LVDS0_LANE5_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_eol_3	lane5_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane5 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane5 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_SOF_01

LVDS0_LANE6_SOF_01 is the configuration register of lane6 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13E0	LVDS0_LANE6_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_sof_1	lane6_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane6 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane6 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE6_SOF_23

LVDS0_LANE6_SOF_23 is the configuration register for lane6 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13E4	LVDS0_LANE6_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_sof_3	lane6_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane6 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane6 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_EOF_01

LVDS0_LANE6_EOF_01 is the end-of-frame synchronization code configuration register for lane6 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13E8	LVDS0_LANE6_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_eof_1	lane6_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane6 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane6 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE6_EOF_23

LVDS0_LANE6_EOF_23 is the end-of-frame synchronization code configuration register for lane6 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13EC	LVDS0_LANE6_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_eof_3	lane6_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane6_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane6 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane6_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane6 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_SOL_01

LVDS0_LANE6_SOL_01 is the LVDS/HiSPi mode, lane6 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x13F0	LVDS0_LANE6_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_sol_1	lane6_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane6_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane6 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane6_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane6 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE6_SOL_23

LVDS0_LANE6_SOL_23 is the configuration register for lane6 line start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13F4	LVDS0_LANE6_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_sol_3	lane6_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane6 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane6 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_EOL_01

LVDS0_LANE6_EOL_01 is the end-of-line synchronous code configuration register for lane6 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13F8	LVDS0_LANE6_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_eol_1	lane6_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane6 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane6 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE6_EOL_23

LVDS0_LANE6_EOL_23 is the end-of-line synchronous code configuration register for lane6 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x13FC	LVDS0_LANE6_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_eol_3	lane6_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane6_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane6 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane6_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane6 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_SOF_01

LVDS0_LANE7_SOF_01 is the LVDS/HiSPi mode, lane7 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1400	LVDS0_LANE7_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_sof_1	lane7_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane7_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane7 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane7_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane7 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE7_SOF_23

LVDS0_LANE7_SOF_23 is the configuration register for lane7 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1404	LVDS0_LANE7_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_sof_3	lane7_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane7 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane7 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_EOF_01

LVDS0_LANE7_EOF_01 is the end-of-frame synchronization code configuration register for lane7 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1408	LVDS0_LANE7_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_eof_1	lane7_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane7 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane7 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE7_EOF_23

LVDS0_LANE7_EOF_23 is the end-of-frame synchronization code configuration register for lane7 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x140C	LVDS0_LANE7_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_eof_3	lane7_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane7 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane7 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_SOL_01

LVDS0_LANE7_SOL_01 is the LVDS/HiSPi mode, lane7 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	LVDS0_LANE7_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_sol_1	lane7_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_sol_1	Line start synchronization code of frame 1 in LVDS, HiSPi mode, lane7 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane7 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE7_SOL_23

LVDS0_LANE7_SOL_23 is the LVDS/HiSPi mode, lane7 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1414	LVDS0_LANE7_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_sol_3	lane7_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane7 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane7 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_EOL_01

LVDS0_LANE7_EOL_01 is the end-of-line synchronous code configuration register for lane7 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1418	LVDS0_LANE7_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_eol_1	lane7_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane7 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane7 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE7_EOL_23

LVDS0_LANE7_EOL_23 is the end-of-line synchronous code configuration register for lane7 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x141C	LVDS0_LANE7_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_eol_3	lane7_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane7 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane7 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_SOF_01

LVDS0_LANE8_SOF_01 is the configuration register of lane8 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1420	LVDS0_LANE8_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_sof_1	lane8_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane8 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane8 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE8_SOF_23

LVDS0_LANE8_SOF_23 is the configuration register of lane8 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1424	LVDS0_LANE8_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_sof_3	lane8_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane8 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane8 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_EOF_01

LVDS0_LANE8_EOF_01 is the end-of-frame sync code configuration register for lane8 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1428	LVDS0_LANE8_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_eof_1	lane8_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane8 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane8 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE8_EOF_23

LVDS0_LANE8_EOF_23 is the end-of-frame sync code configuration register for lane8 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x142C	LVDS0_LANE8_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_eof_3	lane8_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane8 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane8 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_SOL_01

LVDS0_LANE8_SOL_01 is the configuration register for lane8 line start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1430	LVDS0_LANE8_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_sol_1	lane8_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane8 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane8 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE8_SOL_23

LVDS0_LANE8_SOL_23 is the configuration register for lane8 line start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1434	LVDS0_LANE8_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_sol_3	lane8_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane8_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane8 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane8_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane8 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_EOL_01

LVDS0_LANE8_EOL_01 is the end-of-line synchronous code configuration register for lane8 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1438	LVDS0_LANE8_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_eol_1	lane8_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane8_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane8 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane8_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane8 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE8_EOL_23

LVDS0_LANE8_EOL_23 is the end-of-line synchronous code configuration register for lane8 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x143C	LVDS0_LANE8_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_eol_3	lane8_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane8 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane8 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_SOF_01

LVDS0_LANE9_SOF_01 is the configuration register for lane9 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1440	LVDS0_LANE9_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_sof_1	lane9_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane9 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane9 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE9_SOF_23

LVDS0_LANE9_SOF_23 is the configuration register of lane9 frame start synchronization code in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1444	LVDS0_LANE9_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_sof_3	lane9_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane9 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane9 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_EOF_01

LVDS0_LANE9_EOF_01 is the end-of-frame sync code configuration register for lane9 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1448	LVDS0_LANE9_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_eof_1	lane9_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane9 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane9 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE9_EOF_23

LVDS0_LANE9_EOF_23 is the end-of-frame sync code configuration register for lane9 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x144C	LVDS0_LANE9_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_eof_3	lane9_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane9 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane9 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_SOL_01

LVDS0_LANE9_SOL_01 is the LVDS/HiSPi mode, lane9 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1450	LVDS0_LANE9_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_sol_1	lane9_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane9 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane9 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE9_SOL_23

LVDS0_LANE9_SOL_23 is the LVDS/HiSPi mode, lane9 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1454	LVDS0_LANE9_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_sol_3	lane9_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane9 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane9 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_EOL_01

LVDS0_LANE9_EOL_01 is the end-of-line synchronous code configuration register for lane9 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1458	LVDS0_LANE9_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_eol_1	lane9_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane9 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane9 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE9_EOL_23

LVDS0_LANE9_EOL_23 is the end-of-line synchronous code configuration register for lane9 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x145C	LVDS0_LANE9_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_eol_3	lane9_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane9_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane9 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane9_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane9 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_SOF_01

LVDS0_LANE10_SOF_01 is LVDS/HiSPi mode, lane10 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1460	LVDS0_LANE10_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_sof_1	lane10_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane10_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane10 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane10_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane10 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE10_SOF_23

LVDS0_LANE10_SOF_23 is LVDS/HiSPi mode, lane10 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1464	LVDS0_LANE10_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_sof_3	lane10_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane10 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane10 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_EOF_01

LVDS0_LANE10_EOF_01 is the end-of-frame synchronization code configuration register for lane10 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1468	LVDS0_LANE10_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_eof_1	lane10_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane10 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane10 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE10_EOF_23

LVDS0_LANE10_EOF_23 is the end-of-frame synchronization code configuration register for lane10 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x146C	LVDS0_LANE10_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_eof_3	lane10_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane10 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane10 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_SOL_01

LVDS0_LANE10_SOL_01 is the LVDS/HiSPi mode, lane10 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1470	LVDS0_LANE10_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_sol_1	lane10_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane10 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane10 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE10_SOL_23

LVDS0_LANE10_SOL_23 is the LVDS/HiSPi mode, lane10 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1474	LVDS0_LANE10_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_sol_3	lane10_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane10 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane10 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_EOL_01

LVDS0_LANE10_EOL_01 is the end-of-line synchronous code configuration register for lane10 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1478	LVDS0_LANE10_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_eol_1	lane10_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_eol_1	End of line synchronization code of frame 1 in LVDS, HiSPi mode, lane10 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane10 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE10_EOL_23

LVDS0_LANE10_EOL_23 is the end-of-line synchronous code configuration register for lane10 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x147C	LVDS0_LANE10_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_eol_3	lane10_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane10_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane10 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane10_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane10 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_SOF_01

LVDS0_LANE11_SOF_01 is LVDS/HiSPi mode, lane11 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1480	LVDS0_LANE11_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_sof_1	lane11_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane11_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane11 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane11_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane11 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE11_SOF_23

LVDS0_LANE11_SOF_23 is LVDS/HiSPi mode, lane11 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1484	LVDS0_LANE11_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_sof_3	lane11_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane11 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane11 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_EOF_01

LVDS0_LANE11_EOF_01 is the end-of-frame synchronization code configuration register for lane11 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1488	LVDS0_LANE11_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_eof_1	lane11_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane11 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane11 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE11_EOF_23

LVDS0_LANE11_EOF_23 is the end-of-frame synchronization code configuration register for lane11 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x148C	LVDS0_LANE11_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_eof_3	lane11_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane11 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane11 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_SOL_01

LVDS0_LANE11_SOL_01 is the LVDS/HiSPi mode, lane11 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1490	LVDS0_LANE11_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_sol_1	lane11_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane11 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane11 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE11_SOL_23

LVDS0_LANE11_SOL_23 is the LVDS/HiSPi mode, lane11 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1494	LVDS0_LANE11_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_sol_3	lane11_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane11 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane11 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_EOL_01

LVDS0_LANE11_EOL_01 is the end-of-line synchronization code configuration register for lane11 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1498	LVDS0_LANE11_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_eol_1	lane11_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane11 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane11 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE11_EOL_23

LVDS0_LANE11_EOL_23 is the end-of-line synchronization code configuration register for lane11 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x149C	LVDS0_LANE11_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_eol_3	lane11_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane11_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane11 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane11_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane11 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_NXT_SOF_01

LVDS0_LANE0_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane0 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x14A0	LVDS0_LANE0_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_sof_1	lane0_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane0_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane0 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane0_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane0 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE0_NXT_SOF_23

LVDS0_LANE0_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane0 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x14A4	LVDS0_LANE0_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_sof_3	lane0_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane0 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane0 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_NXT_EOF_01

LVDS0_LANE0_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane0 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14A8	LVDS0_LANE0_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_eof_1	lane0_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane0 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane0 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE0_NXT_EOF_23

LVDS0_LANE0_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane0 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14AC	LVDS0_LANE0_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_eof_3	lane0_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane0 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane0 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_NXT_SOL_01

LVDS0_LANE0_NXT_SOL_01 is the start synchronization code configuration register of lane0 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14B0	LVDS0_LANE0_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_sol_1	lane0_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane0 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane0 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE0_NXT_SOL_23

LVDS0_LANE0_NXT_SOL_23 is the start synchronization code configuration register of lane0 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14B4	LVDS0_LANE0_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_sol_3	lane0_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane0 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane0 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE0_NXT_EOL_01

LVDS0_LANE0_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane0 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14B8	LVDS0_LANE0_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_eol_1	lane0_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane0 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane0 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE0_NXT_EOL_23

LVDS0_LANE0_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane0 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14BC	LVDS0_LANE0_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane0_nxt_eol_3	lane0_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane0 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane0 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_NXT_SOF_01

LVDS0_LANE1_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane1 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x14C0	LVDS0_LANE1_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_sof_1	lane1_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane1 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane1 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE1_NXT_SOF_23

LVDS0_LANE1_NXT_SOF_23 is the start synchronization code configuration register of lane1 frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14C4	LVDS0_LANE1_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_sof_3	lane1_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane1 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS, HiSPi mode, lane1 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_NXT_EOF_01

LVDS0_LANE1_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane1 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14C8	LVDS0_LANE1_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_eof_1	lane1_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane1 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane1 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE1_NXT_EOF_23

LVDS0_LANE1_NXT_EOF_23 is the end-of-frame synchronous code configuration register for lane1 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14CC	LVDS0_LANE1_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_eof_3	lane1_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane1 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane1 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_NXT_SOL_01

LVDS0_LANE1_NXT_SOL_01 is the start synchronization code configuration register of lane1 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14D0	LVDS0_LANE1_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_sol_1	lane1_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane1 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane1_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane1 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE1_NXT_SOL_23

LVDS0_LANE1_NXT_SOL_23 is the start synchronization code configuration register of lane1 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14D4	LVDS0_LANE1_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_sol_3	lane1_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_nxt_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane1 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_nxt_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane1 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE1_NXT_EOL_01

LVDS0_LANE1_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane1 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14D8	LVDS0_LANE1_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_eol_1	lane1_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane1 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane1 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE1_NXT_EOL_23

LVDS0_LANE1_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane1 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14DC	LVDS0_LANE1_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane1_nxt_eol_3	lane1_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane1_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane1 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane1_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane1 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_NXT_SOF_01

LVDS0_LANE2_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 lane2 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x14E0	LVDS0_LANE2_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_sof_1	lane2_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane2 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane2 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE2_NXT_SOF_23

LVDS0_LANE2_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane2 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x14E4	LVDS0_LANE2_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_sof_3	lane2_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane2 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane2 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_NXT_EOF_01

LVDS0_LANE2_NXT_EOF_01 is the end-of-frame synchronous code configuration register for lane2 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14E8	LVDS0_LANE2_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_eof_1	lane2_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane2 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane2 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE2_NXT_EOF_23

LVDS0_LANE2_NXT_EOF_23 is the end-of-frame synchronous code configuration register for lane2 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14EC	LVDS0_LANE2_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_eof_3	lane2_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane2 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane2 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_NXT_SOL_01

LVDS0_LANE2_NXT_SOL_01 is the start synchronization code configuration register of lane2 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14F0	LVDS0_LANE2_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_sol_1	lane2_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane2 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane2 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE2_NXT_SOL_23

LVDS0_LANE2_NXT_SOL_23 is the start synchronization code configuration register of lane2 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x14F4	LVDS0_LANE2_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_sol_3	lane2_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_nxt_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane2 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane2 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE2_NXT_EOL_01

LVDS0_LANE2_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane2 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14F8	LVDS0_LANE2_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_eol_1	lane2_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane2_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane2 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane2_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane2 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE2_NXT_EOL_23

LVDS0_LANE2_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane2 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x14FC	LVDS0_LANE2_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane2_nxt_eol_3	lane2_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane2 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane2_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane2 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_NXT_SOF_01

LVDS0_LANE3_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 lane3 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1500	LVDS0_LANE3_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_sof_1	lane3_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane3 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane3 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE3_NXT_SOF_23

LVDS0_LANE3_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane3 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1504	LVDS0_LANE3_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_sof_3	lane3_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane3 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane3 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_NXT_EOF_01

LVDS0_LANE3_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane3 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1508	LVDS0_LANE3_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_eof_1	lane3_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane3 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane3 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE3_NXT_EOF_23

LVDS0_LANE3_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane3 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x150C	LVDS0_LANE3_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_eof_3	lane3_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane3 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane3 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_NXT_SOL_01

LVDS0_LANE3_NXT_SOL_01 is the start synchronization code configuration register of lane3 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1510	LVDS0_LANE3_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_sol_1	lane3_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane3 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane3 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE3_NXT_SOL_23

LVDS0_LANE3_NXT_SOL_23 is the start synchronization code configuration register of lane3 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1514	LVDS0_LANE3_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_sol_3	lane3_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane3 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane3 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE3_NXT_EOL_01

LVDS0_LANE3_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane3 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x1518	LVDS0_LANE3_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_eol_1	lane3_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane3 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi mode, lane3 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE3_NXT_EOL_23

LVDS0_LANE3_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane3 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x151C	LVDS0_LANE3_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane3_nxt_eol_3	lane3_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane3 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane3 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_NXT_SOF_01

LVDS0_LANE4_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane4 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1520	LVDS0_LANE4_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_sof_1	lane4_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane4 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane4 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE4_NXT_SOF_23

LVDS0_LANE4_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane4 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1524	LVDS0_LANE4_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_sof_3	lane4_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane4 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane4 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_NXT_EOF_01

LVDS0_LANE4_NXT_EOF_01 is the end-of-frame synchronization code configuration register for the N+1 frame lane4 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1528	LVDS0_LANE4_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_eof_1	lane4_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane4 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane4 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE4_NXT_EOF_23

LVDS0_LANE4_NXT_EOF_23 is the end-of-frame synchronous code configuration register for lane4 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x152C	LVDS0_LANE4_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_eof_3	lane4_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane4 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane4 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_NXT_SOL_01

LVDS0_LANE4_NXT_SOL_01 is the start synchronization code configuration register of lane4 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1530	LVDS0_LANE4_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_sol_1	lane4_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane4 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane4 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE4_NXT_SOL_23

LVDS0_LANE4_NXT_SOL_23 is LVDS/HiSPi mode, the N+1th frame lane4 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1534	LVDS0_LANE4_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_sol_3	lane4_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane4_nxt_sol_3	Line start synchronization code of frame 3 in LVDS, HiSPi mode, lane4 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane4_nxt_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane4 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE4_NXT_EOL_01

LVDS0_LANE4_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane4 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x1538	LVDS0_LANE4_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_eol_1	lane4_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane4_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane4 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane4_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane4 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE4_NXT_EOL_23

LVDS0_LANE4_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane4 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x153C	LVDS0_LANE4_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane4_nxt_eol_3	lane4_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane4 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane4_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane4 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_NXT_SOF_01

LVDS0_LANE5_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane5 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1540	LVDS0_LANE5_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_sof_1	lane5_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane5 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane5 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE5_NXT_SOF_23

LVDS0_LANE5_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane5 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1544	LVDS0_LANE5_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_sof_3	lane5_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane5 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane5 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_NXT_EOF_01

LVDS0_LANE5_NXT_EOF_01 is the end-of-frame synchronous code configuration register for lane5 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1548	LVDS0_LANE5_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_eof_1	lane5_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane5 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane5 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE5_NXT_EOF_23

LVDS0_LANE5_NXT_EOF_23 is the end-of-frame synchronous code configuration register for lane5 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x154C	LVDS0_LANE5_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_eof_3	lane5_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane5 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane5 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_NXT_SOL_01

LVDS0_LANE5_NXT_SOL_01 is the start synchronization code configuration register of lane5 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1550	LVDS0_LANE5_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_sol_1	lane5_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane5 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane5 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE5_NXT_SOL_23

LVDS0_LANE5_NXT_SOL_23 is the start synchronization code configuration register of lane5 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1554	LVDS0_LANE5_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_sol_3	lane5_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane5 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_sol_2	Line start synchronization code of frame 2 in LVDS, HiSPi mode, lane5 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE5_NXT_EOL_01

LVDS0_LANE5_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane5 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x1558	LVDS0_LANE5_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_eol_1	lane5_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane5 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane5_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane5 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE5_NXT_EOL_23

LVDS0_LANE5_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane5 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x155C	LVDS0_LANE5_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane5_nxt_eol_3	lane5_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane5_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane5 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane5_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane5 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_NXT_SOF_01

LVDS0_LANE6_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 lane6 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1560	LVDS0_LANE6_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_sof_1	lane6_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane6_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane6 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane6_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane6 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE6_NXT_SOF_23

LVDS0_LANE6_NXT_SOF_23 is LVDS/HiSPi mode, N+1 lane6 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1564	LVDS0_LANE6_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_sof_3	lane6_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane6 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane6 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_NXT_EOF_01

LVDS0_LANE6_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane 6 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1568	LVDS0_LANE6_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_eof_1	lane6_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane6 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane6 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE6_NXT_EOF_23

LVDS0_LANE6_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane 6 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x156C	LVDS0_LANE6_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_eof_3	lane6_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane6 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane6 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_NXT_SOL_01

LVDS0_LANE6_NXT_SOL_01 is LVDS/HiSPi mode, the N+1th frame lane6 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1570	LVDS0_LANE6_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_sol_1	lane6_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane6 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane6 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE6_NXT_SOL_23

LVDS0_LANE6_NXT_SOL_23 is the start synchronization code configuration register of lane6 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1574	LVDS0_LANE6_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_sol_3	lane6_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane6 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane6 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE6_NXT_EOL_01

LVDS0_LANE6_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane6 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x1578	LVDS0_LANE6_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_eol_1	lane6_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane6 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane6_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane6 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE6_NXT_EOL_23

LVDS0_LANE6_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane6 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x157C	LVDS0_LANE6_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane6_nxt_eol_3	lane6_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane6_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane6 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane6_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane6 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_NXT_SOF_01

LVDS0_LANE7_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane7 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1580	LVDS0_LANE7_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_sof_1	lane7_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane7_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane7 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane7_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane7 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE7_NXT_SOF_23

LVDS0_LANE7_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane7 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1584	LVDS0_LANE7_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_sof_3	lane7_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane7_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane7 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane7_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane7 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_NXT_EOF_01

LVDS0_LANE7_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane 7 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1588	LVDS0_LANE7_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_eof_1	lane7_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane7_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane7 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane7_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane7 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE7_NXT_EOF_23

LVDS0_LANE7_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane 7 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x158C	LVDS0_LANE7_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_eof_3	lane7_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane7 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane7 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_NXT_SOL_01

LVDS0_LANE7_NXT_SOL_01 is the start synchronization code configuration register of lane7 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1590	LVDS0_LANE7_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_sol_1	lane7_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sol_1	Line start synchronization code of frame 1 in LVDS, HiSPi mode, lane7 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane7 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE7_NXT_SOL_23

LVDS0_LANE7_NXT_SOL_23 is the start synchronization code configuration register of lane7 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1594	LVDS0_LANE7_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_sol_3	lane7_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane7 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane7 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE7_NXT_EOL_01

LVDS0_LANE7_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane7 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x1598	LVDS0_LANE7_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_eol_1	lane7_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane7 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane7 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE7_NXT_EOL_23

LVDS0_LANE7_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane7 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x159C	LVDS0_LANE7_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane7_nxt_eol_3	lane7_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane7 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane7_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane7 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_NXT_SOF_01

LVDS0_LANE8_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 lane8 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15A0	LVDS0_LANE8_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_sof_1	lane8_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane8 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane8 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE8_NXT_SOF_23

LVDS0_LANE8_NXT_SOF_23 is LVDS/HiSPi mode, N+1 lane8 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15A4	LVDS0_LANE8_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_sof_3	lane8_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane8 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane8 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_NXT_EOF_01

LVDS0_LANE8_NXT_EOF_01 is the end-of-frame synchronization code configuration register for the N+1 lane8 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15A8	LVDS0_LANE8_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_eof_1	lane8_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane8 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_eof_0	Frame 0 end synchronization code of frame 0 in LVDS and HiSPi mode, lane8 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE8_NXT_EOF_23

LVDS0_LANE8_NXT_EOF_23 is the end-of-frame synchronous code configuration register for lane 8 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15AC	LVDS0_LANE8_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_eof_3	lane8_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane8 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane8 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_NXT_SOL_01

LVDS0_LANE8_NXT_SOL_01 is the start synchronization code configuration register of lane8 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15B0	LVDS0_LANE8_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_sol_1	lane8_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane8 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane8 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE8_NXT_SOL_23

LVDS0_LANE8_NXT_SOL_23 is the start synchronization code configuration register of lane8 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15B4	LVDS0_LANE8_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_sol_3	lane8_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane8 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane8 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE8_NXT_EOL_01

LVDS0_LANE8_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane8 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x15B8	LVDS0_LANE8_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_eol_1	lane8_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane8 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane8_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane8 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE8_NXT_EOL_23

LVDS0_LANE8_NXT_EOL_23 is the end synchronization code configuration register of lane8 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15BC	LVDS0_LANE8_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane8_nxt_eol_3	lane8_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane8_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane8 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane8_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane8 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_NXT_SOF_01

LVDS0_LANE9_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane9 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15C0	LVDS0_LANE9_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_sof_1	lane9_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane9_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane9 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane9_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane9 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE9_NXT_SOF_23

LVDS0_LANE9_NXT_SOF_23 is the start synchronization code configuration register for lane9 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15C4	LVDS0_LANE9_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_sof_3	lane9_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane9 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane9 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_NXT_EOF_01

LVDS0_LANE9_NXT_EOF_01 is the end-of-frame synchronous code configuration register for lane9 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15C8	LVDS0_LANE9_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_eof_1	lane9_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane9 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane9 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE9_NXT_EOF_23

LVDS0_LANE9_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane9 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15CC	LVDS0_LANE9_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_eof_3	lane9_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane9 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane9 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_NXT_SOL_01

LVDS0_LANE9_NXT_SOL_01 is LVDS/HiSPi mode, the N+1th frame lane9 line start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15D0	LVDS0_LANE9_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_sol_1	lane9_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane9 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane9_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane9 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE9_NXT_SOL_23

LVDS0_LANE9_NXT_SOL_23 is the start synchronization code configuration register of lane9 line of N+1 frame in LVDS/ HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15D4	LVDS0_LANE9_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_sol_3	lane9_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane9_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane9 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane9_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane9 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE9_NXT_EOL_01

LVDS0_LANE9_NXT_EOL_01 is LVDS/HiSPi mode, end synchronization code configuration register of lane9 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x15D8	LVDS0_LANE9_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_eol_1	lane9_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane9_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane9 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane9_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane9 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE9_NXT_EOL_23

LVDS0_LANE9_NXT_EOL_23 is LVDS/HiSPi mode, end synchronization code configuration register of lane9 line of N+1 frame.

Offset Address	Register Name	Total Reset Value
0x15DC	LVDS0_LANE9_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane9_nxt_eol_3	lane9_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane9_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane9 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane9_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane9 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_NXT_SOF_01

LVDS0_LANE10_NXT_SOF_01 is LVDS/HiSPi mode, the N+1th lane10 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15E0	LVDS0_LANE10_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_sof_1	lane10_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane10_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane10 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane10_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane10 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE10_NXT_SOF_23

LVDS0_LANE10_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane10 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x15E4	LVDS0_LANE10_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_sof_3	lane10_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane10 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane10 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_NXT_EOF_01

LVDS0_LANE10_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane10 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15E8	LVDS0_LANE10_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_eof_1	lane10_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane10 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane10 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE10_NXT_EOF_23

LVDS0_LANE10_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane10 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15EC	LVDS0_LANE10_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_eof_3	lane10_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane10 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane10 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_NXT_SOL_01

LVDS0_LANE10_NXT_SOL_01 is the start synchronization code configuration register of lane10 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15F0	LVDS0_LANE10_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_sol_1	lane10_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane10 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane10 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE10_NXT_SOL_23

LVDS0_LANE10_NXT_SOL_23 is the start synchronization code configuration register of lane10 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15F4	LVDS0_LANE10_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_sol_3	lane10_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane10 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane10 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE10_NXT_EOL_01

LVDS0_LANE10_NXT_EOL_01 is the end synchronization code configuration register of lane10 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15F8	LVDS0_LANE10_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_eol_1	lane10_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eol_1	End of line synchronization code of frame 1 in LVDS, HiSPi mode, lane10 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane10 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE10_NXT_EOL_23

LVDS0_LANE10_NXT_EOL_23 is the end synchronization code configuration register of lane10 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x15FC	LVDS0_LANE10_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane10_nxt_eol_3	lane10_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane10 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane10_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane10 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_NXT_SOF_01

LVDS0_LANE11_NXT_SOF_01 is LVDS/HiSPi mode, the N+1 frame lane11 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1600	LVDS0_LANE11_NXT_SOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_sof_1	lane11_nxt_sof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sof_1	Frame start synchronization code of frame 1 in LVDS and HiSPi mode, lane11 SOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_nxt_sof_0	Frame start synchronization code of frame 0 in LVDS and HiSPi mode, lane11 SOF of frame0; In WDR mode, it is the 0th frame SOF, and in linear mode, it is SOF.

LVDS0_LANE11_NXT_SOF_23

LVDS0_LANE11_NXT_SOF_23 is LVDS/HiSPi mode, the N+1 frame lane11 frame start synchronization code configuration register.

Offset Address	Register Name	Total Reset Value
0x1604	LVDS0_LANE11_NXT_SOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_sof_3	lane11_nxt_sof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sof_3	Frame start synchronization code of frame 3 in LVDS and HiSPi mode, lane11 SOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_nxt_sof_2	Frame start synchronization code of frame 2 in LVDS and HiSPi mode, lane11 SOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_NXT_EOF_01

LVDS0_LANE11_NXT_EOF_01 is the end-of-frame synchronization code configuration register for lane11 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1608	LVDS0_LANE11_NXT_EOF_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_eof_1	lane11_nxt_eof_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eof_1	Frame end synchronization code of frame 1 in LVDS and HiSPi mode, lane11 EOF of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_nxt_eof_0	Frame end synchronization code of frame 0 in LVDS and HiSPi mode, lane11 EOF of frame0; In WDR mode, it is EOF of the 0th frame, and in linear mode, it is EOF.

LVDS0_LANE11_NXT_EOF_23

LVDS0_LANE11_NXT_EOF_23 is the end-of-frame synchronization code configuration register for lane11 of frame N+1 in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x160C	LVDS0_LANE11_NXT_EOF_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_eof_3	lane11_nxt_eof_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eof_3	Frame end synchronization code of frame 3 in LVDS and HiSPi mode, lane11 EOF of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_nxt_eof_2	Frame end synchronization code of frame 2 in LVDS and HiSPi mode, lane11 EOF of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_NXT_SOL_01

LVDS0_LANE11_NXT_SOL_01 is the start synchronization code configuration register of lane11 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1610	LVDS0_LANE11_NXT_SOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_sol_1	lane11_nxt_sol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sol_1	Line start synchronization code of frame 1 in LVDS and HiSPi mode, lane11 SOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW	lane11_nxt_sol_0	Line start synchronization code of frame 0 in LVDS and HiSPi mode, lane11 SOL of frame0; In WDR mode, it is the 0th frame SOL, and in linear mode, it is SOL.

LVDS0_LANE11_NXT_SOL_23

LVDS0_LANE11_NXT_SOL_23 is the start synchronization code configuration register of lane11 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1614	LVDS0_LANE11_NXT_SOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_sol_3	lane11_nxt_sol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane11_nxt_sol_3	Line start synchronization code of frame 3 in LVDS and HiSPi mode, lane11 SOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane11_nxt_sol_2	Line start synchronization code of frame 2 in LVDS and HiSPi mode, lane11 SOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LANE11_NXT_EOL_01

LVDS0_LANE11_NXT_EOL_01 is the end synchronization code configuration register of lane11 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x1618	LVDS0_LANE11_NXT_EOL_01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_eol_1	lane11_nxt_eol_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane11_nxt_eol_1	End-of-line synchronization code of frame 1 in LVDS, HiSPi mode, lane11 EOL of frame1; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane11_nxt_eol_0	End-of-line synchronization code of frame 0 in LVDS and HiSPi modes, lane11 EOL of frame0; In WDR mode, it is the 0th frame EOL, and in linear mode, it is EOL.

LVDS0_LANE11_NXT_EOL_23

LVDS0_LANE11_NXT_EOL_23 is the end synchronization code configuration register of lane11 line of N+1 frame in LVDS/HiSPi mode.

Offset Address	Register Name	Total Reset Value
0x161C	LVDS0_LANE11_NXT_EOL_23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lane11_nxt_eol_3	lane11_nxt_eol_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW lane11_nxt_eol_3	End-of-line synchronization code of frame 3 in LVDS, HiSPi mode, lane11 EOL of frame3; It is only configurable in WDR mode, and it is invalid in linear mode.
[15:0]	RW lane11_nxt_eol_2	End-of-line synchronization code of frame 2 in LVDS, HiSPi mode, lane11 EOL of frame2; It is only configurable in WDR mode, and it is invalid in linear mode.

LVDS0_LI_WORD0

LVDS0_LI_WORD0 is the LI register of frame 0 in LVDS DOL mode.

Offset Address	Register Name	Total Reset Value
0x1620	LVDS0_LI_WORD0	0x0211_0201

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	li_word0_1	li_word0_0
Reset	0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 1	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1

Bits	Access Name	Description
[31:16]	RW li_word0_1	The value of Line Information (N+1 Frame) of LEF in DOL mode.
[15:0]	RW li_word0_0	The value of Line Information (N Frame) of LEF in DOL mode.

LVDS0_LI_WORD1

LVDS0_LI_WORD1 is the first frame LI register of LVDS DOL mode.

Offset Address	Register Name	Total Reset Value
0x1624	LVDS0_LI_WORD1	0x0212_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word1_1																li_word1_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	li_word1_1	The value of Line Information (N+1 Frame) of SEF1 in DOL mode.
[15:0]	RW	li_word1_0	The value of Line Information (N Frame) of SEF1 in DOL mode.

LVDS0_LI_WORD2

LVDS0_LI_WORD2 is the LI register of frame 2 in LVDS DOL mode.

Offset Address	Register Name	Total Reset Value
0x1628	LVDS0_LI_WORD2	0x0214_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word2_1																li_word2_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	li_word2_1	The value of Line Information (N+1 Frame) of SEF2 in DOL mode.
[15:0]	RW	li_word2_0	The value of Line Information (N Frame) of SEF2 in DOL mode.

LVDS0_LI_WORD3

LVDS0_LI_WORD3 is the third frame LI register of LVDS DOL mode.

Offset Address	Register Name	Total Reset Value
0x162C	LVDS0_LI_WORD3	0x0218_0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word3_1																li_word3_0															
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	li_word3_1	The value of Line Information (N+1 Frame) of SEF3 in DOL mode.
[15:0]	RW	li_word3_0	The value of Line Information (N Frame) of SEF3 in DOL mode.

LVDS0_IMGSIZE0_STATIS

LVDS0_IMGSIZE0_STATIS is the statistics register of LVDS LEF image width and height.

Offset Address	Register Name	Total Reset Value
0x1680	LVDS0_IMGSIZE0_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_imgheight0	lvds_imgwidth0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight0	In LVDS/HiSPi mode, the image height transmitted by virtual channel0.
[15:0]	RO	lvds_imgwidth0	In LVDS/HiSPi mode, the image width transmitted by virtual channel0.

LVDS0_IMGSIZE1_STATIS

LVDS0_IMGSIZE1_STATIS is the statistics register of LVDS SEF1 image width and height.

Offset Address	Register Name	Total Reset Value
0x1684	LVDS0_IMGSIZE1_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_imgheight1	lvds_imgwidth1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight1	In LVDS/HiSPi mode, the image height transmitted by virtual channel1.
[15:0]	RO	lvds_imgwidth1	In LVDS/HiSPi mode, the image width transmitted by virtual channel1.

LVDS0_IMGSIZE2_STATIS

LVDS0_IMGSIZE2_STATIS is the statistics register of LVDS SEF2 image width and height.

Offset Address	Register Name	Total Reset Value
0x1688	LVDS0_IMGSIZE2_STATIS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_imgheight2	lvds_imgwidth2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RO	lvds_imgheight2 In LVDS/HiSPi mode, the image height transmitted by virtual channel2.
[15:0]	RO	lvds_imgwidth2 In LVDS/HiSPi mode, the image width transmitted by virtual channel2.

LVDS0_IMGSIZE3_STATIS

LVDS0_IMGSIZE3_STATIS is the statistics register of LVDS SEF3 image width and height.

Offset Address	Register Name	Total Reset Value
0x168C	LVDS0_IMGSIZE3_STATIS	0x0000_0000

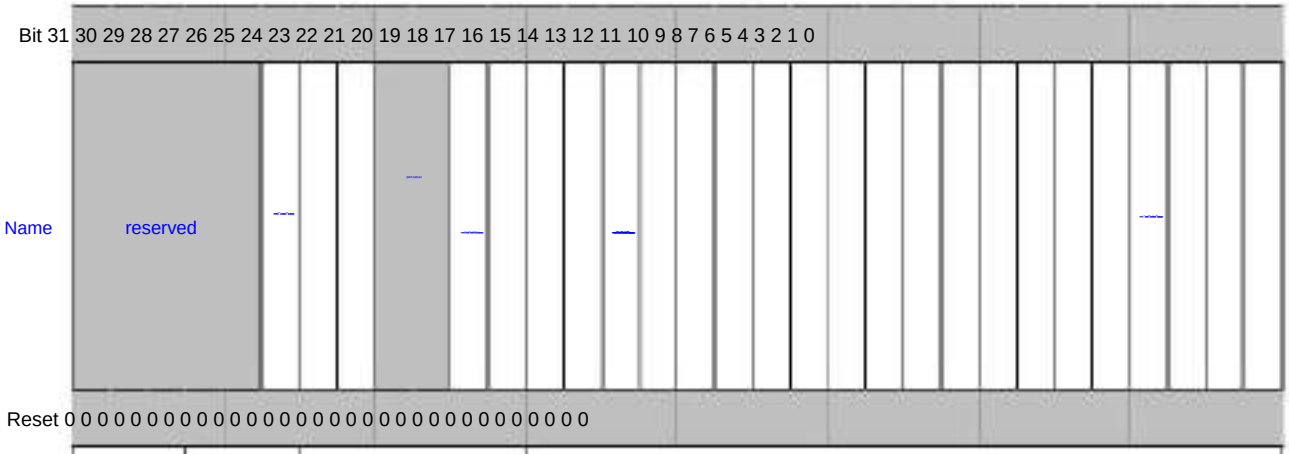
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	lvds_imgheight3	lvds_imgwidth3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RO	lvds_imgheight3 In LVDS/HiSPi mode, the image height transmitted by virtual channel3.
[15:0]	RO	lvds_imgwidth3 In LVDS/HiSPi mode, the image width transmitted by virtual channel3.

LVDS0_CTRL_INT_RAW

LVDS0_CTRL_INT_RAW is the LVDS read data raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F0	LVDS0_CTRL_INT_RAW	0x0000_0000



Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	WC	link2_rderr_raw	Link2 read data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[25]	WC	link1_rderr_raw	Link1 read data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[24]	WC	link0_rderr_raw	Link0 read data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[23:22]	RO	reserved	reserve.
[21]	WC	lvds_stat_err_raw	LVDS Status Error Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[20]	WC	status. lane11_sync_err_ra In	Lane11 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[19]	WC	status. lane10_sync_err_ra In	Lane10 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[18]	WC	lane9_sync_err_ra In	Lane9 synchronous error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

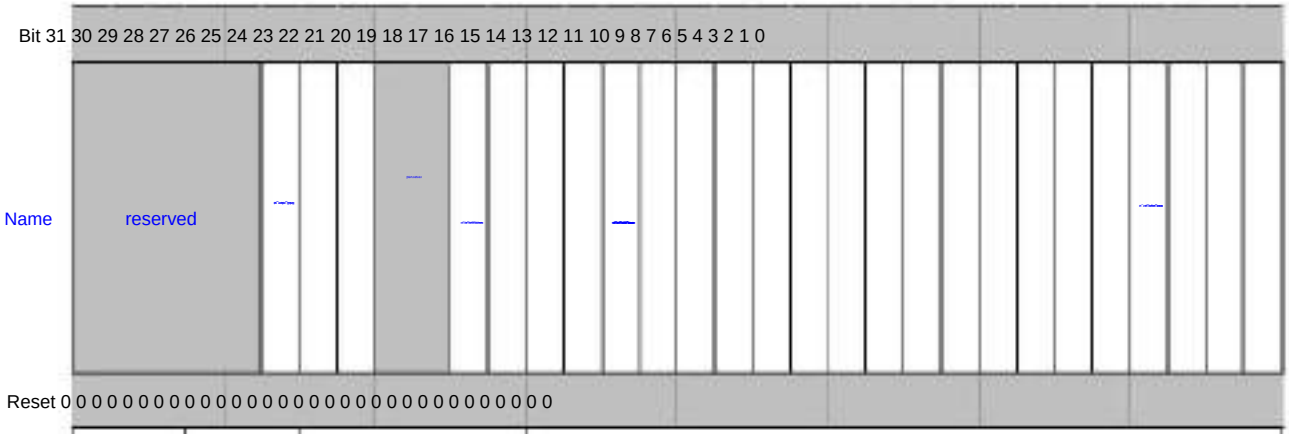
[17] WC		lane8_sync_err_ra In	Lane8 synchronous error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[16] WC		lane7_sync_err_ra In	Lane7 synchronous error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[15] WC		lane6_sync_err_ra In	Lane6 synchronous error raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[14] WC		lane5_sync_err_ra In	Lane5 synchronous error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[13] WC		status. lane4_sync_err_ra In	Lane4 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[12] WC		status. lane3_sync_err_ra In	Lane3 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[11] WC		lane2_sync_err_ra In	Lane2 synchronous error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[10] WC		status. lane1_sync_err_ra In	Lane1 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[9] WC		status. lane0_sync_err_ra In	Lane0 synchronous error raw interrupt 0: no raw interrupt; 1: There is a raw interrupt.
[8] WC		link2_hsync_err_ra In	Link2 hsync sync error raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.
[7] WC		link2_vsync_err_ra In	Link2 vsync sync error raw interrupt status. 0: no raw interrupt; 1: There is a raw interrupt.

[6] WC	link2_wrerr_raw		Link2 write data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[5] WC		link1_hsync_err_ra 0: In	Link1 hsync sync error raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[4] WC		link1_vsync_err_ra 0: In	Link1 vsync sync error raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[3] WC	link1_wrerr_raw		Link1 write data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[2] WC		link0_hsync_err_ra 0: In	Link0 hsync sync error raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[1] WC		link0_vsync_err_ra 0: In	Link0 vsync sync error raw interrupt status. no raw interrupt; 1: There is a raw interrupt.
[0] WC	link0_wrerr_raw		Link0 write data error raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

LVDS0_CTRL_INT

LVDS0_CTRL_INT is the LVDS read data interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F4	LVDS0_CTRL_INT	0x0000_0000



Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	RO	link2_rderr_st	Link2 read data error interrupt status. 0: no interrupt; 1: There is an interrupt.
[25]	RO	link1_rderr_st	Link1 read data error interrupt status. 0: no interrupt; 1: There is an interrupt.
[24]	RO	link0_rderr_st	Link0 read data error interrupt status. 0: no interrupt; 1: There is an interrupt.
[23:22]	RO	reserved	reserve.
[21]	RO	lvds_stat_err_st	LVDS status error interrupt status. 0: no interrupt; 1: There is an interrupt.
[20]	RO	lane11_sync_err_st	Lane11 sync error interrupt status. 0: no interrupt; 1: interrupted.
[19]	RO	lane10_sync_err_st	Lane10 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[18]	RO	lane9_sync_err_st	Lane9 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.

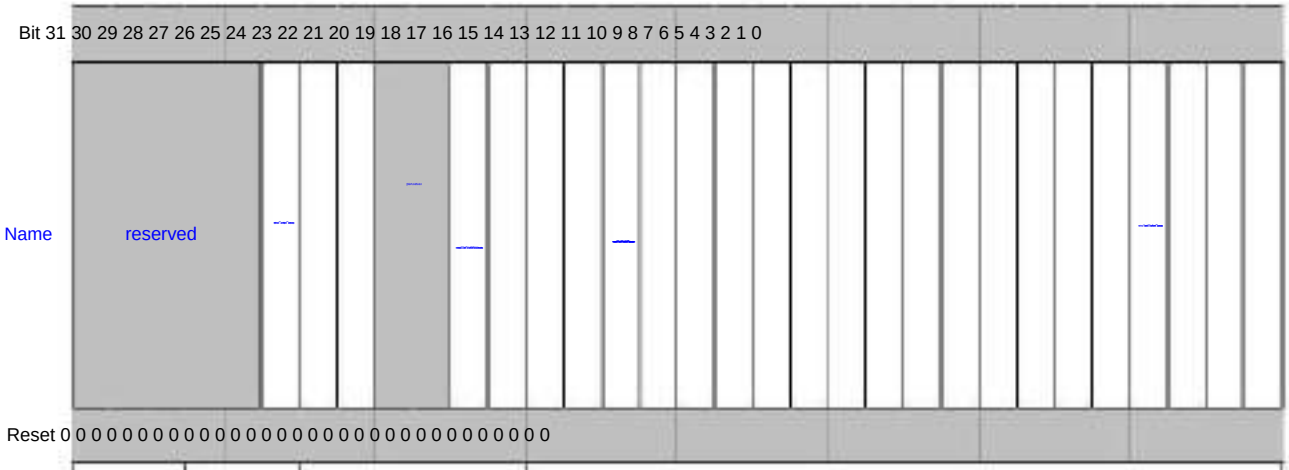
[17] RO		lane8_sync_err_st	Lane8 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[16] RO		lane7_sync_err_st	Lane7 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[15] RO		lane6_sync_err_st	Lane6 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[14] RO		lane5_sync_err_st	Lane5 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[13] RO		lane4_sync_err_st	Lane4 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[12] RO		lane3_sync_err_st	Lane3 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[11] RO		lane2_sync_err_st	Lane2 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[10] RO		lane1_sync_err_st	Lane1 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[9]	RO	lane0_sync_err_st	Lane0 sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[8]	RO	link2_hsync_err_st	Link2 hsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[7]	RO	link2_vsync_err_st	Link2 vsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.

[6]	RO	link2_wrerr_st	Link2 write data error interrupt status. 0: no interrupt; 1: There is an interrupt.
[5]	RO	link1_hsync_err_st	Link1 hsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[4]	RO	link1_vsync_err_st	Link1 vsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	link1_wrerr_st	Link1 write data error interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	link0_hsync_err_st	Link0 hsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[1]	RO	link0_vsync_err_st	Link0 vsync sync error interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	link0_wrerr_st	Link0 write data error interrupt status. 0: no interrupt; 1: There is an interrupt.

LVDS0_CTRL_INT_MSK

LVDS0_CTRL_INT_MSK is LVDS read data interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x16F8	LVDS0_CTRL_INT_MSK	0x0000_0000



Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	RW	link2_rderr_msk	Link2 read data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[25]	RW	link1_rderr_msk	Link1 read data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[24]	RW	link0_rderr_msk	Link0 read data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[23:22]	RO	reserved	reserve.
[21]	RW	lvds_stat_err_st_ms k	LVDS status error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[20]	RW	lane11_sync_err_m sk	Lane11 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[19]	RW	lane10_sync_err_m sk	Lane10 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.

[18] RW		enable. lane9_sync_err_msk	Lane9 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[17] RW		enable. lane8_sync_err_msk	Lane8 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[16] RW		enable. lane7_sync_err_msk	Lane7 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[15] RW		enable. lane6_sync_err_msk	Lane6 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[14] RW		enable. lane5_sync_err_msk	Lane5 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[13] RW		enable. lane4_sync_err_msk	Lane4 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[12] RW		enable. lane3_sync_err_msk	Lane3 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[11] RW		enable. lane2_sync_err_msk	Lane2 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[10] RW		enable. lane1_sync_err_msk	Lane1 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[9] RW		enable. lane0_sync_err_msk	Lane0 synchronous error interrupt status 0: mask interrupt; 1: Interrupts are enabled.
[8] RW		enable. link2_hsync_err_m sk	Link2 hsync sync error interrupt status 0: mask interrupt; 1: Interrupts are enabled.

[7] RW		link2_vsync_err_m 0:	Link2 vsync sync error interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[6] RW	link2_wrerr_msk		Link2 write data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[5] RW		link1_hsync_err_m 0:	Link1 hsync sync error interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[4] RW		link1_vsync_err_m 0:	Link1 vsync sync error interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[3] RW	link1_wrerr_msk		Link1 write data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[2] RW		link0_hsync_err_m 0:	Link0 hsync sync error interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[1] RW		link0_vsync_err_m 0:	Link0 vsync sync error interrupt status enable. mask interrupt; sk 1: Interrupts are enabled.
[0] RW	link0_wrerr_msk		Link0 write data error interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.

LANE_ID0_CHN0

LANE_ID0_CHN0 is the configuration register for each LANE priority of Link0.

Offset Address	Register Name	Total Reset Value
0x1700	LANE_ID0_CHN0	0x0000_3210

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	lane3_id	lane2_id	lane1_id	lane0_id
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0	1 0 0 0	0 1 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:12]	RW	lane3_id	Indicates the channel number of Lane3, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane3.
[11:8]	RW	lane2_id	Indicates the channel number of Lane2, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane2.
[7:4]	RW	lane1_id	Indicates the channel number of Lane1, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane1.
[3:0]	RW	lane0_id	Indicates the channel number of Lane0, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane0.

LANE_ID1_CHN0

LANE_ID1_CHN0 is the configuration register for each LANE priority of Link1.

Offset Address	Register Name	Total Reset Value
0x1704	LANE_ID1_CHN0	0x0000_7654

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	lane7_id	lane6_id	lane5_id	lane4_id
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1	0 1	1 0 0 1	0 1 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:12]	RW	lane7_id	Indicates the channel number of Lane7, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane7.
[11:8]	RW	lane6_id	Indicates the channel number of Lane6, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane6.
[7:4]	RW	lane5_id	Indicates the channel number of Lane5, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane5.

[3:0] RW	lane4_id		Indicates the channel number of Lane4, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane4.

LANE_ID2_CHN0

LANE_ID2_CHN0 is the configuration register for each LANE priority of Link2.

Offset Address	Register Name	Total Reset Value
0x1708	LANE_ID2_CHN0	0x0000_BA98

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	lane11_id	lane10_id	lane9_id	lane8_id
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1	1 0 1 0	1 0 0 1	1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:12]	RW	lane11_id	Indicates the channel number of Lane11, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane11.
[11:8]	RW	lane10_id	Indicates the channel number of Lane10, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane10.
[7:4]	RW	lane9_id	Indicates the channel number of Lane9, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane9.
[3:0]	RW	lane8_id	Indicates the channel number of Lane8, the value range is 0~11. The value is expressed as the actual channel number of the image sensor connected to Lane8.

ALIGN0_INT_RAW

ALIGN0_INT_RAW is the MIPI_ALIGN raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x17F0	ALIGN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	WC	err_lane11_raw	MIPI_ALIGN lane11 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[11]	WC	err_lane10_raw	MIPI_ALIGN lane10 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[10]	WC	err_lane9_raw	MIPI_ALIGN lane9 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[9]	WC	err_lane8_raw	MIPI_ALIGN lane8 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[8]	WC	err_lane7_raw	MIPI_ALIGN lane7 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[7]	WC	err_lane6_raw	MIPI_ALIGN lane6 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[6]	WC	err_lane5_raw	MIPI_ALIGN lane5 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

[5] WC err_lane4_raw			MIPI_ALIGN lane4 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[4] WC err_lane3_raw			MIPI_ALIGN lane3 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[3] WC err_lane2_raw			MIPI_ALIGN lane2 raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[2] WC err_lane1_raw			MIPI_ALIGN lane1 raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[1] WC err_lane0_raw			MIPI_ALIGN lane0 Raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.
[0] WC err_full_raw			MIPI_ALIGN FIFO raw interrupt status. 0: no original interrupt; 1: There is a raw interrupt.

ALIGN0_INT

ALIGN0_INT is MIPI_ALIGN interrupt status register.

Offset Address	Register Name	Total Reset Value
0x17F4	ALIGN0_INT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.

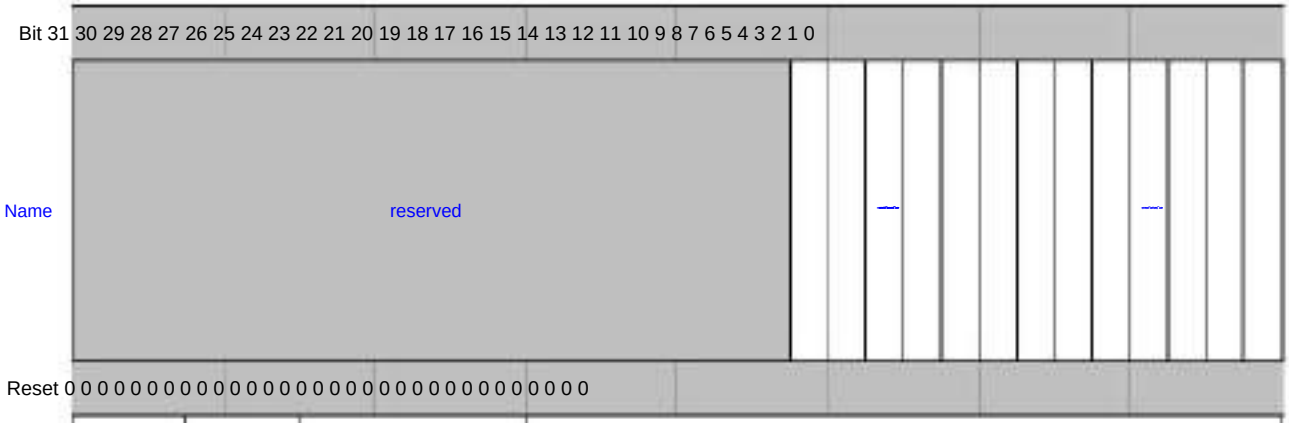
[12] RO		err_lane11_st	MIPI_ALIGN lane11 interrupt status. 0: no interrupt; 1: There is an interrupt.
[11] RO		err_lane10_st	MIPI_ALIGN lane10 interrupt status. 0: no interrupt; 1: There is an interrupt.
[10] RO		err_lane9_st	MIPI_ALIGN lane9 interrupt status. 0: no interrupt; 1: There is an interrupt.
[9]	RO	err_lane8_st	MIPI_ALIGN lane8 interrupt status. 0: no interrupt; 1: There is an interrupt.
[8]	RO	err_lane7_st	MIPI_ALIGN lane7 interrupt status. 0: no interrupt; 1: There is an interrupt.
[7]	RO	err_lane6_st	MIPI_ALIGN lane6 interrupt status. 0: no interrupt; 1: There is an interrupt.
[6]	RO	err_lane5_st	MIPI_ALIGN lane5 interrupt status. 0: no interrupt; 1: There is an interrupt.
[5]	RO	err_lane4_st	MIPI_ALIGN lane4 interrupt status. 0: no interrupt; 1: There is an interrupt.
[4]	RO	err_lane3_st	MIPI_ALIGN lane3 interrupt status. 0: no interrupt; 1: There is an interrupt.
[3]	RO	err_lane2_st	MIPI_ALIGN lane2 interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	err_lane1_st	MIPI_ALIGN lane1 interrupt status. 0: no interrupt; 1: There is an interrupt.

[1]	RO	err_lane0_st	MIPI_ALIGN lane0 interrupt status. 0: no interrupt; 1: There is an interrupt.
[0]	RO	err_full_st	MIPI_ALIGN FIFO interrupt status. 0: no interrupt; 1: There is an interrupt.

ALIGN0_INT_MSK

ALIGN0_INT_MSK is the MIPI_ALIGN interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x17F8	ALIGN0_INT_MSK	0x0000_0000



Bits	Access Name		Description
[31:13]	RO	reserved	reserve.
[12]	RW err_lane11_mask		MIPI_ALIGN lane11 interrupt status enable. 0: mask interrupt; 1: enable interrupt.
[11]	RW err_lane10_mask		MIPI_ALIGN lane10 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[10]	RW err_lane9_mask		MIPI_ALIGN lane9 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[9]	RW err_lane8_mask		MIPI_ALIGN lane8 interrupt status enable. 0: mask interrupt; 1: enable interrupt.

[8] RW	err_lane7_mask		MIPI_ALIGN lane7 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[7] RW	err_lane6_mask		MIPI_ALIGN lane6 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[6] RW	err_lane5_mask		MIPI_ALIGN lane5 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[5] RW	err_lane4_mask		MIPI_ALIGN lane4 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[4] RW	err_lane3_mask		MIPI_ALIGN lane3 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[3] RW	err_lane2_mask		MIPI_ALIGN lane2 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[2] RW	err_lane1_mask		MIPI_ALIGN lane1 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[1] RW	err_lane0_mask		MIPI_ALIGN lane0 interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.
[0] RW	err_full_mask		MIPI_ALIGN FIFO interrupt status enable. 0: mask interrupt; 1: Interrupts are enabled.

Table of contents

illustration catalog

table of contents

10 ISP

10.1 Function Introduction

The Hi3519V100 ISP module supports standard Sensor image data processing, including automatic white balance, automatic exposure,
Basic functions such as Demosaic, dead pixel correction and digital image stabilization also support advanced processing functions such as WDR, DRC and noise reduction. The main image processing functions supported by Hi3519V100 ISP are as follows:

- Support black level correction
- Support static and dynamic dead point correction, dead point cluster correction Support
- bayer noise reduction Support
- fixed noise elimination Advanced
- demosaic processing Support gamma
- correction Support dynamic range
- compression (DRC) Support Sensor internal synthesis
- wide dynamic function (WDR) Support 4-in-1, 3-in-1 1. 2-in-1 wide dynamic function
- (WDR) supports automatic white balance
- Support automatic exposure
- Support auto focus, support
- 3A related statistical information output
- Supports lens shading correction
- Support image sharpening
- Support digital image
- stabilization Support automatic defog
- processing Support color management and enhancement

Processing power and other features:

- Maximum support for 14 bit bayer data input Maximum support
- for image resolution 4608×3456
- Support minimum image resolution 480×240

4608×3456 resolution supports maximum frame rate 15fps 4152×2174

resolution supports maximum frame rate 30fps Minimum horizontal

blanking area 64 pixels

Minimum vertical blanking area 30 lines

10.2 General overview

Functional block diagram

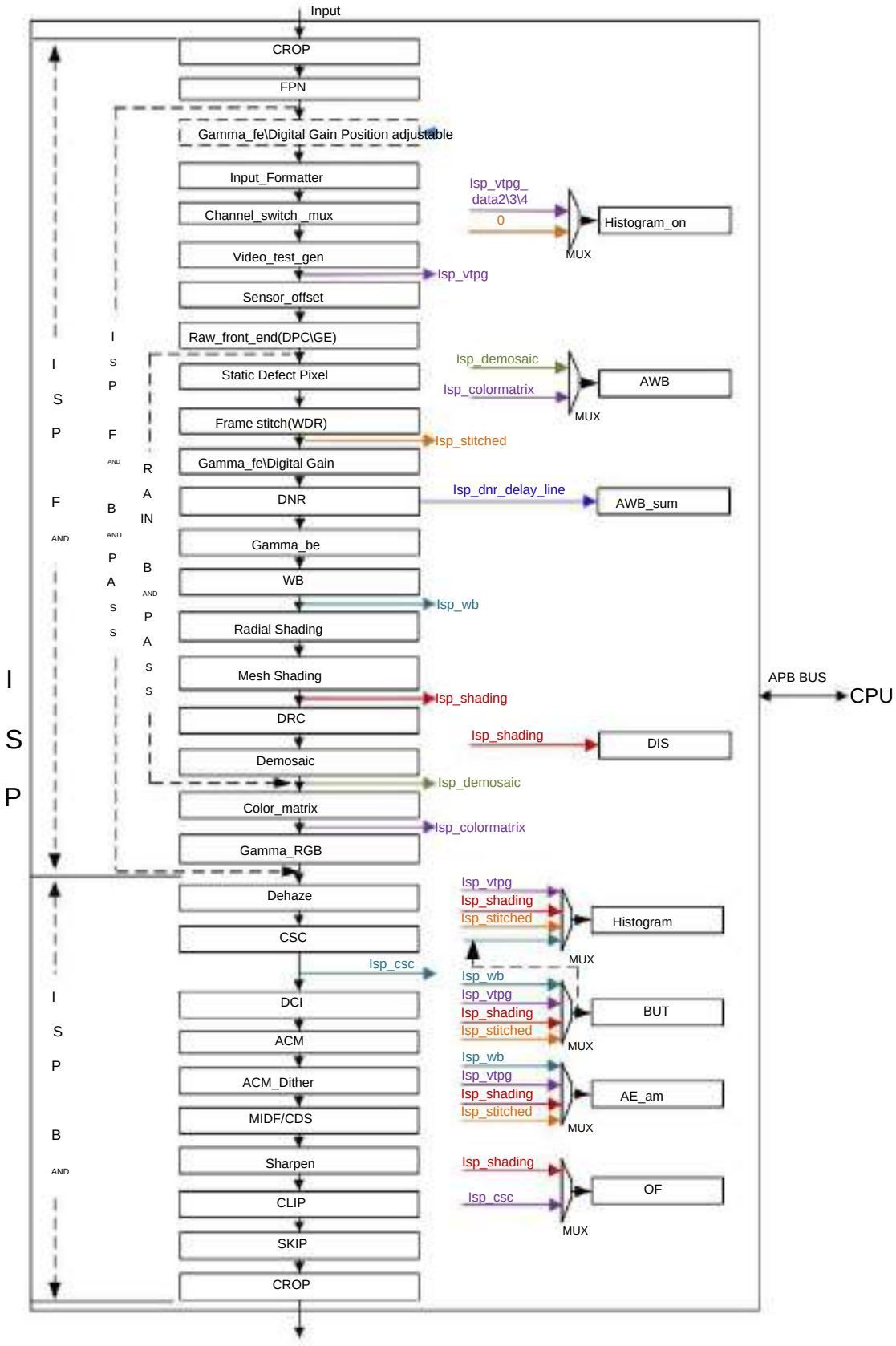
The base address of the ISP register is 0x11380000, and the ISP uses the base address plus the offset address to locate the register address.

The functional structure diagram of ISP is shown in Figure 10-1 . Both this figure and ISP_FE mentioned in this article refer to the part before Dehaze (not included) in the ISP pipeline, and ISP_BE refers to the part after Dehaze (included) in the ISP pipeline.

说明

In this article, ISP uses U*.*, S*.* to represent unsigned and signed numbers. For example: U8.8 indicates that the data type is unsigned, the integer part is 8 bits, and the fractional part is 8 bits; similarly, S8.8 indicates that the data type is signed, the integer part is 8 bits (including 1 bit sign bit), and the fractional part is 8 bits.

Figure 10-1 ISP structure diagram



Operating mode

Support maximum raw 14bit RGB bayer data input When the input

data bit width is less than 14bit, the input image data will be automatically aligned with high bits and filled with zeros at low bits. In this mode, any RGrGbB order is supported, and the three registers ISPFE_RGGB_START, ISPFE_RGGB_START, ISP_DIS_CTRL_F, ISP_FPN_CTRL_F. Support 4 in 1, 3 in 1,

2 in 1 WDR

(1) 2-in-1 supports maximum resolution up to 4152×2174. (2) 3-in-1

and 4-in-1 supports maximum resolution up to 1920×1080. Support infrared mode

This mode needs to

configure the Skip module ISP_SKIP_C_CFG to 0x00000000, discard the C (U, V) component, so that the ISP only outputs the Y component image data. Support external ISP In external ISP

mode, it can support

YUV data format input, and the key parameters are shown in Table 10-1 .

Table 10-1 Key parameters of external ISP

parameter name	describe
BUF_MODE (0x11380070) The register in the video interface VICAP, line_buf input data mode	Mode. 0: RAW data; 1ÿYUV422ÿ
ISP_SEL[6:4] (0x11380050) ISP_BE input data selection selection.	000: ISP_BE is connected with ISP_FE (for RAW input); 001: ISP_BE is connected with LINE_BUF (for YUV input); 011: ISP_BE is connected with SRC0 (for DEBUG); 100: ISP_BE is connected with SRC1 (for DEBUG); 101: ISP_BE is connected with SRC2 connection (used by DEBUG); 110: connection between ISP_BE and SRC3 (used by DEBUG); rest: reserved.

External ISP mode needs to set the ISP_SEL[6:4] register to 0x1, so that the ISP raw domain module is masked; and the BUF_MODE of the video interface VICAP also needs to be set to 0x1, indicating that the line_buf input data of VICAP is YUV422, and the Dehaze module is turned off.

Some modules are supported with

adjustable positions. The modules Gamma_fe\Digital Gain , AWB, AF, Histogram, AE, and AE_SUM support adjustable positions. The relevant parameters are shown in Table 10-2 .

Table 10-2 Key parameters of adjustable module position

ISP_MODULE_POS	describe
ISPFE_AE_SWITCH[1:0]	AE statistics location selection register. 00: after static white balance; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.
ISPFE_AE_SWITCH[17:16]	AE SUM statistics location selection register. 00: after static white balance; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.
ISPFE_AWB_SWITCH[0]	RGB domain AWB statistics module position selection register. 0: before the color matrix; 1: After the color matrix.
ISPFE_HISTOGRAM_SWITCH[1:0] AE global histogram position selection register. 00: at the same position as AE; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.	
ISPFE_MODULE_BYPASS[0] Module Gamma_fe	Digital Gain position selection register. 0: behind WDR stitching; 1: in front of ISP FE.
ISPFE_MODULE_BYPASS[1]	Digital gain position selection register. 0: behind the module FE gamma LUTs; 1: before the module FE gamma LUTs.
ISP_SEL[16](0x11380050)	AF Input data selection. 0: AF is connected with ISP_FE; 1: AF is connected with ISP_BE;

Memory read and write scheme

Table 10-3 Module direct read and write MEM address mapping

MEM offset address range	The module to which the MEM belongs
0x21200~0x2127Cÿ0x21280~0x212FCÿ 0x21300~0x2137Cÿ0x21380~0x213FC	NOISE_PROFILE_FRAME_STITCH
0x21540~0x21560	DNR_SHADING
0x21580~0x215FCÿ0x21600~0x2167Cÿ 0x21680~0x216FCÿ0x21700~0x2177C	NOISE_PROFILE_RAW_FRONTEND
0x21800~0x2187C	NOISE_PROFILE_LUT
0x21880~0x218FC	NOISE_PROFILE_DEMOSAIC
0x21900~0x219FC	AEXP_WEIGHT
0x21B00~0x21EFC	AWB_WEIGHT
0x22800~0x22880ÿ0x23000~0x23400	GAMMA_FE
0x24800~0x24880ÿ0x25000~0x25400	GAMMA_BE
0x26000~0x26200ÿ0x26400~0x26600ÿ 0x26800~0x26A00	RADIAL_SHADING
0x28000~0x2DFFC	METERING_MEM
0x30000~0x33FFC	DEFECT_PIXEL_MEM
0x34000~0x34FFCÿ0x35000~0x353FCÿ 0x35400~0x357FCÿ0x35800~0x35BFC	HISTOGRAM1_MEM
0x37000~0x37400	GAMMA_RGB_MEM
0x38000~0x38200ÿ0x38800~0x38A00	DRC
0x39000~0x393FC	CMD_QUEUES
0x3C000~0x3EFFC	MESH_SHADING

Table 10-4 Module indirect read and write MEM address mapping

MEM offset address range	The module to which the MEM belongs
0x62488~0x6249C	DIS
0x63a80~0x63a8C	FPN
0x46280~0x462BC	DEHAZE

As shown in Table 10-3, the ISP Memory adopts direct read and write, and its read and write method is the same as that of ordinary registers; the ISP Memory shown in Table 10-4 adopts the indirect read and write method, and the memory address segment of the module contains Read data register (RDATA), read address register (RADDR), write data register (WDATA), write address register (WADDR), the indirect read and write methods of ISP Memory are as follows:

The steps to read Memory are as follows:

Step 1. Write the starting address of the data to be read in Memory to the read address register (RADDR);

Step 2. Continuously read the read data register (RDATA). Every time it is read, the address will be automatically increased by 1 within the logic.

----Finish

The steps to write to Memory are as follows:

Step 3. Write data to the write address register (WADDR) and store the starting address in Memory;

Step 4. Write data to the write data register (WADDR) continuously, and the address will be automatically increased by 1 within the logic every time it is written.

----Finish

10.3 ISP interrupt system

Functional description

Support 23 independent interrupts, of which 16 independent interrupts (shown in Table 10-5 , int0~int15) can be selected from 22 interrupt sources, the 22 interrupt sources include statistics of AE, AWB and histogram completion Interrupts, frame start interrupts of some modules on the pipeline, and frame end interrupts of some modules on the pipeline, see Table 10-6 for details .

As shown in Table 10-7, by assigning interrupt vectors corresponding to 22 interrupt sources to the registers interrupt0_source~interrupt15_source as described in Table 10-6 , the corresponding interrupt can be reported.

Table 10-5 Interrupt indication register

offset address	event name	32BIT bit distribution	Description (write 1 to clear, 0: no interrupt 1: interrupt)
0x400F0	reserved	31:17 Reserved.	
	acm_para_finish	16	ACM lookup table load complete interrupt status.
	reserved	15:4	reserve.
	fstart_delay	3	Trigger delay can be configured with interrupt.
	cfg_loss	2 registers configure the lost interrupt status.	

offset address	event name	32BIT bit distribution	Description (write 1 to clear, 0: no interrupt 1: interrupt)
	update_cfg	1	Register update interrupt status.
	fstart	0	ISP start of frame interrupt indication register.
0x600F0	reserved	31:18 Reserved.	
	fe_fstart	17	ISP FE Start of frame interrupt.
	int_dis_stat	16	DIS Current frame statistical completion interrupt.
	int15	15	ISP No. 15 interrupt indication register.
	int14	14	ISP No. 14 interrupt indication register.
	int13	13	ISP No. 13 interrupt indication register.
	int12	12	ISP No. 12 interrupt indication register.
	int11	11	ISP No. 11 interrupt indication register.
	int10	10	ISP No. 10 interrupt indication register.
	int9	9	ISP No. 9 interrupt indication register.
	you8	8	ISP No. 8 interrupt indication register.
	int7	7	ISP No. 7 interrupt indication register.
	int6	6	ISP No. 6 interrupt indication register.
	you5	5	ISP No. 5 interrupt indication register.
	int4	4	ISP No. 4 interrupt indication register.
	int3	3	ISP No. 3 interrupt indication register.
	int2	2	ISP No. 2 interrupt indication register.
	int1	1	ISP No. 1 interrupt indication register.

offset address	event name	32BIT bit distribution	Description (write 1 to clear, 0: no interrupt 1: interrupt)
	int0	0	ISP No. 0 interrupt indication register.

Table 10-6 Optional interrupt event sources

type	interrupt event source	interrupt vector
Statistics complete interrupt auto exposure		8
	auto white balance	9
	auto exposure histogram	11
	per exposure auto exposure histograms	12
	auto exposure sum	13
	auto white balance sum	14
start of frame interrupt	isp input	24
	wdr stitch	25
	static defect pixel	26
	dnr	27
	shading	28
	drc	29
	demosaic	30
	isp output	31
frame complete interrupt	isp input	16
	wdr stitch	17
	static defect pixel	18
	dnr	19
	shading	20
	drc	21
	demosaic	22
	isp output	23

Table 10-7 Key parameters of optional interrupt sources

parameter name	describe
interrupt0_source~ interrupt15_source ÿ0x20080~0x2009Cÿ	There are 16 independent interrupt selection registers, and the interrupt source can be selected from the 22 interrupt sources described in Table 10-6, just write the corresponding interrupt vector.

interrupt timing

The location of many interrupts is determined by the ISP module switch and register configuration. Figure 10-2 is a schematic diagram of each interrupt position. Note that the interrupt positions in the figure are arranged in a temporal relationship within a frame. Table 10-8 is the correspondence table between the interrupt sequence number and the interrupt event in Figure 10-2 , and lists the number of lines between the interrupt and the first rising edge of VALID_I, and the number of lines between the last falling edge of VALID_I.

Figure 10-2 Schematic diagram of interrupt timing

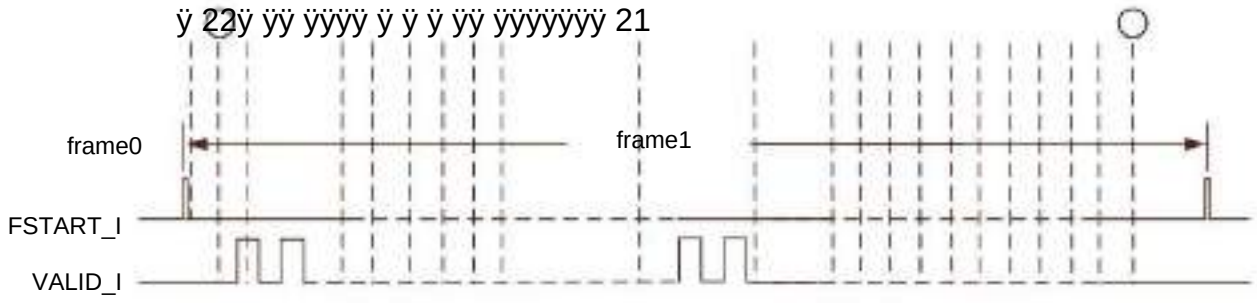


Table 10-8 Interrupt Timing

serial number	interrupt event	VALID_I The number of lines away from the first rising edge	VALID_I The number of lines away from the last falling edge
•1	fe_fstart/be_fstart/be_update_cfg/be_cfg_loss	THAT	THAT
•2	isp inputÿ24ÿ	0	THAT
•3	static defect pixelÿ26ÿ •4 wdr stitchÿ25ÿ	2	THAT
		3	THAT
•5	dnrÿ27ÿ shadingÿ28ÿ	11	THAT
•6	drcÿ29ÿ	12	THAT
•7	demosaicÿ30ÿ	16	THAT
•8	isp outputÿ31ÿ	18	THAT

serial number	interrupt event	VALID_I The number of lines away from the first rising edge	VALID_I The number of lines away from the last falling edge
•9	int_dis_stat •10 isp input	THAT	THAT
ÿ16ÿ •11	per exposure auto	THAT	0
exposure	histogramsÿ12ÿ	THAT	1
•12	static defect pixelÿ18ÿ	THAT	2
•13	wdr stitchÿ17ÿ	THAT	3
•14	dnrÿ19ÿ shadingÿ20ÿ	THAT	11
•15	drcÿ21ÿ	THAT	12
•16	auto exposure sumÿ13ÿ auto exposureÿ8ÿ	THAT	14
•17	auto exposure histogramÿ11ÿ	THAT	15
•18	demosaicÿ22ÿ	THAT	16
•19	isp outputÿ23ÿ auto white balanceÿ9ÿ	THAT	18
•20	auto white balance sumÿ14ÿ	THAT	21
•21	be_fstart_delay	THAT	THAT
•22	acm_para_finish	THAT	THAT

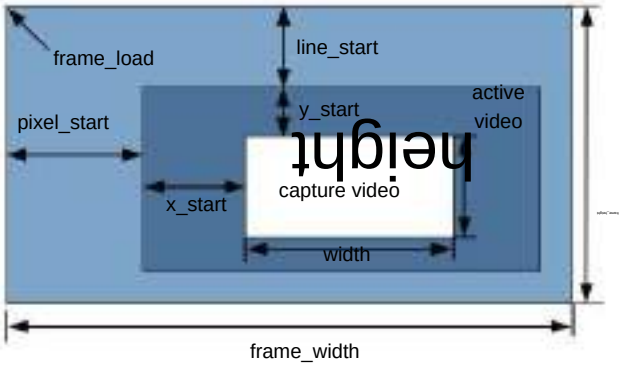
10.4 Module functions

CROP module

This module implements the function of cropping the input image. The actual displayed viewing area is usually contained within the effective video range, and is reduced by several pixels relative to the boundary of the active video.

As shown in Figure 10-3 , the module realizes the cropping of the effective image area by configuring the registers y_start, x_start, height, and width.

Figure 10-3 Relationship between effective image area and horizontal and vertical blanking



FPN module

This module corrects the image input by the Sensor through the calibrated black frame or black line to achieve the purpose of removing the Sensor FPN.

FPN supports calibration and correction in frame mode, as well as calibration and correction in line mode. The Sensor with obvious FPN needs to be turned on when it is connected to the sensor. If the FPN of the Sensor is not obvious, it does not need to be turned on.

Video test gen module

Video test gen supports generating five types of images:

Solid color image (as shown in Figure 10-4), configured by VIDEO_TEST_R_BACKGND[rbackgnd], VIDEO_TEST_G_BACKGND[gbackgnd], VIDEO_TEST_B_BACKGND[bbackgnd] .

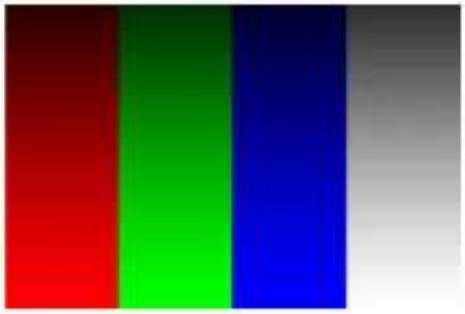
Figure 10-4 Video_test_gen solid color image

There are 4 horizontal colored stripes (as shown in Figure 10-5), the brightness is variable from left to right, and the initial value and incremental value can be configured.

Figure 10-5 Video_test_gen horizontal 4 color stripes image

4 vertical colored stripes (as shown in Figure 10-6), the brightness is variable from top to bottom, and the initial value and incremental value can be configured.

Figure 10-6 Video_test_gen image with 4 vertical color stripes

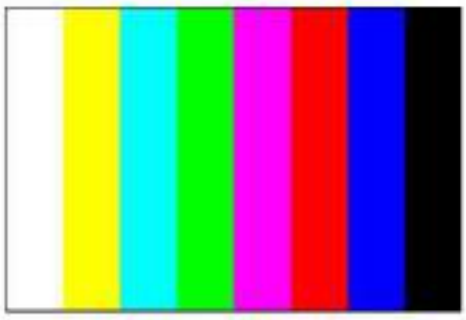


8 vertical color stripes (as shown in Figure 10-7), with adjustable

brightness, configured by

VIDEO_TEST_R_BACKGND[rbackgnd], VIDEO_TEST_G_BACKGND[gbackgnd], VIDEO_TEST_B_BACKGND[bbackgnd] .

Figure 10-7 Video_test_gen vertical 8 stripes image



Generate a rectangular solid-color target on a solid-color background (as shown in Figure 10-8), and the background consists of

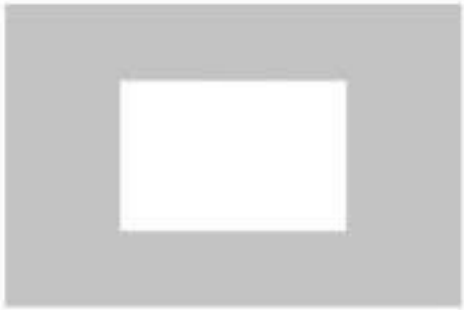
VIDEO_TEST_R_BACKGND[rbackgnd]ÿ

VIDEO_TEST_G_BACKGND[gbackgnd], VIDEO_TEST_B_BACKGND[bbackgnd] configuration, target by

VIDEO_TEST_R_FOREGND[rforegnd],

VIDEO_TEST_G_FOREGND[gforegnd]ÿVIDEO_TEST_B_FOREGND[bforegnd] configurationÿ

Figure 10-8 Video_test_gen solid color target image



Sensor offset module

Provide the black level correction of the Sensor, and compensate the 4 Bayer color channels (R, Gr, Gb, B) respectively through 4 independent parameters black00, black01, black10, black11.

DPC module

It is used to correct the dead pixels of the Sensor. It is divided into dynamic dead pixels and static dead pixels. Static dead pixels can correct up to 4096 dead pixels. It needs to be calibrated to obtain the coordinates of the dead pixels before calibration. There is no limit to the number of dynamic dead pixels, and no prior calibration is required. But static dead pixels are more accurate.

GE module

This module corrects the imbalance of the two channels of Gr and Gb, and improves the image quality of some scenes.

WDR module

Provide multi-frame composite wide dynamic function. Details in bright and dark areas can still be seen in scenes with a large dynamic range.

Gamma_fe module

This module is mainly used for bit width compression of image data. Two compression methods are provided: (1) The compression curve is represented by 2 LUTs. LUT0 contains 33 points with a precision of 20bit, and LUT1 contains 257 points with a precision of 20bit. (2) The compression curve is expressed by the formula:

$$y = \frac{2^{32} \times x}{a_{companding} \times 2^{24} + (4096 - a_{companding})}$$

Where x is the input image data, y is the output image data, and ÿcompandingÿ 4096.

Digital Gain Module

Provide digital gain, and provide U5.8bit gain setting.

DNR module

This module implements image denoising in Bayer domain, the purpose is to remove noise while retaining details. This module can eliminate the noise of the Sensor in a targeted manner according to the noise model provided by the user.

Gamma_be module

This module is mainly used for bit width extension of image data. Two extension methods are provided: (1) The extension curve is represented by 2 LUTs. LUT0 contains 33 points with a precision of 20bit, and LUT1 contains 257 points with a precision of 20bit. (2) The expansion curve is represented by the formula:

$$y - \frac{2^{32} \times x}{\alpha_{decompanding} \times 2^{24} + (4096 - \alpha_{decompanding})}$$

$$\alpha_{decompanding} = \frac{2^{24}}{\alpha_{companding}}$$

Where x is the input image data, y is the output image data, and ÿdecompandingÿ4096.

WB module

Provides white balance function. Provides gain and offset settings for 4 components (R, Gr, Gb, B) respectively.

Mesh shading module

Used for lens shading correction. Each pixel provides the gain of 3 components (R, G, B) respectively. The gain is represented by 8bit data. A total of 3×64×64 =12288 gain coefficients can be set, and the rest of the gain coefficients can be obtained by interpolation.

Radial shading module

Radial shading is an alternative to Mesh shading. Radial shading uses a radial model, which is different from the mesh model of Mesh shading. Radial shading provides a set of correction coefficients for each color channel (R, G, B).

DRC module

This module is used for image dynamic range compression (Dynamic Range Compression). It is used to adjust the display dynamic range of the image so that the display effect on the display device is consistent with human perception.

Demosaic module

Convert the input Bayer data into RGB domain data.

Color_matrix module

The module linearly corrects the input {R, G, B} through a standard 3×3 matrix, and can realize functions such as saturation adjustment and color correction by dynamically adjusting the coefficients of the matrix.

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} m_{RR} & m_{RG} & m_{RB} \\ m_{GR} & m_{GG} & m_{GB} \\ m_{BR} & m_{BG} & m_{BB} \end{pmatrix} \cdot \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

Gamma_RGB module

This module is applied to the (R, G, B) three color channels and outputs the Gamma adjustment result. The Gamma curve is composed of 257 nodes, each point is represented by 16bit data, and the points between two nodes are obtained by linear interpolation.

Gamma curve requires gamma[0]=0x0000, gamma[256]=0xFFFF.

AF module

This module supports the statistics of image definition evaluation information, which is used to complete the auto-focus function. The number of image blocks can be configured, the maximum number of blocks is 17×15, the minimum block width and height is 32×32, and the maximum is 511×511. Each area provides definition evaluation information.

AE module

Realize the statistics of automatic exposure information, and the software can adjust the Sensor according to the statistical information to realize the function of automatic exposure. The image is divided into 17×15 (17 rows and 15 columns) areas, and the weights of the areas can be set. Each area is divided into 5 segments to count the histogram information. The histogram information is normalized to 0xFFFF, so only the 0, 1, 3, Statistics for 4 segments. The weighted final stats can be read, as well as per-zone stats.

Also provides global histogram statistics. As shown in Figure 10-1 , Histogram provides 1024 histogram statistics of 1 data channel, and Histogram pe provides 256 histogram statistics of 3 data channels.

AWB module

Provide RGB domain white point statistical information, the software adjusts (R, G, B) three channel gains (Rgain, Ggain, Bgain) according to the statistical information to realize the automatic white balance function. RGB domain statistical information After the Demosaic module, the image is divided into 32×32 (32 rows and 32 columns) areas, and each area counts the number of pixels that meet the white point conditions, and the G/R and G/B mean values of the white point.

AWB sum module

Provide Bayer domain white point statistical information, the software adjusts (R, G, B) three channel gains (Rgain, Ggain, Bgain) according to the statistical information to realize the automatic white balance function. Bayer Domain Statistical Information Before WB gain, the image is divided into 32×32 (32 rows and 32 columns) regions, and each region counts the number of pixels that meet the white point conditions, and the R, G, and B mean values of the white point.

Dehaze module

This module provides powerful sub-area dehazing capabilities to improve the local contrast of videos in hazy scenes. Users can divide the image into multiple areas through ISP_DEHAZE_BLK_NUM, and the maximum supported area is 32×32.

The module analyzes the image characteristics in the area to obtain the contrast index in each area, and then enhances the pixels in the area. The enhancement strength of each pixel depends on the contrast index of the area and the surrounding area.

CSC module

CSC converts the input { R, G, B } to { Y, U, V } through the standard 3×3 matrix and vector offset, and dynamically adjusts the coefficients of the matrix.

$$\begin{pmatrix} Y \\ U \\ V \end{pmatrix} = \begin{pmatrix} Coefft11 & Coefft12 & Coefft13 \\ Coefft21 & Coefft22 & Coefft23 \\ Coefft31 & Coefft32 & Coefft33 \end{pmatrix} \cdot \begin{pmatrix} R \\ G \\ B \end{pmatrix} + \begin{pmatrix} Coefftо1 \\ Coefftо2 \\ Coefftо3 \end{pmatrix}$$

The parameters can be changed according to the needs of the conversion format.

DCI module

This module implements dynamic enhancement of image contrast. Automatically adjust the brightness and contrast of the image by counting the brightness of the image, and improve the problems of darker, brighter and too small or too large contrast images, so that the image can display a better display effect on the display device.

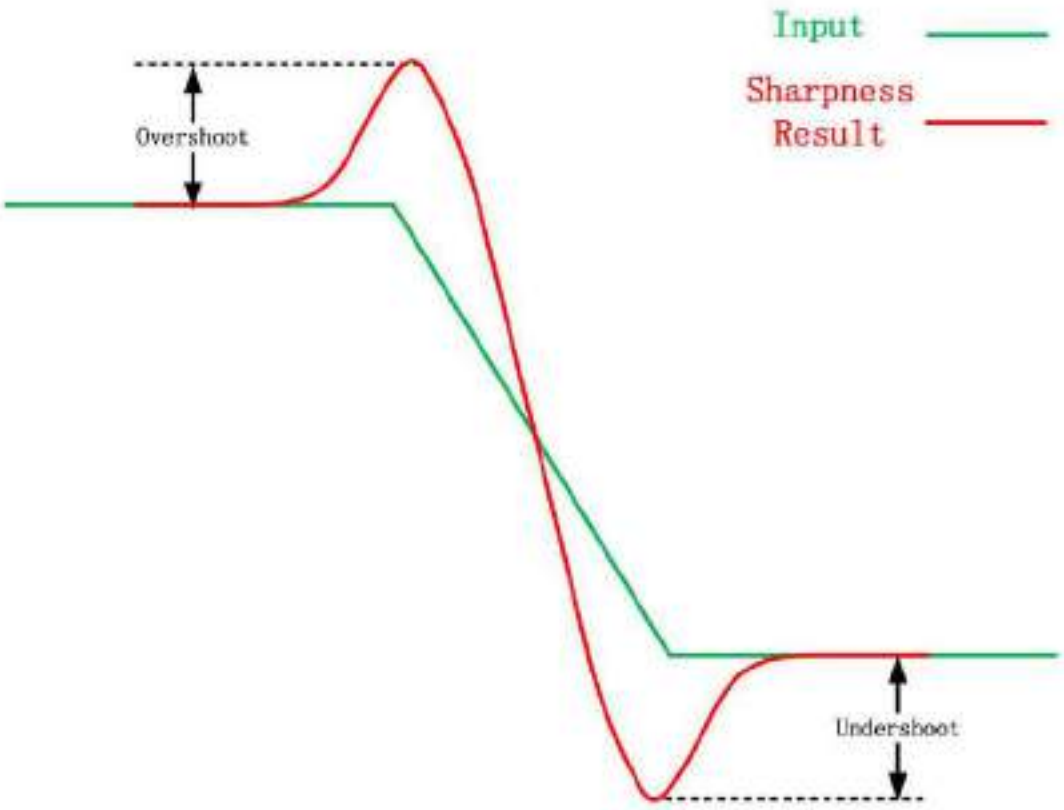
ACM module

Realize automatic management of colors. Corrects hue shift and saturation loss; compensates for differences in performance between different color gamuts; and can enhance specific colors such as skin tones, greens, blues, according to user preference and style.

Sharpen module

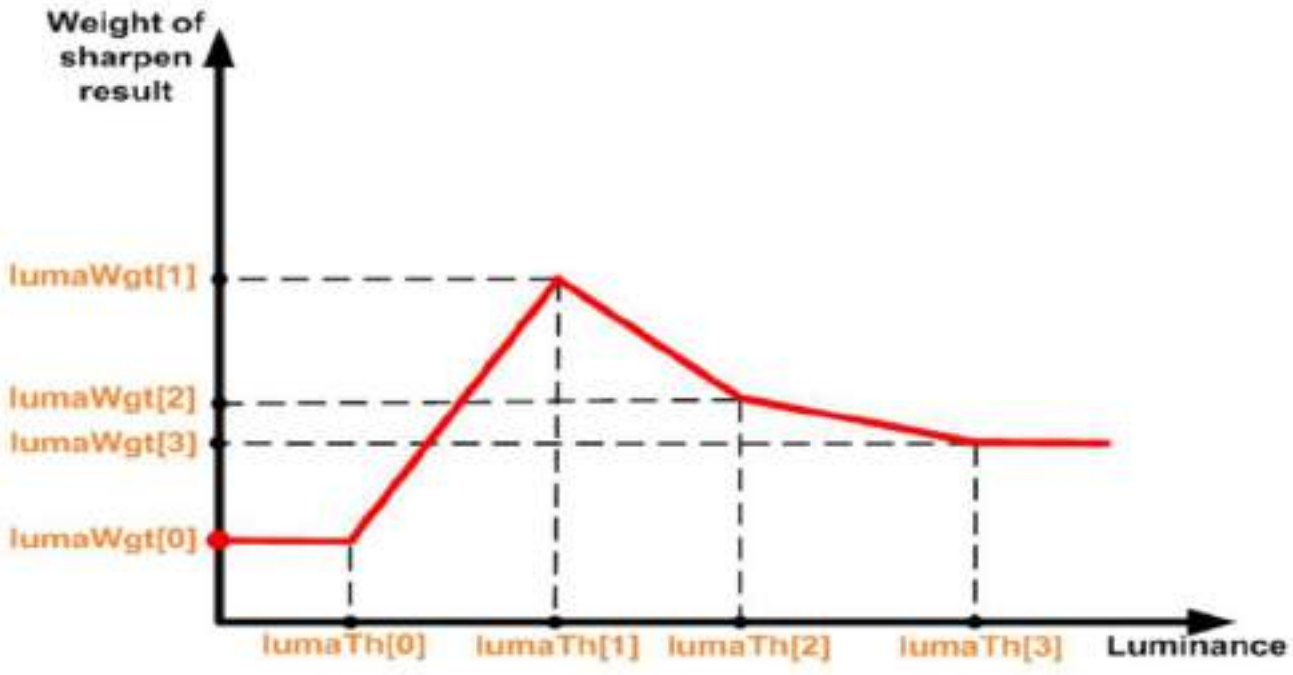
The Sharpen module realizes the sharpening of the image and improves the clarity of the image. By controlling the parameters edge_amt and sharp_amt, the sharpening strength can be adjusted, but too strong sharpening may amplify the noise. The software adjusts the parameter configuration according to the ISO value to achieve a balance between sharpness and noise suppression, and enhance the visual effect of the image.

Figure 10-9 Description of sharpening and overshoot



In addition, sharpening may cause the positive and negative edges to increase too much, resulting in white and black edges, as shown in Figure 10-9 . By adjusting the overshoot and undershoot control parameters, the phenomenon of white and black edges can be suppressed.

Figure 10-10 Brightness control sharpening gain description



As shown in Figure 10-10 , the sharpening gains of the bright and dark areas of the image can be controlled separately according to the brightness control sharpening gain curve, so as to achieve the purpose of improving the definition of bright areas and suppressing noise in dark areas.

In addition, the sharpen module can also independently control the strength of the edge aliasing of the sharpened image and the sharpening strength of the detail texture.

MCDS module

The MCDS module can not only realize the conversion from YUV444 to YUV422 or YUV420, but also realize the chroma noise reduction of the image.

MCDS performs multi-stage filtering on the horizontal direction of chroma, and when it needs to output YUV420, MCDS performs average downsampling on the vertical direction of chroma. By configuring appropriate filtering parameters, the visual loss of image conversion is minimized.

MCDS only denoises the chroma component of the image without affecting the brightness of the image. The noise reduction strength of this module is adjustable, which can balance the degree of color noise removal and the degree of color detail preservation.

10.5 ISP register overview

An overview of the ISP registers is shown in Table 10-9 .

Table 10-9 ISP register overview (base address is 0x1138_0000)

offset address name	describe	page number
0x12000 ISP_AF_CFG	AF Control Register	10-50
0x12010 ISP_AF_ZONE	AF block allocation register	10-52
0x12014 ISP_AF_CROP_START	AF image CROP start coordinate register	10-53
0x12018 ISP_AF_CROP_SIZE	AF image CROP SIZE register	10-54
0x1201C ISP_AF_MEAN_THRES	AF Median Filter Threshold Register	10-54
0x12020 ISP_AF_IIRG0	AF IIR filter parameter 0 register	10-54
0x12024 ISP_AF_IIRG1	AF IIR filter parameter 1 register	10-55
0x12028 ISP_AF_IIRG2	AF IIR filter parameter 2 register	10-55
0x1202C ISP_AF_IIRG3	AF IIR filter parameter 3 register	10-56
0x12030 ISP_AF_IIRG4	AF IIR filter parameter 4 register	10-56
0x12034 ISP_AF_IIRG5	AF IIR filter parameter 5 register	10-57
0x12038 ISP_AF_IIRG6	AF IIR filter parameter 6 register	10-57
0x1203C ISP_AF_IIRPL	AF IIR Filter Preset Register	10-58

offset address name	describe	page number
0x12040 ISP_AF_SHIFT	AF IIR filter shift parameter register	10-59
0x12050 ISP_AF_FIRH0	AF FIR filter parameter 0 register	10-60
0x12054 ISP_AF_FIRH1	AF FIR filter parameter 1 register	10-60
0x12058 ISP_AF_FIRH2	AF FIR filter parameter 2 register	10-61
0x1205C ISP_AF_FIRH3	AF FIR filter parameter 3 register	10-61
0x12060 ISP_AF_FIRH4	AF FIR filter parameter 4 register	10-62
0x12078 ISP_AF_ACC_SHIFT	AF Accumulated Statistics Value Shift Register	10-62
0x1207C ISP_AF_CNT_SHIFT	AF count statistics value shift register	10-63
0x12088 ISP_AF_STAT_IND_RADDR	AF Indirect read address register for statistical information of each block	10-63
0x1208C ISP_AF_STAT_IND_RDATA	AF each block statistical information indirect read data register	10-64
0x120E4 ISP_AF_CTRL_I	Update control register immediately	10-65
0x120EC ISP_AF_UPDATE	configuration update register	10-66
0x120F0 ISP_AF_SIZE	AF Image Size Register	10-66
0x12100 ISP_AF_IIRTHRE	AF IIR filter threshold register	10-67
0x12104 ISP_AF_IIRGAIN	AF IIR Filter Gain Register	10-67
0x12108 ISP_AF_IIRSLOPE	AF IIR filter slope register	10-68
0x1210C ISP_AF_IIRDILATE	AF IIR filter DILATE register	10-68
0x12110 ISP_AF_FIRTHRE	AF FIR filter threshold register	10-69
0x12114 ISP_AF_FIRGAIN	AF FIR filter gain register	10-70
0x12118 ISP_AF_FIRSLOPE	AF FIR filter slope register	10-70
0x12120 ISP_AF_IIRTHRE_CORING	AF IIR Filter CORING Threshold Register	10-71
0x12124 ISP_AF_IIRPEAK_CORING	AF IIR filter CORING peak register	10-71
0x12128 ISP_AF_IIRSLOPE_CORING	AF IIR filter CORING slope register	10-72
0x12130 ISP_AF_FIRTHRE_CORING	AF FIR Filter CORING Threshold Register	10-72

offset address name	describe	page number
0x12134 ISP_AF_FIRPEAK_CORING	AF FIR filter CORING peak register 10-73	
0x12138 ISP_AF_FIRSLOPE_CORING	AF FIR filter CORING slope register 10-73	
0x12140 ISP_AF_HILIGHT	AF high brightness threshold register	10-74
0x12144 ISP_AF_OFFSET	AF Offset Configuration Register	10-74
0x20010 ISPFE_ACTIVE_WIDTH	Image Width Register	10-75
0x20014 ISPFE_ACTIVE_HEIGHT	image height register	10-75
0x20018 ISPFE_RGGB_START	RGGB Mode Register	10-76
0x20020 ISPFE_CHANNEL_SELECT	Module Video Test Gen and Raw FE input data channel select register	10-76
0x20024 ISPFE_DELAY_LINE_MEMORY	Module DNR Line Delay Register	10-78
0x20028 ISPFE_FLUSH_HBLANK	Row Blanking Timing Configuration Register	10-78
0x2002C ISPFE_FS_CHANNEL_SELECT	WDR input data channel selection	10-79
0x20030 ISPFE_CONFIG_BUFFER_MODE	Configuration Update Mode Register	10-80
0x20040 ISPFE_MODULE_BYPASS	ISP FE module BYPASS register	10-80
0x20044 ISPFE_BYPASS_MODE	ISP FE Bypass Mode Selection Register	10-82
0x20048 ISPFE_AE_SWITCH	AE statistics position control register	10-83
0x2004C ISPFE_AWB_SWITCH	RGB Domain AWB Statistics Module Position Control Register 10-84	
0x20050 ISPFE_HISTOGRAM_SWITCH	AE global histogram position control register 10-84	
0x20058 ISPFE_HISTOGRAM_PE_SWITCH	Per exposure AE global histogram control register	10-85
0x20078 ISPFE_GLOBAL_FSM_RESET	State Machine Reset Register	10-86
0x2007C ISPFE_FIELD_STATUS	Field Signal Status Register	10-86

offset address name	describe	page number
0x20080 ISPFE_INTERRUPT 01	0, 1 Interrupt selection register	10-87
0x20084 ISPFE_INTERRUPT 23	2, 3 interrupt selection register	10-87
0x20088 ISPFE_INTERRUPT 45	4, 5 interrupt selection register	10-88
0x2008C ISPFE_INTERRUPT 67	6, 7 interrupt selection register	10-88
0x20090 ISPFE_INTERRUPT 89	8, 9 Interrupt selection register	10-89
0x20094 ISPFE_INTERRUPT 1011	10, 11 Interrupt selection register	10-89
0x20098 ISPFE_INTERRUPT 1213	12, 13 Interrupt selection register	10-90
0x2009C ISPFE_INTERRUPT 1415	14, 15 Interrupt selection register	10-90
0x200A0 ISPFE_INTERRUPT _STATUS	Interrupt Status Register	10-91
0x200A4 ISPFE_INTERRUPT _CLEAR	clear interrupt register	10-91
0x200C0 SENSOR_OFFSET_ WDR_1_BLACK00	WDR_1 BLC R component black level value register 10-92	
0x200C4 SENSOR_OFFSET_ WDR_1_BLACK01	WDR_1 BLC Gr component black level value register 10-92	
0x200C8 SENSOR_OFFSET_ WDR_1_BLACK10	WDR_1 BLC Gb component black level value register 10-93	
0x200CC SENSOR_OFFSET_ WDR_1_BLACK11	WDR_1 BLC B component black level value register 10-93	
0x200D0 SENSOR_OFFSET_ WDR_2_BLACK00	WDR_2 BLC R component black level value register 10-93	
0x200D4 SENSOR_OFFSET_ WDR_2_BLACK01	WDR_2 BLC Gr component black level value register 10-94	
0x200D8 SENSOR_OFFSET_ WDR_2_BLACK10	WDR_2 BLC Gb component black level value register 10-94	
0x200DC SENSOR_OFFSET_ WDR_2_BLACK11	WDR_2 BLC B component black level value register 10-95	
0x200E0 SENSOR_OFFSET_ WDR_3_BLACK00	WDR_3 BLC R component black level value register 10-95	

offset address name	describe	page number
0x200E4 SENSOR_OFFSET_ WDR_3_BLACK01	WDR_3 BLC Gr component black level value register	10-95
0x200E8 SENSOR_OFFSET_ WDR_3_BLACK10	WDR_3 BLC Gb component black level value register	10-96
0x200EC SENSOR_OFFSET_ WDR_3_BLACK11	WDR_3 BLC B component black level value register	10-96
0x200F0 SENSOR_OFFSET_ WDR_4_BLACK00	WDR_4 BLC R component black level value register	10-97
0x200F4 SENSOR_OFFSET_ WDR_4_BLACK01	WDR_4 BLC Gr component black level value register	10-97
0x200F8 SENSOR_OFFSET_ WDR_4_BLACK10	WDR_4 BLC Gb component black level value register	10-97
0x200FC SENSOR_OFFSET_ WDR_4_BLACK11	WDR_4 BLC B component black level value register	10-98
0x20108 INPUTPORT_HC_LI WITH	Inputport Horizontal Count Limit Configuration Register	10-98
0x2010C INPUTPORT_HC_S TART0	Inputport horizontal start register 0	10-99
0x20110 INPUTPORT_HC_SI ZE0	Inputport horizontal size register 0	10-99
0x20114 INPUTPORT_HC_S TART1	Inputport horizontal start register 1	10-99
0x20118 INPUTPORT_HC_SI ZE1	Inputport horizontal size register 1	10-100
0x2011C INPUTPORT_VC_LI WITH	Inputport Vertical Count Limit Configuration Register	10-100
0x20120 INPUTPORT_VC_S TART	Inputport vertical start register	10-101
0x20124 INPUTPORT_VC_SI SHE	Inputport vertical size register	10-101
0x20130 INPUTPORT_CTRL	Inputport Input interface control register	10-101
0x20134 INPUTPORT_STAT US	Inputport status register	10-102
0x20140 INPUT_FORMATTE R_MODE	Input Formatter Mode Control Register	10-103
0x20144 INPUT_FORMATTE R_FACTORML	Input Formatter long and medium exposure ratio registers	10-104

offset address name	describe	page number
0x20148 INPUT_FORMATTER_FACTORMS	Input Formatter short and medium exposure ratio registers	10-104
0x2014C INPUT_FORMATTER_BLACKLEVEL	Input Formatter sensor black level register	10-105
0x20150 INPUT_FORMATTER_KNEEPOINT01	Input Formatter Knee 0, 1 Register	10-105
0x20154 INPUT_FORMATTER_KNEEPOINT2	Input Formatter Knee 2 Register	10-106
0x20158 INPUT_FORMATTER_SLOPESELECT	Slope Registers 10-106 of Input Formatter Compression Table	
0x20160 VIDEO_TEST_GEN_CTRL	VIDEO_TEST_GEN Control Register	10-107
0x20164 VIDEO_TEST_PATTRAIN_TYPE	VIDEO_TEST_GEN mode type selection register	10-107
0x20168 VIDEO_TEST_R_BACKGND	VIDEO_TEST_GEN R component background value register	10-108
0x2016C VIDEO_TEST_G_BACKGND	VIDEO_TEST_GENG G component background value register	10-108
0x20170 VIDEO_TEST_B_BACKGND	VIDEO_TEST_GEN B component background value register	10-109
0x20174 VIDEO_TEST_R_FORAIN	VIDEO_TEST_GEN R component foreground value register	10-109
0x20178 VIDEO_TEST_G_FREG	VIDEO_TEST_GENG G component foreground value register	10-110
0x2017C VIDEO_TEST_B_FORAIN	VIDEO_TEST_GEN B component foreground value register	10-110
0x20180 VIDEO_TEST_RGB_GRADIENT	VIDEO_TEST_GEN first and second channel RGB gradient incremental value register	10-110
0x20184 VIDEO_TEST_RGB_GRADIENT_START	VIDEO_TEST_GEN The third and fourth channel RGB gradient incremental value register	10-111
0x20188 VIDEO_TEST_RGB_GRADIENT_START12	VIDEO_TEST_GEN First and second channel RGB gradient start value register	10-111
0x2018C VIDEO_TEST_RGB_GRADIENT_START34	VIDEO_TEST_GEN The third and fourth channel RGB gradient start value register	10-112

offset address	name	describe	page number
0x20190	VIDEO_TEST_RECT_TOP	VIDEO_TEST_GEN Rectangular top, bottom row number register	10-112
0x20194	VIDEO_TEST_RECT_LEFT	VIDEO_TEST_GEN The number of pixels on the left side of the rectangle	10-113
0x20198	VIDEO_TEST_RECT_RIGHT	VIDEO_TEST_GEN The number of pixels on the right side of the rectangle	10-113
0x201A0	SENSOR_OFFSET_BLACK00	R component black level value register	10-114
0x201A4	SENSOR_OFFSET_BLACK01	Gr component black level value register	10-114
0x201A8	SENSOR_OFFSET_BLACK10	Gb component black level value register	10-115
0x201AC	SENSOR_OFFSET_BLACK11	B component black level value register	10-115
0x201B0	NP_RAW_FRONTEND1_EXP_THRESH	NP_RAW_FRONTEND1 Noise Threshold Register	10-115
0x201B4	NP_RAW_FRONTEND1_SHORT_RATIO	NP_RAW_FRONTEND1 Noise short exposure ratio register	10-116
0x201B8	NP_RAW_FRONTEND1_LONG_RATIO	NP_RAW_FRONTEND1 Noise long exposure ratio register	10-116
0x201BC	NP_RAW_FRONTEND1_OFF	NP_RAW_FRONTEND1 Noise Black Offset Register	10-117
0x201C0	NP_RAW_FRONTEND2_EXP_THRESH	NP_RAW_FRONTEND2 Noise Threshold Register	10-117
0x201C4	NP_RAW_FRONTEND2_SHORT_RATIO	NP_RAW_FRONTEND2 Noise short exposure ratio register	10-118
0x201C8	NP_RAW_FRONTEND2_LONG_RATIO	NP_RAW_FRONTEND2 Noise long exposure ratio register	10-118
0x201CC	NP_RAW_FRONTEND2_OFF	NP_RAW_FRONTEND2 Noise Black Level Offset Register	10-119
0x201D0	NP_RAW_FRONTEND3_EXP_THRESH	NP_RAW_FRONTEND3 Noise Threshold Register	10-119
0x201D4	NP_RAW_FRONTEND3_SHORT_RATIO	NP_RAW_FRONTEND3 Noise short exposure ratio register	10-120

offset address name	describe	page number
0x201D8 NP_RAW_FRONTEND3_LONG_RATIO	NP_RAW_FRONTEND3 Noise long exposure ratio register	10-120
0x201DC NP_RAW_FRONTEND3_OFF	NP_RAW_FRONTEND3 Noise Black Level Offset Register	10-121
0x201E0 NP_RAW_FRONTEND4_EXP_THRESH	NP_RAW_FRONTEND4 Noise Threshold Register	10-121
0x201E4 NP_RAW_FRONTEND4_SHORT_RATIO	NP_RAW_FRONTEND4 Noise short exposure ratio register	10-122
0x201E8 NP_RAW_FRONTEND4_LONG_RATIO	NP_RAW_FRONTEND4 Noise long exposure ratio register	10-122
0x201EC NP_RAW_FRONTEND4_OFF	NP_RAW_FRONTEND4 Noise Black Level Offset Register	10-123
0x20200 RAW_FRONTEND1_CTRL1	RAW_FRONTEND1 Module Control Register 10-123	
0x20204 RAW_FRONTEND1_GE_STRENGTH	RAW_FRONTEND1 GE Strength Register 10-125	
0x20208 RAW_FRONTEND1_DEBUG_SEL	RAW_FRONTEND1 Debug Register	10-125
0x2020C RAW_FRONTEND1_DP_THRESHOLD	RAW_FRONTEND1 dynamic dead pixel detection threshold register	10-125
0x20210 RAW_FRONTEND1_GE_THRESHOLD	RAW_FRONTEND1 GE Threshold Register 10-126	
0x20214 RAW_FRONTEND1_DP_SLOPE	RAW_FRONTEND1 HP mask function slope register	10-126
0x20218 RAW_FRONTEND1_GE_SLOPE	RAW_FRONTEND1 GE mask function slope register	10-127
0x2021C RAW_FRONTEND1_GE_SENS	RAW_FRONTEND1 GE module edge sensitivity control register	10-127
0x20220 RAW_FRONTEND1_DPDEV_THRESHOLD	RAW_FRONTEND1 Dynamic dead point correction to edge influence strength control register	10-127
0x20224 RAW_FRONTEND1_LINE_THRESH	RAW_FRONTEND1 Directional control register for dynamic dead pixel correction near the edge	10-128
0x20228 RAW_FRONTEND1_DP_BLEND	RAW_FRONTEND1 Fusion control register between directional and non-directional replacement values for dynamic dead pixel correction 10	10-128

offset address name	describe	page number
0x2022C RAW_FRONTEND1 _SIGMA_IN	RAW_FRONTEND1 Artificial Noise Estimation Register	10-129
0x20230 RAW_FRONTEND1 _THRESH_SHORT	RAW_FRONTEND1 short exposure data noise threshold control register	10-129
0x20234 RAW_FRONTEND1 _THRESH_LONG	RAW_FRONTEND1 long exposure data noise threshold control register	10-130
0x20240 RAW_FRONTEND2 _CTRL1	RAW_FRONTEND2 module control register 1	10-130
0x20244 RAW_FRONTEND2 _GE_STRENGTH	RAW_FRONTEND2 GE Strength Registers 10-132	
0x2024C RAW_FRONTEND2 _DP_THRESHOLD	RAW_FRONTEND2 dynamic bad point detection threshold register	10-132
0x20250 RAW_FRONTEND2 _GE_THRESHOLD	RAW_FRONTEND2 GE Threshold Register 10-132	
0x20254 RAW_FRONTEND2 _DP_SLOPE	RAW_FRONTEND2 HP mask function slope register	10-133
0x20258 RAW_FRONTEND2 _GE_SLOPE	RAW_FRONTEND2 GE mask function slope register	10-133
0x2025C RAW_FRONTEND2 _GE_SENS	RAW_FRONTEND2 GE module edge sensitivity control register	10-134
0x20260 RAW_FRONTEND2 _DPDEV_THRESHO LD	RAW_FRONTEND2 Dynamic dead point correction has an impact on the edge strength control register	10-134
0x20264 RAW_FRONTEND2 _LINE_THRESH	RAW_FRONTEND2 Directionality control register near the edge for dynamic bad pixel correction	10-134
0x20268 RAW_FRONTEND2 _DP_BLEND	RAW_FRONTEND2 Dynamic Dead Pixel Correction Fusion Control Register 10 between directional and non-directional replacement values	10-135
0x2026C RAW_FRONTEND2 _SIGMA_IN	RAW_FRONTEND2 Artificial Noise Estimation Register	10-135
0x20270 RAW_FRONTEND2 _THRESH_SHORT	RAW_FRONTEND2 short exposure data noise threshold control register	10-136
0x20274 RAW_FRONTEND2 _THRESH_LONG	RAW_FRONTEND2 long exposure data noise threshold control register	10-136
0x20280 STATIC_DPC_MUL TI_CH_MODE	STATIC_DPC Static dead point correction 4k/2k mode selection register	10-137

offset address name	describe	page number
0x20284 STATIC_DPC_CTRL	Static Defect Pixels Module Control Register 10-137	
0x20288 STATIC_DPC_OVERFLOW	Static Defect Pixels Block Table Overflow Flag Register	10-139
0x2028C STATIC_DPC_COUNT	Register of the number of dead pixels detected by the Static Defect Pixels module	10-139
0x20290 STATIC_DPC_TABLE_START	Bad Pixel First Address Register of Static Defect Pixels Module	10-140
0x20294 STATIC_DPC_COUNT_IN	Static Defect Pixels module write bad pixel count register	10-140
0x202A0 WDR_CTRL	WDR Control Register	10-141
0x202A4 WDR_LONG_CTRL1	WDR long exposure control register 1	10-142
0x202A8 WDR_LONG_CTRL2	WDR long exposure control register 2	10-142
0x202AC WDR_LONG_STITCH_ERROR_LIMIT	WDR long exposure intensity setting register	10-143
0x202B0 WDR_MED_CTRL1	WDR medium exposure control register 1	10-143
0x202B4 WDR_MED_CTRL2	WDR medium exposure control register 2	10-144
0x202B8 WDR_MED_CTRL3	WDR medium exposure control register 3	10-145
0x202BC WDR_MED_STITCH_ERROR_LIMIT	Exposure intensity setting in WDR	10-145
0x202C0 WDR_SHORT_CTRL1	WDR short exposure control register 1	10-145
0x202C4 WDR_SHORT_CTRL2	WDR short exposure control register 2	10-146
0x202C8 WDR_SHORT_CTRL3	WDR short exposure control register 3	10-147
0x202CC WDR_SHORT_STITCH_ERROR_LIMIT	WDR short exposure intensity setting register	10-147
0x202D0 WDR_BLACK_LEVEL_LONG	WDR black level register for long exposure input	10-147
0x202D4 WDR_BLACK_LEVEL_MEDIUM1	Black level register 1 for exposure input in WDR	10-148
0x202D8 WDR_BLACK_LEVEL_MEDIUM2	Black level register 2 for exposure input in WDR	10-148

offset address name	describe	page number
0x202DC WDR_BLACK_LEV THE_SHORT	Black Level Register for WDR Short Exposure Input	10-149
0x202E0 WDR_BLACK_LEV EL_OUT	Black level register output by WDR module	10-149
0x202E4 WDR_MODE_IN WDR input mode selection register		10-149
0x20300 FRONTEND_LUT_C TRL	FRONTEND_LUT Control Register	10-150
0x20304 FRONTEND_LUT_ MCU_READY	FRONTEND_LUT status indication	10-151
0x20308 FRONTEND_LUT_ ALPHA	FRONTEND_LUT alpha parameter register 10-152	
0x20310 DG_GAIN	sensor digital gain	10-152
0x20314 DG_OFFSET	DG black level compensation	10-152
0x20320 DNR_CTRL	DNR Control Register	10-153
0x20324 DNR_RM_CENTER _X	Abscissa register of DNR shadow map	10-154
0x20328 DNR_RM_CENTER _AND	Ordinate register for the DNR shadow map	10-154
0x2032C DNR_RM_OFF_CE NTER_MULT	DNR Normalization Factor Register	10-154
0x20330 DNR_THRESH_H01 DNR horizontal airspace high frequency noise threshold register 10-155		
0x20334 DNR_THRESH_H24 Noise threshold register 10-155 at low frequency in DNR horizontal airspace		
0x20338 DNR_THRESH_V01 DNR vertical airspace high frequency noise threshold register 10-156		
0x2033C DNR_THRESH_V24 DNR vertical airspace low frequency noise threshold register 10-156		
0x20344 DNR_THRESH_SH LOCATION	DNR Noise Threshold Adjustment Register for Short Exposure Data 10-157	
0x20348 DNR_THRESH_LO of	DNR Noise Threshold Adjustment Register for Long Exposure Data 10-157	
0x20350 DNR_STRENGTH1 DNR High Spatial Frequency Noise Suppression Effect Register 10-158		
0x20358 DNR_STRENGTH4 DNR low spatial frequency noise suppression effect register 10-158		
0x20360 BACKEND_LUT_C RTL	BACKEND_LUT Control Register	10-158
0x20364 BACKEND_LUT_M CU_READY	BACKEND_LUT status indication	10-160

offset address name	describe	page number
0x20368 BACKEND_LUT_ALPHA	BACKEND_LUT alpha parameter register 10-160	
0x20370 NP_FOR_DNR_EXP_THRESH	NP_FOR_DNR_NOISE THRESHOLD REGISTER	10-161
0x20374 NP_FOR_DNR_SHORT_RATIO	NP_FOR_DNR_NOISE SHORT EXPOSURE RATIO Register 10-161	
0x20378 NP_FOR_DNR_LONG_RATIO	NP_FOR_DNR_NOISE LONG EXPOSURE RATIO Register 10-161	
0x2037C NP_FOR_DNR_OFF	NP_FOR_DNR_NOISE BLACK LEVEL OFFSET Register 10-162	
0x20380 WB_GAIN00	White Balance Block R Component Gain Register 10-162	
0x20384 WB_GAIN01	Gr Component Gain Register for White Balance Block	10-163
0x20388 WB_GAIN10	Gb Component Gain Register for White Balance Block	10-163
0x2038C WB_GAIN11	White Balance Block B Component Gain Register 10-164	
0x203A0 BLC_BLACK00	BLC R component black level offset value	10-164
0x203A4 BLC_BLACK01	BLC Gr component black level offset value	10-164
0x203A8 BLC_BLACK10	BLC Gb component black level offset value	10-165
0x203AC BLC_BLACK11	BLC B component black level offset value	10-165
0x203B0 RADIAL_SHADING_CTRL	Radial_Shading module control register	10-166
0x203B4 RADIAL_SHADING_MCU_READY	Radial_Shading LUT Status Register	10-166
0x203B8 RADIAL_SHADING_RX	Radial_Shading R component center point X coordinate register	10-167
0x203BC RADIAL_SHADING_RY	Radial_Shading R component center point Y coordinate register	10-167
0x203C0 RADIAL_SHADING_GX	Radial_Shading G component center point X coordinate register	10-168
0x203C4 RADIAL_SHADING_GY	Radial_Shading G component center point Y coordinate register	10-168
0x203C8 RADIAL_SHADING_BX	Radial_Shading B component center point X coordinate register	10-169
0x203CC RADIAL_SHADING_BY	Radial_Shading B component center point Y coordinate register	10-169

offset address name	describe	page number
0x203D0 RADIAL_SHADING _MULTR	Radial_Shading red radial table normalization factor 10-169	
0x203D4 RADIAL_SHADING _MULTG	Radial_Shading green radial table normalization factor	10-170
0x203D8 RADIAL_SHADING _MULTB	Radial_Shading blue radial table normalization factor 10-170	
0x203E0 MESH_SHADING_C TRL	Mesh_Shading Control Register	10-171
0x203E4 MESH_SHADING_R ELOAD	Mesh_Shading cache refresh register	10-172
0x203F0 MESH_SHADING_ ALPHAMODE	ÿ fusion mode register between Mesh_Shading entries	10-173
0x203F4 MESH_SHADING_ ALPHA_BANK	Mesh_Shading fusion bank selection register 10-173	
0x203F8 MESH_SHADING_ ALPHA	Mesh_Shading ÿ fusion coefficient register	10-175
0x203FC MESH_SHADING_S NEED	Mesh_Shading Correction Intensity Control Register 10-175	
0x20400 DRC_ENABLE	DRC Enable Register	10-176
0x20408 DRC_CTRL	DRC Module Control Register	10-176
0x20410 DRC_BLACK_LEV HE	DRC Black Level Register	10-177
0x20414 DRC_WHITE_LEVE L	DRC White Level Register	10-177
0x20420 DRC_STRENGTH_I NROI	DRC Region of Interest Intensity Register	10-178
0x20424 DRC_STRENGTH_ OUTROI	Intensity and horizontal start point register in DRC region of interest	10-178
0x20428 DRC_ROI_HOR_ST ART_END	DRC region of interest vertical start point and horizontal end point register	10-179
0x2042C DRC_ROI_VER_EN D	DRC Region of Interest Vertical End Point Register 10-179	
0x20430 DRC_FILTER_MUX	DRC algorithm control register	10-180
0x20434 DRC_DARK_ENH	DRC Dark_Enhance parameter setting register 10-180	
0x20438 DRC_MCU_READY	DRC LUT status indication register	10-181

offset address name	describe	page number
0x20480 DEMOSAIC_VH_SLOPE	Slope register for DEMOSAIC vertical/horizontal blend threshold	10-181
0x20484 DEMOSAIC_AA_SLOPE	DEMOSAIC Angle Blend Threshold Slope Register 10-182	
0x20488 DEMOSAIC_VA_SLOPE	Slope Register for DEMOSAIC VH-AA(VA) Hybrid Threshold	10-182
0x2048C DEMOSAIC_UU_SLOPE	DEMOSAIC Slope Register for Undefined Mixing Threshold	10-183
0x20490 DEMOSAIC_SAT_SLOPE	Slope Register for DEMOSAIC Saturation Blending Threshold	10-183
0x20494 DEMOSAIC_VH_THRESH	Threshold register for DEMOSAIC vertical/horizontal mixed range	10-183
0x20498 DEMOSAIC_AA_THRESH	Threshold Register 10-184 for DEMOSAIC Angle Blending Range	
0x2049C DEMOSAIC_VA_THRESH	DEMOSAIC VA Mixed Range Threshold Register 10-184	
0x204A0 DEMOSAIC_UU_THRESH	DEMOSAIC undefined threshold register for mixed range	10-185
0x204A4 DEMOSAIC_SAT_THRESH	Threshold Register for DEMOSAIC Saturation Mixed Range	10-185
0x204A8 DEMOSAIC_VH_OFFSET	DEMOSAIC Vertical/Horizontal Hybrid Threshold Offset Register	10-185
0x204AC DEMOSAIC_AA_OFFSET	DEMOSAIC Angle Blend Threshold Offset Register 10-186	
0x204B0 DEMOSAIC_VA_OFFSET	DEMOSAIC VA Hybrid Threshold Offset Register 10-186	
0x204B4 DEMOSAIC_UU_OFFSET	DEMOSAIC Undefined Hybrid Threshold Offset Register 10-187	
0x204B8 DEMOSAIC_SAT_OFFSET	DEMOSAIC Saturation Blend Threshold Offset Register 10-187	
0x204BC DEMOSAIC_SHARP_ALT_D	DEMOSAIC Directionalized sharp mask strength register	10-187
0x204C0 DEMOSAIC_SHARP_ALL_OUT	DEMOSAIC Non-directional sharpening mask strength register	10-188
0x204C4 DEMOSAIC_LUM_THRESH	DEMOSAIC Directionalized Sharpen Luminance Threshold Register	10-188

offset address name	describe	page number
0x204C8 DEMOSAIC_NP_OFFSET	DEMOSAIC Noise Configuration Offset Register	10-189
0x204CC DEMOSAIC_DMSC_CONFIG	DEMOSAIC Debug output selection	10-189
0x204D0 DEMOSAIC_AC_THRESH	DEMOSAIC AC Mixed Range Threshold Register 10-189	
0x204D4 DEMOSAIC_AC_SLOPE	DEMOSAIC AC Mixed Threshold Slope Register 10-190	
0x204D8 DEMOSAIC_AC_OFFSET	DEMOSAIC AC Hybrid Threshold Offset Register 10-190	
0x204DC DEMOSAIC_FC_SLPOE	DEMOSAIC pseudo color correction slope (intensity) register	10-191
0x204E0 DEMOSAIC_FC_ALIAS_SLPOE	DEMOSAIC pseudo color correction slope (intensity) register	10-191
0x204E4 DEMOSAIC_FC_ALIAS_THRESH	DEMOSAIC de-false color threshold register	10-191
0x204EC DEMOSAIC_NP_OFF	DEMOSAIC Noise Black Level Offset Register 10-192	
0x204F0 DEMOSAIC_SHARP	DEMOSAIC Sharpen strength register	10-192
0x204F4 DEMOSAIC_MIN_THRESHOLD	DEMOSAIC Threshold Register	10-193
0x204F8 DEMOSAIC_SHARPAND_ALG_SELECT	DEMOSAIC New Sharpen Algorithm Switching Register	10-193
0x20500 COLOR_MATRIX_COEFFT_RR	COLOR_MATRIX RR multiple matrix coefficient register	10-194
0x20504 COLOR_MATRIX_COEFFT_RG	COLOR_MATRIX RG multiple matrix coefficient register	10-194
0x20508 COLOR_MATRIX_COEFFT_RB	COLOR_MATRIX RB multiple matrix coefficient register	10-195
0x2050C COLOR_MATRIX_COEFFT_GR	COLOR_MATRIX GR multiple matrix coefficient register	10-195
0x20510 COLOR_MATRIX_COEFFT_GG	COLOR_MATRIX GG multiple matrix coefficient register	10-196
0x20514 COLOR_MATRIX_COEFFT_GB	COLOR_MATRIX Matrix coefficient register for multiples of GB	10-196
0x20518 COLOR_MATRIX_COEFFT_BR	COLOR_MATRIX BR Multiple matrix coefficient register	10-196

offset address name	describe	page number
0x2051C COLOR_MATRIX_COEFFT_BG	COLOR_MATRIX BG multiple matrix coefficient register	10-197
0x20520 COLOR_MATRIX_COEFFT_BB	COLOR_MATRIX Matrix coefficient register for multiples of BB	10-197
0x20524 COLOR_MATRIX_CTRL	COLOR_MATRIX enable register	10-198
0x20528 COLOR_MATRIX_COEFFT_WBR	COLOR_MATRIX R White balance gain register 10-198	
0x2052C COLOR_MATRIX_COEFFT_WBG	COLOR_MATRIX G White balance gain register 10-199	
0x20530 COLOR_MATRIX_COEFFT_WBB	COLOR_MATRIX B White balance gain register 10-199	
0x20534 COLOR_MATRIX_COEFFT_FOG_OFFSETR	COLOR_MATRIX color matrix R offset 10-199	
0x20538 COLOR_MATRIX_COEFFT_FOG_OFFSETG	COLOR_MATRIX color matrix G offset 10-200	
0x2053C COLOR_MATRIX_COEFFT_FOG_OFFSETB	COLOR_MATRIX color matrix B offset 10-200	
0x20580 GAMMA_RGB_CTRL	GAMMA_RGB Control Register	10-201
0x20584 GAMMA_RGB_MCU_READY	GAMMA_RGB LUT Receive data status flag from CPU	10-202
0x20680 DITHER_CTRL	DITHER control register	10-202
0x20700 STATISTICS_HIST_THRESH_0_1	Histogram Threshold Register for Bin 0/1 Boundary	10-203
0x20704 STATISTICS_HIST_THRESH_1_2	Histogram Threshold Register for Bin 1/2 Boundary	10-203
0x20708 STATISTICS_HIST_THRESH_3_4	Histogram Threshold Register for Bin 2/3 Boundary	10-204
0x2070C STATISTICS_HIST_THRESH_4_5	Histogram Threshold for Bin 3/4 Boundaries	10-204
0x20720 STATISTICS_HIST_0	Normalized histogram result register for Bin 0	10-205
0x20724 STATISTICS_HIST_1	Bin 1 normalized histogram result register	10-205

offset address name	describe	page number
0x20728 STATISTICS_HIST_3	Bin 3 normalized histogram result register	10-205
0x2072C STATISTICS_HIST_4	Bin 4 normalized histogram result register	10-206
0x20730 STATISTICS_AEXP_NODES_USED	AE Active Area Register	10-206
0x20740 STATISTICS_WHITE_LEVEL_AWB	Brightness upper limit register of RGB domain AWB statistical white point	10-207
0x20744 STATISTICS_BLACK_LEVEL_AWB	Brightness lower limit register of RGB domain AWB statistical white point	10-207
0x20748 STATISTICS_CR_REF_MAX_AWB	Chromaticity R/G upper limit register for RGB domain AWB statistical white point	10-207
0x2074C STATISTICS_CR_REF_MIN_AWB	Chromaticity R/G lower limit register for RGB domain AWB statistical white point	10-208
0x20750 STATISTICS_CB_REF_MAX_AWB	Chromaticity B/G Upper Limit Register of AWB Statistical White Point in RGB Domain	10-208
0x20754 STATISTICS_CB_REF_MIN_AWB	Chromaticity B/G lower limit register of RGB domain AWB statistical white point	10-209
0x20758 STATISTICS_AWB_RG	RGB Domain AWB Statistics G/R Mean Register 10-209	
0x2075C STATISTICS_AWB_BG	RGB Domain AWB Statistics G/B Mean Register 10-210	
0x20760 STATISTICS_AWB_SUM	Register 10-210 of the number of white dots counted by RGB domain AWB	
0x20768 STATISTICS_AWB_STATS_MODE	RGB domain AWB statistical result output mode selection register	10-210
0x20770 STATISTICS_AWB_NODES_USED	RGB domain AWB statistical partition number register 10-211	
0x20780 STATISTICS_CR_REF_HIGH_AWB	Chromaticity R/G Hexagon Upper Limit Register for RGB Domain AWB Statistics White Point	10-211
0x20784 STATISTICS_CR_REF_LOW_AWB	Chromaticity R/G Hexagon Lower Limit Register for RGB Domain AWB Statistical White Point	10-212
0x20788 STATISTICS_CB_REF_HIGH_AWB	Chromaticity B/G hexagon upper limit register of RGB domain AWB statistical white point	10-212
0x2078C STATISTICS_CB_REF_LOW_AWB	Chromaticity B/G Hexagon lower limit register of RGB domain AWB statistical white point	10-213

offset address name	describe	page number
0x207A0 STATISTICS_PLANE_TOTAL_0	Total pixel registers processed per plane 0	10-213
0x207A4 STATISTICS_PLANE_TOTAL_1	Total pixel registers processed per plane1	10-214
0x207A8 STATISTICS_PLANE_TOTAL_2	Total pixel registers per plane processed 2	10-214
0x207AC STATISTICS_PLANE_TOTAL_3	Total pixel registers processed per plane3	10-215
0x207B0 STATISTICS_PLANE_COUNTED_0	Accumulated sum register 0 for total pixels per plane	10-215
0x207B4 STATISTICS_PLANE_COUNTED_1	Accumulated sum register of total pixels per plane 1	10-215
0x207B8 STATISTICS_PLANE_COUNTED_2	Accumulation and sum register of total pixels per plane 2	10-216
0x207BC STATISTICS_PLANE_COUNTED_3	Accumulated Sum Register 3 of Total Pixels Per Plane	10-216
0x207C0 STATISTICS_HISTOGRAM_CTRL	Histogram Control Register	10-217
0x207C4 STATISTICS_SCALAND	SCALE Control Register	10-218
0x207C8 STATISTICS_TOTAL_PIXELS	STATISTICS Total Number of Pixels Processed Registers 10-219	
0x207CC STATISTICS_COUNTED_PIXELS	STATISTICS Accumulated pixel number register 10-219	
0x207D0 STATISTICS_PE_HISTOGRAM_CTRL	PE Control Register	10-220
0x207D4 STATISTICS_PE_SCBUT	PE_SCALE Control Register	10-222
0x207D8 STATISTICS_PE_TOTAL_PIXELS	Total Number of Pixels Processed by PE Register	10-222
0x207DC STATISTICS_PE_COUNTED_PIXELS	PE Accumulated pixel number register	10-223
0x207E0 STATISTICS_PLANE_TOTAL_PE_0	PE Total pixel registers processed per plane 0	10-223
0x207E4 STATISTICS_PLANE_TOTAL_PE_1	PE total pixel registers processed per plane1	10-224
0x207E8 STATISTICS_PLANE_TOTAL_PE_2	PE total pixel registers processed per plane2	10-224

offset address name	describe	page number
0x207EC STATISTICS_PLANE_TOTAL_PE_3	PE Total pixel registers processed per plane3	10-224
0x207F0 STATISTICS_PLANE_COUNTED_PE_0	PE Accumulated sum register of total pixels per plane 0	10-225
0x207F4 STATISTICS_PLANE_COUNTED_PE_1	PE Accumulated sum register of total pixels per plane 1	10-225
0x207F8 STATISTICS_PLANE_COUNTED_PE_2	PE Accumulated sum register of total pixels per plane 2	10-226
0x207FC STATISTICS_PLANE_COUNTED_PE_3	PE Accumulated sum register of total pixels per plane 3	10-226
0x20800 STATISTICS_SUM_R	The normalized R component pixel sum	10-226
0x20804 STATISTICS_SUM_RG	The normalized Gr component pixels and	10-227
0x20808 STATISTICS_SUM_BG	The normalized Gb component pixel sum	10-227
0x2080C STATISTICS_SUM_B	The normalized B component pixel sum	10-228
0x20810 STATISTICS_AE_SUM_NODES_USED	AE_SUM Active Area Register	10-228
0x20820 STATISTICS_AVG_R	Bayer domain AWB SUM statistics R component mean 10-228	
0x20824 STATISTICS_AVG_G	Bayer domain AWB SUM statistics G component mean 10-229	
0x20828 STATISTICS_AVG_B	Bayer Domain AWB SUM Statistics B Component Mean 10-229	
0x2082C STATISTICS_COUNT_ALL	Bayer domain AWB SUM counts the number of pixels that meet the white point condition, normalized	10-230
0x20830 STATISTICS_COUNT_MIN	Bayer domain AWB SUM counts the number of pixels less than the lower limit of brightness	10-230
0x20834 STATISTICS_COUNT_MAX	Bayer domain AWB SUM counts the number of pixels greater than the upper limit of brightness	10-230
0x20838 STATISTICS_AWB_SUM_NODES_USED	AWB_SUM Active Area Register	10-231
0x2083C STATISTICS_MIN_THRESHOLD	Lower limit of luminance for Bayer domain AWB SUM statistical white point	10-231

offset address name	describe	page number
0x20840 STATISTICS_MAX_THRESHOLD	Brightness upper limit for white point in Bayer domain AWB SUM statistics	10-232
0x20844 STATISTICS_AWB_SUM_CLIP	AWB SUM clip	10-232
0x20848 STATISTICS_CR_RIF	Chromaticity R/G upper and lower limits of AWB statistical white point in Bayer domain	10-233
0x2084C STATISTICS_CB_RIF	Chroma B/G upper and lower limits of AWB statistical white point in Bayer domain	10-233
0x20850 STATISTICS_CR_HL_REF	Chromaticity R/G Hexagon Limits for Bayer Domain AWB Statistics White Point	10-234
0x20854 STATISTICS_CB_HL_REF	Chromaticity B/G Hexagon Limits of Bayer Field AWB Statistical White Point	10-234
0x20900 FRAME_STATS_STATS_RESET	Status Reset Register	10-235
0x20904 FRAME_STATS_STATS_HOLD	Status Holding Register	10-235
0x20910 FRAME_STATS_ACTIVE_WIDTH_MIN	Minimum Width Register	10-236
0x20914 FRAME_STATS_ACTIVE_WIDTH_MAX	Maximum Width Register	10-236
0x20918 FRAME_STATS_ACTIVE_WIDTH_SUM	Effective Width and Registers	10-237
0x2091C FRAME_STATS_ACTIVE_WIDTH_NUM	Effective Width Register	10-237
0x20920 FRAME_STATS_ACTIVE_HEIGHT_MIN	minimum height register	10-238
0x20924 FRAME_STATS_ACTIVE_HEIGHT_MAX	Maximum Height Register	10-238
0x20928 FRAME_STATS_ACTIVE_HEIGHT_SUM	Effective Height and Registers	10-238
0x2092C FRAME_STATS_ACTIVE_HEIGHT_NUM	effective height register	10-239
0x20930 FRAME_STATS_HBLANK_MIN	minimum horizontal blanking	10-239
0x20934 FRAME_STATS_HBLANK_MAX	Maximum Horizontal Blanking	10-239

offset address name		describe	page number
0x20938	FRAME_STATS_HBLANK_SUM	Horizontal Blanking and Register	10-240
0x2093C	FRAME_STATS_HBLANK_NUM	Horizontal Blanking Register	10-240
0x20940	FRAME_STATS_VBLANK_MIN	Minimum vertical consumption	10-240
0x20944	FRAME_STATS_VBLANK_MAX	Maximum Vertical Blanking	10-241
0x20948	FRAME_STATS_VBLANK_SUM	Vertical Blanking and Register	10-241
0x2094C	FRAME_STATS_VBLANK_NUM	Vertical Blanking Register	10-241
0x21004	NOISE_PROFILE_WDR_4	WDR 4 Noise Offset	10-242
0x21014	NOISE_PROFILE_WDR_3	WDR 3 Noise Offset	10-242
0x21024	NOISE_PROFILE_WDR_2	WDR 2 Noise Offset	10-243
0x21034	NOISE_PROFILE_WDR_1	WDR 1 Noise Offset	10-243
0x21200~0x2127C	NOISE_PROFILE_FCOPPER_STITCH_LUT_1	FRAME_STITCH noise distribution table 1	10-243
0x21280~0x212FC	NOISE_PROFILE_FCOPPER_STITCH_LUT_2	FRAME_STITCH noise distribution table 2	10-244
0x21300~0x2137C	NOISE_PROFILE_FCOPPER_STITCH_LUT_3	FRAME_STITCH noise distribution table 3	10-244
0x21380~0x213FC	NOISE_PROFILE_FCOPPER_STITCH_LUT_4	FRAME_STITCH noise distribution table 4	10-245
0x21540~0x2155C	DNR_SHADING Radial LUT0		10-245
0x21560	DNR_SHADING_LAST	Radial LUT1	10-246
0x21580~0x215FC	NOISE_PROFILE_RAW_FRONTEND_LUT_1	RAW_FRONTEND noise distribution table 1	10-246

offset address	name	describe	page number
0x21600~0x2167C	NOISE_PROFILE_RAW_FRONTEND_LUT_2	RAW_FRONTEND noise distribution table 2	10-247
0x21680~0x216FC	NOISE_PROFILE_RAW_FRONTEND_LUT_3	RAW_FRONTEND noise distribution table 3	10-247
0x21700~0x2177C	NOISE_PROFILE_RAW_FRONTEND_LUT_4	RAW_FRONTEND noise distribution table 4	10-248
0x21800~0x2187C	NOISE_PROFILE_LOUT	DNR Noise Distribution Table	10-248
0x21880~0x218FC	NOISE_PROFILE_DEMOSAIC_LUT	DEMOSAIC Noise Distribution Table	10-249
0x21900~0x219F8	AEXP_WEIGHT	AE block weight	10-249
0x219FC	AEXP_WEIGHT_LAST	AE last block weight	10-250
0x21B00~0x21EFC	AWB_WEIGHT	AWB block weight	10-251
0x22800~0x22880	GAMMA_FE0_MEM0	GAMMA_FE0 Bank0 Lookup Table	10-251
0x22900~0x22980	GAMMA_FE0_MEM1	GAMMA_FE0 Bank1 lookup table	10-252
0x23000~0x23400	GAMMA_FE1_MEM0	GAMMA_FE1 Bank0 Lookup Table	10-252
0x23800~0x23C00	GAMMA_FE1_MEM1	GAMMA_FE1 Bank1 lookup table	10-252
0x24800~0x24880	GAMMA_BE0_MEM0	GAMMA_BE0 Bank0 lookup table	10-253
0x24900~0x24980	GAMMA_BE0_MEM1	GAMMA_BE0 Bank1 lookup table	10-253
0x25000~0x25400	GAMMA_BE1_MEM0	GAMMA_BE1 Bank0 lookup table	10-254
0x25800~0x25C00	GAMMA_BE1_MEM1	GAMMA_BE1 Bank1 lookup table	10-254
0x26000~0x26200	RADIAL_SHADING_MEM_R	RADIAL_SHADING R component lookup table 10-254	
0x26400~0x26600	RADIAL_SHADING_MEM_G	RADIAL_SHADING G component lookup table 10-255	

offset address	name	describe	page number
0x26800~0x26A00	RADIAL_SHADING_MEM_B	RADIAL_SHADING B component lookup table 10-255	
0x28000~0x2DFFC	METERING_MEM	AE stat, AE sum, AWB stat, AWB sum statistics	10-256
0x30000~0x33FFC	DEFECT_PIXEL_MIN	static defect pixels bad pixel table	10-256
0x34000~0x34FFC	HISTOGRAM1_MEM	Histogram Statistics 1	10-256
0x35000~0x353FC	HISTOGRAM2_MEM	Histogram Statistics 2	10-257
0x35400~0x357FC	HISTOGRAM3_MEM	Histogram Statistics 3	10-257
0x35800~0x35BFC	HISTOGRAM4_MEM	Histogram Statistics 4	10-257
0x37000~0x37400	GAMMA_RGB_MEM0	GAMMA_RGB Bank0 Lookup Table	10-258
0x37800~0x37C00	GAMMA_RGB_MEM1	GAMMA_RGB Bank1 lookup table	10-258
0x38000~0x38200	DRC_FWD_MEM	DRC_FWD table	10-259
0x38800~0x38A00	DRC_REV_MEM	DRC_REV table	10-259
0x39000~0x393FC	CMD_QUEUES	CMD table	10-259
0x3C000~0x3EFFC	SHADING_MEM	mesh shading table	10-260
0x40094	ISP_BE_FSTART_DELAY	ISP adjustable interrupt trigger time configuration	10-260
0x400A0	ISP_BE_USER_DEFINE0	User Defined Register 0	10-260
0x400A4	ISP_BE_USER_DEFINE1	User-Defined Register 1	10-261
0x400F0	ISP_BE_INT	ISP Interrupt Indicator Register	10-261
0x400F8	ISP_BE_INT_MASK	ISP interrupt mask register	10-262
0x401E0	ISP_BE_CTRL_F	ISP General Update Control Register	10-263
0x401E4	ISP_BE_CTRL_I	ISP immediately updates the control register	10-264

offset address name	describe	page number
0x4182C ISP_MIDF_SIZE	median filter input image chroma width and height	10-278
0x41844 ISP_MCDS_PARA	NR fusion scale and shift	10-278
0x418F0 ISP_MCDS_SIZE	MCDS input image width and height	10-279
0x45200 ISP_SHARPEN_CFG	SHARPEN control register	10-279
0x45210 ISP_SHARPEN_AMT	SHARPEN Strength	10-280
0x4521C ISP_SHARPEN_SHOOTWAITING FOR	SHARPENshoot AMT Control	10-280
0x45224 ISP_SHARPEN_EDHUNTING	Sawtooth High Frequency Parameters	10-280
0x45228 ISP_SHARPEN_OSHTJAG	sawtooth overshoot parameter	10-281
0x4522C ISP_SHARPEN_USHTJAG	Sawtooth undershoot parameter	10-281
0x45230 ISP_SHARPEN_MID0	SHARPEN IF filter coefficient	10-282
0x45234 ISP_SHARPEN_MID1	SHARPEN IF filter coefficient	10-282
0x45238 ISP_SHARPEN_MID2	SHARPEN IF filter coefficient	10-283
0x4523C ISP_SHARPEN_LINETHD	SHARPEN line detection threshold	10-283
0x45240 ISP_SHARPEN_THD2	SHARPEN Threshold 2	10-284
0x45244 ISP_SHARPEN_CTRL	SHARPEN control	10-284
0x45248 ISP_SHARPEN_LUMATH	LUMATH parameter	10-285
0x4524C ISP_SHARPEN_LUMAWGT	LUMAWgt parameters	10-286
0x45258 ISP_SHARPEN_OSHTVARTH	Variance threshold parameter 0	10-286
0x4525C ISP_SHARPEN_OSHTVAR	overshoot variance parameter 0	10-287
0x45260 ISP_SHARPEN_USHTVARTH	Variance Threshold Parameter 1	10-287

offset address name	describe	page number
0x45264 ISP_SHARPEN_US HTVAR	overshoot variance parameter 1	10-288
0x45268 ISP_SHARPEN_OS HTLUMA	overshoot brightness parameter 0	10-288
0x4526C ISP_SHARPEN_US HTLUMA	Overshoot Brightness Parameter 1	10-289
0x45274 ISP_SHARPEN_SHI FT	SHIFT parameter	10-289
0x452F0 ISP_SHARPEN_SIZ AND	SHARPEN image width and height	10-290
0x46200 ISP_DEHAZE_CFG DEHAZE enable register		10-290
0x46210 ISP_DEHAZE_PRE_ UPDATE	DEHAZE statistical result update register	10-291
0x46214 ISP_DEHAZE_BLK_ SIZE	DEHAZE block size configuration register	10-291
0x46218 ISP_DEHAZE_BLK_ SUM	Total number of DEHAZE chunks	10-292
0x4621C ISP_DEHAZE_DC_S IZE	DEHAZE The number of bilinear interpolation points configuration register	10-292
0x46220 ISP_DEHAZE_X	DEHAZE The horizontal phase difference configuration register between the enlarged image pixels	10-293
0x46224 ISP_DEHAZE_Y	DEHAZE The vertical phase difference configuration register between enlarged image pixels	10-293
0x46228 ISP_DEHAZE_STAT _MODE	DEHAZE Statistics Module Control Register	10-294
0x4622C ISP_DEHAZE_NEG _MODE	DEHAZE Negative processing control register	10-294
0x46230 ISP_DEHAZE_AIR DEHAZE atmospheric light configuration register		10-295
0x46234 ISP_DEHAZE_THL D	DEHAZE's T Threshold Coefficient Configuration Register 10-295	
0x46238 ISP_DEHAZE_GST RTH	Global intensity coefficient for DEHAZE	10-296
0x4623C ISP_DEHAZE_BLT HLD	DEHAZE Minimum Filter Threshold Coefficient Configuration Register	10-296
0x46240 ISP_DEHAZE_STR_ LUT_UPDATE	DEHAZE Intensity Meter Update Register	10-297

offset address name	describe	page number
0x46280 ISP_DEHAZE_MINSTAT_WADDR	DEHAZE Minimum Statistics Write Address Register	10-297
0x46284 ISP_DEHAZE_MINSTAT_WDATA	DEHAZE Minimum Statistics Write Data Register	10-298
0x46288 ISP_DEHAZE_MINSTAT_RADDR	DEHAZE Minimum Statistics Read Address Register	10-298
0x4628C ISP_DEHAZE_MINSTAT_RDATA	DEHAZE Minimum Statistics Read Data Register	10-298
0x46290 ISP_DEHAZE_MAXSTAT_WADDR	DEHAZE Maximum Statistics Write Address Register	10-299
0x46294 ISP_DEHAZE_MAXSTAT_WDATA	DEHAZE Maximum Statistics Write Data Register	10-299
0x46298 ISP_DEHAZE_MAXSTAT_RADDR	DEHAZE Maximum Statistics Read Address Register	10-300
0x4629C ISP_DEHAZE_MAXSTAT_RDATA	DEHAZE Maximum Statistics Read Data Register	10-300
0x462A0 ISP_DEHAZE_PRESTAT_WADDR	DEHAZE Write address register of the minimum value statistics information of the previous frame	10-301
0x462A4 ISP_DEHAZE_PRESTAT_WDATA	DEHAZE Write the minimum value statistics information of the previous frame to the data register	10-301
0x462A8 ISP_DEHAZE_PRESTAT_RADDR	DEHAZE Last frame minimum statistical information read address register	10-302
0x462AC ISP_DEHAZE_PRESTAT_RDATA	DEHAZE Last frame minimum statistical information read data register	10-302
0x462B0 ISP_DEHAZE_LUT_WADDR	DEHAZE Intensity LUT Information Write Address Register	10-303
0x462B4 ISP_DEHAZE_LUT_wdata	DEHAZE Intensity LUT Information Write Data Register	10-303
0x462B8 ISP_DEHAZE_LUT_RADDR	DEHAZE Strength LUT Information Read Address Register	10-304
0x462BC ISP_DEHAZE_LUT_RDATA	DEHAZE Intensity LUT Information Read Data Register	10-304
0x462F0 ISP_DEHAZE_SIZE	DEHAZE image width and height	10-305
0x51400 ISP_ACM_CTRL	ACM control register	10-305
0x51404 ISP_ACM_ADJ	Amount of pixel change after ACM processing	10-306
0x51410 ISP_ACM_SIZE	ACM handles image size registers	10-307

offset address name	describe	page number
0x51414 ISP_ACM_PARA_ADDR	ACM Coefficient Configuration Load Address Register	10-307
0x51420 ISP_ACM_PARA_UP	ACM Coefficient Configuration Update Register	10-307
0x51C00 ISP_VPDCICTRL	DCI Control Register	10-308
0x51C04 ISP_VPDCIHPOS	Register 10-310 of DCI Algorithm Horizontal Adjustment Area	
0x51C08 ISP_VPDCIVPOS	Register 10-310 of DCI Algorithm Vertical Adjustment Area	
0x51C0C ISP_VPDCIHISBLD	DCI histogram statistical weighting coefficient register	10-311
0x51C10 ISP_VPDCIHISOFT	DCI histogram statistical offset register	10-311
0x51C14 ISP_VPDCIHISCOR	DCI histogram coring register	10-312
0x51C18 ISP_VPDCIMERBLD	The blend value register of the DCI adjustment unit	10-312
0x51C1C ISP_VPDCIADJWGT	Curve weight register for DCI manual configuration	10-313
0x51C20 ISP_VPDCICLIP0	DCI curve 0 weight range register	10-313
0x51C24 ISP_VPDCICLIP1	DCI Curve 1 Weight Range Register	10-314
0x51C28 ISP_VPDCICLIP2	DCI Curve 2 Weight Range Register	10-314
0x51C2C ISP_VPDCIGLBGAIN	DCI Dimming Unit Global Gain Register 10-315	
0x51C30 ISP_VPDCIPOSTHR0	Threshold 0 register for forward regulation of DCI regulation unit	10-315
0x51C34 ISP_VPDCIPOSTHR1	Threshold 1 register for forward regulation of DCI regulation unit	10-316
0x51C38 ISP_VPDCIPOSGAIN0	Gain 0 Register for DCI Tuning Unit Forward Tuning	10-316
0x51C3C ISP_VPDCIPOSGAIN1	Gain 1 Register for DCI Tuning Unit Forward Tuning	10-317
0x51C40 ISP_VPDCIPOSSLP0	Slope 0 register for positive regulation of DCI regulation unit	10-317
0x51C44 ISP_VPDCIPOSSLP1	Slope 1 register for positive regulation of DCI regulation unit	10-318
0x51C48 ISP_VPDCIPOSSLP2	Slope 2 register for positive regulation of DCI regulation unit	10-318

offset address name	describe	page number
0x51C4C ISP_VPDCINEGTH R0	Threshold 0 register for negative regulation of the DCI regulation unit	10-319
0x51C50 ISP_VPDCINEGTH R1	Threshold 1 Register for Negative Regulation of DCI Regulation Unit	10-319
0x51C54 ISP_VPDCINEGGAI N0	Gain 0 Register for DCI Tuning Unit Negative Tuning	10-320
0x51C58 ISP_VPDCINEGGAI N1	Gain 1 Register for DCI Tuning Unit Negative Tuning	10-321
0x51C5C ISP_VPDCINEGSLP 0	Slope 0 register for negative regulation of the DCI regulation unit	10-321
0x51C60 ISP_VPDCINEGSLP 1	Slope 1 register for negative regulation of the DCI regulation unit	10-321
0x51C64 ISP_VPDCINEGSLP 2	Slope 2 register for negative regulation of the DCI regulation unit	10-322
0x60000 ISPFE_MAX_ADDR ISP BUFFER maximum address register		10-322
0x60004 ISPFE_MAX_ADDR 2	ISP BUFFER maximum address register 2	10-323
0x60008 ISPFE_MAX_ADDR _NUMBER 1	ISP NR BUFFER1 Maximum address register 10-323	
0x6000C ISPFE_MAX_ADDR _NR2	ISP NR BUFFER2 Maximum address register 10-324	
0x60010 ISPFE_TIMING	ISP Timing Configuration Register	10-324
0x60014 ISPFE_MAX_ADDR 3	ISP BUFFER maximum address register 3	10-325
0x60018 ISPFE_MAX_ADDR 4	ISP BUFFER maximum address register 4	10-325
0x60020 ISPFE_BYTE_EN	ISP BYTE_EN configuration register	10-325
0x60028 ISPFE_CH_SWITCH ISP input switching register		10-326
0x6002C ISPFE_FE_BYPASS _CFG	ISP FE BYPASS Register	10-328
0x60030 ISPFE_CROP_CFG CROP enable register		10-328
0x60034 ISPFE_CROP_WIN CROP window register		10-329
0x60038 ISPFE_CROP0_STA RT	0 area CROP start position register	10-329
0x6003C ISPFE_CROP0_SIZE 0 area CROP size setting register		10-330

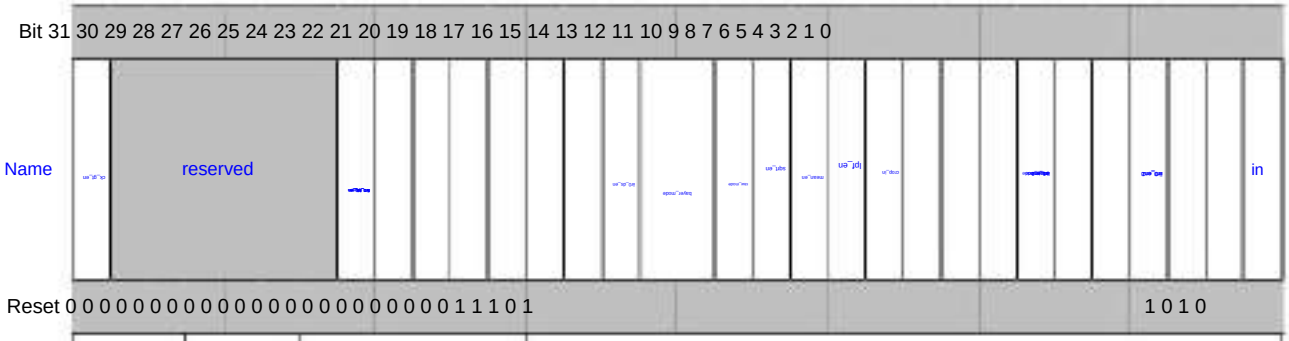
offset address name	describe	page number
0x63a04 ISP_FPN_CALIB_START	FPN calibration start calibration signal register	10-347
0x63a08 ISP_FPN_CORR_CFG	FPN Correction Configuration Register	10-348
0x63a0C ISP_FPN_STAT	FPN Calibration Status Register	10-349
0x63a10 ISP_FPN_WHITE_LEVEL	FPN calibration white point configuration register	10-349
0x63a18 ISP_FPN_DIVCOEF	FPN calibration division coefficient register	10-350
0x63a1C ISP_FPN_FRAMELOG2	FPN calibrated frame number register	10-350
0x63a20 ISP_FPN_SUM0	FPN Scaled Accumulation and Low Register	10-351
0x63a24 ISP_FPN_SUM1	FPN Scale Accumulation and High Register	10-351
0x63a30 ISP_FPN_CORR0	FPN Correction Configuration 0 Register	10-352
0x63a34 ISP_FPN_CORR1	FPN Correction Configuration 1 Register	10-352
0x63a38 ISP_FPN_CORR2	FPN Correction Configuration 2 Register	10-353
0x63a3C ISP_FPN_CORR3	FPN Correction Configuration 3 Register	10-353
0x63a40 ISP_FPN_SHIFT	FPN Shift Configuration Register	10-353
0x63a50 ISP_FPN_MAX_O	FPN output maximum value register	10-354
0x63a54 ISP_FPN_OVERFLOWTHR	FPN correction threshold	10-354
0x63a80 ISP_FPN_LINE_WADDR	FPN Line Mode Black Line Write Address Register	10-355
0x63a84 ISP_FPN_LINE_WDminutes	FPN Line Mode Black Line Write Data Register	10-355
0x63a88 ISP_FPN_LINE_RADDR	FPN row mode black row read address register	10-356
0x63a8C ISP_FPN_LINE_RDminutes	FPN Line Mode Black Line Read Data Register	10-356
0x63aE0 ISP_FPN_CTRL_F	FPN general control register	10-356
0x63aE4 ISP_FPN_CTRL_I	FPN immediate update control register	10-357
0x63aE8 ISP_FPN_TIMING	FPN output timing configuration register	10-358
0x63aEC ISP_FPN_UPDATE	FPN register update register	10-358
0x63aF0 ISP_FPN_SIZE	FPN image width and height register	10-358

10.5.2 ISP register description

ISP_AF_CFG

ISP_AF_CFG is the AF control register.

Offset Address	Register Name	Total Reset Value
0x12000	ISP_AF_CFG	0x0000_01DA



Bits	Access	Name	Description
[31]	RW	ck_gt_en	Clock gating enable for AF. 0: forbidden; 1: enable.
[30:25]	RO	reserved	reserve.
[24]	RW	fir1_ldg_en	Vertical FIR filter LDG (luma dependent gain) enable 1. 0: forbidden; 1: enable.
[23]	RW	fir0_ldg_en	Vertical FIR filter LDG (luma dependent gain) enable 0. 0: forbidden; 1: enable.
[22]	RW	iir1_ldg_en	Horizontal IIR filter LDG (luma dependent gain) enable 1. 0: forbidden; 1: enable.
[21]	RW	iir0_ldg_en	Horizontal IIR filter LDG (luma dependent gain) enable 0. 0: forbidden; 1: enable.
[20]	RW	for 1_lpf_en	Vertical FIR filter LPF (low pass filter) enable 1. 0: forbidden; 1: enable.

[19] RW fir0_lpf_en			Vertical FIR filter LPF (low pass filter) enable 0. 0: forbidden; 1: enable.
[18] RW iir1_ds_en			Horizontal IIR filter DS(down sample) enable 1. 0: disable; 1: enable.
[17] RW iir0_ds_en			Horizontal IIR filter DS(down sample) enable 0. 0: forbidden; 1: enable.
[16:15] RW bayer_mode			AF RAW format. 00ÿRGGBÿ 01ÿGRBGÿ 10ÿGBRGÿ 11ÿBGGRÿ
[14] RW raw_mode			AF data format. 0: YUV data; 1: RAW data.
[13] RW sqrt_en			AF Gamma enabled. 0: forbidden; 1: enable.
[12] RW mean_en			AF median filter enable. 0: forbidden; 1: enable.
[11] RW lpf_en			AF low pass filter enable. 0: forbidden; 1: enable.
[10] RW crop_en			AFcrop Cropping enabled. 0: forbidden; 1: enable.
[9] RW offset_en			offset is enabled. 0: disable; 1: enable.
[8] RW squ_mode			AF Statistical square mode. 0: The statistical value is directly accumulated and counted; 1: Statistical values are squared first and then cumulatively counted.

[7] RW peak_mode			AF stat peaking mode. 0: Select each value in the block for statistics; 1: Select the maximum value of each row in the block for statistics.
[6] RW iir1_en2			Enable of the 2nd IIR in the second set of 3 IIR cascades. 0: disable; 1: enable.
[5] RW iir1_en1			Enable of the 1st IIR in the second set of 3 IIR cascades. 0: forbidden; 1: enable.
[4] RW iir1_en0			Enable of the 0th IIR in the second set of 3 IIR cascades. 0: forbidden; 1: enable.
[3] RW iir0_en2			Enable of the 2nd IIR in the first set of 3 IIR cascades. 0: forbidden; 1: enable.
[2] RW iir0_en1			Enable of the 1st IIR in the first set of 3 IIR cascades. 0: forbidden; 1: enable.
[1] RW iir0_en0			Enable of the 0th IIR in the first set of 3 IIR cascades. 0: forbidden; 1: enable.
[0] RW and			AF is enabled. 0: forbidden; 1: enable.

ISP_OF_ZONE

ISP_AF_ZONE allocates registers for AF zone.

Offset Address	Register Name	Total Reset Value
0x12010	ISP_OF_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				one				----				afterwards			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1		

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:8]	RW	one	The number of windows in the vertical direction of AF (up to 15). crop_en==1, window in CH_AF_CROP_SIZE area; crop_en==0, window in CH_AF_SIZE area.
[7:5]	RO	reserved	reserve.
[4:0]	RW	hnum	The number of windows in the horizontal direction of AF (maximum 17). crop_en==1, window in CH_AF_CROP_SIZE area; crop_en==0, window in CH_AF_SIZE area.

ISP_AF_CROP_START

ISP_AF_CROP_START is the AF image CROP start coordinate register.

Offset Address	Register Name	Total Reset Value
0x12014	ISP_AF_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	----			pos_y													----			pos_x												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	pos_y	The ordinate of the starting point of CROP.
[15:13]	RO	reserved	reserve.
[12:0]	RW	pos_x	The abscissa of the starting point of CROP.

ISP_AF_CROP_SIZE

ISP_AF_CROP_SIZE is the AF image CROP SIZE register.

Offset Address	Register Name	Total Reset Value
0x12018	ISP_AF_CROP_SIZE	0x0000_0000

Bit	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	vsize	—	hsize
Reset	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	vsize	The height of the image after AF CROP. Note: The configuration is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	hsize	The width of the image after AF CROP. Note: The configuration is minus 1 from the actual value.

ISP_AF_MEAN_THRES

ISP_AF_MEAN_THRES is the AF median filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x1201C	ISP_AF_MEAN_THRES	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	mean_thres
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	mean_thres	AF median filter register threshold.

ISP_AF_IIRG0

ISP_AF_IIRG0 is the AF IIR filter parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x12020	ISP_AF_IIRG0	0x00A1_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iirg0_1								reserved							iirg0_0	
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	iirg0_1	AF IIR filter 1 group g0 gain. Note: Affects the configuration value of ISP_AF_SHIFT.
[15:8]	RO	reserved	reserve.
[7:0]	RW	iirg0_0	AF IIR filter group 0 g0 gain. Note: Affects the configuration value of ISP_AF_SHIFT.

ISP_AF_IIRG1

ISP_AF_IIRG1 is the AF IIR filter parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x12024	ISP_AF_IIRG1	0x0244_01BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iirg1_1								reserved							iirg1_0	
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg1_1	AF IIR filter 1 group g1 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg1_0	AF IIR filter group 0 g1 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRG2

ISP_AF_IIRG2 is the AF IIR filter parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x12028	ISP_AF_IIRG2	0x0328_0328

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iirg2_1								reserved							iirg2_0	
Reset	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg2_1	AF IIR filter 1 group g2 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg2_0	AF IIR filter group 0 g2 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRG3

ISP_AF_IIRG3 is the AF IIR filter parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x1202C	ISP_AF_IIRG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iirg3_1								reserved							iirg3_0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg3_1	AF IIR filter 1 group g3 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg3_0	AF IIR filter group 0 g3 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRG4

ISP_AF_IIRG4 is the AF IIR filter parameter 4 register.

Offset Address	Register Name	Total Reset Value
0x12030	ISP_AF_IIRG4	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	iirg4_1	reserved	iirg4_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg4_1	AF IIR filter 1 group g4 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg4_0	AF IIR filter group 0 g4 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRG5

ISP_AF_IIRG5 is the AF IIR filter parameter 5 register.

Offset Address	Register Name	Total Reset Value
0x12034	ISP_AF_IIRG5	0x0284_017C

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	iirg5_1	reserved	iirg5_0
Reset	0 0 0 0 0 1 0 1	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0	1 0 1 1 1 1 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg5_1	AF IIR filter 1 group g5 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg5_0	AF IIR filter group 0 g5 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRG6

ISP_AF_IIRG6 is the AF IIR filter parameter 6 register.

Offset Address	Register Name	Total Reset Value
0x12038	ISP_AF_IIRG6	0x033C_033C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iirg6_1	reserved	iirg6_0
Reset	0 0 0 0 0 0 1 1 0 0 1	1 1 1 0 0 0 0 0 0 0 0 1 1 0 0 1 1	1 0 0

Bits	Access Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	iirg6_1	AF IIR filter 1 group g6 gain. Note: sign number, cannot take negative boundary -512.
[15:10]	RO	reserved	reserve.
[9:0]	RW	iirg6_0	AF IIR filter group 0 g6 gain. Note: sign number, cannot take negative boundary -512.

ISP_AF_IIRPL

ISP_AF_IIRPL is the AF IIR filter preset register.

Offset Address	Register Name	Total Reset Value
0x1203C	ISP_AF_IIRPL	0x0000_0000

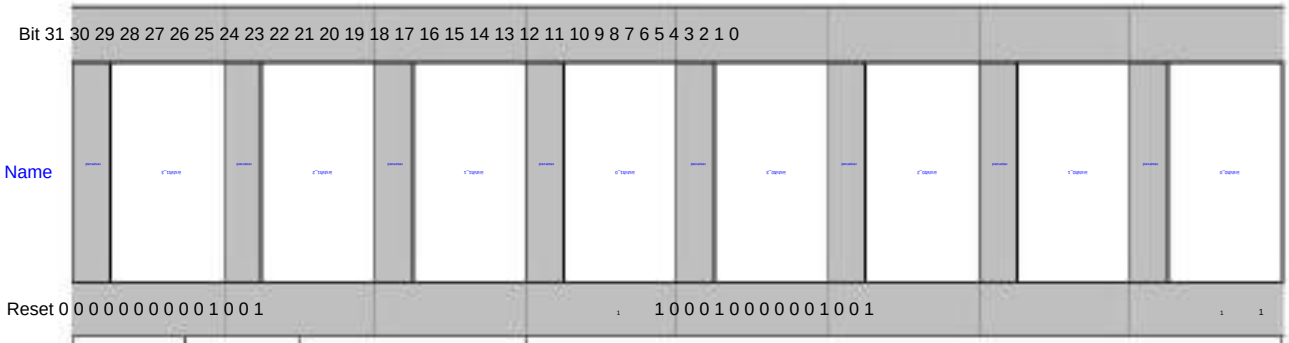
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iirplg_1	reserved	iirplg_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:27]	RO	reserved	reserve.
[26:24]	RW	iirpls_1	AF IIR filter 1 set of preset shifts.
[23:16]	RW	iirplg_1	AF IIR filter 1 group preset gain.
[15:11]	RO	reserved	reserve.
[10:8]	RW	iirpls_0	AF IIR filter group 0 preset shift.
[7:0]	RW	iirplg_0	AF IIR filter group 0 preset gain.

ISP_OF_SHIFT

ISP_AF_SHIFT is the AF IIR filter shift parameter register.

Offset Address	Register Name	Total Reset Value
0x12040	ISP_OF_SHIFT	0x0027_1027



Bits	Access Name		Description
[31]	RO	reserved	reserve.
[30:28]	RW iirshift1_3		AF IIR filter 1 group IIR2 shift adjustment.
[27]	RO	reserved	reserve.
[26:24]	RW iirshift1_2		AF IIR filter 1 group IIR1 shift adjustment.
[23]	RO	reserved	reserve.
[22:20]	RW iirshift1_1		AF IIR filter 1 group IIR0 shift adjustment.
[19]	RO	reserved	reserve.
[18:16]	RW iirshift1_0		AF IIR filter 1 group input shift adjustment. Notice: iirg0_1>=128ÿiirshift0_0>=4ÿ iirg0_1>= 64ÿiirshift0_0>=3ÿ iirg0_1>= 32ÿiirshift0_0>=2ÿ iirg0_1>= 16ÿiirshift0_0>=1ÿ
[15]	RO	reserved	reserve.
[14:12]	RW iirshift0_3		AF IIR filter 0 group IIR2 shift adjustment.
[11]	RO	reserved	reserve.
[10:8]	RW iirshift0_2		AF IIR filter 0 group IIR1 shift adjustment.
[7]	RO	reserved	reserve.
[6:4]	RW iirshift0_1		AF IIR filter 0 group IIR0 shift adjustment.
[3]	RO	reserved	reserve.

[2:0] RW	iirshift0_0		AF IIR Filter Group 0 input shift adjustment. Notice: iirg0_0 >=128ÿiirshift0_0>=4ÿ iirg0_0 >= 64ÿiirshift0_0>=3ÿ iirg0_0 >= 32ÿiirshift0_0>=2ÿ iirg0_0 >= 16ÿiirshift0_0>=1ÿ

ISP_AF_FIRH0

ISP_AF_FIRH0 is the AF FIR filter parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x12050	ISP_AF_FIRH0	0x0030_0030

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	farh0_1	reserved	farh0_0
Reset	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	firh0_1	AF FIR filter group 1 h0 gain. Note: sign number, cannot take negative boundary -32.
[15:6]	RO	reserved	reserve.
[5:0]	RW	firh0_0	AF FIR filter group 0 h0 gain. Note: sign number, cannot take negative boundary -32.

ISP_AF_FIRH1

ISP_AF_FIRH1 is the AF FIR filter parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x12054	ISP_AF_FIRH1	0x0015_002B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	farh1_1	reserved	farh1_0
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.

[21:16]	RW	firh1_1	AF FIR filter 1 group h1 gain. Note: sign number, cannot take negative boundary -32.
[15:6]	RO	reserved	reserve.
[5:0]	RW	firh1_0	AF FIR filter group 0 h1 gain. Note: sign number, cannot take negative boundary -32.

ISP_AF_FIRH2

ISP_AF_FIRH2 is the AF FIR filter parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x12058	ISP_AF_FIRH2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	firh2_1	reserved	firh2_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	firh2_1	AF FIR filter 1 group h2 gain. Note: sign number, cannot take negative boundary -32.
[15:6]	RO	reserved	reserve.
[5:0]	RW	firh2_0	AF FIR filter group 0 h2 gain. Note: sign number, cannot take negative boundary -32.

ISP_AF_FIRH3

ISP_AF_FIRH3 is the AF FIR filter parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x1205C	ISP_AF_FIRH3	0x002B_0015

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	firh3_1	reserved	firh3_0
Reset	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 1	1 0 0 0 0 0 0 0	0 0 0 1 0 1 0 1

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.

[21:16] RW	firh3_1		AF FIR filter 1 group h3 gain. Note: sign number, cannot take negative boundary -32.
[15:6] RO		reserved	reserve.
[5:0] RW	firh3_0		AF FIR filter group 0 h3 gain. Note: sign number, cannot take negative boundary -32.

ISP_AF_FIRH4

ISP_AF_FIRH4 is the AF FIR filter parameter 4 register.

Offset Address	Register Name	Total Reset Value
0x12060	ISP_AF_FIRH4	0x0010_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	firh4_1 reserved firh4_0
Reset	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	firh4_1	AF FIR filter 1 group h4 gain. Note: sign number, cannot take negative boundary -32.
[15:6]	RO	reserved	reserve.
[5:0]	RW	firh4_0	AF FIR filter group 0 h4 gain. Note: sign number, cannot take negative boundary -32.

ISP_AF_ACC_SHIFT

ISP_AF_ACC_SHIFT is the shift register for AF accumulation statistics value.

Offset Address	Register Name	Total Reset Value
0x12078	ISP_AF_ACC_SHIFT	0x0002_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	acc_shift_y acc_shift1_v acc_shift0_v acc_shift1_h acc_shift0_h
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.

[19:16]	RW	acc_shift_y	Brightness Y statistical value shift register (0-15), shifting Y in CH_AF_STAT_RDATA.
[15:12]	RW	acc_shift1_v	1 group of vertical FIR filtering value statistical value shift registers (0-15), shifting V2 in CH_AF_STAT_RDATA.
[11:8]	RW	acc_shift0_v	Group 0 vertical FIR filter value statistical value shift register (0-15), shift V1 in CH_AF_STAT_RDATA.
[7:4]	RW	acc_shift1_h	1 group of horizontal IIR filter value statistical value shift registers (0-15), shifting H2 in CH_AF_STAT_RDATA.
[3:0]	RW	acc_shift0_h	Group 0 horizontal FIR filter value statistical value shift register (0-15), shifting H1 in CH_AF_STAT_RDATA.

ISP_AF_CNT_SHIFT

ISP_AF_CNT_SHIFT is the shift register of AF count statistics value.

Offset Address	Register Name	Total Reset Value
0x1207C	ISP_AF_CNT_SHIFT	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cnt_shift_y cnt_shift1_v cnt_shift0_v cnt_shift1_h cnt_shift0_h
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:16]	RW	cnt_shift_y	Luminance Y count value shift register.
[15:12]	RW	cnt_shift1_v	1 group of vertical FIR filtering value statistical counting shift registers (0-15), shifting vcnt2 in CH_AF_STAT_RDATA.
[11:8]	RW	cnt_shift0_v	Group 0 vertical FIR filter value statistical value shift register (0-15), shift vcnt1 in CH_AF_STAT_RDATA.
[7:4]	RW	cnt_shift1_h	1 group of horizontal IIR filter value statistical shift registers (0-15), shifting hcnt2 in CH_AF_STAT_RDATA.
[3:0]	RW	cnt_shift0_h	Group 0 horizontal FIR filter value statistical value shift register (0-15), to shift hcnt1 in CH_AF_STAT_RDATA.

ISP_AF_STAT_IND_RADDR

ISP_AF_STAT_IND_RADDR is the indirect read address register for the statistical information of each AF block.

Offset Address	Register Name	Total Reset Value
0x12088	ISP_AF_STAT_IND_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	of_state_in_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	af_stat_ind_raddr	Indirect read address register for each block statistics information.

ISP_AF_STAT_IND_RDATA

ISP_AF_STAT_IND_RDATA is the indirect read data register for the statistical information of each AF block.

Offset Address	Register Name	Total Reset Value
0x1208C	ISP_AF_STAT_IND_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	of_stat_ind_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	of_stat_ind_rdata	The statistical information of each block of AF is indirectly read from the data register. Statistics of V1, H1, V2, H2, Y hcnt1, hcnt2, vcnt1, vcnt2 ycnt information of each block. Each address contains the following information: 0x1: {V1(16bit), H1(16bit)} of block 1; 0x2: {V2(16bit), H2(16bit)} of block 1; 0x3: {ycnt(16bit), Y(16bit)} 0x4: {vcnt2(8bit), vcnt1(8bit), hcnt2(8bit), cnt1(8bit)} of block 1; 0x5: {V1(16bit), H1(16bit)} of block 2; … ...and so on. Note: V1 represents the statistical result of the first group of vertical FIR filtering. V2 represents the statistical result of the second group of vertical FIR filtering. H1 represents the statistical results of the first group of horizontal IIR filters. H2 represents the statistical results of the second group of horizontal IIR filtering. Y represents the luminance statistics result. vcnt1 represents the statistical count of FIR filtered values exceeding the threshold. vcnt2 represents the statistical count of FIR filtered values exceeding the threshold. hcnt1 represents the statistical count of IIR filtered values exceeding the threshold. hcnt2 represents the statistical count of IIR filtered values exceeding the threshold. ycnt represents the statistical count of luminances above the threshold.

ISP_AF_CTRL_I

ISP_AF_CTRL_I is the immediate update control register.

Offset Address	Register Name	Total Reset Value
0x120E4	ISP_AF_CTRL_I	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update_mode	The ISP updates the mode register. 0: update update (via ISP_AF_UPDATE register update); 1: frame update.

ISP_AF_UPDATE

ISP_AF_UPDATE is the configuration update register.

Offset Address	Register Name	Total Reset Value
0x120EC	ISP_AF_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update	ISP update register, cleared to 0 automatically every frame.

ISP_AF_SIZE

ISP_AF_SIZE is the AF image size register.

Offset Address	Register Name	Total Reset Value
0x120F0	ISP_AF_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—					vsize											—				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1		1	0	1			1	0	0	0	0	0	1		1	1	0	1	1	1	

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	vsize	The height of the AF input image (configured to the actual value minus 1).
[15:13]	RO	reserved	reserve.
[12:0]	RW	hsize	The width of the AF input image (configured to the actual value minus 1).

ISP_AF_IIRTHRE

ISP_AF_IIRTHRE is the AF IIR filter threshold register.

Offset Address	Register Name	Total Reset Value
0x12100	ISP_AF_IIRTHRE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	iir_thre1_h								iir_thre1_l								iir_thre0_h								iir_thre0_l							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	iir_thre1_h	AF Group 1 IIR filter luma dependent upper threshold.
[23:16]	RW	iir_thre1_l	AF Group 1 IIR filter luma dependent lower threshold.
[15:8]	RW	iir_thre0_h	AF Group 0 IIR filter luma dependent upper threshold.
[7:0]	RW	iir_thre0_l	AF Group 0 IIR filter luma dependent lower threshold.

ISP_AF_IIRGAIN

ISP_AF_IIRGAIN is the AF IIR filter gain register.

Offset Address	Register Name	Total Reset Value
0x12104	ISP_AF_IIRGAIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	iir_gain1_h	iir_gain1_l	iir_gain0_h	iir_gain0_l
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	iir_gain1_h	AF 1 group IIR filter luma dependent high gain.
[23:16]	RW	iir_gain1_l	AF 1 group IIR filter luma dependent low gain.
[15:8]	RW	iir_gain0_h	AF 0 group IIR filter luma dependent high gain.
[7:0]	RW	iir_gain0_l	AF 0 group IIR filter luma dependent low gain.

ISP_AF_IIRSLOPE

ISP_AF_IIRSLOPE is the AF IIR filter slope register.

Offset Address	Register Name	Total Reset Value
0x12108	ISP_AF_IIRSLOPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	iir_slope1_h iir_slope1_l	reserved	iir_slope0_h iir_slope0_l
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	iir_slope1_h	AF Group 1 IIR filter luma dependent high slope.
[19:16]	RW	iir_slope1_l	AF Group 1 IIR filter luma dependent low slope.
[15:8]	RO	reserved	reserve.
[7:4]	RW	iir_slope0_h	AF Group 0 IIR filter luma dependent high slope.
[3:0]	RW	iir_slope0_l	AF Group 0 IIR filter luma dependent low slope.

ISP_AF_IIRDILATE

ISP_AF_IIRDILATE is the AF IIR filter DILATE register.

Offset Address	Register Name	Total Reset Value
0x1210C	ISP_AF_IIRDILATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved		reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:8]	RW	iir_dilate1	Get the local maximum used to calculate the IIR1 luma dependent gain. 000: Take the maximum value among the 8 nearby pixels. 001: Take the maximum value among the 16 nearby pixels. 010: Take the maximum value among the 24 nearby pixels. 011: Take the maximum value among the 32 nearby pixels. 100: Takes the maximum value among the 40 nearby pixels. 101: Take the maximum value among the 48 nearby pixels. 110: Take the maximum value among 56 nearby pixels. 111: Take the maximum value among 64 nearby pixels.
[7:3]	RO	reserved	reserve.
[2:0]	RW	iir_dilate0	Get the local maximum used to calculate the IIR0 luma dependent gain. 000: Take the maximum value among the 8 nearby pixels. 001: Take the maximum value among the 16 nearby pixels. 010: Take the maximum value among the 24 nearby pixels. 011: Take the maximum value among the 32 nearby pixels. 100: Takes the maximum value among the 40 nearby pixels. 101: Take the maximum value among the 48 nearby pixels. 110: Take the maximum value among 56 nearby pixels. 111: Take the maximum value among 64 nearby pixels.

ISP_AF_FIRTHRE

ISP_AF_FIRTHRE is the AF FIR filter threshold register.

Offset Address	Register Name	Total Reset Value
0x12110	ISP_AF_FIRTHRE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	for_thre1_h	for_thre1_l	for_three0_h	for_thre0_l
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	for_thre1_h	AF 1 group FIR filter luma dependent high threshold.
[23:16]	RW	fir_thre1_l	AF 1 group FIR filter luma dependent low threshold.
[15:8]	RW	for_thre0_h	AF 0 group FIR filter luma dependent high threshold.
[7:0]	RW	for_thre0_l	AF 0 group FIR filter luma dependent low threshold.

ISP_AF_FIRGAIN

ISP_AF_FIRGAIN is the AF FIR filter gain register.

Offset Address	Register Name	Total Reset Value
0x12114	ISP_AF_FIRGAIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	for_gain1_h	for_gain1_l	for_gain0_h	for_gain0_l
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	for_gain1_h	AF 1 group of FIR filters luma dependent high gain.
[23:16]	RW	for_gain1_l	AF 1 group FIR filter luma dependent low gain.
[15:8]	RW	for_gain0_h	AF Group 0 FIR filter luma dependent high gain.
[7:0]	RW	for_gain0_l	AF 0 group FIR filter luma dependent low gain.

ISP_AF_FIRSLOPE

ISP_AF_FIRSLOPE is the AF FIR filter slope register.

Offset Address	Register Name	Total Reset Value
0x12118	ISP_AF_FIRSLOPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	for_slope1_h	for_slope1_l	reserved		for_slope0_h	for_slope0_l
Reset	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	for_slope1_h	AF Group 1 FIR filter luma dependent high slope.
[19:16]	RW	for_slope1_l	AF Group 1 FIR filter luma dependent low slope.
[15:8]	RO	reserved	reserve.
[7:4]	RW	for_slope0_h	AF Group 0 FIR filter luma dependent high slope.
[3:0]	RW	for_slope0_l	AF Group 0 FIR filter luma dependent low slope.

ISP_AF_IIRTHRE_CORING

ISP_AF_IIRTHRE_CORING is the AF IIR filter CORING threshold register.

Offset Address	Register Name	Total Reset Value
0x12120	ISP_AF_IIRTHRE_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		iir_thre1_c		reserved		iir_thre0_c
Reset	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	iir_thre1_c	AF Group 1 IIR filter Coring threshold.
[15:11]	RO	reserved	reserve.
[10:0]	RW	iir_thre0_c	AF Group 0 IIR filter Coring threshold.

ISP_AF_IIRPEAK_CORING

ISP_AF_IIRPEAK_CORING is the AF IIR filter CORING peak register.

Offset Address	Register Name	Total Reset Value
0x12124	ISP_AF_IIRPEAK_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iir_peak1_c reserved iir_peak0_c
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	iir_peak1_c	AF 1 group IIR filter Coring peak.
[15:11]	RO	reserved	reserve.
[10:0]	RW	iir_peak0_c	AF 0 group IIR filter Coring peak.

ISP_AF_IIRSLOPE_CORING

ISP_AF_IIRSLOPE_CORING is the AF IIR filter CORING slope register.

Offset Address	Register Name	Total Reset Value
0x12128	ISP_AF_IIRSLOPE_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved iir_slope1_c reserved iir_slope0_c
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	iir_slope1_c	AF Group 1 IIR filter Coring slope.
[7:4]	RO	reserved	reserve.
[3:0]	RW	iir_slope0_c	AF Group 0 IIR filter Coring slope.

ISP_AF_FIRTHRE_CORING

ISP_AF_FIRTHRE_CORING is the AF FIR filter CORING threshold register.

Offset Address	Register Name	Total Reset Value
0x12130	ISP_AF_FIRTHRE_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	for_thre1_c	reserved	for_thre0_c
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	for_thre1_c	AF Group 1 FIR filter Coring threshold.
[15:11]	RO	reserved	reserve.
[10:0]	RW	for_thre0_c	AF 0 Group FIR filter Coring threshold.

ISP_AF_FIRPEAK_CORING

ISP_AF_FIRPEAK_CORING is the AF FIR filter CORING peak register.

Offset Address	Register Name	Total Reset Value
0x12134	ISP_AF_FIRPEAK_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	for_peak1_c	reserved	for_peak0_c
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	for_peak1_c	AF 1 group of FIR filters Coring peak.
[15:11]	RO	reserved	reserve.
[10:0]	RW	for_peak0_c	AF 0 group FIR filter Coring peak.

ISP_OF_FIRSLOPE_CORING

ISP_AF_FIRSLOPE_CORING is the AF FIR filter CORING slope register.

Offset Address	Register Name	Total Reset Value
0x12138	ISP_OF_FIRSLOPE_CORING	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	for_slope1_c	reserved	for_slope0_c
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	for_slope1_c	AF Group 1 FIR filter Coring slope.
[7:4]	RO	reserved	reserve.
[3:0]	RW	for_slope0_c	AF Group 0 FIR filter Coring slope.

ISP_AF_HIGHLIGHT

ISP_AF_HILIGHT is the AF highlight threshold register.

Offset Address	Register Name	Total Reset Value
0x12140	ISP_AF_HIGHLIGHT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	hilight
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hilight	AF brightness count threshold.

ISP_OF_OFFSET

ISP_AF_OFFSET is the AF offset configuration register.

Offset Address	Register Name	Total Reset Value
0x12144	ISP_OF_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	offset_gb															—	offset_gr														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:16]	RW	offset_gb	Gb component offset value.
[15:14]	RO	reserved	reserve.
[13:0]	RW	offset_gr	Gr component offset value.

ISPFE_ACTIVE_WIDTH

ISPFE_ACTIVE_WIDTH is the image width register.

Offset Address	Register Name	Total Reset Value
0x20010	ISPFE_ACTIVE_WIDTH	0x0000_0780

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																active_width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	active_width	Active video width, the unit is pixel.

ISPFE_ACTIVE_HEIGHT

ISPFE_ACTIVE_HEIGHT is the image height register.

Offset Address	Register Name	Total Reset Value
0x20014	ISPFE_ACTIVE_HEIGHT	0x0000_0438

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	active_height
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0 0 0 1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	active_height	Active video height, the unit is line.

ISPFE_RGGB_START

ISPFE_RGGB_START is the RGGB mode register.

Offset Address	Register Name	Total Reset Value
0x20018	ISPFE_RGGB_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	rggb_start	The starting color of the RGGB image. 00ÿR Gr Gb Bÿ 01ÿGr RB Gbÿ 10ÿGb B R Grÿ 11ÿB Gb Gr Rÿ

ISPFE_CHANNEL_SELECT

ISPFE_CHANNEL_SELECT is the input data channel selection register for the module Video Test Gen and Raw FE.

Offset Address	Register Name	Total Reset Value
0x20020	ISPFE_CHANNEL_SELECT	0x0000_00E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:6]	RW	channel4_select	The fourth input data selection for the modules Video Test Gen and Raw FE. 00: Input the first data; 01: Input the data of the second channel; 10: Input the data of the third channel; 11: Input the data of the fourth channel.
[5:4]	RW	channel3_select	The third input data selection for the modules Video Test Gen and Raw FE. 00: input the first channel data; 01: input the second channel data; 10: input the third channel data; 11: input the fourth channel data.
[3:2]	RW	channel2_select	The second input data selection of the modules Video Test Gen and Raw FE. 00: Input the first data; 01: Input the second data; 10: Input the third data; 11: Input the fourth channel data.
[1:0]	RW	channel1_select	The first input data selection of the modules Video Test Gen and Raw FE. 00: Input the first channel data; 01: Input the second channel data; 10: Input the third data; 11: Input the fourth channel data.

ISPFE_DELAY_LINE_MEMORY

ISPFE_DELAY_LINE_MEMORY is the module DNR line delay register.

Offset Address	Register Name	Total Reset Value
0x20024	ISPFE_DELAY_LINE_MEMORY	0x0000_0002

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	delay_line_memory_configuration	DNR Memory row delay control register. 00: the maximum number of lines, the shortest line width; 01: 3/4 the maximum number of lines, 4/3 times the shortest line width; 1X: 1/2 the maximum number of lines, 2 times the shortest line width.

ISPFE_FLUSH_HBLANK

ISPFE_FLUSH_HBLANK is the row blanking timing configuration register.

Offset Address	Register Name	Total Reset Value
0x20028	ISPFE_FLUSH_HBLANK	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	flush_hblank
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	flush_hblank	Horizontal row blanking control register for duplicate rows.

ISPFE_FS_CHANNEL_SELECT

ISPFE_FS_CHANNEL_SELECT is WDR input data channel selection.

Offset Address	Register Name	Total Reset Value
0x2002C	ISPFE_FS_CHANNEL_SELECT	0x0000_00E4

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved			
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 1 0 0			

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
data; [7:6]	RW	fs_channel4_select	The fourth input data selection of the module Frame Stitch. 00: Input the first channel data; 01: Input the second channel 10: Input the third channel data; 11: Input the fourth channel data.
data; [5:4]	RW	fs_channel3_select	The third input data selection for the module Frame Stitch. 00: Input the first channel data; 01: Input the second channel 10: Input the third data; 11: Input the fourth channel data.
[3:2]	RW	fs_channel2_select	The second input data selection of the module Frame Stitch. 00: Input the first data; 01: Input the second data; 10: Input the data of the third channel; 11: Input the data of the fourth channel.
data; [1:0]	RW	fs_channel1_select	The first input data selection of the module Frame Stitch. 00: Input the first data; 01: Input the second channel 10: Input the third channel data; 11: Input the fourth channel data.

ISPFE_CONFIG_BUFFER_MODE

ISPFE_CONFIG_BUFFER_MODE is the configuration update mode register.

Offset Address	Register Name	Total Reset Value
0x20030	ISPFE_CONFIG_BUFFER_MODE	0x0000_0000

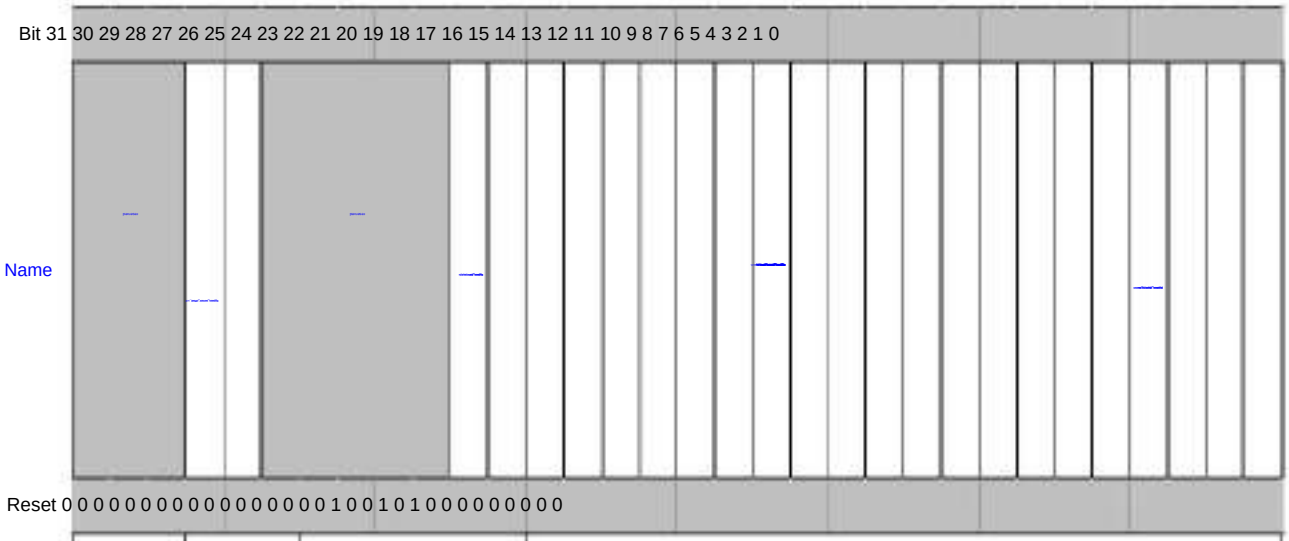
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	immediately; config_buffer_mod It is	ISP FE double buffer mode selection configuration. 00: Close the double buffer mode, the configuration is updated 01: Prevent the configuration update, so that the configuration is never updated; 10: Module configuration is updated in the vertical blanking area of each module; 11: All module configurations are updated in the global vertical blanking area of ISP FE.

ISPFE_MODULE_BYPASS

ISPFE_MODULE_BYPASS is the BYPASS register of the ISP FE module.

Offset Address	Register Name	Total Reset Value
0x20040	ISPFE_MODULE_BYPASS	0x0000_4A00



Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28]	RW	Bypass_sensor_offs et_wdr	configured as 1 to bypass the Sensor offset before the module RAW frontend.
[27]	RW	Bypass_sensor_offs And	configured as 1 to bypass the Sensor offset before the module Frontend lookup.
[26:22]	RO	reserved	reserve.
[21]	RW	bypass_gamma_rgb	is set to 1 to bypass the module RGB gamma LUT.
[20]	RW	Bypass_color_matri x	configured as 1 to bypass the module Color matrix.
[19]	RW	bypass_demosaic	is configured as 1 to bypass the module Demosaic (output RAW data).
[18]	RW	bypass_drc	is configured as 1 to bypass the module DRC.
[17]	RW	bypass_mesh_shadi ng	configured as 1 to bypass the Mesh Shading module.
[16]	RW	Bypass_radial_shad ing	configured as 1 to bypass the module Radial Shading.
[15]	RW	Bypass_white_bala up	configured as 1 to bypass the module Static white balance.
[14]	RW	Bypass_gamma_be _dl	is configured as 1 to bypass the Back end gamma block.
[13]	RW	bypass_gamma_be	is configured as 1 to bypass the Back end gamma LUTs of the module.
[12]	RW	bypass_dnr	is configured as 1 to bypass the module DNR.

[11] RW		Bypass_fs_channel is _switch	configured as 1 to bypass the module Frame stitch channel switch.
[10] RW bypass_digital_gain is configured as 1 to bypass the module Digital gain.			
[9] RW		bypass_gamma_fe_ is dl	configured as 1 to bypass the front end gamma block of the module.
[8] RW bypass_gamma_fe is configured as 1 to bypass the module front end gamma LUTs.			
[7] RW		Bypass_frame_stitc is	configured as 1 to bypass the frame stitching logic of the module. h
[6] RW		Bypass_defect_pixel is	configured as 1 to bypass the module static defect pixel. l
[5] RW		and bypass_raw_front nd	Set it to 1 to bypass the module RAW frontend (green equalization dynamic defect pixel).
[4] RW		bypass_video_test_ is gene	configured as 1 to bypass the video test generator module. the
[3] RW		bypass_channel_sw is itch	configured as 1 to bypass the module channel switch.
[2] RW		bypass_input_form is again	configured as 1 to bypass the module input formatter.
[1] RW		register. position_digital_gai n	Digital gain position selection 0: behind the module FE gamma LUTs; 1: in front of the module FE gamma LUTs.
stitching; [0] RW position_gamma_fe 1:			Block Gamma_fe\Digital Gain Position Selection Register. 0: Behind WDR In front of ISP FE.

ISPFE_BYPASS_MODE

ISPFE_BYPASS_MODE is the ISP FE Bypass mode selection register.

Offset Address	Register Name	Total Reset Value
0x20044	ISPFE_BYPASS_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	isp_raw_bypass	Used to switch between normal mode and RGB\YUV422 input mode, when it is In RGB\YUV422 input mode, the data will be directly inserted behind the demosaic module, and the modules Crop, Scaling, Gamma, and color space conversion are only valid when RGB is input. 0: normal mode; 1: Bypass the ISP RAW processing module.
[8:0]	RO	reserved	reserve.

ISPFE_AE_SWITCH

ISPFE_AE_SWITCH is the AE statistics location control register.

Offset Address	Register Name	Total Reset Value
0x20048	ISPFE_AE_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.

[17:16] RW	ae_sum_switch		AE SUM statistics location selection register. 00: after static white balance; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.
[15:2] RO		reserved	reserve.
[1:0] RW	ae_switch		AE statistics location selection register. 00: after static white balance; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.

ISPFE_AWB_SWITCH

ISPFE_AWB_SWITCH is the position control register of the RGB domain AWB statistics module.

Offset Address	Register Name	Total Reset Value
0x2004C	ISPFE_AWB_SWITCH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	awb_switch	RGB domain AWB statistics module position selection register. 0: Before the color Matrix; 1: After the color Matrix.

ISPFE_HISTOGRAM_SWITCH

ISPFE_HISTOGRAM_SWITCH is the AE global histogram position control register.

Offset Address	Register Name	Total Reset Value
0x20050	ISPFE_HISTOGRAM_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	histogram_switch	AE global histogram position selection register. 00: at the same position as AE; 01: after video test gen (channel 1); 10: after shading; 11: after WDR Frame Stitch.

ISPFE_HISTOGRAM_PE_SWITCH

ISPFE_HISTOGRAM_PE_SWITCH is the Per exposure AE global histogram control register.

Offset Address	Register Name	Total Reset Value
0x20058	ISPFE_HISTOGRAM_PE_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.

[0] RW		exposure. 1: histogram_pe disable.	Enable AE global histogram for each _swit 0: enable (channels 2, 3, 4 after video test gen); ch

ISPFE_GLOBAL_FSM_RESET

ISPFE_GLOBAL_FSM_RESET is the state machine reset register.

Offset Address	Register Name	Total Reset Value
0x20078	ISPFE_GLOBAL_FSM_RESET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	global_fsm_reset	FSM synchronous reset signal.

ISPFE_FIELD_STATUS

ISPFE_FIELD_STATUS is the field signal status register.

Offset Address	Register Name	Total Reset Value
0x2007C	ISPFE_FIELD_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	field_status	field signal status register.

ISPFE_INTERRUPT01

ISPFE_INTERRUPT01 is 0, 1 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x20080	ISPFE_INTERRUPT01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																interrupt1_source						reserved								interrupt0_source						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt1_source	Interrupt source 1 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt0_source	Interrupt source 0 selection.

ISPFE_INTERRUPT23

ISPFE_INTERRUPT23 is 2, 3 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x20084	ISPFE_INTERRUPT23	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt3_source reserved interrupt2_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt3_source	Interrupt source 3 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt2_source	Interrupt source 2 selection.

ISPFE_INTERRUPT45

ISPFE_INTERRUPT45 is 4, 5 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x20088	ISPFE_INTERRUPT45	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt5_source reserved interrupt4_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt5_source	Interrupt source 5 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt4_source	Interrupt source 4 selection.

ISPFE_INTERRUPT67

ISPFE_INTERRUPT67 is the interrupt selection register for 6 and 7.

Offset Address	Register Name	Total Reset Value
0x2008C	ISPFE_INTERRUPT67	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt7_source reserved interrupt6_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt7_source	Interrupt source 7 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt6_source	Interrupt source 6 selection.

ISPFE_INTERRUPT89

ISPFE_INTERRUPT89 is the 8, 9 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x20090	ISPFE_INTERRUPT89	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt9_source reserved interrupt8_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt9_source	Interrupt source 9 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt8_source	Interrupt source 8 selection.

ISPFE_INTERRUPT1011

ISPFE_INTERRUPT1011 is the interrupt selection register for 10 and 11.

Offset Address	Register Name	Total Reset Value
0x20094	ISPFE_INTERRUPT1011	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt11_source reserved interrupt10_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt11_source	Interrupt source 11 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt10_source	Interrupt source 10 selection.

ISPFE_INTERRUPT1213

ISPFE_INTERRUPT1213 is the 12, 13 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x20098	ISPFE_INTERRUPT1213	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt13_source reserved interrupt12_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt13_source	Interrupt source 13 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt12_source	Interrupt source 12 selection.

ISPFE_INTERRUPT1415

ISPFE_INTERRUPT1415 is the 14, 15 interrupt selection register.

Offset Address	Register Name	Total Reset Value
0x2009C	ISPFE_INTERRUPT1415	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt15_source reserved interrupt14_source
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	reserve.
[21:16]	RW	interrupt15_source	Interrupt source 15 selection.
[15:6]	RO	reserved	reserve.
[5:0]	RW	interrupt14_source	Interrupt source 14 selection.

ISPFE_INTERRUPT_STATUS

ISPFE_INTERRUPT_STATUS is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x200A0	ISPFE_INTERRUPT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt_status
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	interrupt_status	Interrupt event flag register.

ISPFE_INTERRUPT_CLEAR

ISPFE_INTERRUPT_CLEAR is to clear the interrupt register.

Offset Address	Register Name	Total Reset Value
0x200A4	ISPFE_INTERRUPT_CLEAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	interrupt_clear
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	interrupt_clear	Interrupt event clear register, first write 0 to a certain bit and then write 1 to clear the interrupt of the corresponding bit.

SENSOR_OFFSET_WDR_1_BLACK00

SENSOR_OFFSET_WDR_1_BLACK00 is the black level value register of WDR_1 BLC R component.

Offset Address	Register Name	Total Reset Value
0x200C0	SENSOR_OFFSET_WDR_1_BLACK00	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved black00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black00	Black level offset for color channel 00 (R).

SENSOR_OFFSET_WDR_1_BLACK01

SENSOR_OFFSET_WDR_1_BLACK01 is the black level value register of WDR_1 BLC Gr component.

Offset Address	Register Name	Total Reset Value
0x200C4	SENSOR_OFFSET_WDR_1_BLACK01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved black01
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black01	Black level offset for color channel 01 (Gr).

SENSOR_OFFSET_WDR_1_BLACK10

SENSOR_OFFSET_WDR_1_BLACK10 is WDR_1 BLC Gb component black level value register.

Offset Address	Register Name	Total Reset Value
0x200C8	SENSOR_OFFSET_WDR_1_BLACK10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / black10
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black10	Black level offset for color channel 10 (Gb).

SENSOR_OFFSET_WDR_1_BLACK11

SENSOR_OFFSET_WDR_1_BLACK11 is the black level value register of WDR_1 BLC B component.

Offset Address	Register Name	Total Reset Value
0x200CC	SENSOR_OFFSET_WDR_1_BLACK11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / black11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black11	Black level offset for color channel 11 (B).

SENSOR_OFFSET_WDR_2_BLACK00

SENSOR_OFFSET_WDR_2_BLACK00 is the black level value register of WDR_2 BLC R component.

Offset Address	Register Name	Total Reset Value
0x200D0	SENSOR_OFFSET_WDR_2_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								black00							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black00	Black level offset for color channel 00 (R).

SENSOR_OFFSET_WDR_2_BLACK01

SENSOR_OFFSET_WDR_2_BLACK01 is the black level value register of WDR_2 BLC Gr component.

Offset Address	Register Name	Total Reset Value
0x200D4	SENSOR_OFFSET_WDR_2_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								black01							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black01	Black level offset for color channel 01 (Gr).

SENSOR_OFFSET_WDR_2_BLACK10

SENSOR_OFFSET_WDR_2_BLACK10 is WDR_2 BLC Gb component black level value register.

Offset Address	Register Name	Total Reset Value
0x200D8	SENSOR_OFFSET_WDR_2_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								black10							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black10	Black level offset for color channel 10 (Gb).

SENSOR_OFFSET_WDR_2_BLACK11

SENSOR_OFFSET_WDR_2_BLACK11 is the black level value register of WDR_2 BLC B component.

Offset Address	Register Name	Total Reset Value
0x200DC	SENSOR_OFFSET_WDR_2_BLACK11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	black11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black11	Black level offset for color channel 11 (B).

SENSOR_OFFSET_WDR_3_BLACK00

SENSOR_OFFSET_WDR_3_BLACK00 is the black level value register of WDR_3 BLC R component.

Offset Address	Register Name	Total Reset Value
0x200E0	SENSOR_OFFSET_WDR_3_BLACK00	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	black00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black00	Black level offset for color channel 00 (R).

SENSOR_OFFSET_WDR_3_BLACK01

SENSOR_OFFSET_WDR_3_BLACK01 is the black level value register of WDR_3 BLC Gr component.

Offset Address	Register Name	Total Reset Value
0x200E4	SENSOR_OFFSET_WDR_3_BLACK01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black01
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black01	Black level offset for color channel 01 (Gr).

SENSOR_OFFSET_WDR_3_BLACK10

SENSOR_OFFSET_WDR_3_BLACK10 is WDR_3 BLC Gb component black level value register.

Offset Address	Register Name	Total Reset Value
0x200E8	SENSOR_OFFSET_WDR_3_BLACK10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black10
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black10	Black level offset for color channel 10 (Gb).

SENSOR_OFFSET_WDR_3_BLACK11

SENSOR_OFFSET_WDR_3_BLACK11 is the black level value register of WDR_3 BLC B component.

Offset Address	Register Name	Total Reset Value
0x200EC	SENSOR_OFFSET_WDR_3_BLACK11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black11	Black level offset for color channel 11 (B).

SENSOR_OFFSET_WDR_4_BLACK00

SENSOR_OFFSET_WDR_4_BLACK00 is the black level value register of WDR_4 BLC R component.

Offset Address	Register Name	Total Reset Value
0x200F0	SENSOR_OFFSET_WDR_4_BLACK00	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black00	Black level offset for color channel 00 (R).

SENSOR_OFFSET_WDR_4_BLACK01

SENSOR_OFFSET_WDR_4_BLACK01 is the black level value register of WDR_4 BLC Gr component.

Offset Address	Register Name	Total Reset Value
0x200F4	SENSOR_OFFSET_WDR_4_BLACK01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black01
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black01	Black level offset for color channel 01 (Gr).

SENSOR_OFFSET_WDR_4_BLACK10

SENSOR_OFFSET_WDR_4_BLACK10 is WDR_4 BLC Gb component black level value register.

Offset Address	Register Name	Total Reset Value
0x200F8	SENSOR_OFFSET_WDR_4_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						black10									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black10	Black level offset for color channel 10 (Gb).

SENSOR_OFFSET_WDR_4_BLACK11

SENSOR_OFFSET_WDR_4_BLACK11 is the black level value register of WDR_4 BLC B component.

Offset Address	Register Name	Total Reset Value
0x200FC	SENSOR_OFFSET_WDR_4_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						black11									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black11	Black level offset for color channel 11 (B).

INPUTPORT_HC_LIMIT

INPUTPORT_HC_LIMIT is the configuration register for Inputport horizontal count limit.

Offset Address	Register Name	Total Reset Value
0x20108	INPUTPORT_HC_LIMIT	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hc_limit															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hc_limit	Horizontal count limit values (example: 0, 1, ... hc_limit-1, hc_limit, 0, 1, ...).

INPUTPORT_HC_START0

INPUTPORT_HC_START0 is Inputport horizontal start register 0.

Offset Address	Register Name	Total Reset Value
0x2010C	INPUTPORT_HC_START0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												hcstart0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hcstart0	ACL gate signal window 0 start value.

INPUTPORT_HC_SIZE0

INPUTPORT_HC_SIZE0 is Inputport horizontal size register 0.

Offset Address	Register Name	Total Reset Value
0x20110	INPUTPORT_HC_SIZE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												hcsize0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hcsize0	ACL gating window 0 size.

INPUTPORT_HC_START1

INPUTPORT_HC_START1 is Inputport horizontal start register 1.

Offset Address	Register Name	Total Reset Value
0x20114	INPUTPORT_HC_START1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hcstart1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hcstart1	HS Gating window 1 start value.

INPUTPORT_HC_SIZE1

INPUTPORT_HC_SIZE1 is Inputport horizontal size register 1.

Offset Address	Register Name	Total Reset Value
0x20118	INPUTPORT_HC_SIZE1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hcsize1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	hcsize1	HS gating window 1 size.

INPUTPORT_VC_LIMIT

INPUTPORT_VC_LIMIT is Inputport vertical count limit configuration register.

Offset Address	Register Name	Total Reset Value
0x2011C	INPUTPORT_VC_LIMIT	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vclimit
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vclimit	Vertical count limit values (examples: 0, 1, ... vclimit-1, vclimit, 0, 1, ...).

INPUTPORT_VC_START

INPUTPORT_VC_START is the vertical start register of Inputport.

Offset Address	Register Name	Total Reset Value
0x20120	INPUTPORT_VC_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vcstart
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vcstart	ACL gate signal window 2 start value.

INPUTPORT_VC_SIZE

INPUTPORT_VC_SIZE is the vertical size register of Inputport.

Offset Address	Register Name	Total Reset Value
0x20124	INPUTPORT_VC_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vcsize
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	vcsize	ACL gating window 2 size.

INPUTPORT_CTRL

INPUTPORT_CTRL is the input interface control register of Inputport.

Offset Address	Register Name	Total Reset Value
0x20130	INPUTPORT_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved — reserved —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	freezeconfig	Used to freeze input port configuration. 0: normal operation; 1: Keep the last configuration status.
[6:3]	RO	reserved	reserve.
[2:0]	RW	moderequest	Used to start and stop the input port. 000: safety stop; 001: safe start; 010: emergency stop; 011: emergency start; 100: reserved; 101: Safer boot; 110: reserved; 111: reserved.

INPUTPORT_STATUS

INPUTPORT_STATUS is the Inputport status register.

Offset Address	Register Name	Total Reset Value
0x20134	INPUTPORT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RO	modest	Used to monitor input port status. Bit[0]: 1: start; 0: stop. Bit[2:1]: Reserved.

INPUT_FORMATTER_MODE

INPUT_FORMATTER_MODE is the Input Formatter mode control register.

Offset Address	Register Name	Total Reset Value
0x20140	INPUT_FORMATTER_MODE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved		reserved			mode_in
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.

[17:16] RW		input_bitwidth_sele 01ÿ	Input data width selection. 00ÿ12 bitsÿ 14 bitsÿ ct 10ÿ16 bitsÿ 11ÿ20 bitsÿ
[15:11] RO		reserved	reserve.
[10:8] RW	mode_out		Output mode selection. 000: 4-channel data input; 001: 2-channel data linear mapping; 010: 3-channel data linear mapping; 011: 4-channel data linear mapping:; Other: reserved.
[7:5] RO		reserved	reserve.
[4:0] RW	mode_in		input mode.

INPUT_FORMATTER_FACTORML

INPUT_FORMATTER_FACTORML is the long and medium exposure ratio register of Input Formatter.

Offset Address	Register Name	Total Reset Value
0x20144	INPUT_FORMATTER_FACTORML	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	factorml
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17:0]	RW	factorml	Long and medium exposure ratio, 6.12 fixed point value.

INPUT_FORMATTER_FACTORMS

INPUT_FORMATTER_FACTORMS is the short and medium exposure ratio register of Input Formatter.

Offset Address	Register Name	Total Reset Value
0x20148	INPUT_FORMATTER_FACTORMS	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													factorms		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	factorms	Short and medium exposure ratio, 1.12 fixed point value.

INPUT_FORMATTER_BLACKLEVEL

INPUT_FORMATTER_BLACKLEVEL is the black level register of Input Formatter sensor.

Offset Address	Register Name	Total Reset Value
0x2014C	INPUT_FORMATTER_BLACKLEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													blacklevel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	blacklevel	sensor black level.

INPUT_FORMATTER_KNEEPOINT01

INPUT_FORMATTER_KNEEPOINT01 is the input formatter knee point 0, 1 register.

Offset Address	Register Name	Total Reset Value
0x20150	INPUT_FORMATTER_KNEEPOINT01	0x0580_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kneepoint1																kneepoint0															
Reset	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	kneepoint1	Inflection point 1.
[15:0]	RW	kneepoint0	Knee point 0.

INPUT_FORMATTER_KNEEPOINT2

INPUT_FORMATTER_KNEEPOINT2 is the Input Formatter knee point 2 register.

Offset Address	Register Name	Total Reset Value
0x20154	INPUT_FORMATTER_KNEEPOINT2	0x0000_0881

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	kneepoint2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	kneepoint2	Knee point 2.

INPUT_FORMATTER_SLOPESELECT

INPUT_FORMATTER_SLOPESELECT is the slope register of the Input Formatter compression table.

Offset Address	Register Name	Total Reset Value
0x20158	INPUT_FORMATTER_SLOPESELECT	0x0906_0402

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	slope3select	reserved	slope2select	reserved	slope1select	reserved	slope0select
Reset	0 0 0 0	1 0 0 1	0 0 0 0	0 0 0 1	1 0 0 0	0 0 0 0	1 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	slope3select	Slope 3 of the compression table, 4bit.
[23:20]	RO	reserved	reserve.
[19:16]	RW	slope2select	Slope 2 of the compression table, 4bit.
[15:12]	RO	reserved	reserve.
[11:8]	RW	slope1select	Slope 1 of the compression table, 4bit.
[7:4]	RO	reserved	reserve.
[3:0]	RW	slope0select	The slope of the compressed table is 0, 4bit.

VIDEO_TEST_GEN_CTRL

VIDEO_TEST_GEN_CTRL is the VIDEO_TEST_GEN control register.

Offset Address	Register Name	Total Reset Value
0x20160	VIDEO_TEST_GEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	bayer_rgb_o_sel	BAYER or RGB output format selection. 0ÿBAYERÿ 1ÿRGBÿ
[1]	RW	bayer_rgb_i_sel	BAYER or RGB input format selection. 0ÿBAYERÿ 1ÿRGBÿ
[0]	RW	test_pattern_off_on	TEST PATTERN enable switch. 0: forbidden; 1: enable.

VIDEO_TEST_PATTREN_TYPE

VIDEO_TEST_PATTREN_TYPE is the VIDEO_TEST_GEN pattern type selection register.

Offset Address	Register Name	Total Reset Value
0x20164	VIDEO_TEST_PATTREN_TYPE	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	patterntype
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	patterntype	Mode type selection. 0x00: solid color; 0x01: horizontal gradient; 0x02: vertical gradient; 0x03: vertical bar; 0x04: rectangle; Other: White target on black background.

VIDEO_TEST_R_BACKGND

VIDEO_TEST_R_BACKGND is the background value register of VIDEO_TEST_GEN R component.

Offset Address	Register Name	Total Reset Value
0x20168	VIDEO_TEST_R_BACKGND	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	rbackgnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rbackgnd	16bit R component background value, aligned with MSB.

VIDEO_TEST_G_BACKGND

VIDEO_TEST_G_BACKGND is the background value register of VIDEO_TEST_GENG G component.

Offset Address	Register Name	Total Reset Value
0x2016C	VIDEO_TEST_G_BACKGND	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	gbackgnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	gbackgnd	16bit G component background value, aligned with MSB.

VIDEO_TEST_B_BACKGND

VIDEO_TEST_B_BACKGND is the background value register of VIDEO_TEST_GEN B component.

Offset Address	Register Name	Total Reset Value
0x20170	VIDEO_TEST_B_BACKGND	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	bbackgnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	bbackgnd	16bit B component background value, aligned with MSB.

VIDEO_TEST_R_FOREGND

VIDEO_TEST_R_FOREGND is the foreground value register of VIDEO_TEST_GEN R component.

Offset Address	Register Name	Total Reset Value
0x20174	VIDEO_TEST_R_FOREGND	0x0000_8FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rforegnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rforegnd	16bit R component foreground value, aligned with MSB.

VIDEO_TEST_G_FOREGND

VIDEO_TEST_G_FOREGND is the foreground value register of VIDEO_TEST_GENG G component.

Offset Address	Register Name	Total Reset Value
0x20178	VIDEO_TEST_G_FOREGND	0x0000_8FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	gforegnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	gforegnd	16bit G component foreground value, aligned with MSB.

VIDEO_TEST_B_FOREGND

VIDEO_TEST_B_FOREGND is the foreground value register of VIDEO_TEST_GEN B component.

Offset Address	Register Name	Total Reset Value
0x2017C	VIDEO_TEST_B_FOREGND	0x0000_8FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	bforegnd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	bforegnd	16bit B component foreground value, aligned with MSB.

VIDEO_TEST_RGB_GRADIENT

VIDEO_TEST_RGB_GRADIENT is the first and second channel RGB gradient value register of VIDEO_TEST_GEN.

Offset Address	Register Name	Total Reset Value
0x20180	VIDEO_TEST_RGB_GRADIENT	0x3CAA_3CAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgbgradient2																rgbgradient															
Reset	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	rgbgradient2	RGB gradient increment value of the second channel, the format is unsigned 4.12bit fixed point.
[15:0]	RW	rgbgradient	Incremental value (0~15) per pixel of the RGB gradient of the first channel, the format is unsigned number 4.12bit fixed point.

VIDEO_TEST_RGB_GRADIENT_START

VIDEO_TEST_RGB_GRADIENT_START is the third and fourth channel RGB gradient increment value register of VIDEO_TEST_GEN.

Offset Address	Register Name	Total Reset Value
0x20184	VIDEO_TEST_RGB_GRADIENT_STA RT	0x3CAA_3CAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgbgradient4																rgbgradient3															
Reset	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	rgbgradient4	RGB gradient increment value of the fourth channel, the format is unsigned number 4.12bit fixed point.
[15:0]	RW	rgbgradient3	RGB gradient increment value of the third channel, the format is unsigned 4.12bit fixed point.

VIDEO_TEST_RGB_GRADIENT_START12

VIDEO_TEST_RGB_GRADIENT_START12 is the first and second channel RGB gradient start value register of VIDEO_TEST_GEN.

Offset Address	Register Name	Total Reset Value
0x20188	VIDEO_TEST_RGB_GRADIENT_START12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rgb_gradient_start_2	rgb_gradient_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rgb_gradient_start_2	The second channel RGB gradient start value.
[15:0]	RW	rgb_gradient_start	The first channel RGB gradient 16bit start value, aligned with the used bit width MSB.

VIDEO_TEST_RGB_GRADIENT_START34

VIDEO_TEST_RGB_GRADIENT_START34 is the RGB gradient start value register for the third and fourth channels of VIDEO_TEST_GEN.

Offset Address	Register Name	Total Reset Value
0x2018C	VIDEO_TEST_RGB_GRADIENT_START34	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rgb_gradient_start_4	rgb_gradient_start_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rgb_gradient_start_4	The fourth channel RGB gradient start value.
[15:0]	RW	rgb_gradient_start_3	The third channel RGB gradient start value.

VIDEO_TEST_RECT_TOP

VIDEO_TEST_RECT_TOP is the row number register of the top and bottom of VIDEO_TEST_GEN rectangle.

Offset Address	Register Name	Total Reset Value
0x20190	VIDEO_TEST_RECT_TOP	0x0100_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—							rect_bot									—								rect_top							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:16]	RW	rect_bot	The number of rows at which the bottom of the rectangle is located.
[15:14]	RO	reserved	reserve.
[13:0]	RW	rect_top	The number of rows the top of the rectangle is on.

VIDEO_TEST_RECT_LEFT

VIDEO_TEST_RECT_LEFT is the number of pixels on the left side of the VIDEO_TEST_GEN rectangle.

Offset Address	Register Name	Total Reset Value
0x20194	VIDEO_TEST_RECT_LEFT	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rectleft	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	rectleft	The number of pixels on the left side of the rectangle.

VIDEO_TEST_RECT_RIGHT

VIDEO_TEST_RECT_RIGHT is the number of pixels on the right side of the VIDEO_TEST_GEN rectangle.

Offset Address	Register Name	Total Reset Value
0x20198	VIDEO_TEST_RECT_RIGHT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														right	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	right	The number of pixels on the right side of the rectangle.

SENSOR_OFFSET_BLACK00

SENSOR_OFFSET_BLACK00 is the black level value register of R component.

Offset Address	Register Name	Total Reset Value
0x201A0	SENSOR_OFFSET_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								black00							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black00	Black level offset for color channel 00 (R).

SENSOR_OFFSET_BLACK01

SENSOR_OFFSET_BLACK01 is the register of black level value of Gr component.

Offset Address	Register Name	Total Reset Value
0x201A4	SENSOR_OFFSET_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								black01							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black01	Black level offset for color channel 01 (Gr).

SENSOR_OFFSET_BLACK10

SENSOR_OFFSET_BLACK10 is the register of black level value of Gb component.

Offset Address	Register Name	Total Reset Value
0x201A8	SENSOR_OFFSET_BLACK10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black10
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black10	Black level offset for color channel 10 (Gb).

SENSOR_OFFSET_BLACK11

SENSOR_OFFSET_BLACK11 is the B component black level value register.

Offset Address	Register Name	Total Reset Value
0x201AC	SENSOR_OFFSET_BLACK11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black11	Black level offset for color channel 11 (B).

NP_RAW_FRONTEND1_EXP_THRESH

NP_RAW_FRONTEND1_EXP_THRESH is the NP_RAW_FRONTEND1 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201B0	NP_RAW_FRONTEND1_EXP_THRESH	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	expthresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	expthresh	Threshold for long/short exposure data.

NP_RAW_FRONTEND1_SHORT_RATIO

NP_RAW_FRONTEND1_SHORT_RATIO is the NP_RAW_FRONTEND1 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201B4	NP_RAW_FRONTEND1_SHORT_RATHAT	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	short ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	short ratio	Short exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND1_LONG_RATIO

NP_RAW_FRONTEND1_LONG_RATIO is the NP_RAW_FRONTEND1 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201B8	NP_RAW_FRONTEND1_LONG_RATIO	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / long distance
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	longshot	Long exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND1_OFF

NP_RAW_FRONTEND1_OFF is the noise black level offset register for NP_RAW_FRONTEND1.

Offset Address	Register Name	Total Reset Value
0x201BC	NP_RAW_FRONTEND1_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

NP_RAW_FRONTEND2_EXP_THRESH

NP_RAW_FRONTEND2_EXP_THRESH is the NP_RAW_FRONTEND2 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201C0	NP_RAW_FRONTEND2_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														expthresh	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	expthresh	Threshold for long/short exposure data.

NP_RAW_FRONTEND2_SHORT_RATIO

NP_RAW_FRONTEND2_SHORT_RATIO is the NP_RAW_FRONTEND2 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201C4	NP_RAW_FRONTEND2_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														short ratio	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	short ratio	Short exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND2_LONG_RATIO

NP_RAW_FRONTEND2_LONG_RATIO is the NP_RAW_FRONTEND2 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201C8	NP_RAW_FRONTEND2_LONG_RATIO	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		long distance
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	longshot	Long exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND2_OFF

NP_RAW_FRONTEND2_OFF is the NP_RAW_FRONTEND2 noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x201CC	NP_RAW_FRONTEND2_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

NP_RAW_FRONTEND3_EXP_THRESH

NP_RAW_FRONTEND3_EXP_THRESH is the NP_RAW_FRONTEND3 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201D0	NP_RAW_FRONTEND3_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														expthresh	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	expthresh	Threshold for long/short exposure data.

NP_RAW_FRONTEND3_SHORT_RATIO

NP_RAW_FRONTEND3_SHORT_RATIO is the NP_RAW_FRONTEND3 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201D4	NP_RAW_FRONTEND3_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														short ratio	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	short ratio	Short exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND3_LONG_RATIO

NP_RAW_FRONTEND3_LONG_RATIO is the NP_RAW_FRONTEND3 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201D8	NP_RAW_FRONTEND3_LONG_RATIO	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		long distance
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	longshot	Long exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND3_OFF

NP_RAW_FRONTEND3_OFF is the noise black level offset register for NP_RAW_FRONTEND3.

Offset Address	Register Name	Total Reset Value
0x201DC	NP_RAW_FRONTEND3_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

NP_RAW_FRONTEND4_EXP_THRESH

NP_RAW_FRONTEND4_EXP_THRESH is the NP_RAW_FRONTEND4 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201E0	NP_RAW_FRONTEND4_EXP_THRESH	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	exp_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	exp_thresh	Threshold for long/short exposure data.

NP_RAW_FRONTEND4_SHORT_RATIO

NP_RAW_FRONTEND4_SHORT_RATIO is the NP_RAW_FRONTEND4 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201E4	NP_RAW_FRONTEND4_SHORT_RATHAT	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	short_ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0

Bits	Access Name		Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	short_ratio	Short exposure noise ratio, the format is unsigned 6.2-bit fixed point.

NP_RAW_FRONTEND4_LONG_RATIO

NP_RAW_FRONTEND4_LONG_RATIO is the NP_RAW_FRONTEND4 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201E8	NP_RAW_FRONTEND4_LONG_RATIO	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / long_ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	long_ratio	Long exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_RAW_FRONTEND4_OFF

NP_RAW_FRONTEND4_OFF is the noise black level offset register for NP_RAW_FRONTEND4.

Offset Address	Register Name	Total Reset Value
0x201EC	NP_RAW_FRONTEND4_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

RAW_FRONTEND1_CTRL1

RAW_FRONTEND1_CTRL1 is the control register of RAW_FRONTEND1 module.

Offset Address	Register Name	Total Reset Value
0x20200	RAW_FRONTEND1_CTRL1	0x0000_0000

Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7] RW	bright_disable		Bright spot detection control. 0: open; 1: Off.
[6] RW	dark_disable		Dark spot detection control. 0: open; 1: Off.
[5:4] RO		reserved	reserve.
[3] RW		pixels. show_dynamic_ect_pixel	Displays detected dead def 0: off; 1: open.
[2] RW	dp_enable		Dynamic dead point detection is enabled. 0: off; 1: open.
[1]	RO	reserved	reserve.
[0] RW	ge_enable		Green balance enabled. 0: off; 1: open.

RAW_FRONTEND1_GE_STRENGTH

RAW_FRONTEND1_GE_STRENGTH is the RAW_FRONTEND1 GE strength register.

Offset Address	Register Name	Total Reset Value
0x20204	RAW_FRONTEND1_GE_STRENGTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ge_strength
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ge_strength	Controls the strength of green balance, set during calibration.

RAW_FRONTEND1_DEBUG_SEL

RAW_FRONTEND1_DEBUG_SEL is the RAW_FRONTEND1 debug register.

Offset Address	Register Name	Total Reset Value
0x20208	RAW_FRONTEND1_DEBUG_SEL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	debug_sel
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	debug_sel	Debug select port.

RAW_FRONTEND1_DP_THRESHOLD

RAW_FRONTEND1_DP_THRESHOLD is the dynamic dead point detection threshold register of RAW_FRONTEND1.

Offset Address	Register Name	Total Reset Value
0x2020C	RAW_FRONTEND1_DP_THRESHOLD	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dp_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	dp_threshold	dead point detection threshold.

RAW_FRONTEND1_GE_THRESHOLD

RAW_FRONTEND1_GE_THRESHOLD is the RAW_FRONTEND1 GE threshold register.

Offset Address	Register Name	Total Reset Value
0x20210	RAW_FRONTEND1_GE_THRESHOLD	0x0000_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ge_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ge_threshold	Green equalization threshold.

RAW_FRONTEND1_DP_SLOPE

RAW_FRONTEND1_DP_SLOPE is the RAW_FRONTEND1 HP mask function slope register.

Offset Address	Register Name	Total Reset Value
0x20214	RAW_FRONTEND1_DP_SLOPE	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dp_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.

[11:0] RW	dp_slope		HP Shield function slope.

RAW_FRONTEND1_GE_SLOPE

RAW_FRONTEND1_GE_SLOPE is the slope register for RAW_FRONTEND1 GE mask function.

Offset Address	Register Name	Total Reset Value
0x20218	RAW_FRONTEND1_GE_SLOPE	0x0000_00AA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ge_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0 1 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ge_slope	GE shield function slope.

RAW_FRONTEND1_GE_SENS

RAW_FRONTEND1_GE_SENS is the edge sensitivity control register of RAW_FRONTEND1 GE module.

Offset Address	Register Name	Total Reset Value
0x2021C	RAW_FRONTEND1_GE_SENS	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ge_sens
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ge_sens	Sensitivity control for the green equalization module to edges.

RAW_FRONTEND1_DPDEV_THRESHOLD

RAW_FRONTEND1_DPDEV_THRESHOLD is the control register of RAW_FRONTEND1 dynamic dead pixel correction on edge strength.

Offset Address	Register Name	Total Reset Value
0x20220	RAW_FRONTEND1_DPDEV_THRESHOLD	0x0000_0266

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dpdev_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 0

Bits	Access Name		Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	dpdev_threshold	Dynamic dead pixel correction controls the intensity of edge influence.

RAW_FRONTEND1_LINE_THRESH

RAW_FRONTEND1_LINE_THRESH Directivity control register near edge for RAW_FRONTEND1 dynamic dead pixel correction.

Offset Address	Register Name	Total Reset Value
0x20224	RAW_FRONTEND1_LINE_THRESH	0x0000_0150

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved line_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0 0 0 0

Bits	Access Name		Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	line_thresh	Directional control near the edge for dynamic dead pixel correction.

RAW_FRONTEND1_DP_BLEND

RAW_FRONTEND1_DP_BLEND Control Register 10 for blending between directional and non-directional replacement values for RAW_FRONTEND1 dynamic dead pixel correction.

Offset Address	Register Name	Total Reset Value
0x20228	RAW_FRONTEND1_DP_BLEND	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / dp_blend
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	dp_blend	Fusion control between directional and non-directional replacement values for dynamic dead point correction, where 0x00 means that detected defects are replaced with non-directional replacement values, and 0xFF means detected defects are replaced with directional replacement values.

RAW_FRONTEND1_SIGMA_IN

RAW_FRONTEND1_SIGMA_IN is the RAW_FRONTEND1 artificial noise estimation register.

Offset Address	Register Name	Total Reset Value
0x2022C	RAW_FRONTEND1_SIGMA_IN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / sigma_in
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	sigma_in	Artificial noise estimation.

RAW_FRONTEND1_THRESH_SHORT

RAW_FRONTEND1_THRESH_SHORT is the noise threshold control register for RAW_FRONTEND1 short exposure data.

Offset Address	Register Name	Total Reset Value
0x20230	RAW_FRONTEND1_THRESH_SHORT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / thresh_short
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	thresh_short	Noise threshold of short exposure data, the format is unsigned 4.4-bit floating point type.

RAW_FRONTEND1_THRESH_LONG

RAW_FRONTEND1_THRESH_LONG is the noise threshold control register of RAW_FRONTEND1 long exposure data.

Offset Address	Register Name	Total Reset Value
0x20234	RAW_FRONTEND1_THRESH_LONG	0x0000_0030

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / thresh_long
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	thresh_long	Noise threshold of long exposure data, the format is unsigned 4.4-bit floating point type.

RAW_FRONTEND2_CTRL1

RAW_FRONTEND2_CTRL1 is the RAW_FRONTEND2 module control register 1.

Offset Address	Register Name	Total Reset Value
0x20240	RAW_FRONTEND2_CTRL1	0x0000_0000

Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7] RW	bright_disable		Bright spot detection control. 0: open; 1: Off.
[6] RW	dark_disable		Dark spot detection control. 0: open; 1: Off.
[5:4] RO		reserved	reserve.
[3] RW		pixels. show_dynamic_ect_pixel	Displays detected dead def 0: off; 1: open.
[2] RW	dp_enable		Dynamic dead point detection is enabled. 0: off; 1: open.
[1]	RO	reserved	reserve.
[0] RW	ge_enable		Green balance enabled. 0: off; 1: open.

RAW_FRONTEND2_GE_STRENGTH

RAW_FRONTEND2_GE_STRENGTH is the RAW_FRONTEND2 GE strength register.

Offset Address	Register Name	Total Reset Value
0x20244	RAW_FRONTEND2_GE_STRENGTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ge_strength
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ge_strength	Controls the strength of green balance, set during calibration.

RAW_FRONTEND2_DP_THRESHOLD

RAW_FRONTEND2_DP_THRESHOLD is the dynamic dead point detection threshold register of RAW_FRONTEND2.

Offset Address	Register Name	Total Reset Value
0x2024C	RAW_FRONTEND2_DP_THRESHOLD	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	dp_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	dp_threshold	Dead pixel detection threshold.

RAW_FRONTEND2_GE_THRESHOLD

RAW_FRONTEND2_GE_THRESHOLD is the RAW_FRONTEND2 GE threshold register.

Offset Address	Register Name	Total Reset Value
0x20250	RAW_FRONTEND2_GE_THRESHOLD	0x0000_0400

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ge_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ge_threshold	Green equalization threshold.

RAW_FRONTEND2_DP_SLOPE

RAW_FRONTEND2_DP_SLOPE is the RAW_FRONTEND2 HP mask function slope register.

Offset Address	Register Name	Total Reset Value
0x20254	RAW_FRONTEND2_DP_SLOPE	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dp_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	dp_slope	HP Shield function slope.

RAW_FRONTEND2_GE_SLOPE

RAW_FRONTEND2_GE_SLOPE is the slope register of RAW_FRONTEND2 GE mask function.

Offset Address	Register Name	Total Reset Value
0x20258	RAW_FRONTEND2_GE_SLOPE	0x0000_00AA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ge_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 1 0 1 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ge_slope	GE shield function slope.

RAW_FRONTEND2_GE_SENS

RAW_FRONTEND2_GE_SENS is the edge sensitivity control register of RAW_FRONTEND2 GE module.

Offset Address	Register Name	Total Reset Value
0x2025C	RAW_FRONTEND2_GE_SENS	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved ge_sens
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:8]	RO reserved	reserve.
[7:0]	RW ge_sens	Sensitivity control for the green equalization module to edges.

RAW_FRONTEND2_DPDEV_THRESHOLD

RAW_FRONTEND2_DPDEV_THRESHOLD is the control register of RAW_FRONTEND2 dynamic dead pixel correction on edge strength.

Offset Address	Register Name	Total Reset Value
0x20260	RAW_FRONTEND2_DPDEV_THRESHOLD	0x0000_0266

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dpdev_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 0

Bits	Access Name	Description
[31:12]	RO reserved	reserve.
[11:0]	RW dpdev_threshold	Dynamic dead pixel correction controls the intensity of edge influence.

RAW_FRONTEND2_LINE_THRESH

RAW_FRONTEND2_LINE_THRESH Directivity control register near edge for RAW_FRONTEND2 dynamic dead pixel correction.

Offset Address	Register Name	Total Reset Value
0x20264	RAW_FRONTEND2_LINE_THRESH	0x0000_0150

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	line_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 0 1 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	line_thresh	Directional control near the edge for dynamic dead pixel correction.

RAW_FRONTEND2_DP_BLEND

RAW_FRONTEND2_DP_BLEND Control Register 10 for blending between directional and non-directional replacement values for RAW_FRONTEND2 dynamic dead pixel correction.

Offset Address	Register Name	Total Reset Value
0x20268	RAW_FRONTEND2_DP_BLEND	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	dp_blend
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	dp_blend	Fusion control between directional and non-directional replacement values for dynamic dead pixel correction. Where 0x00 indicates that the detected defect is replaced with a non-directional replacement value, and 0xFF indicates that the detected defect is replaced with a directional replacement value.

RAW_FRONTEND2_SIGMA_IN

RAW_FRONTEND2_SIGMA_IN is the RAW_FRONTEND2 artificial noise estimation register.

Offset Address	Register Name	Total Reset Value
0x2026C	RAW_FRONTEND2_SIGMA_IN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sigma_in
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	sigma_in	Artificial noise estimation.

RAW_FRONTEND2_THRESH_SHORT

RAW_FRONTEND2_THRESH_SHORT is the noise threshold control register for RAW_FRONTEND2 short exposure data.

Offset Address	Register Name	Total Reset Value
0x20270	RAW_FRONTEND2_THRESH_SHORT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	thresh_short
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	thresh_short	Noise threshold of short exposure data, the format is unsigned 4.4-bit floating point type.

RAW_FRONTEND2_THRESH_LONG

RAW_FRONTEND2_THRESH_LONG is the noise threshold control register of RAW_FRONTEND2 long exposure data.

Offset Address	Register Name	Total Reset Value
0x20274	RAW_FRONTEND2_THRESH_LONG	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														thresh_long	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	thresh_long	Noise threshold of long exposure data, the format is unsigned 4.4-bit floating point type.

STATIC_DPC_MULTI_CH_MODE

STATIC_DPC_MULTI_CH_MODE is the 4k/2k mode selection register for STATIC_DPC static dead point correction.

Offset Address	Register Name	Total Reset Value
0x20280	STATIC_DPC_MULTI_CH_MODE	0x0000_0000

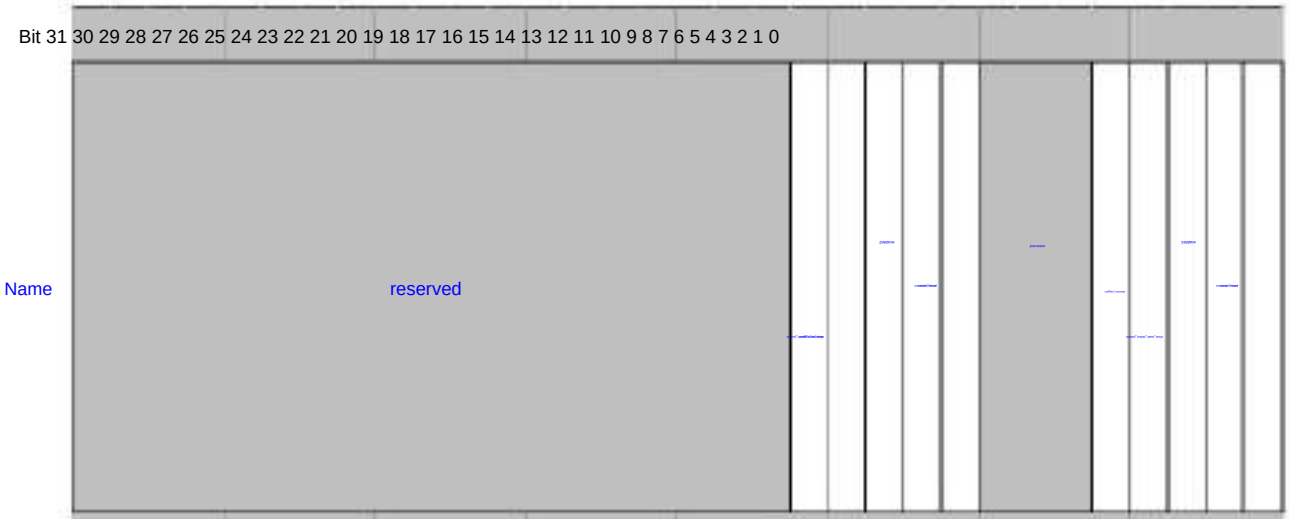
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	multi_ch_mode	4k/2k mode select register. 00: Mode 4ch 4K; 01: Mode 2ch 4K; 10: Mode 2ch 2K; 11: Reserved.

STATIC_DPC_CTRL

STATIC_DPC_CTRL is the Static Defect Pixels module control register.

Offset Address	Register Name	Total Reset Value
0x20284	STATIC_DPC_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	detection_trigger2	Start dead point detection when 0-1 jump edge.
[11]	RW	pixels. show_static_defect _pixels2	Displays pixels detected as dead 0: no display; 1: Display.
[10]	RW	enable2	Dead pixel correction enabled. 0: off; 1: open.
[9]	RW	show_reference2	Show reference value compared with actual value to detect dead pixels.
[8]	RW	pointer_reset2	Reset the bad point table pointer every frame. Set this field when writing bad pixel table from MCU.
[7:5]	RO	reserved	reserve.
[4]	RW	detection_trigger1	Start dead point detection when 0-1 jump edge.
[3]	RW	pixels. show_static_defect _pixels1	Displays pixels detected as dead 0: no display; 1: Display.
[2]	RW	enable1	Dead pixel correction enabled. 0: off; 1: open.

[1] RW	show_reference	1	Displays reference values compared with actual values to detect dead pixels. 0: no display; 1: Display.
[0] RW	pointer_reset	1	Reset the bad point table pointer every frame. Set this field when writing bad pixel table from MCU.

STATIC_DPC_OVERFLOW

STATIC_DPC_OVERFLOW is the overflow flag register of the Static Defect Pixels module table.

Offset Address	Register Name	Total Reset Value
0x20288	STATIC_DPC_OVERFLOW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved — reserved —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8]	RO	overflow2	Table 2 Overflow flags. 0: no overflow; 1: Overflow.
[7:1]	RO	reserved	reserve.
[0]	RO	overflow1	Table 1 Overflow flags. 0: no overflow; 1: Overflow.

STATIC_DPC_COUNT

STATIC_DPC_COUNT is the register for the number of dead pixels detected by the Static Defect Pixels module.

Offset Address	Register Name	Total Reset Value
0x2028C	STATIC_DPC_COUNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	defect_pixel_count2	reserved	defect_pixel_count1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RO	defect_pixel_count	The number of bad pixels detected. 2
[15:12]	RO	reserved	reserve.
[11:0]	RO	defect_pixel_count	The number of bad pixels detected. 1

STATIC_DPC_TABLE_START

STATIC_DPC_TABLE_START is the bad pixel first address register of the Static Defect Pixels module.

Offset Address	Register Name	Total Reset Value
0x20290	STATIC_DPC_TABLE_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	table_start2	reserved	table_start1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RO	table_start2	The address of the first bad point in the bad point table.
[15:12]	RO	reserved	reserve.
[11:0]	RO	table_start1	The address of the first bad point in the bad point table.

STATIC_DPC_COUNT_IN

STATIC_DPC_COUNT_IN is the number of dead pixels written in the Static Defect Pixels module register.

Offset Address	Register Name	Total Reset Value
0x20294	STATIC_DPC_COUNT_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																defect_pixel_count_in2											reserved				defect_pixel_count_in1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	defect_pixel_count_in2	the number of bad pixels in the table.
[15:12]	RO	reserved	reserve.
[11:0]	RW	defect_pixel_count_in1	the number of bad pixels in the table.

WDR_CTRL

WDR_CTRL is the WDR control register.

Offset Address	Register Name	Total Reset Value
0x202A0	WDR_CTRL	0x0F00_C001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				long_short_thresh																reserved											
Reset	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name		Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	long_short_thresh	Data above this threshold will be taken from a shorter exposure range.
[15:13]	RW	rsvd4	Configuration is prohibited.
[12:8]	RO	reserved	reserve.

[7] RW		alpha slope. alpha_slope_from_zero	The starting point for the 0: The starting point of the alpha slope is 1/exposure ratio; 1: The starting point of the alpha slope is 0.
[6] RW	wdr_mode		WDR mode selection. 0: WDR off; 1: Frame switching.
[5] RW	rsvd3		Configuration is prohibited.
[4] RW	enable_np		Configuration is prohibited.
[3]	RO	reserved	reserve.
[2] RW	rsvd2		Configuration is prohibited.
[1] RW	rsvd1		Configuration is prohibited.
[0] RW	rsvd0		Configuration is prohibited.

WDR_LONG_CTRL1

WDR_LONG_CTRL1 is WDR long exposure control register 1.

Offset Address	Register Name	Total Reset Value
0x202A4	WDR_LONG_CTRL1	0x0100_0C00

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	long_exposure_ratio	reserved	long_long_thresh
Reset	0 0 0 0	0 0 0 0 0 0 1 0	0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	long_exposure_rati O	Exposure ratio, the format is unsigned number 6.6bit fixed point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	long_long_thresh	Data below this threshold will be acquired from a longer exposure range.

WDR_LONG_CTRL2

WDR_LONG_CTRL2 is WDR long exposure control register 2.

Offset Address	Register Name	Total Reset Value
0x202A8	WDR_LONG_CTRL2	0x0080_0040

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	long_stitch_correct	reserved	long_stitch_error_thresh
Reset	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	long_stitch_correct	number 1.7-bit fixed The error of the sensor exposure ratio in the fusion area can be adjusted, and the format is unmatched point.
[15:8]	RO	reserved	reserve.
[7:0]	RW	long_stitch_error_t sets	the strength to detect stitching errors due to motion. hresh

WDR_LONG_STITCH_ERROR_LIMIT

WDR_LONG_STITCH_ERROR_LIMIT is the WDR long exposure intensity setting register.

Offset Address	Register Name	Total Reset Value
0x202AC	WDR_LONG_STITCH_ERROR_LIMIT	0x0000_2000

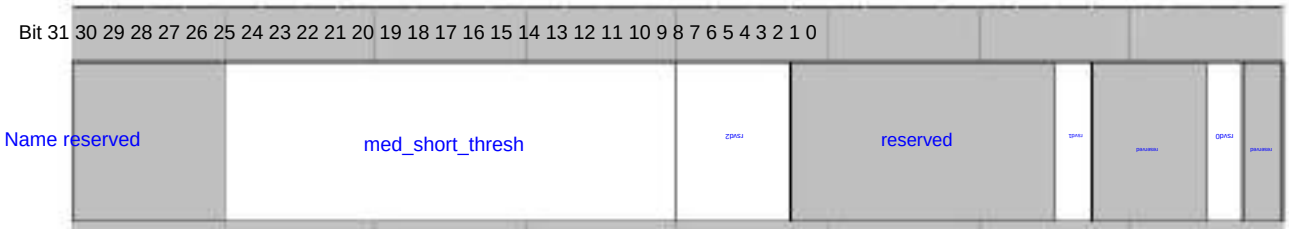
Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			long_stitch_error_limit
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	long_stitch_error_li mit	Long exposure intensity setting, below which stitching error detection will be disabled.

WDR_MED_CTRL1

WDR_MED_CTRL1 is exposure control register 1 in WDR.

Offset Address	Register Name	Total Reset Value
0x202B0	WDR_MED_CTRL1	0x0F00_C000

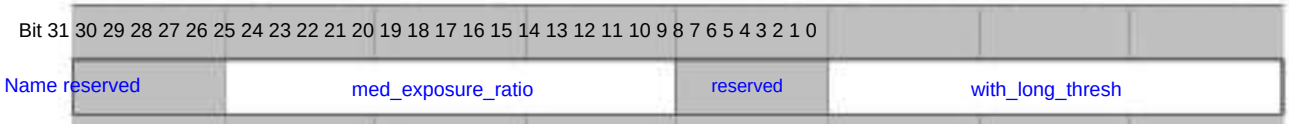


Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	med_short_thresh	Data above this threshold will be taken from a shorter exposure range.
[15:13]	RW	rsvd2	Configuration is prohibited.
[12:6]	RO	reserved	reserve.
[5]	RW	rsvd1	Configuration is prohibited.
[4:2]	RO	reserved	reserve.
[1]	RW	rsvd0	Configuration is prohibited.
[0]	RO	reserved	reserve.

WDR_MED_CTRL2

WDR_MED_CTRL2 is exposure control register 2 in WDR.

Offset Address	Register Name	Total Reset Value
0x202B4	WDR_MED_CTRL2	0x0100_0C00



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	med_exposure_ratio	Exposure ratio, the format is unsigned number 6.6bit fixed point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	med_long_thresh	Data below this threshold will be acquired from a longer exposure range.

WDR_MED_CTRL3

WDR_MED_CTRL3 is exposure control register 3 in WDR.

Offset Address	Register Name	Total Reset Value
0x202B8	WDR_MED_CTRL3	0x0080_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																med_stitch_correct								reserved							med_stitch_error_thresh							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	med_stitch_correct	number 1.7-bit fixed The error of the sensor exposure ratio in the fusion area can be adjusted, and the format is unmatched point.
[15:8]	RO	reserved	reserve.
[7:0]	RW	med_stitch_error_t sets	the strength of detecting stitching errors due to motion. hresh

WDR_MED_STITCH_ERROR_LIMIT

WDR_MED_STITCH_ERROR_LIMIT is the exposure intensity setting in WDR.

Offset Address	Register Name	Total Reset Value
0x202BC	WDR_MED_STITCH_ERROR_LIMIT	0x0000_2000

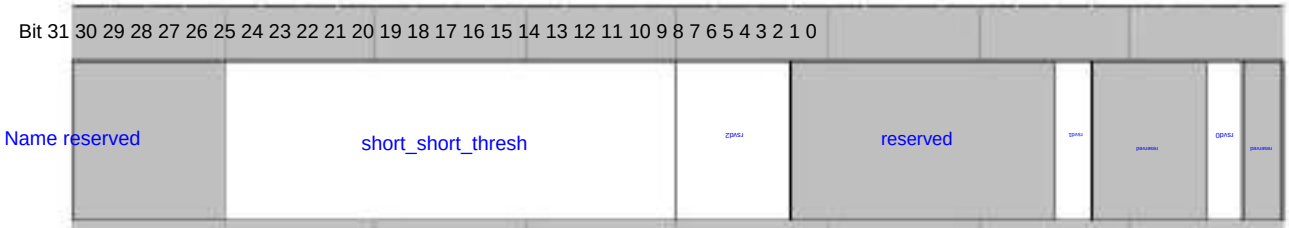
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				med_stitch_error_limit											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	The exposure intensity mit	setting in med_stitch_error_li, below which stitching error detection will be disabled.

WDR_SHORT_CTRL1

WDR_SHORT_CTRL1 is WDR short exposure control register 1.

Offset Address	Register Name	Total Reset Value
0x202C0	WDR_SHORT_CTRL1	0x0F00_C000

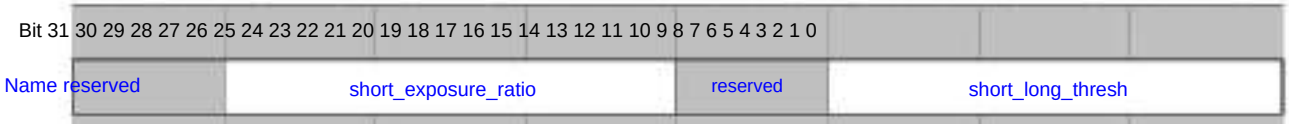


Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	short_short_thresh	Data above this threshold will be taken from a shorter exposure range.
[15:13]	RW	rsvd2	Configuration is prohibited.
[12:6]	RO	reserved	reserve.
[5]	RW	rsvd1	Configuration is prohibited.
[4:2]	RO	reserved	reserve.
[1]	RW	rsvd0	Configuration is prohibited.
[0]	RO	reserved	reserve.

WDR_SHORT_CTRL2

WDR_SHORT_CTRL2 is WDR short exposure control register 2.

Offset Address	Register Name	Total Reset Value
0x202C4	WDR_SHORT_CTRL2	0x0100_0C00



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	short_exposure_ratio	Exposure ratio, the format is unsigned 6.6bit fixed point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	short_long_thresh	Data below this threshold will be acquired from a longer exposure range.

WDR_SHORT_CTRL3

WDR_SHORT_CTRL3 is WDR short exposure control register 3.

Offset Address	Register Name	Total Reset Value
0x202C8	WDR_SHORT_CTRL3	0x0080_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																short_stitch_correct								reserved							short_stitch_error_thresh							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	short_stitch_correct	error adjustable range of sensor exposure ratio in fusion area, format is no match Number 1.7-bit fixed point.
[15:8]	RO	reserved	reserve.
[7:0]	RW	short_stitch_error_t sets	the strength to detect stitching errors due to motion. hresh

WDR_SHORT_STITCH_ERROR_LIMIT

WDR_SHORT_STITCH_ERROR_LIMIT is the WDR short exposure intensity setting register.

Offset Address	Register Name	Total Reset Value
0x202CC	WDR_SHORT_STITCH_ERROR_LIMIT	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				short_stitch_error_limit											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	short_stitch_error_l Short imit	exposure intensity setting, below which stitching error detection will be disabled.

WDR_BLACK_LEVEL_LONG

WDR_BLACK_LEVEL_LONG is the black level register for WDR long exposure input.

Offset Address	Register Name	Total Reset Value
0x202D0	WDR_BLACK_LEVEL_LONG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black_level_long
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black_level_long	Black level of long exposure input.

WDR_BLACK_LEVEL_MEDIUM1

WDR_BLACK_LEVEL_MEDIUM1 is black level register 1 of exposure input in WDR.

Offset Address	Register Name	Total Reset Value
0x202D4	WDR_BLACK_LEVEL_MEDIUM1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black_level_medium1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	The black level of the m1	exposure input in black_level_mediu.

WDR_BLACK_LEVEL_MEDIUM2

WDR_BLACK_LEVEL_MEDIUM2 is black level register 2 of exposure input in WDR.

Offset Address	Register Name	Total Reset Value
0x202D8	WDR_BLACK_LEVEL_MEDIUM2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black_level_medium2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.

[11:0] RW		The black level of the exposure input in black_level_mediu m2	

WDR_BLACK_LEVEL_SHORT

WDR_BLACK_LEVEL_SHORT is the black level register for WDR short exposure input.

Offset Address	Register Name	Total Reset Value
0x202DC	WDR_BLACK_LEVEL_SHORT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / black_level_short
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	black_level_short	Black level for short exposure input.

WDR_BLACK_LEVEL_OUT

WDR_BLACK_LEVEL_OUT is the black level register output by WDR module.

Offset Address	Register Name	Total Reset Value
0x202E0	WDR_BLACK_LEVEL_OUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / black_level_out
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black_level_out	Black level output by the block.

WDR_MODE_IN

WDR_MODE_IN is the WDR input mode selection register.

Offset Address	Register Name	Total Reset Value
0x202E4	WDR_MODE_IN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	mode_in	WDR input mode selection. 00ÿ4 channelÿ 01ÿ2 channelÿ 10ÿ3 channelÿ 11ÿ4 channelÿ

FRONTEND_LUT_CTRL

FRONTEND_LUT_CTRL is the FRONTEND_LUT control register.

Offset Address	Register Name	Total Reset Value
0x20300	FRONTEND_LUT_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	mcu_priority	CPU port priority. 0: low; 1: High.
[30:14]	RO	reserved	reserve.
[13]	RW	bank_select_1	Lookup table 1 valid mem bank switch.
[12]	RW	bank_select_0	Lookup table 0 active mem bank switch.

[11:10] RO		reserved	reserve.
[9] RW	offset_mode_1		Lookup Table 1 Black Level Offset Region Mapping Mode. 0: manual curve mapping; 1: Automatic curve mapping.
[8] RW	offset_mode_0		Lookup Table 0 Black Level Offset Region Mapping Mode. 0: manual curve mapping; 1: automatic curve mapping.
[7:3] RO		reserved	reserve.
[2] RW	enable_dl		Frontend Lookup Table DL Enable Register. 0: forbidden; 1: enable.
[1] RW	enable1		Frontend Lookup Table 1 Enable Register. 0: disable; 1: enable.
[0] RW	enable0		Frontend Lookup Table 0 Enable Register. 0: forbidden; 1: enable.

FRONTEND_LUT_MCU_READY

FRONTEND_LUT_MCU_READY is the status indication of FRONTEND_LUT.

Offset Address	Register Name	Total Reset Value
0x20304	FRONTEND_LUT_MCU_READY	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RO	mcu_ready_1	LUT1 status indicator, when it is 1, it means that LUT1 is ready to receive data from CPU.

[0]	RO	mcu_ready_0	LUT0 status indicator, when it is 1, it means that LUT0 is ready to receive data from CPU.

FRONTEND_LUT_ALPHA

FRONTEND_LUT_ALPHA is the FRONTEND_LUT alpha parameter register.

Offset Address	Register Name	Total Reset Value
0x20308	FRONTEND_LUT_ALPHA	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:18]	RO	reserved	reserve.
[17:0]	RW	alpha	Front end alpha parameter, 6.12 Fixed point.

DG_GAIN

DG_GAIN is sensor digital gain.

Offset Address	Register Name	Total Reset Value
0x20310	DG_GAIN	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	gain
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:13]	RO	reserved	reserve.
[12:0]	RW	gain	sensor digital gain, the format is 5.8 unsigned number.

DG_OFFSET

DG_OFFSET is DG black level compensation.

Offset Address	Register Name	Total Reset Value
0x20314	DG_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	offset	Black level compensation.

DNR_CTRL

DNR_CTRL is the DNR control register.

Offset Address	Register Name	Total Reset Value
0x20320	DNR_CTRL	0x0000_041C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / int_config / rsvd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:8]	RW	int_config	Intensity blend with untreated mosaic.
[7]	RW	rm_enable	Lens shading correction enabled. 0: forbidden; 1: enable.
[6]	RW	int_select	Intensity filter selection. 0: forbidden; 1: enable.
[5]	RW	filter_select	Denoising filter fine-tuning. 0: forbidden; 1: enable.

[4] RW	enable		Noise reduction enabled. 0: forbidden; 1: enable.
[3:0] RW	rsvd		Configuration is prohibited.

DNR_RM_CENTER_X

DNR_RM_CENTER_X is the abscissa register of DNR shadow map.

Offset Address	Register Name	Total Reset Value
0x20324	DNR_RM_CENTER_X	0x0000_0280

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rm_center_x
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rm_center_x	Abscissa of the shadow map.

DNR_RM_CENTER_Y

DNR_RM_CENTER_Y is the ordinate register of DNR shadow map.

Offset Address	Register Name	Total Reset Value
0x20328	DNR_RM_CENTER_Y	0x0000_0168

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rm_center_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 1 0 1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rm_center_y	Vertical coordinate of the shadow map.

DNR_RM_OFF_CENTER_MULT

DNR_RM_OFF_CENTER_MULT is the DNR normalization factor register.

Offset Address	Register Name	Total Reset Value
0x2032C	DNR_RM_OFF_CENTER_MULT	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rm_off_center_mult
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	method is rm_off_center_mul of the image.	Normalization factor, extending the radial table to the edge of the image, the calculation 2^31/R^2, where R represents the furthest t distance from the center coordinates to the edge pixels

DNR_THRESH_H01

DNR_THRESH_H01 is the noise threshold register at high frequency in DNR horizontal space.

Offset Address	Register Name	Total Reset Value
0x20330	DNR_THRESH_H01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	thresh_1h reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	thresh_1h	Noise threshold at high frequencies in the horizontal airspace.
[15:0]	RO	reserved	reserve.

DNR_THRESH_H24

DNR_THRESH_H24 is the noise threshold register at low frequency in DNR horizontal space.

Offset Address	Register Name	Total Reset Value
0x20334	DNR_THRESH_H24	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	thresh_4h	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	thresh_4h	Noise threshold at low frequencies in horizontal airspace.
[15:0]	RO	reserved	reserve.

DNR_THRESH_V01

DNR_THRESH_V01 is the noise threshold register at high frequency in DNR vertical space.

Offset Address	Register Name	Total Reset Value
0x20338	DNR_THRESH_V01	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	thresh_1v	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	thresh_1v	Noise threshold at high frequencies in the vertical airspace.
[15:0]	RO	reserved	reserve.

DNR_THRESH_V24

DNR_THRESH_V24 is the noise threshold register at low frequency in DNR vertical space.

Offset Address	Register Name	Total Reset Value
0x2033C	DNR_THRESH_V24	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	thresh_4v	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	thresh_4v	Noise threshold at low frequencies in the vertical airspace.
[15:0]	RO	reserved	reserve.

DNR_THRESH_SHORT

DNR_THRESH_SHORT is the noise threshold adjustment register for DNR short exposure data.

Offset Address	Register Name	Total Reset Value
0x20344	DNR_THRESH_SHORT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	thresh_short
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	thresh_short	Noise threshold adjustment for short exposure data.

DNR_THRESH_LONG

DNR_THRESH_LONG is the noise threshold adjustment register for DNR long exposure data.

Offset Address	Register Name	Total Reset Value
0x20348	DNR_THRESH_LONG	0x0000_0030

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	thresh_long
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.

[7:0]	RW	thresh_long	Noise threshold adjustment for long exposure data.

DNR_STRENGTH1

DNR_STRENGTH1 is the noise suppression effect register for DNR high spatial frequency.

Offset Address	Register Name	Total Reset Value
0x20350	DNR_STRENGTH1	0x0000_00FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	strength_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	strength_1	Noise suppression effect at high spatial frequencies.

DNR_STRENGTH4

DNR_STRENGTH4 is the noise suppression effect register for DNR low spatial frequency.

Offset Address	Register Name	Total Reset Value
0x20358	DNR_STRENGTH4	0x0000_00FF

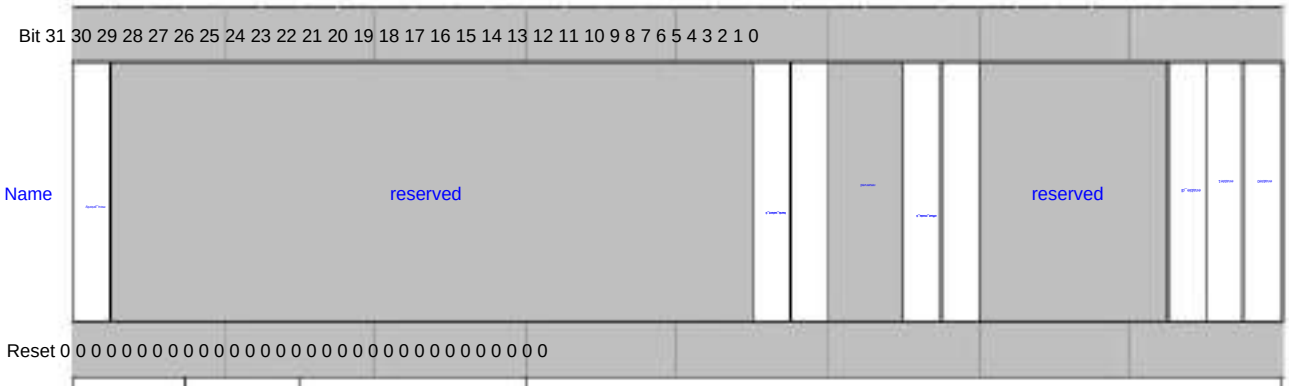
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	strength_4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	strength_4	Noise suppression effect at low spatial frequencies.

BACKEND_LUT_CRTL

BACKEND_LUT_CRTL is the BACKEND_LUT control register.

Offset Address	Register Name	Total Reset Value
0x20360	BACKEND_LUT_CRTL	0x0000_0000



Bits	Access Name		Description
[31] RW	mcu_priority		CPU port priority. 0: low; 1: High.
[30:14] RO		reserved	reserve.
[13] RW	bank_select_1		Lookup table 1 mem bank switching. 0: select mem bank0; 1: Select mem bank1.
[12] RW	bank_select_0		Lookup table 0 mem bank switching. 0: select mem bank0; 1: Select mem bank1.
[11:10] RO		reserved	reserve.
[9] RW	offset_mode_1		Lookup Table 1 Black Level Offset Region Mapping Mode. 0: manual curve mapping; 1: Automatic curve mapping.
[8] RW	offset_mode_0		Lookup Table 0 Black Level Offset Region Mapping Mode. 0: manual curve mapping; 1: Automatic curve mapping.
[7:3] RO		reserved	reserve.
[2] RW	enable_dl		Backend Lookup Table DL Enable Register. 0: forbidden; 1: enable.
[1] RW	enable1		Backend Lookup Table 1 Enable Register. 0: forbidden; 1: enable.

[0] RW	enable	0	Backend Lookup Table 0 Enable Register. 0: forbidden; 1: enable.

BACKEND_LUT_MCU_READY

BACKEND_LUT_MCU_READY is the status indication of BACKEND_LUT.

Offset Address	Register Name	Total Reset Value
0x20364	BACKEND_LUT_MCU_READY	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RO	mcu_ready_1	LUT1 status indicator, when it is 1, it means that LUT1 is ready to receive data from CPU.
[0]	RO	mcu_ready_0	LUT0 status indicator, when it is 1, it means that LUT0 is ready to receive data from CPU.

BACKEND_LUT_ALPHA

BACKEND_LUT_ALPHA is the BACKEND_LUT alpha parameter register.

Offset Address	Register Name	Total Reset Value
0x20368	BACKEND_LUT_ALPHA	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved alpha
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17:0]	RW	alpha	Front end alpha parameter, 6.12 Fixed point.

NP_FOR_DNR_EXP_THRESH

NP_FOR_DNR_EXP_THRESH is the NP_FOR_DNR_noise threshold register.

Offset Address	Register Name	Total Reset Value
0x20370	NP_FOR_DNR_EXP_THRESH	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	exp_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	exp_thresh	Threshold for long/short exposure data.

NP_FOR_DNR_SHORT_RATIO

NP_FOR_DNR_SHORT_RATIO is the NP_FOR_DNR_ noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x20374	NP_FOR_DNR_SHORT_RATIO	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	short_ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	short_ratio	Short exposure noise ratio, the format is unsigned 6.2-bit fixed point.

NP_FOR_DNR_LONG_RATIO

NP_FOR_DNR_LONG_RATIO is the NP_FOR_DNR_noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x20378	NP_FOR_DNR_LONG_RATIO	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		long_ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	long_ratio	Long exposure noise ratio in unsigned 6.2-bit fixed-point format.

NP_FOR_DNR_OFF

NP_FOR_DNR_OFF is the NP_FOR_DNR_noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x2037C	NP_FOR_DNR_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

WB_GAIN00

WB_GAIN00 is the R component gain register of the White Balance module.

Offset Address	Register Name	Total Reset Value
0x20380	WB_GAIN00	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														gain00	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	gain00	The multiple of color channel R, the format is unsigned number, 4.8 bits, fixed point.

WB_GAIN01

WB_GAIN01 is the Gr component gain register of the White Balance module.

Offset Address	Register Name	Total Reset Value
0x20384	WB_GAIN01	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														gain01	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	gain01	The multiple of the color channel Gr, the format is an unsigned number, 4.8 bits, fixed point.

WB_GAIN10

WB_GAIN10 is the Gb component gain register of the White Balance module.

Offset Address	Register Name	Total Reset Value
0x20388	WB_GAIN10	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														gain10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	gain10	The multiple of color channel Gb, the format is unsigned number, 4.8 bits, fixed point.

WB_GAIN11

WB_GAIN11 is the B component gain register of the White Balance module.

Offset Address	Register Name	Total Reset Value
0x2038C	WB_GAIN11	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	gain11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	gain11	Multiple of color channel B in unsigned, 4.8-bit, fixed-point format.

BLC_BLACK00

BLC_BLACK00 is the black level offset value of BLC R component.

Offset Address	Register Name	Total Reset Value
0x203A0	BLC_BLACK00	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black00	Black level offset for color channel R.

BLC_BLACK01

BLC_BLACK01 is the black level offset value of BLC Gr component.

Offset Address	Register Name	Total Reset Value
0x203A4	BLC_BLACK01	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black01
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black01	Black level offset for color channel Gr.

BLC_BLACK10

BLC_BLACK10 is the black level offset value of BLC Gb component.

Offset Address	Register Name	Total Reset Value
0x203A8	BLC_BLACK10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black10
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black10	Black level offset for color channel Gb.

BLC_BLACK11

BLC_BLACK11 is the black level offset value of BLC B component.

Offset Address	Register Name	Total Reset Value
0x203AC	BLC_BLACK11	0x0000_0000

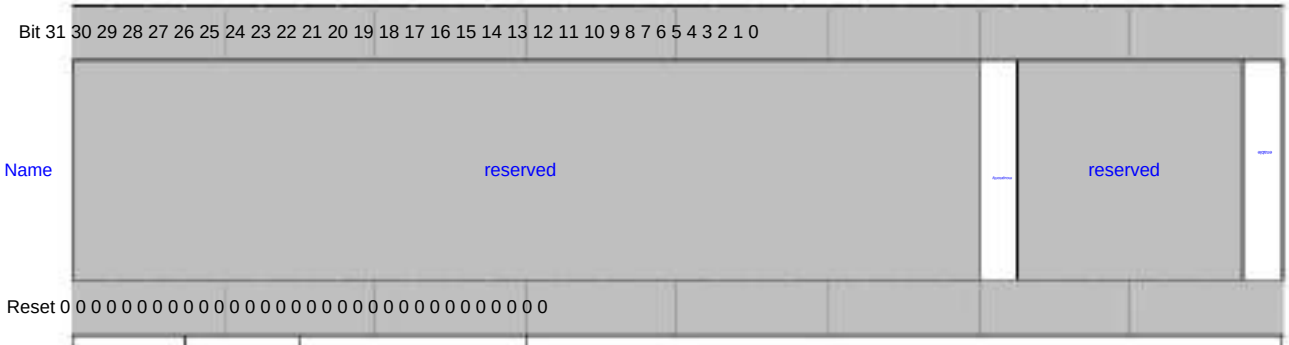
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black11
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black11	Black level offset for color channel B.

RADIAL_SHADING_CTRL

RADIAL_SHADING_CTRL is the control register of Radial_Shading module.

Offset Address	Register Name	Total Reset Value
0x203B0	RADIAL_SHADING_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	mcupriority	CPU write radial shading LUTs priority. 0ÿLOWÿ 1ÿHIGHÿ
[6:1]	RO	reserved	reserve.
[0]	RW	enable	Lens shading correction enabled. 0: forbidden; 1: enable.

RADIAL_SHADING_MCU_READY

RADIAL_SHADING_MCU_READY is the Radial_Shading LUT status register.

Offset Address	Register Name	Total Reset Value
0x203B4	RADIAL_SHADING_MCU_READY	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	mcuready	A 1 indicates that the LUT is ready to receive data from the CPU.

RADIAL_SHADING_RX

RADIAL_SHADING_RX is the X coordinate register of the center point of Radial_Shading R component.

Offset Address	Register Name	Total Reset Value
0x203B8	RADIAL_SHADING_RX	0x0000_03C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	centerr_x
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0	

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerr_x	Red shading map center coordinate x-direction coordinate value.

RADIAL_SHADING_RY

RADIAL_SHADING_RY is the Y coordinate register of the center point of Radial_Shading R component.

Offset Address	Register Name	Total Reset Value
0x203BC	RADIAL_SHADING_RY	0x0000_021C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	centerr_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerr_y	Red shading map center coordinate y-direction coordinate value.

RADIAL_SHADING_GX

RADIAL_SHADING_GX is the X coordinate register of the center point of Radial_Shading G component.

Offset Address	Register Name	Total Reset Value
0x203C0	RADIAL_SHADING_GX	0x0000_03C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	centerg_x
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerg_x	Green shading map center coordinate x-direction coordinate value.

RADIAL_SHADING_GY

RADIAL_SHADING_GY is the Y coordinate register of the center point of Radial_Shading G component.

Offset Address	Register Name	Total Reset Value
0x203C4	RADIAL_SHADING_GY	0x0000_021C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	centerg_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerg_y	Green shading map center coordinate y-direction coordinate value.

RADIAL_SHADING_BX

RADIAL_SHADING_BX is the X coordinate register of the center point of Radial_Shading B component.

Offset Address	Register Name	Total Reset Value
0x203C8	RADIAL_SHADING_BX	0x0000_03C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	centerb_x
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerb_x	The x-direction coordinate value of the blue shading map center coordinate.

RADIAL_SHADING_BY

RADIAL_SHADING_BY is the Y coordinate register of the center point of Radial_Shading B component.

Offset Address	Register Name	Total Reset Value
0x203CC	RADIAL_SHADING_BY	0x0000_021C

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	centerb_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 0 0 0 1 1 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	centerb_y	The center coordinate of the blue shading map is the coordinate value in the y direction.

RADIAL_SHADING_MULTR

RADIAL_SHADING_MULTR is the normalization factor of the Radial_Shading red radial table.

Offset Address	Register Name	Total Reset Value
0x203D0	RADIAL_SHADING_MULTR	0x0000_06EA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	off_center_multr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 0 1 0 1 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	off_center_multr	Normalization factor, which extends the red radial table to the edge of the image, calculated as 2^31/R^2, where R represents the farthest distance from the center coordinates to the edge pixels of the image.

RADIAL_SHADING_MULTG

RADIAL_SHADING_MULTG is the normalization factor of the Radial_Shading green radial table.

Offset Address	Register Name	Total Reset Value
0x203D4	RADIAL_SHADING_MULTG	0x0000_06EA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	off_center_multg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 0 1 0 1 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	off_center_multg	Normalization factor, which extends the green radial table to the edge of the image, calculated as 2^31/R^2, where R represents the furthest distance from the center coordinates to the edge pixels of the image.

RADIAL_SHADING_MULTB

RADIAL_SHADING_MULTB is the normalization factor of the Radial_Shading blue radial table.

Offset Address	Register Name	Total Reset Value
0x203D8	RADIAL_SHADING_MULTB	0x0000_06EA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	off_center_multb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 0 1 0 1 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	off_center_multb	Normalization factor, extending the blue radial table to the edge of the image, the calculation method is 2^31/R^2, where R represents the farthest distance from the center coordinates to the edge pixels of the image.

MESH_SHADING_CTRL

MESH_SHADING_CTRL is the Mesh_Shading control register.

Offset Address	Register Name	Total Reset Value
0x203E0	MESH_SHADING_CTRL	0x3F3F_0006

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name		mesh_height		mesh_width
Reset	0 0 1 1	1 1 1 1 0 0 1	1 1 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:24]	RW	mesh_height	The number of nodes in the vertical direction minus 1.
[23:22]	RO	reserved	reserve.
[21:16]	RW	mesh_width	The number of nodes in the horizontal direction minus 1.
[15:14]	RO	reserved	reserve.
[13:12]	RW	mesh_page_b	Select the corresponding memory page for blue component correction.
[11:10]	RW	mesh_page_g	Select the corresponding memory page for green component correction.
[9:8]	RW	mesh_page_r	Select the corresponding memory page for red component correction.
[7:5]	RO	reserved	reserve.

[4:2] RW mesh_scale			Select the accuracy and maximum gain range. 000ÿ0~2ÿ 001ÿ0~4ÿ 010ÿ0~8ÿ 011ÿ0~16ÿ 100ÿ1~2ÿ 101ÿ1~3ÿ 110ÿ1~5ÿ 111ÿ1~9ÿ Note: Gain is a floating point number.
[1] RW mesh_show			Lens shading correction debugging enabled. 0: forbidden; 1: enable.
[0] RW enable			Lens shading correction enabled. 0: forbidden; 1: enable.

MESH_SHADING_RELOAD

MESH_SHADING_RELOAD is the Mesh_Shading cache refresh register.

Offset Address	Register Name	Total Reset Value
0x203E4	MESH_SHADING_RELOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	mesh_reload	When the value of this bit changes from 0 to 1, cache refresh is triggered.

MESH_SHADING_ALPHAMODE

MESH_SHADING_ALPHAMODE is the alpha fusion mode register between Mesh_Shading entries.

Offset Address	Register Name	Total Reset Value
0x203F0	MESH_SHADING_ALPHAMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															----
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
mesh_alpha_mode			Set the ÿ fusion mode between Mesh_Shading entries. 00: no alpha fusion; 01: 2 banks (odd/even byte); [1:0] RW 10ÿ4 banksÿ 11: Reserved.

MESH_SHADING_ALPHA_BANK

MESH_SHADING_ALPHA_BANK select register for Mesh_Shading fusion bank.

Offset Address	Register Name	Total Reset Value
0x203F4	MESH_SHADING_ALPHA_BANK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5	4 3 2 1 0
Name	reserved	~~~	reserved	~~~	reserved	~~~
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:16]	RW	mesh_alpha_bank_ b	B component fusion bank selection. 000ÿ0+1ÿ 001ÿ1+2ÿ 010ÿ2:3ÿ 011ÿ3+0ÿ 100ÿ0+2ÿ 101ÿ1+3ÿ 11X: reserved.
[15:11]	RO	reserved	reserve.
[10:8]	RW	mesh_alpha_bank_ g	G component fusion bank selection. 000ÿ0+1ÿ 001ÿ1+2ÿ 010ÿ2:3ÿ 011ÿ3+0ÿ 100ÿ0+2ÿ 101ÿ1+3ÿ 11X: reserved.
[7:3]	RO	reserved	reserve.

[2:0] RW		mesh_alpha_bank_r	R component fusion bank selection. 000ÿ0+1ÿ 001ÿ1+2ÿ 010ÿ2:3ÿ 011ÿ3+0ÿ 100ÿ0+2ÿ 101ÿ1+3ÿ 11X: reserved.

MESH_SHADING_ALPHA

MESH_SHADING_ALPHA is the Mesh_Shading ÿ fusion coefficient register.

Offset Address	Register Name	Total Reset Value
0x203F8	MESH_SHADING_ALPHA	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	mesh_alpha_b	mesh_alpha_g	mesh_alpha_r
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	mesh_alpha_b	B component ÿ fusion coefficient.
[15:8]	RW	mesh_alpha_g	G component alpha fusion coefficient.
[7:0]	RW	mesh_alpha_r	R component alpha fusion coefficient.

MESH_SHADING_STRENGTH

MESH_SHADING_STRENGTH is the Mesh_Shading correction strength control register.

Offset Address	Register Name	Total Reset Value
0x203FC	MESH_SHADING_STRENGTH	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		mesh_strength
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0

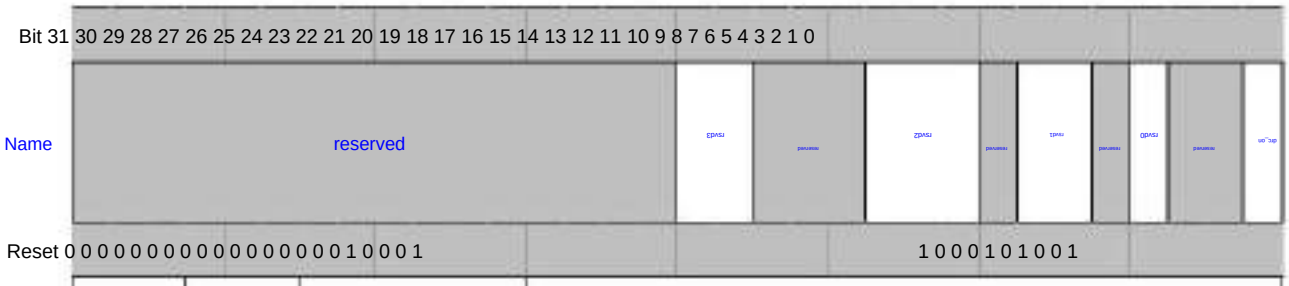
Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RW	mesh_strength		mesh correction strength, the format is 4.12. For example: 0 means no correction, 4096 means correction matching mesh data. Can be used to reduce shading strength depending on AE.

DRC_ENABLE

DRC_ENABLE is the DRC enable register.

Offset Address	Register Name	Total Reset Value
0x20400	DRC_ENABLE	0x0000_4629



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:14]	RW	rsvd3	Configuration is prohibited.
[13:11]	RO	reserved	reserve.
[10:8]	RW	rsvd2	Configuration is prohibited.
[7]	RO	reserved	reserve.
[6:5]	RW	rsvd1	Configuration is prohibited.
[4]	RO	reserved	reserve.
[3]	RW	rsvd0	Configuration is prohibited.
[2:1]	RO	reserved	reserve.
[0]	RW	drc_en	DRC is enabled. 0: forbidden; 1: enable.

DRC_CTRL

DRC_CTRL is the DRC module control register.

Offset Address	Register Name	Total Reset Value
0x20408	DRC_CTRL	0x0040_8012

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	slope_min	slope_max	variance_inten	variance_space sity
Reset	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	0 0 0 0	1 0 0 1 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	slope_min	Limits the minimum slope (gain) that can be generated by the adaptive algorithm.
[15:8]	RW	slope_max	Limits the maximum slope (gain) that can be generated by the adaptive algorithm.
[7:4]	RW	variance_intensity	Set algorithm brightness sensitivity.
[3:0]	RW	variance_space	Set algorithm airspace sensitivity.

DRC_BLACK_LEVEL

DRC_BLACK_LEVEL is the DRC black level register.

Offset Address	Register Name	Total Reset Value
0x20410	DRC_BLACK_LEVEL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black_level
Reset	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	black_level	DRC black level. Pixels below this value will not be affected by DRC.

DRC_WHITE_LEVEL

DRC_WHITE_LEVEL is the DRC white level register.

Offset Address	Register Name	Total Reset Value
0x20414	DRC_WHITE_LEVEL	0x000F_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / white_level
Reset	0 0 0 0 0 0 0 0 0 0 0 0 1 1 / 1 1 1 1 1 1 / 1 1 1 1 1 1

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	white_level	DRC white level. Pixels above this value will not be affected by DRC.

DRC_STRENGTH_INROI

DRC_STRENGTH_INROI is the intensity register of the DRC region of interest.

Offset Address	Register Name	Total Reset Value
0x20420	DRC_STRENGTH_INROI	0x0200_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / strength_inroi / reserved / pasj
Reset	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	strength_inroi	Manually set the strength in the region of interest.
[15:2]	RO	reserved	reserve.
[1:0]	RW	rsvd	Configuration is prohibited.

DRC_STRENGTH_OUTROI

DRC_STRENGTH_OUTROI is the register of the intensity and horizontal starting point in the DRC region of interest.

Offset Address	Register Name	Total Reset Value
0x20424	DRC_STRENGTH_OUTROI	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	roihorstart	reserved	strength_outroi
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	roihorstart	Horizontal starting point of the region of interest.
[15:10]	RO	reserved	reserve.
[9:0]	RW	strength_outroi	Manually set the strength outside the region of interest.

DRC_ROI_HOR_START_END

DRC_ROI_HOR_START_END is the vertical start point and horizontal end point register of the DRC region of interest.

Offset Address	Register Name	Total Reset Value
0x20428	DRC_ROI_HOR_START_END	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	roiverstart		roi_hor_end
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RW	roiverstart	The vertical starting point of the region of interest.
[15:0]	RW	roi_hor_end	Horizontal end point of region of interest.

DRC_ROI_VER_END

DRC_ROI_VER_END is the vertical end point register of the DRC region of interest.

Offset Address	Register Name	Total Reset Value
0x2042C	DRC_ROI_VER_END	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved		king_ver_end
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

Offset Address	Register Name	Total Reset Value
0x2042C	DRC_ROI_VER_END	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																king_ver_end															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access Name	Description
[15:0]	RW roi_ver_end	Vertical end point of region of interest.

DRC_FILTER_MUX

DRC_FILTER_MUX is the DRC algorithm control register.

Offset Address	Register Name	Total Reset Value
0x20430	DRC_FILTER_MUX	0xB0A0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	contrast								bright_pr								reserved				variance				reserved							
Reset	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:24]	RW contrast		drc Algorithm 2 contrast control parameter.
[23:16]	RW bright_pr		Manually control the drc Bright_Preserve parameter.
[15:12]	RO	reserved	reserve.
[11:8]	RW svariance		The transformation sensitivity of the drc algorithm 2 in different regions of the image.
[7:1]	RO	reserved	reserve.
[0]	RW filter_mux		drc Algorithm 2 and Algorithm 1 selection. 0: Algorithm 1; 1: Algorithm 2.

DRC_DARK_ENH

DRC_DARK_ENH Sets the register for the DRC Dark_Enhance parameter.

Offset Address	Register Name	Total Reset Value
0x20434	DRC_DARK_ENH	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dark_enh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15:0] RW	dark_enh		Manually control the drc Dark_Enhance parameter.

DRC_MCU_READY

DRC_MCU_READY is the status indication register of DRC LUT.

Offset Address	Register Name	Total Reset Value
0x20438	DRC_MCU_READY	0x0000_0006

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Bits	Access Name		Description
[31:3] RO		reserved	reserve.
[2]	RO	mcu_ready_rev	rev_percept LUT status indicator, when it is 1, it means that the LUT is ready to receive data from the CPU.
[1]	RO	mcu_ready_fwd	fwd Percept LUT status indicator, when it is 1, it means LUT is ready to receive data from CPU.
[0]	RO	mcu_priority	Priority for CPU to write LUT. 0: low; 1: High.

DEMOSAIC_VH_SLOPE

DEMOSAIC_VH_SLOPE is the slope register for the DEMOSAIC vertical/horizontal blend threshold.

Offset Address	Register Name	Total Reset Value
0x20480	DEMOSAIC_VH_SLOPE	0x0000_00C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	vh_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	vh_slope	Slope of the vertical/horizontal blending threshold, logarithmic in 4.4 format.

DEMOSAIC_AA_SLOPE

DEMOSAIC_AA_SLOPE is the slope register for the DEMOSAIC angle blending threshold.

Offset Address	Register Name	Total Reset Value
0x20484	DEMOSAIC_AA_SLOPE	0x0000_00C0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	aa_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	aa_slope	Slope of the angular blending threshold, logarithmic in 4.4 format.

DEMOSAIC_VA_SLOPE

DEMOSAIC_VA_SLOPE is the slope register of the DEMOSAIC VH-AA(VA) hybrid threshold.

Offset Address	Register Name	Total Reset Value
0x20488	DEMOSAIC_VA_SLOPE	0x0000_00AA

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	va_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0 1 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	va_slope	Slope of the VH-AA(VA) hybrid threshold, logarithmic in 4.4 format.

DEMOSAIC_UU_SLOPE

DEMOSAIC_UU_SLOPE is the slope register for the DEMOSAIC undefined blending threshold.

Offset Address	Register Name	Total Reset Value
0x2048C	DEMOSAIC_UU_SLOPE	0x0000_00AD

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	uu_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 0 1 0 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	uu_slope	Slope of the undefined mixing threshold, logarithmic in 4.4 format.

DEMOSAIC_SAT_SLOPE

DEMOSAIC_SAT_SLOPE is the slope register for the DEMOSAIC saturation mixing threshold.

Offset Address	Register Name	Total Reset Value
0x20490	DEMOSAIC_SAT_SLOPE	0x0000_005D

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	sat_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 1 0 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	sat_slope	The slope of the saturation blending threshold, in linear 2.6 format.

DEMOSAIC_VH_THRESH

DEMOSAIC_VH_THRESH is the threshold register of DEMOSAIC vertical/horizontal mixing range.

Offset Address	Register Name	Total Reset Value
0x20494	DEMOSAIC_VH_THRESH	0x0000_0131

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vh_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 1 1 0 0 0 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	vh_thresh	Threshold for vertical/horizontal blend range.

DEMOSAIC_AA_THRESH

DEMOSAIC_AA_THRESH is the threshold register for DEMOSAIC angle blending range.

Offset Address	Register Name	Total Reset Value
0x20498	DEMOSAIC_AA_THRESH	0x0000_00A0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aa_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	aa_thresh	Threshold for angular blend range.

DEMOSAIC_VA_THRESH

DEMOSAIC_VA_THRESH is the threshold register for the DEMOSAIC VA blending range.

Offset Address	Register Name	Total Reset Value
0x2049C	DEMOSAIC_VA_THRESH	0x0000_0070

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	va_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	va_thresh	Threshold for VA blending range.

DEMOSAIC_UU_THRESH

DEMOSAIC_UU_THRESH is the threshold register for DEMOSAIC undefined mixing range.

Offset Address	Register Name	Total Reset Value
0x204A0	DEMOSAIC_UU_THRESH	0x0000_0171

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	uu_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 0 0 0 1	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	uu_thresh	The threshold for the blend range is not defined.

DEMOSAIC_SAT_THRESH

DEMOSAIC_SAT_THRESH is the threshold register for DEMOSAIC saturation mixing range.

Offset Address	Register Name	Total Reset Value
0x204A4	DEMOSAIC_SAT_THRESH	0x0000_0171

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	sat_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 0 0 0 1	

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	sat_thresh	The threshold of the saturation blending range, in the format of a signed number 2.9.

DEMOSAIC_VH_OFFSET

DEMOSAIC_VH_OFFSET is the DEMOSAIC vertical/horizontal hybrid threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204A8	DEMOSAIC_VH_OFFSET	0x0000_0800

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	vh_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	vh_offset	Vertical/horizontal blend threshold offset.

DEMOSAIC_AA_OFFSET

DEMOSAIC_AA_OFFSET is the DEMOSAIC angle blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204AC	DEMOSAIC_AA_OFFSET	0x0000_0800

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	aa_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	aa_offset	Angular blend threshold offset.

DEMOSAIC_VA_OFFSET

DEMOSAIC_VA_OFFSET is the DEMOSAIC VA blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B0	DEMOSAIC_VA_OFFSET	0x0000_0800

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	va_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	va_offset	VA Blend Threshold Offset.

DEMOSAIC_UU_OFFSET

DEMOSAIC_UU_OFFSET is the DEMOSAIC undefined blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B4	DEMOSAIC_UU_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	uu_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	uu_offset	Blend Threshold Offset is not defined.

DEMOSAIC_SAT_OFFSET

DEMOSAIC_SAT_OFFSET is the DEMOSAIC saturation mixing threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B8	DEMOSAIC_SAT_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sat_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	sat_offset	Saturation blending threshold offset, in format 2.9.

DEMOSAIC_SHARP_ALT_D

DEMOSAIC_SHARP_ALT_D is the sharp mask strength register for DEMOSAIC directionality.

Offset Address	Register Name	Total Reset Value
0x204BC	DEMOSAIC_SHARP_ALT_D	0x0000_0030

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		sharp_alt_d
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	sharp_alt_d	Sharp mask strength for directional, signed number in 4.4 format.

DEMOSAIC_SHARP_ALT_OUT

DEMOSAIC_SHARP_ALT_UD is the DEMOSAIC non-directional sharpening mask strength register.

Offset Address	Register Name	Total Reset Value
0x204C0	DEMOSAIC_SHARP_ALT_OUT	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		sharp_all_out
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	sharp_alt_ud	Sharpening mask strength for non-directional, signed number in 4.4 format.

DEMOSAIC_LUM_THRESH

DEMOSAIC_LUM_THRESH is the sharpening brightness threshold register for DEMOSAIC directionality.

Offset Address	Register Name	Total Reset Value
0x204C4	DEMOSAIC_LUM_THRESH	0x0000_0060

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		lum_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1	0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	lum_thresh	Sharpened luminance threshold for directionality.

DEMOSAIC_NP_OFFSET

DEMOSAIC_NP_OFFSET configures the offset register for DEMOSAIC noise.

Offset Address	Register Name	Total Reset Value
0x204C8	DEMOSAIC_NP_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	np_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	np_offset	Noise configuration offset, logarithmic in 4.4 format.

DEMOSAIC_DMSC_CONFIG

DEMOSAIC_DMSC_CONFIG is selected for DEMOSAIC debug output.

Offset Address	Register Name	Total Reset Value
0x204CC	DEMOSAIC_DMSC_CONFIG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	dmsc_config
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	dmsc_config	Debug output selection, set to 0x00 for normal mode.

DEMOSAIC_AC_THRESH

DEMOSAIC_AC_THRESH is the threshold register for the DEMOSAIC AC mixed range.

Offset Address	Register Name	Total Reset Value
0x204D0	DEMOSAIC_AC_THRESH	0x0000_01B3

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ac_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 0 1 1 0 0 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ac_thresh	Threshold for AC blending range, number of symbols in 2.9 format.

DEMOSAIC_AC_SLOPE

DEMOSAIC_AC_SLOPE is the slope register for the DEMOSAIC AC blending threshold.

Offset Address	Register Name	Total Reset Value
0x204D4	DEMOSAIC_AC_SLOPE	0x0000_00CF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ac_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0 1 1 1 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ac_slope	Slope of the AC mixing threshold, in linear 2.6 format.

DEMOSAIC_AC_OFFSET

DEMOSAIC_AC_OFFSET is the DEMOSAIC AC blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204D8	DEMOSAIC_AC_OFFSET	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ac_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	ac_offset	AC blending threshold offset, number of symbols in 2.9 format.

DEMOSAIC_FC_SLPOE

DEMOSAIC_FC_SLPOE is the DEMOSAIC pseudo-color correction slope (intensity) register.

Offset Address	Register Name	Total Reset Value
0x204DC	DEMOSAIC_FC_SLPOE	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	fc_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	fc_slope	Pseudocolor correction for slope (intensity).

DEMOSAIC_FC_ALIAS_SLPOE

DEMOSAIC_FC_ALIAS_SLPOE is the DEMOSAIC pseudo-color correction slope (intensity) register.

Offset Address	Register Name	Total Reset Value
0x204E0	DEMOSAIC_FC_ALIAS_SLPOE	0x0000_0055

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	fc_alias_slope
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 0 1 0 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	fc_alias_slope	False color correction slope (intensity) when the saturation value is in unsigned 2.6 format.

DEMOSAIC_FC_ALIAS_THRESH

DEMOSAIC_FC_ALIAS_THRESH is the threshold value register for DEMOSAIC de-false color.

Offset Address	Register Name	Total Reset Value
0x204E4	DEMOSAIC_FC_ALIAS_THRESH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	fc_alias_thresh
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	fc_alias_thresh	The false color threshold value when the saturation value is in U0.8 format.

DEMOSAIC_NP_OFF

DEMOSAIC_NP_OFF is the DEMOSAIC noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x204EC	DEMOSAIC_NP_OFF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	np_off
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	np_off_reflect	How to get the value below the black level. 0: repeat the input of the first table; 1: Maps the part of the noise curve below the black level.
[6:0]	RW	np_off	Noise black level offset.

DEMOSAIC_SHARP

DEMOSAIC_SHARP is the DEMOSAIC Sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x204F0	DEMOSAIC_SHARP	0x1010_1010

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	sad_amp	sharp_alt_lu	sharp_alt_ldu	sharp_alt_ld
Reset	0 0 0 1 0 0 0 0	0 0 0 1 0 0 0 0	0 0 0 1 0 0 0 0	0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	sad_amp	Sad amplifier in unsigned 4.4 format.
[23:16]	RW	sharp_alt_lu	L_Lu Sharpen strength in unsigned format 4.4.
[15:8]	RW	sharp_alt_ldu	L_Ldu Sharpen strength in unsigned 4.4 format.
[7:0]	RW	sharp_alt_ld	L_Ld Sharpen strength in unsigned 4.4 format.

DEMOSAIC_MIN_THRESHOLD

DEMOSAIC_MIN_THRESHOLD is the DEMOSAIC threshold register.

Offset Address	Register Name	Total Reset Value
0x204F4	DEMOSAIC_MIN_THRESHOLD	0x1F48_1F33

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	—	min_ud_strength	—	min_d_strength
Reset	0 0 0 1	1 1 1 1 0 1 0 0 1 0 0 0 0 0 0 1 1	1	1 1 0 0 1 1 0 0 1

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	min_ud_strength	L_Lu non-directional minimum threshold, signed 12bit, 2-complement code.
[15:13]	RO	reserved	reserve.
[12:0]	RW	min_d_strength	L_L Directional minimum threshold, signed 12bit, 2-complement code.

DEMOSAIC_SHARPEN_ALG_SELECT

DEMOSAIC_SHARPEN_ALG_SELECT is the new Sharpen algorithm switching register for DEMOSAIC.

Offset Address	Register Name	Total Reset Value
0x204F8	DEMOSAIC_SHARPEN_ALG_SELECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	sharpen_alg_select	New Sharpen algorithm toggle. 0: disabled; 1: Switch to the new algorithm.

COLOR_MATRIX_COEFFT_RR

COLOR_MATRIX_COEFFT_RR is a matrix coefficient register that is a multiple of COLOR_MATRIX RR.

Offset Address	Register Name	Total Reset Value
0x20500	COLOR_MATRIX_COEFFT_RR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftr_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftr_r	Matrix coefficients for RR multiples. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_RG

COLOR_MATRIX_COEFFT_RG is a matrix coefficient register that is a multiple of COLOR_MATRIX RG.

Offset Address	Register Name	Total Reset Value
0x20504	COLOR_MATRIX_COEFFT_RG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftr_g
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftr_g	Matrix coefficients for RG multiples. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_RB

COLOR_MATRIX_COEFFT_RB is a matrix coefficient register that is a multiple of COLOR_MATRIX RB.

Offset Address	Register Name	Total Reset Value
0x20508	COLOR_MATRIX_COEFFT_RB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftr_b
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftr_b	Matrix coefficients for RB multiples. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_GR

COLOR_MATRIX_COEFFT_GR is the matrix coefficient register of COLOR_MATRIX GR multiple.

Offset Address	Register Name	Total Reset Value
0x2050C	COLOR_MATRIX_COEFFT_GR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftg_r
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RW	coefftg_r		Matrix coefficients for multiples of GR. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_GG

COLOR_MATRIX_COEFFT_GG is the matrix coefficient register of COLOR_MATRIX GG multiple.

Offset Address	Register Name	Total Reset Value
0x20510	COLOR_MATRIX_COEFFT_GG	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				coefftg_g											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftg_g	Matrix coefficients for multiples of GG. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_GB

COLOR_MATRIX_COEFFT_GB is the matrix coefficient register for multiples of COLOR_MATRIX GB.

Offset Address	Register Name	Total Reset Value
0x20514	COLOR_MATRIX_COEFFT_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				coefftg_b											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftg_b	Matrix coefficients in multiples of GB. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_BR

COLOR_MATRIX_COEFFT_BR is the matrix coefficient register for multiples of COLOR_MATRIX BR.

Offset Address	Register Name	Total Reset Value
0x20518	COLOR_MATRIX_COEFFT_BR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftb_r
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftb_r	Matrix coefficients for multiples of BR. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_BG

COLOR_MATRIX_COEFFT_BG is the matrix coefficient register of multiples of COLOR_MATRIX BG.

Offset Address	Register Name	Total Reset Value
0x2051C	COLOR_MATRIX_COEFFT_BG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftb_g
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefftb_g	Matrix coefficients for BG multiples. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_BB

COLOR_MATRIX_COEFFT_BB is the matrix coefficient register of COLOR_MATRIX BB multiple.

Offset Address	Register Name	Total Reset Value
0x20520	COLOR_MATRIX_COEFFT_BB	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefftb_b
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RW	coefftb_b		Matrix coefficients for multiples of BB. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_CTRL

COLOR_MATRIX_CTRL is the COLOR_MATRIX enable register.

Offset Address	Register Name	Total Reset Value
0x20524	COLOR_MATRIX_CTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	enable	Color_Matrix enabled. 0: forbidden; 1: enable.

COLOR_MATRIX_COEFFT_WBR

COLOR_MATRIX_COEFFT_WBR is COLOR_MATRIX R white balance gain register.

Offset Address	Register Name	Total Reset Value
0x20528	COLOR_MATRIX_COEFFT_WBR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft_wb_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefft_wb_r	R White balance gain. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_WBG

COLOR_MATRIX_COEFFT_WBG is COLOR_MATRIX G white balance gain register.

Offset Address	Register Name	Total Reset Value
0x2052C	COLOR_MATRIX_COEFFT_WBG	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefft_wb_g
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefft_wb_g	G White balance gain. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_WBB

COLOR_MATRIX_COEFFT_WBB is COLOR_MATRIX B white balance gain register.

Offset Address	Register Name	Total Reset Value
0x20530	COLOR_MATRIX_COEFFT_WBB	0x0000_0100

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefft_wb_b
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	coefft_wb_b	B White balance gain. Format: signed number, 4.8 bits, fixed point.

COLOR_MATRIX_COEFFT_FOG_OFFSETR

COLOR_MATRIX_COEFFT_FOG_OFFSETR is the COLOR_MATRIX color matrix R offset.

Offset Address	Register Name	Total Reset Value
0x20534	COLOR_MATRIX_COEFFT_FOG_OFFESTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefft_fog_offset_r
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	coefft_fog_offset_r	R component offset. Format: unsigned 12bit, integer.

COLOR_MATRIX_COEFFT_FOG_OFFSETG

COLOR_MATRIX_COEFFT_FOG_OFFSETG is the COLOR_MATRIX color matrix G offset.

Offset Address	Register Name	Total Reset Value
0x20538	COLOR_MATRIX_COEFFT_FOG_OFFSETG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefft_fog_offset_g
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	coefft_fog_offset_g	G component offset. Format: unsigned 12bit, integer.

COLOR_MATRIX_COEFFT_FOG_OFFSETB

COLOR_MATRIX_COEFFT_FOG_OFFSETB is the COLOR_MATRIX color matrix B offset.

Offset Address	Register Name	Total Reset Value
0x2053C	COLOR_MATRIX_COEFFT_FOG_OFFSETB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coefft_fog_offset_b
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	-	reserved	reserve.
[11:0]	RW	coefft_fog_offset_b	B component offset. Format: unsigned 12bit, integer.

GAMMA_RGB_CTRL

GAMMA_RGB_CTRL is the GAMMA_RGB control register.

Offset Address	Register Name	Total Reset Value
0x20580	GAMMA_RGB_CTRL	0x0000_0081

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	mcu_priority	CPU write LUT priority. 0: low; 1: High.
[6:5]	RO	reserved	reserve.
[4]	RW	bank_select	LUT RAM Bank selection control. 0: GAMMA_RGB selects bank 0; 1: GAMMA_RGB selects bank 1.
[3:1]	RO	reserved	reserve.

[0] RW enable			Gamma RGB enabled. 0: forbidden; 1: enable.

GAMMA_RGB_MCU_READY

GAMMA_RGB_MCU_READY is the status flag of GAMMA_RGB LUT receiving data from CPU.

Offset Address	Register Name	Total Reset Value
0x20584	GAMMA_RGB_MCU_READY	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access Name		Description
[31:1] RO		reserved	reserve.
[0]	RO	When mcu_ready is 1, it indicates that the LUT is ready to receive data from the CPU.	

DITHER_CTRL

DITHER_CTRL is the DITHER control register.

Offset Address	Register Name	Total Reset Value
0x20680	DITHER_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:5] RO		reserved	reserve.

[4] RW	shift_mode		Output mode selection. 0: Output adopts LSB alignment; 1: Output is MSB aligned.
[3]	RO	reserved	reserve.
[2:1] RW	dither_amount		Mode selection. 00: Adjust the output bit width to 9 bits; 01: Adjust the output bit width to 8 bits; 10: Adjust the output bit width to 7 bits; 11: Adjust the output bit width to 6 bits.
[0] RW	enable_dither		Enables the dithering module. 0: forbidden; 1: enable.

STATISTICS_HIST_THRESH_0_1

STATISTICS_HIST_THRESH_0_1 is the histogram threshold register for Bin 0/1 boundary.

Offset Address	Register Name	Total Reset Value
0x20700	STATISTICS_HIST_THRESH_0_1	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved hist_thresh_0_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hist_thresh_0_1	Histogram threshold for Bin 0/1 boundary.

STATISTICS_HIST_THRESH_1_2

STATISTICS_HIST_THRESH_1_2 is the histogram threshold register for Bin 1/2 boundary.

Offset Address	Register Name	Total Reset Value
0x20704	STATISTICS_HIST_THRESH_1_2	0x0000_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		hist_thresh_1_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hist_thresh_1_2	Histogram threshold for Bin 1/2 boundary.

STATISTICS_HIST_THRESH_3_4

STATISTICS_HIST_THRESH_3_4 is the histogram threshold register for Bin 2/3 boundary.

Offset Address	Register Name	Total Reset Value
0x20708	STATISTICS_HIST_THRESH_3_4	0x0000_00D0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		hist_thresh_3_4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 0 1 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hist_thresh_3_4	Histogram threshold for Bin 2/3 boundary.

STATISTICS_HIST_THRESH_4_5

STATISTICS_HIST_THRESH_4_5 is the histogram threshold of Bin 3/4 boundary.

Offset Address	Register Name	Total Reset Value
0x2070C	STATISTICS_HIST_THRESH_4_5	0x0000_00E0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved		hist_thresh_4_5
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	hist_thresh_4_5	Histogram threshold for Bin 3/4 boundary.

STATISTICS_HIST_0

STATISTICS_HIST_0 is the normalized histogram result register of Bin 0.

Offset Address	Register Name	Total Reset Value
0x20720	STATISTICS_HIST_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hist_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	hist_0	The normalized histogram result for Bin 0.

STATISTICS_HIST_1

STATISTICS_HIST_1 is the normalized histogram result register of Bin 1.

Offset Address	Register Name	Total Reset Value
0x20724	STATISTICS_HIST_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hist_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	hist_1	The normalized histogram result for Bin 1.

STATISTICS_HIST_3

STATISTICS_HIST_3 is the normalized histogram result register of Bin 3.

Offset Address	Register Name	Total Reset Value
0x20728	STATISTICS_HIST_3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hist3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	hist3	The normalized histogram result for Bin 3.

STATISTICS_HIST_4

STATISTICS_HIST_4 is the normalized histogram result register of Bin 4.

Offset Address	Register Name	Total Reset Value
0x2072C	STATISTICS_HIST_4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	hist_4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	hist_4	The normalized histogram result for Bin 4.

STATISTICS_AEXP_NODES_USED

STATISTICS_AEXP_NODES_USED is the AE effective area register.

Offset Address	Register Name	Total Reset Value
0x20730	STATISTICS_AEXP_NODES_USED	0x0000_0F11

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	aexp_nodes_used_vert	aexp_nodes_used_horiz
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1	0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	aexp_nodes_used_ AE vert	Number of vertical valid areas.

[7:0] RW		aexp_nodes_used_horiz	Number of AE horizontal valid areas.

STATISTICS_WHITE_LEVEL_AWB

STATISTICS_WHITE_LEVEL_AWB is the luminance upper limit register of AWB statistic white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20740	STATISTICS_WHITE_LEVEL_AWB	0x0000_03FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	white_level_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	white_level_awb	RGB domain AWB statistical white point brightness data upper limit.

STATISTICS_BLACK_LEVEL_AWB

STATISTICS_BLACK_LEVEL_AWB is the luminance lower limit register of AWB statistical white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20744	STATISTICS_BLACK_LEVEL_AWB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	black_level_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	black_level_awb	RGB domain AWB statistical white point brightness lower limit.

STATISTICS_CR_REF_MAX_AWB

STATISTICS_CR_REF_MAX_AWB is the chromaticity R/G upper limit register of AWB statistical white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20748	STATISTICS_CR_REF_MAX_AWB	0x0000_01FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cr_ref_max_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cr_ref_max_awb	Chroma R/G upper limit of RGB domain AWB statistical white point. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_CR_REF_MIN_AWB

STATISTICS_CR_REF_MIN_AWB is the chromaticity R/G lower limit register of AWB statistical white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x2074C	STATISTICS_CR_REF_MIN_AWB	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cr_ref_min_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cr_ref_min_awb	Chroma R/G lower limit of RGB domain AWB statistical white point. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_CB_REF_MAX_AWB

STATISTICS_CB_REF_MAX_AWB is the chromaticity B/G upper limit register of AWB statistical white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20750	STATISTICS_CB_REF_MAX_AWB	0x0000_01FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cb_ref_max_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cb_ref_max_awb	Chroma B/G upper limit of AWB statistical white point in RGB domain. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_CB_REF_MIN_AWB

STATISTICS_CB_REF_MIN_AWB is the chromaticity B/G lower limit register of AWB statistical white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20754	STATISTICS_CB_REF_MIN_AWB	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cb_ref_min_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cb_ref_min_awb	Chroma B/G lower limit of white point in RGB domain AWB statistics. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_AWB_RG

STATISTICS_AWB_RG is the AWB statistical G/R average value register in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20758	STATISTICS_AWB_RG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	awb_rg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.

[11:0] RO		awb_rg	RGB domain AWB statistics G/R mean. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_AWB_BG

STATISTICS_AWB_BG is the G/B mean value register of RGB domain AWB statistics.

Offset Address	Register Name	Total Reset Value
0x2075C	STATISTICS_AWB_BG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	awb_bg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RO	awb_bg	RGB Domain AWB Statistics G/B mean. Format: unsigned number, 4.8bit, fixed point.

STATISTICS_AWB_SUM

STATISTICS_AWB_SUM is the register of the number of white dots counted by RGB domain AWB.

Offset Address	Register Name	Total Reset Value
0x20760	STATISTICS_AWB_SUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	awb_sum	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	awb_sum	The number of white points counted by AWB in RGB domain, the format is 32bit integer.

STATISTICS_AWB_STATS_MODE

STATISTICS_AWB_STATS_MODE is the output mode selection register for AWB statistical results in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20768	STATISTICS_AWB_STATS_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	awb_stats_mode	RGB domain AWB statistical result output mode selection. 0ÿlegacy(G/R,B/R)ÿ 1ÿcurrent (R/G, B/G)ÿ

STATISTICS_AWB_NODES_USED

STATISTICS_AWB_NODES_USED is the register for the number of AWB statistical partitions in the RGB domain.

Offset Address	Register Name	Total Reset Value
0x20770	STATISTICS_AWB_NODES_USED	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																awb_nodes_used_vert								awb_nodes_used_horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	awb_nodes_used_v	AWB vertical area number. ert
[7:0]	RW	awb_nodes_used_horiz	AWB horizontal area number.

STATISTICS_CR_REF_HIGH_AWB

STATISTICS_CR_REF_HIGH_AWB is the chromaticity R/G hexagon upper limit register of the AWB statistical white point in the RGB domain.

Offset Address	Register Name	Total Reset Value
0x20780	STATISTICS_CR_REF_HIGH_AWB	0x0000_0FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cr_ref_high_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cr_ref_high_awb	Chroma R/G hexagonal upper bound for AWB statistical white point in RGB domain in unsigned 4.8 fixed point format.

STATISTICS_CR_REF_LOW_AWB

STATISTICS_CR_REF_LOW_AWB is the chromaticity R/G hexagonal lower limit register of AWB statistics white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20784	STATISTICS_CR_REF_LOW_AWB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cr_ref_low_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cr_ref_low_awb	Chroma R/G hexagonal lower bound of the AWB statistical white point in the RGB domain, in unsigned 4.8 fixed-point format.

STATISTICS_CB_REF_HIGH_AWB

STATISTICS_CB_REF_HIGH_AWB is the chromaticity B/G hexagon upper limit register of AWB statistics white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x20788	STATISTICS_CB_REF_HIGH_AWB	0x0000_0FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cb_ref_high_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cb_ref_high_awb	Chroma B/G hexagonal upper bound of the RGB domain AWB statistical white point in unsigned 4.8 fixed point format.

STATISTICS_CB_REF_LOW_AWB

STATISTICS_CB_REF_LOW_AWB is the chromaticity B/G hexagon lower limit register of AWB statistics white point in RGB domain.

Offset Address	Register Name	Total Reset Value
0x2078C	STATISTICS_CB_REF_LOW_AWB	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	cb_ref_low_awb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	cb_ref_low_awb	Chroma B/G hexagon lower limit of RGB domain AWB statistical white point in unsigned 4.8 fixed point format.

STATISTICS_PLANE_TOTAL_0

STATISTICS_PLANE_TOTAL_0 Register 0 for total pixels processed per plane.

Offset Address	Register Name	Total Reset Value
0x207A0	STATISTICS_PLANE_TOTAL_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								plane_total_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_0	Total pixels processed by plane 0.

STATISTICS_PLANE_TOTAL_1

STATISTICS_PLANE_TOTAL_1 Register 1 for total pixels processed per plane.

Offset Address	Register Name	Total Reset Value
0x207A4	STATISTICS_PLANE_TOTAL_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								plane_total_1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_1	Total pixels processed by plane 1.

STATISTICS_PLANE_TOTAL_2

STATISTICS_PLANE_TOTAL_2 Register 2 for total pixels processed per plane.

Offset Address	Register Name	Total Reset Value
0x207A8	STATISTICS_PLANE_TOTAL_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								plane_total_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_2	Total pixels processed by plane 2.

STATISTICS_PLANE_TOTAL_3

STATISTICS_PLANE_TOTAL_3 Register 3 for total pixels processed per plane.

Offset Address	Register Name	Total Reset Value
0x207AC	STATISTICS_PLANE_TOTAL_3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_total_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_3	Total pixels processed by plane 3.

STATISTICS_PLANE_COUNTED_0

STATISTICS_PLANE_COUNTED_0 is the cumulative sum register 0 of the total pixels per plane.

Offset Address	Register Name	Total Reset Value
0x207B0	STATISTICS_PLANE_COUNTED_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_counted_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_0	Cumulative sum of plane 0 total pixels.

STATISTICS_PLANE_COUNTED_1

STATISTICS_PLANE_COUNTED_1 is the cumulative sum register 1 of the total pixels per plane.

Offset Address	Register Name	Total Reset Value
0x207B4	STATISTICS_PLANE_COUNTED_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														plane_counted_1	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_1	Cumulative sum of plane 1 total pixels.

STATISTICS_PLANE_COUNTED_2

STATISTICS_PLANE_COUNTED_2 is the accumulated sum register 2 of total pixels per plane.

Offset Address	Register Name	Total Reset Value
0x207B8	STATISTICS_PLANE_COUNTED_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														plane_counted_2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_2	Cumulative sum of plane 2 total pixels.

STATISTICS_PLANE_COUNTED_3

STATISTICS_PLANE_COUNTED_3 is the cumulative sum register 3 of the total pixels per plane.

Offset Address	Register Name	Total Reset Value
0x207BC	STATISTICS_PLANE_COUNTED_3	0x0000_0000

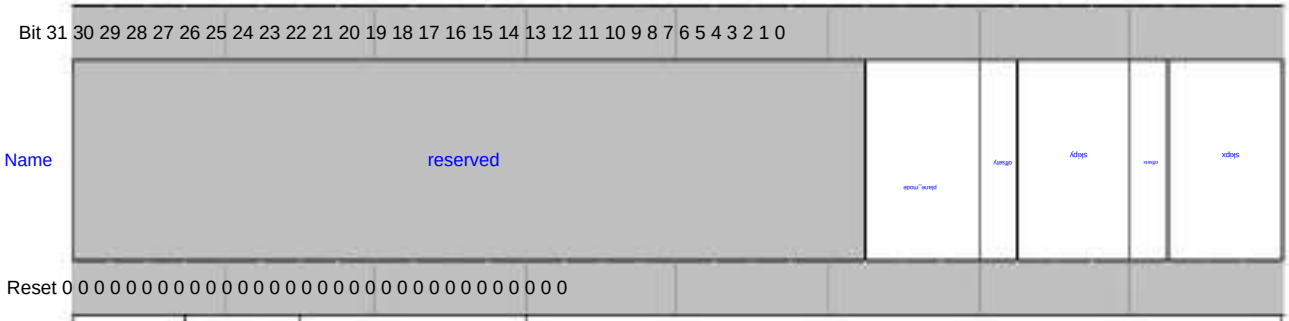
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														plane_counted_3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_3	Cumulative sum of plane 3 total pixels.

STATISTICS_HISTOGRAM_CTRL

STATISTICS_HISTOGRAM_CTRL is the Histogram control register.

Offset Address	Register Name	Total Reset Value
0x207C0	STATISTICS_HISTOGRAM_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:8]	RW	plane_mode	Split mode selection. 000: Collect all faces and put them in a histogram; 001: Collect 4 Bayer faces and put them in 4 independent banks; 010: Reserve; 011: reserved; 100: The coordinate x of the collection surface is an odd number, and the coordinate y is an odd number to bank0, and the rest to bank1; 101: The coordinate x of the collection surface is an even number, and the coordinate y is an odd number to bank0, and the rest to bank1; 110: The coordinate x of the collection surface is an odd number, and the coordinate y is an even number to bank0, and the rest to bank1; 111: The coordinate x of the collection surface is an even number, and the coordinate y is an even number to bank0, and the rest to bank1.
[7]	RW	offsety	Start row selection. 0: start from the first row; 1: Start from the second row.

[6:4] RW skipy			Histogram extraction in the vertical direction. 000: every pixel; 001: every 2 pixels; 010: every 3 pixels; 011: every 4 pixels; 100: every 5 pixels; 101: every 8 pixels; Other: every 9 pixels.
[3] RW offsetx			Start column selection. 0: start from the first column; 1: Start from the second column.
[2:0] RW skipx			Histogram extraction in the horizontal direction. 000: every 2 pixels; 001: every 3 pixels; 010: every 4 pixels; 011: every 5 pixels; 100: every 8 pixels; Other: every 9 pixels.

STATISTICS_SCALE

STATISTICS_SCALE is the SCALE control register.

Offset Address	Register Name	Total Reset Value
0x207C4	STATISTICS_SCALE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	scale_top	scale_bottom
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.

[7:4] RW scale_top			Upper half zoom ratio. 000ÿ1xÿ 001ÿ2xÿ 010ÿ4xÿ 011ÿ8xÿ 100ÿ16xÿ Others: reserved.
[3:0] RW scale_bottom			Bottom half zoom ratio. 000ÿ1xÿ 001ÿ2xÿ 010ÿ4xÿ 011ÿ8xÿ 100ÿ16xÿ Others: reserved.

STATISTICS_TOTAL_PIXELS

STATISTICS_TOTAL_PIXELS Register for the total number of pixels processed by STATISTICS.

Offset Address	Register Name	Total Reset Value
0x207C8	STATISTICS_TOTAL_PIXELS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	total_pixels
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_pixels	The total number of pixels processed (skipped x and y are also counted).

STATISTICS_COUNTED_PIXELS

STATISTICS_COUNTED_PIXELS is the register of the number of pixels accumulated by STATISTICS.

Offset Address	Register Name	Total Reset Value
0x207CC	STATISTICS_COUNTED_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	counted_pixels																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	counted_pixels	The number of accumulated pixels (weight is not 0).

STATISTICS_PE_HISTOGRAM_CTRL

STATISTICS_PE_HISTOGRAM_CTRL is the PE control register.

Offset Address	Register Name	Total Reset Value
0x207D0	STATISTICS_PE_HISTOGRAM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:11]	RO	reserved	reserve.

[10:8] RW plane_mode_pe			Split mode selection. 000: Collect all faces and put them in a histogram; 001: Collect 4 Bayer faces and put them in 4 independent banks; 010: Reserve; 011: reserved; 100: The coordinate x of the collection surface is an odd number, and the coordinate y is an odd number to bank0, and the rest to bank1; 101: The coordinate x of the collection surface is an even number, and the coordinate y is an odd number to bank0, and the rest to bank1; 110: The coordinate x of the collection surface is an odd number, and the coordinate y is an even number to bank0, and the rest to bank1; 111: The coordinate x of the collection surface is an even number, and the coordinate y is an even number to bank0, and the rest to bank1.
[7] RW offset_y_pe			Start row selection. 0: start from the first row; 1: Start from the second row.
[6:4] RW skip_y_pe			Histogram extraction in the vertical direction. 000: every pixel; 001: every 2 pixels; 010: every 3 pixels; 011: every 4 pixels; 100: every 5 pixels; 101: every 8 pixels; Other: every 9 pixels.
[3] RW offset_x_pe			Start column selection. 0: start from the first column; 1: start from the second column.
[2:0] RW skip_x_pe			Histogram extraction in the horizontal direction. 000: every 2 pixels; 001: every 3 pixels; 010: every 4 pixels; 011: every 5 pixels; 100: every 8 pixels; Other: every 9 pixels.

STATISTICS_PE_SCALE

STATISTICS_PE_SCALE is the PE_SCALE control register.

Offset Address	Register Name	Total Reset Value
0x207D4	STATISTICS_PE_SCALE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	scale_top_on	scale_bottom_on
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:4]	RW	scale_top_pe	Upper half zoom ratio. 0x0ÿ1xÿ 0x1ÿ2xÿ 0x2ÿ4xÿ 0x3ÿ8xÿ 0x4ÿ16xÿ Other: reserved.
[3:0]	RW	scale_bottom_pe	Bottom half zoom ratio. 0x0ÿ1xÿ 0x1ÿ2xÿ 0x2ÿ4xÿ 0x3ÿ8xÿ 0x4ÿ16xÿ Other: reserved.

STATISTICS_PE_TOTAL_PIXELS

STATISTICS_PE_TOTAL_PIXELS is the register for the total number of pixels processed by PE.

Offset Address	Register Name	Total Reset Value
0x207D8	STATISTICS_PE_TOTAL_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_pixels_pe																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	total_pixels_pe	Total number of pixels processed (skipped x and y are also counted).

STATISTICS_PE_COUNTED_PIXELS

STATISTICS_PE_COUNTED_PIXELS is the register of the number of pixels accumulated by PE.

Offset Address	Register Name	Total Reset Value
0x207DC	STATISTICS_PE_COUNTED_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	counted_pixels_pe																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	counted_pixels_pe	The number of accumulated pixels (weight is not 0).

STATISTICS_PLANE_TOTAL_PE_0

STATISTICS_PLANE_TOTAL_PE_0 is the total pixel register 0 processed by each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207E0	STATISTICS_PLANE_TOTAL_PE_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					plane_total_pe_0																										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_pe_0	Number of pixels processed per plane.

STATISTICS_PLANE_TOTAL_PE_1

STATISTICS_PLANE_TOTAL_PE_1 is the total pixel register 1 processed by each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207E4	STATISTICS_PLANE_TOTAL_PE_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_total_pe_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_pe_1	Number of pixels processed per plane.

STATISTICS_PLANE_TOTAL_PE_2

STATISTICS_PLANE_TOTAL_PE_2 is the total pixel register 2 processed by each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207E8	STATISTICS_PLANE_TOTAL_PE_2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_total_pe_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_pe_2	Number of pixels processed per plane.

STATISTICS_PLANE_TOTAL_PE_3

STATISTICS_PLANE_TOTAL_PE_3 is the total pixel register 3 processed by each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207EC	STATISTICS_PLANE_TOTAL_PE_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						plane_total_pe_3									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_total_pe_3	Number of pixels processed per plane.

STATISTICS_PLANE_COUNTED_PE_0

STATISTICS_PLANE_COUNTED_PE_0 is the cumulative sum register 0 of the total pixels of each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207F0	STATISTICS_PLANE_COUNTED_PE _0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						plane_counted_pe_0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_pe_0	Cumulative sum of pixels per plane.

STATISTICS_PLANE_COUNTED_PE_1

STATISTICS_PLANE_COUNTED_PE_1 is the accumulation and register 1 of the total pixels of each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207F4	STATISTICS_PLANE_COUNTED_PE _1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						plane_counted_pe_1									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.

[26:0] RO		plane_counted_pe_	Cumulative sum of pixels per plane. 1

STATISTICS_PLANE_COUNTED_PE_2

STATISTICS_PLANE_COUNTED_PE_2 is the cumulative sum register 2 of the total pixels of each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207F8	STATISTICS_PLANE_COUNTED_PE _2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_counted_pe_2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_pe_	Cumulative sum of pixels per plane. 2

STATISTICS_PLANE_COUNTED_PE_3

STATISTICS_PLANE_COUNTED_PE_3 is the accumulative sum register 3 of the total pixels of each plane of PE.

Offset Address	Register Name	Total Reset Value
0x207FC	STATISTICS_PLANE_COUNTED_PE _3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / plane_counted_pe_3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:0]	RO	plane_counted_pe_	Cumulative sum of pixels per plane. 3

STATISTICS_SUM_R

STATISTICS_SUM_R is the normalized R component pixel sum.

Offset Address	Register Name	Total Reset Value
0x20800	STATISTICS_SUM_R	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sum_r
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	sum_r	Normalized sum of R component pixels.

STATISTICS_SUM_RG

STATISTICS_SUM_RG is the normalized Gr component pixel sum.

Offset Address	Register Name	Total Reset Value
0x20804	STATISTICS_SUM_RG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sum_rg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	sum_rg	Normalized Gr component pixel sum.

STATISTICS_SUM_BG

STATISTICS_SUM_BG is the normalized Gb component pixel sum.

Offset Address	Register Name	Total Reset Value
0x20808	STATISTICS_SUM_BG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sum_bg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	sum_bg	Normalized Gb component pixel sum.

STATISTICS_SUM_B

STATISTICS_SUM_B is the normalized B component pixel sum.

Offset Address	Register Name	Total Reset Value
0x2080C	STATISTICS_SUM_B	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	sum_b
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	sum_b	Normalized B-component pixel-point sum.

STATISTICS_AE_SUM_NODES_USED

STATISTICS_AE_SUM_NODES_USED is the AE_SUM effective area register.

Offset Address	Register Name	Total Reset Value
0x20810	STATISTICS_AE_SUM_NODES_USED	0x0000_0F11

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ae_sum_nodes_used_vert	ae_sum_nodes_used_horiz
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 0 0 0 1 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	ae_sum_nodes_used_vert	Number of vertical valid areas.
[7:0]	RW	ae_sum_nodes_used_horiz	Number of horizontal effective regions.

STATISTICS_AVG_R

STATISTICS_AVG_R is the mean of the R component of the Bayer domain AWB SUM statistics.

Offset Address	Register Name	Total Reset Value
0x20820	STATISTICS_AVG_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														avg_r	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	avg_r	Bayer domain AWB SUM Statistic R component mean.

STATISTICS_AVG_G

STATISTICS_AVG_G is the mean value of the G component of the Bayer domain AWB SUM statistics.

Offset Address	Register Name	Total Reset Value
0x20824	STATISTICS_AVG_G	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														avg_g	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	avg_g	Bayer domain AWB SUM Statistic G-component mean.

STATISTICS_AVG_B

STATISTICS_AVG_B is the mean of the B component of the Bayer domain AWB SUM statistics.

Offset Address	Register Name	Total Reset Value
0x20828	STATISTICS_AVG_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														avg_b	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	avg_b	Bayer Domain AWB SUM Statistic B-component mean.

STATISTICS_COUNT_ALL

STATISTICS_COUNT_ALL is the Bayer domain AWB SUM counts the number of pixels that meet the white point condition, and has been normalized.

Offset Address	Register Name	Total Reset Value
0x2082C	STATISTICS_COUNT_ALL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	count_all
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	count_all	Bayer domain AWB SUM counts the number of pixels that meet the white point condition.

STATISTICS_COUNT_MIN

STATISTICS_COUNT_MIN counts the number of pixels less than the lower limit of brightness for Bayer domain AWB SUM.

Offset Address	Register Name	Total Reset Value
0x20830	STATISTICS_COUNT_MIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	count_min
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	count_min	Bayer domain AWB SUM counts the number of pixels less than the lower limit of brightness.

STATISTICS_COUNT_MAX

STATISTICS_COUNT_MAX counts the number of pixels greater than the brightness upper limit for Bayer domain AWB SUM.

Offset Address	Register Name	Total Reset Value
0x20834	STATISTICS_COUNT_MAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	count_max
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	count_max	The Bayer domain AWB SUM counts the number of pixels greater than the brightness upper limit.

STATISTICS_AWB_SUM_NODES_USED

STATISTICS_AWB_SUM_NODES_USED is the AWB_SUM effective area register.

Offset Address	Register Name	Total Reset Value
0x20838	STATISTICS_AWB_SUM_NODES_US ED	0x0000_2020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	awb_sum_nodes_used_vert awb_sum_nodes_used_horiz
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:8]	RW	awb_sum_nodes_used_vert	Number of vertical valid areas.
[7:0]	RW	awb_sum_nodes_used_horiz	Number of horizontal valid areas.

STATISTICS_MIN_THRESHOLD

STATISTICS_MIN_THRESHOLD is the lower limit of brightness of AWB SUM statistical white point in Bayer domain.

Offset Address	Register Name	Total Reset Value
0x2083C	STATISTICS_MIN_THRESHOLD	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	min_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	min_threshold	Bayer Domain AWB SUM Statistical lower luminance limit of the white point.

STATISTICS_MAX_THRESHOLD

STATISTICS_MAX_THRESHOLD is the brightness upper limit of the statistical white point of AWB SUM in Bayer domain.

Offset Address	Register Name	Total Reset Value
0x20840	STATISTICS_MAX_THRESHOLD	0x0000_0FF0

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	max_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_threshold	Bayer Domain AWB SUM Statistical upper luminance upper limit of the white point.

STATISTICS_AWB_SUM_CLIP

STATISTICS_AWB_SUM_CLIP is the clip of AWB SUM.

Offset Address	Register Name	Total Reset Value
0x20844	STATISTICS_AWB_SUM_CLIP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														max_clip	min_clip
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	max_clip	Upper threshold clip of AWB SUM.
[0]	RW	min_clip	Lower threshold clip of AWB SUM.

STATISTICS_CR_REF

STATISTICS_CR_REF is the upper and lower limits of chromaticity R/G of AWB statistical white point in Bayer domain.

Offset Address	Register Name	Total Reset Value
0x20848	STATISTICS_CR_REF	0x0040_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cr_ref_min_awb_sum												reserved				cr_ref_max_awb_sum											
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	unsigned number cr_ref_min_awb_sum	The chromaticity R/G lower limit of AWB statistical white point in Bayer domain, the format is 4.8bit fixed point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	unsigned number cr_ref_max_awb_sum	The chromaticity R/G upper limit of AWB statistical white point in Bayer domain, the format is 4.8bit fixed point.

STATISTICS_CB_REF

STATISTICS_CB_REF is the upper and lower limits of chromaticity B/G of AWB statistical white point in Bayer domain.

Offset Address	Register Name	Total Reset Value
0x2084C	STATISTICS_CB_REF	0x0040_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cb_ref_min_awb_sum														reserved				cb_ref_max_awb_sum					
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access Name		Description
[31:28] RO		reserved	reserve.
[27:16] RW		unsigned number one cb_ref_min_awb_s	The chromaticity B/G lower limit of the AWB statistical white point in Bayer domain, the format is 4.8bit fixed point.
[15:12] RO		reserved	reserve.
[11:0] RW		unsigned number one cb_ref_max_awb_s	The chromaticity B/G upper limit of AWB statistical white point in Bayer domain, the format is 4.8bit fixed point.

STATISTICS_CR_HL_REF

STATISTICS_CR_HL_REF is the chromaticity R/G hexagon limit for the AWB statistics white point in the Bayer domain.

Offset Address	Register Name	Total Reset Value
0x20850	STATISTICS_CR_HL_REF	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cr_ref_low_awb_sum														reserved				cr_ref_high_awb_sum					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access Name		Description
[31:28] RO		reserved	reserve.
[27:16] RW		unsigned cr_ref_low_awb_sum	Bayer domain AWB statistical white point chromaticity R/G hexagonal lower limit, the format is number 4.8bit fixed point.
[15:12] RO		reserved	reserve.
[11:0] RW		unsigned cr_ref_high_awb_s one	Chroma R/G hexagon upper limit of AWB statistical white point in Bayer domain, the format is number 4.8bit fixed point.

STATISTICS_CB_HL_REF

STATISTICS_CB_HL_REF is the chromaticity B/G hexagon limit for the AWB statistical white point in the Bayer domain.

Offset Address	Register Name	Total Reset Value
0x20854	STATISTICS_CB_HL_REF	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cb_ref_low_awb_sum											reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	unsigned cb_ref_low_awb_sone	Bayer domain AWB Statistical white point Chromaticity B/G Hexagonal lower limit, the format is number 4.8bit fixed point.
[15:12]	RO	reserved	reserve.
[11:0]	RW	unsigned cb_ref_high_awb_sone	Chroma B/G hexagon upper limit of AWB statistical white point in Bayer domain, the format is number 4.8bit fixed point.

FRAME_STATS_STATS_RESET

FRAME_STATS_STATS_RESET is the status reset register.

Offset Address	Register Name	Total Reset Value
0x20900	FRAME_STATS_STATS_RESET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	stats_reset	Reset the frame statistics register and start periodic sampling, the maximum statistics of all frames is 2^31.

FRAME_STATS_STATS_HOLD

FRAME_STATS_STATS_HOLD is the state holding register.

Offset Address	Register Name	Total Reset Value
0x20904	FRAME_STATS_STATS_HOLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	stats_hold	When configured as 1, statistics register update is disabled.

FRAME_STATS_ACTIVE_WIDTH_MIN

FRAME_STATS_ACTIVE_WIDTH_MIN is the minimum width register.

Offset Address	Register Name	Total Reset Value
0x20910	FRAME_STATS_ACTIVE_WIDTH_MIN	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	active_width_min
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:0]	RO	active_width_min	Minimum width register.

FRAME_STATS_ACTIVE_WIDTH_MAX

FRAME_STATS_ACTIVE_WIDTH_MAX is the maximum width register.

Offset Address	Register Name	Total Reset Value
0x20914	FRAME_STATS_ACTIVE_WIDTH_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	active_width_max	Maximum width register.

FRAME_STATS_ACTIVE_WIDTH_SUM

FRAME_STATS_ACTIVE_WIDTH_SUM is the active width and register.

Offset Address	Register Name	Total Reset Value
0x20918	FRAME_STATS_ACTIVE_WIDTH_SONE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	active_width_sum	Active width sum register.

FRAME_STATS_ACTIVE_WIDTH_NUM

FRAME_STATS_ACTIVE_WIDTH_NUM is the active width register.

Offset Address	Register Name	Total Reset Value
0x2091C	FRAME_STATS_ACTIVE_WIDTH_NONE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	active_width_num	Active width.

FRAME_STATS_ACTIVE_HEIGHT_MIN

FRAME_STATS_ACTIVE_HEIGHT_MIN is the minimum height register.

Offset Address	Register Name	Total Reset Value
0x20920	FRAME_STATS_ACTIVE_HEIGHT_MIN	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	active_height_min	
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	

Bits	Access Name		Description
[31:0]	RO	active_height_min	minimum height register.

FRAME_STATS_ACTIVE_HEIGHT_MAX

FRAME_STATS_ACTIVE_HEIGHT_MAX is the maximum height register.

Offset Address	Register Name	Total Reset Value
0x20924	FRAME_STATS_ACTIVE_HEIGHT_MAX	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	active_height_max	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	active_height_max	Maximum height register.

FRAME_STATS_ACTIVE_HEIGHT_SUM

FRAME_STATS_ACTIVE_HEIGHT_SUM is the active height sum register.

Offset Address	Register Name	Total Reset Value
0x20928	FRAME_STATS_ACTIVE_HEIGHT_SONE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	active_height_sum	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	active_height_sum	Active height sum register.

FRAME_STATS_ACTIVE_HEIGHT_NUM

FRAME_STATS_ACTIVE_HEIGHT_NUM is the active height register.

Offset Address	Register Name	Total Reset Value
0x2092C	FRAME_STATS_ACTIVE_HEIGHT_NONE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	active_height_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	active_height_num	Active height register.

FRAME_STATS_HBLANK_MIN

FRAME_STATS_HBLANK_MIN is the minimum horizontal blanking.

Offset Address	Register Name	Total Reset Value
0x20930	FRAME_STATS_HBLANK_MIN	0xFFFF_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hblank_min
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:0]	RO	hblank_min	minimum horizontal blanking.

FRAME_STATS_HBLANK_MAX

FRAME_STATS_HBLANK_MAX is the maximum horizontal blanking.

Offset Address	Register Name	Total Reset Value
0x20934	FRAME_STATS_HBLANK_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	hblank_max maximum horizontal blanking.

FRAME_STATS_HBLANK_SUM

FRAME_STATS_HBLANK_SUM is the horizontal blanking sum register.

Offset Address	Register Name	Total Reset Value
0x20938	FRAME_STATS_HBLANK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	hblank_sum Horizontal blanking sum register.

FRAME_STATS_HBLANK_NUM

FRAME_STATS_HBLANK_NUM is the horizontal blanking register.

Offset Address	Register Name	Total Reset Value
0x2093C	FRAME_STATS_HBLANK_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	hblank_num Horizontal blanking register.

FRAME_STATS_VBLANK_MIN

FRAME_STATS_VBLANK_MIN is the minimum vertical blanking.

Offset Address	Register Name	Total Reset Value
0x20940	FRAME_STATS_VBLANK_MIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_min																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access Name	Description
[31:0]	RO	vblank_min minimum vertical blanking.

FRAME_STATS_VBLANK_MAX

FRAME_STATS_VBLANK_MAX is the maximum vertical blanking.

Offset Address	Register Name	Total Reset Value
0x20944	FRAME_STATS_VBLANK_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	vblank_max maximum vertical blanking.

FRAME_STATS_VBLANK_SUM

FRAME_STATS_VBLANK_SUM is the vertical blanking sum register.

Offset Address	Register Name	Total Reset Value
0x20948	FRAME_STATS_VBLANK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	vblank_sum Vertical blanking sum register.

FRAME_STATS_VBLANK_NUM

FRAME_STATS_VBLANK_NUM is the vertical blanking register.

Offset Address	Register Name	Total Reset Value
0x2094C	FRAME_STATS_VBLANK_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	vblank_num	Vertical blanking register.

NOISE_PROFILE_WDR_4

NOISE_PROFILE_WDR_4 is WDR 4 noise offset.

Offset Address	Register Name	Total Reset Value
0x21004	NOISE_PROFILE_WDR_4	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														long_noise_offset	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	long_noise_offset	Noise offset, format is unsigned 5.4bit floating point number.

NOISE_PROFILE_WDR_3

NOISE_PROFILE_WDR_3 is WDR 3 noise offset.

Offset Address	Register Name	Total Reset Value
0x21014	NOISE_PROFILE_WDR_3	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														med1_noise_offset	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	med1_noise_offset	Noise offset, format is unsigned 5.4bit floating point number.

NOISE_PROFILE_WDR_2

NOISE_PROFILE_WDR_2 is WDR 2 noise offset.

Offset Address	Register Name	Total Reset Value
0x21024	NOISE_PROFILE_WDR_2	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved med2_noise_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	med2_noise_offset	Noise offset, format is unsigned 5.4bit floating point number.

NOISE_PROFILE_WDR_1

NOISE_PROFILE_WDR_1 is WDR 1 noise offset.

Offset Address	Register Name	Total Reset Value
0x21034	NOISE_PROFILE_WDR_1	0x0000_0040

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved short_noise_offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	short_noise_offset	Noise offset, the format is unsigned 5.4bit floating point number.

NOISE_PROFILE_FRAME_STITCH_LUT_1

NOISE_PROFILE_FRAME_STITCH_LUT_1 is FRAME_STITCH noise profile table 1.

Offset Address	Register Name	Total Reset Value
0x21200~0x2127C	NOISE_PROFILE_FRAME_STITCH_LUT_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_FRAME_STITCH_LUT_2

NOISE_PROFILE_FRAME_STITCH_LUT_2 is FRAME_STITCH noise profile table 2.

Offset Address	Register Name	Total Reset Value
0x21280~0x212FC	NOISE_PROFILE_FRAME_STITCH_LUT_2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_FRAME_STITCH_LUT_3

NOISE_PROFILE_FRAME_STITCH_LUT_3 is FRAME_STITCH noise profile table 3.

Offset Address	Register Name	Total Reset Value
0x21300~0x2137C	NOISE_PROFILE_FRAME_STITCH_LUT_3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_FRAME_STITCH_LUT_4

NOISE_PROFILE_FRAME_STITCH_LUT_4 is FRAME_STITCH noise profile table 4.

Offset Address	Register Name	Total Reset Value
0x21380~0x213FC	NOISE_PROFILE_FRAME_STITCH_LUT_4	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RW weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW weight_lut_0	Noise distribution weight 0, calculated during calibration.

DNR_SHADING

DNR_SHADING is Radial LUT0.

Offset Address	Register Name	Total Reset Value
0x21540~0x2155C	DNR_SHADING	0x1010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rm_shading_lut_3								rm_shading_lut_2								rm_shading_lut_1								rm_shading_lut_0							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rm_shading_lut_3	Radial LUT data3, 33 in total.
[23:16]	RW	rm_shading_lut_2	Radial LUT data2, 33 in total.
[15:8]	RW	rm_shading_lut_1	Radial LUT data1, 33 in total.
[7:0]	RW	rm_shading_lut_0	Radial LUT data0, 33 in total.

DNR_SHADING_LAST

DNR_SHADING_LAST is Radial LUT1.

Offset Address	Register Name	Total Reset Value
0x21560	DNR_SHADING_LAST	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rm_shading_lut_32	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	rm_shading_lut_32	Radial LUT data32, 33 in total, the last one.

NOISE_PROFILE_RAW_FRONTEND_LUT_1

NOISE_PROFILE_RAW_FRONTEND_LUT_1 is RAW_FRONTEND noise profile table 1.

Offset Address	Register Name	Total Reset Value
0x21580~0x215FC	NOISE_PROFILE_RAW_FRONTEND_LUT_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_RAW_FRONTEND_LUT_2

NOISE_PROFILE_RAW_FRONTEND_LUT_2 is RAW_FRONTEND noise profile table 2.

Offset Address	Register Name	Total Reset Value
0x21600~0x2167C	NOISE_PROFILE_RAW_FRONTEND_LUT_2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_RAW_FRONTEND_LUT_3

NOISE_PROFILE_RAW_FRONTEND_LUT_3 is RAW_FRONTEND noise profile table 3.

Offset Address	Register Name	Total Reset Value
0x21680~0x216FC	NOISE_PROFILE_RAW_FRONTEND_LUT_3	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_RAW_FRONTEND_LUT_4

NOISE_PROFILE_RAW_FRONTEND_LUT_4 is RAW_FRONTEND noise profile table 4.

Offset Address	Register Name	Total Reset Value
0x21700~0x2177C	NOISE_PROFILE_RAW_FRONTEND_LUT_4	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weight_lut_3	weight_lut_2	weight_lut_1	weight_lut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_LUT

NOISE_PROFILE_LUT is the DNR noise profile table.

Offset Address	Register Name	Total Reset Value
0x21800~0x2187C	NOISE_PROFILE_LUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weightlut_3	weightlut_2	weightlut_1	weightlut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3	DNR Noise distribution weight 3, calculated during calibration.
[23:16]	RW	weightlut_2	DNR Noise distribution weight 2, calculated during calibration.
[15:8]	RW	weightlut_1	DNR Noise distribution weight 1, calculated during calibration.
[7:0]	RW	weightlut_0	DNR Noise distribution weight 0, calculated during calibration.

NOISE_PROFILE_DEMOSAIC_LUT

NOISE_PROFILE_DEMOSAIC_LUT is the DEMOSAIC noise profile.

Offset Address	Register Name	Total Reset Value
0x21880~0x218FC	NOISE_PROFILE_DEMOSAIC_LUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	weightlut_3	weightlut_2	weightlut_1	weightlut_0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3	DEMOSAIC Noise distribution weight 3.
[23:16]	RW	weightlut_2	DEMOSAIC Noise distribution weight 2.
[15:8]	RW	weightlut_1	DEMOSAIC Noise distribution weight 1.
[7:0]	RW	weightlut_0	DEMOSAIC Noise distribution with weight 0.

AEXP_WEIGHT

AEXP_WEIGHT is AE block weight.

Offset Address	Register Name	Total Reset Value
0x21900~0x219F8	AEXP_WEIGHT	0x0F0F_0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aexp_weight0_ 3				reserved				aexp_weight0_ 2				reserved				aexp_weight0_ 1				reserved				aexp_weight0_ 0			
Reset	0	0	0	0	1	1	1	1	0	0	0	0	1	1			1	0	0	0	0	1			1	1	0	0	0	0	1	

Bits	Access Name	Description
[31:28]	RO reserved	reserve.
[27:24]	RW aexp_weight0_3	AE block weight 0_3.
[23:20]	RO reserved	reserve.
[19:16]	RW aexp_weight0_2	AE block weight 0_2.
[15:12]	RO reserved	reserve.
[11:8]	RW aexp_weight0_1	AE block weight 0_1.
[7:4]	RO reserved	reserve.
[3:0]	RW aexp_weight0_0	AE block weight 0_0.

AEXP_WEIGHT_LAST

AEXP_WEIGHT_LAST is the last block weight of AE.

Offset Address	Register Name	Total Reset Value
0x219FC	AEXP_WEIGHT_LAST	0x000F_0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aexp_weight16 _14				reserved				aexp_weight16 _13				reserved				aexp_weight16 _12			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1			1	0	0	0	0	1			1	1	0	0	0	0	1	

Bits	Access Name	Description
[31:20]	RO reserved	reserve.
[19:16]	RW aexp_weight16_14	AE block weight 16_14.
[15:12]	RO reserved	reserve.
[11:8]	RW aexp_weight16_13	AE block weight 16_13.
[7:4]	RO reserved	reserve.
[3:0]	RW aexp_weight16_12	AE block weight 16_12.

AWB_WEIGHT

AWB_WEIGHT is AWB block weight.

Offset Address	Register Name	Total Reset Value
0x21B00~0x21EFC	AWB_WEIGHT	0x0F0F_0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				awb_weight0_3				reserved				awb_weight0_2				reserved				awb_weight0_1				reserved				awb_weight0_0			
Reset	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	awb_weight0_3	AWB block weight 0_3.
[23:20]	RO	reserved	reserve.
[19:16]	RW	awb_weight0_2	AWB block weight 0_2.
[15:12]	RO	reserved	reserve.
[11:8]	RW	awb_weight0_1	AWB block weight 0_1.
[7:4]	RO	reserved	reserve.
[3:0]	RW	awb_weight0_0	AWB block weight 0_0.

GAMMA_FE0_MEM0

GAMMA_FE0_MEM0 is the GAMMA_FE0 Bank0 lookup table.

Offset Address	Register Name	Total Reset Value
0x22800~0x22880	GAMMA_FE0_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								date0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_FE0 Bank0 lookup table.

GAMMA_FE0_MEM1

GAMMA_FE0_MEM1 is the lookup table for GAMMA_FE0 Bank1.

Offset Address	Register Name	Total Reset Value
0x22900~0x22980	GAMMA_FE0_MEM1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_FE0 Bank1 lookup table.

GAMMA_FE1_MEM0

GAMMA_FE1_MEM0 is the GAMMA_FE1 Bank0 lookup table.

Offset Address	Register Name	Total Reset Value
0x23000~0x23400	GAMMA_FE1_MEM0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_FE1 Bank0 lookup table.

GAMMA_FE1_MEM1

GAMMA_FE1_MEM1 is the GAMMA_FE1 Bank1 lookup table.

Offset Address	Register Name	Total Reset Value
0x23800~0x23C00	GAMMA_FE1_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				date0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_FE1 Bank1 lookup table.

GAMMA_BE0_MEM0

GAMMA_BE0_MEM0 is the GAMMA_BE0 Bank0 lookup table.

Offset Address	Register Name	Total Reset Value
0x24800~0x24880	GAMMA_BE0_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				date0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_BE0 Bank0 lookup table.

GAMMA_BE0_MEM1

GAMMA_BE0_MEM1 is the lookup table for GAMMA_BE0 Bank1.

Offset Address	Register Name	Total Reset Value
0x24900~0x24980	GAMMA_BE0_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				date0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_BE0 Bank1 lookup table.

GAMMA_BE1_MEM0

GAMMA_BE1_MEM0 is the GAMMA_BE1 Bank0 lookup table.

Offset Address	Register Name	Total Reset Value
0x25000~0x25400	GAMMA_BE1_MEM0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_BE1 Bank0 lookup table.

GAMMA_BE1_MEM1

GAMMA_BE1_MEM1 is the GAMMA_BE1 Bank1 lookup table.

Offset Address	Register Name	Total Reset Value
0x25800~0x25C00	GAMMA_BE1_MEM1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	GAMMA_BE1 Bank1 lookup table.

RADIAL_SHADING_MEM_R

RADIAL_SHADING_MEM_R is the RADIAL_SHADING R component lookup table.

Offset Address	Register Name	Total Reset Value
0x26000~0x26200	RADIAL_SHADING_MEM_R	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														date0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	data0	RADIAL_SHADING R component lookup table.

RADIAL_SHADING_MEM_G

RADIAL_SHADING_MEM_G is the RADIAL_SHADING G component lookup table.

Offset Address	Register Name	Total Reset Value
0x26400~0x26600	RADIAL_SHADING_MEM_G	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														date0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	data0	RADIAL_SHADING G component lookup table.

RADIAL_SHADING_MEM_B

RADIAL_SHADING_MEM_B is the RADIAL_SHADING B component lookup table.

Offset Address	Register Name	Total Reset Value
0x26800~0x26A00	RADIAL_SHADING_MEM_B	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														date0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	data0	RADIAL_SHADING B component lookup table.

METERING_MEM

METERING_MEM is AE stat, AE sum, AWB stat, AWB sum statistical information.

Offset Address	Register Name	Total Reset Value
0x28000~0x2DFFC	METERING_MEM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	date0	AE stat, AE sum, AWB stat, AWB sum statistics.

DEFECT_PIXEL_MEM

DEFECT_PIXEL_MEM is the table of static defect pixels.

Offset Address	Register Name	Total Reset Value
0x30000~0x33FFC	DEFECT_PIXEL_MEM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:25] RO	reserved	reserve.
[24:0] RW	data0	static defect pixels bad pixel table.

HISTOGRAM1_MEM

HISTOGRAM1_MEM is histogram statistics 1.

Offset Address	Register Name	Total Reset Value
0x34000~0x34FFC	HISTOGRAM1_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	date0	Histogram statistics.

HISTOGRAM2_MEM

HISTOGRAM2_MEM is histogram statistics 2.

Offset Address	Register Name	Total Reset Value
0x35000~0x353FC	HISTOGRAM2_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	date0	Histogram statistics.

HISTOGRAM3_MEM

HISTOGRAM3_MEM is histogram statistics 3.

Offset Address	Register Name	Total Reset Value
0x35400~0x357FC	HISTOGRAM3_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	date0	Histogram statistics.

HISTOGRAM4_MEM

HISTOGRAM4_MEM is histogram statistics 4.

Offset Address	Register Name	Total Reset Value
0x35800~0x35BFC	HISTOGRAM4_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	date0	Histogram statistics.

GAMMA_RGB_MEM0

GAMMA_RGB_MEM0 is the GAMMA_RGB Bank0 lookup table.

Offset Address	Register Name	Total Reset Value
0x37000~0x37400	GAMMA_RGB_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				date0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	data0	GAMMA_RGB Bank0 257 node lookup table.

GAMMA_RGB_MEM1

GAMMA_RGB_MEM1 is the GAMMA_RGB Bank1 lookup table.

Offset Address	Register Name	Total Reset Value
0x37800~0x37C00	GAMMA_RGB_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				date0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	data0	GAMMA_RGB Bank1 257 node lookup table.

DRC_FWD_MEM

DRC_FWD_MEM is the DRC_FWD table.

Offset Address	Register Name	Total Reset Value
0x38000~0x38200	DRC_FWD_MEM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	DRC_FWD table.

DRC_REV_MEM

DRC_REV_MEM is the DRC_REV table.

Offset Address	Register Name	Total Reset Value
0x38800~0x38A00	DRC_REV_MEM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / date0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:0]	RW	data0	DRC_REV table.

CMD_QUEUES

CMD_QUEUES is the CMD table.

Offset Address	Register Name	Total Reset Value
0x39000~0x393FC	CMD_QUEUES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data0	CMD table.

SHADING_MEM

SHADING_MEM for mesh shading table.

Offset Address	Register Name	Total Reset Value
0x3C000~0x3EFFC	SHADING_MEM	0x4040_4040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	date0																															
Reset	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	data0	mesh shading tableÿ

ISP_BE_FSTART_DELAY

ISP_BE_FSTART_DELAY is the ISP adjustable interrupt trigger time configuration.

Offset Address	Register Name	Total Reset Value
0x40094	ISP_BE_FSTART_DELAY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delay																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	delay	Adjustable interrupt trigger time configuration.

ISP_BE_USER_DEFINE0

ISP_BE_USER_DEFINE0 is user-defined register 0.

Offset Address	Register Name	Total Reset Value
0x400A0	ISP_BE_USER_DEFINE0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	user_define0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	user_define0	User-defined register 0.

ISP_BE_USER_DEFINE1

ISP_BE_USER_DEFINE1 is user-defined register 1.

Offset Address	Register Name	Total Reset Value
0x400A4	ISP_BE_USER_DEFINE1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	user_define1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	user_define1	User-defined register 1.

ISP_BE_INT

ISP_BE_INT is the ISP interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x400F0	ISP_BE_INT	0x0000_0000

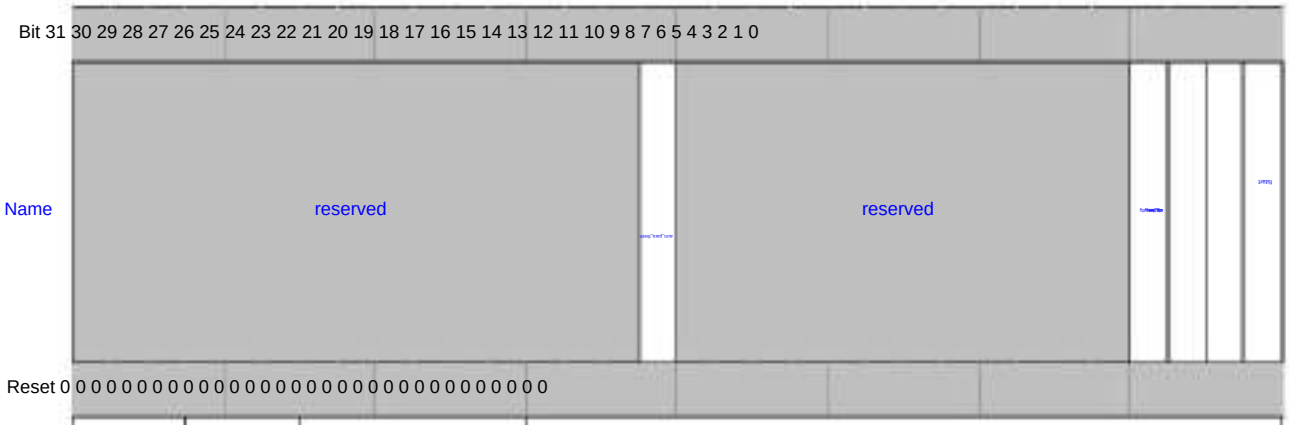
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	WC	acm_for_finish	ACM lookup table loading complete interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[15:4]	RO	reserved	reserve.
[3]	WC	fstart_delay	Trigger delay can be configured with interrupt. 0: no interrupt; 1: There is an interrupt.
[2]	WC	cfg_loss	Register configuration lost interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[1]	WC	update_cfg	Register update interrupt status, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[0]	WC	fstart	ISP frame start interrupt indication register, write 1 to clear. 0: no interrupt; 1: There is an interrupt.

ISP_BE_INT_MASK

ISP_BE_INT_MASK is the ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x400F8	ISP_BE_INT_MASK	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	acm_para_finish	ACM lookup table load complete interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[15:4]	RO	reserved	reserve.
[3]	RW	int_delay	Trigger delay can be configured with interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[2]	RW	cfg_loss	Register configuration lost interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[1]	RW	update_cfg	Register update interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.
[0]	RW	fstart	ISP start of frame interrupt enable. 0: mask interrupt; 1: Interrupts are enabled.

ISP_BE_CTRL_F

ISP_BE_CTRL_F is the ISP general update control register.

Offset Address	Register Name	Total Reset Value
0x401E0	ISP_BE_CTRL_F	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	rggb_cfg	RGGB order. 00ÿR Gr Gb Bÿ 01ÿGr RB Gbÿ 10ÿGb B R Grÿ 11ÿB Gb Gr Rÿ

ISP_BE_CTRL_I

ISP_BE_CTRL_I is the ISP immediate update control register.

Offset Address	Register Name	Total Reset Value
0x401E4	ISP_BE_CTRL_I	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update_mode	ISP register update mode. 0: update update; 1: frame update.

ISP_BE_TIMING_CFG

ISP_BE_TIMING_CFG is the output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x401E8	ISP_BE_TIMING_CFG	0x0000_0080

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	fix_timing
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:14]	RO	reserved	reserve.
[13:1]	RW	fix_timing	Manual timing parameter setting, set the length of the generated line blanking area.
[0]	RO	reserved	reserve.

ISP_BE_REG_UPDATE

ISP_BE_REG_UPDATE is a register update register.

Offset Address	Register Name	Total Reset Value
0x401EC	ISP_BE_REG_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	update	ISP update register, cleared to 0 automatically every frame.

ISP_CLIP_Y_CFG

ISP_CLIP_Y_CFG is the brightness clamp configuration register.

Offset Address	Register Name	Total Reset Value
0x40800	ISP_CLIP_Y_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	The brightness is clamped to the maximum value, and when the data bit width is less than 16 bits, the high bit is valid.
[15:0]	RW	min	Brightness clamps the minimum value, when the data bit width is less than 16bit, the high bit is valid.

ISP_CLIP_C_CFG

ISP_CLIP_C_CFG is the chroma clamp configuration register.

Offset Address	Register Name	Total Reset Value
0x40804	ISP_CLIP_C_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	The maximum value of chroma clamping, when the data bit width is less than 16bit, the high bit is valid.
[15:0]	RW	min	The minimum value of chroma clamping, when the data bit width is less than 16bit, the high bit is valid.

ISP_SKIP_Y_CFG

ISP_SKIP_Y_CFG is the Y component SKIP configuration register.

Offset Address	Register Name	Total Reset Value
0x40810	ISP_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	SKIP configuration.

ISP_SKIP_C_CFG

ISP_SKIP_C_CFG is the C component SKIP configuration register.

Offset Address	Register Name	Total Reset Value
0x40818	ISP_SKIP_C_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	SKIP configuration.

ISP_CROP_Y_CFG

ISP_CROP_Y_CFG is the Y component CROP enable register.

Offset Address	Register Name	Total Reset Value
0x40860	ISP_CROP_Y_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

ISP_CROP_Y_START

ISP_CROP_Y_START is the start position register of Y component CROP.

Offset Address	Register Name	Total Reset Value
0x40868	ISP_CROP_Y_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	y_start	—	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

ISP_CROP_Y_SIZE

ISP_CROP_Y_SIZE is the CROP size register for Y component.

Offset Address	Register Name	Total Reset Value
0x4086C	ISP_CROP_Y_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

ISP_CROP_C_CFG

ISP_CROP_C_CFG is the C component CROP enable register.

Offset Address	Register Name	Total Reset Value
0x40870	ISP_CROP_C_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

ISP_CROP_C_START

ISP_CROP_C_START is the C component CROP start position register.

Offset Address	Register Name	Total Reset Value
0x40878	ISP_CROP_C_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					y_start											reserved			x_start													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	y_start	The line number at which to start fetching the image.
[15:13]	RO	reserved	reserve.
[12:0]	RW	x_start	The pixel number at which to start fetching the image.

ISP_CROP_C_SIZE

ISP_CROP_C_SIZE is the C component CROP size setting register.

Offset Address	Register Name	Total Reset Value
0x4087C	ISP_CROP_C_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Get the width of the image (in pixels), the configuration value is the actual value minus 1.

ISP_Y_SUM0

ISP_Y_SUM0 is the brightness and low register of the input image.

Offset Address	Register Name	Total Reset Value
0x40880	ISP_Y_SUM0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sum	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	sum	Brightness and statistics, low 32bit.

ISP_Y_SUM1

ISP_Y_SUM1 is the brightness and high register of the input image.

Offset Address	Register Name	Total Reset Value
0x40884	ISP_Y_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	sum	Brightness and statistical information, high 32bit.

ISP_CSC_CFG

ISP_CSC_CFG is the CSC enable register.

Offset Address	Register Name	Total Reset Value
0x41500	ISP_CSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	and	CSC is enabled. 0: forbidden; 1: enable.

ISP_CSC_COEF0

ISP_CSC_COEF0 is CSC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x41510	ISP_CSC_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:17]	RW	coef01	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[16]	RO	reserved	reserve.
[15:1]	RW	coef00	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[0]	RO	reserved	reserve.

ISP_CSC_COEF1

ISP_CSC_COEF1 is CSC coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x41514	ISP_CSC_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:17]	RW	coef10	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[16]	RO	reserved	reserve.
[15:1]	RW	coef02	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[0]	RO	reserved	reserve.

ISP_CSC_COEF2

ISP_CSC_COEF2 is CSC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x41518	ISP_CSC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12																				—	coef11										—
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef12	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[16]	RO	reserved	reserve.
[15:1]	RW	coef11	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[0]	RO	reserved	reserve.

ISP_CSC_COEF3

ISP_CSC_COEF3 is CSC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x4151C	ISP_CSC_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21																				—	coef20										—
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef21	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[16]	RO	reserved	reserve.

[15:1] RW	coef20		CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[0]	RO	reserved	reserve.

ISP_CSC_COEF4

ISP_CSC_COEF4 is CSC coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x41520	ISP_CSC_COEF4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	coef22
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[16]	RO	reserved	reserve.
[15:1]	RW	coef22	CSC coefficient. Format (S5.10), signed number, 4bit integer, 10bit decimal.
[0]	RO	reserved	reserve.

ISP_CSC_IN_DC0

ISP_CSC_IN_DC0 is CSC input DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41530	ISP_CSC_IN_DC0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	in_dc1	reserved / in_dc0 / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	in_dc1	Enter the DC offset for the G component. signed integer.

[20:16] RO		reserved	reserve.
[15:5] RW	in_dc0		Enter the DC offset of the R component. signed integer.
[4:0] RO		reserved	reserve.

ISP_CSC_IN_DC1

ISP_CSC_IN_DC1 is CSC input DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41534	ISP_CSC_IN_DC1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Name	reserved	reserved	in_dc2	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:16]	RO	reserved	reserve.
[15:5]	RW	in_dc2	Outputs the DC offset of the B component. signed integer.
[4:0]	RO	reserved	reserve.

ISP_CSC_OUT_DC0

ISP_CSC_OUT_DC0 is CSC output DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41540	ISP_CSC_OUT_DC0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Name	out_dc1	reserved	out_dc0	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	out_dc1	Outputs the DC offset of the U component. signed integer.
[20:16]	RO	reserved	reserve.

[15:5]	RW	out_dc0	Outputs the DC offset of the Y component. signed integer.
[4:0]	RO	reserved	reserve.

ISP_CSC_OUT_DC1

ISP_CSC_OUT_DC1 is CSC output DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41544	ISP_CSC_OUT_DC1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	out_dc2	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:16]	RO	reserved	reserve.
[15:5]	RW	out_dc2	Outputs the DC offset of the V component. signed integer.
[4:0]	RO	reserved	reserve.

ISP_MCDS_CFG

ISP_MCDS_CFG is the MCDS control register.

Offset Address	Register Name	Total Reset Value
0x41800	ISP_MCDS_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.

[4] RW midf_en			MCDSILTER is enabled. 0: off; 1: enable.
[3] RW uv2c_mode			UV2C bypass mode. 0: Output U component data; 1: Output V component data.
[2] RW uv2c_en			UV2C enable, adjust internal two-component UV data to single-component C data. 0: off; 1: enable.
[1] RW vcds_en			Chroma vertical downsampling enabled. 0: off; 1: enable.
[0] RW hcds_en			Chroma level downsampling enabled. 0: off; 1: enable.

ISP_HCDS_SIZE

ISP_HCDS_SIZE is the chroma horizontal downsampling input size setting register.

Offset Address	Register Name	Total Reset Value
0x41814	ISP_HCDS_SIZE	0x077F_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																width_out								—						width_in			
Reset	0	0	0	0	0	1	1	1	0	1							1	1	1						1	0	0	0	0	0	1			
																										1	1	0	1	1	1	

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	width_out	Chroma horizontal downsampling output image U or V width of one line (in pixels), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width_in	Input the width of one row of image U or V (in pixels), and the configuration value is minus 1 from the actual value.

ISP_MIDF_SIZE

ISP_MIDF_SIZE is the median filter input image chroma width and height.

Offset Address	Register Name	Total Reset Value
0x4182C	ISP_MIDF_SIZE	0x0437_077F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	—	height	—	width
Reset	0 0 0 0 0 1 0 0 0 0 1	1 0 1	1 0 0 0 0 0 1	1 1 0 1 1 1

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	The image height (minus 1) after chroma vertical downsampling, such as 720 image height, with 719ÿ
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Image width (minus 1) after chroma vertical downsampling UV2C, such as 1280 image height, match 1279.

ISP_MCDS_PARA

ISP_MCDS_PARA is the fusion scale and shift of NR.

Offset Address	Register Name	Total Reset Value
0x41844	ISP_MCDS_PARA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
Name	—	midf_bldr	—	limit	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	midf_bldr	midf blendratio Unsigned 5bit data, value 0-16.
[23]	RO	reserved	reserve.
[22:16]	RW	limit	coring function, limit setting, configuration range 0-127.

[15:0] RO		reserved	reserve.

ISP_MCDS_SIZE

ISP_MCDS_SIZE is MCDS input image width and height.

Offset Address	Register Name	Total Reset Value
0x418F0	ISP_MCDS_SIZE	0x0437_077F

Bit	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0	0 0 0 1 0 0 0 0 1	1 0 1	1 0 0 0 0 0 1 1 1 0 1 1 1

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Input image height (minus 1), such as 1080P image height, match 1079.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Input image width (minus 1), such as 1080P image width, match 1919.

ISP_SHARPEN_CFG

ISP_SHARPEN_CFG is the SHARPEN control register.

Offset Address	Register Name	Total Reset Value
0x45200	ISP_SHARPEN_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	in
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	and	SHARPEN enabled. 0: forbidden; 1: enable.

ISP_SHARPEN_AMT

ISP_SHARPEN_AMT is the SHARPEN strength.

Offset Address	Register Name	Total Reset Value
0x45210	ISP_SHARPEN_AMT	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	edge_amt	reserved	sharp_amt
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	edge_amt	Edge enhancement strength (u,12.0). Unsigned number, 12bit integer, 0bit decimal. The representation of the registers below Sharpen is similar to this.
[15:12]	RO	reserved	reserve.
[11:0]	RW	sharp_amt	Detail enhancement strength (u,12.0).

ISP_SHARPEN_SHOOTAMT

ISP_SHARPEN_SHOOTAMT is the SHARPENshootAMT control.

Offset Address	Register Name	Total Reset Value
0x4521C	ISP_SHARPEN_SHOOTAMT	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	over_amt	reserved	under_amt
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	over_amt	Overshoot control coefficient (u,8.0).
[15:8]	RO	reserved	reserve.
[7:0]	RW	under_amt	undershoot control coefficient (u,8.0).

ISP_SHARPEN_EDGEJAG

ISP_SHARPEN_EDGEJAG is the sawtooth high frequency parameter.

Offset Address	Register Name	Total Reset Value
0x45224	ISP_SHARPEN_EDGEJAG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	edgejagmt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	edgejagamt	Sawtooth high frequency gain, 12-bit unsigned integer.

ISP_SHARPEN_OSHTJAG

ISP_SHARPEN_OSHTJAG is the sawtooth overshoot parameter.

Offset Address	Register Name	Total Reset Value
0x45228	ISP_SHARPEN_OSHTJAG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	oshtjagamt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	oshtjagamt	sawtooth overshoot gain, 8-bit unsigned integer.

ISP_SHARPEN_USHTJAG

ISP_SHARPEN_USHTJAG is the jagged undershoot parameter.

Offset Address	Register Name	Total Reset Value
0x4522C	ISP_SHARPEN_USHTJAG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	ushtjagamt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	ushtjagamt	jagged undershoot gain, 8-bit unsigned integer.

ISP_SHARPEN_MID0

ISP_SHARPEN_MID0 is the SHARPEN IF filter coefficient.

Offset Address	Register Name	Total Reset Value
0x45230	ISP_SHARPEN_MID0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	mid_tmp02	one_tmp01	one_tmp00
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	mid_tmp02	IF filter coefficient 02(s,8.0). Signed number, 8bit integer, 0bit decimal. The representation of the registers below Sharpen is similar to this.
[15:8]	RW	mid_tmp01	IF filter coefficient 01(s,8.0).
[7:0]	RW	mid_tmp00	IF filter coefficient 00(s,8.0).

ISP_SHARPEN_MID1

ISP_SHARPEN_MID1 is the SHARPEN IF filter coefficient.

Offset Address	Register Name	Total Reset Value
0x45234	ISP_SHARPEN_MID1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	mid_tmp12	one_tmp11	one_tmp10
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	mid_tmp12	IF filter coefficient 12(s,8.0).
[15:8]	RW	mid_tmp11	IF filter coefficient 11(s,8.0).
[7:0]	RW	mid_tmp10	IF filter coefficient 10(s,8.0).

ISP_SHARPEN_MID2

ISP_SHARPEN_MID2 is SHARPEN intermediate frequency filter coefficient.

Offset Address	Register Name	Total Reset Value
0x45238	ISP_SHARPEN_MID2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	mid_tmp22	mid_tmp21	mid_tmp20
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	mid_tmp22	IF filter coefficient 22(s,8.0).
[15:8]	RW	mid_tmp21	IF filter coefficient 21(s,8.0).
[7:0]	RW	mid_tmp20	IF filter coefficient 20(s,8.0).

ISP_SHARPEN_LINETHD

ISP_SHARPEN_LINETHD is the SHARPEN line detection threshold.

Offset Address	Register Name	Total Reset Value
0x4523C	ISP_SHARPEN_LINETHD	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	line_thd2	reserved	line_thd1
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:16]	RW	line_thd2	Line detection threshold 2(u, 8.0).
[15:8]	RO	reserved	reserve.
[7:0]	RW	line_thd1	Line detection threshold 1(u, 8.0).

ISP_SHARPEN_THD2

ISP_SHARPEN_THD2 is the SHARPEN threshold 2.

Offset Address	Register Name	Total Reset Value
0x45240	ISP_SHARPEN_THD2	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	edge_thd2	reserved	sharp_thd2
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	edge_thd2	Edge enhancement threshold (u,10.0).
[15:10]	RO	reserved	reserve.
[9:0]	RW	sharp_thd2	Detail enhancement threshold (u,10.0).

ISP_SHARPEN_CTRL

ISP_SHARPEN_CTRL is the SHARPEN control.

Offset Address	Register Name	Total Reset Value
0x45244	ISP_SHARPEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											jagctrl	shtlumamod	shtvarctrl	lumactrl	enpixsel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	jagctrl	Sawtooth control switch register. 0: not used; 1: use.
[3]	RW	shtlumamod	Whether to use brightness control overshoot. 0: not used; 1: use.
[2]	RW	shtvarctrl	variance control. 0: off; 1: enable.
[1]	RW	lumactrl	Brightness control. 0: off; 1: enable.
[0]	RW	enpixsel	overshoot suppression. 0: select the original value; 1: Select field max/min.

ISP_SHARPEN_LUMATH

ISP_SHARPEN_LUMATH is the LUMATH parameter.

Offset Address	Register Name	Total Reset Value
0x45248	ISP_SHARPEN_LUMATH	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	lumath3	lumath2	lumath1	lumath0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	lumath3	Brightness controls Th3.
[23:16]	RW	lumath2	Brightness controls Th2.
[15:8]	RW	lumath1	Brightness controls Th1.
[7:0]	RW	lumath0	Brightness controls Th0.

ISP_SHARPEN_LUMAWGT

ISP_SHARPEN_LUMAWGT is the LUMAWgt parameter.

Offset Address	Register Name	Total Reset Value
0x4524C	ISP_SHARPEN_LUMAWGT	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	lumawgt3	lumawgt2	1	0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	lumawgt3	Brightness weight Wgt3.
[23:16]	RW	lumawgt2	Brightness weight Wgt2.
[15:8]	RW	lumawgt1	Brightness weight Wgt1.
[7:0]	RW	lumawgt0	Brightness weight Wgt0.

ISP_SHARPEN_OSHTVARTH

ISP_SHARPEN_OSHTVARTH is the variance threshold parameter 0.

Offset Address	Register Name	Total Reset Value
0x45258	ISP_SHARPEN_OSHTVARTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	overvarth1 reserved overvarth0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	overvarth1	overshoot variance threshold 1.
[15:10]	RO	reserved	reserve.
[9:0]	RW	overvarth0	overshoot variance threshold 0.

ISP_SHARPEN_OSHTVAR

ISP_SHARPEN_OSHTVAR is the overshoot variance parameter 0.

Offset Address	Register Name	Total Reset Value
0x4525C	ISP_SHARPEN_OSHTVAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	overvaramt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	overvarams	overshoot variance gain.

ISP_SHARPEN_USHTVARTH

ISP_SHARPEN_USHTVARTH is the variance threshold parameter 1.

Offset Address	Register Name	Total Reset Value
0x45260	ISP_SHARPEN_USHTVARTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	undervarth1	reserved	undervarth0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	undervarth1	Undershoot variance threshold 1.
[15:10]	RO	reserved	reserve.
[9:0]	RW	undervarth0	Undershoot variance threshold 0.

ISP_SHARPEN_USHTVAR

ISP_SHARPEN_USHTVAR is the overshoot variance parameter 1.

Offset Address	Register Name	Total Reset Value
0x45264	ISP_SHARPEN_USHTVAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	under heat
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	undervaramt	undershoot variance gain.

ISP_SHARPEN_OSHTLUMA

ISP_SHARPEN_OSHTLUMA is the overshoot brightness parameter 0.

Offset Address	Register Name	Total Reset Value
0x45268	ISP_SHARPEN_OSHTLUMA	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	overlumawgt1	overlumawgt0	overlumath1	overlumath0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	overlumawgt1	Luma weight 1.
[23:16]	RW	overlumawgt0	Luma weight 0.
[15:8]	RW	overlumath1	Brightness threshold 1.
[7:0]	RW	overlumath0	Brightness threshold 0.

ISP_SHARPEN_USHTLUMA

ISP_SHARPEN_USHTLUMA is overshoot brightness parameter 1.

Offset Address	Register Name	Total Reset Value
0x4526C	ISP_SHARPEN_USHTLUMA	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	underlumawgt1	underlumawgt0	underlumath1	underlumath0
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	underlumawgt1	Luma weight 1.
[23:16]	RW	underlumawgt0	Luma weight 0.
[15:8]	RW	underlumath1	Luminance threshold 1.
[7:0]	RW	underlumath0	Brightness threshold 0.

ISP_SHARPEN_SHIFT

ISP_SHARPEN_SHIFT is the SHIFT parameter.

Offset Address	Register Name	Total Reset Value
0x45274	ISP_SHARPEN_SHIFT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5	4 3 2 1 0
Name	reserved	limit	maxshift	minshift
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	reserve.
[19:16]	RW	limit	The limit of the coring function.
[15:8]	RW	maxshift	The field's maximum offset.
[7:0]	RW	minshift	The smallest offset in the field.

ISP_SHARPEN_SIZE

ISP_SHARPEN_SIZE is the width and height of the SHARPEN image.

Offset Address	Register Name	Total Reset Value
0x452F0	ISP_SHARPEN_SIZE	0x0437_077F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0 0 0 1 0 0 0 0 1	1 0 1	1 0 0 0 0 0 1	1 1 0 1 1 1

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Image height (minus 1), such as 1080P image height, match 1079.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Image width (minus 1), such as 1080P image width, match 1919.

ISP_DEHAZE_CFG

ISP_DEHAZE_CFG is the DEHAZE enable register.

Offset Address	Register Name	Total Reset Value
0x46200	ISP_DEHAZE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	and	dehaze enabled. 0: forbidden; 1: enable.

ISP_DEHAZE_PRE_UPDATE

ISP_DEHAZE_PRE_UPDATE Updates registers for DEHAZE statistics.

Offset Address	Register Name	Total Reset Value
0x46210	ISP_DEHAZE_PRE_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	pre_update	The dehaze statistics configuration update register is automatically cleared to 0 every frame.

ISP_DEHAZE_BLK_SIZE

ISP_DEHAZE_BLK_SIZE is the DEHAZE block size configuration register.

Offset Address	Register Name	Total Reset Value
0x46214	ISP_DEHAZE_BLK_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7	6 5 4 3 2 1 0
Name	reserved	block_sizeh	reserved	block_sizev
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:16]	RW	block_sizeh	The size of the horizontal window, minus 1 for allocation.
[15:9]	RO	reserved	reserve.
[8:0]	RW	block_sizev	Vertical window size, minus 1 for allocation.

ISP_DEHAZE_BLK_SUM

ISP_DEHAZE_BLK_SUM is the total number of DEHAZE blocks.

Offset Address	Register Name	Total Reset Value
0x46218	ISP_DEHAZE_BLK_SUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7	6 5 4 3 2 1 0
Name	reserved			block_sum
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:0]	RW	block_sum	The total number of dehaze blocks. The configuration value is: the number of horizontal windows x (the number of vertical windows 1)

ISP_DEHAZE_DC_SIZE

ISP_DEHAZE_DC_SIZE is the configuration register for the number of DEHAZE bilinear interpolation points.

Offset Address	Register Name	Total Reset Value
0x4621C	ISP_DEHAZE_DC_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	dc_numh	dc_numv
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:5]	RW	dc_numh	The number of points in the horizontal direction of bilinear interpolation, minus 1 to match. Configured as the number of horizontal windows -1.
[4:0]	RW	dc_numv	The number of points in the vertical direction of bilinear interpolation, minus 1 to match. The configuration is the number of vertical windows -1.

ISP_DEHAZE_X

ISP_DEHAZE_X is the configuration register for the horizontal phase difference between the pixels of DEHAZE enlarged image.

Offset Address	Register Name	Total Reset Value
0x46220	ISP_DEHAZE_X	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	phase_x
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	phase_x	Magnifies the horizontal phase difference between image pixels. Configured as horizontal window size*(1<<22). unsigned integer.

ISP_DEHAZE_Y

ISP_DEHAZE_Y is the configuration register for the vertical phase difference between the pixels of DEHAZE enlarged image.

Offset Address	Register Name	Total Reset Value
0x46224	ISP_DEHAZE_Y	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	phase_y
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	phase_y	Magnifies the vertical phase difference between image pixels. Configured as horizontal window size*(1<<22). unsigned integer.

ISP_DEHAZE_STAT_MODE

ISP_DEHAZE_STAT_MODE is the DEHAZE statistical module control register.

Offset Address	Register Name	Total Reset Value
0x46228	ISP_DEHAZE_STAT_MODE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	~~
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	max_mode	Maximum statistical control. 0: Perform mean filtering on RGB first, and then count the RGB components corresponding to the maximum value of RGB sum in each window; 1: Count the RGB components corresponding to the maximum value of the RGB sum in each window.

ISP_DEHAZE_NEG_MODE

ISP_DEHAZE_NEG_MODE is the DEHAZE negation processing control register.

Offset Address	Register Name	Total Reset Value
0x4622C	ISP_DEHAZE_NEG_MODE	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	neg_mode	Inverts the processing mode control. 0: normal processing mode; 1: Negate the processing mode.

ISP_DEHAZE_AIR

ISP_DEHAZE_AIR is the DEHAZE air light configuration register.

Offset Address	Register Name	Total Reset Value
0x46230	ISP_DEHAZE_AIR	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: — | air_r | air_g | air_b

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:20]	RW	air_r	Atmospheric light A corresponding to the R channel.
[19:10]	RW	air_g	Atmospheric light A corresponding to the G channel.
[9:0]	RW	air_b	Atmospheric light A corresponding to channel B.

ISP_DEHAZE_THLD

ISP_DEHAZE_THLD is the T threshold coefficient configuration register for DEHAZE.

Offset Address	Register Name	Total Reset Value
0x46234	ISP_DEHAZE_THLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved		thld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	thld	Threshold coefficient for T. unsigned integer.

ISP_DEHAZE_GSTRTH

ISP_DEHAZE_GSTRTH is the global strength coefficient of DEHAZE

Offset Address	Register Name	Total Reset Value
0x46238	ISP_DEHAZE_GSTRTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved		gstrth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	gstrth	Calculation coefficient for G. unsigned integer.

ISP_DEHAZE_BLTHLD

ISP_DEHAZE_BLTHLD is the configuration register for DEHAZE minimum filtering threshold coefficient.

Offset Address	Register Name	Total Reset Value
0x4623C	ISP_DEHAZE_BLTHLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Name	reserved		blthld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.

[9:0] RW	blthld		Minimum filter threshold coefficient. unsigned integer.

ISP_DEHAZE_STR_LUT_UPDATE

ISP_DEHAZE_STR_LUT_UPDATE update register for DEHAZE strength table

Offset Address	Register Name	Total Reset Value
0x46240	ISP_DEHAZE_STR_LUT_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RW	reserved	reserve.
[0]	RW	str_lut_update	The dehaze intensity meter configuration update register is automatically cleared to 0 every frame.

ISP_DEHAZE_MINSTAT_WADDR

ISP_DEHAZE_MINSTAT_WADDR Write address register for DEHAZE minimum statistics.

Offset Address	Register Name	Total Reset Value
0x46280	ISP_DEHAZE_MINSTAT_WADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	minstat_waddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	minstat_waddr	Dehaze minimum statistical information write address, range [0-511].

ISP_DEHAZE_MINSTAT_WDATA

ISP_DEHAZE_MINSTAT_WDATA Write data register for DEHAZE minimum statistics.

Offset Address	Register Name	Total Reset Value
0x46284	ISP_DEHAZE_MINSTAT_WDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	minstat_wdata_h	reserved	minstat_wdata_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	minstat_wdata_h	Dehaze minimum statistical information write data, the ID of the block with the larger ID among the two blocks being operated.
[15:10]	RO	reserved	reserve.
[9:0]	RW	minstat_wdata_l	Dehaze minimum statistic information write data, the ID of the block with the smaller ID among the two blocks being operated.

ISP_DEHAZE_MINSTAT_RADDR

ISP_DEHAZE_MINSTAT_RADDR is the DEHAZE minimum statistical information read address register.

Offset Address	Register Name	Total Reset Value
0x46288	ISP_DEHAZE_MINSTAT_RADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	minstat_rowdr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	reserve.
[8:0]	RW	minstat_raddr	The read address of dehaze minimum statistical information, range [0-511].

ISP_DEHAZE_MINSTAT_RDATA

ISP_DEHAZE_MINSTAT_RDATA Read data register for DEHAZE minimum statistics.

Offset Address	Register Name	Total Reset Value
0x4628C	ISP_DEHAZE_MINSTAT_RDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	minstat_rdata_h	reserved	minstat_rdata_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	minstat_rdata_h	Dehaze minimum value statistical information read data, the ID of the block with the larger ID among the two blocks being operated.
[15:10]	RO	reserved	reserve.
[9:0]	RO	minstat_rdata_l	Dehaze minimum statistic information read data, the ID of the block with the smaller ID among the two blocks being operated.

ISP_DEHAZE_MAXSTAT_WADDR

ISP_DEHAZE_MAXSTAT_WADDR Write address register for DEHAZE maximum statistics.

Offset Address	Register Name	Total Reset Value
0x46290	ISP_DEHAZE_MAXSTAT_WADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	maxstat_waddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	maxstat_waddr	Dehaze maximum statistical information write address register, range [0-1023].

ISP_DEHAZE_MAXSTAT_WDATA

ISP_DEHAZE_MAXSTAT_WDATA Write data register for DEHAZE maximum statistics.

Offset Address	Register Name	Total Reset Value
0x46294	ISP_DEHAZE_MAXSTAT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—																															
	maxstat_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:0]	RW	maxstat_wdata	The dehaze maximum statistics are written to the data register.

ISP_DEHAZE_MAXSTAT_RADDR

ISP_DEHAZE_MAXSTAT_RADDR is the read address register for DEHAZE maximum statistics information.

Offset Address	Register Name	Total Reset Value
0x46298	ISP_DEHAZE_MAXSTAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						maxstat_raddr									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	maxstat_raddr	dehaze maximum statistical information read address register, range [0-1023].

ISP_DEHAZE_MAXSTAT_RDATA

ISP_DEHAZE_MAXSTAT_RDATA Read data register for DEHAZE maximum statistics.

Offset Address	Register Name	Total Reset Value
0x4629C	ISP_DEHAZE_MAXSTAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	maxstat_rdata																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:30]	RO	reserved	reserve.
[29:0]	RO	maxstat_rdata	dehaze maximum statistical information read data register, R:[29:20]G:[19:10]B:[9:0].

ISP_DEHAZE_PRESTAT_WADDR

ISP_DEHAZE_PRESTAT_WADDR is the write address register for the minimum statistical information of the previous frame of DEHAZE.

Offset Address	Register Name	Total Reset Value
0x462A0	ISP_DEHAZE_PRESTAT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						rendered_waddr									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	prestat_waddr	dehaze Write address register of the minimum statistical information of the previous frame, range [0-511]

ISP_DEHAZE_PRESTAT_WDATA

ISP_DEHAZE_PRESTAT_WDATA Write data register for DEHAZE previous frame minimum statistics.

Offset Address	Register Name	Total Reset Value
0x462A4	ISP_DEHAZE_PRESTAT_WDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	prestat_wdata_h	reserved	borrowed_wdata_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:26]	RO	reserved	reserve.
[25:16]	RW	rendered_wdata_h	dehaze Write the data register of the minimum value statistics information of the previous frame, and the ID of the block with the larger ID among the two blocks being operated.
[15:10]	RO	reserved	reserve.
[9:0]	RW	rendered_wdata_l	Dehaze writes the data register of the minimum value statistics information of the previous frame, and the ID of the block with the smaller ID among the two blocks being operated.

ISP_DEHAZE_PRESTAT_RADDR

ISP_DEHAZE_PRESTAT_RADDR is the address register for reading the minimum statistical information of the previous frame of DEHAZE.

Offset Address	Register Name	Total Reset Value
0x462A8	ISP_DEHAZE_PRESTAT_RADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	provided_raddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	prestat_raddr	dehaze read address register of the minimum statistical information of the previous frame, range [0-511]

ISP_DEHAZE_PRESTAT_RDATA

ISP_DEHAZE_PRESTAT_RDATA is the read data register for the minimum statistical information of the previous frame of DEHAZE.

Offset Address	Register Name	Total Reset Value
0x462AC	ISP_DEHAZE_PRESTAT_RDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Name	reserved	prestat_rdata_h	reserved	loan_rdata_l
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:16]	RO	prestat_rdata_h	dehaze Read the data register of the minimum statistical information of the previous frame, and the ID of the block with the larger ID among the two blocks being operated.
[15:10]	RO	reserved	reserve.
[9:0]	RO	loan_rdata_l	dehaze Read the data register of the minimum statistical information of the previous frame, and the ID of the block with the smaller ID among the two blocks being operated.

ISP_DEHAZE_LUT_WADDR

ISP_DEHAZE_LUT_WADDR Write address register for DEHAZE strength LUT information.

Offset Address	Register Name	Total Reset Value
0x462B0	ISP_DEHAZE_LUT_WADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	lut_waddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	lut_waddr	Dehaze intensity LUT information write address register, range [0-255].

ISP_DEHAZE_LUT_WDATA

ISP_DEHAZE_LUT_WDATA Write data register for DEHAZE intensity LUT information.

Offset Address	Register Name	Total Reset Value
0x462B4	ISP_DEHAZE_LUT_WDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	lut_wdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	lut_wdata	Dehaze intensity LUT information write data register.

ISP_DEHAZE_LUT_RADDR

ISP_DEHAZE_LUT_RADDR is the read address register for DEHAZE intensity LUT information.

Offset Address	Register Name	Total Reset Value
0x462B8	ISP_DEHAZE_LUT_RADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	lut_raddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	lut_raddr	dehaze intensity LUT information read address register, range [0-255].

ISP_DEHAZE_LUT_RDATA

ISP_DEHAZE_LUT_RDATA Read data register for DEHAZE intensity LUT information.

Offset Address	Register Name	Total Reset Value
0x462BC	ISP_DEHAZE_LUT_RDATA	0x0000_0000

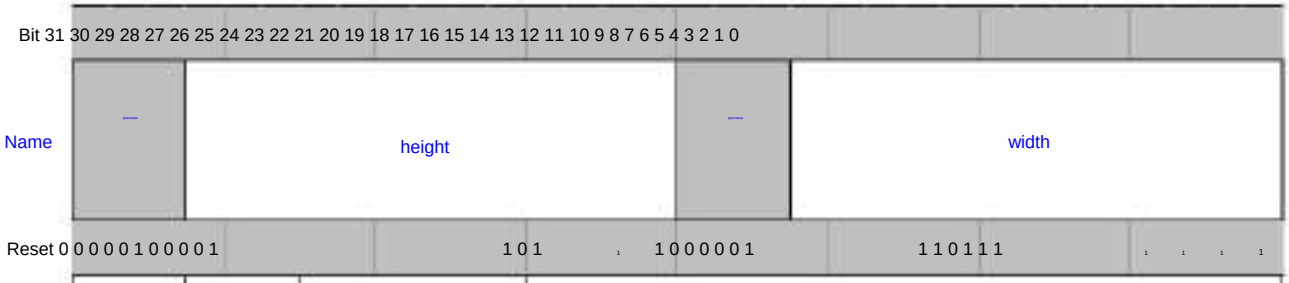
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	lut_rdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RO	lut_rdata	dehaze intensity LUT information read data register.

ISP_DEHAZE_SIZE

ISP_DEHAZE_SIZE is the width and height of DEHAZE image.

Offset Address	Register Name	Total Reset Value
0x462F0	ISP_DEHAZE_SIZE	0x0437_077F

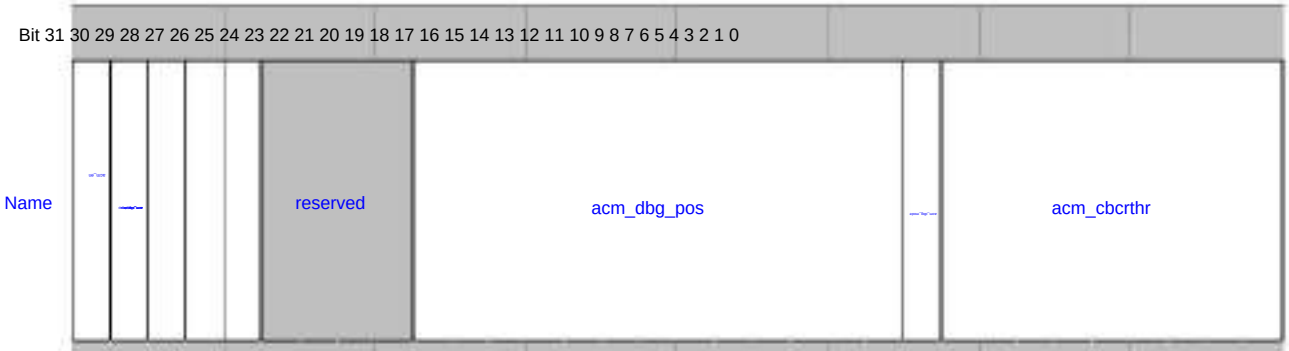


Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Window height (in row units), the configuration value is minus 1 from the actual value.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Window width (in pixels), the configuration value is the actual value minus 1.

ISP_ACM_CTRL

ISP_ACM_CTRL is the ACM control register.

Offset Address	Register Name	Total Reset Value
0x51400	ISP_ACM_CTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	acm_en	ACM module enable register. 0: ACM function off, data BYPASS output; 1: ACM function is enabled to realize brightness and contrast adjustment.

[30] RW	acm_dbg_en		acm debug enable. When acm_dbg_en is valid, the original image is displayed on the left side of the screen, and the abc processed image is displayed on the right side.
[29] RW	acm_stretch		Input pixel range limit register. 0ÿY 64-940ÿC 64-960ÿ 1ÿY 0-1023ÿC 0-1023ÿ
[28] RW	acm_cliprange		Output pixel range limit register. 0ÿY 64-940ÿC 64-960ÿ 1ÿY 0-1023ÿC 0-1023ÿ
[27] RW	acm_cliporwrap		Register for limiting mode of hue component value after ACM transformation. 0: If the hue component wrap-around is within the range of [0, 1023]; 1: Clip the hue component to the range of [0, 1023].
[26:23] RO		reserved	reserve.
[22:10] RW	acm_dbg_pos		acm debug location configuration.
[9] RW	acm_dbg_mode		ACM Debug mode. 0: The left is the original image, and the right is the image processed by ACM. 1: The left is the image processed by ACM, and the right is the original image.
[8:0] RW	acm_cbcrthr		ACM algorithm adjustment enable threshold value, 9bit unsigned number (0~255).

ISP_ACM_ADJ

ISP_ACM_ADJ is the amount of pixel change after ACM processing.

Offset Address	Register Name	Total Reset Value
0x51404	ISP_ACM_ADJ	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	—	acm_gain0	acm_gain1	acm_gain2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:20]	RW	acm_gain0	The control coefficient of the brightness (luma) adjustment range, the range is (0-512).
[19:10]	RW	acm_gain1	The control coefficient of hue (hue) adjustment range, the range is (0-512).
[9:0]	RW	acm_gain2	The control coefficient of the saturation (sat) adjustment range, the range is (0-512).

ISP_ACM_SIZE

ISP_ACM_SIZE handle image size register for ACM.

Offset Address	Register Name	Total Reset Value
0x51410	ISP_ACM_SIZE	0x0000_0000

Bit	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	—	height	—	width
Reset	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	The height of the image (in pixels), the configuration value is the actual value minus 1.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	The width of the image (in pixels), the configuration value is the actual value minus 1.

ISP_ACM_PARA_ADDR

ISP_ACM_PARA_ADDR is the load address register for ACM coefficient configuration.

Offset Address	Register Name	Total Reset Value
0x51414	ISP_ACM_PARA_ADDR	0x0000_0000

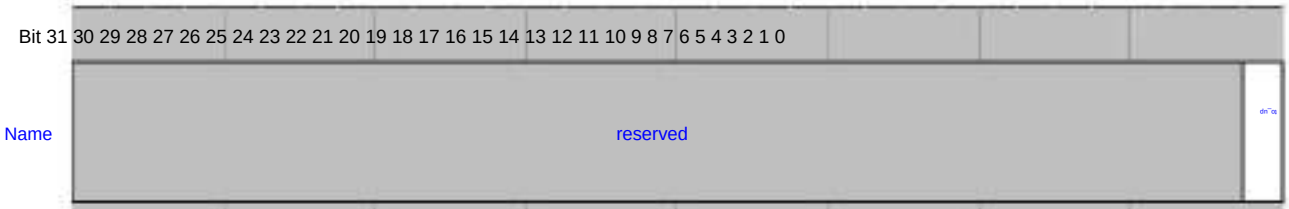
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	acm_para_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	acm_para_addr	ACM coefficient load address.

ISP_ACM_PARA_UP

ISP_ACM_PARA_UP configures the update register for the ACM coefficients.

Offset Address	Register Name	Total Reset Value
0x51420	ISP_ACM_PARA_UP	0x0000_0000

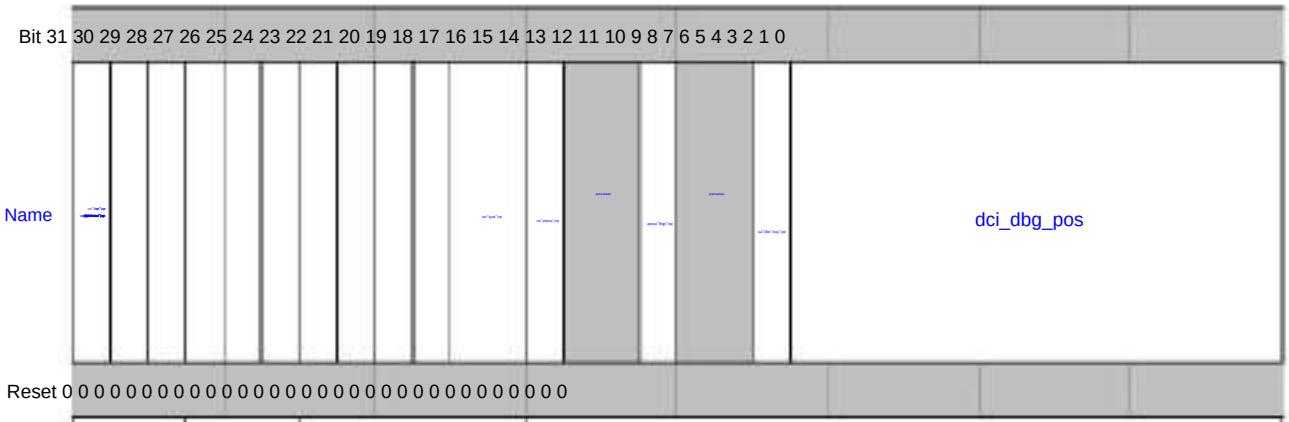


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	para_up	The parameter update register is automatically cleared to 0 every frame.

ISP_VPDCICTRL

ISP_VPDCICTRL is the DCI control register.

Offset Address	Register Name	Total Reset Value
0x51C00	ISP_VPDCICTRL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	dci_en	DCI enable control register. 0: DCI function off, data bypass output. 1: Enable the DCI function to realize brightness and contrast adjustment.
[30]	RW	dci_dbg_en	DCI demo mode enable signal. 0: disable; 1: The left side of the screen displays the original image, and the right side shows the DCI-processed image.
[29]	RW	dci_scene_flg	DCI scene switching enable signal. 0: Disable; 1: Enable.

[28] RW	dci_man_adj0		Curve 0 adjustment mode selection. 0: automatic mode, use the result of hardware calculation; 1: Manual mode, use the result of software configuration.
[27] RW	dci_man_adj1		Curve 1 adjustment mode selection. 0: Automatic mode, use the result of hardware calculation; 1: Manual mode, use the result of software configuration.
[26] RW	dci_man_adj2		Curve 2 Adjustment mode selection. 0: automatic mode, use the result of hardware calculation; 1: Manual mode, use the result of software configuration.
[25] RW	dci_cbcrcmp_en		DCI chroma compensation enable. 0: The DCI algorithm does not adjust the chroma component; 1: The DCI algorithm adjusts the chroma components.
[24] RW	dci_cbcrsta_en		Histogram statistics for selected signals. 0: Perform histogram statistics on the brightness component only; 1: Perform histogram statistics on the weighted components of the three YCbCr components.
[23] RW	dci_in_range		Enter scope configuration. 0: limit range, the input 10bit pixel data range is Y-64~940ÿC-64~960ÿ 1: full range, the input 10bit pixel data range is Y-0~1023, C 0~1023ÿ
[22] RW	dci_out_range		Output range configuration. 0: limit range, the output 10bit pixel data range is Y-64~940, C 64~960; 1: full range, the output 10bit pixel data range is Y-0~1023, C 0~1023ÿ
[21:20] RW	dci_shift_ctrl		DCI histogram statistics shift control. 00: shift right by 6 bits; 01: shift right by 7 bits; 10: shift right by 8 bits; 11: Shift right by 9 bits.
[19] RW	dci_histlpf_en		Histogram low-pass filter enable signal. 0: forbidden; 1: enable.
[18:17] RO		reserved	reserve.

[16] RW	dci_dbg_mode		DCI demo mode. 0: The left side of the screen is the original image, and the right side is the DCI adjusted image; 1: The left side of the screen is the DCI adjusted image, and the right side is the original image.
[15:14] RO		reserved	reserve.
[13] RW	dci_hist_wgt_en		Histogram statistical method selection signal: 0: use the original histogram; 1: Use a weighted histogram;
[12:0] RW	dci_dbg_pos		DCI DEBUG location configuration.

ISP_VPDCIHPOS

ISP_VPDCIHPOS is the register for the horizontal direction adjustment area of the DCI algorithm.

Offset Address	Register Name	Total Reset Value
0x51C04	ISP_VPDCIHPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	dci_hstart	dci_hend	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:19]	RW	dci_hstart	The initial value of the DCI algorithm's horizontal action area.
[18:6]	RW	dci_hend	The end value of the DCI algorithm's horizontal area of action.
[5:0]	RO	reserved	reserve.

ISP_VPDCIVPOS

ISP_VPDCIVPOS is the register for vertical adjustment area of DCI algorithm.

Offset Address	Register Name	Total Reset Value
0x51C08	ISP_VPDCIVPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	dci_vstart	dci_vend	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:19]	RW	dci_vstart	The initial value of the DCI algorithm vertical area of action.

Offset Address	Register Name	Total Reset Value
0x51C08	ISP_VPDCIVPOS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_vstart	dci_vend reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[18:6]	RW	dci_vend	The end value of the vertical area of action of the DCI algorithm.
[5:0]	RO	reserved	reserve.

ISP_VPDCIHISBLD

ISP_VPDCIHISBLD is the DCI histogram statistical weighting coefficient register.

Offset Address	Register Name	Total Reset Value
0x51C0C	ISP_VPDCIHISBLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dci_cbcrsta_y	dci_cbcrsta_cb	dci_cbcrsta_cr	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_cbcrsta_y	The weighting coefficient of the Y component when the histogram statistics are superimposed. 8bit signed number, the highest bit is the sign bit.
[23:16]	RW	dci_cbcrsta_cb	The weighting coefficient of the cb component when the histogram statistics are superimposed. 8bit signed number, the highest bit is the sign bit.
[15:8]	RW	dci_cbcrsta_cr	The weighting coefficient of the cr component when the histogram statistics are superimposed. 8bit signed number, the highest bit is the sign bit.
[7:0]	RO	reserved	reserve.

ISP_VPDCIHISOFT

ISP_VPDCIHISOFT is the DCI histogram statistical offset register.

Offset Address	Register Name	Total Reset Value
0x51C10	ISP_VPDCIHISOFT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_cbcrsta_oft / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:23]	RW	dci_cbcrsta_oft	Offset when histogram statistics are superimposed. 9bit signed number, the highest bit is the sign bit.
[22:0]	RO	reserved	reserve.

ISP_VPDCIHISCOR

ISP_VPDCIHISCOR is the DCI histogram coring register.

Offset Address	Register Name	Total Reset Value
0x51C14	ISP_VPDCIHISCOR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_histcor_thr0 / dci_histcor_thr1 / dci_histcor_thr2 / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_histcor_thr0	Histogram 0 coring threshold.
[23:16]	RW	dci_histcor_thr1	Threshold for histogram 1 coring.
[15:8]	RW	dci_histcor_thr2	Threshold for histogram 2 coring.
[7:0]	RO	reserved	reserve.

ISP_VPDCIMERBLD

ISP_VPDCIMERBLD is the blend value register of the DCI adjustment unit.

Offset Address	Register Name	Total Reset Value
0x51C18	ISP_VPDCIMERBLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_metrc_abld0								dci_metrc_abld1								dci_metrc_abld2								dci_hist_abld						dci_org_abld			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	dci_metrc_abld0	Metric0 alphablend weighted value for current frame.
[25:20]	RW	dci_metrc_abld1	Metric1 alphablend weighted value for the current frame.
[19:14]	RW	dci_metrc_abld2	Metric2 alphablend weighted value for the current frame.
[13:8]	RW	dci_hist_abld	Weighted value of current histogram and previous frame histogram alphablend.
[7:2]	RW	dci_org_abld	Alpha blend value when adjusting brightness component.
[1:0]	RO	reserved	reserve.

ISP_VPDCIADJWGT

ISP_VPDCIADJWGT is the curve weight register for DCI manual configuration.

Offset Address	Register Name	Total Reset Value
0x51C1C	ISP_VPDCIADJWGT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_man_adjwgt0								dci_man_adjwgt1								dci_man_adjwgt2								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_man_adjwgt0	In manual mode, configure the weight value of curve 0.
[23:16]	RW	dci_man_adjwgt1	In manual mode, configure the weight value of curve 1.
[15:8]	RW	dci_man_adjwgt2	In manual mode, configure the weight value of curve 2.
[7:0]	RO	reserved	reserve.

ISP_VPDCICLIP0

ISP_VPDCICLIP0 is the DCI curve 0 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C20	ISP_VPDCICLIP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_wgt_cliplow0	dci_wgt_cliphigh0	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow0	Lower limit of curve 0 weight value.
[23:16]	RW	dci_wgt_cliphigh0	Upper limit of curve 0 weight value.
[15:0]	RO	reserved	reserve.

ISP_VPDCICLIP1

ISP_VPDCICLIP1 is the DCI curve 1 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C24	ISP_VPDCICLIP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_wgt_cliplow1	dci_wgt_cliphigh1	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow1	Lower limit for curve 1 weight value.
[23:16]	RW	dci_wgt_cliphigh1	High limit for curve 1 weight value.
[15:0]	RO	reserved	reserve.

ISP_VPDCICLIP2

ISP_VPDCICLIP2 is the DCI curve 2 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C28	ISP_VPDCICLIP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_wgt_cliplow2	dci_wgt_cliphigh2	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow2	Lower limit for curve 2 weight value.
[23:16]	RW	dci_wgt_cliphigh2	High limit for curve 2 weight value.
[15:0]	RO	reserved	reserve.

ISP_VPDCIGLBGAIN

ISP_VPDCIGLBGAIN is the DCI brightness adjustment unit global gain register.

Offset Address	Register Name	Total Reset Value
0x51C2C	ISP_VPDCIGLBGAIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_glb_gain0	dci_glb_gain1	dci_glb_gain2	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RW	dci_glb_gain0	Global gain 0 for luma component adjustment.
[25:20]	RW	dci_glb_gain1	Global gain 1 for luma component adjustment.
[19:14]	RW	dci_glb_gain2	Global gain 2 for luma component adjustment.
[13:0]	RO	reserved	reserve.

ISP_VPDCIPOSTHR0

ISP_VPDCIPOSTHR0 is the threshold 0 register when the DCI regulation unit is positively regulated.

Offset Address	Register Name	Total Reset Value
0x51C30	ISP_VPDCIPOSTHR0	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dci_gainpos_thr1	dci_gainpos_thr2	dci_gainpos_thr3	dci_gainpos_thr4
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr1	Threshold 1 for brightness Y when the image is adjusted from dark to bright.
[23:16]	RW	dci_gainpos_thr2	Threshold 2 of brightness Y when the image is adjusted from dark to bright.
[15:8]	RW	dci_gainpos_thr3	Threshold 3 of brightness Y when the image is adjusted from dark to bright.
[7:0]	RW	dci_gainpos_thr4	Threshold 4 of brightness Y when the image is adjusted from dark to bright.

ISP_VPDCIPOSTHR1

ISP_VPDCIPOSTHR1 is the threshold value 1 register when the DCI regulation unit is positively regulated.

Offset Address	Register Name	Total Reset Value
0x51C34	ISP_VPDCIPOSTHR1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dci_gainpos_thr5	dci_gainpos_thr6	dci_gainpos_thr7	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr5	Brightness Y threshold 5 when adjusting the image from dark to bright.
[23:16]	RW	dci_gainpos_thr6	Brightness Y threshold 6 when the image is adjusted from dark to bright.
[15:8]	RW	dci_gainpos_thr7	Threshold 7 of brightness Y when the image is adjusted from dark to bright.
[7:0]	RO	reserved	reserve.

ISP_VPDCIPOSGAIN0

ISP_VPDCIPOSGAIN0 is the gain 0 register when the DCI adjustment unit is in forward adjustment.

Offset Address	Register Name	Total Reset Value
0x51C38	ISP_VPDCIPOSGAIN0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_cbcr4				dci_gainpos_cbcr5				dci_gainpos_cbcr6				dci_gainpos_cbcr7				dci_gainpos_cbcr0				dci_gainpos_cbcr1				dci_gainpos_cbcr2				dci_gainpos_cbcr3			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:28]	RW	dci_gainpos_cbcr0	Chromaticity compensation gain of threshold 0 when the image is adjusted from dark to light.
[27:24]	RW	dci_gainpos_cbcr1	Chromaticity compensation gain of threshold 1 when adjusting the image from dark to light.
[23:20]	RW	dci_gainpos_cbcr2	Chromaticity compensation gain of threshold 2 when the image is adjusted from dark to light.
[19:16]	RW	dci_gainpos_cbcr3	Chromaticity compensation gain of threshold 3 when adjusting the image from dark to light.
[15:12]	RW	dci_gainpos_cbcr4	Chromaticity compensation gain of threshold 4 when the image is adjusted from dark to light.
[11:8]	RW	dci_gainpos_cbcr5	Chromaticity compensation gain of threshold 5 when the image is adjusted from dark to bright.
[7:4]	RW	dci_gainpos_cbcr6	Chroma compensation gain of threshold 6 when the image is adjusted from dark to bright.
[3:0]	RW	dci_gainpos_cbcr7	Chromaticity compensation gain of threshold 7 when the image is adjusted from dark to bright.

ISP_VPDCIPOSGAIN1

ISP_VPDCIPOSGAIN1 is the gain 1 register for DCI adjustment unit forward adjustment.

Offset Address	Register Name	Total Reset Value
0x51C3C	ISP_VPDCIPOSGAIN1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_cbcr8				reserved																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:28]	RW	dci_gainpos_cbcr8	Chroma compensation gain of threshold 8 when adjusting the image from dark to light.
[27:0]	RO	reserved	reserve.

ISP_VPDCIPOSSLP0

ISP_VPDCIPOSSLP0 is the slope 0 register when the DCI adjustment unit is in forward adjustment.

Offset Address	Register Name	Total Reset Value
0x51C40	ISP_VPDCIPOSSLP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainpos_slp0	dci_gainpos_slp1 dci_gainpos_slp2 —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp0	When the image is adjusted from dark to bright, the slope of interval 1, 10bit signed number.
[21:12]	RW	dci_gainpos_slp1	When the image is adjusted from dark to bright, the slope of interval 2, 10bit signed number.
[11:2]	RW	dci_gainpos_slp2	When the image is adjusted from dark to bright, the slope of interval 3, 10bit signed number.
[1:0]	RO	reserved	reserve.

ISP_VPDCIPOSSLP1

ISP_VPDCIPOSSLP1 is the slope 1 register when the DCI adjustment unit is positively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C44	ISP_VPDCIPOSSLP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainpos_slp3	dci_gainpos_slp4 dci_gainpos_slp5 —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp3	When the image is adjusted from dark to bright, the slope of interval 4, 10bit signed number.
[21:12]	RW	dci_gainpos_slp4	When the image is adjusted from dark to bright, the slope of interval 5, 10bit signed number.
[11:2]	RW	dci_gainpos_slp5	When the image is adjusted from dark to bright, the slope of interval 6, 10bit signed number.
[1:0]	RO	reserved	reserve.

ISP_VPDCIPOSSLP2

ISP_VPDCIPOSSLP2 is the slope 2 register when the DCI adjustment unit is positively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C48	ISP_VPDCIPOSSLP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainpos_slp6	dci_gainpos_slp7 reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp6	When the image is adjusted from dark to bright, the slope of interval 7, 10bit signed number.
[21:12]	RW	dci_gainpos_slp7	When the image is adjusted from dark to bright, the slope of interval 8, 10bit signed number.
[11:0]	RO	reserved	reserve.

ISP_VPDCINEGTHR0

ISP_VPDCINEGTHR0 is the threshold 0 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C4C	ISP_VPDCINEGTHR0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainneg_thr1	dci_gainneg_thr2 dci_gainneg_thr3 dci_gainneg_thr4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr1	Brightness Y threshold 1 when the image is adjusted from bright to dark.
[23:16]	RW	dci_gainneg_thr2	Brightness Y threshold 2 when the image is adjusted from bright to dark.
[15:8]	RW	dci_gainneg_thr3	Brightness Y threshold 3 when the image is adjusted from bright to dark.
[7:0]	RW	dci_gainneg_thr4	Brightness Y threshold 4 when the image is adjusted from bright to dark.

ISP_VPDCINEGTHR1

ISP_VPDCINEGTHR1 is the threshold value 1 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C50	ISP_VPDCINEGTHR1	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	dci_gainneg_thr5	dci_gainneg_thr6	dci_gainneg_thr7	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr5	Brightness Y threshold 5 when adjusting the image from bright to dark.
[23:16]	RW	dci_gainneg_thr6	Brightness Y threshold 6 when the image is adjusted from light to dark.
[15:8]	RW	dci_gainneg_thr7	Brightness Y threshold 7 when the image is adjusted from bright to dark.
[7:0]	RO	reserved	reserve.

ISP_VPDCINEGGAIN0

ISP_VPDCINEGGAIN0 is the gain 0 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C54	ISP_VPDCINEGGAIN0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_c bcr5	dci_gainneg_c bcr6	dci_gainneg_c bcr7	dci_gainneg_c	dci_gainneg_c	dci_gainneg_c	dci_gainneg_c	dci_gainneg_c bcr0 bcr1 bcr2 bcr3 bcr4
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr0	Chroma compensation gain for threshold 0 when adjusting the image from light to dark.
[27:24]	RW	dci_gainneg_cbcr1	Chroma compensation gain for threshold 1 when adjusting the image from light to dark.
[23:20]	RW	dci_gainneg_cbcr2	Chroma compensation gain for threshold 2 when adjusting the image from light to dark.
[19:16]	RW	dci_gainneg_cbcr3	Chroma compensation gain for threshold 3 when adjusting the image from light to dark.
[15:12]	RW	dci_gainneg_cbcr4	Chroma compensation gain of threshold 4 when adjusting the image from light to dark.
[11:8]	RW	dci_gainneg_cbcr5	Chroma compensation gain of threshold 5 when the image is adjusted from light to dark.
[7:4]	RW	dci_gainneg_cbcr6	Chroma compensation gain of threshold 6 when the image is adjusted from light to dark.
[3:0]	RW	dci_gainneg_cbcr7	Chroma compensation gain of threshold 7 when the image is adjusted from light to dark.

ISP_VPDCINEGGAIN1

ISP_VPDCINEGGAIN1 is the gain 1 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C58	ISP_VPDCINEGGAIN1	0x0000_0000

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainneg_cbcr8	reserved
Reset	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr8	Chroma compensation gain with threshold 8 when adjusting the image from light to dark.
[27:0]	RO	reserved	reserve.

ISP_VPDCINEGSLP0

ISP_VPDCINEGSLP0 is the slope 0 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C5C	ISP_VPDCINEGSLP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22	21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	dci_gainneg_slp0	dci_gainneg_slp1	dci_gainneg_slp2	—
Reset	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp0	When the image is adjusted from bright to dark, the slope of interval 1, 10bit signed number.
[21:12]	RW	dci_gainneg_slp1	When the image is adjusted from bright to dark, the slope of interval 2, 10bit signed number.
[11:2]	RW	dci_gainneg_slp2	When the image is adjusted from bright to dark, the slope of interval 3, 10bit signed number.
[1:0]	RO	reserved	reserve.

ISP_VPDCINEGSLP1

ISP_VPDCINEGSLP1 is the slope 1 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C60	ISP_VPDCINEGSLP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainneg_slp3 / dci_gainneg_slp4 / dci_gainneg_slp5 / —
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp3	When the image is adjusted from light to dark, the slope of interval 4, 10bit signed number.
[21:12]	RW	dci_gainneg_slp4	When the image is adjusted from bright to dark, the slope of interval 5, 10bit signed number.
[11:2]	RW	dci_gainneg_slp5	When the image is adjusted from bright to dark, the slope of interval 6, 10bit signed number.
[1:0]	RO	reserved	reserve.

ISP_VPDCINEGSLP2

ISP_VPDCINEGSLP2 is the slope 2 register when the DCI adjustment unit is negatively adjusted.

Offset Address	Register Name	Total Reset Value
0x51C64	ISP_VPDCINEGSLP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dci_gainneg_slp6 / dci_gainneg_slp7 / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp6	When the image is adjusted from light to dark, the slope of interval 7, 10bit signed number.
[21:12]	RW	dci_gainneg_slp7	When the image is adjusted from light to dark, the slope of interval 8, 10bit signed number.
[11:0]	RO	reserved	reserve.

ISPFE_MAX_ADDR

ISPFE_MAX_ADDR is the maximum address register of ISP BUFFER.

Offset Address	Register Name	Total Reset Value
0x60000	ISPFE_MAX_ADDR	0x0000_090F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	max_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1	1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr	ISP FE BUFFER Maximum address register.

ISPFE_MAX_ADDR2

ISPFE_MAX_ADDR2 is the maximum address register 2 of ISP BUFFER.

Offset Address	Register Name	Total Reset Value
0x60004	ISPFE_MAX_ADDR2	0x0000_090F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	max_addr2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1	1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr2	ISP FE BUFFER2 Maximum address register.

ISPFE_MAX_ADDR_NR1

ISPFE_MAX_ADDR_NR1 is the maximum address register of ISP NR BUFFER1.

Offset Address	Register Name	Total Reset Value
0x60008	ISPFE_MAX_ADDR_NR1	0x0000_060F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	max_addr_nr1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr_nr1	NR BUFFER1 Maximum address register.

ISPFE_MAX_ADDR_NR2

ISPFE_MAX_ADDR_NR2 is the maximum address register of ISP NR BUFFER2.

Offset Address	Register Name	Total Reset Value
0x6000C	ISPFE_MAX_ADDR_NR2	0x0000_030F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								max_addr_nr2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr_nr2	NR BUFFER2 Maximum address register.

ISPFE_TIMING

ISPFE_TIMING is the ISP timing configuration register.

Offset Address	Register Name	Total Reset Value
0x60010	ISPFE_TIMING	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	vsync_sel	Whether vsync performs toggle processing. 0: do not process; 1: processing.
[0]	RW	hsync_sel	hsync source selection. 0: input hsync; 1: input de.

ISPFE_MAX_ADDR3

ISPFE_MAX_ADDR3 is the maximum address register 3 of ISP BUFFER.

Offset Address	Register Name	Total Reset Value
0x60014	ISPFE_MAX_ADDR3	0x0000_051F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	max_addr3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 0 0 0 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr3	ISP FE BUFFER3 Maximum address register.

ISPFE_MAX_ADDR4

ISPFE_MAX_ADDR4 is the maximum address register 4 of ISP BUFFER.

Offset Address	Register Name	Total Reset Value
0x60018	ISPFE_MAX_ADDR4	0x0000_051F

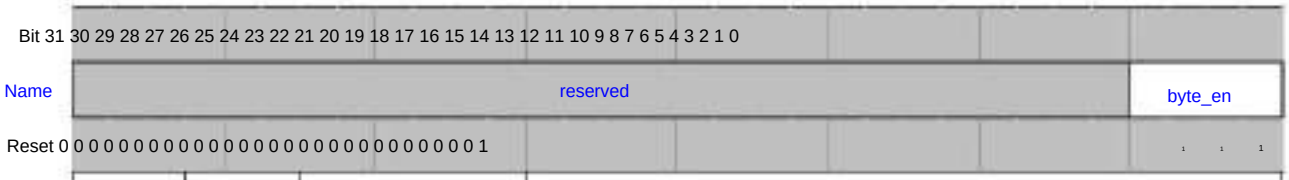
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	max_addr4
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 1 0 0 0 1

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	max_addr4	ISP FE BUFFER4 Maximum address register.

ISPFE_BYTE_EN

ISPFE_BYTE_EN is the ISP BYTE_EN configuration register.

Offset Address	Register Name	Total Reset Value
0x60020	ISPFE_BYTE_EN	0x0000_000F

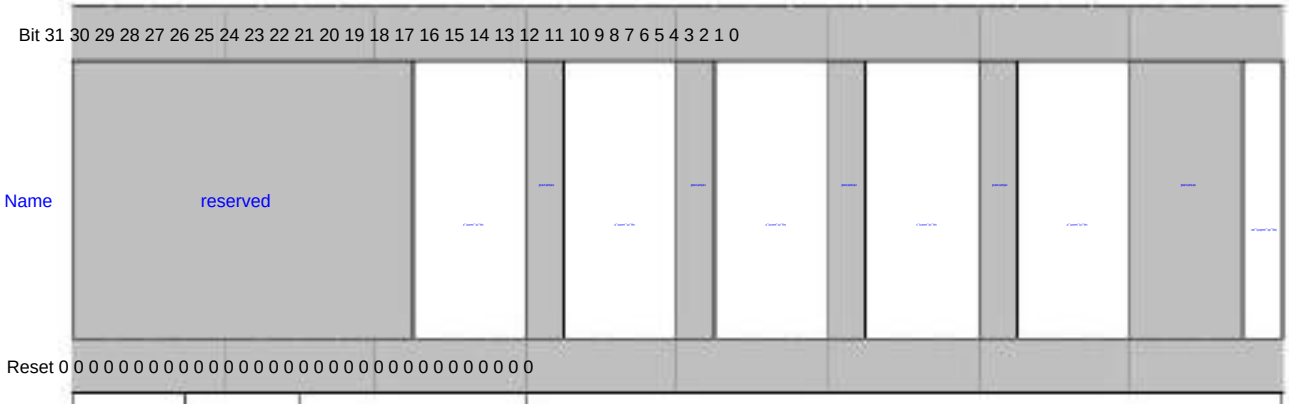


Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	byte_one	byte enable. 0: forbidden; 1: enable.

ISPFE_CH_SWITCH

ISPFE_CH_SWITCH is the ISP input switching register.

Offset Address	Register Name	Total Reset Value
0x60028	ISPFE_CH_SWITCH	0x0000_0000



Bits	Access	Name	Description
[31:23]	RO	reserved	reserve.
[22:20]	RW	isp_ch_switch_4	ISP FPN black frame data input selection. 000: for the 0th input; 001: input for the first channel; 010: for the second channel input; 011: for the third channel input; 100: for the FPN black frame input; Others: Input for FPN black frame.
[19]	RO	reserved	reserve.

[18:16]	RW	isp_ch_switch_3	ISP No. 3 data input selection. 000: for the 0th input; 001: for the 1st input; 010: for the second input; 011: for the third input; 100: input for FPN black frame; others: input for the third channel.
[15]	RO	reserved	reserve.
[14:12]	RW	isp_ch_switch_2	ISP No. 2 data input selection. 000: for the 0th input; 001: for the 1st input; 010: for the second input; 011: for the third input; 100: input for FPN black frame; others: input for the second channel.
[11]	RO	reserved	reserve.
[10:8]	RW	isp_ch_switch_1	ISP No. 1 data input selection. 000: for the 0th input; 001: for the 1st input; 010: for the second input; 011: for the third input; 100: input for FPN black frame; Others: for the 1st input.
[7]	RO	reserved	reserve.
[6:4]	RW	isp_ch_switch_0	ISP channel 0 data input selection. 000: for the 0th input; 001: for the 1st input; 010: for the 2nd input; 011: for the 3rd input; 100: input for FPN black frame; Others: It is the 0th input.
[3:1]	RO	reserved	reserve.
[0]	RW	isp_ch_switch_en	ISP input conversion enable. 0: forbidden; 1: enable.

ISPFE_FE_BYPASS_CFG

ISPFE_FE_BYPASS_CFG is the ISP FE BYPASS register.

Offset Address	Register Name	Total Reset Value
0x6002C	ISPFE_FE_BYPASS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	input_mode	ISP input mode selection. 00: Linear 16bit input, after ch_switch, the data of channel 0 is valid; 01: WDR input, 12bit input for each channel; 10: One 16bit extended input, after ch_switch, the 0th channel is valid; one 12bit input, after ch_switch, the 3rd channel is valid; 11: Two 12bit inputs, after ch_switch, the 0th and 3rd channels are valid.
[29:1]	RO	reserved	reserve.
[0]	RW	bypass_en	ISP FE BYPASS enabled. 0: data passes through ISP FE; 1: Data bypasses ISP FE.

ISPFE_CROP_CFG

ISPFE_CROP_CFG is the CROP enable register.

Offset Address	Register Name	Total Reset Value
0x60030	ISPFE_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	n1_en	1 Zone enabled. 0: forbidden; 1: enable.
[0]	RW	n0_en	0 zone enabled. 0: forbidden; 1: enable.

ISPFE_CROP_WIN

ISPFE_CROP_WIN is the CROP window register.

Offset Address	Register Name	Total Reset Value
0x60034	ISPFE_CROP_WIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Window height (in row units), the configuration value is minus 1 from the actual value.
[15:0]	RW	width	Window width (in pixels), the configuration value is the actual value minus 1.

ISPFE_CROP0_START

ISPFE_CROP0_START is the CROP start position register for area 0.

Offset Address	Register Name	Total Reset Value
0x60038	ISPFE_CROP0_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	y_start	x_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	y_start	The line number at which to start fetching the image.
[15:0]	RW	x_start	The pixel number at which to start fetching the image.

ISPFE_CROP0_SIZE

ISPFE_CROP0_SIZE is 0 area CROP size setting register.

Offset Address	Register Name	Total Reset Value
0x6003C	ISPFE_CROP0_SIZE	0xFFFF_FFFF

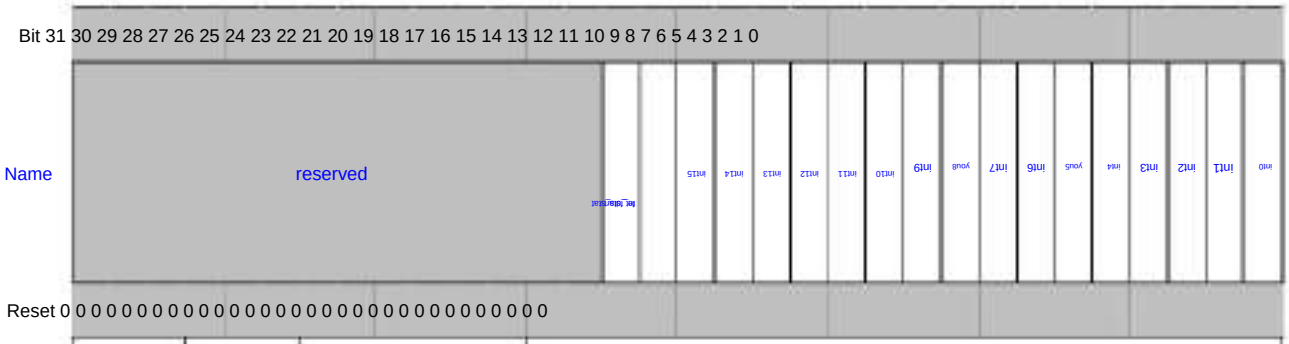
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	height	width
Reset	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:16]	RW	height	Get the height of the image (in line units), the configuration value is minus 1 from the actual value.
[15:0]	RW	width	Get the width of one line of the image (in pixels), the configuration value is minus 1 from the actual value.

ISPFE_INT

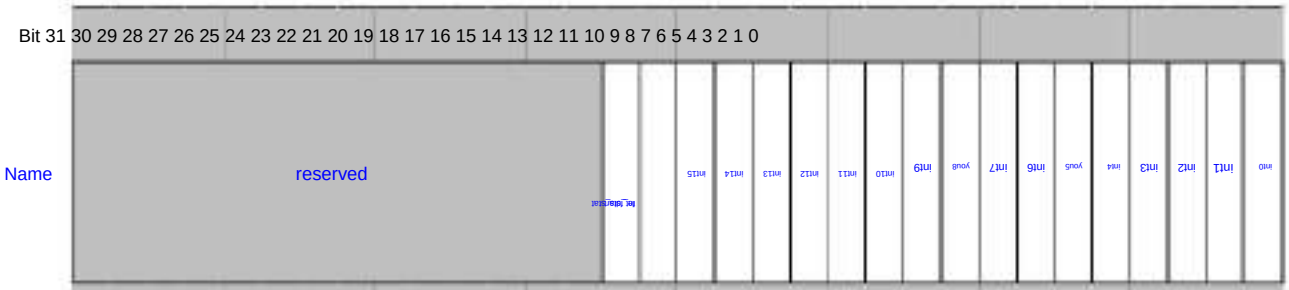
ISPFE_INT is the ISP interrupt indication register.

Offset Address	Register Name	Total Reset Value
0x600F0	ISPFE_INT	0x0000_0000



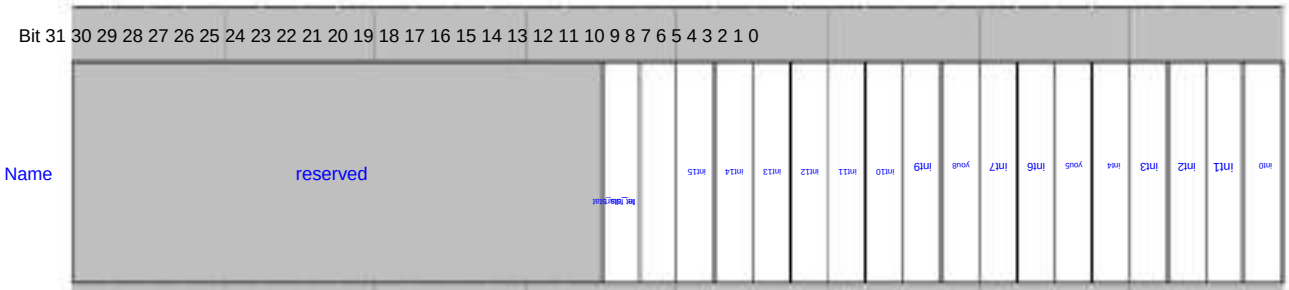
Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	WC	fe_fstart	ISP FE Frame start interrupt, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[16]	WC	int_dis_stat	DIS The current frame statistical completion interrupt, write 1 to clear. 0: no interrupt; 1: There is an interrupt.
[15]	WC	int15	ISP No. 15 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[14]	WC	int14	ISP No. 14 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[13]	WC	int13	ISP No. 13 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[12]	WC	int12	ISP No. 12 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[11]	WC	int11	ISP No. 11 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[10]	WC	int10	ISP No. 10 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.

Offset Address	Register Name	Total Reset Value
0x600F0	ISPFE_INT	0x0000_0000



Bits	Access	Name	Description
[9]	WC	int9	ISP No. 9 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[8]	WC	int8	ISP No. 8 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[7]	WC	int7	ISP No. 7 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[6]	WC	int6	ISP No. 6 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[5]	WC	int5	ISP No. 5 interrupt indication register, write 1 and clear 0: no interrupt; 1: interrupt.
[4]	WC	int4	ISP No. 4 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.
[3]	WC	int3	ISP No. 3 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[2]	WC	int2	ISP No. 2 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.

Offset Address	Register Name	Total Reset Value
0x600F0	ISPFE_INT	0x0000_0000

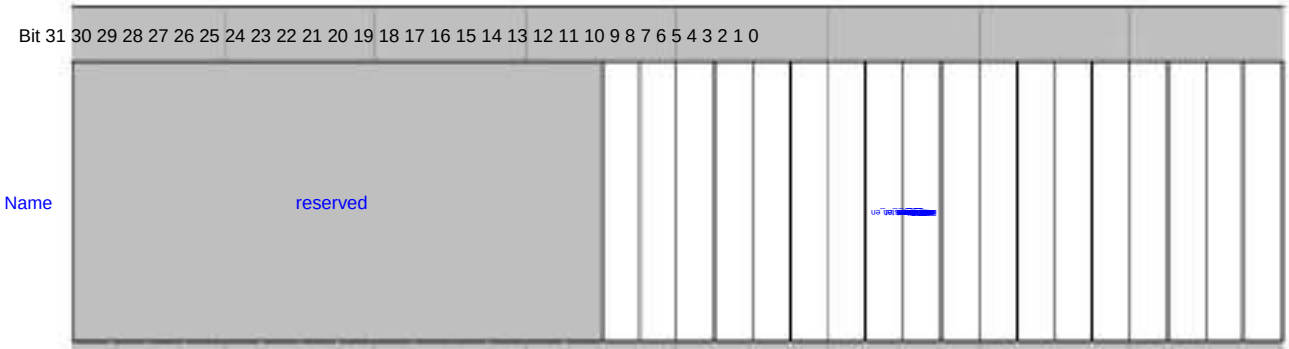


Bits	Access	Name	Description
[1]	WC	int1	ISP No. 1 interrupt indication register, write 1 to clear 0: no interrupt; 1: There is an interrupt.
[0]	WC	int0	ISP No. 0 interrupt indication register, write 1 and clear 0: no interrupt; 1: There is an interrupt.

ISPFE_INT_MASK

ISPFE_INT_MASK is the ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x600F8	ISPFE_INT_MASK	0x0000_0000



Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RW	fe_fstart_en	ISP FE Start of frame interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.

[16] RW	int_dis_stat_en		DIS Current frame statistics completed interrupt mask register. 0: mask interrupt; 1: Interrupts are enabled.
[15] RW	int15_en		ISP No. 15 interrupt mask register 0: mask interrupt; 1: enable interrupt.
[14] RW	int14_en		ISP Interrupt Mask Register No. 14 0: mask interrupt; 1: Interrupts are enabled.
[13] RW	int13_en		ISP Interrupt Mask Register No. 13 0: mask interrupt; 1: Interrupts are enabled.
[12] RW	int12_en		ISP No. 12 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.
[11] RW	int11_en		ISP Interrupt Mask Register No. 11 0: mask interrupt; 1: Interrupts are enabled.
[10] RW	int10_en		ISP Interrupt Mask Register No. 10 0: mask interrupt; 1: Interrupts are enabled.
[9] RW	int9_en		ISP No. 9 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.
[8] RW	int8_en		ISP No. 8 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.
[7] RW	int7_en		ISP No. 7 Interrupt Mask Register 0: mask interrupt; 1: Interrupts are enabled.
[6] RW	int6_en		ISP No. 6 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.

[5] RW int5_en			ISP No. 5 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.
[4] RW int4_en			ISP No. 4 interrupt mask register 0: mask interrupt; 1: enable interrupt.
[3] RW int3_en			ISP No.3 Interrupt Mask Register 0: mask interrupt; 1: Interrupts are enabled.
[2] RW int2_en			ISP No. 2 Interrupt Mask Register 0: mask interrupt; 1: Interrupts are enabled.
[1] RW int1_en			ISP No. 1 interrupt mask register 0: mask interrupt; 1: Interrupts are enabled.
[0] RW int0_en			ISP No.0 Interrupt Mask Register 0: mask interrupt; 1: Interrupts are enabled.

ISP_DIS_CFG

ISP_DIS_CFG is the work enable register.

Offset Address	Register Name	Total Reset Value
0x62400	ISP_DIS_CFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	work_en	DIS is enabled. 0: off, 1: enable.

ISP_DIS_BLK

ISP_DIS_BLK is a block configuration register.

Offset Address	Register Name	Total Reset Value
0x62404	ISP_DIS_BLK	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17	16	15 14 13 12 11 10 9	8 7 6 5 4 3 2 1	0
Name	reserved	srch_range		reserved	blk_size	
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:17]	RW	srch_range	search range high 7bit. The configuration range is 4-64.
[16]	RO		srch_range_0 is fixed at zero. The lowest bit in the search range.
[15:9]	RO	reserved	reserve.
[8:1]	RW	blk_size	The side length of the block square is 8 bits. The configuration range is 8-128.
[0]	RO		blk_size_0 is fixed at zero. The lowest bit of the side length of the block square.

ISP_DIS_V0POS

ISP_DIS_V0POS is the vertical PRJ0 block address.

Offset Address	Register Name	Total Reset Value
0x62410	ISP_DIS_V0POS	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Vertical PRJ 0 Block vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

[15:12] RO		reserved	reserve.
[11:0] RW hor			Vertical PRJ 0 Block horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_V4POS

ISP_DIS_V4POS is the vertical PRJ4 block address.

Offset Address	Register Name	Total Reset Value
0x62414	ISP_DIS_V4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																to see								reserved							before	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27] RO		reserved	reserve.
[26:16] RW ver			Vertical PRJ 4 blocks of vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.
[15:12] RO		reserved	reserve.
[11:0] RW hor			Vertical PRJ 4 blocks of horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_V8POS

ISP_DIS_V8POS is the vertical PRJ8 block address.

Offset Address	Register Name	Total Reset Value
0x62418	ISP_DIS_V8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																to see								reserved							before	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27] RO		reserved	reserve.
[26:16] RW ver			Vertical PRJ 8 blocks of vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.
[15:12] RO		reserved	reserve.

[11:0] RW hor			Vertical PRJ 8 blocks of horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_V0POSE

ISP_DIS_V0POSE is the vertical PRJ0 block address.

Offset Address	Register Name	Total Reset Value
0x62420	ISP_DIS_V0POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	to see reserved before
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:27] RO		reserved	reserve.
[26:16] RW ver			Vertical PRJ 0 The vertical coordinate of the end point of the block, excluding the lowest bit of the coordinate value, reducing the 1bit register.
[15:12] RO		reserved	reserve.
[11:0] RW hor			Vertical PRJ 0 The horizontal coordinate of the end point of the block, excluding the lowest bit of the coordinate value, reducing the 1bit register.

ISP_DIS_V4POSE

ISP_DIS_V4POSE is the vertical PRJ4 block address.

Offset Address	Register Name	Total Reset Value
0x62424	ISP_DIS_V4POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	to see reserved before
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:27] RO		reserved	reserve.
[26:16] RW ver			Vertical PRJ The vertical coordinate of the end point of 4 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.
[15:12] RO		reserved	reserve.
[11:0] RW hor			Vertical PRJ The horizontal coordinates of the end point of 4 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.

ISP_DIS_V8POSE

ISP_DIS_V8POSE is the vertical PRJ8 block address.

Offset Address	Register Name	Total Reset Value
0x62428	ISP_DIS_V8POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Vertical PRJ The vertical coordinate of the end point of 8 blocks, excluding the lowest bit of the coordinate value, reducing the 1-bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Vertical PRJ Horizontal coordinate of the end point of 8 blocks, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_H0POS

ISP_DIS_H0POS is the horizontal PRJ0 block address.

Offset Address	Register Name	Total Reset Value
0x62430	ISP_DIS_H0POS	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ 0 Block vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ 0 Block horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_H4POS

ISP_DIS_H4POS is the horizontal PRJ4 block address.

Offset Address	Register Name	Total Reset Value
0x62434	ISP_DIS_H4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																to see								reserved				before				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ 4 blocks of vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ 4 blocks of horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_H8POS

ISP_DIS_H8POS is the horizontal PRJ8 block address.

Offset Address	Register Name	Total Reset Value
0x62438	ISP_DIS_H8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																to see								reserved				before				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ 8 blocks of vertical coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ 8 blocks of horizontal coordinates, excluding the lowest bit of coordinate value, reduce 1bit register.

ISP_DIS_H0POSE

ISP_DIS_H0POSE is the horizontal PRJ0 block address.

Offset Address	Register Name	Total Reset Value
0x62440	ISP_DIS_H0POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ 0 The vertical coordinate of the end point of the block, excluding the lowest bit of the coordinate value, reducing the 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ 0 The horizontal coordinate of the end point of the block, excluding the lowest bit of the coordinate value, reducing the 1bit register.

ISP_DIS_H4POSE

ISP_DIS_H4POSE is the horizontal PRJ4 block address.

Offset Address	Register Name	Total Reset Value
0x62444	ISP_DIS_H4POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ The vertical coordinates of the end point of 4 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ The horizontal coordinates of the end point of 4 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.

ISP_DIS_H8POSE

ISP_DIS_H8POSE is the horizontal PRJ8 block address.

Offset Address	Register Name	Total Reset Value
0x62448	ISP_DIS_H8POSE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	to see	reserved	before
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26:16]	RW	ver	Horizontal PRJ The vertical coordinates of the end point of 8 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.
[15:12]	RO	reserved	reserve.
[11:0]	RW	hor	Horizontal PRJ The horizontal coordinates of the end point of 8 blocks, excluding the lowest bit of the coordinate value, reducing the 1bit register.

ISP_DIS_RAW_LUMA

ISP_DIS_RAW_LUMA is a data type register.

Offset Address	Register Name	Total Reset Value
0x62450	ISP_DIS_RAW_LUMA	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved			
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	raw_luma	Enter the data type. 0ÿYESÿ 1ÿRAWÿ

ISP_DIS_GAMMA_EN

ISP_DIS_GAMMA_EN enables gamma.

Offset Address	Register Name	Total Reset Value
0x62454	ISP_DIS_GAMMA_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	gamma_en	GAMMA is enabled. 0: off; 1: enable.

ISP_DIS_H_STAT_RADDR

ISP_DIS_H_STAT_RADDR is the read address of the horizontal statistical value.

Offset Address	Register Name	Total Reset Value
0x62488	ISP_DIS_H_STAT_RADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	h_stat_raddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	h_stat_raddr	h_delta, h_sad, h_mv information of each block. Each address contains only one piece of information. like: 0x00: h_delta[15:0] of block 0; 0x01: h_sad[23:0] of block 0; 0x02: h_mv[8:0] of block 0; ...and so on.

ISP_DIS_H_STAT_RDATA

ISP_DIS_H_STAT_RDATA Read data for horizontal statistics.

Offset Address	Register Name	Total Reset Value
0x6248C	ISP_DIS_H_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	h_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	h_stat_rdata	Statistical value in the horizontal direction.

ISP_DIS_V_STAT_RADDR

ISP_DIS_V_STAT_RADDR is the vertical statistical value read address.

Offset Address	Register Name	Total Reset Value
0x62498	ISP_DIS_V_STAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RW	v_stat_raddr	v_delta, v_sad, v_mv information of each block. Each address contains only one piece of information. like: 0x00: v_delta[15:0] of block 0; 0x01: v_sad[23:0] of block 0; 0x02: v_mv[8:0] of block 0; ...and so on.

ISP_DIS_V_STAT_RDATA

ISP_DIS_V_STAT_RDATA Read data for vertical statistics.

Offset Address	Register Name	Total Reset Value
0x6249C	ISP_DIS_V_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	v_stat_rdata Statistics in the vertical direction.

ISP_DIS_CTRL_F

ISP_DIS_CTRL_F is DIS common control register.

Offset Address	Register Name	Total Reset Value
0x624E0	ISP_DIS_CTRL_F	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name	Description
[31:2]	RO reserved	reserve.
[1:0]	RW rggb_cfg	RGGB order. 00ÿR Gr Gb Bÿ 01ÿGr RB Gbÿ 10ÿGb B R Grÿ 11ÿB Gb Gr Rÿ

ISP_DIS_CTRL_I

ISP_DIS_CTRL_I Immediate update register for DIS.

Offset Address	Register Name	Total Reset Value
0x624E4	ISP_DIS_CTRL_I	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update_mode	ISP update mode register: 0: reg_newer update; 1: frame update.

ISP_DIS_UPDATE

ISP_DIS_UPDATE updates the register for the DIS register.

Offset Address	Register Name	Total Reset Value
0x624EC	ISP_DIS_UPDATE	0x0000_0000

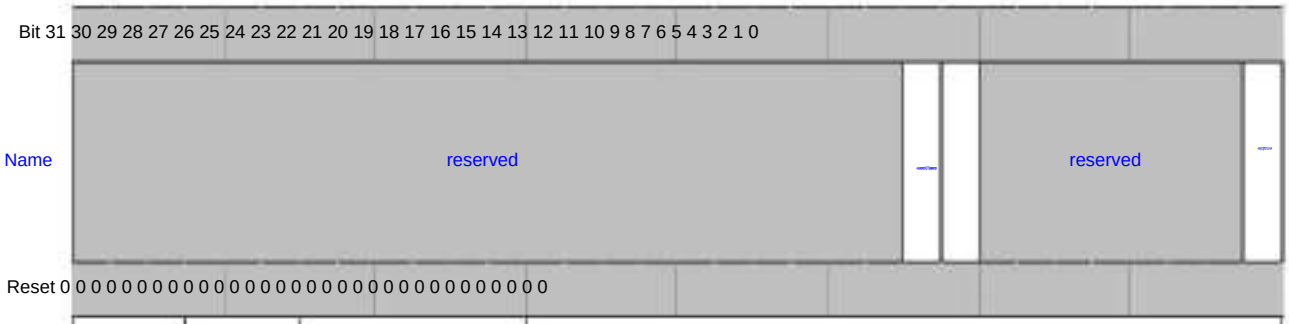
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update	The ISP updates the register, which is automatically cleared every frame.

ISP_FPN_CFG

ISP_FPN_CFG is the FPN configuration register.

Offset Address	Register Name	Total Reset Value
0x63a00	ISP_FPN_CFG	0x0000_0000



Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	line_frame	FPN frame/line mode selection. 0: frame mode; 1: Line mode.
[8]	RW	calib_corr	FPN correction/calibration mode selection. 0: Calibration mode; 1: Calibration mode.
[7:1]	RO	reserved	reserve.
[0]	RW	enable	FPN enabled. 0: forbidden; 1: enable.

ISP_FPN_CALIB_START

ISP_FPN_CALIB_START is the FPN calibration start calibration signal register.

Offset Address	Register Name	Total Reset Value
0x63a04	ISP_FPN_CALIB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	calib_start	FPN Calibration start signal. Automatically cleared.

ISP_FPN_CORR_CFG

ISP_FPN_CORR_CFG is the FPN correction configuration register.

Offset Address	Register Name	Total Reset Value
0x63a08	ISP_FPN_CORR_CFG	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3]	RW	correct3_en	FPN 3rd channel correction enable. 0: forbidden; 1: enable.
[2]	RW	correct2_en	FPN 2nd channel correction enable. 0: forbidden; 1: enable.

[1] RW	correct1_en		FPN 1st channel correction enable. 0: forbidden; 1: enable.
[0] RW	correct0_en		FPN channel 0 correction enable. 0: disable; 1: enable.

ISP_FPN_STAT

ISP_FPN_STAT is the FPN calibration status register.

Offset Address	Register Name	Total Reset Value
0x63a0C	ISP_FPN_STAT	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hcnt																reserved		vcnt						reserved							busy
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	hcnt	row count.
[15:14]	RO	reserved	reserve.
[13:8]	RO	vcnt	Scaled frame count.
[7:1]	RO	reserved	reserve.
[0]	RO	busy	FPN calibration status register. 0: idle; 1: calibration.

ISP_FPN_WHITE_LEVEL

ISP_FPN_WHITE_LEVEL is the white point configuration register for FPN calibration.

Offset Address	Register Name	Total Reset Value
0x63a10	ISP_FPN_WHITE_LEVEL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	white_level
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	white_level	FPN calibrated white point configuration.

ISP_FPN_DIVCOEF

ISP_FPN_DIVCOEF is the division coefficient register for FPN calibration.

Offset Address	Register Name	Total Reset Value
0x63a18	ISP_FPN_DIVCOEF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	divcoef
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	divcoef	FPN Scale division factor.

ISP_FPN_FRAMELOG2

ISP_FPN_FRAMELOG2 is the FPN calibration frame number register.

Offset Address	Register Name	Total Reset Value
0x63a1C	ISP_FPN_FRAMELOG2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2:0]	RW	cpi_fpn_framelog2	FPN calibrated frame number, the logarithm of the frame number to 2 is allocated.

ISP_FPN_SUM0

ISP_FPN_SUM0 is the FPN calibration sum and low register.

Offset Address	Register Name	Total Reset Value
0x63a20	ISP_FPN_SUM0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sum
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	sum	FPN scales the accumulated sum low.

ISP_FPN_SUM1

ISP_FPN_SUM1 is the FPN calibration sum and high register.

Offset Address	Register Name	Total Reset Value
0x63a24	ISP_FPN_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	FPN scales the accumulated sum high.

ISP_FPN_CORR0

ISP_FPN_CORR0 Configure 0 register for FPN correction.

Offset Address	Register Name	Total Reset Value
0x63a30	ISP_FPN_CORR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN Corrected Intensity, U8.8.
[15:12]	RO	reserved	reserve.
[11:0]	RW	offset	FPN correction bias.

ISP_FPN_CORR1

ISP_FPN_CORR1 Configuration 1 register for FPN correction.

Offset Address	Register Name	Total Reset Value
0x63a34	ISP_FPN_CORR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN Corrected Intensity, U8.8.
[15:12]	RO	reserved	reserve.

[11:0]	RW	offset	FPN correction bias.

ISP_FPN_CORR2

ISP_FPN_CORR2 Configuration 2 register for FPN correction.

Offset Address	Register Name	Total Reset Value
0x63a38	ISP_FPN_CORR2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	strength	reserved / offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN Corrected Intensity, U8.8.
[15:12]	RO	reserved	reserve.
[11:0]	RW	offset	FPN correction bias.

ISP_FPN_CORR3

ISP_FPN_CORR3 Configuration 3 register for FPN correction.

Offset Address	Register Name	Total Reset Value
0x63a3C	ISP_FPN_CORR3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	strength	reserved / offset
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN Corrected Intensity, U8.8.
[15:12]	RO	reserved	reserve.
[11:0]	RW	offset	FPN correction bias.

ISP_FPN_SHIFT

ISP_FPN_SHIFT is the FPN shift configuration register.

Offset Address	Register Name	Total Reset Value
0x63a40	ISP_FPN_SHIFT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	frame_calib_shift	reserved	out_shift	reserved	in_shift	reserved	fpn_shift
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:24]	RW	frame_calib_shift	Frame calibration last frame output left shift number.
[23:20]	RO	reserved	reserve.
[19:16]	RW	out_shift	Output left shift bits.
[15:12]	RO	reserved	reserve.
[11:8]	RW	in_shift	Enter the number of right shifts.
[7:4]	RO	reserved	reserve.
[3:0]	RW	fpn_shift	Input FPN right shift number.

ISP_FPN_MAX_O

ISP_FPN_MAX_O is the FPN output maximum value register.

Offset Address	Register Name	Total Reset Value
0x63a50	ISP_FPN_MAX_O	0x0000_3FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						max_o	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	max_o	FPN output max.

ISP_FPN_OVERFLOWTHR

ISP_FPN_OVERFLOWTHR is the FPN correction threshold.

Offset Address	Register Name	Total Reset Value
0x63a54	ISP_FPN_OVERFLOWTHR	0x0000_3FFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	overflowthr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:0]	RW	overflowthr	FPN correction threshold.

ISP_FPN_LINE_WADDR

ISP_FPN_LINE_WADDR is the write address register for FPN line mode black line.

Offset Address	Register Name	Total Reset Value
0x63a80	ISP_FPN_LINE_WADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fpn_line_waddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_waddr	FPN line mode black line write address register.

ISP_FPN_LINE_WDATA

ISP_FPN_LINE_WDATA is the FPN line mode black line write data register.

Offset Address	Register Name	Total Reset Value
0x63a84	ISP_FPN_LINE_WDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fpn_line_wdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_wdata	FPN line mode black line write data register.

ISP_FPN_LINE_RADDR

ISP_FPN_LINE_RADDR is the FPN line mode black line read address register.

Offset Address	Register Name	Total Reset Value
0x63a88	ISP_FPN_LINE_RADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fpn_line_raddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_raddr	FPN line mode black line read address register.

ISP_FPN_LINE_RDATA

ISP_FPN_LINE_RDATA is the FPN line mode black line read data register.

Offset Address	Register Name	Total Reset Value
0x63a8C	ISP_FPN_LINE_RDATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	fpn_line_rdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_rdata	FPN line mode black line read data register.

ISP_FPN_CTRL_F

ISP_FPN_CTRL_F is the general control register of FPN.

Offset Address	Register Name	Total Reset Value
0x63aE0	ISP_FPN_CTRL_F	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1:0]	RW	rggb_cfg	RGGB order. 00ÿR Gr Gb Bÿ 01ÿGr RB Gbÿ 10ÿGb B R Grÿ 11ÿB Gb Gr Rÿ

ISP_FPN_CTRL_I

ISP_FPN_CTRL_I is the FPN immediate update control register.

Offset Address	Register Name	Total Reset Value
0x63aE4	ISP_FPN_CTRL_I	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	update_mode	ISP update mode register. 0: update register update; 1: frame update.

ISP_FPN_TIMING

ISP_FPN_TIMING is the FPN output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x63aE8	ISP_FPN_TIMING	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								cpi_fix_timing_stat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:14]	RO	reserved	reserve.
[13:1]	RW	cpi_fix_timing_stat	Manual timing parameter setting, set the generated line blanking length.
[0]	RO	reserved	reserve.

ISP_FPN_UPDATE

ISP_FPN_UPDATE is an update register for the FPN register.

Offset Address	Register Name	Total Reset Value
0x63aEC	ISP_FPN_UPDATE	0x0000_0000

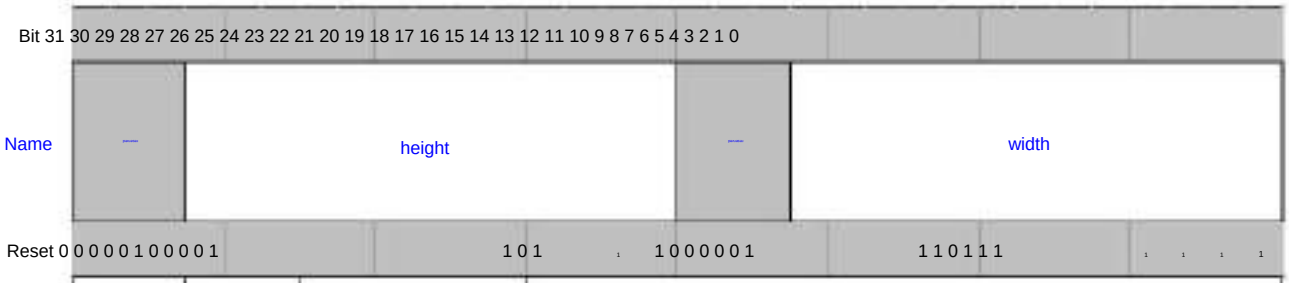
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RW	update	ISP update register, cleared to 0 automatically every frame.

ISP_FPN_SIZE

ISP_FPN_SIZE is the FPN image width and height register.

Offset Address	Register Name	Total Reset Value
0x63aF0	ISP_FPN_SIZE	0x0437_077F



Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:16]	RW	height	Image height (minus 1), such as 1080 image height, match 1079.
[15:13]	RO	reserved	reserve.
[12:0]	RW	width	Image width (minus 1), such as 1920 image width, match 1919.

Table of contents

illustration catalog

table of contents

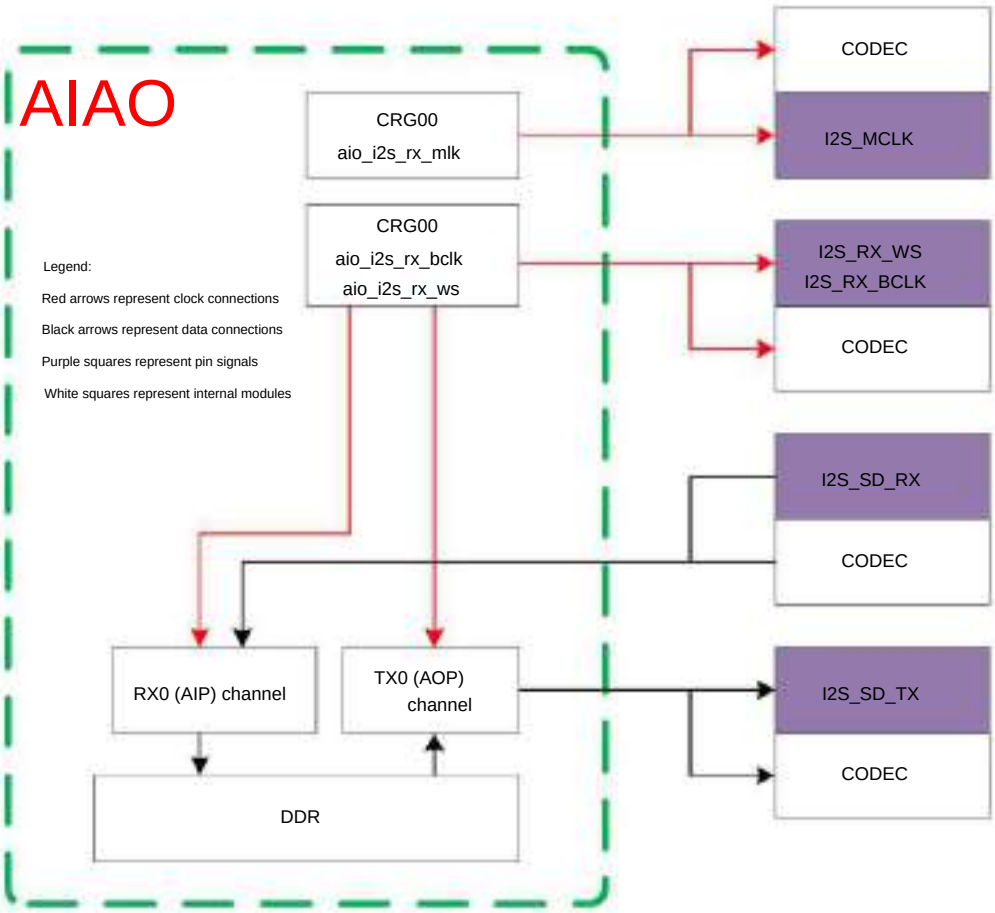
11 audio port

11.1 TECHNOLOGY

11.1.1 Overview

The audio input and output interface AIAO (Audio Input/Audio Output) is used to connect with the on-chip or off-chip AudioCodec to complete the input and output of audio data to realize functions such as recording, intercom, and playback. Hi3519V100 integrates 1 AIAO, including 1 AIP (Audio Input Port) and 1 AOP (Audio Output Port), supporting stereo input and output. The block diagram of the basic module is shown in Figure 11-1 :

Figure 11-1 Hi3519V100 AIAO block diagram



11.1.2 Features

The AIAO interface supports I^2S and PCM (Pulse Code Modulation) two modes, using DMA access data.

PCM interface

The PCM interface has the following characteristics:

Support main mode mono 16bit linear PCM coded transmission and reception.

PCM interface frame synchronization signal only supports short pulse synchronization signal (the duration of the synchronization signal is 1 clock cycle), and supports standard and custom modes.

Receive (AIP) and send (AOP) are independent of each other and can be enabled or disabled individually.

Both receiving (AIP) and sending (AOP) adopt DMA operation, and access data through the circular buffer opened by software, and the size and waterline of the circular buffer are adjustable.

I2S interface

I^2S The interface has the following characteristics:

Support master mode stereo 16/24bit data sending and receiving. Support 8kHz

ÿ192kHz sampling rate.

Receive (AIP) and send (AOP) are independent of each other and can be enabled or disabled individually.

Both receiving (AIP) and sending (AOP) adopt DMA operation, and access data through the circular buffer opened by software, and the size and waterline of the circular buffer are adjustable.

11.1.3 Functional Description

typical application

Hi3519V100 integrates 1 AIP and 1 AOP, among which:

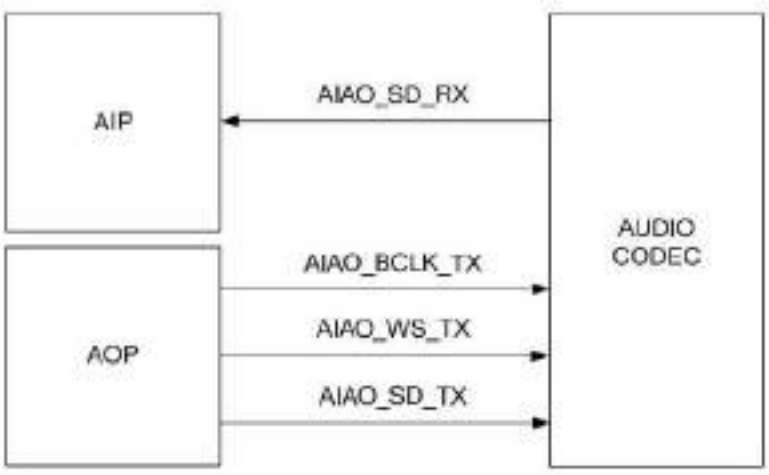
AIP supports data reception in PCM or I2S mode mentioned above.

AOP supports music playback in PCM or I2S mode mentioned above.

AIP supports master mode I2S docking internal Audio Codec or I2S/PCM master mode docking external ADC for sound collection.

AOP supports master mode I2S docking internal Audio Codec or I2S/PCM master mode docking external DAC for music playback.

Figure 11-2 I ^{2} S/PCM interface master mode connection diagram



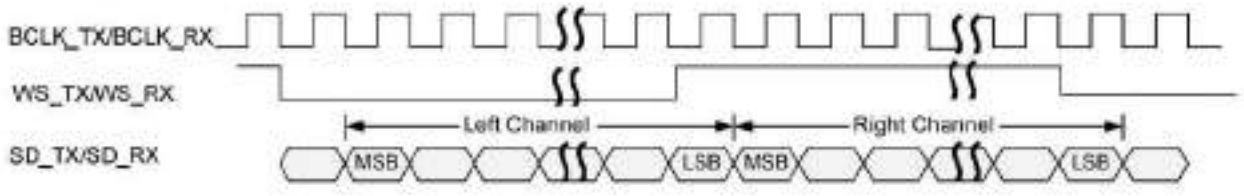
Functional principle

AIP through I ^{2} The S or PCM interface receives the audio data after AD (Analog-to-Digital) conversion by connecting to the internally integrated Audio Codec or an external ADC, stores it in the circular buffer created for the AIP, and then takes it away and stores it by the CPU, thus completing recording function.

AOP reads the audio data from the circular buffer, and then transmits the audio data through the IPCM interface to the internally integrated ^{2} S or Audio Codec or an external DAC for DA (Digital-to-Analog) conversion according to the set sampling rate. play.

When connecting to an external I2S interface, the supported I2S timing is shown in Figure 11-3.

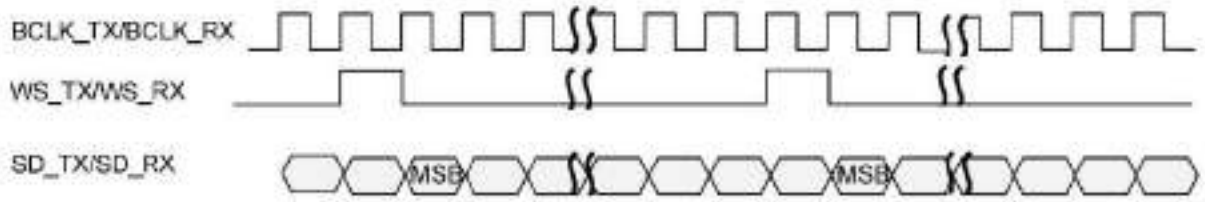
Figure 11-3 I 2 S interface timing



I2S adopts MSB FIRST mode for transmission, data and WS signals are sent out on the falling edge of BCLK, and sampled on the rising edge of BCLK. Data is delayed by one BCLK period relative to the WS signal.

When connected to an external PCM interface, it supports PCM standard timing and data left-aligned timing. The standard timing is shown in Figure 11-4.

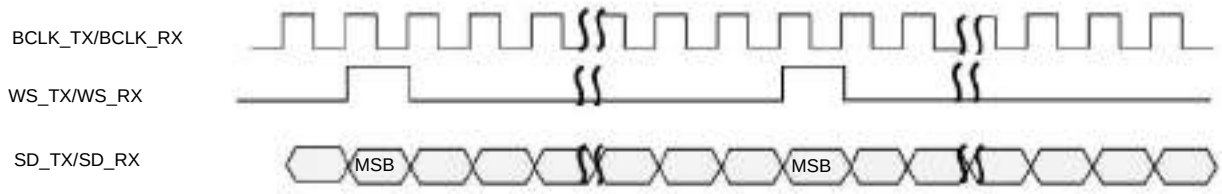
Figure 11-4 Timing sequence of PCM interface standard mode



PCM mode adopts MSB FIRST mode for transmission, data and WS signal are sent out on BCLK rising edge, and are sampled on BCLK falling edge. Data is delayed by one BCLK period relative to the WS signal in standard mode.

The timing sequence of PCM custom mode is shown in Figure 11-5 .

Figure 11-5 Timing sequence of PCM interface custom mode



In the custom mode, the data starts to be sent out in sync with the WS pulse.

11.1.4 Working method

Channel multiplexing configuration

Since there is only one pair of AIP/AOP channels, the internally integrated Audio Codec and the external I2S/PCM interfaced ADC/DAC cannot work simultaneously.

In the system MISC register, when configuring the i2s_pad_enable register as 1 and the audio_enable register as 0, connect the AIP/AOP channel to the external I2S/PCM pin. Conversely, when configuring the i2s_pad_enable register as 0 and the audio_enable register as 1, connect the AIP/AOP to the internally integrated Audio Codec.

Clock gating and clock configuration

When enabling AIAO for recording or playback, the clock gate of the corresponding channel (AIP/AOP) in AIAO must be turned on first. Specific steps are as follows:

Step 1. Configure the PERI_CRG32 of the system CRG register as 0x2, release the AIAO reset, and enable the clock gating.

Step 2. Configure I2S_CRG_CFG0_00, I2S_CRG_CFG1_00 of AIAO register. Choose an appropriate frequency division factor . Note that when using the internally integrated Audio Codec, the MCLK/WS frequency division ratio of the i2s1_fs_sel register configured by the Audio Codec must be consistent with that configured here.

----Finish

soft reset

The 2 channels (AIP, AOP) inside AIAO support independent soft reset. When the AIAO module is reset, the 2 channels are reset at the same time.

recording workflow

The recording steps are as follows: (assuming the scene is I2S mode 48K, 2-channel 16bit precision, assuming AIAO PLL source clock is 1188M, system controller AIAO clock has been enabled):

Step 1. Configure the register I2S_CRG_CFG0_00 as 0x152EF0, and the clock output MCLK frequency is 12.288MHzÿ

Step 2. Configure the register I2S_CRG_CFG1_00 as 0x0000c133, enable the clock at this time, and configure BCLK as The frequency of MCLK is divided by 4, and FCLK is configured as the frequency of BCLK by 64. At this time, the frequency of FCLK is 48KHz.

Step 3. Set RX_IF_ATTRI to 0xE4800014, and set the receiving channel to work at I and the sampling precision to ^{2} In S mode, two channels, be 16bit.

Step 4. Configure the RX_BUFF_SADDR register to assign the starting address of DDR, such as 0x00000100 configuration The RX_BUFF_SIZE register is the size of the allocated DDR_BUF, such as 0x0000F000, configure The RX_BUFF_WPTR register and the RX_BUFF_RPTR register are 0x0, and the read and write pointers are initialized. configuration RX_TRANS_SIZE register, such as 0x00000F00.

Step 5. According to the need, enable the corresponding interrupt bit of the receiving channel, that is, the configuration register RX_INT_ENA, for example, configure as 0x00000001, only able to trans_int interrupt.

Step 6. Configure the register RX_DSP_CTRL to 0x10000000, enable the receiving channel, the receiving channel starts to work, and record start.

Step 7. Judge the empty/full status of the circular buffer and the amount of valid data by reading the values of RX_BUFF_WPTR and RX_BUFF_RPTR; ensure that the data is taken away before the circular buffer is full, and write the updated read address of the circular buffer into RX_BUFF_RPTR, otherwise the circular buffer may overflow and the sound will be discontinuous.

Step 8. After the recording is completed, write the register RX_DSP_CTRL to 0x00000000, and continuously query the RX_DSP_CTRL register until it changes to 0x20000000, indicating that the receiving channel has stopped and completed.

----Finish

注意

Before starting AIP, the AIP clock configuration must be completed to ensure that AIAO_BCLK_RX and AIAO_WS_RX are normal.

playback workflow

The playback steps are as follows: (Assume that the I^2S mode 48K2 channel 16bit precision, assuming AIAO PLL source clock scene I is 1188M, and the AIAO clock of the system controller has been enabled):

Step 1. Configure the register I2S_CRG_CFG0_00 as 0x152EF0, and the clock output MCLK frequency is 12.288MHzÿ

Step 2. Configure the register I2S_CRG_CFG1_00 as 0x0000c133, enable the clock at this time, and configure BCLK as The frequency of MCLK is divided by 4, and FCLK is configured as the frequency of BCLK by 64. At this time, the frequency of FCLK is 48KHz.

Step 3. Configure the TX_IF_ATTRI register as 0xE4000014, that is, configure the transmit interface to work on the I^2S mode, two beeps channel with 16bit sampling precision.

Step 4. Configure TX_BUFF_SADDR as the starting address of BUF, such as 0x00000100, TX_BUFF_SIZE as the size of BUF, initialize TX_BUFF_WPTR to 0x0, TX_BUFF_RPTR to 0x0, set TX_TRANS_SIZE. (This step of configuration can refer to the recording process)

Step 5. According to the needs, enable the corresponding interrupt bit of the receiving channel, that is, the configuration register TX_INT_ENA, for example, configure as 0x00000001, only enable trans_int interrupt.

Step 6. Configure the register TX_DSP_CTRL as 0x10000000 to enable the playback channel.

Step 7. By reading the values of TX_BUFF_WPTR and TX_BUFF_RPTR , determine the empty/full status of the circular buffer and the amount of valid data; ensure that the new audio data is filled in before the circular buffer is empty, and write the updated circular buffer Write the address into TX_BUFF_WPTR, otherwise the circular buffer may overflow and the sound will be discontinuous.

Step 8. After the playback is over, configure the register TX_DSP_CTRL to 0x00000000, stop playing the channel, query the TX_DSP_CTRL register, and when the value changes to 0x20000000, it means that the channel is stopped.

----Finish

注意

Before starting AOP, the AOP clock configuration must be completed to ensure that AIAO_BCLK_TX and AIAO_WS_TX are normal.

When writing data to the AOP circular buffer and updating TX_BUFF_WPTR , the AOP cycle must be guaranteed The buffer free space is not less than 32 bytes.

11.1.5 AIAO register overview

An overview of the AIAO registers is shown in Table 11-1 .

Table 11-1 AIAO register overview (base address is 0x1108_0000)

offset address	name	describe	page number
0x0000	AIAO_INT_ENA	AIAO module interrupt enable register	11-8
0x0004	AIAO_INT_STATUS	AIAO module interrupt status register	11-9
0x0008	AIAO_INT_RAW	AIAO module raw interrupt register	11-9
0x0100	I2S_CRG_CFG0_00	I2S00 CRG configuration register 0	11-10
0x0104	I2S_CRG_CFG1_00	I2S00 CRG configuration register 1	11-10
0x0144	I2S_CRG_CFG1_08	I2S08 CRG configuration register 1	11-11
0x1000	RX_IF_ATTRI	Receive channel interface attribute setting register	11-12
0x1004	RX_DSP_CTRL	Control register for receive processing channel	11-13
0x1080	RX_BUFF_SADDR	Receive channel DDR buffer start address register 11-14	
0x1084	RX_BUFF_SIZE	Receive channel DDR buffer size register	11-15
0x1088	RX_BUFF_WPTR	Receive channel DDR buffer write address register 11-15	
0x108C	RX_BUFF_RPTR	Receive channel DDR buffer read address register 11-15	
0x1090	RX_BUFF_ALFULL_TH	The DDR buffer of the receive channel is almost full of the watermark register	11-16
0x1094	RX_TRANS_SIZE	Receive channel data transfer length register	11-16
0x10A0	RX_INT_ENA	Receive channel interrupt enable register	11-17
0x10A4	RX_INT_RAW	RAW interrupt register of receive channel	11-18
0x10A8	RX_INT_STATUS	Receive channel interrupt status register	11-19
0x10AC	RX_INT_CLR	Receive channel interrupt clear register	11-20
0x2000	TX_IF_ATTRI	interface attribute setting register of the transmit channel	11-22
0x2004	TX_DSP_CTRL	Transmit processing channel control register	11-23
0x2080	TX_BUFF_SADDR	DDR buffer start address register 11-25 of transmit channel	
0x2084	TX_BUFF_SIZE	DDR buffer size register for transmit channel	11-25
0x2088	TX_BUFF_WPTR	DDR buffer write address register 11-26 of transmit channel	
0x208C	TX_BUFF_RPTR	Transmit channel DDR buffer read address register 11-26	

offset address name	describe	page number
0x2090 TX_BUFF_ALEMPT Y_TH	DDR buffer of transmit channel almost empty watermark register	11-27
0x2094	TX_TRANS_SIZE Data transmission length register of the sending channel	11-27
0x20A0 TX_INT_ENA	Transmit channel interrupt enable register	11-27
0x20A4 TX_INT_RAW	Raw interrupt register of transmit channel	11-29
0x20A8 TX_INT_STATUS	Transmit channel interrupt status register	11-30
0x20AC TX_INT_CLR	Transmit channel interrupt clear register	11-31

11.1.6 AIAO Register Description

AIAO_INT_ENA

AIAO_INT_ENA is the AIAO module interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0000	AIAO_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	tx_ch0_int_ena	Interrupt enable for transmit channel 0. 0: disable; 1: enable.
[15:1]	RO	reserved	reserve.
[0]	RW	rx_ch0_int_ena	Interrupt enable for receive channel 0. 0: disable; 1: enable.

AIAO_INT_STATUS

AIAO_INT_STATUS is the interrupt status register of AIAO module.

Offset Address	Register Name	Total Reset Value
0x0004	AIAO_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:17]	RO	reserved	reserve.
[16]	RO	tx_ch0_int_status	Transmit the interrupt status of channel 0. 0: no interrupt status; 1: interrupt status.
[15:1]	RO	reserved	reserve.
[0]	RO	rx_ch0_int_status	Receive channel 0 interrupt status. 0: no interrupt status; 1: There is an interrupt status.

AIAO_INT_RAW

AIAO_INT_RAW is the raw interrupt register of AIAO module.

Offset Address	Register Name	Total Reset Value
0x0008	AIAO_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:17]	RO	reserved	reserve.

[16] RO		tx_ch0_int_raw	Send raw interrupt for channel 0. 0: no original interrupt; 1: There is a raw interrupt.
[15:1] RO		reserved	reserve.
[0]	RO	rx_ch0_int_raw	Receive raw interrupt for channel 0. 0: no original interrupt; 1: There is a raw interrupt.

I2S_CRG_CFG0_00

I2S_CRG_CFG0_00 Configure register number 0 for I2S00 CRG.

Offset Address	Register Name	Total Reset Value
0x0100	I2S_CRG_CFG0_00	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																right_mclk_div																
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27] RO		reserved	reserve.
[26:0] RW	science_mclk_div		The frequency division clock configuration value of mclk, the configuration value is (target mclk frequency/mclk clock source pll frequency)×2^27. Wherein mclk clock source pll frequency see 3.2 clock, the default is 1188M.

I2S_CRG_CFG1_00

I2S_CRG_CFG1_00 Configure register 1 for I2S00 CRG.

Offset Address	Register Name	Total Reset Value
0x0104	I2S_CRG_CFG1_00	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														science_bclk_div	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	aiao_srst_req	Independent soft reset request for RX0 channel. 0: cancel reset; 1: reset.
[8]	RW	science_cken	MCLK/BCLK/WS clock gating for CRG00. 0: off; 1: open.
[7]	RO	reserved	reserve.
[6:4]	RW	science_fsclk_div	Frequency division relationship between bit clock BCLK and sampling clock FS. 000: FS is divided by 16 of BCLK; 001: FS is the 32 frequency division of BCLK; 010: FS is the 48 frequency division of BCLK; 011: FS is the 64 frequency division of BCLK; 100: FS is the 128 frequency division of BCLK; 101: FS is the 256 frequency division of BCLK; Others: FS is divided by 8 of BCLK.
[3:0]	RW	science_bclk_div	Frequency division relationship between main clock MCLK and bit clock BCLK. 0000: BCLK is divided by 1 of MCLK; 0001: BCLK is divided by 3 of MCLK; 0010: BCLK is divided by 2 of MCLK; 0011: BCLK is divided by 4 of MCLK; 0100: BCLK is divided by 6 of MCLK; 0101: BCLK is divided by 8 of MCLK; 0110: BCLK is 12 frequency division of MCLK; 0111: BCLK is 16 frequency division of MCLK; 1000: BCLK is divided by 24 of MCLK; 1001: BCLK is the 32 frequency division of MCLK; 1010: BCLK is 48 frequency division of MCLK; 1011: BCLK is 64 frequency division of MCLK; Others: BCLK is divided by 8 of MCLK.

I2S_CRG_CFG1_08

I2S_CRG_CFG1_08 Configure register 1 for I2S08 CRG.

Offset Address	Register Name	Total Reset Value
0x0144	I2S_CRG_CFG1_08	0x0000_0131

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	aiao_srst_req	Independent soft reset request for TX0 channel. 0: cancel reset; 1: Reset.
[8:0]	RO	reserved	reserve.

RX_IF_ATTRI

RX_IF_ATTRI Sets the register for the interface attribute of the receive channel.

Offset Address	Register Name	Total Reset Value
0x1000	RX_IF_ATTRI	0xE400_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_sd_source_sel	rx_sd_offset
Reset	1 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	rx_sd_source_sel	Configured to 0x1000 for normal operation.
[19]	RO	reserved	reserve.

[18:16] RW rx_trackmode			I²S In S mode, left and right channel mode control. 000: no processing; 001: Both channels are left channel sound; 010: Both channels are right channel sound; 011: Two channels are interchanged; 100: The output of the left and right channels is the addition of the left and right channels; 101: The left channel is muted, and the right channel plays the original right channel sound; 110: The right channel is muted, and the left channel plays the original left channel sound; 111: The left and right channels are muted. 说明 When receiving on 1ch, trackmode is still valid.
[15:8] RW rx_sd_offset			In PCM mode, data is delayed by BCLK cycles relative to WS signal. 0x0: left justified mode; 0x1: standard mode; others: reserved.
[7]	RO	reserved	reserve.
[6:4] RW rx_ch_num			Received channel number selection. 00: 1 channel (ch) receiving; 01: 2 channels (ch) receiving; Others: reserved;
[3:2] RW rx_i2s_precision			Data sampling precision configuration bits. I2S mode: 01ÿ16bitÿ 10ÿ24bitÿ Other: reserved. PCM mode: 01ÿ16bitÿ Other: reserved.
[1:0] RW rx_mode			Interface mode selection for the receive channel. 00ÿI²S mode; 01: PCM mode; Others: Reserved.

RX_DSP_CTRL

RX_DSP_CTRL is the control register of the receive processing channel.

Offset Address	Register Name	Total Reset Value
0x1004	RX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	—	—	reserved																												
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:30]	RO reserved	reserve.
[29]	RO rx_disable_done	The stop completion flag of the receiving channel. 0: disable not completed; 1: disable complete.
[28]	RW rx_enable	Receive channel start, stop control bit. 0: stop; 1: start.
[27]	RW bypass_en	Data processing prohibition bit, the control function is still valid. 0: Perform data processing normally; 1: Do not perform operations such as trackmode.
[26:0]	RO reserved	reserve.

RX_BUFF_SADDR

RX_BUFF_SADDR is the DDR buffer start address register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x1080	RX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW rx_buff_saddr	DDR buffer start address of receive channel 0, in bytes. 说明 The DDR buffer start address requires 128 × 8 bit alignment.

RX_BUFF_SIZE

RX_BUFF_SIZE is the DDR buffer size register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x1084	RX_BUFF_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / rx_buff_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	rx_buff_size	DDR buffer size for the receive channel, in bytes. 说明 It is required that rx_buff_size be an integer multiple of 128 bytes.

RX_BUFF_WPTR

RX_BUFF_WPTR is the DDR buffer write address register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x1088	RX_BUFF_WPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / rx_buff_wptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	rx_buff_wptr	The DDR buffer write address of the receive channel, in bytes. 说明 The write address in the receiving direction is maintained by the logic, which is the offset relative to the start address of the DDR buffer. address. Requires 128 × 2 bit alignment.

RX_BUFF_RPTR

RX_BUFF_RPTR is the DDR buffer read address register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x108C	RX_BUFF_RPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_buff_rptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:0]	RW rx_buff_rptr	The DDR buffer read address of the receive channel, in bytes. 说明 The read address in the receive direction is maintained by software and is the offset address relative to the start address of the DDR buffer. The software uses bytes as the unit, and the hardware internally operates according to 128×2 bit alignment

RX_BUFF_ALFULL_TH

RX_BUFF_ALFULL_TH DDR buffer almost full watermark register for receive channel.

Offset Address	Register Name	Total Reset Value
0x1090	RX_BUFF_ALFULL_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_buff_alfull_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:24]	RO reserved	reserve.
[23:0]	RW rx_buff_alfull_th	The DDR buffer of the receive channel is almost watermarked in bytes. When the DDR cache writable space is less than the almost full watermark, an almost full raw interrupt is generated. 说明 If rx_alfull_int interrupt is used, rx_buff_alfull_th is required to be configured as a 16-byte integer Several times, and greater than or equal to 0x40.

RX_TRANS_SIZE

RX_TRANS_SIZE is the data transfer length register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x1094	RX_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rx_trans_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:0]	RW rx_trans_size		The receiving channel generates a transmission completion interrupt when the audio data of rx_trans_size length (in bytes) is received.

RX_INT_ENA

RX_INT_ENA is the interrupt enable register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x10A0	RX_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:8]	RO	reserved	reserve.
[7]	RW	interrupt is enabled. this one rx_if_full_lost_int_	The interface data of the receiving channel is full and the raw 0: Disable; 1: Enable.
[6]	RO	reserved	reserve.
[5]	RW rx_stop_int_ena		Stop interrupt enable for receive channel. 0: disable; 1: enable.
[4]	RO	reserved	reserve.

[3] RW		channel. rx_bfifo_full_int_e already	Bus fifo overflow interrupt enable for receive 0: disable; 1: enable.
[2] RW	rx_alfull_int_ena		The DDR buffer almost full interrupt for the receive channel is enabled. 0: disable; 1: enable.
[1] RW	rx_full_int_ena		DDR buffer full interrupt enable for receive channel. 0: disable; 1: enable.
[0] RW	rx_trans_int_ena		The transfer complete interrupt enable for the receive channel. 0: disable; 1: enable.

RX_INT_RAW

RX_INT_RAW is the raw interrupt register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x10A4	RX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RO	original interrupt is lost. raw rx_if_full_lost_int_	The interface data of the receiving channel is full and the 0: no raw interrupt; 1: There is a raw interrupt.
[6]	RO	reserved	reserve.

[5]	RO	rx_stop_int_raw	Receive channel's stop raw interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[4]	RO	reserved	reserve.
[3]	RO	rx_bfifo_full_int_ra 0: no raw In	Receive channel's bus fifo overflow raw interrupt. interrupt; 1: There is a raw interrupt.
[2]	RO	rx_alfull_int_raw	The DDR buffer of the receive channel is almost full of raw interrupts. 0: no original interrupt; 1: There is a raw interrupt.
[1]	RO	rx_full_int_raw	The DDR buffer of the receive channel is full of raw interrupts. 0: no original interrupt; 1: There is a raw interrupt.
[0]	RO	rx_trans_int_raw	Receive channel's transfer complete raw interrupt. 0: no original interrupt; 1: There is a raw interrupt.

RX_INT_STATUS

RX_INT_STATUS is the interrupt status register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x10A8	RX_INT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

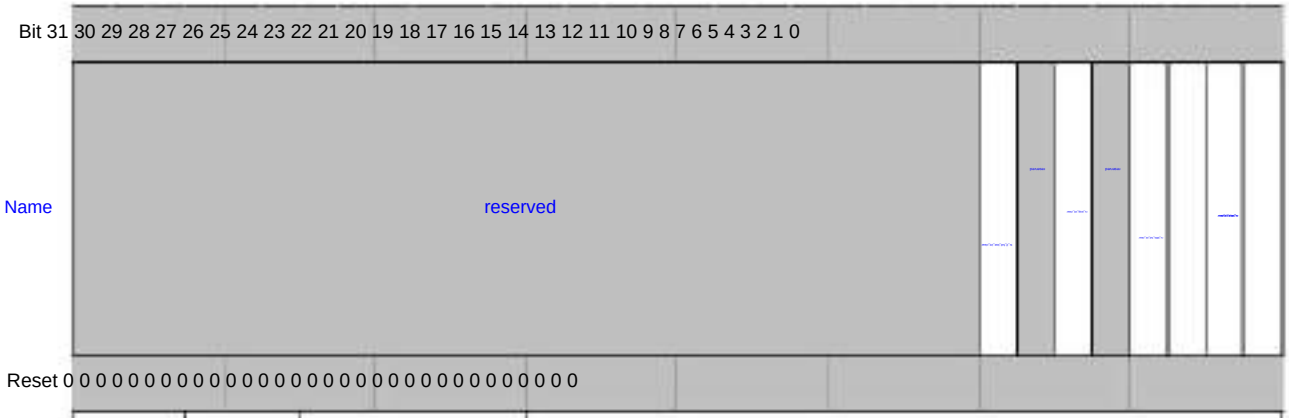
Bits	Access Name		Description
[31:8]	RO	reserved	reserve.

[7]	RO	channel. tx_if_full_lost_int_ 0:	The interface data full loss interrupt status of the sending no interrupt status; status 1: There is an interrupt status.
[6]	RO	reserved	reserve.
[5]	RO	rx_stop_int_status	Receive channel stop interrupt status. 0: no interrupt status; 1: There is an interrupt status.
[4]	RO	reserved	reserve.
[3]	RO	rx_bfifo_full_int_st 0: no hundred	Receive channel bus fifo overflow interrupt status. interrupt status; 1: There is an interrupt status.
[2]	RO	rx_alfull_int_status 1: interrupt	Receive channel DDR buffer almost full interrupt status. 0: no interrupt status; status.
[1]	RO	rx_full_int_status	Receive channel's DDR buffer full interrupt status. 0: no interrupt status; 1: There is an interrupt status.
[0]	RO	rx_trans_int_status	Receive channel's transfer complete interrupt status. 0: no interrupt status; 1: There is an interrupt status.

RX_INT_CLR

RX_INT_CLR is the interrupt clear register of the receive channel.

Offset Address	Register Name	Total Reset Value
0x10AC	RX_INT_CLR	0x0000_0000

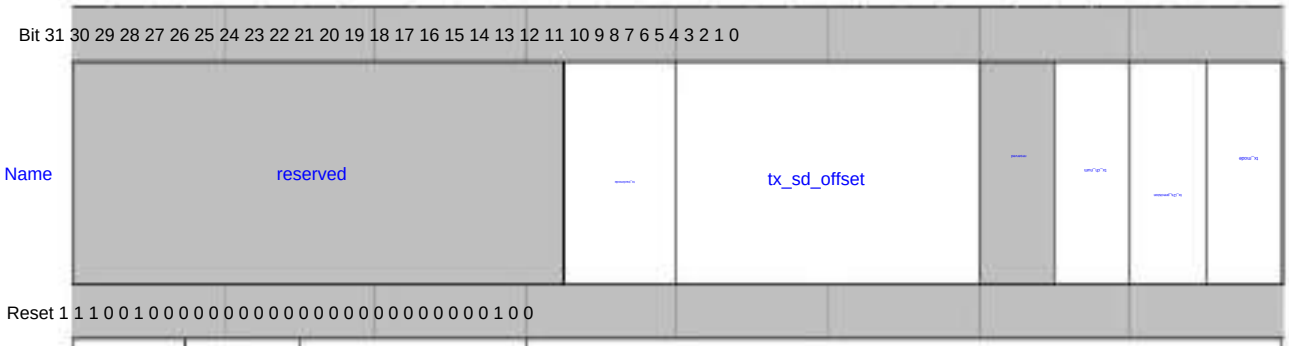


Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7] WC		channel is cleared. not tx_if_full_lost_int_ 0: Do clear; clear 1: Clear stop interrupt.	The interface data full loss interrupt of the sending
[6]	RO	reserved	reserve.
[5] WC rx_stop_int_clear			Stop interrupt clear bit for receive channel. 0: do not clear; 1: Clear stop interrupt.
[4]	RO	reserved	reserve.
[3] WC		rx_bfifo_full_int_cl 0: do not clear; ear	Bus fifo overflow interrupt clear bit for receive channel. 1: Clear fifo overflow interrupt.
WC rx_alfull_int_clear			Receive channel DDR buffer almost full interrupt clear bit. 0: not clear; [2] 1: Clear DDR buffer almost full interrupt.
[1] WC rx_full_int_clear			Receive channel DDR buffer full interrupt clear bit. 0: do not clear; 1: Clear DDR buffer full interrupt.
[0] WO rx_trans_int_clear			Receive channel transfer complete interrupt clear bit. 0: do not clear; 1: Clear transfer complete interrupt.

TX_IF_ATTRI

TX_IF_ATTRI Sets the register for the interface attribute of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x2000	TX_IF_ATTRI	0xE400_0004



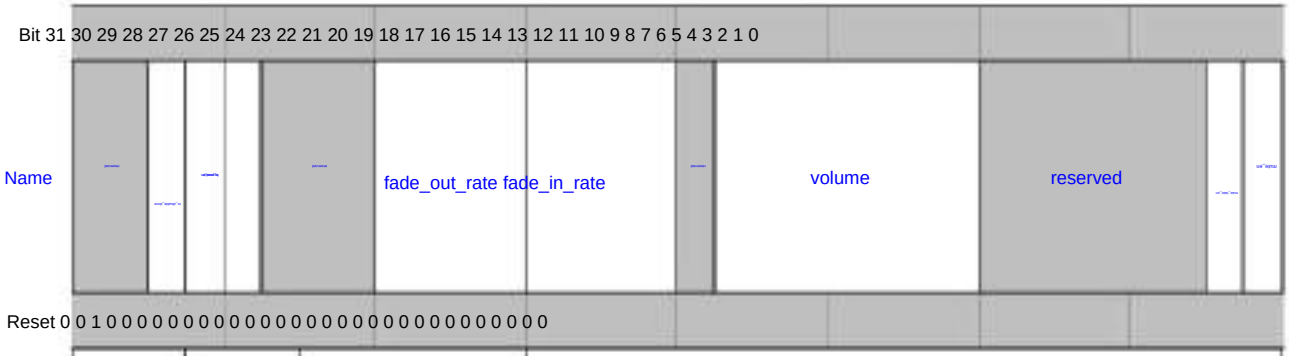
Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18:16]	RW	tx_trackmode	I²S In S mode, left and right channel mode control. 000: no processing; 001: Both channels are left channel sound; 010: Both channels are right channel sound; 011: The two channels are swapped; 100: The output of the left and right channels is the addition of the left and right channels; 101: The left channel is muted, and the right channel plays the original right channel sound; 110: The right channel is muted, and the left channel plays the original left channel sound; 111: The left and right channels are muted. 说明 When receiving on 1ch, trackmode is still valid.
[15:8]	RW	tx_sd_offset	In PCM mode, data is delayed by BCLK cycles relative to WS signal. 0x0: left- aligned mode; 0x1: standard mode; Other: reserved.
[7:6]	RW	reserved	reserve.
[5:4]	RW	tx_ch_num	Send channel selection. 00: Mono transmission; 01: Stereo transmission; Other: reserved.

[3:2] RW	tx_i2s_precision		Data sampling precision configuration bits. I2S mode: 01ÿ16bitÿ 10ÿ24bitÿ Other: reserved. PCM mode: 01ÿ16bitÿ Other: reserved.
[1:0] RW	tx_mode		Interface mode selection for the send channel. 00: I2S mode; 01: PCM mode; Other: reserved.

TX_DSP_CTRL

TX_DSP_CTRL is the control register of the transmit processing channel.

Offset Address	Register Name	Total Reset Value
0x2004	TX_DSP_CTRL	0x2000_0000



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RO	tx_disable_done	Send the stop completion flag of the channel. 0: not completed; 1: Done.
[28]	RW	tx_enable	Send the start and stop control bits of the channel. 0: stop; 1: start.

[27] RW	bypass_en		Data processing prohibition bit, the control function is still valid. 0: Normal data processing; 1: Do not perform calculations such as trackmode and volume processing.
[26:24] RO		reserved	reserve.
[23:20] RW	fade_out_rate		Fade out speed. 0000: 1 sampling point is changed once; 0001: 2 sampling points are changed once; 0010: 4 sampling points are changed once; 0011: 8 sampling points are changed once; 0100: 16 sampling points are changed once; 0101: 32 sampling points are changed once; 0110: 64 sampling points are changed once; 0111: 128 sampling points are changed once; others: reserved.
[19:16] RW	fade_in_rate		Fade in speed. 0000: 1 sampling point is changed once; 0001: Change once for 2 sampling points; 0010: Change once for 4 sampling points; 0011: Change once for 8 sampling points; 0100: Change once for 16 sampling points; 0101: Change once for 32 sampling points; 0110: Change once for 64 sampling points 0111: 128 sampling points are changed once; Other: reserved.
[15] RO		reserved	reserve.
[14:8] RW	volume		Volume, 1DB per division. 0x00~0x28: Mute; 0x29ÿ–80dBÿ 0x2Aÿ–79dBÿ …… 0x75ÿ-4dBÿ 0x77ÿ-2dBÿ 0x79ÿ+0dBÿ 0x7Bÿ+2dBÿ 0x7Dÿ+4dBÿ 0x7F: +6dB (maximum).

[7:2] RO		reserved	reserve.
[1] RW	mute_fade_en		Silent fade control. 0: Fade in and fade out function is off; 1: The fade in and fade out function is turned on.
[0] RW	Mute		Mute control. 0: mute cancel; 1: Mute enabled.

TX_BUFF_SADDR

TX_BUFF_SADDR is the DDR buffer start address register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x2080	TX_BUFF_SADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	tx_buff_saddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	tx_buff_saddr	The starting address of the DDR buffer of the sending channel, in bytes. 说明 The DDR buffer start address requires 128 × 8 bit alignment.

TX_BUFF_SIZE

TX_BUFF_SIZE is the DDR buffer size register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x2084	TX_BUFF_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / tx_buff_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_buff_size	The DDR buffer size of the transmit channel, in bytes. 说明 It is required that tx_buff_size is an integer multiple of 128 bytes.

TX_BUFF_WPTR

TX_BUFF_WPTR is the DDR buffer write address register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x2088	TX_BUFF_WPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_buff_wptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_buff_wptr	DDR buffer write address of transmit channel. 说明 The write address in the sending direction is maintained by software and is relative to the start address of the DDR buffer. address. Software must ensure that the free space of TX_BUF is not less than 128 bytes. The software takes the byte as the unit, and the internal hardware operates according to the 128×2 bit alignment.

TX_BUFF_RPTR

TX_BUFF_RPTR is the DDR buffer read address register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x208C	TX_BUFF_RPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_buff_rptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_buff_rptr	DDR buffer read address of transmit channel. 说明 The read address in the send direction is logically maintained and is an offset relative to the start address of the DDR cache address. Note: 128 × 2 bit alignment is required.

TX_BUFF_ALEMPTY_TH

TX_BUFF_ALEMPTY_TH DDR buffer almost empty watermark register for transmit channel.

Offset Address	Register Name	Total Reset Value
0x2090	TX_BUFF_ALEMPTY_TH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_buff_alempty_th
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_buff_alempty_th	The DDR buffer of the transmit channel is almost empty, in bytes. When the DDR cache readable space is less than the almost empty watermark, an almost empty raw interrupt is generated. 说明 If tx_alempty_int interrupt is used, it is required that tx_buff_alempty_th be configured as an integer multiple of 16 bytes and be greater than or equal to 0x20.

TX_TRANS_SIZE

TX_TRANS_SIZE is the data transmission length register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x2094	TX_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_trans_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	tx_trans_size	Transmitting channel, when the audio data transmission of tx_trans_size length (in bytes) is completed, a transmission completion interrupt will be generated.

TX_INT_ENA

TX_INT_ENA is the interrupt enable register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x20A0	TX_INT_ENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RW	tx_dat_break_int_e	The interface data cut-off interrupt of the transmit channel is enabled. 0: no raw break already; 1: There is a raw interrupt.
[6]	RW	tx_mfade_int_ena	Mute fade complete interrupt enable for transmit channel. 0: disable; 1: enable.
[5]	RW	tx_stop_int_ena	Stop interrupt enable for transmit channel. 0: disable; 1: enable.
[4]	RW	tx_ififo_empty_int	Interface fifo underflow interrupt enable for transmit channel. 0: disable; 1: enable.
[3]	RW	tx_bfifo_empty_int	Bus fifo underflow interrupt enable for transmit channel. 0: disable; 1: enable.
[2]	RW	tx_alempty_int_ena	The DDR buffer almost empty interrupt for the transmit channel is enabled. 0: Disable; 1: Enable.
[1]	RW	tx_empty_int_ena	DDR buffer empty interrupt enable for transmit channel. 0: disable; 1: enable.

[0] RW	tx_trans_int_ena		Transmit complete interrupt enable for transmit channel. 0: disable; 1: enable.

TX_INT_RAW

TX_INT_RAW is the raw interrupt register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x20A4	TX_INT_RAW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RO	tx_dat_break_int_r	The interface data cut-off of the send channel is the original interrupt. 0: no raw break; 1: There is a raw interrupt.
[6]	RO	tx_mfade_int_raw	A mute fade of the send channel completes the original interruption. 0: no original interrupt; 1: There is a raw interrupt.
[5]	RO	tx_stop_int_raw	Send channel's stop raw interrupt. 0: no original interrupt; 1: There is a raw interrupt.
[4]	RO	tx_ififo_empty_int_raw	Interface fifo underflow raw interrupt for transmit channel. 0: no raw interrupt; 1: There is a raw interrupt.
[3]	RO	tx_bfifo_empty_int_raw	Transmit channel's bus fifo underflow raw interrupt. 0: no raw interrupt; 1: There is a raw interrupt.

[2]	RO	tx_alempty_int_ra ln	The DDR buffer of the transmit channel is almost empty for raw interrupts. 0: no original interrupt; 1: There is a raw interrupt.
[1]	RO	tx_empty_int_raw	DDR buffer empty raw interrupt for transmit channel. 0: no original interrupt; 1: There is a raw interrupt.
[0]	RO	tx_trans_int_raw	The transmit channel's transfer complete raw interrupt. 0: no original interrupt; 1: There is a raw interrupt.

TX_INT_STATUS

TX_INT_STATUS is the interrupt status register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x20A8	TX_INT_STATUS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RO	channel. tx_dat_break_int_st 0: original break.	The interface data interruption status of the sending no original break; atus 1:
[6]	RO	tx_mfade_int_statu s	Mute fade complete interrupt status bit for transmit channel. 0: no interrupt status; 1: There is an interrupt status.
[5]	RO	tx_stop_int_status	Send the stop interrupt status of the channel. 0: no interrupt status; 1: There is an interrupt status.

[4]	RO	tx_ififo_empty_int 0: no interrupt	Transmit channel's interface fifo underflow interrupt status. status; _status 1: There is an interrupt status.
[3]	RO	tx_bfifo_empty_int 0: no interrupt	Transmit channel's bus fifo underflow interrupt status. status; _status 1: There is an interrupt status.
[2]	RO	condition. tx_alempty_int_stat 0: no interrupt status; us 1: There is an interrupt status.	The DDR buffer of the transmit channel is almost empty interrupt
[1]	RO	tx_empty_int_statu 0: no interrupt status; s 1: There is an interrupt status.	DDR buffer empty interrupt status of transmit channel.
[0]	RO	tx_trans_int_status	Send channel's transfer complete interrupt status. 0: no interrupt status; 1: There is an interrupt status.

TX_INT_CLR

TX_INT_CLR is the interrupt clear register of the transmit channel.

Offset Address	Register Name	Total Reset Value
0x20AC	TX_INT_CLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7]	RO	is cleared. tx_dat_break_int_clear	The interface data interruption interrupt of the sending channel 0: no raw break; 1: There is a raw interrupt.

[6] WC	tx_mfade_int_clear		Mute fade complete interrupt clear bit for transmit channel. 0: do not clear; 1: Clear stop interrupt.
[5] WC	tx_stop_int_clear		Stop interrupt clear bit for transmit channel. 0: do not clear; 1: Clear stop interrupt.
[4] WC		channel. tx_ififo_empty_int_clear	Interface fifo underflow interrupt clear bit for transmit 0: do not clear; 1: Clear fifo underflow interrupt.
[3] WC		channel. tx_bfifo_empty_int_clear	Bus fifo underflow interrupt clear bit for transmit 0: do not clear; 1: Clear fifo underflow interrupt.
[2] WC		channel. tx_alempty_int_clear	DDR buffer almost empty interrupt clear bit for transmit 0: do not clear; 1: Clear DDR cache almost empty interrupt.
clear; [1] WC	tx_empty_int_clear		DDR buffer empty interrupt clear bit for transmit channel. 0: not 1: Clear DDR buffer empty interrupt.
[0] WC	tx_trans_int_clear		Transmit complete interrupt clear bit for transmit channel. 0: do not clear; 1: Clear transfer complete interrupt.

11.2 Audio Codec

11.2.1 Overview

Hi3519V100 integrates high-performance Audio Codec, including high-quality stereo playback DAC (96dB DR A Weighted), supports two single-ended lineout outputs or one differential lineout output; high-quality stereo recording ADC (93dB DR A-Weighted), supports two stereo single-ended inputs or one differential input, microphone input supports -1.5~30dB, where -1.5dB~0dB is 1.5dB step size, 0dB~30dB is 2dB step size gain Control, the other boost gain is 20dB. I2S data interface, supports standard sampling rate from 8kHz to 192kHz, can support two sampling rates to work at the same time, and supports digital mixing.

11.2.2 Features

The Audio Codec module has the following features:

96dBA DR Stereo DAC

Stereo single-ended Lineout output or one differential lineout output

DAC digital volume control range: -121dBÿ6dB, 1dB step

93dBA DR Stereo ADC

ADC channel analog volume control range: -1.5~30dB, 2dB step size, the other boost gain is 20dB

ADC channel digital volume control range: -96dB ~ 30dB, 1dB step

Two selectable stereo single-ended inputs or one differential input

Provide internal microphone bias,

support master-slave mode I2S data interface, support 24/20/18/16bits, binary code audio sampling rate:

support 48kHz, 44.1kHz, 32kHz three series of sampling rates. The sampling rates of each series are as follows:

ÿ 32kHz series sampling rate includes 8kHz, 16kHz, 32kHz, 64kHz, 128kHz;

ÿ 44.1kHz series sampling rates include 11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHzÿ

ÿ The sampling rate of the 48kHz series includes 12kHz, 24kHz, 48kHz, 96kHz, and 192kHz.

Jitter tolerance of analog clock CLKIN of 50psRMS.

11.2.3 Functional Description

Audio Codec provides recording and playback functions. When recording, the analog signal is input from the microphone or line, after the analog part is amplified, then converted into a digital signal, and finally output from the I2S interface to realize the recording function and support stereo recording; during playback, the audio The signal is input from the I2S interface, and then converted into an analog signal output by the DAC, which supports stereo music playback.

recording mode

In the recording mode, the microphone or line input signal is input from the analog input terminal, converted to ADC after programmable gain, and then filtered and volume controlled by the digital part, and the final recorded data is output from the I2S interface to complete the entire recording function operation.

The operation process is as follows:

Step 1. Power on the power supply, wait for 1s and then the reference voltage starts to work normally.

Step 2. Configure the corresponding register value according to the register description.

Step 3. Input the analog audio signal to start the recording operation, and the signal is output from the I2S interface.

----Finish

play mode

In the playback mode, the audio signal is ^{2} The S interface is sent to the digital part of the DAC, which is filtered and volume controlled by the digital part. controlled from I, and then filtered by the analog part, and finally the analog audio signal is output from the Lineout port.

The operation process is as follows:

Step 1. Power on the power supply, and wait for 1s for the reference voltage to work normally.

Step 2. Configure the corresponding register value according to the register description.

Step 3. Send signal from I2S interface, and output analog music signal from Lineout.

----Finish

11.2.4 Audio Codec Register Overview

The AUDIO CODEC is directly controlled by registers in the peripheral controller whose base address is 0x1203_0000 (the offset address is divided into 0x00A0 ~ 0X00D8). There is no direct configuration of the interface.

11.2.5 Audio Codec Register Description

For register information, please refer to "3.5.5.1 Register Overview" and "3.5.5.2 Register Description".

Table of contents

illustration catalog

table of contents

12 peripheral equipment

12.1 I2C

12.1.1 Overview

I 2 The role of the C module is to complete the CPU to I 2 Read and write from slave devices connected on the C bus. When the CPU writes to the slave device During operation, the CPU configures the data 2 configuration registers of the C module, and then send control information and operands to the I 2 C communication registers of the I module through 2 After the C module parses the command, the data of the data channel register passes through the I 2 C bus send the bus; I is sent to the slave device, and the final state is fed back to the CPU through an interrupt after the transmission is completed. The process of CPU reading slave device data is similar to writing operation.

12.1.2 Functional Description

I 2 C has the following features:

The I of the Hi3519V100 chip 2 C is the Master interface, I 2 The working reference clock of C is 50MHz.

Bus arbitration when multi-master is supported. Support

Clock synchronization and Bit and Byte waiting. Support standard address (7bit) and extended

address (10bit). Can work in two speed modes: standard mode (100kbit/s), fast

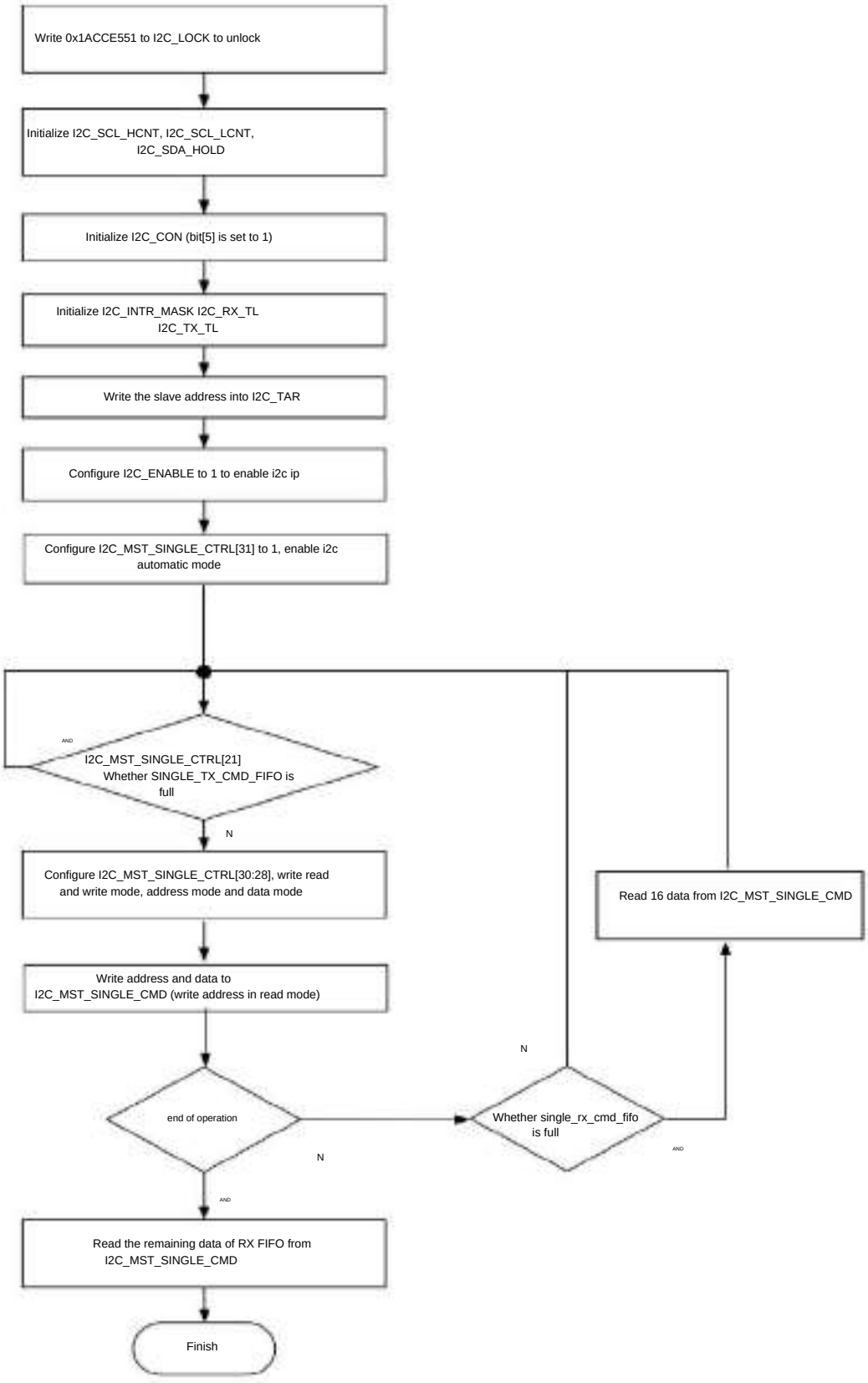
mode (400kbit/s). Support General Call and Start Byte functions. CBUS devices are not supported. DMA operations are supported.

12.1.3 Working method

The process of sending and receiving data in a single operation of the host

Figure 12-1 shows the process of sending and receiving data in a single operation of the host .

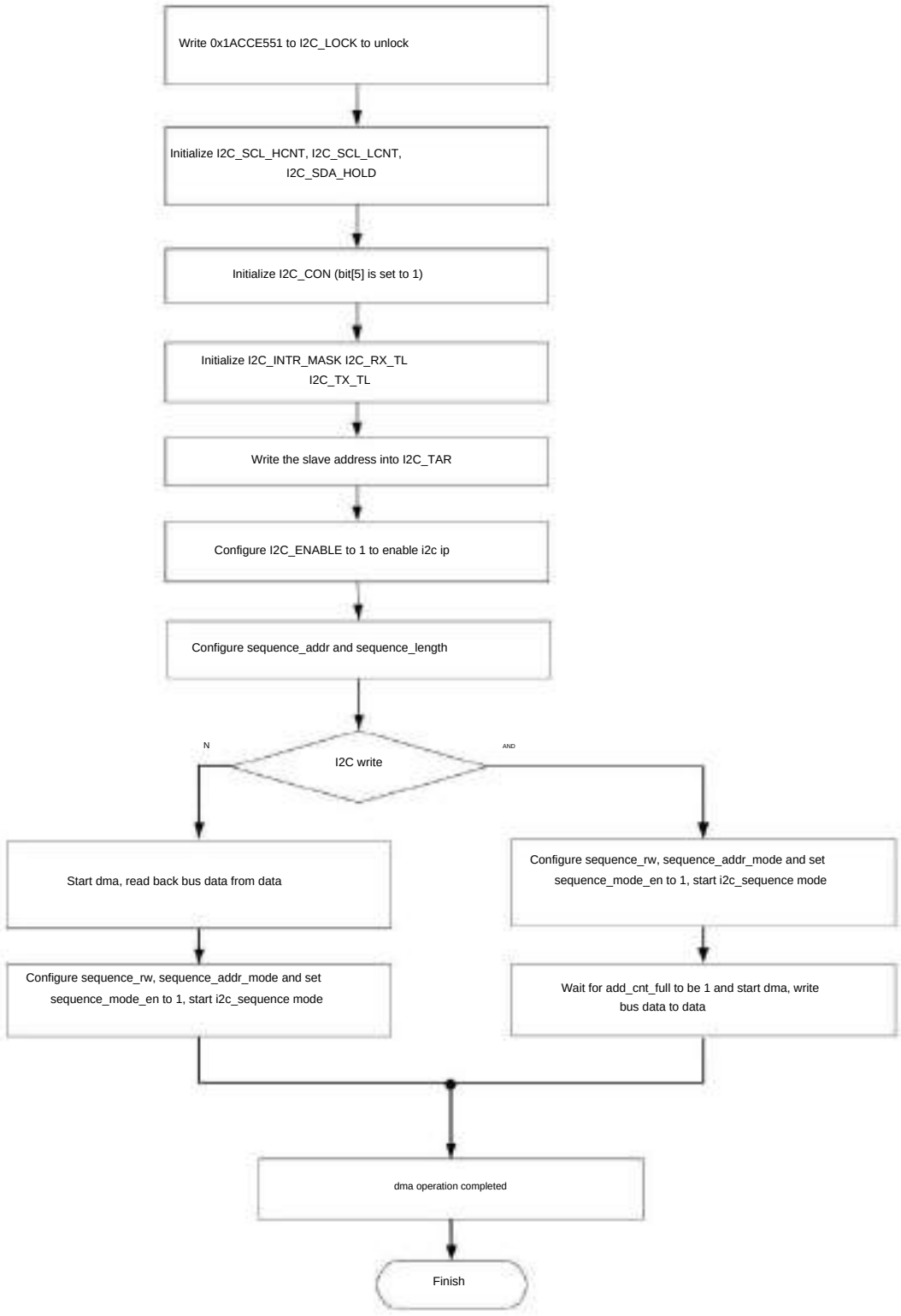
Figure 12-1 Flowchart of sending and receiving data in a single operation of the host



The host continuously sends and receives data process

Figure 12-2 shows the process of the host continuously sending and receiving data .

Figure 12-2 Flowchart of the host continuously sending and receiving data



12.1.4 Overview of I2C Registers

Hi3519V100 contains 4 I ^{2} C module, the register overview is shown in Table 12-1 .

Table 12-1 I2C register overview (the base addresses of I2C0, I2C1, I2C2 and I2C3 are 0x1211_0000, 0x1211_1000, 0x1211_2000 and 0x1211_3000 respectively)

offset address name		describe	page number
0x000	I2C_CON	I ^{2} C control register	12-5
0x004	I2C_TAR	I2C access Slave address register	12-6
0x010	I2C_DATA_CMD	I2C Transaction Register	12-6
0x01C	I2C_SCL_HCNT	I2C_SCL High Level Configuration Register	12-7
0x020	I2C_SCL_LCNT	I2C_SCL low level configuration register	12-8
0x02C	I2C_INTR_STAT	I2C Masked Interrupt Status Register	12-8
0x030	I2C_INTR_MASK	I2C Interrupt Mask Register	12-9
0x034	I2C_INTR_RAW	I2C Raw Interrupt Status Register	12-11
0x038	I2C_RX_TL	RX_FIFO watermark setting register	12-13
0x03C	I2C_TX_TL	TX_FIFO watermark setting register	12-13
0x040	I2C_CLR_INTR	I2C Interrupt Clear Register	12-14
0x06C	I2C_ENABLE	I2C Operation Enable Register	12-14
0x070	I2C_STATUS	I2C Status Register	12-15
0x074	I2C_TXFLR	TX_FIFO valid data indication register	12-16
0x078	I2C_RXFLR	RX_FIFO valid data indication register	12-16
0x07C	I2C_SDA_HOLD	SDA Hold Time Configuration Register	12-17
0x080	I2C_TX_ABRT_SRC	I2C transmit failure interrupt source register	12-17
0x088	I2C_DMA_CR	DMA interface control register for I2C	12-19
0x08C	I2C_DMA_TDLR	TX_FIFO DMA Operation Threshold Register 12-20	
0x090	I2C_DMA_RDLR	RX_FIFO DMA Operation Threshold Register 12-20	
0x0A0	I2C_SCL_SWITCH	I2C Anti-hangup Enable Register	12-20
0x0A4	I2C_SCL_SIM	I2C Anti-Hangup Analog Register	12-21
0x0AC	I2C_LOCK	I2C Lock Register	12-21

offset address	name	describe	page number
0x00B0	I2C_MST_SINGLE_CTRL	I2C_MST_SINGLE_CTRL Register 12-22	
0x00B4	I2C_MST_SINGLE_CMD	I2C_MST_SINGLE_CMD Register 12-24	
0x00B8	I2C_SEQUENCE_CMD0	I2C_SEQUENCE_CMD0 Register 12-25	
0x00BC	I2C_SEQUENCE_CMD1	I2C_SEQUENCE_CMD1 Register 12-26	
0x00C0	I2C_SEQUENCE_CMD2	I2C_SEQUENCE_CMD2 Register 12-26	

12.1.5 I2C Register Description

I2C_CON

I2C_CON is the I2C control register.

Offset Address	Register Name	Total Reset Value
0x000	I2C_CON	0x0000_0065

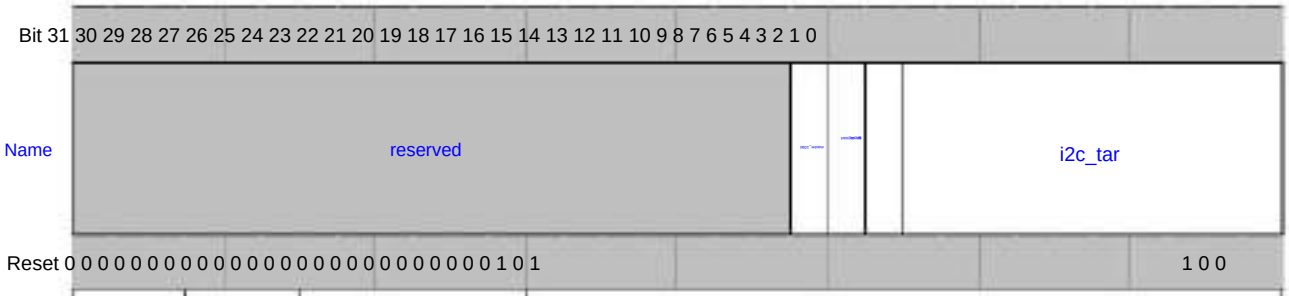
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 0 0 1 0 1

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RO	reserved	reserve.
[5]	RW	restart_en	Restart command sending enable in master mode. 0: forbidden; 1: enable. Note: If the Restart function is disabled, the following functions are not supported: 1. Send start byte 2. Read operation in 10bit addressing mode 3. Combined addressing mode
[4:0]	RO	reserved	reserve.

I2C_TAR

I2C_TAR is the I2C access slave address register.

Offset Address	Register Name	Total Reset Value
0x004	I2C_TAR	0x0000_002C



Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	master_10bit	Address length in master mode. 0ÿ7bitÿ 1ÿ10bitÿ
[11]	RW	special	General Call or Start Byte function is enabled. 0: forbidden; 1: enable.
[10]	RW	gc_or_start	When the Special bit is 1, this bit defines the I2C command executed. 0: General Call command (after sending the General Call command, only write operation can be performed; if read operation is performed, the tx_abort interrupt will be triggered) 1: Start Byte command.
[9:0]	RW	i2c_tar	The address of the Slave to be accessed when I2C is used as the Master. Note: If the slave address length is set to 7bit, only bit[6:0] is valid.

I2C_DATA_CMD

I2C_DATA_CMD is the I2C data operation register.

Offset Address	Register Name	Total Reset Value
0x010	I2C_DATA_CMD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	data	Data to be sent/received on the I2C bus. Read: Read the data received on the I2C bus; Write: The written data is sent to the I2C bus.

I2C_SCL_HCNT

I2C_SCL_HCNT is the I2C_SCL high level configuration register.

Offset Address	Register Name	Total Reset Value
0x01C	I2C_SCL_HCNT	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	i2c_scl_hcnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	i2c_scl_hcnt	Set the high-level time of the SCL clock, and the timing unit is the i2c working reference clock 50MHz. It is recommended to be 1/2 of the SCL period in standard mode and 1/2 in fast mode. 0.36 of the SCL period. That is, in standard mode: i2c_scl_hcnt=(fi2c / fSCL)*0.5; in fast mode: i2c_scl_hcnt=(fi2c / fSCL)*0.36; taking 400KHz in fast mode as an example, i2c_scl_hcnt=(50MHz / 400KHz)*0.36= 45. Notice: 1. Before I2C bus transmission, this domain must be configured correctly to get proper I/O timing. 2. Only when the I2C interface is disabled (I2C_ENABLE=0) can the write operation be performed.

I2C_SCL_LCNT

I2C_SCL_LCNT is the I2C_SCL low level configuration register.

Offset Address	Register Name	Total Reset Value
0x020	I2C_SCL_LCNT	0x0000_0010

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	i2c_scl_lcnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	i2c_scl_lcnt	Set the low-level time of the SCL clock, and the timing unit is the i2c working reference clock 50MHz. It is recommended to be 1/2 of the SCL period in standard mode and 1/2 in fast mode. 0.64 of the SCL period. That is, in standard mode: i2c_scl_lcnt=(fi2c / fSCL)*0.5; in fast mode: i2c_scl_lcnt=(fi2c / fSCL)*0.64; taking 400KHz in fast mode as an example, i2c_scl_lcnt=(50MHz / 400KHz)*0.64= 80. Note: 1. Before I2C bus transmission, this domain must be configured correctly to get proper I/O timing. 2. Only when the I2C interface is disabled (I2C_ENABLE=0) can the write operation be performed.

I2C_INTR_STAT

I2C_INTR_STAT is the I2C masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x02C	I2C_INTR_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:12]	RO	reserved	reserve.
[11]	RO	gen_call	The interrupt status when a general call request is received. 0: no interrupt; 1: There is an interrupt.

[10] RO		start_it	start detect Interrupt status indicating whether there is a START or RESTART condition on the I2C-bus interface. 0: no interrupt; 1: There is an interrupt.
[9]	RO	stop it	stop detect Interrupt status, indicating whether there is a STOP condition on the I2C bus interface. 0: no interrupt; 1: There is an interrupt.
[8]	RO	activity	activity Interrupt status, records I2C activity status until cleared. 0: no interrupt; 1: interrupt.
[7]	RO	reserved	reserve.
[6]	RO	tx_abrt	Send abort interrupt status. 0: no interrupt; 1: There is an interrupt.
[5]	RO	reserved	reserve.
[4]	RO	tx_empty	TX_FIFO reaches or falls below threshold interrupt status. 0: no interrupt; 1: interrupt.
[3]	RO	tx_over	TX_FIFO overflow interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	rx_full	RX_FIFO reached or exceeded threshold interrupt status. 0: no interrupt; 1: There is an interrupt.
[1]	RO	rx_over	RX_FIFO overflow interrupt status. 0: no interrupt; 1: interrupt.
[0]	RO	rx_under	Read data overflow (that is, CPU reads FIFO when RX_FIFO is empty) interrupt status. 0: no interrupt; 1: interrupt.

I2C_INTR_MASK

I2C_INTR_MASK is the I2C interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x030	I2C_INTR_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

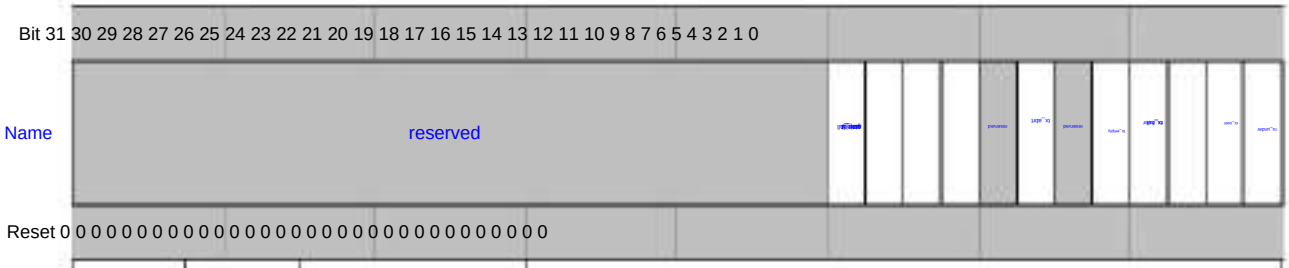
Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11]	RW	gen_call_mask	A general call request is masked by the received interrupt. 0: no shielding; 1: Shielded.
[10]	RW	start_it_mask	start detect interrupt mask. 0: no shielding; 1: Shielded.
[9]	RW	stop_it	stop detect interrupt mask. 0: no shielding; 1: Shielded.
[8]	RW	activity	Activity interrupt mask. 0: no shielding; 1: Shielded.
[7]	RO	reserved	reserve.
[6]	RW	tx_abrt	Transmit abort interrupt mask. 0: no shielding; 1: Shielded.
[5]	RO	reserved	reserve.
[4]	RW	tx_empty	TX_FIFO reached or below threshold interrupt mask. 0: no shielding; 1: Shielded.
[3]	RW	tx_over	TX_FIFO overflow interrupt mask. 0: no shielding; 1: Shielded.

[2] RW rx_full			RX_FIFO met or exceeded threshold interrupt mask. 0: no shielding; 1: Shielded.
[1] RW rx_over			RX_FIFO overflow interrupt mask. 0: no shielding; 1: Shielded.
[0] RW rx_under			Read data overflow (that is, CPU reads FIFO when RX_FIFO is empty) interrupt mask. 0: Not shielded; 1: Shielded.

I2C_INTR_RAW

I2C_INTR_RAW is the I2C raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x034	I2C_INTR_RAW	0x0000_0000



Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11]	RO	gen_call	The interrupt status when a general call request is received. 0: no interrupt; 1: Slave has received a General Call. Notice: Set to 1 only when the General Call address is received and confirmed. It remains until cleared.
[10]	RO	start_it	start detect Interrupt status indicating whether there is a START or RESTART condition on the I2C- bus interface. 0: No interrupt; 1: A START or RESTART condition was detected.

[9]	RO	stop it	stop detect Interrupt status, indicating whether there is a STOP condition on the I2C bus interface. 0: no interrupt; 1: A STOP condition has been detected.
[8]	RO	activity	activity Interrupt status, records I2C activity status until cleared. 0: in idle state; 1: In busy state.
[7]	RO	reserved	reserve.
[6]	RO	tx_abrt	Send abort interrupt status. 0: no interrupt; 1: There is an interrupt. Notice: When this bit is set to 1 , the I2C_TX_ABRT_SRC register indicates the reason for the transmit interrupt. Whatever it is, as long as this bit is set, the I2C will be cleared TX_FIFO. TX_FIFO will remain empty until this interrupt is cleared. Once the interrupt clear is performed, the TX_FIFO is ready to read more data from the APB interface.
[5]	RO	reserved	reserve.
[4]	RO	tx_empty	TX_FIFO reaches or falls below threshold interrupt status. 0: no interrupt; 1: There is an interrupt. Notice: When the amount of data in TX_FIFO exceeds the threshold, the hardware will automatically clear the interrupt. When I2C is disabled, TX_FIFO will be cleared.
[3]	RO	tx_over	TX_FIFO overflow interrupt status. 0: no interrupt; 1: There is an interrupt.
[2]	RO	rx_full	RX_FIFO reached or exceeded threshold interrupt status. 0: no interrupt; 1: There is an interrupt. Notice: This bit is set to 1 when the RX_FIFO is at or above the threshold set by I2C_RX_TL. When the RX_FIFO falls below the threshold, it is automatically cleared by hardware. When I2C is disabled, the RX_FIFO will be automatically cleared, and the interrupt will be automatically cleared.

[1]	RO	rx_over	RX_FIFO overflow interrupt status. 0: no interrupt; 1: There is an interrupt. Notice: This interrupt is set if the RX_FIFO is completely full and more bytes are received from the external I2C device. I2C will respond to data received on the I2C bus, but any data bytes received after the FIFO is full will be lost.
[0]	RO	rx_under	Read data overflow (that is, CPU reads FIFO when RX_FIFO is empty) interrupt status. 0: no interrupt; 1: There is an interrupt.

I2C_RX_TL

I2C_RX_TL is the RX_FIFO watermark setting register.

Offset Address	Register Name	Total Reset Value
0x038	I2C_RX_TL	0x0000_0003

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	rx_tl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1

Bits	Access Name		Description
[31:4]	RO	reserved	reserve.
[3:0]	RW rx_tl		RX_FIFO watermark setting (watermark level). Notice: The legal value is 0~15, and the actual value is the configuration value plus 1. When the number of data in RX_FIFO is greater than or equal to this value, the interrupt rx_full is triggered. The maximum value should depend on the RX_FIFO depth. When the configuration value is greater than the RX_FIFO depth, the watermark is configured as the RX_FIFO depth value by default.

I2C_TX_TL

I2C_TX_TL is the TX_FIFO watermark setting register.

Offset Address	Register Name	Total Reset Value
0x03C	I2C_TX_TL	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	tx_tl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	tx_tl	TX_FIFO watermark setting (watermark level). Notice: The legal value is 0~15, and the actual value is equal to the configured value. When the number of data in TX_FIFO is less than or equal to this value, an interrupt tx_empty is triggered. The maximum value should depend on the TX_FIFO depth. When the configuration value is greater than the TX_FIFO depth, the watermark is configured as the TX_FIFO depth value by default.

I2C_CLR_INTR

I2C_CLR_INTR is the I2C interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x040	I2C_CLR_INTR	0x0000_0000

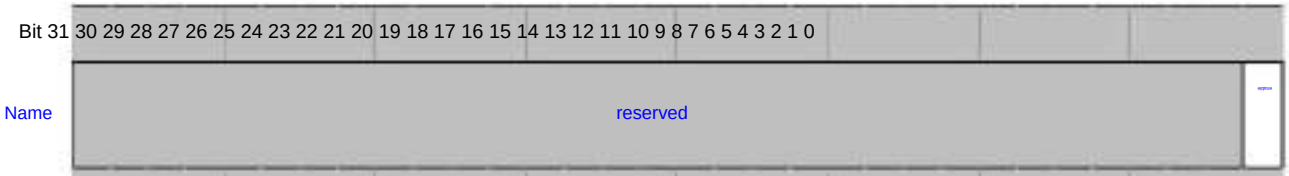
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	clr_intr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WO	clr_intr	Writing data "1" to this bit will clear the combined interrupt, all individual interrupts and the I2C_TX_ABRT_SRC register.

I2C_ENABLE

I2C_ENABLE is the I2C work enable register.

Offset Address	Register Name	Total Reset Value
0x06C	I2C_ENABLE	0x0000_0000

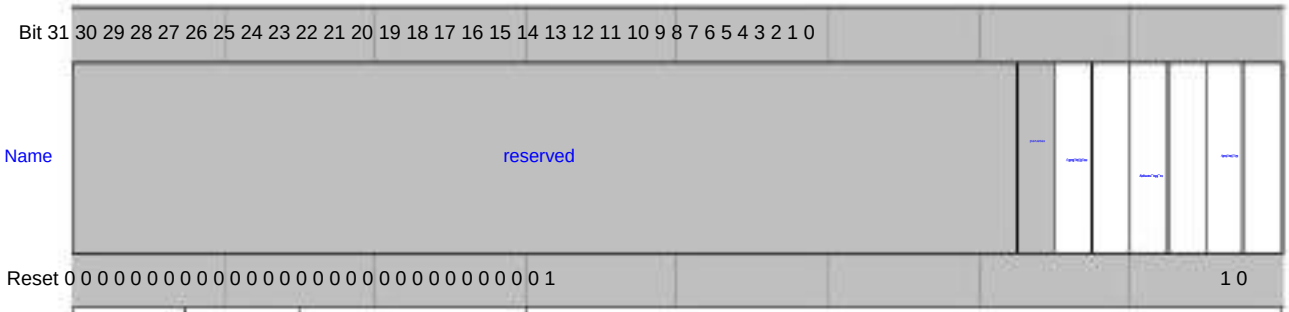


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	enable	I2C is enabled. 0: forbidden; 1: enable.

I2C_STATUS

I2C_STATUS is the I2C status register.

Offset Address	Register Name	Total Reset Value
0x070	I2C_STATUS	0x0000_0006



Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RO	reserved	reserve.
[5]	RO	mst_activity	I2C Master function active status. 0: Master enters the idle state, and the master mode part of I2C is inactive; 1: Master has not entered idle state, the master mode part of I2C is active.
[4]	RO	rx_fifo_full	RX_FIFO full flag. 0: less than full; 1: full.

[3]	RO	rx_fifo_nempty	RX_FIFO not empty flag. 0: empty; 1: not null.
[2]	RO	tx_fifo_nempty	TX_FIFO empty flag. 0: not empty; 1: Empty.
[1]	RO	tx_fifo_full	TX_FIFO not full flag. 0: full; 1: not full.
[0]	RO	i2c_activity	I2C working status. 0: idle; 1: Active.

I2C_TXFLR

I2C_TXFLR is the TX_FIFO valid data indication register.

Offset Address	Register Name	Total Reset Value
0x074	I2C_TXFLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / tx_flr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:5]	RO	reserved	reserve.
[4:0]	RO	tx_flr	The number of valid data in TX_FIFO. This register is cleared to 0 when a tx_abort interrupt occurs.

I2C_RXFLR

I2C_RXFLR is the RX_FIFO valid data indication register.

Offset Address	Register Name	Total Reset Value
0x078	I2C_RXFLR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / rx_flr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4:0]	RO	rx_flr	The number of valid data in RX_FIFO. This register is cleared to 0 when a tx_abort interrupt occurs.

I2C_SDA_HOLD

I2C_SDA_HOLD is the SDA hold time configuration register.

Offset Address	Register Name	Total Reset Value
0x07C	I2C_SDA_HOLD	0x0000_0001

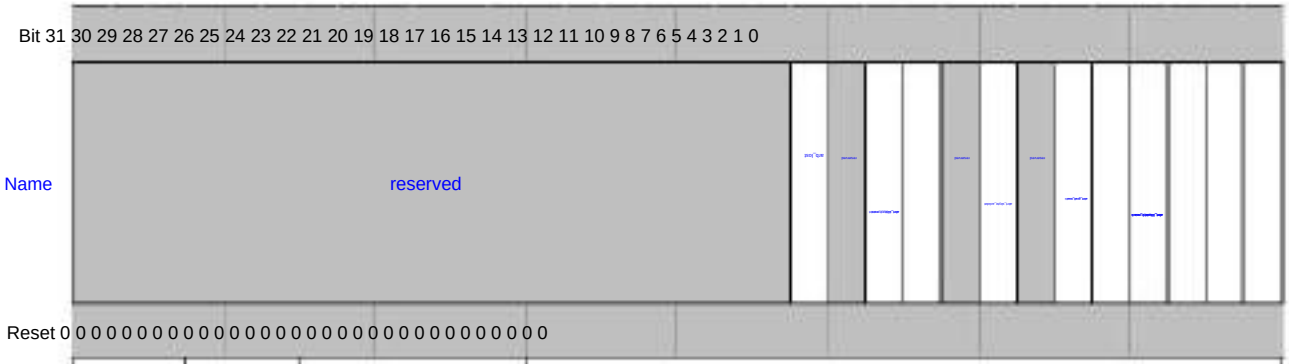
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / sda_hold_fs
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	sda_hold_fs	SDA hold time setting, the unit is 20ns, the recommended configuration is I2C_SCL_LCNT [i2c_scl_lcnt]/2. Note: This value is the delay count value from the falling edge of SCL to the change of SDA, that is, the data line SDA can only change in sda_hold_fs i2c_clk cycles after the falling edge of SCL. This value must be set according to the requirements of each speed mode.

I2C_TX_ABRT_SRC

I2C_TX_ABRT_SRC is the I2C transmit failure interrupt source register.

Offset Address	Register Name	Total Reset Value
0x080	I2C_TX_ABRT_SRC	0x0000_0000



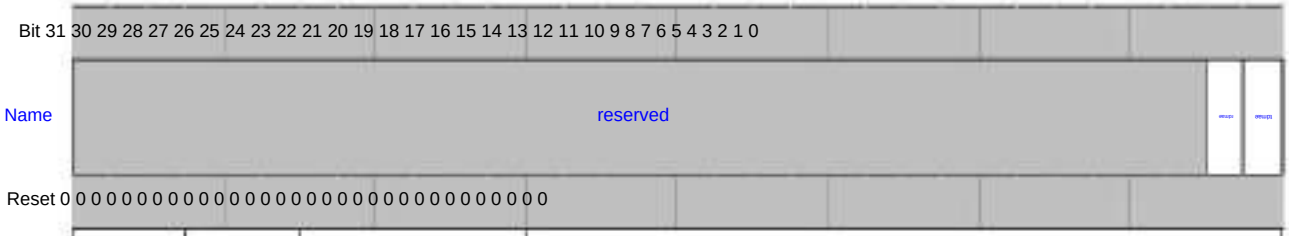
Bits	Access Name		Description
[31:13] RO		reserved	reserve.
[12] RO		arb_lost	The Master lost control of the bus causing an error. 0: no error; 1: There is an error.
[11] RO		reserved	reserve.
[10] RO		abrt_10b_rd_norstrt 0: no error;	The Restrt function is disabled (I2C_CON[restart_en]=0), and the Master tries to initiate a read operation in 10bit mode, resulting in an error. 1: There is an error.
[9]	RO	abrt_sbyte_norstrt	The Restart function is disabled (I2C_CON[restart_en]=0), and the user attempts to initiate a "Start" operation, resulting in an error. 0: no error; 1: There is an error.
[8]	RO	reserved	reserve.
[7]	RO	abrt_sbyte_ackdet	The Master issued a "start" command and got a response, resulting in an error. 0: no error; 1: There is an error. (the start command does not require Slave response).
[6]	RO	reserved	reserve.
[5]	RO	abrt_gcall_read	Sending failure tx_abort causes. 0: tx_abort is triggered due to the reason defined by this bit; 1: Master sends a general request, and the user initiates a read operation after sending the request.
[4]	RO	abrt_gcall_noack	Sending failure tx_abort causes. 0: tx_abort is triggered due to the reason defined by this bit; 1: Master sends a general request, but there is no slave response on the bus.

[3]	RO	abrt_txdata_noack	Sending failure tx_abort causes. 0: tx_abort is triggered due to the reason defined by this bit; 1: After the address sent by the Master to the Slave has been responded, the data sent by the Master has not been responded.
[2]	RO	abrt_10addr2_noack 1: Master is in 10bit address mode. The address [10:8] sent for the second time did not get a response from the Slave on the bus.	Sending failure tx_abort causes. 0: tx_abort is triggered by the cause defined by this bit;
[1]	RO	abrt_10addr1_noack 1: Master is in 10bit address mode. The address [7:0] sent for the first time did not get a response from the Slave on the bus.	Sending failure tx_abort causes. 0: tx_abort is triggered by the reason defined by this bit;
[0]	RO	abrt_7b_addr_noack 1: When the Master is in 7-bit address mode, the address sent by the master has not been responded by any Slave on the bus.	Sending failure tx_abort causes. 0: tx_abort is triggered by the cause defined by this bit;

I2C_DMA_CR

I2C_DMA_CR is the I2C DMA interface control register.

Offset Address	Register Name	Total Reset Value
0x088	I2C_DMA_CR	0x0000_0000



Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.
[1]	RW	rdmae	The DMA interface to the transmit FIFO is enabled. 0: forbidden; 1: enable.
[0]	RW	tdmae	The DMA interface to the receive FIFO is enabled. 0: forbidden; 1: enable.

I2C_DMA_TDLR

I2C_DMA_TDLR is the TX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x08C	I2C_DMA_TDLR	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dma_txtl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	dma_txtl	Transmit FIFO DMA operation threshold. When the number of sending FIFO data is less than or equal to this value, initiate a DMA operation request. DMA will move data to send FIFO.

I2C_DMA_RDLR

I2C_DMA_RDLR is the RX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x090	I2C_DMA_RDLR	0x0000_0004

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved dma_rxtl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	dma_rxtl	Receive FIFO DMA operation threshold. When the number of receiving FIFO data is greater than or equal to this value, initiate a DMA operation request. DMA will move the data in the receive FIFO to the designated location. The actual value is equal to the configured value + 1.

I2C_SCL_SWITCH

I2C_SCL_SWITCH ÿ I ^{2}C Anti-hangup enable register.

Offset Address	Register Name	Total Reset Value
0x0A0	I2C_SCL_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:1]	RO reserved	reserve.
[0]	RW scl_switch	Simulate SCL enable signal when acting as Master. 0: disable simulation; 1: Emulation enabled.

I2C_SCL_SIM

I2C_SCL_SIM is the I2C anti-hang simulation register.

Offset Address	Register Name	Total Reset Value
0x0A4	I2C_SCL_SIM	0x0000_0001

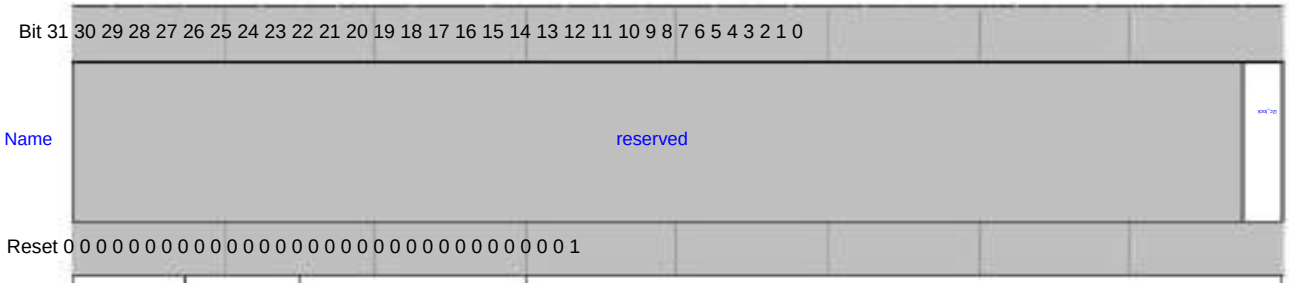
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_sim
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access Name	Description
[31:1]	RO reserved	reserve.
[0]	RW scl_sim	Simulated SCL signal when used as Master. 0: Output SCL is 0; 1: Output SCL is 1.

I2C_LOCK

I2C_LOCK is the I2C lock register.

Offset Address	Register Name	Total Reset Value
0x0AC	I2C_LOCK	0x0000_0001

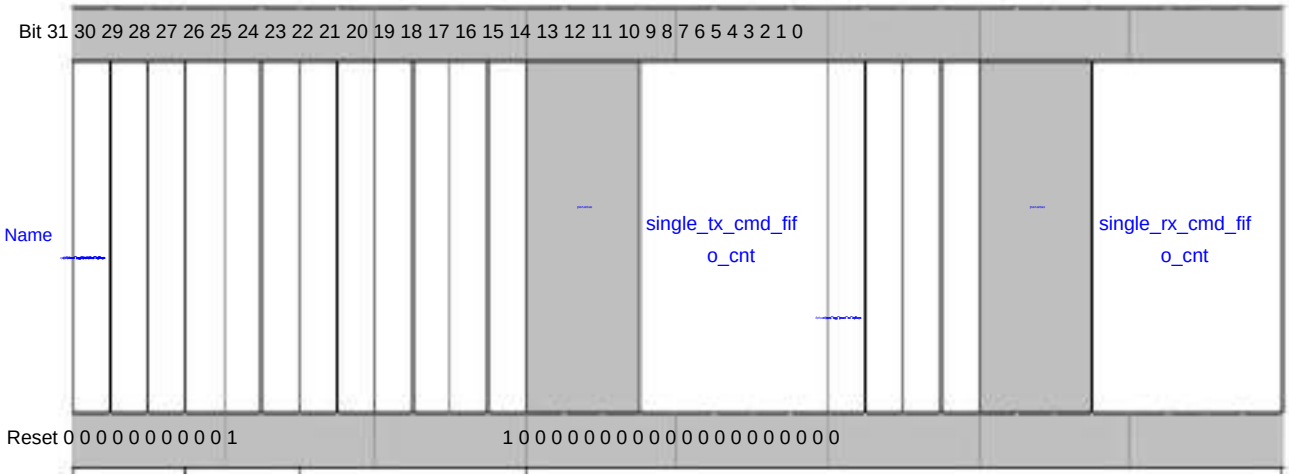


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	i2c_lock	I2C lock register. Write 1ACCE551 to this register to unlock it, and write other values to lock it. When reading back from this register, 0: unlock register, all registers can be configured; 1: lock register, only this register can be configured.

I2C_MST_SINGLE_CTRL

I2C_MST_SINGLE_CTRL is the I2C_MST_SINGLE_CTRL register.

Offset Address	Register Name	Total Reset Value
0x00B0	I2C_MST_SINGLE_CTRL	0x0030_0000



Bits	Access	Name	Description
[31]	RW	single_model_en	i2c master one-shot function enable control. 0: off; 1: open.

[30] RW	single_model		i2c master single operation function mode control. 0: write; 1: Read.
of slave is 8bits; [29] RW	single_addr_model		i2c master single operation function address mode control. 0: The register address 1: The slave register address is 16bits.
[28] RW	single_data_model		i2c master single operation function data mode control. 0: The register data of slave is 8bits; 1: The register data of slave is 16bits.
[27] WC		single_mst_tx_abrt Single _clr	operation mode transmit failure indication is cleared.
[26] WC		single_tx_cmd_fifo _over_clr	SINGLE_TX_FIFO overflow indication cleared.
[25] WC		single_rx_cmd_fifo _under_clr	SINGLE_RX_FIFO Read data overflow indication clear.
[24] WC		single_rx_cmd_fifo _over_clr	SINGLE_RX_FIFO overflow indication cleared.
[23] RO		single_mst_tx_abrt	Single operation mode sends failure indication. 0: None; 1: There is a sending failure.
[22] RO		single_tx_cmd_fifo 0: _over	SINGLE_TX_FIFO overflow indication. no overflow; 1: There is an overflow.
[21] RO		single_tx_cmd_fifo 0:	SINGLE_TX_FIFO not full indication. full, fifo data is not less than 16; _not_full 1: Not full, fifo data is less than 16.
[20] RO		indication. single_tx_cmd_fifo 0: not empty, there is data in fifo; _empty	SINGLE_TX_FIFO empty 1: Empty, there is no data in the fifo.
[19:17] RO		reserved	reserve.
[16:12] RO		single_tx_cmd_fifo is _cnt 0), this register is cleared to 0.	The number of valid data in SINGLE_TX_FIFO. When the I2C master single operation function is disabled (I2C_MST_SINGLE_CTRL[31]

[11] RO		single_rx_cmd_fifo 0: No	Read data overflow (that is, CPU reads FIFO when SINGLE_RX_FIFO is empty) status. read data overflow; _under 1: There is read data overflow.
[10] RO		single_rx_cmd_fifo 0: no	SINGLE_RX_FIFO overflow status. overflow; _over 1: There is an overflow.
[9]	RO	single_rx_cmd_fifo 0: not data is not less than 16.	SINGLE_RX_FIFO full indication. full, fifo data is less than 16; _full 1: full, fifo
[8]	RO	single_rx_cmd_fifo 0:	SINGLE_RX_FIFO not empty indication. empty, fifo has no data; _not_empty 1: Not empty, fifo has data.
[7:5] RO		reserved	reserve.
[4:0] RO		single_rx_cmd_fifo When _cnt 0), this register is cleared to 0.	The number of valid data in SINGLE_RX_FIFO. the I2C master single operation function is disabled (I2C_MST_SINGLE_CTRL[31] is

I2C_MST_SINGLE_CMD

I2C_MST_SINGLE_CMD is the I2C_MST_SINGLE_CMD register.

Offset Address	Register Name	Total Reset Value
0x00B4	I2C_MST_SINGLE_CMD	0x0000_0000

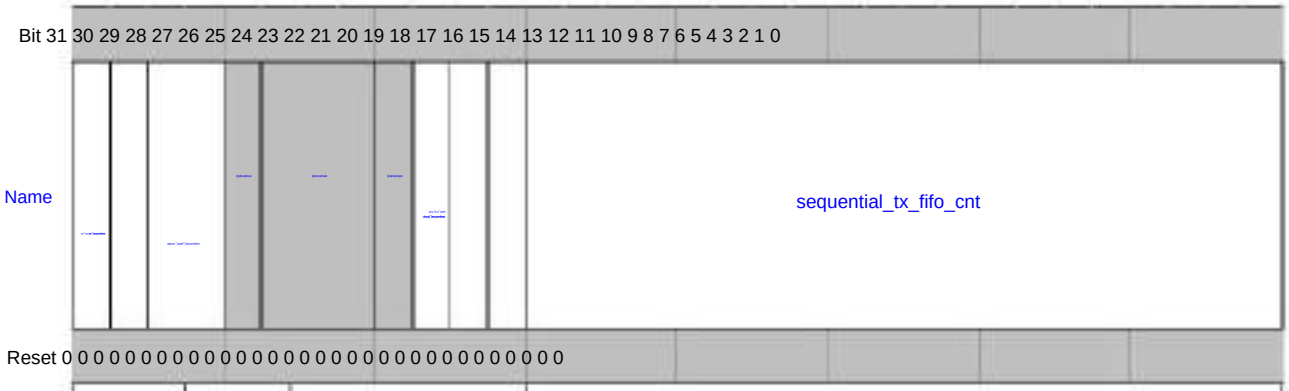
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	single_addr	single_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	WO	single_addr	The i2c master single operation function accesses the register address of the slave. Note: The low 8 bits are sent first, and the high 8 bits are sent last.
[15:0]	RW	single_data	The i2c master single operation function accesses the register data of the slave Notice: The low 8 bits are sent first, and the high 8 bits are sent last.

I2C_SEQUENCE_CMD0

I2C_SEQUENCE_CMD0 is the I2C_SEQUENCE_CMD0 register.

Offset Address	Register Name	Total Reset Value
0x00B8	I2C_SEQUENCE_CMD0	0x0000_0000



Bits	Access	Name	Description
[31]	RW	sequential_mode_en	Continuous mode is enabled (this function needs to be completed in cooperation with DMA). 0: off; 1: enable.
[30]	RW	sequential_rw	Continuous mode operation type. 0: read; 1: Write.
[29:28]	RW	sequential_addr_mo de	Continuous mode first address type. 00ÿ8 bitsÿ 01ÿ16 bitsÿ 10ÿ24 bitsÿ 11ÿ32 bitsÿ
[27]	RO	reserved	reserve.
[26:24]	RO	reserved	reserve.
[23]	RO	reserved	reserve.
[22]	RO	add_cnt_full	First address sending completion flag, indicating that the dma operation can be started.
[21]	RO	sequential_busy	Continuous mode operation busy flag.
[20]	RO	sequential_finish	Sequential mode operation complete flag.
[19:0]	RO	sequential_tx_fifo_c nt	The number of operations that have been completed in sequential mode.

I2C_SEQUENCE_CMD1

I2C_SEQUENCE_CMD1 is the I2C_SEQUENCE_CMD1 register.

Offset Address	Register Name	Total Reset Value
0x00BC	I2C_SEQUENCE_CMD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_addr	Note for the first address in continuous mode: The low 8 bits are sent first, and the high 8 bits are sent last.

I2C_SEQUENCE_CMD2

I2C_SEQUENCE_CMD2 is the I2C_SEQUENCE_CMD2 register.

Offset Address	Register Name	Total Reset Value
0x00C0	I2C_SEQUENCE_CMD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_length																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_length	The length of the continuous mode (minus one configuration, that is, the configuration value is the actual value RO1).

12.2 UART

12.2.1 Overview

Universal Asynchronous Receiver Transmitter UART (Universal Asynchronous Receiver Transmitter) is an asynchronous serial communication interface. Its main function is to transfer data from peripheral devices to the internal bus after serial-to-parallel conversion, and output the data to the outside after parallel-to-serial conversion. equipment. The main function of UART is to connect with the UART of the external chip, so as to realize the communication between the two chips.

Hi3519V100 provides 5 UART units:

UART0: 2-wire UART, mainly used for debugging.

UART1/2: 4-wire UART.

UART3/4: 2-wire UART.

12.2.2 Features

The UART module has the following features:

Support 64 x 8bit transmit FIFO and 64 x 12bit receive FIFO. Support data bit and stop bit width programmable. Data bits can be programmed as 5/6/7/8 bits; stop bits can be programmed as 1bit or 2bit.

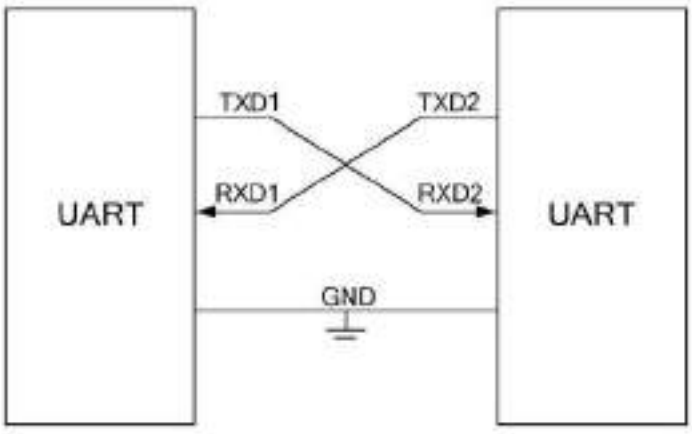
Support odd, even parity or no parity. Support transfer rate programmable. Support receive FIFO interrupt, send FIFO interrupt, receive timeout interrupt, error interrupt. Supports initial interrupt status query and masked interrupt status query. Support programming to disable UART module or UART transmit/receive function to reduce power consumption. Supports shutting down the UART clock to save power. DMA operation is supported.

12.2.3 Functional description

Application Block Diagram

A typical application block diagram of UART is shown in Figure 12-3 .

Figure 12-3 Typical application block diagram of UART



UART is an asynchronous bidirectional serial bus that provides a simple and efficient way of data transmission, requiring only two data lines to be connected to each other.

Functional principle

A frame transmission of UART mainly includes start signal, data, parity bit and end signal, as shown in Figure 12-4 . The data frame is output from the TXD end of one UART and input from the RXD end of another UART.

Figure 12-4 UART frame format

The meanings of start signal, data, parity bit and end signal are as follows:

Start signal (start bit) A sign of the

beginning of a data frame. The UART protocol stipulates that a low level of the TXD signal indicates the beginning of a data frame. When the UART is not transmitting data, it should be kept high. Data signal (data bit)

The data bit width can be adjusted according to different application requirements, and can be configured as 5bit/6bit/7bit/8bit data bit width. Parity bit

(parity bit) The parity bit is a 1-bit

error correction signal. The parity bit of UART includes odd parity, even parity and fixed parity. It also supports the enable and disable of the parity bit. Please refer to See UART_LCR_H register. End signal (stop bit) The end signal is the stop bit of the data frame,

which supports two configurations

of 1-bit stop bit and 2-bit stop bit. The end signal of the data frame is to pull TXD into high level.

12.2.4 Working method

12.2.4.1 Baud Rate Configuration

The baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD . The formula for calculating the baud rate is:

Current baud rate = UART reference clock frequency (24MHz by default) / (16 x frequency division factor)

The frequency division coefficient consists of two parts, integer and decimal, which correspond to registers UART_IBRD and UART_FBRD respectively.

For example: UART reference clock frequency is 24MHz, if UART_IBRD is set to 0x1E, UART_FBRD is set to 0x00, according to the baud rate calculation formula, the current baud rate is 24/(16 x 30)=0.005Mbit/s.

Typical values of UART baud rate configuration are: 9,600bit/s, 14,400bit/s, 19,200bit/s, 38,400bit/s, 57,600bit/s, 76,800bit/s, 115,200bit/s, 230,400bit/s, 460,800bit/s.

The calculation of the frequency division coefficient value and the configuration of the frequency division coefficient register are as follows:

If the required baud rate is 230,400bit/s, and the UART reference clock frequency is 24MHz, then the frequency division factor is (24 x 106)/(16 x 230400) = 6.5104, so IBRD (integer part) is 6, FBRD (decimal part) is 0.5104.

Calculate the value in the 6bit UART_FBRD register: According to m=integer (FBRDx2n +0.5) (n= the width of the UART_FBRD register), calculate m=integer (0.5104x26 +0.5)=33, configure 0x0006 in the UART_IBRD register, and in the UART_FBRD register Configure 0x21.

When the fractional part of the frequency division factor is configured as 33, the actual value of the baud rate divisor is 6+33/64=6.5156, the resulting baud rate is (24 x 106) /(16 x 6.5156)=230216.7107, and the error rate is (230216.7107–230400)/ 230400x100=-0.07956%.

Using the 6bit UART_FBRD register, the maximum error rate is 1/64 x 100=1.56%, which occurs when m=1, and the error rate accumulates over 64 clock cycles.

12.2.4.2 Soft Reset

A separate soft reset for the UART controller can be achieved by configuring the CRG register.

By configuring the CRG register PERI_CRG57[8] as 1, a separate soft reset for the UART0 controller can be realized.

By configuring the CRG register PERI_CRG57[9] to be 1, the individual soft reset of the UART1 controller can be realized. By

configuring the CRG register PERI_CRG57[10] to be 1, the individual soft reset of the UART2 controller can be realized. By

configuring the CRG register PERI_CRG57[11] to be 1, the individual soft reset of the UART3 controller can be realized.

By configuring the CRG register PERI_CRG57[12] to be 1, the individual soft reset of the UART4 controller can be realized.

说明

For the reset register, please refer to 3.2.7 CRG register description.

The value of each configuration register is the default value after reset, so these registers need to be initialized and configured again after reset.

12.2.4.3 Data Transfer in Interrupt or Query Mode

initialization

The initialization steps are as follows:

Step 1. Write 0 to UART_CR bit[0] to disable UART.

Step 2. Write corresponding configuration values to the UART_IBRD and UART_FBRD registers to configure the transmission rate.

Step 3. Configure UART_CR, UART_LCR_H, and set the corresponding UART working mode.

Step 4. Configure UART_IFLS to set corresponding transmit and receive FIFO thresholds.

Step 5. If the driver program uses the interrupt method , it is necessary to set UART_IMSC to enable the corresponding interrupt signal; when the query method is used, the generation of the corresponding interrupt signal should be prohibited.

Step 6. Write 1 to UART_CR bit[0] to enable UART and complete the initial configuration.

----Finish

data transmission

The data sending steps are as follows:

Step 1. Write the sending data into UART_DR to start data sending.

Step 2. In the query mode, read the UART_FR bit[5] to detect the TX_FIFO status when sending continuous data , according to
The state of TX_FIFO determines whether to send data to TX_FIFO; in interrupt mode, it detects according to the corresponding interrupt status bit;
decides whether to send data to TX_FIFO.

Step 3. By checking whether the UART_FR bit[7] is 1, judge whether the UART has finished sending all the data.

----Finish

data reception

Data reception is handled as follows:

In the query mode, when receiving data, check the RX_FIFO status by reading UART_FR[rxfe], according to
The state of RX_FIFO determines whether to read the data in RX_FIFO. In the interrupt
mode, it is determined whether to read the data in RX_FIFO according to the detection of the corresponding interrupt status bit.

12.2.4.4 Data transfer in DMA mode

initialization

The initialization steps are as follows:

Step 1. Write 0 to UART_CR[uarten] to disable UART.

Step 2. Write corresponding configuration values to the UART_IBRD and UART_FBRD registers to configure the transmission rate.

Step 3. Configure UART_CR, UART_LCR_H, and set the corresponding UART working mode.

Step 4. Configure UART_IFLS to set corresponding transmit and receive FIFO thresholds.

Step 5. If the driver program uses the interrupt method , it is necessary to set UART_IMSC to enable the corresponding interrupt signal; when the query method is used, the generation
of the corresponding interrupt signal should be prohibited.

Step 6. Write 1 to UART_CR[uarten] to enable UART and complete the initial configuration.

----Finish

data transmission

The steps of data transmission (taking DMA mode as an example) are as follows:

Step 1. Configure the DMA data channel, including parameters such as data transfer source and destination address, number of data transfers, transfer type, etc.
number. For specific configuration, please refer to the related description of "Direct Memory Access Controller".

Step 2. Configure UART_DMACR as 0x2 to enable the DMA transmission function of UART.

Step 3. Report through the DMA interrupt to judge whether the data transmission is completed, and if it is completed, turn off the DMA transmission of the UART
Function.

----Finish

data reception

Data receiving (taking DMA mode as an example) steps are as follows:

Step 1. Configure the DMA data channel, including data transfer source and destination address, data receiving area address, data transfer Number, transmission type and other parameters.

Step 2. Configure UART_DMACR as 0x1 to enable the DMA receiving function of UART.

Step 3. Through the DMA status query, judge whether the data reception is completed, and if it is completed, close the DMA reception of UART Function.

----Finish

12.2.5 UART register overview

Hi3519V100 provides 5 UART units, the base addresses are as follows:

The UART0 register base address is 0x1210_0000.

The UART1 register base address is 0x1210_1000.

The UART2 register base address is 0x1210_2000.

The UART3 register base address is 0x1210_3000.

The UART4 register base address is 0x1210_4000.

An overview of the UART registers is shown in Table 12-2 .

Table 12-2 UART Register Overview

offset address name		describe	page number
0x000	UART_DR data register		12-32
0x004	UART_RSR Receive Status Register/Error Clear Register 12-33		
0x018	UART_FR Flag Register		12-34
0x024	UART_IBRD Integer Baud Rate Register		12-35
0x028	UART_FBRD Fractional Baud Rate Register		12-35
0x02C	UART_LCR_H line control register		12-36
0x030	UART_CR Control Register		12-37
0x034	UART_IFLS Interrupt FIFO Threshold Select Register		12-39
0x038	UART_IMSC Interrupt Mask Register		12-40
0x03C	UART_RIS Raw Interrupt Status Register		12-41
0x040	UART_MIS Masked Interrupt Status Register		12-42

offset address name		describe	page number
0x044	UART_ICR Interrupt Clear Register		12-43
0x048	UART_DMACR DMA Control Register		12-44

12.2.6 UART register description

UART_DR

UART_DR is a UART data register, which stores received data and sent data, and can read the receiving status from this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			you are		fe	data							
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	RO	reserved	reserve.
[11]	RO	are you	Overflow error. 0: no overflow error; 1: There is an overflow error, and data is received after the receive FIFO is full.
[10]	RO	be	Break Error. 0: no break error; 1: There is a break error, that is, the input of the received data remains low for longer than a full-word transfer (including start, data, parity, and stop bit).
[9]	RO	on	Validation error. 0: No parity error; 1: There is a verification error.
[8]	RO	fe	Framing error. 0: no frame error; 1: Framing error (wrong stop bit).
[7:0]	RW	data	Receive data and send data.

UART_RSR

UART_RSR is the receive status register/error clear register.

The register reads as a receive status register. When

the register is written, it acts as an error clear register.

Receive status can also be read from UART_DR . The status information of break, frame, and parity read from UART_DR has higher priority than the information read from UART_RSR (that is, the state changes in UART_DR are faster than UART_RSR).

Any write operation to the UART_RSR register will reset the UART_RSR register.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				are you	be	on	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[7:4] RO	reserved	reserve.
[3] RW you		Overflow error. 0: no overflow error; 1: Overflow error. When the FIFO is full, the content in the FIFO remains valid, because there will be no next data written to the FIFO, but the shift register will overflow. The CPU must immediately read the data to empty the FIFO.
[2] RW be		Break Error. 0: no break error; 1: break error. Condition of Break: The input to receive data remains low for longer than a full word transfer (start, data, parity, stop bit are defined).
[1] RW or		Validation error. 0: No parity error; 1: The checksum of received data is wrong. In FIFO mode, this error is associated with the data at the top of the FIFO.

[0] RW fe			Framing error. 0: no frame error; 1: Received data has wrong stop bit (valid stop bit is 1).

UART_FR

UART_FR is the UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12 11	10 9	8	7	6	5	4	3	2	1	0
Name	reserved						txfe	rxff	txff	rxfe	busy			reserved
Reset 0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved.
[7]	RO	txfe	The meaning of this bit is determined by the state of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is 1 when the sending holding register is empty; if UART_LCR_H[fen] is 1, this bit is 1 when the sending FIFO is empty.
[6]	RO	rxff	The meaning of this bit is determined by the state of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is 1 when the receiving holding register is full; if UART_LCR_H[fen] is 1, this bit is 1 when the receiving FIFO is full.
[5]	RO	txff	The meaning of this bit is determined by the state of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is 1 when the sending holding register is full; if UART_LCR_H[fen] is 1, this bit is 1 when the sending FIFO is full.
[4]	RO	rxfe	The meaning of this bit is determined by the state of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the receiving holding register is empty; if UART_LCR_H[fen] is 1, this bit is set to 1 when the receiving FIFO is empty.

[3] RO busy			UART busy status bit. 0: UART is idle or finished sending data; 1: UART is busy sending data. Once this bit is set, it remains in this state until the entire byte (including all stop bits) has been completely sent out of the shift register. This bit is set whenever the transmit FIFO is not empty, regardless of whether the UART is enabled or not.
[2:0] RO reserved Reserved.			

UART_IBRD

UART_IBRD is an integer baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	baud became													
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[15:0] RW baud divint	Integer baud rate divider value. All cleared to 0 at reset.	

UART_FBRD

UART_FBRD is the fractional baud rate register.

注意

The value of the integer baud rate register and the fractional baud rate register must wait until the current data is sent and received. renew.

The minimum division value is 1, and the maximum division value is 65535 (216–1). That is, UART_IBRD=0 is invalid, and UART_FBRD will be ignored at this time. Similarly, if UART_IBRD=65535 (0xFFFF), UART_FBRD can only be 0, if it is greater than 0, it will cause the failure of sending and receiving.

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							baud divfrac
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	reserve.
[5:0]	RW	baud divfrac	Fractional baud rate divider value. All cleared to 0 at reset.

UART_LCR_H

UART_LCR_H is the line control register, and UART_LCR_H, UART_IBRD, and UART_FBRD form a 30bit wide register. If updating the contents of UART_IBRD and UART_FBRD , UART_LCR_H must be updated at the same time .

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12 11 10 9	8	7	6	5	4	3	2	1	0
Name	reserved					sps	wlen		fen	stp2	eps	pen	brk
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	reserve.
[7]	RW	sps	Check selection. When bit[1], bit[2], bit[7] of this register are set, the parity bit will be sent and detected as 0; when bit[1], bit[7] of this register are set , when bit[2] is 0, the parity bit will be sent and detected as 1. When bit[1], bit[2] and bit[7] are all cleared to 0, stick parity is disabled.
[6:5]	RW	wlen	Indicates the number of data bits sent and received in a frame. 00ÿ5bitÿ 01ÿ6bitÿ 10ÿ7bitÿ 11ÿ8bitÿ
[4]	RW	fen	Transmit and receive FIFO enable control. 0: Transmit and receive FIFO disabled; 1: Transmit and Receive FIFOs enabled.

[3] RW stp2			2-bit stop bit judgment at the end of the sent frame. 0: There is no 2-bit stop bit at the end of the sent frame; 1: There is a 2-bit stop bit at the end of the transmitted frame. The receive logic does not check the 2-bit stop bit when receiving.
[2] RW eps			Parity selection during transmit and receive. 0: Generate odd parity or check odd parity during sending and receiving; 1: Generate even parity or check even parity during sending and receiving. When UART_LCR_H[fen] is 0, this bit has no effect.
[1] RW pen			Check select bit. 0: no verification; 1: The sending direction generates verification, and the receiving direction performs verification check.
[0] RW brk			Send a break. 0: invalid; 1: After sending the current data, UTXD outputs low level continuously. Note: To execute the break command correctly, software must set this bit to 1 for more than 2 complete frames; in normal use, this bit must be cleared to 0.

UART_CR

UART_CR is the UART control register.

To configure UART_CR follow these steps:

Step 1. Write 0 to UART_CR[uarten] to disable UART.

Step 2. Wait for the current data sending or receiving to end.

Step 3. Clear UART_LCR_H[fen] to 0.

Step 4. Configure UART_CR.

Step 5. Write 1 to UART_CR[uarten] to enable UART.

----Finish

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts			dtr	rxe	txe	lbe		reserved			types
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable. 0: Disable CTS hardware flow control; 1: Enable CTS hardware flow control, only send data when nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable. 0: Disable RTS hardware flow control; 1: Enable RTS hardware flow control, request to receive data only when there is space in the receive FIFO.
[13:12]	RO	reserved	reserve.
[11]	RW	rts	request to send. This bit is the inversion of UART modem status output signal nUARTRTS. 0: The output signal remains unchanged; 1: That is, if the bit is configured as 1, the output signal is 0.
[10]	RW	dtr	Data sending preparation. This bit is the inversion of the UART modem status output signal nUARTDTR. 0: The output signal remains unchanged; 1: That is, if the bit is configured as 1, the output signal is 0.
[9]	RW	rxe	UART receive enable. 0: forbidden; 1: enable. If the UART is disabled during reception, the reception of the current data will end before normal stop.

[8] RW house			UART transmit enable. 0: forbidden; 1: enable. If the UART is disabled during transmission, the current data transmission will end before normal stop.
[7] RW lbe			Loopback enabled. 0: forbidden; 1: UARTTXD output loops back to UARTRXD.
[6:1] RO reserved			reserve.
[0] RW uarten			UARTs are enabled. 0: forbidden; 1: enable. If the UART is disabled during transmission and reception, the current data transmission ends before a normal stop.

UART_IFLS

UART_IFLS is the interrupt FIFO threshold selection register, which is used to set the FIFO interrupt (UART_TXINTR or UART_RXINTR) trigger line.

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rxiflsel			txiflsel		
Reset 0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	RO	reserved	reserve.
[5:3]	RW	rxiflsel	Threshold selection of receive interrupt FIFO, the trigger point of receive interrupt is as follows. 000: Receive FIFOÿ1/8full; 001: Receive FIFOÿ1/4full; 010: Receive FIFOÿ1/2full; 011: Receive FIFOÿ3/4full; 100: Receive FIFOÿ7/8full; 101~111: Reserved.

[2:0] RW txiflsel			Threshold selection of transmit interrupt FIFO, the trigger point of transmit interrupt is as follows. 000: send FIFOÿ1/8full; 001: Send FIFOÿ1/4full; 011: Transmit FIFOÿ3/4full; 010: Transmit FIFOÿ1/2full; 100: send FIFOÿ7/8full; 101~111: Reserved.

UART_IMSC

UART_IMSC is an interrupt mask register, which is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13 12 11 10	9	8	7	6	5	4	3	2	1	0
Name	reserved			oeim	beim	peim	feim	rtim	txim	rxim	reserved		
Reset 0	0	0	0 0 0 0	0	0	0	0	0	0	0	0 0	0	0

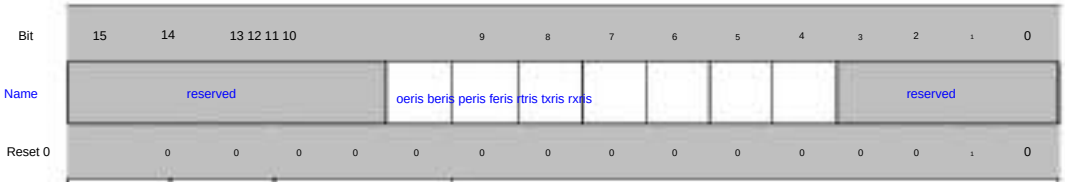
Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved.
[10]	RW	oeim	Mask status of the overflow error interrupt. 0: mask the interrupt; 1: do not mask the interrupt.
[9]	RW	at	break Mask state of error interrupt. 0: Mask the interrupt; 1: Do not mask the interrupt.
[8]	RW	peim	Verify the masking status of interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[7]	RW	feim	Mask status of the framing error interrupt. 0: mask the interrupt; 1: do not mask the interrupt.
[6]	RW	rtim	Mask status of receive timeout interrupt. 0: Mask the interrupt; 1: Do not mask the interrupt.

[5] RW guilty			Mask status for transmit interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[4] RW rxim			Mask status of receive interrupts. 0: Mask the interrupt; 1: Do not mask the interrupt.
[3:0] RO reserved	Reserved.		

UART_RIS

UART_RIS is the raw interrupt status register and its content is not affected by the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0002



Bits	Access Name	Description
[15:11]	RO reserved	reserve.
[10]	RO oeris	Raw overflow error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[9]	RO beris	Raw break Error break state. 0: no interrupt is generated; 1: An interrupt has been generated.
[8]	RO peris	Raw parity interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[7]	RO	Raw error interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[6]	RO rtris	Raw receive timeout interrupt status. 0: Interrupt not generated; 1: Interrupt generated.

[5] RO txris			Raw send interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[4] RO rxris			Raw receive interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[3:0] RO reserved			reserve.

UART_MIS

UART_MIS is the masked interrupt status register, and its content is the result of the "AND" operation between the original interrupt status and the interrupt mask.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13 12 11 10	9	8	7	6	5	4	3 2 1	0
Name	reserved			oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved
Reset 0	0	0	0 0	0	0	0	0	0	0	0 0 0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved.
[10]	RO	oemis	Masked overflow error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[9]	RO	bemis	Masked break Error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[8]	RO	pemis	Masked verification interrupt status. 0: Interrupt not generated; 1: Interrupt generated.
[7]	RO	femis	Masked error interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[6]	RO	rtmis	Masked receive timeout interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.

[5] RO txmis			Masked transmit interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[4] RO rxmis			Masked receive interrupt status. 0: no interrupt is generated; 1: An interrupt has been generated.
[3:0] RO reserved	Reserved.		

UART_ICR

UART_ICR is an interrupt clear register, when writing 1, the corresponding interrupt is cleared, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						oeic	beic	peic	see	rtic	txic	rxic	reserved		
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved.
[10]	WO	oec	Clear overflow error interrupt. 0: invalid; 1: Clear interrupt.
[9]	WO	bicycle	Clear break Error interrupt. 0: invalid; 1: Clear interrupt.
[8]	WO	pic	Clear verify interrupt. 0: invalid; 1: Clear interrupt.
[7]	WO	feic	Clear the error interrupt. 0: invalid; 1: Clear interrupt.
[6]	WO	rtic	Clear receive timeout interrupt. 0: invalid; 1: Clear interrupt.

[5] WO txic			Clear transmit interrupt. 0: invalid; 1: Clear interrupt.
[4] WO rxic			Clear receive interrupt. 0: invalid; 1: Clear interrupt.
[3:0] RO reserved Reserved.			

UART_DMACR

UART_DMACR is the DMA control register, which is used to configure the DMA enable of transmit FIFO and receive FIFO.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	RO	reserved	Reserved.
[2]	RW	dmaonerr	Receive channel DMA enable control when UART error interrupt (UARTEINTR) occurs. 0: When the UART error interrupt (UARTEINTR) is valid, the request output of the receiving channel DMA (UARTRXDMASREQ or UARRTXDMABREQ) is valid; 1: When the UART error interrupt (UARTEINTR) is valid, the request output of the receiving channel DMA (UARTRXDMASREQ or UARRTXDMABREQ) is invalid.
[1]	RW	txdmae	DMA enable control for transmit FIFO. 0: forbidden; 1: enable.
[0]	RW	rxdmae	DMA enable control for receive FIFO. 0: forbidden; 1: enable.

12.3 SPI

12.3.1 Overview

The SPI controller realizes serial-to-parallel and parallel-serial conversion of data, and can be used as a Master to perform synchronous serial communication with external devices.

Support MOTOROLA's SPI, TI serial synchronization, and MicroWire three peripheral interface protocols.

12.3.2 Features

注意

Hi3519V100 has 3 groups of SPI interfaces, among which SPI0/2 supports single chip selection, and SPI1 supports 2 chip selections.

The SPI of the Hi3519V100 chip only supports the Master interface, the working reference clock is the APB bus clock, and the SPI_CLK output by the SPI supports a maximum of 24.75MHz.

The functional characteristics of SPI are:

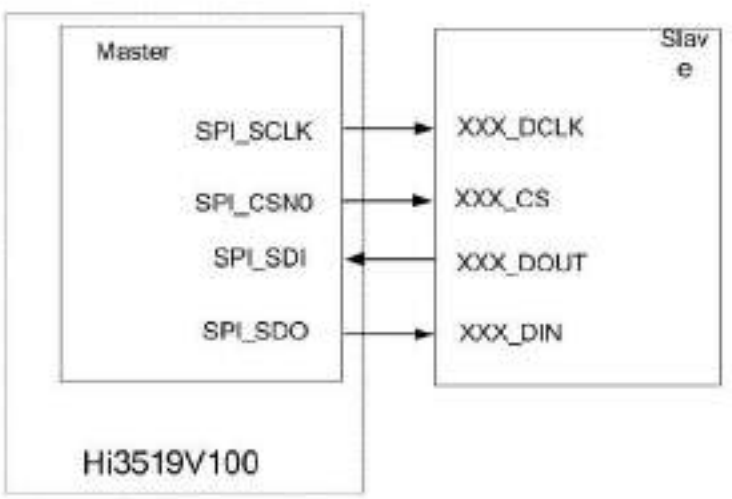
- The interface clock frequency is programmable.
- FIFO with a width of 16bit and a depth of 256 for receiving/transmitting.
- The serial data frame length is programmable: 4bit ~ 16bit. A loopback test mode is provided internally.
- DMA operation is supported.
- Support SPI, MicroWire, TI synchronous serial interface, support single frame and continuous frame format.
- Support SPI full-duplex working mode, clock polarity and phase can be configured. Supports MicroWire half-duplex mode of operation.
- Support TI synchronous serial interface full-duplex working mode.

12.3.3 Functional description

typical application

The application block diagram when SPI is connected to Slave is shown in Figure 12-5 .

Figure 12-5 Application when SPI is connected to Slave



12.3.4 Three peripheral bus timings

The meanings of the abbreviations in Figure 12-6 to Figure 12-13 are:

MSBÿMost Significant Bit

LSBÿLeast Significant Bit

QÿQ is an undefined signal

SPI interface

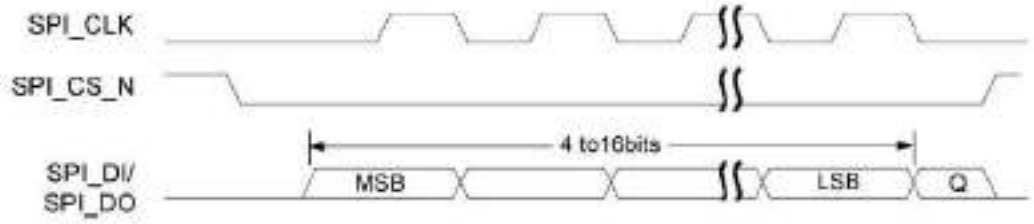
说明

SPO indicates SPICLKOUT polarity and SPH indicates SPICLKOUT phase. They are register SPICR0 bits[7:6].

ÿ1ÿSPO=0ÿSPH=0

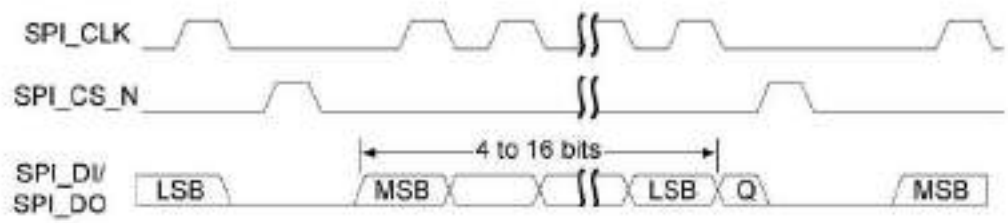
The SPI single frame frame format is shown in Figure 12-6 .

Figure 12-6 SPI single frame frame format (SPO=0, SPH=0)



The frame format of SPI continuous frame is shown in Figure 12-7 .

Figure 12-7 SPI continuous frame frame format (SPO=0, SPH=0)



In this mode, when the SPI is idle:

SPI_CLK signal is set low

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When the SPI is enabled and there is valid data in the send FIFO, set the SPI_CS_N signal to be low, which means start to transmit data. The data from Slave is immediately sent to Master's receiving data line SPI_DI. Valid Master data is transferred to SPI_DO after half a SPI_CLK clock cycle. At this time, both Master and Slave data are valid, and the SPI_CLK pin becomes high level after the next half SPI_CLK clock cycle. Data is captured on the rising edge of the SPI_CLK clock and transferred on the falling edge of the clock.

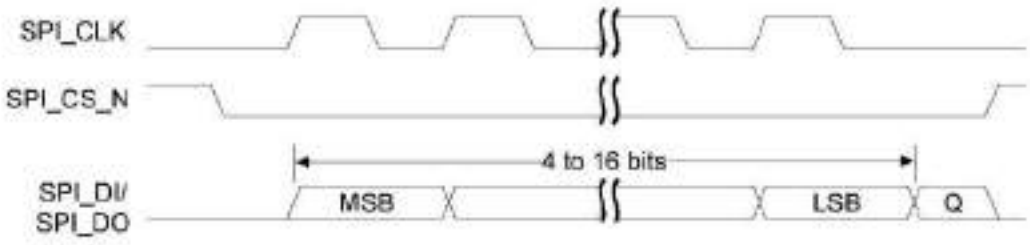
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock cycle.

If it is a continuous transmission, the SPI_CS_N signal must pull the SPI_CLK clock high for one clock cycle between each word transmission. This is because when SPH is 0, the Salve selection pin will fix the data of its internal serial device register so that it will not change. Therefore, during continuous transmission, the master device must pull the SPI_CS_N signal high between each word transmission. At the end of the continuous transmission, SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after the last 1 bit is captured.

ÿ2ÿSPO=0ÿSPH=1

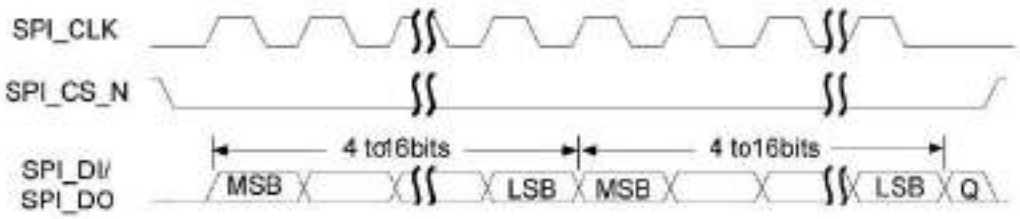
The SPI single frame frame format is shown in Figure 12-8 .

Figure 12-8 SPI single frame frame format (SPO=0, SPH=1)



The frame format of SPI continuous frame is shown in Figure 12-9 .

Figure 12-9 SPI continuous frame frame format (SPO=0, SPH=1)



In this mode, when the SPI is idle:

SPI_CLK signal is set low

SPI_CS_N set high transmit

data line SPI_DO forced low

When the SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N signal to low to start transmitting data. After half a SPI_CLK clock cycle, the valid data of Master and Slave are valid on their respective transmission lines. At the same time, SPI_CLK is valid from the first rising edge. Data is captured on the falling edge of the SPI_CLK clock and transferred on the rising edge of the clock.

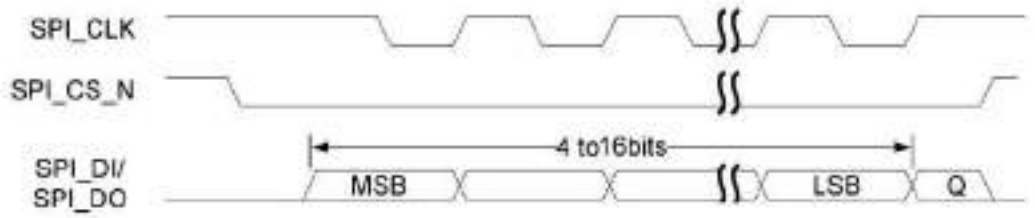
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock.

When transmitting continuously, SPI_CS_N is kept low between transmitted data words. At the end of the continuous transfer, SP_CS_N returns to high level after 1 SPI_CLK clock after the last 1 bit capture.

ÿ3ýSPO=1ÿSPH=0

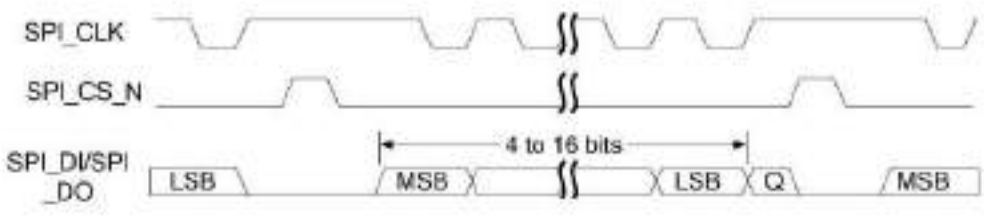
The SPI single frame frame format is shown in Figure 12-10 .

Figure 12-10 SPI single frame frame format (SPO=1, SPH=0)



The frame format of SPI continuous frame is shown in Figure 12-11 .

Figure 12-11 SPI continuous frame frame format (SPO=1, SPH=0)



In this configuration, when the SPI is idle:

SPI_CLK signal is set high

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When the SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N signal to low to start transmitting data. At this time, the data of Slave is sent to the receiving data line SPI_DI of Master immediately. After half a SPI_CLK cycle, the valid data of Master is transferred to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK Master pin is set low. This means that data is captured on the falling edge of the SPI_CLK clock and transferred on the rising edge of the SPI_CLK clock.

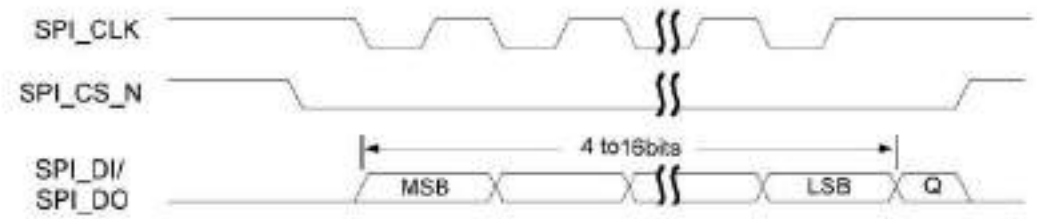
If a single word is transmitted, when the last 1-bit data is captured, SPI_CS_N returns to high level after the next SPI_CLK clock.

If it is a continuous transfer, the SPI_CS_N signal must be pulled high between each word transfer. This is because when SPH is 0, the Salve select pin fixes the data of its internal serial device register so that it will not change.
SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after capturing the last 1-bit data.

ÿ4ÿSPO=1ÿSPH=1

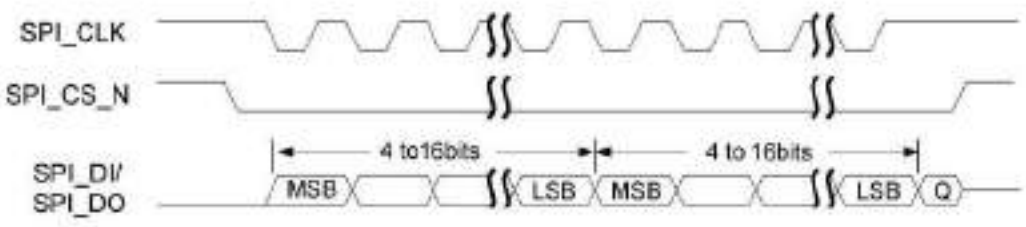
The SPI single frame frame format is shown in Figure 12-12 .

Figure 12-12 SPI single frame frame format (SPO=1, SPH=1)



The frame format of SPI continuous frame is shown in Figure 12-13 .

Figure 12-13 SPI continuous frame frame format (SPO=1, SPH=1)



In this mode, when the SPI is idle:

SPI_CLK signal is set high

SPI_CS_N signal is set high to

transmit data line SPI_DO is forced low

When SPI is enabled and there is valid data in the transmit FIFO, set the SPI_CS_N Master signal to low to start transmitting data. After half a SPI_CLK clock cycle, the Master and Slave data are valid on their respective transmission lines. At the same time, the clock SPI_CLK is valid from 1 falling edge. Data is captured on the rising edge of the SPI_CLK clock and transferred on the falling edge of the clock. When transmitting a single word, SPI_CS_N returns to high level after 1 SPI_CLK clock cycle after the last 1 bit capture of the transmission.

For continuous transfers, the SPI_CS_N signal is always kept low. SPI_CS_N returns to high state 1 SPI_CLK clock cycle after the last 1 bit is captured. For continuous transfers, SPI_CS_N remains low during the transfer and ends in the same way as a single transfer.

(5) Interface timing

Figure 12-14 SPI interface timing diagram

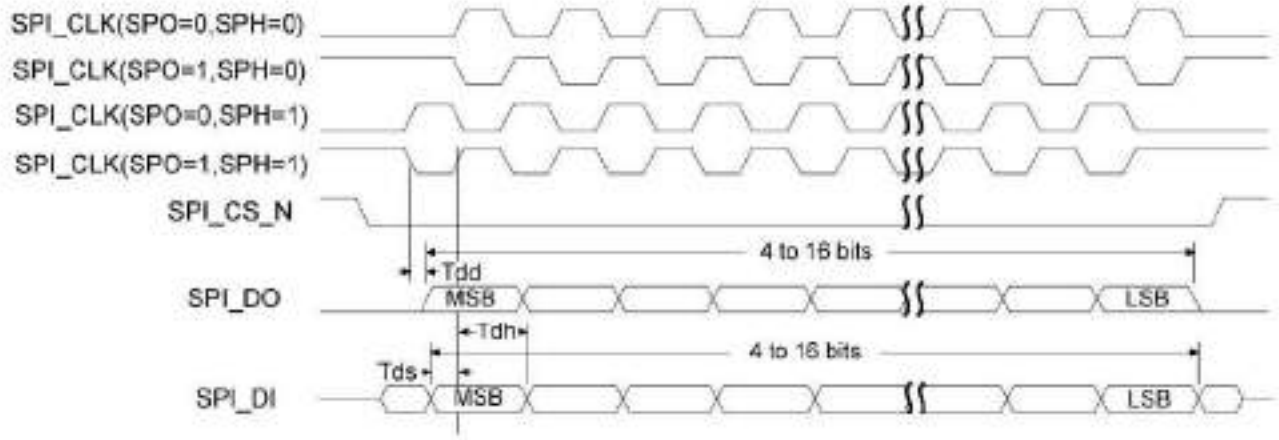


Table 12-3 SPI interface timing parameters

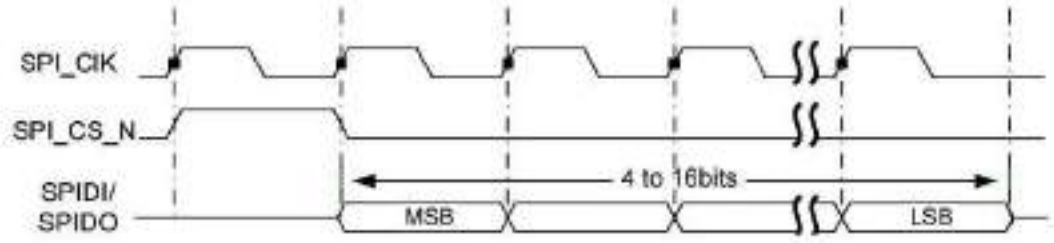
Parameter Description		min max unit		
Tdd output data delay		-3.5	5	ns

Tds	Input control signal setup time	23		ns
Tdh input control signal hold time		0	-	ns

TI synchronous serial interface

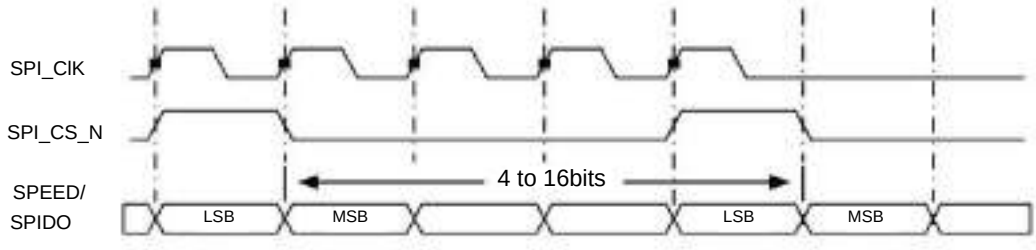
The frame format of TI synchronous serial single frame is shown in Figure 12-15 .

Figure 12-15 TI synchronous serial single frame frame format



The frame format of TI synchronous serial continuous frame is shown in Figure 12-16 .

Figure 12-16 TI synchronous serial continuous frame frame format



In this mode, when the SPI is idle:

SPI_CK is low.

SPI_CS_N is low. The transmit data

line SPIDO remains high impedance.

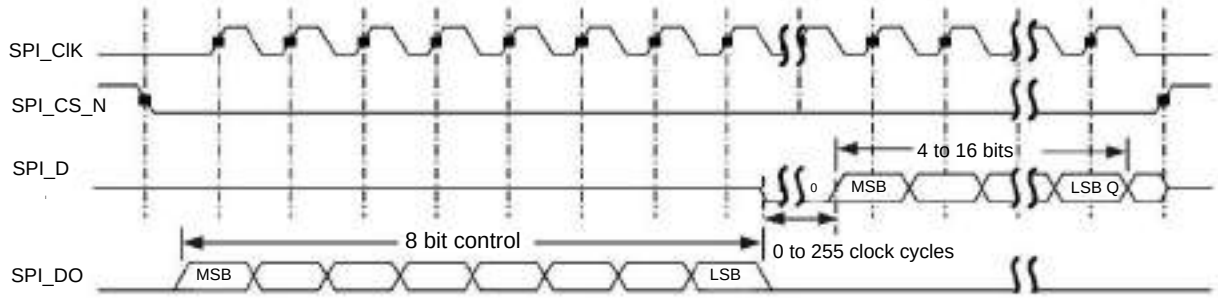
Once there is data in the transmit FIFO, SPICSN will generate a high-level pulse of a SPICK clock cycle, and the data to be transmitted will be transferred from the transmit FIFO to the transmit logic serial shift register. On the next rising edge of the SPICK clock, the MSB of the 4bit~16bit data frame will be shifted out from SPIDO. Likewise, the MSB of data received from an external serial slave device is shifted in from the SPIDI pin.

SPI and off-chip serial devices clock data into the serial shift register on the falling edge of the SPICK clock. The receive serial register sends data to the receive FIFO on the first rising edge of the SPICK clock after receiving the LSB.

National Semiconductor Microwire interface

The National Semiconductor Microwire single frame frame format is shown in Figure 12-17 .

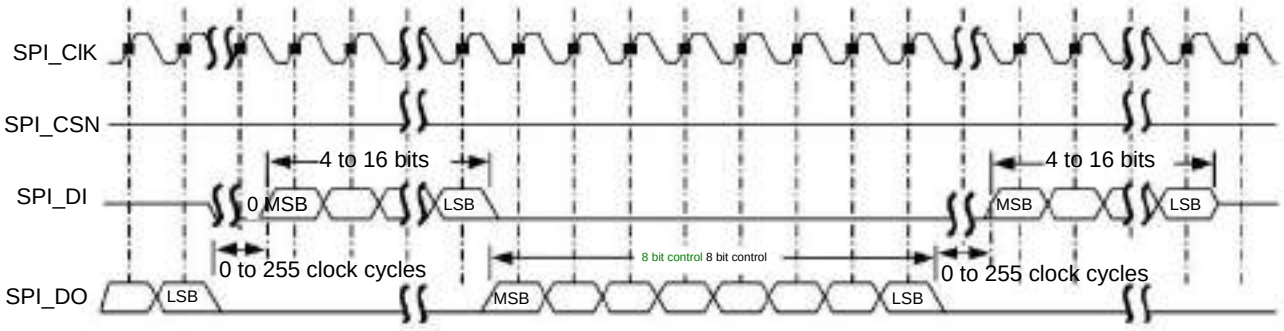
Figure 12-17 National Semiconductor Microwire single frame frame format



There can be a delay between 0 and 255 clock cycles between the end of the SPIDO LSB and the start of the SPIDI MSB.

The National Semiconductor Microwire continuous frame frame format is shown in Figure 12-18 .

Figure 12-18 National Semiconductor Microwire continuous frame frame format



There can be a delay of 0 to 255 clock cycles between the end of the SPI_DO LSB and the start of the SPI_DI MSB.

The format of Microwire is very similar to that of SPI, using master-slave information transmission technology, but SPI is full-duplex communication, while Microwire is half-duplex communication. When SPI sends serial data to external chips, 8-bit control word must be added first. During this process, the SPI does not receive any data. After the transmission is completed, the off-chip chip decodes the received data, and after a clock cycle interval from the 8bit control information, the slave starts to respond to the required data. The length of the returned data is 4bit~16bit, so that the length of the whole frame is 13bit~25bit.

In this mode, when the SPI is idle:

The SPI_CLK signal is set low.

SPI_CS_N is set high. The transmit

data line SPI_DO is forced low.

Writing a control byte internally to the transmit FIFO starts a transfer. The falling edge of SPI_CS_N triggers data transmission, the data in the transmit FIFO is sent to the serial shift register, and the MSB of the 8bit control frame is sent to the transmit pin SPIDO. During frame transmission, SPI_CS_N remains low. SPI_DI remains high impedance during this transfer.

The off-chip serial slave latches data into the serial shift register on every rising edge of the SPI_CLK clock. After the slave device has latched the last bit of data, it starts to decode the received data during the waiting time of the next clock cycle, and then feeds back the data required by the SPI from the device. Every 1 bit is in

The falling edge of the SPICK clock writes to SPI_DI. For a single data transfer, at the end of the frame, SPI_CS_N is pulled high 1 clock cycle after the last bit is written to the receive serial register, thus causing the received data to be transferred to the receive FIFO.

For continuous transfers, the data transfer starts and ends in the same way as a single data transfer. During this transmission process, the signal SPI_CS_N is always kept low, and the transmitted data is also continuous. The control word of the next frame is directly adjacent to the LSB of the previous frame. After the LSB of the frame is latched into the SPI, each received value is taken from the receive shift register on the falling edge of the SPI_CLK clock.

12.3.5 Working method

Operating mode

The working mode of SPI is divided into data transmission in interrupt or query mode and data transmission in DMA mode.

Clock and Reset

The output SPI clock frequency is calculated as follows:

Fsspclkout = Fsspclk/ÿCPSDVRxÿ1+SCRÿÿ

Fsspclk: SPI working reference clock, 1/4 bus clock (49.5MHz).

For CPSDVR and SCR, please check the corresponding registers.

The SPI in Hi3519V100 supports independent soft reset, which is controlled by register PERI_CRG57 bit[6:4]. Write "0" to the corresponding bit, SPI exits soft reset; write "1" to the corresponding bit, SPI enters soft reset. The default value is 0 after power-on.

interrupt handling

The SPI has 5 interrupts, the first 4 of which are independent interrupt sources, maskable, active high.

SPIRXINTR

Receive FIFO interrupt request. This interrupt is set when there are 4 or more valid data in the receive FIFO.

SPITCHINTR

Send FIFO interrupt request. This interrupt is set when there are 4 or fewer valid data in the transmit FIFO.

SPIRO INTR

Receive overrun interrupt request. When FIFO is full and new data needs to be written into FIFO, it will cause FIFO overrun and this interrupt will be set. At this point data is written to the receive shift register instead of the FIFO.

SPIRINTTR

Receive time out interrupt request. This interrupt is set when the receive FIFO is not empty and the SPI is in idle state for more than a fixed 32bit period. This

indicates that there is still data to be transmitted in the receive FIFO. This interrupt is deasserted if the receive FIFO is read empty or when new data is received into SPIRXD. The interrupt can also be cleared by writing register SPIICR[RTIC].

SPINTR

Combined interrupt is the result of the above 4 interrupts after "OR" operation. This interrupt is asserted if any of the above 4 individual interrupts is asserted and enabled.

SPI Interrupt SPIINTR Please refer to the Interrupt Handling chapter.

initialization

The initialization steps are as follows:

Step 1. Write "0" to register SPICR1[sse] to disable SPI.

Step 2. Write register SPICR0 to configure parameters such as frame format and transmission data bit width.

Step 3. Configure the register SPICPSR to set the clock frequency division factor.

Step 4. In the interrupt mode, set the register SPIIMSC to enable the corresponding interrupt signal; in the query and DMA mode, the generation of the corresponding interrupt signal should be prohibited.

Step 5. In interrupt or DMA mode, set SPITXFIFOCR and SPIRXFIFOCR.

Step 6. In DMA mode, configure the register SPIDMACR to enable the DMA function of SPI.

----Finish

Data transfer in query mode

Since the transmit/receive FIFO depth is 512, it is generally not necessary to consider FIFO fullness.

Specific steps are as follows:

Step 1. Write "1" to register SPICR1[sse] to enable SPI.

Step 2. Write the data to be sent to the register SPIDR continuously.

Step 3. Poll the register SPISR until [BSY]=0 (indicating that the bus is not busy), [TFE]=1 (indicating that the sending FIFO is empty), [RNE]=1 (indicating that the receiving FIFO is not empty), then go to step 5 .

Step 4. To read data, it is necessary to ensure that the receiving FIFO is empty (obtained by querying SPISR[RNE]).

The full-duplex feature of SPI/Microwire, every time a data is sent, a data is received, even if only data is sent,

The receive FIFO needs to be emptied.

Step 5. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

Data transfer in interrupt mode

Specific steps are as follows:

Step 1. Write "1" to register SPICR1[sse] to enable SPI.

Step 2. Write the data to be sent to the register SPIDR continuously.

Step 3. Wait for the interrupt SPIRXINTR to read the data. Loop until all data is read.

注意

The full-duplex feature of SPI/Microwire, every time a data is sent, a data is received, even if only data is sent, the receiving FIFO needs to be cleared.

Step 4. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

Data transfer in DMA mode

Specific steps are as follows:

Step 1. Acquire a DMAC channel.

Step 2. Write "1" to register SPICR1[sse] to enable SPI.

Step 3. Send data

a. Configure the relevant parameters in the configuration register and control register of the DMAC channel.

b. Start the DMAC to respond to the DMA request of the SPI transmit FIFO for data transmission.

c. Report through DMA interrupt to judge whether the data transmission is completed, and if it is completed, turn off the DMA function of SPI able.

Step 4. Receive data

a. Configure the relevant parameters in the configuration register and control register of the DMAC channel.

b. Start the DMAC to respond to the DMA request of the SPI receive FIFO for data transmission.

c. Report through the DMA interrupt to judge whether the data is received, and if it is completed, turn off the DMA function of the SPI able.

Step 5. Write "0" to register SPICR1[sse] to disable SPI.

----Finish

12.3.6 Register overview

An overview of the SPI registers is shown in Table 12-4 . The SPI base address is as follows:

SPI0 base address is 0x1212_0000

SPI1 base address is 0x1212_1000

SPI2 base address is 0x1212_2000

Table 12-4 SPI register overview

offset address	name	describe	page number
0x000	SPICR0	control register 0	12-56
0x004	SPICR1	control register 1	12-57
0x008	SPIDR	data register	12-58
0x00C	SPISR	status register	12-59
0x010	SPICPSR	Clock Divider Register	12-60
0x014	SPIIMSC	interrupt mask register	12-60
0x018	BREATHED	Raw Interrupt Status Register	12-61
0x01C	SPAM	Masked Interrupt Status Register	12-61
0x020	SPIICR	Interrupt Clear Register	12-62
0x024	SPIDMACR	DMA Control Register	12-62
0x028	SPITXFIFOCR	Transmit FIFO Control Register	12-63
0x02C	SPIRXFIFOCR	Receive FIFO Control Register	12-64

12.3.7 Register Description

SPICR0

SPICR0 is Control Register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit 15	14	13	12 11 10 9	8	7	6	5	4	3	2	1	0
Name	SCR				SPH	SPO		FRF		DSS		
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0

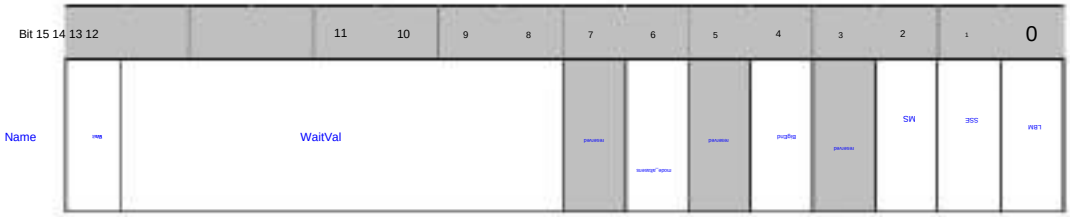
Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, the value ranges from 0 to 255. The SCR value is used to generate the SPI transmit and receive bit rate, the formula is FSSPCLK/(CPSDVSR (1+SCR)). CPSDVSR is an even number between 2 and 254, configured by register SPICPSR.
[7]	RW	SPH	SPICLKOUT phase, for specific meaning, please refer to the SPI frame format in "12.3.4 Three Peripheral Bus Timings" .

[6] RW SPO			SPICLKOUT polarity, please refer to the SPI frame format in "12.3.4 Three Peripheral Bus Timings" for specific meaning.
[5:4] RW FRF			Frame format selection. 00: Motorola SPI frame format; 01: TI synchronous serial frame format; 10: National Microwire frame format; 11: Reserved.
[3:0] RW DSS			Set the data bit width. 0011ÿ4bitÿ 1000ÿ9bitÿ 1101ÿ14bitÿ 0100ÿ5bitÿ 1001ÿ10bitÿ 1110ÿ15bitÿ 0101ÿ6bitÿ 1010ÿ11bitÿ 1111ÿ16bitÿ 0110ÿ7bitÿ 1011ÿ12bitÿ 0111ÿ8bitÿ 1100ÿ13bitÿ Other: reserved.

SPICR1

SPICR1 is Control Register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00



Reset 0	1	1	1	1	1	1	000	0	0	0	0	0

Bits Access Name	Description
[15] RW WaitEn	Waiting to be enabled, it is valid when the FRF of SPICR0 register is configured as National Microwire frame format. 0: Disable; 1: Enable.
[14:8] RW WaitVal	The number of beats to wait between writing and reading in National Microwire frame format. Valid when WaitEn is 1 and the frame format is National Microwire.
[7] RO reserved	Reserved.
[6] RO mode_altase	0: The chip select signal is automatically generated by the chip logic according to the selected timing ns 1: When the Motorola SPI frame format is used, the chip select CS signal is controlled by the SPI enable signal. After enabling, the chip select is pulled low, otherwise the chip select is pulled high .
[5] RO reserved	Reserved.
[4] RW BigEnd	Set the data size endian mode. 0: little endian mode; 1: big endian mode.
[3] RO reserved	Reserved.
[2] RW MS	Set Master or Slave mode, this bit can only be changed when SPI is disabled. 0: Master mode (default); 1: Reserved.
[1] RW SSE	Set SPI enable. 0: disable; 1: enable.
[0] RW LBM	Set the loopback mode. 0: Normal serial interface operation enabled; 1: The output of the transmit serial shift register is internally connected to the input of the receive serial shift register.

SPIDR

SPIDR is the data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	Transmit/receive FIFO. Read: Receive FIFO; Write: Transmit FIFO. If the number of data bits is less than 16, it must be right justified. The transmit logic ignores the upper unused bits, and the receive logic automatically right-aligns the data.

SPISR

SPISR is the status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RO	reserved	Reserved.
[4]	RW	BSY	SPI busy flag. 0: idle; 1: Busy.
[3]	RW	RFF	Whether the receive FIFO is full. 0: less than full; 1: Full.
[2]	RW	RNE	Whether the receive FIFO is not empty. 0: empty; 1: not empty.

[1]	RW	TNF	Whether the transmit FIFO is not full. 0: full; 1: Not full.
[0]	RW	TFE	Whether the transmit FIFO is empty. 0: not empty; 1: Empty.

SPICPSR

SPICPSR is the clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	reserve.
[7:0]	RW	CPSDVSR	Clock division factor. This value must be an even number between 2 and 254, depending on the frequency of the input clock SPICLK. The lowest bit is read as "0".

SPIIMSC

SPIIMSC is the interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RW	EXCLUSIVE	Transmit FIFO interrupt mask. 0: Interrupts are masked when half-empty or less; 1: Interrupts are not masked when half-empty or less.

[2] RW RXIM	Receive FIFO interrupt mask. 0: Interrupts are masked when half-empty or less; 1: Interrupts are not masked on half empty or less.
[1] RW RTIM	Receive timeout interrupt. 0: receive timeout interrupt mask; 1: Receive timeout interrupt is not masked.
[0] RW RORIM	Receive overflow interrupt mask. 0: receive FIFO overflow interrupt mask; 1: receive FIFO overflow interrupt not mask. When the value is "1", the hardware flow control function is enabled, that is, the SPI stops sending data when the receive FIFO is full.

BREATHED

SPIRIS is the raw interrupt status register. A value of "0" means no interruption and a value of "1" means interruption.

Offset Address	Register Name	Total Reset Value
0x018	BREATHED	0x0008

Bit	15 14 13 12 11 10 9 8 7 6 5 4	3	2	1	0
Name	reserved	TXRIS	RXRIS	RTRIS	RORRIS
Reset	0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXRIS	Raw interrupt status of transmit FIFO interrupt.
[2]	RO	RXRIS	Raw interrupt status for receive FIFO interrupts.
[1]	RO	RTRIS	Raw interrupt status of receive timeout interrupt.
[0]	RO	RORRIS	Raw interrupt status of receive overflow interrupt.

SPAM

SPIMIS is the masked interrupt status register. A value of "0" means no interruption and a value of "1" means interruption.

Offset Address	Register Name	Total Reset Value
0x01C	SPAM	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXMIS	Transmit FIFO interrupt masked status.
[2]	RO	RXMIS	Receive FIFO interrupt masked status.
[1]	RO	RTMIS	Receive timeout interrupt masked state.
[0]	RO	RORMIS	Receive overflow interrupt masked status.

SPIICR

SPIICR is the interrupt clear register. Writing a "1" clears the interrupt, writing a "0" has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	reserve.
[1]	RO	RTIC	Clear receive timeout interrupt.
[0]	RO	RORIC	Clear receive overflow interrupt.

SPIDMACR

SPIDMACR is the DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13 12 11	10 9 8 7 6 5	4 3 2	1	0
Name	reserved					TXDMAE	RXDMAE
Reset 0	0	0	0	0 0 0 0 0 0 0 0 0 0		0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved bits.
[1]	WO	TXDMAE	DMA transmit FIFO enable register. 0: disable; 1: enable.
[0]	WO	RXDMAE	DMA receive FIFO enable register. 0: forbidden; 1: enable.

SPITXFIFOCR

SPITXFIFOCR is the transmit FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0009

Bit	15 14	13	12	11	10	9	8 7	6	5	4	3	2	1	0
Name	reserved								TXINTSize			DMATXBRSize		
Reset 0	0	0	0	0	0	0	0 0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RO	reserved	reserve.
[5:3]	RW	TXINTSize	Configure the waterline for transmit FIFO request interrupts. That is, send When the number of data in FIFO is less than or equal to the number of words configured by TXINTSize, TXRIS is valid. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ64ÿ

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize				DMATXBRSize	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[2:0]	RW	DMATXBRSize	Configure the waterline that sends FIFO requests to DMA for burst transfers. That is, when the number of data in the transmit FIFO is less than or equal to the number of words configured by (256-DMATXBRSize), DMATXBREQ is valid, and the word length here is 16 bits. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ128ÿ

SPIRXFIFOCR

SPIRXFIFOCR is the receive FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize				DMARXBRSize	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[15:6]	RO	reserved	reserve.

[5:3]	RW	RXINTSize	Configure the watermark for receive FIFO request interrupts. That is, when the number of data in the receiving FIFO is greater than or equal to the number of words configured by (256-RXINTSize), RXRIS is valid, and the word length here is 16 bits. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ64ÿ 111ÿ64ÿ
[2:0]	RW	DMARXBRSize 010ÿ8ÿ	Configure the waterline for receiving FIFO request DMA for burst transfer. That is, when the number of data in the receive FIFO is greater than or equal to the number of words configured by DMARXBRSize, DMARXBREQ is valid. 000ÿ1ÿ 001ÿ4ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ224ÿ

12.4 3WIRE SPI

12.4.1 Overview

Hi3519V100 provides a 3-wire SPI interface for connecting with MN34120 Sensor.

12.4.2 Working method

The 3-wire SPI works internally on the APB bus clock. The initialization steps are as follows:

Calculate the SPI interface clock as required, and write the configuration into the register SPI_3WIRE_COEF0.

For example: if the SPI interface clock is required to be 1MHz, spi_clk_div should be configured as (50MHz/1MHz)/2 -1

=24, so configure spi_clk_div as 0x18.

The read operation steps are as follows:

Step 1. Write the address of the read register to SPI_3WIRE_COEF1[spi_add], write 1 to SPI_3WIRE_COEF1[spi_rw] .

Step 2. Write 1 to SPI_3WIRE_COEF2[start] to start the read operation.

Step 3. Query SPI_3WIRE_COEF2[spi_busy] until the status bit is 0.

Step 4. Read the required data from SPI_3WIRE_COEF2[spi_rdata].

----Finish

The write operation steps are as follows:

Step 1. Write the address and data of the write register to SPI_3WIRE_COEF1[spi_add] and SPI_3WIRE_COEF1[spi_wdata], SPI_3WIRE_COEF1[spi_rw]ÿ0ÿ

Step 2. Write 1 to SPI_3WIRE_COEF2[start] to start the write operation.

Step 3. Query SPI_3WIRE_COEF2[spi_busy] until the status bit is 0.

----Finish

12.4.3 spi_3wire_reg register overview

An overview of the spi_3wire_reg registers is shown in Table 12-5 .

Table 12-5 spi_3wire_reg register overview (base address is 0x1212_4000)

offset address	name	describe	page number
0x0000	SPI_3WIRE_COEF0	3-wire SPI configuration register 0	12-66
0x0004	SPI_3WIRE_COEF1	3-wire SPI configuration register 1	12-67
0x000C	SPI_3WIRE_COEF2	3-wire SPI configuration register 2	12-67

12.4.4 spi_3wire_reg register description

SPI_3WIRE_COEF0

SPI_3WIRE_COEF0 is 3-wire SPI configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_3WIRE_COEF0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	spi_clk_div
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RW	spi_clk_div	Clock rate of the SPI interface. The value range is 1 to 255. The value of spi_clk_div is used to generate the SPI clock, the formula is FSPICLK=FAPBCLK/(2x(spi_clk_div+1)). Where FAPBCLK is the clock frequency of the bus. For example, the bus clock is 50MHz, and the expected SPI clock is 1MHz, then spi_clk_div should be configured as (50MHz/1MHz)/2 -1 =24ÿ

SPI_3WIRE_COEF1

SPI_3WIRE_COEF1 is the 3-wire SPI configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_3WIRE_COEF1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	spi_add	spi_wdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RW	spi_rw	SPI read and write operation selection. 0: write; 1: Read.
[30:16]	RW	spi_add	SPI operation address.
[15:0]	RW	spi_wdata	SPI write data.

SPI_3WIRE_COEF2

SPI_3WIRE_COEF2 is 3-wire SPI configuration register 2.

Offset Address	Register Name	Total Reset Value
0x000C	SPI_3WIRE_COEF2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	spi_rdata
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:18]	RO	reserved	reserve.
[17]	RO	spi_busy	SPI operation status bit. 1: There is an operation on the SPI bus; 0: SPI bus is in IDLE.
[16]	RW start		Start SPI read and write operations. It can only be started when spi_busy is 0, and the readback value is 0, meaningless.
[15:0]	RO	spi_rdata	SPI read back data.

12.5 MMC/SD/SDIO Controller

12.5.1 Functional description

Functional block diagram

The MMC/SD/SDIO controller (hereinafter referred to as MMC) is used to handle operations such as reading and writing SD/MMC cards, and supports extended peripherals (such as Bluetooth, WiFi, etc.) through the SDIO protocol. Hi3519V100 provides 3 MMC/SD/SDIO controllers.

MMC0 supports devices conforming to the following protocols:

- Secure Digital MemoryÿSD mem-version3.0ÿ Secure Digital I/OÿSDIO-version 3.0ÿ

MMC1 supports devices conforming to the following protocols:

- Secure Digital MemoryÿSD mem-version3.0ÿ Secure Digital I/OÿSDIO-version 3.0ÿ

MMC2 supports devices conforming to the following protocols:

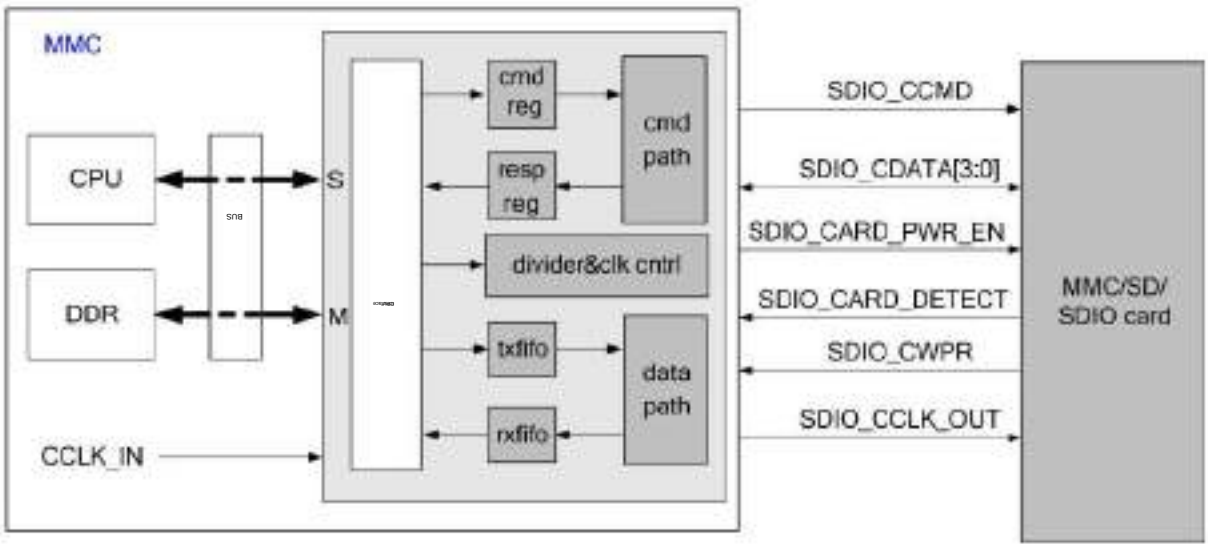
- MultiMediaCardÿeMMC-version 5.0ÿ

說明

Support eMMC-version 5.0, but kernel version 3.16 and above is required.

The functional block diagram of MMC is shown in Figure 12-19 .

Figure 12-19 MMC functional block diagram



Note: S: slave interface; M: master interface.

The MMC is connected to the system through an internal bus and consists of the following units:

The command channel completes the sending of commands and the receiving of responses. The data channel cooperates with the command channel to complete data read and write operations. The interface clock control unit changes the frequency of the interface clock according to requirements, and controls the closing and opening of the interface clock. SDIO_CCLK_OUT can be a frequency divider of CCLK_IN.

The features of MMC are:

Support internal DMA data transfer mode. Support ADMA3 transfer mode, and support commands to be transferred in a queue. Support multi-packet interrupt and timeout interrupt. Support automatic detection of response.

Contains 2 FIFOs for data sending direction and receiving direction, FIFO depth is 256word, supports configurable FIFO threshold, and configurable burst size during DMA transmission.

Support FIFO overflow and underflow interrupt alarm to prevent data transmission errors. Supports CRC generation and verification of commands and data.

The interface clock frequency is

programmable. Support low power mode to turn off MMC clock and interface clock.

The data bit width supports 1, 4bit, and 8bit, which can be selected according to the connected device.

Support block data read and write operations from 1byte to 65535byte.

Support MMC card streaming data reading and

writing. Support SDIO suspend operation, resume operation and read wait operation.

Features supported by MMC4.41: DDR_4bit, DDR_8bit, support GO_PRE_IDLE_STATE command.

eMMC4.41 supports Hardware Reset. Features

supported by eMMC4.5: HS200 (4bit, 8bit), support CMD21, CMD49, support

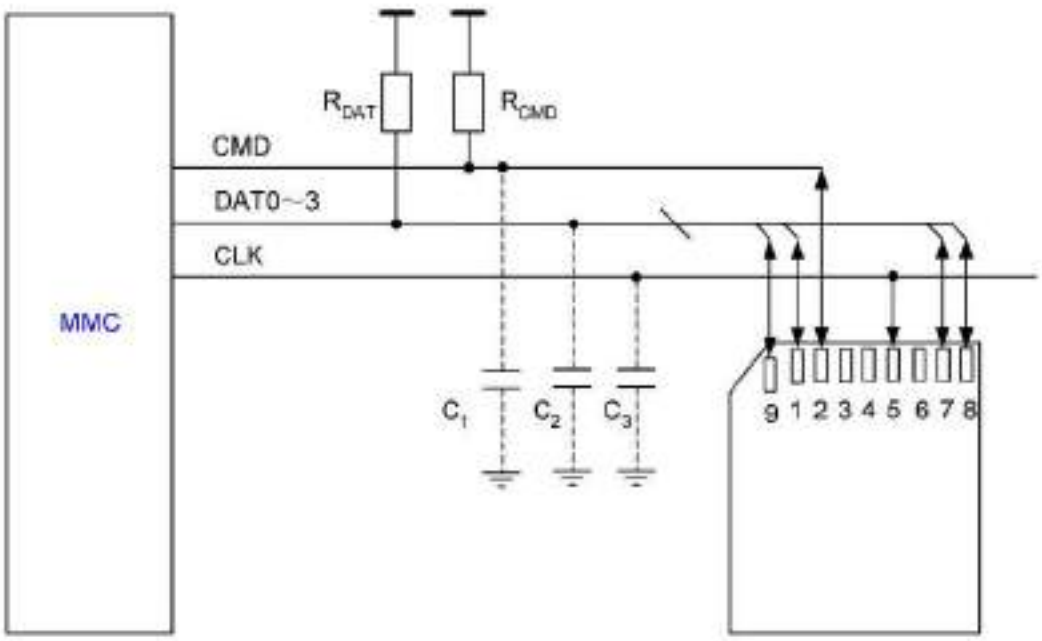
3.3/1.8V voltage (HS200 supports 1.8V).

Features supported by eMMC5.0: HS400 mode.

typical application

The typical application circuit of MMC is shown in Figure 12-20 .

Figure 12-20 Typical application circuit diagram of MMC



The MMC connects with the card device through 1 clock signal line, 1 bidirectional command signal line and 4 bidirectional data signal lines to complete the command and data interaction. Both command signal and data signal work in pull-up mode. The pull-up resistor parameters and the load capacitance limits of each signal line are shown in Table 12-6 .

Table 12-6 Signal cable load parameters

parameter	min max description	
RDATÿRCMD 10kÿ		100kÿ pull-up resistor.
Load capacitance Cx -		30pF load capacitance Cx=Cmmchost+Cbus+Ccard. The maximum load capacitance Ccard of each card is 10pF, so Cmmchost+Cbus should be less than 30pF.
Signal Line Inductive Reactance-		16nH Fppÿ20MHzÿ

注意

In addition to the signal lines in Figure 12-20 , the card slot generally provides mechanical write protection signals and card detection signals. The chip provides these interfaces, which are not shown in the schematic diagram.

command and response

All interactive operations between the MMC and the card device are completed through instructions, including card initialization, register reading and writing, status query, data transmission, etc.

MMC command is 48bit serial data, which is composed of start bit, transmission bit, command serial number, command parameter, CRC check bit and stop bit. After the card receives the command, it will return a 48bit or 136bit response according to the command type.

Figure 12-21 MMC instruction format

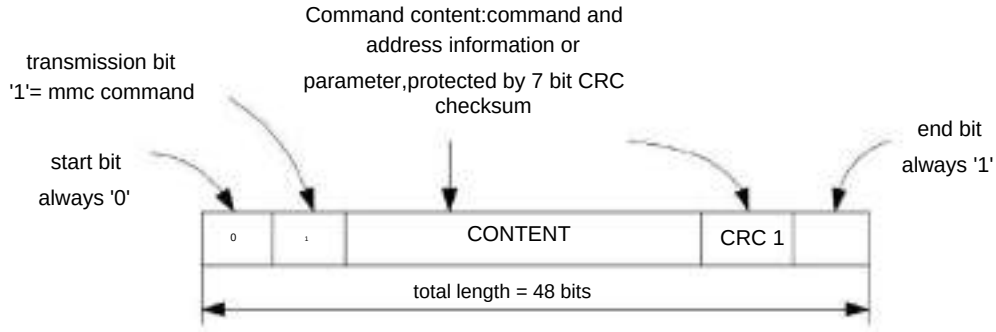
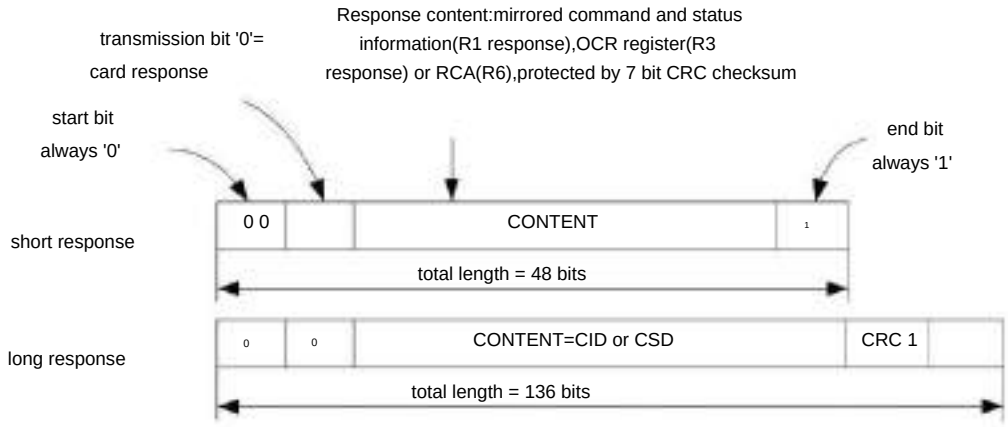


Figure 12-22 MMC command response format



According to whether there is data transmission or not, the commands are divided into the following two types:

non-data transfer instructions

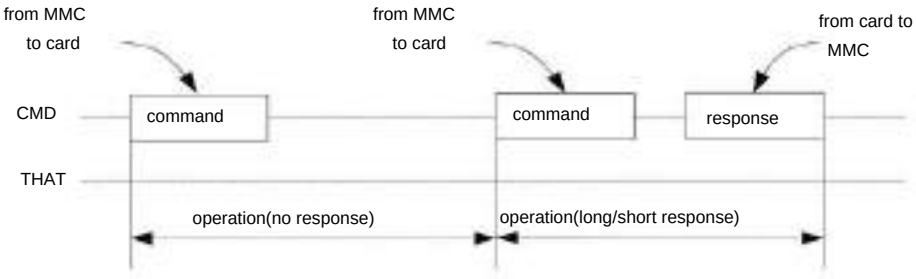
Based on the command signal line CMD, the MMC and the card use serial mode to send commands and receive responses. In addition to the interaction on the command

line, the data transmission command also has data transmission on the data line DAT0~DAT3.

(1) Non-data transfer instructions

The non-data transfer instruction operation between MMC and card device is shown in Figure 12-23 .

Figure 12-23 MMC non-data instruction operation



(2) Data transmission command

The MMC card supports the following data transfer commands:

Streaming data read and write

instructions are only supported by MMC cards, and only one data line (ie DAT0) is used for data transmission without CRC check. The single-block data read and write instruction transfers

a block of data at a time, and there is no need to use the stop command to end a data transfer.

Multi-block data read and write instructions

ÿ predefined block count method

Before multi-block read and write commands, send the block quantity command to specify the amount of data to be transmitted.

ÿ open ended mode

After sending the read and write commands, at the end of the data transmission, a stop command needs to be used to end a data transmission.

The difference between the two methods lies in the way the MMC notifies the card to end a transmission. SD card only supports open ended mode, and MMC card supports both modes.

The multi-block read and write commands of SDIO devices are different from the above two methods. When sending read and write commands, the command parameters include the amount of data to be transmitted.

According to the type of response, commands are divided into the following 3 types:

Unresponsive command

such as card reset command.

short response command

Data transmission instructions, card status inquiries, etc. all belong to this category of instructions. The

long response command

is only used to read the card's register CID and CSD information.

data transmission

Single-block reading and writing and multi-block reading and writing are more commonly used data transmission methods. Usually, the block size of SD/MMC card data transmission is 512byte, and SDIO device can be customized according to the application.

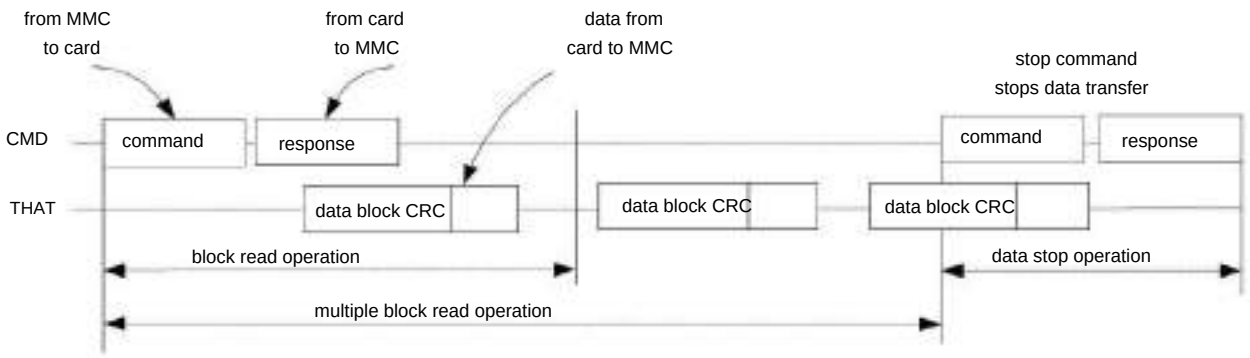
说明

When data transmission is performed in the form of block read and write instructions, the total amount of transmitted data must be an integer multiple of the block size.

Data transmission commands are all short response commands, accompanied by data transmission on the data line. Figure 12-24 and Figure 12-25 show the timing coordination relationship of commands, responses, and data lines .

(1) Single-block and multi-block read operations

Figure 12-24 Single-block and multi-block read operations

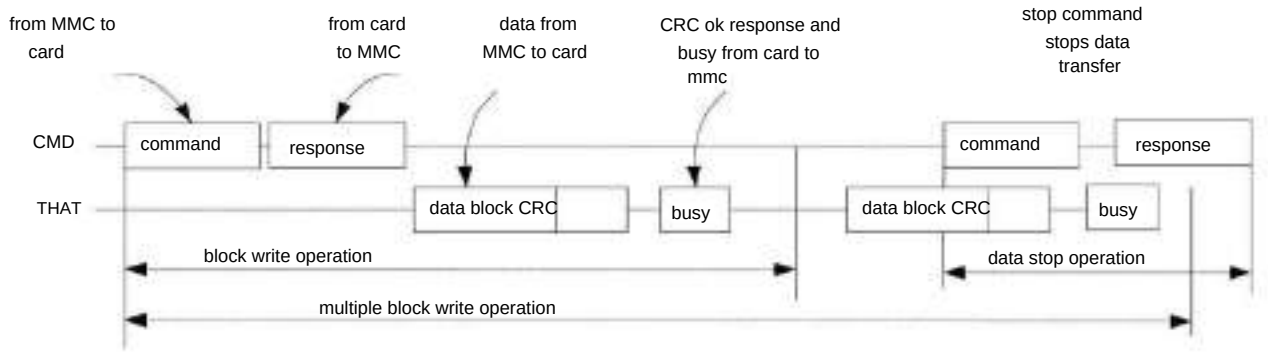


MMC sends single-block or multi-block read commands to the card. In the process of receiving the response, the data in blocks is received, and each block of data contains a CRC check digit to ensure the integrity of data transmission.

When operating a single-block read command, MMC completes a data transmission after receiving one block of data; when operating a multi-block read command, MMC needs to send a stop command to end this data transmission after receiving multiple blocks of data (only open ended multi-block read instruction).

(2) Single-block and multi-block write operations

Figure 12-25 Single-block and multi-block write operations



MMC sends single-block or multi-block write commands to the card. After receiving the response, send data in blocks to the card, each block of data contains a CRC check digit, the card will perform a CRC check on each block of data, and feedback the CRC status to confirm the correctness of the data transmission sex.

When operating a single-block write command, MMC completes a data transmission after sending a block of data; when operating a multi-block write command, MMC needs to send a stop command to complete this data transmission after sending multiple blocks of data (only open ended multi-block read instruction). After the write operation is finished, the card may be in a busy state due to programming Flash, and the MMC needs to query the DAT0 state to confirm that the card is out of the busy state before proceeding to the next operation on the card.

(3) Data transmission format

In block reading and writing, 1bit or 4bit data line can be used for data transmission between MMC and card. Before sending the data transmission command, the data transmission bit width mode (1bit or 4bit) of the MMC and the card should be set respectively to make them consistent. The data bit width of the MMC is set through the register MMC_CTYPE , and the data bit width of the card is set by sending corresponding commands. The data transmission formats in 1bit and 4bit modes are shown in Figure 12-26 and Figure 12-27 .

Figure 12-26 Block data format in 1bit data line transmission mode

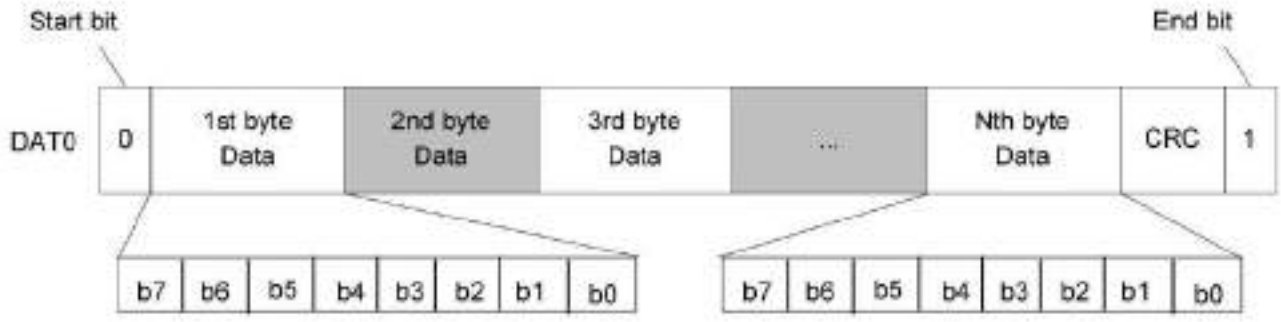
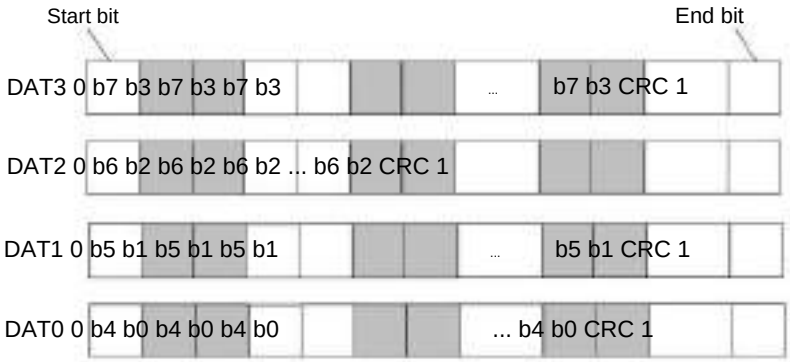


Figure 12-27 Block data format in 4bit data line transmission mode



Speed mode and voltage switching supported by SD3.0

The controller supports SD3.0 Ultra High Speed (UHS-I), and supports voltage switching in SD-mode mode. The transmission modes are shown in Table 12-7 .

Table 12-7 Transmission mode table

model	Supported Input Clocks ÿMHzÿ	card side clock	Maximum Data Width	Voltage
SDR104	100MHz	100MHz	4 bits	1.8V
SDR50	100MHz	100MHz	4 bits	1.8V
DDR50	50MHz	50MHz	4 bits	1.8V
SDR25	50MHz	50MHz	4 bits	1.8V
SDR12	25MHz	25MHz	4 bits	1.8V
HS	50MHz	50MHz	4 bits	3.3V
DS	25MHz	25MHz	4 bits	3.3V
HS400	100MHz	100MHz	8bit	1.8V
HS200	100MHz	100MHz	8bit	1.8V
DDR-4bit	50MHz	50MHz	4 bits	3.3V
DDR-8bit	100MHz	50MHz	8bit	3.3V
MMC HS	50MHz	50MHz	4 bits	3.3V

12.5.2 Application note

说明

For the clock reset register, please refer to 3.2.7 "CRG Register Description".

clock gating

The SDIO_CCLK_OUT clock can be turned off when the software completes the current command or data transfer and does not start a new transfer, but it needs to ensure that the MMC is already in the idle state.

Specific steps are as follows:

Step 1. Read register MMC_STATUS.

Step 2. If both MMC_STATUS[Command fsm states] and MMC_STATUS[data_state_mc_busy] are 0,

Then write "0" to MMC_CTRL , shield MMC interrupt, enable DMA request, etc., and go to step 3. If one of them is non-zero, wait for a delay and return to step 1.

Step 3. Write "0" to the CRG register PERI_CRG49 bit[9] to turn off the SDIO0 clock; write to the CRG register

Write "0" to PERI_CRG49 bit[1], turn off SDIO1 clock, write "0" to CRG register PERI_CRG49 bit[17], turn off SDIO2 (eMMC) clock.

If you need to restart the SDIO0 working clock, write "1" to the CRG register PERI_CRG49 bit[9]; if you need to restart the SDIO1 working clock, write 1 to the CRG register PERI_CRG49 bit[1]; if you need to restart SDIO2(eMMC) If the working clock is used, write 1 to the PERI_CRG49 bit[17] of the CRG register.

----Finish

soft reset

When the data transmission is abnormal and the MMC cannot return to the idle state, configure the CRG register PERI_CRG49 bit[8] to write "1" to soft reset the SDIO0 module, and configure the CRG register PERI_CRG49 bit[0] to write "1" to reset the SDIO1 module. Soft reset, configure the CRG register PERI_CRG49 bit[16] to write "1" to soft reset the SDIO2 module. Query the register MMC_STATUS[Data_busy] to confirm whether the controller is in idle state.

It is recommended to soft reset the MMC before using the MMC and after hot swapping the card.

Work Clock Configuration

Before using MMC, it is necessary to configure an appropriate working clock frequency. SDIO0 is configured through CRG register PERI_CRG49bit[12:10], SDIO1 is configured through CRG register PERI_CRG49 bit[4:2], SDIO2(eMMC) is configured through CRG register PERI_CRG49 bit[20:18].

Interface Clock Configuration

MMC cards that comply with different protocol versions, and when the MMC card is in different states, use different clock frequencies. An even frequency divider is provided inside the MMC to divide the working clock to the appropriate interface clock. The frequency relationship between the controller working clock CCLK_IN and the interface clock SDIO_CCLK_OUT is:

FSDIO_CCLK_OUT=FCCLK_IN/ÿ2 x clk_dividerÿ

Wherein, the frequency division factor clk_divider is the value of the register MMC_CLKDIV[clk_divider]. The clock frequency supported by different card types is different, and the maximum FSDIO_CCLK_OUT on the card side does not exceed 200MHz.

Before changing the clock frequency of the MMC card, it must be ensured that no data or instructions are being transmitted. In order to avoid glitches in the clock output to the MMC card, the following steps should be followed when changing the clock frequency of the MMC card:

Step 1. Turn off the interface clock.

Configure the register MMC_CLKENA to 0x0000_0000, and set the register MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only] and MMC_CMD[Wait_prvdata_complete] are set to "1", waiting for the register MMC_CMD[Start_cmd] to be automatically cleared.

Step 2. Set the frequency division factor.

Set the register MMC_CLKDIV according to the required clock frequency , and set the registers MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to "1", and wait for the register MMC_CMD[Start_cmd] to be automatically cleared.

Step 3. Re-enable the interface clock.

Configure the register MMC_CLKENA as 0x0000_0001, and set the registers MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to "1", and wait for the register MMC_CMD[Start_cmd] to be automatically cleared.

----Finish

Only when registers MMC_CMD [Start_cmd] and MMC_CMD [Update_clk_only] are set to "1", the values of registers MMC_CLKDIV and MMC_CLKENA will be loaded. After loading successfully, MMC will automatically clear the register MMC_CMD[Start_cmd]. If there are other instructions being executed at this time, an HLE (Hardware Locked Error) interrupt will be generated. If an HLE interrupt occurs, clear the interrupt and resend the command.

When there is instruction execution and data transmission, the clock parameters of the card cannot be changed.

initialization

Before exchanging commands and data with the card, MMC needs to be initialized, the steps are as follows:

Step 1. Configure the MMC working clock frequency. Please refer to "Working Clock Configuration" in "12.5.2 Application Notes".

Step 2. When the card is powered on and the command and data signal lines are pulled up stably, soft reset the MMC. See "12.5.2 Application Notes" "Soft Reset" in .

Step 3. Clear the interrupt. Set all bits of register MMC_RINTSTS bit[15:0] to "1" to clear the original interrupt status bit.

Step 4. Set the register MMC_INTMASK. Set all bits of the register MMC_INTMASK bit[15:0] to "1", so that

Can be interrupted by each source.

If DMA is used for data transmission, MMC_INTMASK bit[4] and MMC_INTMASK bit[5] should be set to "0" to shield the receive/send FIFO data request interrupt.

Step 5. Set the register MMC_CTRL[Int_enable] to "1" to enable the MMC interrupt.

Step 6. Configure the timeout parameter register MMC_TMOUT.

Step 7. Configure the FIFO parameter register MMC_FIFOTH.

----Finish

After completing the above steps, you can configure the interface clock and send commands to the card.

non-data transfer instructions

MMC will set the register MMC_RINTSTS bit[2] once it receives a response (regardless of right or wrong or timeout) after the command is sent . The short response is stored in the register MMC_RESP0 , the long response is stored in the registers MMC_RESP0~MMC_RESP3 , the register MMC_RESP3 bit[31] is the highest bit, and the MMC_RESP0 bit[0] is the lowest bit. After the command is issued, its error is reflected by the command response and the error bit of the register MMC_RINTSTS .

The steps to send a non-data transfer command are as follows:

Step 1. Set the corresponding instruction parameters in the register MMC_CMDARG .

Step 2. Set the command register MMC_CMD according to Table 12-8 .

Step 3. Wait for the command to be executed by MMC. If the instruction has been executed, the MMC automatically clears the register MMC_CMD [Start_cmd]ÿ

Step 4. Check if register MMC_RINTSTS bit[12] generates HLE interrupt.

Step 5. Wait for the command to be executed. MMC will register MMC_RINTSTS when it receives a response (whether true or false or timed out) Bit[2] is set to "1", which means Command Done.

Step 6. Check whether there is an abnormal response, and read the response value if necessary.

Read registers MMC_RINTSTS bit[8], MMC_RINTSTS bit[6] and MMC_RINTSTS bit[1] to check response timeout, response CRC error and response error.

----Finish

注意

Only when register MMC_CMD[Start_cmd] is set to "1" and MMC_CMD[Update_clock_registers_only] is set to "0", the values of registers MMC_BYTCNT, MMC_BLKSIZ, MMC_CMDARG and MMC_CMD can be loaded. After loading successfully, MMC automatically clears MMC_CMD[Start_cmd].

If other instructions are being executed, an HLE interrupt will be generated, and the operation can be re-executed at this time. When non-data transfer instructions are executed, the values of registers MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 12-8 Register MMC_CMD configuration reference for non-data transfer instructions (default value)

parameter	value	describe
Start_cmd	1	The start command is sent.

parameter	value	describe
Update_clock_registers_only 0		Off-clock parameter update instruction.
data_transfer_expected	0	non-data transfer instructions.
card_number	0	.
cmd_index	Cmd index Command number.	
send_initialization	0	Set to "1" when the command is card reset, such as command CMD0.
stop_abort_cmd	0	Set "1" when the instruction is to stop data transmission, such as instruction CMD12.
response_length	0	Set to "1" when the response is a long response type.
response_expect	1	Set "0" when there is no response to the command, such as: command CMD0, command CMD4, command CMD15.
Wait_prvdata_complete	1 or 0	The MMC must wait for the data transfer command being processed to complete before sending the command. It is recommended that this bit is always set to "1", unless the command is to query the card status during data transmission or stop the current data transmission.
Check_response_crc	1 or 0	Whether the MMC checks the CRC check digit of the response.

Single block or multi-block read data

The steps to read single or multiple blocks of data are as follows:

Step 1. Write "1" to the register MMC_CTRL[fifo_reset], reset the FIFO pointer, query and wait for the bit to be automatically cleared.

Step 2. Write the number of bytes of data to be transmitted to the register MMC_BYTCNT .

Step 3. Write the block size to register MMC_BLKSIZ .

Step 4. Write the starting address of the read data to the register MMC_CMDARG .

Step 5. Set register MMC_CMD according to Table 12-9 .

For SD/MMC card, use command CMD17/CMD18 for single block/multiple block read operation; for SDIO card, use command CMD53 for single block/multiple block read operation.

Once the register MMC_CMD is written, the MMC executes the command; when the command is sent to the bus, a cmd_done interrupt is generated.

Step 6. Check the registers MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10], if one of them is 1 or both are 1, then read the data in the FIFO from the register MMC_DATA so that MMC can receive the following data; check for data errors at the same time Interrupt, namely register MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13] and MMC_RINTSTS bit[15]. At this point, the program can send a stop command to abort the data transmission.

Step 7. When the register MMC_RINTSTS bit[3] is 1, the data transmission is completed, read from the register MMC_DATA

Fetches the data remaining in the FIFO.

Step 8. If the register MMC_CMD[Send_auto_stop] has been set to "1" when the command is executed , MMC will automatically send a stop command to end a data transmission.

Please refer to "Auto-stop Configuration" in "12.5.2 Application Notes".

----Finish

Table 12-9 Register MMC_CMD configuration reference when reading data in single or multiple blocks (default value)

parameter	value description	
Start_cmd	1	The start command is sent.
Update_clock_registes_only 0		Off-clock parameter update instruction.
card_number	0	.
send_initialization	0	Set to "1" when the command is card reset, such as command CMD0.
stop_abort_cmd	0	Set "1" when the instruction is to stop data transmission, such as instruction CMD12.
send_auto_stop	0 or 1	Please refer to "Auto stop usage configuration" in "12.5.2 Application Note".
transfer_mode	0	block transfer.
read/write	0	Read data from the card.
response_length	0	Data commands are all short responses.
data_transfer_expected	1	Data transfer instructions.
response_expect	1	Set "0" when there is no response to the command, such as: command CMD0, CMD4, CMD15.
cmd_index	Cmd index Command number.	
Wait_prvdata_complete	1 or 0 The master must wait for the data transfer command being processed to complete before sending the command. It is recommended that this bit is always set to 1, unless the command is to inquire about the card status or stop the current data transmission.	
Check_response_crc	1 or 0	Whether the MMC checks the CRC check digit of the response.

Single-block and multi-block write data

The steps to write a single block or multiple blocks of data are as follows:

Step 1. Write "1" to the register MMC_CTRL[fifo_reset], reset the FIFO pointer, query and wait until the bit is automatically cleared zero.

Step 2. Write the size of the data to be transferred to the register MMC_BYTCNT .

Step 3. Write the block size to register MMC_BLKSIZ .

Step 4. Write the starting address of the data to the register MMC_CMDARG .

Step 5. Write data into the FIFO, ie write register MMC_DATA, usually the FIFO should be full at the beginning.

Step 6. Set register MMC_CMD according to Table 12-10 .

For SD/MMC card, use command CMD24/CMD25 for single block/multiple block write operation; for SDIO card, use command CMD53 for single block/multiple block write operation.

Step 7. Check the register MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If one of them is 1 or both are 1, write the register MMC_DATA to fill the FIFO with data; at the same time, check the data error interrupt, that is, check the register MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13] and MMC_RINTSTS bit[15]. If necessary, the program can send a stop command to abort the data transfer. When the register MMC_RINTSTS bit[3] is 1, the data transmission ends.

Step 8. If the register MMC_CMD[Send_auto_stop] has been set to "1" when executing the command , MMC will automatically send a stop command to end a data transmission. Please refer to "Auto-stop Usage Configuration" in "12.5.2 Application Note".

Step 9. Query and wait for the register MMC_STATUS[data_busy] to change from 1 to 0.

----Finish

Table 12-10 Register MMC_CMD configuration reference when writing data in single or multiple blocks (default value)

parameter	value description
Start_cmd	1 Start command sending.
Update_clock_registes_only 0 Non-clock parameter update command.	
card_number	0 .
send_initialization	0 Set to "1" when the command is card reset, such as command CMD0.
stop_abort_cmd	0 Set "1" when the instruction is to stop data transmission, such as instruction CMD12ÿ
send_auto_stop	0 or 1 , please refer to "Auto-stop Configuration" in "12.5.2 Application Note".
transfer_mode	0 block transfers.
read_write	1 Write data to the card.
response_length	0 Data commands are all short responses.
data_transfer_expected	1 Data transfer instruction.
response_expect	1 Set "0" when there is no response to the command, such as: command CMD0, CMD4ÿCMD15ÿ
cmd_index	Cmd index Command sequence number.

parameter	value description
Wait_prvdata_complete	1 or 0 The master must wait until the end of the data transfer command being processed before sending the command. It is recommended that this bit be set to "1" all the time, unless the command is to inquire about the card status or stop the current data transmission.
Check_response_crc	1 or 0 Whether MMC checks the CRC check digit of the response.

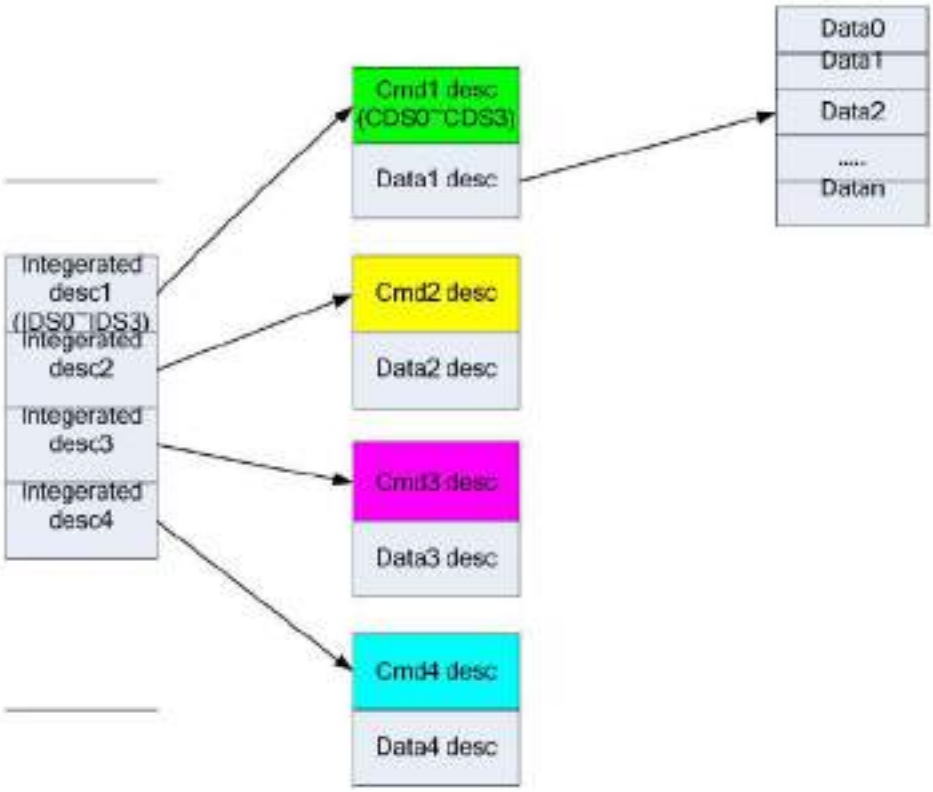
Stream data read and write

The reading and writing method of stream data is consistent with the reading and writing method of block data except that the register MMC_CMD[Transfer_mode] is set to "1". For the transmission of streaming data, it is usually necessary to use the Auto-stop function.

Data transfer in ADMA3 mode

The data and command description substructure is shown in Figure 12-28 .

Figure 12-28 Overall description substructure



Comprehensive Descriptor Structure

IDS0 represents the control information of the integrated descriptor, and the meaning of each bit is shown in Table 12-11 .

Table 12-11 Meaning of each bit of IDS0

bit	name	illustrate
31	OWN	Description sub-property indication. 0: Indicates that the descriptor belongs to the CPU; 1: Indicates that the descriptor belongs to ADMA3. Clear this bit to 0 after the internal ADMA3 completes the data transfer.
30	RES	reserve.
29	INT	Whether to report multi-packet interruption. 0: Do not report interruption; 1: Report interruption.
28:0	RES	reserve.

IDS1 indicates the address information of the command descriptor, and the meaning of each bit is shown in Table 12-12 .

Table 12-12 Meaning of each bit of IDS1

bit	name	illustrate
31:0	The CMD_ADDR command	describes the subaddress, pointing to the command address to be sent.

Command Descriptor Substructure

CDS0 indicates the size of the data block, and the meaning of each bit is shown in Table 12-13 .

Table 12-13 The meaning of each bit of CDS0

bit	name	illustrate
31:16	RES	reserve.
15:0	BLK_SIZE block size for data transfer.	

CDS1 indicates the transmitted data length, and the meaning of each bit is shown in Table 12-14 .

Table 12-14 The meaning of each bit of CDS1

bit	name	illustrate
31:0	BYTECNT The length of the data block to be transferred.	

CDS2 indicates the parameter value of the command, and the meaning of each bit is shown in Table 12-15 .

Table 12-15 Meaning of each bit of CDS2

bit	name	illustrate
31:0	CMD_ARG command command parameter value.	

CDS3 indicates the command configuration value of the command, and the meaning of each bit is shown in Table 12-16 .

Table 12-16 Meaning of each bit of CDS3

bit	name	illustrate
31:0	CMD	command register value.

The data description substructure is the same as that of the descriptor's IDMAC.

ADMA3 initialization

Step 1. Configure the ADMA_DEEPTH register to set the command queue depth.

Step 2. Configure ADMA_TIMEOUT and set the timeout time.

Step 3. Configure ADMA_IDS_ADDR, and configure the start address of the comprehensive descriptor.

Step 4. Configure the MMC_IDINTEN register to mask unnecessary registers.

Step 5. Configure ADMA_CONTROL to enable ADMA3.

Step 6. Create a comprehensive descriptor, command descriptor, and data descriptor linked list, and then configure the ADMA_ID_WRPTR register to set the pointer address of a valid command.

Step 7. ADMA3 tries to get the descriptor from the descriptor linked list.

----Finish

Built-in DMA mode data transmission

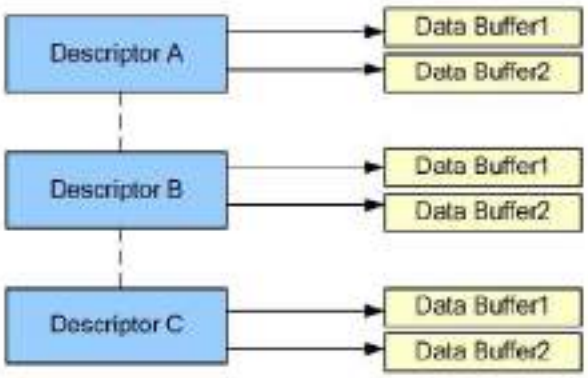
The MMC controller contains a built-in DMA controller (IDMAC), and the IDMAC can move data from the original address to the destination address according to the specified descriptor.

descriptor

IDMAC can use the following two types of descriptors:

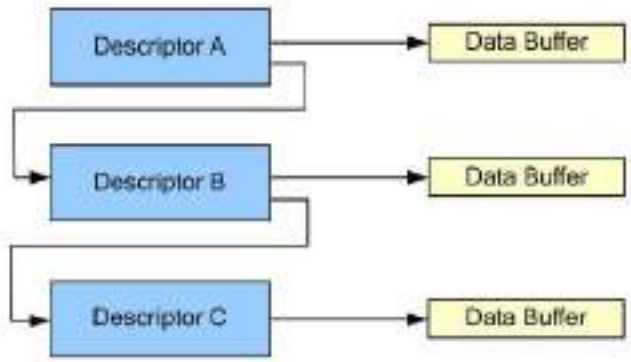
Double Buffer structure: The interval between two descriptors is specified by the DSL bit of the MMC_BMOD register. The schematic diagram of the double buffer structure is shown in Figure 12-29 .

Figure 12-29 Schematic diagram of double buffer structure



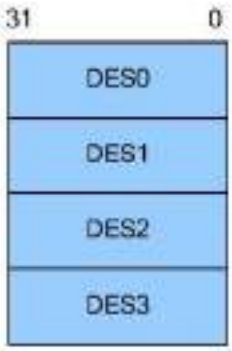
Chain structure: each descriptor points to a unique buffer and the next descriptor. A schematic diagram of the chain structure is shown in Figure 12-30 .

Figure 12-30 Schematic diagram of chain structure



Descriptors must be word-aligned, and each descriptor contains 16bytes of control and status information. The internal structure of the descriptor is shown in Figure 12-31 .

Figure 12-31 The structure of a 32bit wide descriptor



DES0 Protection control and status information, the specific meaning is shown in Table 12-17 .

Table 12-17 Meaning of each bit of DES0

bit	name	illustrate
31	OWN	Description sub-property indication. 0: Indicates that the descriptor belongs to the CPU; 1: Indicates that the descriptor belongs to IDMAC. IDMAC clears this bit to 0 after data transfer using internal DMA
30	THESE	Error status indication when reading or writing the card. 0: no error; 1: Error.
29:6	RES	reserve.
5	IS	Describes the sublink end indication. 0: not the last one; 1: The last descriptor of this link. Only meaningful to the descriptor of the double buffer structure.
4	CH	The meaning of the second address (the address of DES3). 0: The second address in DES3 refers to the address of the second buffer; 1: The second address in DES3 refers to the address of the next descriptor. But when this bit is 1, DES1[25:13] should be 0.
3	FS	If it is 1, it means that the descriptor contains the first data buffer. If the size of the first data buffer is 0, then the next descriptor contains the initial data.
2	LD	If it is 1, it means that the buffer pointed to by this descriptor is the last data buffer.
1	DIC	When it is 1, it prevents the end of data transmission from reporting interrupt.
0	RES	reserve.

DES1 indicates the buffer size, and the specific meaning is shown in Table 12-18 .

Table 12-18 Meaning of each bit of DES1

bit name description		
31:26	RES reserved.	
25:13	BS2 The byte number of the second data buffer must be an integer multiple of 4. This bit is meaningless when DES0[4] is 1.	
12:0	BS1 The byte number of the first data buffer must be an integer multiple of 4.	

DES2 indicates the address pointer of the first data buffer, and the specific meaning is shown in Table 12-19 .

Table 12-19 Meaning of each bit of DES2

bit	name	illustrate
31:0	BAP1	The physical address of the first data buffer must be word-aligned.

DES3 indicates the second address, and its specific meaning is shown in Table 12-20 .

Table 12-20 Meaning of each bit of DES3

bit	name	description
31:0	BAP2	When the double buffer structure is used, it indicates the physical address of the second data buffer. If DES0[4] is 1, this address indicates the physical address of the next descriptor.

initialization

Step 1. Configure the MMC_BMOD register and set the bus parameters.

Step 2. Configure the MMC_IDINTEN register to mask unnecessary registers.

Step 3. Create a send or receive description sub-link list, then configure the MMC_DBADDR register and set the start address.

Step 4. IDMAC tries to get the descriptor from the descriptor linked list.

----Finish

send

Step 1. CPU creates descriptors (DES0~DES3) and sets DES0[31] bit OWN to 1, and prepares data at the same time bufferÿ

Step 2. Write the write data command into the MMC_CMD register.

Step 3. Set TX_Wmark through MMC_FIFOTH register.

Step 4. IDMAC obtains the descriptor and judges whether OWN is 1. If OWN is not 1, it needs to wait for the CPU to release the descriptor. At the same time, the IDMAC will enter the suspend state, and the CPU needs to configure the MMC_PLDMND register to enable the IDMAC to obtain the descriptor again .

Step 5. When OWN is 1, IDMAC moves data from data buffer to MMC internal FIFO.

Step 6. If the interrupt is enabled, the corresponding bit of the IDMAC status register MMC_IDSTS will be updated and the OWN bit will be cleared to 0 after the data transfer is completed.

----Finish

take over

Step 1. CPU creates descriptors (DES0~DES3) and sets DES0[31] bit OWN to 1.

Step 2. Write the read data command into the MMC_CMD register.

Step 3. Set RX_WMark by MMC_FIFOTH register.

Step 4. IDMAC obtains the descriptor and judges whether OWN is 1. If OWN is not 1, it needs to wait for the CPU to release the descriptor. At the same time, the IDMAC will enter the suspend state, and the CPU needs to configure the MMC_PLDMND register to enable the IDMAC to obtain the descriptor again .

Step 5. When OWN is 1, IDMAC moves data from MMC internal FIFO to external data buffer.

Step 6. If the interrupt is enabled, the corresponding bit of the IDMAC status register MMC_IDSTS will be updated and the OWN bit will be cleared to 0 after the data transfer is completed.

----Finish

Auto-stop usage configuration

In the operation of multi-block read and write commands, a stop command is required to complete a data transmission. The stop command can be sent by means of non-data transmission command, or by using the Auto-stop function.

The application occasions of the Auto-stop function are as follows:

SD card

multi-block read and write operations, such as command CMD18 and command CMD25.

MMC card ÿ

stream data read and write

operations. ÿ Multi-block read and write operations in open-ended mode, such as command CMD18 and command CMD25.

It is recommended to use the Auto-stop function provided by the controller. The configuration process is as follows:

Step 1. Set the register MMC_CMD[Send_auto_stop] to “1” during the block data transfer instruction operation .

Step 2. After all data transfer is completed, MMC automatically sends a stop command so that the card can return to the corresponding status.

Step 3. Check the register MMC_RINTSTS[auto_cmd_done] to determine whether the stop command is completed. Its response is held in register MMC_RESP1 .

----Finish

Stop or abort data transfer

The stop command is used to interrupt the data transfer between MMC and the card, and the stop command is used to interrupt the I/O data transfer (only for SDIO_IOONLY or SDIO_COMBO).

The usage of these two instructions is as follows:

stop command

This command can be sent at any stage of data transfer. Because this instruction is used to stop data transmission, it is necessary to set register MMC_CMD bit[5:0] to instruction CMD12, register MMC_CMD bit[14] to 1, and register MMC_CMD bit[13] to 0. abort command

This command is only used for SDIO_IOONLY or SDIO_COMBO. In order to stop the data transmission, it is necessary to set the register CCCR[ASx] of the SDIO card through the command CMD52.

Suspend and Resume operations

For the SDIO card (up to 7 functional devices inside), MMC can suspend the data transmission of a certain functional device through the Suspend operation, and relinquish the SD interface bus to another functional device with higher priority. After the high-priority functional device completes the data transmission, MMC resumes the incomplete transmission of the previous functional device through the Resume operation.

Suspend and Resume operations are realized by setting the register CCCR of the SDIO card. To read and write register CCCR, use instruction CMD52.

Suspend operation steps are as follows:

Step 1. Check the register CCCR[SBS] to determine whether the SDIO card supports suspend/resume operation.

Step 2. Check the registers CCCR[FSx] and [BS] to determine whether the functional device to be suspended is transmitting data.

If [BS] is 1, the functional device specified by [FSx] bit is in data transmission.

Step 3. Set the register CCCR[BR] to "1" to suspend the current data transmission.

Step 4. Check whether the status of registers CCCR[BS] and [BR] is cleared.

[BS] (Bus Status) remains 1 while the data bus is being used. [BR] (Bus Release) remains 1 until the bus is fully released. When both [BR] and [BS] are 0, the data transmission of the selected function device is suspended.

Step 5. If an ongoing read operation is suspended, the register must be set after the suspend operation completes successfully MMC_CTRL[Abort_read_data] to reset the data transmission function of MMC. After reset, the register MMC_CTRL[Abort_read_data] is automatically cleared.

Step 6. Read the register MMC_TCBCNT to get the number of transferred data bytes.

----Finish

Resume operation steps are as follows:

Step 1. Check that the card is not transmitting to confirm that the bus is idle.

Step 2. If the card is in the disconnect state, use the command CMD7 to select it. The status of the card can be commanded by CMD52/CMD53 get.

Step 3. Check if the functional device to be restored is ready for data transfer (query register CCCR[RF]). if [RF]=1, the functional device is ready for data transmission.

Step 4. To resume the transfer, write the function device number into the register CCCR[FS] using the command CMD52. send command

At the same time of CMD52, MMC should be started to enter the data transmission state, that is, the size of the block is written to the register MMC_BLKSIZ , and the remaining amount of data to be transmitted is written to the register MMC_BYTCNT .

The configuration of the register MMC_CMDARG is shown in Table 12-21 , and the configuration of the register MMC_CMD is similar to the block transfer.

Step 5. After the command CMD52 is successfully sent, the data transmission returns to normal. Read the DF of the SDIO device (Resume Data Flag) flag bit, if it is 1, the data starts to be transmitted while the function is restored; if it is 0, there is no data to be transmitted.

Step 6. If the DF flag is 0, in the case of reading data, MMC will wait for a period of time and generate a data timeout error interruption.

----Finish

Table 12-21 Register MMC_CMDARG configuration reference during Resume operation

MMC_CMDARG value		describe
Bit[31]	1	Read and write flags.
Bit[30:28]	0	Function device number, access register CCCR.
Bit[27]	1	Real-time flag, read after write.
Bit[26]	.	.
Bit[25:9]	0x0D	register address.
Bit[8]	.	.
Bit[7:0]	The restored function number writes data.	

注意

After the system is in low power consumption mode, it cannot be woken up by MMC.

Read wait operation

The read wait operation is used to suspend the data transmission of the current functional device of the SDIO card. The MMC decides how long to suspend data transfers as needed.

Read wait operation steps are as follows:

Step 1. Check whether the card supports read wait operation.

Use the command CMD52 to read the register CCCR[SRW]. If it is 1, all functional devices of the card support read wait operation.

Step 2. Set the register MMC_CTRL[Read_wait] to "1".

Step 3. To resume data transfer, clear register MMC_CTRL[Read_wait].

----Finish

12.5.3 Register overview

An overview of the MMC registers is shown in Table 12-22 .

Table 12-22 MMC register overview (SDIO0 base address is 0x100C_0000, SDIO1 base address is 0x100D_0000, EMMC base address is 0x100E_0000)

offset address name	describe	page number
0x0000 MMC_CTRL	MMC Control Register	12-92
0x0004 MMC_PWREN	Power_en Control Register	12-94
0x0008 MMC_CLKDIV	Clock frequency division coefficient register, display module output clock and input clock frequency division ratio	12-95
0x0010 MMC_CLKENA clock enable register		12-95
0x0014 MMC_TMOUT	timeout register	12-96
0x0018 MMC_CTYPE	card type register	12-96
0x001C WITHOUT MMC_BLK	Block Size Configuration Register	12-97
0x0020 MMC_BYTCNT block transfer count register		12-97
0x0024 MMC_INTMASK	MMC Interrupt Mask Register	12-98
0x0028 MMC_CMDARG	MMC instruction parameter register	12-99
0x002C MMC_CMD	MMC command register	12-100
0x0030 MMC_RESP0	MMC Response Register 0	12-102
0x0034 MMC_RESP1	MMC Response Register 1	12-103
0x0038 MMC_RESP2	MMC Response Register 2	12-103
0x003C MMC_RESP3	MMC Response Register 3	12-104
0x0040 MMC_MINTSTS	MMC Masked Interrupt Status Register	12-104
0x0044 MMC_RINTSTS	MMC Raw Interrupt Status Register	12-105
0x0048 MMC_STATUS	MMC status register	12-106
0x004C MMC_FIFOTH	FIFO Watermark Value Register	12-108
0x0050 MMC_CDETECT card detection register		12-109
0x0054 MMC_WRTPRT card write protection register		12-109
0x005C MMC_TCBCNT sent to the card byte number register		12-110
0x0060 MMC_TBBCNT	BIU FIFO transmit data byte number register	12-110

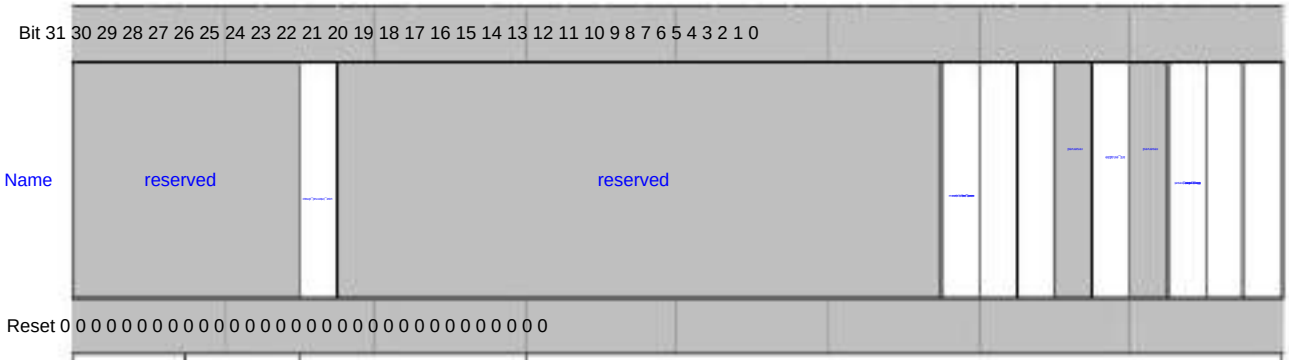
offset address name	describe	page number
0x0064 MMC_DEBNCE debounce counter		12-111
0x0074 MMC_UHS_REG	UHS-1 Register	12-111
0x0078 MMC_CARD_RSTN EMMC device reset control register		12-112
0x0080 MMC_BMOD	bus mode register	12-113
0x0084 MMC_PLDMND	Poll demand register	12-113
0x0088 MMC_DBADDR describes the base address register of the sub-link list		12-114
0x008C MMC_IDSTS	IDMAC Status Register	12-114
0x0090 MMC_IDINTEN	IDMAC Interrupt Enable Register	12-114
0x0094 MMC_DSCADDR current description subaddress register		12-117
0x0098 MMC_BUFADDR current data buffer address register		12-119
0x00B0 ADMA_CONTROL adma3 control register		12-120
0x00B4 ADMA_IDS_ADDR queue start address register		12-121
0x00B8 ADMA_DEEPTH queue depth register		12-121
0x00BC ADMA_ID_RDPTR queue read pointer register		12-121
0x00C0 ADMA_ID_WRPTR queue write pointer register		12-122
0x00C4 ADMA_TIMEOUT	timeout configuration register	12-122
0x0100 MMC_CARDTHRCTL threshold control register		12-120
0x0108 MMC_UHS_REG_EXT	UHS Extended Registers	12-123
0x010C MMC_DDR_REG	EMMC4.5 DDR START bit detection control register	12-124
0x0110 MMC_ENABLE_SHIFT	phase shift register	12-125
0x0200 MMC_DATA	Data register, for FIFO entry address 12-126	

12.5.4 Register Description

MMC_CTRL

MMC_CTRL is the MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000



Bits	Access Name		Description
[31:26]	RO	reserved	reserve.
RW	use_internal_dmac		Whether to use the built-in DMA to move data. 0: CPU uses slave interface to move data; [25] 1: Use internal DMA to move data.
[24:9]	RO	reserved	reserve.
[8] RW	abort_read_data		Whether to abort during reading data. 0: Invalid; 1: After sending the suspend command during the read operation, the software asks the card to find when the suspend appears. Once the suspend appears, the software will set this bit to "1", so that the data transmission state machine returns to the Idle state and waits for the next block transmission. After the state machine returns to the Idle state, this bit is automatically cleared.
[7] RW	send_irq_response		Send interrupt response control. 0: invalid; 1: Send an automatic IRQ reply. This bit is automatically cleared when the reply has been sent. In order to wait for the MMC to generate an interrupt, the host sends the command CMD40 and waits for the interrupt reply from the MMC. At the same time, if the host does not want to stay in the interrupt waiting state, it can set this bit to "1", send the command CMD40 and return to the IDLE state.
[6] RW	read_wait		Read wait control. 0: disable read waiting; 1: Enable read wait. This bit is only used on the card with SDIO function, and the card is required to support the read wait function.
[5]	RO	reserved	reserve.

[4] RW int_enable			Global interrupt enable. 0: forbidden; 1: enable. When this bit is valid and an interrupt source is enabled, the interrupt output is valid.
[3]	RO	reserved	reserve.
[2] RW dma_reset			Internal DMAC soft reset control. 0: invalid; 1: Reset internal DMA interface. This bit is automatically reset after two AHB clock cycles.
[1] RW fifo_reset			Internal FIFO soft reset control. 0: invalid; 1: Reset FIFO pointer. This bit is automatically reset when the reset operation is complete.
[0] RW controller_reset			Controller soft reset control. 0: invalid; 1: Reset MMC/SD/SDIO Host module.

MMC_PWREN

MMC_PWREN is the Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0] RW		power_enable	POWER control. 0: power off; 1: Turn on the power.

MMC_CLKDIV

MMC_CLKDIV is the clock frequency division coefficient register, which displays the frequency division ratio of the module output clock and input clock. If the input clock of the module is 40MHz and the register configuration is 1, the output clock is 20MHz. The clock frequency division factor value is 2×N. For example, when N is 0x0, 2×0=0 (no frequency division); when N is 0x1, it is 2 frequency division; when N is 0xFF, it is 510 frequency division.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	clk_divider0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:8]	RO	reserved	reserve.
[7:0]	RW clk_divider0		SDIO clock frequency division factor. The clock frequency division coefficient is 2*n, for example, 0 means no frequency division, 1 means 2 frequency division, ff means 510 frequency division and so on.

MMC_CLKENA

MMC_CLKENA is the clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:17]	RO	reserved	reserve.
[16]	RW cclk_low_power		Low power control of the card, used to turn off the card clock. 0: no low power consumption mode; 1: Low power mode. When the card is in IDLE state, stop the card clock. This function is generally only used for MMC/SD card. For SDIO, the clock cannot be stopped in order to detect the interrupt.
[15:1]	RO	reserved	reserve.

[0] RW	cclk_enable		Card clock enable control. 0: clock off; 1: Clock enabled.

MMC_TMOUT

MMC_TMOUT is the timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	data_timeout	response_timeout
Reset	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 0 1 0 0 0 0 0 0

Bits	Access	Name	Description
[31:8]	RW	data_timeout	Card data transmission timeout time, this value is also used as CPU data starvation timeout time. The unit is the mmc_clk cycle of the card.
[7:0]	RW	response_timeout	Reply timeout time, the unit is the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is the card type register.

Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.

[16] RW	card_width_0		Configure the bus width of the card. 0: not 8bit mode; 1: 8bit mode. The following is the description of the card configuration: If bit[16]=0, the card will be in 1bit or 4bit mode, depending on the configuration of bit[0].
[15:1] RO	reserved		reserve.
[0] RW	card_width_1		Configure the bus width of the card. 0: 1bit mode; 1: 4bit mode.

MMC_BLKSIZ

MMC_BLKSIZ is the block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	block_size
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	block_size	block size value, the initial value is 512byte/block.

MMC_BYTCNT

MMC_BYTCNT is the block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	byte_count	The number of bytes to be transferred should be an integer multiple of the block size. If it is non-block transfer, this register needs to be set to "0", at this time the software must issue a stop/abort command to control the data transfer operation.

MMC_INTMASK

MMC_INTMASK is the MMC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	sdio_int_mask	Interrupt mask control. 0: shielded; 1: enable.

[15:0]	RW	int_mask	Mask interrupts. 0: Shield; 1: enable. The corresponding meaning of each bit is as follows: Bit[15]ÿEnd-bit error (read)/Write no CRC (EBE) Bit[14]ÿAuto command done (ACD) Bit[13]ÿStart-bit error (SBE) /Busy Complete Interrupt(BCI) Bit[12]ÿHardware locked write error (HLE) Bit[11]ÿFIFO underrun/overrun error (FRUN) Bit[10]ÿData starvation-by-host timeout(HTO) /Volt_switch_int Bit[9]ÿData read timeout (DRTO) Bit[8]ÿResponse timeout (RTO) Bit[7]ÿData CRC error (DCRC) Bit[6]ÿResponse CRC error (RCRC) Bit[5]ÿReceive FIFO data request (RXDR) Bit[4]ÿTransmit FIFO data request (TXDR) Bit[3]ÿData transfer over (DTO) Bit[2]ÿCommand done (CD) Bit[1]ÿResponse error (RE) Bit[0]ÿCard detect (CD)

MMC_CMDARG

MMC_CMDARG is the MMC instruction parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

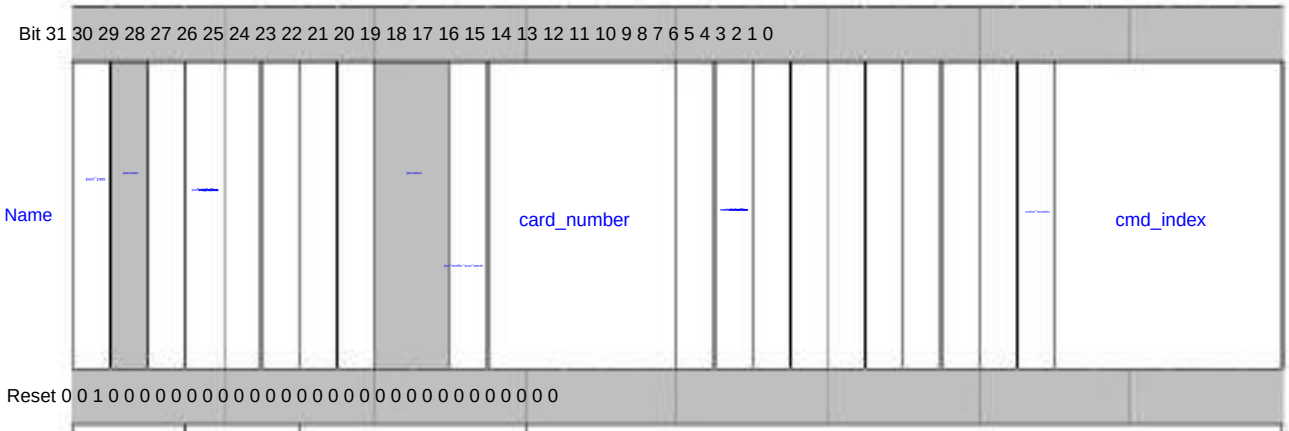
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cmd_arg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	cmd_arg	Configure command parameters transmitted to the card. Command parameters are related to the protocol, and each command corresponds to a specific command parameter.

MMC_CMD

MMC_CMD is the MMC command register.

Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x2000_0000



Bits	Access	Name	Description
[31]	RW	start_cmd	Launch control. 0: do not start; 1: Start command. This bit is cleared when the command has been passed to the CIU. The CPU is not allowed to modify this register. If modified, a hardware lock error interrupt is generated. The CPU needs to check this bit after sending the command, and send the next command after checking that the bit becomes 0.
[30]	RO	reserved	reserve.
[29]	RW	use_hold_reg	Use Hold register. 0: The CMD and DATA signals sent to the card do not pass through the HOLD register; 1: The CMD and DATA signals sent to the card go through the HOLD register.
[28]	RW	volt_switch	Voltage switching control. 0: Disable voltage switching; 1: Enable voltage switching.
[27]	RW	boot_mode	Boot mode. 0: Forced Boot mode; 1: Alternate Boot mode.
[26]	RW	disable_boot	Disable Boot. When the software enables this bit and Start_cmd at the same time, the controller terminates the Boot operation. It is not allowed to enable Enable_boot and Disable_boot at the same time.

[25] RW	expect_boot_ack		Enable Boot Response. When the software enables this bit and Enable_boot at the same time, the controller will detect the Boot response signal, that is, "0-1-0" sequence.
[24] RW	enable_boot		Enable Boot. This bit can only be used in "Forced Boot Mode". When the software enables this bit and Start_cmd at the same time, the controller pulls down the CMD signal to start the Boot process. It is not allowed to enable Enable_boot and Disable_boot at the same time.
[23:22] RO		reserved	reserve.
[21] RW		command; update_clock_regis values of the registers tes_only	Whether to update automatically. 0: Normal command sequence, registers MMC_CMD, MMC_CMDARG, MMC_TMOUTÿMMC_CTYPEÿMMC_BLKSIZÿ The value of MMC_BYTCNT will be passed from BIU to CIU. CIU uses the new value of the register in the new 1: No command is sent, only the clock register value of the card clock domain is updated. The MMC_CLKDIV, MMC_CLKENA are converted to the card clock domain. Convert the card clock (conversion frequency and clock switch) without sending commands to the card, used to adjust the card clock frequency and control the card clock switch. This bit needs to be set to "1" every time the card clock is changed. At this time, no command will be sent to the card, and no Command Done interrupt will be generated.
[20:16] RW	card_number	Serial number of the card being used.	
[15] RW	send_initialization		Whether to send the initial sequence. 0: Do not send the initial sequence before sending the Send_initialization command ("1" for 80 clock cycles); 1: Send the initial sequence before sending the Send_initialization command. When the card is powered on, before sending any command, it must first send the initial sequence for initialization, that is, this bit is set to "1".
[14] RW	stop_abort_cmd		When the open_end or fixed-length data transmission operation is in progress, the meaning of the value of this bit is as follows. 0: Do not send stop/abort command; 1: Send stop/abort command to terminate the ongoing data transmission.
[13] RW		completed); wait_prvdata_complete	Whether to send the command immediately. 0: Send the command immediately (even if the previous data transmission is not 1: Wait until the previous data transmission is completed before sending the command. "0" is a typical value, which is used to read status or interrupt transmission during data transmission.
[12] RW	send_auto_stop		Whether to send stop command. 0: No stop command will be issued after data transmission; 1: Stop command will be issued after data transmission. This bit is ignored during non-data transfers.

[11] RW transfer_mode			transfer mode. 0: block transmission command; 1: stream transmission command. This bit is ignored during non-data transfers.
[10] RW read_write			Read-write control. 0: read data from the card; 1: Write data to the card. This bit is ignored during non-data transfers.
[9] RW		indication. card; ted data_transfer_expec	Data transfer 0: no data transfer from 1: There is data output from the card.
response; [8] RW check_response_crc		1: Check CRC	Whether to CRC check. 0: Do not check CRC response. Some command replies did not return a valid CRC. In order to prohibit the Host from checking the CRC, the software needs to disable this function for these commands.
[7] RW response_length			Response length. 0: Short response is output from the card; 1: Long response is output from the card. The long response is 128bit, and the short response is 32bit.
[6] RW response_expect			Is there a response. 0: no response is output from the card; 1: response is output from the card.
[5:0] RW cmd_index			Command sequence number.

MMC_RESP0

MMC_RESP0 is MMC response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	response0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	response0	Bit[31:0] of Response.

MMC_RESP1

MMC_RESP1 is MMC response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	response1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	response1	Bit[63:32] of the long Response. When CIU issues Auto-stop command, the response will be saved in this register. The response of the previous command will still be saved in the register MMC_RESP0 . Auto-stop is only used for data transmission, and the reply type is always short response.

MMC_RESP2

MMC_RESP2 is MMC response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	response2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	response2	Bit[95:64] of the long Response.

MMC_RESP3

MMC_RESP3 is MMC response register 3.

Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	response3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	response3	Bit[127:96] of the long Response.

MMC_MINTSTS

MMC_MINTSTS is the MMC masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	int_status
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RO	sdio_interrupt	Interrupt mask status. SDIO interrupt is valid only when the corresponding MMC_INTMASK [sdio_int_mask] is enabled. 0: no SDIO interrupt output from the card; 1: There is SDIO interrupt output from the card.

[15:0] RO		int_status	state of each interrupt. Bit[15]ÿEnd-bit error(read)/write no CRC(EBE) Bit[14]ÿAuto command done(ACD) Bit[13]ÿStart bit error(SBE)/Busy Complete Interrupt(BCI) Bit[12]ÿHardware locked write error(HLE) Bit[11]ÿFIFO underrun/overrun error(FRUN) Bit[10]ÿData starvation by host timeout(HTO)/Volt_switch_int Bit[9]ÿData read timeout(DRTO) Bit[8]ÿResponse timeout(RTO) Bit[7]ÿData CRC error(DCRC) Bit[6]ÿResponse CRC error(RCRC) Bit[5]ÿReceive FIFO data request(RXDR) Bit[4]ÿTransmit FIFO data request(TXDR) Bit[3]ÿData transfer over(DTO) Bit[2]ÿCommand done(CD) Bit[1]ÿResponse error(RE) Bit[0]ÿCard detect(CD)

MMC_RINTSTS

MMC_RINTSTS is the MMC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	int_status
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

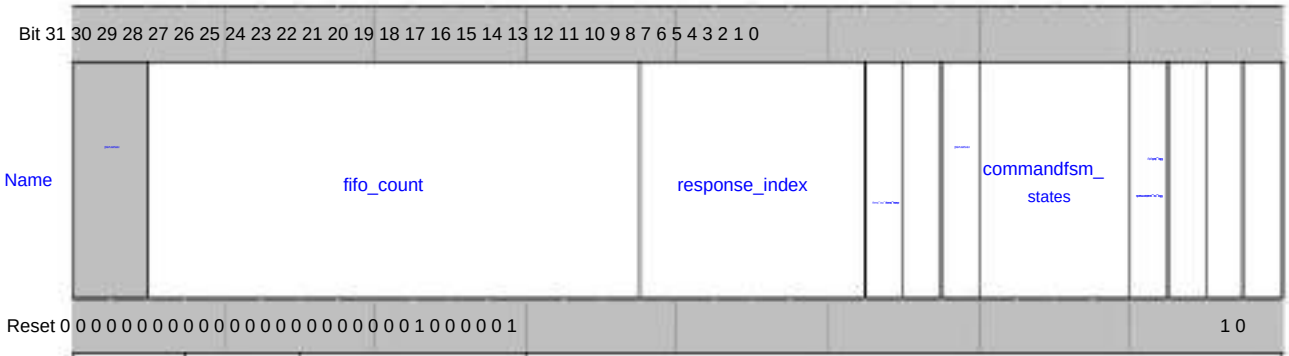
Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	sdio_interrupt	interrupt the original state. 0: no SDIO interrupt output from the card; 1: There is SDIO interrupt output from the card. The value of the interrupt status bits is independent of the interrupt mask.

[15:0] RW	int_status		Raw state of each interrupt. Write "1" to clear, write "0" not to modify. The value of the interrupt status bits is independent of the interrupt mask. Bit[15]ÿEnd-bit error (read)/write no CRC (EBE) Bit[14]ÿAuto command done (ACD) Bit[13]ÿStart bit error(SBE)/Busy Complete Interrupt(BCI) Bit[12]ÿHardware locked write error (HLE) Bit[11]ÿFIFO underrun/overrun error (FRUN) Bit[10]ÿData starvation by host timeout(HTO)/Volt_switch_int Bit[9]ÿData read timeout (DRTO)/Boot Data Start(BDS) Bit[8]ÿResponse timeout (RTO)/Boot Ack Received(BAR) Bit[7]ÿData CRC error (DCRC) Bit[6]ÿResponse CRC error (RCRC) Bit[5]ÿReceive FIFO data request (RXDR) Bit[4]ÿTransmit FIFO data request (TXDR) Bit[3]ÿData transfer over (DTO) Bit[2]ÿCommand done (CD) Bit[1]ÿResponse error (RE) Bit[0]ÿCard detect (CD)

MMC_STATUS

MMC_STATUS is the MMC status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106



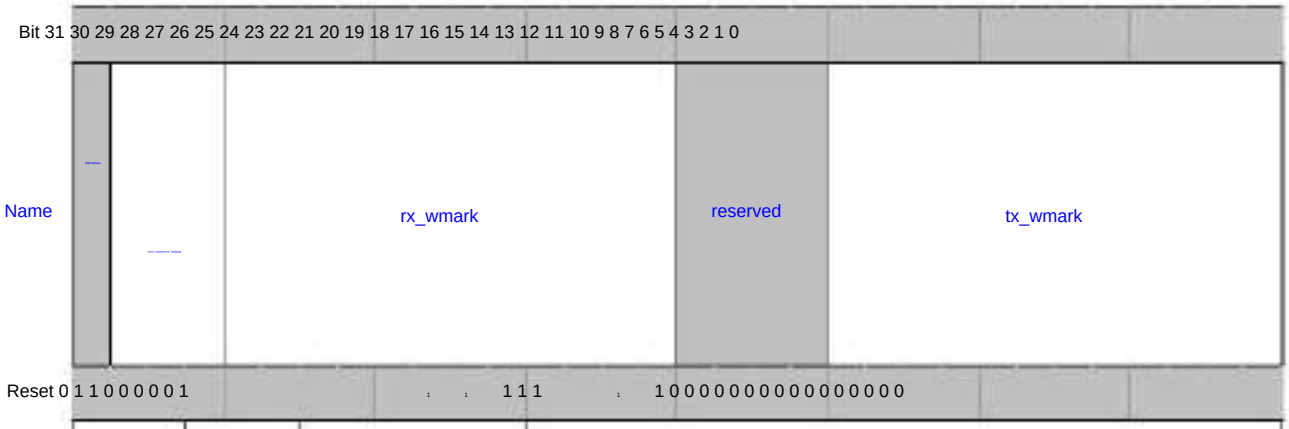
Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29:17]	RO	fifo_count	FIFO count value.
[16:11]	RO	response_index	The serial number of the previous response, including the Auto-stop response.

[10] RO		data_state_mc_bus 0:	Data send and receive state machine state. data transmission/reception state machine is idle; y 1: The data transmit/receive state machine is busy.
[9]	RO	data_busy	The state of data_busy indicated by DAT[0]. 0: card idle; 1: The card is busy.
[8]	RO	reserved	reserved
[7:4] RO		commandfsm_state 0x7ÿ s	Command state machine state. 0x0ÿIdleÿ 0x1ÿSend init sequenceÿ 0x2ÿTx cmd start bitÿ 0x3ÿTx cmd tx bitÿ 0x4ÿTx cmd index +argÿ 0x5ÿTx cmd crc7ÿ 0x6ÿTx cmd end bitÿ Rx resp start bitÿ 0x8ÿRx resp IRQ responseÿ 0x9ÿRx resp tx bitÿ 0xAÿRx resp cmd idxÿ 0xBÿRx resp dataÿ 0xCÿRx resp crc7ÿ 0xDÿRx resp end bitÿ 0xEÿCmd path wait NCCÿ 0xFÿWaitÿCMD-to-response turnaroundÿ
[3]	RO	fifo_full	FIFO full flag. 0: FIFO empty; 1: FIFO is full.
[2]	RO	fifo_empty	FIFO empty flag. 0: FIFO is not empty; 1: FIFO empty.
[1]	RO	reached; fifo_tx_watermark	Whether the FIFO has reached the Transmit watermark level. 0: Watermark not 1: Reach the waterline.
[0]	RO	reached; fifo_rx_watermark	Whether the FIFO has reached the Receive watermark level. 0: Watermark not 1: Watermark reached.

MMC_FIFOTH

MMC_FIFOTH is the FIFO watermark value register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x60FF_0000



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:28]	RW	Multiple_Transacti on_Size	The burst length of the transfer. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ256ÿ
[27:16]	RW	rx_wmark	FIFO threshold watermark level when reading data. When FIFO count is greater than this value, enable DMA request. In order to complete the remaining data after data transfer, no matter what the value is, a DMA request will be generated. In non-DMA mode, enable RXDR interrupt. If the FIFO count is not greater than this value after the data transfer is complete, no interrupt will be generated. This requires software to actively poll the DTD interrupt to read the remaining data. In DMA mode, when the data transfer ends, even if the remaining data is lower than the threshold, the DMA will send a single transfer request to read the data until a DTD breaks. Limit: RX_WMark(FIFO_DEPTH) – 2. Suggestion: Configure to (FIFO_DEPTH/2)–1.
[15:12]	RO	reserved	reserve.

[11:0] RW tx_wmark			FIFO threshold watermark level when sending data. When FIFO count is less than this value, enable DMA request. In order to complete the remaining data after data transfer, no matter what the value is, a DMA request will be generated. In non- DMA mode, enable RXDR interrupt. If the FIFO count is not greater than this value after the data transfer is complete, no interrupt will be generated. This requires software to actively poll the DTD interrupt to read the remaining data. In DMA mode, when the data transfer ends, even if the remaining data is lower than the threshold, the DMA will send a single transfer request to read the data until a DTD breaks. Limit: TX_WMark(FIFO_DEPTH) – 2. Recommendation: Request when greater than (FIFO_DEPTH/2)–1.

MMC_CDETECT

MMC_CDETECT is the card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0001

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RO	card_detect_n	Card detect signal. The value is determined by the pin SDIO_CARD_DETECT.

MMC_WRTPRT

MMC_WRTPRT is the card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	write_protect	Card write protect signal. The value is determined by the pin SDIO_CWPR.

MMC_TCBCNT

MMC_TCBCNT is the byte number register sent to the card.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_card_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	trans_card_byte_co 32bit to avoid read-coherency errors.	The number of bytes sent from CIU to card. When the AHB bus accesses this register, unt 32bit should be read at one time

MMC_TBBCNT

MMC_TBBCNT is the byte number register of data transmitted by BIU FIFO.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_co 32bit time	The byte number of data transferred between CPU/DMA and BIU FIFO. When the AHB bus accesses this register, unt 32bit should be read at one time to avoid read-coherency errors.

MMC_DEBNCE

MMC_DEBNCE is the debounce counter.

Offset Address	Register Name	Total Reset Value
0x0064	MMC_DEBNCE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								debounce_count																							
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:0]	RW	debounce_count	The number of bus clock cycles used by the debounce filter logic, the typical debounce time is 5ms-25ms.

MMC_UHS_REG

MMC_UHS_REG is the UHS-1 register.

Offset Address	Register Name	Total Reset Value
0x0074	MMC_UHS_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	ddr_reg	DDR mode control register. 0: non-DDR mode; 1: DDR mode.
[15:1]	RO	reserved	reserve.
[0]	RW	volt_reg	Voltage Mode Control Register. Bit[1], bit[0] respectively control EMMC, SDIO voltage mode. Take bit0 as an example 0ÿ3.3Vÿ 1ÿ1.8Vÿ

MMC_CARD_RSTN

MMC_CARD_RSTN is the reset control register of EMMC device.

Offset Address	Register Name	Total Reset Value
0x0078	MMC_CARD_RSTN	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	card_reset	The EMMC device reset controller controls the pin CARD_RESET. 0: reset; 1: Cancel reset.

MMC_BMOD

MMC_BMOD is the bus mode register.

Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pbl			of	dsl					fb	swr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:8]	RO	pbl	The length of the IDMAC burst transfer. 000ÿ1ÿ 001ÿ4ÿ 010ÿ8ÿ 011ÿ16ÿ 100ÿ32ÿ 101ÿ64ÿ 110ÿ128ÿ 111ÿ256ÿ
[7]	RW	de	IDMAC is enabled. 0: disable; 1: enable.
[6:2]	RW	dsl	The length of the descriptor span. That is, how many WORDs are separated between two non-linked descriptors. This parameter is only used for double buffer structure descriptors.
[1]	RW	fb	Fixed burst length. 0: Use SINGLE and INCR burst types; 1: Use SINGLE, INCR4, INCR8, INCR16 burst types.
[0]	RW	swr	IDMAC internal register soft reset control. 0: no reset; 1: Reset. It is automatically cleared 1 clock cycle after being set.

MMC_PLDMND

MMC_PLDMND is the Poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	pd
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	pd	If the descriptor DES0[OWN] is 0, the IDMAC will enter the suspend state, and the CPU can write any value to this register to make the IDMAC reacquire the descriptor.

MMC_DBADDR

MMC_DBADDR is the base address register describing the sub-link list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

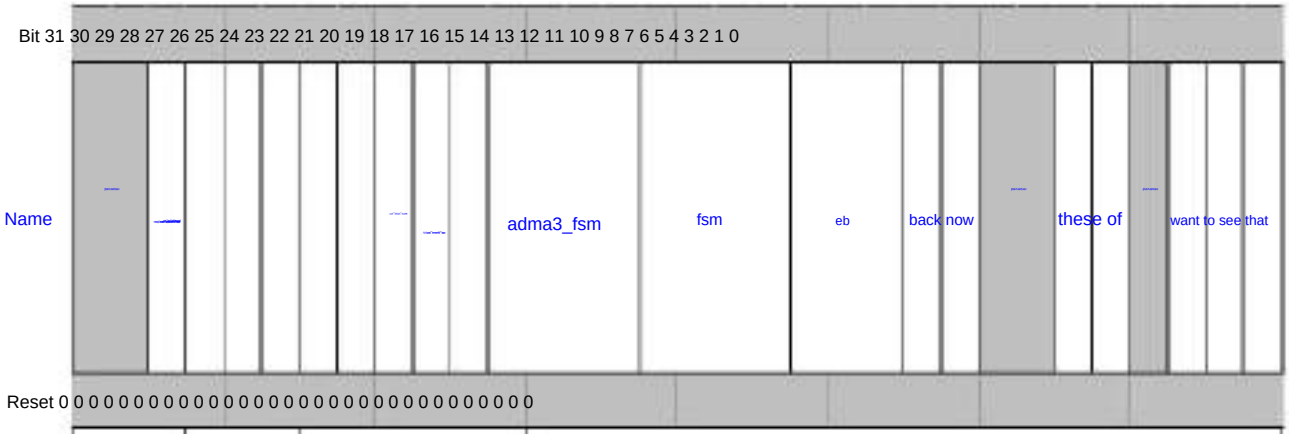
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sdl
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sdl	Describes the starting address of the sub-list. That is, the base address of the first descriptor.

MMC_IDSTS

MMC_IDSTS is the IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RWC	cmd_lock_err	Command Conflict Register. 0: normal; 1: Command conflict.
[28]	RWC	ids_ownbit_err	ownbit error register. 0: ownbit is normal; 1: ownbit error.
[27]	RWC	ids_queue_overflo ln	Queue overflow register. 0: no overflow; 1: Overflow.
[26]	RWC	resp_check_err	resp Error detection register. 0: no error; 1: There is an error.
[25]	RWC	packet_int	Multi-packet interrupt register. 0: no interrupt; 1: Multi-packet interrupt.
interrupt; [24]	RWC	packet_timeout_int	Timeout interrupt register. 0: no 1: Timeout interrupt.
[23]	RWC	auto_stop_err	Hardware stop error detection register. 0: no error; 1: There is an error.

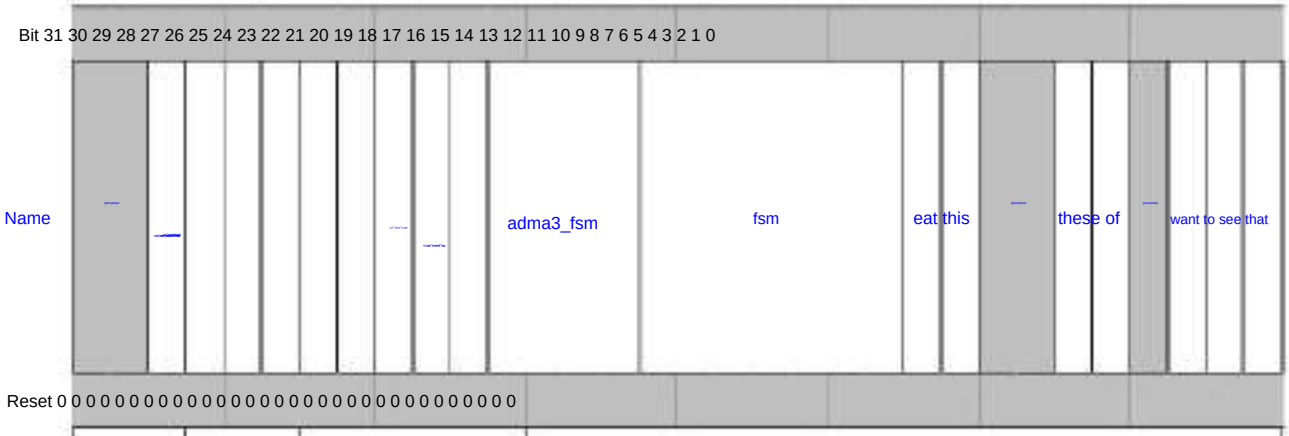
[22] RWC	ids_queue_full		Queue full register. 0: The queue is not full; 1: The queue is full.
[21] RWC	ids_queue_empty		Queue empty register. 0: the queue is not empty; 1: The queue is empty.
[20:17] RO		adma3_fsm	ADMA3 state machine current state. 0x0ÿADMA3_IDLEÿ 0X1ÿADMA3_FIDSÿ 0X2ÿADMA3_SREGÿ 0X3ÿADMA3_CMDÿ 0X4ÿADMA3_TRANSÿ 0X5ÿADMA3_DESC_CLOSEÿ 0X6ÿADMA3_AUTO_STOPÿ 0X7: ADMA3_WAIT; Others: Reserved.
[16:13] RO		fsm	The current state of the IDMAC state machine. 0x0ÿDMA_IDLEÿ 0x1ÿDMA_SUSPENDÿ 0x2ÿDESC_RDÿ 0x3ÿDESC_CHKÿ 0x4ÿDMA_RD_REQ_WAITÿ 0x5ÿDMA_WR_REQ_WAITÿ 0x6ÿDMA_RDÿ 0x7ÿDMA_WRÿ 0x8: DESC_CLOSE; Others: reserved.
[12:10] RW	eb		Indicates the type of bus error. 001: Sending is suspended; 010: Receiving is suspended; Others: Reserved.
[9] RW	ais		Abnormal total interrupt. It is the OR of FBE, DU, and CES. Write 1 to clear 0.
[8] RW	nis		Normal total interruption. It is the OR of TI and RI. Write 1 to clear 0.
[7:6] RO		reserved	reserve.

[5] RW ces			Card error indication. Indicates the status of the card in the process of receiving and sending data. 0: no error indication; 1: There is an error indication
[4] RW you			Descriptor invalid interrupt. This bit is set when DES0[OWN] is 0. Write 1 to clear 0.
[3]	RO	reserved	reserve.
[2] RW fbe			Fatal bus error interrupt. When this bit is set, the IDMAC stops bus access. Write 1 to clear 0.
[1] RW ri			Receive complete interrupt. Indicates that data reception for a descriptor is complete. Write 1 to clear 0. 0: receiving is not completed; 1: Receive complete.
[0] RW ti			Transmit complete interrupt. Indicates that data transmission for a descriptor is complete. Write 1 to clear 0. 0: sending is not completed; 1: Sending is complete.

MMC_IDINTEN

MMC_IDINTEN is the IDMAC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000



Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RW	cmd_lock_err	Command Conflict Register. 0: disable; 1: enable.

[28] RW	ids_ownbit_err		ownbit error register. 0: disable; 1: enable.
[27] RW		ids_queue_overflo ln	Queue overflow register. 0: disable; 1: enable.
[26] RW	resp_check_err		resp Error detection register. 0: disable; 1: enable.
[25] RW	packet_int		Multi-packet interrupt register. 0: disable; 1: enable.
disable; [24] RW	packet_timeout_int		Timeout interrupt register. 0: 1: enable.
[23] RW	auto_stop_err		Hardware stop error detection register. 0: disable; 1: enable.
[22] RW	ids_queue_full		Queue full register. 0: disable; 1: enable.
[21] RW	ids_queue_empty		Queue empty register. 0: disable; 1: enable.
[20:17] RO		adma3_fsm	reserve.
[16:10] RO		fsm	reserve.
[9] RW	ai		Abort enable bit. 0: disable; 1: Enable FBE/DU/CES interrupt.
[8] RWni			Normal interrupt enable bit. 0: disable; 1: Enable TI/RI interrupt.
[7:6] RO		reserved	reserve.

[5] RW ces			Card error interrupt enable bit. 0: disable; 1: enable.
[4] RW you			Descriptor invalid interrupt enable bit. 0: disable; 1: enable.
[3]	RO	reserved	reserve.
[2] RW fbe			Fatal bus error interrupt enable bit. 0: disable; 1: enable.
[1] RW ri			Receive interrupt enable bit. 0: disable; 1: enable.
[0] RW ti			Transmit interrupt enable bit. 0: disable; 1: enable.

MMC_DSCADDR

MMC_DSCADDR is the current description subaddress register.

Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	had																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	had	Descriptor pointer. Automatic updates during data transfer. This register points to the start address of the descriptor currently being used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is the current data buffer address register.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	hba
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	hba	Data buffer pointer. Automatically updated during data transmission, this register points to the data buffer address currently being accessed by IDMAC.

ADMA_CONTROL

ADMA_CONTROL is the adma3 control register

Offset Address	Register Name	Total Reset Value
0x00B0	ADMA_CONTROL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	reserve.
[4]	RW	resp_check_en	resp Error detection function enable register. 0: disable 1: enable
[3]	RW	soft_change_rdptr_ in	Software overrides the logic read pointer function enable register. 0: disable 1: enable
[2]	RW	packet_int_en	Multi-packet interrupt function enable register. 0: disable 1: enable

[1] RW	adma3_restart		adma3 reset register. 0: disable 1: enable
[0] RW	adma3_enable		adma3 enable register. 0: disable; 1: enable.

ADMA_IDS_ADDR

ADMA_IDS_ADDR is the queue start address register

Offset Address	Register Name	Total Reset Value
0x00B4	ADMA_IDS_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ids_start_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ids_start_addr	Synthesis descriptor start address register.

ADMA_DEEPTH

ADMA_DEEPTH is the queue depth register

Offset Address	Register Name	Total Reset Value
0x00B8	ADMA_DEEPTH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ids_deepth
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ids_deepth	Synthesis Descriptor Depth Register.

ADMA_ID_RDPTR

ADMA_ID_RDPTR is the queue read pointer register

Offset Address	Register Name	Total Reset Value
0x00BC	ADMA_ID_RDPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ids_rdptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ids_rdptr	Comprehensive descriptor read pointer.

ADMA_ID_WRPTR

ADMA_ID_WRPTR write pointer register for the queue

Offset Address	Register Name	Total Reset Value
0x00C0	ADMA_ID_WRPTR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ids_wrptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	ids_wrptr	Comprehensive descriptor write pointer.

ADMA_TIMEOUT

ADMA_TIMEOUT is a timeout configuration register

Offset Address	Register Name	Total Reset Value
0x00C4	ADMA_TIMEOUT	0x0000_0000

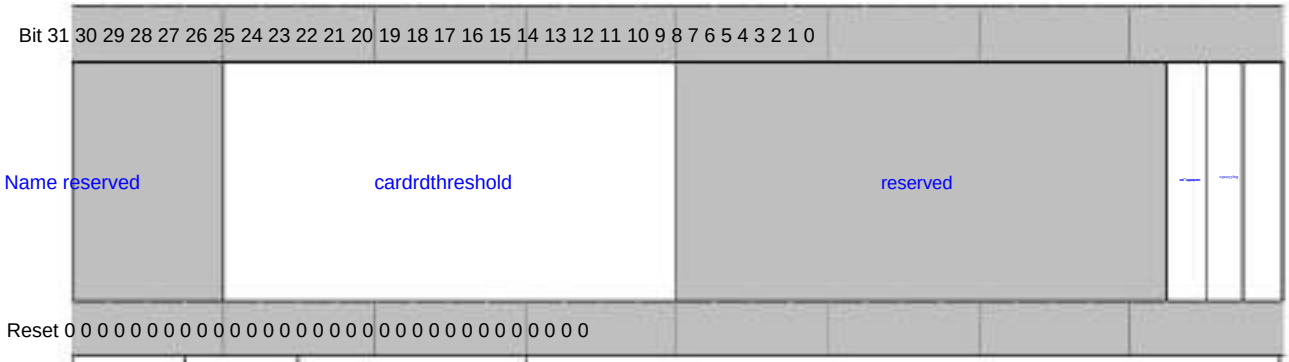
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	timeout_count
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	timeout_count	Multi-packet timeout interrupt timeout count configuration register.

MMC_CARDTHRCTL

MMC_CARDTHRCTL is the threshold control register.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_CARDTHRCTL	0x0000_0000



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27:16]	RW	cardrdthreshold	Read threshold size. The maximum can only be configured to 512.
[15:3]	RO	reserved	reserve.
[2]	RW	cardwrthr_en	Write threshold enable control. 0: disable; 1: enable.
[1]	RW	BsyClrIntEn	Busy Clear Interrupt is enabled. 0: Disable Busy Clear Interrupt; 1: Enable Busy Clear Interrupt.
[0]	RW	cardrdthr_en	Read Threshold Enable Control. 0: Disable; 1: Enable.

MMC_UHS_REG_EXT

MMC_UHS_REG_EXT is the UHS extended register

Offset Address	Register Name	Total Reset Value
0x0108	MMC_UHS_REG_EXT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / ~~~~ / reserved / ~~~~ / reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	reserve.
[25:23]	RW	clk_drv_phase_ctrl	Controls the clock phase of clk_in_drv. 000:0°; 001ÿ45°ÿ 010ÿ90°ÿ 011ÿ135°ÿ 100ÿ180°ÿ 101ÿ225°ÿ 110ÿ270°ÿ 111ÿ315°ÿ
[22:19]	RO	reserved	reserve.
[18:16]	RW	clk_smpl_phase_ctr	Controls the clock phase of clk_in_sample. 000:0°; 001ÿ45°ÿ 010ÿ90°ÿ 011ÿ135°ÿ l 100ÿ180°ÿ 101ÿ225°ÿ 110ÿ270°ÿ 111ÿ315°ÿ
[15:0]	RO	reserved	reserve.

MMC_DDR_REG

MMC_DDR_REG is the EMMC4.5 DDR START bit detection control register.

Offset Address	Register Name	Total Reset Value
0x010C	MMC_DDR_REG	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31] RW	hs400_mode		HS400 mode control register. 0: Non-HS400 mode; 1: HS400 mode.
[30:2] RO		reserved	reserve.
[1] RW	half_start_bit		For EMMC4.5 device, when harf_start_bit is set to 1'b1, when transmitting in DDR mode, RINTSTS[15] interrupt will be set when receiving CMD12.
[0]	RO	reserved	reserve.

MMC_ENABLE_SHIFT

MMC_ENABLE_SHIFT is a phase shift register.

Offset Address	Register Name	Total Reset Value
0x0110	MMC_ENABLE_SHIFT	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:2] RO		reserved	reserve.

[1:0] RW	Enable Shift		Phase shift control register. 00: default phase shift; 01: Phase shift takes effect on the next rising edge; 10: Phase shift takes effect on the next falling edge; 11: Reserved.

MMC_DATA

MMC_DATA is the data register, which is the FIFO entry address. When reading and writing FIFO, the FIFO overflow should be read first.

Offset Address	Register Name	Total Reset Value
0x0200	MMC_DATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	data	Read and write FIFO address. The address range is 0x200~0x200+FIFO_DEPTH, all select FIFO.

12.6 Infrared interface

12.6.1 Overview

The infrared remote control receiving unit IR (Infrared Remoter) receives infrared data through the infrared interface.

12.6.2 Features

The IR module has the following features:

- The software can be configured to close the infrared remote control receiver module. Supports 2 working modes: ÿMode 0: supports decoding of four data formats of NEC with simple repeat code, NEC with full repeat code, SONY and TC9012, and functions such as receiving data error detection and infrared remote control wake-up.
- ÿMode 1: Support symbol level width detection in any data format. In mode 0, it supports received data frame overflow interrupt, received data frame format error interrupt, received data frame interrupt, button release interrupt, and combined interrupts composed of various interrupts. In mode 1, it supports received symbol overflow interrupt, received symbol interrupt, symbol timeout interrupt, and combined interrupts composed of various interrupts.

Supports initial interrupt status query and masked interrupt status query.

Interrupt clear and mask (write clear) are supported.

Support infrared remote control wake-up.

Support reference clock frequency 1MHzÿ128MHz optional, software programmable control frequency division factor to prescale the working clock to 1MHz.

12.6.3 Functional description

When the IR module receives the infrared signal emitted by the infrared remote control, it decodes it and sends it to the ARM system. The ARM system performs corresponding operations according to the received codes to realize the expected functions. The IR module is connected to the APB bus in the ARM subsystem. When the chip is in a low power consumption state (the CPU is in low frequency mode), the IR module will generate an interrupt signal to the CPU after receiving a complete frame of data to realize infrared remote control. Wake up function.

By analyzing the signals sent by various infrared remote controllers, it is found that in the infrared commands sent by different remote controllers, the guide codes are different, and the subsequent control commands are also quite different, even the digits of the command codes are different. , this is because the design of these infrared remote controls does not follow the unified infrared remote control standard. Although the standards followed are different, the basic coding ideas are the same, and pulses with different periods and different duty cycles are used to represent 0 and 1 respectively. The duty cycle of different remote controllers may be different, and the pulse period is also different. According to these differences, some infrared data with similar code types are classified: NEC with simple repeat code data format, NEC with full repeat code data format, TC9012 data format and SONY data format.

Table 12-23 to Table 12-25 show the statistics of infrared received data code patterns .

说明

This statistical table is based on the actual measurement of the chip. The data on the table are only previous measurement values and are not completely correct.

Table 12-23 Statistical Table of Infrared Received Data Patterns (NEC with simple repeat code)

Data Format		NEC with simple repeat code			
		uPD6121G D6121/BU5777/D1913 LC7461M-C13 AEHA			
Lead Code (10µs) LEAD_S		900	900	900	337.6
	LEAD_E	450	450	450	168.8
bit0ÿ10µsÿ	B0_L	56	56	56	42.2
	B0_FUL	56	56	56	42.2
bit1ÿ10µsÿ	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
simple repeat code ÿ10µsÿ	SLEAD_S 900		900	900	337.6
	SLEAD_E 225		225	225	337.6
burstÿ10µsÿ		55	55	55	42.2
Frame length (10µs)		10800	10800	10800	8777.6ÿ 12828.8

Data Format	NEC with simple repeat code			
	uPD6121G D6121/BU5777/D1913 LC7461M-C13 AEHA			
valid data bits	32	32	42	48

Table 12-24 Statistical Table of Infrared Received Data Patterns (NEC with full repeat code)

Data Format		NEC with full repeat code						
		uPD6121G LC7461	M-C13	MN602 4-C5D6	MN6014 -C6D6	MATNEW MN6030 LORD		SONIC
boot code ÿ10µsÿ	LEAD_S 900		900	337.6	349.2	348.8	349	352
	LEAD_E 450		450	337.6	349.2	374.4	349	352
bit0 ÿ10µsÿ	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_FUL	56	56	84.4	87.3	43.6	87.3	88
bit1 ÿ10µsÿ	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
simple repeat code ÿ10µsÿ	SLEAD_S None		none	none	none	none	none	none
	SLEAD_E							
burstÿ10µsÿ		55	55	84.4	87.3	43.6	87.3	88
Frame length (10µs)		10800	10800	10130	10470	12413.6ÿ 16594.4	10500	10400
valid data bits		32	42	22	24	48	22	22

Table 12-25 Statistical table of infrared receiving data code types (TC9012 and SONY codes)

Data Format		TC9012	SONY			
		TC9012F/9243 SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13	
boot code ÿ10µsÿ	LEAD_S 450		240	240	240	240
	LEAD_E 450		60	60	60	60
bit0 ÿ10µsÿ	B0_L	56	60	60	60	60
	B0_FUL	56	60	60	60	60
bit1 ÿ10µsÿ	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
simple repeat code ÿ10µsÿ	SLEAD_S None		none	none	none	none
	SLEAD_E					
burstÿ10µsÿ		56	none	none	none	none
Frame length (10µs)		10800	4500	4500	4500	4500
valid data bits		32	12	13	15	20

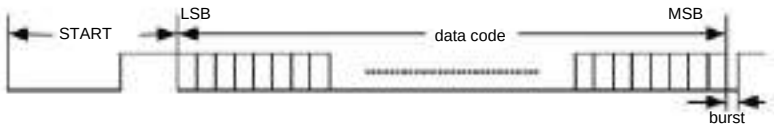
12.6.3.1 NEC with simple repeat code data format

frame format

The data format of NEC with simple repeat code is composed of three parts: START (boot code), data code and burst, among which START is composed of a start code (low level) and an end code (high level); The effective number of digits and the meaning of a certain bit depend on the specific code pattern, which is received in the order of LSB first; the burst signal is used to receive the last data code bit.

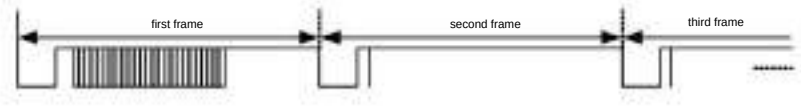
The frame format for sending a single NEC with simple repeat code is shown in Figure 12-32 .

Figure 12-32 Frame format for sending a single NEC with simple repeat code



If the key press lasts longer than one frame, after receiving the complete data frame, the next received data frame only consists of simplified preamble code and burst signal. The boot code is also composed of a start code (low level) and an end code (high level). The frame format of continuously sending the NEC with simple repeat code code is shown in Figure 12-33 .

Figure 12-33 The frame format of continuously sending NEC with simple repeat code by pressing the button continuously



code format

The definition of bit0 or bit1 of NEC with simple repeat code is shown in Figure 12-34 .

Figure 12-34 Definition of bit0 and bit1 of NEC with simple repeat code

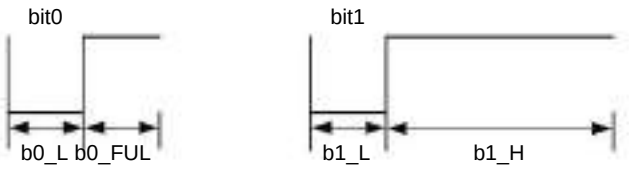


Figure 12-35 and Figure 12-36 show the NEC simple repeat code single-issue code format and continuous-issue code format respectively .

Figure 12-35 NEC with simple repeat code single-issue code format

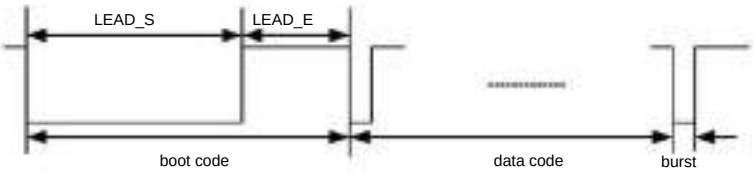
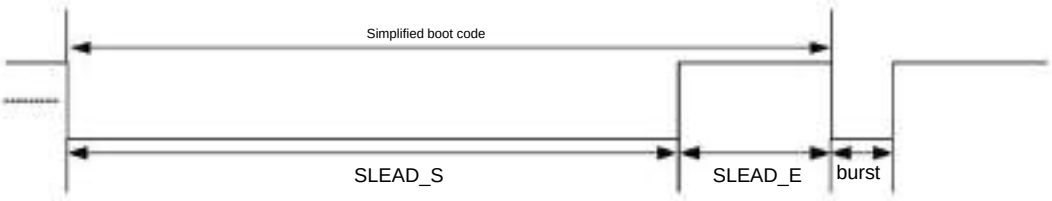


Figure 12-36 NEC with simple repeat code code format



Note 1: The width of the high and low level pulse width and the frame length in the figure are determined by each specific pattern, please refer to Table 12-23~Table 12-25. Note

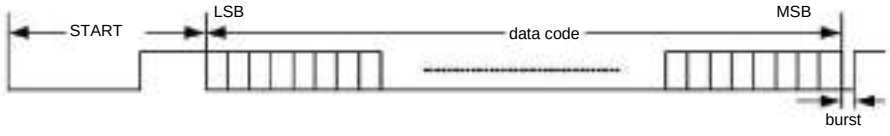
2: The frame length cannot be greater than 160ms, otherwise the simplified boot code cannot be recognized.

12.6.3.2 NEC with full repeat code data format

frame format

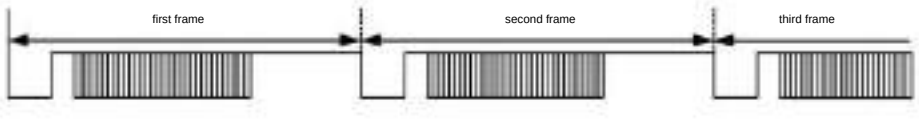
The data format of NEC with full repeat code is composed of three parts: START (boot code), data code and burst. START is composed of a start code (low level) and an end code (high level); the effective number of digits of the data code and the meaning of a certain bit are determined by the specific code pattern, which is in the order of LSB first Received; the burst signal is used to receive the last data bit. The frame format for sending a single NEC with full repeat code is shown in Figure 12-37 .

Figure 12-37 Frame format for sending a single NEC with full repeat code



If the key press lasts for more than one frame, after receiving the complete data frame (the first frame), the next received data frame is still a complete data frame format (that is, the first frame of data is sent repeatedly according to the frame interval) , keep pressing the key to continuously send the NEC with full repeat code frame format as shown in Figure 12-38 .

Figure 12-38 The frame format of continuously sending NEC with full repeat code by pressing the button continuously

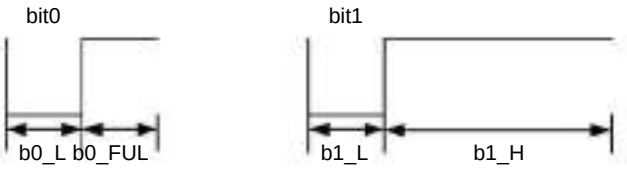


From Figure 12-37 and Figure 12-38, it can be seen that the only difference between NEC with simple repeat code and NEC with full repeat code is the format of the repeated frame. NEC with simple repeat code sends a simplified boot code, while NEC With full repeat code sends the full frame format, the first frame is exactly the same as the repeated frame.

code format

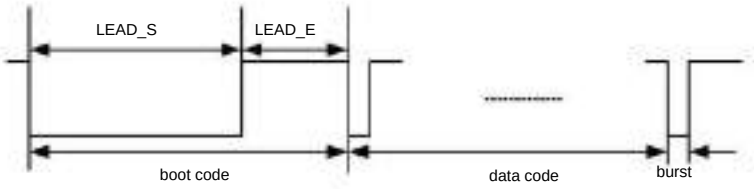
The definition of bit0 or bit1 of NEC with full repeat code is shown in Figure 12-39 .

Figure 12-39 Definition of bit0 and bit1 of NEC with full repeat code



The single-issue code format of NEC with full repeat code is shown in Figure 12-40 .

Figure 12-40 NEC with full repeat code single-issue code format



Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern, please refer to Table 12-23~Table 12-25.

12.6.3.3 TC9012 Data Format

frame format

注意

According to the data format characteristics of the TC9012 code, the first digits of all key codes must be all 1 or all 0, otherwise

Unnecessary continuous key frames will be generated.

The data format of TC9012 is composed of three parts: START (boot code), data code and burst, among which START is composed of a start code (low level) and an end code (high level); the effective number of data codes And the meaning of a certain bit depends on the specific code pattern, which is received in the order of LSB first; the burst signal is used to receive the last data code bit. The frame format for sending a single TC9012 code is shown in Figure 12-41 .

Figure 12-41 Frame format for sending a single TC9012 code

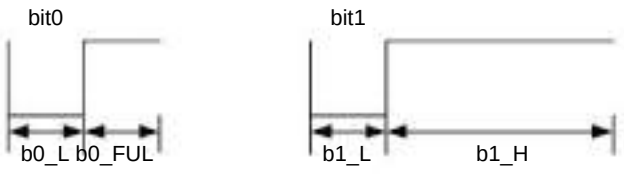
If the pressing time lasts longer than one frame, after receiving the complete data frame, the next received data frame consists of three parts: the pilot code, a data bit and the burst signal. The leading code is also composed of a start code (low level) and an end code (high level); this data bit is the inverse code of the first data bit (C0) received in the previous frame. The frame format for sending continuous TC9012 codes is shown in Figure 12-42 .

Figure 12-42 The frame format of continuously sending TC9012 codes by continuously pressing the key

code format

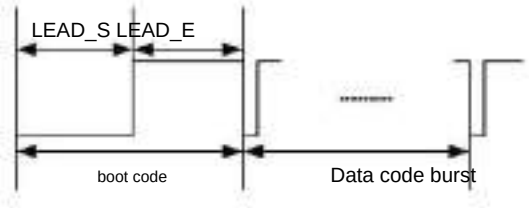
The definition of TC9012 code bit0 or bit1 is shown in Figure 12-43 .

Figure 12-43 Definition of bit0 and bit1 of TC9012 code



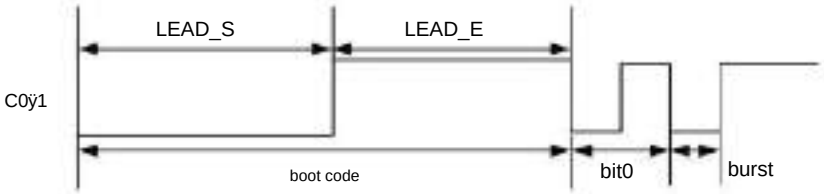
The single-issue code format of TC9012 code is shown in Figure 12-44 .

Figure 12-44 TC9012 single-issue code format



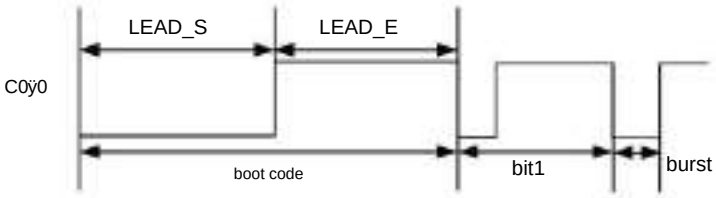
When C0=1, the code format of TC9012 code burst is shown in Figure 12-45 .

Figure 12-45 TC9012 code format for continuous sending (C0ÿ1)



When C0=0, the TC9012 code burst code format is shown in Figure 12-46 .

Figure 12-46 TC9012 code format for continuous sending (C0ÿ0)



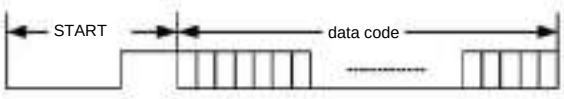
Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern. See Table 12-23 to Table 12-25. It is also worth noting that the frame length cannot be greater than 160ms, otherwise repeated frames cannot be identified.

12.6.3.4 SONY data format

frame format

The SONY code data format is composed of two parts: START (boot code) and data code. Among them, START is composed of a start code (low level) and an end code (high level); the effective number of digits of the data code and the meaning of a certain bit are determined by the specific code pattern, which is in the order of LSB first Received. The frame format for sending a single SONY code is shown in Figure 12-47 .

Figure 12-47 Send a single SONY frame format



If the pressing time lasts longer than one frame, after receiving the complete data frame, the next received data frame is still in a complete data frame format.

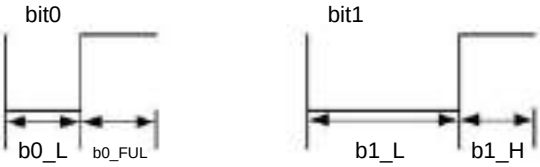
Press and hold the key to continuously send the SONY code frame format as shown in Figure 12-48 .

Figure 12-48 Continuously send SONY code frame format by pressing the key

code format

The definition of bit0 or bit1 of SONY code is shown in Figure 12-49 .

Figure 12-49 Definition of bit0 and bit1



Note: The pulse width and frame length of the high and low levels in the figure are determined by each specific code pattern. See Table 12-23 to Table 12-25.

12.6.4 Working method

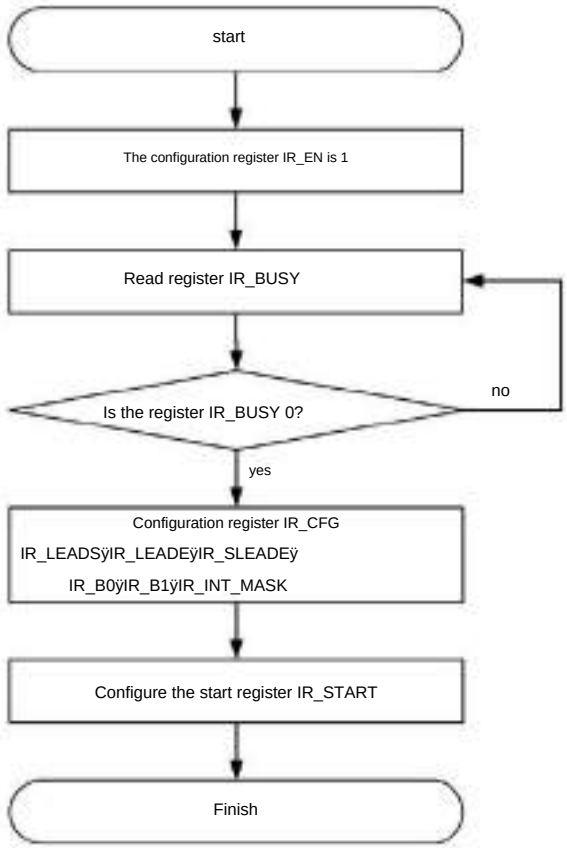
soft reset

Configure the CRG register PERI_CRG57[ir_srst_req] as 1, and soft reset the IR module separately. After reset, the values of each configuration register are reset to default values, so these registers need to be initialized and configured again after reset.

Register Configuration Example

Figure 12-50 shows the operation flow of IR module initialization .

Figure 12-50 IR module initialization operation flow



The IR module initialization operation flow is as follows:

Step 1. Select the address space of the IR module and start the IR initialization configuration operation.

Step 2. Set IR_EN bit[0] to 1 to enable the IR receiving module.

Step 3. Read IR_BUSY to determine the current status of the IR module configuration.

If the read value is 1, it means that the IR module is in the configuration busy state, then continue to query IR_BUSY (note: the software should not configure other control registers of the IR module at this time , otherwise the configuration will be

invalid). If the read value is 0, it indicates that the IR module is in the configuration idle state, then go to step 4.

Step 4. ConfigurationIR_CFG ÿIR_LEADSÿIR_LEADEÿIR_SLEADEÿIR_B0ÿIR_B1ÿ

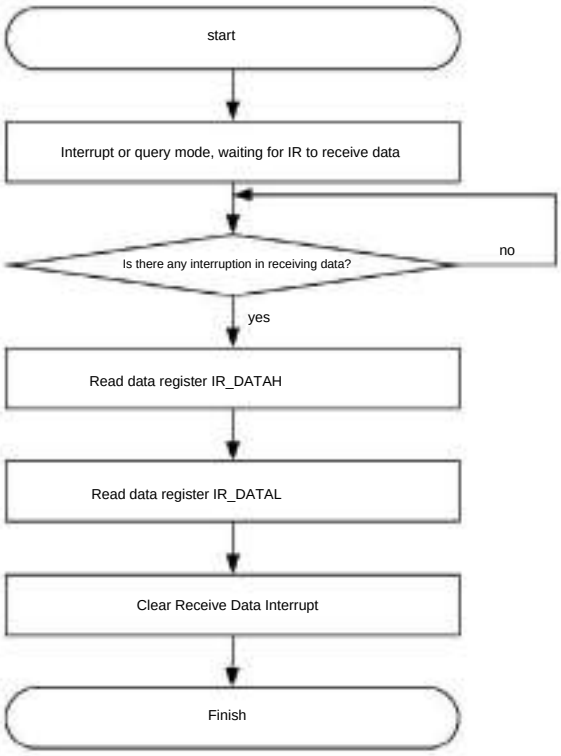
IR_INT_MASK. Note: Users can update the corresponding registers as needed, if not, the registers will keep the original value.

Step 5. Configure IR_START. You must wait for all the IR control registers to be configured before configuring

IR_START, because it is used to generate a start signal, as long as it is configured, the IR module will receive infrared data according to the value of the control register.

----Finish

Figure 12-51 Operation flow of reading decoded data



The operation flow of reading decoded data is as follows:

Step 1. Select the IR module address space.

Step 2. Wait for receiving data frames in interrupt or query mode.

In the interrupt mode, when the CPU receives the interrupt request signal from the IR module, query the value of IR_INT_STATUS[intms_rcv]. If the read value is 1, it means that the IR module has received a data frame, go to step 3; if the read value is 0, go to step 2 again and continue to wait for the interrupt.

In the query mode, the software reads the value of IR_INT_STATUS[intrs_rcv] continuously (or at regular intervals) . If the read value is 1, it means that the IR module has received a data frame, and then perform step 3; if the read value is 0 , it indicates that the IR module has not received the data frame, and re-execute step 2 to continue the query.

Step 3. Read the data register IR_DATAH. (If the number of data bits in a frame is not greater than 32 bits, this step can be omitted step)

Step 4. Read the data register IR_DATAL.

Step 5. Clear the receive data interrupt.

----Finish

12.6.5 IR register overview

An overview of the IR registers is shown in Table 12-26 .

Table 12-26 IR register overview (base address is 0x120F_0000)

offset address	name	describe	page number
0x000	GO	IR Receive Enable Control Register	12-137
0x004	IR_CFG	IR configuration register	12-138
0x008	IR_LEADS	Boot code start bit margin configuration register (only in IR_CFG [ir_mode]=0)	12-140
0x00C	IR_LEADE	Boot code end bit margin configuration register (only in IR_CFG [ir_mode]=0)	12-141
0x010	IR_SLEADE	Simplified boot code end bit margin configuration register (only in IR_CFG [ir_mode]=0)	12-142
0x014	IR_B0	Judgment level margin configuration register for data 0 (only in IR_CFG [ir_mode]=0)	12-143
0x018	IR_B1	Judgment level margin configuration register for data 1 (only in IR_CFG [ir_mode]=0)	12-144
0x01C	AND_BUSY	Configure Busy Flag Register	12-145
0x020	IR_DATAH	IR Receives high 16-bit register of decoded data (when IR_CFG[ir_mode]=0) or symbol number register in symbol FIFO (when When IR_CFG[ir_mode]=1)	12-146
0x024	IR_DATAL	IR Receives the low 32-bit register of decoded data (when IR_CFG[ir_mode]=0) or the symbol width register received by the IR module (when When IR_CFG[ir_mode]=1)	12-146
0x028	IR_INT_MASK	IR interrupt mask register	12-147
0x02C	IR_INT_STATUS	IR interruot status register	12-149
0x030	IR_INT_CLR	IR Interrupt Clear Register	12-151
0x034	IS_START	IR Boot Configuration Register	12-153

12.6.6 IR Register Description

GO

IR_EN is the IR receive enable control register.

注意

The software must configure the register IR_EN[ir_en]=1 before configuring other registers, otherwise the configuration is invalid.

When the register IR_EN[ir_en]=0, other registers can only be read but not written, and the read value is the reset value of the register.

Offset Address	Register Name	Total Reset Value
0x000	GO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	go
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	go_in	Enable of the IR receiver module. 0: Turn off the IR receiving module; 1: Turn on the IR receiving module.

IR_CFG

IR_CFG is the IR configuration register.

注意

This register must be configured when IR_BUSY[ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value.

The reference clock frequency supported by IR is 1MHz~128MHz, and its corresponding relationship with the frequency division factor ir_freq is:

When the reference clock frequency is 1MHz, the frequency division factor ir_freq needs to be configured as 0x00. When the reference clock frequency is 128MHz, the frequency division factor ir_freq needs to be configured as 0x7F.

When the IR reference clock is a non-integer multiple frequency within 1MHz ~ 128MHz, choose the corresponding frequency division factor by rounding off. Example: The reference clock is 12.1MHz, and the selected frequency division factor is 0x0B; the reference clock is 12.8MHz, the selected frequency division factor is 0x0C.

For the relationship between frequency offset and counting deviation: base frequency f, frequency change Df, then frequency deviation rate ratio=Df/f; counter counting deviation Dcnt; judgment level width s (unit: ÿs), then counting deviation: Dcnt = ÿ ÿ 0when the reference clock frequency offset, the effective range of the parameter value must be shifted. If the frequency increases, the corresponding margin value

Should be changed to: [min+Dcnt, max+Dcnt], where min and max are margin values without offset; if the frequency drops, the corresponding margin value should be changed to: [min-Dcnt, max-Dcnt] . Take the start bit margin of the pilot code as an example: If the base frequency is 100MHz, and the frequency drifts up by 0.1MHz, then ratio=0.1/100=0.001, and s=9000ÿs, then

Dcnt = ÿ ÿ 0.1×9000×0.001=1, the margin value of ir_leads should be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14	13 12 11 10 9 8	7 6	5 4 3 2 1 0
Name	ir_max_level_width	is_format	ir_bits	is_fashion	ir_freq
Reset	0 0 1 1 1 1 1 0 1 0 0 0 0 0 0 0	0 0	0 1 1 1 1 1	0 0	0 0 1 0 1 1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	When IR_CFG [ir_mode]=0, it is invalid; When IR_CFG [ir_mode]=1, it indicates the maximum level width of symbol (unit 10ÿs), which is used to determine the end of a symbol stream.
[15:14]	RW	ir_format	When IR_CFG [ir_mode]=0, it means data pattern. 00: NEC with simple repeat code data format; 01: TC9012 data format; 10: NEC with full repeat code data format; 11: SONY data format. Please refer to Table 12-23 to Table 12-25 for the code family to which the specific code pattern belongs . When IR_CFG [ir_mode]=1, it means symbol format. bit[15]: Reserved; the meaning of bit[14] is as follows: 0: The format of the symbol is low before high, and the symbol stream ends at high level; 1: The format of the symbol is high before low, and the symbol stream ends at low level.
[13:8]	RW	ir_bits	When IR_CFG [ir_mode]=0, it means the number of data bits in one frame. 0x00ÿ0x2F: corresponding to 1ÿ48 data bits in a frame; 0x30ÿ 0x3F: reserved. If the software configures this field with a value in the range of 0x30~0x3F, the configuration will be invalid, and the original value of ir_bits will remain unchanged. When IR_CFG [ir_mode]=1, it means receiving symbol interrupt watermark. bit[13]: Reserved; bit[12:8]: 0x0~0x1F: corresponding to at least 1~32 symbols in the FIFO reporting interrupt.

[7] RW ir_mode			IR working mode. 0: Output the complete data frame after decoding; 1: Only output the symbol width.
[6:0] RW ir_freq			Working clock frequency division factor. 0x00~0x7F correspond to the working clock frequency division factor 1~128 respectively.

IR_LEADS

IR_LEADS is the boot code start bit margin configuration register (only used when Table 12-23~Table 12-25 [ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN[ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

In order to accurately determine the start bit of the leading code, a certain margin needs to be considered around the typical value of the specific code type. For the typical value of the specific code type, please refer to the value of LEAD_S in Table 12-23 to Table 12-25 .

For pulse widths with a typical value not less than 400 (its accuracy is 10ÿs), it is recommended that the margin range be set to 8% of the typical value. For example: D6121 pattern, the typical value of LEAD_S is 900, then the corresponding cnt_leads_min=900 x 92%=828=0x33C, cnt_leads_max=900 x 108%=972=0x3CC. For pulse widths with a typical value less than 400 (with an accuracy of 10 ÿs), it is recommended that the margin range be set to 20% of the typical value. For example: SONY-D7C5 pattern, its typical value of LEAD_S is 240, then the corresponding cnt_leads_min=240 x 80%=192=0xC0, cnt_leads_max=240 x 120%=288=0x120.

Basic configuration principle: cnt_leads_max is not less than cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt_leads_min	reserved	cnt_leads_max
Reset	0 0 0 0 0 0 1 1	0 0 1 1	1 1 1 0	0 0 1 1

Bits	Access Name		Description
[31:26] RO		reserved	reserve.
[25:16] RW	cnt_leads_min		The minimum pulse width of the start bit of the boot code. 0x000~0x007: Reserved.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved	cnt_leads_min	reserved	cnt_leads_max
Reset	0 0 0 0 0 0 1 1 0 0 1	1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 0 0 1		1 0 0

Bits	Access Name		Description
[15:10]	RO	reserved	reserve.
[9:0]	RW cnt_leads_max		The maximum pulse width of the start bit of the boot code. 0x000~0x007: Reserved.

IR_LEADE

IR_LEADE is the boot code end bit margin configuration register (only used when IR_CFG [ir_mode]=0).

注意

This register can only be configured when IR_BUSY [ir_busy] =0 and IR_EN [ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

For the code family of NEC with simple repeat code, the margin range of cnt_sleade and the margin range setting of cnt_leade cannot overlap. Otherwise, when the actual count value falls within the coincident range, the simplified guide code cannot be recognized, which will cause a frame format error.

In order to accurately judge the end bit of the pilot code, it is necessary to consider a certain margin around the typical value of the specific code pattern, and the margin range is about 8% of the typical value. For typical values of specific code types, see the values of LEAD_E in Table 12-23 to Table 12-25 .

For a pulse width with a typical value not less than 400 (its accuracy is 10ÿs), it is recommended that the margin range be set at 8% of the typical value. For example: D6121 pattern, the typical value of LEAD_E is 450, then the corresponding cnt_leade_min=450 x 92%=414=0x19E, cnt_leade_max=450 x 108%=486=0x1E6. For pulse widths with a typical value less than 400 (with an accuracy of 10 ÿs), it is recommended that the margin range be set to 20% of the typical value. For example: SONY-D7C5 pattern, its typical value of LEAD_E is 60, then the corresponding cnt_leade_min=60 x 80%=48=0x030, cnt_leade_max=60 x 120%=72=0x048.

The basic configuration principle is: cnt_leade_max is not less than the value of cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt_leade_min	reserved	cnt_leade_max
Reset	0 0 0 0 0 0 0 1	1 0 0 1 1 1 0 0	1 0 0 0 0 0 0 0	1 0

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:16]	RW	cnt_leade_min	The minimum pulse width of the boot code end bit. 0x000~0x007: Reserved.
[15:9]	RO	reserved	reserve.
[8:0]	RW	cnt_leade_max	The maximum pulse width of the end bit of the boot code. 0x000~0x007: Reserved.

AND_SLEADE

IR_SLEADE is the configuration register for the end bit margin of the simplified boot code (only used when IR_CFG [ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN [ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

For the code family of NEC with simple repeat code, the margin range of cnt_sleade and the margin range setting of cnt_leade cannot overlap, otherwise when the actual count value falls within the coincident range, the simplified guide code cannot be recognized and the frame format error will result.

For the data format of NEC with simple repeat code, this register needs to be configured; for other formats, this register does not need to be configured.

In order to accurately judge the end bit of the simplified pilot code, it is necessary to consider a certain margin around the typical value of the specific code pattern. For typical values of specific code types, see the values of SLEAD_E in Table 12-23 to Table 12-25 .

For pulse widths with a typical value not less than 225 (its accuracy is 10μs), it is recommended to set the margin range to 8% of the typical value. For example: D6121 pattern, the typical value of SLEAD_E is 225, then the corresponding cnt_sleade_min=225 x 92%=207=0xCF, cnt_sleade_max=225 x 108%=243=0xF3.

For pulse widths typically less than 225 (with an accuracy of 10μs), it is recommended that the margin range be set to 20% of the typical value. For example: For example, the typical value of SLEAD_E of a code pattern is 60, then the corresponding cnt_sleade_min=60 x 80%=48=0x30, cnt_sleade_max=60 x 120%=72=0x48.

The basic configuration principle is: cnt_sleade_max is not less than the value of cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	AND_SLEADE	0x00CF_00F3

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Name	reserved	cnt_sleade_min	reserved	cnt_sleade_max
Reset	0 0 0 0 0 0 0 0	1 0 0 1 1	1	1 0 0 0 0 0 0 0 0 1 1 1 1 0 0 1

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:16]	RW	cnt_sleade_min	The minimum pulse width of the end bit of simplified preamble code. 0x000~0x007: Reserved.
[15:9]	RO	reserved	reserve.
[8:0]	RW	cnt_sleade_max	Simplifies the maximum pulse width of the start bit of the preamble. 0x000~0x007: Reserved.

IR_B0

IR_B0 is the judgment level margin configuration register for data 0 (only used when IR_CFG [ir_mode]=0).

注意

This register must be configured when IR_BUSY [ir_busy]=0 and IR_EN [ir_en]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the reserved value configuration of the register is invalid and the original value remains unchanged.

For the four code types, the bit0 judgment level margin range and the bit1 judgment level range setting cannot overlap, otherwise when the actual count value falls within the overlapping range, bit1 cannot be recognized and bit0 can only be misunderstood.

In order to accurately judge bit0, it is necessary to consider a certain margin around the typical value of the specific pattern, and the margin range is about 20% of the typical value.

For the three code types of NEC with simple repeat code, NEC with full repeat code and TC9012, please refer to the value of B0_H in Table 12-23 to Table 12-25 for the typical values of the specific code types included. For example: D6121 pattern, the typical value of B0_H is 56 (its precision is 10μs), then the corresponding cnt0_b_min=56 x 80%=45=0x2D, cnt0_b_max=56 x 120%=67=0x43.

For the SONY data format, please refer to the value of B0_L in Table 12-23~Table 12-25 for the typical value of the specific code pattern it contains. For example: SONY-D7C5 pattern, the typical value of B0_L is 60 (its precision is 10μs), then the corresponding cnt0_b_min=60 x 80%ÿ48ÿ0x30, cnt0_b_max=60 x 120%=72=0x48ÿ

The basic configuration principle is: cnt0_b_max is not less than the value of cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt0_b_min								reserved						cnt0_b_max		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:16]	RW	cnt0_b_min	bit0 determines the minimum pulse width of the level. 0x000~0x007: Reserved.
[15:9]	RO	reserved	reserve.
[8:0]	RW	cnt0_b_max	bit0 judges the maximum pulse width of the level. 0x000~0x007: Reserved.

IR_B1

IR_B1 is the judgment level margin configuration register for data 1 (only used when IR_CFG [ir_mode]=0).

注意

This register must be configured when IR_BUSY [0]=0 and IR_EN [0]=1, otherwise the configuration is invalid and the register keeps the original value; in addition, the configuration of the reserved value of the register is invalid and the original value remains unchanged.

For the four code types, the bit0 judgment level margin range and the bit1 judgment level range setting cannot overlap, otherwise when the actual count value falls within the overlapping range, bit1 cannot be recognized and bit0 can only be misunderstood.

In order to accurately judge bit1, a certain margin needs to be considered around the typical value of the specific pattern, and the margin range is about 20% of the typical value.

For the code families of NEC with simple repeat code, NEC with full repeat code and TC9012, please refer to the value of B1_H in Table 12-23 to Table 12-25 for the typical values of the specific code types included. For example: D6121 pattern, the typical value of B1_H is 169 (its precision is 10μs), then the corresponding cnt1_b_min=169 x 80%=135=0x87, cnt1_b_max=169 x 120%=203=0xCB.

For the SONY data format, please refer to the value of B1_L in Table 12-23 to Table 12-25 for the typical value of the specific code pattern it contains. For example: SONY-D7C5 pattern, the typical value of B1_L is 120 (its precision is 10μs), then the corresponding cnt1_b_min=120 x 80%=96=0x60, cnt1_b_max=120 x 120%=144=0x90ÿ

The basic configuration principle is: cnt1_b_max is not less than the value of cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	reserved	cnt1_b_min	reserved	cnt1_b_max
Reset	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 1 0 0 1 0 1 1	

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:16]	RW	cnt1_b_min	bit1 The minimum pulse width for judging the level. 0x000~0x007: Reserved.
[15:9]	RO	reserved	reserve.
[8:0]	RW	cnt1_b_max	Bit1 judges the maximum pulse width of the level. 0x000~0x007: Reserved.

AND_BUSY

IR_BUSY is the configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	AND_BUSY	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RO	and_busy	Busy flag. 0: idle state, software can configure data; 1: In busy state, the software cannot configure data.

IR_DATAH

IR_DATAH is the upper 16-bit register of IR receiving and decoding data (when IR_CFG [ir_mode]=0) or the symbol number register in symbol FIFO (when IR_CFG [ir_mode]=1).

IR_DATAH is the upper 16 bits of the received decoded data , and IR_DATAL is the lower 32 bits of the received decoded data. Which data bits are valid depends on the number of valid data bits contained in one frame of the specific pattern, please refer to the valid data bits in Table 12-23 to Table 12-25 .

Data storage principle: store in IR_DATAH and IR_DATAL in order from high to low (MSB... LSB), store IR_DATAL first, and then store IR_DATAH, the unused high bits are reserved bits. The order in which the software reads data must be: first read IR_DATAH, then read IR_DATAL.

For the specific meaning of each data bit, the hardware does not make judgments, but is only responsible for receiving all the data bits, and finally the software handles it uniformly.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	is_datah
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	is_datah	When IR_CFG [ir_mode]=0, it means the upper 16 bits of the received decoded data. When IR_CFG [ir_mode]=1, it means the number of symbols in symbol FIFO. bit[15:6]: reserved; bit[5:0]: the number of symbols in the symbol FIFO.

IR_DATAL

IR_DATAL is the low 32-bit register of the decoded data received by IR (when IR_CFG [ir_mode]=0) or the symbol width register received by the IR module (when IR_CFG [ir_mode]=1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	ir_data	When IR_CFG [ir_mode]=0, it means the low 32 bits of received decoded data. When IR_CFG [ir_mode]=1, it indicates the symbol width received by the IR module. The meaning of bit[31:16] is as follows: When the format of the symbol is low first and then high, it indicates the high level width of the received symbol (the unit is 10ÿs); When the format of the symbol is high first and then low, it indicates the low level width of the received symbol (the unit is 10ÿs). The meaning of bit[15:0] is as follows: When the format of symbol is first low and then high, it indicates the low level width of the received symbol (unit is 10ÿs); When the format of the symbol is high first and then low, it indicates the high level width of the received symbol (the unit is 10ÿs).

IR_INT_MASK

IR_INT_MASK is the IR interrupt mask register.

注意

This register can only be configured when IR_EN [ir_en]=1 is ensured , otherwise the configuration is invalid and the register keeps the original value.

If all interrupts are shielded, the infrared remote control wake-up function cannot be supported.

When IR_CFG [ir_mode]=0, IR_INT_MASK bit[3:0] is valid; when IR_CFG [ir_mode]=1, IR_INT_MASK bit[18:16] is valid.

The interrupts involved are defined as follows:

Receive data overflow interrupt

If the CPU does not respond in time to take away the data of the current frame and the data of the next frame has been received, the data of the next frame will overwrite the data of the current frame, and at the same time, an interrupt request for receiving data overflow error before masking will be reported.

Receive data frame format error interrupt

If the received data frame is incomplete and the data pulse width does not meet the margin range, the received frame format error interrupt request before masking will

be reported. Received data

frame interrupt When a complete frame data is received, it will report a data frame interrupt request received before masking.

Support the detection interrupt of key

release For the data format of NEC with simple repeat code and TC9012 code family, within 160ms after detecting a valid start synchronization code, if the start synchronization code is not detected again, or a non-simplified boot is detected When the code is a valid data frame, it will report the remote control key release interrupt before shielding.

For NEC with full repeat code and SONY two code systems do not support key release

interrupt. Receive symbol

overflow interrupt If the CPU does not respond in time to take away the data, resulting in the symbol FIFO being full, but the next symbol has been received, it will report a received symbol

overflow error interrupt

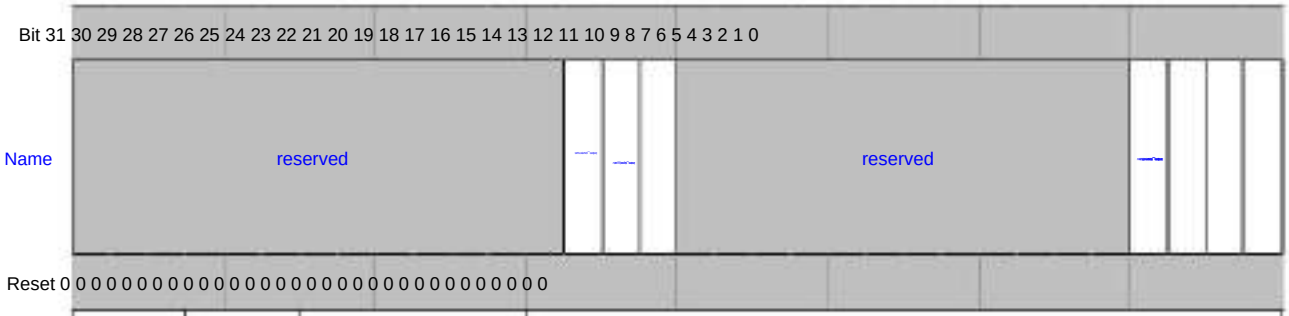
request before masking. When a symbol interrupt is received and a complete symbol is received, and the number of symbols in the symbol FIFO exceeds the waterline set by IR_CFG [ir_bits], a symbol

interrupt request

received before masking will be reported. After the symbol timeout interrupt receives a valid symbol , if no new symbol interrupt request is received within the time set by IR_CFG [ir_max_level_width], the symbol timeout interrupt request before masking will be

The hardware does not have interrupt priority arbitration, and any one or more masked interrupt sources are valid, and an interrupt will be generated.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000



Bits	Access Name		Description
[31:19] RO		reserved	reserve.
[18] RW intm_overrun			When IR_CFG [ir_mode]=1, symbol overflow interrupt mask. 0: no shielding; 1: Shielded.

[17] RW	intm_time_out		When IR_CFG [ir_mode]=1, symbol timeout interrupt mask. 0: no shielding; 1: Shielded.
[16] RW	intm_symb_rcv		When IR_CFG [ir_mode]=1, receive N symbol interrupt mask. 0: no shielding; 1: Shielded.
[15:4] RO		reserved	reserve.
[3] RW	intm_release		When IR_CFG [ir_mode]=0, key release interrupt mask. 0: no shielding; 1: Shielded.
[2] RW	intm_overflow		When IR_CFG [ir_mode]=0, receive data overflow interrupt mask. 0: no shielding; 1: Shielded.
[1] RW	intm_frame		When IR_CFG [ir_mode]=0, receive data frame format error interrupt mask. 0: no shielding; 1: Shielded.
[0] RW	intm_rcv		When IR_CFG [ir_mode]=0, received data frame interrupt mask. 0: no shielding; 1: Shielded.

IR_INT_STATUS

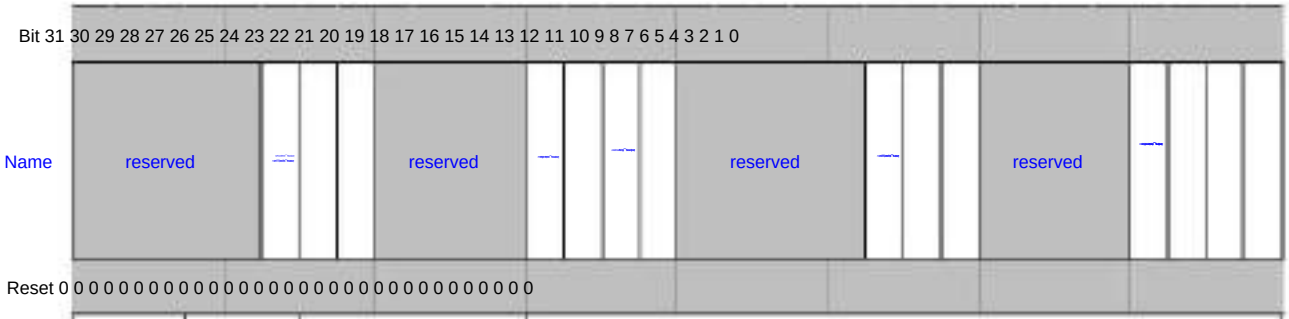
IR_INT_STATUS is the IR interrupt status register.

注意

When IR_CFG [ir_mode]=0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid;

When IR_CFG [ir_mode]=1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] have effect.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000



Bits	Access	Name	Description
[31:27]	RO	reserved	reserve.
[26]	RO	intms_overrun	When IR_CFG [ir_mode]=1, masked symbol overflow interrupt status. 0: no interrupt; 1: There is an interrupt.
[25]	RO	intms_time_out	When IR_CFG [ir_mode]=1, the masked symbol timeout interrupt status. 0: no interrupt; 1: interrupt.
[24]	RO	intms_symb_rcv	When IR_CFG [ir_mode]=1, masked received symbol interrupt status. 0: no interrupt; 1: interrupt.
[23:20]	RO	reserved	reserve.
[19]	RO	intms_release	When IR_CFG [ir_mode]=0, the interrupt status of the masked key release. 0: no interrupt; 1: There is an interrupt.
[18]	RO	intms_overflow	When IR_CFG [ir_mode]=0, the masked receive data overflow error interrupt status. 0: no interrupt; 1: There is an interrupt.
[17]	RO	intms_framerr	When IR_CFG [ir_mode]=0, the masked received data frame format error interrupt status. 0: no interrupt; 1: There is an interrupt.

[16] RO		intms_rcv	When IR_CFG [ir_mode]=0, masked received data frame interrupt status. 0: no interrupt; 1: There is an interrupt.
[15:11] RO		reserved	reserve.
[10] RO		intrs_overrun	When IR_CFG [ir_mode]=1, symbol overflow interrupt status before masking. 0: no interrupt; 1: There is an interrupt.
[9]	RO	intrs_time_out	When IR_CFG [ir_mode]=1, symbol timeout interrupt status before masking. 0: no interrupt; 1: There is an interrupt.
[8]	RO	intrs_symb_rcv	When IR_CFG [ir_mode]=1, the interrupt status of received symbol before masking. 0: no interrupt; 1: There is an interrupt.
[7:4] RO		reserved	reserve.
[3]	RO	intrs_release	When IR_CFG [ir_mode]=0, the interrupt status of the key release before masking. 0: no interrupt; 1: There is an interrupt.
[2]	RO	intrs_overflow	When IR_CFG [ir_mode]=0, the received data before masking overflows the interrupt state. 0: no interrupt; 1: There is an interrupt.
[1]	RO	intrs_framerr	When IR_CFG [ir_mode]=0, the received data frame format error interrupt status before masking. 0: no interrupt; 1: There is an interrupt.
[0]	RO	intrs_rcv	When IR_CFG [ir_mode]=0, the received data frame interrupt status before masking. 0: no interrupt; 1: There is an interrupt.

IR_INT_CLR

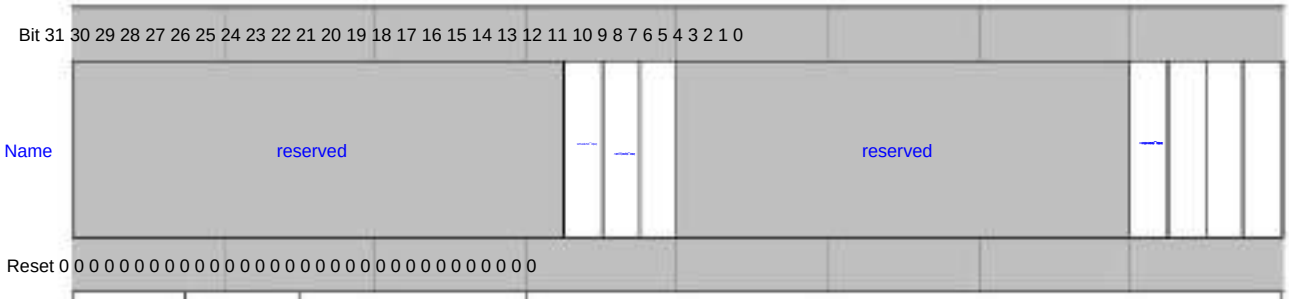
IR_INT_CLR is the IR interrupt clear register.

注意

When IR_CFG [ir_mode]=0, IR_INT_CLR bit[3:0] is valid;

When IR_CFG [ir_mode]=1, IR_INT_CLR bit[18:16] is valid.

Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000



Bits	Access	Name	Description
[31:19]	RO	reserved	reserve.
[18]	WC	intc_overrun	When IR_CFG [ir_mode]=1, clear symbol overflow interrupt request. 0: no effect; 1: Clear.
[17]	WC	intc_time_out	When IR_CFG [ir_mode]=1, clear symbol timeout interrupt request. 0: no effect; 1: Clear.
[16]	WC	intc_symb_rcv	When IR_CFG [ir_mode]=1, clear the received symbol interrupt request. 0: no effect; 1: Clear.
[15:4]	RO	reserved	reserve.
[3]	WC	intc_release	When IR_CFG [ir_mode]=0, clear the remote control button release interrupt request. 0: no effect; 1: Clear.
[2]	WC	intc_overflow	When IR_CFG [ir_mode]=0, clear the received data overflow error interrupt request. 0: no effect; 1: Clear.
[1]	WC	intc_framerr	When IR_CFG [ir_mode]=0, clear the received data frame format error interrupt request. 0: no effect; 1: Clear.

[0] WC	intc_rcv		When IR_CFG [ir_mode]=0, clear the received data frame interrupt request. 0: no effect; 1: Clear. If the interrupt request of received data frame is generated, the software directly writes 1 to this bit without reading the data in IR_DATAL , and the interrupt request cannot be cleared.

IS_START

IR_START is the IR start configuration register.

After the value configuration of other registers is completed, when starting the IR module, only one write operation to this address (the write operand can be any value) can start the configuration register.

Offset Address	Register Name	Total Reset Value
0x034	IS_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
Name	reserved		is_start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	WO	ir_start	IR Boot Configuration Register.

12.7 GPIO

12.7.1 Overview

Hi3519V100 supports 14 groups of GPIO (General Purpose Input/Output), namely GPIO0~GPIO13. Each group of GPIO provides 8 programmable input and output pins (GPIO13 only has 4). Each pin can be configured as input or output. These pins are used to generate application-specific output signals or to acquire application-specific input signals. When used as an input pin, GPIO can be used as an interrupt source; when used as an output pin, each GPIO can be independently cleared or set to 1.

GPIOs can generate maskable interrupts based on level or transition values. The GPIOINTR (General Purpose Input Output Interrupt) signal gives an indication to the interrupt controller that an interrupt has occurred.

注意

Please refer to

Hi3519V100_PINOUT_CN.xlsxÿ

For the GPIO multiplexed on the pins that are output signals by default, please note that the pins connected to the chip and device must be enter.

Since the pins SDIO0_CCLK_OUT, SDIO0_CCMD and SDIO0_CDATA0~3 (corresponding to GPIO8_1, GPIO8_2, GPIO8_3, GPIO8_4, GPIO8_5 and GPIO8_6) are powered by powerswitch0 inside the chip, so when these pins are used for GPIO functions, the control of powerswitch0 needs to be configured as Controlled by the MISC_CTRL3 register, i.e. configuration MISC_CTRL3[powerswitch0_sel_mux] is 0x1, MISC_CTRL3[powerswitch0_enable_mux] is 0x1, MISC_CTRL3[powerswitch0_enable] is 0x1. For these pins, the voltage to be supported is 3.3V, you need to configure MISC_CTRL3[powerswitch0_sel] to 0x0; if the voltage to be supported is 1.8V, you need to set MISC_CTRL3[powerswitch0_sel] to 0x1, and the power pin DVDD18_SDIO must be connected to 1.8V power supply.

Since the pins SDIO1_CCLK_OUT, SDIO1_CCMD and SDIO1_CDATA0~3 (corresponding to GPIO9_2, GPIO9_3, GPIO9_4, GPIO9_5, GPIO9_6 and GPIO9_7) are powered by powerswitch1 inside the chip, so when these pins are used for GPIO functions, the control of powerswitch1 needs to be configured as Controlled by the MISC_CTRL3 register, i.e. configuration MISC_CTRL3[powerswitch1_sel_mux] is 0x1 MISC_CTRL3[powerswitch1_enable_mux] is 0x1, MISC_CTRL3[powerswitch1_enable] is 0x1. For these pins, the voltage to be supported is 3.3V, you need to configure MISC_CTRL3[powerswitch1_sel] as 0x0; the supported voltage is 1.8V, you need to set MISC_CTRL3[powerswitch1_sel] to 0x1, and the power pin DVDD18_SDIO must be connected to 1.8V power supply.

12.7.2 Features

Each GPIO pin can be configured as input or output.

When used as an input pin, it can be used as an interrupt source. When used as output pins, each GPIO pin can be independently cleared or set to 1.

12.7.3 Working method

interface reset

When the chip is powered on or the system is reset, the GPIO module is reset at the same time, and the GPIO pins are in the input state after reset.

GPIO

Each pin can be configured as input or output, the specific steps are as follows:

Step 1. Refer to the corresponding bits of the "Pin Multiplexing Control Register" to configure the pins, and enable the functions of the GPIO pins to be used.

Step 2. Configure the register GPIO_DIR to select whether GPIO is used as input or output.

Step 3. When configured as an input pin, read the GPIO_DATA register to view the input signal value; when configured as an output pin, write the output value to the GPIO_DATA register to control the output level of the GPIO pin.

----Finish

When the GPIO is used as an output, the interrupt function of the GPIO should not be enabled, otherwise when the output signal meets the interrupt generation condition , a GPIO interrupt is generated.

interrupt operation

GPIO interrupts are controlled by 7 registers such as GPIO_IS . The interrupt source, polarity and edge characteristics can be selected through these registers. For the interrupt number corresponding to GPIO, please refer to "3.3 Interrupt System".

When multiple interrupts occur at the same time, they will be aggregated into one interrupt for reporting. For the GPIO interrupt mapping relationship, please refer to "3.3 Interrupt System".

The three registers GPIO_IS, GPIO_IBE, and GPIO_IEV jointly determine the characteristics of the interrupt source and the type of interrupt trigger.

Read the original state and masked state of the interrupt through GPIO_RIS and GPIO_MIS respectively. The final reporting of interrupts can be controlled through GPIO_IE. In addition, a separate GPIO_IC is provided for clearing control of interrupt status.

Each GPIO pin can be configured as an interrupt mode, the configuration steps are as follows:

Step 1. Configure GPIO_IS, select edge trigger or level trigger.

Step 2. Configure GPIO_IEV, select falling edge/rising edge trigger and high level/low level trigger.

Step 3. If edge trigger is selected, GPIO_IBE needs to be configured to select single-edge or double-edge trigger.

Step 4. Write 0xFF to the register GPIO_IC to clear the interrupt.

Step 5. Set GPIO_IE to 1 to enable interrupt.

----Finish

注意

During the initialization process, the data on the GPIO pins should be kept stable to avoid false interrupts.

The interrupt setting of GPIO is controlled by 7 registers. When one or more GPIO pins generate an interrupt, a combined interrupt output is sent to the interrupt controller. Edge trigger and level trigger have the following differences:

Edge Triggered Interrupt: Software must clear this interrupt to enable deeper interrupts.

Level-triggered interrupt: The external interrupt source should maintain this level until the processor recognizes the interrupt.

12.7.4 GPIO register overview

The base addresses of the 14 groups of GPIO registers are shown in Table 12-27 .

Table 12-27 Base addresses corresponding to 14 groups of GPIO registers

register	base address
GPIO13	0x1214_D000
GPIO12	0x1214_C000
GPIO11	0x1214_B000
GPIO10	0x1214_A000
GPIO9	0x1214_9000
GPIO8	0x1214_8000
GPIO7	0x1214_7000
GPIO6	0x1214_6000
GPIO5	0x1214_5000
GPIO4	0x1214_4000
GPIO3	0x1214_3000
GPIO2	0x1214_2000
GPIO1	0x1214_1000
GPIO0	0x1214_0000

Table 12-28 is the offset address and definition of a single group of GPIO internal registers. GPIO0~GPIO13 have the same register group.

说明

The register address corresponding to GPIOn is: GPIOn base address + offset address of this register.

The value range of n: [0, 13]

Table 12-28 GPIO register overview

offset address name		describe	page number
0x000ÿ0x3FC GPIO_DATA		GPIO data register	12-157
0x400	GPIO_DIR	GPIO direction control register	12-158
0x404	GPIO_IS	GPIO interrupt trigger register	12-158
0x408	GPIO_IBE	GPIO double-edge trigger interrupt register	12-159
0x40C	GPIO_IEV	GPIO trigger interrupt condition register	12-159
0x410	GPIO_IE	GPIO Interrupt Mask Register	12-160
0x414	GPIO_RIS	GPIO Raw Interrupt Status Register	12-160
0x418	GPIO_MIS	GPIO Mask Status Interrupt Register	12-161
0x41C	GPIO_IC	GPIO Interrupt Clear Register	12-161

12.7.5 GPIO register description

GPIO_DATA

GPIO_DATA is the GPIO data register. Used to cache input or output data.

When the corresponding bit in GPIO_DIR is configured as an output, the value written to the GPIO_DATA register will be output to the corresponding pin (note that the correct pin multiplexing needs to be configured); if it is configured as an input, the corresponding input pin will be read value.

注意

When the corresponding bit of GPIO_DIR is configured as an input, the valid read result will return the value of the pin; when configured as an output, the valid read result will return the written value.

The GPIO_DATA register uses PADDR[9:2] to realize the masking operation of reading and writing register bits. This register corresponds to 256 address spaces. PADDR[9:2] correspond to GPIO_DATA[7:0] respectively. When the corresponding bit is high, the corresponding bit can be read and written; otherwise, if the corresponding bit is low, the operation cannot be performed. For example:

If the address is 0x3FC (0b11_1111_1100), all 8-bit operations of GPIO_DATA[7:0] are valid.

If the address is 0x200 (0b10_0000_0000), it is only valid for the operation of GPIO_DATA[7].

Offset Address	Register Name	Total Reset Value
0x000ý0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:0]	RW	gpio_data		When GPIO is configured as input mode, it is input data for GPIO; when GPIO is configured as output mode, it is output data. Each bit can be controlled independently. Works with GPIO_DIR .

GPIO_DIR

GPIO_DIR is the GPIO direction control register. Used to configure the direction of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:0]	RW	gpio_dir		GPIO direction control register. bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit can be controlled independently. 0: input; 1: output.

GPIO_IS

GPIO_IS is the GPIO interrupt trigger register. It is used to configure the trigger level mode of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: Edge triggered interrupt; 1: Level triggered interrupt.

GPIO_IBE

GPIO_IBE is the GPIO double edge trigger interrupt register. Used to configure GPIO pin edge trigger mode.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge trigger control register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: single-edge trigger interrupt, specifically rising or falling edge trigger is controlled by GPIO_IEV ; 1: bilateral trigger interrupt.

GPIO_IEV

GPIO_IEV is the GPIO trigger interrupt condition register. Used to configure GPIO pins to trigger interrupt conditions.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO trigger interrupt condition register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: Falling edge or low level trigger interrupt; 1: Rising edge or high level trigger interrupt.

GPIO_IE

GPIO_IE is the GPIO interrupt mask register. Used to mask GPIO pin interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit is controlled independently. 0: mask interrupt; 1: Do not mask interrupts.

GPIO_RIS

GPIO_RIS is the GPIO raw interrupt status register. Used to query the original interrupt status of GPIO pins.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, indicating unmasked interrupt status. This state is not controlled by the GPIO_IE register mask. 0: Interrupt has not occurred; 1: Interrupt has occurred.

GPIO_MIS

GPIO_MIS is the GPIO mask status interrupt register. Used to query the interrupt status of the GPIO pins masked.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, indicating the masked interrupt status. This state is controlled by the GPIO_IE register mask. 0: Interrupt is invalid; 1: Interrupt is valid.

GPIO_IC

GPIO_IC is the GPIO interrupt clear register. It is used to clear the interrupt generated by GPIO pin, and clear the GPIO_RIS register and GPIO_MIS register at the same time.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name		Description
[7:0]	WC	gpio_ic		GPIO interrupt clear register, bit[7:0] correspond to GPIO_DATA[7:0] respectively, each bit can be controlled independently. 0: no effect; 1: Clear interrupt.

12.8 PCI Express

12.8.1 Overview

Hi3519V100's PCI Express (hereinafter referred to as PCIe) is mainly used for PCIe external expansion of SATA, network ports, WIFI and inter-chip cascading, etc.

12.8.2 Features

The PCI Express controller in Hi3519V100 has the following features:

- One PCI Express Gen2 X1 controller is supported. Support 1 VC, 1 TC. RC mode is supported.
- Support EP mode.
- Support DMA function.

12.8.3 Signal description

The PCI Express interface signals in Hi3519V100 are described as follows:

Table 12-29 PCI Express interface signal description

Signal Name	Direction	Description	Corresponding pin
Refclk_m	I	PCIe reference clock pin negative	PCIE_REFCLKM
Refclk_p	I	PCIe reference clock pin positive	PCIE_REFCLKP
Rx_m	I	PCIe receive differential signal negative	USB3_PCIE_RXM

Signal Name	Direction	Description	Corresponding pin
Rx_p	I	PCIe receive differential signal positive	USB3_PCIE_RXP
Tx_m	O	PCIe send differential signal negative	USB3_PCIE_TXM
Tx_p	O	PCIe send differential signal positive	USB3_PCIE_TXP

注意

In Hi3519V100 chip, because PCI Express interface and USB3.0 Port interface signals are multiplexed, when these signals are used as PCI Express interface, USB3.0 function is not available.

The interface is set to PCI Express mode by confirming the following pins:

The pin VO_DATA7 of the chip must be set as a pull-down resistor.

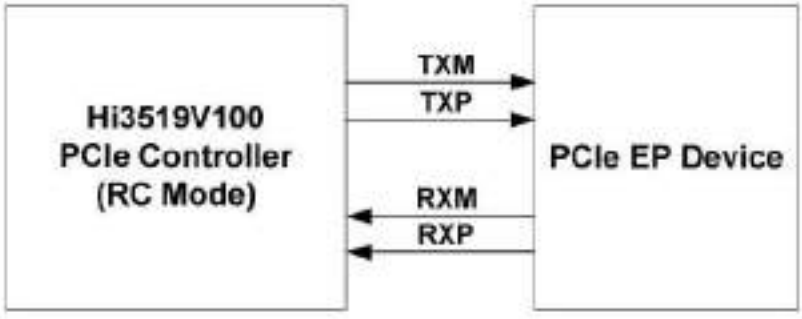
12.8.4 Functional description

RC (Root-Complex) mode

Hi3519V100 PCIe interface can be connected with other PCIe EP devices in RC mode to realize function expansion.

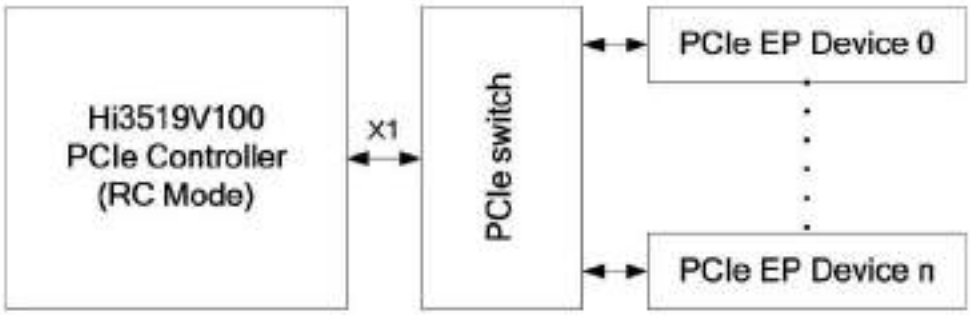
The application block diagram of the PCIe controller in RC mode is shown in Figure 12-52 .

Figure 12-52 PCIe controller application block diagram (RC mode external EP device)



The Hi3519V100 PCIe controller can also be connected to SWITCH devices to achieve more function expansion. The application block diagram of connecting with SWITCH devices in RC mode is shown in Figure 12-53 .

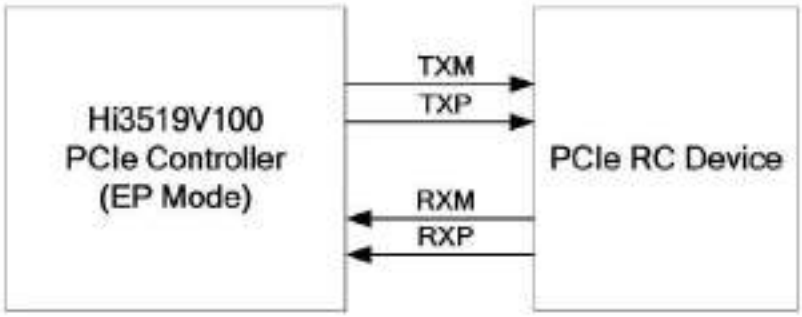
Figure 12-53 Application block diagram of the connection between PCIe controller and PCIe switch device (RC mode)



EP (End-Point) mode

The PCIe interface in Hi3519V100 can be set to EP mode to realize the connection with PCIe RC or SWITCH equipment.

Figure 12-54 Hi3519V100 and RC device connection application block diagram (EP mode)



12.8.5 Working method

12.8.5.1 Clock and Reset

clock setting

PCIe PHY needs a 100MHz reference clock when it works. There are two sources of this reference clock:

Hi3519V100 internal CRG

Pull down the chip VO_DATA5, at this time the PCIe interface clock pin is set to output mode, Hi3519V100 accepts the clock generated by the internal CRG as the PHY reference clock and outputs this internal differential clock to the peer device through the PCI Express clock pin as a reference clock . The external PCIe differential clock pulls up the chip VO_DATA5. At this time, the PCIe interface clock pin is set to input mode, and the external differential clock is accepted as the reference clock of PHY.

PCIe soft reset

Software can control the PCI Express reset through the PCI Express reset register. The PCI Express controller reset register is located in the PERI_CRG44 register in the CRG register. Please refer to the description of the PERI_CRG44 register in the CRG register.

12.8.5.2 Enable PCIe Controller

To enable the PCIe controller, proceed as follows:

Step 1. Turn off the PCIe controller by writing 0 to the PCIe internal system control register PCIE_SYS_CTRL7[pcie_app_ltssm_enable].

Step 2. Set CRG register PERI_CRG44 to enable PCIe controller clock.

Step 3. Set by PCIE_SYS_CTRL0[pcie_device_type] register in PCIe internal system control register
The working mode of the PCIe controller (RC mode/EP mode).

Step 4. Write 1 to the CRG register PERI_CRG44[pcie_bus_srst_req] to reset the PCIe controller.

Step 5. Write 0 to the CRG register PERI_CRG44[pcie_bus_srst_req] to deactivate the PCIe controller reset.

Step 6. When working in RC mode, you need to configure the corresponding controller class code register (CLASS Code
Register) is 0x060400 (corresponding to PCI to PCI bridge device). The class code registers for the PCIe controllers are located in the respective PCIe configuration register space.

Step 7. By writing 1 to PCIe internal system control register PCIE_SYS_CTRL7[pcie_app_ltssm_enable], enable
capable PCIe controller. After the PCIe controller is enabled, the PCIe controller starts the link establishment process.

----Finish

注意

Do not enable the PCIe controller without initializing the related system controller.

Link initialization and orientation is the process of configuring and initializing the physical layer of the device, ports, and associated links so that the link can carry normal packet traffic. The establishment of the link is automatically completed by the hardware. After the initialization and enabling of the PCIe controller, the establishment of the PCIe link is automatically initiated without any software participation.

The connection between the PCIe controller and the peer device is not established, and no PCIe transaction can be initiated to the peer device.

The software can determine whether the PCIe controller has established a connection with the peer device by querying the system control register PERI_PCIE_STAT0 [pcie_rdlh_link_up].

Please refer to the definition of the PERI_PCIE_STAT0 register in the system controller .

12.8.5.3 Initiate a PCIe transaction

Through the local bus interface, the bus read and write operations can be initiated by the CPU, and converted into corresponding PCIe transactions by the address conversion unit.

configuration transaction

Configuration transactions can only be initiated in RC mode.

It can be known from Section 12.8.5.5 Address Translation that the configuration transaction address space of the PCIe controller is 0x20000000~0x27FFFFFF.

The address conversion unit of the PCIe controller is responsible for converting the local bus operations within the address range of 0x20000000 to 0x27FFFFFF into corresponding PCIe configuration transactions.

The CPU initiates a bus read/write request on the local bus, and the fields of the bus address are configured as shown in Figure 12-55 , and the PCIe controller can issue a configuration read/write transaction.

Figure 12-55 PCIe controller configuration transaction local address field definition

BIT	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
Field	2	0	BUS_ID	DEV_ID FUN_ID	REG_NUM	0

in:

BUS_ID: The target bus number of the configuration transaction.

DEV_ID: The target device number of the configuration transaction.

FUN_ID: The target function number of the configuration transaction.

REG_NUM: The target register number of the configuration transaction

注意

The ATU in the PCIe controller shall implement the Type 0 and Type 1 configuration transaction translation area (CFG TYPE0 & CFG TYPE 1) to enable initiation of Type 0 and Type 1 configuration transactions. The setting reference is as follows:

Assume that the bus number of the PCIe controller is I, the bus number of the next-level device is J (J=I+1), and the bus number of the bus with the bus number J is K (K=I+2).

According to the PCIe protocol, the configuration operation initiated by the PCIe controller on the bus whose bus number is J is a type 0 configuration transaction, and the configuration operation initiated by the bus number greater than J is a type 1 operation.

Therefore, it is necessary to create an address conversion area to realize the conversion from the local bus address 0x20J00000ÿ0x20JFFFFF to the class Type 0 configures the address translation area for operation; at the same time, an address translation area is created to realize the local bus address 0x20K00000ÿ0x27FFFFFF is converted to the address conversion area of type 1 configuration transaction.

memory transaction

In RC and EP modes, the bus read/write operations initiated by the CPU in the memory address space will be translated into PCIe memory read/write transactions on the PCIe bus.

The CPU initiates a read/write request on the local bus, and the fields of the bus address are configured as shown in Figure 12-56 , and the PCIe controller can initiate a memory read/write transaction.

Figure 12-56 PCIe controller memory transaction local address field definition

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	2																															
	1	Target_address[26:0]																														

注意

If the ATU in the PCIe controller does not set the original address range of 0x28000000 ~ 0x2FFFFFFF address translation area, the address translation operation will not be performed on the addresses on the bus in the range of 0x28000000~0x2FFFFFFF, and the PCIe controller can only initiate memory transactions in the address range of 0x28000000~0x2FFFFFFF.

If it is necessary for the PCIe controller to initiate a memory transaction outside the address range of 0x28000000ÿ0x2FFFFFF, for example, to initiate a memory transaction of 0x50000000ÿ0x5FFFFFFF, the PCIe controller needs to create an address translation area to realize the address mapping from address 0x28000000ÿ0x2FFFFFF to address 0x50000000ÿ0x5FFFFFFF shoot. In this way, the read and write transactions of addresses 0x28000000~0x2FFFFFF initiated by the CPU on the local bus can be converted into memory read/write transactions of 0x50000000~0x5FFFFFFF through the address conversion unit.

I/O transactions

The CPU initiates a read/write request on the local bus, and the fields of the bus address are configured as shown in Figure 12-57 , and the PCIe controller can initiate an IO read/write transaction.

Figure 12-57 PCIe controller IO transaction local address field definition

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	2	Target_address[27:0]																														

注意

The ATU in the PCIe controller should implement the IO transaction translation area to implement the function of converting local bus operations into PCIe IO transactions. And the operation address initiated on the local bus is in the original address range of this IO transaction conversion area Inside.

Since IO transactions are mainly compatible with PCI cards, the current chip does not reserve a dedicated IO address space.

However, the IO address space can use the remaining unallocated addresses in 0x20000000~0x27FFFFFF (PCIe configuration transaction space) or 0x28000000~0x2FFFFFFF (PCIe memory transaction space) for IO transaction conversion.

For example: if the PCIe controller needs to initiate IO events outside the address range of 0x28000000~0x2FFFFFF

For example, to initiate an IO transaction of 0x50000000~0x5FFFFFFF, the PCIe controller needs to create an

The IO transaction conversion area realizes address 0x28000000ÿ0x2FFFFFF to address 0x50000000ÿ0x5FFFFFFF address mapping. In this way, the read and write transactions of addresses 0x28000000~0x2FFFFFF initiated by the CPU on the local bus can be converted into IO read/write transactions of 0x50000000~0x5FFFFFFF through the address conversion unit.

12.8.5.4 Transfer using DMA

The Hi3519V100 PCIe controller contains a DMA controller, and the DMA controller contains two DMA channels (one DMA read channel and one DMA write channel). The DMA controller included in the PCIe controller is used for large data storage read and write transactions to increase the rate of data transfer.

The DMA controller can implement the following memory read and write transactions:

DMA write: Move a piece of data from the local memory space to the memory space of the peer device.

DMA read: Move a piece of data from the memory space of the peer device to the local memory space.

By configuring the DMA control register, the full-duplex operation of the DMA read channel and the DMA write channel can be realized, that is, DMA read operations and DMA write operations can be performed simultaneously.

DMA Control Register

Software can configure the DMA transfer through the DMA control register, and can also start and stop the DMA transfer through the DMA control register. The DMA control register is located in the configuration register space of the PCIe controller. For the definition of the DMA control register, please refer to the description of the PCIe register in this chapter.

In order to reduce the configuration register space occupied by the DMA control register, part of the DMA control register address is The DMA read channel is shared with the DMA write channel. When it is necessary to configure this part of registers, the software needs to pass the configuration DMA channel index register (DMA_CH_INDEX) to indicate whether the subsequent operation object of these registers is to write the channel control register or read the channel control register.

This section of DMA control registers contains:

1. DMA_CH_CTRL register
2. DMA_TRANS_SIZE register
3. DMA_SAR_LOW and DMA_SAR_HIGH registers
4. DMA_DAR_LOW and DMA_DAR_HIGH registers

For example: if the software wants to set the DMA transfer length of DMA read channel 0 to 1024Byte, it needs to operate in the following order:

The software sets DMA_CH_INDEX[ch_dir]=1, indicating that the target register of the subsequent operation is to read the channel control register.

The software sets DMA_TRANS_SIZE=0x400, indicating that the transfer length is 1024Byte.

DMA read and write channel enable

The DMA channel is not enabled by default after the system is reset. To use the PCIe DMA channel, the DMA read and write channel must be enabled.

Enable DMA read channel by setting DMA_RD_ENGINE_EN[dma_rd_engine_en] to 1. Enable DMA write channel by setting DMA_WR_ENGINE_EN[dma_wr_engine_en] to 1.

DMA source and destination addresses

DMA write: the source address (SAR) is the local memory space, and the destination address (DAR) is the memory space of the peer device.

DMA read: the source address (SAR) is the memory space of the peer device, and the destination address (DAR) is the local memory space.

Configure the DMA_SAR_LOW and DMA_SAR_HIGH registers of the DMA read or write channel to specify the source address of the DMA transfer, and configure the DMA_DAR_LOW and DMA_DAR_HIGH registers of the DMA read or write channel to specify the destination address of the DMA transfer. For DMA source address and destination address registers, please refer to the definition of PCIe DMA control registers.

During a DMA transfer, the source address and destination address registers are incremented as the transfer progresses. The source address of the data currently transferred by the DMA and the target address of the currently written data can be determined by reading the values of the source address and destination address registers.

Both the DMA source address and the DMA destination address are double-byte aligned, so the lowest two bits must be set to 0. The lowest two bits are always 0 during transmission.

DMA transfer length

The transfer size of a DMA read or write operation is specified by the DMA_TRANS_SIZE register of the DMA read or write channel . The value of this register indicates the number of bytes of data that the DMA requests to transfer. During the DMA transfer process, the value of this register will decrement along with the transfer process, you can read this register to determine how many bytes are currently untransmitted. The value of this register should be 0 after the transfer is successfully completed.

The value range of DMA transfer length is: the minimum is 1 byte, and the maximum is 4G bytes.

Start DMA transfer

After configuring the control register of the DMA read channel, start the DMA read transfer by writing 0 to DMA_RD_DOORBELL[rd_doorbell_num].

After configuring the control register of the DMA write channel, start the DMA write transfer by writing 0 to DMA_WR_DOORBELL[wr_doorbell_num].

stop DMA transfer

If you need to stop the DMA transfer during the DMA transfer, you can manually stop it through the following register control DMA read or DMA write transfer:

Stop the DMA read transfer by writing 1 to DMA_RD_DOORBELL[dma_rd_stop]. Stop the DMA write transfer by writing 1 to DMA_WR_DOORBELL[dma_wr_stop].

If no errors occur during the DMA transfer, the DMA transfer will stop automatically after all data transfers are completed.

DMA interrupt

The DMA channel generates two types of interrupts:

Completion interrupt: Indicates that the DMA has successfully completed a DMA transfer.

Abort Interrupt: Indicates that the DMA transfer was unsuccessful, or an error occurred during the transfer.

The DMA read and DMA write channels share the same interrupt. After the CPU receives the PCIe DMA local interrupt, it checks the DMA_RD_INT_STAT and DMA_WR_INT_STAT registers to determine whether it is a DMA read channel interrupt or a DMA write channel interrupt, and whether it is a DMA completion interrupt or a DMA abort interrupt. Please refer to the description of DMA_RD_INT_STAT and DMA_WR_INT_STAT in the PCIe DMA register .

Through the DMA_RD_INT_CLR and DMA_WR_INT_CLR registers, the completion or abort interrupt of the corresponding read or write channel can be cleared. Please refer to the description of DMA_RD_INT_CLR and DMA_WR_INT_CLR in the register .

12.8.5.5 Address translation

address space

The PCIe controller in Hi3519V100 uses three address spaces:

Configuration register space: The CPU can access the configuration registers of the PCIe controller through this space.

Memory and IO Transaction Address Space: This space allows the CPU to initiate PCIe memory or IO transactions. Configuration transaction address space: CPU can initiate PCIe configuration read and write transactions through this space.

The three address spaces used by the PCIe controller are shown in Table 12-30 .

Table 12-30 PCIe controller-related address space

Address space type size start address end address description				
PCIe internal configuration register space	4K	0x12160000 0x12160FFF This space is the configuration register space defined by the PCI Express protocol and the PCIe internal system control register space.		
PCIe internal system control register space	4K	0x12161000 0x12161FFF This space is PCI Express P internal system control register space.		

Memory and IO Transaction Address Space	128M	0x20000000	0x27FFFFFF	The read and write operations in this space will on the PCIe link translates to Memory read and write or I/O read and write transactions defined by the PCIe protocol (requires the cooperation of the address translation function, please refer to the next section for the address translation function).
Configure Transaction Address Space	128M	0x28000000	0x2FFFFFFF	The read and write operations in this space will on the PCIe link translates to Type 0 configuration transaction or type 1 configuration transaction defined by PCIe protocol (requires the cooperation of address translation function, please refer to the next section for address translation function).

In the above address space, except that the target address of the address "configuration register space" is the PCIe controller itself, the target addresses of the rest of the address space are all peer devices that establish a connection with the PCIe controller. The address translation unit implements the function of converting operations in different address space ranges into corresponding PCIe transactions, or realizing target address translation.

Address Translation Unit (ATU)

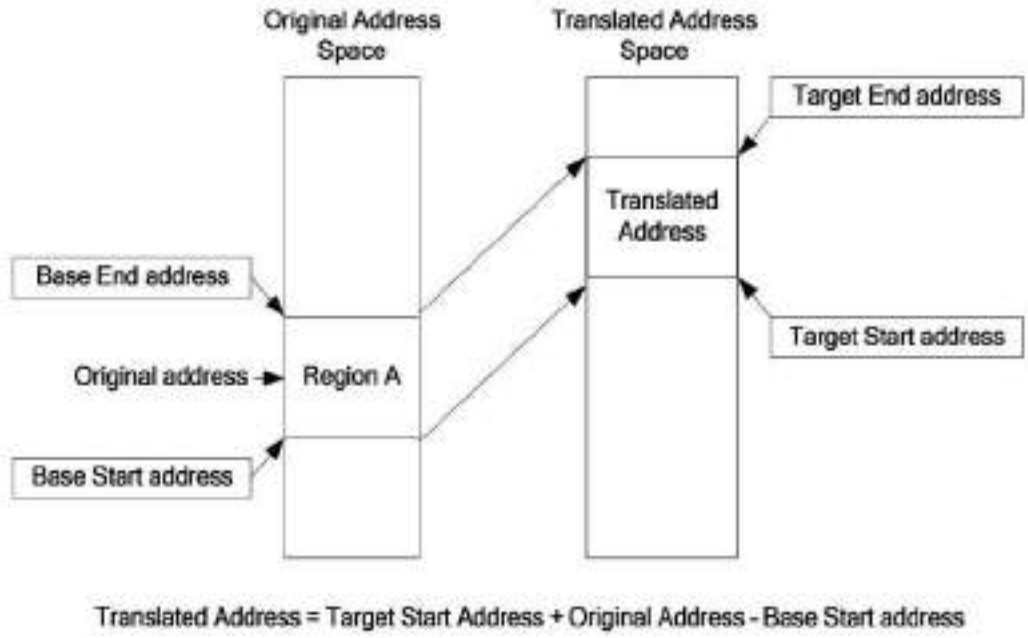
In different applications, the configuration of transaction type translation and target address translation may be different. Hi3535 provides an address translation unit (ATU) to realize the conversion of read and write operations of different addresses on the local bus to PCIe transaction types. The address translation unit (ATU) realizes the function of the translation of the target address.

Hi3535 provides 6 address conversion areas for the sending direction and receiving direction, and each area can independently implement a certain transaction type or address conversion function.

The address conversion unit in the sending direction can realize the conversion from the address operated by the local bus to the type of PCIe transaction or the conversion from the address operated by the local bus to the address of the PCIe transaction.

The translation from the local operation address to the PCIe transaction address is shown in Figure 12-58 , the original address of the address on the local bus (Original address) If it is within the range of the address translation area Region A, the address translation unit will translate this address into the address (Translated Address) translated by this address translation area, and the address in the PCIe transaction that appears on the PCIe bus will be given by The translated address (Translated Address) instead.

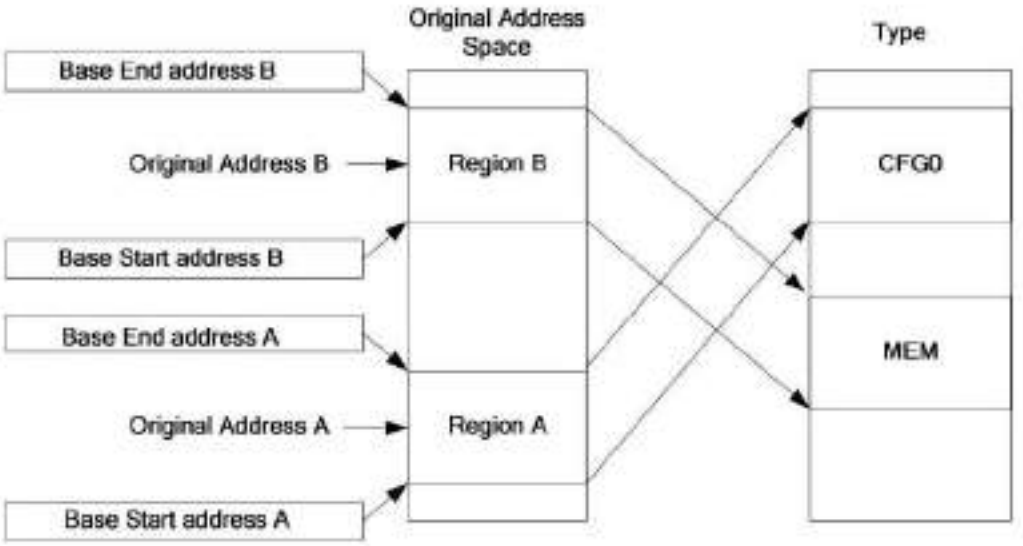
Figure 12-58 The address translation unit in the sending direction implements PCIe transaction address translation



The conversion from local operation address to PCIe transaction type is shown in Figure 12-59 . Address translation area A is configured as the conversion area from a certain address range to PCIe configuration 0 transaction (CFG Type 0), and the local operation address is in the range of address translation area A. Operations within will be converted to CFG0 operations on the PCIe bus. Address translation area B is configured as a translation area from a certain address range to PCIe memory transactions, and operations with local operation addresses within the range of address translation area B will be converted to

Memory transactions on the PCIe bus.

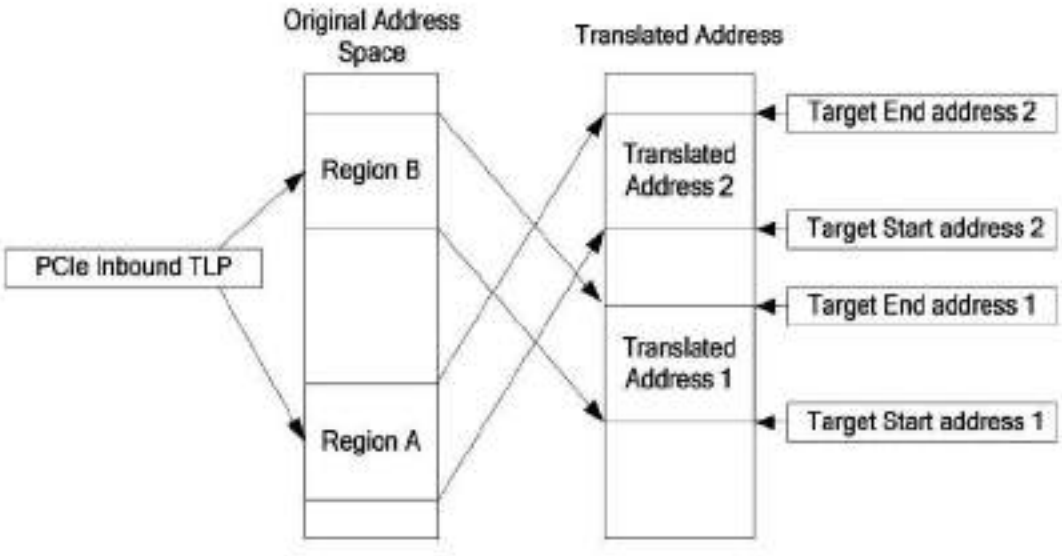
Figure 12-59 The address conversion unit in the sending direction implements PCIe transaction type conversion



By flexibly configuring the address translation area of each sending direction, various conversion modes from local bus operations to PCIe transactions can be realized.

Similar to the transmit direction, the receive direction also has an address translation unit to implement address translation from PCIe transactions to the internal bus. As shown in Figure 12-60 , after the PCIe transaction received in the receiving direction is converted by the address conversion area A or B, the corresponding operation can be converted to the address area Translated Address 1 or Translated Address 2, if Translated Address 1 corresponds to DDR memory address space, the operation received from the PCIe bus that meets the conditions of the address translation area can be converted into an operation on the DDR memory space.

Figure 12-60 The address translation unit in the receiving direction implements PCIe transaction address translation



ATU Control Registers

The address translation unit in the sending and receiving direction is disabled by default after system reset, so after system reset, the address translation unit needs to be configured and enabled to realize the address translation function.

Hi3519V100 provides a set of register interfaces in the PCIe configuration register space to configure the address translation unit (ATU). Through this group of registers, it is possible to configure the six address conversion areas in the sending direction and receiving direction.

ATU setting steps are as follows:

Step 1. Set the ATU area number register to the address translation area number to be configured.

Step 2. Set ATU Region Lower Base Address Register and ATU Region Upper Base Address Register. (Destination addresses in this area will be translated by the ATU where the area number register is located)

Step 3. Set ATU Region Limit Address Register.

Step 4. Set ATU Region Lower Target Address Register and ATU Region Upper Target Address Registerÿ

Step 5. Set ATU Region Control 1 Register.

Step 6. Set ATU Region Control 2 Register and enable this ATU Region.

----Finish

注意

In order to reduce the configuration register space occupied by the ATU control register, each of the six ATU areas in the sending and receiving directions is configured by the same set of registers. When configuring one of the ATU areas, you must first set

ATU_VIEWPORT register to indicate the ATU control register of which ATU area the subsequent operation on the ATU register targets.

For example: when it is necessary to set the ATU area 3 in the sending direction as an address translation area and make it effective, it needs to be set according to the following steps:

1. Set ATU_VIEWPORT[atu_reg_region_dir]=0x0, indicating that the operation object is the ATU region register in the sending direction.

2. Set ATU_VIEWPORT[atu_reg_region_index]=0x3, indicating that the operation object is in the sending direction

ATU zone 3.

3. Set other ATU registers according to the characteristics of this ATU area.

ATU settings

After the system is powered on and reset, the ATU register is not configured, the ATU function is not enabled, and the functions of address conversion and transaction type conversion cannot be realized. At this time, the address initiated on the local bus in the configuration transaction space or memory and IO transaction space operations are transferred as memory transactions on the PCIe bus, and the PCIe controller cannot initiate configuration transactions or IO transactions, nor can it implement the address translation function .

To enable the PCIe controller to issue configuration transactions or IO transactions, or to implement address mapping functions, an address translation area must be created through the ATU configuration registers.

In RC mode, RC needs to have the ability to convert operations initiated on the local bus into configuration transactions on the PCIe bus. In order to convert local bus operations into different PCIe transactions, at least the following send direction needs to be set:
ATU zone:

Area 1: Type 0 configuration transaction conversion area, this area implements the conversion of local bus operations into type 0 configuration transactions (CFG0). Area

2: Type 1 configuration transaction conversion area, this area implements the conversion of local bus operations into type 1 configuration transactions (CFG1). Area

3: IO operation conversion area, this area realizes the conversion of local bus operations into IO read and write transactions.

The above three areas can realize the basic transaction type conversion of RC mode. If necessary, the configuration of the three areas can be adjusted according to the actual situation, and the number of address translation areas can also be increased (up to 6 address translation areas in the sending direction).

In EP mode, the ATU input area needs to be configured to enable the peer device to access the internal address space of Hi3519V100. This configuration can be performed according to actual application needs.

For example, in EP mode, the operation of accessing the Hi3519V100 PCIe BAR0 address space of the peer RC device is mapped to the read and write operation of the DDR memory space, and the address conversion area 0 in the receiving direction can be configured as BAR0 to DDR memory in BAR address matching mode The address translation area for the address.

12.8.6 PCI Express Controller Registers

The PCIe controller configuration register space contains the PCIe standard registers.

When the PCIe controller is configured in RC mode, this PCIe controller configuration register space contains a type 1 PCIe configuration register header; when the PCIe controller is set to EP mode, this PCIe controller configuration register space contains a type 0 PCIe Configuration register header.

For the definition of type 0 and type 1 configuration register header, please refer to the PCIe specification, which will not be detailed here.

The following only describes in detail the registers defined by the manufacturer in Hi3519V100.

12.8.6.1 PCIe_iATU register overview

An overview of the PCIe_iATU registers is shown in Table 12-31 .

Table 12-31 PCIe_iATU register overview (base address is 0x1216_0000)

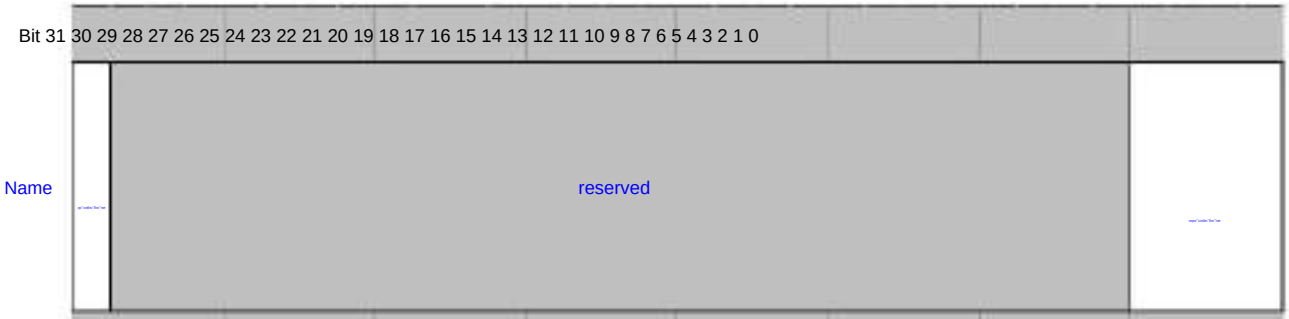
offset address name	describe	page number
0x0900 ATU_VIEWPORT	ATU Area Number Register	12-175
0x0904 ATU_REGION_CTRL1	ATU Region Control Register	12-176
0x0908 ATU_REGION_CTRL2	ATU Region Control Register	12-177
0x090C ATU_BASE_LOW	ATU base address low register	12-180
0x0910 ATU_BASE_HIGH	ATU base address high register	12-181
0x0914 OTHER_LIMIT	ATU Address Bounds Register	12-181
0x0918 ATU_TARGET_LOW	ATU target address low register	12-182
0x091C ATU_TARGET_HIGH	ATU target address high register	12-182

12.8.6.2 PCIe_iATU Register Description

ATU_VIEWPORT

ATU_VIEWPORT is ATU area number register.

Offset Address	Register Name	Total Reset Value
0x0900	ATU_VIEWPORT	0x0000_0000

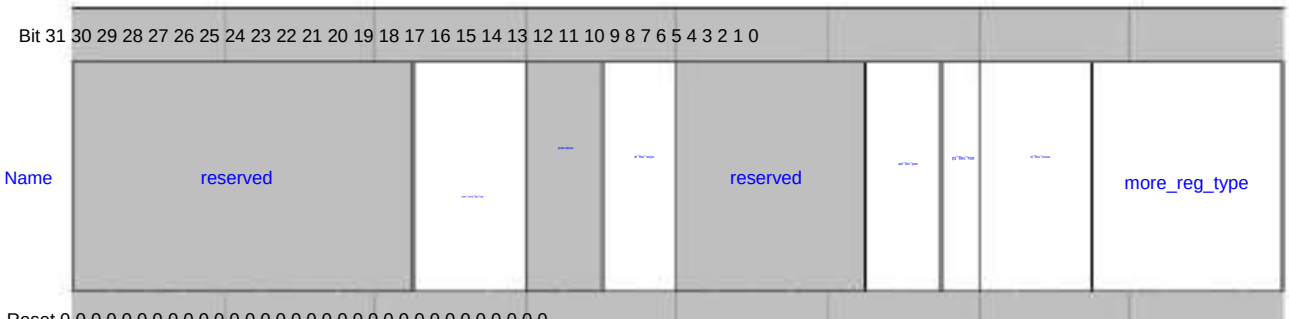


Bits	Access Name		Description
[31]	RW	atu_reg_region_dir	0: output address translation area; 1: input address translation area. area direction. Indicates whether it is a sending or receiving address translation area, and it is used together with the area number to determine the specific ATU area for operation.
[30:4]	RO	reserved	reserve.
[3:0]	RW	atu_reg_region_ind indicates the ex	area number. region number corresponding to the operation of the address translation control register. The area code assignment ranges from 0 to 5.

ATU_REGION_CTRL1

ATU_REGION_CTRL1 is the ATU region control register.

Offset Address	Register Name	Total Reset Value
0x0904	ATU_REGION_CTRL1	0x0000_0000



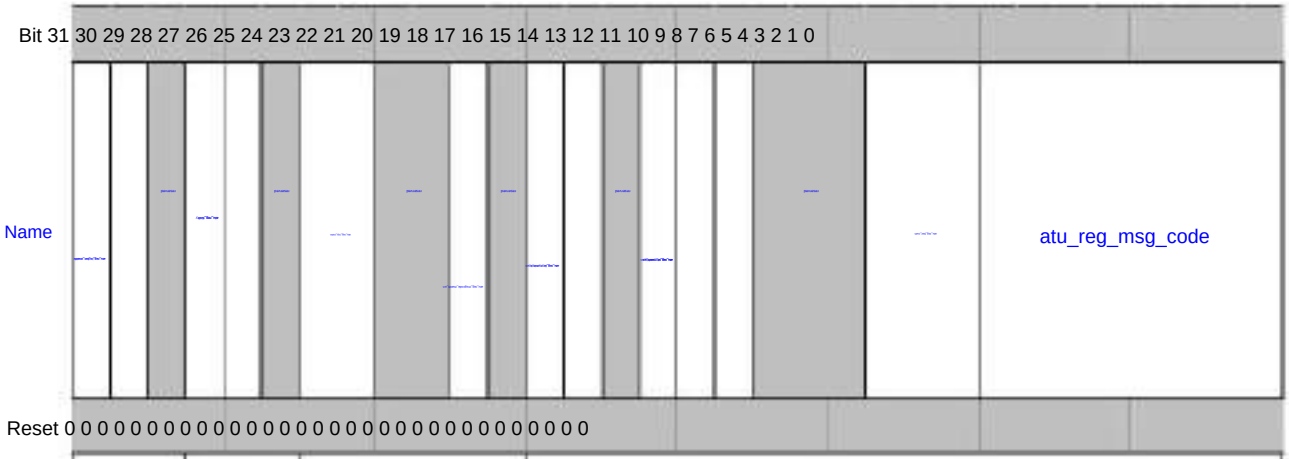
Bits	Access Name		Description
[31:23]	RO	reserved	reserve.

[22:20] RW	atu_reg_func_num	Receive (Inbound):	function number. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the function number field in the TLP data packet with the value of this register. When the BAR address of the function number corresponding to the register value in the received TLP packet matches, then do address conversion processing for the received TLP (only when the receiving area matches pattern is BAR address matching).
[19:18] RO		reserved	reserve.
[17:16] RW	atu_reg_at		AT field. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the AT field in the TLP data packet with the value of this register. Receive (Inbound): When the AT field in the received TLP packet matches this register, the address conversion process will be performed on the received TLP.
[15:11] RO		reserved	reserve.
[10:9] RW	other_reg_attr		ATTR field. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the ATTR field in the TLP data packet with the value of this register. Receiving (Inbound): When the ATTR field in the received TLP packet matches this register, the address translation process will be performed on the received TLP.
[8] RW	atu_reg_td		TD field. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the TD field in the TLP data packet with the value of this register. Receive (Inbound): When the TD field in the received TLP packet matches this register, the address conversion process will be performed on the received TLP.
[7:5] RW	other_reg_tc		TC field. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the TC field in the TLP data packet with the value of this register. Receiving (Inbound): When the TC field in the received TLP packet matches this register, the address translation process will be performed on the received TLP.
[4:0] RW	atu_reg_type		TYPE field. Outbound: When the TLP to be sent belongs to the range of this ATU area, replace the TYPE field in the TLP data packet with the value of this register. Receiving (Inbound): When the TYPE field in the received TLP packet matches this register, the address translation process will be performed on the received TLP.

ATU_REGION_CTRL2

ATU_REGION_CTRL2 is the ATU region control register.

Offset Address	Register Name	Total Reset Value
0x0908	ATU_REGION_CTRL2	0x0000_0000



Bits	Access	Name	Description
[31]	RW	atu_reg_region_ena	ATU zone enable. 0: Disable. ble 1: enable.
[30]	RW	atu_reg_in_bar_ma	Receive ATU matching mode selection. Send (Outbound): no effect. Receive (Inbound): Select the matching mode for receiving MEM/IO data packets. 0: address matching mode: when the received MEM/IO TLP address matches the address in ATU control register 1, do address translation. 1: BAR matching mode: When the received MEM/IO TLP address matches the BAR number, do address translation.
[29]	RO	reserved	reserve.
[28]	RW	atu_reg_shift	Configure the transaction shift function. This register is enabled when doing configuration type conversion, and can realize the conversion of operation address and bus number, device number, and function number (to realize the function of accessing all configuration spaces with 256M address space.). Send (Outbound): Assign 27~12 bits of the untranslated address to 31~16 bits of the converted address. Receiving (Inbound): Assign the 31~16 bits of the untranslated address of the received configuration transaction to the 27~12 bits of the converted address. 0: disable; 1: enable.
[27]	RW	atu_reg_fuzzy	Fuzzy type matching pattern. If enabled, enable transaction type fuzzy matching mode. 0: disable; 1: enable.

[26] RO		reserved	reserve.
[25:24] RW	atu_reg_rsp_code		Completion status code: Must be set to 0.
[23:22] RO		reserved	reserve.
[21] RW		atu_reg_msgcode_match_en	Message code matching enabled. Send (Outbound): Not used. Receive (Inbound): When enabled, match the message code in the received TLP with the atu_reg_msg_code in ATURegionCtrl2. 0: disable; 1: enable.
[20] RO		reserved	reserve.
[19] RW		number in the	Function number matching enabled. Send (Outbound): Not used. Inbound: When enabled, match the function received TLP with the atu_reg_func_num in atu_reg_func_match_en ATURegionCtrl1. 0: disable; 1: enable.
[18] RW		atu_reg_at_match_in	AT field matching enable. Send (Outbound): Not used. Receive (Inbound): When enabled, match the AT field in the received TLP with the atu_reg_at in ATURegionCtrl1. 0: disable; 1: enable.
[17] RO		reserved	reserve.
[16] RW		atu_reg_attr_match_en	ATTR field matching enable. Send (Outbound): Not used. Receive (Inbound): When enabled, match the ATTR field in the received TLP with the atu_reg_attr in ATURegionCtrl1. 0: disable; 1: enable.
[15] RW		atu_reg_td_match_in	TD field matching enabled. Send (Outbound): Not used. Receive (Inbound): When enabled, match the TD field in the received TLP with the atu_reg_td in ATURegionCtrl1. 0: disable; 1: enable.

[14] RW		received TLP with the in	TC field match enable. Send (Outbound): Not used. Inbound: When enabled, match the TC field atu_reg_tc_match_ in the atu_reg_tc in ATURegionCtrl1. 0: disable; 1: enable.
[13:11] RO		reserved	reserve.
[10:8] RW	atu_reg_bar_num		BAR number. Send (Outbound): Not used. Receiving (Inbound): When the BAR address in the received TLP matches the BAR address corresponding to this register, the address translation process will be performed on this TLP. 000ÿBAR#0ÿ 001ÿBAR#1ÿ 010ÿBAR#2ÿ 011ÿBAR#3ÿ 100ÿBAR#4ÿ 101ÿBAR#5ÿ 110ÿROMÿ 111: Reserved.
[7:0] RW	atu_reg_msg_code	reception (Inbound):	message code. Send (Outbound): When the sent TLP address matches this area, and the atu_reg_type field in ATURegionCtrl1 is MSG, then set the MSP field in the converted TLP to the value of this register. When atu_reg_msgcode_match_en in ATURegionCtrl2 is enabled, and the message code in the received message transaction matches the value of this register, the address translation process will be performed on this transaction packet.

ATU_BASE_LOW

ATU_BASE_LOW is the low register of ATU base address.

Offset Address	Register Name	Total Reset Value
0x090C	ATU_BASE_LOW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	atu_reg_base_low	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:12]	RW	atu_reg_base_low	Indicates the 31~12 bits of the start address of this area. When the untranslated address is within the range of the start address and the address boundary, the address matching condition is met. ATUBaseLow and ATUBaseHigh together form the base address.
[11:0]	RO	reserved	reserve.

ATU_BASE_HIGH

ATU_BASE_HIGH is the high register of ATU base address.

Offset Address	Register Name	Total Reset Value
0x0910	ATU_BASE_HIGH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	atu_reg_base_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
address is within the range of start	[31:0]	RW atu_reg_base_high	The upper 32 bits of the base address. Bits 63-32 of the start address of this area, when the untranslated address and the address boundary, the address matching condition is met. (This register is only valid in 64-bit address mode, it needs to be set to 0.)ATUBaseLow and ATUBaseHigh together form the base address.

OTHER_LIMIT

ATU_LIMIT is the ATU address limit register.

Offset Address	Register Name	Total Reset Value
0x0914	OTHER_LIMIT	0x0000_FFFF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	atu_reg_limit	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:12]	RW	atu_reg_limit	Address boundaries. 31~12 bits of the boundary address of this area, when the untranslated address is within the range of the start address and the address boundary, the address matching condition is met.
[11:0]	RO	reserved	reserve.

OTHER_TARGET_LOW

ATU_TARGET_LOW is the low register of ATU target address.

Offset Address	Register Name	Total Reset Value
0x0918	OTHER_TARGET_LOW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	atu_reg_trgt_low	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	atu_reg_trgt_low	When doing address conversion, the 31~12 bits of the converted address. ATUTargetLow and ATUTargetHigh together form the target address. The address translation formula is: Converted address = converted address - base address + target address. Converted address = converted address - base address + target address.
[11:0]	RO	reserved	reserve.

ATU_TARGET_HIGH

ATU_TARGET_HIGH is ATU target address high register.

Offset Address	Register Name	Total Reset Value
0x091C	ATU_TARGET_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_trgt_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW atu_reg_trgt_high	The upper 32 bits of the target address. When performing address conversion, the 63~32 bits of the converted address. ATUTargetHigh together form the target address.

12.8.6.3 PCIe_DMA register overview

An overview of the PCIe_DMA registers is shown in Table 12-32 .

Table 12-32 PCIe_DMA register overview (base address is 0x1216_0000)

offset address	name	describe	page number
0x097C	DMA_WR_ENGINE_IN	DMA Write Channel Enable Register	12-185
0x0980	DMA_WR_DOORBHE	DMA Write Operation Start and Stop Control Register 12-185	
0x099C	DMA_RD_ENGINE_IN	DMA read channel enable register	12-186
0x09A0	DMA_RD_DOORBELL	DMA Read Start and Stop Control Register 12-187	
0x09BC	DMA_WR_INT_STAT	DMA Write Interrupt Status Register	12-187
0x09C4	DMA_WR_INT_MASK	DMA Write Interrupt Mask Register	12-188
0x09C8	DMA_WR_INT_CLR	DMA Write Interrupt Clear Register	12-189
0x09CC	DMA_WR_ERR_STAT	DMA Write Operation Error Status Register	12-190
0x09D0	DMA_WR_DONE_IMWR_ADDR_LOW	DMA Write Complete Message Interrupt Address Low Register 12-191	
0x09D4	DMA_WR_DONE_IMWR_ADDR_HIGH	DMA Write Complete Message Interrupt Address High Register 12-191	
0x09D8	DMA_WR_ABORT_IMWR_ADDR_LOW	DMA Write Abort Message Interrupt Address Low Register 12-191	

offset address	name	describe	page number
0x09DC	DMA_WR_ABORT_IMWR_ADDR_HIGH	DMA Write Abort Message Interrupt Address High Register	12-192
0x09E0	DMA_WR_IMWR_DATA_0	DMA Write Operation Message Interrupt Data Register	12-192
0x0A10	DMA_RD_INT_STAT	DMA Read Interrupt Status Register	12-193
0x0A18	DMA_RD_INT_MASK	DMA Read Interrupt Mask Register	12-193
0x0A1C	DMA_RD_INT_CLR	DMA read operation interrupt clear register	12-194
0x0A24	DMA_RD_ERR_STAT_LOW	DMA Read Operation Error Status Low Register	12-195
0x0A28	DMA_RD_ERR_STAT_HIGH	DMA Read Error Status High Register	12-196
0x0A3C	DMA_RD_DONE_IMWR_ADDR_LOW	DMA Read Complete Message Interrupt Address Low Register	12-196
0x0A40	DMA_RD_DONE_IMWR_ADDR_HIGH	DMA Read Complete Message Interrupt Address High Register	12-197
0x0A44	DMA_RD_ABORT_IMWR_ADDR_LOW	DMA Read Abort Message Interrupt Address Low Register	12-197
0x0A48	DMA_RD_ABORT_IMWR_ADDR_HIGH	DMA Read Abort Message Interrupt Address High Register	12-198
0x0A4C	DMA_RD_IMWR_DATA_0	DMA read operation message interrupt data register	12-198
0x0A6C	DMA_CH_INDEX	DMA channel index register	12-198
0x0A70	DMA_CH_CTRL	DMA channel control register	12-199
0x0A78	DMA_TRANS_SIZE	DMA transfer length register register	12-201
0x0A7C	DMA_SAR_LOW	DMA data source address low register	12-201
0x0A80	DMA_SAR_HIGH	DMA data source address high register	12-201
0x0A84	DMA_DAR_LOW	DMA target address low register	12-202
0x0A88	DMA_DAR_HIGH	DMA target address high register	12-202

12.8.6.4 PCIe_DMA Register Description

DMA_WR_ENGINE_EN

DMA_WR_ENGINE_EN is the DMA write channel enable register.

Offset Address	Register Name	Total Reset Value
0x097C	DMA_WR_ENGINE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	dma_wr_engine_en	DMA write channel enable. 0: Disable DMA write channel. 1: Enable DMA write channel.

DMA_WR_DOORBELL

DMA_WR_DOORBELL is the DMA write operation start and stop control register.

Offset Address	Register Name	Total Reset Value
0x0980	DMA_WR_DOORBELL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dma_wr_stop	DMA write channel stopped. This register is used in conjunction with wr_doorbell_num to stop the data transmission of the corresponding DMA write channel. 0: No effect. 1: Stop the current DMA transfer.
[30:3]	RO	reserved	reserve.
[2:0]	RW	wr_doorbell_num	DMA write channel start. Start the DMA write transfer by writing 0 to this register (the DMA engine detects the write operation to this register and starts the DMA operation of the corresponding write channel. Since the current PCIe controller only supports one write channel, this register must be written 0).

DMA_RD_ENGINE_EN

DMA_RD_ENGINE_EN is the DMA read channel enable register.

Offset Address	Register Name	Total Reset Value
0x099C	DMA_RD_ENGINE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

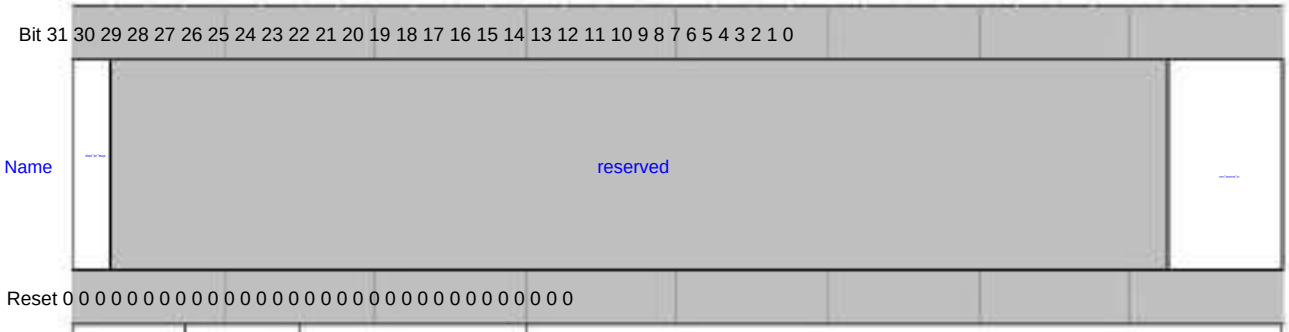
Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.

[0] RW	dma_wr_engine_en		DMA read channel enable. 0: Disable DMA read channel. 1: Enable DMA read channel.

DMA_RD_DOORBELL

DMA_RD_DOORBELL is the DMA read operation start and stop control register.

Offset Address	Register Name	Total Reset Value
0x09A0	DMA_RD_DOORBELL	0x0000_0000



Bits	Access	Name	Description
[31]	RW	dma_rd_stop	DMA read channel stopped. This register is used in conjunction with rd_doorbell_num to stop the data transmission of the corresponding DMA read channel. 0: No effect. 1: Stop the current DMA transfer.
[30:3]	RO	reserved	reserve.
[2:0]	RW	rd_doorbell_num	DMA read channel starts. Start the DMA read transfer by writing 0 to this register (the DMA engine detects the write operation to this register and starts the DMA operation of the corresponding read channel. Since the current PCIe controller only supports one read channel, this register must be written 0).

DMA_WR_INT_STAT

DMA_WR_INT_STAT is the DMA write interrupt status register.

Offset Address	Register Name	Total Reset Value
0x09BC	DMA_WR_INT_STAT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	dma_wr_abort_int_stat	DMA write operation aborted interrupt status. Indicates that the DMA write channel detected an error or manually stopped the DMA write operation. 0: invalid. 1: Valid.
[15:1]	RO	reserved	reserve.
[0]	RW	dma_wr_done_int_stat	DMA write operation complete interrupt status. Indicates that a DMA write operation has completed successfully. 0: No effect. 1: Valid.

DMA_WR_INT_MASK

DMA_WR_INT_MASK is the interrupt mask register for DMA write operation.

Offset Address	Register Name	Total Reset Value
0x09C4	DMA_WR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	dma_wr_abort_int_mask	DMA write abort interrupt mask. 0: dma_wr_abort_int_stat does not generate edma_int interrupt. 1: dma_wr_abort_int_stat can generate edma_int interrupt.
[15:1]	RO	reserved	reserve.
[0]	RW	dma_wr_done_int_mask	DMA write operation complete interrupt mask. 0: dma_wr_done_int_stat does not generate edma_int interrupt. 1: dma_wr_done_int_stat can generate edma_int interrupt.

DMA_WR_INT_CLR

DMA_WR_INT_CLR is the interrupt clear register for DMA write operation.

Offset Address	Register Name	Total Reset Value
0x09C8	DMA_WR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	dma_wr_abort_int_the	DMA write abort interrupt clear. Writing a 1 to this bit clears the clr dma_wr_abort_int_stat interrupt status in DMA_WR_INT_STAT register.
[15:1]	RO	reserved	reserve.
[0]	RW	interrupt clear. dma_wr_done_int_	DMA write operation complete Writing a 1 to this bit clears the clr dma_wr_done_int_stat interrupt status in the DMA_WR_INT_STAT register.

DMA_WR_ERR_STAT

DMA_WR_ERR_STAT is the DMA write operation error status register.

Offset Address	Register Name	Total Reset Value
0x09CC	DMA_WR_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	reserved	reserve

[15:1] RO		reserved	reserve.
[0] RW	app_rd_err_det	DMA write channel read data error.	

DMA_WR_DONE_IMWR_ADDR_LOW

DMA_WR_DONE_IMWR_ADDR_LOW is the low register of DMA write completion message interrupt address.

Offset Address	Register Name	Total Reset Value
0x09D0	DMA_WR_DONE_IMWR_ADDR_LOIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_wr_done_imwr_addr_low
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_done_imw DMA bits. r_addr_low	write complete interrupt message address lower 32

DMA_WR_DONE_IMWR_ADDR_HIGH

DMA_WR_DONE_IMWR_ADDR_HIGH is the high register of DMA write complete message interrupt address.

Offset Address	Register Name	Total Reset Value
0x09D4	DMA_WR_DONE_IMWR_ADDR_HIGH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_wr_done_imwr_addr_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_done_imw DMA bits. r_addr_high	write done interrupt message address upper 32

DMA_WR_ABORT_IMWR_ADDR_LOW

DMA_WR_ABORT_IMWR_ADDR_LOW is the low register of DMA write abort message interrupt address.

Offset Address	Register Name	Total Reset Value
0x09D8	DMA_WR_ABORT_IMWR_ADDR_LOW	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_wr_abort_imwr_addr_low
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	dma_wr_abort_im DMA bits. wr_addr_low	write abort interrupt message address lower 32

DMA_WR_ABORT_IMWR_ADDR_HIGH

DMA_WR_ABORT_IMWR_ADDR_HIGH is the DMA write abort message interrupt address high register.

Offset Address	Register Name	Total Reset Value
0x09DC	DMA_WR_ABORT_IMWR_ADDR_HIGH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_wr_abort_imwr_addr_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	dma_wr_abort_im DMA bits. wr_addr_high	write abort interrupt message address upper 32

DMA_WR_IMWR_DATA_0

DMA_WR_IMWR_DATA_0 is the DMA write operation message interrupt data register.

Offset Address	Register Name	Total Reset Value
0x09E0	DMA_WR_IMWR_DATA_0	0x0000_0000

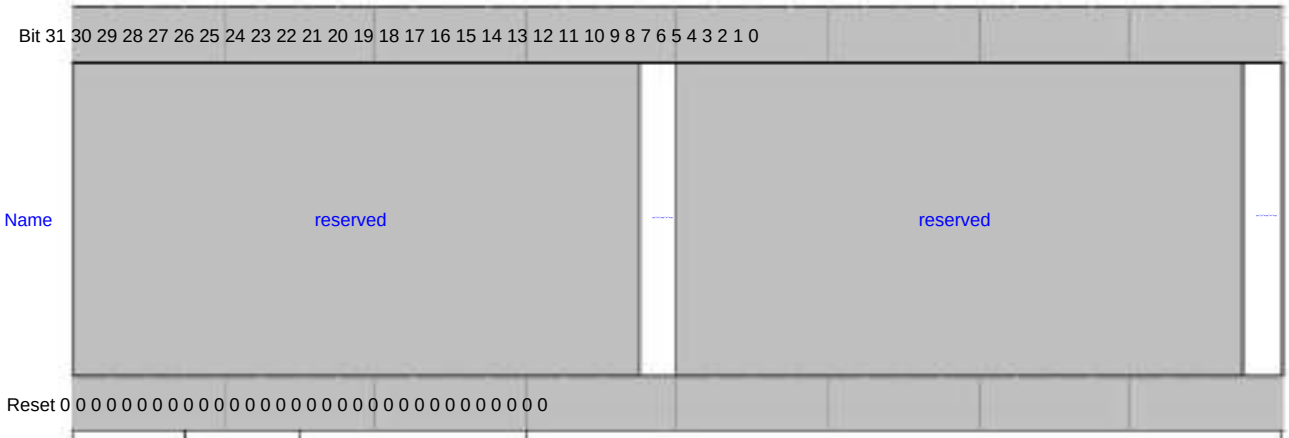
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / dma_wr_imwr_data_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	dma_wr_imwr_dat DMA	write channel 0 interrupt message data. a_0

DMA_RD_INT_STAT

DMA_RD_INT_STAT is the DMA read interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0A10	DMA_RD_INT_STAT	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	write operation. dma_wr_abort_int_stat 0: invalid. 1: Valid.	DMA read operation aborted interrupt status. Indicates that the DMA read channel detected an error or manually stopped the DMA
[15:1]	RO	reserved	reserve.
[0]	RW	completed successfully. dma_wr_done_int_stat 0: No	DMA read operation complete interrupt status. Indicates that a DMA read operation has effect. 1: Valid.

DMA_RD_INT_MASK

DMA_RD_INT_MASK is the interrupt mask register for DMA read operation.

Offset Address	Register Name	Total Reset Value
0x0A18	DMA_RD_INT_MASK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16]	RW	dma_wr_abort_int_mask	DMA read abort interrupt mask. 0: dma_rd_abort_int_stat does not generate edma_int interrupt. 1: dma_rd_abort_int_stat can generate edma_int interrupt.
[15:1]	RO	reserved	reserve.
[0]	RW	dma_wr_done_int_mask	DMA read complete interrupt mask. 0: dma_rd_done_int_stat does not generate edma_int interrupt. 1: dma_rd_done_int_stat can generate edma_int interrupt.

DMA_RD_INT_CLR

DMA_RD_INT_CLR is the interrupt clear register for DMA read operation.

Offset Address	Register Name	Total Reset Value
0x0A1C	DMA_RD_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:17]	RO	reserved	reserve.
[16]	RW	dma_wr_abort_int_the	DMA read abort interrupt clear. Writing a 1 to this bit clears the clr dma_rd_abort_int_stat interrupt status in DMA_RD_INT_STAT register.
[15:1]	RO	reserved	reserve.
[0]	RW	dma_wr_done_int_in	DMA read abort interrupt clear. Writing a 1 to this bit will clear the clr dma_rd_done_int_stat interrupt status the DMA_RD_INT_STAT register.

DMA_RD_ERR_STAT_LOW

DMA_RD_ERR_STAT_LOW is the DMA read operation error status low register.

Offset Address	Register Name	Total Reset Value
0x0A24	DMA_RD_ERR_STAT_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

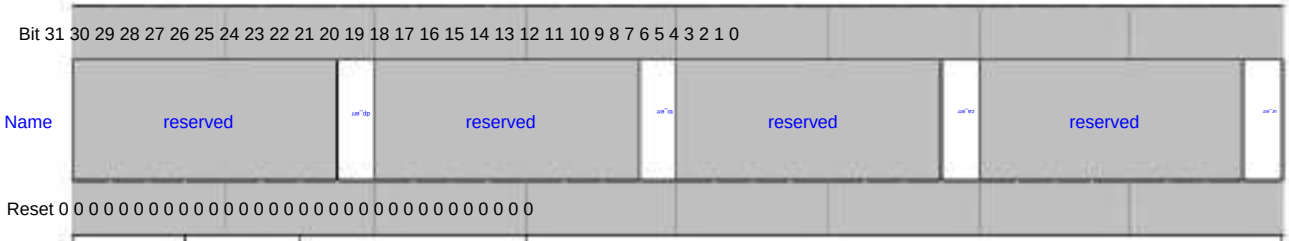
Bits	Access Name		Description
[31:17]	RO	reserved	reserve.

[16] RW	reserved		reserve.
[15:1] RO		reserved	reserve.
[0] RW	app_rd_err_det	DMA read channel detected AXI bus error response.	

DMA_RD_ERR_STAT_HIGH

DMA_RD_ERR_STAT_HIGH is the DMA read operation error status high register.

Offset Address	Register Name	Total Reset Value
0x0A28	DMA_RD_ERR_STAT_HIGH	0x0000_0000



Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24]	RW	dp_err	The DMA channel detected poisoned data from a peer device.
[23:17]	RO	reserved	reserve.
[16]	RW	to_err	DMA channel read operation timed out.
[15:9]	RO	reserved	reserve.
[8]	RW	ca_err	The DMA channel detects a CA (Completion Abort) completion packet from the peer device.
[7:1]	RO	reserved	reserve.
[0]	RW	ur_err	The DMA channel detects a UR (Unsupported Request) completion packet from the peer device.

DMA_RD_DONE_IMWR_ADDR_LOW

DMA_RD_DONE_IMWR_ADDR_LOW is the low register of DMA read completion message interrupt address.

Offset Address	Register Name	Total Reset Value
0x0A3C	DMA_RD_DONE_IMWR_ADDR_LOIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_done_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_rd_done_imw DMA bits. r_addr_low	read done interrupt message address lower 32

DMA_RD_DONE_IMWR_ADDR_HIGH

DMA_RD_DONE_IMWR_ADDR_HIGH is the high register of DMA read completion message interrupt address.

Offset Address	Register Name	Total Reset Value
0x0A40	DMA_RD_DONE_IMWR_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_done_imwr_addr_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_rd_done_imw DMA bits. r_addr_high	read done interrupt message address upper 32

DMA_RD_ABORT_IMWR_ADDR_LOW

DMA_RD_ABORT_IMWR_ADDR_LOW is the DMA read abort message interrupt address low register.

Offset Address	Register Name	Total Reset Value
0x0A44	DMA_RD_ABORT_IMWR_ADDR_LOIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_abort_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_rd_abort_imw DMA bits. r_addr_low	read abort interrupt message address lower 32

DMA_RD_ABORT_IMWR_ADDR_HIGH

DMA_RD_ABORT_IMWR_ADDR_HIGH is the DMA read abort message interrupt address high register.

Offset Address	Register Name	Total Reset Value
0x0A48	DMA_RD_ABORT_IMWR_ADDR_HIGH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_rd_abort_imwr_addr_high
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	dma_rd_abort_imw DMA bits. r_addr_high	read abort interrupt message address upper 32

DMA_RD_IMWR_DATA_0

DMA_RD_IMWR_DATA_0 is the DMA read operation message interrupt data register.

Offset Address	Register Name	Total Reset Value
0x0A4C	DMA_RD_IMWR_DATA_0	0x0000_0000

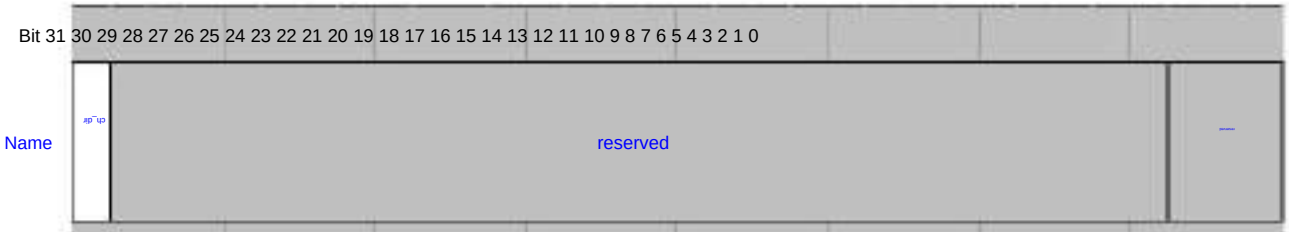
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / dma_wr_imwr_data_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	dma_wr_imwr_dat DMA	read channel 0 interrupt message data. a_0

DMA_CH_INDEX

DMA_CH_INDEX is the DMA channel index register.

Offset Address	Register Name	Total Reset Value
0x0A6C	DMA_CH_INDEX	0x0000_0000

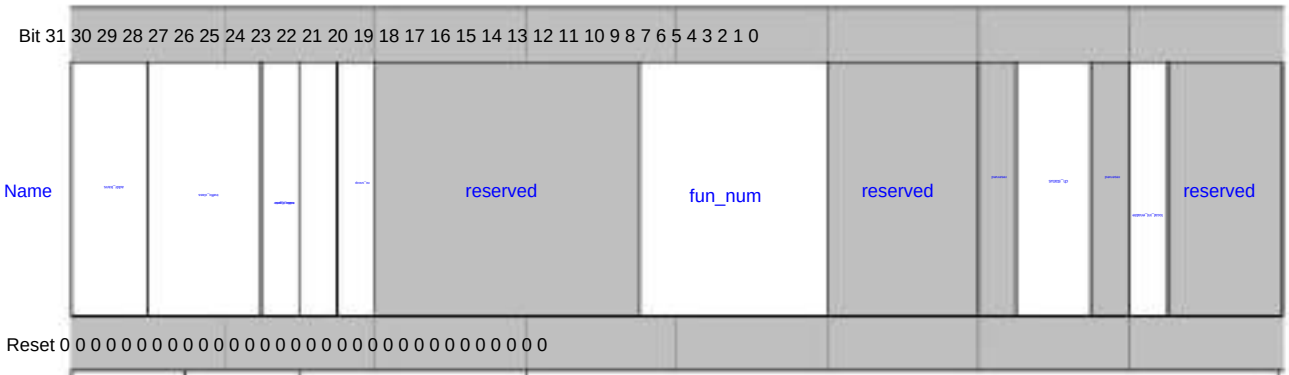


Bits	Access	Name	Description
[31]	RW	ch_dir	channel direction. This bit selects whether the register to be configured belongs to the read channel or the write channel. 0: Write channel. 1: Read channel.
[30:3]	RO	reserved	reserve.
[2:0]	RO	reserved	Reserved, must be set to 0.

DMA_CH_CTRL

DMA_CH_CTRL is the DMA channel control register.

Offset Address	Register Name	Total Reset Value
0x0A70	DMA_CH_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:30]	RW	addr_trans	PCIe transaction AT bit. The AT bit in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.
[29:27]	RW	traffic_class	PCIe transaction TC bit. The TC bit in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.

[26] RW traffic_digest			PCIe transaction TD bit. The TD bit in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.
[25] RW relaxed_order			PCIe transaction RO bit. The RO bit in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.
[24] RW no_snoop			PCIe transaction NS bit. The NS bit in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.
[23:17] RO		reserved	reserve.
[16:12] RW fun_num			PCIe transaction fun_num bits. The function number in the PCIe memory read and write transaction packet initiated by DMA will be replaced by this member value.
[11:10] RO		reserved	reserve.
[9]	RO	reserved	reserve.
[8]	RO	reserved	reserve.
[7]	RO	reserved	reserve.
[6:5] RW ch_status			channel status. Indicates the working state of the channel. 00: reserved. 01: DMA transfer in progress. 10: Operation error. 11: The channel successfully completed the DMA transfer or the channel was manually stopped from transferring.
[4]	RO	reserved	reserve.
[3] RW local_int_enable			Local DMA interrupt enable. Setting this bit to enable a DMA local interrupt can be issued when a DMA transfer completes or fails. 0: Disable DMA local interrupt; 1: Enable DMA local interrupt.
[2]	RO	reserved	reserve.
[1]	RO	reserved	reserve.
[0]	RO	reserved	reserve.

DMA_TRANS_SIZE

DMA_TRANS_SIZE is the DMA transfer length register register.

Offset Address	Register Name	Total Reset Value
0x0A78	DMA_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_trans_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dma_trans_size	DMA transfer length. Before DMA transfer, write the data length to be transferred into this register, the minimum transfer length is 1 byte, and the maximum is 4G bytes. During DMA transfers, this register value is automatically decremented. The value of the register is the number of bytes not transferred, and this register is 0 after the transfer is successfully completed.

DMA_SAR_LOW

DMA_SAR_LOW is the low register of DMA data source address.

Offset Address	Register Name	Total Reset Value
0x0A7C	DMA_SAR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_sar_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW dma_sar_low	The source address (lower 32 bits) of DMA transfer data. Write the start address of the source data into this register before DMA transfer, and the DMA channel will get the data to be transferred from this address. During DMA transfers, the value of this register is automatically incremented. The lower 2 bits of this register must be 0.

DMA_SAR_HIGH

DMA_SAR_HIGH is the high register of DMA data source address.

Offset Address	Register Name	Total Reset Value
0x0A80	DMA_SAR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_sar_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_sar_high	Source address (upper 32 bits) of DMA transfer data. Must be 0 in 32-bit address mode. In 64-bit address mode, it forms 64-bit source address with DMA_SAR_LOW .

DMA_DAR_LOW

DMA_DAR_LOW is the DMA target address low register.

Offset Address	Register Name	Total Reset Value
0x0A84	DMA_DAR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_dar_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_dar_low	Destination address of DMA transfer data (lower 32 bits). Write the destination address to this register before DMA transfer, and the DMA channel will write the data fetched from the source address into the destination address. During DMA transfers, the value of this register is automatically incremented. The lower 2 bits of this register must be 0.

DMA_DAR_HIGH

DMA_DAR_HIGH is the DMA target address high register.

Offset Address	Register Name	Total Reset Value
0x0A88	DMA_DAR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_dar_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	dma_dar_high	Destination address (upper 32 bits) of DMA transfer data. Must be 0 in 32-bit address mode. In 64-bit address mode, it forms a 64-bit target address with DMA_DAR_LOW .

12.8.6.5 PCIe MISC Register Overview

An overview of the PCIe MISC registers is shown in Table 12-33 .

Table 12-33 PCIe MISC register overview (base address is 0x1216_0000)

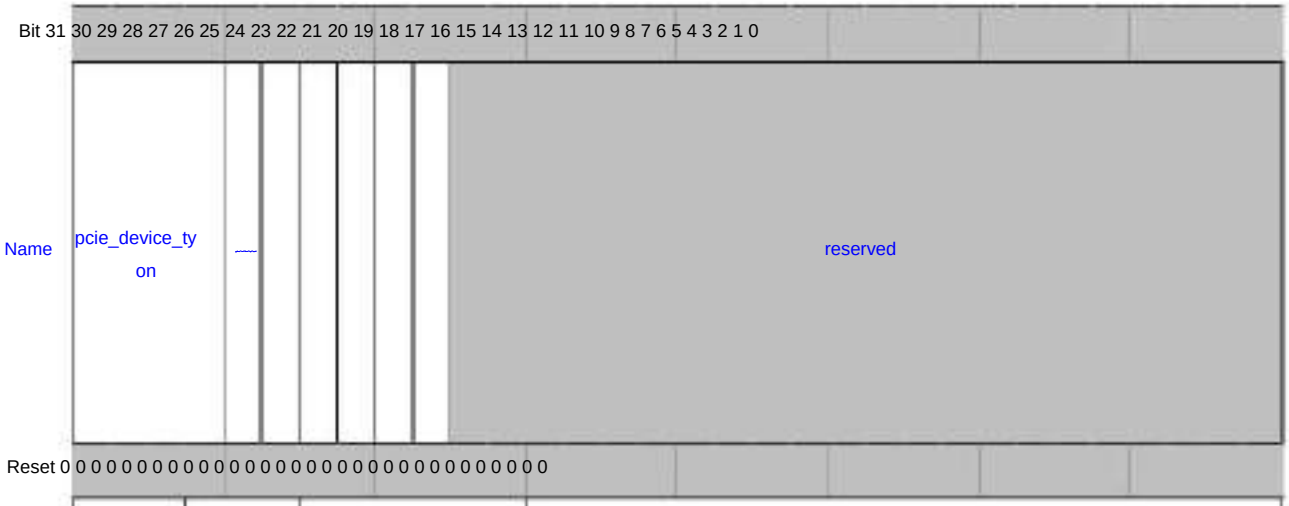
offset address	name	describe	page number
0x1000	PCIE_SYS_CTRL0	PCIE Control Register 0	12-203
0x1004	PCIE_SYS_CTRL1	PCIE Control Register 1	12-205
0x1008	PCIE_SYS_CTRL2	PCIE Control Register 2	12-205
0x100C	PCIE_SYS_CTRL3	PCIE Control Register 3	12-206
0x1010	PCIE_SYS_CTRL4	PCIE Control Register 4	12-207
0x1014	PCIE_SYS_CTRL5	PCIE Control Register 5	12-208
0x1018	PCIE_SYS_CTRL6	PCIE Control Register 6	12-208
0x101C	PCIE_SYS_CTRL7	PCIE control register 7	12-209
0x1100	PERI_PCIE_STAT0	PCIE status register 0	12-210

12.8.6.6 PCIe MISC Register Description

PCIE_SYS_CTRL0

PCIE_SYS_CTRL0 is PCIE control register 0.

Offset Address	Register Name	Total Reset Value
0x1000	PCIE_SYS_CTRL0	0x0000_0000



Bits	Access	Name	Description
[31:28]	RW	pcie_device_type	The mode of the PCIe controller. 0x0: PCI Express EP device; 0x1: Legacy PCI Express device; 0x4: PCI Express RC device; Others: Reserved.
[27]	RW	pcie_slv_resp_err_Map	PCIe bus SLV port CPL TIMEOUT error mapping control. 0: Map CPL TIMEOUT errors to DEC_ERR; map5 1: CPL TIMEOUT errors to SLV_ERR.
[26]	RW	pcie_slv_resp_err_Map	PCIe bus SLV port CPL ECRC error map control. 0: Map CPL ECRC errors to DEC_ERR; map4 1: CPL ECRC errors to SLV_ERR.
[25]	RW	pcie_slv_resp_err_Map	PCIe bus SLV port CPL poisoned error mapping control. 0: Map CPL poisoned errors to DEC_ERR; map3 1: CPL poisoned errors to SLV_ERR.
[24]	RW	pcie_slv_resp_err_map	PCIe bus SLV port CPL CA error mapping control. 0: map CPL CAT errors to DEC_ERR; map2 1: CPL CA errors to SLV_ERR.
[23]	RW	pcie_slv_resp_err_map	PCIe bus SLV port CPL CRS error mapping control. 0: map CPL CRS errors to DEC_ERR; map1 1: CPL CRS errors to SLV_ERR.

[22] RW		pcie_slv_resp_err_ 0: CPL UR errors to SLV_ERR.	PCIe bus SLV port CPL UR error mapping control. Map CPL UR errors to DEC_ERR; map0 1: Map
[21:0] RO		reserved	reserve.

PCIE_SYS_CTRL1

PCIE_SYS_CTRL1 is PCIE control register 1.

Offset Address	Register Name	Total Reset Value
0x1004	PCIE_SYS_CTRL1	0x0000_0000

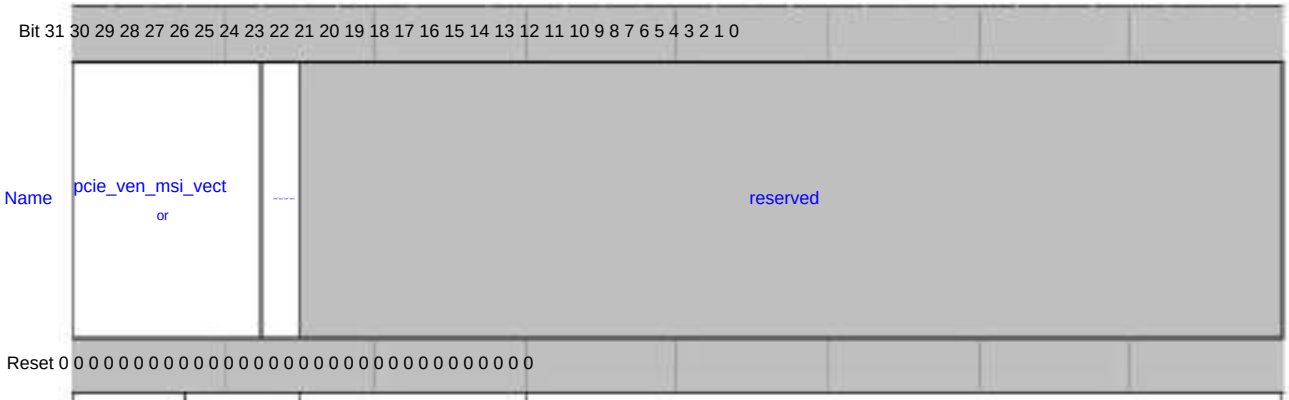
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23]	RW	pcie_app_clk_req_n	PCIe controller application layer clock request. 0: apply clock; 1: Do not apply clock.
[22:0]	RO	reserved	reserve.

PCIE_SYS_CTRL2

PCIE_SYS_CTRL2 is PCIE control register 2.

Offset Address	Register Name	Total Reset Value
0x1008	PCIE_SYS_CTRL2	0x0000_0000



Bits	Access Name		Description
[31:27] RW		pcie_ven_msi_vect When the or	PCIe Controller MSI Data Alignment Control Register. PCIe controller initiates an MSI interrupt request, the value of this register is the lowest 5 bits of the MSI data (the value of this register and the value of the MSI data register are bitwise or the value is the new MSI data).
[26] RW	pcie_ven_msi_req		Indicates whether the PCIe controller requests to send a Message Interrupt (MSI). 0: no request; 1: request.
[25:0] RO		reserved	reserve.

PCIE_SYS_CTRL3

PCIE_SYS_CTRL3 is PCIE control register 3.

Offset Address	Register Name	Total Reset Value
0x100C	PCIE_SYS_CTRL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_ven_msg_code								pcie_ven_msg_tag								reserved												pcie_ven_msg_typ			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	pcie_ven_msg_cod	Message codes for PCIe vendor-defined messages. This register specifies the message code for a vendor-defined message when sent by PCIe.
[23:16]	RW	pcie_ven_msg_tag	When a PCIe vendor-defined message request is initiated by the PCIe controller, this register is used to configure the TAG field of the PCIe vendor-defined message request packet.
[15:12]	RO	reserved	reserve.
[11:10]	RW	pcie_ven_msg_attr	When a PCIe vendor-defined message request is initiated by the PCIe controller, this register is used to configure the ATTR field of the PCIe vendor-defined message request packet.
[9]	RW	pcie_ven_msg_ep	When a PCIe vendor-defined message request is initiated by the PCIe controller, this register is used to configure the EP field of the PCIe vendor-defined message request packet.
[8]	RW	pcie_ven_msg_td	When a PCIe vendor-defined message request is initiated by the PCIe controller, this register is used to configure the TD field of the PCIe vendor-defined message request packet.
[7:3]	RW	pcie_ven_msg_type	When the PCIe controller initiates a PCIe vendor-defined message request, this register is used to configure the TYPE field of the PCIe vendor-defined message request packet.
[2:1]	RW	pcie_ven_msg_fmt	When a PCIe vendor-defined message request is initiated by the PCIe controller, this register is used to configure the FMT field of the PCIe vendor-defined message request packet.
[0]	RW	pcie_ven_msg_req	Indicates whether the PCIe controller requests to send a vendor-defined message. 0: no request; 1: request.

PCIE_SYS_CTRL4

PCIE_SYS_CTRL4 is PCIE control register 4.

Offset Address	Register Name	Total Reset Value
0x1010	PCIE_SYS_CTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_ven_msg_data_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	register pcie_ven_msg_data	When a PCIe vendor-defined message transaction is initiated by the PCIe controller, this is used to configure the third double word _low (DWORD) of the PCIe vendor-defined message transaction data packet.

PCIE_SYS_CTRL5

PCIE_SYS_CTRL5 is PCIE control register 5.

Offset Address	Register Name	Total Reset Value
0x1014	PCIE_SYS_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_ven_msg_data_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	register pcie_ven_msg_data message	When a PCIe vendor-defined message transaction is initiated by the PCIe controller, this is used to configure the fourth double word _high (DWORD) of the PCIe vendor-defined transaction data packet.

PCIE_SYS_CTRL6

PCIE_SYS_CTRL6 is PCIE control register 6.

Offset Address	Register Name	Total Reset Value
0x1018	PCIE_SYS_CTRL6	0x0000_0000

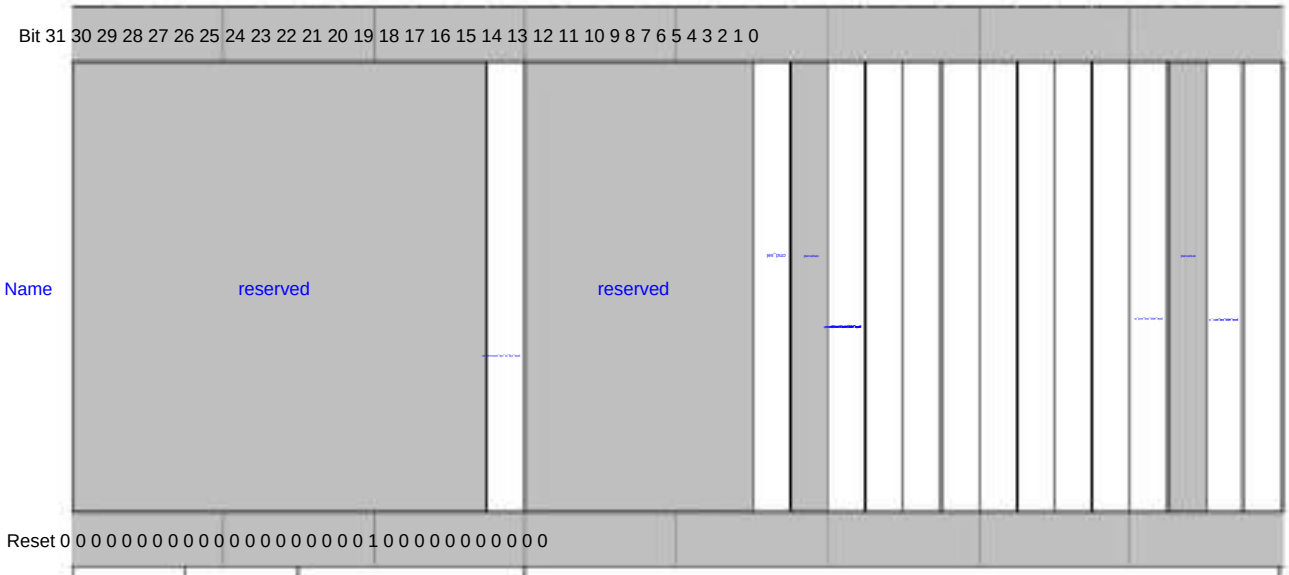
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_sys_ctrl6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	pcie_sys_ctrl6	PCIE link establishment timeout limit register.

PCIE_SYS_CTRL7

PCIE_SYS_CTRL7 is PCIE control register 7.

Offset Address	Register Name	Total Reset Value
0x101C	PCIE_SYS_CTRL7	0x0000_2800



Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20]	RW	state. pcie_cfg_l1_clk_re state; move_en	Reference clock control in L1 0: disable reference clock removal in L1 1: Allow reference clock removal in L1 state.
[19:14]	RO	reserved	reserve.
[13]	RW	cmd_sel	PCIe register access enable. 0: Local CPU cannot access PCIe registers; 1: Local CPU can access PCIe registers.
[12]	RO	reserved	reserve.
[11]	RW	pcie_app_ltssm_en 0:	PCIe controller enable. disable PCIe controller; able 1: Enable PCIe controller.
[10]	RW	detection. present; det	PCIe controller auxiliary power pcie_sys_aux_pwr_0: auxiliary power not 1: Auxiliary power is present.
[9]	RW	state. pcie_apps_pm_xmt up; _pme	PCIe controller wake-up from low-power 0: do not wake 1: Wake up.

[8] RW		request. pcie_apps_pm_xmt request; _turnoff	PCIe controller PM_TRUN_OFF message 0: no 1: request.
[7] RW		pcie_app_unlock_msg	PCIe controller Unlock message request. 0: no request; 1: request.
[6] RW		state. pcie_outband_pwru up; p_cmd	PCIe controller wake-up from low-power 0: do not wake 1: Wake up.
[5] RW	pcie_sys_int		PCIe controller interrupt request. When the value of this register changes from 0 to 1, the PCIe controller generates an Assert_INTx message; when the value of this register changes from 1 to 0, the PCIe controller generates a Deassert_INTx message.
[4] RW		configuration requests. pcie_app_req_retry 0: void; _en	The PCIe controller defers receiving 1: Valid.
[3] RW		L1 state. pcie_app_req_exit	The PCIe controller application layer requests to exit the 0: no request; l1 1: request.
[2]	RO	reserved	reserve.
[1] RW		the L1 state. pcie_app_req_entr_ request; l1	The PCIe controller application layer requests to enter 0: no 1: request.
[0] RW	pcie_app_init_rst		Changing the value of this register from 0 to 1 will cause the PCIe controller to send a HOT_RESET to the downstream device.

PERI_PCIE_STAT0

PERI_PCIE_STAT0 is the PCIE status register 0.

Offset Address	Register Name	Total Reset Value
0x1100	PERI_PCIE_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RO	pcie_xmlh_link_up	PCIe PHY link connection status. 0: the connection is disconnected; 1: Connection established.
[14:6]	RO	reserved	reserve.
[5]	RO	pcie_rdlh_link_up	PCIe controller data link layer connection status indication. 0: the connection is disconnected; 1: Connection established.
[4:0]	RO	reserved	reserve.

12.9 USB 2.0

12.9.1 Overview

USB 2.0 Host controller supports High-speed (480Mbit/s), Full-speed (12Mbit/s) and Low speed (1.5Mbit/s) three kinds of data transmission. The USB 2.0 Host Controller supports USB 2.0, OHCI Rev 1.0a and EHCI Rev 1.0 protocols. The USB 2.0 Host controller contains a Root Hub (a part of the USB system, through which the USB interface can be extended). The features of the USB 2.0 Host controller are as follows:

- Complete control and processing of transmissions
- Parsing and packaging of data packets
- The encoding and decoding of USB transmission
- signals provide the driver with interfaces such as interrupt vectors

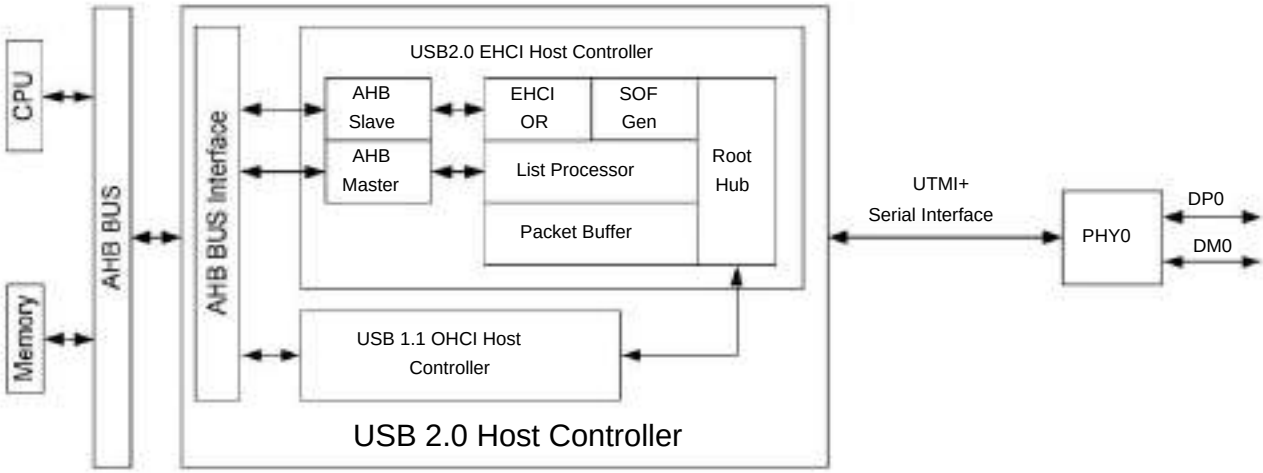
The USB 2.0 Device controller supports High-speed (480Mbit/s) and Full-speed (12Mbit/s) data transmission. Support host/device intelligent switching.

12.9.2 Functional description

Logic block diagram

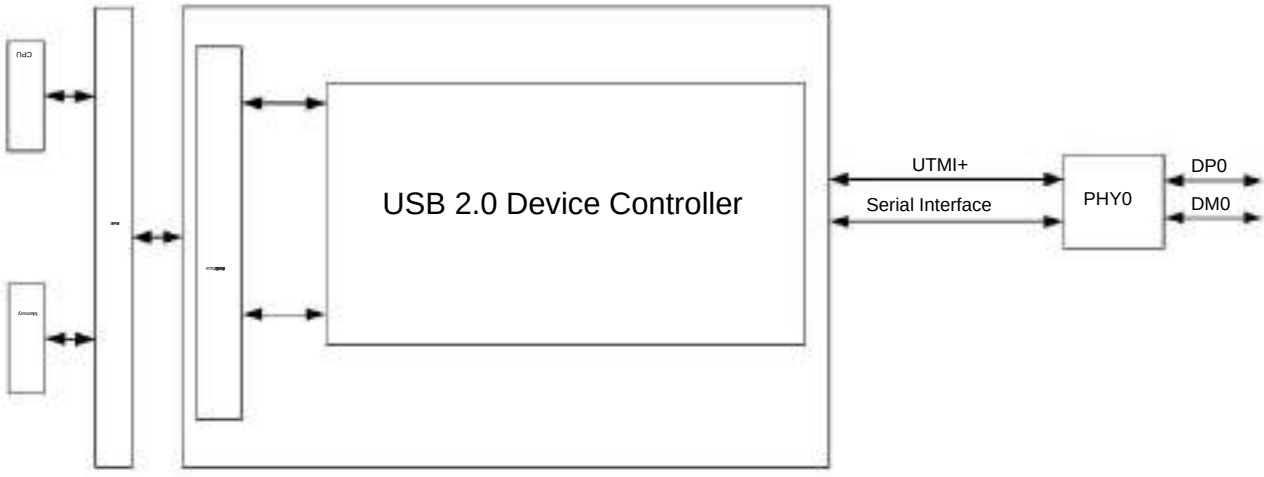
The logic block diagram of USB 2.0 Host is shown in Figure 12-61 .

Figure 12-61 USB 2.0 Host logic block diagram



The logic block diagram of USB 2.0 Device is shown in Figure 12-62 .

Figure 12-62 Logical block diagram of USB 2.0 Device



UTMIÿUSB2.0 Transceiver Macrocell Interface
EHCIÿEnhanced Host Controller Interface
OHCIÿOpen Host Controller Interface

typical application

The reference design of USB 2.0 Host is shown in Figure 12-63 .

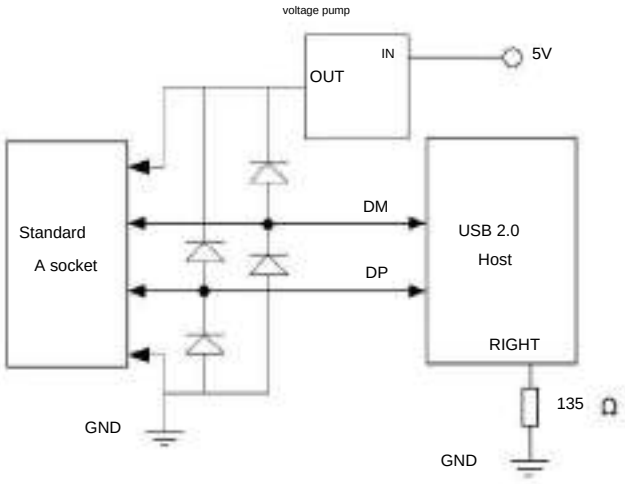
注意

The single-ended impedance of DP and DM is 45ÿ±1%, so DP and DM do not need any external matching resistors.

The accuracy of the REXT resistor is ±1%.

Need to use high-speed ESD devices, the recommended capacitance value is about 1pF.

Figure 12-63 USB 2.0 Host reference design



Features

USB 2.0 Host has the following features:

Fully compatible with USB 2.0.

Fully compliant with OHCI Rev 1.0a, EHCI Rev 1.0. Can support High-speed, Full-speed, Low-speed three devices. Supports low power solutions. Supports four basic data transfer types: Control Transfer, Bulk Transfer, Isochronous Transfer, and Interrupt Transfer. Up to 127 devices can be connected by connecting the USB Hub.

USB 2.0 Device has the following features:

Fully compatible with USB 2.0.

Both High-speed and Full-speed devices can be supported.

Supports four basic data transfer types: Control Transfer, Bulk Transfer, Isochronous Transfer, and Interrupt Transfer.

working principle

USB 2.0 Host supports the following four standard transmission methods:

Control Transfer (control transfer) is

mainly used for the transfer between USB Host and USB Device endpoint 0, and the control transfer of certain types of USB devices may use other endpoints. Control transmission is two-way transmission, the amount of data is usually small, can transmit 8byte, 16byte, 32byte or 64byte of data, depending on the device and transmission speed.

Bulk Transfer

It is mainly used to send and receive a large amount of data without bandwidth and interval time requirements. This type of device is suitable for transmitting very slow and a large amount of delayed data. It can wait until all other types of data transmission is completed before sending and receiving. Receive data. It is characterized by error detection and retransmission to ensure error-free data transmission between USB Host and USB Device.

Isochronous Transfer (synchronous transfer) is

mainly used for time-critical and fault-tolerant data transfer, or for real-time applications with constant data transfer rate. Isochronous transmission provides deterministic bandwidth and interval time.

Interrupt Transfer (interrupt transfer) is mainly

used for the transmission of small amount, scattered and unpredictable data. In the interrupt transmission mode, periodically check whether the device has interrupt data to send. The structure of the endpoint mode device of the device determines its query frequency is 1ms ~ 255ms. Typical interrupt mode transmission is unidirectional, and there is only input mode for USB Host.

12.9.3 Working method

Host/Device switching

It can be set to work in Host mode or Device mode by configuring the system control register MISC_CTRL30[usb2_chipid].

If working in Device mode, set MISC_CTRL30[usb2_chipid] to 0, MISC_CTRL30[usb2_phy_dmpulldown] to 1, and MISC_CTRL30[usb2_phy_dppulldown] to 1.

If working in DEVICE mode, configure MISC_CTRL30[usb2_chipid] as 1, MISC_CTRL30[usb2_phy_dmpulldown] as 0, MISC_CTRL30[usb2_phy_dppulldown] as 0.

Pin Polarity Control

The effective polarity of USB PHY power shutdown can be set by setting the system control register MISC_CTRL30 [usbpwr_pctrl]; the effective polarity of USB overcurrent protection can be set by setting the system control register MISC_CTRL30 [usbovr_p_ctrl].

clock gating

When the USB 2.0 Host is not in use, the clock of the USB 2.0 Host can be turned off to reduce power consumption.

The procedure for shutting down the clock is as follows:

Step 1. Send to PERI_CRG45 [usb_phy_port0_treq], PERI_CRG45[usb_phy_req], PERI_CRG45[usb_ctrl_utmi0_req]ÿPERI_CRG45[usb2_device_ctrl_srst_req]ÿ
Write 1 to PERI_CRG45[usb_hrst_req] to reset the USB controller and PHY;

Step 2. Set the system controller PERI_CRG45[usb_cken] to 0, and turn off the clocks related to the USB 2.0 Host.

----Finish

The steps to turn on the clock are as follows:

Step 1. Set the PERI_CRG45 [usb_cken] of the system controller to 1, and turn on the clock related to the USB 2.0 Host;

Step 2. Undo the reset of the USB controller and PHY, see "Undoing Reset" for details.

----Finish

undo reset

The USB controller and PHY are in the reset state by default after power-on, and the steps to cancel the reset are as follows:

Step 1. Delay at least 10us;

Step 2. Write 0 to PERI_CRG45[usb_phy_req] to cancel the POR (Power On Reset) reset of USB PHY;

Step 3. Delay at least 1ms, write 0 to PERI_CRG45[usb_phy_port0_treq], cancel USB PHY port0 port soft reset;

Step 4. After a delay of at least 100us, send to PERI_CRG45[usb_ctrl_utmi0_req],
Write 0 to PERI_CRG45[usb2_device_ctrl_srst_req] and PERI_CRG45[usb_hrst_req] to cancel the port0 soft reset of the USB Host controller, the soft reset of the USB Device controller, and the soft reset of the USB bus side.

----Finish

Reset port individually during work

The steps to reset port individually during work are as follows:

Step 1. Write 1 to PERI_CRG45[usb_ctrl_utmi0_req], PERI_CRG45[usb2_device_ctrl_srst_req] to soft reset port0 of the USB controller;

Step 2. Write 1 to PERI_CRG45[usb_phy_port0_treq] to soft reset the port0 port of USB PHY;

Step 3. After a delay of at least 100us, write 0 to PERI_CRG45[usb_phy_port0_treq] to cancel USB PHY port0 port reset;

Step 4. Write 0 to PERI_CRG45[usb_ctrl_utmi0_req], PERI_CRG45[usb_device_ctrl_srst_req], undo Port0 of the USB controller is reset.

----Finish

USB 2.0 Register Offset Address Variable Table

Table 12-34 shows the value range and meaning of the variables in the register offset address of each module .

Table 12-34 Register offset address variable table of each module

variable name	Ranges	describe
FIFO_num	0ÿ14	Number of FIFOs
n	0ÿ15	nth endpoint

12.9.4 USB 2.0 Register Overview

USB HOST Register Overview

An overview of the USB 2.0 registers is shown in Table 12-35 .

Table 12-35 USB 2.0 Register Overview (Base Address: 0x1012_0000)

offset address	name	describe	page number
0x90	INTNREG00	Configure Microframe Length Register	12-219
0x94	INSNREG01	Configure PBUF OUT/IN Register	12-220
0x98	INSNREG02	Configure PBUF Depth Register	12-220
0x9C	INSNREG03	Interrupt memory transfer enable register	12-221
0xA0	INTNREG04	DEBUG register	12-222
0xA4	INTNREG05	UTMI Vendor Control and Status Register	12-223
0xA8	INTNREG06	AHB Error Status Register	12-223
0xAC	INTNREG07	AHB Error Address Register	12-224

Note: The base address of the EHCI register is 0x1012_0000, the base address of the OHCI register is 0x1011_0000, and the base address of the register in Table 12-35 is the base address of the EHCI register.

USB Device Register Overview

An overview of the USB Device registers is shown in Table 12-36 .

Table 12-36 USB Device register overview (base address is 0x1013_0000)

offset address name		describe	page number
0x0000	GOTGCTL	Device Behavior Control and Status Query Register 12-224	

offset address name		describe	page number
0x0004	GOTGINT	Device interrupt occurrence indication/clear register	12-227
0x0008	GAHBCFG	AHB configuration register	12-228
0x000C	GUSBCFG	USB configuration register	12-230
0x0010	GRSTCTL	Reset hardware feature register	12-233
0x0014	GINTSTS	System Interrupt Register	12-237
0x0018	GINTMSK	System Interrupt Mask Register	12-240
0x001C	GRXSTSR	Receive status debug read register	12-244
0x0020	GRXSTSP	Receive status read&pop register	12-244
0x0024	WITHOUT GRXF	Receive FIFO size configuration register	12-245
0x0028	WITHOUT GNPTXF	Non-Periodic Transmit FIFO Size Configuration Register	12-246
0x002C	GNPTXSTS	Non-periodic TxFIFO ÿ the Nonperiodic Transmit Request Queue information query register	12-246
0x0030	GI2CCTL	I2C Access Registers	12-248
0x0034	GPVNDCTL	PHY Vendor Control Registers	12-249
0x0038	GGPIO	General purpose input/output registers	12-250
0x003C	GUID	User ID Lookup Register	12-250
0x0040	GSNPSID	Synopsys ID Lookup Register	12-251
0x0044	GHWCFG1	User Hardware Configuration Register 1	12-251
0x0048	GHWCFG2 User hardware configuration register 2		12-252
0x004C	GHWCFG3	User Hardware Configuration Register 3	12-254
0x0050	GHWCFG4 User hardware configuration register 4		12-255
0x0054	GLPMCFG	LPM configuration register	12-257
0x0058	GPWRDN	power down register	12-260
0x005C	GDFIFOCFG	DFIFO software configuration register	12-264
0x0060	GADPCTL	ADP's Timers, Control and Status Register 12-264	
0x0100	WITHOUT HPTXF	TxFIFO configuration register	12-267
0x0104ÿ 0x0004× FIFO_num	DPTXFSIZN	Device Periodic Transmit FIFO-n Size Register	12-267

offset address name		describe	page number
0x0104ÿ 0x0004× FIFO_num	DIEPTXFN	Device IN Endpoint Transmit FIFO Size Register	12-268
0x0800	DCFG	Device configuration register	12-268
0x0804	DCTL	Device Control Register	12-269
0x0808	STD	Device status query register	12-271
0x0810	DIEPMSK	Device IN Endpoint common Interrupt Mask Register	12-272
0x0814	DOEPMSK	Device OUT Endpoint Common Interrupt Mask Register	12-273
0x0818	TEETH	Device All Endpoint Interrupt Registers	12-275
0x081C	DAINTMSK All Endpoint interrupt mask registers		12-276
0x0820	DTKNQR1	Device IN Token Sequence Learning Queue read register 1	12-276
0x0824	DTKNQR2	Device IN Token Sequence Learning Queue read register 2	12-277
0x0830	DTKNQR3	Device IN Token Sequence Learning Queue read register 3	12-277
0x0834	DTKNQR4	Device IN Token Sequence Learning Queue read register 4	12-278
0x0828	DVBUSDIS	Device VBUS discharge time register	12-278
0x082C	DVBUSPULSE Device VBUS pulsing time register		12-279
0x0830	DTHRCTL	device waterline control register	12-279
0x0834	DIEPEMPMSK Device IN Endpoint FIFO Empty Interrupt Mask Register		12-280
0x0838	DEACHINT	Device Each Endpoint Interrupt Register	12-281
0x083C	DEACHINTMSK Device Each Endpoint Interrupt Mask Register 12-281		
0x0840ÿ (0x0004×n)	DIEPEACHMSK N	device each in Endpoint-n Interrupt Register 12-282	
0x0880ÿ (0x0004×n)	DOEPEACHMSK N	device each out Endpoint-n Interrupt Register 12-284	
0x0900	THEPCTL0	Device Control IN Endpoint 0 Control Register	12-285

offset address	name	describe	page number
0x0B00	DOEPCTL0	Device Control OUT Endpoint 0 Control Register	12-287
0x0900ÿ (0x0020×n)	DEEPCTLN	Device IN Endpoint-n Control Register	12-289
0x0B00ÿ (0x0020×n)	DOEPCTLN	Device OUT Endpoint-n Control Register 12-292	
0x0908ÿ (0x0020×n)	DIEPINTn	Device IN Endpoint-n Interrupt Register	12-295
0x0B08ÿ (0x0020×n)	DOEPINTn	Device OUT Endpoint-n Interrupt Register 12-298	
0x0910	DIEPTSIZ0	Device IN Endpoint 0 Transfer Size Register 12-300	
0x0B10	DOEPTSIZ0	Device OUT Endpoint 0 Transfer Size Register 12-300	
0x0910ÿ (0x0020×n)	DIEPTSIZn	Device IN Endpoint-n transfer size register 12-301	
0x0B10ÿ (0x0020×n)	DOEPTSIZn	Device OUT Endpoint-n Transfer Size Register 12-302	
0x0914ÿ (0x0020×n)	DIEPDMAN	Device IN Endpoint-n DMA Address Register 12-303	
0x0B14ÿ (0x0020×n)	DOEPDMAN	Device OUT Endpoint-n DMA address register	12-303
0x091Cÿ (0x0020×n)	DIEPDMABN	Device IN Endpoint-n DMA buffer address register	12-304
0x0B1Cÿ (0x0020×n)	DOEPDMABN	Device OUT Endpoint-n DMA buffer ÿÿ register	12-304
0x0938	DTXFSTSn	Device IN Endpoint Transmit FIFO Status Register	12-305

12.9.5 USB 2.0 Register Description

12.9.5.1 USB HOST register description

INTNREG00

INTNREG00 is the configuration microframe length register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														val	in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	reserve.
[13:1]	RW	val	Microframe counter value. This register is for emulation only. During normal operation, the microframe length is 125μs specified in the protocol; during simulation, in order to shorten the simulation time, this register can be configured to change the microframe length as required.
[0]	RW	and	Enables the microframe length register. 0: forbidden; 1: enable.

INSNREG01

INSNREG01 is the configuration PBUF OUT/IN register.

Offset Address	Register Name	Total Reset Value
0x94	INSNREG01	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_threshold																in_threshold															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	out_threshold	Send waterline. When sending data, when the data in PBUF exceeds the sending watermark, start sending data. The unit is 32bit.
[15:0]	RW	in_threshold	Receive waterline. When receiving data, when the data in PBUF exceeds the receive watermark, read the data from PBUF. The unit is 32bit.

INSNREG02

INSNREG02 is the configuration PBUF depth register.

Offset Address	Register Name	Total Reset Value
0x98	INSNREG02	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pbuf_depth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RW	pbuf_depth	PBUF depth. The unit is 32bit.

INSNREG03

INSNREG03 is the interrupt memory transfer enable register.

Offset Address	Register Name	Total Reset Value
0x9C	INSNREG03	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		dis	ctrl	val						offset					brk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14]	RW	dis	256MHz clock check enable 0: disable; 1: enable.
[13]	RW	ctrl	Line state is ignored during TESTSE0 NAK. 0: forbidden; 1: enable.
[12:10]	RW	val	tx-tx turnaround delay append.
[9]	RW	fetch	Periodic frame list fetch instruction, only valid in CONFIG1 mode. 0: The controller fetches instructions from the periodic linked list only at microframe 0; 1: The controller fetches instructions from the periodic linked list every microframe.
[8:1]	RW	offset	Available time offset.

[0]	RO	brk_en	Interrupt memory transfer enable. 0: forbidden; 1: enable.

INTNREG04

INTNREG04 is the DEBUG register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name reserved

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:6]	RO	reserved	reserve.
[5]	RW	auto_en	Auto specification enabled. 0: enable (the suspend signal is valid when the software resets run/stop, but the hchalted bit is not set); 1: Disabled (that is, the port does not hang when software clears the run/stop bit). The default is 0.
[4]	RW	nak_reldfix_en	NAK reload enable. 0: enable; 1: Prohibited.
[3]	RO	reserved	reserve.
[2]	RW	time. scaledwn_enum_ti me	Reduce port enumeration 0: disabled; 1: enable.
[1]	RW	hccparam_en	HCCPARAMS register writable enable. 0: forbidden; 1: enable.

[0] RW	hcsparam_en		HCSPARAMS register writable enable. 0: forbidden; 1: enable.

INTNREG05

INTNREG05 is a UTMI Vendor control and status register, used to read and write UTMI PHY registers.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12	11 10 9 8 7 6 5 4	3 2 1 0
Name	reserved	vport	vcontrol_loadm	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1	0	0 0 0 0 0 0 0 0	0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RO	vbusy	"1" indicates that the hardware is currently performing a data write operation, and only when the process ends, this bit is cleared.
[16:13]	RW	vport	The port number, which cannot exceed the number of supported ports.
[12]	RW	vcontrol_loadm	Load enable. 0: enable; 1: Prohibited.
[11:0]	RO	reserved	reserve.

INTNREG06

INTNREG06 is the AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	reserved																							hbusrt_err				num_beat_err			num_beat_ok	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31]	RW err_capture	An AHB error has occurred.
[30:12]	RO reserved	reserve.
[11:9]	RO hbusrt_err	Controls the transfer phase hburst value when an AHB error occurs.
[8:4]	RO num_beat_err	The number of beats for this burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00~0x10: valid; 0x11~0x1F: Reserved.
[3:0]	RO num_beat_ok	The number of beats that have been successfully completed in this burst transfer when an AHB error occurs.

INTNREG07

INTNREG07 is the AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

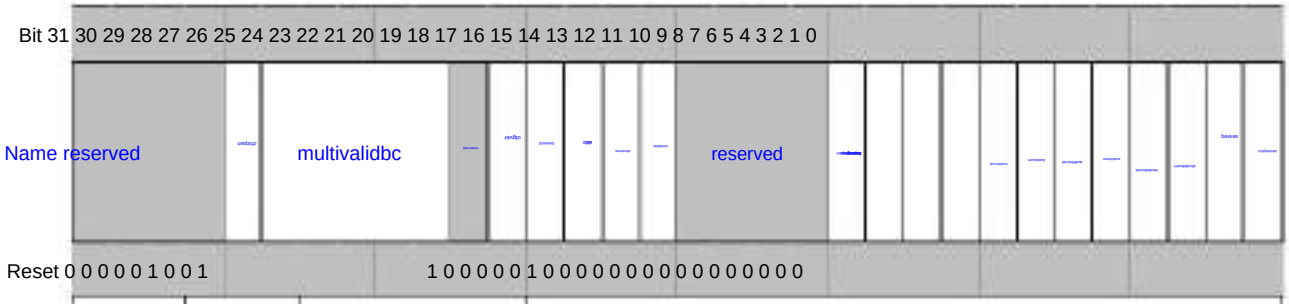
Bits	Access Name	Description
[31:0]	RO err_addr	Address of the control transfer phase when an AHB error occurs.

12.9.5.2 USB Device Register Description

GOTGCTL

GOTGCTL is the device behavior control and status query register.

Offset Address	Register Name	Total Reset Value
0x0000	GOTGCTL	0x04C1_0000



Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.
[27]	RW	chirpen	Chirp On enabled. 0: forbidden; 1: enable. Note: This bit is only valid when OTG_BC_SUPPORT=1, if OTG_BC_SUPPORT is not equal to 1, this bit is reserved.
[26:22]	RO	multivalidbc	The BC ACA is entered as follows: Bit[26]ÿrid_floatÿ Bit[25]ÿrid_gndÿ Bit[24]ÿrid_aÿ Bit[23]ÿrid_bÿ Bit[22]ÿrid_cÿ
[21]	RO	reserved	reserve.
[20]	RW	otgver	Device version ID. 0: Device version 1.3; 1: Device version 2.0.
[19]	RO	bsesvld	Transceiver status indication under Device Mode. 0: B-session is invalid; 1: B-session is valid.
[18]	RO	vice vld	Transceiver status indication under Host Mode. 0: A-session is invalid; 1: A-session is valid.
[17]	RO	dbnctime	Debounce time indication. 0: long debounce time; 1: Short debounce time.

[16] RO		conidsts	USB_ID status. 0: Device works in A-Device mode; 1: Device works in B-Device mode.
[15:12] RO		reserved	reserve.
[11] RW	devhnpen		Device HNP enabled. 0: forbidden; 1: enable.
[10] RW	hstsethnpen		Host HNP enabled. 0: forbidden; 1: enable.
[9] RW	hnpreq		HNP request. 0: no request; 1: request.
[8]	RO	hstnegscs	Host Negotiation instructions. 0: Host Negotiation failed; 1: Host Negotiation succeeded.
[7] RW	bvalidovval		Bvalid setting. 0ÿBvalid = 0ÿ 1ÿBvalid = 1ÿ When GOTGCTL.BvalidOvEn =1, this bit is valid.
[6] RW	bvalidoven		Bvalid signal override assignment enable/disable. 0: Bvalid can be overwritten; 1: Bvalid cannot be overwritten.
[5] RW	avalidovval		Avalid setting. 0ÿAvalid = 0ÿ 1ÿAvalid = 1ÿ When GOTGCTL.AvalidOvEn = 1, this bit is valid.
[4] RW	avalidoven		Avalid signal override assignment enable/disable. 0: Avalid can be overwritten; 1: Avalid cannot be overwritten.
[3] RW	vbvalidovval		vbusvalid signal setting. 0ÿvbusvalid = 0ÿ 1ÿvbusvalid = 1ÿ This is valid when GOTGCTL.VbvalidOvEn = 1.

[2] RW vbvalidoven			vbusvalid signal override assignment enable/disable. 0: vbusvalid can be overridden; 1: vbusvalid cannot be overridden.
[1] RW sesreq			session request. 0: no request; 1: request.
[0]	RO	sesreqscs	session request status indication. 0: session request failed; 1: The session request is successful.

GOTGINT

GOTGINT is the device interrupt indication/cancellation register.

Offset Address	Register Name	Total Reset Value
0x0004	GOTGINT	0x0000_0000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name	reserved				reserved		reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0								

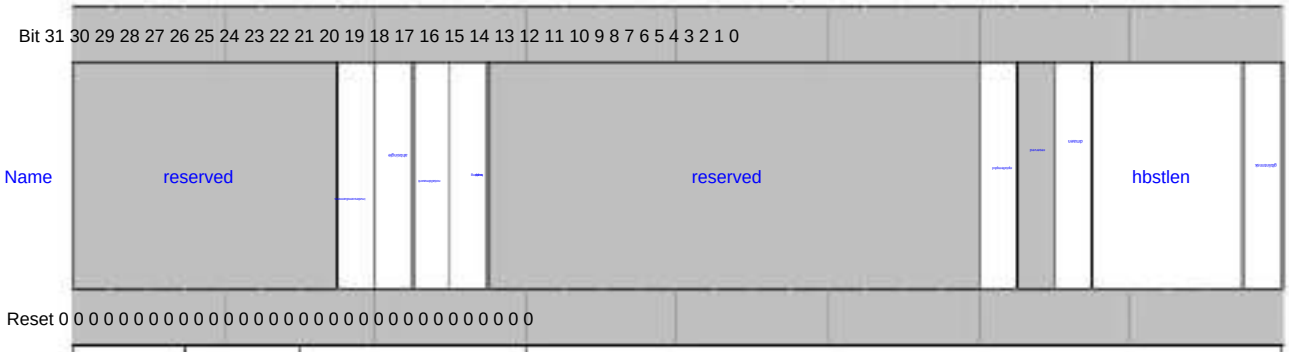
Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20]	RO	multivalipchng	When the value of at least one ACA pin changes, an interrupt occurs, and the interrupt is cleared by setting 1. This bit is valid only when OTG_BC_SUPPORT=1.
[19]	RO	dbncedone	An interrupt occurs when the debounce is successful, and the interrupt is cleared by setting 1. This bit is valid only when HNP Capable or SRP Capable is set to 1.
[18]	RO	adevtoutchg	waits for the B-device connection timeout interrupt, set 1 to clear the interrupt.
[17]	RO	hstnegdet	Interrupt occurs when Host Negotiation is detected, set to 1 to clear the interrupt.
[16:10]	RO	reserved	reserve.
[9]	RO	hstnegsucstschng	When an interrupt occurs when the Host Negotiation request succeeds or fails, set 1 to clear it.

[8]	RO	sesreqsucstschng	Interrupt occurs when the Session request succeeds or fails, set 1 to clear the interrupt.
[7:3] RO		reserved	reserve.
[2]	RO	seen sent	Interrupt occurs when utmiotg_bvalid is deasserted, set 1 to clear the interrupt.
[1:0] RO		reserved	reserve.

GAHBCFG

GAHBCFG is the AHB configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	GAHBCFG	0x0000_0000



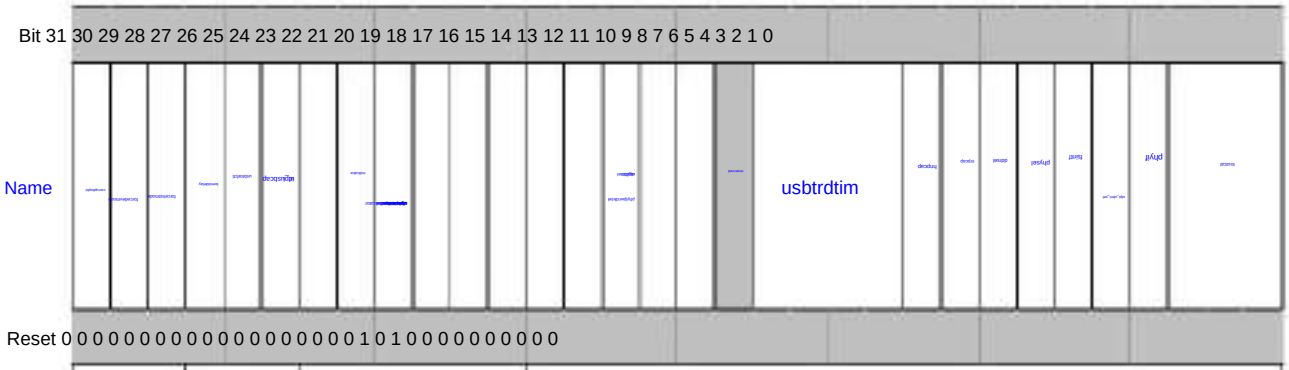
Bits	Access Name		Description
[31:25] RO		reserved	reserve.
[24] RW	invdescendianness		The Descriptor byte is negated. 0: Descriptor byte order is similar to AHB master byte order; 1: When AHB master byte order is Big Endian, Descriptor byte order is Little Endian. When the byte order of AHB master is Little Endian, the byte order of Descriptor is Big Endian.
[23] RW	ahbsingle		During a transfer in DMA mode. 0: The remaining data is transmitted with INCR burst size; 1: The remaining data is transmitted using Single burst size.
[22] RW	notialldmawrit		Notify all DMA write operations, this bit is only valid when GAHBCFG.RemMemSupp is 1.

[21] RW	remmemsupp		Remote memory support. 0: The int_dma_req signal and int_dma_done signal will not be set, the controller core will process the XferComp interrupt immediately after the DMA write operation is completed; 1: When the HSOTG DMA starts to write data to the external memory, the int_dma_req will be set, and then when the controller The core completes the transfer and sets int_dma_done to indicate that the write operation through HSOTG has been completed. At this time, the controller core waits for the sys_dma_done signal given by the system to be valid, and then proceeds to the next step of DMA transmission.
[20:8]	RO	reserved	reserve.
[7] RW	nptxfemplvl		Aperiodic TxFIFO empty state level. 0: TxFEmp interrupt indicates that the TxFIFO status of the IN endpoint is half empty; 1: TxFEmp interrupt indicates that the TxFIFO status of the IN endpoint is completely empty.
[6]	RO	reserved	reserve.
[5] RW	dmaen		DMA mode enabled. 0: core works in Slave mode; 1: core works in DMA mode.
[4:1] RW	hbstlen		Burst length/type, available in both external and internal DMA modes. External DMA mode: 0x0ÿ1 wordÿ 0x1ÿ4 wordsÿ 0x2ÿ8 wordsÿ 0x3ÿ16 wordsÿ 0x4ÿ32 wordsÿ 0x5ÿ64 wordsÿ 0x6ÿ128 wordsÿ 0x7ÿ256 wordsÿ Other: reserved. Internal DMA mode: 0x0ÿSingleÿ 0x1ÿINCRÿ 0x3ÿINCR4ÿ 0x5ÿINCR8ÿ 0x7ÿINCR16ÿ Other: reserved.
[0] RW	glblintrmsk		Global interrupt mask. 0: Shield; 1: No shielding.

GUSBCFG

GUSBCFG is the USB configuration register.

Offset Address: 0x000C
Register Name: GUSBCFG
Total Reset Value: 0x0000_1400



Bits	Access	Name	Description
[31]	WO	corrupttxpkt	Unexpected tx package. For debug only, this bit is always set to 0.
[30]	RW	forcedevmode	Force Device mode. 0: normal mode; 1: Forcibly set to Device mode.
[29]	RW	forcehstmode	Force Host mode. 0: normal mode; 1: Forcibly set to Host mode.
[28]	RW	txenddelay	Tx end delay enable. 0: forbidden; 1: enable.
[27]	RW	usbtrafctl	USB pull-up resistor control (traffic signaling). 0: The pull-up and pull-down resistors are attached; 1: The pull-up and pull-down resistors are detached. Notice: This bit is valid only when OTG_ENABLE_IC_USB=1 and USBCFG.IC_USBCap = 1.
[26]	RO	ic_usbcap	IC_USB enable control. 0: IC_USB PHY interface is not selected; 1: IC_USB PHY interface is selected.

[25] RW ulpi			ULPI interface protection is disabled and enabled. 0: Enable interface protection circuit; 1: Abolish the interface protection circuit.
[24] RW indicator			Indicator Pass Through. 0: The complementary output signal is determined by the internal Vbusvalid comparator; 1: The complementary output signal is not determined by the internal Vbusvalid comparator. When TG_HSPHY_INTERFACE = 1, this bit is read-only; when TG_HSPHY_INTERFACE = 0, this bit is reserved.
[23] RW complement			Indicator Complementary 0: PHY does not invert the ExternalVbusIndicator signal; 1: PHY inverts ExternalVbusIndicator signal.
[22] RW termseldlpulse			Row pulse drive in SRP. 0: utmi_txvalid drives line pulses; 1: utmi_termsel drives line pulses.
[21] RW		ulpiextvbusindicato r	1: PHY uses external VBUS valid comparator. This bit is valid only when OTG_HSPHY_INTERFACE = 2 or 3.
[20] RW ulpiextvbusdrv			ULPI external VBUS driver. 0: PHY uses internal charge pump to drive VBUS; 1: PHY uses external power to drive VBUS. Note: This bit is valid only when OTG_HSPHY_INTERFACE = 2 or 3.
[19] RW ulpiclksusm			ULPI clock suspend. 0: PHY turns off internal clock when suspend; 1: PHY doesn't turn off internal clock when suspend. Notice: This bit is valid only when OTG_HSPHY_INTERFACE = 2 or 3.
[18] RW ulpiautores			ULPI automatically recovers. 0: PHY does not use the auto-recovery feature; 1: The PHY uses the auto-recovery feature. Note: This bit is only valid when OTG_HSPHY_INTERFACE=2 or 3.

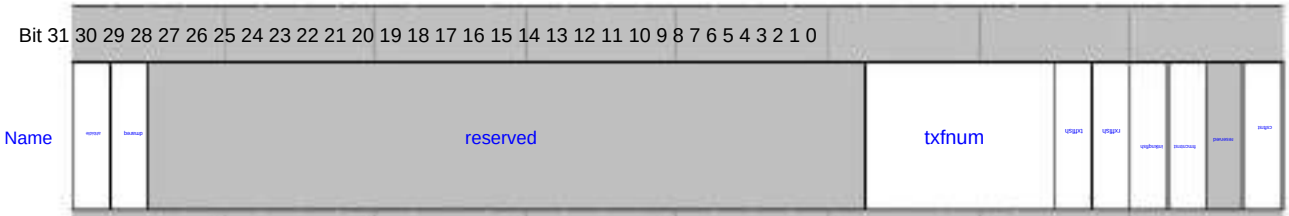
[17] RW	ulpifsls		ULPI FS/LS selection. 0: ULPI interface; 1: ULPI FS/LS serial interface. Notice: Setting this bit needs to ensure that GUSBCFG.ULPI_UTMI_SEL=1.
[16] RW	otgi2csel		UTMI or I2C interface selection. 0: UTMI USB1.1 full speed interface; 1: I2C interface. Note: This bit is only valid when OTG_I2C_INTERFACE=2, reading this bit will return 0.
[15] RW	phylpwrclksel		PHY low power clock selection. 0: 480-MHz internal PLL clock; 1: 48-MHz external clock.
[14] RO		reserved	reserve.
[13:10] RW	usbtrdtim		USB Turnaround time. 0101: When the MAC interface is 16bit UTMI+; 1001: When the MAC interface is 8bit UTMI+; Other: reserved.
[9] RW	hnpcap		HNP enabled. 0: disable; 1: enable.
[8] RW	srpcap		SRP is enabled. 0: forbidden; 1: enable.
[7] RW	ddrsel		ULPI DDR selection. 0: Odd rate ULPI interface; 1: Even rate ULPI interface. This bit is valid only when OTG_HSPHY_INTERFACE=2 or 3.

[6] RW physel			USB2.0 high-speed PHY or USB1.1 full-speed serial Transceiver selection. 0: USB2.0 high-speed UTMI+ or ULPI PHY; 1: USB1.1 full speed serial Transceiver. If the USB1.1 full-speed serial Transceiver is not selected, this bit is always 0, and it is read-only. If the USB2.0 high-speed PHY is not selected, this bit is always 1, and it is read-only. If neither interface type is selected (non-zero parameter), this bit is used to select which interface is activated, and this bit is readable and writable.
[5] RW fsintf			Full-speed serial interface selection. 0: 6-pin unidirectional full-speed serial interface; 1: 3-pin bidirectional full- speed serial interface. If the USB1.1 full-speed serial Transceiver is not selected, this bit is always 0, and it is write-only. If the USB1.1 full-speed interface is selected, this bit can be used to select the 3-pin or 6-pin interface, and it is readable and writable.
[4] RW ulpi_utmi_sel			ULPI or UTMI selection. 0: UTMI+ interface; 1: ULPI interface.
[3] RW phyif			PHY interface. 0: 8 bits; 1: 16 bits.
[2:0] RW toutcal			HS/FS timeout calibration. High speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit timesÿ

GRSTCTL

GRSTCTL is the reset hardware feature register.

Offset Address	Register Name	Total Reset Value
0x0010	GRSTCTL	0x8000_0000



Bits	Access Name		Description
[31] RO		ahbidle	AHB Master Idle Indicates that the AHB Master state machine is in the IDLE state. 0: AHB Master state machine is in non-IDLE state 1: AHB Master state machine is in IDLE state
[30] RO		dmareq	DMA request signal. Indicates that a DMA request is being processed, only for debug. 0: other 1: DMA request is in progress
[29:11] RO		reserved	reserve.

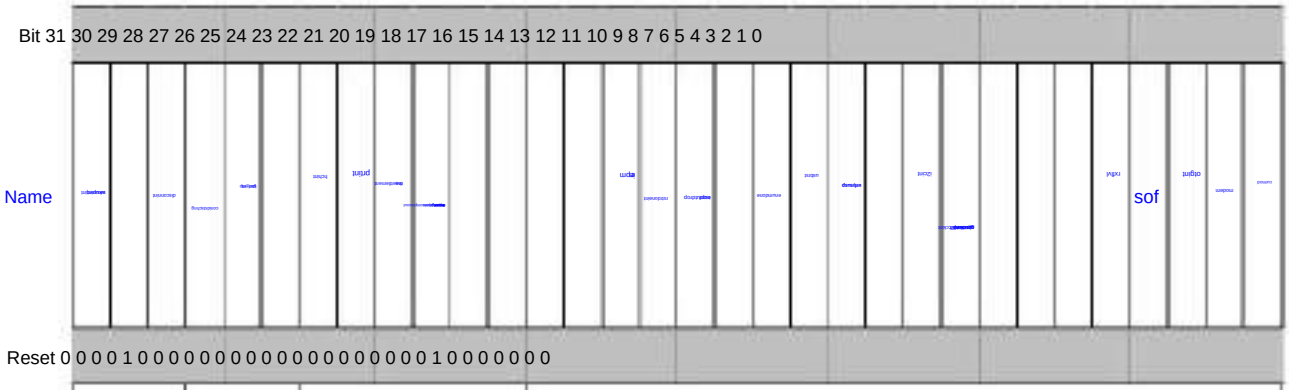
[10:6]	RW	txfnum	TxFIFO number, the FIFO number must be refreshed with the TxFIFO Flush bit, and cannot be rewritten before the controller core clears the TxFIFO Flush bit. 0x0ÿ - Periodic TxFIFO clearing in host mode; - Periodic TxFIFO clearing in device mode in shared FIFO operation; - In dedicated FIFO mode, TxFIFO 0 is cleared in device mode. 0x1ÿ - In host mode, periodic TxFIFO is cleared; - In shared FIFO operation, periodic TxFIFO 1 is cleared in device mode; - In dedicated FIFO mode, TxFIFO 1 is cleared in device mode. 0x2ÿ - In shared FIFO operation, periodic TxFIFO 2 is cleared in device mode; - In dedicated FIFO mode, TxFIFO 2 is cleared in device mode; ... 0xFÿ - In shared FIFO operation, periodic TxFIFO 15 is cleared in device mode; - In dedicated FIFO mode, TxFIFO 15 is cleared in device mode; 0x10ÿ - Clear all transmits FIFO in device mode or host mode.
[5]	R_WS_SC	txfflsh	TxFIFO cleared. This bit can choose to refresh a single or all transmit FIFOs, but it cannot be done in the middle of a transaction. The application must check that the controller core is not reading or writing the TxFIFO before writing this bit. It takes 8 clock cycles to clear this bit, during which the application must wait. 0: do not clear; 1: Clear.
[4]	RO	rxfflsh	RxFIFO is cleared, but not in the middle of a transaction. The application must check that the controller core is not reading or writing to the RxFIFO before writing this bit. It takes 8 clock cycles to clear this bit, during which the application must wait. 0: do not clear; 1: Clear.

[3]	R_WS_Sc	intknqflsh	In Token Sequence Learning Queue Cleared. This bit is only valid when OTG_EN_DED_TX_FIFO=0. 0: do not clear; 1: Clear.
[2]	RO	frmcntrrst	The Host Frame Counter is reset. This bit is used to reset the frame number counter. When the frame number counter is reset, the SOF microframe number sent next will be 0. 0: no reset; 1: Reset.
[1]	RO	reserved	reserve.
[0] RW csftrst			Kernel soft interrupt. 1) Clear all interrupt and csr registers except the following bits: - PCGCCTL.RstPdwnModule - PCGCCTL.GateHclk - PCGCCTL.PwrClmp - PCGCCTL.StopPPhyLPwrClkSelclk - GUSBCFG.PhyLPwrClkSel - GUSBCFG.DDRSel - GUSBCFG.PHYSel - GUSBCFG.FSIntf - GUSBCFG.ULPI_UTMI_Sel - GUSBCFG.PHYIf - GUSBCFG.TxEndDelay - GUSBCFG.TermSelDLPulse - GUSBCFG.ULPIClkSusM - GUSBCFG.ULPIAutoRes - GUSBCFG.ULPIFsLs - GGPIO - GPWRDN - GADPCTL - HCFG.FSLSPclkSel - DCFG.DevSpd - DCTL.SftDiscon 2) All module state machines are reset to idle state, all transmit FIFO and receive FIFO are cleared. 3) All transactions on the AHB Master are interrupted as soon as possible, and all transactions on the USB are immediately interrupted. 4) When the Hibernation or ADP feature is enabled, the PMU module will not be soft reset by the kernel.

GINTSTS

GINTSTS is the system interrupt register.

Offset Address: 0x0014
Register Name: GINTSTS
Total Reset Value: 0x0800_0080



Bits	Access	Name	Description
[31]	RWSC	wkupint	Recovery/wake-up detection interrupt, set to clear the interrupt.
[30]	RWSC	sessreqint	In Host mode, an interrupt occurs when a device session request is detected. In Device mode, an interrupt occurs when utmisrp_bvalid is 1. One in this bit position clears the interrupt.
[29]	RWSC	disconnint	An interrupt occurs when a device disconnection is detected. One in this bit position clears the interrupt.
[28]	RWSC	conference	Interrupt occurs when slot ID state changes. One in this bit position clears the interrupt.
[27]	RWSC	lpm_int	In DEVICE mode, an interrupt occurs when the device receives an LPM transaction and responds without error. In HOST mode, an interrupt occurs when the device receives an LPM transaction and responds with no errors, or when the host core completes the number of LPM transaction subscriptions. Note: This bit is only valid when LPMCapable is 1 or OTG_ENABLE_LPM is 1. Setting this bit position clears the interrupt.
[26]	RO	ptxfemp	Interrupt occurs when the Periodic Transmit FIFO is full or half empty.
[25]	RO	hchint	Indicates that in HOST mode, a channel of the kernel issued an interrupt. This bit elimination requires elimination of the associated status bits.

[24] RO		prtint	In HOST mode, an interrupt occurs when the port state of a certain port of DWC_otg core changes. Notice: This bit elimination needs to eliminate the relevant bits in the Host Port Control and Status register.
[23] RWSC	resetdet		In DEVICE mode, when the device is suspended, an interrupt occurs when the USB is detected to reset in power down mode, and in host mode, this interrupt will not occur. Note: A 1 in this bit clears the interrupt.
[22] RWSC	fetsusp		This interrupt is only valid in DMA mode. This interrupt tells the core to stop fetching data from the IN endpoint.
[21] RWSC	incomplpin	OUT Transfer	In HOST mode, an interrupt occurs when an outstanding transaction is still pending. In DEVICE mode, an interrupt occurs when there is an outstanding isochronous compiso. out Note: One bit in this bit clears the interrupt.
[20] RWSC	incompisoin		Interrupt occurs when there is an outstanding Isochronous IN Transfer. This interrupt does not occur in Scatter/Gather DMA mode. Note: A 1 in this bit clears the interrupt.
[19] RO		oepint	Indicates that in DEVICE mode, an interrupt occurs on an OUT terminal. Clearing this interrupt requires clearing the associated status bit in the DOEPINTn register.
[18] RO		iepint	Indicates that in DEVICE mode, an interrupt occurs at an IN terminal. Clearing this interrupt requires clearing the associated status bit in the DOEPINTn register.
[17] RO		in epm	An interrupt occurs when the endpoint does not match, this bit is only valid when the shared FIFO operates. Notice: Setting this bit position clears the interrupt.
[16] RWSC	rstrdoneint		Instructs Hibernation that a restore command after completion caused an interruption. Notice: This bit is only valid when the hibernation feature is enabled.
[15] RWSC	eopf		Periodic Frame end interrupt. Setting this bit position clears the interrupt.

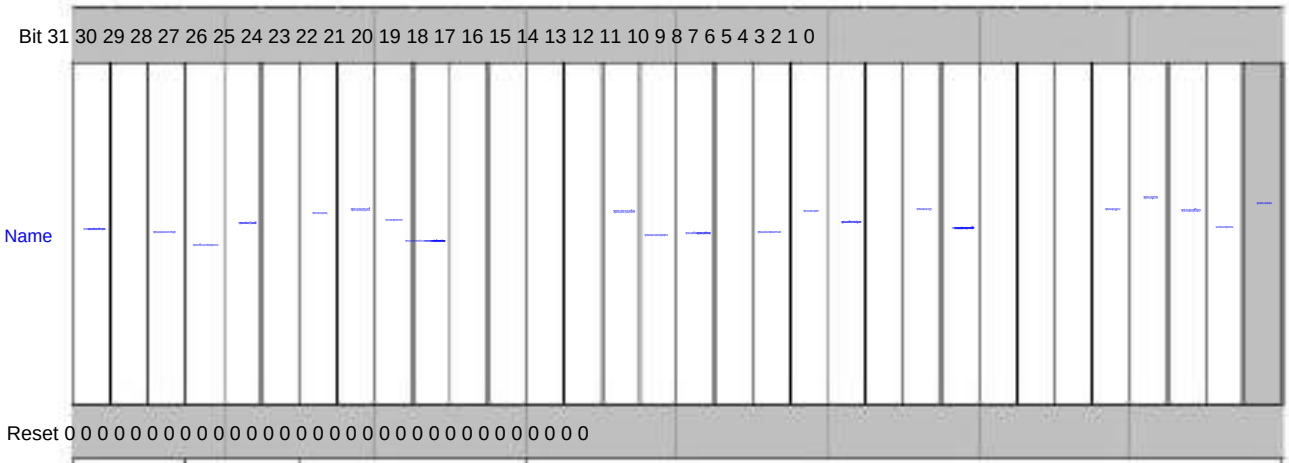
[14] RWSC isooutdrop			Isochronous OUT packet drop interrupt. Note: A 1 in this bit clears the interrupt.
[13] RWSC enumdone			Indicates that velocity enumeration is complete. Notice: Setting this bit position clears the interrupt.
[12] RWSC usbrst			Indicates that the USB has detected a reset. Note: A 1 in this bit clears the interrupt.
[11] RWSC usbsusp			Indicates that the USB has detected suspend. Notice: Setting this bit position clears the interrupt.
[10] RWSC susp			Indicates that the detection is idle for 3ms on the USB. Note: A 1 in this bit clears the interrupt.
[9]	RWSC i2ct		Interrupt occurs when an I2C access is complete on the I2C interface. This bit is only enabled when OTG_I2C_INTERFACE=1. Note: A 1 in this bit clears the interrupt.
[8]	RWSC ulpickinti2cckint		When a ULPI Carkit interrupt occurs, the core sets this interrupt bit. This bit is only valid when OTG_ULPI_CARKIT = 1, otherwise it returns 0; When I2C Carkit Interrupt, the core sets this interrupt bit. This bit is valid only when OTG_I2C_INTERFACE = 1, otherwise it returns 0 when read. Note: A 1 in this bit clears the interrupt.
[7]	RO	goutnakeff	Indicates that the global OUT NAK bit in the Device control register is set. This interrupt can be achieved by clearing Global OUT NAK.
[6]	RO	ginnakeff	An interrupt occurs when Set Global Non-periodic IN NAK is set in the device control register.
[5]	RO	nptxfemp	Generates an interrupt when the Non-periodic TxFIFO is full or half empty.
[4]	RO	rxflvl	Indicates that at least one packet is pending for the RxFIFO to read.

[3]	RWSC sof		Host mode: Indicates that a SOF, micro-SOF or Keep-acitve is being sent. Device mode: Indicates that a SOF token is received by USB.
[2]	RO	otgint	Indicates that an OTG protocol event is in progress. Clearing this interrupt requires clearing the associated bit in the GOTGINT register.
[1]	RWSC modemis		Pattern mismatch interrupt. - When the core works in DEVICE mode, a register in host mode should be accessed; - When the core works in HOST mode, a register in device mode should be accessed. 0: invalid; 1: Valid. Note: A 1 in this bit clears the interrupt.
[0]	RO	curmod	current working mode. 0: DEVICE mode; 1: HOST mode.

GINTMSK

GINTMSK is the system interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0018	GINTMSK	0x0000_0000



Bits	Access Name		Description
[31]	RW wkupintmsk		Resume/Remote Wakeup detection interrupt mask. 0: Shield; 1: No shielding.

[30] RW	sessreqintmsk		Session Request/New Session detection interrupt mask. 0: Shield; 1: No shielding.
[29] RW	disconnintmsk		Disconnect detection interrupt mask. 0: Shield; 1: No shielding.
[28] RW	conidstschngmsk		Connector ID state change interrupt mask. 0: Shield; 1: No shielding.
[27] RW	lpm_intmsk		LPM Transaction receive interrupt mask. 0: Shield; 1: No shielding.
[26] RW	ptxfempmsk		Periodic TxFIFO Empty interrupt mask. 0: Shield; 1: No shielding.
[25] RW	hchintmsk		Host Channel interrupt mask. 0: Shield; 1: No shielding.
[24] RW	prtintmsk		Host Port Interrupt Mask 0: Shield; 1: No shielding.
[23] RW	resetdetmsk		Reset detection interrupt mask. 0: Shield; 1: No shielding.
[22] RW	fetsuspmsk		Data Fetch Suspended interrupt mask. 0: Shield; 1: No shielding.
[21] RW		incomplpmskincompisooutmsk	Incomplete Periodic Transfer interrupt mask. 0: Shield; 1: No shielding. Incomplete Isochronous OUT Transfer interrupt mask. 0: Shield; 1: No shielding.

[20] RW incompisoinmsk			Incomplete Isochronous IN Transfer interrupt mask. 0: Shield; 1: No shielding. This bit is only enabled in Dedicated TxFIFO mode when periodic endpoints are enabled.
[19] RW oepintmsk			OUT Endpoints interrupt mask. 0: Shield; 1: No shielding.
[18] RW iepintmsk			IN Endpoints interrupt mask. 0: Shield; 1: No shielding.
[17] RW epmismsk			Endpoint Mismatch Interrupt interrupt mask. 0: shielded; 1: not shielded.
[16] RW rstrdoneintmsk			Restore Done interrupt mask. 0: Shield; 1: No shielding. This field is only available when the Hibernation feature is enabled (OTG_EN_PWROPT=2).
[15] RW eopfmsk			End of Periodic Frame interrupt mask. 0: Shield; 1: No shielding.
[14] RW isooutdropmsk			Device only Isochronous OUT packet loss interrupt mask. 0: Shield; 1: No shielding.
[13] RW enumdonemsk			Enumeration Done interrupt mask. 0: Shield; 1: No shielding.
[12] RW usbrstmsk			USB Reset interrupt mask. 0: shielded; 1: not shielded.
[11] RW usbsuspmsk			USB Suspend interrupt mask. 0: Shield; 1: No shielding.

[10] RW erlysuspmsk			Early Suspend interrupt mask. 0: Shield; 1: No shielding.
[9] RW i2cintmsk			I2C interrupt mask. 0: Shield; 1: No shielding.
[8] RW ulpickintmsk			ULPI Carkit interrupt mask. 0: Shield; 1: No shielding. I2C Carkit interrupt mask. 0: Shield; 1: No shielding.
[7] RW goutnakeffmsk			Global OUT NAK Effective interrupt mask. 0: Shield; 1: No shielding.
[6] RW ginnakeffmsk			Global Non-periodic IN NAK Effective interrupt mask. 0: shielded; 1: not shielded.
[5] RW nptxfempmsk			Non-periodic TxFIFO Empty interrupt mask. 0: Shield; 1: No shielding.
[4] RW rxflvlmsk			Receive FIFO Non-Empty interrupt mask. 0: Shield; 1: No shielding.
[3] RW sofmsk			Start of (micro)Frame interrupt mask. 0: Shield; 1: No shielding.
[2] RW otgintmsk			Device interrupt mask. 0: Shield; 1: No shielding.
[1] RW modemismsk			Mode Mismatch interrupt mask. 0: Shield; 1: No shielding.
[0]	RO	reserved	reserve.

GRXSTSR

GRXSTSR is the receive status debug read register.

Offset Address	Register Name	Total Reset Value
0x001C	GRXSTSR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_devicemode							fn_devicemode					-----				-----						bcnt_devicemode								-----	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	reserve.
[24:21]	RO	fn_devicemode	Number of Frames.
[20:17]	RO	pktsts_devicemode	packet status 0001: Global OUT NAK (causing interrupt); 0010: IN data packet reception; 0011: IN transmission completed (causing interrupt); 0101: Data toggle error (causing interrupt); 0111: Channel stop (causing interrupt); Others: Reserved .
[16:15]	RO	dpid_devicemode	Data PID identification of received packets. 00ÿDATE0ÿ 10ÿDATA1ÿ 01ÿDATA2ÿ 11ÿMDATAÿ
[14:4]	RO	bcnt_devicemode	calculates the size in bytes of received IN packets.
[3:0]	RO	chnum_devicemod It is	indicates the number of channels to which the currently received data packets belong.

GRXSTSP

GRXSTSP is the receive status read&pop register.

Offset Address	Register Name	Total Reset Value
0x0020	GRXSTSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_devicemode																fn_devicemode				bcnt_devicemode											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved_devicemode	Reserved.
[24:21]	RO	fn_devicemode	Number of Frames.
[20:17]	RO	pktsts_devicemode	Packet status. 0x1: Global OUT NAK (causing interrupt); 0x2: IN data packet reception; 0x3: IN transmission completed (causing interrupt); 0x4: Data toggle error (causing interrupt); 0x7: Channel stop (causing interrupt); Others: Reserved .
[16:15]	RO	dpid_devicemode	Data PID identification of received packets. 00ÿDATE0ÿ 10ÿDATA1ÿ 01ÿDATA2ÿ 11ÿMDATAÿ
[14:4]	RO	bcnt_devicemode	calculates the size in bytes of received IN packets.
[3:0]	RO	chnum_devicemode	indicates the number of channels to which the currently received data packets belong. It is

WITHOUT GRXF

GRXFSIZ configures the register for Receive FIFO size.

Offset Address	Register Name	Total Reset Value
0x0024	WITHOUT GRXF	0x0000_0211

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	rxfdep
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0 1 0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	rxfdep	RxFIFO depth. 16 to 32,768.

WITHOUT GNPTXF

GNPTXFSIZ is the Non-Periodic Transmit FIFO Size configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	WITHOUT GNPTXF	0x0100_0211

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ineptxf0dep	ineptxf0staddr
Reset	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0 0 1 0 0 0 1

Bits	Access	Name	Description
[31:16]	RW	ineptxf0dep	IN Endpoint TxFIFO 0 depth. 16 to 32,768.
[15:0]	RW	ineptxf0staddr	IN Endpoint FIFO0 Transmit RAM start address.

GNPTXSTS

GNPTXSTS for Non-periodic TxFIFO and the Nonperiodic

Transmit Request Queue information query register.

Offset Address	Register Name	Total Reset Value
0x002C	GNPTXSTS	0x0008_0100

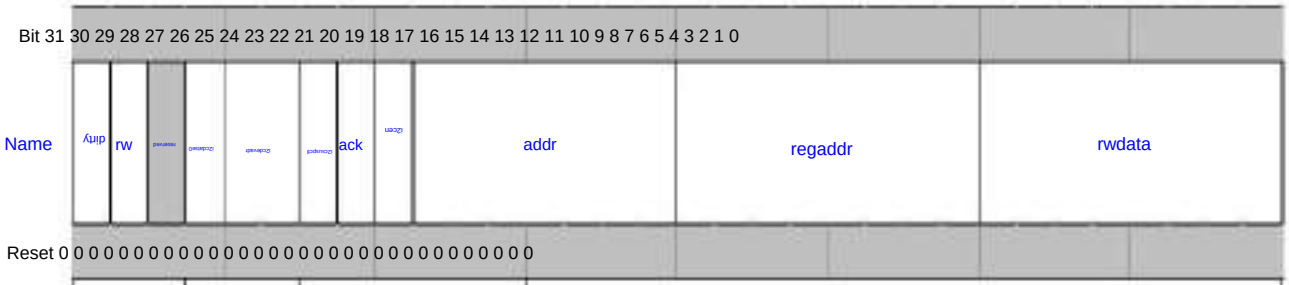
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	nptxqtop							nptxqspcavail														nptxfspcavail									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:24]	RO	nptxqtop	Non-periodic Transmit Request Queue top layer. bit[30:27]: Channel/endpoint number. bit[26:25]ÿ 00ÿIN/OUT tokenÿ 01ÿZero-length transmit packet (device IN/host OUT)ÿ 10ÿPING/CSPLIT tokenÿ 11: Channel stop command. bit[24]: stop (last attempt for selected channel/endpoint).
[23:16]	RO	nptxqspcavail	Non-periodic Transmit Request Queue space is available 0x0: Non-periodic Transmit Request Queue is full; 0x1: 1 address is available; 0x2: 2 addresses are available; 0xn: n addresses are available (0 ÿ n ÿ 8); Others: reserved.
[15:0]	RO	nptxfspcavail	The total amount of free space in the Non-periodic Transmit Request Queue. 0x0: Non-periodic TxFIFO is full; 0x1: 1 word is available; 0x2: 2 words available; 0xn: n words are available (0 ÿ n ÿ 32,768); 0x8000: 32,768 words are available; others: reserved.

GI2CCTL

GI2CCTL is the I2C access register.

Offset Address	Register Name	Total Reset Value
0x0030	GI2CCTL	0x0000_0000



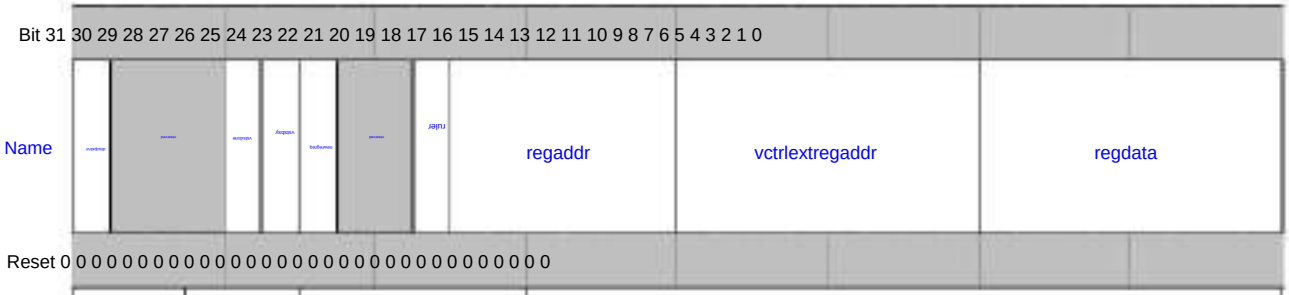
Bits	Access Name		Description
[31] RWSC	bsydne		I2C Busy/Doneÿ 0ÿI2C Doneÿ 1ÿI2C Busyÿ
[30] RW	rw		Read and write instructions. 0: write; 1: Read.
[29] RO		reserved	reserve.
[28] RW	i2cdatse0		FS interface USB mode selection. 0: VP_VM USB mode; 1: DAT_SE0 USB mode.
[27:26] RW	i2cdevadr		I2C device address. 00ÿ7'h2Cÿ 01ÿ7'h2Dÿ 10ÿ7'h2Eÿ 11ÿ7'h2Fÿ
[25] RW	i2csuspctl		I2C suspend control. 0: Use utmi_suspend_n; 1: Use I2C write to edit Suspend bit of PHY register.
[24] RO		ack	I2C ACKÿ 0ÿWANTEDÿ 1ÿACKÿ
[23] RW	i2cen		I2C Transaction Enable. 0: forbidden; 1: enable.

[22:16] RW	addr		I2C slave address.
[15:8] RW	regaddr		I2C register address.
[7:0] RW	rwdata		I2C reads and writes data.

GPVNDCTL

GPVNDCTL is the PHY Vendor Control Register.

Offset Address	Register Name	Total Reset Value
0x0034	GPVNDCTL	0x0000_0000



Bits	Access	Name	Description
[31]	RWSC	disulpidrvr	ULPI drive disabled. 0: ULPI interface is enabled; 1: ULPI interface disabled. Notice: This bit is only valid when OTG_ULPI_CARKIT=1, otherwise it returns 0 when read.
[30:28]	RO	reserved	reserve.
[27]	RWSC	vstsdone	vendor control access status (done) 0: New Register request is set; 1: Vendor Control access ends.
[26]	RO	vstsbsy	vendor control access (busy) 0: Vendor control access ends; 1: Vendor control is being accessed.
[25]	RWSC	newregreq	New vendor control access 0: no access request; 1: A new vendor control access request.
[24:23]	RO	reserved	reserve.

[22] RW regwer			Register read and write. 0: read; 1: Write.
[21:16] RW regaddr			Register access address.
[15:8] RW vctrlextregaddr			UTMI+ Vendor Control register address. [15:12] Addressing for 4-bit parallel output bus [11:8] from utmi_vcontrol[3:0]
[7:0] RW regdata			register data. Valid when Vstatus Done is set.

GGPIO

GGPIO is a general-purpose input/output register.

Offset Address	Register Name	Total Reset Value
0x0038	GGPIO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	gpo	gpi
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	gpo	General output, driven by gp_o[15:0] in core.
[15:0]	RW	gpi	General input, reflecting the value of gp_i[15:0] in core.

GUID

GUID is the user ID query register.

Offset Address	Register Name	Total Reset Value
0x003C	GUID	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	userid	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	userid	user ID.

GSNPSID

GSNPSID is the Synopsys ID query register.

Offset Address	Register Name	Total Reset Value
0x0040	GSNPSID	0x4F54_300A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	synopsysid																															
Reset	0	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access Name	Description
[31:0]	RW synopsysid	DWC_otg core number currently used.

GHWCFG1

GHWCFG1 is user hardware configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0044	GHWCFG1	0x0000_0000

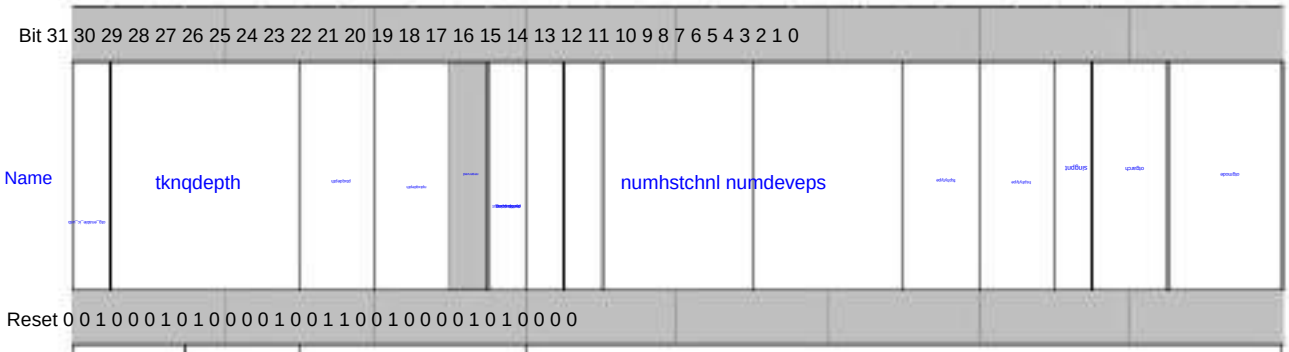
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epdir																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	epdir	Endpoint direction Each endpoint uses two bits to indicate its direction Endpoint Bits [31:30]: the direction of Endpoint 15; Bits [29:28]: the direction of Endpoint 14; ... Bits [3:2]: the direction of Endpoint 1; Bits [1:0]: the direction of Endpoint 0 (always bidirectional). 00: bidirectional (IN and OUT) endpoint; 01ÿIN endpointÿ 10: OUT endpoint; 11: reserved.

GHWCFG2

GHWCFG2 is user hardware configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0048	GHWCFG2	0x2284_C850



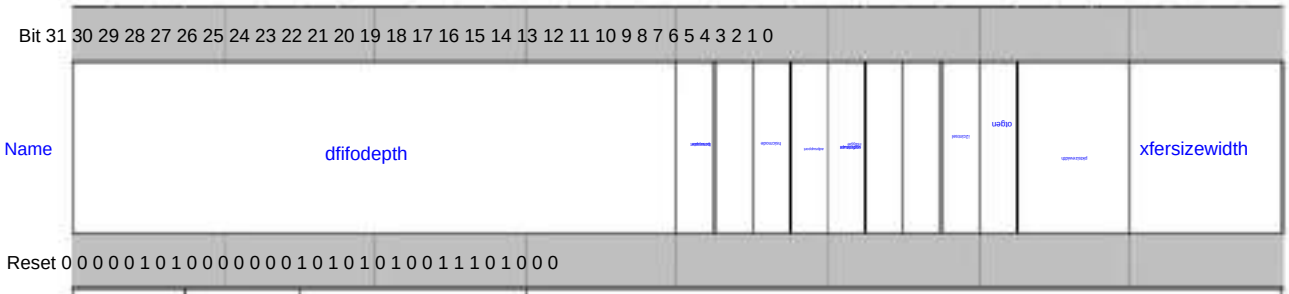
Bits	Access Name		Description
[31] RO		disable; otg_enable_ic_usb	IC_USB selection enable. 0: 1: enable.
[30:26] RO		tknqdepth	Device mode IN Token Sequence Learning Queue depth. Range: 0~30.
[25:24] RO		ptxqdepth	Host mode Periodic Request Queue depth. 00ÿ2ÿ 01ÿ4ÿ 10ÿ8ÿ 11ÿ16ÿ
[23:22] RO		nptxqdepth	Non-periodic Request Queue depth. 00ÿ2ÿ 01ÿ4ÿ 10ÿ8ÿ Other: reserved.
[21] RO		reserved	reserve.
[20] RW	multiprocintrpt		Multiprocessor interrupt enable. 0: forbidden; 1: enable.
[19] RO		dynfifosizing	Dynamic FIFO size change enabled. 0: forbidden; 1: enable.

[18] RO		periosupport	Host mode Periodic OUT Channels support. 0: not supported; 1: Support.
[17:14] RO		number	Number of Host Channels. 0~15: 0 means 1 channel, 15 means 16 channels.
[13:10] RO		numdeveps	Number of Device Endpoints other than Endpoint 0. Range: 1~15.
[9:8] RO		fsphytype	Full-Speed PHY interface type. 00: Full-speed interface is not supported; 01: Full-speed interface is supported; 10: FS pins are shared with UTMI+ pins; 11: FS pins are shared with ULPI pins.
[7:6] RO		hsphytype	High-Speed PHY interface type. 00: does not support high-speed interface; 01ÿUTMI+ÿ 10:ULPI: 11:UTMI+ ÿ ULPIÿ
[5]	RO	singpnt	Point-to-Pointÿ 0: multi-point application (support hub and split); 1: single-point application (do not support hub and split).
[4:3] RO		otgarch	Device schema. 00: Slave-Only; 01: External DMA; 10: Internal DMA; Other: reserved.
[2:0] RO		otgmode	operating mode. 000ÿHNP- and SRP-Capable OTG (Host & Device)ÿ 001ÿSRP-Capable OTG (Host & Device)ÿ 010ÿNon-HNP and Non-SRP Capable OTG (Host & Device)ÿ 011ÿSRP-Capable Deviceÿ 100ÿNon-OTG Deviceÿ 101ÿSRP-Capable Hostÿ 110ÿNon-OTG Hostÿ Other: reserved.

GHWCFG3

GHWCFG3 is user hardware configuration register 3.

Offset Address	Register Name	Total Reset Value
0x004C	GHWCFG3	0x0501_54E8



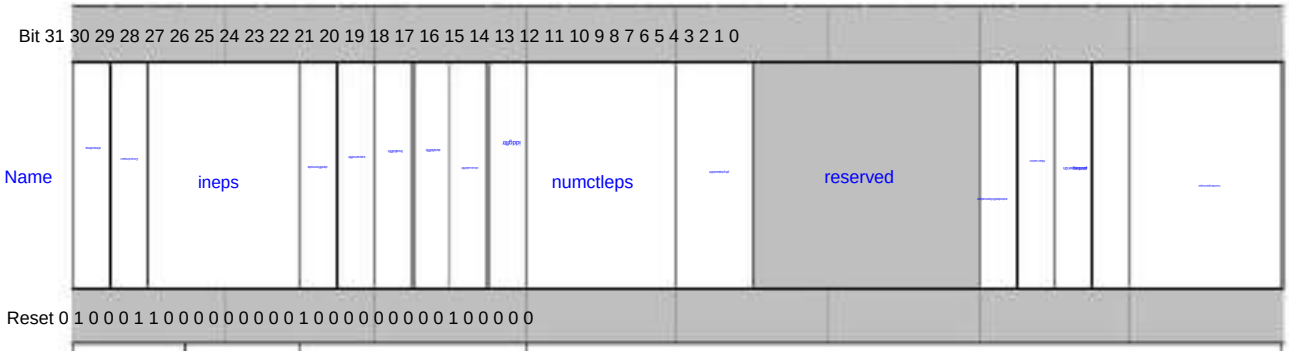
Bits	Access	Name	Description
[31:16]	RO	dfifodepth	DFIFO depth. 32 to 32,768.
[15]	RO	lpmmode	The LPM working mode is specified and configurable.
[14]	RO	bcsupport	Indicates whether the HS Device controller supports Battery Charger. 0: not supported; 1: Support.
[13]	RO	hsicmode	HSIC mode selection. 0: HSIC-capable share UTMI PHY interface; 1: Not selected.
[12]	RO	adpsupport	Indicates whether the Device controller has ADP logic. 0: without; 1: with.
[11]	RO	rsttype	Reset method of Clock always Blocks. 0: asynchronous reset; 1: Synchronous reset.
[10]	RO	optfeature	Optional features removed. Features include User ID register, GPIO interface ports, and SOF toggle and counter ports. 0: do not remove; 1: remove.
[9]	RO	vndctlsupt	Vendor control interface support. 0: not supported; 1: Support.

[8]	RO	i2cintsel	I2C interface selection. 0: no selection; 1: Select.
[7]	RO	otgen	The Device function is enabled. 0: disable; 1: enable.
[6:4] RO		pktsizewidth	Packet width. 000ÿ4 bitsÿ 001ÿ5 bitsÿ 010ÿ6 bitsÿ 011ÿ7 bitsÿ 100ÿ8 bitsÿ 101ÿ9 bitsÿ 110ÿ10 bitsÿ Other: reserved.
[3:0] RO		xfersizewidth	transfer width. 0000ÿ11 bitsÿ 0001ÿ12 bitsÿ 1000ÿ19 bitsÿ Other: reserved.

GHWCFG4

GHWCFG4 is user hardware configuration register 4.

Offset Address	Register Name	Total Reset Value
0x0050	GHWCFG4	0x4600_8020



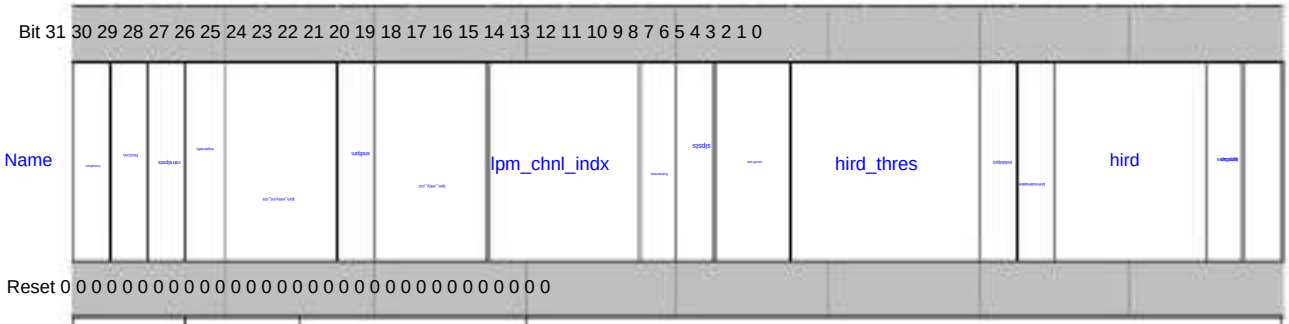
Bits	Access	Name	Description
[31]	RO	descdma	Scatter/Gather DMAÿ 0: no dynamic configuration; 1: Dynamic configuration.
[30]	RO	Descdmaen	PAD Slew rateÿ 0ÿfastÿ 1ÿslowÿ
[29:26]	RO	ineps	The number of IN Endpoints in Device mode. 0: 1 IN Endpoint; 1: 2 IN Endpoints; .... 15: 16 IN Endpoints.
[25]	RO	dedfifomode	The Dedicated Transmit FIFO of Device IN Endpoint is enabled. 0: forbidden; 1: enable.
[24]	RO	sessendfltr	session_end Filter enabled. 0: forbidden; 1: enable.
[23]	RO	bvalidfltr	b_valid Filter enabled. 0: disable; 1: enable.
[22]	RO	avalidfltr	a_valid Filter enabled. 0: forbidden; 1: enable.

[21] RO		vbusvalidfltr	VBUS Valid Filter enabled. 0: forbidden; 1: enable.
[20] RO		iddgfltr	IDDIG Filter is enabled. 0: forbidden; 1: enable.
[19:16] RO		numctleps	In Device mode, the control Endpoint quantity range except Enpoint 0: 0 ÿ15.
[15:14] RO		phydatawidth	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper data width. 00ÿ8 bitsÿ 01ÿ16 bitsÿ 10: 8/16 bits, software can be configured; others: reserved.
[13:8] RO		reserved	reserve.
[7]	RO	extndedhibernation	Extended Hibernation enabled. 0: forbidden; 1: enable.
[6]	RO	hibernation	Hibernation is enabled. 0: forbidden; 1: enable.
[5]	RO	ahbfreq	The AHB minimum frequency is below 60 MHz. 0: No; 1: Yes.
[4]	RO	partialpwrdn	Partial Power Down is enabled. 0: disable; 1: enable.
[3:0] RO		numdevperioeps	The number range of Periodic IN Endpoints in Device mode: 0~15.

GLPMCFG

GLPMCFG is the LPM configuration register.

Offset Address	Register Name	Total Reset Value
0x0054	GLPMCFG	0x0000_0000



Bits	Access	Name	Description
[31]	RW	invselhsic	HSIC enable is selected by HSIC-Invert. If if_sel_hsic = 1; InvSelHsic = 1: prohibited; InvSelHsic = 0: Enable. If if_sel_hsic = 0; InvSelHsic = 1: enable; InvSelHsic = 0: disable.
[30]	RW	hsiccon	HSIC-Connectÿ Host Mode: When this bit is set to 1, the HSIC on the drive bus is in IDLE state, and waits for the device to issue HSIC Connect Sequence; Device Mode: When this bit is set to 1, the device waits for the HSIC Idle line state to appear on the bus, and Idle Start HSIC Connect after the line status. Notice: This bit is valid only when OTG_ENABLE_HSIC = 1, otherwise it returns 0 when read.
[29]	RW	rstrslpsts	Restore SlpSts. 0: core enters Shallow Sleep mode; 1: core enters Deep Sleep mode.
[28]	RW	enbesl	Best Effort Service Latency enabled. 0: forbidden; 1: enable.
[27:25]	RO	lpm_retrycnt_sts	LPM Retry count status. Count the remaining retry times.
[24]	RWSC	sndlpm	LPM Transaction sent.
[23:21]	RW	lpm_retry_cnt	Statistics of LPM Retry times. When the device gives an error message, it displays the additional LPM Retry times of the host before the valid signal of the device arrives.

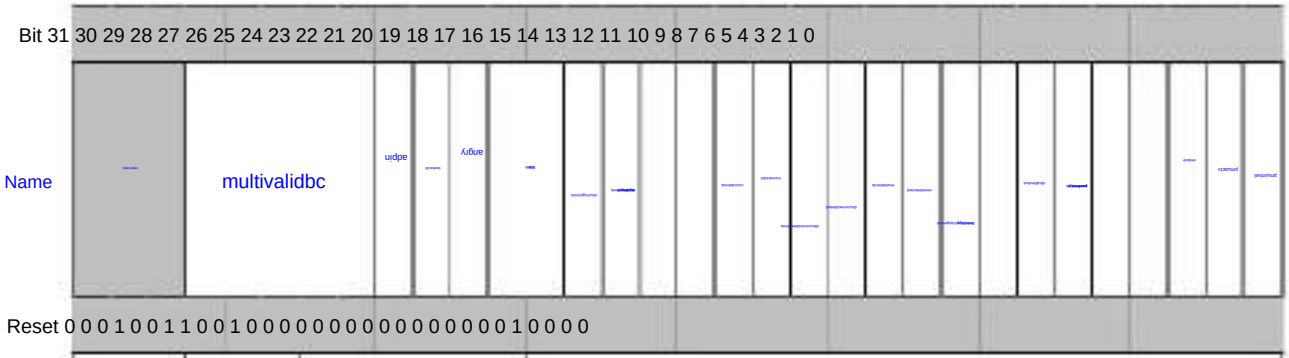
[20:17] RW	lpm_chnl_indx		LPM Channel Index. The channel number of the LPM transaction has been given, based on the LPM Channel index, the core will automatically calculate the address of the device and the number of endpoints.
[16] RO		l1resumes	Restoration of sleep state. 0: restore; 1: No recovery.
[15] RO		slpsts	Port sleep state. 0: restore; 1: sleep.
[14:13] RO		corel1res	LPM response. Device mode: The response of LPM Transaction is reflected by these two bits; Host mode: Handshake response received from device in LPM transaction. 11ÿACKÿ 10ÿNYETÿ 01ÿSTALLÿ 00: ERROR (no handshake response).
[12:8] RW	hird_thres		BESL or HIRD waterline.
[7] RW	enblslpm		utmi_sleep_n enable. 0: forbidden; 1: enable.
[6] RW	bremotewake		RemoteWake is enabled. host mode: the enable signal is sent by wIndex field of LPM Transaction; device mode (read-only): when ACK, NYET or STALL response is sent to LPM Transaction, this bit will follow the received LPM Token, bRemoteWake and bmAttribute Updated.

[5:2] RW hird			When EnBESL = 0 Host-Initiated recovery cycle Host mode: assigned by LPM transaction. Device mode: updated by LPM Token HIRD bmAttribute. Sl. No HIRD[3:0] THIRD (µs) 1 4'b0000 50 2 4'b0001 125 3 4'b0010 200 4 4'b0011 275 5 4'b0100 350 6 4'b0101 425 7 4'b0110 500 8 4'b0111 575 9 4'b1000 650 10 4'b1001 725 11 4'b1010 800 12 4'b1011 875 13 4'b1100 950 14 4'b1101 1025 15 4'b1110 1100 16 4'b1111 1175 When EnBESL = 1 Best Effort Service Latency(BESL) Host mode: The value of BESL is sent to LPM transaction. Device mode: It is updated by LPM Token BESL bmAttribute.
[1] RW appl1res			LPM response. 0ÿNYETÿ 1ÿACKÿ
[0] RW lpmcap			LPM enable 0: forbidden; 1: enable.

GPWRDN

GPWRDN is the power down register.

Offset Address	Register Name	Total Reset Value
0x0058	GPWRDN	0x1320_0010



Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RO	multivalidbc	The BC ACA input is as follows: Bit 28 - rid_float Bit 27 - rid_gnd Bit 26 - rid_a Bit 25 - rid_b Bit 24 - rid_c.
[23]	RWSC	adpint	Interrupt occurs when ADP is in progress. Set to 1 to clear the interrupt.
[22]	RO	bsessvld	B Session is valid. 0ÿB-Valid = 0ÿ 1ÿB-valid = 1ÿ
[21]	RO	angry	IDDIG signal status indication. current working mode. 0: Host mode; 1: Device mode.
[20:19]	RO	line state	USB current status indicator. 00ÿDM = 0, DP = 0ÿ 01ÿDM = 0, DP = 1ÿ 10ÿDM = 1, DP = 0ÿ 11: Undefined.
[18]	RW	stschngintmsk	StsChng interrupt mask. 0: Shield; 1: No shielding.

[17] RWSC	stschngint		StsChng interrupt. This bit indicates a change of state of the IDDIG or BSessVld signal. 0: no state change; 1: Status change.
[16] RW	srpdetectmsk		SRPDetect interrupt mask, only valid in HOST mode. 0: no shielding; 1: Mask interrupt.
[15] RWSC	srpdetect		SRP detection. 0: not detected; 1: Detected.
[14] RW	conndetmsk		Connection detection interrupt mask. 0: Shield; 1: No shielding. This bit is valid only when OTG_EN_PWROPT = 2.
[13] RO		connectdet	Connection detection. 0: not connected; 1: Connected. This bit is only valid when OTG_EN_PWROPT = 2
[12] RW		disconnectdetectms k	Disconnect detection interrupt mask. 0: Shield; 1: No shielding. This bit is valid only when OTG_EN_PWROPT = 2.
[11] RWSC	disconnectdetect		Disconnect detection. 0: not disconnected; 1: Disconnected. This bit is valid only when OTG_EN_PWROPT = 2.
[10] RW	resetdetmsk		Reset detect interrupt mask. 0: Shield; 1: No shielding. This bit is valid only when OTG_EN_PWROPT = 2.
[9]	RWSC	resetdetected	Reset detection. 0: not reset; 1: Reset. This bit is valid only when OTG_EN_PWROPT = 2.

[8] RW		linestagechangems k	Line state change interrupt mask. 0: shielded; 1: No shielding. This bit is valid only when OTG_EN_PWROPT = 2.
[7]	RWSC lnstschng		Line state change detection. 0: unchanged; 1: Changed. This bit is valid only when GPWRDN.PMUActv = 1 and OTG_EN_PWROPT = 2.
[6] RW disablevbus			Vbus Disableÿ host modeÿ 0: PrtPwr is not equal to 0; 1: PrtPwr is equal to 0; device modeÿ 0: bvalid signal is high level; 1: The bvalid signal is low. This bit is valid only when GPWRDN.PMUActv = 1.
[5] RW pwrdnswtch			Power down switch. 0: open; 1: off.
[4] RW pwrdnrst_n			Power down reset. 0: reset; 1: Do not reset.
[3] RW pwrdnclmp			power down tap enabled. 0: forbidden; 1: enable.
[2] RW restore			Restoreÿ 0: DWC_otg is in normal mode; 1: DWC_otg is in restore mode. Note: This bit is only valid when OTG_EN_PWROPT = 2.
[1] RW pmuactv			The PMU is enabled. 0: disable PMU module; 1: PMU module enabled.
[0] RW pmuintsel			PMU interrupt selection. 0: Internal DWC_otg_core interrupt; 1: External DWC_otg_core interrupt.

GDFIFOCFG

GDFIFOCFG is the DFIFO software configuration register.

Offset Address	Register Name	Total Reset Value
0x005C	GDFIFOCFG	0x0501_0511

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epinfobaseaddr																				gdfifocfg											
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	epinfobaseaddr	This field provides the starting address of the EP info controller.
[15:0]	RW	gdfifocfg	Dynamically configure the size of DFIFO.

GADPCTL

GADPCTL is the ADP timer, control and status register.

Offset Address	Register Name	Total Reset Value
0x0060	GADPCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					With																			quickly								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:27]	RW	ar	access request. 00: Read and write are valid; 01: Read only; 10: write only; 11: Reserved.

[26] RW adptoutmsk			ADP timeout interrupt mask. 0: Shield; 1: No shielding. Notice: This bit is only valid when OTG_Ver = 1.
[25] RW adpsnsintmsk			ADP Sense interrupt mask. 0: Shield; 1: No shielding. Note: This bit is only valid when OTG_Ver = 1.
[24] RWC adpprbintmsk			ADP Probe interrupt mask. 0: Shield; 1: No shielding. Note: This bit is only valid when OTG_Ver = 1.
[23] RWC adptoutint			ADP timeout interrupt. Set to 1 to remove interrupt. Note: This bit is only valid when OTG_Ver = 1.
[22] RWC adpsnsint			ADP Sense is interrupted. Set to 1 to remove interrupt. Notice: This bit is only valid when OTG_Ver = 1.
[21] RWC reprint			ADP Probe interrupted. Set to 1 to remove interrupt. Notice: This bit is only valid when OTG_Ver = 1.
[20] RW adpen			ADP enabled. 0: forbidden; 1: enable. Note: This bit is only valid when OTG_Ver = 1.

[19] RWC adpres			ADP reset. 0: not reset; 1: Reset. Notice: This bit is only valid when OTG_Ver = 1.
[18] RW enasns			sense is enabled. 0: forbidden; 1: enable. Note: This bit is only valid when OTG_Ver = 1.
[17] RW enaprb			probe enable. 0: forbidden; 1: enable. Note: This bit is only valid when OTG_Ver = 1.
[16:6] RO		quickly	Ramp Time. 32kHz clock cycle number definition. 0x000ÿ1 cyclesÿ 0x001ÿ2 cyclesÿ 0x002ÿ3 cyclesÿ ... 0x7FFÿ2048 cyclesÿ
[5:4] RW prdper			Probe Periodÿ 00: 0.625 to 0.925s (usually 0.775s); 01: 1.25 to 1.85s (usually 1.55s); 10: 1.9 to 2.6s (usually 2.275s); 11: reserved.
[3:2] RW prddelta			Probe Deltaÿ 32kHz clock cycle number definition. 00ÿ1 cycleÿ 01ÿ2 cyclesÿ 10ÿ3 cyclesÿ 11ÿ4 cyclesÿ

[1:0] RW	prbdschg		Probe discharge. Defines the time for TADP_DSCHG. 00ÿ4 msÿ 01ÿ8 msÿ 10ÿ16 msÿ 11ÿ32 msÿ

WITHOUT HPTXF

HPTXFSIZ is the TxFIFO configuration register.

Offset Address	Register Name	Total Reset Value
0x0100	WITHOUT HPTXF	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	ptxfsize	ptxfstaddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	ptxfsize	Host Periodic TxFIFO depth. 16~32768.
[15:0]	RW	ptxfstaddr	Host Periodic TxFIFO start address.

DPTXFSIZN

DPTXFSIZN is the device Periodic Transmit FIFO-n Size register.

说明

This register is valid only in share FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104ÿ0x0004×FIFO_num (FIFO_num =0~14)	DPTXFSIZN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dptxfsize	dptxfstaddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	dptxfsize	Device Periodic TxFIFO Size 4ÿ768ÿ
[15:0]	RW	dptxfstaddr	Device Periodic TxFIFO RAM start address.

DIEPTXFN

DIEPTXFN is the Device IN Endpoint Transmit FIFO Size register.

说明

This register is valid only in dedicated FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104ÿ0x0004×FIFO_num (FIFO_num = 0ÿ14)	DIEPTXFN	0x0300_0251

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	inepntxfdep	inepntxfstaddr
Reset	0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 1 0 1 0 0 0 1

Bits	Access Name	Description
[31:16]	RW inepntxfdep	IN Endpoint TxFIFO Depth 16ÿ32768ÿ
[15:0]	RW inepntxfstaddr	IN Endpoint FIFOn Transmit RAM start address.

DCFG

DCFG configures registers for Device

Offset Address	Register Name	Total Reset Value
0x0800	DCFG	0x8100_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	resvalid	they mix reserved devaddr
Reset	1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

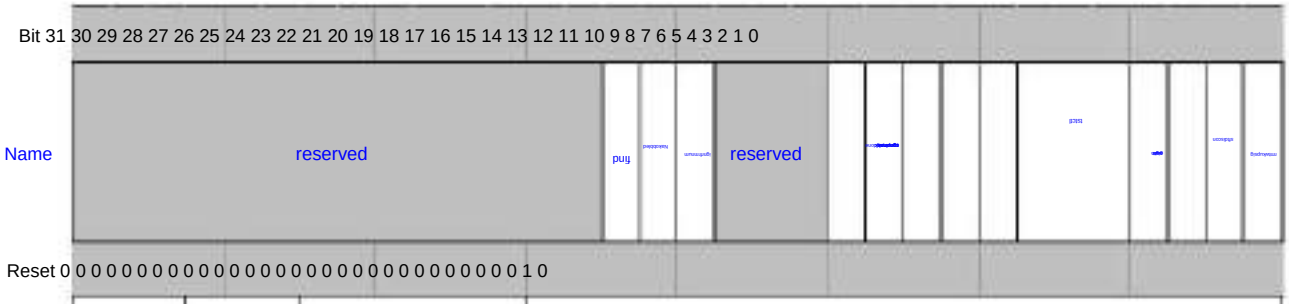
Bits	Access Name	Description
[31:26]	RW resvalid	Resume required time control. This bit is valid only when DCFG.Ena32kHzSusp = 1.

[25:24] RW	pressinfl		The ratio of (micro)frame is determined in Scatter/Gather DMA mode. 00ÿ25% of (micro)frameÿ 01ÿ50% of (micro)frameÿ 10ÿ75% of (micro)frameÿ 11ÿReservedÿ
[23] RW	descdma		Scatter/Gather DMA is enabled in Device mode. 0: forbidden; 1: enable.
[22:18] RW	epmiscnt		IN Endpoint mismatch statistics.
[17:14] RO		reserved	reserve.
[13] RW	endevoutnak		Device OUT NAK Enabled. 0: forbidden; 1: enable.
[12:11] RW	perfrint		Periodic frame interval. 00ÿ80% of the (micro)frame intervalÿ 01ÿ85%ÿ 10ÿ90%ÿ 11ÿ95%ÿ
[10:4] RW	devaddr		Device address.
[3] RW	ena32khzsusp		32 kHz Suspend mode enabled. 0: disable; 1: enable.
[2] RW	nzstsouthshk		Non-Zero-Length Status OUT handshake selection.
[1:0] RW	devspd		Device speed. 00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz); 01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz); 10: Low speed (USB 1.1 transceiver clock is 6 MHz); 11: Full speed (USB 1.1 transceiver clock is 6 MHz); 1.1 The transceiver clock is 48 MHz).

DCTL

DCTL is the Device control register.

Offset Address: 0x0804 | Register Name: DCTL | Total Reset Value: 0x0000_0002



Bits	Access	Name	Description
[31:18]	RO	reserved	reserve.
[17]	RW	found	Continue on BNA enabled. 0: forbidden; 1: enable.
[16]	RW	nakobble	NAK on Babble error. 0: no operation; 1: Set NAK on received babble.
[15]	RW	ignrfrmnum	Ignore the number of frames for isochronous endpoints. 0: do not ignore the number of frames; 1: Ignore the frame number.
[14:12]	RO	reserved	reserve.
[11]	RW	pwronprgdone	Indicates wakeup from power-down mode. 0: do not wake up; 1: Wake up.
[10]	WO	cgoutnak	Clear Global OUT NAK. 0: no operation; 1: Clear.
[9]	WO	sgoutnak	Set Global OUT NAK. 0: no operation, no setting; 1: set.
[8]	WO	cgnpinnak	Clear Global Non-periodic IN NAK. 0: no operation; 1: Clear.
[7]	WO	sgnpinnak	Set Global Non-periodic IN NAK. 0: no operation, no setting; 1: set.

[6:4] RW tstctl			Test controls. 000: test mode disabled; 001: Test_J mode; 010: Test_K mode; 011: Test_SE0_NAK mode; 100: Test_Packet mode; 101: Test_Force_Enable; Others: reserved.
[3]	RO	goutnaksts	Global OUT NAK status. 0: send handshake; 1: NAK handshake is sent.
[2]	RO	gnpinnaksts	Global Non-periodic IN NAK status. 0: send handshake; 1: NAK handshake is sent.
[1] RW sftdiscon			Soft disconnection. 0: normal mode; 1: The core drives phy_opmode_o to 2'b01, and then triggers USB disconnection.
[0] RW rmtwkupsig			Remote Wakeup signal sent. 0: Do not wake up remotely; 1: Remote wakeup.

STD

DSTS is the device status query register.

Offset Address	Register Name	Total Reset Value
0x0808	STD	0x0007_FF02

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Name	reserved	soft	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 1 1 1 1	1 1 0 0 0 0 0 0 1 0

Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.

[23:22] RO		devlnsts	Indicates the logic level of the current USB data line. Bit[23]ÿLogic level of D+ÿ Bit[22]ÿLogic level of D–ÿ
[21:8] RO		soft	The number of Frame or Microframe of the received SOF packet.
[7:4] RO		reserved	reserve.
[3]	RO	errticerr	Irregular error indication. When any irregular error occurs on the UTMI+ interface (for example, phy_rxvalid_i is set for 2ms due to PHY error), the controller core sets this bit. 0: normal; 1: An irregular error occurred on the UTMI+ interface.
[2:1] RO		enumspd	Enumeration speed. 00: High speed (PHY clock is 30 or 60 MHz); 01: Full speed (PHY clock is 30 or 60 MHz); 10: Low speed (PHY clock is 6 MHz); 11: Full speed (PHY clock is 48 MHz).
[0]	RO	suspsts	Suspend state, when the suspend condition is detected, this bit is 1.

DIEPMSK

DIEPMSK is the Device IN Endpoint common interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0810	DIEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

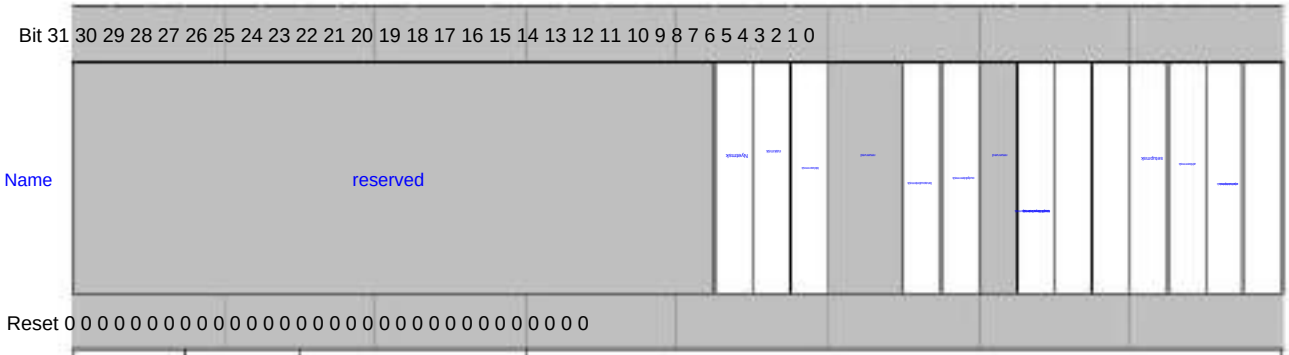
Bits	Access Name		Description
[31:14] RO		reserved	reserve.
[13] RW	nakmsk		NAK interrupt mask. 0: Shield; 1: No shielding.
[12:10] RO		reserved	reserve.

[9] RW	bnainintrmsk		BNA interrupt mask. 0: Shield; 1: No shielding.
[8] RW	txfifoundrnmsk		FIFO Underrun interrupt masking. 0: Shield; 1: No shielding.
[7]	RO	reserved	reserve.
[6] RW	inepnakeffmsk		IN Endpoint NAK Effective Interrupt masking. 0: Shield; 1: No shielding.
[5] RW	intknepmismsk		IN Token received with EP Mismatch interrupt mask. 0: Shield; 1: No shielding.
[4] RW	intkntxfempmsk		IN Token Received When TxFIFO Empty interrupt mask. 0: Shield; 1: No shielding.
[3] RW	timeoutmsk		Timeout condition interrupt mask. 0: Shield; 1: No shielding.
[2] RW	ahberrmsk		AHB error interrupt mask. 0: shielded; 1: not shielded.
[1] RW	epdisbldmsk		Endpoint Disabled interrupt masking. 0: Shield; 1: No shielding.
[0] RW	xfercomplmsk		Transfer Completed interrupt mask. 0: Shield; 1: No shielding.

DOEPMSK

DOEPMSK is the Device OUT Endpoint public interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0814	DOEPMSK	0x0000_0000



Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14]	RW	nyetmsk	NYET interrupt mask. 0: Shield; 1: No shielding.
[13]	RW	nakmsk	NAK interrupt mask. 0: Shield; 1: No shielding.
[12]	RW	bbleerrmsk	Babble Error interrupt mask. 0: Shield; 1: No shielding.
[11:10]	RO	reserved	reserve.
[9]	RW	bnaoutintrmsk	BNA interrupt mask. 0: Shield; 1: No shielding.
[8]	RW	outpkterrmsk	OUT Packet Error interrupt mask. 0: Shield; 1: No shielding.
[7]	RO	reserved	reserve.
[6]	RW	back2backsetupms	Back-to-Back SETUP Packets Received interrupt mask. 0: shield; k 1: No shielding.
[5]	RW	stsphsercvdmsk	Status Phase Received Interrupt mask. 0: shielded; 1: not shielded.

[4] RW	outtknepdismsk		W OUT Token Received when Endpoint Disabled Interrupt mask. 0: Shield; 1: No shielding.
[3] RW	setupmsk		SETUP Phase Done interrupt mask. 0: Shield; 1: No shielding.
[2] RW	ahberrmsk		AHB Error interrupt mask. 0: Shield; 1: No shielding.
[1] RW	epdisbldmsk		Endpoint Disabled interrupt masking. 0: Shield; 1: No shielding.
[0] RW	xfercomplmsk		Transfer Completed interrupt mask. 0: Shield; 1: No shielding.

TEETH

DAINT is all Endpoint interrupt registers of Device.

Offset Address	Register Name	Total Reset Value
0x0818	TEETH	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	outepint	inepint
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	outepint	OUT Endpoint interrupt bit. bit16 means out endpoint 0; ..... bit31 means out endpoint 15.
[15:0]	RO	inepint	IN Endpoint interrupt bit. bit0 means in endpoint 0 ..... bit15 means in endpoint 15.

DAINTMSK

DAINTMSK is the mask register for all Endpoint interrupts.

Offset Address	Register Name	Total Reset Value
0x081C	DAINTMSK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	outepmsk	inepmsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:16]	RW outepmsk	OUT Endpoint interrupt mask bit. bit16 means out endpoint 0; ..... bit31 means out endpoint 15.
[15:0]	RW inepmsk	IN Endpoint interrupt mask bit. bit0 means in endpoint 0; ..... bit15 means in endpoint 15.

DTKNQR1

DTKNQR1 is Device IN Token Sequence Learning Queue read register 1.

Offset Address	Register Name	Total Reset Value
0x0820	DTKNQR1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	eptkn	intknwptr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:8] RO	eptkn	The endpoint number of the token. Each token uses 4 bits but the endpoint number of the token Bits[31:28]: the endpoint number of Token 5; Bits[27:24]: the endpoint number of Token 4; ..... Bits[15:12]: endpoint number of Token 1; Bits[11:8]: endpoint number of Token 0.

[7]	RO	wrapbit	Packed bits. 0: The learning queue of the IN token is cleared; 1: Write pointer packing.
[6:5] RO		reserved	reserve.
[4:0] RO		intknwptr	IN Token Queue write pointer.

DTKNQR2

DTKNQR2 reads register 2 for Device IN Token Sequence Learning Queue.

Offset Address	Register Name	Total Reset Value
0x0824	DTKNQR2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	eptkn
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0] RO		eptkn	The endpoint number of the token. 4 bits per token are just the endpoint number of the token Bits[31:28]: endpoint number of Token 13; Bits[27:24]: Token 12 endpoint number; ..... Bits[7:4]: endpoint number of Token 7; Bits[3:0]: endpoint number of Token 6.

DTKNQR3

DTKNQR3 reads register 3 for Device IN Token Sequence Learning Queue.

Offset Address	Register Name	Total Reset Value
0x0830	DTKNQR3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	eptkn
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	eptkn	The endpoint number of the token. 4 bits per token are just the endpoint number of the token Bits[31:28]: Token 21 endpoint number; Bits[27:24]: endpoint number of Token 20; ..... Bits[7:4]: endpoint number of Token 15; Bits[3:0]: endpoint number of Token 14.

DTKNQR4

DTKNQR4 Read register 4 for Device IN Token Sequence Learning Queue.

Offset Address	Register Name	Total Reset Value
0x0834	DTKNQR4	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	eptkn
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RO	eptkn	The endpoint number of the token. 4 bits per token are just the endpoint number of the token Bits[31:28]: endpoint number of Token 29; Bits[27:24]: endpoint number of Token 28; ..... Bits[7:4]: endpoint number of Token 23; Bits[3:0]: endpoint number of Token 22.

DVBUSDIS

DVBUSDIS is the device VBUS discharge time register.

Offset Address	Register Name	Total Reset Value
0x0828	DVBUSDIS	0x0000_17D7

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dvbusdis
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 0 1 0 1

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	dvbusdis	Device Vbus discharge time.

DVBUSPULSE

DVBUSPULSE is the Device VBUS pulsing time register.

Offset Address	Register Name	Total Reset Value
0x082C	DVBUSPULSE	0x0000_05B8

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	dvbuspulse
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 0 1 1 1 0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	reserve.
[11:0]	RO	dvbuspulse	Device Vbus pulse time.

DTHRCTL

DTHRCTL is the device waterline control register.

Offset Address	Register Name	Total Reset Value
0x0830	DTHRCTL	0x0C10_0020

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved rxthrlen txthrlen
Reset	0 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	reserve.

[27] RW arbprken			Arbiter parking enabled. 0: forbidden; 1: enable.
[26] RO		reserved	reserve.
[25:17] RW rxthrlen			Receive waterline length.
[16] RW rxthren			Receive waterline enable. After enabling it, it may cause some problems in RxFIFO, especially in error cases such as RxError and Babble. 0: disable 1: enable
[15:13] RO		reserved	reserve.
[12:11] RW ahbthrratio			AHB Waterline Ratio. 00: AHB waterline = MAC waterline; 01: AHB waterline = MAC waterline / 2; 10: AHB waterline = MAC waterline / 4; 11: AHB waterline = MAC waterline / 8.
[10:2] RW txthrlen			Transmit waterline length.
[1] RW isothren			ISO IN Endpoints watermark enable. 0: forbidden; 1: enable.
[0] RW nonisothren			Non-ISO IN Endpoints watermark enable. 0: forbidden; 1: enable.

DEEPMPMSK

DIEPEMPMSK is the Device IN Endpoint FIFO Empty interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0834	DEEPMPMSK	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ineptxfempmsk
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0]	RW	ineptxfempmsk	IN EP Tx FIFO Empty interrupt mask. Bit[0] controls IN endpoint 0; ... Bit[15] controls endpoint 15.

DEACHINT

DEACHINT is the Device Each Endpoint interrupt register.

Offset Address	Register Name	Total Reset Value
0x0838	DEACHINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepint																of the pint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	echoutepint	OUT Endpoint interrupt. Bit[16] controls OUT endpoint 0; ... Bit[31] controls OUT endpoint 15.
[15:0]	RW	echinepint	IN Endpoint interrupt. Bit[15] controls IN endpoint 0; ... Bit[0] controls IN endpoint 15.

DEACHINTMSK

DEACHINTMSK is the Device Each Endpoint interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x083C	DEACHINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepmsk																echinapmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:16]	RW	echoutepmsk	OUT Endpoint interrupt mask. Bit[16] controls OUT endpoint 0; ... Bit[31] controls OUT endpoint 15. 0: Shield; 1: No shielding.
[15:0]	RW	echinepmsk	IN Endpoint interrupt mask. Bit[16] controls IN endpoint 0; ... Bit[31] controls IN endpoint 15. 0: Shield; 1: No shielding.

DIEPEACHMSKN

DIEPEACHMSKN is the device each in Endpoint-n interrupt register.

Offset Address	Register Name	Total Reset Value
0x0840ÿ(0x0004×n) (n = 0ÿ15)	DIEPEACHMSKN	0x0040_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

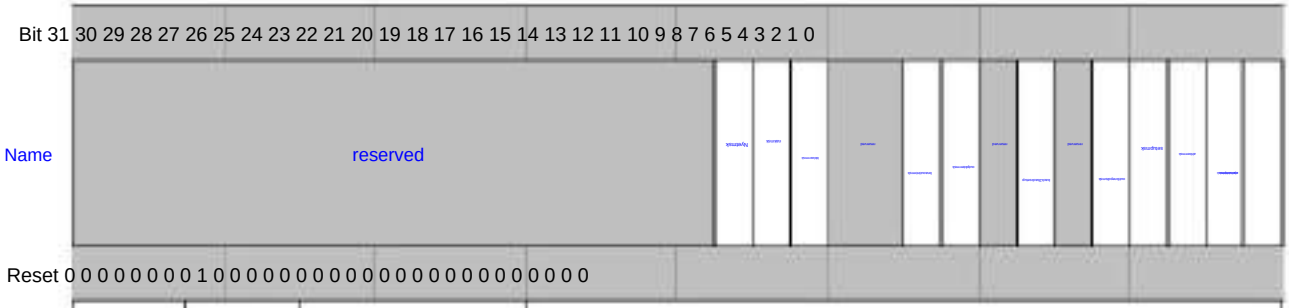
Bits	Access Name		Description
[31:14]	RO	reserved	reserve.

[13] RW nakmsk			NAK interrupt mask. 0: Shield; 1: No shielding.
[12:10] RO		reserved	reserve.
[9] RW bnainintrmsk			BNA interrupt mask. 0: Shield; 1: No shielding.
[8] RW txfifoundrnmsk			FIFO Underrun interrupt masking. 0: Shield; 1: No shielding.
[7]	RO	reserved	reserve.
[6] RW inepnakeffmsk			IN Endpoint NAK Effective Interrupt masking. 0: shielded; 1: not shielded.
[5] RW intknepmismsk			IN Token received with EP does not match interrupt mask. 0: Shield; 1: No shielding.
[4] RW intkntxfempmsk			IN Token Received When TxFIFO Empty interrupt mask. 0: Shield; 1: No shielding.
[3] RW timeoutmsk			Timeout interrupt mask (Non-isochronous endpoints). 0: Shield; 1: No shielding.
[2] RW ahberrmsk			AHB error interrupt mask. 0: Shield; 1: No shielding.
[1] RW epdisbldmsk			Endpoint failure interrupt mask. 0: Shield; 1: No shielding.
[0] RW xfercomplmsk			Transfer completes interrupt masking. 0: Shield; 1: No shielding.

DOEPEACHMSKN

DOEPEACHMSKN is the device each out Endpoint-n interrupt register.

Offset Address	Register Name	Total Reset Value
0x0880ÿ(0x0004×n) (n = 0ÿ15)	DOEPEACHMSKN	0x0080_0000



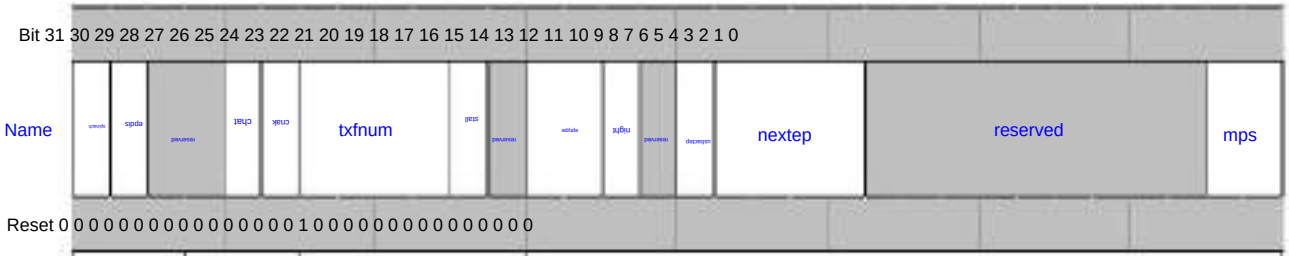
Bits	Access	Name	Description
[31:15]	RO	reserved	reserve.
[14]	RW	nyetmsk	NYET interrupt mask. 0: shielded; 1: not shielded.
[13]	RW	nakmsk	NAK interrupt mask. 0: Shield; 1: No shielding.
[12]	RW	bbleerrmsk	Babble error interrupt mask. 0: Shield; 1: No shielding.
[11:10]	RO	reserved	reserve.
[9]	RW	bnaoutintrmsk	BNA interrupt mask. 0: Shield; 1: No shielding.
[8]	RW	outpkterrmsk	OUT Packet error interrupt mask. 0: Shield; 1: No shielding.
[7]	RO	reserved	reserve.
[6]	RW	back2backsetup	Back-to-Back SETUP Packets Received interrupt mask. 0: Shield; 1: No shielding.
[5]	RO	reserved	reserve.

[4] RW	outknepdismsk		OUT Token Received when Endpoint Disabled Interrupt Mask. 0: Shield; 1: No shielding.
[3] RW	setupmsk		SETUP Phase Done interrupt mask. 0: Shield; 1: No shielding.
[2] RW	ahberrmsk		AHB error interrupt mask. 0: Shield; 1: No shielding.
[1] RW	epdisbldmsk		Endpoint Disabled interrupt masking. 0: Shield; 1: No shielding.
[0] RW	xfercomplmsk		Transfer completes interrupt masking. 0: Shield; 1: No shielding.

THEPCTL0

DIEPCTL0 is the Device Control IN Endpoint 0 control register.

Offset Address	Register Name	Total Reset Value
0x0900	THEPCTL0	0x0000_8000



Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable. When the IN endpoint is working in Scatter/Gather DMA mode, this bit is valid to indicate that the description substructure and data cache of the data to be sent have been established; when the Scatter/Gather DMA mode is disabled, this bit is valid to indicate that the data to be sent is ready. 0: invalid; 1: Valid.

[30] RWSC	epdis		Endpoint prohibited. The application program sets this bit to terminate data transmission for this endpoint. Enabled in DMA mode only. 0: invalid; 1: valid.
[29:28] RO		reserved	reserve.
[27] WO talk			NAK settings. A write operation sets the NAK bit of the endpoint. The application program can use this bit to control the NAK handshake of an endpoint during a transmission. The controller core can also set this bit of an endpoint after an endpoint receives a SETUP packet. 0: invalid; 1: Valid.
[26] Wo cnak			NAK cleared. A write operation clears the NAK bit of the endpoint. 0: invalid; 1: Valid.
[25:22] RW	txfnum		Number of TxFIFOs.
[21] RWSC	stall		STALL handshake. The application can set this bit, and the controller core clears this bit after the endpoint receives the SETUP packet. 0: invalid; 1: Valid.
[20] RO		reserved	reserve.
[19:18] RO		eptype	Endpoint type. 00: Control transfer endpoint; 01: Real-time transfer endpoint; 10: Bulk transfer endpoint; 11: Interrupt transfer endpoint.
[17] RO		night	NAK status. 0: non-NAK handshake sent; 1: NAK handshake is sent.
[16] RO		reserved	reserve.

[15] RO		usbactep	USB activates endpoint 0. This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid; 1: Valid.
[14:11] RO		nextep	Near Endpoint. Indicates the number of the next endpoint to receive data.
[10:2] RO		reserved	reserve.
[1:0] RW	mps		Minimum packet size. 00ÿ64 bytesÿ 01ÿ32 bytesÿ 10ÿ 16 bytesÿ 11ÿ8 bytesÿ

DOEPCTL0

DOEPCTL0 is the Device Control OUT Endpoint 0 control register.

Offset Address	Register Name	Total Reset Value
0x0B00	DOEPCTL0	0x0000_8000

Bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name: reserved | snp | reserved | mps

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enabled. Scatter/Gather DMA enable 0: Descriptor structure and data buffer receive data function disabled; 1: The descriptor structure and data buffer receive data function is enabled. Scatter/Gather DMA disable 0: Disable the function of memory receiving data directly from USB; 1: Enable the function of memory directly receiving data from USB.
[30] RO		epdis	The endpoint is disabled. The application cannot disable endpoint 0 of OUT control transfers 0: enable; 1: Disable.

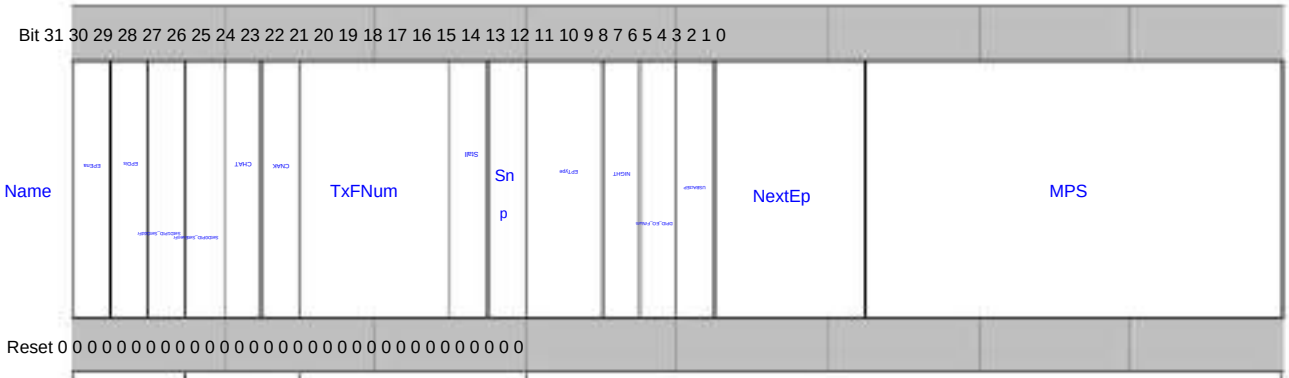
[29:28] RO		reserved	reserve.
[27] WO talk			NAK settings. A write operation sets the NAK bit of the endpoint. The application program can use this bit to control the NAK handshake of an endpoint during a transmission. The controller core can also set this bit of an endpoint after an endpoint receives a SETUP packet. 0: invalid; 1: Valid.
[26] Wo cnak			NAK cleared. A write operation clears the NAK bit of the endpoint. 0: invalid; 1: Valid.
[25:22] RO		reserved	reserve.
[21] RWSC stall			STALL handshake. The application can set this bit, and the controller core clears this bit after the endpoint receives the SETUP packet. 0: invalid 1: Valid
[20] RW snp			snoop mode. Set the endpoint to work in snoop mode. In snoop mode, the controller core sends OUT packets to the application memory before checking if the packets are correct. 0: invalid 1: valid
[19:18] RO		eptype	The type of endpoint. 00: Control transfer endpoint; 01: Real-time transfer endpoint; 10: Bulk transfer endpoint; 11: Interrupt transfer endpoint.
[17] RO		night	NAK status. 0: non-NAK handshake sent; 1: NAK handshake is sent.
[16] RO		reserved	reserve.
[15] RO		usbactep	USB activates endpoint 0. This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid; 1: Valid.
[14:2] RO		reserved	reserve.

[1:0] RW mps			Minimum packet size. 00ÿ64 bytesÿ 01ÿ32 bytesÿ 10ÿ16 bytesÿ 11ÿ8 bytesÿ

DEEPCTLN

DIEPCTLN is the Device IN Endpoint-n control register.

Offset Address	Register Name	Total Reset Value
0x0900ÿ(0x0020×n) (n = 0ÿ15)	DEEPCTLN	0x0000_0000



Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable. When Scatter/Gather DMA is enabled. 0: Descriptor structure and data buffer send data function disabled; 1: Descriptor structure and data buffer send data function is enabled. When Scatter/Gather DMA is disabled. 0: The data on the endpoint is not ready; 1: The data on the endpoint is ready.
[30]	RWSC	EPDis	The endpoint is disabled. Applies to both IN and OUT endpoints. Setting this bit by the application stops sending/receiving data to this endpoint. 0: enable; 1: Disable.

[29] WHERE	Invalid; Fr	SetD1PID_SetOdd	DATA1 PID setting/odd microframe setting. Interrupt endpoints, Bulk IN and Bulk OUT endpoints: The Data PID of the endpoint can be set to DATA1 by setting this bit. 0: 1: Valid. Live IN and OUT endpoints: Even or odd numbered microframes can be set to odd numbered microframes by setting this bit 0: invalid; 1: Valid.
[28] WHERE	SetD0PID_SetEven 1: Fr	valid.	DATA0 PID setting/even microframe setting. Interrupt endpoints, Bulk IN and Bulk OUT endpoints: By setting this bit, the Data PID of the endpoint can be set to DATA0 0: invalid; Live IN and OUT endpoints: By setting this bit, the even or odd numbered microframe can be set as an even numbered microframe 0: invalid; 1: Valid.
[27] WO TALK			NAK settings. A write operation sets the NAK bit of the endpoint. The application program can use this bit to control the NAK handshake of an endpoint during a transmission. For an OUT endpoint, the controller core can set this bit of the endpoint when it receives a transfer completion interrupt, or after the endpoint receives a SETUP packet. 0: invalid; 1: Valid.
[26] WO CNAK			NAK cleared. Applies to both IN and OUT endpoints A write operation clears the NAK bit for this endpoint 0: invalid; 1: Valid.
[25:22] RW TxFNum			Number of TxFIFOs Shared FIFO Operationÿ 0ÿNon-Periodic TxFIFOÿ Others: Specified Periodic TxFIFO.number. Dedicated FIFO Operation: FIFO quantity indication. Valid only for IN Endpoints.

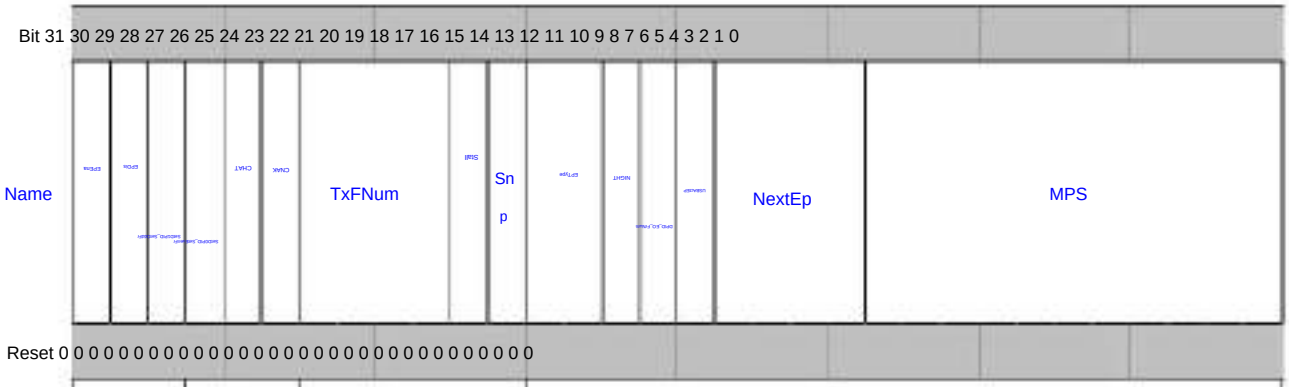
[21] RW Stall			STALL handshake. IN and OUT endpoints for non-control transfers and non-real-time transfers. Setting this bit by the application blocks token packets sent by the USB host controller to the endpoint. 0: invalid; 1: Valid. For the control endpoint (RWSC), this bit can only be set by the application program and cleared by the controller core when the endpoint receives a SETUP token. 0: invalid; 1: Valid.
[20] RW Snp			snoop mode. Applicable to OUT endpoint only. This bit configures the endpoint to work in snoop mode, and the controller core does not check the correctness of the packet before transferring the OUT packet to the application memory. 0: invalid; 1: Valid.
[19:18] RW	EPType		endpoint type. 00: Control transfer endpoint; 01: Real-time transfer endpoint; 10: Bulk transfer endpoint; 11: Interrupt transfer endpoint.
[17] RO	NIGHT		NAK status. 0: non-NAK handshake sent; 1: NAK handshake is sent.
[16] RO		DPID_EO_FrNum	Endpoint data PID. 0ÿDATE0ÿ 1ÿDATA1ÿ Even/Odd Frame. non-Scatter/Gather DMA modeÿ 0: even frame; 1: Odd frames. Scatter/Gather DMA modeÿ reserve.
[15] RWSC	USBActEP		The USB endpoint activates the endpoint. Applies to IN endpoints and OUT endpoints, indicates whether the endpoint is valid. 0: invalid 1: Valid

[14:11] RW	NextEp		near endpoint. Indicates the number of the next endpoint to receive data.
[10:0] RW	MPS		Maximum packet size.

DOEPCTLN

DOEPCTLN is the Device OUT Endpoint-n control register.

Offset Address	Register Name	Total Reset Value
0x0B00ÿ(0x0020×n) (n = 0ÿ15)	DOEPCTLN	0x0000_0000



Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable. When Scatter/Gather DMA is enabled 0: Descriptor structure and data buffer receive data function disabled; 1: The descriptor structure and data buffer receive data function is enabled. When Scatter/Gather DMA is disabled 0: The function of memory directly receiving data from USB is disabled; 1: The function of memory directly receiving data from USB is enabled.
[30]	RWSC	EPDis	The endpoint is disabled. Applies to both IN and OUT endpoints. Setting this bit by the application stops sending/receiving data to this endpoint. 0: enable; 1: Disable.

[29] WHERE		Invalid; Fr SetD1PID_SetOdd	DATA1 PID setting/odd microframe setting. Interrupt endpoints, Bulk IN and Bulk OUT endpoints: The Data PID of the endpoint can be set to DATA1 by setting this bit. 0: 1: Valid. Live IN and OUT endpoints: Even or odd numbered microframes can be set to odd numbered microframes by setting this bit 0: invalid; 1: Valid.
[28] WHERE		SetD0PID_SetEven Fr 1: valid	DATA0 PID setting/even microframe setting. Interrupt endpoints, Bulk IN and Bulk OUT endpoints: By setting this bit, the Data PID of the endpoint can be set to DATA0 0: invalid Real-time IN and OUT endpoints: By setting this bit, you can set even or odd numbered microframes to even numbered microframes 0: invalid 1: valid
[27] WO TALK			NAK settings. A write operation sets the NAK bit of the endpoint. The application program can use this bit to control the NAK handshake of an endpoint during a transmission. For an OUT endpoint, the controller core can set this bit of the endpoint when it receives a transfer completion interrupt, or after the endpoint receives a SETUP packet. 0: invalid; 1: Valid.
[26] WO CNAK			NAK cleared. Applies to both IN and OUT endpoints A write operation clears the NAK bit for this endpoint 0: invalid; 1: Valid.

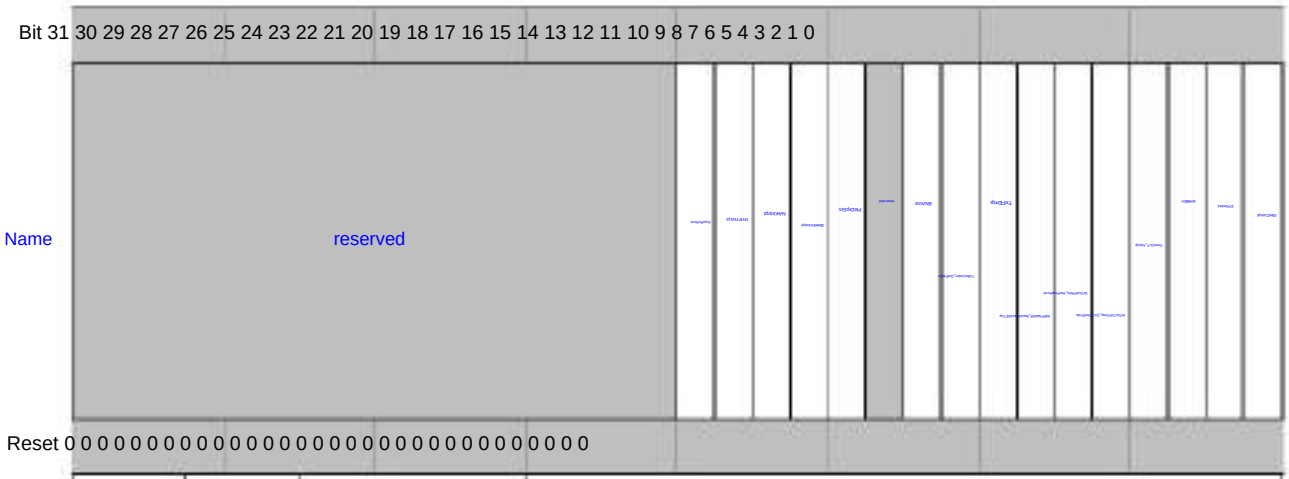
[25:22] RW TxFNum			Number of TxFIFOs. Shared FIFO Operationÿ 0ÿNon-Periodic TxFIFOÿ Others: Specified Periodic TxFIFO.number. Dedicated FIFO Operation: FIFO quantity indication. Valid only for IN Endpoints.
[21] RW Stall			STALL handshake (RW). IN and OUT endpoints for non-control transfers and non-real-time transfers. The application sets this bit to block token packets sent by the USB host controller to the endpoint. 0: invalid; 1: Valid. For the control endpoint (RWSC), this bit can only be set by the application program and cleared by the controller core when the endpoint receives a SETUP token. 0: invalid; 1: Valid.
[20] RW Snp			snoop mode. Applies to OUT endpoints only. Configure the endpoint to work in the snoop mode. In the snoop mode, the controller core does not check the correctness of the OUT packet before transferring it to the application memory. 0: invalid; 1: Valid.
[19:18] RW EPType			endpoint type. 00: Control transfer endpoint; 01: Real-time transfer endpoint; 10: Bulk transfer endpoint; 11: Interrupt transfer endpoint.
[17] RO NIGHT			NAK status. 0: non-NAK handshake sent; 1: NAK handshake is sent.

[16] RO		DPID_EO_FrNum	Endpoint data PID. 0ÿDATE0ÿ 1ÿDATA1 Even/Odd Frame. non-Scatter/Gather DMA modeÿ 0: even frame; 1: Odd frames. Scatter/Gather DMA modeÿ reserve.
[15] RWSC	USBActEP		The USB endpoint activates the endpoint. Applies to IN endpoints and OUT endpoints, indicates whether the endpoint is valid. 0: invalid; 1: Valid.
[14:11] RW	NextEp		Near Endpoint. Indicates the number of the next endpoint to receive data.
[10:0] RW	MPS		Maximum packet size.

DIEPINTn

DIEPINTn is the Device IN Endpoint-n interrupt register.

Offset Address	Register Name	Total Reset Value
0x0908ÿ(0x0020×n) (n = 0ÿ15)	DIEPINTn	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

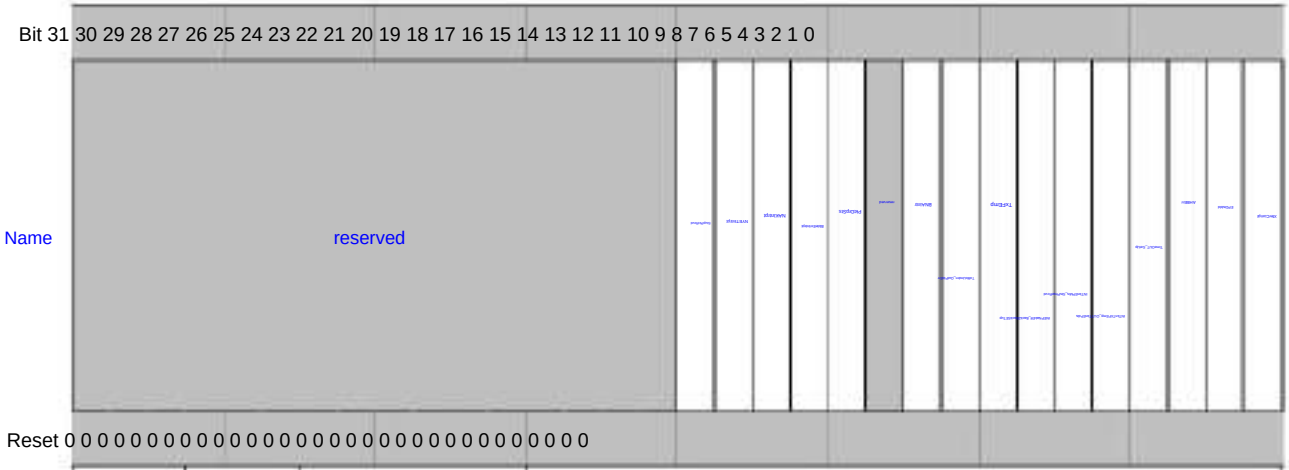
[15] RWSC	StupPktRcvd		Received setup package. 0: no setup package received; 1: setup package received.
[14] RWSC	NYETIntrpt		NYET interruptÿ Interrupted while NYET response was sent. 0: clear; 1: Interrupt.
[13] RWSC	NAKIntrpt		NAK interrupted. Interrupt when NAK is sent. 0: clear; 1: Interrupt.
[12] RWSC	BbleErrIntrpt		Babble error interrupt. The endpoint interrupts when it receives a babble. 0: clear; 1: Interrupt.
[11] RWSC	PktDrpSts		The packet loss state is interrupted. 0: Clear; 1: Interrupt.
[10] RO		reserved	reserve.
[9]	RWSC	BNAIntr	BNA interrupted. Abort occurs when descriptor access is not ready. 0: clear; 1: Interrupt.
[8]	RWSC	TxfifoUndrn_OutP ktErr OUT packet error.	FIFO Underrun interrupted. An interrupt occurs when a FIFO underrun condition is sent. Interrupts are enabled when the following conditions are met: - OTG_EN_DED_TX_FIFO=1; - Thresholding enable. An interrupt occurs when an overflow or CRC error is detected. Interrupts are enabled when the following conditions are met: - OTG_EN_DED_TX_FIFO=1; - Thresholding enable.

[7]	RO	TxFEmp	Transmit FIFO empty status interrupt. Interrupt occurs when TxFIFO is full or half empty. 0: clear; 1: Interrupt. 说明 This bit is only valid for IN Endpoint.
[6]	RWSC	INEPNakEff_Back2BackSETup core interrupt	IN Endpoint NAK Effective abort. An interrupt occurs when the IN Endpoint bit has been set. Receive the Back-to-Back SETUP package. when receiving more than 3 back-to-back SETUP packets. 0: clear; 1: Interrupt.
[5]	RWSC	INTknEPMis_StsPhseRcvd 0: Clear;	Interrupt indicating receipt of IN Token with mismatched EP. Indicates the receipt of a status pulse for Control Write. 1: Receive.
[4]	RWSC	INTknTXFEmp_OUTTknEPdis 0: clear;	When the corresponding TxFIFO is empty, an interrupt occurs when an IN Token is received. When the Endpoint fails, the OUT Token is received and interrupted. 1: Interrupt.
[3]	RWSC TimeOUT_SetUp		A timeout condition interrupts. Indicates that an interrupt occurred when a timeout condition was detected. SETUP Phase Done aborted. 0: clear; 1: Interrupt.
[2]	RWSC AHBErr		AHB error interrupt. AHB error occurs only when AHB read/write in Internal DMA mode. 0: clear; 1: Interrupt.
[1]	RWSC EPDisbld		Endpoint failure interrupt. 0: Clear; 1: Interrupt.
[0]	RWSC XferCompl		Transfer complete interrupt. 0: clear; 1: Interrupt.

DOEPINTn

DOEPINTn is the Device OUT Endpoint-n interrupt register.

Offset Address	Register Name	Total Reset Value
0x0B08ÿ(0x0020×n) (n = 0ÿ15)	DOEPINTn	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RWSC	StupPktRcvd	Received setup package. 0: no setup package received; 1: setup package received.
[14]	RWSC	NYETIntrpt	NYET interruptÿ Interrupted while NYET response was sent. 0: clear; 1: Interrupt.
[13]	RWSC	NAKIntrpt	NAK interrupted. Interrupt when NAK is sent. 0: clear; 1: Interrupt.
[12]	RWSC	BbleErrIntrpt	Babble error interrupt. The endpoint interrupts when it receives a babble. 0: clear; 1: Interrupt.
[11]	RWSC	PktDrpSts	Packet loss status interrupt 0: clear; 1: interrupt.

[10] RO		reserved	reserve.
[9]	RWSC	BNAIntr	BNA interrupted. Abort occurs when descriptor access is not ready. 0: clear; 1: Interrupt.
[8]	RWSC	TxfifoUndrn_OutP ktErr OUT packet error.	FIFO Underrun interrupted. An interrupt occurs when a FIFO underrun condition is sent. Interrupts are enabled when the following conditions are met: - OTG_EN_DED_TX_FIFO=1; - Thresholding enable. An interrupt occurs when an overflow or CRC error is detected. Interrupts are enabled when the following conditions are met: - OTG_EN_DED_TX_FIFO=1; - Thresholding enable.
[7]	RO	TxFEmp	Transmit FIFO empty status interrupt. Interrupt occurs when TxFIFO is full or half empty. This bit is only valid for IN Endpoint. 0: clear; 1: Interrupt.
[6]	RWSC	INEPNakEff_Back 2BackSETup core	IN Endpoint NAK Effective abort. An interrupt occurs when the IN Endpoint bit has been set. Receive the Back-to-Back SETUP package. interrupt when receiving more than 3 back-to-back SETUP packets. 0: Clear; 1: Interrupt.
[5]	RWSC	INTknEPMis_StsP hseRcvd 0: Clear;	Indicates that an IN Token with a mismatched EP was received. Indicates the receipt of a status pulse for Control Write. 1: Interrupt.
[4]	RWSC	INTknTXFEmp_O UTTknEPdis 0: clear;	When the corresponding TxFIFO is empty, an interrupt occurs when an IN Token is received. When the Endpoint fails, the OUT Token is received and interrupted. 1: Interrupt.

[3]	RWSC TimeOUT_SetUp		A timeout condition interrupts. Indicates that an interrupt occurred when a timeout condition was detected. SETUP Phase Done is interrupted. 0: Clear; 1: Interrupt.
[2]	RWSC AHBErr		AHB error interrupt. AHB error occurs only when AHB read/write in Internal DMA mode. 0: clear; 1: Interrupt.
[1]	RWSC EPDisbld		Endpoint failure interrupt. 0: clear; 1: Interrupt.
[0]	RWSC XferCompl		Transfer complete interrupt. 0: clear; 1: Interrupt.

DIEPTSIZ0

DIEPTSIZ0 is the transfer size register for Device IN Endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0910	DIEPTSIZ0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	MCNT	reserved	XferSize
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	reserve.
[20:19]	RW	PktCnt	number of packets.
[18:7]	RO	reserved	reserve.
[6:0]	RW	XferSize	transfer size.

DOEPTSIZ0

DOEPTSIZ0 is the Device OUT Endpoint 0 transfer size register.

Offset Address	Register Name	Total Reset Value
0x0B10	DOEPTSIZ0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reserved																	reserved										XferSize			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30:29]	RW	SUPCnt	SETUP package statistics. 00ÿ0 packetsÿ 01ÿ1 packetsÿ 10ÿ2 packetsÿ 11ÿ3 packetsÿ
[28:20]	RO	reserved	reserve.
[19]	RW	PktCnt	number of packets.
[18:7]	RO	reserved	reserve.
[6:0]	RW	XferSize	transfer size.

DIEPTSIZn

DIEPTSIZn is the Device IN Endpoint-n transfer size register.

Offset Address	Register Name	Total Reset Value
0x0910ÿ(0x0020×n) (n = 0ÿ15)	DIEPTSIZn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PktCnt																	XferSize													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.

[30:29] RW	mc_rxdpid_supcnt		Packet statistics (IN endpoint) (RW). 00ÿ0 packetsÿ 01ÿ1 packetsÿ 10ÿ2 packetsÿ 11: 3 packets. Packet statistics (Non-periodic IN endpoints) (RO). This bit is only valid in internal DMA mode. Received data PID (isochronous OUT endpoints) (RO). 00ÿDATE0ÿ 01ÿDATA2ÿ 10ÿDATA1ÿ 11ÿMDATAÿ SETUP packet statistics (OUT Endpoint) (RW) 01: 1 packet; 10ÿ2 packetsÿ 11ÿ3 packetsÿ
[28:19] RW	PktCnt		number of packets.
[18:0] RW	XferSize		transfer size.

DOEPTSIZn

DOEPTSIZn is the Device OUT Endpoint-n transfer size register.

Offset Address	Register Name	Total Reset Value
0x0B10ÿ(0x0020×n) (n = 0ÿ15)	DOEPTSIZn	0x0000_0000

Bit	31	30 29	28 27 26 25 24 23 19	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	---	---	PktCnt	XferSize
Reset	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	reserve.

[30:29] RW	mc_rxdpid_supcnt		Packet statistics (IN endpoint) (RW). 00ÿ0 packetsÿ 01ÿ1 packetsÿ 10ÿ2 packetsÿ 11: 3 packets; Packet statistics (Non-periodic IN endpoints) (RO) This bit is only valid in internal DMA mode. Received data PID (isochronous OUT endpoints) (RO). 00ÿDATE0ÿ 01ÿDATA2ÿ 10ÿDATA1ÿ 11ÿMDATAÿ SETUP package statistics (OUT Endpoint) (RW). 01: 1 packet; 10ÿ2 packetsÿ 11ÿ3 packetsÿ
[28:19] RW	PktCnt		number of packets.
[18:0] RW	XferSize		transfer size.

DIEPDMAN

DIEPDMAN is the Device IN Endpoint-n DMA address register.

Offset Address	Register Name	Total Reset Value
0x0914ÿ(0x0020×n) (n = 0ÿ15)	DIEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address.

DOEPDMAN

DOEPDMAN is the Device OUT Endpoint-n DMA address register.

Offset Address	Register Name	Total Reset Value
0x0B14ÿ(0x0020×n) (n = 0ÿ15)	DOEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address.

DIEPDMABN

DIEPDMABN is the address register of Device IN Endpoint-n DMA buffer.

Offset Address	Register Name	Total Reset Value
0x091Cÿ(0x0020×n) (n = 0ÿ15)	DIEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address.

DOEPDMABN

DOEPDMABN is the address register of Device OUT Endpoint-n DMA buffer.

Offset Address	Register Name	Total Reset Value
0x0B1Cÿ(0x0020×n) (n = 0ÿ15)	DOEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address.

DTXFSTSn

DTXFSTSn is the Device IN Endpoint Transmit FIFO status register

Offset Address	Register Name	Total Reset Value
0x0938	DTXFSTSn	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	INEPTxFSpcAvail
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	INEPTxFSpcAvail	IN Endpoint TxFIFO space availability. 0x0: Endpoint TxFIFO is full; 0x1: 1 word is available; 0x2: 2 words available; 0xn: n words available (0 ÿ n ÿ 32,768); 0x8000: 32,768 words available; Other: reserved.

12.10 USB3.0 DRD

12.10.1 Overview

The USB3.0 DRD (Dule Role Device) module supports the static operation of USB3.0 host and USB3.0 device, that is, it only needs to configure the relevant registers to make the module work in USB3.0 host or USB3.0 device mode; this module Support the 5Gbit/s transmission rate stipulated in the USB3.0 protocol and backward compatible with the 480Mbit/s transmission rate stipulated in the USB2.0 protocol; fully support the XHCI 1.0 protocol; support the pipe interface protocol for super-speed transmission and the UTMI interface protocol for high-speed transmission; A Root Hub is integrated inside the module, which can expand the USB interface or other Hubs; most of the hardware logic of the USB3.0 DRD controller can be completed:

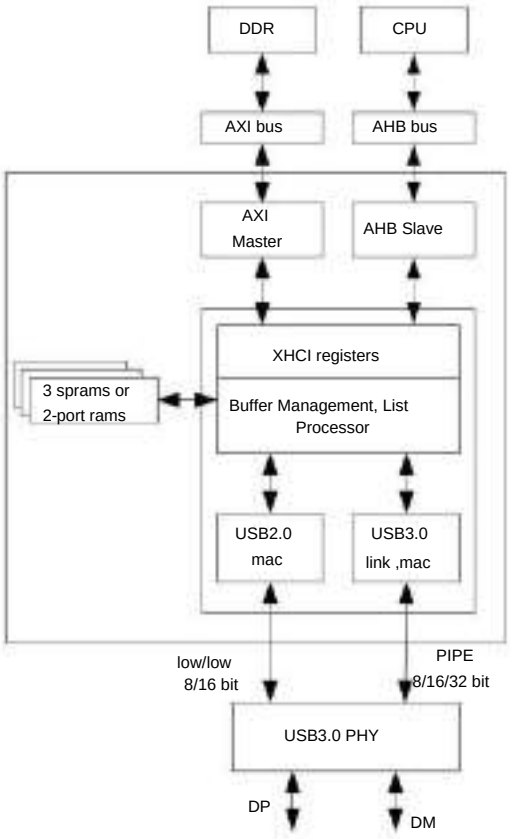
- Complete control and processing of transmissions
- Parsing and packaging of data packets
- Coding and decoding of USB transmission signals
- Provide drivers with interfaces such as interrupt vectors

12.10.2 Functional description

Logic block diagram

The logic block diagram of USB 3.0 DRD is shown in Figure 12-61 .

Figure 12-64 USB 3.0 DRD logic block diagram



UTMIÿUSB2.0 Transceiver Macrocell Interface

XHCIÿeXtensible Host Controller Interface

typical application

The reference design of the USB 3.0 DRD is shown in Figure 12-63 .

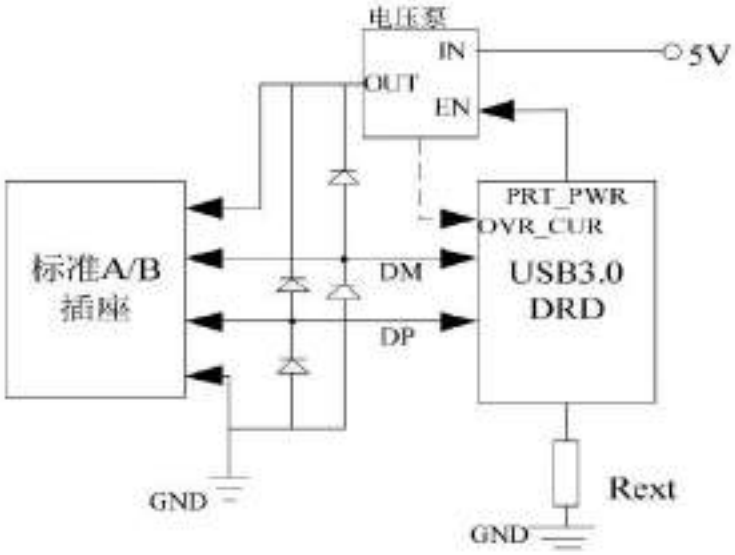
注意

The single-ended impedance of DP and DM is 45ÿ±1%, so DP and DM do not need any external matching resistors.

The accuracy of the REXT resistor is ±1%.

High-speed ESD devices need to be used, and the recommended capacitance value is about 1pF.

Figure 12-65 USB 3.0 DRD Reference Design



Features

The USB 3.0 DRD has the following features:

Fully compatible with USB3.0 and backward compatible with USB 2.0.

Fully compliant with XHCI 1.0.

Can work independently in Host or Device mode. Can support

Super-speed, High-speed, Full-speed, Low-speed four devices. Support USB 2.0 low power consumption solution

and four power consumption states of U0, U1, U2 and U3 of USB3.0. Support Control Transfer, Bulk Transfer, Isochronous Transfer,

Interrupt Transfer Four basic data transfer types. Supports four basic data transfer types: Control Transfer, Bulk Transfer, Isochronous Transfer, and Interrupt Transfer in Device working mode.

Supports internal DMA controller. Up

to 127 devices can be connected by connecting the USB Hub.

working principle

When USB 3.0 DRD works in host mode, it supports the following four standard transmission methods:

Control Transfer

It is mainly used for the transmission between USB Host and USB Device endpoint 0, and the control transmission of certain types of USB devices may use other endpoints. Control transmission is two-way transmission, and the amount of data is usually small. It can transmit 8byte, 16byte, 32byte or 64byte data, depending on the device and transmission speed.

Bulk Transfer (bulk transfer) is mainly

used to send and receive a large amount of data without bandwidth and interval time requirements. This type of device is suitable for very slow transmission and a large amount of delayed transmission. It can wait until all other types of data Send and receive data after the transfer is complete. Its characteristic is to ensure that the data of USB Host and USB Device is sent without error by means of error detection and retransmission.

Isochronous Transfer (synchronous transfer) is

mainly used for streaming data transmission with strict time and strong fault tolerance, or for real-time applications with constant data transmission rate. Isochronous transmission provides deterministic bandwidth and interval time.

Interrupt Transfer (interrupt transfer) is mainly

used for the transmission of small amount, scattered and unpredictable data. In the interrupt transmission mode, periodically check whether the device has interrupt data to send. The structure of the endpoint mode device of the device determines its query frequency is 1ms ~ 255ms. Typical interrupt mode transmission is unidirectional, and there is only input mode for USB Host.

When USB3.0 DRD works in Device mode, it supports Control Transfer (control transfer), Bulk Transfer (bulk transfer), Isochronous Transfer (synchronous transfer) and Interrupt Transfer (interrupt transfer).

12.10.3 Working method

clock reset

Before initializing the controller, configure the clock reset register accordingly.

The procedure for shutting down the clock is as follows:

Step 1. Write 0xF9 to PERI_CRG45 to release U2PHY reset.

Step 2. Write 0x1F01 to PERI_CRG46, U3 controller UTMI clock source select U2PHY supply.

Step 3. Write 0x1 to PERI_CRG43[9] to select COMPHYPHY reference clock 25M.

Step 4. Write 0x1 to PERI_CRG43[8] to enable COMPHY clock gating.

Step 5. Write 0x1 to PERI_CRG43[1], the COMPHY port soft reset mode selection is controlled by PERI_CRG45[0] system.

Step 6. Write 0x0 to PERI_CRG43[0] to release COMPHY from reset.

Step 7. Write 0x0 to PERI_CRG46[0] to remove the reset of U3 controller.

----Finish

Host/device working mode switching

The switching operation is as follows:

Write 2'b01 to PERI_USB3_GCTL [prtcapdir], DRD controller will work in Host mode. Write 2'b10 to PERI_USB3_GCTL [prtcapdir], DRD controller will work in Device mode.

注意

Host/Device working mode switching only supports static switching, not dynamic switching.

12.10.4 Register overview

The USB3.0 register overview is shown in Table 12-37 .

Table 12-37 USB3.0 register overview (base address is 0x1018_0000)

offset address name	describe	page number
0xC100 PERI_USB3_GSBUS CFG0	Global SOC Bus Configuration Register 0	12-311
0xC104 PERI_USB3_GSBUS CFG1	Global SOC Bus Configuration Register 1	12-313
0xC108 PERI_USB3_GTXT HRCFG	Global Transmit Threshold Control Register	12-314
0xC10C PERI_USB3_GRXT HRCFG	Global Receive Threshold Control Register	12-315
0xC110 PERI_USB3_GCTL global core control register		12-315
0xC118 PERI_USB3_GSTS global status register		12-320
0xC11C PERI_USB3_GUCTL [1]	Global User Control Register 1	12-321
0xC124 PERI_USB3_GGPIO Global GPIO register		12-322
0xC128 PERI_USB3_GUID global user ID register		12-322
0xC12C PERI_USB3_GUCTL Global User Control Register		12-322
0xC130 PERI_USB3_GBUSE RRADDR_EN	Global Bus Error Address Upper 32-bit Register	12-324
0xC134 PERI_USB3_GBUSE RRADDR_LO	Global bus error address lower 32-bit register	12-324
0xC138 PERI_USB3_GPRTB IMAP_EN	SuperSpeed Port - Bus Map Upper 32-Bit Register 12-325	

offset address name	describe	page number
0xC13C PERI_USB3_GPRTB IMAP_LO	SuperSpeed Port - Bus Mapping Lower 32-Bit Register 12-325	
0xC180 PERI_USB3_GPRTB IMAP_HS_HI	High Speed Port-Bus Mapping Upper 32-Bit Register 12-326	
0xC184 PERI_USB3_GPRTB IMAP_HS_LO	High Speed Port-Bus Mapping Lower 32-Bit Register 12-326	
0xC188 PERI_USB3_GPRTB IMAP_FS_HI	Full-Speed Port-Bus Mapping Upper 32-Bit Register 12-326	
0xC18C PERI_USB3_GPRTB IMAP_FS	Full-Speed Port-Bus Mapping Lower 32-Bit Register 12-327	
0xC200 PERI_USB3_GUSB2 PHYCFGN	Global USB2.0 PHY configuration registers	12-327
0xC2C0 PERI_USB3_GUSB3 PIPECTLN	Global USB3.0 PIPE Control Register	12-329
0xC304	PERI_USB3_GTXFI FACIST	Global Transmit FIFO Size Register	12-333
0xC384 PERI_USB3_GRXFI FACIST	Global Receive FIFO Size Register	12-333
0xC410 PERI_USB3_GEVN TADRN_EN	Global event buffer address high 32-bit register 12-334	
0xC414 PERI_USB3_GEVN TADRN_LO	The lower 32-bit register of the address of the global event buffer is 12-334	
0xC418 PERI_USB3_GEVN TSIZN	The size register of the global event buffer	12-334
0xC41C PERI_USB3_GEVN TCOUNTN	Global event buffer count register	12-335
0xC610	PERI_USB3_GTXFI FOPRIDEV	Global TX FIFO DMA Priority Register for Peripherals 12-335	
0xC618	PERI_USB3_GTXFI FOPRIHST	Host Global TX FIFO DMA Priority Register 12-336	
0xC61C PERI_USB3_GRXFI FOPRIHST	Host's Global RX FIFO DMA Priority Register 12-336	
0xC620	PERI_USB3_GFIFO PRIDBC	DMA priority register for the global Debug performance of the host	12-337
0xC624 PERI_USB3_GDMA HLRATIO	Host's global FIFO DMA high and low priority ratio register	12-338
0xC630 PERI_USB3_GFLAD J	GFLADJ Global Frame Length Adjustment Register 12-338	

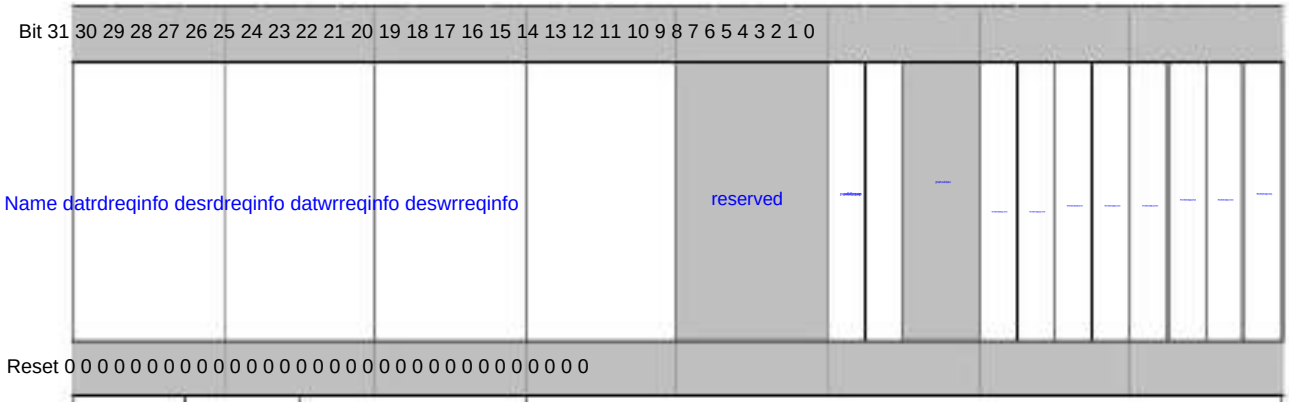
offset address	name	describe	page number
0xC700	PERI_USB3_DCFG	peripheral configuration register	12-340
0xC704	PERI_USB3_DCTL	peripheral control register	12-341
0xC708	PERI_USB3_DEVTEN	Peripheral Event Enable Register	12-344
0xC70C	PERI_USB3_DSTS	peripheral status register	12-346
0xC710	PERI_USB3_DGCMDPAR	Peripheral Class Command Parameter Register	12-348
0xC714	PERI_USB3_DGCMD	Peripheral Class Command Register	12-348
0xC718	PERI_USB3_DALEPEN	Peripheral USB Endpoint Enable Register	12-349
0xC810	PERI_USB3_DEPCMDPAR2N	Peripheral Endpoint Command Parameter Register 2	12-350
0xC814	PERI_USB3_DEPCMDPAR1N	Peripheral Endpoint Command Parameter Register 1	12-350
0xC818	PERI_USB3_DEPCMDPAR0N	Peripheral Endpoint Command Parameter Register 0	12-351
0xC81C	PERI_USB3_DEPCMDN	Peripheral Physical Endpoint Command Register	12-351

12.10.5 USB3.0 Register Description

PERI_USB3_GSBUSCFG0

PERI_USB3_GSBUSCFG0 is global SOC bus configuration register 0.

Offset Address	Register Name	Total Reset Value
0xC100	PERI_USB3_GSBUSCFG0	0x0000_0000



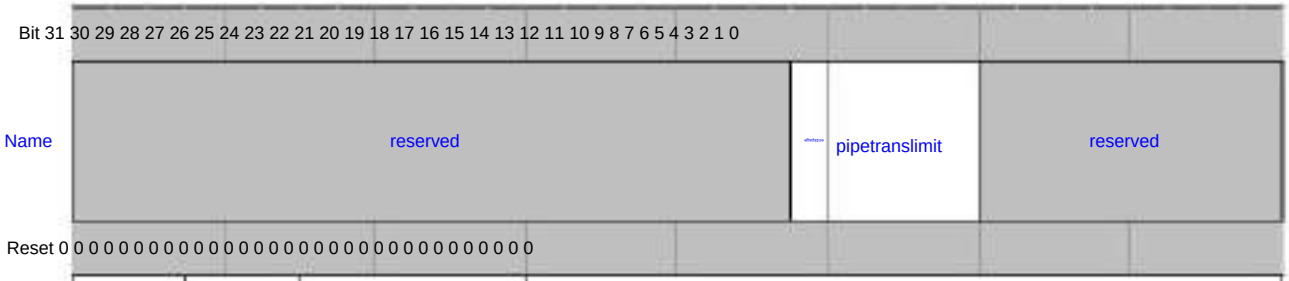
Bits	Access	Name	Description
[31:28]	RW	datrdreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Request to read data.
[27:24]	RW	desrdreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo read linked list request.
[23:20]	RW	datwrreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo write data request.
[19:16]	RW	deswrreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Write linked list request.
[15:12]	RW	reserved	reserve.
[11]	RW	datbigend	Data access endian selection. 0: little endian; 1: Big endian.
[10]	RW	descbigend	Endian selection for linked list access. 0: little endian; 1: Big endian.
[9:8]	RO	reserved	reserve.
[7]	RW	incr256brstena	AHB master INCR enables signal for 128 beat burst transmission. 0: disable; 1: enable.
[6]	RW	incr128brstena	AHB master INCR enables signal for 128 beat burst transmission. 0: disable; 1: enable.
[5]	RW	incr64brstena	AHB master INCR 64 beat burst transmission enable signal. 0: disable; 1: enable.

[4] RW	incr32brstena		AHB master INCR 32 beat burst transmission enable signal. 0: disable; 1: enable.
[3] RW	incr16brstena		AHB master INCR 16 beat burst transmission enable signal. 0: disable; 1: enable.
[2] RW	incr8brstena		AHB master INCR 8 beat burst transmission enable signal. 0: disable; 1: enable.
[1] RW	incr4brstena		AHB master INCR 4 beat burst transmission enable signal. 0: disable; 1: enable.
[0] RW	incrbrstena		AHB master INCR 1 beat burst transmission enable signal. 0: disable; 1: enable.

PERI_USB3_GSBUSCFG1

PERI_USB3_GSBUSCFG1 is global SOC bus configuration register 1.

Offset Address	Register Name	Total Reset Value
0xC104	PERI_USB3_GSBUSCFG1	0x0000_0000



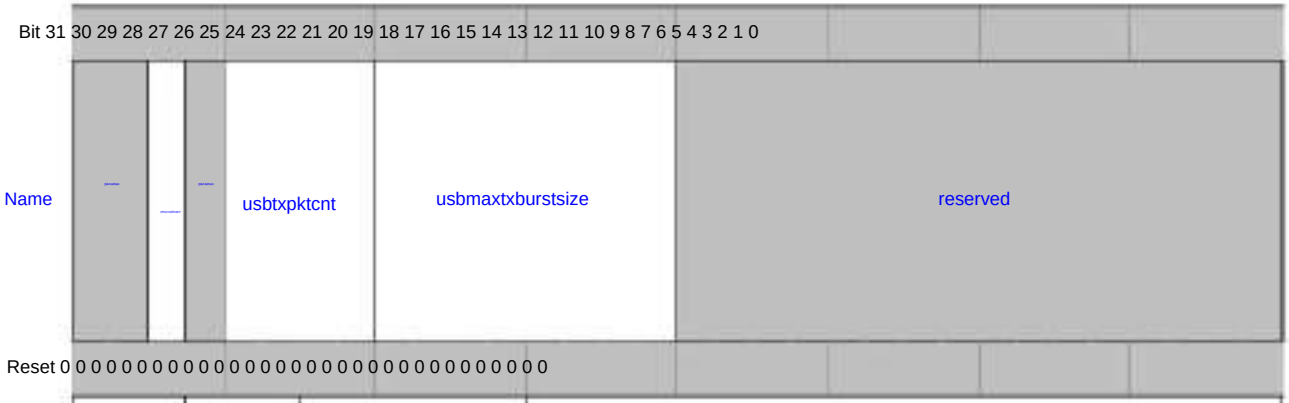
Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12]	RW	en1kpage	1K Byte boundary selection. 0: 4K Byte boundary; 1: 1K Byte boundary.

[11:8] RW	pipetranslimit		The number of AXI master outstanding requests. 0x0: 1 request; 0x1: 2 requests; 0x2: 3 requests; 0x3: 4 requests; … 0xF: 16 requests.
[7:0] RO		reserved	reserve.

PERI_USB3_GTXTHRCFG

PERI_USB3_GTXTHRCFG is the global transmit threshold control register.

Offset Address	Register Name	Total Reset Value
0xC108	PERI_USB3_GTXTHRCFG	0x0000_0000

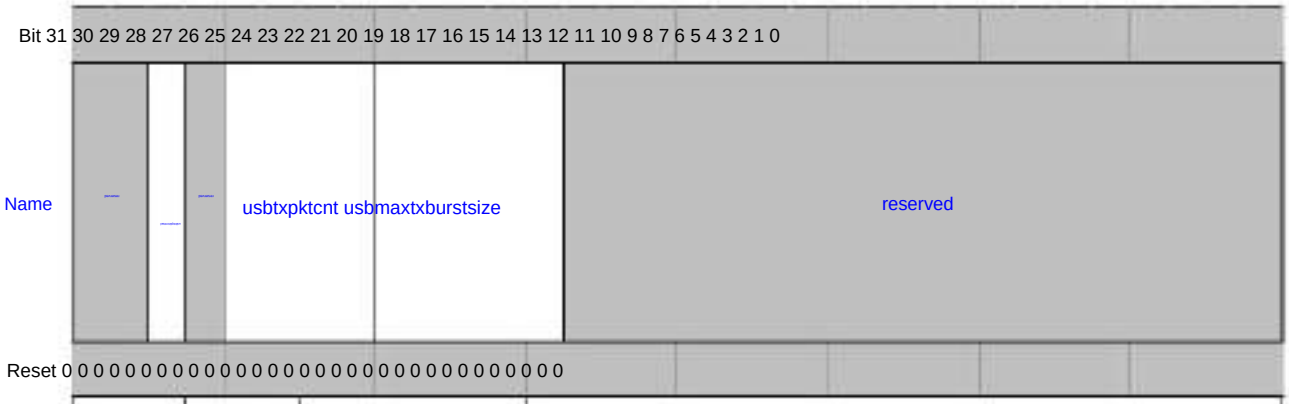


Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RW	usbtxpktcntsel	USB TXFIFO threshold selection, only valid in SuperSpeed. 0: USB starts to transmit only after all packets are read into the specified TXFIFO; 1: USB starts to transmit only after the set packet is read into the given TXFIFO.
[28]	RO	reserved	reserve.
[27:24]	RW	usbtxpktcnt	TXFIFO threshold setting, effective value is within 1-15.
[23:16]	RW	usbmaxtxburstsize	The maximum value of sending burst is valid only for SuperSpeed bulk, Isochronous and Interrupt transmission Out endpoints in host mode, valid values are between 1-16.
[15:0]	RO	reserved	reserve.

PERI_USB3_GRXTHRCFG

PERI_USB3_GRXTHRCFG is the global receive threshold control register.

Offset Address	Register Name	Total Reset Value
0xC10C	PERI_USB3_GRXTHRCFG	0x0000_0000

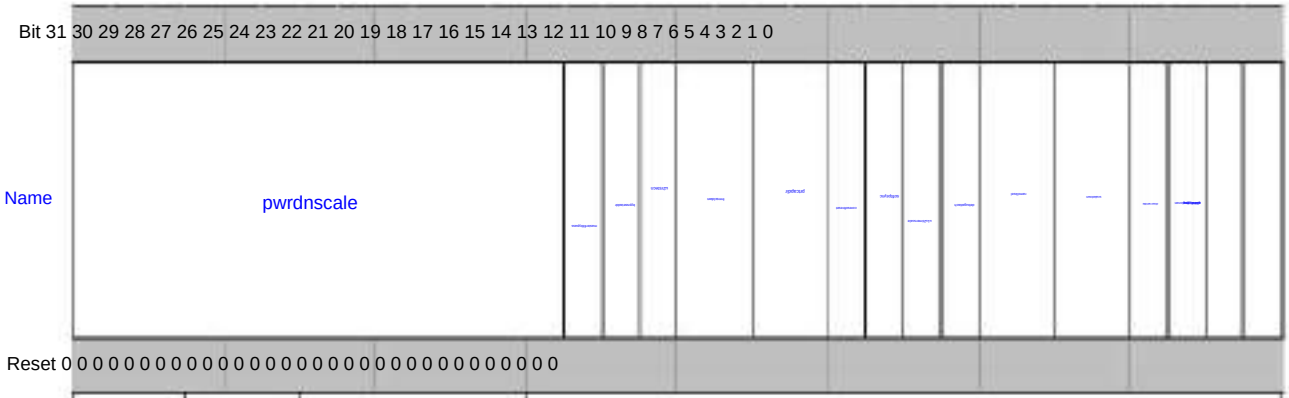


Bits	Access Name		Description
[31:30]	RO	reserved	reserve.
[29]	RW	usbtxpktcntsel	USB RXFIFO threshold selection, only valid in SuperSpeed. 0: USB starts to transmit only after all packets are read into the specified RXFIFO; 1: USB only starts to transmit after the set packet is read into the given RXFIFO.
[28]	RO	reserved	reserve.
[27:24]	RW	usbtxpktcnt	RXFIFO threshold setting, the effective value is within 1-15.
[23:19]	RO	usbmaxtxburstsize	The maximum value of received burst is only valid for the IN endpoint of SuperSpeed bulk, Isochronous and Interrupt transmission in host mode, and the effective value is between 1-16.
[18:0]	RO	reserved	reserve.

PERI_USB3_GCTL

PERI_USB3_GCTL is the global core control register.

Offset Address	Register Name	Total Reset Value
0xC110	PERI_USB3_GCTL	0x0000_0000



Bits	Access	Name	Description
[31:19]	RW	pwrdnscale	Suspend_clk setting, GCTL[31:19] * 16K = Suspend_clk Description: 32kHz<Suspend_clk<125MHz.
[18]	RW	masterfiltbypass	Filter function selection. 0: When the value of DWC_USB3_EN_BUS_FILTERS is 1, the filtering function is selected; 1: Regardless of the value of DWC_USB3_EN_BUS_FILTERS, disable the filter function.
[17]	RW	bypssetaddr	SetAddress command selection in Device mode. 0: Host sends SetAddress command to Device normally; 1: Host does not send SetAddress command to Device, and Device reads the value of DCFG[DevAddress] bit as the value of Address. Description: This bit is only set during emulation.
[16]	RW	u2rstecn	Timed out connection selection. 0: When the super speed connection fails, the device is in HS mode; 1: When the super-speed connection fails, Devcie will spend more than 3 cycles waiting for the connection. Note: This bit is only valid in Device mode.

[15:14] RW frmscldwn			SOF/USOF/ITP time interval selection. For SS/HS mode: 00: 125us; 01ÿ62.5usÿ 10ÿ31.25usÿ 11ÿ15.625usÿ Other: reserved. For FS mode, the above value*8 is enough. When the xHCI Debug mode is selected, the MaxPacketSize of bulk in and bulk out transmission during simulation can be configured, 00ÿ1024 bytesÿ 01ÿ512 bytesÿ 10ÿ256 bytesÿ 11: 128bytes; Others: Reserved.
[13:12] RW prtcapdir			Port configuration type. 00: reserved; 01: Host configuration; 10: Device configuration; 11: Otg configuration.
[11] RW coresoftreset			Core soft reset selection. 0: no soft reset; 1: Soft reset the core. Description: When performing a soft reset operation on the core, the interrupt and all interrupts other than the following registers will be cleared: -GCTL -GUCTL -GSTS -GSNPSID -GGPIO -GUID -GUSB2PHYCFGn -GUSB3PIPECTLn -DCFG -DCTL -DEVTEN -STD

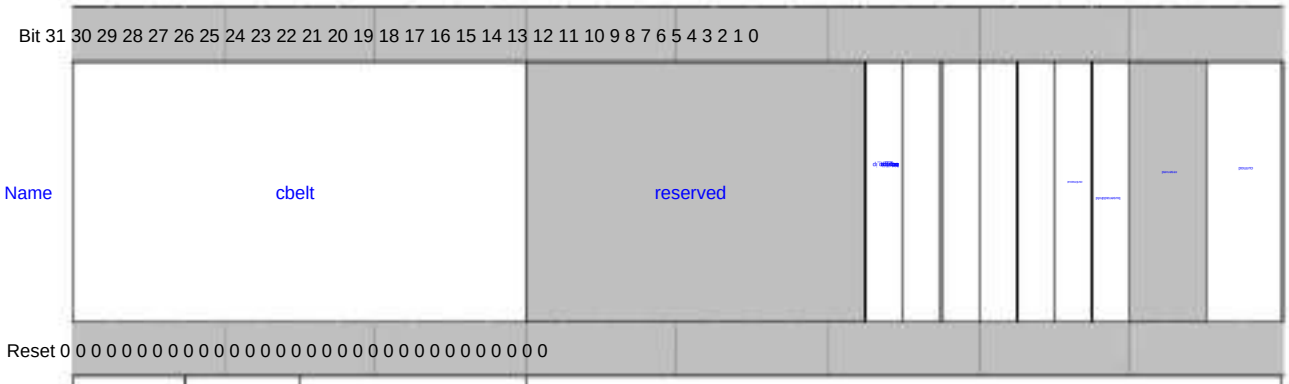
[10] RW sofitpsync			0: The first port of UTMI/ULPI PHY will be in non-suspended state, no matter whether there are other SS ports not in Rx.Detect, SS.Disable and U3 states; 1: The first port of the UTMI/ULPI PHY will be in the non-suspend state, regardless of whether there are other non-SS ports that are not in the non-suspend state. Note: This bit is only valid when the controller works in Host mode.
[9] RW u1u2timerscale			U1/U2 timer scaledown selection. 0: not closed; 1: If PERI_USB3_GCTL[5:4] (ScaleDown) = X1, turn off the U1/U2 response time scaledown.
[8] RW debugattach			Debug Attach signal when this bit is set to 1 -When the Ru/Stop bit in the DCTL register is set, the SS controller will directly enter the polling link state without the need to detect the connection of the remote device -the timeout time of Link LFPS polling is limited -the polling timeout time of TS1 is limited.
[7:6] RW ramclksel			RAM Clock selection. 00ÿbus clockÿ 01ÿpipe clockÿ 10ÿ pipe/2 clockÿ 11ÿreservedÿ Note: When in host mode, the hardware will set this 2 bits to 00, that is, connect ram_clk to bus_clk, because when SS port is in P3 state, pipe_clk will be closed, and USB2.0 port will not work.

[5:4] RW scaledown			scale-down timing selection. In HS/FS/LS mode: 00: Disable all scale-down timing, and use actual timing for simulation; 01: Enable all scale-down timing except the following functions: -speed enumeration -HNP/SRP - suspend and resume in host mode; 10: only enable the scale-down timing when the suspend and resume functions are enabled in device mode; 11: enable all scale-down timings. In SS mode 00 in HS/FS/LS mode: turn off all scale-down timing, and use actual timing for simulation; 01: enable scale-down timing of SS, including: - reduce TxEq training sequences to 8 - reduce LFPS polling burst time to 100ns - reduce LFPS warm reset receive to 30us 10: Do not send TxEq training sequences; 11: Turn on all scale-down timing.
[3] RW disscramble			Turn off scrambling. 1: off; 0: Do not close.
[2] RW u2exit_lfps			U2 state exit signal. 0: The link will regard the LFPS signal of 248ns as a valid U2 exit status signal; 1: The link layer waits for 8us before detecting a valid U2 exit signal.
[1] RW gbl hibernationen			Sleep enabled. 0: Turn off the global sleep function, the pmu receives the state switch of D0->D3 or D3->D0, and the internal state of the core will not be saved or restored; 1: Turn on the global sleep function.
[0] RW dsbclkgtng			Internal Clock Gating selection. 0: Select internal clock gating; 1: When the core is in lpm mode, turn off internal clock gating. Note: This bit can be set to 1 after power-on reset

PERI_USB3_GSTS

PERI_USB3_GSTS is the global status register.

Offset Address	Register Name	Total Reset Value
0xC118	PERI_USB3_GSTS	0x0000_0000



Bits	Access Name		Description
[31:20] RO		cbelt	Indicates the minimum value of all received device BELT values and the BELT value set by the Set Latency Tolerance Value command in Host mode.
[19:11] RO		reserved	reserve.
[10] RO		otg_ip	Indicates that an OTG-related interrupt is pending in the OEVT register. 0: no indication; 1: There are instructions.
[9]	RO	bc_ip	Indicates that a BC-related interrupt is pending in the BCEVT register. 0: no indication; 1: There are instructions.
[8]	RO	adp_ip	Indicates that an ADP-related interrupt is pending in the ADPEVT register. 0: no indication; 1: There are instructions.
[7]	RO	host_ip	Indicates that there is an xHCI-related interrupt pending in the Host event queue. 0: no indication; 1: There are instructions.
[6]	RO	device_ip	Indicates that there is an xHCI-related interrupt pending in the Device event queue. 0: no indication; 1: There are instructions.

[5]	RO	csrtimeout	Indicates that software access to registers took longer than defined by DWC_USB3_CSR_ACCESS_TIMEOUT. 0: no indication; 1: There are instructions.
[4]	RO	buserraddrvld	Indicates whether the GBUSERRADDR register is valid and indicates the first address where the error occurred. 0: no indication; 1: There are instructions.
[3:2] RO		reserved	reserve.
[1:0] RO		curmod	Current working mode: 00: Device mode; 01: Host mode; Others: Reserved.

PERI_USB3_GUCTL1

PERI_USB3_GUCTL1 is Global User Control Register 1.

Offset Address	Register Name	Total Reset Value
0xC11C	PERI_USB3_GUCTL1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:2] RO		reserved	reserve.
RW ovrld_l1_	susp_com	and stops providing clock.	If this bit is written as 1, the utmi_l1_suspend_com_n signal will be replaced by utmi_sleep_n. This bit is usually set when PHY enters L1 sleep mode [1]
[0] RW loa_filter_en			Check the shutdown status of the port. When this bit is set to 1, the controller will send three consecutive cycles to check the status of the port before the port is closed.

PERI_USB3_GGPIO

PERI_USB3_GGPIO is the global GPIO register.

Offset Address	Register Name	Total Reset Value
0xC124	PERI_USB3_GGPIO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	gpo	gpi
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	gpo	Drives the value of gp_o[15:0].
[15:0]	RO	gpi	Read the value of gp_i[15:0].

PERI_USB3_GUID

PERI_USB3_GUID is the global user ID register.

Offset Address	Register Name	Total Reset Value
0xC128	PERI_USB3_GUID	0x0000_0000

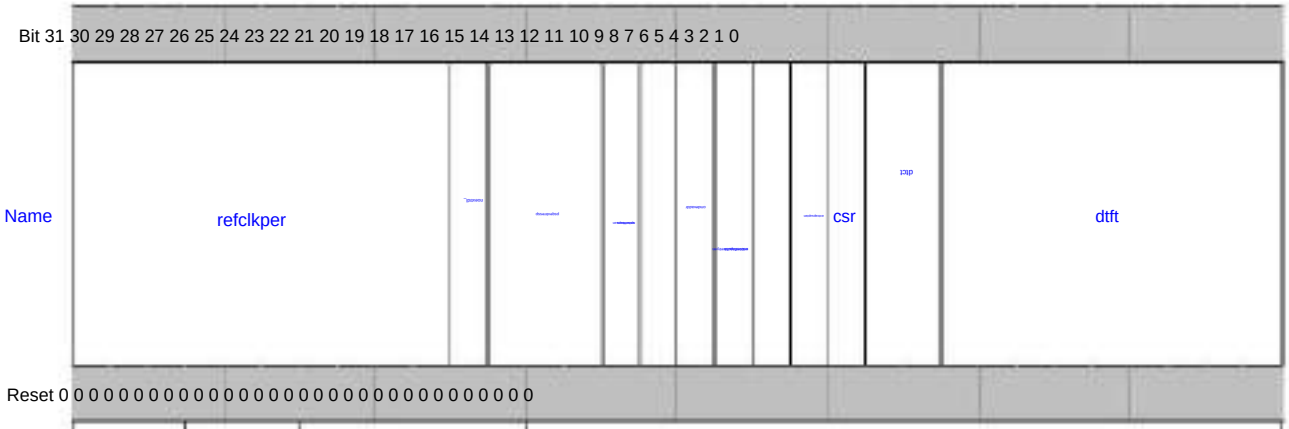
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	reserved	User information, including: system version; Hardware Configuration.

PERI_USB3_GUCTL

PERI_USB3_GUCTL is the global user control register.

Offset Address	Register Name	Total Reset Value
0xC12C	PERI_USB3_GUCTL	0x0000_0000



Bits	Access	Name	Description
[31:22]	RW	refclkper	The reference clock ref_clk is represented by ns. For example: ref_clk=125MHz, then here is 1/125MHz=8ns.
[21]	RW	noextrdl_	Extra delay option between SOF packet and first packet. 0: Host waits for 2ms after the SOF packet before sending the first packet; 1: Host sends the first packet directly after SOF without delay.
[20:18]	RW	psqextrressp	reserved
[17]	RW	sprsctrltransen	Decentralized control transfer enable. 0: forbidden; 1: enable. Some devices respond slowly to control transfers, and multiple transfers within 1 frame/microframe will cause the device to behave in disorder. When this bit is set, the host controller will spread a control transfer over different frames or microframes.
[16]	RW	resbwhseps	85% of the bandwidth is reserved for high-speed periodic endpoints, and it is only valid in HOST mode or Host operation mode in DRD mode.
[15]	RW	cmdevaddr	The mode of the Device address. 1: Increment according to each device allocation address command; 0: The device address is equal to the Slot ID.
= 1 and NumP = 0); [14]	RW	usbhstlnautoretryen	Host input transfer automatic retransmission enable. 0: The automatic retransmission function is disabled; If the input transmission error of the host occurs, the host will automatically reply to the device with a final ACK (Retry = 1 and NumP = 0). 1: The automatic retransmission function is enabled. When the automatic retransmission function is enabled, if an error occurs in the host's input transmission, the host will automatically reply to the device with an ACK that is not final (Retry = 1 and NumP != 0).

[13] RW	enoverlapchk		LFPS superimposed signal detection enable. 0: Do not detect LFPS superimposed signal; 1: Detect LFPS superimposed signal to avoid glitch effect.
[12] RW	extcapsupten	Reserved	
[11] RW	csr		Inserts additional delay between full-speed BULKOUT transfers. 0: do not insert; 1: insert.
[10:9] RW	dtct		Device responds to the rough Timeout time of Host. If this bit is 0, the timeout time is defined by DTFT. If this bit is not 0, then: 00ÿ0usÿ 01ÿ500usÿ 10ÿ1.5msÿ 11ÿ6.5msÿ
[8:0] RW	dtft		Device responds to the precise time of the Timeout of Host, and it is valid when DTCT is 0. T=DTFT*256*8 usÿ

PERI_USB3_GBUSERRADDR_HI

PERI_USB3_GBUSERRADDR_HI is the global bus error address high 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC130	PERI_USB3_GBUSERRADDR_HI	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	busaddrhi
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	busaddrhi	The upper 32-bit address where the error occurred. Note: only valid when GSTS.BusErrAddrVld is 1 Only cleared to 0 at reset, only supports AHB and AXI bus configuration.

PERI_USB3_GBUSERRADDR_LO

PERI_USB3_GBUSERRADDR_LO is the global bus error address low 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC134	PERI_USB3_GBUSERRADDR_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	busaddrlo																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	busaddrlo	The lower 32-bit address where the error occurred. Note: only valid when GSTS.BusErrAddrVld is 1 Only cleared to 0 at reset, only supports AHB and AXI bus configuration.

PERI_USB3_GPRTBIMAP_HI

PERI_USB3_GPRTBIMAP_HI is the SuperSpeed Port-Bus Map Higher 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC138	PERI_USB3_GPRTBIMAP_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	reserve

PERI_USB3_GPRTBIMAP_LO

PERI_USB3_GPRTBIMAP_LO is the SuperSpeed port-bus map lower 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC13C	PERI_USB3_GPRTBIMAP_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														binumn	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	binumn	Indicates the bus number of the currently connected superspeed.

PERI_USB3_GPRTBIMAP_HS_HI

PERI_USB3_GPRTBIMAP_HS_HI is the high-speed port-bus map high 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC180	PERI_USB3_GPRTBIMAP_HS_HI	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	reserved	reserve.

PERI_USB3_GPRTBIMAP_HS_LO

PERI_USB3_GPRTBIMAP_HS_LO is the lower 32-bit register of the high-speed port-bus map.

Offset Address	Register Name	Total Reset Value
0xC184	PERI_USB3_GPRTBIMAP_HS_LO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	binumn
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	binumn	Indicates the bus number of the currently connected highspeed.

PERI_USB3_GPRTBIMAP_FS_HI

PERI_USB3_GPRTBIMAP_FS_HI is the full-speed port-bus mapping high 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC188	PERI_USB3_GPRTBIMAP_FS_HI	0x0000_0000

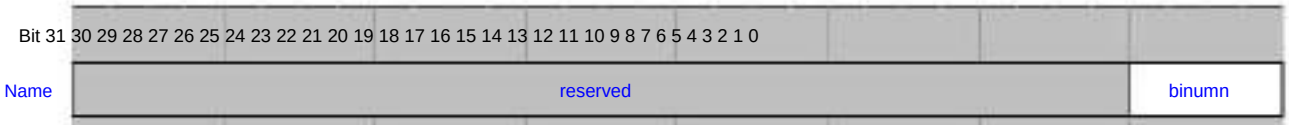
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	reserved	reserve.

PERI_USB3_GPRTBIMAP_FS

PERI_USB3_GPRTBIMAP_FS is the full-speed port-to-bus map lower 32-bit register.

Offset Address	Register Name	Total Reset Value
0xC18C	PERI_USB3_GPRTBIMAP_FS	0x0000_0000

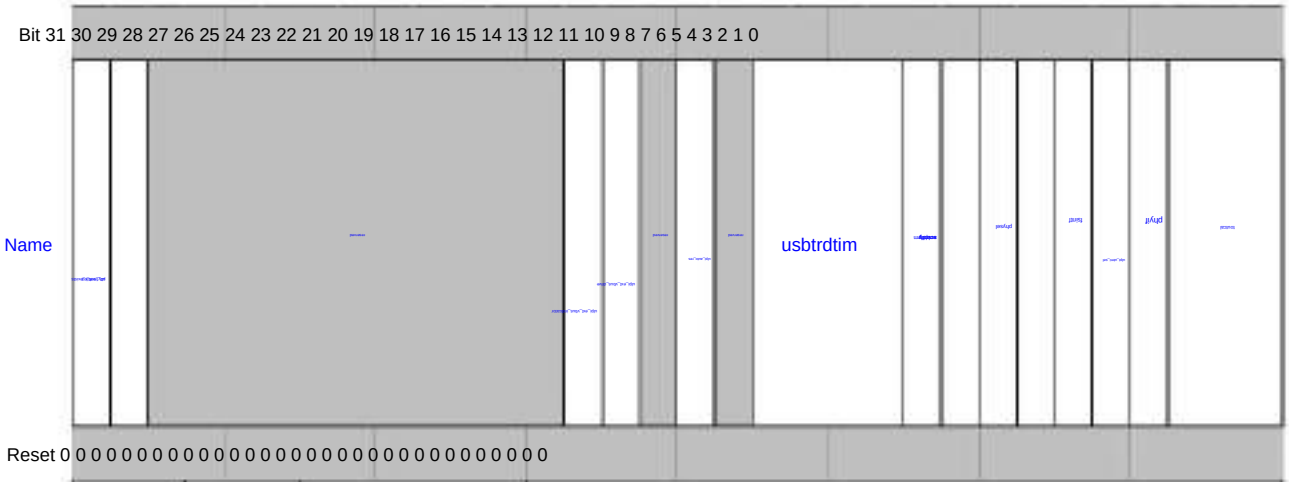


Bits	Access	Name	Description
[31:4]	RO	reserved	reserve.
[3:0]	RW	binumn	Indicates the fullspeed bus number of the current connection.

PERI_USB3_GUSB2PHYCFGN

PERI_USB3_GUSB2PHYCFGN is the global USB2.0 PHY configuration register.

Offset Address	Register Name	Total Reset Value
0xC200	PERI_USB3_GUSB2PHYCFGN	0x0000_0000



Bits	Access	Name	Description
[31]	RW	phy_soft_rst	Toggle the usb2phy_reset signal to soft reset the UTMI PHY. The ULPI PHY is not reset here, because the ULPIPHY is reset through the FunctionControl.Reset register. When the core is reset, the core automatically configures the following registers for reset: vcc_reset_n, small xHCI_USBCMD[hcrst], PERI_USB3_DCTL[SoftReset] or PERI_USB3_GCTL[SoftReset]ÿ

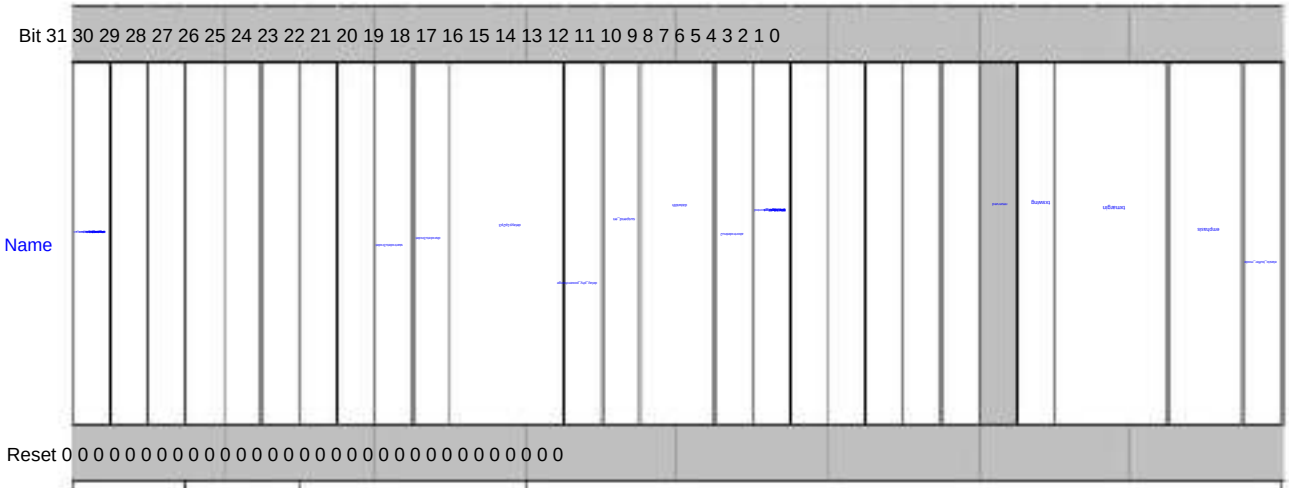
[30] RW	u2_freeclk_exists		Whether the USB2 PHY provides free_clk. 0: No free clock is provided; 1: Provide free clock.
[29:19] RO		reserved	reserve.
[18] RW		indication. ulpi_ext_vbus_ voltage; cator	ULPI interface external Vbus indi 0: PHY uses internal Vbus as comparison 1: PHY uses external Vbus as comparison voltage.
[17] RW	ulpi_ext_vbus_drv	1: PHY is driven by	ULPI external Vbus driver. 0: PHY is driven by internal VBUS voltage; external VBUS voltage.
[16] RO		reserved	reserve.
[15] RW	ulpi_auto_res		ULPI automatically wakes up. 0: PHY does not enable the automatic wake-up function; 1: PHY enables the automatic wake-up function.
[14] RO		reserved	reserve.
[13:10] RW	usbtrdtim		USB2 turnaround time (Turnround Time), refers to the response time for MAC to request Packet FIFO Controller (PFC) to retrieve data from DFIFO (SPRAM). When 16-bit UTMI+: 0x5 When 8-bit UTMI+/ULPI interface: 0x9.
[9] RW	xcvrdly		Transceiver delay selection, when this bit is set to 1, a delay of 2.5us is added between Transceiver Select being set to 00 (high speed) and TxValid being pulled to 0 for sending chirp-K handshake signals.
[8] RW	enblslpm		The utmi_sleep_n and utmi_l1_suspend_n signals are enabled. 0: utmi_sleep_n and utmi_l1_suspend_n signals are not connected to PHY; 1: utmi_sleep_n and utmi_l1_suspend_n signals are connected to PHY.
[7] RW	physel		Interface type selection for the PHY. 0: USB2.0 high-speed UTMI+ or ULPI PHY; 1: USB1.1 full-speed serial interface; when it is write-only, this bit is 1.
[6] RW	susphy		USB2.0 HS/FS/LS PHY suspend selection. 0: do not suspend; 1: suspend. Note: In DRD mode, set this bit to 1 after core initialization is completed.

[5] RW fsintf			Full-speed PHY serial interface type selection. 0: 6-pin unidirectional full-speed serial transmission interface; 1: 3-pin bidirectional full-speed serial transmission interface. When set as read-only, the return value is 0.
[4] RW ulpi_utmi_sel			High-speed PHY interface type selection. 0ÿUTMI+ ÿ 1:ULPIÿ
[3] RW phyif			UTMI interface data width selection. 0ÿ8bitsÿ 1ÿ16bitsÿ
[2:0] RW toutcal			HS/FS Timeout Calibration. Each PHY clock plus the corresponding bit time High-speed mode: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed mode: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

PERI_USB3_GUSB3PIPECTLN

PERI_USB3_GUSB3PIPECTLN is the global USB3.0 PIPE control register

Offset Address	Register Name	Total Reset Value
0xC2C0	PERI_USB3_GUSB3PIPECTLN	0x0000_0000



Bits	Access	Name	Description
[31]	RW	phy_soft_rst	USB3.0 soft reset. 0: no reset; 1: Reset.
[30]	RW	hstprtcmpl	reserve.
[29]	RW	u2ssinactp3ok	State selection of PHY in U2/SSInactive state. 0: PHY enters P2 state; 1: PHY enters P3 state.
[28]	RW	disrxdetp3	p3 status receive detection enable. 0: If the PHY is in the P3 state and the core needs to receive detection, the core will perform the reception detection in the P3 state; 1: If the PHY is in the P3 state and the core needs to receive detection, the Core will change the PHY state to P2, and then perform the reception detection. After the detection is completed, the core will change the PHY state back to P2.
[27]	RW	ux_exit_in_px	When the core state is switched, the state selection of the PHY. 0: The core is in the P0 state of the PHY when it exits the U1/U2/U3 state; 1: The core is in the corresponding P1/P2/P3 state of the PHY when it exits the U1/u2/ u3 state. Description: When using synopsys PHY, this bit is 0
[26]	RW	change; ping_enhancement_en	The timeout of the ping command on the downlink port U1 is changed from 500ms to 300ms. 0: no 1: change. Description: When using synopsys PHY, this bit is 0.

[25] RW		u1u2exitfail_to_recov	Exit the signal selection of P3 in P2 state. When this bit is set to 1, the core will set the state of the PHY to P2 before issuing the handshake signal to exit U3.
[24] RW	request_p1p2p3		When the core switches from state U0 to U1/U2/U3, the core will always request the PHY to switch from state P0 to P1/P2/P3 0: do not switch; 1: Toggle. Description: This bit is set to 1 when using synopsys' PHY.
[23] RW	startrxdetu3rxdet	should be fixed to 0.	
[22] RW	disrxdetu3rxdet	should be fixed to 0.	
[21:19] RW	delayp1p2p3		Delay from P0 to P1/P2/P3 state When core enters U1/U2/U3 state, extend the time for P0 to enter P1/P2/P3 until Pipe3_RxValid is pulled to 0, or 8B10B error occurs. Note: The 18th bit must be set to 1 to be valid.
[18] RW		pipe3_RxValid; delay_phy_powerc	PHY state switch delay register. 0: When the core enters the U1/U2/U3 state from U0, the PHY directly enters the P1/P2/P3 state without checking the values of Pipe3_RxElecIlde and change 1: When the core enters the U1/U2/U3 state from U0 , the state of PHY to P1/P2/P3 will be delayed until Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0. Note: If using Synopsys PHY, this bit is 1.
[17] RW	suspend_en		USB3.0 PHY suspend enable. 0: do not suspend; 1: suspend. Note: In DRD mode, set this bit to 1 after core initialization is completed.
[16:15] RW	datwidth		The data bit width of the PIPE interface. 00ÿ32 bitsÿ 01ÿ16 bitsÿ 10ÿ8 bitsÿ Other: reserved.

[14] RW abortrxdetinu2			Cancel Rx Detect in U2 state. 0: do not cancel; 1: cancel. When this bit is set to 1 and the connection state is U2, when the core receives the U2 exit signal sent by the remote connection device, it will not take the reception detection. Description: When using synopsys PHY, this bit is 0.
[13] RW skiprxdet			Skip the Rx Detect state. 0: do not skip; 1: Skip. If this bit is set to 1, when pipe3_RxElecIdle is pulled low, Rx will be skipped Detectionÿ
[12] RW lfps_p0_align			When the controller exits the U1/U2/U3 state, it terminates sending LFPS at the clock edge of the request PHY P0 signal, otherwise the LFPS signal will be sent one cycle earlier. When the PHY switches from the P1 or P2 state to the P0 state, the PHY setting 2 clock cycles after PhyStatus, the controller requests a transfer.
[11] RW p3p2_tran_ok			The P3/P2 state is switched directly. 0: PHY needs to go through the intermediate state every time it switches to P2P3 quality inspection P0ÿ 1: PHY twins switch directly from P2 to P3, or directly from P3 to P2, without going through the intermediate state P0. Description: When using synopsys PHY, this bit is 0.
[10] RW p3exsigp2			P3 Exit state selection. When this bit is 1, when the core exits from U3, the state of PHY must exit from P3 to P2, otherwise it can exit from P3 to p1 or P0. Description: When using synopsys PHY, this bit is 0.
[9] RW lfps_filter			LFPS filtering. 0: no filtering; 1: filter. When this bit is set, the controller will filter the LFPS signal from the PHY unless pipe3_Rxelecidle and pipe3_RxValid are deasserted.
[8] RW		polling_lfps_control 0:	RX_DETECT to Polling.LFPS control. (Default value) Start Polling LFPS with a delay of 400us after RX_DETECT; l 1: Start Polling LFPS without delay after RX_DETECT.
[7]	RO	reserved	reserve.
[6] RW txswing			The PIPE interface sends the swing.
[5:3] RW txmargin			Headroom at the sending end of the PIPE interface.
[2:1] RW txdeemphasis			Pre-emphasis at the sending end of the PIPE interface.

[0] RW		enable. elastic_buffer_mod It is	Elastic buffer mode selection 0: disable; 1: enable.

PERI_USB3_GTXFIFOSIZN

PERI_USB3_GTXFIFOSIZN is the global transmit FIFO size register.

Offset Address	Register Name	Total Reset Value
0xC304	PERI_USB3_GTXFIFOSIZN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	txfstaddr_n	txfdep_n
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	txfstaddr_n	Transmit FIFOn RAM start address in memory.
[15:0]	RW	txfdep_n	Transmit FIFO depth. Minimum: 32 MDWIDTH-bit words; Maximum: 32768 MDWIDTH-bit words.

PERI_USB3_GRXFIFOSIZN

PERI_USB3_GRXFIFOSIZN is the global receive FIFO size register.

Offset Address	Register Name	Total Reset Value
0xC384	PERI_USB3_GRXFIFOSIZN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rxfstaddr_n	rxfdep_n
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	rxfstaddr_n	Receive FIFOn RAM start address in memory.
[15:0]	RW	rxfdep_n	Receive FIFO depth. Minimum: 32 MDWIDTH-bit words; Maximum: 32768 MDWIDTH-bit words.

PERI_USB3_GEVNTADRN_EN

PERI_USB3_GEVNTADRN_HI is the high 32-bit register of the global event buffer address.

Offset Address	Register Name	Total Reset Value
0xC410	PERI_USB3_GEVNTADRN_EN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	evntadrhi
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RWSC	evntadrhi	Event Buffer high 32-bit address.

PERI_USB3_GEVNTADRN_LO

PERI_USB3_GEVNTADRN_LO is the lower 32-bit register of the global event buffer address.

Offset Address	Register Name	Total Reset Value
0xC414	PERI_USB3_GEVNTADRN_LO	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	evntadrlo
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RWSC	evntadrlo	The lower 32-bit address of Event Buffer.

PERI_USB3_GEVNTSIZN

PERI_USB3_GEVNTSIZN is the size register of global event buffer.

Offset Address	Register Name	Total Reset Value
0xC418	PERI_USB3_GEVNTSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	reserved																							without event							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31]	RW	evntintmask	Event interrupt Mask.
[30:16]	RO	reserved	reserve.
[15:0]	RW	is not available	Event Buffer size (byte).

PERI_USB3_GEVNTCOUNTN

PERI_USB3_GEVNTCOUNTN is the count register of the global event buffer.

Offset Address	Register Name	Total Reset Value
0xC41C	PERI_USB3_GEVNTCOUNTN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										evntcount					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RWSC	evntcount	When reading this register, return the effective number of events in the Event Buffer; when writing this register, the hardware will decrement the written count.

PERI_USB3_GTXFIFOPRIDEV

PERI_USB3_GTXFIFOPRIDEV is the peripheral's global TX FIFO DMA priority register.

Offset Address	Register Name	Total Reset Value
0xC610	PERI_USB3_GTXFIFOPRIDEV	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	device_txfifo_priority
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	device_txfifo_priority	Device TXFIFO priority. 0:low;ity 1ÿhighÿ

PERI_USB3_GTXFIFOPRIHST

PERI_USB3_GTXFIFOPRIHST is the global TX FIFO DMA priority register of Host.

Offset Address	Register Name	Total Reset Value
0xC618	PERI_USB3_GTXFIFOPRIHST	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	host_txfifo_priority
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	host_txfifo_priority	Host TXFIFO priority. 0ÿlowÿ 1ÿhighÿ

PERI_USB3_GRXFIFOPRIHST

PERI_USB3_GRXFIFOPRIHST is the global RX FIFO DMA priority register of Host.

Offset Address	Register Name	Total Reset Value
0xC61C	PERI_USB3_GRXFIFOPRIHST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															host_rxfifo_priority
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	host_rxfifo_priority	Host RXFIFO priority. 0ÿlowÿ 1ÿhighÿ

PERI_USB3_GFIFOPRIDBC

PERI_USB3_GFIFOPRIDBC is the DMA priority register for the global Debug performance of the host.

Offset Address	Register Name	Total Reset Value
0xC620	PERI_USB3_GFIFOPRIDBC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	reserve.

[1:0] RW		host_dbc_dma_priority	Host DbC DMA priority. 00ÿLowÿ 01ÿNormalÿ 10: High; Others: Reserved.

PERI_USB3_GDMAHLRATIO

PERI_USB3_GDMAHLRATIO is the host's global FIFO DMA high and low priority ratio register.

Offset Address	Register Name	Total Reset Value
0xC624	PERI_USB3_GDMAHLRATIO	0x0000_0000

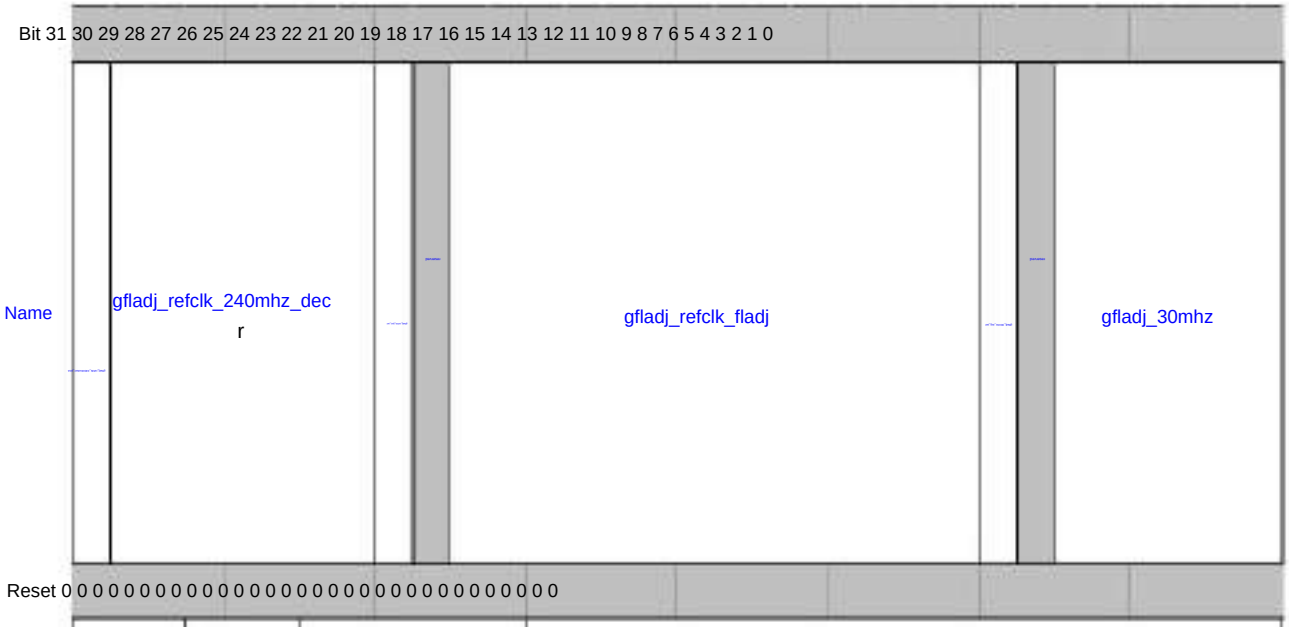
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5	4 3 2 1 0
Name	reserved	hst_rxfifo_dma_hilo_priority_ratio	—	hst_txfifo_dma_hilo_priority_ratio
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0	0 0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	reserve.
[12:8]	RW	hst_rxfifo_dma_hilo	Host RXFIFO DMA high-low priority ratio. o_priority_ratio
[7:5]	RO	reserved	reserve.
[4:0]	RW	hst_txfifo_dma_hilo	Host TXFIFO DMA high-low priority ratio. o_priority_ratio

PERI_USB3_GFLADJ

PERI_USB3_GFLADJ is GFLADJ is the global frame length adjustment register.

Offset Address	Register Name	Total Reset Value
0xC630	PERI_USB3_GFLADJ	0x0000_0000

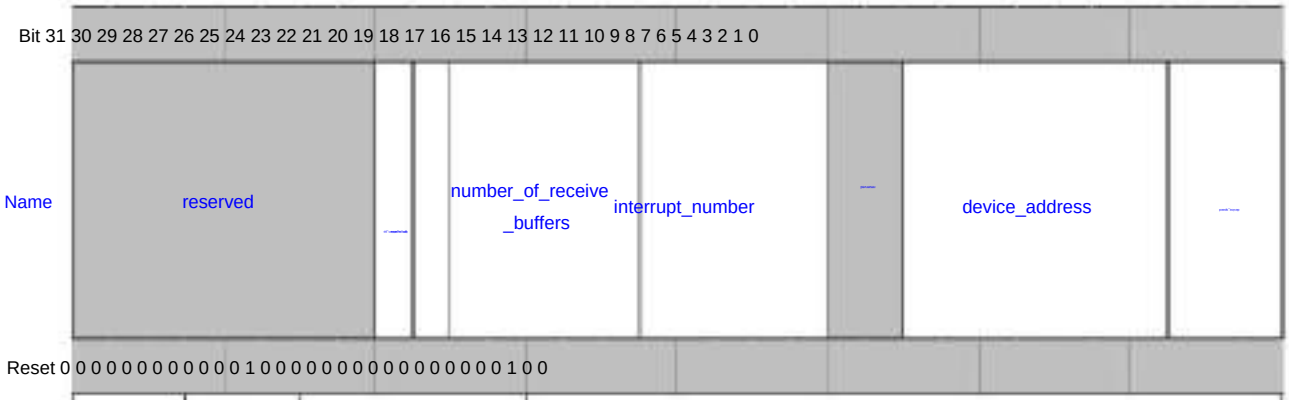


Bits	Access	Name	Description
[31]	RW	gfladj_refclk_240mhzdecr_pls1	Precision adjustment for GFLADJ_REFCLK_240MHZ_DECR/ref_frequency. 0: remainder less than 0.5; 1: The remainder is greater than or equal to 0.5.
[30:24]	RW	gfladj_refclk_240mhz_decr	Counter value calculated as 240/ref_clk_frequency: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency.
[23]	RW	gfladj_refclk_lpm_sel	SOF/ITP count clock selection. If this bit is set, SOF/ITP has ref_clk as clock count.
[22]	RO	reserved	reserve
[21:8]	RW	gfladj_refclk_fladj	When bit[23] is 1, SOF/ITP calibration value FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer)- (125000/ref_clk_period)) * ref_clk_periodÿ
[7]	RW	gfladj_30mhz_reg_sel	SOF/ITP calibration selection signal. 0: The controller uses the value of fladj_30mhz_reg to calibrate SOF/ITP; 1: The controller uses the value of GFLADJ.GFLADJ_30MHZ to calibrate SOF/ITP.
[6]	RO	reserved	reserve.
[5:0]	RW	gfladj_30mhz	When bit[7] is 1 and SOF/ITP counts with UTMI/ULPI as the clock, the controller uses the value of this field to calibrate SOF/ITP.

PERI_USB3_DCFG

PERI_USB3_DCFG is the peripheral configuration register.

Offset Address	Register Name	Total Reset Value
0xC700	PERI_USB3_DCFG	0x0008_0004

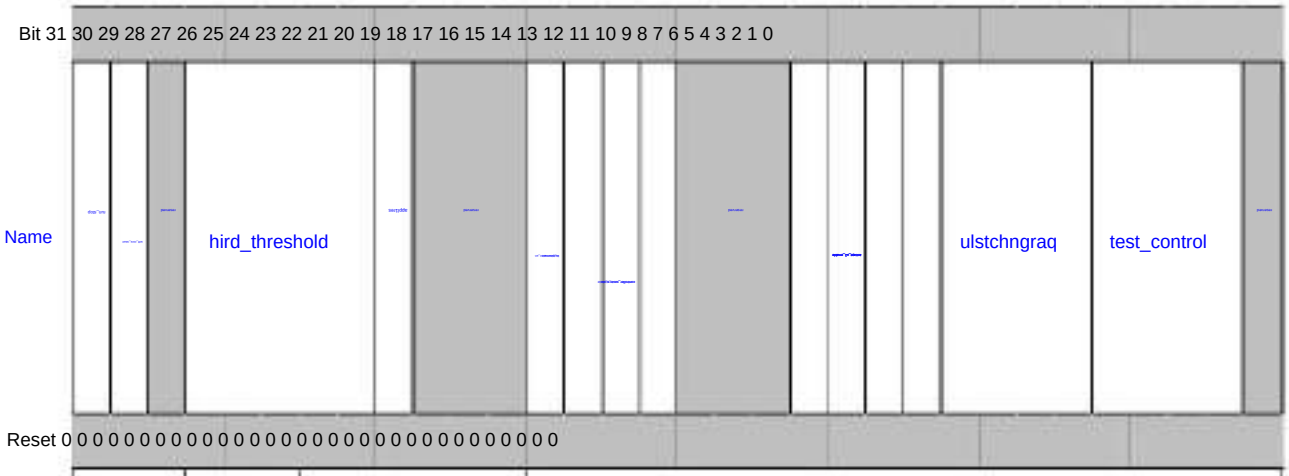


Bits	Access Name		Description
[31:24] RO		reserved	reserve.
[23] RW	ignore_stream_pp		The Packet Pending bit is ignored. 0: do not ignore; 1: Ignore.
[22] RW	lpm_capable		LPM function selection. 0: LPM function is enabled; 1: LPM function is off.
[21:17] RW		number.	Receive Buffer number_of_receive_buffers indicates the received buffer number returned in ACK TP.
[16:12] RW	interrupt_number		Interrupt number indication. Indicates the interrupt number of a non-endpoint interrupt generated by the device.
[11:10] RO		reserved	reserve.
[9:3] RW	device_address		device address. Whenever Device receives the SetAddress command, configure the address of the device here. After USB reset, this bit is cleared to 0.
[2:0] RW	device_speed		Device transfer rate selection. 000: high speed; 001: full speed; 100: Overspeed; Other: reserved.

PERI_USB3_DCTL

PERI_USB3_DCTL is the peripheral control register.

Offset Address	Register Name	Total Reset Value
0xC704	PERI_USB3_DCTL	0x0000_0000



Bits	Access Name	Description
[31] RW run_stop		Device on/off selection. The software writes 1 to start the operation of the device; if you want to stop the operation of the device, first stop all ongoing transmissions, and then write 0 to this bit. The Run/stop bit must be operated under the following conditions: 1. After power-on reset, the software must write 1 to this bit to initialize the device controller, otherwise the device controller will not notify that the host has been connected; 2. If the software To restart the connection after soft disconnection or detection of a disconnection event, you need to set DCTL[8:5] to 5 before writing 1 to this bit; 3. When the USB is in a low power state and the USB is a dual power domain Configuration, software writing 0 to this bit means that the core power domain will be turned off. Set this bit to 1 after the software restarts the core power domain and device controller.

[30] RWSC	soft_core_reset		core soft reset. The interrupts and registers of all clock domains will be operated as follows: 1: Clear all interrupts and reset all registers except the following registers; - GCTL - GUCTL - GSTS - GSNPSID - GGPIO - GUID - GUSB2PHYCFGn registers - GUSB3PIPECTLn registers - DCFG - DCTL - DEVTEN - STD 2: All state machines will return to IDLE state, and all FIFOs will be cleared to 0; 3: All transfers on the SoC bus will be terminated immediately.
[29] RO		reserved	reserve.
[28:24] RW	hird_threshold		HIRD Threshold The core will generate utmi_l1_suspend_n and utmi_sleep_n signals under the following conditions. 1. When the following conditions are met, the core generates utmi_l1_suspend_n in the L1 state, and switches the PHY to the deep Low-Power: -HIRD value is greater than or equal to DCTL.HIRD_Thres[3:0] -The value of HIRD_Thres[4] is 1 2. When the following conditions are met, the core will generate utmi_sleep_n in the L1 state: -The value of HIRD is less than HIRD_Thres[3:0] - the value of HIRD_Thres[4] is 0

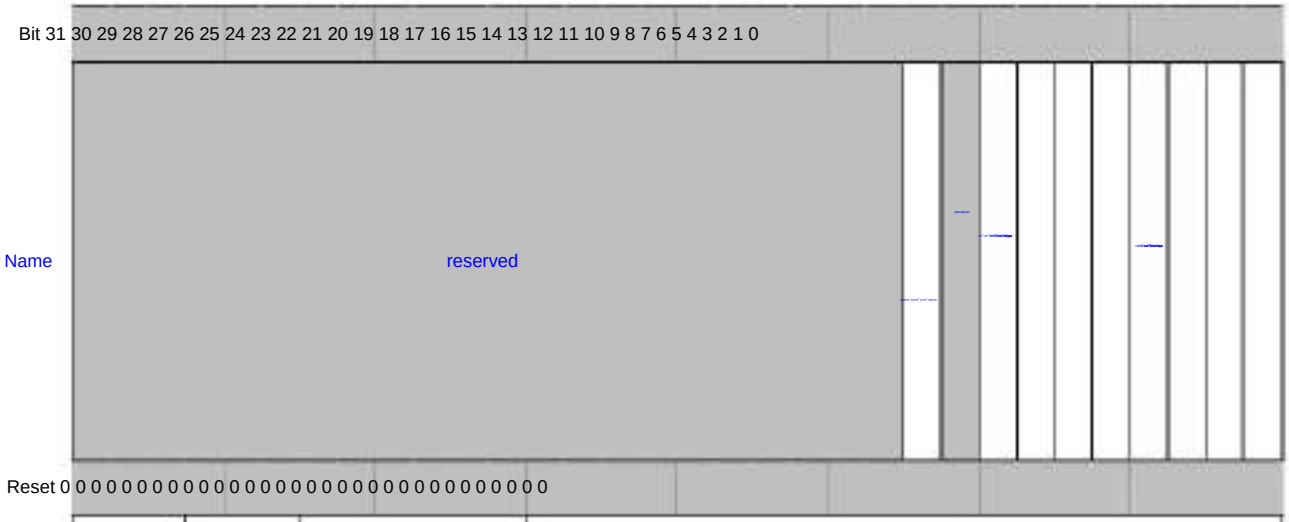
[23] RW	appl1res		LPM response configuration. When PERI_USB3_DCFG[lpm_capable] is 0: core has no response; When PERI_USB3_DCFG[lpm_capable] is 1: 0: When the following conditions are met, LPM will return ACK after successful transmission - no verification error - received valid bLinkState = 0001B (L1) - There is no data remaining in the sending FIFO and the OUT endpoint is not in the flow controlled state (except NYET) 1: When the following conditions are met, the LPM will return ACK after successful sending and receiving - No verification error - Received a valid bLinkState = 0001B (L1).
[22:20]	RO	reserved	reserve.
[19]	RW keepconnect		Stay connected. If this bit is set to 1, all involved models will be saved or restored when runStop =0. At the same time, when the link enters U3 or L2, it will enable Hibernation Request Eventÿ
[18]	RW l1_hibernation_en		When keepconnect is 1 and this bit is 1, if L1 is enabled and the value of HIRD is greater than the threshold configured in PERI_USB3_DCTL[hird_threshold], the device core will generate a Hibernation Request Event.
[17]	RW	DSTS.RSS to 1, and sets the controller . tate Description: When reading this bit, return 0.	The controller restores state. When the software writes 1 to this bit, the controller immediately sets PERI_USB3_DSTS[rss] to 0 when the controller_restore_s restores
[16]	RW	to 1, and sets PERI_USB3_DSTS[sss] to 0 after the controller_save_sta is saved . te Description: When reading this bit, return 0.	The controller saves state. When the software writes 1 to this bit, the controller immediately sets DSTS.SSS
[15:13]	RO	reserved	reserve.
[12]	RW initiate_u2_enable		Initialize the U2 enable register. 0: Do not initialize U2; 1: Initialize U2.
[11]	RW accept_u2_enable		U2 state enable. 0: The core refuses to enter the U1 state unless; Force_LinkPM_Accep is 1 1: If there is no device waiting at the user end, the core can accept and allow to enter the U2 state. Note: After USB reset, the hardware will clear this bit automatically.

[10] RW	initiate_u1_enable		Initialize the U1 enable register. 0: Do not initialize U1; 1: Initialize U1.
[9] RW	accept_u1_enable		U1 state is enabled. 0: The core refuses to enter the U1 state unless; Force_LinkPM_Accep is 1; 1: If there is no device waiting at the user end, the core can accept and allow to enter the U1 state Note: After USB reset, the hardware will clear this bit automatically.
[8:5] WO	ulstchngraq		USB/Link state switching request. The software initiates a corresponding state switching request for the configuration here SS mode: 0x0ÿNo Actionÿ 0x4ÿSS.Disabledÿ 0x5ÿRx.Detectÿ 0x6ÿSS.Inactiveÿ 0x8ÿRecoveryÿ 0xA: Compliance; Others: Reserved. HS/FS/LS mode: 0x8: Remote wakeup request; Others: Reserved.
[4:1] RW	test_control		Test controls. 0x0: Test mode is off; 0x1ÿTest_J modeÿ 0x2ÿTest_K modeÿ 0x3ÿTest_SE0_NAK modeÿ 0x4ÿTest_Packet modeÿ 0x5: Test_Force_Enable; Others: Reserved.
[0]	RO	reserved	reserve.

PERI_USB3_DEVTEN

PERI_USB3_DEVTEN is the peripheral event enable register.

Offset Address	Register Name	Total Reset Value
0xC708	PERI_USB3_DEVTEN	0x0000_0000



Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9]	RW	erratic_error_event_enable	Irregular error event enable. 0: disable; 1: enable.
[8]	RO	reserved	reserve.
[7]	RW	sof_en	SOF packet enable. 0: forbidden; 1: enable.
[6]	RW	u3l2l1_susp_en	U3/L2-L1 suspend event enable. 0: forbidden; 1: enable.
[5]	RW	hibernation_req_ev t_en	Sleep request enabled. 0: disable; 1: enable.
[4]	RW	wkup_evt_en	Resume/remote wakeup detection event enable. 0: forbidden; 1: enable.
[3]	RW	ulst_cng_en	USB/LINK state transition event enable. 0: disable; 1: enable.

[2] RW	connect_done_en		Connection complete enable. 0: forbidden; 1: enable.
[1] RW	usbrst_en		USB reset enable. 0: forbidden; 1: enable.
[0] RW	disconn_evt_en		Disconnect detection enable. 0: forbidden; 1: enable.

PERI_USB3_DSTS

PERI_USB3_DSTS is the peripheral status register.

Offset Address	Register Name	Total Reset Value
0xC70C	PERI_USB3_DSTS	0x0012_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	reserve.
[29]	RO	dcnrd	Device controller is not ready. Indicates that a state transition is in progress after the controller exited from hibernation.
[28:26]	RO	reserved	reserve.
[25]	RO	rss	restore state. Set this bit to 0 when the controller completes the recovery operation.
[24]	RO	sss	Save state. When the controller finishes saving the operation, set this bit to 0.
[23]	RO	core_idle	core idle state. Indicates that the core has completed the transfer of all RxFIFO data to the system memory, completed the output of all linked lists, and reset all event counters to 0.

[22] RO		devctrlhlt	Device controller hangs. When PERI_USB3_DCTL[run_stop] is 1, this bit is 0; when the software writes 0 to PERI_USB3_DCTL[run_stop], and the core is idle and the lower layer completes the disconnection operation, the core will write 1 to this bit.
[21:18] RO		usb_lnk_st	USB/Link status. SS mode: 0x0ÿU0ÿ 0x1ÿU1ÿ 0x2ÿU2ÿ 0x3ÿU3ÿ 0x4ÿSS_DISÿ 0x5ÿRX_DETÿ 0x6ÿSS_INACTÿ 0x7ÿPOLLÿ 0x8ÿRECOVÿ 0x9ÿHRESETÿ 0xaÿCMPLYÿ 0xbÿLPBKÿ 0xfÿResume/Resetÿ Other: reserved. HS/FS/LS mode: 0x0: On state; 0x2: Sleep (L1) state; 0x3: Suspend (L2) state; 0x4: Disconnected state (default state); 0x5: Early Suspend state (only valid when the sleep function is off); 0xe: Reset (valid only when the sleep function is enabled); 0xf: Resume (only valid when the sleep function is enabled); Others: reserved.
[17] RO		reserved	reserve.
[16:3] RO		soft	Number of SOF frames/microframes: HS mode [16:6] Indicates the number of frames [5:3] Indicates the number of microframes Full speed mode [16:14] Don't use [13:3] to refer to the number of frames

[2:0] RO		connect_spd	Connection speed indication. 000: High speed (PHY clock works at 30 or 60MHz); 001: Full speed (PHY clock works at 30 or 60MHz); 010: Low speed (PHY clock works at 6MHz); 010: Low speed (PHY clock works at 48MHz) 100: Overspeed (PHY clock works at 125 or 250MHz).

PERI_USB3_DGCMDPAR

PERI_USB3_DGCMDPAR is the peripheral class command parameter register.

Offset Address	Register Name	Total Reset Value
0xC710	PERI_USB3_DGCMDPAR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	parameter31_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0] RW	parameter31_0	Configure peripheral class command parameter register.	

PERI_USB3_DGCMD

PERI_USB3_DGCMD is the peripheral class command register.

Offset Address	Register Name	Total Reset Value
0xC714	PERI_USB3_DGCMD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
Name	reserved		reserved			reserved	cmdtyp
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0						

Bits	Access Name		Description
[31:16] RO		reserved	reserve.
[15] RO		cmd_status	command status. 0: The Device controller processes the command successfully; 1: The Device controller encountered an error while processing the command.

[14:11] RO		reserved	reserve.
[10] RWSC cmdact			The software sets this bit to 1 to enable the Device controller to execute the generated command The controller sets this bit to 0 after executing the command.
[9]	RO	reserved	reserve.
[8] WO cmdloc			command complete interrupt. Note: When PERI_USB3_DCTL[run_stop] is 0, this bit is 1.
[7:4] RO		reserved	reserve.
[3:0] RW cmdtyp			command type. 0x0: reserved; 0x1: set the configuration of the endpoint; 0x2: Set the endpoint transmission source configuration; 0x3: get endpoint status; 0x4: setup pending; 0x5: clear pending; 0x6: start transmission; 0x7: follow new transmission; 0x8: end transmission; 0x9: start new configuration; others: reserved.

PERI_USB3_DALEPENA

PERI_USB3_DALEPENA is the peripheral USB endpoint enable register.

Offset Address	Register Name	Total Reset Value
0xC718	PERI_USB3_DALEPENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usbactep																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW usbactep	Indicates whether the USB port is valid under the current configuration and interface. For USB input endpoints 0-15 and output endpoints 0-15, all 32 endpoints are controlled by 1 bit each, the even bits control the output endpoints, and the odd bits control the input endpoints. Example: Bit[0]: USB output endpoint 0 Bit[1]: USB input endpoint 0 Bit[2]: USB output endpoint 1 Bit[3]: USB input endpoint 1 Bit0 and bit1 must be set when operating this register, so The control endpoint in the physical endpoint will be enabled after USBReset. When a USB reset is detected, the application software will clear the bits corresponding to all endpoints except output endpoint 0/input endpoint 0. When receiving the setting configuration and setting interface request, the application program correspondingly sets the endpoint register and these bits of this register.

PERI_USB3_DEPCMDPAR2N

PERI_USB3_DEPCMDPAR2N is Peripheral Endpoint Command Parameter Register 2.

Offset Address	Register Name	Total Reset Value
0xC810	PERI_USB3_DEPCMDPAR2N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW parameter2	The peripheral's physical endpoint command parameter register 2, which must be configured before executing the command.

PERI_USB3_DEPCMDPAR1N

PERI_USB3_DEPCMDPAR1N is Peripheral Endpoint Command Parameter Register 1.

Offset Address	Register Name	Total Reset Value
0xC814	PERI_USB3_DEPCMDPAR1N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter1	The physical endpoint command parameter register 1 of the peripheral, which must be configured before executing the command.

PERI_USB3_DEPCMDPAR0N

PERI_USB3_DEPCMDPAR0N is Peripheral Endpoint Command Parameter Register 0.

Offset Address	Register Name	Total Reset Value
0xC818	PERI_USB3_DEPCMDPAR0N	0x0000_0000

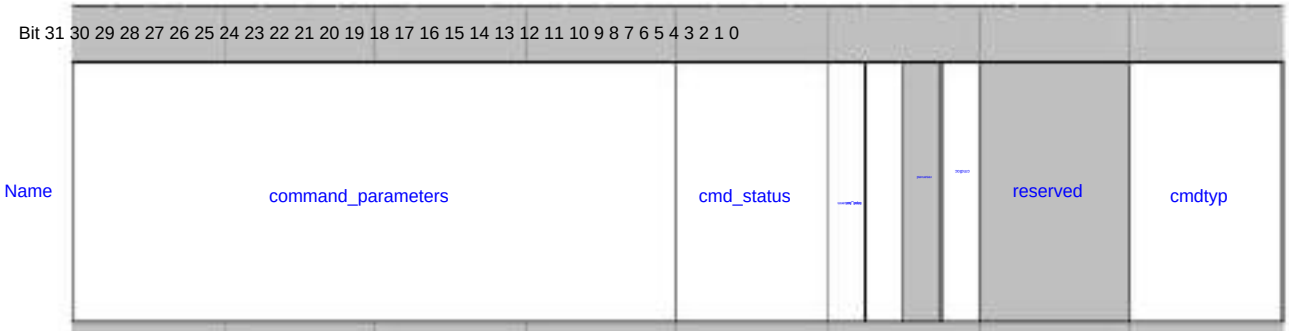
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter0	The peripheral's physical endpoint command parameter register 0, which must be configured before or with the command. Because the command only requires 32bit parameters, this register must be configured along with the command register.

PERI_USB3_DEPCMDN

PERI_USB3_DEPCMDN is the peripheral physical endpoint command register.

Offset Address	Register Name	Total Reset Value
0xC81C	PERI_USB3_DEPCMDN	0x0000_0000



Bits	Access Name		Description
[31:16] RW		command_paramet [31:16]: ers	These bits represent the parameters of the command, and the meaning of writing the relevant value to the register is as follows: For the start transfer command: [31:16]: Indicates the USB StreamID declared for this transfer. For the start transmission command of the real-time endpoint: Indicates the number of microframes (frames) when the first TRB is applied. For update transfer, end transfer, and start new configuration commands: [22:16]: Transmission resource index (XferRscIdx). The hardware declares the transfer resource index for the transfer, which returns a response to the start transfer command; the application software declares the transfer resource index for the start new configuration command.
[15:12] RW	cmd_status		Command Completion Status: These bits hold additional information about the completed command. This information is exactly the same as bit[15:12] of the endpoint command completion event.
[11] RW	hipri_forcerm		HighPriority: Valid only at the beginning of the transfer command. ForceRM: only works at the end of the transfer command.
[10] RW	cmd_act		Software sets this bit to 1 to enable the peripheral endpoint controller to execute class commands. When the CmdStatus of this register is valid and the endpoint is ready to receive another command, the peripheral controller will set this bit to 0. But this does not indicate that the previously sent commands have been fulfilled.
[9]	RO	reserved	reserve.
[8] RW	cmdloc		Command completion interrupt: When this bit is set to 1, it indicates that after executing the command, the peripheral controller generates a general endpoint command completion event. Note: When PERI_USB3_DCTL[run_stop]=0 , this bit cannot be set to 1.
[7:4] RO		reserved	reserve.

[3:0] RW cmdtyp			Defines the type of command the driver asks the core to execute. 0x0: reserved; 0x1: Set endpoint configuration (64 or 96bit parameter); 0x2: Set endpoint transmission resource configuration (32bit parameter); 0x3: Get endpoint status (no parameter required); 0x4: Set Stall (no parameter needed); 0x5: Clear Stall (0x6: start transmission (64bit parameter); 0x7: update transmission (no parameter); 0x8: end transmission (no parameter); 0x9: start new configuration (no parameter); others: reserved.

12.11 LSADC_CTRL

12.11.1 Overview

LSADC_CTRL (LSADC Controller) provides the ADC controller interface to connect to the on-chip LSADC, and completes functions such as driving the on-chip LSADC and reporting key values.

12.11.2 Features

LSADC has the following characteristics:

The supply voltage is 3.3V.

The scanning frequency cannot be higher than 200K/

s. 4 independent channels.

LSADC_CTRL has the following characteristics:

Supports single startup, scans one channel at a time, does not filter glitches, and provides interrupts and queries.

Support continuous scanning function:

ÿAutomatically poll each channel according to ch_vld;

ÿStart continuous query according to Tscan (scanning interval); ÿFilter

glitches according to Tglitch to complete effective judgment of glitches; ÿReport LSADC

conversion results and corresponding channel numbers; ÿReport interruption:

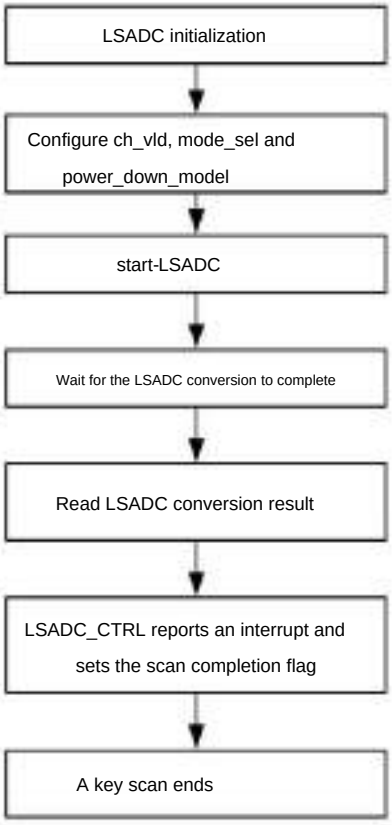
Yes Key interrupt, key change interrupt.

12.11.3 Working method

Single scan processing flow

In the single read mode (LSADC_CTRL0[model_sel]=0), the CPU configures the scan channel number, scan mode, and key-value mapping table information, and starts LSADC to complete a channel scan. LSADC_CTRL Gets the ADC conversion value, reports an interrupt and sets the conversion completion flag. In single read mode, glitch filtering is not performed.

Figure 12-66 Single scan processing flow



Continuous Scanning Process Flow

In the continuous reading mode (LSADC_CTRL0[model_sel]=1), the CPU sets the continuous scanning time interval Tscan, glitch width (Tglitch), and valid channel number (ch_vld) according to the application scenario, and starts LSADC_CTRL.

LSADC_CTRL completes the scan of a valid channel within a time interval Tscan. When the next scanning time arrives, the scanning of the next valid channel is started. After the scanning of all valid channels is completed, start the next round of scanning of valid channels (as shown in Figure 12-68). The polling of each channel is shown in Figure 12-67 .

Figure 12-67 Schematic diagram of channel polling scan in continuous scan mode

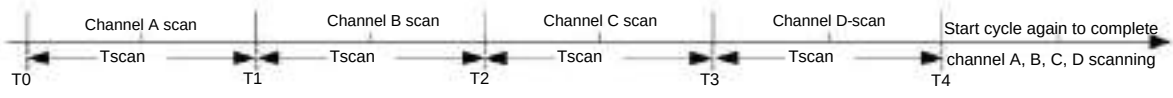
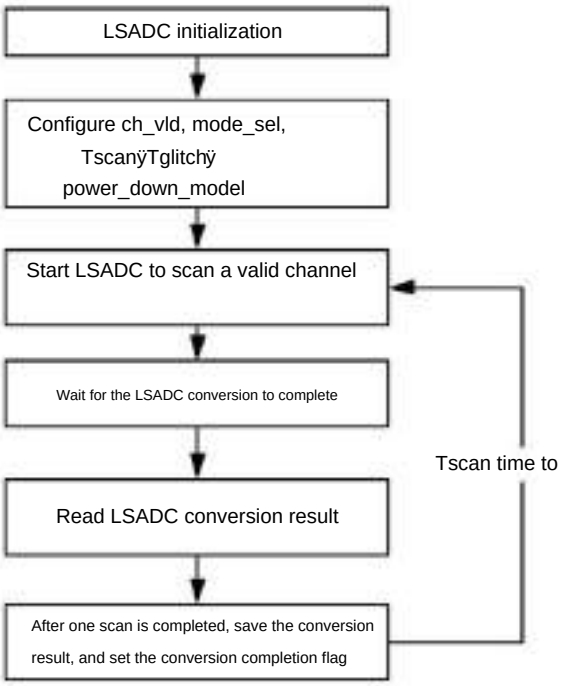


Figure 12-68 Continuous scan processing flow



Filtration Burr Process

The glitch filtering circuit adopts majority decision algorithm. In the glitch filtering window Tglitch, if there are many times of ADC sampling value value, and value is not the ADC sampling value when the key is empty, then value is considered as a valid key value, otherwise it is considered as a glitch signal.

In the continuous scan mode, for the effective scan value obtained after filtering the burr, an interrupt is reported and the scan completion flag is set. Because LSADC has an error every time it samples, the result value is 6bit precision.

Users can set whether to enable the hardware glitch filtering function.

Reported interrupts include: there is a key interrupt.

12.11.4 LSADC_CTRL register overview

An overview of the LSADC_CTRL register is shown in Table 12-38 .

Table 12-38 LSADC_CTRL register overview (base address is 0x120E_0000)

offset address	name	describe	page number
0x0000	LSADC_CTRL0	LSADC_CTRL Configuration Register	12-356
0x0004	LSADC_CTRL1	glitch filter configuration register	12-357
0x0008	LSADC_CTRL2	scan interval configuration register	12-358
0x0010	LSADC_CTRL4	Interrupt Enable Register	12-358

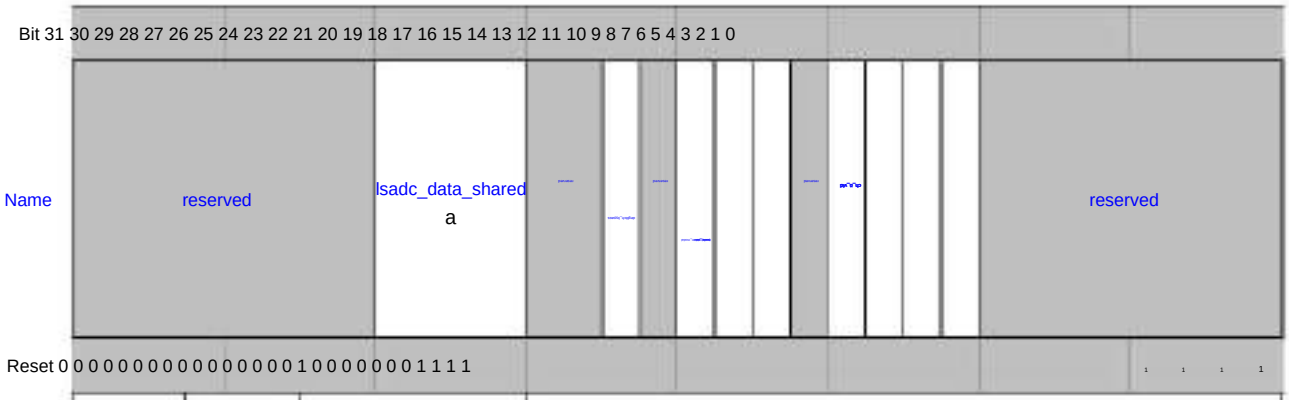
offset address	name	describe	page number
0x0014	LSADC_CTRL5	Interrupt Status Register	12-359
0x0018	LSADC_CTRL6	interrupt clear register	12-360
0x001C	LSADC_CTRL7	Start configuration register	12-361
0x0020	LSADC_CTRL8	Stop configuration register	12-361
0x0024	LSADC_CTRL9	conversion result precision register	12-362
0x0028	LSADC_CTRL10	LSADC_ZERO Register	12-362
0x002C	LSADC_CTRL11	LSADC Data Holding Register 1	12-362
0x0030	LSADC_CTRL12	LSADC Data Holding Register 2	12-363
0x0034	LSADC_CTRL13	LSADC Data Holding Register 3	12-363
0x0038	LSADC_CTRL14	LSADC Data Holding Register 4	12-364

12.11.5 LSADC_CTRL register description

LSADC_CTRL0

LSADC_CTRL0 is the LSADC_CTRL configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	LSADC_CTRL0	0x0000_80FF



Bits	Access	Name	Description
[31:24]	RO	reserved	reserve.
[23:20]	RW	lsadc_data_delta	LSADC conversion result error range (used in continuous scan mode, use to determine the error range between two conversion results, within the error range, the two conversion results are considered to be the same).
[19:18]	RO	reserved	reserve.

[17] RW	deglitch_bypass		Burr filtering function bypass. (This function is used in continuous scan mode) 0: enable glitch filtering function; 1ÿbypassÿ
[16] RO		reserved	reserve.
[15] RW	lsadc_reset		Set whether LSADC enters reset state. 1: enter reset state; 0: Exit reset state.
[14] RW		operation. supported;1 power_down_mode 0: not	Whether to support power_down 1: Support.
[13] RW	model_sel		LSADC_CTRL Scan mode selection. 0: single scan mode; 1: continuous scan mode;
[12] RO		reserved	reserve.
[11] RW	ch_d_vld		Whether LSADC channel D is valid. 0: invalid; 1: valid;
[10] RW	ch_c_vld		Whether LSADC channel C is valid. 0: invalid; 1: valid;
[9] RW	ch_b_vld		Whether LSADC channel B is valid. 0: invalid; 1: valid;
[8] RW	ch_a_vld		Whether LSADC channel A is valid. 0: invalid; 1: Valid.
[7:0] RO		reserved	reserve.

LSADC_CTRL1

LSADC_CTRL1 is the glitch filter configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	LSADC_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	glitch_sample																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW glitch_sample	Glitch filtering time window (when the conversion result of LSADC remains unchanged within this time window, the conversion result is considered to be a valid value, otherwise it is considered to be a glitch. The value of this window is generally set to ms level, and cannot be used in continuous scan mode configured as 0).

LSADC_CTRL2

LSADC_CTRL2 is the scan interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	LSADC_CTRL2	0x0000_0000

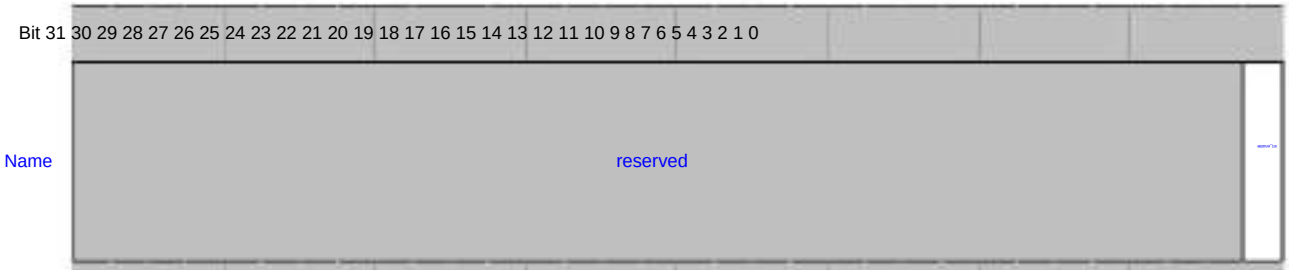
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	time_scan																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RW time_scan	In continuous scanning mode, the continuous scanning time interval between two scanning channels (3M clock domain N/3MHz, the continuous scanning time interval should be greater than the conversion time of LSADC 14cycle, and cannot be configured as 0 in continuous scanning mode).

LSADC_CTRL4

LSADC_CTRL4 is the interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0010	LSADC_CTRL4	0x0000_0000

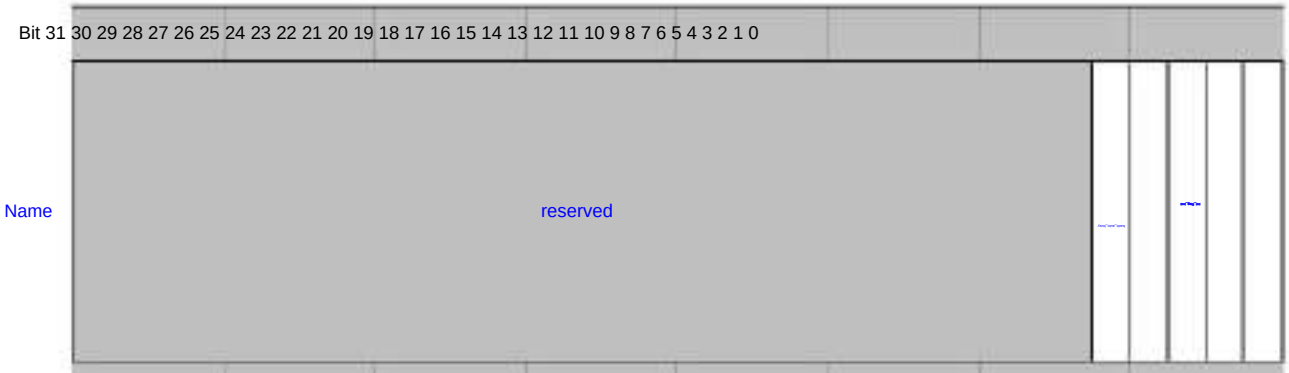


Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	int_enable	Scan value valid interrupt enable bit. 0: disable; 1: enable.

LSADC_CTRL5

LSADC_CTRL5 is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	LSADC_CTRL5	0x0000_0000



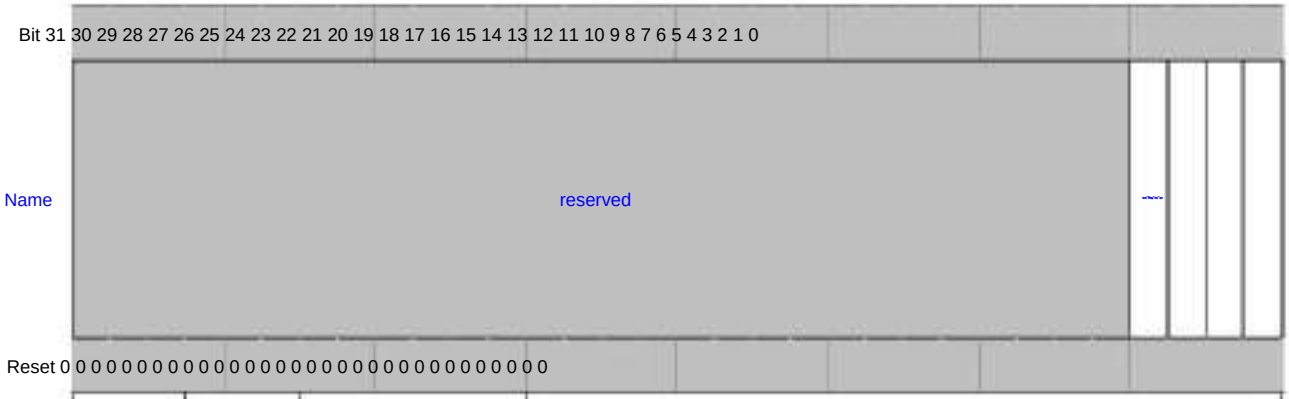
Bits	Access	Name	Description
[31:5]	RO	reserved	reserve. Invalid for write, read as 0.
[4]	RO	lsadc_auto_busy	In auto scan mode, LSADC busy status indication. 0ÿIDLEÿ 1ÿBUSYÿ

[3]	RO	int_flag_ind	Channel D scan value valid interrupt flag. 0: no interrupt; 1: There is an interrupt.
[2]	RO	int_flag_inc	Channel C scan value valid interrupt flag. 0: no interrupt; 1: There is an interrupt.
[1]	RO	int_flag_inb	Channel B scan value valid interrupt flag. 0: no interrupt; 1: There is an interrupt.
[0]	RO	int_flag_ina	Channel A scan value valid interrupt flag. 0: no interrupt; 1: There is an interrupt.

LSADC_CTRL6

LSADC_CTRL6 is the interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0018	LSADC_CTRL6	0x0000_0000



Bits	Access Name		Description
[31:4] RO		reserved	reserve.
[3] WO clr_int_	flag_ind		Channel D Interrupt Clear Register. 0: do not clear; 1: Clear interrupt.
[2] WO clr_int_	flag_inc		Channel C Interrupt Clear Register. 0: do not clear; 1: Clear interrupt.

[1] WO	clr_int_flag_inb		Channel B Interrupt Clear Register. 0: do not clear; 1: Clear interrupt.
[0] WO	clr_int_flag_ina		Channel A Interrupt Clear Register. 0: do not clear; 1: Clear interrupt.

LSADC_CTRL7

LSADC_CTRL7 is the Start configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	LSADC_CTRL7	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	start
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	start	LSADC_CTRL start signal (writing any value to this register can start LSADC_CTRL).

LSADC_CTRL8

LSADC_CTRL8 is the Stop configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	LSADC_CTRL8	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	stop
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	stop	Stop auto-scanning (in auto-scanning mode, writing any value to this register can stop the auto-scanning function of lsadc_ctrl, you need to write enable start again to restart auto-scanning)

LSADC_CTRL9

LSADC_CTRL9 is the conversion result precision register.

Offset Address	Register Name	Total Reset Value
0x0024	LSADC_CTRL9	0x0000_03FF

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	lsadc_active_bit
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_active_bit	Precision of lsadc conversion result. 10'b1111111111 means 10-bit precision; 10'b1111111110 means 9-bit precision; …… 10'b1000000000 means 1 bit precision

LSADC_CTRL10

LSADC_CTRL10 is the LSADC_ZERO register.

Offset Address	Register Name	Total Reset Value
0x0028	LSADC_CTRL10	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	lsadc_zero
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_zero	The value of LSADC when no key is pressed on the keyboard.

LSADC_CTRL11

LSADC_CTRL11 is LSADC data holding register 1.

Offset Address	Register Name	Total Reset Value
0x002C	LSADC_CTRL11	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / lsadc_data_where
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_data_ina	LSADC channel A scan value.

LSADC_CTRL12

LSADC_CTRL12 is LSADC data holding register 2.

Offset Address	Register Name	Total Reset Value
0x0030	LSADC_CTRL12	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / lsadc_data_inb
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_data_inb	LSADC channel B scan value.

LSADC_CTRL13

LSADC_CTRL13 is LSADC data holding register 3.

Offset Address	Register Name	Total Reset Value
0x0034	LSADC_CTRL13	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / lsadc_data_inc
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_data_inc	LSADC channel C scan value.

LSADC_CTRL14

LSADC_CTRL14 is LSADC data holding register 4.

Offset Address	Register Name	Total Reset Value
0x0038	LSADC_CTRL14	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / lsadc_data_ind
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	lsadc_data_ind	LSADC channel D scan value.

12.12 PWM

12.12.1 Overview

Hi3519V100 provides a group of 8 independent pulse width modulation signal outputs.

12.12.2 Features

For each set of PWM outputs:

3MHz, 24MHz and 50MHz clock sources are selectable.

There is a 32bit counter inside, and the output cycle can be configured. Support the highest 25MHz (50MHz/2) output, the lowest about 0.0007Hz (3MHz/ 4294967296) output.

There is a 32bit counter inside, and the number of output high level beats can be configured.

Internal 10bit counter, the number of output pulses (up to 1023) can be configured. It can work in fixed number output mode and constant output mode:

ÿWhen pwmn_keep (pwmn indicates the nth channel pwm) is configured as 0, pwmn outputs a fixed number of square waves, and the number is determined by the pwmn_num (pwmn indicates the nth channel pwm)

register control. ÿWhen pwmn_keep (pwmn indicates nth PWM) is configured as 1, pwmn always outputs square wave.

12.12.3 Working method

The PWM works internally at 3MHz or 24MHz or 50MHz, and the PWM (taking PWM0 as an example) output configuration process is as follows:

Step 1. Select an appropriate clock source, and obtain the required number of cycles and high-level beats by calculation.

Step 2. Write the corresponding data into PWM0_CFG0, PWM0_CFG1, PWM0_CFG2 registers.

Step 3. Write 1 to PWM0_CTRL bit[0] to enable PWM output.

----Finish

For example: It is necessary to output a waveform with a frequency of 3kHz, a high level of 72.5% (that is, a duty cycle), and a pulse number of 10.

Select the 3MHz clock as the clock source, and configure the number of cycles as 3MHz /3kHz=1000, which is 1000 after rounding, and the hexadecimal value is 0x00003E8. The number of high levels is configured as 1000 (number of cycles) x 72.5% (duty cycle) = 725, which is 725 after rounding, and the hexadecimal value is 0x00002D5.

Follow the steps below to operate the registers to output the required waveform:

Step 4. Write 0x2 to PERI_CRG55, select the PWM clock source as 3MHz, and turn on the PWM clock.

Step 5. Read PWM0_STATE2 bit[10], wait for bit[10] to be 0 (indicating PWM is idle and can output square wave)

Step 6. Write 0x0000_03E8 to PWM0_CFG0 .

Step 7. Write 0x0000_02D5 to PWM0_CFG1 .

Step 8. Write 0x0000_000A to PWM0_CFG2 .

Step 9. Write 0x1 to PWM0_CTRL . (The following steps can be omitted, just to verify whether the square wave being output output by configuration)

Step 10. Read PWM0_STATE2 bit[10], wait for bit10 to be 1 (means PWM is outputting square wave)

Step 11. Read PWM0_STATE0 and 0x0000_03E8 for verification.

Step 12. Read PWM0_STATE1 and 0x0000_02D5 for verification.

Step 13. Read PWM0_STATE2 bit[9:0] and 0x0A for verification (when bit[10] is 1, it means that PWM is outputting a square wave; when this bit is 0, it means that the set number of square waves has been output) .

----Finish

12.12.4 PWM register overview

The registers of PWMn (n=0, 1, 2, 3, 4, 5, 6, 7) have the same function except for the different base addresses. The base addresses of each PWM register are shown in Table 12-39 .

Table 12-39 Register base address table of PWMn

n value	base address
0	0x1213_0000
1	0x1213_0020
2	0x1213_0040
3	0x1213_0060

n value	base address
4	0x1213_0080
5	0x1213_00A0
6	0x1213_00C0
7	0x1213_00E0

Taking the description of the PWM0 register as an example, the register overview is shown in Table 12-40 .

Table 12-40 PWM0 register overview (base address is 0x1213_0000)

offset address	name	describe	page number
0x0000	PWM0_CFG0	Configuration 0 Register for PWM0	12-366
0x0004	PWM0_CFG1	Configuration 1 Register for PWM0	12-367
0x0008	PWM0_CFG2	Configuration 2 Register for PWM0	12-367
0x000C	PWM0_CTRL	Control register for PWM0	12-367
0x0010	PWM0_STATE0	PWM0 state 0 register	12-368
0x0014	PWM0_STATE1	PWM0 state 1 register	12-368
0x0018	PWM0_STATE2	PWM0 state 2 register	12-369

12.12.5 PWM register description

PWM0_CFG0

PWM0_CFG0 is the configuration 0 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	pwm0_period	
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 0 0 0 1 1 1 1

Bits	Access	Name	Description
[31:0]	RW	pwm0_period	The period number of PWM0. 说明 The required configuration value must be ÿ 2.

PWM0_CFG1

PWM0_CFG1 is the configuration 1 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	pwm0_duty
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1

Bits	Access	Name	Description
[31:0]	RW	pwm0_duty	If the number of high-level beats of PWM0 is greater than or equal to the number of cycles, the output will always be high-level. Notice: The required configuration value must be ÿ 1.

PWM0_CFG2

PWM0_CFG2 is the configuration 2 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved / pwm0_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	reserve.
[9:0]	RW	pwm0_num	The number of square waves output by PWM0.

PWM0_CTRL

PWM0_CTRL is the control register of PWM0.

Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Name	reserved		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:3]	RO	reserved	reserve.
[2]	RW	pwm0_keep	PWM output mode. 0: PWM0 outputs a fixed number of square waves; 1: PWM0 outputs square wave all the time.
[1]	RW	pwm0_inv	PWM output positive and negative phase control. 0: PWM0 outputs square wave normally; 1: PWM0 inverts and outputs a square wave.
[0]	RW	pwm0_enable	PWM enable control. 0: PWM0 module is off; 1: PWM0 module is enabled.

PWM0_STATE0

PWM0_STATE0 is the state 0 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	pwm0_period_st
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	pwm0_period_st	The number of counting periods used by the internal modules of PWM0.

PWM0_STATE1

PWM0_STATE1 is the state 1 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm0_duty_st																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0] RO	pwm0_duty_st	The number of high-level pulses used by internal modules of PWM0.

PWM0_STATE2

PWM0_STATE2 is the state 2 register of PWM0.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										pwmn_cnt_st														pwm0_period_st							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:22] RO	reserved	reserve.
[21:12] RO	pwm0_cnt_st	The PWM0 module also needs to output the number of square waves. Only meaningful when pwm0_busy==1, pwm0_keep_st==0.
[11] RO	pwm0_keep_st	The internal module of PWM0 adopts the output square wave mode. 0: output a fixed number of square waves; 1: Output square wave all the time.
[10] RO	pwm0_busy	Working status of PWM0 module. 0: idle, output completed; 1: A square wave is being output.
[9:0] RO	pwm0_period_st	The number of output square waves used by internal modules of PWM0.

Table of contents

illustration catalog

table of contents

13 security module

13.1 CIPHER

13.1.1 Overview

CIPHER is a module that implements DES (Data Encryption Standard)/3DES and AES (Advanced Encryption Standard) encryption and decryption processing. The implementation of DES/3DES and AES algorithms complies with FIPS46-3/FIPS 197 standards. The working mode of DES/3DES and AES complies with FIPS -81/NIST special800-38a standard.

The CIPHER module is suitable for efficient encryption and decryption processing of large amounts of data, and can support the encryption and decryption of a single packet or the encryption and decryption of multiple packets at a time.

13.1.2 Features

The CIPHER module has the following characteristics:

The AES key length supports 128 bits, 192 bits, and 256 bits. When the key is configured by the chip key management module, the key length only supports 128 bits.

The DES key length supports 64 bits, and the value of 0, 8, 16, 24, 32, 40, 48, and 56 bits is the parity value of each byte, which is not used in actual encryption and decryption operations.

3DES supports the mode of 3 keys and also supports the mode of 2 keys. When the key is configured by the chip key management module, it only supports the mode of 2 keys.

AES ÿÿ CCM(Counter with Cipher Block Chaining-Message Authentication Code)ÿ
GCM (Galois/Counter Mode), ECB (Electronic CodeBook), CBC (Cipher Block Chaining), 1/8/128-CFB (Cipher FeedBack), 128-OFB (Output FeedBack) and CTR (Counter) several working modes, The working mode complies with NIST special800-38a standard.

DES/3DES supports ECB, CBC, 1/8/64-CFB, 1/8/64-OFB several working modes, and the working mode complies with the FIPS-81 standard.

In ECB, CBC, CFB, OFB, and CTR working modes, it supports the encryption and decryption operations of multiple packets at one time, and also supports the encryption and decryption operations of a single packet at one time.

In the CTR working mode of AES, it supports the encryption and decryption operation of multiple packets at one time, and also supports the encryption and decryption operation of a single packet at one time.

Provide encryption and decryption keys for 8 CPU configurations, which can be configured as 64bits, 128bits, 192bits or 256bits.

Provide 8 keys configured by the chip key management module, fixed at 128bits, the main CPU can write but not read.

Provide a single packet encryption and decryption channel and 7 channels of multi-packet encryption and decryption channels. The single-packet encryption and decryption channel can only complete one single-packet encryption and decryption at a time, and the data is written into the channel register by the CPU, and the result is read by the CPU. The multi-packet encryption and decryption channel automatically reads data from DDR by logic, completes encryption and decryption, and then

automatically writes back to DDR. Each channel adopts the weighted round-robin working method. Except the weight value of the single group channel is 1 by default, the weight value of other multi-group

channels can be configured. Any channel can use the same set of keys or a different set of keys.

When the multi-packet channel data is not an integer multiple of the encryption and decryption block, the last data less than one block will not be encrypted and decrypted.

Multi-packet encryption and decryption channels support byte

addresses. The multi-packet encryption and decryption channel supports multi-linked list structure, and supports splicing multiple linked list data. The length of each linked list is represented by 20 bits, that is, the maximum data volume

is 1M-1 byte. Provide interrupt status query, interrupt mask and interrupt clear functions.

Each channel provides individual interrupt handling and control. Support

multi-packet interrupt and aging time interrupt.

13.1.3 Functional Description

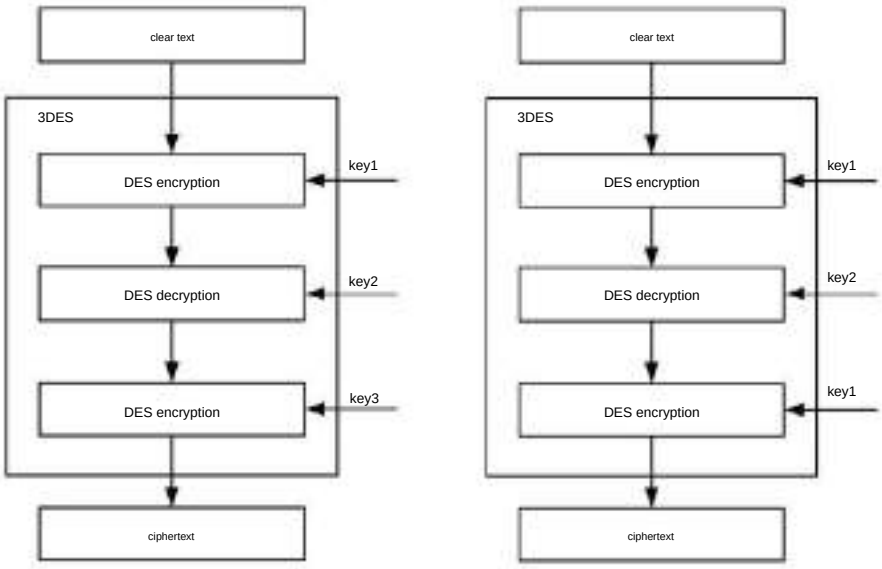
Several working modes supported by DES/3DES and AES algorithms conform to FIPS-81 standard and NIST special800-38a/c/d standard respectively. For DES/3DES and AES algorithms, the working modes of ECB, CBC and CFB are the same, OFB and CTR (Only included in the AES algorithm) the working mode is slightly different.

3DES algorithm

3DES supports the operation of 3 keys and 2 keys. The operation of 2 keys can be regarded as a simplified case of 3 keys. The third key (key3) in the operation of 2 keys Both use the first key (key1) instead.

The 3DES encryption operation process of 3 keys and 2 keys is shown in Figure 13-1 .

Figure 13-1 3DES encryption operation with 3 keys and 2 keys

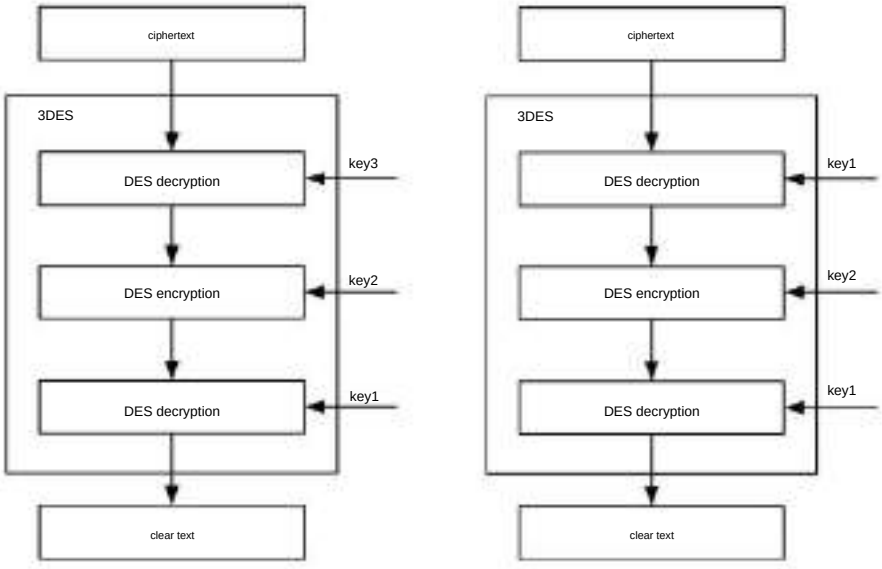


Cryptographic operations with 3 keys

Cryptographic operations with 2 keys

The 3DES decryption operation process of 3 keys and 2 keys is shown in Figure 13-2 .

Figure 13-2 3DES decryption operation with 3 keys and 2 keys



Decryption operation with 3 keys

Decryption operation with 2 keys

ECB mode

In ECB (Electronic CodeBook) mode, the encryption and decryption algorithms are directly applied to each packet data, and the operations of each packet are independent. This feature enables the encryption operation of the plaintext and the decryption operation of the ciphertext to be performed in parallel. The electronic codebook (ECB) modes of AES/DES and 3DES are shown in Figure 13-3 and Figure 13-4 respectively .

Figure 13-3 Electronic Code Book (ECB) mode of AES/DES

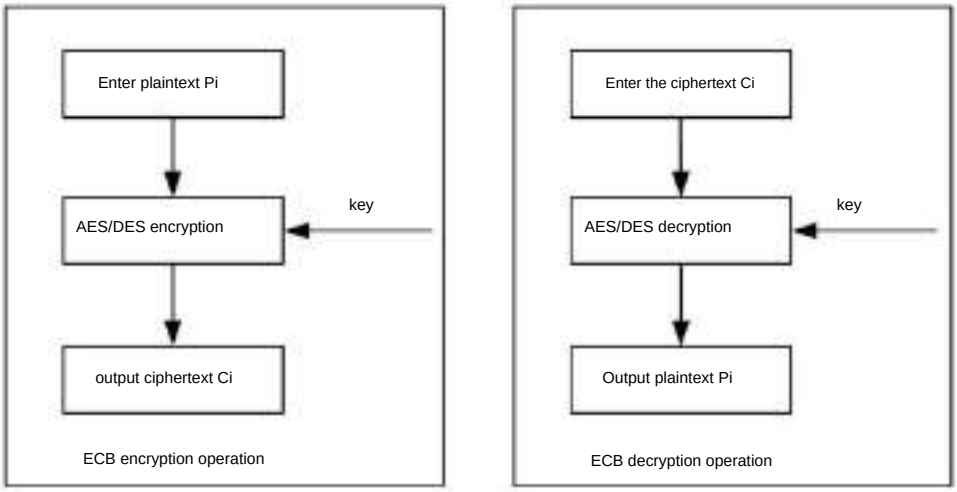
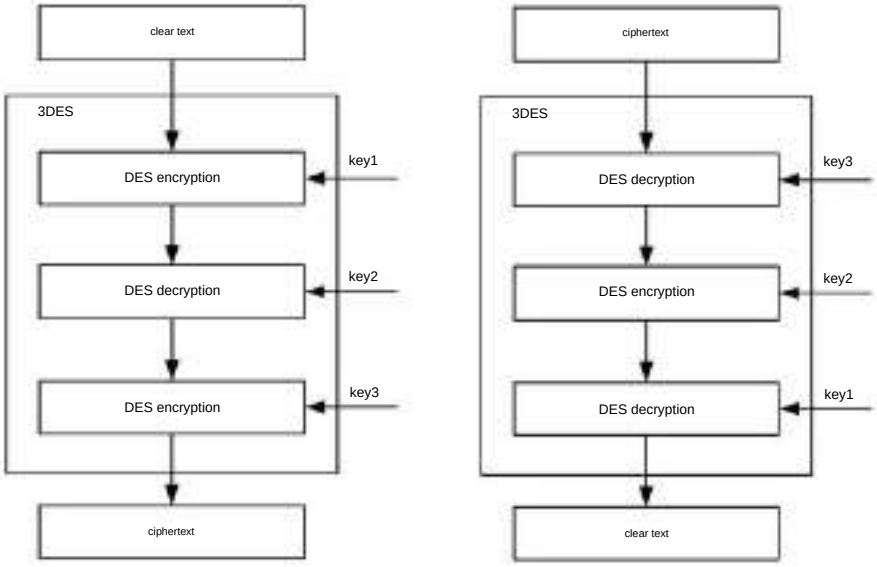


Figure 13-4 Electronic Code Book (ECB) Mode of 3DES



CBC mode

In CBC (Cipher Block Chaining) mode, the encrypted input plaintext group needs to be XORed with the input vector IV (Intialization Vector) before entering the encryption operation, and the encryption processing of each plaintext group is the same as that of the previous plaintext group. The results (ie, ciphertext) are correlated, so encryption operations in CBC mode cannot be processed in parallel. However, the decryption operation does not depend on the plaintext output of the previous packet, and can be processed in parallel. The cipher block chaining (CBC) modes of AES/DES and 3DES are shown in Figure 13-5 and Figure 13-6 , respectively .

Figure 13-5 Cipher Block Chaining (CBC) mode of AES/DES

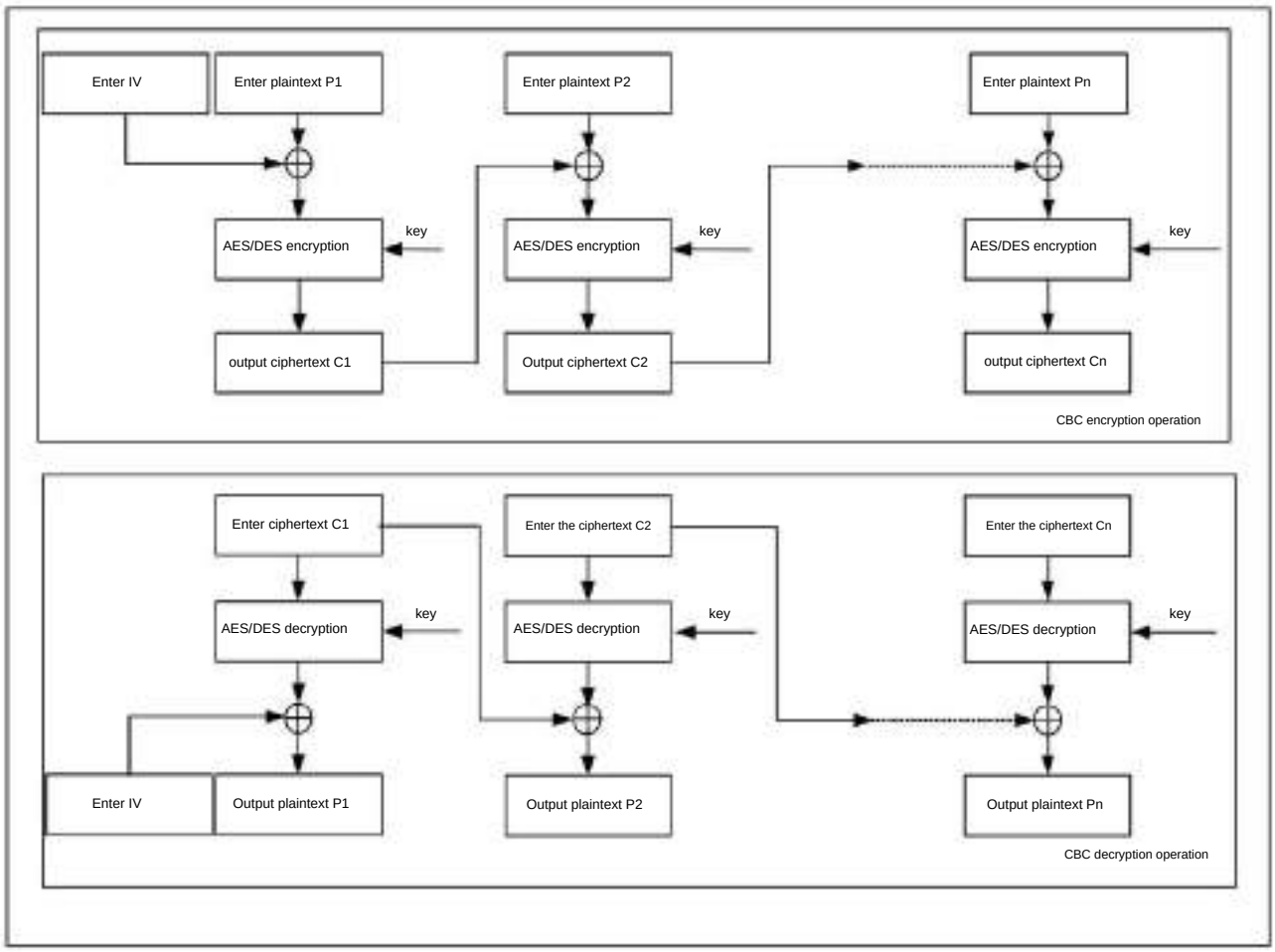
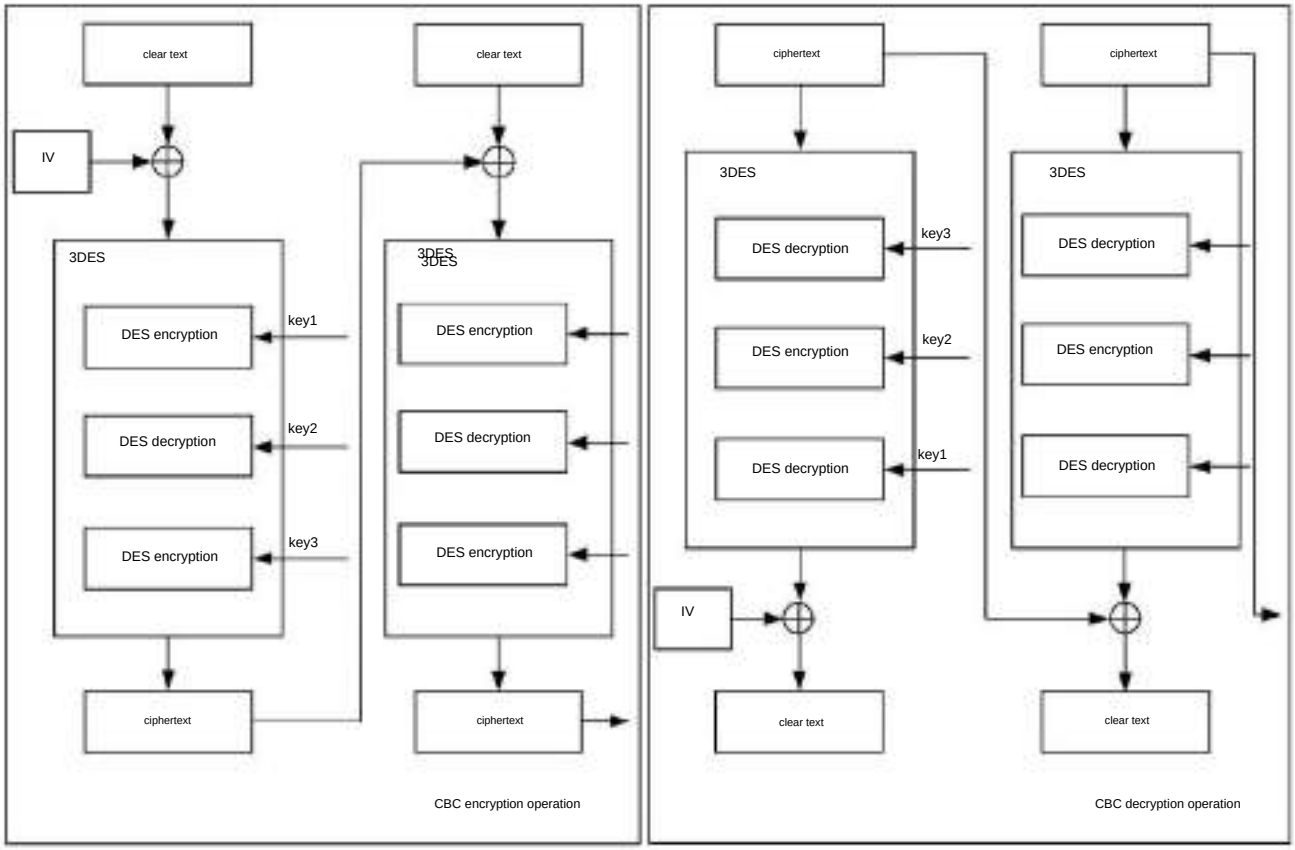


Figure 13-6 Cipher block chaining (CBC) mode of 3DES



CFB mode

The CFB (Cipher FeedBack) mode is a working mode for converting block ciphers into stream ciphers, which can be realized by selecting the number of CFB operations. The number of bits in the shift operation is represented by s bits, and there are the following two situations regarding the s bits:

For DES/3DES, s bits can be 1, 8, or 64 bits.

For AES, s bits can be 1 bit, 8 bits, or 128 bits.

The s-bit cipher feedback (CFB) mode of AES/DES and the s-bit cipher feedback (CFB) mode of 3DES are shown in Figure 13-7 and Figure 13-8 respectively .

Figure 13-7 s-bit cipher feedback (CFB) mode of AES/DES

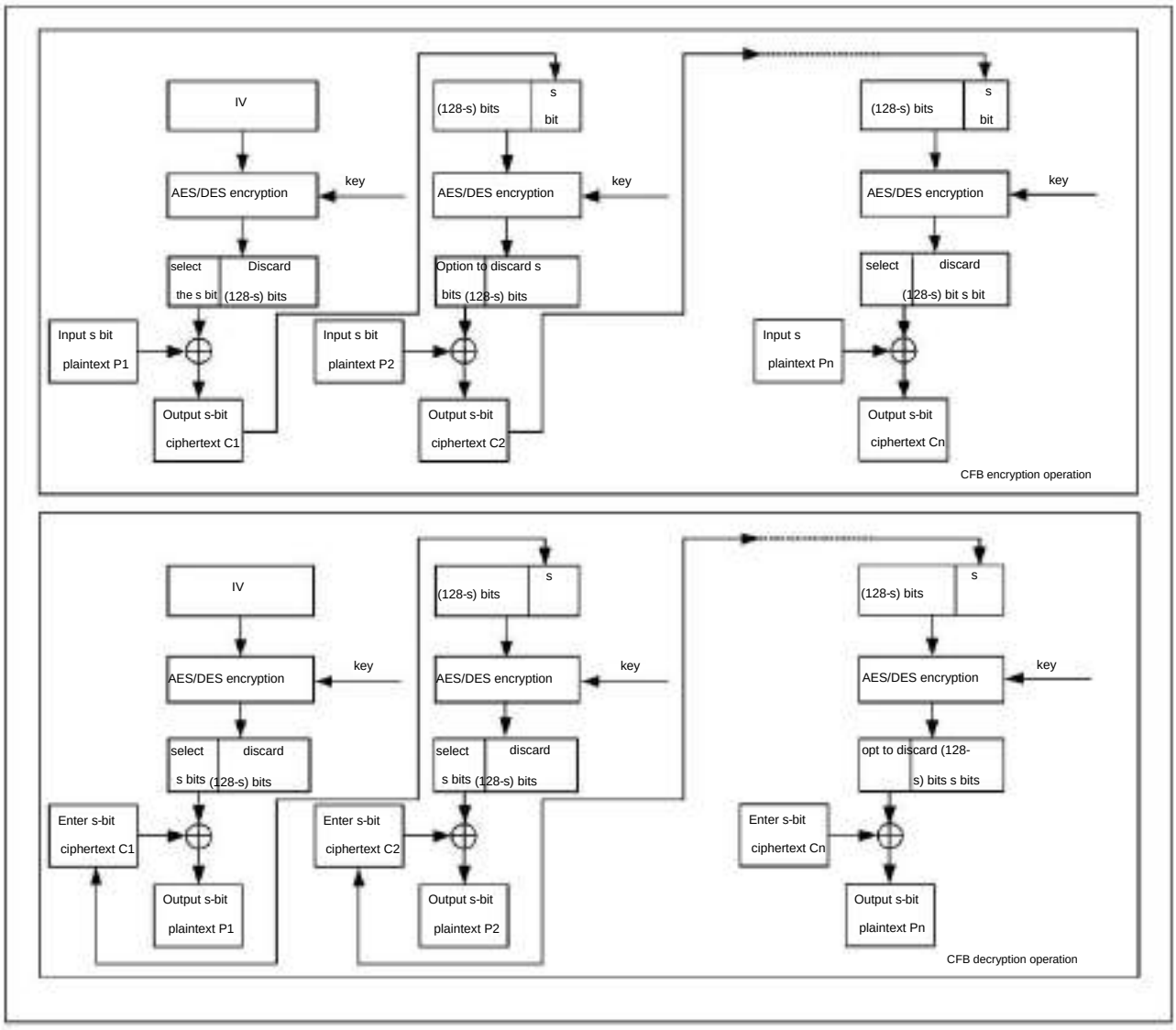
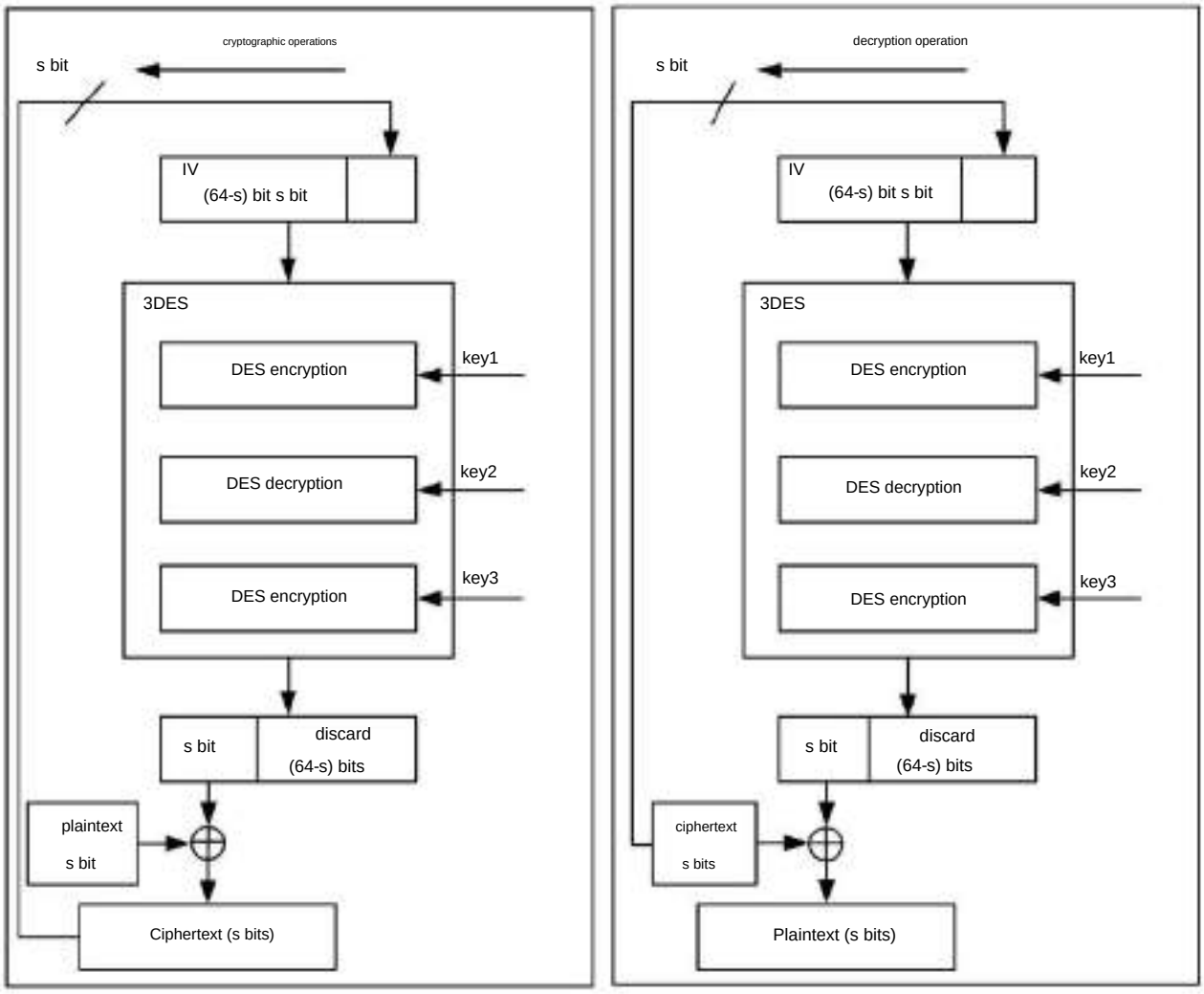


Figure 13-8 s-bit cipher feedback (CFB) mode of 3DES



OFB mode

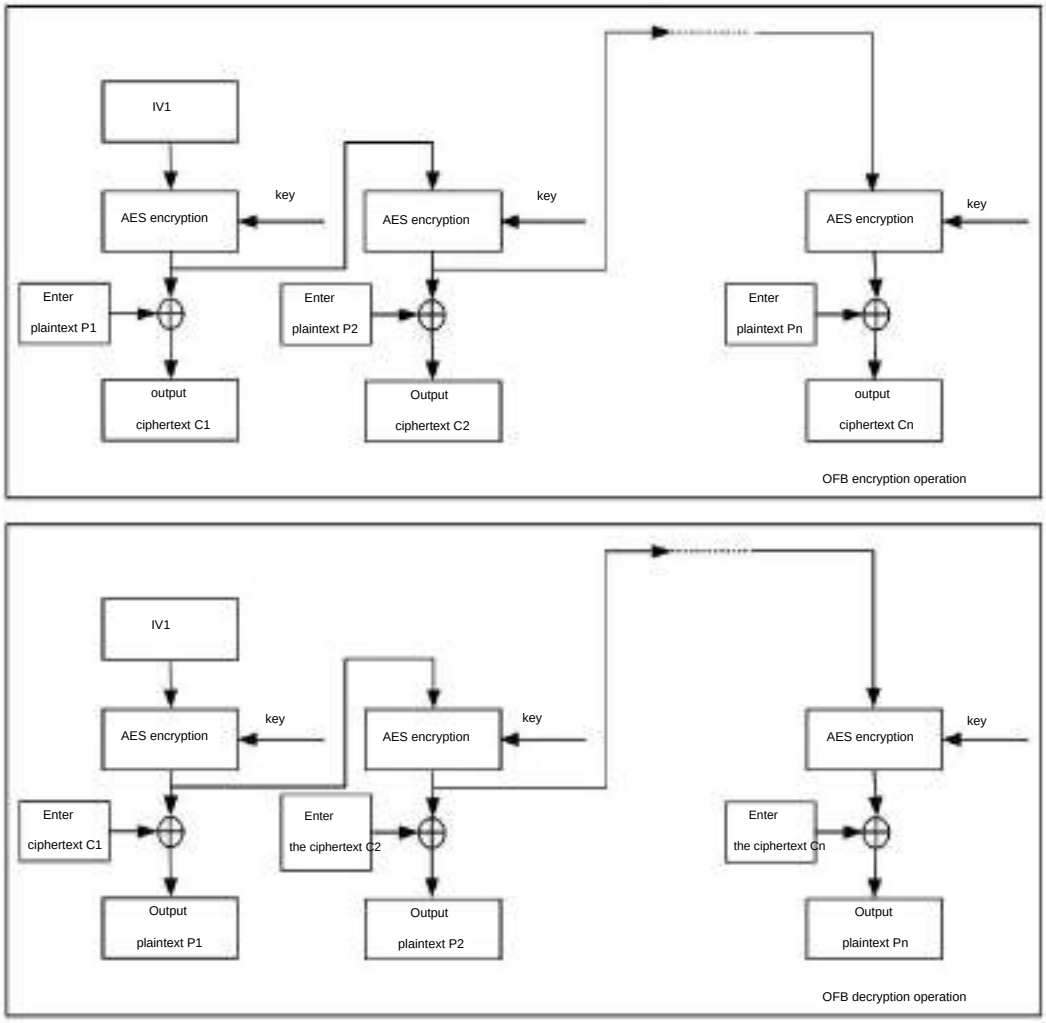
In the OFB (Output FeedBack) mode, the IV is directly used as the input of the encryption operation, so in the case of the same key operation, different IVs should be used to avoid reducing the security of the operation. Regarding the s bit, there are the following 2 situations:

For DES/3DES, s bits can be 1, 8, or 64 bits.

For AES, the s bits can only be 128 bits.

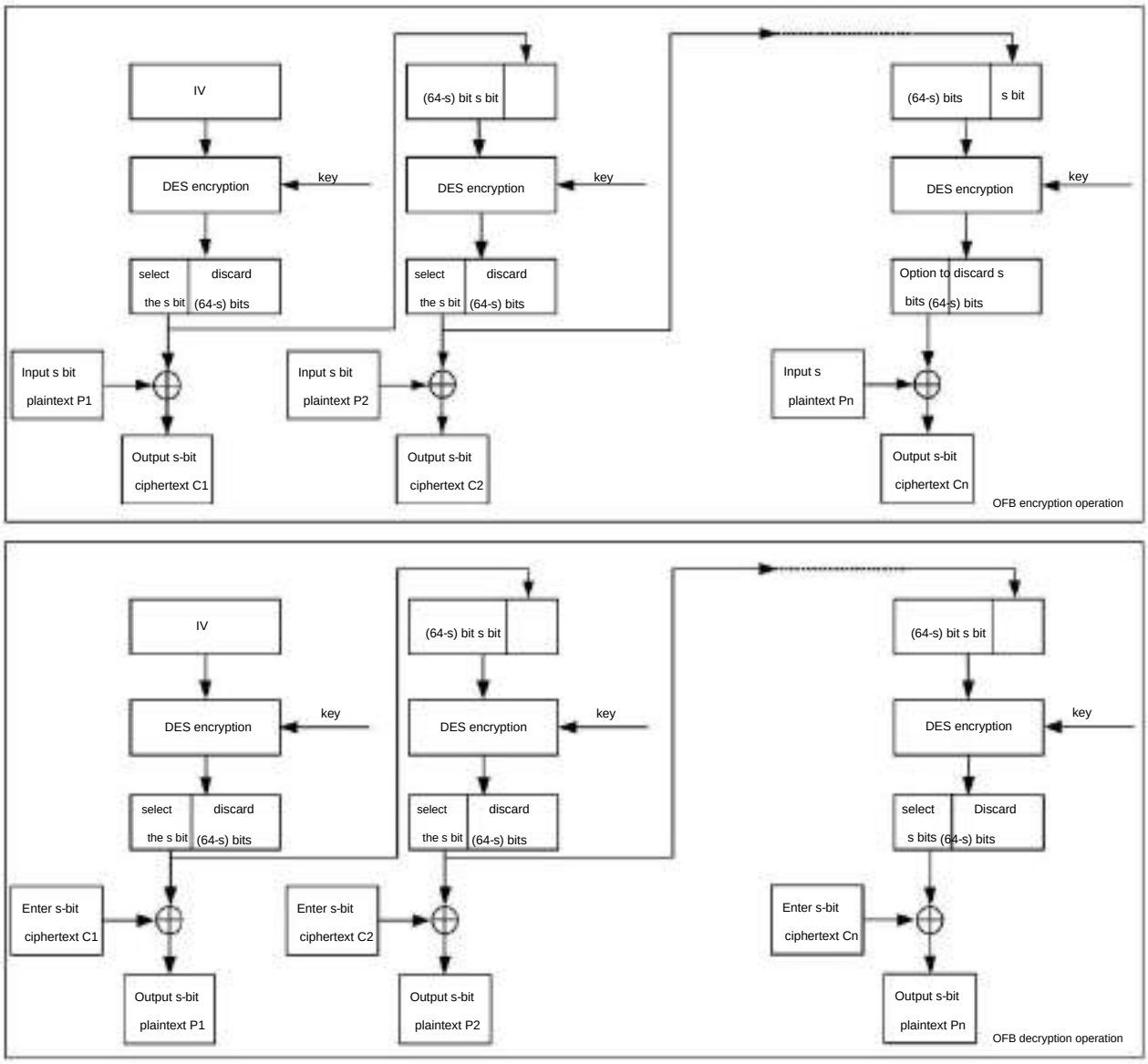
The output feedback (OFB) mode of AES is shown in Figure 13-9 .

Figure 13-9 Output Feedback (OFB) Mode of AES



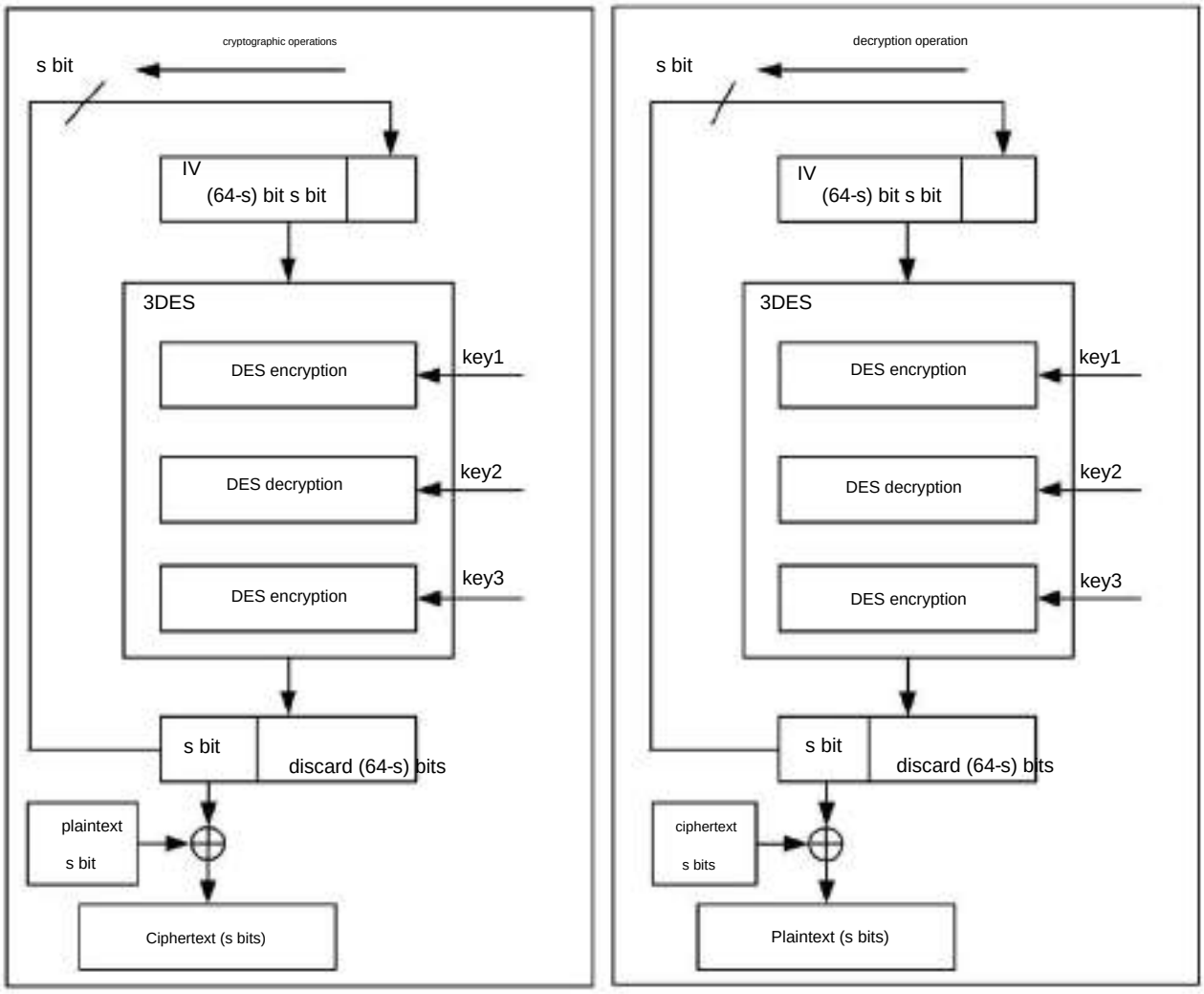
The s-bit output feedback mode of DES is shown in Figure 13-10 .

Figure 13-10 s-bit output feedback (OFB) mode of DES



The s-bit output feedback mode of 3DES is shown in Figure 13-11 .

Figure 13-11 s-bit output feedback (OFB) mode of 3DES



CTR mode

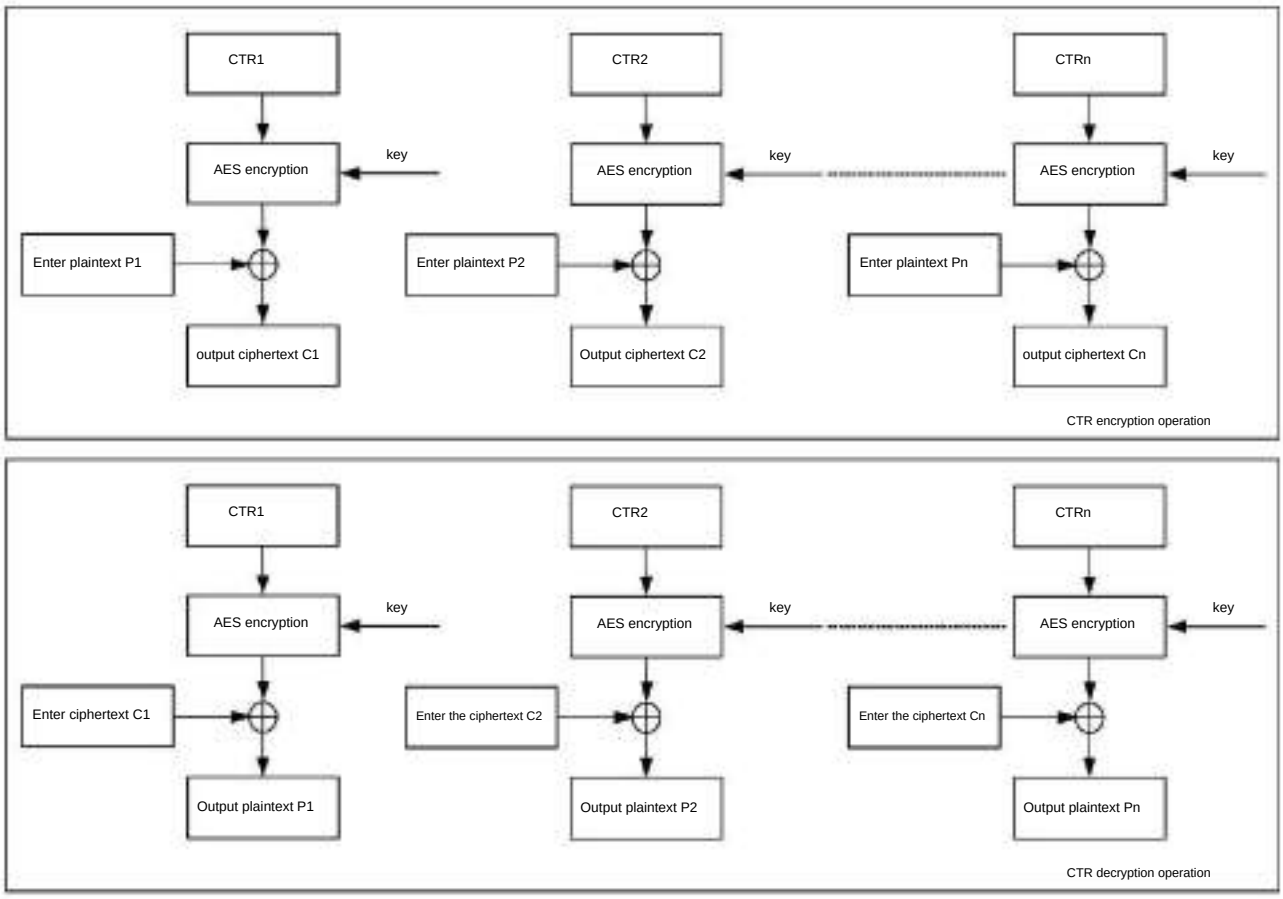
In the CTR (Counter) mode, different data is input to the AES encryption or decryption processing module to ensure the security of data processing, and this data can be a count value. Therefore, the selection of the count value CTRn also determines the security of the application of this method.

说明

CTRn is generally obtained by accumulative counting.

The CTR mode of AES is shown in Figure 13-12 .

Figure 13-12 CTR mode of AES

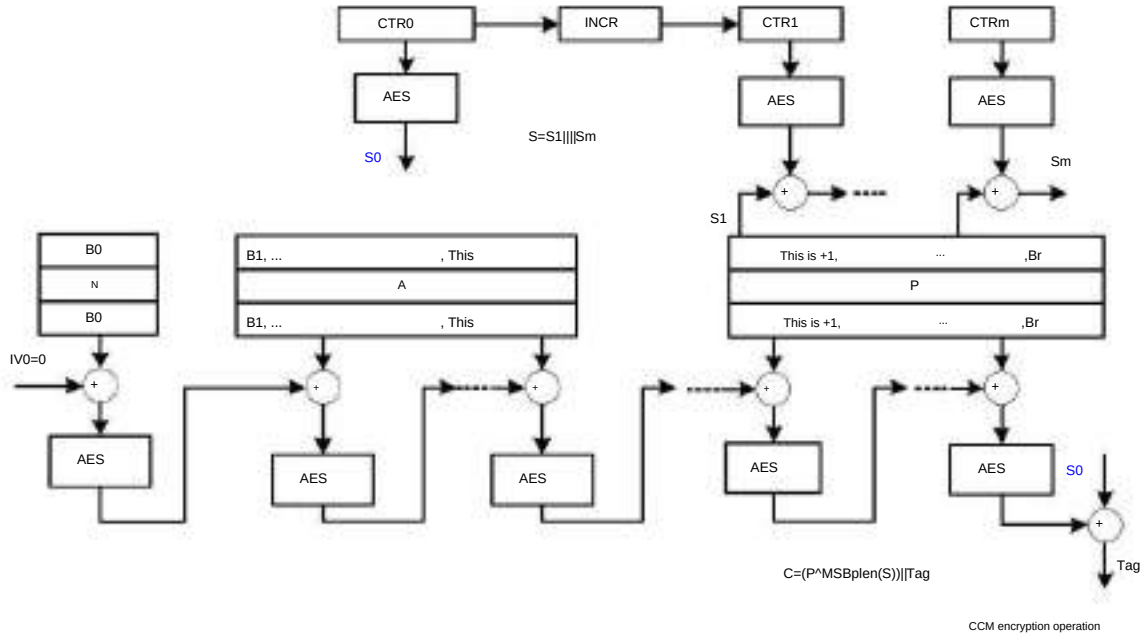


CCM mode

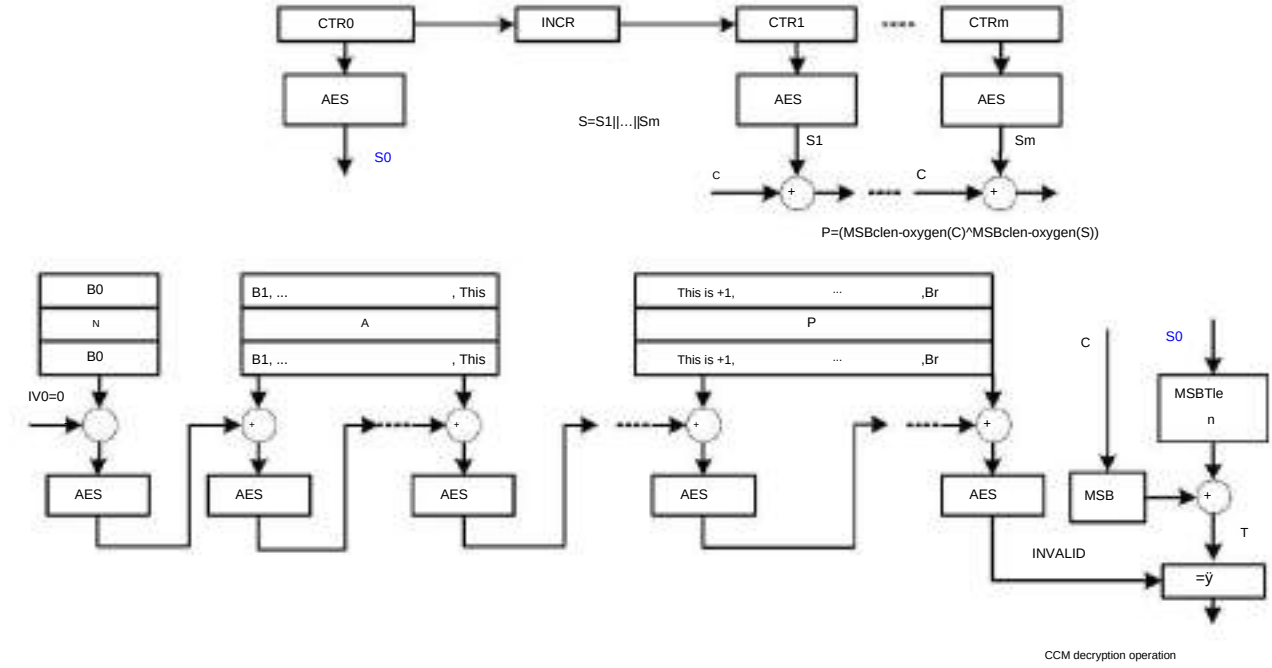
The AES algorithm CCM mode consists of AES CTR and AES CBC modes, which can not only ensure the confidentiality of data, but also ensure the integrity of data.

The CCM mode of AES is shown in Figure 13-13 .

Figure 13-13 CCM mode of AES



CCM encryption operation



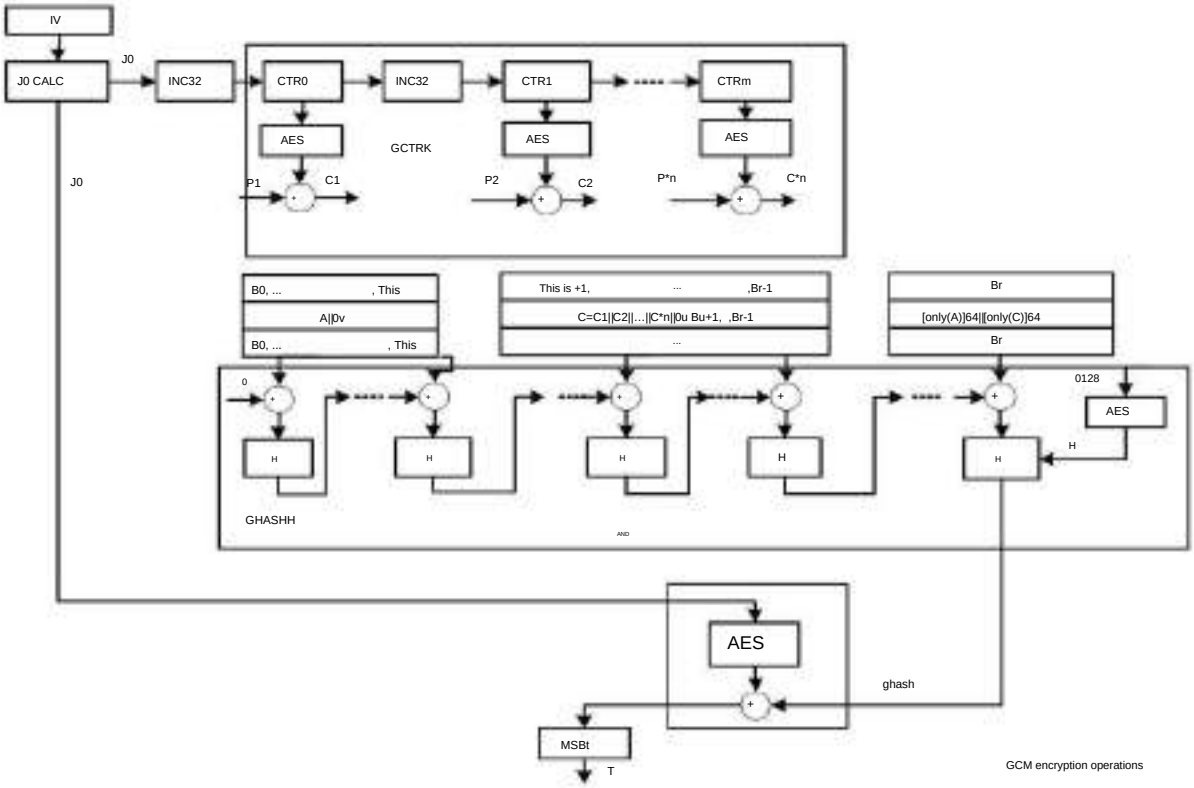
CCM decryption operation

GCM mode

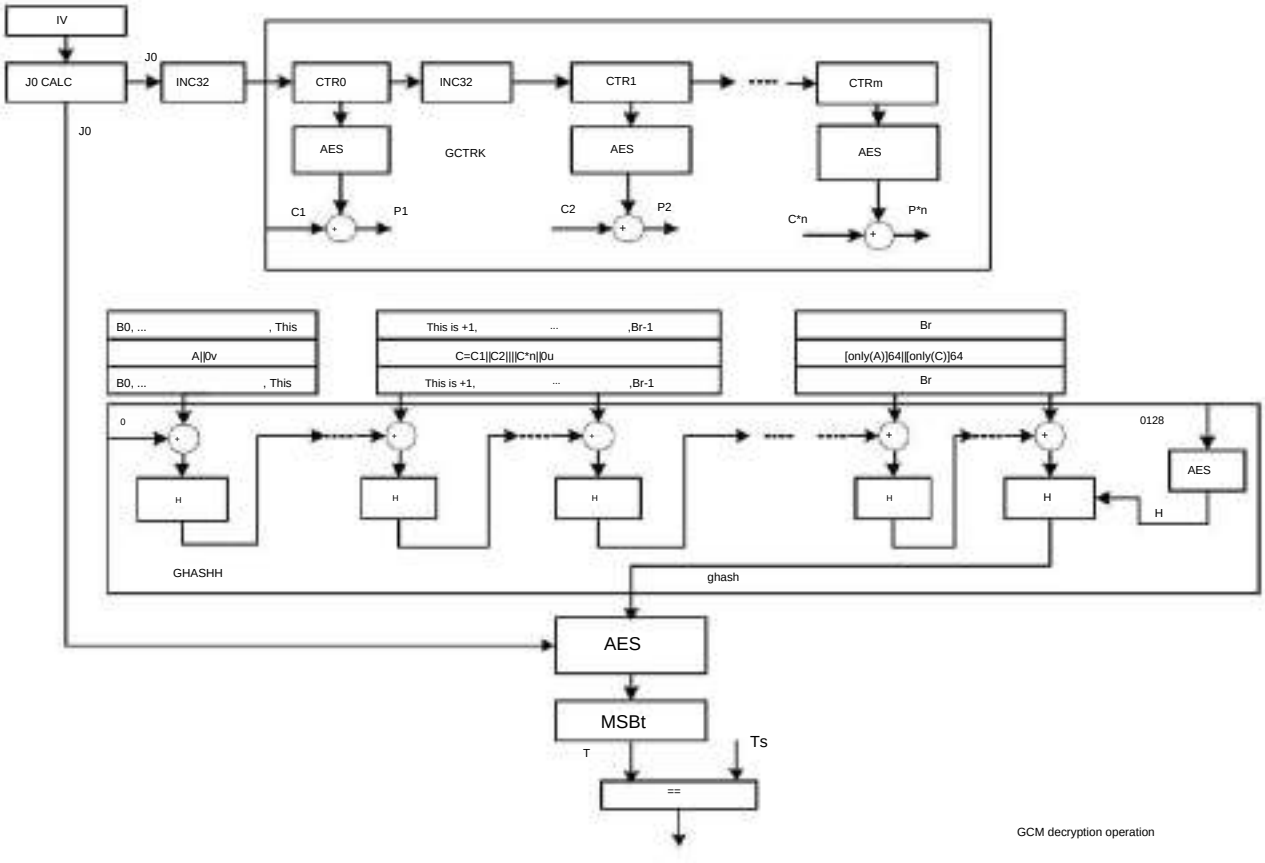
The AES algorithm GCM mode is composed of AES CTR and GHASH, which can not only ensure the confidentiality of data, but also ensure the integrity of data.

The GCM mode of AES is shown in Figure 13-14 .

Figure 13-14 GCM mode of AES



GCM encryption operations



GCM decryption operation

13.1.4 Working method

CIPHER's single group operation process

CIPHER provides channel 0 as a single packet encryption and decryption channel, the operation process is as follows:

Step 1. Query the ch0_busy field of channel 0 configuration register CHAN0_CFG . If channel 0 is not busy, configure the data input of channel 0 and write the relevant configuration information into the register of channel 0.

Step 2. Write the ch0_start field of channel 0 configuration register CHAN0_CFG to start channel 0 encryption and decryption.

----Finish

There are two ways to judge the end of encryption and decryption of channel 0:

Step 1. Query and wait for the channel 0 encryption and decryption to end, ch0_busy becomes not busy or enable the channel 0 interrupt, when the channel 0 data is completed Read data after the interrupt becomes valid.

Step 2. Encryption and decryption of channel 0 is completed, from the CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0 Read the corresponding result in the register.

----Finish

CIPHER's multi-group operation process

The CIPHER module provides 7 multi-packet encryption and decryption channels, and the software can set the weight of each channel according to the rate of each channel. The multi-packet encryption and decryption channel automatically reads data from DDR, and writes data into DDR after completing encryption and decryption.

CIPHER's multi-group operation process is as follows:

Step 1. Channel initialization configuration. That is, the depth of the input queue and the depth of the output queue of each channel, the first place of the input and output queues address, the number of multi-packet interrupts and aging interrupt time, and configure the CTRL register information of each channel.

Step 2. When there is data to be encrypted and decrypted, query the CHANn_IBUF_CNT register. If the value of this register is less than the value of CHANn_IBUF_NUM , configure the head of the data link list to be encrypted and decrypted in the input queue, and enter step 4; otherwise, enter step 3;

Step 3. Open the interrupt corresponding to the input queue channel, and wait for the interrupt to occur. Read the CHANn_IEMPTY_CNT register to represent the number of packets processed by the input queue. The software clears the interrupt by writing the corresponding value to the register, and then can write to the input queue. Add new data.

Step 4. Add the corresponding output buffer list header to the output queue;

Step 5. Open the output queue channel corresponding to the interrupt;

Step 6. When the output queue interrupt occurs, the software takes the output queue data and writes the number of received packets to CHANn_OFULL_CNT to clear the interrupt.

----Finish

The structure of the multi-packet encryption and decryption channel link list header is shown in Figure 13-15 :

Figure 13-15 Multi-packet encryption and decryption channel link list header structure

addr indicates the first address of the Buffer pointed to by the head of the linked list, which can be a byte address.

data_len indicates the length of valid data indicated by the head of the linked list. cas

represents the control information of cipher encryption and decryption, and the specific bit number is shown in Figure 13-16 :

Figure 13-16 Each bit flag of CAS

iv_set: It indicates that the data indicated by the head of the current linked list needs to be replaced with the initial vector. At this time, the initial address of the current IV in the DDR needs to be indicated through iv_start_addr. This address must be a WORD-aligned

address. last_lst: Indicates that the data indicated by the head of the current linked list is the last linked list of a data block. If the logic encounters less than one encrypted and decrypted group of data at the end of the linked list processing, the logic will directly write the remaining data into the output Buffer without Encryption and decryption.

clock gating

When no encryption operation is required and the CIPHER module is in an idle state, the clock of the CIPHER module can be turned off by configuring the registers of the system controller to reduce power consumption.

soft reset

The CIPHER module can be soft reset by configuring the registers of the system controller.

13.1.5 CIPHER Register Overview

An overview of the CIPHER registers is shown in Table 13-1 .

Table 13-1 CIPHER register overview (base address is 0x1008_0000)

offset address name		describe	page number
0x0000ÿ 0x000C	CHAN0_CIPHER_D OUT	CIPHER module channel 0 (single packet encryption and decryption) output register	13-20

offset address name		describe	page number
0x0010ÿ 0x001C	CHAN0_CIPHER_IV OUT	Vector output register after CIPHER operation completes	13-21
0x0020ÿ 0x008C	CHAN_CIPHER_IV OUT	Channel 1~7 vector output register	13-22
0x0090ÿ 0x018C	CIPHER_KEY	CPU configuration key register for CIPHER module	13-22
0x0840	CHAN0_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN0	13-24
0x0844	CHAN0_GCM_A_LE N_1	A high 32bit register of AES GCM of CHAN0	13-24
0x0848	CHAN1_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN1	13-24
0x084C	CHAN1_GCM_A_LE N_1	A high 32bit register of AES GCM of CHAN1	13-25
0x0850	CHAN2_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN2	13-25
0x0854	CHAN2_GCM_A_LE N_1	A high 32bit register of AES GCM of CHAN2	13-26
0x0858	CHAN3_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN3	13-26
0x085C	CHAN3_GCM_A_LE N_1	A high 32bit register of AES GCM of CHAN3	13-26
0x0860	CHAN4_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN4	13-27
0x0864	CHAN4_GCM_A_LE N_1	A high 32bit register of AES GCM of CHAN4	13-27
0x0868	CHAN5_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN5	13-27
0x086C	CHAN5_GCM_A_LE N_1	The high 32bit register of AES GCM of CHAN5	13-28
0x0870	CHAN6_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN6	13-28
0x0874	CHAN6_GCM_A_LE N_1	The high 32bit register of AES GCM of CHAN6	13-29
0x0878	CHAN7_GCM_A_LE N_0	The lower 32bit register of AES GCM of CHAN7	13-29

offset address	name	describe	page number
0x087C	CHAN7_GCM_A_LEN_1	The high 32bit register of AES GCM of CHAN7	13-29
0x0880	CHAN0_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN0	13-30
0x0884	CHAN0_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN0	13-30
0x0888	CHAN1_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN1	13-30
0x088C	CHAN1_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN1	13-31
0x0890	CHAN2_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN2	13-31
0x0894	CHAN2_GCM_PC_LIN_0	The high 32bit register of PayLoad of AES GCM of CHAN2	13-31
0x0898	CHAN3_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN3	13-32
0x089C	CHAN3_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN3	13-32
0x08A0	CHAN4_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN4	13-33
0x08A4	CHAN4_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN4	13-33
0x08A8	CHAN5_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN5	13-33
0x08AC	CHAN5_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN5	13-34
0x08B0	CHAN6_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN6	13-34
0x08B4	CHAN6_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN6	13-35
0x08B8	CHAN7_GCM_PC_LIN_0	The lower 32bit register of PayLoad of AES GCM of CHAN7	13-35
0x08BC	CHAN7_GCM_PC_LIN 1	The high 32bit register of PayLoad of AES GCM of CHAN7	13-35
0x08C0	CHAN0_3_GCM_IV_ONLY	The length of IV of AES GCM of CHAN0~3	13-36

offset address name		describe	page number
0x08C4	CHAN4_7_GCM_IV _ONLY	The length of IV of AES GCM of CHAN4~7	13-36
0x08CC	CHANs_GCM_IV_L EN_VLD	IV length valid signal for GCM	13-37
0x08D0	CHANs_GCM_TAG _VLD	TAG valid signal for GCM	13-37
0x08D4	CHANs_GCM_GHA SH_A_END	GCM's A calculation end signal	13-38
0x0900+0x10 x n+0x00	CHANs_GCM_TAG _0	TAG register 0 of GCM of CHANn	13-38
0x0900+0x10 x n+0x04	CHANs_GCM_TAG _1	TAG register 1 of GCM of CHANn	13-38
0x0900+0x10 x n+0x08	CHANs_GCM_TAG _2	TAG register 2 of GCM of CHANn	13-39
0x0900+0x10 x n+0x0C	CHANs_GCM_TAG _3	TAG register 3 of GCM of CHANn	13-39
0x1000	CHAN0_CIPHER_C TRL	Channel 0 encryption and decryption control register	13-39
0x1004ÿ 0x1010	CHAN0_CIPHER_IV IN	Input register for the vector grouping of channel 0 of the CIPHER module	13-42
0x1014ÿ 0x1020	CHAN0_CIPHER_DI N	128-bit grouped input register for the CIPHER module	13-43
0x1000+ n x 0x80	CHANn_IBUF_NUM	The total depth of the input queue of channel n (n is 1 to 7), that is, the total number of registers that can configure the head of the linked list	13-44
0x1000+ n x 0x80+0x4	CHANn_IBUF_CNT	channel n input queue pending data Buffer number register	13-44
0x1000+ n x 0x80+0x8	CHANn_IEMPTY_C NT	The processed data in the channel n input queue Buffer count register	13-45
0x1000+ n x 0x80+0xC	CHANn_INT_ICNTC FG	Channel n Input Queue Multipacket Interrupt Watermark Register	13-45
0x1000+ n x 0x80+0x10	CHANn_CIPHER_C TRL	Channel n encryption and decryption control register	13-46
0x1000+ n x 0x80+0x14	CHANs_SRC_LST_S ADDR	Channel n Input Queue Start Address Register	13-48
0x1000+ n x 0x80+0x18	CHAN_IAGE_TIM IS	Channel n Input Queue Interrupt Aging Time Configuration Register	13-48
0x1000+ nx	CHANn_OBUF_NU	channel n output queue total depth, which can be configured with	13-49

offset address name		Describe	page number
0x80+0x3C M		the total number of registers at the head of the linked list	
0x1000+ n x 0x80+0x40	CHANn_OBUF_CNT The data to be processed in the output queue of channel n	Buffer number register	13-49
0x1000+ n x 0x80+0x44	CHANs_OFULL_CN T	The processed data in the channel n output queue Buffer count register	13-50
0x1000+ n x 0x80+0x48	CHANn_INT_OCNT CFG	Channel n Output Queue Multipacket Interrupt Watermark Register 13-50	
0x1000+ n x 0x80+0x4C	CHANn_DEST_LST _SADDR	Channel n Output Queue Start Address Register 13-50	
0x1000+ n x 0x80+0x50	CHANn_OAGE_TIM IS	Channel n Output Queue Interrupt Aging Time Configuration Register	13-51
0x1400	INT_STATUS	Interrupt Status Register	13-51
0x1404	INT_EN	interrupt enable register	13-52
0x1408	INT_RAW	Raw Interrupt Status Register	13-53
0x140C	RST_STATUS	Reset Status Indication Register	13-54
0x1410	CHAN0_CFG	Channel 0 Configuration Register	13-55

The value range and meaning of the variables in the offset address of the CIPHER register are shown in Table 13-2 .

Table 13-2 CIPHER register offset address variable table

variable name	Ranges	describe
n	1ÿ7	Channel 1 to Channel 7 of the CIPHER module.

13.1.6 CIPHER register description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is the output register of CIPHER module channel 0 (single packet encryption and decryption).

Note when reading this register:

The data read from this register is the result data of a single group operation. The situation corresponding to AES operation and DES or 3DES operation is different:

If AES operation is selected ÿ If 1-

CFB mode is selected, the lowest bit is valid, that is, CIPHER_DOUT bit[0] is valid data. ÿ If 8-CFB mode is selected, the lower 8 bits are valid, that is, CIPHER_DOUT bit[7:0] is valid data.

ÿIf 128-CFB operation is selected, all 128-bit data are valid.

ÿ128 -bit data is valid in other modes.

If you choose to perform DES or 3DES operation

ÿ If 1-CFB or 1-OFB mode is selected, the lower 1 bit is valid, that is, CIPHER_DOUT bit[0] is valid data.

ÿIf 8-CFB or 8-OFB mode is selected, the lower 8 bits are valid, that is, CIPHER_DOUT bit[7:0] is active valid data.

ÿ If 64-CFB or 64-OFB mode is selected, the lower 64-bit data is valid, that is, CIPHER_DOUT bit[63:0] is valid data. ÿIn

other modes, the lower 64-bit data is valid, that is, CIPHER_DOUT bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x0000ÿ0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_cipher_dout
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	chan0_cipher_dout	The CIPHER module outputs 128-bit groups, and each address corresponds to 32-bit data. CIPHER_DOUT[31:0]: 0x0000 address; CIPHER_DOUT[63:32]: 0x0004 address; CIPHER_DOUT[95:64]: 0x0008 address; CIPHER_DOUT[127:96]: 0x000C address.

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is the vector output register after the CIPHER operation is completed.

Note when reading this register:

If the ECB or CTR mode is implemented, this register does not need to be concerned. If

you choose to process a single packet, the data in this register is the vector result output of this packet, which can be used as the vector input for the next packet operation of the same data packet.

ÿ If AES operation is selected, all 128-bit data is valid.

ÿIf DES or 3DES operation is selected (CIPHER_CTRL[cipher_mode]=0b00, 0b01 or 0b11), the lower 64-bit data is valid, that is, CIPHER_IVOUT bit[63:0] is valid data. If you choose to perform multi-group processing, the data read in this register is the vector result output of the last group operation.

ÿ If AES operation is selected, all 128-bit data is valid.

ÿ If DES or 3DES operation is selected, the lower 64-bit data is valid, that is, CIPHER_IVOUT bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x0010ÿ0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_cipher_ivout
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	chan0_cipher_ivout	The output of the vector IV after the operation of the CIPHER module is completed (no need to pay attention in the ECB and CTR working modes), and each address corresponds to 32 bits of data. CIPHER_IVOUT[31:0]: 0x0010 address; CIPHER_IVOUT[63:32]: 0x0014 address; CIPHER_IVOUT[95:64]: 0x0018 address; CIPHER_IVOUT[127:96]: 0x001C address.

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is the channel 1~7 vector output register.

Offset Address	Register Name	Total Reset Value
0x0020ÿ0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan_cipher_ivout
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	chan_cipher_ivout	0x0020~0x002C: channel 1; 0x0030~0x003C: channel 2; 0x0040~0x004C: channel 3; 0x0050ÿ0x005C: channel 4; 0x0060ÿ0x006C: channel 5; 0x0070~0x007C: channel 6; 0x0080~0x008C: Channel 7.

CIPHER_KEY

CIPHER_KEY is the CPU configuration key register of the CIPHER module, the key is the CPU configuration value, and the CPU can read and write.

Note when configuring this register:

When DES operation is selected, the lower 64-bit data is valid, that is, CIPHER_KEY[63:0] is valid data.

Select 3DES operation:

When selecting 3 key operations (CIPHER_CTRL[key_length]=0b00, 0b01 or 0b10), the lower 192 bits of data are valid, at this time: ÿ

CIPHER_KEYbit [63:0] indicates the first key.

ÿ CIPHER_KEY bit[127:64] indicates the second key.

ÿ CIPHER_KEY bit[191:128] indicates the third key. When two

key operations are selected (ie CIPHER_CTRL[key_length]=0b11), the lower 128 bits of data are valid, at this time: ÿ

CIPHER_KEY bit[63:0] indicates the first key.

ÿ CIPHER_KEY bit[127:64] indicates the second key. When

AES operation is

selected: ÿ If 128-bit key operation is selected, the lower 128-bit data is valid, that is, CIPHER_KEY bit[127:0] is valid data.

ÿ If 192-bit key operation is selected, the lower 192 bits of data are valid, that is, CIPHER_KEY bit[191:0] is valid data.

ÿIf 256-bit key operation is selected, all 256-bit data are valid.

The CIPHER module supports the configuration of 8 keys in total, each channel can be configured to use one of the keys, and multiple channels can share the same key.

Offset Address	Register Name	Total Reset Value
0x0090ÿ0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	For the key input of the CIPHER module, each address corresponds to a 32-bit wide data. CIPHER_KEY[31:0]: 0x0090 address; CIPHER_KEY[63:32]: 0x0094 address; CIPHER_KEY[95:64]: 0x0098 address; CIPHER_KEY[127:96]: 0x009C address; CIPHER_KEY[159:128]: 0x00A0 address; CIPHER_KEY[191:160]: 0x00A4 address; CIPHER_KEY[223:192]: 0x00A8 address; CIPHER_KEY[255:224]: 0x00AC address. 0x0090~0x00AC: host_key0; 0x00B0ÿ0x00CCÿhost_key1ÿ 0x00D0ÿ0x00ECÿhost_key2ÿ

			0x00F0ÿ0x010Cÿhost_key3ÿ 0x0110ÿ0x012Cÿhost_key4ÿ 0x0130ÿ0x014Cÿhost_key5ÿ 0x0150ÿ0x016Cÿhost_key6ÿ 0x0170ÿ0x018Cÿhost_key7ÿ

CHAN0_GCM_A_LEN_0

CHAN0_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN0.

Offset Address	Register Name	Total Reset Value
0x0840	CHAN0_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_	A length of AES GCM of CHAN0, lower 32 bits, unit is 8 bits. 0

CHAN0_GCM_A_LEN_1

CHAN0_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN0.

Offset Address	Register Name	Total Reset Value
0x0844	CHAN0_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_	A length of AES GCM of CHAN0, high 32bit, unit is 8bit. 1

CHAN1_GCM_A_LEN_0

CHAN1_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN1.

Offset Address	Register Name	Total Reset Value
0x0848	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan1_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_	A length of AES GCM of CHAN1, lower 32 bits, unit is 8 bits. 0

CHAN1_GCM_A_LEN_1

CHAN1_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN1.

Offset Address	Register Name	Total Reset Value
0x084C	CHAN1_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan1_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_	A length of AES GCM of CHAN1, high 32bit, unit is 8bit. 1

CHAN2_GCM_A_LEN_0

CHAN2_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN2.

Offset Address	Register Name	Total Reset Value
0x0850	CHAN2_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan2_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_	A length of AES GCM of CHAN2, lower 32 bits, unit is 8 bits. 0

CHAN2_GCM_A_LEN_1

CHAN2_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN2.

Offset Address	Register Name	Total Reset Value
0x0854	CHAN2_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan2_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_	A length of AES GCM of CHAN2, high 32bit, unit is 8bit. 1

CHAN3_GCM_A_LEN_0

CHAN3_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN3.

Offset Address	Register Name	Total Reset Value
0x0858	CHAN3_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan3_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_	A length of AES GCM of CHAN3, lower 32 bits, unit is 8 bits. 0

CHAN3_GCM_A_LEN_1

CHAN3_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN3.

Offset Address	Register Name	Total Reset Value
0x085C	CHAN3_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan3_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_	A length of AES GCM of CHAN3, high 32bit, unit is 8bit. 1

CHAN4_GCM_A_LEN_0

CHAN4_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN4.

Offset Address	Register Name	Total Reset Value
0x0860	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan1_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_	A length of AES GCM of CHAN4, lower 32 bits, unit is 8 bits. 0

CHAN4_GCM_A_LEN_1

CHAN4_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN4.

Offset Address	Register Name	Total Reset Value
0x0864	CHAN4_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan1_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_	A length of AES GCM of CHAN4, high 32bit, unit is 8bit. 1

CHAN5_GCM_A_LEN_0

CHAN5_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN5.

Offset Address	Register Name	Total Reset Value
0x0868	CHAN5_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan5_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_	A length of AES GCM of CHAN5, lower 32 bits, unit is 8 bits. 0

CHAN5_GCM_A_LEN_1

CHAN5_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN5.

Offset Address	Register Name	Total Reset Value
0x086C	CHAN5_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan5_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_	A length of AES GCM of CHAN5, high 32bit, unit is 8bit. 1

CHAN6_GCM_A_LEN_0

CHAN6_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN6.

Offset Address	Register Name	Total Reset Value
0x0870	CHAN6_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan6_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_	A length of AES GCM of CHAN6, lower 32bit, unit is 8bit. 0

CHAN6_GCM_A_LEN_1

CHAN6_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN6.

Offset Address	Register Name	Total Reset Value
0x0874	CHAN6_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan6_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_	A length of AES GCM of CHAN6, high 32bit, unit is 8bit. 1

CHAN7_GCM_A_LEN_0

CHAN7_GCM_A_LEN_0 is the lower 32bit register of A of AES GCM of CHAN7.

Offset Address	Register Name	Total Reset Value
0x0878	CHAN7_GCM_A_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan7_gcm_a_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_	A length of AES GCM of CHAN7, lower 32bit, unit is 8bit. 0

CHAN7_GCM_A_LEN_1

CHAN7_GCM_A_LEN_1 is the high 32bit register of A of AES GCM of CHAN7.

Offset Address	Register Name	Total Reset Value
0x087C	CHAN7_GCM_A_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan7_gcm_a_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_	A length of AES GCM of CHAN7, high 32bit, unit is 8bit. 1

CHAN0_GCM_PC_LEN_0

CHAN0_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN0.

Offset Address	Register Name	Total Reset Value
0x0880	CHAN0_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan0_gcm_pc_len _0	The length of PayLoad of AES GCM of CHAN0, the lower 32 bits, the unit is 8bitÿ

CHAN0_GCM_PC_LEN_1

CHAN0_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN0.

Offset Address	Register Name	Total Reset Value
0x0884	CHAN0_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan0_gcm_pc_len _1	The length of PayLoad of AES GCM of CHAN0, high 32bit, the unit is 8bitÿ

CHAN1_GCM_PC_LEN_0

CHAN1_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN1.

Offset Address	Register Name	Total Reset Value
0x0888	CHAN1_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len _0	The length of PayLoad of AES GCM of CHAN1, the lower 32 bits, the unit is 8bitÿ

CHAN1_GCM_PC_LEN_1

CHAN1_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN1.

Offset Address	Register Name	Total Reset Value
0x088C	CHAN1_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan1_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len _1 8bit.	The length of PayLoad of AES GCM of CHAN1, high 32bit, the unit is

CHAN2_GCM_PC_LEN_0

CHAN2_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN2.

Offset Address	Register Name	Total Reset Value
0x0890	CHAN2_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan2_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_pc_len_0 8bit.	The length of PayLoad of AES GCM of CHAN2, the lower 32bit, the unit is

CHAN2_GCM_PC_LEN_1

CHAN2_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN2.

Offset Address	Register Name	Total Reset Value
0x0894	CHAN2_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan2_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan2_gcm_pc_len _1	The length of PayLoad of AES GCM of CHAN2, high 32bit, the unit is 8bitÿ

CHAN3_GCM_PC_LEN_0

CHAN3_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN3.

Offset Address	Register Name	Total Reset Value
0x0898	CHAN3_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan3_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan3_gcm_pc_len _0	The length of PayLoad of AES GCM of CHAN3, the lower 32 bits, the unit is 8bitÿ

CHAN3_GCM_PC_LEN_1

CHAN3_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN3.

Offset Address	Register Name	Total Reset Value
0x089C	CHAN3_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan3_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan3_gcm_pc_len	The length of PayLoad of AES GCM of CHAN3, high 32bit, unit is _1

			8bitÿ

CHAN4_GCM_PC_LEN_0

CHAN4_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN4.

Offset Address	Register Name	Total Reset Value
0x08A0	CHAN4_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan4_gcm_pc_len_0 8bit.	The length of PayLoad of AES GCM of CHAN4, the lower 32bit, the unit is

CHAN4_GCM_PC_LEN_1

CHAN4_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN4.

Offset Address	Register Name	Total Reset Value
0x08A4	CHAN4_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan4_gcm_pc_len _1	The length of PayLoad of AES GCM of CHAN4, high 32bit, the unit is 8bitÿ

CHAN5_GCM_PC_LEN_0

CHAN5_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN5.

Offset Address	Register Name	Total Reset Value
0x08A8	CHAN5_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len _0	The length of PayLoad of AES GCM of CHAN5, the lower 32 bits, the unit is 8bitÿ

CHAN5_GCM_PC_LEN_1

CHAN5_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN5.

Offset Address	Register Name	Total Reset Value
0x08AC	CHAN5_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len _1 8bit.	The length of PayLoad of AES GCM of CHAN5, high 32bit, the unit is

CHAN6_GCM_PC_LEN_0

CHAN6_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN6.

Offset Address	Register Name	Total Reset Value
0x08B0	CHAN6_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_pc_len_0 8bit.	The length of PayLoad of AES GCM of CHAN6, the lower 32bit, the unit is

CHAN6_GCM_PC_LEN_1

CHAN6_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN6.

Offset Address	Register Name	Total Reset Value
0x08B4	CHAN6_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan6_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan6_gcm_pc_len _1	The length of PayLoad of AES GCM of CHAN6, high 32bit, the unit is 8bitÿ

CHAN7_GCM_PC_LEN_0

CHAN7_GCM_PC_LEN_0 is the lower 32bit register of PayLoad of AES GCM of CHAN7.

Offset Address	Register Name	Total Reset Value
0x08B8	CHAN7_GCM_PC_LEN_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan7_gcm_pc_len_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan7_gcm_pc_len _0	The length of PayLoad of AES GCM of CHAN7, the lower 32 bits, the unit is 8bitÿ

CHAN7_GCM_PC_LEN_1

CHAN7_GCM_PC_LEN_1 is the high 32bit register of PayLoad of AES GCM of CHAN7.

Offset Address	Register Name	Total Reset Value
0x08BC	CHAN7_GCM_PC_LEN_1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan7_gcm_pc_len_1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	RW	chan7_gcm_pc_len	The length of PayLoad of CHAN7's AES GCM, high 32bit, unit is _1

			8bitÿ

CHAN0_3_GCM_IV_LEN

CHAN0_3_GCM_IV_LEN is the IV length register of AES GCM of CHAN0~3.

Offset Address	Register Name	Total Reset Value
0x08C0	CHAN0_3_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	chan3_gcm_iv_len	IV length of CHAN3.
[23:21]	RO	reserved	reserve.
[20:16]	RW	chan2_gcm_iv_len	IV length of CHAN2.
[15:13]	RO	reserved	reserve.
[12:8]	RW	chan1_gcm_iv_len	IV length of CHAN1.
[7:5]	RO	reserved	reserve.
[4:0]	RW	chan0_gcm_iv_len	IV length of CHAN0.

CHAN4_7_GCM_IV_LEN

CHAN4_7_GCM_IV_LEN is the IV length register of AES GCM of CHAN4~7.

Offset Address	Register Name	Total Reset Value
0x08C4	CHAN4_7_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	reserve.
[28:24]	RW	chan7_gcm_iv_len	IV length of CHAN7.
[23:21]	RO	reserved	reserve.

[20:16] RW	chan6_gcm_iv_len	IV length of CHAN6.	
[15:13] RO		reserved	reserve.
[12:8] RW	chan5_gcm_iv_len	IV length of CHAN5.	
[7:5] RO		reserved	reserve.
[4:0] RW	chan4_gcm_iv_len	IV length of CHAN4.	

CHANn_GCM_IV_LEN_VLD

CHANn_GCM_IV_LEN_VLD is the IV length valid signal of GCM.

Offset Address	Register Name	Total Reset Value
0x08CC	CHANn_GCM_IV_LEN_VLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	chann_gcm_iv_len_vld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RO	chann_gcm_iv_len_vld	In AES GCM mode, it indicates whether the nth channel IV is a valid signal after the operation is started. 0: invalid (channel length is 0 or greater than 16Byte); 1: valid.

CHANs_GCM_TAG_VLD

CHANn_GCM_TAG_VLD is the valid TAG signal of GCM.

Offset Address	Register Name	Total Reset Value
0x08D0	CHANs_GCM_TAG_VLD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	cann_gcm_tag_vld
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access	Name	Description
[31:8]	RO	reserved	reserve.
[7:0]	RWC	cann_gcm_tag_vld	In AES GCM mode, it indicates whether the tag of the nth channel is valid or not. 0: invalid;

			1: Valid, write 1 to clear.

CHANs_GCM_GHASH_A_END

CHANn_GCM_GHASH_A_END is the end signal for GCM a calculation.

Offset Address	Register Name	Total Reset Value
0x08D4	CHANs_GCM_GHASH_A_END	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Name	reserved	cann_gcm_ghash_a_end
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits	Access Name		Description
[31:8] RO		reserved	reserve.
[7:0] RWC		chann_gcm_ghash_ a_end 1: end, write 1 to	In AES GCM mode, if the length of A is not 0, it indicates whether the nth channel ghash is the end signal. clear; 0: not end.

CHANs_GCM_TAG_0

CHANn_GCM_TAG_0 is TAG register 0 of CHANn's GCM.

Offset Address	Register Name	Total Reset Value
0x0900+0x10 x n+0x00	CHANs_GCM_TAG_0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	cann_gcm_tag_0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0] RO		chann_gcm_tag_0 CHANn ÿ GCM ÿ TAG[31:0]ÿ	

CHANs_GCM_TAG_1

CHANn_GCM_TAG_1 is TAG register 1 of CHANn's GCM.

Offset Address	Register Name	Total Reset Value
0x0900+0x10 x n+0x04	CHANs_GCM_TAG_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cann_gcm_tag_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_1	CHANn ÿ GCM ÿ TAG[63:32]ÿ

CHANs_GCM_TAG_2

CHANn_GCM_TAG_2 is TAG register 2 of CHANn's GCM.

Offset Address	Register Name	Total Reset Value
0x0900+0x10 x n+0x08	CHANs_GCM_TAG_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cann_gcm_tag_2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_2	CHANn ÿ GCM ÿ TAG[95:64]ÿ

CHANs_GCM_TAG_3

CHANn_GCM_TAG_3 is TAG register 3 of CHANn's GCM.

Offset Address	Register Name	Total Reset Value
0x0900+0x10 x n+0x04	CHANs_GCM_TAG_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cann_gcm_tag_3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_3	CHANn ÿ GCM ÿ TAG[127:96]ÿ

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is the encryption and decryption control register of channel 0, and channel 0 is the single packet encryption and decryption channel.

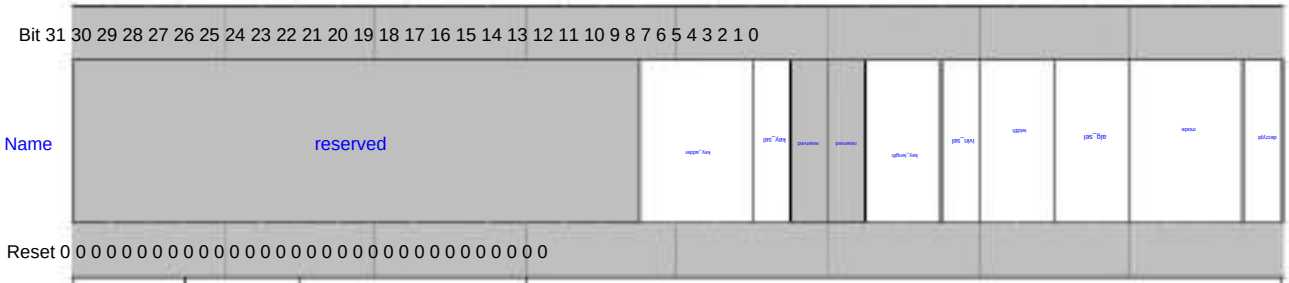
Note when configuring this register:

This register must be configured before configuring other registers of the module.

Except CFB mode under AES, it is not allowed to set CIPHER_CTRL[width] to 01 or 10 in other modes.

In DES/3DES except CFB and OFB modes, other modes do not allow CIPHER_CTRL[width] to be configured as 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000



Bits	Access	Name	Description
[31:17]	RO	reserved	reserve.
[16:14]	RW	key_adder	The sequence number of the Key used by the current channel. 000ÿhost_key0ÿ 001ÿhost_key1ÿ 010ÿhost_key2ÿ 011ÿ host_key3ÿ 100ÿhost_key4ÿ 101ÿhost_key5ÿ 110ÿhost_key6ÿ 111ÿhost_key7ÿ
[13]	RW	key_sel	Select the key currently configured by the CPU or the key generated by the chip key management module. 0: Use the key configured by the CPU; 1: Use the key generated by the chip key management module.
[12]	RO	reserved	reserve.
[11]	RO	reserved	reserve.

[10:9] RW key_length			Key length control. Under the AES algorithm: 00: 128-bit key length; 01: 192-bit key length; 10: 256- bit key length; 11: 128-bit key length. Under the DES algorithm: 00: 3 keys; 01: 3 keys; 10: 3 keys; 11: 2 keys.
[8] RW ivin_sel			Input selection control for CIPHER_IVIN. 0: CIPHER_IVIN does not need to be configured; 1: CIPHER_IVIN needs to be configured.
[7:6] RW width			bit width control. Under DES/3DES algorithm: 00: 64- bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 64-bit mode. Under AES algorithm: 00: 128- bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 128-bit mode.
[5:4] RW alg_sel			Algorithm type selection control. 00: DES operation; 01: 3DES operation; 10: AES operation; 11: DES operation.

[3:1] RW mode			Work mode control. Under the AES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; 100: CTR mode; Others: ECB mode. Under the DES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; others: ECB mode.
[0] RW decrypt			Encryption and decryption control. 0: encryption; 1: Decrypt.

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is the input register for the vector grouping of channel 0 of the CIPHER module.

Note when configuring this register:

If you choose to use channel 0 for single-packet encryption and decryption and the execution is not in ECB mode (CIPHER_CTRL[mode]=0b001, 0b010, 0b011 or 0b100):

If you choose not to configure the input vector (CIPHER_CTRL[ivin_sel]=0b0), you don't need to configure this register. If you choose

to configure the input vector (CIPHER_CTRL[ivin_sel]=0b1), you need to configure this register. If AES operation is selected at this time (ie CIPHER_CTRL [alg_sel]=0b10), CIPHER_IVIN bit[127:0] is valid data; if DES or 3DES operation is selected (CIPHER_CTRL[alg_sel]=0b00, 0b01 or 0b11), the lower 64 Bit data is valid, that is, CIPHER_IVIN bit[63:0] is valid data.

Offset Address	Register Name	Total Reset Value
0x1004ÿ0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_cipher_ivin
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
chan0_cipher_ivin	CIPHER_IVIN	[63:32]: 0x1008 address;	The 128-bit IV vector of the channel 0 CIPHER module or the data input by the Counter, each address corresponds to a 32-bit wide data. CIPHER_IVIN[31:0]: 0x1004 address; [31:0] RW CIPHER_IVIN[95:64]: 0x100C address; CIPHER_IVIN[127:96]: 0x1010 address.

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is the 128-bit group input register of the CIPHER module.

Note when configuring this register:

If channel 0 is selected for single packet processing, this register needs to be configured:

If AES operation is selected (CIPHER_CTRL[alg_sel]=0b10) ÿ If 1-CFB operation is selected, the lower 1 bit is valid, that is, CIPHER_DIN bit[0] is valid data. ÿ If 8-CFB operation is selected, the lower 8 bits are valid, that is, CIPHER_DIN bit[7:0] is valid data. ÿIf 128-CFB operation is selected, all 128-bit data are valid.

ÿIf other operation modes are selected, 128-bit data is valid.

If you choose to perform DES or 3DES operation (CIPHER_CTRL[alg_sel]=0b00, 0b01 or 0b11)

ÿ If 1-CFB/1-OFB operation is selected, the lower 1 bit is valid, that is, CIPHER_DIN bit[0] is a valid number according to.

ÿIf 8-CFB/8-OFB operation is selected, the lower 8 bits are valid, that is, CIPHER_DIN bit[7:0] is a valid number according to.

ÿ If 64-CFB/64-OFB operation is selected, the lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid data.

ÿ If other operation modes are selected, the lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is the valid number according to.

Offset Address	Register Name	Total Reset Value
0x1014ÿ0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	chan0_cipher_din
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit group input of channel 0CIPHER module, each address corresponds to a 32-bit wide data. CIPHER_DIN[31:0]: 0x1014 address; CIPHER_DIN[63:32]: 0x1018 address; CIPHER_DIN[95:64]: 0x101c address; CIPHER_DIN[127:96]: 0x1020 address.

CHANn_IBUF_NUM

CHANn_IBUF_NUM is CHANn_IBUF_BUN is channel n (n is 1~7) input queue total depth, which is the total number of configurable linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80	CHANn_IBUF_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved ibuf_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	ibuf_num	Enter the queue depth, that is, the total number of linked list header information that can be configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is the number of data buffers to be processed in the input queue of channel n. When the software writes this register, the logic will add the value newly written by the software to the original value of the register; after the logic processes a Buffer block, the value of this register will be reduced by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ibuf_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	ibuf_cnt	Enter the number of data buffers to be processed in the queue.

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is the number of processed data buffers in the channel n input queue. When the software writes this register, the logic will subtract the value newly written by the software from the original value of the register. After the logic processes a Buffer block, the register The value will be incremented by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iempty_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	iempty_cnt	Input the number of processed Buffers in the queue.

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is the channel n input queue multi-packet interrupt watermark. When the number of input queue buffers completed by logic processing is greater than or equal to this value, the input queue interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	int_icnt_cfg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.

[15:0] RW	int_icnt_cfg	Input queue multi-packet interrupt threshold.	

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is the encryption and decryption control register for channel n.

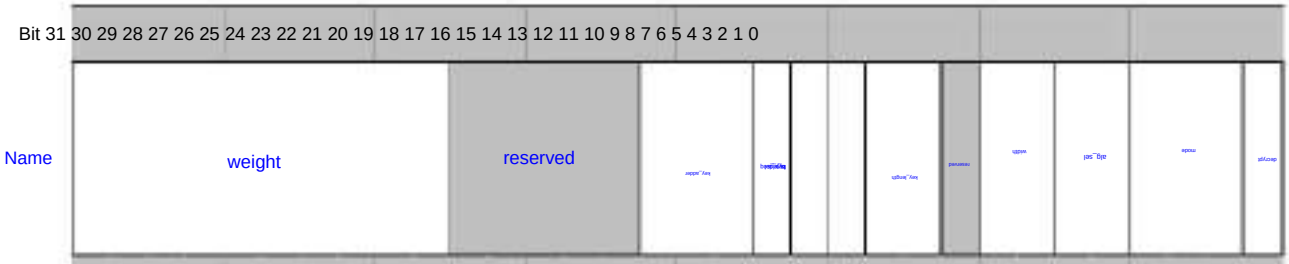
Note when configuring this register:

Before starting the encryption and decryption processing of this channel, this register must be configured first.

Except CFB mode under AES, it is not allowed to set CIPHER_CTRL[width] to 01 or 10 in other modes.

In DES/3DES except CFB and OFB modes, other modes do not allow CIPHER_CTRL[width] to be configured as 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x10	CHANn_CIPHER_CTRL	0x0000_0000



Bits	Access Name		Description
[31:22]	RO	weight	The weight of the current channel, the unit is 64bytes.
[21:17]	RO	reserved	reserve.
[16:14]	RW key_adder		The serial number of the Key used by the current channel can be configured to select a Key from addresses 0 to 7.
[13]	RW key_sel		Select the key currently configured by the CPU or the key generated by the chip key management module. 0: Use the key configured by the CPU; 1: Use the key generated by the chip key management module.
[12:11]	RO	reserved	reserve.

[10:9]	RW	key_length	Key length control. Under the AES algorithm: 00: 128-bit key length; 01: 192-bit key length; 10: 256-bit key length; 11: 128-bit key length. Under the DES algorithm: 00: 3 keys; 01: 2 keys; 10: 3 keys; 11: 2 keys.
[8]	RO	reserved	reserve.
[7:6]	RW	width	bit width control. Under DES/3DES algorithm: 00: 64-bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 64-bit mode. Under the AES algorithm: 00: 128-bit mode; 01: 8-bit mode; 10: 1-bit mode; 11: 128-bit mode.
[5:4]	RW	alg_sel	Algorithm type selection control. 00: DES operation; 01: 3DES operation; 10: AES operation; 11: DES operation.

[3:1] RW mode			Work mode control. Under the AES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; 100: CTR mode; Others: ECB mode. Under the DES algorithm: 000: ECB mode; 001: CBC mode; 010: CFB mode; 011: OFB mode; others: ECB mode.
[0] RW decrypt			Encryption and decryption control. 0: encryption; 1: Decrypt.

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is the starting address of the channel n input queue, which must be a WORD-aligned address.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	The start address of the input queue.

CHAN_IAGE_TIMER

CHANn_IAGE_TIMER is configured for the aging time of the input queue interrupt of channel n. If the aging time counter overflows and the number of Buffers processed by the input queue is greater than 0, the input queue processing completion interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x18	CHAN_IAGE_TIMER	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	iage_hours
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	iage_timer	Aging interrupt timer.

CHANs_OBUF_NUM

CHANn_OBUF_NUM is the total depth of the channel n output queue, that is, the total number of configurable linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x3C	CHANs_OBUF_NUM	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	obuf_num
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	obuf_num	Total output queue depth.

CHANn_OBUF_CNT

CHANn_OBUF_CNT is the number of data buffers to be processed in the output queue of channel n. When the software writes this register, the logic will add the value newly written by the software to the original value of the register; after the logic processes a Buffer block, the value of this register will be reduced by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	obuf_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.

[15:0] RW	obuf_cnt		The number of data buffers to be processed in the output queue.

CHANn_OFULL_CNT

CHANn_OFULL_CNT is the number of processed data buffers in the channel n output queue. When the software writes this register, the logic will subtract the value newly written by the software from the original value of the register. After the logic processes a Buffer block, the register The value will be incremented by 1.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	ofull_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	ofull_cnt	The number of Buffers processed in the output queue.

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is the multi-packet interrupt watermark of the output queue of channel n. When the number of output queue buffers completed by logic processing is greater than or equal to this value, the output queue interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	int_ocnt_cfg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold.

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is the starting address of the channel n output queue, which must be a WORD-aligned address.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dest_lst_saddr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	The starting address of the output queue.

CHAN_OAGE_TIMER

CHANn_OAGE_TIMER is configured for the aging time of the output queue interrupt of channel n. If the aging time counter overflows and the number of Buffers processed by the output queue is greater than 0, an output queue processing interrupt will be reported.

Offset Address	Register Name	Total Reset Value
0x1000+ n x 0x80+0x50	CHAN_OAGE_TIMER	0x0000_0000

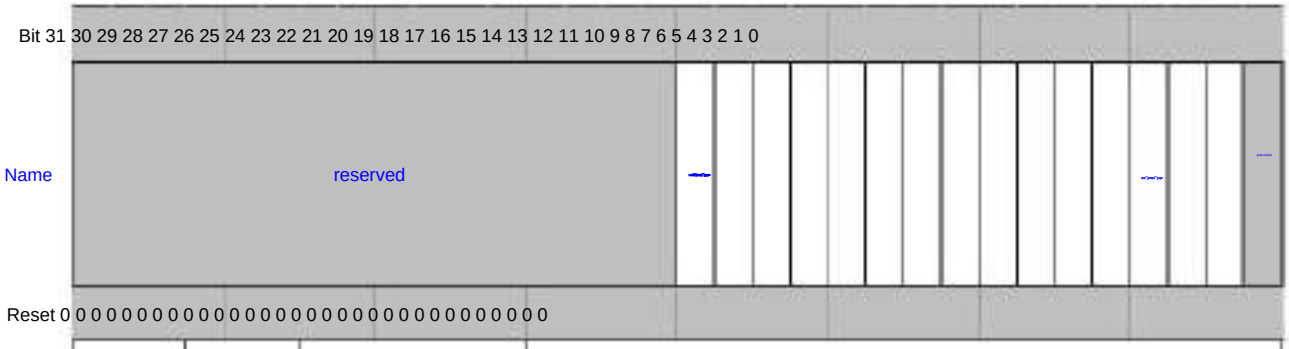
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved	oage_hours
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15:0]	RW	oage_timer	Aging interrupt timer.

INT_STATUS

INT_STATUS is the interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000



Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15]	RO	ch7_ibuf_int	Channel 7 input queue data interrupt.
[14]	RO	ch6_ibuf_int	Channel 6 input queue data interrupt.
[13]	RO	ch5_ibuf_int	Channel 5 input queue data interrupt.
[12]	RO	ch4_ibuf_int	Channel 4 input queue data interrupt.
[11]	RO	ch3_ibuf_int	Channel 3 input queue data interrupt.
[10]	RO	ch2_ibuf_int	Channel 2 input queue data interrupt.
[9]	RO	ch1_ibuf_int	Channel 1 input queue data interrupt.
[8]	RO	ch0_ibuf_int	Channel 0 data transaction complete interrupt.
[7]	RO	ch7_obuf_int	Channel 7 output queue data interrupt.
[6]	RO	ch6_obuf_int	Channel 6 output queue data interrupt.
[5]	RO	ch5_obuf_int	Channel 5 output queue data interrupt.
[4]	RO	ch4_obuf_int	Channel 4 output queue data interrupt.
[3]	RO	ch3_obuf_int	Channel 3 output queue data interrupt.
[2]	RO	ch2_obuf_int	Channel 2 output queue data interrupt.
[1]	RO	ch1_obuf_int	Channel 1 output queue data interrupt.
[0]	RO	reserved	reserve.

INT_EN

INT_EN is the interrupt enable register.

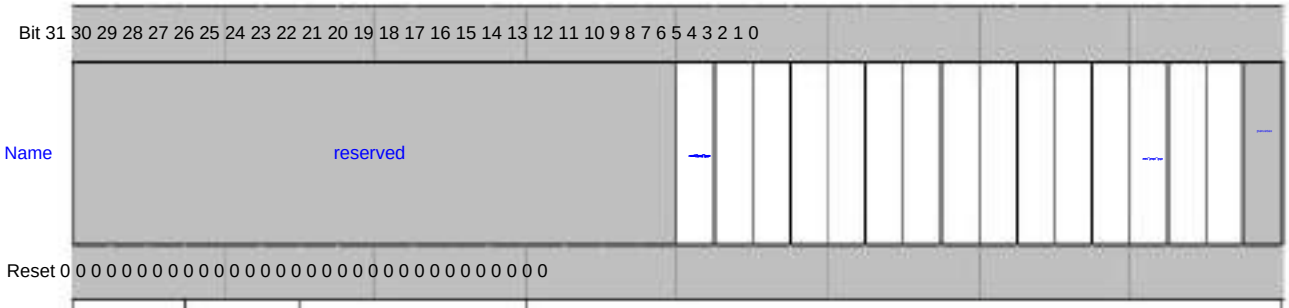
Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bits	Access	Name	Description
[31]	RW	int_en	Global interrupt enable for the Cipher module.
[30:16]	RO	reserved	reserve.
[15]	RW	ch7_ibuf_en	Channel 7 input queue data interrupt enable.
[14]	RW	ch6_ibuf_en	Channel 6 input queue data interrupt enable.
[13]	RW	ch5_ibuf_en	Channel 5 input queue data interrupt enable.
[12]	RW	ch4_ibuf_en	Channel 4 input queue data interrupt enable.
[11]	RW	ch3_ibuf_en	Channel 3 input queue data interrupt enable.
[10]	RW	ch2_ibuf_en	Channel 2 input queue data interrupt enable.
[9]	RW	ch1_ibuf_en	Channel 1 input queue data interrupt enable.
[8]	RW	ch0_ibuf_en	Channel 0 data processing complete interrupt enable.
[7]	RW	ch7_obuf_en	Channel 7 output queue data interrupt enable.
[6]	RW	ch6_obuf_en	Channel 6 output queue data interrupt enable.
[5]	RW	ch5_obuf_en	Channel 5 output queue data interrupt enable.
[4]	RW	ch4_obuf_en	Channel 4 output queue data interrupt enable.
[3]	RW	ch3_obuf_en	Channel 3 output queue data interrupt enable.
[2]	RW	ch2_obuf_en	Channel 2 output queue data interrupt enable.
[1]	RW	ch1_obuf_en	Channel 1 output queue data interrupt enable.
[0]	RO	reserved	reserve.

INT_RAW

INT_RAW is the raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000



Bits	Access	Name	Description
[31:16]	RO	reserved	reserve.
[15]	RWC	ch7_obuf_raw	Channel 7 output queue data raw interrupt.
[14]	RWC	ch6_obuf_raw	Channel 6 output queue data raw interrupt.
[13]	RWC	ch5_obuf_raw	Channel 5 output queue data raw interrupt.
[12]	RWC	ch4_obuf_raw	Channel 4 output queue data raw interrupt.
[11]	RWC	ch3_obuf_raw	Channel 3 output queue data raw interrupt.
[10]	RWC	ch2_obuf_raw	Channel 2 output queue data raw interrupt.
[9]	RWC	ch1_obuf_raw	Channel 1 output queue data raw interrupt.
[8]	RWC	ch0_ibuf_raw	Channel 0 data processing complete raw interrupt.
[7]	RWC	ch7_ibuf_raw	Channel 7 input queue data raw interrupt.
[6]	RWC	ch6_ibuf_raw	Channel 6 input queue data raw interrupt.
[5]	RWC	ch5_ibuf_raw	Channel 5 input queue data raw interrupt.
[4]	RWC	ch4_ibuf_raw	Channel 4 input queue data raw interrupt.
[3]	RWC	ch3_ibuf_raw	Channel 3 input queue data raw interrupt.
[2]	RWC	ch2_ibuf_raw	Channel 2 input queue data raw interrupt.
[1]	RWC	ch1_ibuf_raw	Channel 1 input queue data raw interrupt.
[0]	RO	reserved	reserve.

RST_STATUS

Module reset status indication signal.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	rst_status	CIPHER module reset status indication signal. 0: CIPHER is currently in reset state; 1: CIPHER is currently working normally.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	ch0_busy	Channel 0 status signal.
[0]	RW	ch0_start	Channel 0 encryption and decryption start signal.

13.2 HASH

13.2.1 Overview

HASH is a module that implements the SHA1/SHA256/HMAC_SHA1/HMAC_SHA256 algorithm.

The implementation of the SHA1/SHA256 algorithm conforms to the FIPS180-2 standard. The implementation of the HMAC_SHA1/HMAC_SHA256 algorithm conforms to the RFC2104 standard.

The HASH module is suitable for data integrity authentication and building digital signatures.

13.2.2 Features

The HASH module has the following characteristics:

Support algorithms SHA1, SHA256, HMAC-SHA1, HMAC-SHA256. Support CPU configuration input data

and DMA mode to read input data. The total length of the input data (after software

padding) must be aligned according to the block, that is, a multiple of 64Byte, configured by software, and the maximum supported length is 264-64Byte. For SHA1 and SHA256, the configured data length is the message length after padding (filling needs to be completed by software); for HMAC-SHA1 and HMAC-SHA256, the configured data length is the message length after padding + 64Byte.

The HMAC key supports hardware (Cipher Hash Key Ctrl) configuration or software configuration, and the HMAC key length supports configuration of 128 bits.

SHA1 and SHA256 support configurable initial values.

13.2.3 Functional Description

The HASH module is mainly used for data integrity authentication and building digital signatures. The software can be configured as the initial value update mode (the initial value update mode needs to configure the initial value) or non-initial value update mode, and then start the SHA1 or SHA256 algorithm to calculate the message digest; the software can start the HMAC_SHA1 or HMAC_SHA256 algorithm to calculate the MAC, and does not support the initial value configuration .

13.2.4 Working method

CPU mode SHA1 operation flow

CPU configuration input data, the operation process is as follows:

Step 1. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 2. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 3. Configure HASH_CTRL.read_ctrl=1, HASH_CTRL.sha_sel=0, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0, HASH_CTRL.small_end_en=0, HASH_CTRL.sha_init_update_en=0 (if you need to update the initial value, then configure it to 1);

Step 4. Configure SHA_START.sha_start;

Step 5. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 6. CPU configuration DATA_IN.data_in;

Step 7. Repeat steps 5 and 6 until all the data that needs to be calculated are input;

Step 8. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~5.sha_out1~5; otherwise wait.

----Finish

DMA mode SHA1 operation flow

DMA reads input data, the operation flow is as follows:

Step 1. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 2. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 3. Configure HASH_CTRL.read_ctrl=0, HASH_CTRL.sha_sel=0, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0, HASH_CTRL.small_end_en=0, HASH_CTRL.sha_init_update_en=0 (if you need to update the initial value, then configure it to 1);

Step 4. Configure SHA_START.sha_start;

Step 5. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 6. CPU configuration DMA_START_ADDR.dma_start_addr;

Step 7. CPU configuration DMA_LEN.dma_len;

Step 8. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~5.sha_out1~5; otherwise wait.

----Finish

CPU mode SHA256 operation flow

CPU configuration input data, the operation process is as follows:

Step 1. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 2. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 3. Configure HASH_CTRL.read_ctrl=1, HASH_CTRL.sha_sel=1, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0, HASH_CTRL.small_end_en=0, HASH_CTRL.sha_init_update_en=0 (if you need to update the initial value, then configure it to 1);

Step 4. Configure SHA_START.sha_start;

Step 5. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 6. CPU configuration DATA_IN.data_in;

Step 7. Repeat steps 5 and 6 until all the data that needs to be calculated are input;

Step 8. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~8.sha_out1~8; otherwise wait.

----Finish

DMA mode SHA256 operation flow

DMA reads input data, the operation flow is as follows:

Step 9. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 10. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 11. Configure HASH_CTRL.read_ctrl=0, HASH_CTRL.sha_sel=1, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0, HASH_CTRL.small_end_en=0, HASH_CTRL.sha_init_update_en=0 (if you need to update the initial value, then configure it to 1);

Step 12. Configure SHA_START.sha_start;

Step 13. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 14. CPU configuration DMA_START_ADDR.dma_start_addr;

Step 15. CPU configures DMA_LEN.dma_len;

Step 16. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~8.sha_out1~8; otherwise wait.

----Finish

CPU mode HMAC_SHA1 operation flow

CPU configuration input data, the operation process is as follows:

Step 17. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 18. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 19. Configure HASH_CTRL.read_ctrl=1, HASH_CTRL.sha_sel=0, HASH_CTRL.hmac_flag=1, HASH_CTRL.hardkey_sel=1 (Cipher Hash Key Ctrl needs to configure key first, if it is 0, then you need CPU ÿÿÿ MCU_KEY0~3.mcu_key0~3)ÿHASH_CTRL.small_end_en=0ÿ HASH_CTRL.sha_init_update_en=0ÿ

Step 20. Configure SHA_START.sha_start;

Step 21. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 22. CPU configuration DATA_IN.data_in;

Step 23. Repeat step 5 and step 6 until all the data to be calculated are input;

Step 24. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~5.sha_out1~5; otherwise wait.

----Finish

DMA mode HMAC_SHA1 operation flow

DMA reads input data, the operation flow is as follows:

Step 25. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 26. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 27. Configure HASH_CTRL.read_ctrl=0, HASH_CTRL.sha_sel=0, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0 (Cipher Hash Key Ctrl needs to configure key first, if it is 0, then you need CPU ÿÿÿ MCU_KEY0~3.mcu_key0~3)ÿHASH_CTRL.small_end_en=0ÿ HASH_CTRL.sha_init_update_en=0ÿ

Step 28. Configure SHA_START.sha_start;

Step 29. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 30. CPU configuration DMA_START_ADDR.dma_start_addr;

Step 31. CPU configuration DMA_LEN.dma_len;

Step 32. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~5.sha_out1~5; otherwise wait.

----Finish

CPU mode HMAC_SHA256 operation flow

CPU configuration input data, the operation process is as follows:

Step 33. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 34. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 35. Configure HASH_CTRL.read_ctrl=1, HASH_CTRL.sha_sel=1, HASH_CTRL.hmac_flag=1, HASH_CTRL.hardkey_sel=1 (Cipher Hash Key Ctrl needs to configure key first, if it is 0, then you need CPU pre-allocation MCU_KEY0~3.mcu_key0~3), SHA_CTRL.small_end_en=0, HASH_CTRL.sha_init_update_en=0ÿ

Step 36. Configure SHA_START.sha_start;

Step 37. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 38. CPU configuration DATA_IN.data_in;

Step 39. Repeat step 5 and step 6 until all the data to be calculated are input;

Step 40. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~8.sha_out1~8; otherwise wait.

----Finish

DMA mode HMAC_SHA256 operation flow

DMA reads input data, the operation flow is as follows:

Step 1. First judge whether HASH_STATUS.hash_rdy is 1, if it is 1, it means that it is not currently calculated; if it is 0, then wait;

Step 2. Configure TOTAL_LEN1.total_len1 and TOTAL_LEN2.total_len2, the configured message length is 64Byte together;

Step 3. Configure HASH_CTRL.read_ctrl=0, HASH_CTRL.sha_sel=1, HASH_CTRL.hmac_flag=0, HASH_CTRL.hardkey_sel=0 (Cipher Hash Key Ctrl needs to configure key first, if it is 0, then you need CPU ÿÿÿ MCU_KEY0~3.mcu_key0~3)ÿHASH_CTRL.small_end_en=0ÿ HASH_CTRL.sha_init_update_en = 0ÿ

Step 4. Configure SHA_START.sha_start;

Step 5. Determine that HASH_STATUS.rec_rdy is 1, if it is 1, continue to execute; if it is 0, wait;

Step 6. CPU configuration DMA_START_ADDR.dma_start_addr;

Step 7. CPU configuration DMA_LEN.dma_len;

Step 8. Determine whether HASH_STATUS.hash_rdy is 1, if it is 1, then read the calculation result SHA_OUT1~8.sha_out1~8; otherwise wait.

----Finish

clock gating

When HASH calculation is not needed, the HASH module clock can be turned off to reduce power consumption by configuring the registers of the system controller.

soft reset

The HASH module can be soft reset by configuring the registers of the system controller.

13.2.5 HASH register overview

An overview of the HASH registers is shown in Table 13-3 .

Table 13-3 HASH register overview (base address is 0x1009_0000)

offset address	name	describe	page number
0x0	TOTAL_LEN1	Hash message total length lower 32bit register	13-62
0x4	TOTAL_LEN2	The total length of the hash message is 32bit higher Register	13-62

offset address	name	describe	page number
0x8	HASH_STATUS	HASH status register	13-63
0xC	HASH_CTRL	HASH control register	13-64
0x10	SHA_START	Start SHA calculation register	13-65
0x14	DMA_START_ADDR	read the starting address of the message	13-65
0x18	DMA_LEN	DMA Transfer Length Register	13-65
0x1C	DATA_IN	SHA calculation input data register	13-66
0x20	REC_LEN1	Receive message length register 1	13-66
0x24	REC_LEN2	Receive message length register 2	13-67
0x30	SHA_OUT1	SHA output result register 1	13-67
0x34	SHA_OUT2	SHA output result register 2	13-67
0x38	SHA_OUT3	SHA output result register 3	13-68
0x3C	SHA_OUT4	SHA output result register 4	13-68
0x40	SHA_OUT5	SHA output result register 5	13-69
0x44	SHA_OUT6	SHA output result register 6	13-69
0x48	SHA_OUT7	SHA output result register 7	13-69
0x4C	SHA_OUT8	SHA output result register 8	13-70
0x70	MCU_KEY0	hmac input key 0~31bit (cpu configuration) register	13-70
0x74	MCU_KEY1	hmac input key 32~63bit (cpu configuration) register	13-71
0x78	MCU_KEY2	hmac input key 64~95bit (cpu configuration) register	13-71
0x7C	MCU_KEY3	hmac input key 96~127bit (cpu configuration) register	13-71
0x90	SHA_INIT1_UPDATE	SHA initial value register 1	13-72
0x94	SHA_INIT2_UPDATE	SHA initial value register 2	13-72
0x98	SHA_INIT3_UPDATE	SHA initial value register 3	13-73
0x9C	SHA_INIT4_UPDATE	SHA initial value register 4	13-73
0xA0	SHA_INIT5_UPDATE	SHA initial value register 5	13-73
0xA4	SHA_INIT6_UPDATE	SHA initial value register 6	13-74

offset address	name	describe	page number
0xA8	SHA_INIT7_UPDATE	SHA initial value register 7	13-74
0xAC	SHA_INIT8_UPDATE	SHA initial value register 8	13-74

13.2.6 HASH register description

TOTAL_LEN1

TOTAL_LEN1 is the lower 32bit register of the total length of the hash message.

Offset Address	Register Name	Total Reset Value
0x0	TOTAL_LEN1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	total_len1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	total_len1	SHA: the low bit of the Byte length of the padded message; HMAC: the low bit of the Byte length of the entire i_key_pad + padded message.

TOTAL_LEN2

TOTAL_LEN2 is the high 32bit register of the total length of the hash message.

Offset Address	Register Name	Total Reset Value
0x4	TOTAL_LEN2	0x0000_0000

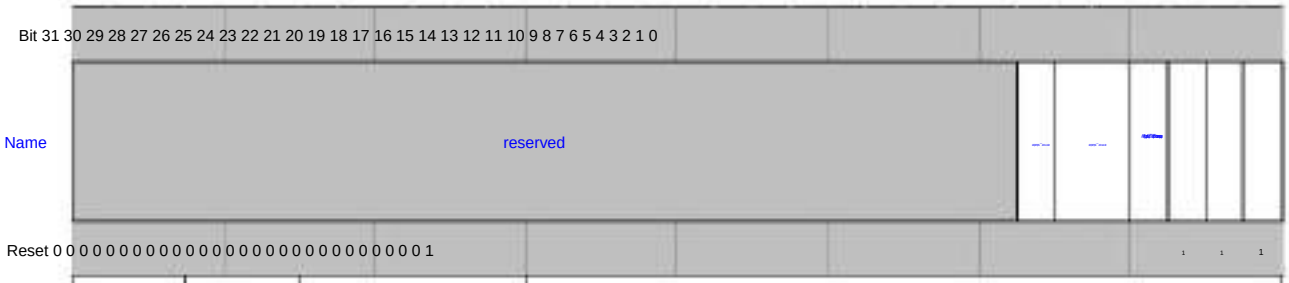
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	total_len2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	total_len2	SHA: the high bit of the Byte length of the padded message; HMAC: the high bit of the Byte length of the entire i_key_pad + padded message.

HASH_STATUS

HASH _STATUS is the HASH status register.

Offset Address	Register Name	Total Reset Value
0x8	HASH_STATUS	0x0000_000F

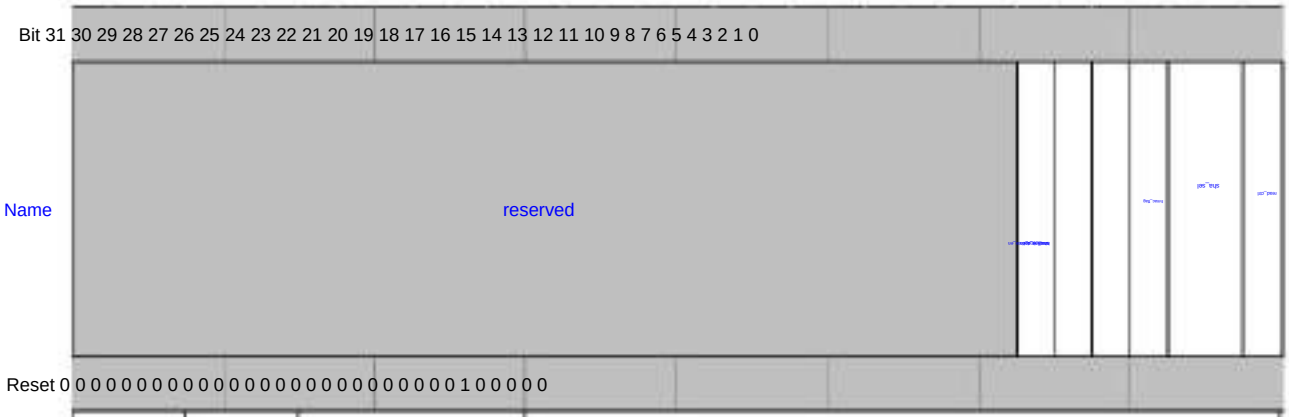


Bits	Access Name		Description
[31:7] RO		reserved	reserve.
[6]	RO	len_err	Length signal correct flag. 0: the length is correct; 1: The length is wrong.
[5:4] RO		error_state	AHB bus status. err_state[4]ÿ 0ÿahb OKÿ 1ÿahb Erroÿ err_state[5]ÿ 0ÿahb slave is idleÿ 1ÿahb slave is busyÿ
[3]	RO	rec_rdy	New data can be received (reg_rdy = msg_rdy & dma_rdy). 0: The logic internal receiving data is not ready; 1: The logic is ready to receive data internally.
[2]	RO	msg_rdy	block computes debug information. 0: CPU channel is not ready to receive data; 1: CPU channel is ready to receive data.
[1]	RO	dma_rdy	DMA debug information. 0: The dma reading of a piece of data has not been completed; 1: DMA reading of a block of data is complete.
[0]	RO	hash_rdy	Signal that the entire TOTAL_LEN calculation is complete. 0: The calculation has not been completed; 1: The calculation is complete.

HASH_CTRL

HASH_CTRL is the HASH control register.

Offset Address	Register Name	Total Reset Value
0xC	HASH_CTRL	0x0000_0020



Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
SHA algorithm; [6]	RW	sha_init_update_en	1: SHA initial value update is enabled; HMAC configuration is 0. 0: Disable, use the default initial value of the Enable, when starting the SHA calculation, the value of sha_initn_update will be used as the initial value.
[5]	RW	small_end_en	The word size of the output result is enabled. 0: enable big-endian storage; 1: little-endian storage enabled.
[4]	RW	hardkey_sel	HMAC key selection; SHA configuration is 0. 0: Select kl_key (hardware key); 1: Select mcu key (software key).
[3]	RW	hmac_flag	Calculation mode selection. 0: SHA calculation; 1: HMAC calculation.
[2:1]	RW	sha_sel	SHA mode selection. 00: SHA1 mode; 01: SHA256 mode; Others: reserved, this mode cannot be configured.
[0]	RW	read_ctrl	How to read computed data. 0ÿread message by DMAÿ 1ÿread message by CPUÿ

SHA_START

SHA_START is the start SHA calculation register.

Offset Address	Register Name	Total Reset Value
0x10	SHA_START	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	reserve.
[0]	RW	sha_start	HASH calculation start signal. 0: Do not start SHA calculation; 1: Start SHA calculation.

DMA_START_ADDR

DMA_START_ADDR is the start address register for reading message.

Offset Address	Register Name	Total Reset Value
0x14	DMA_START_ADDR	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	dma_start_addr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	dma_start_addr	DMA reads the starting address of the message. Byte address, the software needs to be configured as Word alignment.

DMA_LEN

DMA_LEN is the DMA transfer length register.

Offset Address	Register Name	Total Reset Value
0x18	DMA_LEN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	segment_len1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	segment_len1	DMA read data length. The unit is Byte. Only Word alignment is supported. After the length is configured, the logic automatically starts data reading and calculation.

DATA_IN

DATA_IN is the input data register for SHA calculation.

Offset Address	Register Name	Total Reset Value
0x1C	DATA_IN	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	data_in
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	data_in	The input data (CPU configuration input data) that needs to calculate the digest through SHA is 1 in debug_disable, and this register cannot be read.

REC_LEN1

REC_LEN1 is the receive message length register.

Offset Address	Register Name	Total Reset Value
0x20	REC_LEN1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	receive_byte_cnt
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	receive_byte_cnt	The number of bytes calculated by the current HASH module (each block calculation is 64Byte), cleared when the operation is started.

REC_LEN2

REC_LEN2 is the receive message length register.

Offset Address	Register Name	Total Reset Value
0x24	REC_LEN2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	receive_byte_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	receive_byte_cnt	The byte number of the current HASH module (each block calculation is 64byte), cleared when the operation is started.

SHA_OUT1

SHA_OUT1 is HASH output result register 1.

Offset Address	Register Name	Total Reset Value
0x30	SHA_OUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	sha_out1	SHA1/SHA256 digest output 0~31bit. Remove the reset terminal, the initial value is random.

SHA_OUT2

SHA_OUT2 is HASH output result register 2.

Offset Address	Register Name	Total Reset Value
0x34	SHA_OUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out2	SHA1/SHA256 summary output 32~63bit. Remove the reset terminal, the initial value is random.

SHA_OUT3

SHA_OUT3 is HASH output result register 3.

Offset Address	Register Name	Total Reset Value
0x38	SHA_OUT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out3	SHA1/SHA256 summary output 64~95bit. Remove the reset terminal, the initial value is random.

SHA_OUT4

SHA_OUT4 is HASH output result register 4.

Offset Address	Register Name	Total Reset Value
0x3C	SHA_OUT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out4	SHA1/SHA256 digest output 96~127bit. Remove the reset terminal, the initial value is random.

SHA_OUT5

SHA_OUT5 is HASH output result register 5.

Offset Address	Register Name	Total Reset Value
0x40	SHA_OUT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	sha_out5	SHA1/SHA256 digest output 128~159bit. Remove the reset terminal, the initial value is random.

SHA_OUT6

SHA_OUT6 is HASH output result register 6.

Offset Address	Register Name	Total Reset Value
0x44	SHA_OUT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RO	sha_out6	SHA1 is meaningless, SHA256 summary output 160~191bit.

SHA_OUT7

SHA_OUT7 is HASH output result register 7.

Offset Address	Register Name	Total Reset Value
0x48	SHA_OUT7	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_out7
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	sha_out7	SHA1 is meaningless, SHA256 summary output 192~223bit.

SHA_OUT8

SHA_OUT8 is HASH output result register 8.

Offset Address	Register Name	Total Reset Value
0x4C	SHA_OUT8	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_out8
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	sha_out8	SHA1 is meaningless, SHA256 summary output 224~255bit.

MCU_KEY0

MCU_KEY0 input key 0~31bit (cpu configuration) register for hmac.

Offset Address	Register Name	Total Reset Value
0x70	MCU_KEY0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mcu_key0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mcu_key0	HMAC input key 0~31bit (cpu configuration). When debug_disable is 1, this register cannot be read

MCU_KEY1

MCU_KEY1 input key 32~63bit (cpu configuration) register for hmac.

Offset Address	Register Name	Total Reset Value
0x74	MCU_KEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	mcu_key1	HMAC input key 32~63bit (cpu configuration). When debug_disable is 1, this register cannot be read

MCU_KEY2

MCU_KEY2 input key 64~95bit (cpu configuration) register for hmac.

Offset Address	Register Name	Total Reset Value
0x78	MCU_KEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:0]	RW	mcu_key2	HMAC input key 64~95bit (cpu configuration). When debug_disable is 1, this register cannot be read

MCU_KEY3

MCU_KEY3 input key 96~127bit (cpu configuration) register for hmac.

Offset Address	Register Name	Total Reset Value
0x7C	MCU_KEY3	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	mcu_key3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	mcu_key3	HMAC input key 96~127bit (cpu configuration). When debug_disable is 1, this register cannot be read

SHA_INIT1_UPDATE

SHA_INIT1_UPDATE is SHA initial value register 1.

Offset Address	Register Name	Total Reset Value
0x90	SHA_INIT1_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_init1_update
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sha_init1_update	31bit~0bit of SHA initial value.

SHA_INIT2_UPDATE

SHA_INIT2_UPDATE is SHA initial value register 2.

Offset Address	Register Name	Total Reset Value
0x94	SHA_INIT2_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_init2_update
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sha_init2_update	63bit~32bit of SHA initial value.

SHA_INIT3_UPDATE

SHA_INIT3_UPDATE is SHA initial value register 3.

Offset Address	Register Name	Total Reset Value
0x98	SHA_INIT3_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init3_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init3_update	95bit~64bit of SHA initial value.

SHA_INIT4_UPDATE

SHA_INIT4_UPDATE is SHA initial value register 4.

Offset Address	Register Name	Total Reset Value
0x9C	SHA_INIT4_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init4_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init4_update	127bit~96bit of SHA initial value.

SHA_INIT5_UPDATE

SHA_INIT5_UPDATE is SHA initial value register 5.

Offset Address	Register Name	Total Reset Value
0xA0	SHA_INIT5_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init5_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init5_update	159bit~128bit of SHA initial value.

SHA_INIT6_UPDATE

SHA_INIT6_UPDATE is SHA initial value register 6.

Offset Address	Register Name	Total Reset Value
0xA4	SHA_INIT6_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_init6_update
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sha_init6_update	191bit~160bit of SHA initial value.

SHA_INIT7_UPDATE

SHA_INIT7_UPDATE is SHA initial value register 7.

Offset Address	Register Name	Total Reset Value
0xA8	SHA_INIT7_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_init7_update
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sha_init7_update	223bit~192bit of SHA initial value.

SHA_INIT8_UPDATE

SHA_INIT8_UPDATE is SHA initial value register 8.

Offset Address	Register Name	Total Reset Value
0xAC	SHA_INIT8_UPDATE	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sha_init8_update
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	sha_init8_update	255bit~224bit of SHA initial value.

13.3 RNG_GEN

13.3.1 Overview

RNG_GEN is a module capable of generating truly random numbers. The generated true random numbers meet the random test standard of FIPS140-1.

13.3.2 Features

The RNG_GEN module has the following characteristics:

- Support true random number generation.
- Supports three random source selections, CPU configurable. Support for turning off the random number source.

13.3.3 Working method

RNG_GEN operation process

The operation process is as follows:

Step 1. First judge whether RNG_STAT.rng_data_count is greater than or equal to 1, if it means there is a random number, continue to execute; otherwise wait;

Step 2. Read RNG_FIFO_DATA.rng_fifo_data;

Step 3. Repeat steps 1 and 2 until the required number of random numbers is read.

----Finish

13.3.4 RNG_GEN register overview

An overview of the RNG_GEN register is shown in Table 13-4 .

Table 13-4 RNG_GEN register overview (base address is 0x120C_0000)

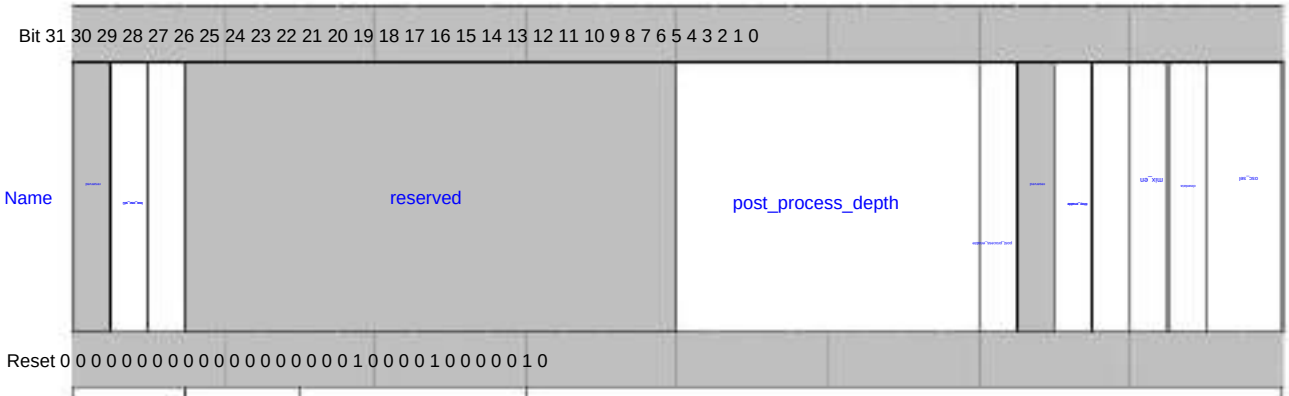
offset address name		describe	page number
0x00	RNG_CTRL	RNG Control Register	13-75
0x04	RNG_FIFO_DATA	RNG FIFO data	13-77
0x08	RNG_STAT	RNG Status Register	13-77

13.3.5 RNG_GEN register description

RNG_CTRL

RNG_CTRL is the RNG control register.

Offset Address	Register Name	Total Reset Value
0x00	RNG_CTRL	0x0000_1082



Bits	Access	Name	Description
[31]	RO	reserved	reserve.
[30]	WC	low_osc_st1	LFO anomaly test. 0: The low- frequency oscillator is normal; 1: The low-frequency oscillator output is always 1, write to clear.
[29]	WC	low_osc_st0	LFO anomaly test. 0: Low frequency oscillator is normal; 1: Low frequency oscillator output is always 0, cleared by writing.
[28:16]	RO	reserved	reserve.
[15:8]	RW	post_process_depth	Post-processing mixing depth, the larger the random effect, the better, but the slower the speed.
[7]	RW	post_process_enabl	Random number pre-processing is enabled. After using this function, the speed of random number generation is reduced by 1/ (post_process_depth+1). It is 0: disable; 1: enable.
[6]	RO	reserved	reserve.
[5]	RW	drop_enable	The 2-bit data enable with the same two consecutive bit values is discarded, and the random number generation speed is reduced by 1/3 after using this function. 0: disable; 1: enable.
[4]	RW	filter_enable	Random number pre-processing filtering is enabled. After using this function, the speed of random number generation is reduced by 4 times. 0: disable; 1: enable.

[3] RW mix_en			Data mixing enabled. 0: disable; 1: enable.
[2] WC cleardata			Clear the random number. 0: do not clear; 1: Clear.
[1:0] RW osc_sel			Random source selection. 00ÿdisable RNGÿ 01: use random source 1; 10: use random source 2; 11: Use random source 3.

RNG_FIFO_DATA

RNG_FIFO_DATA is RNG FIFO number.

Offset Address	Register Name	Total Reset Value
0x04	RNG_FIFO_DATA	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rng_fifo_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rng_fifo_data	Read this register directly to read random numbers.

RNG_STAT

RNG_STAT is the RNG status register.

Offset Address	Register Name	Total Reset Value
0x08	RNG_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:3]	RO	reserved	reserve.
[2:0]	RO	rng_data_count How many	32bit random numbers are there in the random number fifo, up to 4.

13.4 RSA

13.4.1 Overview

RSA is a public key encryption and decryption algorithm, which mainly realizes encryption and decryption through modular exponentiation calculation.

Encryption: C = ME mod N; Decryption: M=CD mod N. M is the plaintext, C is the ciphertext, (N,E) is the public key, and (N,D) is the private key.

RSA supports RSA1024/2048/4096 and complies with PKCS#1 V1.5/2.1 standard.

The RSA module is suitable for data encryption and decryption, and digital signature verification.

13.4.2 Features

RSA has the following characteristics:

Supports key bit widths of 1024bit, 2048bit, and 4096bit. Support

2048 key bit width, the minimum performance is 10 ops/s (10 operations/

second). Support CRC16 to debug the key.

Support the clearing of RSA internal key RAM, message RAM, and result RAM.

13.4.3 Functional Description

Functional principle

The RSA module is mainly used for data encryption and decryption, and digital signature verification. Software can configure the registers, and then start the RSA module to complete the modular exponentiation. RSA also supports CRC16 to calculate the key stored inside the logic, and output the result to

It is convenient to debug whether the key is correct; at the same time, it also supports clearing the internal key RAM, message RAM, and result RAM.

13.4.4 Working method

RSA encryption and decryption operation process

The operation process is as follows:

Step 1. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 2. Configure SEC_RSA_MOD_REG. sec_rsa_mod_sel=0;

Configure SEC_RSA_MOD_REG..sec_rsa_key_width=1; (RSA key bit width value: RSA1024=0; RSA2048=1; RSA4096=2; RSA1024=3);

configSEC_RSA_MOD_REG . sec_rsa_data0_clr=0ÿ

configure SEC_RSA_MOD_REG.sec_rsa_data1_clr =0;

configure SEC_RSA_MOD_REG.sec_rsa_data2_clr =0;

Step 3. Configure SEC_RSA_WPKT_REG. sec_rsa_wpkt_reg, the configuration message length needs to be the same as the key bit width indicated in the mode register;

Step 4. Configure SEC_RSA_WSEC_REG. sec_rsa_wsec_reg, first configure the key parameter N, and then configure the key parameter E/D. The length of each parameter needs to be the same as the key bit width indicated in the mode register;

Step 5. Configure SEC_RSA_START_REG. sec_rsa_start_reg=1;

Step 6. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 7. Read SEC_RSA_RRSLT_REG. sec_rsa_rrslt_reg, the length of the read result needs to be the same as the key bit width indicated in the mode register.

----Finish

CRC16 key debugging

The operation process is as follows:

Step 1. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 2. Configure SEC_RSA_MOD_REG. sec_rsa_mod_sel=3;

Configure SEC_RSA_MOD_REG. sec_rsa_key_width=1; (RSA key bit width value: RSA1024=0; RSA2048=1; RSA4096=2; RSA1024=3);

configSEC_RSA_MOD_REG . sec_rsa_data0_clr=0ÿ

configure SEC_RSA_MOD_REG.sec_rsa_data1_clr =0;

configure SEC_RSA_MOD_REG.sec_rsa_data2_clr =0;

Step 3. Configure SEC_RSA_START_REG. sec_rsa_start_reg=1;

Step 4. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 5. Read the CRC result SEC_CRC16_REG. sec_rsa_crc16_dat.

----Finish

Clear RAM to 0

The operation process is as follows:

Step 1. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 2. Configure SEC_RSA_MOD_REG. sec_rsa_mod_sel=2;

Configure SEC_RSA_MOD_REG. sec_rsa_key_width=1; (RSA key bit width value: RSA1024=0; RSA2048=1; RSA4096=2; RSA1024=3);

Configure SEC_RSA_MOD_REG.sec_rsa_data0_clr =1; (1 is to clear the data in the key RAM; 0 is not to clear the key RAM);

Configure SEC_RSA_MOD_REG.sec_rsa_data1_clr =1; (1 means to clear the data in the message RAM; 0 means not to clear the message RAM);

Configure SEC_RSA_MOD_REG.sec_rsa_data2_clr =1; (1 is to clear the data in the result RAM; 0 is to clear the result RAM);

Step 3. Configure SEC_RSA_START_REG. sec_rsa_start_reg=1;

Step 4. Read the SEC_RSA_BUSY_REG. sec_rsa_busy_reg status register to determine whether it is 0; if it is 0 continue execution; otherwise wait;

Step 5. Read SEC_RSA_RPKT_REG sec_rsa_rpkt_reg to determine whether the message RAM is cleared to 0;

Step 6. Read SEC_RSA_RRSLT_REG sec_rsa_rrslt_reg to determine whether the result RAM is cleared to 0;

Step 7. Verify the key through the CRC process; judge whether the key RAM is cleared to 0.

----Finish

13.4.5 RSA register overview

An overview of the RSA registers is shown in Table 13-5 .

Table 13-5 RSA register overview (base address is 0x120B_0000)

offset address	name	describe	page number
0x50	SEC_RSA_BUSY_REG	SEC_RSA Module BUSY Status Register 13-81	
0x54	SEC_RSA_MOD_REG	SEC_RSA Module Operating Mode Register 13-82	

offset address name		describe	page number
0x58	SEC_RSA_WSEC_REG SEC_RSA module write key register		13-83
0x5C	SEC_RSA_WPKT_REG SEC_RSA module write message data register 13-83		
0x60	SEC_RSA_RPKT_REG SEC_RSA module read message register		13-83
0x64	SEC_RSA_RRSLT_REG SEC_RSA module read calculation result register 13-84		
0x68	SEC_RSA_START_REG SEC_RSA module start modular power configuration register 13-84		
0x6C	SEC_RSA_ADDR_REG SEC_RSA module key, message, result	RAM Address Register	13-84
0x70	SEC_RSA_ERROR_REG SEC_RSA Module Error Alarm Status Register 13-85		
0x74	SEC_CRC16_REG	Key CRC calculation result of SEC_RSA 13-86	

13.4.6 RSA register description

SEC_RSA_BUSY_REG

SEC_RSA_BUSY_REG is the BUSY status register of the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x50	SEC_RSA_BUSY_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name		Description
[31:1]	RO	reserved	reserve.
[0]	RO	sec_rsa_busy_reg	BUSY status register for SEC_RSA. 0: The module is in idle state; 1: The module is in BUSY state.

SEC_RSA_MOD_REG

SEC_RSA_MOD_REG is the working mode register of SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x54	SEC_RSA_MOD_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	reserve.
[6]	RW	sec_rsa_data2_clr	Clear RSA result RAM enable. 0: Do not clear the result RAM; 1: Clear the RAM data storing the result.
[5]	RW	sec_rsa_data1_clr	Clear RSA message RAM enable. 0: Do not clear message RAM; 1: Clear RAM data for storing messages.
[4]	RW	sec_rsa_data0_clr	Clear RSA key RAM enable. 0: Do not clear key RAM; 1: Clear the RAM data where the key is stored.
[3:2]	RW	sec_rsa_key_width	Key bit width selection. 00: The key bit width is 1024; 01: The key bit width is 2048; 10: The key bit width is 4096; 11: The key bit width is 1024.
[1:0]	RW	sec_rsa_mod_sel	Working mode selection. 00: Modular exponentiation encryption and decryption calculation; 01: Update key without modular exponentiation calculation (this mode configuration is not supported at the moment); 10: Clear 0 to RAM; 11: Perform CRC16 calculation on key.

SEC_RSA_WSEC_REG

SEC_RSA_WSEC_REG Write key register for SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x58	SEC_RSA_WSEC_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wsec_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	WO	sec_rsa_wsec_reg CPU configuration key address register.

SEC_RSA_WPKT_REG

SEC_RSA_WPKT_REG Write message data register for SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x5C	SEC_RSA_WPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	WO	sec_rsa_wpkt_reg CPU configuration message address register.

SEC_RSA_RPKT_REG

SEC_RSA_RPKT_REG read message register for SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x60	SEC_RSA_RPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_rpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access Name	Description
[31:0]	RO	sec_rsa_rpkt_reg CPU read message address register.

SEC_RSA_RRSLT_REG

SEC_RSA_RRSLT_REG read calculation result register for SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x64	SEC_RSA_RRSLT_REG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	sec_rsa_rrslt_reg
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:0] RO	sec_rsa_rrslt_reg	CPU read result address register.

SEC_RSA_START_REG

SEC_RSA_START_REG Start modular exponentiation configuration register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x68	SEC_RSA_START_REG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name	Description
[31:1] RO	reserved	reserve.
[0] RW	sec_rsa_start_reg	CPU configuration starts. 0: do not start RSA; 1: Start RSA.

SEC_RSA_ADDR_REG

SEC_RSA_ADDR_REG is the RAM address register of SEC_RSA module key, message and result.

Offset Address	Register Name	Total Reset Value
0x6C	SEC_RSA_ADDR_REG	0x0000_0000

Bit	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Name	sec_rsa_add_rslt	sec_rsa_addre_pkt	sec_rsa_addre_d	sec_rsa_addr_n
Reset	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	sec_rsa_addere_rslt has	The resulting RAM address. Each address offset value is 4B; that is, if the value indicates 1, it means that stored 4B data internally; since counting starts from 0, when storing to the maximum key bit width, the value is 0.
[23:16]	RO	has been stored or read	Message RAM address. Each address offset value is 4B; that is, if the value indicates 1, it means that 4B data internally by sec_rsa_addre_pkt; since counting starts from 0, when storing to the maximum key bit width, the value is 0.
[15:8]	RO	sec_rsa_addre_d	Key parameter E/D RAM address. The address offset value is 4B each time; that is, if the value indicates 1, it means that 4B data has been stored internally; since counting starts from 0, when storing to the maximum key bit width, the value is 0.
[7:0]	RO	sec_rsa_addr_n	Key parameter N RAM address. The address offset value is 4B each time; that is, if the value indicates 1, it means that 4B data has been stored internally; since counting starts from 0, when storing to the maximum key bit width, the value is 0.

SEC_RSA_ERROR_REG

SEC_RSA_ERROR_REG is the SEC_RSA module error alarm status register.

Offset Address	Register Name	Total Reset Value
0x70	SEC_RSA_ERROR_REG	0x0000_0000

Bit	31:2	1	0
Name	reserved		
Reset	0	0	0

Bits	Access Name		Description
[31:2]	RO	reserved	reserve.
[1]	RO	sec_rsa_err1	Current external RSA input key N even warning. (When the key RAM is cleared to 0, no detection is performed) 0: There is no abnormality in the external input key; 1: The external input key N is an even number.
[0]	RO	reserved	reserve.

SEC_CRC16_REG

SEC_CRC16_REG is the key CRC calculation result of SEC_RSA.

Offset Address	Register Name	Total Reset Value
0x74	SEC_CRC16_REG	0x0000_0000

Bit	31:16	15:0
Name	reserved	sec_rsa_crc16_dat
Reset	0	0

Bits	Access Name		Description
[31:16]	RO	reserved	reserve.
[15:0]	RO	CRC calculation result of sec_rsa_crc16_dat key.	

13.5 Cipher Hash Key Ctrl

13.5.1 Working method

Cipher Hash Key Ctrl has three working modes: burning KEY to OTP, loading KEY to cipher, loading KEY to hash.

13.5.1.1 Burn KEY to OTP

Before programming, the data in OTP is all 0; after programming is enabled, Cipher Key Ctrl will program the macrocell corresponding to the KEY value and the OTP address (otp_key_add) of the KEY to 1.

Step 1. Assign values to the KEY registers KL_WKEY0, KL_WKEY1, KL_WKEY2, and KL_WKEY3 .

Step 2. Query the state of the status register KL_STA , and wait for ctrl_rdy to be 1, ctrl_busy0 to be 0, and ctrl_busy1 to be 0.

Step 3. Write the OTP address of the KEY to otp_key_add in the control register KL_CTRL , write otp_kd_mode

1. Write 0 in cipher_kl_mode and hash_kl_mode to enable programming KEY to OTP mode.

Step 4. Write 1 to start in the control register KL_CTRL to start the operation.

Step 5. Check that the value of key_wt_finish in the status register KL_STA changes from 0 to 1, indicating that all the data has been programmed. The programming operation ends. Note: If key_wt_error is 1, it means programming failed, and the KEY address has already been programmed.

----Finish

13.5.1.2 Load KEY to cipher

The operation process is as follows:

Step 1. Query the state of the status register KL_STA, and wait for ctrl_rdy to be 1, ctrl_busy0 to be 0, and ctrl_busy1 to be 0.

Step 2. Write the OTP address of KEY to otp_key_add in the control register KL_CTRL , cipher_key_add to load KEY to the KEY address of cipher, write 1 to cipher_kl_mode, and write 0 to otp_kd_mode and hash_kl_mode to enable loading KEY to cipher mode.

Step 3. Write 1 to start in the control register KL_CTRL to start the operation.

Step 4. Check that the value of cipher_kl_finish in the status register KL_STA changes from 0 to 1, indicating that the KEY is loaded into cipher complete. Operation complete.

----Finish

13.5.1.3 Load KEY to hash

The operation process is as follows:

Step 1. Query the state of the status register KL_STA , and wait for ctrl_rdy to be 1, ctrl_busy0 to be 0, and ctrl_busy1 to be 0.

Step 2. Write the OTP address of KEY to otp_key_add in the control register KL_CTRL , and write hash_kl_mode

1. Write 0 in otp_kd_mode and cipher_kl_mode to enable loading KEY to hash mode.

Step 3. Write 1 to start in the control register KL_CTRL to start the operation.

Step 4. Check that the value of hash_key_read_busy in the status register KL_STA changes from 1 to 0, indicating that all data has been loaded. Operation complete.

----Finish

13.5.2 Cipher Hash Key Ctrl Register Overview

The Cipher Hash Key Ctrl register overview is shown in Table 13-6 .

Table 13-6 Cipher Hash Key Ctrl register overview (base address is 0x1207_0800)

offset address name		describe	page number
0x0000	KL_WKEY0	KEY programming register 0	13-88
0x0004	KL_WKEY1	KEY programming register 1	13-88
0x0008	KL_WKEY2	KEY programming register 2	13-89
0x000C	KL_WKEY3	KEY programming register 3	13-89
0x0010	KL_CTRL	KL_CTRL Register	13-89
0x0014	KL_STA	Status Indication Register	13-91

13.5.3 Cipher Hash Key Ctrl Register Description

KL_WKEY0

KL_WKEY0 is KEY programming register 0.

Offset Address	Register Name	Total Reset Value
0x0000	KL_WKEY0	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	key0
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access Name		Description
[31:0]	WO key0		The key[31:0] programmed into OTP.

KL_WKEY1

KL_WKEY1 is KEY programming register 1.

Offset Address	Register Name	Total Reset Value
0x0004	KL_WKEY1	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	key1
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	key1	The key[63:32] programmed to OTP.

KL_WKEY2

KL_WKEY2 is KEY programming register 2.

Offset Address	Register Name	Total Reset Value
0x0008	KL_WKEY2	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	key2
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	key2	The key[95:64] programmed to OTP.

KL_WKEY3

KL_WKEY3 is KEY programming register 3.

Offset Address	Register Name	Total Reset Value
0x000C	KL_WKEY3	0x0000_0000

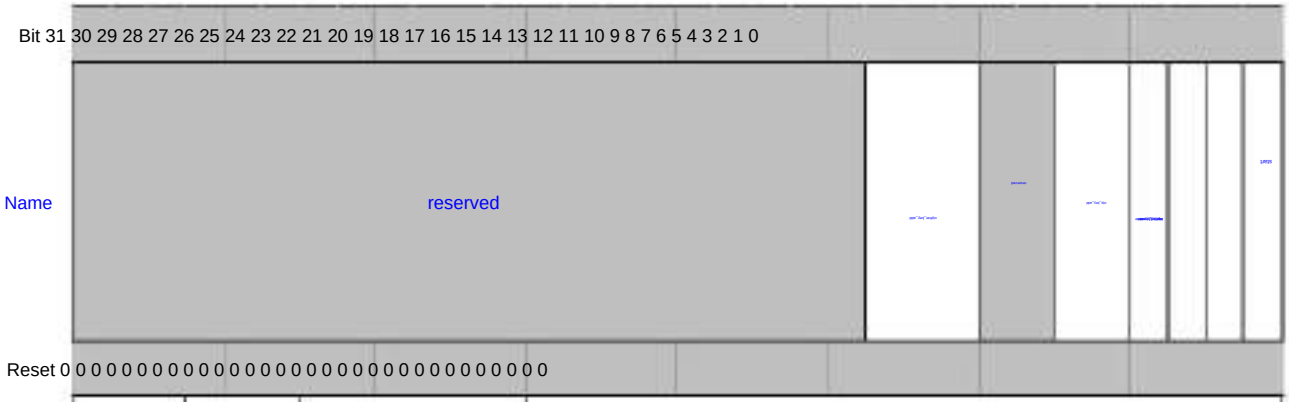
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	key3
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	key3	The key[127:96] programmed to OTP.

KL_CTRL

KL_CTRL is the KL_CTRL register.

Offset Address	Register Name	Total Reset Value
0x0010	KL_CTRL	0x0000_0000

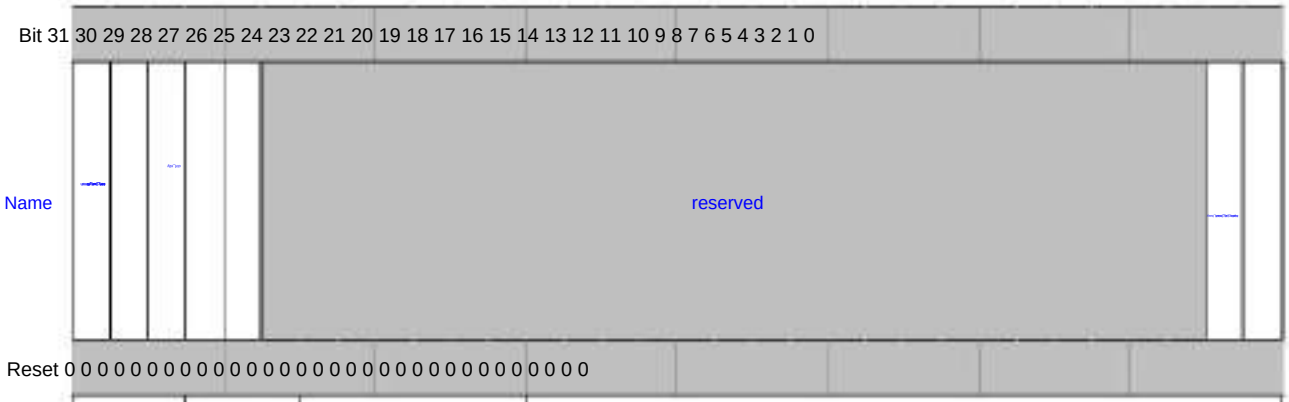


Bits	Access	Name	Description
[31:11]	RO	reserved	reserve.
[10:8]	RW	cipher_key_add	Load KEY to the KEY address of cipher.
[7:6]	RW	reserved	reserve.
[5:4]	RW	otp_key_add	The address of KEY in OTP. Used to burn or load KEY.
[3]	RW	hash_kl_mode	Load KEY to hash operation enable. 0: disable; 1: enable. hash_kl_mode, otp_kd_mode, and cipher_kl_mode all have one and only one is 1, that is, only one function can take effect at the same time.
[2]	RW	otp_kd_mode	The operation of writing KEY to OTP is enabled. 0: disable; 1: enable. hash_kl_mode, otp_kd_mode, and cipher_kl_mode all have one and only one is 1, that is, only one function can take effect at the same time.
[1]	RW	cipher_kl_mode	Load KEY to cipher operation enable. 0: disable; 1: enable. hash_kl_mode, otp_kd_mode, and cipher_kl_mode all have one and only one is 1, that is, only one function can take effect at the same time.
[0]	RW	start	Initiate operation, write 1 to initiate. Reading back is meaningless. Only when ctrl_busy1 and ctrl_busy0 are both 0 and ctrl_rdy is 1 can a new operation be initiated.

KL_STA

KL_STA is the status indication register.

Offset Address	Register Name	Total Reset Value
0x0014	KL_STA	0x0000_0000



Bits	Access Name		Description
[31] RO		key_wt_finish	Whether the operation of burning key to OTP is over. 0: not completed; 1: Completed.
[30] RO		key_wt_error	Is there any error in the operation of burning key to OTP? 0: No error, programming is successful; 1: Error, the KEY address has been programmed.
[29] RO		ctrl_busy1	Controller busy1 signal, only when both ctrl_busy1 and ctrl_busy0 are 0, and ctrl_rdy is 1, can initiate a new operation.
[28] RO		ctrl_busy0	Controller busy0 signal, only when both ctrl_busy1 and ctrl_busy0 are 0, and ctrl_rdy is 1, can initiate a new operation.
[27] RO		ctrl_rdy	Controller ready signal, only when ctrl_busy1 and ctrl_busy0 are both 0, and ctrl_rdy is 1, can initiate a new operation.
[26:2] RO		reserved	reserve.
[1]	RO	completed; completed. the hash_key_read_bus	Whether the operation of loading key to hash has ended. 0: 1: not The hash encryption and decryption operations are started only after the loading is complete.
[0]	RO	cipher_kl_finish	Whether the operation of loading key to cipher has ended. 0: not completed; 1: Completed. The encryption and decryption operation of cipher is started only after the loading is completed.

14 Difference between Hi3519V100 and Hi3519V101

The differences between Hi3519V100 and Hi3519V101 are shown in Table 14-1 .

Table 14-1 Difference between Hi3519V100 and Hi3519V101

point of difference	Hi3519V100	Hi3519V101
CPU A17	Support up to 1.15Ghz	Support up to 1.25Ghz
DDR	DDR maximum frequency support up to 800Mhz	DDR maximum frequency support up to 933Mhz
JPEG	base version	Add OSD, loop buffer function
intelligent	base version	The SVM lookup table supports up to 4K*16bit
double sensor	not support	Support dual-channel sensor input Support dual-channel ISP processing, the maximum resolution of the first channel is 16M, and the maximum resolution of the second channel is 8M The maximum performance of the system supports the first 8M input + the second 2M input
ISP	The highest frequency is supported up to 300Mhz	The highest frequency of the first channel ISP supports up to 600Mhz Support bayer scaler Support camera ZSL (Zero Second Later) mode
two-way splicing	not support	Support dual-channel input, maximum support two-channel 4M@30fps real-time splicing, support two-channel 8M non-real-time splicing. Support video, capture and work at the same time

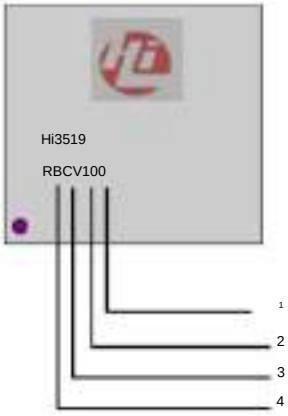
GDC	Support 180, 360 degrees and normal basic correction modes	Supports PMF (project mapping function)/ LMF (Lens mapping function) specifications. Optimize the interpolation algorithm and improve image quality. Support pincushion distortion correction.
Encoder performance	8M@30fps+720P@30fps	The performance is improved to 8M@30fps+1080P@30fps. H265/H264 supports B-frames. H265 encoding supports SSD and PSNR statistical reporting. Support smart QP (QP map), support QP histogram statistics report. Support madi and madp reporting.
craft	TSMC 28HPC	TSMC 28HPC+
encapsulation	15x15 TFBGA 0.65pitch	10x10 FC-BGA 0.4pitch
power consumption	1.6w	1.25W (single-channel 4K2K H265 dual-stream 8M@30fps+720P@30fps encoding scene)

Table of contents

A Ordering Information

The Hi3519V100 chip identification is shown in Figure A-1 .

Figure A-1 Hi3519V100 chip identification



The definition of Hi3519V100 chip identification is shown in Table A-1 .

Table A-1 Hi3519V100 chip identification definition

ID number		meaning
1 version number		Chip version number
2 temperature marking		C: Commercial (commercial supplies)
3 Package marking		BÿBGA
4 Environmental label		RÿRoHS