Hi3519 V100 Professional HD IP Camera SoC

Data Sheet

Issue 00B02

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Contents

About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of Hi3519 V100. This document also describes the interface timings and related parameters in diagrams. In addition, this document describes the pins, pin usages, performance parameters, and package dimension of Hi3519 V100 in detail.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3519	V100

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.

Symbol	Description
 WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
 CAUTION	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
TIP	Indicates a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2015-10-20)

This issue is the second draft release.

Chapter 1 Product Description

Section 1.3.11 is modified.

Chapter 8 Intelligent Video Engine

In section 8.1.3.2, the descriptions of **SAD** is added.

02-A Ordering Information

The contents related to Hi3519 V100 mark is added.

Issue 00B01 (2015-09-15)

This issue is the first draft release.

Contents

Figures

Tables

1 Product Description

1.1 Description

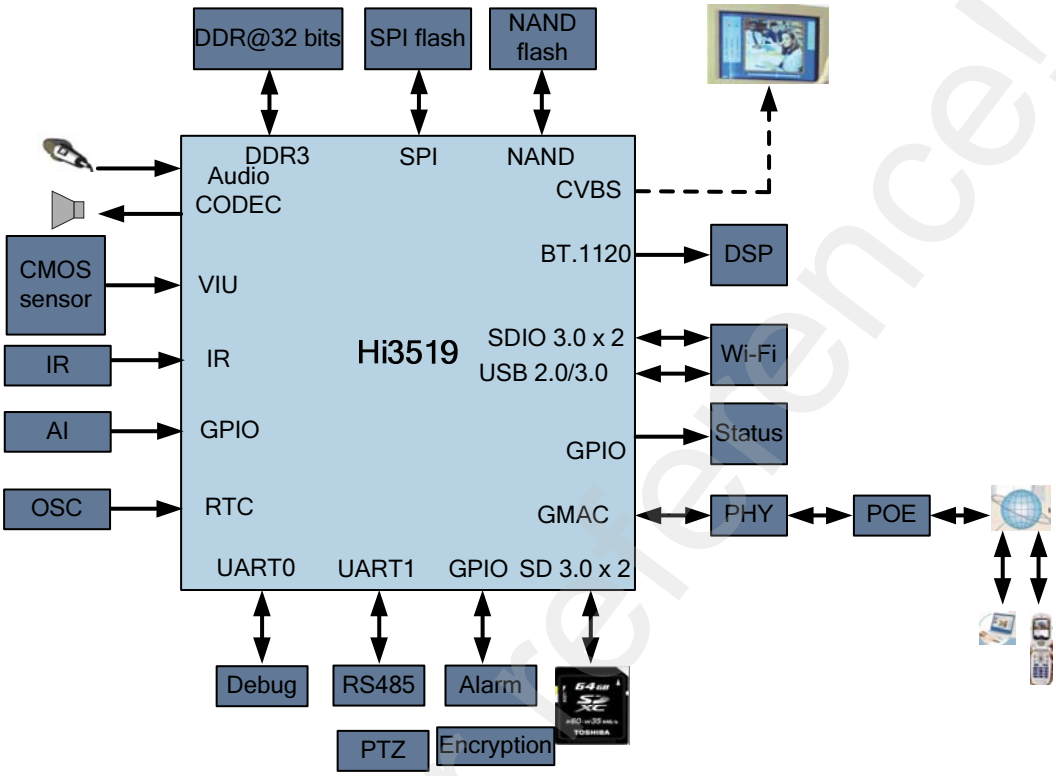
As a new-generation industry-specific SoC designed for the HD IP camera, Hi3519 V100 integrates a new-generation ISP and uses the latest H.265 video compression encoder in the industry as well as advanced low-power technology and architecture design. These features enable Hi3519 V100 to continuously maintain the leading position in the aspects of low bit rate, high picture quality, and low power consumption. Hi3519 V100 supports 90° or 270° rotation and lens distortion correction by using hardware, which meet requirements in various surveillance application scenarios. It also supports 3A algorithms, which allow customers to design various models of IP cameras that contain integrated camera cores. Hi3519 V100 integrates the POR, RTC, and audio CODEC and supports various sensor levels and clock outputs, which significantly reduces the EBOM cost of the HD IP camera based on Hi3519 V100. The Hi3519 V100 HiSilicon SDK features high stability and ease of use, supports rapid mass production, and facilitates system layout of DVRs, NVRs, and IP cameras.

1.2 Application Scenarios

1.2.1 Hi3519 V100 HD IP Camera Solution

Figure 1-1 shows the typical application scenario of the Hi3519 V100.

Figure 1-1 Application block diagram of Hi3519 V100

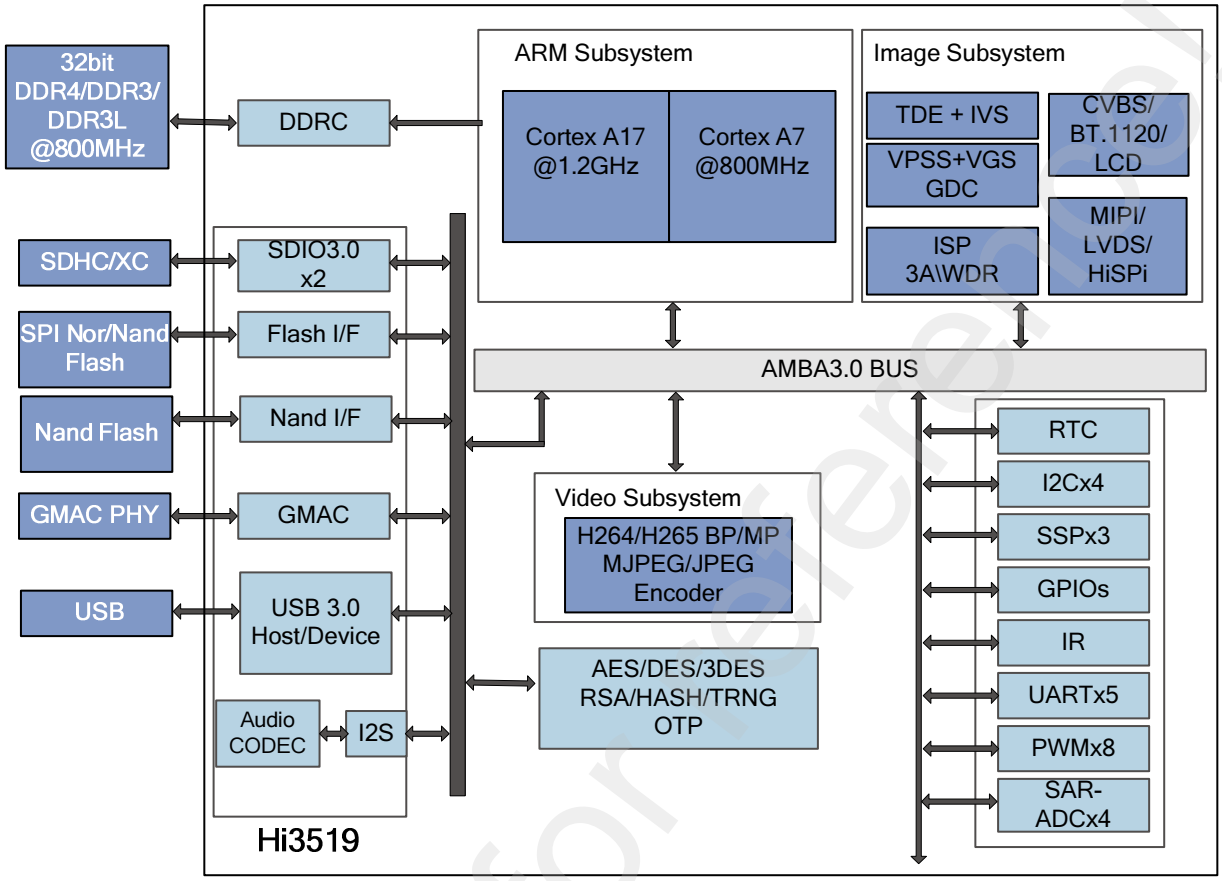


1.3 Architecture

1.3.1 Overview

Figure 1-2 shows the logic block diagram of the Hi3519 V100.

Figure 1-2 Logic block diagram of the Hi3519 V100



1.3.2 Processor Core

- 800 MHz A7 core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache
- 1.2 GHz A17 core, supporting 32 KB I-cache, 32 KB D-cache, and 256 KB L2 cache
- Neon acceleration, integrated FPU
- ARM@big-LITTLE architecture

1.3.3 Video Encoding

- H.264 BP/MP/HP
- H.265 Main Profile
- I/P frame H.264/H.265 encoding
- MJPEG/JPEG baseline encoding

1.3.4 Video Encoding Performance

- Maximum 16-megapixel resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capabilities
  - 4K x 2K@30 fps+720p@30 fps
  - 16 megapixels@2 fps
- JPEG snapshot at 8-megapixel@30 fps

- CBR/VBR control, ranging from 16 kbit/s to 100 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 60 fps
- Encoding of eight ROIs

1.3.5 Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

1.3.6 Video and Graphics Processing

- 3D denoising, image enhancement, and dynamic contrast improvement
- Anti-flicker for output videos and graphics
- 1/15.5x to 16x video scaling
- 1/2x to 2x graphics scaling
- OSD overlaying of eight regions before encoding
- Video graphics overlaying of two layers (video layer and graphics layer)

1.3.7 ISP

- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilization
- Anti-fog
- Lens distortion correction and fisheye correction
- Picture rotation by 90° or 270°
- Picture mirroring and flipping
- 4F/3F/2F frame-/line-based digital WDR and tone mapping
- ISP tuning tools for the PC

1.3.8 Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, ADPCM, and G.726 protocols
- Audio 3A functions (AEC, ANR, and ALC)

1.3.9 Security Engine

- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA1024/2048/4096 signature verification algorithm implemented by using hardware
- Hash-SHA1/256 and HMAC_SHA1/256 tamper proofing algorithms implemented by using hardware
- Integrated 512-bit OTP storage space and hardware random number generator

1.3.10 Video Interfaces

- VI Interfaces
  - 8-/10-/12-/14-bit RGB Bayer DC timing VI, at most 150 MHz clock frequency
  - BT.601, BT.656, or BT.1120 VI interface
  - 12-lane MIPI, LVDS/sub-LVDS interface, and HiSPI
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
- VO interfaces
  - One PAL/NTSC output for automatic load detection
  - One BT.1120/BT.656 VO interface for connecting to an external HDMI or SDI, supporting at most 1080p@60 fps LCD output

1.3.11 Audio Interfaces

- Integrated audio CODEC supporting 16-bit audio inputs and outputs
- I2S interface for connecting to an external audio CODEC
- Dual-channel differential MIC inputs for reducing background noises

1.3.12 Peripheral Interfaces

- POR
- One integrated high-precision RTC
- Integrated 4-channel SAR ADC
- Five UART interfaces
- IR interface, I^2C interface, SSP master interface, and GPIO interface
- Eight PWM interfaces (four independent interfaces and four ones multiplexed with other pins)
- Two SD 3.0/SDIO 3.0 interfaces, supporting SDXC
- One USB 3.0/USB 2.0 host/device port
- One PCIe 2.0 interface in master/slave mode
- RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and 1000 Mbit/s full-duplex mode, and TSO network acceleration

1.3.13 External Memory Interfaces

- DDR4/DDR3/DDR3L interface
  - One 32-bit DDR4/3/3L interface with the maximum frequency of 800 MHz (1.6 Gbit/s)
  - Maximum capacity of 1024 MB for a 16-bit DDR SDRAM
  - Maximum total capacity of 2048 MB for two 16-bit DDR SDRAMs
- SPI NOR flash interface
  - 1-/2-/4-wire mode

  - 3-byte or 4-byte address mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface, supporting the maximum capacity of 512 MB
- eMMC 5.0 interface, supporting the maximum capacity of 64 GB
- NAND flash interface
  - 8-bit data width
  - SLC or MLC
  - 4-/8-/24-/40-/64-bit ECC
  - Components with 8 GB or larger capacity
- Booting from the SPI NOR flash, SPI NAND flash, or NAND flash
- Booting from an eMMC

1.3.14 SDK

- Linux-3.18-based SDK
- High-performance H.264/H.265 PC/iOS/Android decoding library

1.3.15 Physical Specifications

- Power consumption
  - 1.5 W typical power consumption in the 4K x 2K scenario
  - Multi-level power saving mode
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
  - 1.2 V, 1.35 V, or 1.5 V DDR4/3/3L SDRAM interface voltage
- Package
  - RoHS, TFBGA
  - Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.)
  - Ball pitch of 0.65 mm (0.026 in.)

1.4 Boot Modes

Hi3519 V100 can boot from:

- BOOTROM
- External SPI flash
- External NAND flash
- External eMMC
- A DDR of the slave chip over the PCIe interface

During power-on reset (POR), the boot mode of the Hi3519 V100 depends on the values of the BOOTROM_SEL, BOOT_SEL1, and BOOT_SEL0 signals. Table 1-1 describes the mapping between the signal values and boot modes.

Table 1-1 Boot modes

BOOTROM_SEL	BOOT_SEL0	BOOT_SEL1	SFC_EMMC_BOOT_MODE	SFC_DEVICE_MODE	SPI_NAND_SEL	UPDATE_FROM_SDIO	Boot Mode
1	x	x	x	x	x	x	BOOTROM
0	0	0	0	0	x	x	External SPI NOR flash (3-byte address mode)
0	0	0	1	0	x	x	External SPI NOR flash (4-byte address mode)
0	0	0	0	1	0	x	External SPI NAND flash (1-wire mode; the plane address bit is disabled)
0	0	0	1	1	0	x	External SPI NAND flash (4-wire mode; the plane address bit is disabled)
0	0	0	0	1	1	x	External SPI NAND flash (1-wire mode; the plane address bit is enabled)
0	0	0	1	1	1	x	External SPI NAND flash (4-wire mode; the plane address bit is enabled)
0	0	1	x	x	x	x	External NAND flash
0	1	0	0	x	x	x	External eMMC (4-wire mode)
0	1	0	1	x	x	x	External eMMC (8-wire mode)
0	1	1	x	x	x	x	A DDR of the slave chip over the PCIe interface

NOTE

- The BOOTROM_SEL signal is multiplexed with the external pin VO_DAT2.
- The BOOT_SEL0 signal is multiplexed with the external pin VO_DAT0.

- The BOOT_SEL1 signal is multiplexed with the external pin VO_DAT1.
- The SFC_EMMC_BOOT_MODE signal is multiplexed with the external pin VO_DAT3.
- The SFC_DEVICE_MODE signal is multiplexed with the external pin VO_DAT4.
- The SPI_NAND_SEL signal is multiplexed with the external pin EPHY_RSTN.
- The UPDATE_FROM_SDIO signal is multiplexed with the external pin VO_DAT6.

In BOOTROM boot mode, Hi3519 V100 boots from the BOOTROM after the serial port communication mechanism is started, the communication between the serial port and related software running on the PC is set up, and the boot program is downloaded. For details, see the *HiBurn User Guide*. If the serial port communication times out, the levels of BOOT_SEL1 and BOOT_SEL0 are checked. If BOOT_SEL1 and BOOT_SEL0 are 0, Hi3519 V100 boots from the external SPI flash; if BOOT_SEL1 is 0 and BOOT_SEL0 is 1, Hi3519 V100 boots from the external NAND flash; if BOOT_SEL1 is 1 and BOOT_SEL0 is 0, Hi3519 V100 boots from the external eMMC.

When Hi3519 V100 boots from a DDR of the slave chip over the PCIe interface, the CPU does not start after the POR is deasserted. Instead, the master chip loads the boot program to a DDR of the slave chip over the PCIe interface, and deasserts the reset on the CPU of the slave chip over the PCIe interface. Then the slave chip loads the boot program from the DDR.

1.5 Address Space Mapping

Table 1-2 describes the address space mapping.

Table 1-2 Address space mapping

Start Address	End Address	Function	Size	Description
0x0000_0000	0x03FF_FFFF	Memory selected for address remapping. The address points to the on-chip RAM after remapping is cleared.	64 MB	Remapping: {BOOTROM_SEL, BOOT_SEL1, BOOT_SEL0} 3'b000: SPI flash memory space 3'b001: NAND flash memory space 3'b011: BOOTRAM Other values: BOOTROM The address points to the on-chip RAM after remapping is cleared.
0x0400_0000	0x0400_FFFF	BOOTROM address space	64 KB	The actual size is 16 KB.
0x0401_0000	0x0401_FFFF	BOOTRAM address space	64 KB	The actual size is 28 KB.
0x0402_0000	0x0406_FFFF	Reserved	320 KB	

Start Address	End Address	Function	Size	Description
0x0407_0000	0x0FFF_FFFF	Reserved	-	
0x1000_0000	0x1000_FFFF	FMC register	64 KB	
0x1001_0000	0x1001_FFFF	Reserved	64 KB	
0x1002_0000	0x1002_FFFF	Reserved	64 KB	
0x1003_0000	0x1003_FFFF	DMAC register	64 KB	
0x1004_0000	0x1004_FFFF	Reserved	64 KB	
0x1005_0000	0x1005_FFFF	GSF register	64 KB	
0x1006_0000	0x1006_FFFF	Reserved	64 KB	
0x1007_0000	0x1007_FFFF	Reserved	64 KB	
0x1008_0000	0x1008_FFFF	Cipher register	64 KB	
0x1009_0000	0x1009_FFFF	Hash register	64 KB	
0x100A_0000	0x100A_FFFF	Reserved	64 KB	
0x100B_0000	0x100B_FFFF	Reserved	64 KB	
0x100C_0000	0x100C_FFFF	SDIO0 register	64 KB	
0x100D_0000	0x100D_FFFF	SDIO1 register	64 KB	
0x100E_0000	0x100E_FFFF	eMMC register	64 KB	
0x100F_0000	0x100F_FFFF	Reserved	64 KB	
0x1010_0000	0x1010_FFFF	Reserved	64 KB	
0x1011_0000	0x1011_FFFF	USB 2.0 host OHCI register	64 KB	
0x1012_0000	0x1012_FFFF	USB 2.0 host EHCI register	64 KB	
0x1013_0000	0x1013_FFFF	USB 2.0 device register	64 KB	
0x1014_0000	0x1014_FFFF	Reserved	64 KB	
0x1015_0000	0x1015_FFFF	Reserved	64 KB	
0x1016_0000	0x1016_FFFF	Reserved	64 KB	
0x1017_0000	0x1017_FFFF	Reserved	64 KB	
0x1018_0000	0x1018_FFFF	USB 3.0 register	64 KB	
0x1019_0000	0x1019_FFFF	Reserved	-	
0x101A_0000	0x101A_FFFF	Reserved	64 KB	
0x101B_0000	0x101B_FFFF	Reserved	64 KB	
0x101C_0000	0x101D_FFFF	Reserved	128 KB	
0x101E_0000	0x101F_FFFF	Reserved	128 KB	

Start Address	End Address	Function	Size	Description
0x1020_0000	0x1020_FFFF	Reserved	64 KB	
0x1021_0000	0x102F_FFFF	Reserved	-	
0x1030_0000	0x1030_FFFF	GIC register	64 KB	
0x1031_0000	0x103F_FFFF	Reserved	64 KB	
0x1040_0000	0x1051_FFFF	Reserved	1088 KB	
0x1060_0000	0x106F_FFFF	Reserved	-	
0x1070_0000	0x1070_FFFF	Reserved	64 KB	
0x1071_0000	0x10FF_FFFF	Reserved	-	
0x1100_0000	0x1100_FFFF	VDP register	64 KB	
0x1101_0000	0x1101_FFFF	Reserved	64 KB	
0x1102_0000	0x1102_FFFF	Reserved	64 KB	
0x1103_0000	0x1103_FFFF	Reserved	64 KB	
0x1104_0000	0x1104_FFFF	IVE register	64 KB	
0x1105_0000	0x1105_FFFF	Reserved	64 KB	
0x1107_0000	0x1107_FFFF	Reserved	64 KB	
0x1108_0000	0x1108_FFFF	AIAO register	64 KB	
0x1109_0000	0x1109_FFFF	Reserved	64 KB	
0x110A_0000	0x110A_FFFF	Reserved	64 KB	
0x110B_0000	0x110B_FFFF	Reserved	64 KB	
0x110C_0000	0x110C_FFFF	GZIP register	64 KB	
0x110D_0000	0x110F_FFFF	Reserved	-	
0x1110_0000	0x1110_FFFF	TDE register	64 KB	
0x1111_0000	0x1111_FFFF	GDC register	64 KB	
0x1112_0000	0x1112_FFFF	VGS register	64 KB	
0x1113_0000	0x1117_FFFF	Reserved	-	
0x1118_0000	0x1118_FFFF	VPSS register	64 KB	
0x1119_0000	0x1119_FFFF	Reserved	64 KB	
0x111A_0000	0x111A_FFFF	Reserved	64 KB	
0x111B_0000	0x111B_FFFF	Reserved	64 KB	
0x111C_0000	0x111F_FFFF	Reserved	-	
0x1120_0000	0x1120_FFFF	JPGE register	64 KB	

Start Address	End Address	Function	Size	Description
0x1121_0000	0x1121_FFFF	Reserved	64 KB	
0x1122_0000	0x1123_FFFF	Reserved	-	
0x1124_0000	0x1124_FFFF	Reserved	64 KB	
0x1125_0000	0x1125_FFFF	Reserved	64 KB	
0x1126_0000	0x1126_FFFF	Reserved	64 KB	
0x1127_0000	0x1127_FFFF	Reserved	64 KB	
0x1128_0000	0x1128_FFFF	VEDU register	64 KB	
0x1129_0000	0x1129_FFFF	Reserved	64 KB	
0x112A_0000	0x112A_FFFF	Reserved	64 KB	
0x112B_0000	0x112B_FFFF	Reserved	64 KB	
0x112C_0000	0x112F_FFFF	Reserved	64 KB	
0x1130_0000	0x1130_FFFF	MIPI register	64 KB	
0x1131_0000	0x1137_FFFF	Reserved	-	
0x1138_0000	0x113E_FFFF	VICAP register	448 KB	
0x113F_0000	0x1147_FFFF	Reserved	-	
0x1148_0000	0x114E_FFFF	Reserved	448 KB	
0x114F_0000	0x11FF_FFFF	Reserved	-	
0x1200_0000	0x1200_0FFF	Timer0/Timer1 register	4 KB	
0x1200_1000	0x1200_1FFF	Timer2/Timer3 register	4 KB	
0x1200_2000	0x1200_2FFF	Timer4/Timer5 register	4 KB	
0x1200_3000	0x1200_3FFF	Reserved	4 KB	
0x1200_4000	0x1200_FFFF	Reserved	48 KB	
0x1201_0000	0x1201_FFFF	CRG register	64 KB	
0x1202_0000	0x1202_FFFF	SYSCTRL register	64 KB	
0x1203_0000	0x1203_FFFF	MISC register	64 KB	
0x1204_0000	0x1204_07FF	I/O MUX configuration register	2 KB	Multiplexing relationship
0x1204_0800	0x1204_FFFF	I/O CTRL configuration register	62 KB	Drive current
0x1205_0000	0x1205_0FFF	DDRT register	4 KB	
0x1205_1000	0x1205_1FFF	Reserved	60 KB	
0x1206_0000	0x1206_FFFF	MDDRC/DDR PHY register	64 KB	

Start Address	End Address	Function	Size	Description
0x1207_0000	0x1207_07FF	Reserved	2 KB	
0x1207_0800	0x1207_FFFF	Cipher hash key control register	62 KB	
0x1208_0000	0x1208_FFFF	WDG register	64 KB	
0x1209_0000	0x1209_FFFF	RTC register	64 KB	
0x120A_0000	0x120A_FFFF	PMC register	64 KB	
0x120B_0000	0x120B_FFFF	RSA register	64 KB	
0x120C_0000	0x120C_FFFF	TRNG register	64 KB	
0x120D_0000	0x120D_FFFF	SYSCNT register	64 KB	
0x120E_0000	0x120E_FFFF	SAR_ADC register	64 KB	
0x120F_0000	0x120F_FFFF	IR register	64 KB	
0x1210_0000	0x1210_0FFF	UART0 register	4 KB	
0x1210_1000	0x1210_1FFF	UART1 register	4 KB	
0x1210_2000	0x1210_2FFF	UART2 register	4 KB	
0x1210_3000	0x1210_3FFF	UART3 register	4 KB	
0x1210_4000	0x1210_4FFF	UART4 register	4 KB	
0x1210_5000	0x1210_FFFF	Reserved	44 KB	
0x1211_0000	0x1211_0FFF	I^2C0 register	4 KB	
0x1211_1000	0x1211_1FFF	I^2C1 register	4 KB	
0x1211_2000	0x1211_2FFF	I^2C2 register	4 KB	
0x1211_3000	0x1211_3FFF	I^2C3 register	4 KB	
0x1211_4000	0x1211_4FFF	Reserved	4 KB	
0x1211_5000	0x1211_FFFF	Reserved	44 KB	
0x1212_0000	0x1212_0FFF	SSP0 register	4 KB	
0x1212_1000	0x1212_1FFF	SSP1 register	4 KB	
0x1212_2000	0x1212_2FFF	SSP2 register	4 KB	
0x1212_3000	0x1212_3FFF	Reserved	4 KB	
0x1212_4000	0x1212_4FFF	SPI 3-wire register	4 KB	
0x1212_5000	0x1212_5FFF	Reserved	4 KB	
0x1212_6000	0x1212_FFFF	Reserved	40 KB	
0x1213_0000	0x1213_FFFF	PWM register	64 KB	
0x1214_0000	0x1214_0FFF	GPIO0 register	4 KB	

Start Address	End Address	Function	Size	Description
0x1214_1000	0x1214_1FFF	GPIO1 register	4 KB	
0x1214_2000	0x1214_2FFF	GPIO2 register	4 KB	
0x1214_3000	0x1214_3FFF	GPIO3 register	4 KB	
0x1214_4000	0x1214_4FFF	GPIO4 register	4 KB	
0x1214_5000	0x1214_5FFF	GPIO5 register	4 KB	
0x1214_6000	0x1214_6FFF	GPIO6 register	4 KB	
0x1214_7000	0x1214_7FFF	GPIO7 register	4 KB	
0x1214_8000	0x1214_8FFF	GPIO8 register	4 KB	
0x1214_9000	0x1214_9FFF	GPIO9 register	4 KB	
0x1214_A000	0x1214_AFFF	GPIO10 register	4 KB	
0x1214_B000	0x1214_BFFF	GPIO11 register	4 KB	
0x1214_C000	0x1214_CFFF	GPIO12 register	4 KB	
0x1214_D000	0x1214_DFFF	GPIO13 register	4 KB	
0x1214_E000	0x1214_EFFF	GPIO14 register	4 KB	
0x1214_F000	0x1214_FFFF	Reserved	4 KB	
0x1215_0000	0x1215_FFFF	Reserved	64 KB	
0x1216_0000	0x1216_FFFF	PCIe register	64 KB	
0x1217_0000	0x1217_FFFF	Reserved	64 KB	
0x1218_0000	0x12FF_FFFF	Reserved	-	
0x1300_0000	0x13FF_FFFF	Reserved	-	
0x1400_0000	0x14FF_FFFF	FMC storage address space	16 MB	
0x1500_0000	0x1EFF_FFFF	Reserved	-	
0x1F00_0000	0x1FFF_FFFF	CCI register	1 MB	
0x2000_0000	0x27FF_FFFF	PCIe configuration space	128 MB	
0x2800_0000	0x2FFF_FFFF	PCIe memory space	128 MB	
0x3000_0000	0x37FF_FFFF	Reserved	128 MB	
0x3800_0000	0x3FFF_FFFF	Reserved	128 MB	
0x8000_0000	0xFFFF_FFFF	DDR address space	2 GB	

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

Hi3519 V100 uses the thin & fine-pitch ball grid array (TFBGA) package. It has 389 pins, its body size is 15 mm x 15 mm (0.59 in. x 0.59 in.), and its ball pitch is 0.65 mm (0.026 in.). Figure 2-1 to Figure 2-4 show the package of Hi3519 V100. Figure 2-5 shows the package dimensions.

Figure 2-1 Top view

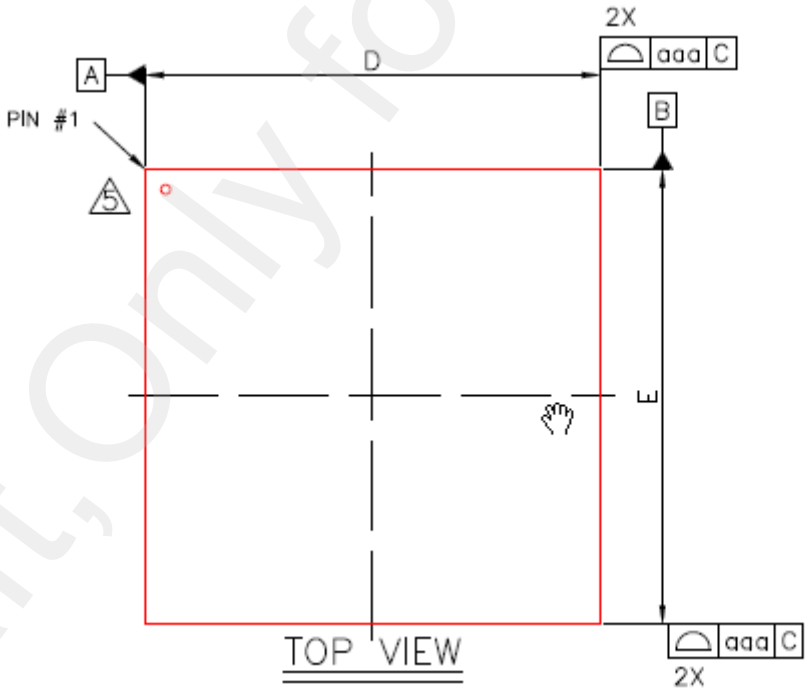


Figure 2-2 Bottom view

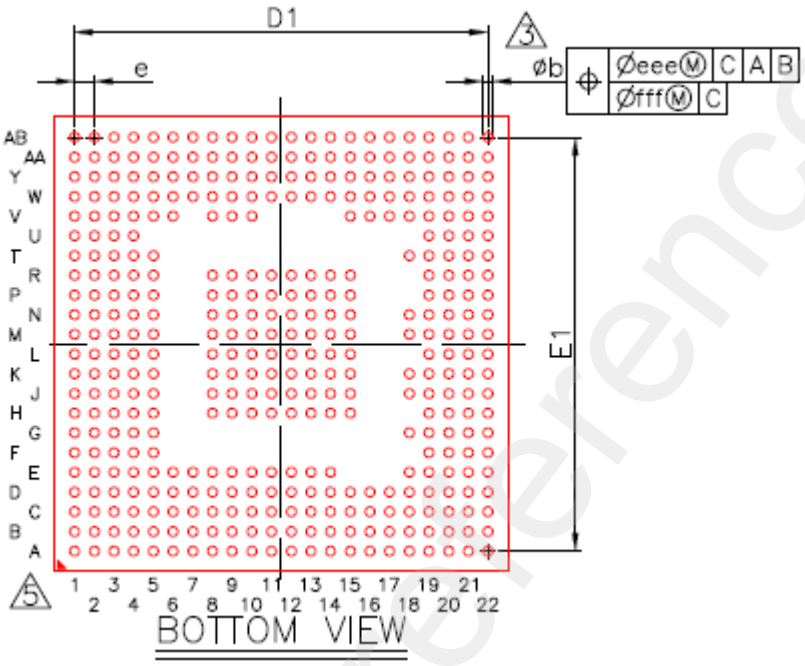


Figure 2-3 Side view

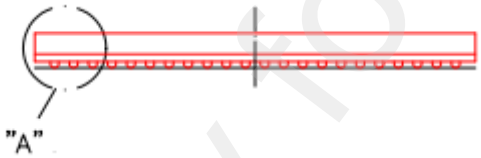


Figure 2-4 Enlarged view of detail "A"

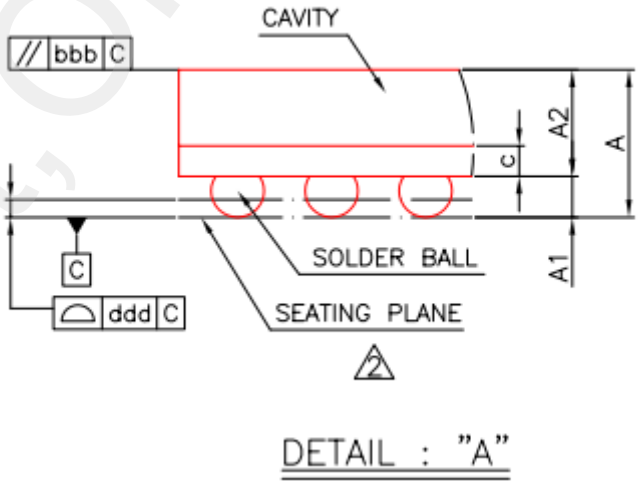


Figure 2-5 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	13.65	---	---	0.537	---
E1	---	13.65	---	---	0.537	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	22/22					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

2.1.2 Pinout

Table 2-1 lists the pin quantity of the Hi3519 V100 by type.

Table 2-1 Pin quantity

Pin Type	Quantity
I/O	240
Digital power	32
Digital GND	66
Others/Analog power	14
Others/Analog GND	25
DDR reference power	12

Pin Type	Quantity
Total	389

2.2 Pin Description

For details about the pins, see the *HI3519V100_PINOUT_EN*.

2.3 Electrical Specifications

2.3.1 Power Consumption Parameters

Table 2-2 describes power consumption parameters.

CAUTION

- The values of power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3519 V100 Hardware Design User Guide*.

Table 2-2 Power consumption parameters

Parameter	Description	Typ	Max	Unit
Core power	Core power current	-	-	mA
IO power	IO power current	-	-	mA

NOTE

The typical application scenario of Hi3519 V100 is as follows: A7@800 MHz+4K x 2K@30 ISP processing+3DNR+one-channel VGS/GDC (only one of the rotation, scaling, fisheye correction, and LDC functions is selected)+(4K x 2K@30 fps+720p@30 fps) dual-stream H.264/H.265 encoding.

2.3.2 Temperature and Thermal Resistance Parameters

Table 2-3 describes temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3519 V100 Hardware Design User Guide*.

- You are advised to store products at a temperature lower than 30°C (86°F) and at most 60% relative humidity (RH).
- The soldering temperature curve is based on the JSTD020 standard.

Table 2-3 Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	0	-	70	℃
Rated temperature	T_{JMAX}	–20	-	125	℃
Junction-to-ambient thermal resistance	θ_{JA}	-	24	-	℃/W
Junction-to-board thermal resistance	θ_{JB}	-	12.2	-	℃/W
Junction-to-case thermal resistance	θ_{JC}	-	6.2	-	℃/W

2.3.3 Operating Conditions

Table 2-4 describes operating conditions.

Table 2-4 Operating conditions

Symbol	Description	Min	Typ	Max	Unit
VDD	Internal core power	TBD	0.9	TBD	V
VDD_CPU	CPU core power	TBD	0.9	TBD	V
VDD_MEDIA	MEDIA core power	TBD	0.9	TBD	V
VDD_DDR	DDR3/DDR3L/DDR4 interface power	1.425/1.323/1.2	1.5/1.35/1.2	1.575/1.425/1.26	V
DVDD33	I/O power	2.97	3.3	3.63	V
DVDD3318_SENS0	Sensor 0 I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_UART1	UART1 I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_EMMC	eMMC I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD18_SDIO	SDIO 1.8 V I/O power	1.62	1.8	1.98	V
DVDDIO_RGMII	RGMII interface power	2.97/1.62	3.3/1.8	3.63/1.98	V

Symbol	Description	Min	Typ	Max	Unit
VDDIO_DDR	DDR3 /DDR3L/DDR4 interface power	1.425/1.323/1.2	1.5/1.35/1.2	1.575/1.425/1.26	V
VDDIO_CK_DDR	DDR3 /DDR3L/DDR4 clock interface power	1.425/1.323/1.2	1.5/1.35/1.2	1.575/1.425/1.26	V
AVDD_DDRPLL1 AVDD_DDRPLL2	3.3 V DDR3/DDR3L/DDR4 PLL analog power	3.125	3.3	3.6	V
AVDD_PLL	PLL core analog power	TBD	0.9	TBD	V
AVDD33_PLL	3.3 V PLL analog power	2.97	3.3	3.63	V
AVDD33_USB2	3.3 V USB 2.0 analog power	3.0	3.3	3.6	V
AVDD3318_MIPI	Mobile industry processor interface (MIPI) analog power	1.71	1.8	1.89	V
	3.3 V power when the MIPI signal is multiplexed as a single-ended signal	2.97	3.3	3.63	V
AVDD_U3_PCIE	USB 3.0/PCIe core analog power	TBD	0.9	TBD	V
AVDD33_U3_PCIE	3.3 V USB 3.0/PCIe analog power	3.0	3.3	3.6	V
AVDD33_AC	3.3 V audio CODEC analog power	2.97	3.3	3.63	V
AVDD33_VDAC	3.3 V VDAC analog power	2.97	3.3	3.63	V
AVDD_BAT	RTC battery power	1.6	3.3	3.6	V
AVDD33_RTC	RTC analog power	1.6	3.3	3.6	V

2.3.4 Power-On and Power-Off Sequences

To avoid large currents for I/O pins during power-on, it is required that DVDD33, DVDDIO_DDR, and DVDD_CORE be powered on in sequence (the four core power supplies VDD, VDD_CPU, VDD_MEDIA, and VDD_DDR must be turned on simultaneously). The power-off sequence is in the reverse order of the power-on sequence.

2.3.5 DC and AC Electrical Parameters

Table 2-5 describe DC electrical parameters.

Table 2-5 DC electrical parameters (DVDD3318_SENS0/DVDD3318_UART1/DVDD3318_EMMC/DVDDIO_RGMII/DVDD33 = 3.3 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD33	Interface voltage	2.97	3.3	3.63	V	-
V_{IH}	High-level input voltage	2.0	-	DVDD33 + 0.3	V	Incompatible with the 5 V input
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up resistor	34	44	58	kΩ	-
R_{PD}	Internal pull-down resistor	31	40	55	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	6.7	8.54	10.54	kΩ	
R_{PD8k}	8 kΩ pull-down resistor	6.53	8.32	10.38	kΩ	

Table 2-6 DC electrical parameters (DVDD3318_SENS0/DVDD3318_UART1/DVDD3318_EMMC/DVDD18_SDIO/DVDDIO_RGMII = 1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD18	Interface voltage	1.62	1.8	1.98	V	-
V_{IH}	High-level input voltage	1.17	-	DVDD 18 + 0.3	V	-
V_{IL}	Low-level input voltage	–0.3	-	0.63	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	1.35	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU}	Internal pull-up resistor	45	64	92	kΩ	-
R_{PD}	Internal pull-down resistor	41	56	93	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	6.76	8.68	10.84	kΩ	-
R_{PD8k}	8 kΩ pull-down resistor	6.49	8.34	10.43	kΩ	-

Table 2-7 describes DC electrical parameters in DDR3 mode.

Table 2-7 DC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V, DDR3 mode)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V	-
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-	(0.49 to 0.51) x DDR_DVDDIO
VTT	Termination voltage	Vref – 40 mV	Vref	Vref + 40 mV	mV	-
$V_{IH(DC)}$	High-level input voltage	Vref + 0.1	-	VDDIO_DDR + 0.3	V	-
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	Vref − 0.1	V	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	-	(1 + 0.1) x VDDIO_DDR	V	The drive impedance is configurable.
V_{OL}	Low-level output voltage	0	-	0.2 x VDDIO_DDR	V	The drive impedance is configurable.
I_{OH}	High-level output current	-	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
I_{OL}	Low-level output current	-	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
Output impedance	-	34	-	80	Ω	-

Table 2-8 describes AC electrical parameters in DDR3 mode.

Table 2-8 AC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V, DDR3 mode)

Symbol	Description	Min	Max	Unit	Remarks
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR + 0.3	V	-
$V_{IL(AC)}$	Low-level input voltage	-	Vref − 0.15	V	-

Table 2-9 describes DC electrical parameters in DDR3L mode.

Table 2-9 DC electrical parameters in DDR3L mode (VDDIO_DDR =1.35 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.283	1.35	1.45	V	-
VREF	Reference voltage of the DDR interface	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	
VTT	Termination voltage	0.49 x VDDQ − 40	0.5 x VDDQ	0.51 x VDDQ + 40	mV	-
VIH(DC)	High-level input voltage	0.49 x VDDQ + 0.125	-	VDDQ + 0.3	V	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
VIL(DC)	Low-level input voltage	−0.3	-	0.51 x VDDQ − 0.125	V	-
VOH	High-level output voltage	VDDQ − 0.28	-	-	V	-
VOL	Low-level output voltage	-	-	VDDQ + 0.28	V	-
IOH	High-level output current	-	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
IOL	Low-level output current	-	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.

Table 2-10 describes AC electrical parameters in DDR3L mode.

Table 2-10 AC electrical parameters in DDR3L mode (VDDIO_DDR = 1.35 V)

Symbol	Description	533−1600 Mbit/s		Unit	Remarks
		Min	Max		
VIH (AC)	AC High-level input voltage	0.49 x VDDQ + 0.25	-	V	-
VIL (AC)	AC Low-level input voltage	-	0.51 x VDDQ − 0.25	V	-

Table 2-11 describes the AC and DC electrical parameters for the data lines in DDR4 mode.

Table 2-11 AC and DC electrical parameters for the data lines (VDDIO_DDR = 1.2 V, DDR4 mode)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.2	1.2	1.26	V	-
Vref	Reference voltage	0.4 x VDDIO_DDR	0.5 x VDDIO_DDR	0.8 x VDDIO_DDR	-	(0.4−0.8) x DDR_DVDDIO

Symbol	Description	Min	Typ	Max	Unit	Remarks
VOH (DC)	High-level output voltage	-	1.1 x VDDIO_DDR	-	V	The drive impedance is configurable.
VOL (DC)	Low-level output voltage	-	0.5 x VDDIO_DDR	-	V	The drive impedance is configurable.
VOH (AC)	High-level output voltage	-	0.85 x VDDIO_DDR	-	V	The drive impedance is configurable.
VOL (AC)	Low-level output voltage	-	0.55 x VDDIO_DDR	-	V	The drive impedance is configurable.
Output impedance	-	34	-	240	Ω	-

Table 2-12 describes the AC and DC electrical parameters for the address/command lines in DDR4 mode.

Table 2-12 AC and DC electrical parameters for the address/command lines (VDDIO_DDR = 1.2 V, DDR4 mode)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.2	1.2	1.26	V	-
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-	(0.49−0.51) x DDR_DVDDIO
VIH (DC75)	High-level input voltage	Vref + 0.075	-	VDDIO_DDR	V	-
VIL (DC75)	Low-level input voltage	0	-	Vref − 0.075	V	-
VIH (AC100)	High-level input voltage	Vref + 0.1	-	VDDIO_DDR	V	-
VIL (AC100)	Low-level input voltage	0	-	Vref − 0.1	V	-
VOH (DC)	High-level output voltage	-	1.1 x VDDIO_DDR	-	V	The drive impedance is configurable.
VOL (DC)	Low-level output voltage	-	0.5 x VDDIO_DDR	-	V	The drive impedance is configurable.

Symbol	Description	Min	Typ	Max	Unit	Remarks
VOH (AC)	High-level output voltage	-	0.85 x VDDIO_DDR	-	V	The drive impedance is configurable.
VOL (AC)	Low-level output voltage	-	0.55 x VDDIO_DDR	-	V	The drive impedance is configurable.
Output impedance	-	34	-	240	Ω	-

2.3.6 MIPI/LVDS RX Electrical Parameters

Table 2-13 describes low-voltage differential signaling (LVDS) differential DC electrical parameters.

Table 2-13 LVDS differential DC electrical parameters

Symbol	Description		Min	Typ	Max	Unit
VIDTH (SL)	Differential input threshold voltage (VP − VM)/2(MIN)	Sub-LVDS	-	-	±25	mV
VIDTH (HS)		HiSPi	-	-	±25	
VIDTH (DP)		D-PHY HS	-	-	±70	
VIDTH (LV)		LVDS	-	-	±100	
VIDTH (ML)		Mini-LVDS	-	-	±100	
VCM (SL)	Common mode voltage range (VP + VM)/2	Sub-LVDS	0.5	0.9	1.3	V
VCM (HS)		HiSPi	0.135	0.2	0.275	
VCM (DP)		D-PHY HS	0.07	0.2	0.33	
VCM (LV)		LVDS	0.925	1.2	1.475	
VCM (ML)		Mini-LVDS	1.025	1.2	1.375	
VISVR (SL)	Single-ended input voltage range VP, VM	Sub-LVDS	0.4	-	1.4	V
VCM (HS)		HiSPi	−0.165	-	0.575	
VCM (DP)		D-PHY HS	−0.04	-	0.46	
VCM (LV)		LVDS	0	-	1.8	
VCM (ML)		Mini-LVDS	0.825	-	1.575	
ZID (SL)	Internal termination resister value	Sub-LVDS	80	100	120	Ω
ZID (HS)		HiSPi			125	
ZID (LV)		LVDS			120	

Symbol	Description		Min	Typ	Max	Unit
ZID (ML)		Mini-LVDS			120	
ZID (DP)		D-PHY HS			125	

Table 2-14 to Table 2-16 describe the MIPI parameters.

Table 2-14 MIPI high-speed (HS) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VTERM-EN	Single-ended threshold for HS termination enable	-	-	450	mV

Table 2-15 MIPI HS AC parameters

Symbol	Description	Min	Typ	Max	Unit
ΔVCMRX (HF)	Common-mode interface beyond 450 MHz	-	-	100	-
ΔVCMRX (LF)	Common-mode interface 50 MHz−450 MHz	-50	-	50	mV
CCM	Common-mode termination	-	-	60	pF

Table 2-16 MIPI low-power (LP) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VIHLP	Logic 1 input voltage	880	-	-	mV
VILLP	Logic 0 input voltage	-	-	550	
VHYST	Input hysteresis	25	-	-	

2.3.7 SDIO Electrical Parameters

Table 2-17 describes the SDIO electrical parameters (3.3 V).

Table 2-17 SDIO electrical parameters (3.3 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDD	Power voltage	2.7	-	3.6	V	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
VOH	High-level output	0.75 x VDD	-	-	V	
VOL	Low-level output	-	-	0.125 x VDD	V	
VIH	High-level input	0.625 x VDD	-	VDD + 0.3	V	
VIL	Low-level input	Vss − 0.3	-	0.25 x VDD	V	
-	Power-on time	-	-	250	ms	0 V to VDD

Table 2-18 describes the SDIO electrical parameters (1.8 V).

Table 2-18 SDIO electrical parameters (1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDD	Power voltage	2.7	-	3.6	V	-
VDDIO	I/O voltage	1.70	-	1.95	V	
VOH	High-level output	1.4	-	-	V	
VOL	Low-level output	-	-	0.45	V	
VIH	High-level input	1.27	-	2.00	V	
VIL	Low-level input	Vss – 0.3	-	0.58	V	
-	Power-on time	-	-	250	ms	0 V to VDD

2.3.8 Audio CODEC Electrical Parameters

Table 2-19 to Table 2-22 describe the electrical parameters of the audio CODEC.

Table 2-19 Overall specifications

Description	Min	Typ	Max	Unit	Remarks
Analog circuit power AVDD	3	3.3	3.6	V	Relative to AGND

Description	Min	Typ	Max	Unit	Remarks
VREF	-	AVDD/2		V	Relative to AGND

Table 2-20 Major DAC specifications

Description	Min	Typ	Max	Unit	Remarks
Output amplitude at full scale	-	0.875	-	Vrms	Maximum output signal swing
SNR	-	76	-	dBA	Fin = 1 kHz, Fs = 48 kHz, −20 dBFS
	-	96	-		The signal amplitude is tested at full scale, and the noise level is tested at −60 dBFS.
PSRR	-	30	-	dB	20 Hz to 200 Hz
	-	40	-		200 kHz to 20 kHz

Table 2-21 Major ADC specifications

Description	Min	Typ	Max	Unit	Remarks
Maximum input amplitude	-	1	-	Vrms	Maximum input signal swing of the ADC
SNR		73	-	dBA	Fin = 1 kHz, Fs = 48 kHz, −20 dBFS
		93	-		Fin = 1 kHz, Fs = 48 kHz, gain = 0 dB The signal amplitude is tested at full scale, and the noise level is tested when VIN = −60 dBV. Then calculate 20log(Signal amplitude/Noise level).
PSRR	-	30	-	dB	20 Hz to 200 Hz
	-	40	-		200 kHz to 20 kHz

Table 2-22 Major MICBIAS specifications

Description	Min	Typ	Max	Unit	Remarks
Bias voltage	-	2.1 x AVDD/3.3	-	V	MIC bias voltage
Maximum output current	-	-	3	mA	-
PSRR	-	60	-	dB	The 1 kHz 100 mVpp signal is added to the power signal.

2.4 PCB Design Recommendations

For details about printed circuit board (PCB) design recommendations, see the *Hi3519V100 Hardware Design User Guide*.

2.5 Interface Timings

2.5.1 DDR Interface Timings

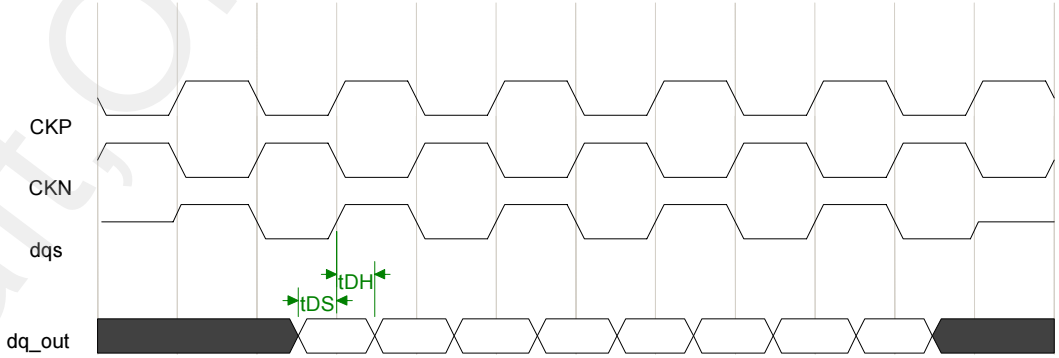
2.5.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH.

Figure 2-6 shows the write timing of dqs_out relative to dq_out for the DDR3/4.

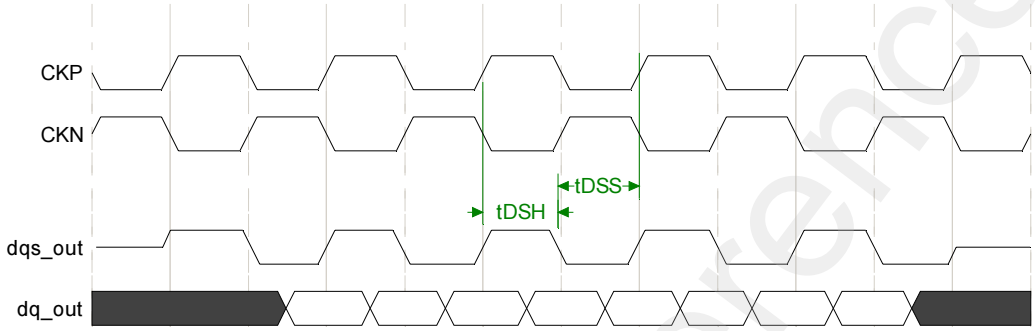
Figure 2-6 Write timing of dqs_out relative to dq_out for the DDR3/4



Write Timings of dqs_out Relative to CK

Figure 2-7 shows the write timing of dqs_out relative to CK for the DDR3/4.

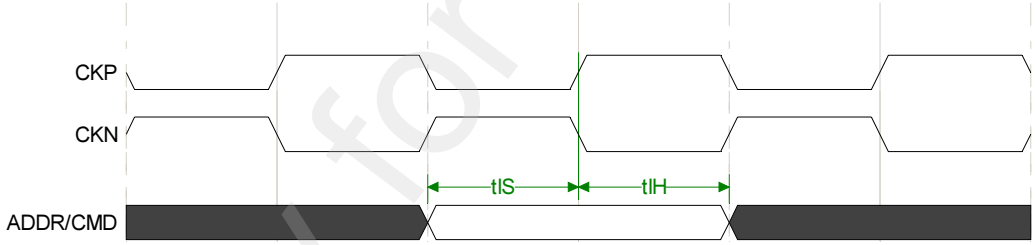
Figure 2-7 Write timing of dqs_out relative to CK for the DDR3/4



Write Timing of CMD/ADDR Relative to CK

Figure 2-8 shows the write timing of CMD/ADDR relative to CK.

Figure 2-8 Write timing of CMD/ADDR relative to CK



2.5.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK."

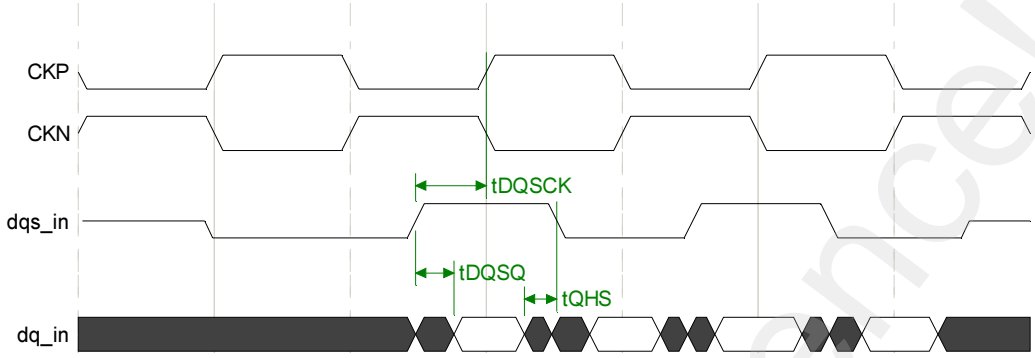
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-9 shows the output timing of the DDRn SDRAM.

Figure 2-9 Output timing of the DDRn SDRAM



2.5.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3519V100 is based on the timing parameters of the DDR3-1600 SDRAMs.

Table 2-23 and Table 2-24 describe the clock parameters of the DDR3-1600 SDRAM.

Table 2-23 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	800.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-24 Parameters for the DDR3-1600 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

Table 2-25 and Table 2-26 describe the clock parameters of the DDR4-2133 SDRAM.

Table 2-25 DDR4 clock parameters

Parameter	Typ	Unit
DDR clock frequency	1066.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	48.000	%
Clock skew	0.100	ns

Table 2-26 Parameters for the DDR4-2133 SDRAM

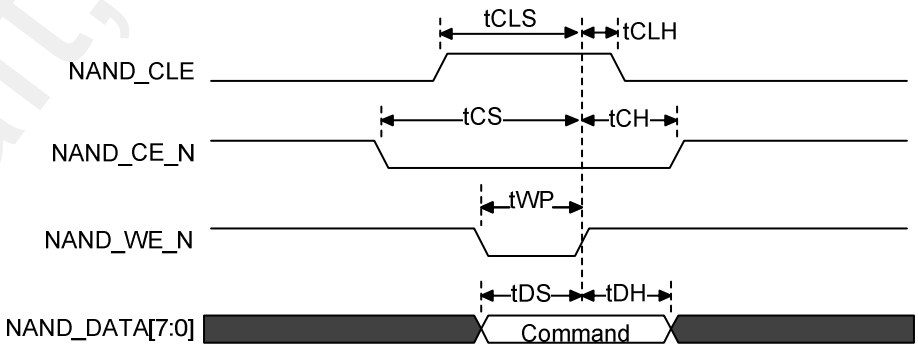
Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.18	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.18	tCK
Setup time, DQ/DM to DQS	tDS	0.068	ns
Hold time, DQ/DM to DQS	tDH	0.050	ns
Skew between DQS and DQ	tDQSQ	0.070	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.108	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.100	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.160	ns

2.5.2 Timings of the NANDC Interface

2.5.2.1 Command Cycle Timing

Figure 2-10 shows the command cycle timing of the NANDC) interface.

Figure 2-10 Command cycle timing of the NANDC interface



NOTE

The level widths of NAND_WE_N and NAND_RE_N can be set by configuring the NF_PULSE_WIDTH register of the NANDC. Therefore, some parameters in the timing diagrams of the NANDC interface vary according to the settings of NF_PULSE_WIDTH. In the following tables, these parameters are marked with "Configurable."

Table 2-27 describes the command cycle timing parameters of the NANDC interface.

Table 2-27 Command cycle timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CLE	tCLS	15	N/A	ns	N/A
Hold time of NAND_CLE	tCLH	10	N/A	ns	Configurable
Setup time of NAND_CE_N	tCS	15	N/A	ns	N/A
Hold time of NAND_CE_N	tCH	10	N/A	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	N/A	ns	Configurable
Data setup time	tDS	10	N/A	ns	Configurable
Data hold time	tDH	10	N/A	ns	Configurable

2.5.2.2 Address Cycle Timing

Figure 2-11 shows the address cycle timing of the NANDC interface.

Figure 2-11 Address cycle timing of the NANDC interface

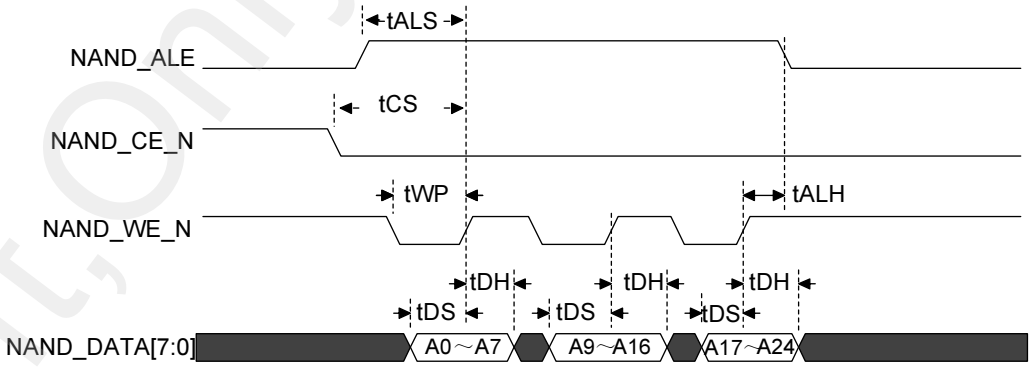


Table 2-28 describes the address cycle timing parameters of the NANDC interface.

Table 2-28 Address cycle timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CE_N	tCS	15	N/A	ns	N/A
Pulse width of NAND_WE_N	tWP	15	N/A	ns	Configurable
Setup time of NAND_ALE	tALS	15	N/A	ns	N/A
Hold time of NAND_ALE	tALH	10	N/A	ns	Configurable
Data setup time	tDS	10	N/A	ns	Configurable
Data hold time	tDH	10	N/A	ns	Configurable

2.5.2.3 Write Data Timing

Figure 2-12 shows the write data timing of the NANDC interface.

Figure 2-12 Write data timing of the NANDC interface

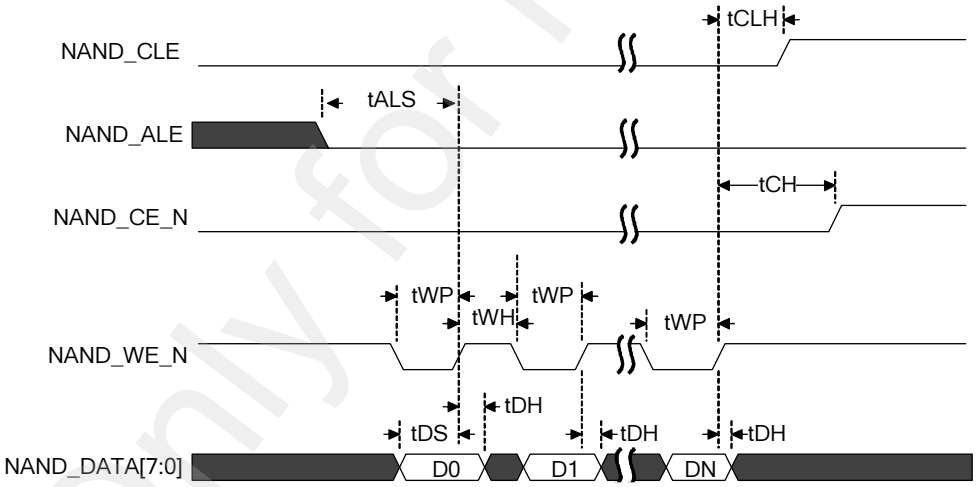


Table 2-29 describes the write data timing parameters of the NANDC interface.

Table 2-29 Write data timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Hold time of NAND_CLE	tCLH	10	N/A	ns	Configurable
Hold time of NAND_CE_N	tCH	10	N/A	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	N/A	ns	Configurable
Setup time of NAND_ALE	tALS	15	N/A	ns	Configurable

Parameter	Symbol	Min	Max	Unit	Remarks
Data setup time	tDS	10	N/A	ns	Configurable
Data hold time	tDH	10	N/A	ns	Configurable
High-level hold time of NAND_WE_N	tWH	15	N/A	ns	Configurable

2.5.2.4 Read Data Timing

Figure 2-13 shows the read data timing of the NANDC interface.

Figure 2-13 Read data timing of the NANDC interface

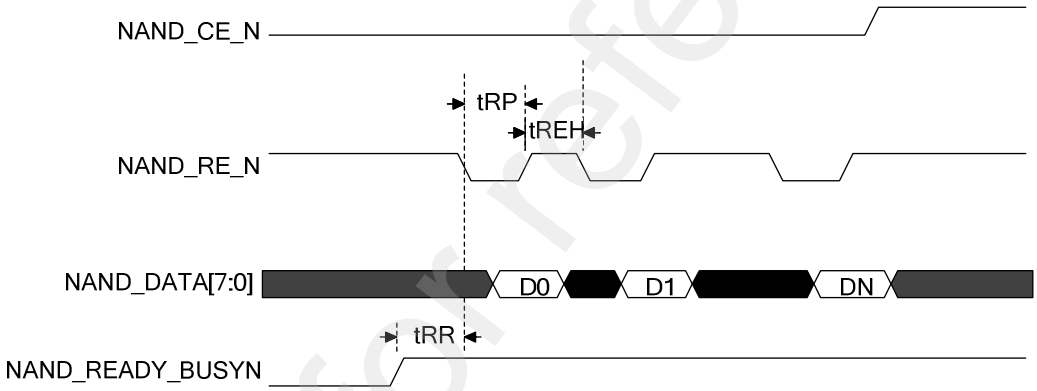


Table 2-30 describes the read data timing parameters of the NANDC interface.

Table 2-30 Read data timing parameters of the NANDC interface

Parameter	Symbol	Min	Max	Unit	Remarks
Low-level wait time of NAND_RE_N	tRR	15	N/A	ns	Configurable
Pulse width of NAND_RE_N	tRP	15	N/A	ns	Configurable
High-level width of NAND_RE_N	tREH	15	N/A	ns	Configurable

NOTE

The tRR delay is configurable.

2.5.3 SFC Interface Timings

Figure 2-14 and Figure 2-15 show the SFC input timings.

Figure 2-14 SFC input timing (SDR mode)

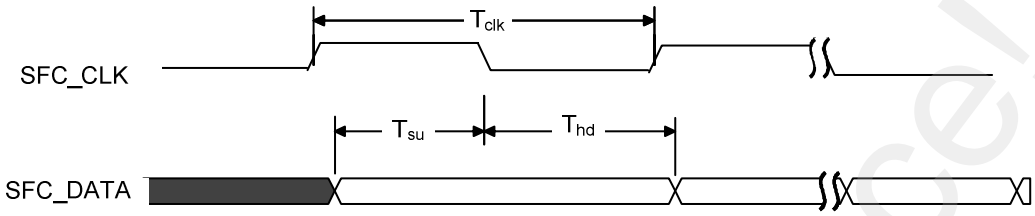


Figure 2-15 SFC input timing (DDR mode)

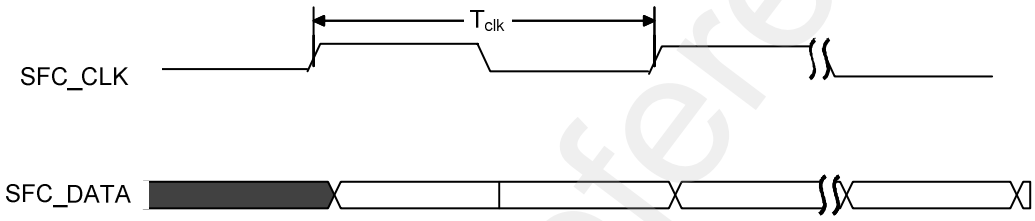


Table 2-31 describes the SFC input timing parameters.

Table 2-31 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK (SDR mode)	T_{clk}	8	N/A	83.2	ns
Clock cycle of SFC_CLK (DDR mode)	T_{clk}	10	-	83.2	ns
Input signal setup time	T_{su}	2	N/A	N/A	ns
Input signal hold time	T_{hd}	0.5	N/A	N/A	ns

Figure 2-16 and Figure 2-17 show the SFC output timings.

Figure 2-16 SFC output timing (SDR mode)

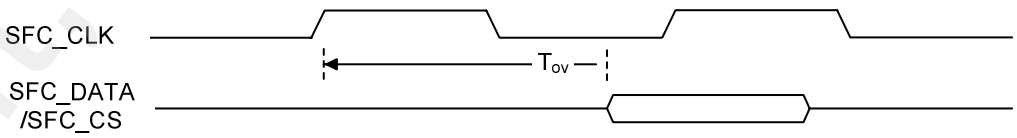


Figure 2-17 SFC output timing (DDR mode)

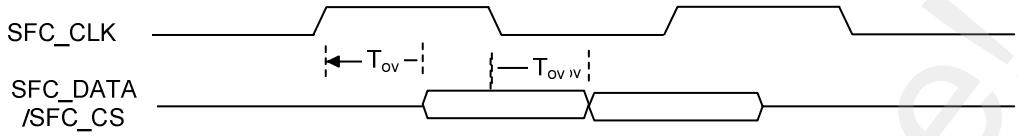


Table 2-32 describes the SFC output timing parameters.

Table 2-32 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK (SDR mode)	T	8	N/A	83.2	ns
Clock cycle of SFCCLK (DDR mode)	T	10	N/A	83.2	ns
Output data signal delay	T_{ov}	5	N/A	T-5	ns
Output CS signal delay	T_{ov}	5	N/A	T-5	ns

2.5.4 Ethernet MAC Port Timings

2.5.4.1 RMII Timings

Figure 2-18 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-18 100 Mbit/s RX timing of the RMII

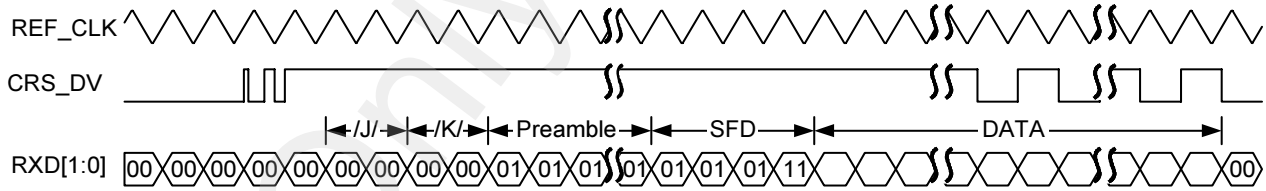


Figure 2-19 shows the 100 Mbit/s TX timing of the RMII.

Figure 2-19 100 Mbit/s TX timing of the RMII

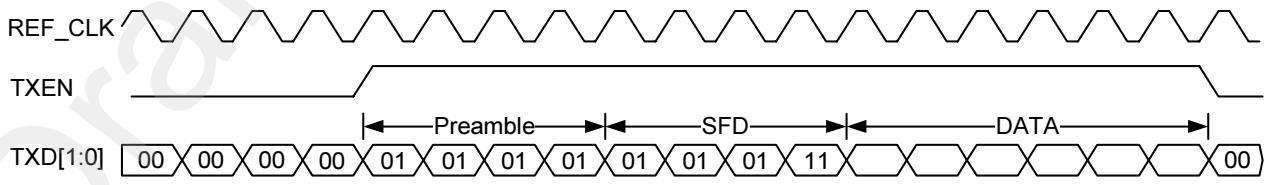


Figure 2-20 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-20 10 Mbit/s RX timing of the RMII

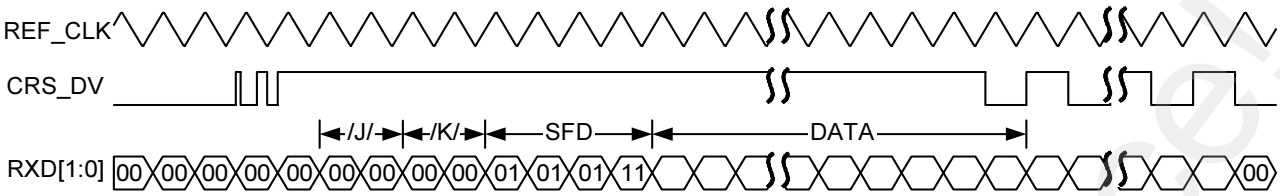


Figure 2-21 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-21 10 Mbit/s TX timing of the RMII

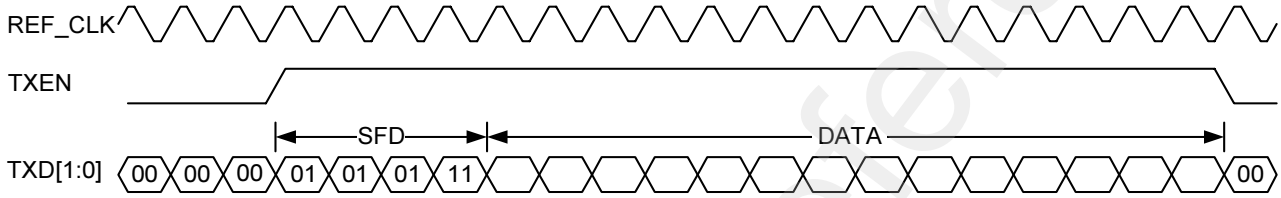


Figure 2-22 illustrates the timing parameters of the RMII.

Figure 2-22 Timing parameters of the RMII

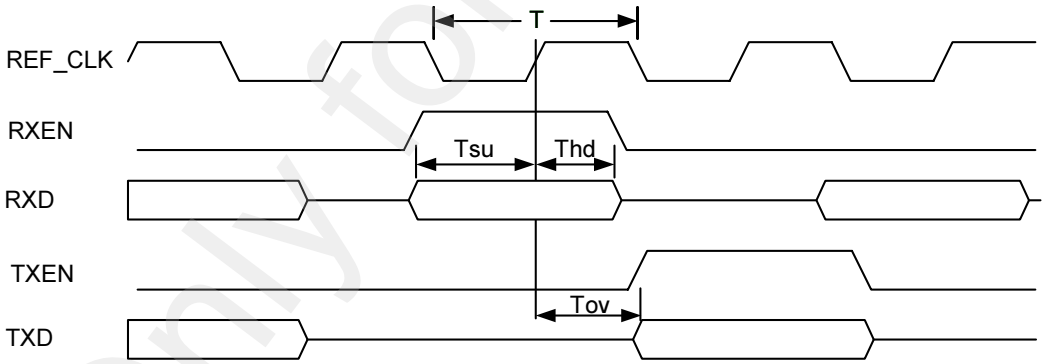


Table 2-33 describes the RMII timing parameters of the RMII.

Table 2-33 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	REF_CLK	20	20	ns
Setup time of RMII signal	Tsu (RX)	CRS_DV/RXD[1:0]	4	N/A	ns
Hold time of RMII signal	Thd (RX)	CRS_DV/RXD[1:0]	2	N/A	ns
RMII output signal delay	Tov (TX)	TXEN/TXD[1:0]	3	16	ns

2.5.4.2 RGMII Timings

Figure 2-23 shows the 1000 Mbit/s RX timing of the RGMII.

Figure 2-23 1000 Mbit/s RX timing of the RGMII

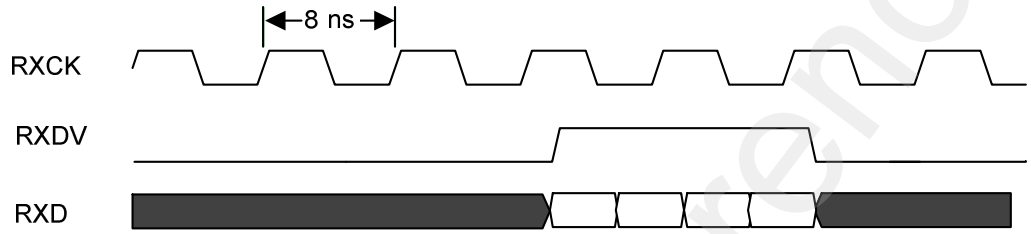


Figure 2-24 shows the 1000 Mbit/s TX timing of the RGMII.

Figure 2-24 1000 Mbit/s TX timing of the RGMII

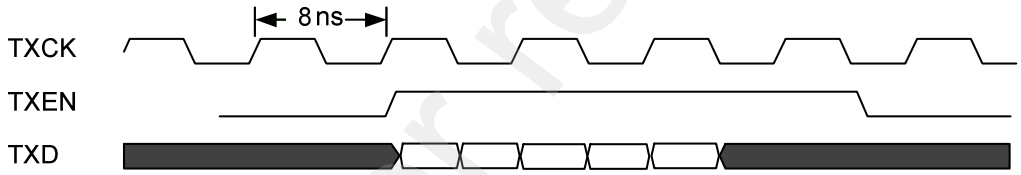


Table 2-34 describes the timing parameters of the RGMII.

Table 2-34 Timing parameters of the RGMII

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	RXCK, TXCK	8	8	ns
RGMII signal setup time	Tsu (RX)	RXER, RXDV, RXD[3:0]	1	N/A	ns
RGMII signal hold time	Thd (RX)	RXER, RXDV, RXD[3:0]	1	N/A	ns
RGMII output signal delay	Tov (TX)	TXD[3:0], TXEN	-0.5	0.5	ns

2.5.4.3 MDIO Interface Timings

Figure 2-25 shows the read timing of the MDIO interface.

Figure 2-25 Read timing of the MDIO interface

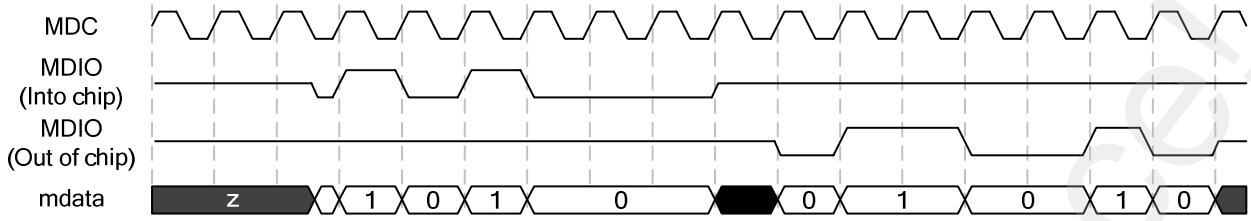


Figure 2-26 shows the write timing of the MDIO interface.

Figure 2-26 Write timing of the MDIO interface

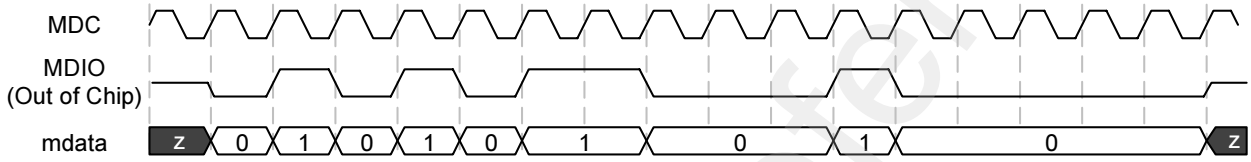


Figure 2-27 illustrates the RX timing parameters of the MDIO interface.

Figure 2-27 RX timing parameters of the MDIO interface

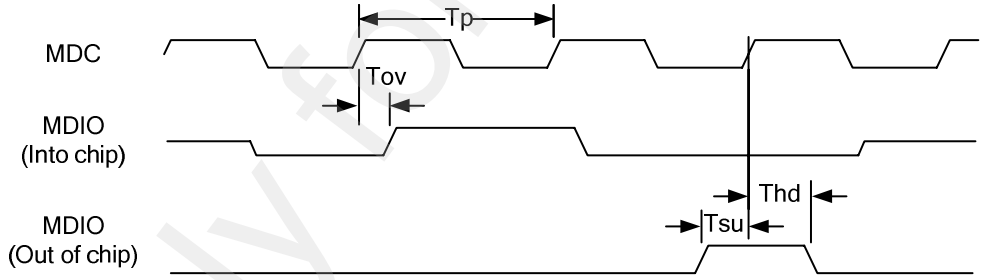


Table 2-35 describes the timing parameters of the MDIO interface.

Table 2-35 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDCK	400	666	ns
MDIO data TX setup time	Tsu	MDIO	10	N/A	ns
MDIO data TX hold time	Thd	MDIO	10	N/A	ns

2.5.5 VI Interface Timing

Figure 2-28 shows the VI interface timing in CMOS mode.

Figure 2-28 VI interface timing in CMOS mode

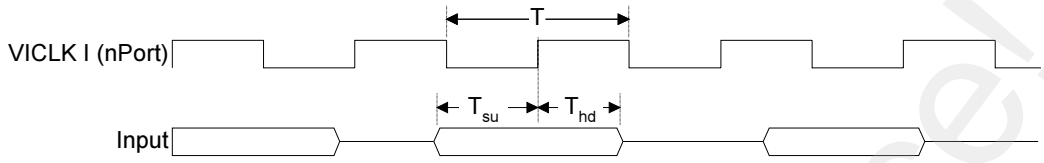


Table 2-36 describes the VI interface timing parameters.

Table 2-36 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	N/A	N/A	ns
Input signal setup time	T_{su}	2.5	N/A	N/A	ns
Input signal hold time	T_{hd}	2.0	N/A	N/A	ns

2.5.6 VO Interface Timings

Figure 2-29 shows the BT.656 interface timing.

Figure 2-29 BT.656 interface timing

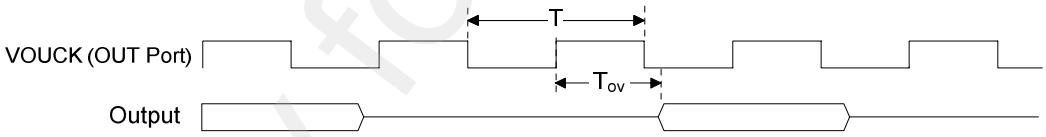


Table 2-37 describes the timing parameters of the BT.656 interface.

Table 2-37 Timing parameters of the BT.656 interface

Parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock cycle	T	13.46	13.48	37	ns
Output signal delay	T_{ov}	T/2-1.5	N/A	T/2+1.5	ns

Figure 2-30 shows the liquid crystal display (LCD) interface timing.

Figure 2-30 LCD interface timing

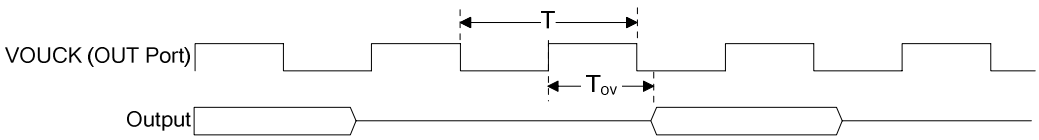


Table 2-38 describes the timing parameters of the LCD interface.

Table 2-38 Timing parameters of the LCD interface

Parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock cycle	T	37	N/A	500	ns
Output signal delay	T_{ov}	T/2 − 1.5	N/A	T/2 + 1.5	ns

2.5.7 AIAO Interface Timings

2.5.7.1 I²S Interface Timing

Figure 2-31 shows the RX timing of the I²S interface.

Figure 2-31 RX timing of the I²S interface

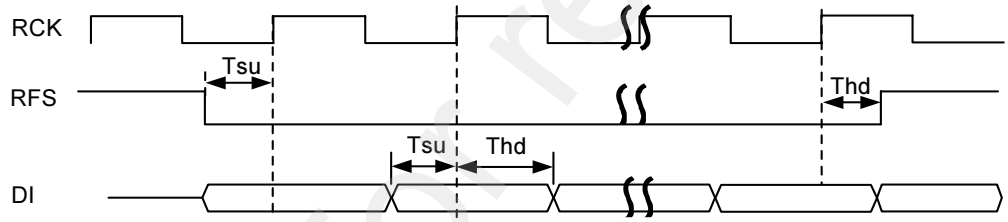


Figure 2-32 shows the TX timing of the I²S interface.

Figure 2-32 TX timing of the I²S interface

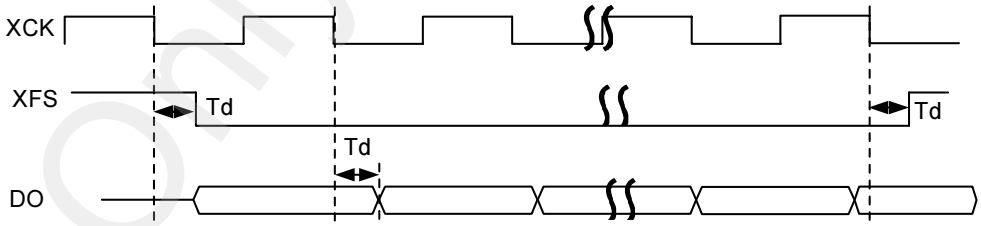


Table 2-39 describes the timing parameters of the I²S interface.

Table 2-39 Timing parameters of the I²S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	N/A	N/A	ns
Input signal hold time	T_{hd}	10	N/A	N/A	ns
Output signal delay	T_d	0	N/A	8	ns

2.5.7.2 PCM Interface Timings

Figure 2-33 shows the RX timing of the PCM interface.

Figure 2-33 RX timing of the PCM interface

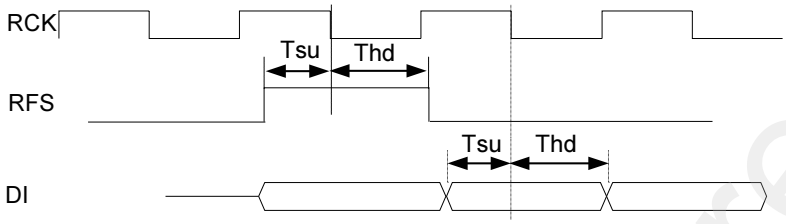


Figure 2-34 shows the TX timing of the PCM interface

Figure 2-34 TX timing of the PCM interface

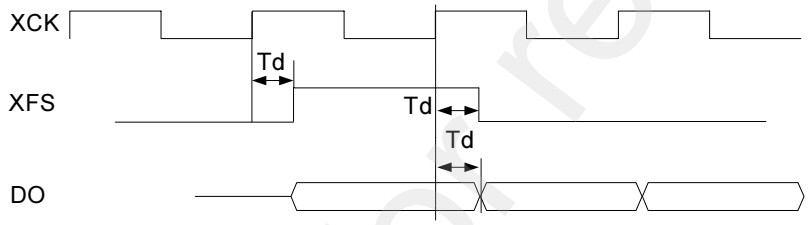


Table 2-40 describes the timing parameters of the PCM interface.

Table 2-40 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	N/A	N/A	ns
Input signal hold time	T_{hd}	10	N/A	N/A	ns
Output signal delay	T_d	0	N/A	8	ns

2.5.8 I²C Interface Timing

Figure 2-35 shows the I²C transfer timing.

Figure 2-35 I^2C transfer timing

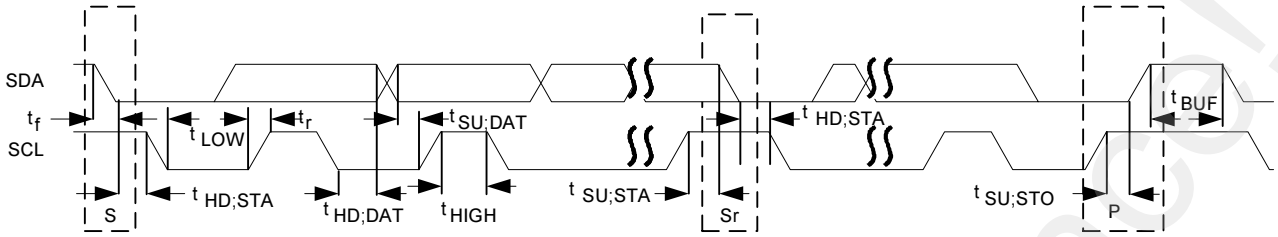


Table 2-41 describes the timing parameters of the I^2C interface.

Table 2-41 Timing parameters of the I^2C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	N/A	0.6	N/A	µs
SCL low-level cycle	t_{LOW}	4.7	N/A	1.3	N/A	µs
SCL high-level cycle	t_{HIGH}	4.0	N/A	0.6	N/A	µs
Start setup time	$t_{SU;STA}$	4.7	N/A	0.6	N/A	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	N/A	100	N/A	ns
Serial data (SDA) and SCL rising time	t_r	N/A	1000	20 + 0.1 x C_b	300	ns
SDA and SCL falling time	t_f	N/A	300	20 + 0.1 x C_b	300	ns
End setup time	$t_{SU;STO}$	4.0	N/A	0.6	N/A	µs
Bus release time from start to end	t_{BUF}	4.7	N/A	1.3	N/A	µs
Bus load	C_b	N/A	400	N/A	400	pF
Low-level noise tolerance	V_{nL}	0.1 x V_{DD}	N/A	0.1 x V_{DD}	N/A	V
High-level noise tolerance	V_{nH}	0.2 x V_{DD}	N/A	0.2 x V_{DD}	N/A	V

2.5.9 SPI Timings

NOTE

In Figure Figure 2-36 to Figure 2-38, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-36 shows the SPI clock (SPICK) timing.

Figure 2-36 SPICK timing

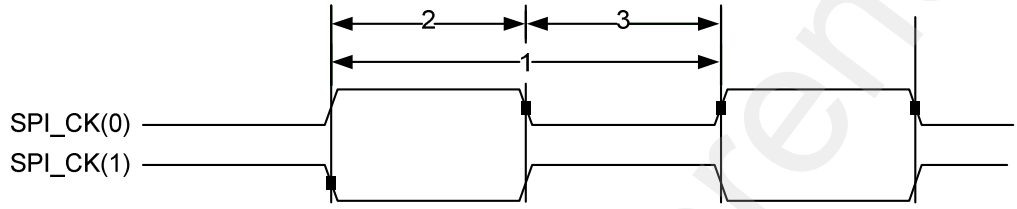


Figure 2-37 and Figure 2-38 show the SPI timings in master mode.

Figure 2-37 SPI timing in master mode (sph = 0)

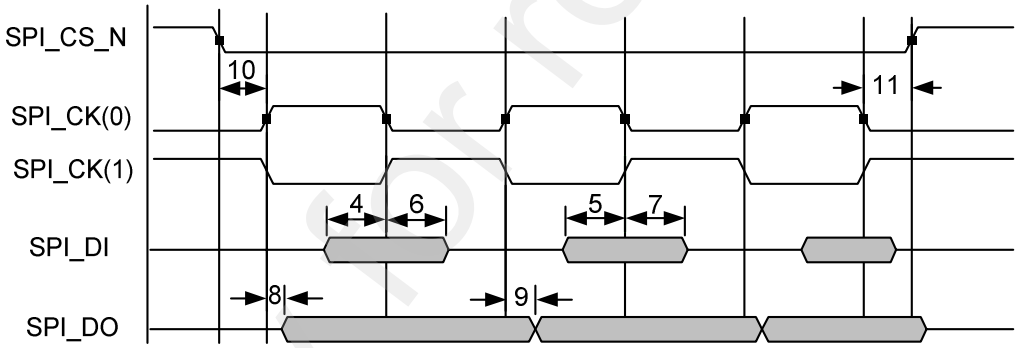


Figure 2-38 SPI timing in master mode (sph = 1)

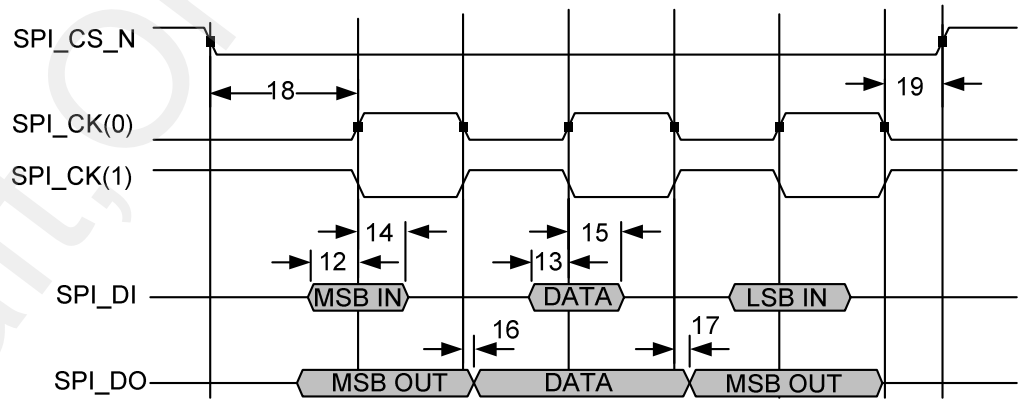


Table 2-42 describes the SPI timing parameters.

Table 2-42 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	N/A	N/A	N/A	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	N/A	N/A	N/A	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	N/A	N/A	N/A	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	N/A	N/A	N/A	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	N/A	N/A	N/A	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	N/A	N/A	N/A	ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	N/A	N/A	N/A	ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	N/A	N/A	N/A	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	N/A	N/A	N/A	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	N/A	N/A	N/A	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	N/A	N/A	N/A	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	N/A	N/A	N/A	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	N/A	N/A	N/A	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	N/A	N/A	N/A	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	N/A	N/A	N/A	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	N/A	N/A	N/A	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	N/A	N/A	N/A	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	N/A	N/A	N/A	ns

No.	Parameter	Symbol	Min	Typ	Max	Unit
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	N/A	N/A	N/A	ns

2.5.10 MIPI RX Timings

Table 2-43 describes the MIPI RX timing parameters.

Table 2-43 MIPI RX timing parameters

Symbol	Description	Min	Tye	Max	Unit
F_{MAX}	Data rate	N/A	N/A	1.5	Gbit/s
T_{PERIOD}	Differential clock cycle	2	T	N/A	ns
T_{DUTY}	Differential clock duty cycle	0.45T	N/A	0.55T	ns
T_{SET}	Differential clock setup time	0.15 x UI	N/A	N/A	ns
T_{HD}	Differential clock hold time	0.15 x UI	N/A	N/A	ns
T_{RISE}	Differential clock rising time (20%−80%)	0.15	N/A	N/A	ns
T_{FALL}	Differential clock falling time (20%−80%)	N/A	N/A	0.3 x UI	ns

NOTE

UI = T/2

2.5.11 SDIO/MMC Interface Timings

Figure 2-39 shows the single-edge data input and output timings of the SDIO/MMC interface.

Figure 2-39 Single-edge data input and output timings of the SDIO/MMC interface

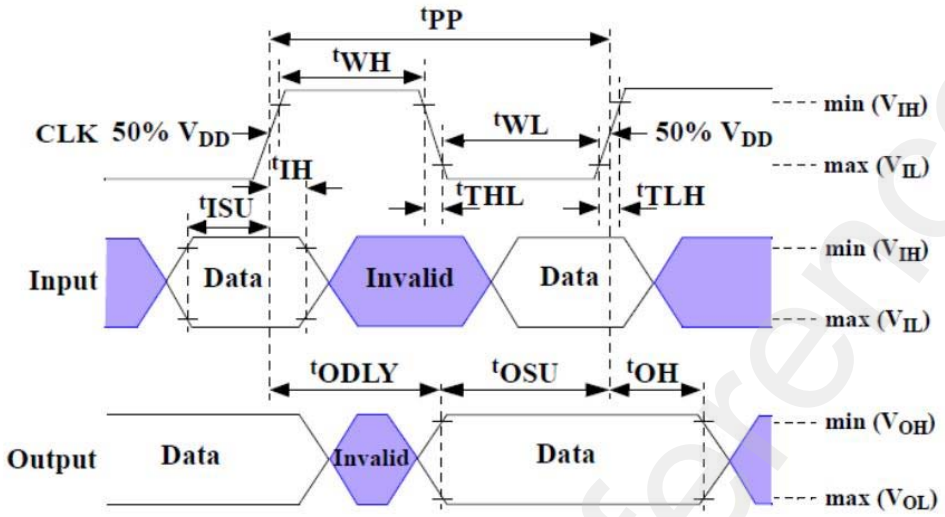


Figure 2-40 shows the dual-edge data input and output timings of the SDIO/MMC interface.

Figure 2-40 Dual-edge data input and output timings of the SDIO/MMC interface

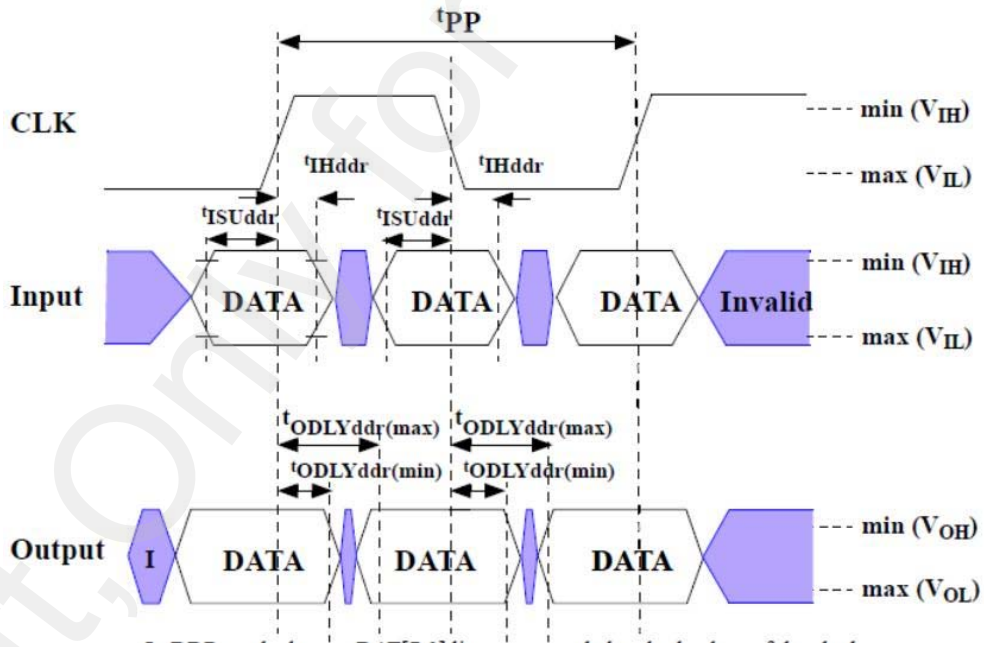


Table 2-44 describes the timing parameters of the SDIO/MMC interface.

Table 2-44 Timing parameters of the SDIO/MMC interface

Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time	Minimum Setup Time	Maximum Output Delay of the Card	High Level Duration of the Card Clock
MMC_HS400	150 MHz	10 ns	0.4 ns	0.4 ns	N/A	(0.45−0.55) clock cycle
MMC_HS200	200 MHz	10 ns	1.4 ns	0.8 ns	N/A	
MMC DDR (CMD line)	50 MHz	20 ns	3.0 ns	3.0 ns	13.7 ns	
MMC DDR (DAT line)	50 MHz	20 ns	2.5 ns	2.5 ns	7.0 ns	
MMC_HS	50 MHz	20 ns	3.0 ns	3.0 ns	13.7 ns	
SD_SDR104	200 MHz	10 ns	0.8 ns	1.4 ns	10.0 ns	
SD_SDR50	100 MHz	10 ns	0.8 ns	3.0 ns	7.5 ns	
SD_DDR50 (CMD line)	50 MHz	20 ns	0.8 ns	6.0 ns	13.7 ns	
SD_DDR50 (DAT line)	50 MHz	20 ns	0.8 ns	3.0 ns	7 ns	
SD_SDR25	50 MHz	20 ns	2.0 ns	6.0 ns	14 ns	
SD_SDR12	25 MHz	40 ns	5.0 ns	5.0 ns	14 ns	
SD_HS	50 MHz	20 ns	2.0 ns	6.0 ns	14 ns	
SD_DS	25 MHz	40 ns	5.0 ns	5.0 ns	14 ns	
Identification mode	400 kHz	2.5 μs	5.0 ns	5.0 ns	50 ns	

Contents

Figures

Tables

3 System

3.1 Reset

3.1.1 Overview

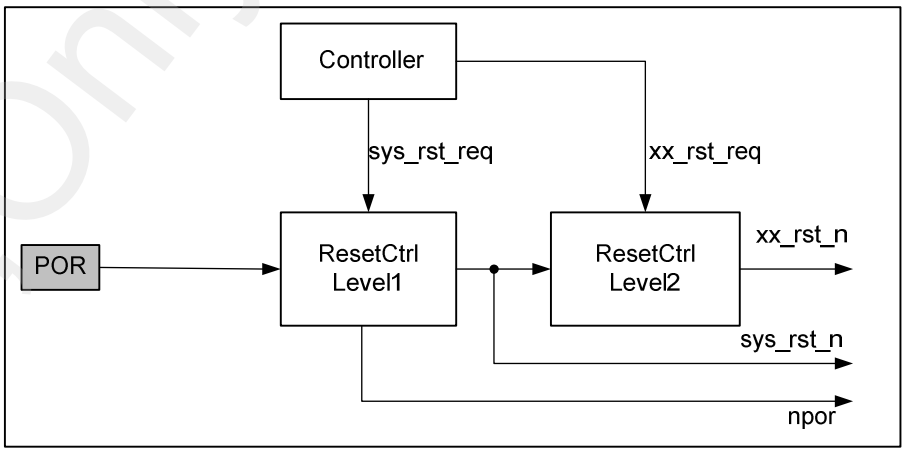
The reset management module resets the entire chip and all functional modules in a unified manner as follows:

- Manages and controls power-on reset.
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.
- Generates reset signals for each internal functional module.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals



NOTE

- POR: internal power-on reset (POR) module
- sys_rst_req: global soft reset request signal. This signal is derived from the system controller.

- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_n, and npor: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from the internal POR module	Globally resets the entire.
Global soft reset signal (syn_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3519 V100, excluding the clock reset circuits, test circuits, and registers that do not support soft reset
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3519 V100.

3.1.3 Reset Configuration

Power-On Reset

To implement power-on reset, the following conditions must be met:

- The internal POR module generates a low-level pulse, and the low pulse duration is greater than 12 XIN crystal clock cycles.
- The clock input by the XIN pin of the crystal oscillator clock works properly.

System Reset

The system is reset in either of the following ways:

- Power-on reset
- Global soft reset, controlled by the system controller

Soft Reset

Soft reset control is implemented by configuring the corresponding CRG controller. For details about configurations, see the description of the reset register for each module.

CAUTION

- After a system soft reset request is sent, the circuit reset is deasserted after at least 360 system clock cycles.

- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

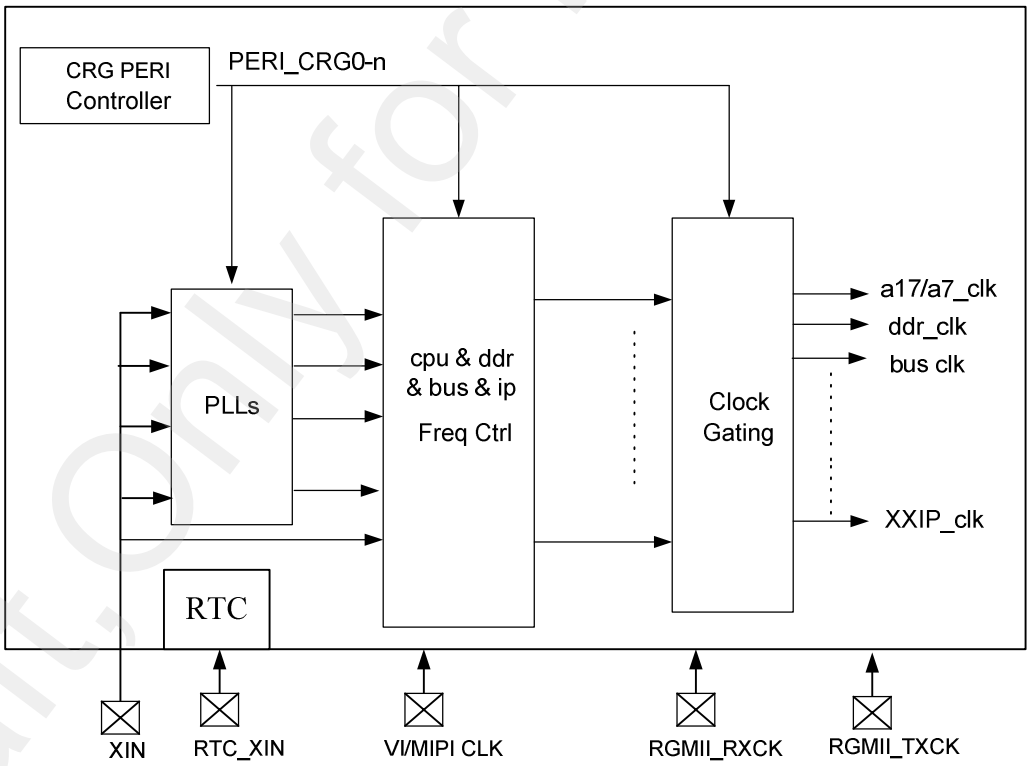
The clock and reset generator (CRG) manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the CRG.

Figure 3-2 Functional block diagram of the CRG



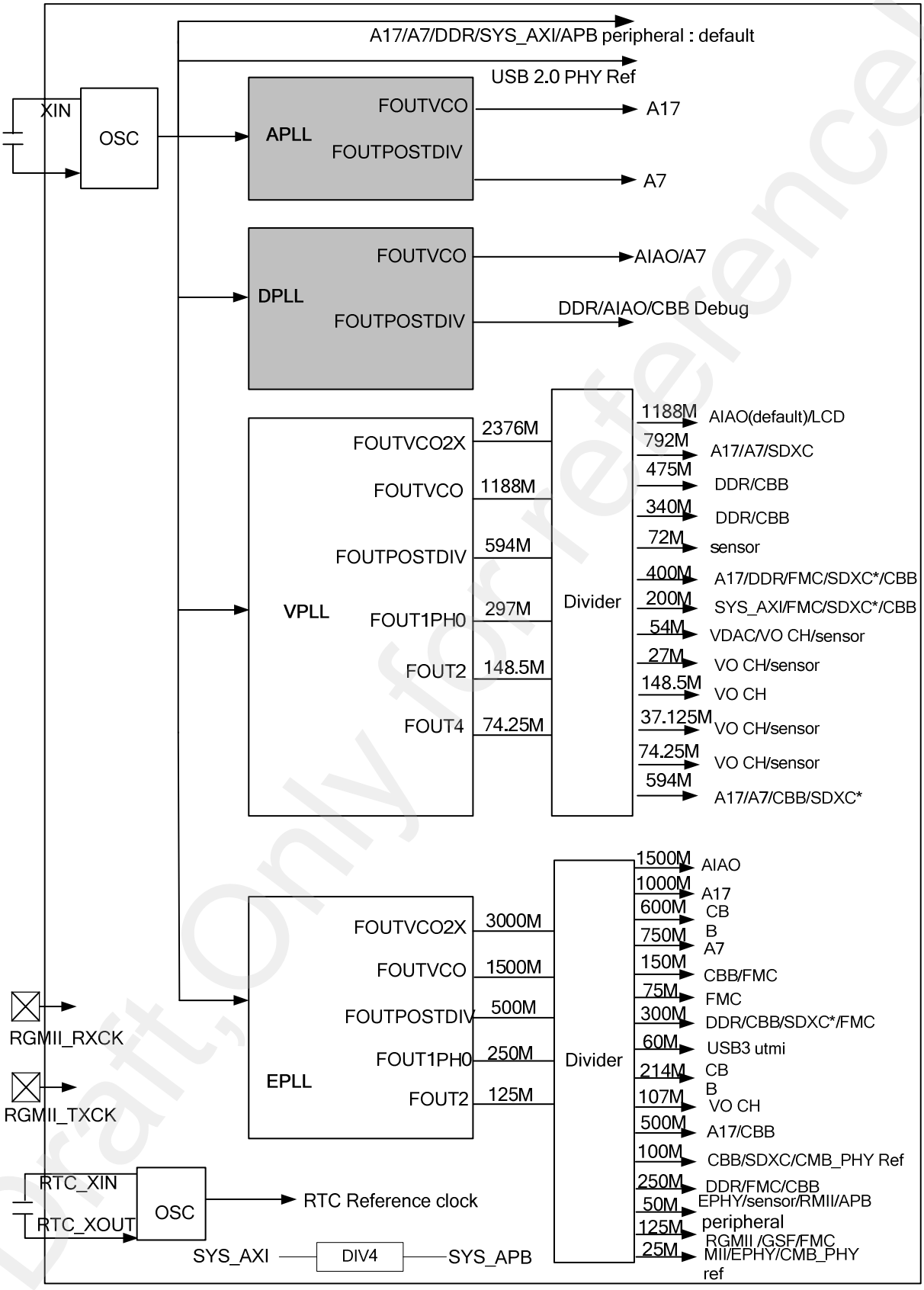
NOTE

XIN is the PLL input clock and is always connected to a 24 MHz crystal, whereas RTC_XIN is the RTC input clock and is always connected to a 32.768 kHz crystal.

3.2.3 Clock Distribution

The CRG configures, controls, and manages the internal PLLs and the input clocks from pins. It also generates the clocks required by each module. Figure 3-3 shows the clock distribution diagram.

Figure 3-3 Clock distribution diagram



NOTE

The APLL and DPLL with the gray background can be configured by programming, whereas the configurations of other PLLs are fixed. If a module has multiple clock sources, the clock source marked with "Default" indicates the default clock source. CBB indicates other media service modules apart from the CPU, DDR, bus, and peripherals.

3.2.4 PLL Configuration

The Hi3519 V100 has three internal PLLs. Each PLL uses two configuration registers. See Table 3-2.

Table 3-2 Configuration registers corresponding to PLLs

PLL	Configuration Register 0	Configuration Register 1
APLL	PERI_CRG_PLL0	PERI_CRG_PLL1
DPLL	PERI_CRG_PLL4	PERI_CRG_PLL5
VPLL	PERI_CRG_PLL6	PERI_CRG_PLL7
EPLL	PERI_CRG_PLL8	PERI_CRG_PLL9

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-3.

Table 3-3 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	PLL working frequency. It must be greater than 800 MHz but less than or equal to 2.3 GHz.
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	N/A
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	N/A
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	N/A
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	N/A
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	N/A

NOTE

- fbdiv: integral frequency multiplier
- frac: decimal frequency multiplier
- refdiv: frequency divider of the reference clock

- pstdiv1: level-1 output frequency divider
- pstdiv2: level-2 output frequency divider

For details about the frequency multiplier and divider of each PLL, see Table 3-1.

The following uses APLL as an example. If APLL outputs the 1200 MHz FOUTPOSTDIV clock to the CPU A17 core, the configured values of the register are calculated as follows:

- If postdiv2 is 2 and postdiv1 is 1, the value of FOUTVCO is 1200 MHz based on the following formula:

  FOUTVCO = FREF /(pstdiv1 x pstdiv2)
- If refdiv is 1, fbdiv and frac can be calculated based on the following formula:

  24 x (fbdiv + frac/2^24)/1 = 1200 MHz

  That is, fbdiv =50 and frac = 000000

3.2.5 Frequency Configurations

3.2.5.1 Frequency Configurations of CPU/DDR/Bus Clocks

Table 3-4 describes the frequency configurations of CPU/DDR/bus clocks.

Table 3-4 Frequency configurations of CPU/DDR/bus clocks

Signal	Configuration Register
cpu_a7_cksel	You can control this signal by configuring PERI_CRG13 bit[9:7].
a7clk_loaden	You can control this signal by configuring PERI_CRG11 bit[17].
a7clk_skipcfg	You can control this signal by configuring PERI_CRG11 bit[16:12].
ddr_sc_sel	You can control this signal by configuring PERI_CRG13 bit[2:0].
bus_sc_sel	You can control this signal by configuring PERI_CRG13 bit[13:12].

3.2.5.2 Frequency Configurations of Module Clocks

Table 3-5 describes the frequency configurations of clocks for each module.

Table 3-5 Frequency configurations of clocks for each module

Signal	Description
VDP clock configurations	
vo_out_cksel	PERI_CRG17 bit[16:14]
hd_div_mode	PERI_CRG17 bit[13:12]
vdac_pctrl	PERI_CRG17 bit[3]
vo_out_pctrl	PERI_CRG17 bit[2]
lcd_mclk_div	PERI_CRG18 bit[26:0]
VI_MIPI clock configurations	

Signal	Description
sensor_cksel	PERI_CRG16 bit[3:0]
vimipi0_cksel	PERI_CRG19 bit[2:0]
vi_pctrl	PERI_CRG15 bit[9]
vi_isp_ckdiv	PERI_CRG15 bit[11:10]
VEDU clock configurations	
vedu_cksel	PERI_CRG19 bit[12:10]
veduclk_loaden	PERI_CRG20 bit[9]
veduclk_skipcfg	PERI_CRG20 bit[8:4]
VPSS clock configurations	
vpss0_cksel	PERI_CRG19 bit[7:5]
vpssclk_loaden	PERI_CRG22 bit[9]
vpssclk_skipcfg	PERI_CRG22 bit[8:4]
TDE clock configurations	
tdeclk_loaden	PERI_CRG25 bit[9]
tdeclk_skipcfg	PERI_CRG25 bit[8:4]
VGS clock configurations	
vgs_cksel	PERI_CRG19 bit[15:13]
vgsclk_loaden	PERI_CRG23 bit[9]
vgsclk_skipcfg	PERI_CRG23 bit[8:4]
JPGE clock configurations	
jpgeclk_loaden	PERI_CRG24 bit[9]
jpgeclk_skipcfg	PERI_CRG24 bit[8:4]
IVE clock configurations	
ive_cksel	PERI_CRG19 bit[21:19]
GDC clock configurations	
gdc_cksel	PERI_CRG19 bit[18:16]
gdcclk_loaden	PERI_CRG29 bit[9]
gdcclk_skipcfg	PERI_CRG29 bit[8:4]
FMC clock configurations	
fmc_cksel	PERI_CRG48 bit[4:2]
SDIO clock configurations	

Signal	Description
emmc_clk_mode	PERI_CRG49 bit[21]
emmc_cksel	PERI_CRG49 bit[20:18]
sdxc0_clk_mode	PERI_CRG49 bit[13]
sdxc0_cksel	PERI_CRG49 bit[12:10]
sdxc1_clk_mode	PERI_CRG49 bit[5]
CIPHER clock configurations	
ca_cksel	PERI_CRG31 bit[6]
PWM&I2C&UART clock configurations	
pwm_cksel	PERI_CRG55 bit[3:2]
i2c_cksel	PERI_CRG57 bit[26]
uart_cksel	PERI_CRG57 bit[25]
GSF&GMAC clock configurations	
mac_speed	PERI_CRG59 bit[1]
port_select	PERI_CRG59 bit[0]
ext_fephy_cksel	PERI_CRG51 bit[6]
rmii_cksel	PERI_CRG51 bit[4]
AIAO clock configurations	
ai0_cksel	PERI_CRG32 bit[3:2]
COMB PHY clock configurations	
combphy_refclk_sel	PERI_CRG43 bit[9]
usb3_utmi_cksel	PERI_CRG46 bit[13]

3.2.5.3 Precautions

Take the following precautions when configuring clocks:

- If the frequency of the PLL is changed, the PLL can output a clock with a stable frequency 0.1 ms later. Before changing the PLL frequency, you need to switch the target clock to the non-PLL clock mode.
- You can determine whether the PLL is stable by checking the PLL lock indicator bit. The status of the PLL lock indicator bit can be obtained by reading PERI_CRG58 bit[3:0].

3.2.6 Register Summary

Table 3-6 describes CRG registers.

Table 3-6 Summary of CRG registers (base address: 0x1201_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG_PLL 0	APLL configuration register 0	3-11
0x0004	PERI_CRG_PLL 1	APLL configuration register 1	3-12
0x0010	PERI_CRG_PLL 4	DPLL configuration register 0	3-13
0x0014	PERI_CRG_PLL 5	DPLL configuration register 1	3-14
0x0018	PERI_CRG_PLL 6	VPLL configuration register 0	3-15
0x001C	PERI_CRG_PLL 7	VPLL configuration register 1	3-16
0x0020	PERI_CRG_PLL 8	EPLL configuration register 0	3-17
0x0024	PERI_CRG_PLL 9	EPLL configuration register 1	3-18
0x0028	PERI_CRG10	CoreSight & A17 clock reset configuration register	3-19
0x002C	PERI_CRG11	A7 clock reset configuration register	3-20
0x0030	PERI_CRG12	DDR clock configuration register	3-22
0x0034	PERI_CRG13	SoC frequency profile configuration register	3-22
0x003C	PERI_CRG15	VI-MIPI clock reset configuration register	3-24
0x0040	PERI_CRG16	Sensor clock configuration register	3-25
0x0044	PERI_CRG17	VOU clock and reset control register	3-26
0x0048	PERI_CRG18	LCD clock configuration register	3-28
0x004C	PERI_CRG19	Media CBB frequency profile configuration register	3-28
0x0050	PERI_CRG20	VEDU clock and soft reset control register	3-30
0x0058	PERI_CRG22	VPSS clock and soft reset control register	3-31
0x005C	PERI_CRG23	VGS clock and soft reset control register	3-32
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-32
0x0064	PERI_CRG25	TDE clock and soft reset control register	3-33
0x006C	PERI_CRG27	IVE clock and soft reset control register	3-34
0x0074	PERI_CRG29	GDC clock and soft reset control register	3-34

Offset Address	Register	Description	Page
0x007C	PERI_CRG31	Hash/SAR_ADC/Cipher clock and soft reset control register	3-35
0x0080	PERI_CRG32	AIAO clock reset control register	3-36
0x0084	PERI_CRG33	GZIP clock and soft reset control register	3-37
0x00AC	PERI_CRG43	COMB PHY clock reset control register	3-37
0x00B0	PERI_CRG44	PCIe CTRL clock and soft reset control register	3-39
0x00B4	PERI_CRG45	USB 2.0 clock and soft reset control register	3-40
0x00B8	PERI_CRG46	USB 3.0 CTRL clock and soft reset control register	3-41
0x00C0	PERI_CRG48	FMC clock and soft reset control register	3-42
0x00C4	PERI_CRG49	SDIO0/SDIO1/eMMC clock and soft reset control register	3-43
0x00CC	PERI_CRG51	GSF/GMAC clock and soft reset control register	3-45
0x00D8	PERI_CRG54	DDRT clock and soft reset control register	3-47
0x00DC	PERI_CRG55	PWM clock and reset control register	3-47
0x00E0	PERI_CRG56	RSA/TRNG/DMA clock and soft reset control register	3-48
0x00E4	PERI_CRG57	Clock soft reset control register for other APB modules	3-49
0x00E8	PERI_CRG58	CRG status register	3-52
0x00EC	PERI_CRG59	GMAC interface control register	3-53
0x00F0	PERI_CRG60	GMAC interface status register	3-55
0x013C	PERI_CRG79	SoC frequency profile status register	3-55

3.2.7 Register Description

PERI_CRG_PLL0

PERI_CRG_PLL0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG_PLL0	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	apll_postdiv2			reserved	apll_postdiv1			apll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	apll_postdiv2	Level-2 output divider of the APLL
[27]	RO	reserved	Reserved
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL
[23:0]	RW	apll_frac	Decimal divider of the APLL

PERI_CRG_PLL1

PERI_CRG_PLL1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG_PLL1	0x0910_1032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				apll_foutvco2xpd	apll_bypass	apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	reserved				apll_refdiv				apll_fbdiv											
Reset	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[27]	RW	apll_foutvco2xpd	APLL VCO2X output power-down control 0: normal output clock 1: no output clock

[26]	RW	apll_bypass	APLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	apll_dacpd	APLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	apll_dsmpd	APLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	apll_pd	APLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	apll_foutvcopd	APLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	apll_postdivpd	APLL POSTDIV output power-down control 0: normal clock output 1: no output clock
[20]	RW	apll_fout4phasepd	APLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	apll_refdiv	Frequency divider of the APLL reference clock
[11:0]	RW	apll_fbdiv	Integral frequency multiplier of the APLL

PERI_CRG_PLL4

PERI_CRG_PLL4 is DPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG_PLL4	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		vpll_postdiv2		reserved		vpll_postdiv1		vpll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	dpll_postdiv2	Level-2 output divider of DPLL
[27]	RO	reserved	Reserved
[26:24]	RW	dpll_postdiv1	Level-1 output divider of DPLL
[23:0]	RW	dpll_frac	Decimal divider of DPLL

PERI_CRG_PLL5

PERI_CRG_PLL5 is DPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG_PLL5	0x0910_60E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dpll_foutvco2xpd	dpll_bypass	dpll_dacpd	dpll_dsmpd	dpll_pd	dpll_foutvcopd	dpll_postdivpd	dpll_fout4phasepd	reserved				dpll_refdiv				dpll_fbdiv												
Reset	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	dpll_foutvco2xpd	DPLL VCO2X output power-down control 0: normal output clock 1: no output clock

[26]	RW	dpll_bypass	DPLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	dpll_dacpd	DPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	dpll_dsmpd	DPLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	dpll_pd	DPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	dpll_foutvcopd	DPLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	dpll_postdivpd	DPLL POSTDIV output power-down control 0: normal clock output 1: no output clock
[20]	RW	dpll_fout4phasepd	DPLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	dpll_refdiv	Frequency divider of the DPLL reference clock
[11:0]	RW	dpll_fbdiv	Integral frequency multiplier of the DPLL

PERI_CRG_PLL6

PERI_CRG_PLL6 is VPLL configuration register 0

Offset Address	Register Name	Total Reset Value
0x0018	PERI_CRG_PLL6	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll_postdiv2			reserved	vpll_postdiv1			vpll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	vpll_postdiv2	Level-2 output divider of VPLL
[27]	RO	reserved	Reserved
[26:24]	RW	vpll_postdiv1	Level-1 output divider of VPLL
[23:0]	RW	vpll_frac	Decimal divider of VPLL

PERI_CRG_PLL7

PERI_CRG_PLL7 is VPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG_PLL7	0x0100_2063

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vpll_foutvco2xpd	vpll0_bypass	vpll0_dacpd	vpll0_dsmpd	vpll0_pd	vpll0_foutvcopd	vpll0_postdivpd	vpll0_fout4phasepd	reserved				vpll0_refdiv				vpll0_fbdiv											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	vpll_foutvco2xpd	VPLL VCO2X output power-down control 0: normal output clock 1: no output clock

[26]	RW	vpll_bypass	VPLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	vpll_dacpd	VPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	vpll_dsmpd	VPLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	vpll_pd	VPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	vpll_foutvcopd	VPLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	vpll_postdivpd	VPLL POSTDIV output power-down control 0: normal output clock 1: no output clock
[20]	RW	vpll_fout4phasepd	VPLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	vpll_refdiv	Frequency divider of the VPLL reference clock
[11:0]	RW	vpll_fbdiv	Integral frequency multiplier of VPLL

PERI_CRG_PLL8

PERI_CRG_PLL8 is EPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG_PLL8	0x1300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	epll_postdiv2			reserved	epll_postdiv1			epll_frac																							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	epll_postdiv2	Level-2 output divider of the EPLL
[27]	RO	reserved	Reserved
[26:24]	RW	epll_postdiv1	Level-1 output divider of the EPLL
[23:0]	RW	epll_frac	Decimal divider of the EPLL

PERI_CRG_PLL9

PERI_CRG_PLL9 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG_PLL9	0x0100_207D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				epll_foutvco2xpd	epll_bypass	epll_dacpd	epll_dsmpd	epll_pd	epll_foutvcopd	epll_postdivpd	epll_fout4phasepd	reserved				epll_refdiv				epll_fbdiv											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	epll_foutvco2xpd	EPLL VCO2X output power-down control 0: normal output clock 1: no output clock

[26]	RW	epll_bypass	EPLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	epll_dacpd	EPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	epll_dsmpd	EPLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	epll_pd	EPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	epll_foutvcopd	EPLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	epll_postdivpd	EPLL POSTDIV output power-down control 0: normal output clock 1: no output clock
[20]	RW	epll_fout4phasepd	EPLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	epll_refdiv	Frequency divider of the EPLL reference clock
[11:0]	RW	epll_fbdiv	Integral frequency multiplier of the EPLL

PERI_CRG10

PERI_CRG10 is a CoreSight & A17 clock reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0318_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						cs_cken	cs_dbg_pwrup_mode	reserved		a17_wakeup_cken	a17_toppdbg_cken	a17_wakeup_srst_req	reserved																		
Reset	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	cs_cken	CoreSight TOP clock gating, valid only in manual mode 0: disabled 1: enabled
[24]	RW	cs_dbg_pwrup_mode	CoreSight TOP power-up mode 0: automatic mode 1: manual mode
[23:22]	RO	reserved	Reserved
[21]	RW	a17_wakeup_cken	A17 subsystem global clock gating, valid only in slave mode 0: disabled 1: enabled
[20]	RW	a17_toppdbg_cken	PCLKDBG clock gating 0: disabled 1: enabled
[19]	RW	a17_wakeup_srst_req	A17 subsystem global soft reset, valid only in slave mode 0: deassert reset 1: reset
[18:0]	RO	reserved	Reserved

PERI_CRG11

PERI_CRG11 is an A7 clock reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0010_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											a7_ddrboot_srst_req	reserved		a7clk_loaden		a7clk_skipcfg				a7_wakeup_srst_req	reserved									a7_wakeup_cken	pclkdbg_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RW	a7_ddrboot_srst_req	A7 global soft reset, valid only when the system boots from a DDR of the slave chip over the PCIe interface 0: deassert reset 1: reset
[19:18]	RO	reserved	Reserved
[17]	RW	a7clk_loaden	Skip configuration enable for the CPU clock To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to a7clk_loaden. 2. Write 1 to a7clk_loaden.
[16:12]	RW	a7clk_skipcfg	Skip configuration of the CPU clock N: *N*-beat clocks are disabled every 32-beat CPU clocks.
[11]	RW	a7_wakeup_srst_req	A7 global soft reset, valid only when the system does not boot from a DDR of the slave chip 0: deassert reset 1: reset
[10:2]	RO	reserved	Reserved
[1]	RW	a7_wakeup_cken	A7 global clock gating, valid only in non-master CPU mode 0: disabled 1: enabled
[0]	RW	pclkdbg_cken	A7 PCLKDBG clock gating 0: disabled 1: enabled

PERI_CRG12

PERI_CRG12 is a DDR clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ddr_apb_cken	ddr_hipack_cken	ddr_cfg_cken	reserved			ddr_apb_srst_req	ddr_hipack_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	ddr_apb_cken	DDR APB gating 0: disabled 1: enabled
[5]	RW	ddr_hipack_cken	DDR HiPack gating 0: disabled 1: enabled
[4]	RW	ddr_cfg_cken	DDR CFG gating 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved
[1]	RW	ddr_apb_srst_req	DDR APB soft reset 0: deassert reset 1: reset
[0]	RW	ddr_hipack_srst_req	DDR HiPack soft reset 0: deassert reset 1: reset

PERI_CRG13

PERI_CRG13 is an SoC frequency profile configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		bus_cksel		reserved		cpu_a7_cksel				cpu_a17_cksel				reserved		ddr_cksel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:12]	RW	bus_cksel	Bus clock profile x0: XTAL clock x1: 200 MHz clock
[11:10]	RO	reserved	Reserved
[9:7]	RW	cpu_a7_cksel	A7 CPU profile 000: XTAL clock 001: DPLL VCO 010: APLL POSTDIV 011: 792 MHz clock 100: 750 MHz clock 101: 594 MHz clock Other values: reserved
[6:4]	RW	cpu_a17_cksel	A17 CPU clock profile 000: XTAL clock 001: APLL VCO 010: DPLL VCO 011: 1000 MHz clock 100: 792 MHz clock 101: 594 MHz clock 110: 500 MHz clock 111: 400 MHz clock
[3]	RO	reserved	Reserved

[2:0]	RW	ddr_cksel	DDR clock profile 000: XTAL clock 001: DPLL POSTDIV 010: 476 MHz clock 011: 396 MHz clock 100: 346 MHz clock 101: 300 MHz clock 110: 250 MHz clock 111: reserved

PERI_CRG15

PERI_CRG15 is a VI-MIPI clock reset configuration register.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_CRG15	0x0000_033F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vi0_isp_ckdiv		vi0_pctrl	vi0_cken	reserved		isp0_cfg_srst_req	isp0_core_srst_req	mipi_hrst_req	mipi0_srst_req	vi0_hrst_req	vi0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:10]	RW	vi0_isp_ckdiv	ISP0 clk_ppc frequency division coefficient 00: DIV2 01: DIV4 1X: DIV1
[9]	RW	vi0_pctrl	Phase of the VI0 interface clock 0: positive-phase clock 1: negative-phase clock
[8]	RW	vi0_cken	VI0 clock gating 0: disabled 1: enabled
[7:6]	RO	reserved	Reserved

[5]	RW	isp0_cfg_srst_req	ISP0 CFG soft reset 0: deassert reset 1: reset
[4]	RW	isp0_core_srst_req	ISP0 core soft reset 0: deassert reset 1: reset
[3]	RW	mipi_hrst_req	MIPI CTRL bus soft reset 0: deassert reset 1: reset
[2]	RW	mipi0_srst_req	MIPI CTRL CH0 soft reset 0: deassert reset 1: reset
[1]	RW	vi0_hrst_req	VI0 bus soft reset 0: deassert reset 1: reset
[0]	RW	vi0_srst_req	VI0 soft reset 0: deassert reset 1: reset

PERI_CRG16

PERI_CRG16 is a sensor clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sensor0_ctrl_srst_req	sensor0_srst_req	sensor0_cken	sensor0_cksel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved

[6]	RW	sensor0_ctrl_srst_req	Soft reset on the slave mode control module of sensor0 0: deassert reset 1: reset
[5]	RW	sensor0_srst_req	Sensor0 soft reset 0: deassert reset 1: reset
[4]	RW	sensor0_cken	Sensor0 CLKOUT clock gating 0: disabled 1: enabled
[3:0]	RW	sensor0_cksel	Sensor0 CLKOUT clock configuration 0000: 74.25 MHz 0001: 72 MHz 0010: 54 MHz 0011: 50 MHz 01xx: 24 MHz 1000: 37.125 MHz 1001: 36 MHz 1010: 27 MHz 1011: 25 MHz 11xx: 12 MHz

PERI_CRG17

PERI_CRG17 is a VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0044	PERI_CRG17	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vo_out_cksel				hd_div_mode				vdac_cken	vou_sd_cken	vou_hd_cken	vo_out_cken	vou_acken	vou_pcken	vou_ppc_cken	vou_cfg_cken	vdac_pctrl		vo_out_pctrl		reserved		vo_srst_req	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved

[16:14]	RW	vo_out_cksel	VO OUT_CLK frequency select 000: 148.5 MHz 001: 74.25 MHz 010: 37.125 MHz 011: 107 MHz 100: 54 MHz 101: 27 MHz 110: LCD frequency divider clock 111: reserved
[13:12]	RW	hd_div_mode	Frequency division ratio of VO_OUT_CLK to the DHD channel clock 00: DIV1 01: DIV2 10: DIV3 11: DIV4
[11]	RW	vdac_cken	VDACH clock gating 0: disabled 1: enabled
[10]	RW	vou_sd_cken	VOU SD clock gating 0: disabled 1: enabled
[9]	RW	vou_hd_cken	VOU HD clock gating 0: disabled 1: enabled
[8]	RW	vo_out_cken	VO_CLKOUT clock gating 0: disabled 1: enabled
[7]	RW	vou_acken	VOU AXI bus clock gating 0: disabled 1: enabled
[6]	RW	vou_pcken	VOU APB clock gating 0: disabled 1: enabled
[5]	RW	vou_ppc_cken	VOU PPC clock gating 0: disabled 1: enabled
[4]	RW	vou_cfg_cken	VOU CFG clock gating (internally configured) 0: disabled 1: enabled

[3]	RW	vdac_pctrl	VDAC clock phase 0: positive-phase clock 1: negative-phase clock
[2]	RW	vo_out_pctrl	Phase control for the VOU HD output associated clock 0: positive-phase clock 1 (default): negative-phase clock
[1]	RO	reserved	Reserved
[0]	RW	vo_srst_req	VOU soft reset 0: deassert reset 1: reset

PERI_CRG18

PERI_CRG18 is an LCD clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0015_E4C3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				lcd_cken	lcd_mclk_div																										
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	1	0	0	1	1	0	0	0	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	lcd_cken	LCD frequency divider clock gating 0: disabled 1: enabled
[26:0]	RW	lcd_mclk_div	LCD frequency division clock (configurable) Assume that the target frequency is X (MHz), the LCD frequency division clock (lcd_mclk_div) is calculated as follows: lcd_mclk_div = (X/1188) x 2^{27}

PERI_CRG19

PERI_CRG19 is a media CBB frequency profile configuration register.

Offset Address	Register Name	Total Reset Value
0x004C	PERI_CRG19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										ive_cksel		gdc_cksel				vgs_cksel				vedu_cksel		vpss1_cksel		vpss0_cksel				vimipi1_cksel			vimipi0_cksel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:19]	RW	ive_cksel	IVE frequency 000: 200 MHz 001: 300 MHz 010: 400 MHz 011: 475 MHz 100: 594 MHz Other values: reserved
[18:16]	RW	gdc_cksel	GDC frequency 000: 200 MHz 001: 300 MHz 010: 400 MHz 011: 500 MHz 100: 340 MHz 101: 475 MHz 110: 594 MHz 111: reserved
[15:13]	RW	vgs_cksel	VGS frequency 000: 150 MHz 001: 250 MHz 010: 300 MHz 011: 475 MHz 100: 400 MHz 101: 500 MHz 110: 594 MHz 111: reserved

[12:10]	RW	vedu_cksel	VEDU frequency 000: 200 MHz 001: 250 MHz 010: 300 MHz 011: 500 MHz 100: 594 MHz Other values: reserved
[9:8]	RO	reserved	Reserved
[7:5]	RW	vpss0_cksel	VPSS0 frequency 000: 100 MHz 001: 150 MHz 010: 214 MHz 011: 300 MHz 100: 340 MHz 101: 400 MHz Other values: reserved
[4:3]	RO	reserved	Reserved
[2:0]	RW	vimipi0_cksel	VIMIPI0 frequency 000: 100 MHz 001: 150 MHz 010: 214 MHz 011: 300 MHz 100: 340 MHz 101: 398 MHz 110: 500 MHz 111: 600 MHz

PERI_CRG20

PERI_CRG20 is a VEDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0050	PERI_CRG20	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vedu_cken	vedu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vedu_cken	VEDU clock gating 0: disabled 1: enabled
[0]	RW	vedu_srst_req	VEDU soft reset 0: deassert reset 1: reset

PERI_CRG22

PERI_CRG22 is a VPSS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG22	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vps0_cken	vps0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vps0_cken	VPSS0 clock gating 0: disabled 1: enabled

[0]	RW	vps0_srst_req	VPSS0 soft reset 0: deassert reset 1: reset

PERI_CRG23

PERI_CRG23 a VGS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_CRG23	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vgs_cken	vgs_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vgs_cken	VGS clock gating 0: disabled 1: enabled
[0]	RW	vgs_srst_req	VGS soft reset 0: deassert reset 1: reset

PERI_CRG24

PERI_CRG24 is a JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	jpge_cken	JPGE clock gating 0: disabled 1: enabled
[0]	RW	jpge_srst_req	JPGE soft reset 0: deassert reset 1: reset

PERI_CRG25

PERI_CRG25 is a TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_CRG25	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tde_cken	tde_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tde_cken	TDE clock gating 0: disabled 1: enabled

[0]	RW	tde_srst_req	TDE soft reset 0: deassert reset 1: reset

PERI_CRG27

PERI_CRG27 is an IVE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							hash_cken	hash_srst_req	vapu_cken	vapu_srst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	ive_cken	IVE clock gating 0: disabled 1: enabled
[0]	RW	ive_srst_req	IVE soft reset 0: deassert reset 1: reset

PERI_CRG29

PERI_CRG29 is a GDC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_CRG29	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														gdc_cken	gdc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	gdc_cken	GDC clock gating 0: disabled 1: enabled
[0]	RW	gdc_srst_req	GDC soft reset 0: deassert reset 1: reset

PERI_CRG31

PERI_CRG31 is a hash/SAR_ADC/cipher clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ca_cksel	hash_cken	hash_srst_req	sar_adc_cken	sar_adc_srst_req	cipher_cken	cipher_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	ca_cksel	Cipher clock select 0: 200 MHz 1: 250 MHz

[5]	RW	hash_cken	Hash clock gating 0: disabled 1: enabled
[4]	RW	hash_srst_req	HASH soft reset 0: deassert reset 1: reset
[3]	RW	sar_adc_cken	SAR ADC clock gating 0: disabled 1: enabled
[2]	RW	sar_adc_srst_req	SAR ADC soft reset 0: deassert reset 1: reset
[1]	RW	cipher_cken	Cipher clock gating 0: disabled 1: enabled
[0]	RW	cipher_srst_req	Cipher soft reset 0: deassert reset 1: reset

PERI_CRG32

PERI_CRG32 is an AIAO clock reset control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												aiao_cksel		aiao_cken	aiao_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3:2]	RW	aiao_cksel	AIAO MCLK PLL clock source select 00: 1188 MHz 01: 1500 MHz 10: DPLL FOUTVCO 11: DPLL FOUTPOSTDIV
[1]	RW	aiao_cken	AIAO bus clock gating 0: disabled 1: enabled
[0]	RW	aiao_srst_req	AIAO bus soft reset 0: deassert reset 1: reset

PERI_CRG33

PERI_CRG33 is a GZIP clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_CRG33	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														gzip_cken	gzip_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	gzip_cken	GZIP clock gating 0: disabled 1: enabled
[0]	RW	gzip_srst_req	GZIP soft reset 0: deassert reset 1: reset

PERI_CRG43

PERI_CRG43 is a COMB PHY clock reset control register.

Offset Address	Register Name	Total Reset Value
0x00AC	PERI_CRG43	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						combphy_refclk_sel	combphy_ref_cken	reserved					combphy_ref_cken_mode	combphy_srst_req_sel	combphy_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	combphy_refclk_sel	Internal clock source select for the COMB PHY reference clock 0: 100 MHz clock 1: 25 MHz clock
[8]	RW	combphy_ref_cken	COMB PHY reference clock gating In PCIe mode: 0: The clock gating is controlled by PERI_CRG43 bit[2]. 1: enabled In USB mode: 0: disabled 1: enabled
[7:3]	RO	reserved	Reserved
[2]	RW	combphy_ref_cken_mode	Clock gating of the COMB PHY in PCIe mode 0: The clock is controlled by wifi_clk_req_n and misc_local_clk_req_n. 1: The clock is controlled by misc_local_clk_req_n.
[1]	RW	combphy_srst_req_sel	Soft reset mode for the COMB PHY port In USB 3.0 mode, the soft reset mode is directly controlled by PERI_CRG43 bit[0]. In PCIe mode: 0: The soft reset mode is controlled by PCIe CTRL. 1: The soft reset mode is controlled by PERI_CRG43 bit[0].
[0]	RW	combphy_srst_req	Soft reset for the COMB PHY port 0: deassert reset 1: reset

PERI_CRG44

PERI_CRG44 is a PCIe CTRL clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B0	PERI_CRG44	0x0000_00F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					wifi_clk_ctrl			pcie_aux_cken	pcie_pipe_cken	pcie_sys_cken	pcie_bus_cken	reserved	pcie_srst_req	pcie_sys_srst_req	pcie_bus_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	wifi_clk_ctrl	PAD OE control mode for the PCIe output differential clock 000: PAD OE control is forcibly enabled. 001: PAD OE control is forcibly disabled. 010: PAD OE control is controlled by wifi_clk_req_n. 011: PAD OE control is controlled by misc_local_clk_req_n. 100: PAD OE control is controlled by wifi_clk_req_n and misc_local_clk_req_n. 101: PAD OE control is controlled by PERI_CRG43 bit[8]. Other values: reserved
[7]	RW	pcie_aux_cken	PCIe CTRL AUX clock gating 0: disabled 1: enabled
[6]	RW	pcie_pipe_cken	PCIe CTRL PIPE clock gating 0: disabled 1: enabled
[5]	RW	pcie_sys_cken	PCIe CTRL SYS clock gating 0: disabled 1: enabled
[4]	RW	pcie_bus_cken	PCIe CTRL bus clock gating 0: disabled 1: enabled
[3]	RO	reserved	Reserved

[2]	RW	pcie_srst_req	PCIe CTRL soft reset 0: deassert reset 1: reset
[1]	RW	pcie_sys_srst_req	PCIe CTRL SYS soft reset 0: deassert reset 1: reset
[0]	RW	pcie_bus_srst_req	PCIe CTRL bus soft reset 0: deassert reset 1: reset

PERI_CRG45

PERI_CRG45 is a USB 2.0 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_CRG45	0x0000_00EF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							usb_otg_phy_srst_req	usb_cken	reserved	usb_ctrl_utmi0_req	reserved		usb_phy_port0_treq	usb_phy_req	usb_hrst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	usb_otg_phy_srst_req	OTG PHY soft reset 0: deassert reset 1: reset
[7]	RW	usb_cken	Clock gating of the USB PHY reference clock 0: disabled 1: enabled
[6]	RO	reserved	Reserved
[5]	RW	usb_ctrl_utmi0_req	Soft reset on USB controller port 0 0: deassert reset 1: reset

[4:3]	RO	reserved	Reserved
[2]	RW	usb_phy_port0_treq	Soft reset on USB PHY port 0 0: deassert reset 1: reset
[1]	RW	usb_phy_req	USB PHY soft reset 0: deassert reset 1: reset
[0]	RW	usb_hrst_req	Soft reset on the USB controller bus 0: deassert reset 1: reset

PERI_CRG46

PERI_CRG46 is a USB 3.0 CTRL clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_3F01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		usb3_utmi_cksel	usb3_utmi_cken	usb3_pipe_cken	usb3_suspend_cken	usb3_ref_cken	usb3_bus_cken	reserved							usb3_vcc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	usb3_utmi_cksel	USB 3.0 UTMI clock source select 0: The USB 2.0 PHY clock is selected. 1: The internal 60 MHz clock is selected.
[12]	RW	usb3_utmi_cken	USB 3.0 CTRL UTMI clock gating 0: disabled 1: enabled
[11]	RW	usb3_pipe_cken	USB 3.0 CTRL PIPE clock gating 0: disabled 1: enabled

[10]	RW	usb3_suspend_cken	USB 3.0 CTRL suspend clock gating 0: disabled 1: enabled
[9]	RW	usb3_ref_cken	USB 3.0 CTRL REF clock gating 0: disabled 1: enabled
[8]	RW	usb3_bus_cken	USB 3.0 CTRL bus clock gating 0: disabled 1: enabled
[7:1]	RO	reserved	Reserved
[0]	RW	usb3_vcc_srst_req	Soft reset on the USB 3.0 CTRL VCC 0: deassert reset 1: reset

PERI_CRG48

PERI_CRG48 is an FMC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											fmc_cksel			fmc_cken	fmc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

[4:2]	RW	fmc_cksel	FMC clock source select (PHY_CLK_OUT is the clock obtained after the source clock is divided by 2 in SDR mode, and the clock obtained after the source clock is divided by 4 in DDR mode) 000: 24 MHz clock 001: 75 MHz clock 010: 125 MHz clock 011: 150 MHz clock 100: 200 MHz clock 101: 250 MHz clock 110: 300 MHz clock (available only in DDR mode) 111: 400 MHz clock (available only in DDR mode)
[1]	RW	fmc_cken	FMC clock gating 0: disabled 1: enabled
[0]	RW	fmc_srst_req	FMC soft reset 0: deassert reset 1: reset

PERI_CRG49

PERI_CRG49 is an SDIO0/SDIO1/eMMC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0002_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								emmc_dll_srst_req	emmc_dll_cken	emmc_clk_mode	emmc_cksel			sdxc2_cken	sdxc2_srst_req	reserved		sdxc0_clk_mode	sdxc0_cksel			sdxc0_cken	sdxc0_srst_req	reserved		sdxc1_clk_mode	sdxc1_cksel			sdxc1_cken	sdxc1_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RW	emmc_dll_srst_req	eMMC DLL soft reset 0: deassert reset 1: reset

[22]	RW	emmc_dll_cken	eMMC DLL clock gating 0: disabled 1: enabled
[21]	RW	emmc_clk_mode	eMMC clock frequency division mode 0: DIV4 (corresponding to 8-phase tuning) 1: DIV8 (corresponding to 16-phase tuning)
[20:18]	RW	emmc_cksel	eMMC clock source select 000: 100 MHz 001: 200 MHz 010: 300 MHz 011: 400 MHz 100: 594 MHz 101: 792 MHz 110: 1500 MHz (if the 1500 MHz clock is selected, the frequency division mode must be DIV8) 111: reserved
[17]	RW	emmc_cken	eMMC clock gating 0: disabled 1: enabled
[16]	RW	emmc_srst_req	eMMC soft reset 0: deassert reset 1: reset
[15:14]	RO	reserved	Reserved
[13]	RW	sdxc0_clk_mode	SDIO0 clock frequency division mode 0: DIV4 (corresponding to 8-phase tuning) 1: DIV8 (corresponding to 16-phase tuning)
[12:10]	RW	sdxc0_cksel	SDIO0 clock source select 000: 100 MHz 001: 200 MHz 010: 300 MHz 011: 400 MHz 100: 594 MHz 101: 792 MHz 110: 1500 MHz (if the 1500 MHz clock is selected, the frequency division mode must be DIV8) 111: reserved
[9]	RW	sdxc0_cken	SDIO0 clock gating 0: disabled 1: enabled

[8]	RW	sdxc0_srst_req	SDIO0 soft reset 0: deassert reset 1: reset
[7:6]	RO	reserved	Reserved
[5]	RW	sdxc1_clk_mode	SDIO1 clock frequency division mode 0: DIV4 (corresponding to 8-phase tuning) 1: DIV8 (corresponding to 16-phase tuning)
[4:2]	RW	sdxc1_cksel	SDIO1 clock source select 000: 100 MHz 001: 200 MHz 010: 300 MHz 011: 400 MHz 100: 594 MHz 101: 792 MHz 110: 1500 MHz (if the 1500 MHz clock is selected, the frequency division mode must be DIV8) 111: reserved
[1]	RW	sdxc1_cken	SDIO1 clock gating 0: disabled 1: enabled
[0]	RW	sdxc1_srst_req	SDIO1 soft reset 0: deassert reset 1: reset

PERI_CRG51

PERI_CRG51 is a GSF/GMAC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ext_fephy_srst_req	ext_fephy_cksel	gsf_cksel	rmii_cksel	gmac_if_cken	gmac_if_srst_req	gsf_cken	gsf_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ext_fephy_srst_req	External FE PHY soft reset 0: deassert reset 1: reset
[6]	RW	ext_fephy_cksel	Clock select for the external FE PHY 0: 25 MHz clock 1: 50 MHz clock
[5]	RW	gsf_cksel	GSF clock select 0: 125 MHz clock 1: 75 MHz clock
[4]	RW	rmii_cksel	RMII clock select 0: CRG clock 1: PAD input clock
[3]	RW	gmac_if_cken	MAC_IF clock gating 0: disabled 1: enabled
[2]	RW	gmac_if_srst_req	MAC_IF soft reset 0: deassert reset 1: reset
[1]	RW	gsf_cken	GSF clock gating 0: disabled 1: enabled
[0]	RW	gsf_srst_req	GSF soft reset 0: deassert reset 1: reset

PERI_CRG54

PERI_CRG54 is a DDRT clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ddrt_cken	ddrt_srst_req	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	ddrt_cken	DDRT clock gating 0: disabled 1: enabled
[2]	RW	ddrt_srst_req	DDRT soft reset 0: deassert reset 1: reset
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

PERI_CRG55

PERI_CRG55 is a PWM clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x00DC	PERI_CRG55	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												pwm_cksel		pwm_cken	pwm_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:2]	RW	pwm_cksel	PWM clock select 00: 3 MHz clock 01: 50 MHz clock 1X: 24 MHz clock
[1]	RW	pwm_cken	PWM clock gating 0: disabled 1: enabled
[0]	RW	pwm_srst_req	PWM soft reset 0: deassert reset 1: reset

PERI_CRG56

PERI_CRG56 is an RSA/TRNG/DMA clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00E0	PERI_CRG56	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rsa_cken	rsa_srst_req	trng_cken	trng_srst_req	reserved		dmac_cken	dmac_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rsa_cken	RSA clock gating 0: disabled 1: enabled
[6]	RW	rsa_srst_req	RSA soft reset 0: deassert reset 1: reset
[5]	RW	trng_cken	TRNG clock gating 0: disabled 1: enabled
[4]	RW	trng_srst_req	TRNG soft reset 0: deassert reset 1: reset
[3:2]	RO	reserved	Reserved
[1]	RW	dmac_cken	DMA clock gating 0: disabled 1: enabled
[0]	RW	dmac_srst_req	DMA soft reset 0: deassert reset 1: reset

PERI_CRG57

PERI_CRG57 is a clock soft reset control register for other APB modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x1FFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		pmc_srst_req	reserved	test_clk_en	i2c_cksel	uart_cksel	uart4_cken	uart3_cken	uart2_cken	uart1_cken	uart0_cken	ir_cken	ssp2_cken	ssp1_cken	ssp0_cken	reserved		i2c3_srst_req	uart4_srst_req	uart3_srst_req	uart2_srst_req	uart1_srst_req	uart0_srst_req	ir_srst_req	ssp2_srst_req	ssp1_srst_req	ssp0_srst_req	rtc_srst_req	i2c2_srst_req	i2c1_srst_req	i2c0_srst_req
Reset	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	pmc_srst_req	PMC soft reset 0: deassert reset 1: reset
[28]	RO	reserved	Reserved
[27]	RW	test_clk_en	Test clock enable 0: All test clocks are disabled. 1: All test clocks are enabled.
[26]	RW	i2c_cksel	I^2C clock select 0: reserved 1: 50 MHz clock
[25]	RW	uart_cksel	UART clock select 0: reserved 1: 24 MHz clock
[24]	RW	uart4_cken	UART4 clock gating 0: disabled 1: enabled
[23]	RW	uart3_cken	UART3 clock gating 0: disabled 1: enabled
[22]	RW	uart2_cken	UART2 clock gating 0: disabled 1: enabled
[21]	RW	uart1_cken	UART1 clock gating 0: disabled 1: enabled

[20]	RW	uart0_cken	UART0 clock gating 0: disabled 1: enabled
[19]	RW	ir_cken	IR clock gating 0: disabled 1: enabled
[18]	RW	ssp2_cken	SSP2 clock gating 0: disabled 1: enabled
[17]	RW	ssp1_cken	SSP1 clock gating 0: disabled 1: enabled
[16]	RW	ssp0_cken	SSP0 clock gating 0: disabled 1: enabled
[15]	RO	reserved	Reserved
[14]	RO	reserved	Reserved
[13]	RW	i2c3_srst_req	I^2C3 soft reset 0: deassert reset 1: reset
[12]	RW	uart4_srst_req	UART4 soft reset 0: deassert reset 1: reset
[11]	RW	uart3_srst_req	UART3 soft reset 0: deassert reset 1: reset
[10]	RW	uart2_srst_req	UART2 soft reset 0: deassert reset 1: reset
[9]	RW	uart1_srst_req	UART1 soft reset 0: deassert reset 1: reset
[8]	RW	uart0_srst_req	UART0 soft reset 0: deassert reset 1: reset

[7]	RW	ir_srst_req	IR soft reset 0: deassert reset 1: reset
[6]	RW	ssp2_srst_req	SSP2 soft reset 0: deassert reset 1: reset
[5]	RW	ssp1_srst_req	SSP1 soft reset 0: deassert reset 1: reset
[4]	RW	ssp0_srst_req	SSP0 soft reset 0: deassert reset 1: reset
[3]	RW	rtc_srst_req	T_CAP soft reset 0: deassert reset 1: reset
[2]	RW	i2c2_srst_req	I^2C2 soft reset 0: deassert reset 1: reset
[1]	RW	i2c1_srst_req	I^2C1 soft reset 0: deassert reset 1: reset
[0]	RW	i2c0_srst_req	I^2C0 soft reset 0: deassert reset 1: reset

PERI_CRG58

PERI_CRG58 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							gzip_rst_ok	reserved			epll_lock	vpll_lock	dpll_lock	reserved	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	gzip_rst_ok	GZIP reset status 0: not reset 1: reset
[7:5]	RO	reserved	Reserved
[4]	RO	epll_lock	EPLL lock status 0: unlocked 1: locked
[3]	RO	vpll_lock	VPLL lock status 0: unlocked 1: locked
[2]	RO	dpll_lock	DPLL lock status 0: unlocked 1: locked
[1]	RO	reserved	Reserved
[0]	RO	apll_lock	APLL lock status 0: unlocked 1: locked

PERI_CRG59

PERI_CRG59 is a GMAC interface control register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_CRG59	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							loopback_mode	phy_select			duplex_mode	tx_config	link_status	mac_speed	port_select
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	loopback_mode	Loopback mode enable 0: disabled 1: enabled
[7:5]	RW	phy_select	PHY interface mode 000: GMII/MII mode 001: RGMII mode 100: RMII mode Other values: reserved
[4]	RW	duplex_mode	PHY duplex mode 0: half-duplex mode 1: full-duplex mode
[3]	RW	tx_config	TX configuration enable 0: disabled 1: enabled
[2]	RW	link_status	PHY link status 0: link down 1: link up
[1]	RW	mac_speed	10/100 Mbit/s mode 0: 10 Mbit/s 1: 100 Mbit/s
[0]	RW	port_select	Network port mode select 0: 1000 Mbit/s 1: 10/100 Mbit/s

PERI_CRG60

PERI_CRG60 is a GMAC interface status register.

Offset Address	Register Name	Total Reset Value
0x00F0	PERI_CRG60	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				gmac_if_sys_stat			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	link_status	Link status when rxdv and rxer are 0 in RGMII mode 0: link down 1: link up
[2:1]	RO	link_speed	Rate status when rxdv and rxer are 0 in RGMII mode 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: reserved
[0]	RO	link_mode	Mode status when rxdv and rxer are 0 in RGMII mode 0: half-duplex mode 1: full-duplex mode

PERI_CRG79

PERI_CRG79 is an SoC frequency profile status register.

Offset Address	Register Name	Total Reset Value
0x013C	PERI_CRG79	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1 0
Name	reserved						bus_sc_seled	ddr_sc_seled	a17_sc_seled	a7_sc_seled
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved

[9]	RO	bus_sc_seled	Bus clock switching completion indicator 0: The clock is switched to a crystal oscillator clock. 1: The clock is switched to a 200 MHz clock.
[8:6]	RO	ddr_sc_seled	DDR clock switching completion indicator 000: The clock is switched to a crystal oscillator clock. 001: The clock is switched to the DPLL FOUTPOSTDIV clock. 010: The clock is switched to a 476 MHz clock. 011: The clock is switched to a 396 MHz clock. 100: The clock is switched to a 346 MHz clock. 101: The clock is switched to a 300 MHz clock. 110: The clock is switched to a 250 MHz clock. Other values: reserved
[5:3]	RO	a17_sc_seled	A17 clock switching completion indicator 000: The clock is switched to a crystal oscillator clock. 001: The clock is switched to the APLL FOUTVCOV clock. 010: The clock is switched to the DPLL FOUTVCO clock. 011: The clock is switched to a 1000 MHz clock. 100: The clock is switched to a 792 MHz clock. 101: The clock is switched to a 594 MHz clock. 110: The clock is switched to a 500 MHz clock. 111: The clock is switched to a 400 MHz clock.
[2:0]	RO	a7_sc_seled	A7 clock switching completion indicator 000: The clock is switched to a crystal oscillator clock. 001: The clock is switched to the DPLL FOUTVCO clock. 010: The clock is switched to the APLL FOUTPOSTDIV clock. 011: The clock is switched to a 792 MHz clock. 100: The clock is switched to a 750 MHz clock. 101: The clock is switched to a 594 MHz clock. Other values: reserved

3.3 Processor Subsystem

The Hi3519 V100 uses the ARMCortex-A17UP and Cortex-A7UP single-core processors with the HMP (asymmetric multi-core) architecture.

- The Cortex-A17UP processor has the following features:
  - Maximum 1200 MHz dominant working frequency, supporting dynamic voltage and frequency scaling (DVFS) and adaptive voltage scaling (AVS)
  - 32 KB L1 I-cache and 32 KB L1 D-cache
  - 256 KB L2 cache

  - 3.3 DMIPS/MHz performance
  - Integrated memory management unit (MMU)
  - Integrated NEON with the floating-point unit (FPU) coprocessor
- The Cortex-A7UP processor has the following features:
  - Maximum 800 MHz dominant working frequency, supporting dynamic frequency scaling (DFS)
  - 32 KB L1 I-cache and 32 KB L1 D-cache
  - 128 KB L2 cache
  - 1.9 DMIPS/MHz performance
  - Integrated MMU
  - Integrated NEON with the FPU coprocessor
- The HMP architecture has the following features:
  - A7/A17 big-little architecture
  - Dynamic enabling and disabling of the A17 core
  - Unified interrupt handling

3.4 Interrupt System

3.4.1 Interrupt Source Allocation

The Hi3519 V100 supports 128 interrupt sources. Table 3-7 describes the mapping between the interrupt bits and interrupt sources.

Table 3-7 Mapping between the interrupt bits and interrupt sources

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
0−31	CPU internal interrupt	67	VGS
32	WatchDog	68	AIAO
33	RTC/TEM_CAP	69	VEDU
34	Reserved	70	JPGE
35	Reserved	71	IVE
36	UART0	72	Reserved
37	UART1	73	GZIP
38	UART2	74	Software int
39	UART3	75	GPIO0−7
40	UART4	76	GPIO8−13
41	SSP0/I^2C0	77	A7_PMU
42	SSP1/I^2C1	78	A17_PMU
43	SSP2/I^2C2	79	CCI

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
44	I^2C3	80	GDC
45	eMMC	81	A17_COMMRX
46	Reserved	82	A17_COMMTX
47	IR	83	A7_COMMRX
48	SAR_ADC	84	A7_COMMTX
49	DMAC	85	Reserved
50	FMC	86	PCIE_CFG_LINK_AUTO_BW
51	USB2_EHCI	87	PCIE_CFG_BW_MGT
52	USB2_OHCI	88	PCIE_PM
53	USB2_DEV	89	PCIE_INTA
54	USB3	90	PCIE_INTB
55	SDIO0	91	PCIE_INTC
56	SDIO1	92	PCIE_INTD
57	GSF	93	PCIE_EDMA
58	Cipher	94	PCIE_MSI
59	VDP	95	PCIE_LINK_DOWN
60	MIPI	96	Timer0
61	Reserved	97	Timer1
62	VICAP	98	Timer2
63	Reserved	99	Timer3
64	VPSS	100	Timer4
65	Reserved	101	Timer5
66	TDE	102−127	Reserved

3.5 System Controller

3.5.1 Overview

The system controller manages important system functions and configures some functions of the peripherals.

3.5.2 Features

The system controller has the following features:

- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.5.3 Function Description

3.5.3.1 Soft Reset

The system controller can soft-reset the entire chip or some modules.

After the global soft reset register SC_SYSRES is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3519 V100.

3.5.3.2 System Address Remap Control

For details, see section 1.3 "Boot Modes."

3.5.3.3 Write Protection for Key Registers

To prevent the entire system from being affected by misoperations on the system controller, the system controller provides write protection for the key configuration register: global soft reset control register SC_SYSRES. You must configure SC_LOCKEN to enable the write permission before writing to SC_SYSRES. After the write operation is complete, you need to disable the write permission by configuring SC_LOCKEN, ensuring that SC_SYSRES is not incorrectly written by software.

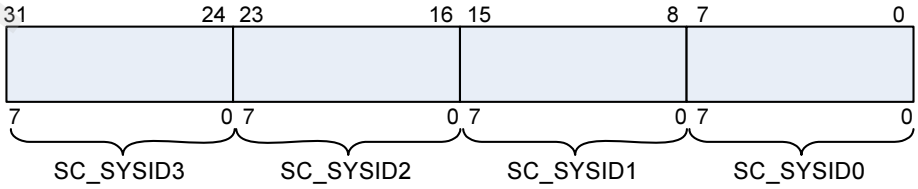
NOTE

By default, write protection is not enabled for key registers after reset. You are advised to enable write protection by configuring SC_LOCKEN when the system starts.

3.5.3.4 System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SCSYSID3, SCSYSID2, SCSYSID1, and SCSYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0x3519_0100, is obtained. Figure 3-4 shows the bit allocation of chip ID registers.

Figure 3-4 Bit allocation of chip ID registers



3.5.4 System Controller Registers

3.5.4.1 Register Summary

Table 3-8 describes system controller registers.

Table 3-8 Summary of system controller registers (base address: 0x1202_0000)

Offset Address	Register	Description	Page
0x000	SC_CTRL	System control register	3-60
0x004	SC_SYSRES	System soft reset register	3-62
0x001C	SOLFINT	Software interrupt register	3-63
0x0044	SC_LOCKEN	Key register lock register	3-63
0x008C	SYSSTAT	System status register (PLL_LOCK)	3-64
0xEE0	SCSYSID0	Chip ID register 0	3-66
0xEE4	SCSYSID1	Chip ID register 1	3-67
0xEE8	SCSYSID2	Chip ID register 2	3-67
0xEEC	SCSYSID3	Chip ID register 3	3-67

3.5.4.2 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations to be performed by the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					timeren5ov	reserved	timeren4ov	reserved	timeren3ov	reserved	timeren2ov	reserved	timeren1ov	reserved	timeren0ov	reserved	reserved					remapstat	remapclear	reserved								

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	timeren5ov	Timer 5 count clock select 0: 3 MHz clock 1: bus clock
[25]	RO	reserved	Reserved
[24]	RW	timeren4ov	Timer 4 count clock select 0: 3 MHz clock 1: bus clock
[23]	RO	reserved	Reserved
[22]	RW	timeren3ov	Timer 3 count clock select 0: 3 MHz clock 1: bus clock
[21]	RO	reserved	Reserved
[20]	RW	timeren2ov	Timer 2 count clock select 0: 3 MHz clock 1: bus clock
[19]	RW	reserved	Reserved
[18]	RW	timeren1ov	Timer 1 count clock select 0: 3 MHz clock 1: bus clock
[17]	RW	reserved	Reserved
[16]	RW	timeren0ov	Timer 0 count clock select 0: 3 MHz clock 1: bus clock
[15]	RW	reserved	Reserved
[14:10]	RO	reserved	Reserved. Reading this field returns 0, and writing to this field has no effect.
[9]	RO	remapstat	Address remap status 0: The address is not remapped. 1: The address is remapped. The BOOTROM, or FMC CS0 is remapped to address 0.

[8]	RW	remapclear	Address remap clear 0: The remap status is retained. 1: The remap status is cleared. For details about the address mapping relationships before and after remapping is cleared, see section 1.4 "Boot Mode" and section 1.5"Address Space Mapping" in chapter 1.
[7:0]	RO	reserved	Reserved

SC_SYSRES

SC_SYSRES is a system soft reset register. When a value is written to this register, the system controller sends a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	Writing any value to this register soft-resets the system.

SOLFINT

SOLFINT is a software interrupt register.

Offset Address	Register Name	Total Reset Value
0x001C	SOLFINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															software_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	software_int	Software interrupt 0: No interrupt is generated. 1: An interrupt is generated.

SC_LOCKEN

SC_LOCKEN is a key register lock registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL and SYSSTAT. When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status but not the written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

SYSSTAT

SYSSTAT is a system status register (PLL_LOCK).

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bootrom_sel_in	a17_standbywfil	a17_standbywfe	a17_standbywfi	a7_standbywfil2	a7_standbywfe	a7_standbywfi	reserved	update_from_sdio0	pcie_ref_clk_sel	combo_phy_mode_sel	reserved													sfc_emmc_boot_mode	reserved	boot_mode		sfc_device_mode	spi_nand_sel	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	bootrom_sel_in	Whether the system boots from the BOOTROM 0: no 1: yes
[30]	RW	a17_standbywfil2	Whether the A17 L2 is in wait for interrupt (WFI) status 0: no 1: yes
[29]	RW	a17_standbywfe	Whether the A17 is in wait for event (WFE) status 0: no 1: yes
[28]	RW	a17_standbywfi	Whether the A17 is in WFI status 0: no 1: yes
[27]	RW	a7_standbywfil2	Whether the A7 L2 is in WFI status 0: no 1: yes
[26]	RW	a7_standbywfe	Whether the A7 is in WFE status 0: no 1: yes
[25]	RW	a7_standbywfi	Whether the A7 is in WFI status 0: no 1: yes
[24]	RO	reserved	Reserved

[23]	RO	update_from_sdio0	Whether to upgrade the firmware by using the SDIO0 0: no 1: yes For details, see the description of the boot_mode register.
[22]	RO	pcie_ref_clk_sel	Reference clock select for the PCIe PHY 0: internal CRG clock 1: external input clock
[21]	RO	combo_phy_mode_sel	COMBO PHY mode 0: PCIe mode 1: USB 3.0 mode
[20:8]	RO	reserved	Reserved
[7]	RO	sfc_emmc_boot_mode	Boot address mode of the SPI NOR flash when boot_mode is 2'b00 and sfc_device_mode is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when boot_mode is 2'b00 and sfc_device_mode is 1 0: 1-wire boot mode 1: 4-wire boot mode eMMC boot mode when boot_mode is 2'b10 0: 4-wire boot mode 1: 8-wire boot mode
[6]	RO	reserved	Reserved

[5:4]	RO	boot_mode	Chip boot mode When bootrom_sel is 0 00: booting from the SPI flash 01: booting from the NAND flash 10: booting from the eMMC 11: booting from a DDR of the slave chip over the PCIe interface When bootrom_sel is 1 and update_from_sdio is 0 00: entering the fastboot mode and skipping to boot from the SPI flash when timeout occurs 01: entering the fastboot mode and skipping to boot from the NAND flash when timeout occurs 10: entering the fastboot mode and skipping to boot from the eMMC when timeout occurs 11: reserved When bootrom_sel and update_from_sdio0 are 1 00: The firmware is upgraded from the SDIO0 to the SPI flash. 01: The firmware is upgraded from the SDIO0 to the NAND flash. 10: The firmware is upgraded from the SDIO0 to the eMMC. 11: reserved
[3]	RW	sfc_device_mode	SPI flash select 0: SPI NOR flash 1: SPI NAND flash
[2]	RO	spi_nand_sel	Timing select for the SPI NAND flash 0: The plane address bit is disabled. 1: The plane address bit is enabled.
[1:0]	RO	reserved	Reserved

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chipid								reserved																sysid0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	chipid	Version
[23:8]	RO	reserved	Reserved

[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0x01

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0x01.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x19

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	0	1	1	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x19.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							

Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5.5 Peripheral Control Registers

3.5.5.1 Register Summary

Table 3-9 describes peripheral control registers.

Table 3-9 Summary of peripheral control registers (base address: 0x1203_0000)

Offset Address	Register	Description	Page
0x0000	MISC_CTRL0	VICAP/VPSS/MIPI PHY control register	3-70
0x0004	MISC_CTRL1	Peripheral function selection register 0	3-71
0x0008	MISC_CTRL2	PCIe read outstanding limit control register	3-74
0x000C	MISC_CTRL3	Power switch control register	3-74
0x0010	MISC_CTRL4	RET1N control register	3-76
0x0014	MISC_CTRL5	System bus arbitration control register 0	3-77
0x0018	MISC_CTRL6	System bus arbitration control register 1	3-78
0x001C	MISC_CTRL7	System bus arbitration control register 2	3-78
0x0020	MISC_CTRL8	System bus priority control register 0	3-79
0x0024	MISC_CTRL9	System bus priority control register 1	3-80
0x002C	MISC_CTRL11	Media 0 bus arbitration control register 0	3-81
0x0030	MISC_CTRL12	Media 0 bus arbitration control register 1	3-82
0x0038	MISC_CTRL14	Media 0 bus priority control register	3-83
0x003C	MISC_CTRL15	Media 1 bus arbitration control register 0	3-84
0x0040	MISC_CTRL16	Media 1 bus arbitration control register 1	3-86
0x0048	MISC_CTRL18	Media 1 bus priority control register	3-87
0x0054	MISC_CTRL21	DDR QoS control register 0	3-87

Offset Address	Register	Description	Page
0x0058	MISC_CTRL22	DDR QoS control register 1	3-88
0x005C	MISC_CTRL23	DDR QoS control register 2	3-88
0x0060	MISC_CTRL24	DDR QoS control register 3	3-89
0x0074	MISC_CTRL29	USB 3.0 control register	3-90
0x0078	MISC_CTRL30	USB 2.0 control register 0	3-91
0x007C	MISC_CTRL31	Test clock and USB 2.0 PHY access test channel mode selection register	3-94
0x0080	MISC_CTRL32	USB 2.0 PHY test channel register	3-94
0x0084	MISC_CTRL33	COMB PHY test channel register	3-95
0x0088	MISC_CTRL34	PCIe and USB 3.0 PHY control register	3-96
0x00A0	MISC_CTRL40	Audio CODEC fast power-on and power-off control register 0	3-98
0x00A4	MISC_CTRL42	Audio CODEC fast power-on and power-off control register 1	3-98
0x00A8	MISC_CTRL43	Audio CODEC fast power-on and power-off control register 2	3-100
0x00AC	MISC_CTRL41	Audio CODEC fast power-on and power-off control register 3	3-101
0x00B0	MISC_CTRL44	Audio CODEC fast power-on and power-off control register 4	3-102
0x00B4	MISC_CTRL45	Audio CODEC ANA register 0	3-103
0x00B8	MISC_CTRL46	Audio CODEC ANA register 1	3-105
0x00BC	MISC_CTRL47	Audio CODEC ANA register 2	3-107
0x00C0	MISC_CTRL48	Audio CODEC ANA register 3	3-108
0x00CC	MISC_CTRL51	Audio CODEC DIG control register 0	3-109

Offset Address	Register	Description	Page
0x00D0	MISC_CTRL52	Audio CODEC DIG control register 1	3-111
0x00D4	MISC_CTRL53	Audio CODEC DIG control register 2	3-112
0x00D8	MISC_CTRL54	Audio CODEC DIG control register 3	3-113
0x00E0	MISC_CTRL56	I^2S channel selection control register	3-114
0x00F0	MISC_CTRL60	Core layer memory high-speed control register 0	3-115
0x00F4	MISC_CTRL61	Core layer memory high-speed control register 1	3-116
0x0140	MISC_CTRL80	eMMC DLL control register 0	3-117
0x0144	MISC_CTRL81	eMMC DLL control register 1	3-118
0x0154	MISC_CTRL85	Peripheral bus arbitration control register 0	3-119
0x0158	MISC_CTRL86	Peripheral bus arbitration control register 1	3-120
0x0160	MISC_CTRL88	Peripheral bus priority control register 0	3-120
0x0164	MISC_CTRL89	Peripheral bus priority control register 1	3-121
0x0174	MISC_CTRL93	VO_AIO bus arbitration control register	3-122
0x0178	MISC_CTRL94	VO_AIO bus priority control register	3-123

3.5.5.2 Register Description

MISC_CTRL0

MISC_CTRL0 is a VICAP/VPSS/MIPI PHY control register.

Offset Address	Register Name	Total Reset Value
0x0000	MISC_CTRL0	0x0000_0054

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep000																						vicap0_vpss0_online	reserved	mipi0_work_mode				reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved_keep000	Reserved
[9]	RW	vicap0_vpss0_online	VICAP0/VPSS0 mode 0: offline mode 1: online mode
[8]	RO	reserved	Reserved
[7:6]	RW	mipi0_work_mode	MIPI0 mode select 00: MIPI mode 01: LVDS mode 10: CMOS mode 11: reserved
[5:0]	RW	reserved	Reserved

MISC_CTRL1

MISC_CTRL1 is peripheral function selection register 0.

Offset Address	Register Name	Total Reset Value
0x0004	MISC_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ssp1_cs_sel		reserved	dma_01_sel	reserved		dma_89_sel	dma_ab_sel	dma_cd_sel	reserved			bootrom_pg	reserved	spi2_cs0_ctrl		spi1_cs1_ctrl		spi1_cs0_ctrl		spi0_cs0_ctrl		uart1_rst_ctrl	uart2_rst_ctrl	bootram3_ck_gt_en	bootram2_ck_gt_en	bootram1_ck_gt_en	bootram0_ck_gt_en	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RO	reserved	Reserved
[29]	RO	reserved	Reserved
[28]	RO	reserved	Reserved
[27:26]	RW	ssp1_cs_sel	SSP1 output CS select 00: CS0 01: CS1 1X: reserved
[25]	RO	reserved	Reserved
[24]	RW	dma_01_sel	Connection select for the DMA hardware request lines 0 and 1 0: UART0 connects to DMA hardware request lines 0 and 1. 1: UART4 connects to DMA hardware request lines 0 and 1.
[23:22]	RO	reserved	Reserved
[21]	RW	dma_89_sel	Connection select for the DMA hardware request lines 8 and 9 0: I^2C0 connects to DMA hardware request lines 8 and 9. 1: SSP0 connects to DMA hardware request lines 8 and 9.
[20]	RW	dma_ab_sel	Connection select for the DMA hardware request lines 10 and 11 0: I^2C1 connects to DMA hardware request lines 10 and 11. 1: SSP1 connects to DMA hardware request lines 10 and 11.
[19]	RW	dma_cd_sel	Connection select for the DMA hardware request lines 12 and 13 0: I^2C2 connects to DMA hardware request lines 12 and 13. 1: SSP2 connects to DMA hardware request lines 12 and 13.
[18:14]	RO	reserved	Reserved

[13]	RW	bootrom_pg	BOOTROM low-power mode control 0: normal mode 1: low-power mode
[12]	RO	reserved	Reserved
[11]	RW	spi2_cs0_ctrl	Phase inversion control for the spi2_cs0 signal 0: not inverted 1: inverted
[10]	RW	spi1_cs1_ctrl	Phase inversion control for the spi1_cs1 signal 0: not inverted 1: inverted
[9]	RW	spi1_cs0_ctrl	Phase inversion control for the spi1_cs0 signal 0: not inverted 1: inverted
[8]	RW	spi0_cs0_ctrl	Phase inversion control for the spi0_cs0 signal 0: not inverted 1: inverted
[7]	RW	uart1_rst_ctrl	Phase inversion control for the uart1_rst signal 0: not inverted 1: inverted
[6]	RW	uart2_rst_ctrl	Phase inversion control for the uart2_rst signal 0: not inverted 1: inverted
[5]	RW	bootram3_ck_gt_en	BOOTRAM3 clock enable 0: enabled 1: disabled
[4]	RW	bootram2_ck_gt_en	BOOTRAM2 clock enable 0: enabled 1: disabled
[3]	RW	bootram1_ck_gt_en	BOOTRAM1 clock enable 0: enabled 1: disabled
[2]	RW	bootram0_ck_gt_en	BOOTRAM0 clock enable 0: enabled 1: disabled
[1:0]	RO	reserved	Reserved

MISC_CTRL2

MISC_CTRL2 is a PCIe read outstanding limit control register.

Offset Address	Register Name	Total Reset Value
0x0008	MISC_CTRL2	0x0000_0104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep001																							pcie_m_od_bypass_limit	pcie_m_od_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved_keep001	Reserved
[8]	RW	pcie_m_od_bypass_limit	PCIe master read outstanding limit enable 1: disabled 0: enabled
[7:0]	RW	pcie_m_od_max	Number of PCIe master read outstandings. This field cannot be set to 0. The value that takes effect is the configured value plus 1.

MISC_CTRL3

MISC_CTRL3 is a power switch control register.

Offset Address	Register Name	Total Reset Value
0x000C	MISC_CTRL3	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								powerswitch1_enable_mux	powerswitch0_enable_mux	powerswitch1_enable	powerswitch0_enable	powerswitch1_sel_mux	powerswitch1_sel	powerswitch0_sel_mux	powerswitch0_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	powerswitch1_enable_mux	Power switch 1 enable source select 0: SDIO1 controller 1: powerswitch1_enable register
[6]	RW	powerswitch0_enable_mux	Power switch 0 enable source select 0: SDIO0 controller 1: powerswitch0_enable register
[5]	RW	powerswitch1_enable	Power switch 1 enable (valid only when powerswitch1_enable_mux is 1) 0: disabled 1: enabled
[4]	RW	powerswitch0_enable	Power switch 0 enable (valid only when powerswitch0_enable_mux is 1) 0: disabled 1: enabled
[3]	RW	powerswitch1_sel_mux	Power switch 1 switch source select 0: SDIO1 controller 1: powerswitch1_sel register
[2]	RW	powerswitch1_sel	Power switch 1 output voltage select (valid only when powerswitch1_sel_mux is 1) 0: 3.3 V 1: 1.8 V

[1]	RW	powerswitch0_sel_mux	Power switch 0 switch source select 0: SDIO0 controller 1: powerswitch0_sel register
[0]	RW	powerswitch0_sel	Power switch 0 output voltage select (valid only when powerswitch0_sel_mux is 1) 0: 3.3 V 1: 1.8 V

MISC_CTRL4

MISC_CTRL4 is an RET1N control register.

Offset Address	Register Name	Total Reset Value
0x0010	MISC_CTRL4	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vedu_ret1n_bypass	reserved																							emmc_ret1n	sdio1_ret1n	sdio0_ret1n	reserved		reserved	cipher_ret1n	bootram_ret1n
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	vedu_ret1n_bypass	Automatic memory RET1N function bypass for the VEDU module 0: enabled 1: bypassed
[30:8]	RO	reserved	Reserved
[7]	RW	emmc_ret1n	Memory RET1N signal in the eMMC CTRL. Set this bit to 1 when the eMMC CTRL is enabled and set this bit to 0 when the eMMC CTRL is disabled to reduce memory power consumption.
[6]	RW	sdio1_ret1n	Memory RET1N signal in the SDIO1 CTRL. Set this bit to 1 when the SDIO1 CTRL is enabled and set this bit to 0 when the SDIO1 CTRL is disabled to reduce memory power consumption.
[5]	RW	sdio0_ret1n	Memory RET1N signal in the SDIO0 CTRL. Set this bit to 1 when the SDIO0 CTRL is enabled and set this bit to 0 when the SDIO0 CTRL is disabled to reduce memory power consumption.
[4]	RO	reserved	Reserved
[3]	RO	reserved	Reserved

[2]	RO	reserved	Reserved
[1]	RW	cipher_ret1n	Memory RET1N signal in the cipher. Set this bit to 1 when the cipher is enabled and set this bit to 0 when the cipher is disabled to reduce memory power consumption.
[0]	RW	bootram_ret1n	Memory RET1N signal in the BOOTRAM. Set this bit to 1 when the BOOTRAM is enabled and set this bit to 0 when the BOOTRAM is disabled to reduce memory power consumption.

MISC_CTRL5

MISC_CTRL5 is system bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0014	MISC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysaxi_timeout_en_m2	sysaxi_timeout_value_m2															sysaxi_timeout_en_m1	sysaxi_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_m2	Timeout count enable for the SYS AXI bus M2 port (AHB1) 0: disabled 1: enabled
[30:16]	RW	sysaxi_timeout_value_m2	Timeout count value of the SYS AXI bus M2 port (AHB1) Count value = sysaxi_timeout_value_m2 x 2
[15]	RW	sysaxi_timeout_en_m1	Timeout count enable for the SYS AXI bus M1 port (AHB0) 0: disabled 1: enabled
[14:0]	RW	sysaxi_timeout_value_m1	Timeout count value of the SYS AXI bus M1 port (AHB0) Count value = sysaxi_timeout_value_m1 x 2

MISC_CTRL6

MISC_CTRL6 is system bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0018	MISC_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				sysaxi_timeout_value_m4												sysaxi_timeout_en_m3				sysaxi_timeout_value_m3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_m4	Timeout count enable for the SYS AXI bus M4 port (USB3.0) 0: disabled 1: enabled
[30:16]	RW	sysaxi_timeout_value_m4	Timeout count value of the SYS AXI bus M4 port (USB3.0) Count value = sysaxi_timeout_value_m4 x 2
[15]	RW	sysaxi_timeout_en_m3	Timeout count enable for the SYS AXI bus M3 port (GSF) 0: disabled 1: enabled
[14:0]	RW	sysaxi_timeout_value_m3	Timeout count value of the SYS AXI bus M3 port (GSF) Count value = sysaxi_timeout_value_m3 x 2

MISC_CTRL7

MISC_CTRL7 is system bus arbitration control register 2.

Offset Address	Register Name	Total Reset Value
0x001C	MISC_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysaxi_timeout_en_m6	sysaxi_timeout_value_m6															sysaxi_timeout_en_m5	sysaxi_timeout_value_m5														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_timeout_en_m6	Timeout count enable for the SYS AXI bus M6 port (AHB2) 0: disabled 1: enabled
[30:16]	RW	sysaxi_timeout_value_m6	Timeout count value of the SYS AXI bus M6 port (AHB2) Count value = sysaxi_timeout_value_m6 x 2
[15]	RW	sysaxi_timeout_en_m5	Timeout count enable for the SYS AXI bus M5 port (PCIe) 0: disabled 1: enabled
[14:0]	RW	sysaxi_timeout_value_m5	Timeout count value of the SYS AXI bus M5 port (PCIe) Count value = sysaxi_timeout_value_m5 x 2

MISC_CTRL8

MISC_CTRL8 is system bus priority control register 0.

Offset Address	Register Name	Total Reset Value
0x0020	MISC_CTRL8	0x0001_2345

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									sysaxi_port6_pri			reserved	sysaxi_port5_pri			reserved	sysaxi_port4_pri			reserved	sysaxi_port3_pri			reserved	sysaxi_port2_pri			reserved	sysaxi_port1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	sysaxi_port6_pri	Priority of the SYS AXI bus M6 port (AHB2) The value 7 indicates the highest priority.
[19]	RO	reserved	Reserved
[18:16]	RW	sysaxi_port5_pri	Priority of the SYS AXI bus M5 port (PCIe) The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved
[14:12]	RW	sysaxi_port4_pri	Priority of the SYS AXI bus M4 port (USB3.0) The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	sysaxi_port3_pri	Priority of the SYS AXI bus M3 port (GSF) The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	sysaxi_port2_pri	Priority of the SYS AXI bus M2 port (AHB1) The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	sysaxi_port1_pri	Priority of the SYS AXI bus M1 port (AHB0) The value 7 indicates the highest priority.

MISC_CTRL9

MISC_CTRL9 is system bus priority control register 1.

Offset Address	Register Name	Total Reset Value
0x0024	MISC_CTRL9	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sysaxi_slave_priority_s2				reserved			sysaxi_slave_priority_s1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	sysaxi_slave_priority_s2	Bus access priority of the SYS AXI s2 (peri_axi) port The value 3 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	sysaxi_slave_priority_s1	Bus access priority of the SYS AXI s1 (mddrc) port The value 3 indicates the highest priority.

MISC_CTRL11

MISC_CTRL11 is media 0 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x002C	MISC_CTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media0axi_timeout_en_m2				media0axi_timeout_value_m2												media0axi_timeout_en_m1				media0axi_timeout_value_m1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media0axi_timeout_en_m2	Timeout count enable for the media 0 AXI bus M2 port (VGS) 0: disabled 1: enabled
[30:16]	RW	media0axi_timeout_value_m2	Timeout count value of the media 0 AXI bus M2 port (VGS) Count value = media0axi_timeout_value_m2 x 2
[15]	RW	media0axi_timeout_en_m1	Timeout count enable for the media 0 AXI bus M1 port (VEDU) 0: disabled 1: enabled
[14:0]	RW	media0axi_timeout_value_m1	Timeout count value of the media 0 AXI bus M1 port (VEDU) Count value = media0axi_timeout_value_m1 x 2

MISC_CTRL12

MISC_CTRL12 is media 0 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0030	MISC_CTRL12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep0																media0axi_timeout_en_m3	media0axi_timeout_value_m3														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved_keep0	Reserved
[15]	RW	media0axi_timeout_en_m3	Timeout count enable for the media 0 AXI bus M3 port (GDC) 0: disabled 1: enabled
[14:0]	RW	media0axi_timeout_value_m3	Timeout count value of the media 0 AXI bus M3 port (GDC) Count value = media0axi_timeout_value_m1 x 2

MISC_CTRL14

MISC_CTRL14 is a media 0 bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0038	MISC_CTRL14	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					media0axi_port3_pri			reserved	media0axi_port2_pri			reserved	media0axi_port1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	media0axi_port3_pri	Priority of the media 0 AXI bus M3 port (GDC) The value 3 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	media0axi_port2_pri	Priority of the media 0 AXI bus M2 port (VGS) The value 3 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	media0axi_port1_pri	Priority of the media 0 AXI bus M1 port (VEDU) The value 3 indicates the highest priority.

MISC_CTRL15

MISC_CTRL15 is media 1 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x003C	MISC_CTRL15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media1axi_timeout_en_m2	media1axi_timeout_value_m2															media1axi_timeout_en_m1	media1axi_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media1axi_timeout_en_m2	Timeout count enable for the media 1 AXI bus M2 port (JPGE) 0: disabled 1: enabled
[30:16]	RW	media1axi_timeout_value_m2	Timeout count value of the media 1 AXI bus M2 port (JPGE) Count value = media1axi_timeout_value_m2 x 2
[15]	RW	media1axi_timeout_en_m1	Timeout count enable for the media 1 AXI bus M1 port (TDE) 0: disabled 1: enabled
[14:0]	RW	media1axi_timeout_value_m1	Timeout count value of the media 1 AXI bus M1 port (TDE) Count value = media1axi_timeout_value_m1 x 2

MISC_CTRL16

MISC_CTRL16 is media 1 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0040	MISC_CTRL16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media1axi_timeout_en_m4	media1axi_timeout_value_m4															media1axi_timeout_en_m3	media1axi_timeout_value_m3														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media1axi_timeout_en_m4	Timeout count enable for the media 1 AXI bus M4 port (GZIP) 0: disabled 1: enabled
[30:16]	RW	media1axi_timeout_value_m4	Timeout count value of the media 1 AXI bus M4 port (GZIP) Count value = media1axi_timeout_value_m4 x 2
[15]	RW	media1axi_timeout_en_m3	Timeout count enable for the media 1 AXI bus M3 port (IVE) 0: disabled 1: enabled
[14:0]	RW	media1axi_timeout_value_m3	Timeout count value of the media 1 AXI bus M3 port (IVE) Count value = media1axi_timeout_value_m3 x 2

MISC_CTRL18

MISC_CTRL18 is a media 1 bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0048	MISC_CTRL 18	0x0001_2345

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	media1axi_port4_pri			reserved			media1axi_port3_pri			reserved			media1axi_port2_pri			reserved			media1axi_port1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	media1axi_port4_pri	Priority of the media 1 AXI bus M4 port (GZIP) The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	media1axi_port3_pri	Priority of the media 1 AXI bus M3 port (IVE) The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	media1axi_port2_pri	Priority of the media 1 AXI bus M2 port (JPGE) The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	media1axi_port1_pri	Priority of the media 1 AXI bus M1 port (TDE) The value 7 indicates the highest priority.

MISC_CTRL21

MISC_CTRL21 is DDR QoS control register 0.

Offset Address	Register Name	Total Reset Value
0x0054	MISC_CTRL21	0x0004_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep4																				gzip_qosmap				reserved				pcie_qosmap			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	gzip_qosmap	QoS value of the GZIP in the MDDRC
[7:4]	RO	reserved	Reserved
[3:0]	RW	pcie_qosmap	QoS value of the PCIe in the MDDRC

MISC_CTRL22

MISC_CTRL22 is DDR QoS control register 1.

Offset Address	Register Name	Total Reset Value
0x0058	MISC_CTRL22	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hash_qosmap				ive_qosmap				aio_qosmap				jpge_qosmap				tde_qosmap				vicap_qosmap				vdp_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	hash_qosmap	QoS value of the HASH in the MDDRC
[23:20]	RW	ive_qosmap	QoS value of the IVE in the MDDRC
[19:16]	RW	aio_qosmap	QoS value of the AIAO in the MDDRC
[15:12]	RW	jpge_qosmap	QoS value of the JPGE in the MDDRC
[11:8]	RW	tde_qosmap	QoS value of the TDE in the MDDRC
[7:4]	RW	vicap_qosmap	QoS value of the VICAP in the MDDRC
[3:0]	RW	vdp_qosmap	QoS value of the VDP in the MDDRC

MISC_CTRL23

MISC_CTRL23 is DDR QoS control register 2.

Offset Address	Register Name	Total Reset Value
0x005C	MISC_CTRL23	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emmc_qosmap				reserved				fmc_qosmap				sdio1_qosmap				sdio0_qosmap				cpu_qosmap				vpss_qosmap				vgs_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	emmc_qosmap	QoS value of the eMMC in the MDDRC
[27:24]	RO	reserved	Reserved
[23:20]	RW	fmc_qosmap	QoS value of the FMC in the MDDRC
[19:16]	RW	sdio1_qosmap	QoS value of SDIO1 in the MDDRC
[15:12]	RW	sdio0_qosmap	QoS value of SDIO0 in the MDDRC
[11:8]	RW	cpu_qosmap	QoS value of the CPU in the MDDRC
[7:4]	RW	vpss_qosmap	QoS value of the VPSS in the MDDRC
[3:0]	RW	vgs_qosmap	QoS value of the VGS in the MDDRC

MISC_CTRL24

MISC_CTRL24 is DDR QoS control register 3.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gdc_qosmap				usb3_qosmap				vedu_qosmap				usb2_qosmap				cipher_qosmap				dma2_qosmap				dma1_qosmap				gsf_qosmap			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	gdc_qosmap	QoS value of the GDC in the MDDRC
[27:24]	RW	usb3_qosmap	QoS value of USB 3.0 in the MDDRC
[23:20]	RW	vedu_qosmap	QoS value of the VEDU in the MDDRC
[19:16]	RW	usb2_qosmap	QoS value of USB 2.0 in the MDDRC
[15:12]	RW	cipher_qosmap	QoS value of the cipher in the MDDRC
[11:8]	RW	dma2_qosmap	QoS value of DMA 2 in the MDDRC
[7:4]	RW	dma1_qosmap	QoS value of DMA 1 in the MDDRC
[3:0]	RW	gsf_qosmap	QoS value of the GSF in the MDDRC

MISC_CTRL29

MISC_CTRL29 is a USB 3.0 control register.

Offset Address	Register Name	Total Reset Value
0x0074	MISC_CTRL29	0x0004_0FD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												usb3_host_port_power_control_present	usb3_fladj_30mhz_reg						usb3_host_msi_enable	usb3_bus_filter_bypass				usb3_port_ovrcur_pol	usb3_port_pwren_pol	usb3_port_ovrcur_ctrl_en	usb3_port_pwr_ctrl_en	usb3_host_u3_port_disable	usb3_host_u2_port_disable	usb3_hub_port_perm_attach	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	usb3_host_port_power_control_present	Whether the USB 3.0 port has a power control switch 0: The port has no power control switch, and USB device is always supplied with power. 1: The port has a power control switch to control the power supplied to the USB device.
[18:13]	RW	usb3_fladj_30mhz_reg	HS clock jitter control Indicates the correction required to accommodate mac3 clock and UTMI clock jitter to measure 125 µs duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933 ns. The value needs to be programmed in terms of high-speed bit times in a 30 MHz cycle.
[12]	RW	usb3_host_msi_enable	Interrupt type of the USB 3.0 port 0: level type 1: pulse type
[11:8]	RW	usb3_bus_filter_bypass	USB 3.0 bus filter bypass. This field must be set to 4'b1111.
[7]	RW	usb3_port_ovrcur_pol	Over-current protection polarity control for the USB 3.0 port 0: active low 1: active high

[6]	RW	usb3_port_pwren_pol	Power enable polarity control for the USB 3.0 port 0: active low 1: active high
[5]	RW	usb3_port_ovrcur_ctrl_en	Over-current protection enable of the USB 3.0 port 0: disabled 1: enabled
[4]	RW	usb3_port_pwr_ctrl_en	USB 3.0 port power enable 0: disabled 1: enabled (output by the USB 3.0 controller)
[3]	RW	usb3_host_u3_port_disable	USB 3.0 (SS) port disable 0: enabled 1: disabled
[2]	RW	usb3_host_u2_port_disable	USB 2.0 (HS) port disable 0: enabled 1: disabled
[1:0]	RW	usb3_hub_port_perm_attach	Whether the downstream port device is permanently attached to the USB 3.0 port 0: no 1: yes

MISC_CTRL30

MISC_CTRL30 is USB 2.0 control register 0.

Offset Address	Register Name	Total Reset Value
0x0078	MISC_CTRL30	0x0C03_13A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb_chipid	reserved			usb2_phy_dmpulldown	usb2_phy_dppulldown	ss_scaledown_mode		reserved	ss_hubsetup_min_i	reserved		usbovr_p_ctrl	usbpwr_pctrl			reserved	port_ovr_en	reserved	port_pwr_en	reserved		ss_ena_incr16_i	ss_ena_incr8_i	ss_ena_incr4_i	ss_ena_incr_align_i	ss_autoppd_on_overcur_en_i	reserved			app_start_clk_i	ohci_susp_lgcy_i	ss_word_if_i
Reset	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	usb_chipid	USB2.0 host and device switching control 0: host 1: device
[30:28]	RO	reserved	Reserved
[27]	RW	usb2_phy_dmpulldown	D− pull-down resistor enable 0: disabled 1: enabled
[26]	RW	usb2_phy_dppulldown	D+ pull-down resistor enable 0: disabled 1: enabled
[25:24]	RW	ss_scaledown_mode	Scale-down mode 00: Scale-down is disabled for all timings, and the actual timings are used. 01: Scale-down is enabled for all timings except the suspended and resumed timings in device mode. 10: Scale-down is enabled only for the suspended and resumed timings in device mode. 11: Scale-down timings of bit 0 and bit 1 are enabled.
[23]	RO	reserved	Reserved
[22]	RW	ss_hubsetup_min_i	Number of idle cycles after the full-speed preamble packet 0: five idle full-speed cycles 1: four full-speed idle cycles
[21:18]	RO	reserved	Reserved

[17]	RW	usbovr_p_ctrl	Over-current protection polarity 0: active low 1: active high
[16]	RW	usbpwr_pctrl	USB 2.0 PHY power shutdown polarity 0: active low 1: active high
[15]	RO	reserved	Reserved
[14]	RW	port_ovr_en	Over-current protection enable for the USB 2.0 PHY 0: disabled 1: enabled
[13]	RO	reserved	Reserved
[12]	RW	port_pwr_en	USB 2.0 PHY power shutdown control 0: The power is shut down. 1: The controller power output is enabled.
[11:10]	RO	reserved	Reserved
[9]	RW	ss_ena_incr16_i	AHB burst16 enable 0: disabled 1 (default): enabled
[8]	RW	ss_ena_incr8_i	AHB burst8 enable 0: disabled 1 (default): enabled
[7]	RW	ss_ena_incr4_i	AHB burst4 enable 0: disabled 1 (default): enabled
[6]	RW	ss_ena_incr_align_i	Burst alignment enable 0 (default): disabled 1: enabled
[5]	RW	ss_autoppd_on_overcur_en_i	Automatic port power shutdown enable during over-current 0: disabled 1 (default): enabled
[4:3]	RO	reserved	Reserved
[2]	RW	app_start_clk_i	Open host controller interface (OHCI) clock control 0 (default): The OHCI works normally. 1: The OHCI clock is enabled in suspend mode.
[1]	RW	ohci_susp_lgcy_i	Strap input signal when the OHCI is suspended

[0]	RW	ss_word_if_i	Data bit width select for the UTMI interface 0 (default): 8 bits 1: 16 bits

MISC_CTRL31

MISC_CTRL31 is a test clock and USB 2.0 PHY access test channel mode selection register.

Offset Address	Register Name	Total Reset Value
0x007C	MISC_CTRL31	0x3323_8A00

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved_keep7							test_clk_sel
Reset	0 0 1 1	0 0 1 1	0 0 1 0	0 0 1 1	1 0 0 0	1 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RO	reserved_keep7	Reserved
[3:0]	RW	test_clk_sel	Test clock select 0x0: pll_test_out[0] 0x1: pll_test_out[1] 0x2: pll_test_out[2] 0x3: pll_test_out[3] 0x4: pll_test_out[4] 0x5: clk_test_out[0] 0x6: clk_test_out[1] 0x7: clk_test_out[2] 0x8: clk_24m 0x9: clk_rtc_out 0xA: rtc_iso 0xB: audio_codec_mclk Other values: reserved

MISC_CTRL32

MISC_CTRL32 is a USB 2.0 PHY test channel register.

Offset Address	Register Name	Total Reset Value
0x0080	MISC_CTRL32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb2_phy_testdataout								usb2_phy_test_rstn	reserved	usb2_phy_wren	reserved	usb2_phy_testaddr												usb2_phy_testdatain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	usb2_phy_testdataout	USB 2.0 PHY read test data bus
[23]	RW	usb2_phy_test_rstn	USB 2.0 PHY read test interface reset 0: reset 1: not reset
[22]	RO	reserved	Reserved
[21]	RW	usb2_phy_wren	Read/Write control signal of the USB 2.0 PHY test interface register. If the value is changed from 0 to 1, the write operation is performed; if the value is 0, the read operation is performed.
[20:19]	RO	reserved	Reserved
[18:8]	RW	usb2_phy_testaddr	Address for the USB 2.0 PHY test interface register
[7:0]	RW	usb2_phy_testdatain	USB 2.0 PHY write test data bus

MISC_CTRL33

MISC_CTRL33 is a COMB PHY test channel register.

Offset Address	Register Name	Total Reset Value
0x0084	MISC_CTRL33	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep8															comb_phy_test_write	reserved				comb_phy_test_addr				comb_phy_test_o				comb_phy_test_i			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved_keep8	Reserved
[16]	RW	comb_phy_test_write	Read/Write control for the COMB PHY test register 0: read enable 1: write enable
[15:13]	RO	reserved	Reserved
[12:8]	RW	comb_phy_test_addr	Address of the COMB PHY test register
[7:4]	RO	comb_phy_test_o	Read data of the COMB PHY test register
[3:0]	RW	comb_phy_test_i	Write data of the COMB PHY test register

MISC_CTRL34

MISC_CTRL34 is a PCIe and USB 3.0 PHY control register.

Offset Address	Register Name	Total Reset Value
0x0088	MISC_CTRL34	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep9																							pcie_clkreq_filter_bypass	reserved	reserved	usb3_phy_rx_standby	usb3_phy_bypass_codec	reserved		pcie_phy_rx_standby	pcie_phy_bypass_codec
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved_keep9	Reserved
[8]	RW	pcie_clkreq_filter_bypass	pcie_clk_req input filtering control 0: enabled 1: disabled
[7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RW	usb3_phy_rx_standby	USB 3.0 PHY RX status 0: The PHY RX is in active status. 1: The PHY RX is in standby status.
[4]	RW	usb3_phy_bypass_codec	USB 3.0 PHY BYPASS_CODEC control 0: The 8b/10b encoding/decoding function is normally implemented. 1: The 8b/10b encoding/decoding function is bypassed.
[3:2]	RO	reserved	Reserved
[1]	RW	pcie_phy_rx_standby	PCIe PHY RX status in P0/P0s mode 0: The PHY RX is in active status. 1: The PHY RX is in standby status.
[0]	RW	pcie_phy_bypass_codec	PCIe PHY BYPASS_CODEC control 0: The 8b/10b encoding/decoding function is normally implemented. 1: The 8b/10b encoding/decoding function is bypassed.

MISC_CTRL40

MISC_CTRL40 is audio CODEC fast power-on and power-off control register 0.

Offset Address	Register Name	Total Reset Value
0x00A0	MISC_CTRL40	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											vref_sel_dat0					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	vref_sel_dat0	Configured value of vref_sel (fast power-on). For details, see the description of acodec_vref_sel.

MISC_CTRL42

MISC_CTRL42 is audio CODEC fast power-on and power-off control register 1.

Offset Address	Register Name	Total Reset Value
0x00A4	MISC_CTRL42	0x8C06_E79D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdb_ctcm_ibias_dat0	pd_ctcm_dat0	pd_micbias1_dat0	pd_vref_dat0	dacl_pop_en_dat0_t0	dacr_pop_en_dat0_t0	dacd_pop_en_dat0_t0	dacl_pop_en_dat0_t1	dacr_pop_en_dat0_t1	dacd_pop_en_dat0_t1	dacl_pop_direct_dat0_t0	dacr_pop_direct_dat0_t0	dacd_pop_direct_dat0_t0	dacl_pop_direct_dat0_t1	dacr_pop_direct_dat0_t1	dacd_pop_direct_dat0_t1	mute_dacl_dat0_t0	mute_dacr_dat0_t0	mute_lineout_d_dat0_t0	mute_dacl_dat0_t1	mute_dacr_dat0_t1	mute_lineout_d_dat0_t1	pd_dacl_dat0_t0	pd_dacr_dat0_t0	pd_lineout_d_dat0_t0	pd_dacl_dat0_t1	pd_dacr_dat0_t1	pd_lineout_d_dat0_t1	pop_rampclk_sel_dat0		pop_res_sel_dat0	
Reset	1	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0	1	1	1	0	1

Bits	Access	Name	Description
[31]	RW	pdb_ctcm_ibias_dat0	Configured value of pdb_ctcm_ibias (fast power-on). For details, see the description of acodec_pdb_ctcm_ibias.
[30]	RW	pd_ctcm_dat0	Configured value of pd_ctcm (fast power-on). For details, see the description of acodec_pd_ctcm.
[29]	RW	pd_micbias1_dat0	Configured value of pd_micbias1 (fast power-on). For details, see the description of acodec_pd_micbias1.
[28]	RW	pd_vref_dat0	Configured value of pd_vref (fast power-on). For details, see the description of acodec_pd_vref.

[27]	RW	dacl_pop_en_dat0_t0	Configured value 0 of dacl_pop_en (fast power-on). For details, see the description of acodec_dacl_pop_en.
[26]	RW	dacr_pop_en_dat0_t0	Configured value 0 of dacr_pop_en (fast power-on). For details, see the description of acodec_dacr_pop_en.
[25]	RW	dacd_pop_en_dat0_t0	Configured value 0 of dacd_pop_en (fast power-on). For details, see the description of acodec_dacd_pop_en.
[24]	RW	dacl_pop_en_dat0_t1	Configured value 1 of dacl_pop_en (fast power-on). For details, see the description of acodec_dacl_pop_en.
[23]	RW	dacr_pop_en_dat0_t1	Configured value 1 of dacr_pop_en (fast power-on). For details, see the description of acodec_dacr_pop_en.
[22]	RW	dacd_pop_en_dat0_t1	Configured value 1 of dacd_pop_en (fast power-on). For details, see the description of acodec_dacd_pop_en.
[21]	RW	dacl_pop_direct_dat0_t0	Configured value 0 of dacl_pop_direct (fast power-on). For details, see the description of acodec_dacl_pop_direct.
[20]	RW	dacr_pop_direct_dat0_t0	Configured value 0 of dacr_pop_direct (fast power-on). For details, see the description of acodec_dacr_pop_direct.
[19]	RW	dacd_pop_direct_dat0_t0	Configured value 0 of dacd_pop_direct (fast power-on). For details, see the description of acodec_dacd_pop_direct.
[18]	RW	dacl_pop_direct_dat0_t1	Configured value 1 of dacl_pop_direct (fast power-on). For details, see the description of acodec_dacl_pop_direct.
[17]	RW	dacr_pop_direct_dat0_t1	Configured value 1 of dacr_pop_direct (fast power-on). For details, see the description of acodec_dacr_pop_direct.
[16]	RW	dacd_pop_direct_dat0_t1	Configured value 1 of dacd_pop_direct (fast power-on). For details, see the description of acodec_dacd_pop_direct.
[15]	RW	mute_dacl_dat0_t0	Configured value 0 of mute_dacl (fast power-on). For details, see the description of acodec_mute_dacl.
[14]	RW	mute_dacr_dat0_t0	Configured value 0 of mute_dacr (fast power-on). For details, see the description of acodec_mute_dacr.
[13]	RW	mute_lineout_d_dat0_t0	Configured value 0 of mute_lineout_d (fast power-on). For details, see the description of acodec_mute_lineout_d.
[12]	RW	mute_dacl_dat0_t1	Configured value 1 of mute_dacl (fast power-on). For details, see the description of acodec_mute_dacl.
[11]	RW	mute_dacr_dat0_t1	Configured value 1 of mute_dacr (fast power-on). For details, see the description of acodec_mute_dacr.
[10]	RW	mute_lineout_d_dat0_t1	Configured value 1 of mute_lineout_d (fast power-on). For details, see the description of acodec_mute_lineout_d.
[9]	RW	pd_dacl_dat0_t0	Configured value 0 of pd_dacl (fast power-on). For details, see the description of acodec_pd_dacl.
[8]	RW	pd_dacr_dat0_t0	Configured value 0 of pd_dacr (fast power-on). For details, see the description of acodec_pd_dacr.

[7]	RW	pd_lineout_d_dat0_t0	Configured value 0 of pd_lineout_d (fast power-on). For details, see the description of acodec_pd_lineout_d.
[6]	RW	pd_dacl_dat0_t1	Configured value 1 of pd_dacl (fast power-on). For details, see the description of acodec_pd_dacl.
[5]	RW	pd_dacr_dat0_t1	Configured value 1 of pd_dacr (fast power-on). For details, see the description of acodec_pd_dacr.
[4]	RW	pd_lineout_d_dat0_t1	Configured value 1 of pd_lineout_d (fast power-on). For details, see the description of acodec_pd_lineout_d.
[3:2]	RW	pop_rampclk_sel_dat0	Configured value of pop_rampclk_sel (fast power-on). For details, see the description of acodec_pop_rampclk_sel.
[1:0]	RW	pop_res_sel_dat0	Configured value of pop_res_sel (fast power-on). For details, see the description of acodec_pop_res_sel.

MISC_CTRL43

MISC_CTRL43 is audio CODEC fast power-on and power-off control register 2.

Offset Address	Register Name	Total Reset Value
0x00A8	MISC_CTRL43	0x007F_C7FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep18									pd_dacl_dat1	pd_dacr_dat1	pd_lineout_d_dat1	mute_dacl_dat1	mute_dacr_dat1	mute_lineout_d_dat1	dacl_pop_direct_dat1_t0	dacr_pop_direct_dat1_t0	dacd_pop_direct_dat1_t0	dacl_pop_direct_dat1_t1	dacr_pop_direct_dat1_t1	dacd_pop_direct_dat1_t1	dacl_pop_en_dat1	dacr_pop_en_dat1	dacd_pop_en_dat1	pdb_ctcm_ibias_dat1	pd_ctcm_dat1	pd_micbias1_dat1	pd_vref_dat1	pop_rampclk_sel_dat1		pop_res_sel_dat1	
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:23]	RO	reserved_keep18	Reserved
[22]	RW	pd_dacl_dat1	Configured value of pd_dacl (fast power-off). For details, see the description of acodec_pd_dacl.
[21]	RW	pd_dacr_dat1	Configured value of pd_dacr (fast power-off). For details, see the description of acodec_pd_dacr.
[20]	RW	pd_lineout_d_dat1	Configured value of pd_lineout_d (fast power-off). For details, see the description of acodec_pd_lineout_d.

[19]	RW	mute_dacl_dat1	Configured value of mute_dacl (fast power-off). For details, see the description of acodec_mute_dacl.
[18]	RW	mute_dacr_dat1	Configured value of mute_dacr (fast power-off). For details, see the description of acodec_mute_dacr.
[17]	RW	mute_lineout_d_dat1	Configured value of mute_lineout_d (fast power-off). For details, see the description of acodec_mute_lineout_d.
[16]	RW	dacl_pop_direct_dat1_t0	Configured value 0 of dacl_pop_direct (fast power-off). For details, see the description of acodec_dacl_pop_direct.
[15]	RW	dacr_pop_direct_dat1_t0	Configured value 0 of dacr_pop_direct (fast power-off). For details, see the description of acodec_dacr_pop_direct.
[14]	RW	dacd_pop_direct_dat1_t0	Configured value 0 of dacd_pop_direct (fast power-off). For details, see the description of acodec_dacd_pop_direct.
[13]	RW	dacl_pop_direct_dat1_t1	Configured value 1 of dacl_pop_direct (fast power-off). For details, see the description of acodec_dacl_pop_direct.
[12]	RW	dacr_pop_direct_dat1_t1	Configured value 1 of dacr_pop_direct (fast power-off). For details, see the description of acodec_dacr_pop_direct.
[11]	RW	dacd_pop_direct_dat1_t1	Configured value 1 of dacd_pop_direct (fast power-off). For details, see the description of acodec_dacd_pop_direct.
[10]	RW	dacl_pop_en_dat1	Configured value of dacl_pop_en (fast power-off). For details, see the description of acodec_dacl_pop_en.
[9]	RW	dacr_pop_en_dat1	Configured value of dacr_pop_en (fast power-off). For details, see the description of acodec_dacr_pop_en.
[8]	RW	dacd_pop_en_dat1	Configured value of dacd_pop_en (fast power-off). For details, see the description of acodec_pop_res_sel.
[7]	RW	pdb_ctcm_ibias_dat1	Configured value of pdb_ctcm_ibias (fast power-off). For details, see the description of acodec_pdb_ctcm_ibias.
[6]	RW	pd_ctcm_dat1	Configured value of pd_ctcm (fast power-off). For details, see the description of acodec_pd_ctcm.
[5]	RW	pd_micbias1_dat1	Configured value of pd_micbias1 (fast power-off). For details, see the description of acodec_pd_micbias1.
[4]	RW	pd_vref_dat1	Configured value of pd_vref (fast power-off). For details, see the description of acodec_pd_vref.
[3:2]	RW	pop_rampclk_sel_dat1	Configured value of pop_rampclk_sel (fast power-off). For details, see the description of acodec_pop_rampclk_sel.
[1:0]	RW	pop_res_sel_dat1	Configured value of pop_res_sel (fast power-off). For details, see the description of acodec_pop_res_sel.

MISC_CTRL41

MISC_CTRL41 is audio CODEC fast power-on and power-off control register 3.

Offset Address	Register Name	Total Reset Value
0x00AC	MISC_CTRL41	0x00FF_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wait_threshold3																wait_threshold2															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	wait_threshold3	Reference source disable wait time. The timing unit is 20 ms.
[15:0]	RW	wait_threshold2	Power-off pop circuit climbing falling wait time. The timing unit is 20 ms.

MISC_CTRL44

MISC_CTRL44 is audio CODEC fast power-on and power-off control register 4.

Offset Address	Register Name	Total Reset Value
0x00B0	MISC_CTRL44	0x00FF_F001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wait_threshold1																wait_threshold0				reserved									dac_powon_en	dac_powoff_en	bypass_en
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	wait_threshold1	Power-on pop circuit climbing rising wait time. The timing unit is 20 ms.
[15:12]	RW	wait_threshold0	Configured value for the state transition delay. The timing unit is the APB bus clock.
[11:3]	RO	reserved	Reserved
[2]	RW	dac_powon_en	Fast power-on logic enable for the audio CODEC. A fast power-on operation is started after software writes 0 and then 1 to this bit.
[1]	RW	dac_powoff_en	Fast power-off logic enable for the audio CODEC. A fast power-off operation is started after software writes 0 and then 1 to this bit.
[0]	RW	bypass_en	Fast power-on/power-off logic enable for the audio CODEC 0: enabled 1: disabled

MISC_CTRL45

MISC_CTRL45 is audio CODEC ANA register 0 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B4	MISC_CTRL45	0x6405_FCFD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													acodec_dacl_pop_en	reserved	acodec_dacr_pop_en	reserved	acodec_mute_dacr	acodec_mute_dacl	acodec_pd_dacr	acodec_pd_dacl	reserved	acodec_pd_dacr_dff	acodec_pd_dacl_dff	acodec_pd_micbias2	acodec_pd_micbias1	acodec_pd_linein_r	acodec_pd_linein_l	acodec_pd_adcr	acodec_pd_adcl	acodec_pdb_ctcm_ibias	acodec_pd_vref
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	acodec_dacl_pop_en	Audio-left channel pop circuit enable 0: The pop tone removal function is disabled. 1: The pop tone removal function is enabled. Note: acodec_dacl_pop_en must be set to 1 only during the power-on/power-off pop suppression process and be set to 0 when the DAC channel works properly.
[17]	RO	reserved	Reserved
[16]	RW	acodec_dacr_pop_en	Audio-right channel pop circuit enable 0: The pop tone removal function is disabled. 1: The pop tone removal function is enabled. Note: acodec_dacr_pop_en must be set to 1 only during the power-on/power-off pop suppression process and be set to 0 when the DAC channel works properly.
[15]	RO	reserved	Reserved
[14]	RW	acodec_mute_dacr	Mute control for the DAC audio-right channel 0: The DAC audio-right channel works properly. 1: The DAC audio-right channel is muted.
[13]	RW	acodec_mute_dacl	Mute control for the DAC audio-left channel 0: The DAC audio-left channel works properly. 1: The DAC audio-left channel is muted.

[12]	RW	acodec_pd_dacr	Power-down control for the DAC audio-right channel (DACR) 0: The analog DACR works properly. 1: The analog DACR is powered down.
[11]	RW	acodec_pd_dacl	Power-down control for the DAC audio-left channel (DACL) 0: The analog DACL works properly. 1: The analog DACL is powered down.
[10]	RO	reserved	Reserved
[9]	RW	acodec_pd_dacr_dff	Power-down control for the DACR D trigger 0: The DACR D trigger works properly. 1: The DACR D trigger is powered down.
[8]	RW	acodec_pd_dacl_dff	Power-down control for the DACL D trigger 0: The DACL D trigger works properly. 1: The DACL D trigger is powered down.
[7]	RW	acodec_pd_micbias2	Power down control for the MICBIAS2 0: The MICBIAS2 works properly. 1: The MICBIAS2 is powered down.
[6]	RW	acodec_pd_micbias1	Power down control for the MICBIAS1 0: The MICBIAS1 works properly. 1: The MICBIAS1 is powered down.
[5]	RW	acodec_pd_linein_r	LINEIN_R power-down control 0: The LINEIN_R works properly. 1: The LINEIN_R is powered down.
[4]	RW	acodec_pd_linein_l	LINEIN_L power-down control 0: The LINEIN_L works properly. 1: The LINEIN_L is powered down.
[3]	RW	acodec_pd_adcr	Power down control for the ADC audio-right channel (ADCR) 0: The digital and analog ADCRs work properly. 1: The digital and analog ADCRs are powered down.
[2]	RW	acodec_pd_adcl	Power down control for the ADC audio-left channel (ADCL) 0: The digital and analog ADCLs work properly. 1: The digital and analog ADCLs are powered down.
[1]	RW	acodec_pdb_ctcm_ibias	Reserved,this bit is set to 1 in normal mode.
[0]	RW	acodec_pd_vref	Power-down control for the reference voltage 0: The reference voltage works properly. 1: The reference voltage is powered down.

MISC_CTRL46

MISC_CTRL46 is audio CODEC ANA register 1 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B8	MISC_CTRL46	0x0000_0034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acodec_linein_r_sel				acodec_linein_l_sel				reserved	acodec_adcr_gain_boost	reserved		acodec_linein_r_gain_codec				acodec_adcl_dwa_byp	acodec_adcl_gain_boost	acodec_adcl_mode_sel		acodec_linein_l_gain_code				reserved		acodec_mute_lineinr	acodec_mute_lineinl	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	acodec_linein_r_sel	Input signal select for the line-in right channel 0x0: IN0L/IN0R differential input 0x1: IN0R single-ended input 0x2: IN0R/IN1R differential input 0x3: IN1R single-ended input 0x4: IN1R/IN1L differential input Other values: reserved
[27:24]	RW	acodec_linein_l_sel	Input signal select for the line-in left channel 0x0: IN0L/IN0R differential input 0x1: IN0L single-ended input 0x2: IN0L/IN1L differential input 0x3: IN1L single-ended input 0x4: IN1R/IN1L differential input Other values: reserved
[23]	RO	reserved	Reserved
[22]	RW	acodec_adcr_gain_boost	ADCR gain boost control 0: 0 dB 1: 20 dB
[21]	RO	reserved	Reserved
[20:16]	RW	acodec_linein_r_gain_codec	LINEINR input gain control 0x0: 0 dB 0x1: 2 dB 0x2: 4 dB

			0x3: 6 dB 0x4: 8 dB 0x5: 10 dB 0x6: 12 dB 0x7: 14 dB 0x8: 16 dB 0x9: 18 dB 0xA: 20 dB 0xB: 22 dB 0xC: 24 dB 0xD: 26 dB 0xE: 28 dB 0xF: 30 dB 0x10: −1.5 dB Other values: reserved
[15]	RW	acodec_adcl_dwa_byp	ADCL DWA bypass 0: enabled 1: bypassed
[14]	RW	acodec_adcl_gain_boost	ADCL gain boost control 0: 0 dB 1: 20 dB
[13]	RW	acodec_adcl_mode_sel	ADCL mode select 0: 6.144 MHz sampling rate 1: 4.096 MHz sampling rate

[12:8]	RW	acodec_linein_l_gain_code	LINEINL input gain control 0x0: 0 dB 0x1: 2 dB 0x2: 4 dB 0x3: 6 dB 0x4: 8 dB 0x5: 10 dB 0x6: 12 dB 0x7: 14 dB 0x8: 16 dB 0x9: 18 dB 0xA: 20 dB 0xB: 22 dB 0xC: 24 dB 0xD: 26 dB 0xE: 28 dB 0xF: 30 dB 0x10: −1.5 dB Other values: reserved
[7:6]	RO	reserved	Reserved
[5]	RW	acodec_mute_linein_r	LINEINR mute control of the right channel 0: The right channel LINEINR works properly. 1: The right channel LINEINR is muted.
[4]	RW	acodec_mute_linein_l	LINEINL mute control of the left channel 0: The left channel LINEINL works properly. 1: The left channel LINEINL is muted.
[3:0]	RO	reserved	Reserved

MISC_CTRL47

MISC_CTRL47 is audio CODEC ANA register 2 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00BC	MISC_CTRL47	0x4018_008D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	acodec_pd_ctcm	reserved						acodec_rst	reserved																						
Reset	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	acodec_pd_ctcm	Reserved,this bit is set to 0 in normal mode.
[29:24]	RO	reserved	Reserved
[23]	RW	acodec_rst	Analog signal reset 0: deassert reset 1: reset
[22:0]	RO	reserved	Reserved

MISC_CTRL48

MISC_CTRL48 is audio CODEC ANA register 3 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00C0	MISC_CTRL48	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_keep23																								acodec_vref_exmode	reserved		acodec_pop_res_sel		acodec_dacl_opo_direct	reserved	acodec_dacr_opo_direct
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved_keep23	Reserved
[7]	RW	acodec_vref_exmode	VREF PD 0: pull-down, normal PD 1: 1: no pull-down. The external VREF is supported.
[6:5]	RO	reserved	Reserved
[4:3]	RW	acodec_pop_res_sel	Resistance of the resistor between the pop-free circuit and the main output 00: 100 Ω 01: 1 kΩ 10: 10 kΩ 11: 100 kΩ
[2]	RW	acodec_dacl_opo_direct	Climbing direction of the DACL pop circuit 0: The pop circuit connects to a pull-down resistor. 1: The pop circuit connects to a pull-up resistor and then to VCM.
[1]	RO	reserved	Reserved
[0]	RW	acodec_dacr_opo_direct	Climbing direction of the DACR pop circuit 0: The pop circuit connects to a pull-down resistor. 1: The pop circuit connects to a pull-up resistor and then to VCM.

MISC_CTRL51

MISC_CTRL51 is audio CODEC DIG control register 0 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00CC	MISC_CTRL51	0x00F3_5A4A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_rst_n	dacr_rst_n	adcl_rst_n	adcr_rst_n	dacl_en	dacr_en	adcl_en	adcr_en	reserved								i2s1_fs_sel				reserved											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[31]	RW	dacl_rst_n	DACL reset 0: valid 1: invalid
[30]	RW	dacr_rst_n	DACR reset 0: valid 1: invalid
[29]	RW	adcl_rst_n	ADCL reset 0: valid 1: invalid
[28]	RW	adcr_rst_n	ADCR reset 0: valid 1: invalid
[27]	RW	dacl_en	DACL enable 0: disabled 1: enabled
[26]	RW	dacr_en	DACR enable 0: disabled 1: enabled
[25]	RW	adcl_en	ADCL enable 0: disabled 1: enabled
[24]	RW	adcr_en	ADCR enable 0: disabled 1: enabled
[23:18]	RO	reserved	Reserved
[17:13]	RW	i2s1_fs_sel	Sampling rate of the I^2S channel 11000: mclk/512/2 11001: mclk/256/2 11010: mclk/128/2 11011: mclk/64/2 111xx: mclk/32/2

[12:0]	RO	reserved	Reserved

MISC_CTRL52

MISC_CTRL52 is audio CODEC DIG control register 1 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D0	MISC_CTRL52	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smutel	smuter	sunmutel	sunmuter	dacvu	mutel_rate		muter_rate	reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	smutel	DACL soft mute control 0: disabled 1: enabled
[30]	RW	smuter	DACR soft mute control 0: disabled 1: enabled
[29]	RW	sunmutel	DACL soft unmute control 0: disabled 1: enabled
[28]	RW	sunmuter	DACR soft unmute control 0: disabled 1: enabled
[27]	RW	dacvu	DAC volume update control 0: not updated 1: updated
[26:25]	RW	mutel_rate	DACL soft mute rate control 00: fs/2 01: fs/8 10: fs/32 11: fs/64

[24:23]	RW	muter_rate	DACR soft mute rate control 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[22:0]	RO	reserved	Reserved

MISC_CTRL53

MISC_CTRL53 is audio CODEC DIG control register 2 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D4	MISC_CTRL53	0x0606_2424

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_mute	dacl_vol							dacr_mute	dacr_vol							reserved															
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	dacl_mute	DACL digital mute control 0: normal mode 1: muted
[30:24]	RW	dacl_vol	DACL digital volume control The volume is calculated as follows: (6 − dacl_vol x 1) dB 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB … 0x7E: −120 dB 0x7F: muted
[23]	RW	dacr_mute	DACR digital mute control 0: normal mode 1: muted

[22:16]	RW	dacr_vol	DACR digital volume control The volume is calculated as follows: (6 − dacr_vol x 1) dB 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB … 0x7E: −120 dB 0x7F: muted
[15:0]	RO	reserved	Reserved

MISC_CTRL54

MISC_CTRL54 is audio CODEC DIG control register 3 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D8	MISC_CTRL54	0x1E1E_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adcl_mute	adcl_vol							adcr_mute	adcr_vol							adcl_hpf_en	adcr_hpf_en	reserved													
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	adcl_mute	ADCL digital mute control 0: unmuted 1: muted
[30:24]	RW	adcl_vol	ADCL volume control The volume is calculated as follows: (30 − adcl_vol x 1) dB 00: 30 dB 01: 29 dB 02: 28 dB … 7E: −96 dB 7F: −97 dB
[23]	RW	adcr_mute	ADCR digital mute control 0: unmuted 1: muted

[22:16]	RW	adcr_vol	ADCR volume control The volume is calculated as follows: (30 − adcr_vol x 1) dB 00: 30 dB 01: 29 dB 02: 28 dB … 7E: −96 dB 7F: −97 dB
[15]	RW	adcl_hpf_en	ADCL high-pass filter enable 0: disabled 1: enabled
[14]	RW	adcr_hpf_en	ADCR high-pass filter enable 0: disabled 1: enabled
[13:0]	RO	reserved	Reserved

MISC_CTRL56

MISC_CTRL56 is an I^{2}S channel selection control register (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00E0	MISC_CTRL56	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								i2s_pad_enable	audio_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[1]	RW	i2s_pad_enable	Enable for the channel between the I²S interface of the chip and AIAO 0: The channel between the I²S interface of the chip and AIAO is disabled, and the I²S interface of the chip has no output. 1: The channel between the I²S interface of the chip and AIAO is enabled, and the I²S interface of the chip connects to the I²S interface of the AIAO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.
[0]	RW	audio_enable	Enable for the channel between the I²S interface of the internal audio CODEC and AIAO 0: The channel between the I²S interface of the internal audio CODEC and AIAO is disabled, and the I²S interface of the internal audio CODEC has no output. 1: The channel between the I²S interface of the internal audio CODEC and AIAO is enabled, and the I²S interface of internal audio CODEC connects to the I²S interface of the AIAO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.

MISC_CTRL60

MISC_CTRL60 is core layer memory high-speed control register 0.

Offset Address	Register Name	Total Reset Value
0x00F0	MISC_CTRL 60	0x0013_3313

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		core_mem_ras_emaw	reserved	core_mem_ras_emab	reserved	core_mem_rft_emab	reserved	core_mem_rft_emaa	reserved	core_mem_rfs_emaw	reserved	core_mem_rfs_ema
Reset	0 0 0 0	0 0 0 0	0 0 0 1	0 0 1 1	0 0 1 1	0 0 1 1	0 0 0 1	0 0 1 1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:20]	RW	core_mem_ras_emaw	emaw speed adjustment control signal of ras_mem at the core layer
[19]	RO	reserved	Reserved
[18:16]	RW	core_mem_ras_emab	ema speed adjustment control signal of ras_mem at the core layer

[15]	RO	reserved	Reserved
[14:12]	RW	core_mem_rft_emab	emab speed adjustment control signal of rft_mem at the core layer
[11]	RO	reserved	Reserved
[10:8]	RW	core_mem_rft_emaa	emaa speed adjustment control signal of rft_mem at the core layer
[7:6]	RO	reserved	Reserved
[5:4]	RW	core_mem_rfs_emaw	emaw speed adjustment control signal of rfs_mem at the core layer
[3]	RO	reserved	Reserved
[2:0]	RW	core_mem_rfs_ema	ema speed adjustment control signal of rfs_mem at the core layer

MISC_CTRL61

MISC_CTRL61 is core layer memory high-speed control register 1.

Offset Address	Register Name	Total Reset Value
0x00F4	MISC_CTRL 61	0x0003_1313

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												core_mem_ros_ema				reserved				core_mem_rad_emawb				reserved				core_mem_rad_emab			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	core_mem_ros_ema	ema speed adjustment control signal of ros_mem at the core layer
[15:14]	RO	reserved	Reserved
[13:12]	RW	core_mem_rad_emawb	emawb speed adjustment control signal of rad_mem at the core layer
[11]	RO	reserved	Reserved
[10:8]	RW	core_mem_rad_emab	emab speed adjustment control signal of rad_mem at the core layer

[7:6]	RO	reserved	Reserved
[5:4]	RW	core_mem_rad_emawa	emawa speed adjustment control signal of rad_mem at the core layer
[3]	RO	reserved	Reserved
[2:0]	RW	core_mem_rad_emaa	emaa speed adjustment control signal of rad_mem at the core layer

MISC_CTRL80

MISC_CTRL80 is eMMC DLL control register 0.

Offset Address	Register Name	Total Reset Value
0x0140	MISC_CTRL80	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3 2 1 0
Name	reserved				emmc_dll_ssel		emmc_dll_mode	emmc_dll_stop	emmc_dll_bypass	emmc_dll_slave_en	emmc_dll_tune
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	emmc_dll_ssel	DLL ssel signal of the eMMC interface for selecting the number of initial delay levels of the DLL slave line
[7]	RW	emmc_dll_mode	DLL mode signal of the eMMC interface 0: normal mode 1: The slave line is controlled by dll_dllssel.
[6]	RW	emmc_dll_stop	DLL stop signal of the eMMC interface 0: The clock detection is enabled. 1: The clock detection is disabled.
[5]	RW	emmc_dll_bypass	DLL bypass signal of the eMMC interface 0: normal mode. The phase shift of the output clock relative to the input clock is 90°. 1: bypassed. The phase of the output clock is not shifted.
[4]	RW	emmc_dll_slave_en	DLL slave_en signal of the eMMC interface 0: The slave line stops working. 1: The slave line starts working.

[3:0]	RW	emmc_dll_tune	DLL tune signal of the eMMC interface 0x0: no tuning 0x1: increase the delay by 1 level 0x2: increase the delay by 2 levels 0x3: increase the delay by 3 levels … 0x7: increase the delay by 7 levels 0x8: no tuning 0x9: decrease the delay by 1 level 0xA: decrease the delay by 2 levels 0xB: decrease the delay by 3 levels … 0xF: decrease the delay by 7 levels

MISC_CTRL81

MISC_CTRL81 is eMMC DLL control register 1.

Offset Address	Register Name	Total Reset Value
0x0144	MISC_CTRL81	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1 0
Name	reserved									
						emmc_dll_lock	emmc_dll_ready	emmc_dll_overflow	emmc_dll_mdly_tap	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RO	emmc_dll_lock	DLL lock signal of the eMMC interface 0: unlocked 1: locked
[9]	RO	emmc_dll_ready	DLL ready signal of the eMMC interface 0: not ready 1: ready

[8]	RO	emmc_dll_overflow	DLL overflow signal of the eMMC interface 0: no overflow 1: overflow
[7:0]	RO	emmc_dll_mdly_tap	DLL mdly_tap signal of the eMMC interface DLL mater line tap value

MISC_CTRL85

MISC_CTRL85 is peripheral bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0154	MISC_CTRL85	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	periaxi_timeout_en_m2	periaxi_timeout_value_m2															periaxi_timeout_en_m1	periaxi_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	periaxi_timeout_en_m2	Timeout count enable for the peripheral AXI bus port M2 (SYSAXI_S2) 0: disabled 1: enabled
[30:16]	RW	periaxi_timeout_value_m2	Timeout count value of the peripheral AXI bus port M2 (SYSAXI_S2) Count value = periaxi_timeout_value_m2 x 2
[15]	RW	periaxi_timeout_en_m1	Timeout count enable for the peripheral AXI bus port M1 (CCI_M0) 0: disabled 1: enabled
[14:0]	RW	periaxi_timeout_value_m1	Timeout count value of the peripheral AXI bus port M1 (CCI_M0) Count value = periaxi_timeout_value_m1 x 2

MISC_CTRL86

MISC_CTRL86 is peripheral bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x0158	MISC_CTRL86	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	periaxi_timeout_en_m4	periaxi_timeout_value_m4															periaxi_timeout_en_m3	periaxi_timeout_value_m3														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	periaxi_timeout_en_m4	Timeout count enable for the peripheral AXI bus port M4 (j2c) 0: disabled 1: enabled
[30:16]	RW	periaxi_timeout_value_m4	Timeout count value of the peripheral AXI bus port M4 (j2c) Count value = periaxi_timeout_value_m4 x 2
[15]	RW	periaxi_timeout_en_m3	Timeout count enable for the peripheral AXI bus port M3 (debug_axi) 0: disabled 1: enabled
[14:0]	RW	periaxi_timeout_value_m3	Timeout count value of the peripheral AXI bus port M3 (debug_axi) Count value = periaxi_timeout_value_m3 x 2

MISC_CTRL88

MISC_CTRL88 is peripheral bus priority control register 0.

Offset Address	Register Name	Total Reset Value
0x0160	MISC_CTRL88	0x0000_0123

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	periaxi_port4_pri			reserved			periaxi_port3_pri			reserved			periaxi_port2_pri			reserved			periaxi_port1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	periaxi_port4_pri	Priority of the peripheral AXI bus port M4 (j2c) The value 3 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	periaxi_port3_pri	Priority of the peripheral AXI bus port M3 (debug_axi) The value 3 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	periaxi_port2_pri	Priority of the peripheral AXI bus port M2 (SYSAXI_S2) The value 3 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	periaxi_port1_pri	Priority of the peripheral AXI bus port M1 (CCI_M0) The value 3 indicates the highest priority.

MISC_CTRL89

MISC_CTRL89 is peripheral bus priority control register 1.

Offset Address	Register Name	Total Reset Value
0x0164	MISC_CTRL89	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												periaxi_slave_priority_s5				reserved				reserved				reserved				reserved			
	periaxi_slave_priority_s4								periaxi_slave_priority_s3								periaxi_slave_priority_s2								periaxi_slave_priority_s1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	periaxi_slave_priority_s5	Bus access priority of the peripheral AXI S5 (pcie_slave) port The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved
[14:12]	RW	periaxi_slave_priority_s4	Bus access priority of the peripheral AXI S4 (GIC) port The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	periaxi_slave_priority_s3	Bus access priority of the peripheral AXI S3 (ahb_cfg) port The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	periaxi_slave_priority_s2	Bus access priority of the peripheral AXI S2 (media_apb) port The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	periaxi_slave_priority_s1	Bus access priority of the peripheral AXI S1 (sys_apb) port The value 7 indicates the highest priority.

MISC_CTRL93

MISC_CTRL93 is a VO_AIO bus arbitration control register.

Offset Address	Register Name	Total Reset Value
0x0174	MISC_CTRL93	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_aio_axi_timeout_en_m2	vo_aio_axi_timeout_value_m2															vo_aio_axi_timeout_en_m1	vo_aio_axi_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_aio_axi_timeout_en_m2	Timeout count enable for the VO_AIO AXI bus port M2 (AIAO) 0: disabled 1: enabled
[30:16]	RW	vo_aio_axi_timeout_value_m2	Timeout count value of the VO_AIO AXI bus port M2 (AIAO) Count value = vpssaxi_timeout_value_m2 x 2
[15]	RW	vo_aio_axi_timeout_en_m1	Timeout count enable for the VO_AIO AXI bus port M1 (VO) 0: disabled 1: enabled
[14:0]	RW	vo_aio_axi_timeout_value_m1	Timeout count value of the VO_AIO AXI bus port M1 (VO) Count value = vpssaxi_timeout_value_m1 x 2

MISC_CTRL94

MISC_CTRL94 is a VO_AIO bus priority control register.

Offset Address	Register Name	Total Reset Value
0x0178	MISC_CTRL94	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												reserved	vo_aio_axi_port2_pri			reserved	vo_aio_axi_port1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	vo_aio_axi_port2_pri	Priority of the VO_AIO AXI bus port M2 (AIAO) The value 1 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	vo_aio_axi_port1_pri	Priority of the VO_AIO AXI bus port M1 (VO) The value 1 indicates the highest priority.

3.6 DMA Controller

3.6.1 Overview

The direction memory access (DMA) operation is a high-speed data transfer operation. It supports data read/write between peripherals and memories without using the CPU. The direction memory access controller (DMAC) directly transfers data between a memory and a peripheral, between peripherals, or between memories. This avoids the CPU intervention and reduces the interrupt handling overhead of the CPU.

3.6.2 Features

The DMAC has the following features:

- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides four DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports the DMA requests controlled through software.
- Programs the DMA burst size.

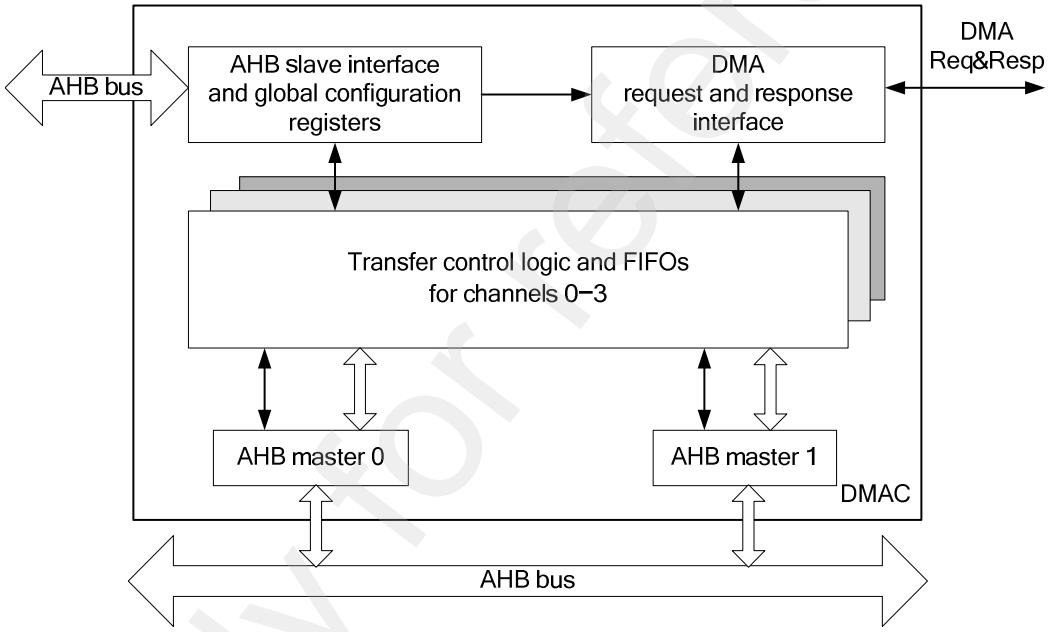
- Configures the source address and the destination address as automatic incremental or decremented addresses during DMA transfer.
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.

3.6.3 Function Description

Functional Block Diagram

Figure 3-5 shows the functional block diagram of the DMAC.

Figure 3-5 Functional block diagram of the DMAC



NOTE

- The priorities of DMAC channels are fixed. DMA channel 0 has the highest priority; whereas channel 3 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- DMA channel 0 and DMA channel 1 have one 4 x 32-bit FIFO each, and DMA channel 2 and DMA channel 3 have one 16 x 32-bit FIFO each.

Each DMA channel has a group of transfer control logic and one FIFO. The transfer control logic automatically performs the following operations:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer data in the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

----End

Workflow

The workflow of the DMAC is as follows:

Step 1 The software selects one DMA channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Header pointer of the linked list
- Amount of the transferred data
- Source and destination peripheral request signal numbers
- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request lines of the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then the DAMC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

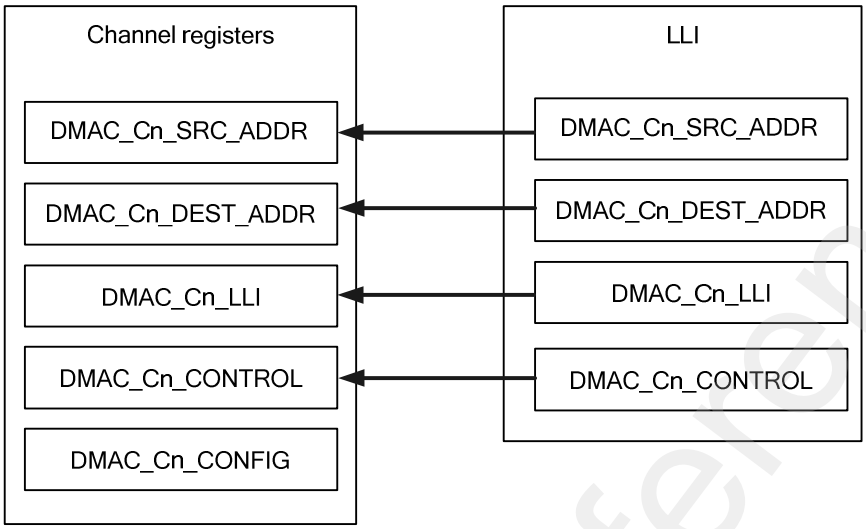
Step 5 The DMA channel responds to the DMA request of the destination device. Then the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

Step 6 The steps 2 and step 3 as well as step 4 and 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, step 2 to step 5 are performed repeatedly until the specified data is completely transferred and a maskable transfer terminal interrupt is sent. If the value of DMAC_Cn_LLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the read values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_Cn_LLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-5), and then go to step 2. If the value of DMAC_Cn_LLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

----End

Figure 3-6 illustrates how to update channel registers through the LLI.

Figure 3-6 Updating channel registers through the LLI



Connection Between the DMA and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides the following two DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preconfigured.
- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC provides a request clear signal DMACLR.

This signal is sent to each peripheral by the DMAC as a response to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-10 describes the mapping between DMAC hardware request signals and corresponding peripheral requests.

Table 3-10 DMAC hardware request signals and corresponding peripheral requests

DMAC Hardware Request Signal No.	Peripheral Request
0	DMA request of the UART0 RX channel/DMA request of the UART4 RX channel (for details about the select configuration, see dma_01_sel of the MISC_CTRL1 register)

DMAC Hardware Request Signal No.	Peripheral Request
1	DMA request of the UART0 TX channel/DMA request of the UART4 TX channel (for details about the select configuration, see dma_01_sel of the MISC_CTRL1 register)
2	DMA request of the UART1 RX channel
3	DMA request of the UART1 TX channel
4	DMA request of the UART2 RX channel
5	DMA request of the UART2 TX channel
6	DMA request of the UART3 RX channel
7	DMA request of the UART3 TX channel
8	DMA request of the I^2C0 RX channel/DMA request of the SSP0 RX channel (for details about the select configuration, see dma_89_sel of the MISC_CTRL1 register)
9	DMA request of the I^2C0 TX channel/DMA request of the SSP0 TX channel (for details about the select configuration, see dma_89_sel of the MISC_CTRL1 register)
10	DMA request of the I^2C1 RX channel/DMA request of the SSP1 RX channel (for details about the select configuration, see dma_ab_sel of the MISC_CTRL1 register)
11	DMA request of the I^2C1 TX channel/DMA request of the SSP1 TX channel (for details about the select configuration, see dma_ab_sel of the MISC_CTRL1 register)
12	DMA request of the I^2C2 RX channel/DMA request of the SSP2 RX channel (for details about the select configuration, see dma_cd_sel of the MISC_CTRL1 register)
13	DMA request of the I^2C2 TX channel/DMA request of the SSP2 TX channel (for details about the select configuration, see dma_cd_sel of the MISC_CTRL1 register)
14	DMA request of the I^2C3 RX channel
15	DMA request of the I^2C3 TX channel

The source and destination requests of each DMA channel are configured by software. For example, DMA request 4 is the request of the UART2 RX channel. To transmit the UART2 RX data by using channel 3, you must configure DMA request 4 as the source request of channel 3.

As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 2 or channel 3. In this way, the master with a higher priority channel can transfer data

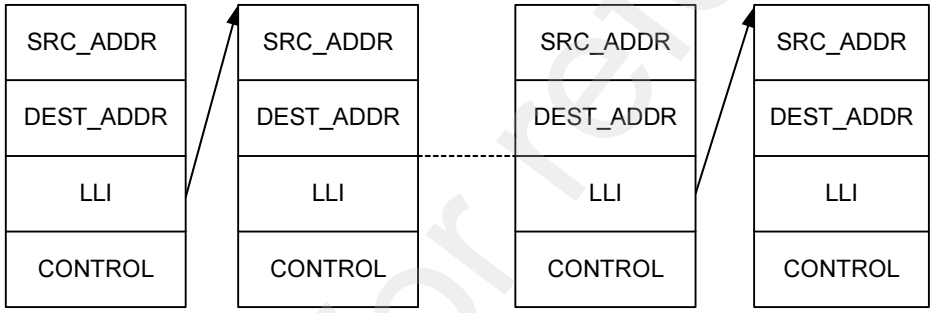
on the bus first. Therefore, to prevent other channels from waiting for the bus for a long time, you are advised to transmit data from memory to memory using channel 2 or channel 3.

DMA Linked List

The data structure of the DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address for the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address for the destination device
- Channel register DMAC_Cn_LLI, for setting the address for the next node
- Channel register DMAC_Cn_CONTROL, for setting the master, data width, burst size, address increment, and transfer size of the source device and destination device

Figure 3-7 Structure of DMAC LLIs



CAUTION

The LLI field value must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a consecutive address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after data blocks corresponding to the current node are transferred.

3.6.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMA channels are idle and there is no DMA transfer request.
- DMAC_Cn_CONFIG[ch_en] is set to 0 and all the DMA channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG[ch_en] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG [dmac_enable] to disable the DMAC.

Step 3 Write 0 to PERI_CRG54[dma_cken] to disable DMAC bus clock gating. Then the DMAC clock is disabled.

Step 4 Enable the clock and the DMAC again when the DMAC is required for data transfer.

----End

Initialization

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endianness of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[dmac_enable] to enable the DMAC.

Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupts.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable channels in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG[ch_en] of each channel.

----End

Enabling a Channel

After the DMAC is initialized, the DMAC can transmit data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

Step 1 Read DMAC_ENABLED_CHNS to search for idle channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Write to DMAC_Cn_SRC_ADDR to set the access start address for the source device.

Step 4 Write to DMAC_Cn_DEST_ADDR to set the access start address for the destination device.

Step 5 Write to DMAC_Cn_LLI to set the linked list information. If the channel is used for single-block data transfer, set DMAC_Cn_LLI to 0. If the channel is used for linked list data transfer, set DMAC_Cn_LLI to the linked list header pointer.

Step 6 Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.

Step 7 Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel.

Step 8 Write 1 to DMAC_Cn_CONFIG[ch_en] to enable this channel.

----End

Usage of DMAC_Cn_CONTROL

The DMAC_Cn_CONTROL register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register value is updated when being loaded from an LLI node after a complete data block is transferred.

If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. As a result, the register can be read after the channel stops data transfer.

Table 3-11 lists the mapping between the value of dbsize or sbsize of DMAC_Cn_CONTROL and the burst length.

Table 3-11 Mapping between the value of dbsize or sbsize and the burst length

Value of bsize or sbSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 3-12 describes mapping between the value of dwidth or swidth of DMAC_Cn_CONTROL and the transfer data width.

Table 3-12 Mapping between the value of dwidth or swidth and the transfer bit width

Value of swidth or dwidth	Transfer Bit Width
000	Byte (8 bits)
001	Halfword (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- swidth and dwidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Never conduct common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and read value may be the same. During the write operation, this field serves as a control register, because it determines the number of data segments transferred by the DMAC. During the read operation, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.
- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO but not the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-incremental mode. Otherwise, the peripheral FIFO may overflow.

The bus access information is provided for the source device or destination device over the master interface signals during data transfer. Such information is related to the bits DMAC_Cn_CONTROL[prot_stat] and DMAC_Cn_CONFIG[ch_lock] that are configured by programming channel registers. Table 3-13 describes the three protection bits of the prot field of DMAC_Cn_CONTROL.

Table 3-13 Definitions of the prot_stat field of DMAC_Cn_CONTROL

Bit	Description	Purpose
[2]	Cacheable or non-cacheable	Indicates whether the access is cacheable. 0: non-cacheable 1: cacheable For example, this bit can notify an advanced micro-controller bus architecture (AMBA) bridge of the following information: When finding the first read operation of the 8-digit burst, this bridge can originate one 8-digit burst read operation on the destination bus directly instead of transmitting the read operations on the source bus to the destination bus one by one. This bit controls the output of the bus signal HPROT[3].
[1]	Bufferable or non-bufferable	Indicates whether the access is bufferable. 0: non-bufferable 1: bufferable For example, this bit is used to notify an AMBA bridge that the write operation on the source bus can be complete without waiting. That is, the operation can be performed even when the bridge does not arbitrate the operation to the destination bus and the slave device does not receive data completely. This bit controls the output of the bus signal HPROT[2].

Bit	Description	Purpose
[0]	Privileged or User	Access mode. 0: user mode 1: privileged mode This bit controls the output of the bus signal HPROT[1].

NOTE

AMBA: advanced micro-controller bus architecture

Usage of DMAC_Cn_CONFIG

Table 3-14 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-14 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC
100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Interrupt Handling

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is handled as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels initiate interrupt requests at the same time, the interrupt request with the highest priority is handled first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a transfer terminal interrupt. If the value is 1, the interrupt is a transfer terminal interrupt. In this case, go to step 4; otherwise, go to step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to step 5; otherwise, end the operation.

Step 4 Handle the transfer terminal interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.
2. Fetch or use up the data buffered in the memory. If necessary (for example, you need to create a buffer in the memory), configure and enable the channel again.
3. End interrupt handling.

Step 5 Handle the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.
2. Provide the error information. If necessary, configure and enable the channel again.
3. End interrupt handling.

----End

3.6.5 Register Summary

NOTE

The *n* in the offset addresses for DMA registers indicates the DMA channel and its value range is 0−3.

Table 3-15 describes the DMAC registers.

Table 3-15 Summary of the DMAC registers (base address: 0x1003_0000)

Offset Address	Register	Description	Page
0x0000	DMAC_INT_STAT	DMAC interrupt status register	3-135
0x0004	DMAC_INT_TC_STAT	DMAC transfer terminal interrupt status register	3-136
0x0008	DMAC_INT_TC_CLR	DMAC transfer terminal interrupt clear register	3-137
0x000C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-138
0x0010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-139
0x0014	DMAC_RAW_INT_TC_STAT	DMAC raw transfer terminal interrupt status register	3-140
0x0018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-141
0x001C	DMAC_ENABLED_CHNS	DMAC channel enable status register	3-142
0x0020	DMAC_SOFT_BREQ	DMAC software burst transfer request register	3-142
0x0024	DMAC_SOFT_SREQ	DMAC software single transfer request register	3-143
0x0028	DMAC_SOFT_LBREQ	DMAC software last burst request register	3-144

Offset Address	Register	Description	Page
0x002C	DMAC_SOFT_LSREQ	DMAC software last single request register	3-144
0x0030	DMAC_CONFIG	DMAC configuration register	3-145
0x0034	DMAC_SYNC	DMAC request line sync enable register	3-146
0x0100 + *n* x 0x20	DMAC_Cn_SRC_ADDR	Source address register of DMA channel *n* (*n* = 0−3)	3-146
0x0104 + *n* x 0x20	DMAC_Cn_DEST_ADDR	Destination address register of DMA channel *n* (*n* = 0−3)	3-147
0x0108 + *n* x 0x20	DMAC_Cn_LLI	LLI information register of DMA channel *n* (*n* = 0−3)	3-147
0x010C + *n* x 0x20	DMAC_Cn_CONTROL	Control register of DMA channel *n* (*n* = 0−3)	3-148
0x110 + *n* x 0x20	DMAC_Cn_CONFIG	Configuration register of DMA channel *n* (*n* = 0−3)	3-151

3.6.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	DMAC_INT_STAT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							ch3_int_stat	ch2_int_stat	ch1_int_stat	ch0_int_stat
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_stat	Masked interrupt status of channel 3 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

[2]	RO	ch2_int_stat	Masked interrupt status of channel 2 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[1]	RO	ch1_int_stat	Masked interrupt status of channel 1 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[0]	RO	ch0_int_stat	Masked interrupt status of channel 0 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is a DMAC transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_stat		ch2_int_tc_stat		ch1_int_tc_stat		ch0_int_tc_stat	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_tc_stat	Status of the masked transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_tc_stat	Status of the masked transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_tc_stat	Status of the masked transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.

[0]	RO	ch0_int_tc_stat	Status of the masked transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a DMAC transfer terminal interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_clr		ch2_int_tc_clr		ch1_int_tc_clr		ch0_int_tc_clr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_tc_clr	Transfer terminal interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_tc_clr	Transfer terminal interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_tc_clr	Transfer terminal interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_tc_clr	Transfer terminal interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is a DMAC error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_stat		ch2_int_err_stat		ch1_int_err_stat		ch0_int_err_stat	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_err_stat	Status of the masked error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_err_stat	Status of the masked error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_err_stat	Status of the masked error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_err_stat	Status of the masked error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is a DMAC transfer error interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_clr		ch2_int_err_clr		ch1_int_err_clr		ch0_int_err_clr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_err_clr	Error interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_err_clr	Error interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_err_clr	Error interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_err_clr	Error interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_RAW_INT_TC_STAT

DMAC_RAW_INT_TC_STAT is a DMAC raw transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	DMAC_RAW_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_tc		ch2_raw_int_tc		ch1_raw_int_tc		ch0_raw_int_tc	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_tc	Status of the raw transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_tc	Status of the raw transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_tc	Status of the raw transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_tc	Status of the raw transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_RAW_INT_ERR_STAT

DMAC_RAW_INT_ERR_STAT is a DMAC raw error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	DMAC_RAW_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_err		ch2_raw_int_err		ch1_raw_int_err		ch0_raw_int_err	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_err	Status of the raw error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_err	Status of the raw error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_err	Status of the raw error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_err	Status of the raw error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_ENABLED_CHNS

DMAC_ENABLED_CHNS is a DMAC channel enable status register.

Offset Address	Register Name	Total Reset Value
0x001C	DMAC_ENABLED_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_enabled		ch2_enabled		ch1_enabled		ch0_enabled	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_enabled	Channel 3 enable 0: disabled 1: enabled
[2]	RO	ch2_enabled	Channel 2 enable 0: disabled 1: enabled
[1]	RO	ch1_enabled	Channel 1 enable 0: disabled 1: enabled
[0]	RO	ch0_enabled	Channel 0 enable 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMAC software burst transfer request register.

Software controls the generation of a DMA burst transfer request by using this register.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_breq	Controls whether to generate a DMA burst transfer request When this register is written: 0: no effect 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not send any DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting the DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMAC software single transfer request register.

Software controls the generation of DMA single transfer requests by using this register.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_sreq	Controls whether to generate a DMA single transfer request When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

			When this register is read: 0: The peripheral corresponding to the request signal DMACSREQ[15:0] does not send a DMA single request. 1: The peripheral corresponding to the request signal DMACSREQ[15:0] is requesting the DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMAC software last burst request register.

Software controls the generation of the DMA last burst transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x0028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_lbreq	Last burst request issued by the software 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMAC software last single transfer request register.

Software controls the generation of the DMA last single transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x002C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	soft_lsreq	Last single transfer request issued by software 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2_endianness	m1_endianness	dmac_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	m2_endianness	Byte endianness of master 2 0: little endian 1: big endian
[1]	RW	m1_endianness	Byte endianness of master 1 0: little endian 1: big endian
[0]	RW	dmac_enable	DMA enable 0: disabled 1: enabled

DMAC_SYNC

DMAC_SYNC is a DMAC request line sync enable register.

Offset Address	Register Name	Total Reset Value
0x0034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dmac_sync	Controls whether to synchronize the request signals 0: The sync logic provided for the DMA request signals of the corresponding peripheral is enabled. 1: The sync logic provided for the DMA request signals of the corresponding peripheral is disabled.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a source address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x100 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0100 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x104 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register contains the destination address for the data to be transferred. Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- Destination address increment.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0104 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address

DMAC_Cn_LLI

DMAC_Cn_LLI is an LLI information register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x108 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3. For details, see section "DMA Linked List."

Offset Address	Register Name	Total Reset Value
0x0108 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_LLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ll_item																														reserved	ll_master
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	ll_item	The bit[31:2] in the next LLI node address and the address bit[1:0] are set to 0. A linked list address must be 4-byte aligned.
[1]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[0]	RW	ll_master	Master for loading the next LLI node 0: master 1 1: master 2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a control register of DMA channel *n* (*n* = 0–3).

Its offset address is 0x10C + n x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Offset Address	Register Name	Total Reset Value
0x010C + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_tc_enable		prot_stat		dest_incr	src_incr	dest_select	src_select	dwidth				swidth				dbsize				sbsize				trans_size							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_tc_enable	Transfer terminal interrupt enable. This bit determines whether the current LLI node triggers a transfer terminal interrupt. 0: do not trigger 1: trigger
[30:28]	RW	prot_stat	HPROT[2:0] access protection signal transmitted by the master
[27]	RW	dest_incr	Destination address increment 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	src_incr	Source address increment 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	dest_select	Master for accessing the destination device 0: master 1 1: master 2
[24]	RW	src_select	Master for accessing the source device 0: master 1 1: master 2

[23:21]	RW	dwidth	Transfer bit width of the destination device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of dwidth and the bit width, see Table 3-12.
[20:18]	RW	swidth	Transfer bit width of the source device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of swidth and the bit width, see Table 3-12.
[17:15]	RW	dbsize	Burst size of the destination device It indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCxBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of dbsize and the transfer length, see Table 3-11.
[14:12]	RW	sbsize	Burst size of the source device It indicates the amount of data to be transferred by the source device in a burst transfer, that is, the amount of transferred data when DMACCxBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of sbsize and the transfer length, see Table 3-11.
[11:0]	RW	trans_size	The DMA transfer size can be configured by writing to this register only when the DMAC is a flow controller. This field indicates the amount of data to be transferred by the source device. When this register is read, the amount of data transferred through the bus connected to the destination device is obtained. If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer stops.

DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a configuration register of channel *n* (*n* = 0−3).

Its offset address is 0x110 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													ch_halt	ch_active	ch_lock	tc_int_msk	err_int_msk	flow_ctrl		reserved		dest_periph				reserved		src_periph			ch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[18]	RW	ch_halt	Halt bit 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transmitted. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RW	ch_active	Active bit 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	ch_lock	Lock bit 0: Lock transfer on the bus is disabled. 1: Lock transfer on the bus is enabled.
[15]	RW	tc_int_msk	Transfer terminal interrupt mask 0: The transfer terminal interrupts of the channel are masked. 1: The transfer terminal interrupts of the channel are not masked.

[14]	RW	err_int_msk	Transfer error interrupt mask 0: The error interrupts of the channel are masked. 1: The error interrupts of the channel are not masked.
[13:11]	RW	flow_ctrl	Flow control and transfer type This field specifies the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-14.
[10]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[9:6]	RW	dest_periph	Destination device. This field is used to select a peripheral request signal as the request signal for the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[4:1]	RW	src_periph	Source device. This field is used to select a peripheral request signal as the request signal for the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	ch_en	Channel enable. The current status of the channel can be queried by reading this field or DMAC_ENABLED_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI node is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0, indicating that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. Before enabling a channel by setting this bit to 1, you must reinitialize the channel; otherwise, unexpected results may occur. When a channel is disabled by writing DMAC_Cn_CONFIG [ch_en], DMAC_Cn_CONFIG [ch_en] can be reset again only after the corresponding bit of DMAC_ENABLED_CHNS is 0. This is because the channel is not disabled immediately after the Channel Enable bit is cleared. The running delay during a bus burst operation also needs to be considered.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The Hi3519 V100 has six timers.

3.7.2 Features

Timer has the following features:

- Provides 16-bit or 32-bit down counter that has a programmable 8-bit prescaler.
- Provides a configurable count clock, that is, the clock can serve as the 49.5 MHz bus clock or 3 MHz crystal oscillator clock.
- Supports three count modes: free-running mode, periodic mode, and one-shot mode.
- Loads the initial value through either of the following registers: TIMERx_LOAD and
- TIMERx_BGLOAD.
- Reads the current count value at any time.
- Generates an interrupt when the count value is decreased to 0.

3.7.3 Function Description

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

  The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF. When the count length is 16 bits, the maximum value is 0xFFFF. In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.
- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from

  TIMERx_BGLOAD again and then continues to count.
- One-shot mode

  The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256. In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.

- The count cycle in periodic mode can be set by writing
- TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of
- TIMERx_BGLOAD and starts to count.

3.7.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timer*X* (*X* ranges from 0 to 3), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the bus clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0sel] to 0.

Step 2 Initialize the timer and start to count.

----End

3.7.5 Register Summary

The timer module consists of six timers and each timer involves a group of registers. The six groups of registers have the same features except that their base addresses are different. The details about their base addresses are as follows:

- The base address of timer 0: 0x1200_0000.
- The base address of timer 1: 0x1200_0020.
- The base address of timer 2: 0x1200_1000.
- The base address of timer 3: 0x1200_1020.
- The base address of timer 4: 0x1200_2000.
- The base address of timer 5: 0x1200_2020.

NOTE

The value of *X* in timerX ranges from 0 to 5. The registers for timer 0 to timer 5 are the same. In this section, timer 0 registers are described as an example.

Table 3-16 Summary of timer registers

Offset Address	Register	Description	Page
0x000	TIMERx_LOAD	Initial count value register	3-155
0x004	TIMERx_VALUE	Current count value register	3-156
0x008	TIMERx_CONTROL	Control register	3-156
0x00C	TIMERx_INTCLR	Interrupt clear register	3-158
0x010	TIMERx_RIS	Raw interrupt status register	3-158
0x014	TIMERx_MIS	Masked interrupt status register	3-159
0x018	TIMERx_BGLOAD	Initial count value register in periodic mode	3-159

3.7.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is an initial count value register. It is used to set the initial count value of each timer. Each timer (timers 0–5) has one such register.

NOTE

- The minimum valid value written to TIMERx_LOAD is 1.
- When the value 0 is written to TIMERx_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOAD before the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of

TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and TIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer 0

TIMERx_VALUE

TIMERx_VALUE is a current count value register. It shows the current value of the counter that is decremented. Each timer (timers 0–5) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer 0 that is decremented

TIMERx_CONTROL

TIMERx_CONTROL is a control register. Each timer (timers 0–5) has one such register.

NOTE

When the periodic mode is selected, TIMERx_CONTROL[timermode] must be set to 1 and TIMERx_CONTROL[oneshot] must be set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	timeren	Timer enable 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode 0: free-running mode 1: periodic mode
[5]	RW	intenable	TIMERx_RIS interrupt mask 0: masked 1: not masked
[4]	RO	reserved	Reserved
[3:2]	RW	timerpre	Prescaling factor configuration 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select 0: periodic mode or free-running mode 1: one-shot mode

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timers 0–5) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer 0.

TIMERx_RIS

TIMERx_RIS is a raw interrupt status register. Each timer (timers 0–5) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer 0 0: No interrupt is generated. 1: An interrupt is generated.

TIMERx_MIS

TIMERx_MIS is a masked interrupt status register. Each timer (timers 0–5) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	timer0mis	Masked interrupt status of timer 0 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is an initial count value register in periodic mode. Each timer (timers 0–5) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer 0 Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

3.8 Watchdog

3.8.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.8.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.
- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

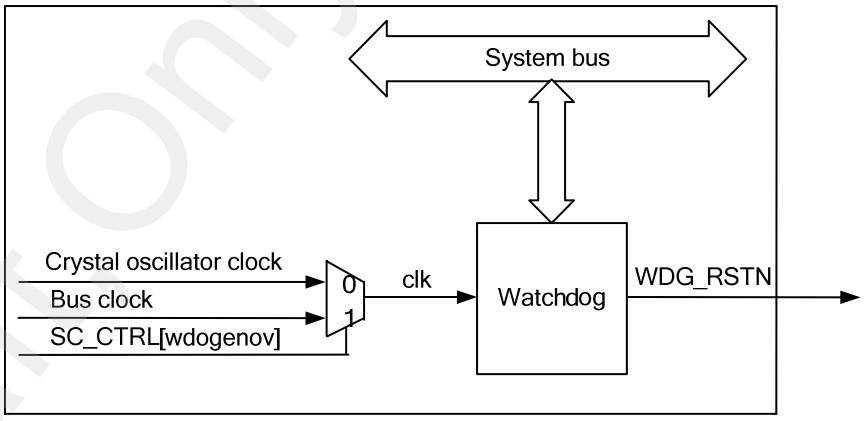
3.8.3 Function Description

Application Block Diagram

The system configures the parameter values of watchdog registers by using the system bus. The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the WDG_RSTN reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-8 shows the application block diagram of the watchdog.

Figure 3-8 Application block diagram of the watchdog



Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on

the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal WDG_RSTN and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.
- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.8.4 Operating Mode

Configuring the Frequency of the Count Clock

The watchdog counting clock is a 3 MHz clock.

The count time T_{WDG} of the watchdog is calculated as follows: $T_{WDG} = Value_{WDG\_LOAD} \times (1/f_{clk})$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG\_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The counting time of the watchdog counting clock ranges from 0s to 1400s.

Initializing the System

The watchdog counter stops counting after the system power-on reset. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

----End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

----End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.8.5 Register Summary

Table 3-17 describes watchdog registers.

Table 3-17 Summary of watchdog registers (base address: 0x1208_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-163
0x0004	WDG_VALUE	Current count value register	3-163
0x0008	WDG_CONTROL	Control register	3-163
0x000C	WDG_INTCLR	Interrupt clear register	3-164
0x0010	WDG_RIS	Raw interrupt register	3-164
0x0014	WDG_MIS	Masked interrupt status register	3-165
0x0C00	WDG_LOCK	Lock register	3-165

3.8.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter

WDG_VALUE

WDG_VALUE is a current count value register It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	resen	Output enable of the watchdog reset signal 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write

			permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.9 RTC

3.9.1 Overview

The RTC is used to display the time in real time and periodically generate alarms.

3.9.2 Features

The RTC has the following features:

- Provides a 40-bit counter. Of the 40 bits, 16 bits are for counting days, five bits are for counting hours, six bits are for counting minutes, six bits are for counting seconds, and the other seven bits are for counting 10 ms.
- Provides a 100 Hz count clock.
- Supports the configurable initial count value.
- Supports the configurable count comparison value.
- Generates the timeout interrupt.
- Supports soft reset.
- Supports configurable frequency division parameters.
- Stores user data in a 64-bit user register.
- Supports battery low-voltage detection.
- Supports the 128-bit DDR standby information register.

3.9.3 Function Description

The RTC has a 40-bit up counter for counting days, hours, minutes, seconds, and 10 ms. The initial values are loaded from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, and RTC_LR_D_H. This section assumes that the counter is divided into the day counter, hour counter, minute counter, second counter, and 10 ms counter. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt. Then, the counter continues to count in incremental mode on the rising edge of the next count clock.

By configuring RTC_IMSC, you can allow or forbid the RTC to generate interrupts. Note the following two cases:

- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MSC_INT shows the status of masked interrupts and RTC_RAW_INT shows the status of raw interrupts.

- When the function of generating interrupts is enabled, the RTC counter still counts in incremental mode. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt.

The RTC uses a 100 Hz count clock and a 16-bit day counter. The value of the day counter can be used to reckon the specific year, month, and day.

3.9.4 Operating Mode

3.9.4.1 Count Clock Frequency

The RTC uses a 100 Hz count clock. The maximum RTC count time (T_{RTC}) is calculated as follows:

$T_{RTC} = 2^{16} = 65536$ days

NOTE

T_{RTC} is the RTC count time.

3.9.4.2 Soft Reset

The RTC can be separately soft-reset by configuring RTC_POR_N. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To soft-reset the RTC, perform the following steps:

Step 1 Write 0 to RTC_POR_N.

Step 2 Wait 30 ms.

----End

3.9.4.3 Initializing the RTC

The system needs to initialize the RTC when the RTC is powered on for the first time. The initialization process is as follows:

Step 1 Configure RTC_POR_N to reset the RTC.

Step 2 Wait 30 ms.

Step 3 Configure RTC_IMSC to set the interrupt mask bit of the RTC.

Step 4 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the RTC match value.

Step 5 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the initial count value of the RTC.

Step 6 Set RTC_LORD to 1 to load the initial count value to the RTC counter.

Step 7 Wait 5 ms.

Step 8 Based on the 100 Hz count clock, the RTC counts starting from the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H. When the count value is equal to the values of RTC_MR_10MS,

RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC determines whether to generate an interrupt based on the settings of RTC_IMSC.

----End

3.9.4.4 Handling Interrupts

If the system receives an interrupt from the RTC, the configured time is reached. Then user-defined operations can be performed. The RTC counter, however, still counts in incremental mode. To clear an RTC interrupt, set RTC_INT_CLR to 1. To continue to configure time, write a new match value to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H.

3.9.4.5 Accessing RTC Registers

Internal RTC registers are located in the RTC module, not on the bus. The RTC registers on the bus are used only for accessing internal RTC registers.

To write to internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This example assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to write 0x10 to RTC_MR_10MS, write 0x01060010 to SPI_RW. That is, spi_start is 1, spi_rw is 0, spi_add is 0x06, and spi_wdata is 0x10.

----End

To read internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This step assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to read SPI_RW, write 0x01860000 to SPI_RW. That is, spi_start is 1, spi_rw is 0, and spi_add is 0x06.

Step 4 Read SPI_RW bit[31] until it is 0. SPI_RW [15:8] is the value that is returned after RTC_MR_10MS is read.

----End

3.9.5 Register Summary

Table 3-18 describes RTC registers.

Table 3-18 Summary of RTC registers (base address: 0x1209_0000)

Offset Address	Register	Description	Page
0x0000	SPI_CLK_DIV	SPI clock divider register	3-172
0x0004	SPI_RW	SPI read/write register	3-173
0x0080	CONVER_T	External temperature sensor DS1820 (DS18B20) measurement control register	3-173
0x0084	CRC_EN	External temperature sensor DS1820 (DS18B20) measurement CRC check enable register	3-174
0x0088	INT_MASK	External temperature sensor DS1820 (DS18B20) measurement interrupt mask register	3-174
0x008C	INT_CLEAR	External temperature sensor DS1820 (DS18B20) measurement interrupt clear register	3-175
0x0090	BUSY	External temperature sensor DS1820 (DS18B20) measurement status register	3-175
0x0094	INT_RAW	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-176
0x0098	INT_TCAP	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-176
0x009C	T_VALUE	External temperature sensor DS1820 (DS18B20) measurement value register	3-177
0x00A0	FILTER_NUM	Filter glitch width configuration register	3-177

Table 3-19 describes the internal RTC registers.

Table 3-19 Summary of internal RTC registers (base address: 0x00)

Offset Address	Register	Description	Page
0x00	RTC_10MS_COUNT	Count value register for the RTC 10 ms counter	3-178

Offset Address	Register	Description	Page
0x01	RTC_S_COUNT	Count value register for the RTC second counter	3-178
0x02	RTC_M_COUNT	Count value register for the RTC minute counter	3-179
0x03	RTC_H_COUNT	Count value register for the RTC hour counter	3-179
0x04	RTC_D_COUNT_L	Lower-8-bit count value register for the RTC day counter	3-180
0x05	RTC_D_COUNT_H	Upper-8-bit count value register for the RTC day counter	3-180
0x06	RTC_MR_10MS	Match value register for the RTC 10 ms counter	3-181
0x07	RTC_MR_S	Match value register for the RTC second counter	3-181
0x08	RTC_MR_M	Match value register for the RTC minute counter	3-182
0x09	RTC_MR_H	Match value register for the RTC hour counter	3-182
0x0A	RTC_MR_D_L	Lower-8-bit match value register for the RTC day counter	3-183
0x0B	RTC_MR_D_H	Upper-8-bit match value register for the RTC day counter	3-183
0x0C	RTC_LR_10MS	Configured value register for the RTC 10 ms counter	3-184
0x0D	RTC_LR_S	Configured value register for the RTC second counter	3-184
0x0E	RTC_LR_M	Configured value register for the RTC minute counter	3-185
0x0F	RTC_LR_H	Configured value register for the RTC hour counter	3-185
0x10	RTC_LR_D_L	Lower-8-bit configured value register for the RTC day counter	3-186
0x11	RTC_LR_D_H	Upper-8-bit configured value register for the RTC day counter	3-186
0x12	RTC_LORD	RTC configured value loading enable register	3-187
0x13	RTC_IMSC	RTC interrupt enable register	3-188
0x14	RTC_INT_CLR	RTC interrupt clear register	3-188

Offset Address	Register	Description	Page
0x15	RTC_MSC_INT	RTC mask interrupt status register.	3-189
0x16	RTC_RAW_INT	RTC raw interrupt status register	3-189
0x17	RTC_CLK	RTC output clock select register	3-190
0x18	RTC_POR_N	RTC reset control register	3-190
0x1A	RTC_UV_CTRL	RTC internal low-voltage detection control register	3-191
0x51	SDM_COEF_OUSIDE_H	External frequency division coefficient upper four bits register	3-192
0x52	SDM_COEF_OUSIDE_L	External frequency division coefficient lower eight bits register	3-192
0x53	USER_REGISTER1	64-bit user register 1	3-192
0x54	USER_REGISTER2	64-bit user register 2	3-193
0x55	USER_REGISTER3	64-bit user register 3	3-193
0x56	USER_REGISTER4	64-bit user register 4	3-193
0x57	USER_REGISTER5	64-bit user register 5	3-194
0x58	USER_REGISTER6	64-bit user register 6	3-194
0x59	USER_REGISTER7	64-bit user register 7	3-194
0x5A	USER_REGISTER8	64-bit user register 8	3-195
0x5F	DDR_SB_CTRL	DDR standby control register	3-195
0x60	DDR_SB_REGISTER0	128-bit DDR standby information register 0	3-196
0x61	DDR_SB_REGISTER1	128-bit DDR standby information register 1	3-196
0x62	DDR_SB_REGISTER2	128-bit DDR standby information register 2	3-196
0x63	DDR_SB_REGISTER3	128-bit DDR standby information register 3	3-197
0x64	DDR_SB_REGISTER4	128-bit DDR standby information register 4	3-197
0x65	DDR_SB_REGISTER5	128-bit DDR standby information register 5	3-198
0x66	DDR_SB_REGISTER6	128-bit DDR standby information register 6	3-198
0x67	DDR_SB_REGISTER7	128-bit DDR standby information register 7	3-198

Offset Address	Register	Description	Page
0x68	DDR_SB_REGISTER8	128-bit DDR standby information register 8	3-199
0x69	DDR_SB_REGISTER9	128-bit DDR standby information register 9	3-199
0x6A	DDR_SB_REGISTER10	128-bit DDR standby information register 10	3-199
0x6B	DDR_SB_REGISTER11	128-bit DDR standby information register 11	3-200
0x6C	DDR_SB_REGISTER12	128-bit DDR standby information register 12	3-200
0x6D	DDR_SB_REGISTER13	128-bit DDR standby information register 13	3-201
0x6E	DDR_SB_REGISTER14	128-bit DDR standby information register 14	3-201
0x6F	DDR_SB_REGISTER15	128-bit DDR standby information register 15	3-201

3.9.6 RTC Register Description

SPI_CLK_DIV

SPI_CLK_DIV is an SPI clock divider register.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	spi_clk_div	SPI clock divider. The SPI clock frequency cannot be higher than 20 MHz. The value 12 MHz is recommended. The field value ranges from 1 to 255. The value of spi_clk_div is used to define the SPI RX and RX bit rates. The formula is as follows: FSPICLK = FAPBCLK/[2 x (spi_clk_div + 1)]. FAPBCLK is the clock frequency. If the clock is 120 MHz and the expected SPI clock is 12 MHz, the configured value of spi_clk_div is calculated as follows: (120/12)/2 – 1 = 4

SPI_RW

SPI_RW is an SPI read/write register.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_busy	reserved							spi_start	spi_rw	spi_add						spi_rdata								spi_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	spi_busy	SPI read/write status indicator 0: The SPI is idle, and a new read/write operation can be initiated over the SPI. 1: A read/write operation is being performed over the SPI, and no new operation is allowed.
[30:25]	RO	reserved	Reserved
[24]	W1_PULSE	spi_start	SPI read/write start. Writing 1 automatically clears this field. Writing has no effect when spi_busy is 1. That is, no new SPI operation is started before the previous read/write operation is complete. If a start request is sent, hardware ignores this request.
[23]	RW	spi_rw	SPI operation type 0: write 1: read
[22:16]	RW	spi_add	SPI operation address The address range is 0–127.
[15:8]	RO	spi_rdata	Data read from the SPI
[7:0]	RW	spi_wdata	Data to be written to the SPI

CONVER_T

CONVER_T is an external temperature sensor DS1820 (DS18B20) measurement control register.

Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															conver_t
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	conver_t	External temperature sensor DS1820 (DS18B20) measurement start. This field must be set to 1. 1: start. Hardware automatically sets this field to 0 when the interrupt is cleared.

CRC_EN

CRC_EN is an external temperature sensor DS1820 (DS18B20) measurement CRC check enable register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	crc_en	External temperature sensor DS1820 (DS18B20) measurement CRC check enable 0: disabled 1: enabled

INT_MASK

INT_MASK is an external temperature sensor DS1820 (DS18B20) measurement interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_mask	External temperature sensor DS1820 (DS18B20) measurement interrupt mask 0: not masked 1: masked

INT_CLEAR

INT_CLEAR is an external temperature sensor DS1820 (DS18B20) measurement interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_clear	External temperature sensor DS1820 (DS18B20) measurement interrupt clear Writing 1 clears the interrupt. Hardware automatically sets this field to 0 after the interrupt is cleared.

BUSY

BUSY is an external temperature sensor DS1820 (DS18B20) measurement status register.

Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	busy	External temperature sensor DS1820 (DS18B20) measurement status 0: ready 1: busy

INT_RAW

INT_RAW is an external temperature sensor DS1820 (DS18B20) raw measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														int_err	get_tmprt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	int_err	Error interrupt
[0]	RO	get_tmprt_int	External temperature sensor DS1820 (DS18B20) measurement completion interrupt

INT_TCAP

INT_TCAP is an external temperature sensor DS1820 (DS18B20) measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_tcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	int_tcap	Masked interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

T_VALUE

T_VALUE is an external temperature sensor DS1820 (DS18B20) measurement value register.

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				t_value											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	t_value	Temperature measured by the external temperature sensor DS1820 (DS18B20)

FILTER_NUM

FILTER_NUM is a filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												filter_num			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	filter_num	Filter glitch width for inputs. The glitch with the width of (*N* + 1) APB clocks is filtered.

3.9.7 Internal Register Description

RTC_10MS_COUNT

RTC_10MS_COUNT is a count value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_10ms_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RO	rtc_10ms_count	RTC 10 ms counter value. It indicates the currently counted time. Its unit is 10 ms. The value range is 0–99.

RTC_S_COUNT

RTC_S_COUNT is a count value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_s_count					

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_s_count	RTC second counter value. It indicates the currently counted seconds. The value range is 0–59.

RTC_M_COUNT

RTC_M_COUNT is a count value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_m_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_m_count	RTC minute counter value. It indicates the currently counted minutes. The value range is 0–59.

RTC_H_COUNT

RTC_H_COUNT is a count value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved

[4:0]	RO	rtc_h_count	RTC hour counter value. It indicates the currently counted hours. The value range is 0–23.

RTC_D_COUNT_L

RTC_D_COUNT_L is a lower-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	Lower eight bits of the RTC day counter value. This field works with RTC_D_COUNT_H to indicate the currently counted days. The day range is 0–65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is an upper-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	Upper eight bits of the RTC day counter value. This field works with RTC_D_COUNT_L to indicate the currently counted day. The day range is 0–65535.

RTC_MR_10MS

RTC_MR_10MS is a match value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_mr_10ms	Match value of the RTC 10 ms counter The value range is 0–99.

RTC_MR_S

RTC_MR_S is a match value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_mr_s	Match value of the RTC second counter The value range is 0–59.

RTC_MR_M

RTC_MR_M is a match value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_mr_m	Match value of the RTC minute counter The value range is 0–59.

RTC_MR_H

RTC_MR_H is a match value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RW	rtc_mr_h	Match value of the RTC hour counter The value range is 0–23.

RTC_MR_D_L

RTC_MR_D_L is a lower-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	Lower eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_H to indicate the matched day. The day range is 0–65535.

RTC_MR_D_H

RTC_MR_D_H is an upper-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	Upper eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_L to indicate the matched day. The day range is 0–65535.

RTC_LR_10MS

RTC_LR_10MS is a configured value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_lr_10ms	Configured value of the RTC 10 ms counter The value range is 0–99.

RTC_LR_S

RTC_LR_S is a configured value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_s					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_s	Configured value of the RTC second counter The value range is 0–59.

RTC_LR_M

RTC_LR_M is a configured value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_m					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_m	Configured value of the RTC minute counter The value range is 0–59.

RTC_LR_H

RTC_LR_H is a configured value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RW	rtc_lr_h	Configured value of the RTC hour counter The value range is 0–23.

RTC_LR_D_L

RTC_LR_D_L is a lower-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_l	Lower eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_H to indicate the configured day. The day range is 0–65535.

RTC_LR_D_H

RTC_LR_D_H is an upper-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_h	Upper eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_L to indicate the configured day. The day range is 0–65535.

RTC_LORD

RTC_LORD is an RTC configured value loading enable register.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_lock_bypass	rtc_lock	rtc_load
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved
[2]	RW	rtc_lock_bypass	RTC lock enable 0: enabled. The RTC count value (0x00−0x05) is updated only after the RTC is successfully locked. 1: disabled. The RTC count value (0x00−0x05) is updated in real time.
[1]	RW	rtc_lock	RTC lock. If software writes 1, hardware is automatically cleared after the RTC is successfully locked. Note: This field is valid only when rtc_lock_bypass is 0.
[0]	RW	rtc_load	RTC configured value loading enable. When the field is enabled, the RTC configured value will be loaded to the RTC accumulator. If software writes 1 to load the configured value, hardware will automatically set this field to 0 after successful loading.

RTC_IMSC

RTC_IMSC is an RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_imsc	rtc_imsc_uv	rtc_imsc_time
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved
[2]	RW	rtc_imsc	RTC global interrupt output enable 0: disabled 1: enabled
[1]	RW	rtc_imsc_uv	Battery low-voltage detection interrupt output enable 0: disabled 1: enabled
[0]	RW	rtc_imsc_time	RTC timing interrupt output enable 0: disabled 1: enabled

RTC_INT_CLR

RTC_INT_CLR is an RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_int_clr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	WO	rtc_int_clr	RTC interrupt clear register. Writing any value by software clears the interrupt. Reading back the value has no effect.

RTC_MSC_INT

RTC_MSC_INT is an RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						mask_int_uv	mask_int_time
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1]	RO	mask_int_uv	Status of the masked battery low-voltage detection interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	mask_int_time	Status of the masked RTC timing interrupt 0: No interrupt is generated. 1: An interrupt is generated.

RTC_RAW_INT

RTC_RAW_INT is an RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						raw_int_uv	raw_int_time
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved

[1]	RO	raw_int_uv	Status of the raw battery low-voltage detection interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	raw_int_time	Status of the raw RTC timing interrupt 0: No interrupt is generated. 1: An interrupt is generated.

RTC_CLK

RTC_CLK is an RTC output clock select register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						clk_out_sel	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1:0]	RW	clk_out_sel	Output test clock of the RTC 00: crystal oscillator clock 01: corrected 100 Hz clock 1x: 1 Hz clock

RTC_POR_N

RTC_POR_N is an RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_por_n

Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	RW	rtc_por_n	RTC reset. This field is automatically set to 1 after the RTC is successfully reset. 0: reset

RTC_UV_CTRL

RTC_UV_CTRL is an RTC internal low-voltage detection control register.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_UV_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		bat_uv_ctrl_en	bat_uv_ctrl_sel	reserved		sample_time	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5]	RW	bat_uv_ctrl_en	Low-voltage detection enable 0: disabled 1: enabled
[4]	RW	bat_uv_ctrl_sel	Low-voltage detection source select 0: no filtering 1: filtering
[3:2]	RO	reserved	Reserved
[1:0]	RW	sample_time	Low-voltage detection cycle 00: 1s 01: 1 minute 10: 10 minutes 11: 30 minutes

SDM_COEF_OUSIDE_H

SDM_COEF_OUSIDE_H is an external frequency division coefficient upper four bits register.

Offset Address	Register Name	Total Reset Value
0x51	SDM_COEF_OUSIDE_H	0x8

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Sdm_coef_ouside_h			
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3:0]	RW	Sdm_coef_ouside_h	Upper four bits of the frequency division coefficient in fixed frequency-division mode

SDM_COEF_OUSIDE_L

SDM_COEF_OUSIDE_L is an external frequency division coefficient lower eight bits register.

Offset Address	Register Name	Total Reset Value
0x52	SDM_COEF_OUSIDE_L	0x1B

Bit	7	6	5	4	3	2	1	0
Name	sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	sdm_coef_ouside_l	Lower eight bits of the frequency division coefficient in fixed frequency-division mode Note: When clock divider registers (addresses of 0x51 and 0x52) are read or written, you need to read or write to the upper four bits and then the lower eight bits continuously. The clock divider is calculated as follows: (f − 32700) x 30.52. f indicates the oscillation frequency of the external crystal and ranges from 32700 to 32799.

USER_REGISTER1

USER_REGISTER1 is 64-bit user register 1.

Offset Address	Register Name	Total Reset Value
0x53	USER_REGISTER1	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register1	64-bit user register 1 corresponding to bit[7:0]

USER_REGISTER2

USER_REGISTER2 is 64-bit user register 2.

Offset Address	Register Name	Total Reset Value
0x54	USER_REGISTER2	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register2	64-bit user register 2 corresponding to bit[15:8]

USER_REGISTER3

USER_REGISTER3 is 64-bit user register 3.

Offset Address	Register Name	Total Reset Value
0x55	USER_REGISTER3	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register3	64-bit user register 3 corresponding to bit[23:16]

USER_REGISTER4

USER_REGISTER4 is 64-bit user register 4.

Offset Address	Register Name	Total Reset Value
0x56	USER_REGISTER4	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register4	64-bit user register 4 corresponding to bit[31:24]

USER_REGISTER5

USER_REGISTER5 is 64-bit user register 5.

Offset Address	Register Name	Total Reset Value
0x57	USER_REGISTER5	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register5	64-bit user register 5 corresponding to bit[39:32]

USER_REGISTER6

USER_REGISTER6 is 64-bit user register 6.

Offset Address	Register Name	Total Reset Value
0x58	USER_REGISTER6	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register6	64-bit user register 6 corresponding to bit[47:40]

USER_REGISTER7

USER_REGISTER7 is 64-bit user register 7.

Offset Address	Register Name	Total Reset Value
0x59	USER_REGISTER7	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register7	64-bit user register 7 corresponding to bit[55:48]

USER_REGISTER8

USER_REGISTER8 is 64-bit user register 8.

Offset Address	Register Name	Total Reset Value
0x5A	USER_REGISTER8	0x0

Bit	7	6	5	4	3	2	1	0
Name	2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register8	64-bit user register 8 corresponding to bit[63:56]

DDR_SB_CTRL

DDR_SB_CTRL is a DDR standby control register.

Offset Address	Register Name	Total Reset Value
0x5F	DDR_SB_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						ddr_ioctrl_lhen	ddrc_ctrl_iso
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved

[1]	RW	ddr_ioctrl_lhen	DDR I/O latch enable 0: disabled 1: enabled
[0]	RW	ddrc_ctrl_iso	Isolated control of the DDRC system reset 0: The system is reset. 1: The system fails to be reset.

DDR_SB_REGISTER0

DDR_SB_REGISTER0 is 128-bit DDR standby information register 0.

Offset Address	Register Name	Total Reset Value
0x60	DDR_SB_REGISTER0	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register0	128-bit DDR standby information register 0, corresponding to bit[7:0]

DDR_SB_REGISTER1

DDR_SB_REGISTER1 is 128-bit DDR standby information register 1.

Offset Address	Register Name	Total Reset Value
0x61	DDR_SB_REGISTER1	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register1	128-bit DDR standby information register 1, corresponding to bit[15:8]

DDR_SB_REGISTER2

DDR_SB_REGISTER2 is 128-bit DDR standby information register 2.

Offset Address	Register Name	Total Reset Value
0x62	DDR_SB_REGISTER2	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register2	128-bit DDR standby information register 2, corresponding to bit[23:16]

DDR_SB_REGISTER3

DDR_SB_REGISTER3 is 128-bit DDR standby information register 3.

Offset Address	Register Name	Total Reset Value
0x63	DDR_SB_REGISTER3	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register3	128-bit DDR standby information register 3, corresponding to bit[31:24]

DDR_SB_REGISTER4

DDR_SB_REGISTER4 is 128-bit DDR standby information register 4.

Offset Address	Register Name	Total Reset Value
0x64	DDR_SB_REGISTER4	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register4	128-bit DDR standby information register 4, corresponding to bit[39:32]

DDR_SB_REGISTER5

DDR_SB_REGISTER5 is 128-bit DDR standby information register 5.

Offset Address	Register Name	Total Reset Value
0x65	DDR_SB_REGISTER5	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register5	128-bit DDR standby information register 5, corresponding to bit[47:40]

DDR_SB_REGISTER6

DDR_SB_REGISTER6 is 128-bit DDR standby information register 6.

Offset Address	Register Name	Total Reset Value
0x66	DDR_SB_REGISTER6	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register6	128-bit DDR standby information register 6, corresponding to bit[55:48]

DDR_SB_REGISTER7

DDR_SB_REGISTER7 is 128-bit DDR standby information register 7.

Offset Address	Register Name	Total Reset Value
0x67	DDR_SB_REGISTER7	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register7	128-bit DDR standby information register 7, corresponding to bit[63:56]

DDR_SB_REGISTER8

DDR_SB_REGISTER8 is 128-bit DDR standby information register 8.

Offset Address	Register Name	Total Reset Value
0x68	DDR_SB_REGISTER8	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register8							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register8	128-bit DDR standby information register 8, corresponding to bit[71:64]

DDR_SB_REGISTER9

DDR_SB_REGISTER9 is 128-bit DDR standby information register 9.

Offset Address	Register Name	Total Reset Value
0x69	DDR_SB_REGISTER9	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register9							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register9	128-bit DDR standby information register 9, corresponding to bit[79:72]

DDR_SB_REGISTER10

DDR_SB_REGISTER10 is 128-bit DDR standby information register 10.

Offset Address	Register Name	Total Reset Value
0x6A	DDR_SB_REGISTER10	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register10							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register10	128-bit DDR standby information register 10, corresponding to bit[87:80]

DDR_SB_REGISTER11

DDR_SB_REGISTER11 is 128-bit DDR standby information register 11.

Offset Address	Register Name	Total Reset Value
0x6B	DDR_SB_REGISTER11	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register11							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register11	128-bit DDR standby information register 11, corresponding to bit[95:88]

DDR_SB_REGISTER12

DDR_SB_REGISTER12 is 128-bit DDR standby information register 12.

Offset Address	Register Name	Total Reset Value
0x6C	DDR_SB_REGISTER12	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register12							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register12	128-bit DDR standby information register 12, corresponding to bit[103:96]

DDR_SB_REGISTER13

DDR_SB_REGISTER13 is 128-bit DDR standby information register 13.

Offset Address	Register Name	Total Reset Value
0x6D	DDR_SB_REGISTER13	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register13							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register13	128-bit DDR standby information register 13, corresponding to bit[111:104]

DDR_SB_REGISTER14

DDR_SB_REGISTER14 is 128-bit DDR standby information register 14.

Offset Address	Register Name	Total Reset Value
0x6E	DDR_SB_REGISTER14	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register14							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register14	128-bit DDR standby information register 14, corresponding to bit[119:112]

DDR_SB_REGISTER15

DDR_SB_REGISTER15 is 128-bit DDR standby information register 15.

Offset Address	Register Name	Total Reset Value
0x6F	DDR_SB_REGISTER15	0x00

Bit	7	6	5	4	3	2	1	0
Name	ddr_sb_register15							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ddr_sb_register15	128-bit DDR standby information register 15, corresponding to bit[127:120]

3.10 Power Management and Low-Power Mode Control

3.10.1 Overview

In low-power mode, the power consumption of the chip is reduced effectively. The Hi3519 V100 reduces its power consumption in the following low-power control modes:

- Clock gating and clock frequency adjustment

  The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.
- Module low-power control

  When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.
- DDR low-power control

  The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.
- DVFS based on A17 CPU load monitoring

3.10.2 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce chip power consumption. For details about the process, see the description in section "clock gating" of each module.

The system can adjust its working frequency to reduce chip power consumption. To adjust the system working frequency, perform the following steps:

- Disable the service module to prevent it from accessing the DDR.
- Enable the system to run in the off-chip memory.

When DDRC_CTRL_SREF [sr_seq] is set to a valid value, the DDRC forces the DDR*n* SDRAM to enter the self-refresh mode.

Step 1 Set PERI_CRG13 to select the clock sources for the system bus, DDRC, and CPU.

Step 2 Wait and configure DDRC_CTRL_SREF to enable the DDRC to exit the self-refresh mode based on the configuration requirements of the DDRC.

Step 3 The program starts to run in the DDR.

----End

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.3 "Clock Distribution."

3.10.3 Module Low-Power Control

Most modules including USB 2.0 host/device, USB 3.0 host/device, PCIe, video DAC and PLL modules support low-power operating modes. For details, see the descriptions of the system controller and clocks.

- Low-power control for the USB 2.0 host/device module

  If the USB 2.0 function is not used, the USB 2.0 PHY clock can be disabled by setting PERI_CRG45 bit[7] to 0.

- Lower-power control for the USB 3.0 host/device and PCIe module

  If the USB 3.0 function is not used, the USB 3.0 CTRL clock can be disabled by configuring the corresponding clock gating bit of PERI_CRG46.

  If the PCIe function is not used, the PCIe CTRL clock can be disabled by configuring the corresponding clock gating bit of PERI_CRG44.

  If the USB 3.0 and PCIe functions are not used, the COMB PHY clock can be disabled by configuring the corresponding clock gating bit of PERI_CRG43.

- Low-power control for the video DAC module

  If the video DAC function is not used, the CVBS channel can be disabled to reduce power consumption. For details, see section 9.2 "VDP."

- The PLL also supports the low-power mode. If the PLL is not used, it can be disabled to switch the system to low-power mode. For details, see the description of the power-down control bit in the CRG register PERI_CRG_PLLn.

3.10.4 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

3.10.5 DVFS and AVS

The DVFS technology is used to dynamically configure the voltage and frequency based on the application scenario to meet the requirements on the current circuit timings and performance. The working frequency and operating voltage of the CPU can be configured based on the application scenario.

The AVS technology further reduces power consumption by dynamically adjusting the voltage in real time based on the chip technology, temperature, and circuit timings. The system obtains the chip PVT information by using the PMC and implements automatic voltage scaling by using the PWM output signal in the PMC. For details, see section 3.11 "PMC."

3.11 PMC

3.11.1 Function Description

The PMC provides basic information about power consumption management of the chip and controls the power consumption.

- PWM output

The PMC provides a programmable PWM module. The peripheral PWM voltage scaling circuit can be used to adjust the power supply voltage of the chip through the PWM outputs of the chip. Hi3519 V100 provides four PWM outputs.

- High performance monitor (HPM) control

  The HPM can be used to obtain the comprehensive PVT information about the chip. The reference power supply voltage scaling solution can be developed based on the PVT information.

- Hardware AVS

  After the hardware AVS function is enabled, the chip obtains the HPM monitoring value periodically. The PWM output duty cycle is adjusted based on the configured policy to implement adaptive adjustment of the power supply voltage.

- Internal temperature detection

  The chip has an integrated temperature sensor for obtaining the internal chip temperature and providing temperature information for temperature protection.

- Power-on/Power-off control for the CPU A17 core

  The power switch control register and related logic of the CPU A17 core are provided to control its power-on and power-off.

3.11.2 Operating Mode

PWM Output

The PWM module in the PMC has a 24 MHz working clock, a 16-bit cycle counter, and a 16-bit duty cycle counter. The count cycle and duty cycle of the PWM output can be specified by configuring the PWM-related registers in the PMC.

To configure the count cycle and duty cycle of the PWM output, perform the following steps:

Step 1 Calculate the number of PWM count cycles and the count value of the high level based on the required PWM output frequency and duty cycle.

The number of count cycles is calculated as follows: pwm_period = (24000000/Frequency) − 1

The count value of the high level is calculated as follows: pwm_duty = (24000000/Frequency) x Duty − 1

Step 2 Configure the PWM count cycle and high level count value register.

Step 3 Enable the PWM output.

----End

For example, the voltage of the core power supply is controlled by the PWM0 signal. Perform the following steps if the required PWM0 output frequency is 200 kHz and the duty cycle is 75%:

Step 1 Calculate the required number of count cycles and count value of the high level.

Pwm_period = (24000000/200000) − 1 = 119

Pwm_duty = (24000000/200000) x 0.75 – 1 = 89

Step 2 Configure the parameters of the PWM corresponding to the core power supply by setting PERI_PMC0 bit[15:0] to **0x77** and PERI_PMC0 bit[31:16] to **0x59**.

Step 3 Enable the PWM corresponding to the core power supply by setting PERI_PMC4 bit[0] to **1**.

----End

HPM Control

The chip has four core HPMs for obtaining the PVT information about the core, MDDRC, A17 CPU, and media modules.

The source clock of the HPM reference clock is a 200 MHz clock. You are advised to set core_hpm_div to 0x3 to ensure that the HPM monitoring value is precise and the frequency of the HPM reference clock is close to 50 MHz.

The following describes the HPM configuration procedure by taking the core HPM monitoring value as an example:

Step 1 Set the HPM capture mode.

The HPM has two capture modes: single capture mode and cyclic capture mode. For details, see the description of PERI_PMC10.

If the cyclic capture mode is used, the capture cycle needs to be configured. The capture cycle T (in ms) is calculated as follows: T = (N x 2048 + M x 16)/1000 (N = PERI_PMC13 bit[31:24], M = PERI_PMC31 bit[7:0])

Step 2 Set core_hpm_div to 0x3, deassert reset, and start HPM capture.

Set PERI_PMC10 to 0x04000003 and 0x05000003 in sequence. Then enable the cyclic HPM capture mode.

Step 3 Wait until core_hpm_pc_valid is 1. Then software reads the HPM monitoring value.

Step 4 In single capture mode, only HPM original code pattern 0 recorded in PERI_PMC11 bit[9:0] is valid.

In cyclic capture mode, the latest four HPM original code patterns (patterns 0−3) are recorded in PERI_PMC11 bit[9:0], PERI_PMC11 bit[21:12], PERI_PMC12 bit[9:0], and PERI_PMC12 bit[21:12]. The latest recorded value is HPM original code pattern 0.

----End

Hardware AVS

The chip automatically adjusts the PWM output duty cycle based on the HPM monitoring value by using the hardware AVS function of the PMC to implement automatic power supply voltage scaling.

The Hi3519 V100 supports hardware AVS for the HPMs of the core, MDDRC, A17 CPU, and media modules. The following describes the hardware AVS start process by taking the core module as an example:

Step 1 Specify the hardware AVS calculation mode by configuring PERI_PMC5 bit[2:1].

Step 2 Specify the voltage scaling step of hardware AVS by configuring PERI_PMC5 bit[31:16].

Step 3 Enable hardware AVS by setting PERI_PMC5 bit[0] to 1.

----End

Internal Temperature Detection

The chip has an integrated temperature sensor and the detected temperature ranges from −40ºC (−40ºF) to +140ºC (+284ºF). To enable the temperature sensor to collect data, perform the following steps:

Step 1 Set the capture mode of the temperature sensor.

The temperature sensor captures the temperature in two modes: single capture mode and cyclic capture mode. For details, see the description of PERI_PMC68.

If the cyclic capture mode is used, the capture cycle needs to be configured. The capture cycle (in ms) is calculated as follows: Capture cycle = tsensor_monitor_period x 2.

Step 2 Enable the temperature sensor to start collecting the temperature code.

Step 3 Software reads the temperature code captured by the temperature sensor.

In single capture mode, only temperature code 0 recorded in PERI_PMC70 bit[9:0] is valid.

In cyclic capture mode, the latest eight temperature codes (codes 0−7) are recorded in PERI_PMC70 to PERI_PMC73. The latest recorded temperature data is temperature code 0.

Step 4 Calculate the corresponding temperature value based on the recorded temperature code.

The temperature value T (in ºC) is calculated as follows: T = [(tsensor_temp_code − 125)/806] x 165 − 40

Note: The value range of tsensor_temp_code is [125, 931].

----End

Power-on/Power-off Control for the CPU A17 Core

The PMC supports power-on/power-off control for the CPU A17 core by using logic.

To power-off the A17, perform the following steps:

Step 1 Set PERI_PMC79[mode_onoff] to 0x0 to enable the A17 power-on/power-off logic control function. Write 0 and then 1 to PERI_PMC79[power_off_en] to enable the power-on timing state machine of the PMC A17 core.

Step 2 The logic isolates the A17 output signal after the related handshake signal is detected, and turns off the power supply of A17.

----End

To power-on the A17, perform the following steps:

Step 1 Set PERI_PMC79[mode_onoff] to 0x0 to enable the A17 power-on/power-off logic control function.

Step 2 Configure PERI_PMC79[trigger_mode] to select the interrupt trigger mode or software trigger mode.

If the interrupt trigger mode is selected, irq_poweron_en and fiq_poweron_en need to be configured to determine the interrupt source that triggers the power-on operation.

Step 3 The logic turns on the power supply of A17 and deasserts the isolation on the A17 output signal after detecting the power-on trigger condition.

When the interrupt trigger mode is selected, the power-on trigger condition is determined by irq_poweron_en and fiq_poweron_en.

When the software trigger mode is selected, the power-on operation is triggered when the level of power_on_en is changed from low to high (that is, writing 0 and then 1 to power_on_en).

----End

3.11.3 PMC Register Summary

Table 3-20 describes PMC registers.

Table 3-20 Summary of PMC registers (base address: 0x120A_0000)

Offset Address	Register	Description	Page
0x0000	PERI_PMC0	PMC register 0	3-208
0x0004	PERI_PMC1	PMC register 1	3-209
0x0008	PERI_PMC2	PMC register 2	3-209
0x000C	PERI_PMC3	PMC register 3	3-210
0x0010	PERI_PMC4	PMC register 4	3-210
0x0014	PERI_PMC5	PMC register 5	3-212
0x0018	PERI_PMC6	PMC register 6	3-213
0x001C	PERI_PMC7	PMC register 7	3-214
0x0020	PERI_PMC8	PMC register 8	3-215
0x0028	PERI_PMC10	Core HPM control register 1	3-216
0x002C	PERI_PMC11	Core HPM status register 1	3-217
0x0030	PERI_PMC12	Core HPM status register 2	3-218
0x0034	PERI_PMC13	Core HPM control register 2	3-219
0x0038	PERI_PMC14	A17 HPM control register 1	3-220
0x003C	PERI_PMC15	A17 HPM status register 1	3-221
0x0040	PERI_PMC16	A17 HPM status register 2	3-221
0x0044	PERI_PMC17	A17 HPM control register 2	3-222
0x0048	PERI_PMC18	DDR HPM control register 1	3-223
0x004C	PERI_PMC19	DDR HPM status register 1	3-224
0x0050	PERI_PMC20	DDR HPM status register 2	3-224
0x0054	PERI_PMC21	DDR HPM control register 2	3-225

Offset Address	Register	Description	Page
0x0058	PERI_PMC22	MDA0 HPM control register 1	3-226
0x005C	PERI_PMC23	MDA0 HPM status register 1	3-227
0x0060	PERI_PMC24	MDA0 HPM status register 2	3-227
0x0064	PERI_PMC25	MDA0 HPM control register 2	3-228
0x0078	PERI_PMC30	HPM control register (fine 1)	3-229
0x007C	PERI_PMC31	HPM control register (fine 2)	3-229
0x110	PERI_PMC68	PMC register 68	3-230
0x0114	PERI_PMC69	PMC register 69	3-230
0x0118	PERI_PMC70	PMC register 70	3-231
0x011C	PERI_PMC71	PMC register 71	3-231
0x0120	PERI_PMC72	PMC register 72	3-232
0x0124	PERI_PMC73	PMC register 73	3-232
0x0128	PERI_PMC74	PMC register 74	3-233
0x0134	PERI_PMC77	PMC register 77	3-234
0x0138	PERI_PMC78	PMC register 78	3-235
0x013C	PERI_PMC79	PMC register 79	3-237
0x0140	PERI_PMC80	PMC register 80	3-238
0x0144	PERI_PMC81	PMC register 81	3-239
0x0148	PERI_PMC82	PMC register 82	3-239
0x014C	PERI_PMC83	PMC register 83	3-240
0x0150	PERI_PMC84	PMC register 84	3-240
0x0154	PERI_PMC85	PMC register 85	3-240
0x0158	PERI_PMC86	PMC register 86	3-241
0x015C	PERI_PMC87	PMC register 87	3-241
0x0160	PERI_PMC88	PMC register 88	3-242

3.11.4 PMC Register Description

PERI_PMC0

PERI_PMC0 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_PMC0	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_pwm_duty																core_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	core_pwm_duty	Number of PWM high-level beats for the core AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	core_pwm_period	Number of PWM cycles for the core AVS output

PERI_PMC1

PERI_PMC1 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_PMC1	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_pwm_duty																a17_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	a17_pwm_duty	Number of PWM high-level beats for the A17 AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	a17_pwm_period	Number of PWM cycles for the A17 AVS output. The value cannot be 0. If the configured value is 0, the value 1 takes effect. That is, the value that takes effect is the configured value plus 1.

PERI_PMC2

PERI_PMC2 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_PMC2	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddr_pwm_duty																ddr_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ddr_pwm_duty	Number of PWM high-level beats for the DDR AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	ddr_pwm_period	Number of PWM cycles for the DDR AVS output. The value cannot be 0. If the configured value is 0, the value 1 takes effect. That is, the value that takes effect is the configured value plus 1.

PERI_PMC3

PERI_PMC3 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x000c	PERI_PMC3	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0_pwm_duty																mda0_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mda0_pwm_duty	Number of PWM high-level beats for the MDA0 AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	mda0_pwm_period	Number of PWM cycles for the MDA0 AVS output. The value cannot be 0. If the configured value is 0, the value 1 takes effect. That is, the value that takes effect is the configured value plus 1.

PERI_PMC4

PERI_PMC4 is PMC register 4.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_PMC4	0x0000_E400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pwm3_reuse_cfg		pwm2_reuse_cfg		pwm1_reuse_cfg		pwm0_reuse_cfg		mda_pwm_inv	mda_pwm_enable	ddr_pwm_inv	ddr_pwm_enable	a17_pwm_inv	a17_pwm_enable	core_pwm_inv	core_pwm_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:14]	RW	pwm3_reuse_cfg	PWM3 source select for the AVS output 00: core 01: CPU 10: DDR 11: MDA
[13:12]	RW	pwm2_reuse_cfg	PWM2 source select for the AVS output 00: core 01: CPU 10: DDR 11: MDA
[11:10]	RW	pwm1_reuse_cfg	PWM1 source select for the AVS output 00: core 01: CPU 10: DDR 11: MDA
[9:8]	RW	pwm0_reuse_cfg	PWM0 source select for the AVS output 00: core 01: CPU 10: DDR 11: MDA
[7]	RW	mda_pwm_inv	PWM phase control for the MDA0 AVS output 0: normal output 1: inverted output

[6]	RW	mda_pwm_enable	PWM enable for the MDA0 AVS output 0: disabled 1: enabled
[5]	RW	ddr_pwm_inv	PWM phase control for the DDR AVS output 0: normal output 1: inverted output
[4]	RW	ddr_pwm_enable	PWM enable for the DDR AVS output 0: disabled 1: enabled
[3]	RW	a17_pwm_inv	PWM phase control for the A17 AVS output 0: normal output 1: inverted output
[2]	RW	a17_pwm_enable	PWM enable for the A17 AVS output 0: disabled 1: enabled
[1]	RW	core_pwm_inv	PWM phase control for the core AVS output 0: normal output 1: inverted output
[0]	RW	core_pwm_enable	PWM enable for the core AVS output 0: disabled 1: enabled

PERI_PMC5

PERI_PMC5 is PMC register 5.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_PMC5	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	core_avs_fsm_inc_pwm_step		core_avs_fsm_dec_pwm_step		reserved			core_avs_hpm_fsm_calc_mode	core_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RW	core_avs_fsm_inc_pwm_step	Automatic increase step of the core AVS FSM PWM
[23:16]	RW	core_avs_fsm_dec_pwm_step	Automatic decrease step of the core AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	core_avs_hpm_fsm_calc_mode	Calculation mode of the core AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	core_hpm_fsm_en	Core AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC6

PERI_PMC6 is PMC register 6.

Offset Address	Register Name	Total Reset Value
0x0018	PERI_PMC6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	a17_avs_fsm_inc_pwm_step		a17_avs_fsm_dec_pwm_step		reserved			a17_avs_hpm_fsm_calc_mode	a17_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RW	a17_avs_fsm_inc_pwm_step	Automatic increase step of the A17 AVS FSM PWM
[23:16]	RW	a17_avs_fsm_dec_pwm_step	Automatic decrease step of the A17 AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	a17_avs_hpm_fsm_calc_mode	Calculation mode of the A17 AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	a17_hpm_fsm_en	A17 AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC7

PERI_PMC7 is PMC register 7.

Offset Address	Register Name	Total Reset Value
0x001c	PERI_PMC7	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	ddr_avs_fsm_inc_pwm_step		ddr_avs_fsm_dec_pwm_step		reserved			ddr_avs_hpm_fsm_calc_mode	ddr_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RW	ddr_avs_fsm_inc_pwm_step	Automatic increase step of the DDR AVS FSM PWM
[23:16]	RW	ddr_avs_fsm_dec_pwm_step	Automatic decrease step of the DDR AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	ddr_avs_hpm_fsm_calc_mode	Calculation mode of the DDR AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	ddr_hpm_fsm_en	DDR AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC8

PERI_PMC8 is PMC register 8.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_PMC8	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	mda0_avs_fsm_inc_pwm_step		mda0_avs_fsm_dec_pwm_step		reserved			mda0_avs_hpm_fsm_calc_mode	mda0_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RW	mda0_avs_fsm_inc_pwm_step	Automatic increase step of the MDA0 AVS FSM PWM
[23:16]	RW	mda0_avs_fsm_dec_pwm_step	Automatic decrease step of the MDA0 AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	mda0_avs_hpm_fsm_calc_mode	Calculation mode of the MDA0 AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	mda0_hpm_fsm_en	MDA0 AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC10

PERI_PMC10 is core HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_PMC10	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_srst_req	core_hpm_monitor_en	core_hpm_bypass	core_hpm_en	reserved				core_hpm_offset								reserved		core_hpm_shift		reserved				core_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	core_hpm_srst_req	Core HPM reset request, active high 0: deassert reset 1: reset
[26]	RW	core_hpm_monitor_en	Core HPM cyclic monitoring enable 0: disabled 1: enabled
[25]	RW	core_hpm_bypass	Core HPM cyclic monitoring bypass 0: not bypassed 1: bypassed
[24]	RW	core_hpm_en	Core HPM measurement enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved
[21:12]	RW	core_hpm_offset	Core HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	core_hpm_shift	Core HPM shift
[7:6]	RO	reserved	Reserved
[5:0]	RW	core_hpm_div	Divider of the core HPM reference clock *n*: (*n* + 1) frequency division (*n* must be greater than 0)

PERI_PMC11

PERI_PMC11 is core HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_PMC11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						core_hpm_up_warning	core_hpm_low_warning	reserved				core_hpm_pc_record1								reserved	core_hpm_pc_valid	core_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	core_hpm_up_warning	Upper limit for the core HPM warning
[24]	RO	core_hpm_low_warning	Lower limit for the core HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	core_hpm_pc_record1	Core HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	core_hpm_pc_valid	Core HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	core_hpm_pc_record0	Core HPM original code pattern 0

PERI_PMC12

PERI_PMC12 is core HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_PMC12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_rcc				reserved				core_hpm_pc_record3								reserved				core_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	core_hpm_rcc	Core HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	core_hpm_pc_record3	Core HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	core_hpm_pc_record2	Core HPM original code pattern 2

PERI_PMC13

PERI_PMC13 is core HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_PMC13	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_monitor_period								reserved				core_hpm_lowlimit								reserved				core_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	core_hpm_monitor_period	Core HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved

[21:12]	RW	core_hpm_lowlimit	Core HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	core_hpm_uplimit	Core HPM upper limit

PERI_PMC14

PERI_PMC14 is A17 HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_PMC14	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				a17_hpm_srst_req	a17_hpm_monitor_en	reserved	a17_hpm_en	reserved				a17_hpm_offset								reserved		a17_hpm_shift		reserved				a17_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	a17_hpm_srst_req	A17 HPM reset, active high 0: deassert reset 1: reset
[26]	RW	a17_hpm_monitor_en	A17 HPM cyclic monitoring enable 0: one-time monitoring 1: cyclic monitoring
[25]	RO	reserved	Reserved
[24]	RW	a17_hpm_en	One-time A17 HPM measurement process enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved
[21:12]	RW	a17_hpm_offset	A17 HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	a17_hpm_shift	A17 HPM shift
[7:6]	RW	reserved	Reserved

[5:0]	RW	a17_hpm_div	Frequency division ratio of the A17 HPM clock *n*: (*n* + 1) frequency division (*n* must be greater than 0)

PERI_PMC15

PERI_PMC15 is A17 HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_PMC15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						a17_hpm_up_warning	a17_hpm_low_warning	reserved				a17_hpm_pc_record1								reserved	a17_hpm_pc_valid	a17_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	a17_hpm_up_warning	Upper limit for the A17 HPM warning
[24]	RO	a17_hpm_low_warning	Lower limit for the A17 HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	a17_hpm_pc_record1	A17 HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	a17_hpm_pc_valid	A17 HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	a17_hpm_pc_record0	A17 HPM original code pattern 0

PERI_PMC16

PERI_PMC16 is A17 HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_PMC16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				a17_hpm_rcc				reserved				a17_hpm_pc_record3								reserved				a17_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	a17_hpm_rcc	A17 HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	a17_hpm_pc_record3	A17 HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	a17_hpm_pc_record2	A17 HPM original code pattern 2

PERI_PMC17

PERI_PMC17 is A17 HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0044	PERI_PMC17	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_hpm_monitor_period								reserved				a17_hpm_lowlimit								reserved				a17_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	a17_hpm_monitor_period	A17 HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved

[21:12]	RW	a17_hpm_lowlimit	A17 HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	a17_hpm_uplimit	A17 HPM upper limit

PERI_PMC18

PERI_PMC18 is DDR HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_PMC18	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ddr_hpm_srst_req	ddr_hpm_monitor_en	reserved	ddr_hpm_en	reserved				ddr_hpm_offset								reserved		ddr_hpm_shift		reserved				ddr_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	ddr_hpm_srst_req	DDR HPM reset, active high 0: deassert reset 1: reset
[26]	RW	ddr_hpm_monitor_en	DDR HPM cyclic monitoring enable 0: one-time monitoring 1: cyclic monitoring
[25]	RO	reserved	Reserved
[24]	RW	ddr_hpm_en	One-time DDR HPM measurement process enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved
[21:12]	RW	ddr_hpm_offset	DDR HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	ddr_hpm_shift	DDR HPM shift
[7:6]	RO	reserved	Reserved

[5:0]	RW	ddr_hpm_div	Frequency division ratio of the DDR HPM clock *n*: (*n* + 1) frequency division (*n* must be greater than 0)

PERI_PMC19

PERI_PMC19 is DDR HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x004C	PERI_PMC19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						ddr_hpm_up_warning	ddr_hpm_low_warning	reserved				ddr_hpm_pc_record1								reserved	ddr_hpm_pc_valid	ddr_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	ddr_hpm_up_warning	Upper limit for the DDR HPM warning
[24]	RO	ddr_hpm_low_warning	Lower limit for the DDR HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	ddr_hpm_pc_record1	DDR HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	ddr_hpm_pc_valid	DDR HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	ddr_hpm_pc_record0	DDR HPM original code pattern 0

PERI_PMC20

PERI_PMC20 is DDR HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0050	PERI_PMC20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ddr_hpm_rcc				reserved				ddr_hpm_pc_record3								reserved				ddr_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	ddr_hpm_rcc	DDR HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	ddr_hpm_pc_record3	DDR HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	ddr_hpm_pc_record2	DDR HPM original code pattern 2

PERI_PMC21

PERI_PMC21 is DDR HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0054	PERI_PMC21	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ddr_hpm_monitor_period								reserved				ddr_hpm_lowlimit								reserved				ddr_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ddr_hpm_monitor_period	DDR HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved

[21:12]	RW	ddr_hpm_lowlimit	DDR HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	ddr_hpm_uplimit	DDR HPM upper limit

PERI_PMC22

PERI_PMC22 is MDA0 HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_PMC22	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mda0_hpm_srst_req	mda0_hpm_monitor_en	reserved	mda0_hpm_en	reserved				mda0_hpm_offset								reserved		mda0_hpm_shift		reserved				mda0_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	mda0_hpm_srst_req	MDA0 HPM reset, active high 0: deassert reset 1: reset
[26]	RW	mda0_hpm_monitor_en	MDA0 HPM cyclic monitoring enable 0: one-time monitoring 1: cyclic monitoring
[25]	RO	reserved	Reserved
[24]	RW	mda0_hpm_en	One-time MDA0 HPM measurement process enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved
[21:12]	RW	mda0_hpm_offset	MDA0 HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	mda0_hpm_shift	MDA0 HPM shift
[7:6]	RW	reserved	Reserved

[5:0]	RW	mda0_hpm_div	Frequency division ratio of the MDA0 HPM clock *n*: (*n* + 1) frequency division (*n* must be greater than 0)

PERI_PMC23

PERI_PMC23 is MDA0 HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_PMC23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						mda0_hpm_up_warning	mda0_hpm_low_warning	reserved				mda0_hpm_pc_record1								reserved	mda0_hpm_pc_valid	mda0_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	mda0_hpm_up_warning	Upper limit for the MDA0 HPM warning
[24]	RO	mda0_hpm_low_warning	Lower limit for the MDA0 HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	mda0_hpm_pc_record1	MDA0 HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	mda0_hpm_pc_valid	MDA0 HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	mda0_hpm_pc_record0	MDA0 HPM original code pattern 0

PERI_PMC24

PERI_PMC24 is MDA0 HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_PMC24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mda0_hpm_rcc				reserved				mda0_hpm_pc_record3								reserved				mda0_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	mda0_hpm_rcc	MDA0 HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	mda0_hpm_pc_record3	MDA0 HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	mda0_hpm_pc_record2	MDA0 HPM original code pattern 2

PERI_PMC25

PERI_PMC25 is MDA0 HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_PMC25	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mda0_hpm_monitor_period								reserved				mda0_hpm_lowlimit								reserved				mda0_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	mda0_hpm_monitor_period	MDA0 HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T, in ms) is as follows: T = N x 2048/1000 The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved

[21:12]	RW	mda0_hpm_lowlimit	MDA0 HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	mda0_hpm_uplimit	MDA0 HPM upper limit

PERI_PMC30

PERI_PMC30 is an HPM control register (fine 1).

Offset Address	Register Name	Total Reset Value
0x0078	PERI_PMC30	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_hpm_monitor_period_fine								ddr_hpm_monitor_period_fine								mda0_hpm_monitor_period_fine								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	a17_hpm_monitor_period_fine	Parameter for fine tuning the A17 HPM cyclic monitoring cycle
[23:16]	RW	ddr_hpm_monitor_period_fine	Parameter for fine tuning the DDR HPM cyclic monitoring cycle
[15:8]	RW	mda0_hpm_monitor_period_fine	Parameter for fine tuning the MDA0 HPM cyclic monitoring cycle
[7:0]	RO	reserved	Reserved

PERI_PMC31

PERI_PMC31 is an HPM control register (fine 2).

Offset Address	Register Name	Total Reset Value
0x007C	PERI_PMC31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								core_hpm_monitor_period_fine							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	core_hpm_monitor_period_fine	Parameter for fine tuning the core HPM cyclic monitoring cycle

PERI_PMC68

PERI_PMC68 is PMC register 68.

Offset Address	Register Name	Total Reset Value
0x110	PERI_PMC68	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	tsensor_en	tsensor_monitor_en	reserved	reserved				tsensor_monitor_period								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	tsensor_en	Temperature sensor enable 0: disabled 1: enabled
[29]	RW	tsensor_monitor_en	Cyclic temperature monitoring enable 0: disabled 1: enabled
[28]	RO	reserved	Reserved
[27:24]	RO	reserved	Reserved
[23:16]	RW	tsensor_monitor_period	Cyclic temperature monitoring cycle. The timing reference is 2 ms.
[15:0]	RO	reserved	Reserved

PERI_PMC69

PERI_PMC69 is PMC register 69.

Offset Address	Register Name	Total Reset Value
0x0114	PERI_PMC69	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tsensor_temp_uplimit								reserved								tsensor_temp_lowlimit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	tsensor_temp_uplimit	Temperature overflow value
[15:10]	RO	reserved	Reserved
[9:0]	RW	tsensor_temp_lowlimit	Temperature underflow value

PERI_PMC70

PERI_PMC70 is PMC register 70.

Offset Address	Register Name	Total Reset Value
0x0118	PERI_PMC70	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tsensor_temp_code1								reserved								tsensor_temp_code0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	tsensor_temp_code1	Temperature record value 1
[15:10]	RO	reserved	Reserved
[9:0]	RO	tsensor_temp_code0	Temperature record value 0

PERI_PMC71

PERI_PMC71 is PMC register 71.

Offset Address	Register Name	Total Reset Value
0x011C	PERI_PMC71	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tsensor_temp_code3								reserved								tsensor_temp_code2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	tsensor_temp_code3	Temperature record value 3
[15:10]	RO	reserved	Reserved
[9:0]	RO	tsensor_temp_code2	Temperature record value 2

PERI_PMC72

PERI_PMC72 is PMC register 72.

Offset Address	Register Name	Total Reset Value
0x0120	PERI_PMC72	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tsensor_temp_code5								reserved								tsensor_temp_code4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	tsensor_temp_code5	Temperature record value 5
[15:10]	RO	reserved	Reserved
[9:0]	RO	tsensor_temp_code4	Temperature record value 4

PERI_PMC73

PERI_PMC73 is PMC register 73.

Offset Address	Register Name	Total Reset Value
0x0124	PERI_PMC73	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tsensor_temp_code7		reserved		tsensor_temp_code6	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	tsensor_temp_code7	Temperature record value 7
[15:10]	RO	reserved	Reserved
[9:0]	RO	tsensor_temp_code6	Temperature record value 6

PERI_PMC74

PERI_PMC74 is PMC register 74.

Offset Address	Register Name	Total Reset Value
0x0128	PERI_PMC74	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							tsensor_low_warning, tsensor_up_warning
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	tsensor_low_warning	Temperature underflow alarm 0: No alarm is generated. 1: An alarm is generated.
[0]	RO	tsensor_up_warning	Temperature overflow alarm 0: No alarm is generated. 1: An alarm is generated.

PERI_PMC77

PERI_PMC77 is PMC register 77.

Offset Address	Register Name	Total Reset Value
0x0134	PERI_PMC77	0x011F_EC01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							a17_poweroff_flag	a17_poweron_flag	reserved			a17_mtcmos_overtime							a17_mtcmos_overtime_en	a17_irq_n	a17_fiq_n	a17_standbywfe	a17_standbywfil2	a17_standbywfi	a17_bus_pwrdn_ack_n	a17_bus_pwrdn_req_n_cfg	a17_bus_cactives	a17_bus_cactivem	a17_pwrdn_ack	a17_pwrdn_req_cfg	a17_pwrdn_iso_cfg
Reset	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RO	a17_poweroff_flag	A17 power-off completion flag 0: not complete 1: complete
[23]	RO	a17_poweron_flag	A17 power-on completion flag, active high 0: not complete 1: complete
[22:21]	RO	reserved	Reserved
[20:13]	RW	a17_mtcmos_overtime	Timeout parameter (time unit: 1 μs) Note: This field is valid only when mode_onoff is 2'b0.
[12]	RW	a17_mtcmos_overtime_en	Overtime mechanism enable, active high Note: This field is valid only when mode_onoff is 2'b0.
[11]	RO	a17_irq_n	A17 fast interrupt indicator 0: The interrupt is valid (A17 is powered on in interrupt wakeup mode). 1: The interrupt is invalid.
[10]	RO	a17_fiq_n	A17 common interrupt indicator 0: The interrupt is valid (A17 is powered on in interrupt wakeup mode). 1: The interrupt is invalid.

[9]	RO	a17_standbywfe	A17 core WFE indicator 0: The WFE is invalid. 1: The WFE is valid.
[8]	RO	a17_standbywfil2	A17 non-CPU WFI indicator 0: The WFI is invalid. 1: The WFI is valid.
[7]	RO	a17_standbywfi	A17 core WFI indicator 0: The WFI is invalid. 1: The WFI is valid.
[6]	RO	a17_bus_pwrdn_ack_n	A17_CPU_SUBSYS bus power-off handshake indicator 0: The power-off request is complete. 1: The power-on request is complete.
[5]	RW	a17_bus_pwrdn_req_n_cfg	A17_CPU_SUBSYS bus power-off handshake control signal 0: power-off request 1: power-on request
[4]	RO	a17_bus_cactives	A17 async bridge activity status indicator (slave end) 0: The async bridge is idle. 1: The async bridge is busy.
[3]	RO	a17_bus_cactivem	A17 async bridge activity status indicator (master end) 0: The async bridge is idle. 1: The async bridge is busy.
[2]	RO	a17_pwrdn_ack	A17 power supply status 0: powered off 1: powered on
[1]	RW	a17_pwrdn_req_cfg	A17 power-off request 0: powered off 1: powered on
[0]	RW	a17_pwrdn_iso_cfg	A17 signal isolation control. The A17 signal must be isolated before power-off, and the bus must be idle when isolation is enabled. 0: not isolated 1: isolated

PERI_PMC78

PERI_PMC78 is PMC register 78.

Offset Address	Register Name	Total Reset Value
0x0138	PERI_PMC78	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			cci_arch_clkgate_enable	use_cs_pr	lp_mode_en	wfi_ret_en	pgen_pulse_width	pgenf2retnr_timing	retnf2pgenr_timing	a17_l2_ram_lp_mode					cci_sf_ram_lp_mode_update			cci_sf_ram_lp_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	cci_arch_clkgate_enable	CCI arch automatic gating 0: disabled 1: enabled
[11]	RW	use_cs_pr	CoreSight power requestor component switch 0: disabled 1: enabled
[10]	RW	lp_mode_en	A17 L2 retention low-power mode enable 0: disabled 1: enabled
[9]	RW	wfi_ret_en	A17 Wi-Fi signal trigger low-power mode enable switch 0: disabled 1: enabled
[8]	RW	pgen_pulse_width	pgen signal broadening control 0: no increase 1: increase by two cycles
[7]	RW	pgenf2retnr_timing	Broadening control for the time interval between the falling edge of the pgen signal to the rising edge of the ret1n signal 0: no increase 1: increase by two cycles

[6]	RW	retnf2pgenr_timing	Broadening control for the time interval between the falling edge of the ret1n signal to the rising edge of the pgen signal 0: no increase 1: increase by two cycles
[5:4]	RW	a17_l2_ram_lp_mode	Low-power mode select for the A17 L2 RAM 00: normal mode 01: pre-charge mode 10: reserved 11: ret mode
[3]	RW	cci_sf_ram_lp_mode_update	cci_sf_ram_lp_mode update enable 0: The configuration of cci_sf_ram_lp_mode is not updated to the logic 1: The configuration of cci_sf_ram_lp_mode is updated to the logic
[2:0]	RW	cci_sf_ram_lp_mode	Low-power mode select for the CCI snoop filter RAM 00: The CCI snoop filter RAM retains the normal operating status. 01: The CCI snoop filter RAM is allowed to dynamically enter the retention mode. 1x: The CCI snoop filter RAM is powered off. Note: The configuration of this field is updated to the logic only when cci_sf_ram_lp_mode_update is 1.

PERI_PMC79

PERI_PMC79 is PMC register 79.

Offset Address	Register Name	Total Reset Value
0x013C	PERI_PMC79	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								a17_pon_rstime								reserved								a17_ac_inactive	irq_poweron_en	fiq_poweron_en	trigger_mode	power_off_en	power_on_en	fsm_step	mode_onoff				
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:16]	RW	a17_pon_rstime	Global reset duration cycles during the power-on process (unit: 20 ns)
[15:9]	RO	reserved	Reserved
[8]	RW	a17_ac_inactive	Disable control signal for the AC channel of the A17 ACE bus 0: The AC channel is not masked. 1: The AC channel is masked.
[7]	RW	irq_poweron_en	A17 power-on enable triggered by the interrupt request (IRQ), valid only when trigger_mode is 1 and mode_onoff is 0 0: disabled 1: enabled
[6]	RW	fiq_poweron_en	A17 power-on enable triggered by the fast interrupt request (FIQ), valid only when trigger_mode is 1 and mode_onoff is 0 0: disabled 1: enabled
[5]	RW	trigger_mode	Power-on trigger mode select in automatic logic mode 1: interrupt-triggered power-on 0: non-interrupt-triggered power-on
[4]	RW	power_off_en	A17 power-off enable. A17 is powered off when the level is changed from low to high (valid only when mode_onoff is 0).
[3]	RW	power_on_en	A17 power-on enable. A17 is powered on when the level is changed from low to high (valid only when trigger_mode and mode_onoff are 0).
[2]	RW	fsm_step	Next operation control in single-step logic mode. The next operation is triggered when the level is changed from low to high.
[1:0]	RW	mode_onoff	A17 power-on/power-off control mode 00: automatic logic mode 01: single-step logic mode 1X: manual software mode

PERI_PMC80

PERI_PMC80 is PMC register 80.

Offset Address	Register Name	Total Reset Value
0x0140	PERI_PMC80	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_on_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	a17_power_on_cnt	Number of A17 power-on times

PERI_PMC81

PERI_PMC81 is PMC register 81.

Offset Address	Register Name	Total Reset Value
0x0144	PERI_PMC81	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_off_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	a17_power_off_cnt	Number of A17 power-off times

PERI_PMC82

PERI_PMC82 is PMC register 82.

Offset Address	Register Name	Total Reset Value
0x0148	PERI_PMC82	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_on_time_max																a17_power_on_time_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	a17_power_on_time_max	Maximum time consumption of A17 power-on (unit: 5 µs)
[15:0]	RO	a17_power_on_time_min	Minimum time consumption of A17 power-on (unit: 5 µs)

PERI_PMC83

PERI_PMC83 is PMC register 83.

Offset Address	Register Name	Total Reset Value
0x014C	PERI_PMC83	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																a17_power_on_time_now															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	a17_power_on_time_now	Time consumption of the current A17 power-on operation (unit: 5 µs)

PERI_PMC84

PERI_PMC84 is PMC register 84.

Offset Address	Register Name	Total Reset Value
0x0150	PERI_PMC84	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_on_time_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	a17_power_on_time_sum	Accumulated time consumption of A17 power-on (unit: 5 µs)

PERI_PMC85

PERI_PMC85 is PMC register 85.

Offset Address	Register Name	Total Reset Value
0x0154	PERI_PMC85	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															stop_a17_poweron_time_cnt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	stop_a17_poweron_time_cnt	Enable for terminating the counting of A17 power-on time consumption. The configuration takes effect only after 0 and 1 are written to this field in sequence.

PERI_PMC86

PERI_PMC86 is PMC register 86.

Offset Address	Register Name	Total Reset Value
0x0158	PERI_PMC86	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_off_time_max																a17_power_off_time_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	a17_power_off_time_max	Maximum time consumption of A17 power-off (unit: 5 µs)
[15:0]	RO	a17_power_off_time_min	Minimum time consumption of A17 power-off (unit: 5 µs)

PERI_PMC87

PERI_PMC87 is PMC register 87.

Offset Address	Register Name	Total Reset Value
0x015C	PERI_PMC87	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																a17_power_off_time_now															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	a17_power_off_time_now	Time consumption of the current A17 power-off operation (unit: 5 µs)

PERI_PMC88

PERI_PMC88 is PMC register 88.

Offset Address	Register Name	Total Reset Value
0x0160	PERI_PMC88	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	a17_power_off_time_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	a17_power_off_time_sum	Accumulated time consumption of A17 power-off (unit: 5 µs)

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4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR synchronous dynamic random access memory (SDRAM) controller (DDRC) controls access to the DDR3/DDR4 SDRAM.

4.1.2 Features

The DDRC has the following features:

- Single channel that provides space only for one chip select (CS). The width of the DDR SDRAM data bus corresponding to the channel is 32 bits. That is, the maximum width of the DDR SDRAM is 32 bits. The 16-bit DDR SDRAM can also be connected. However, only the lower two bytes can be used.
- Maximum 2 GB storage space
- 800 MHz DDR3/DDR4 SDRAM bus working frequency (933 MHz when the chip working voltage increases) and 1600 Mbit/s data rate (1866 Mbit/s when the chip working voltage increases)
- Various DDR SDRAM low-power modes, such as the power-down and self-refresh modes
- Support for the INCR and wrap commands but not the fixed command in burst8 transfer mode of the DDR SDRAM

4.1.3 Function Description

4.1.3.1 Application Block Diagram

The DDRC enables the master devices of the SoC such as the CPU to access the external DDR3/DDR4 SDRAM. It supports the DDR3/DDR4 SDRAM that complies with the JEDEC standard after the timing parameter registers of the DDRC are configured by using the CPU. Table 4-1 lists the mainstream DDR3/DDR4 SDRAMs supported by the DDRC. The descriptions in Table 4-1 are based on the working frequencies of DDR3/DDR4 SDRAMs. The restrictions such as the capacity are not taken into account.

Table 4-1 DDR3/DDR4 SDRAMs supported by the DDRC

Vendor	800 MHz	933 MHz
Samsung	DDR4-1866 DDR3-1866 DDR3-2133 DDR3-1600 DDR4-1600 DDR4-2133	DDR4-1866 DDR3-1866 DDR3-2133 DDR4-2133
lanya	DDR3-1600 DDR3-1866 DDR3-2133 DDR4-1600 DDR4-1866 DDR4-2133	DDR3-1866 DDR3-2133 DDR4-1866 DDR4-2133
Hynix	DDR3-1600 DDR3-1866 DDR3-2133 DDR4-1600 DDR4-1866 DDR4-2133	DDR3-1866 DDR3-2133 DDR4-1866 DDR4-2133

NOTE

For details about the supported component types, see the JEDEC standard and the component data sheet.

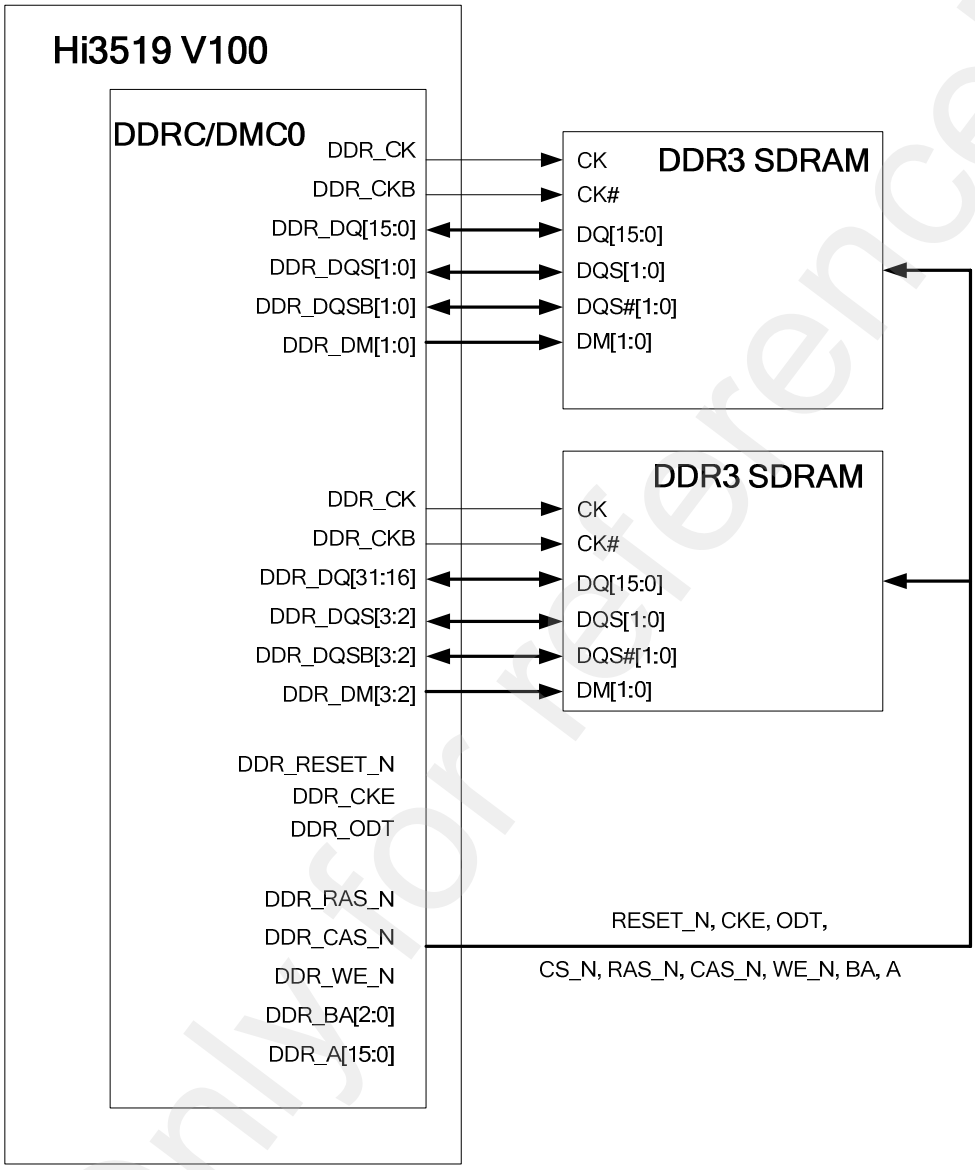
In single-channel mode, the DDRC channel supports the 32-bit interconnection mode.

NOTE

Figure 4-1 and Figure 4-2 show the connection mode of DDR3 SDRAMs. For details about the connection mode of DDR4 SDRAMs, see the swap solution.

Figure 4-1 shows the connection between the DDRC channel and two 16-bit DDR3 SDRAMs.

Figure 4-1 Connection between the DDRC channel and two 16-bit DDR3 SDRAMs

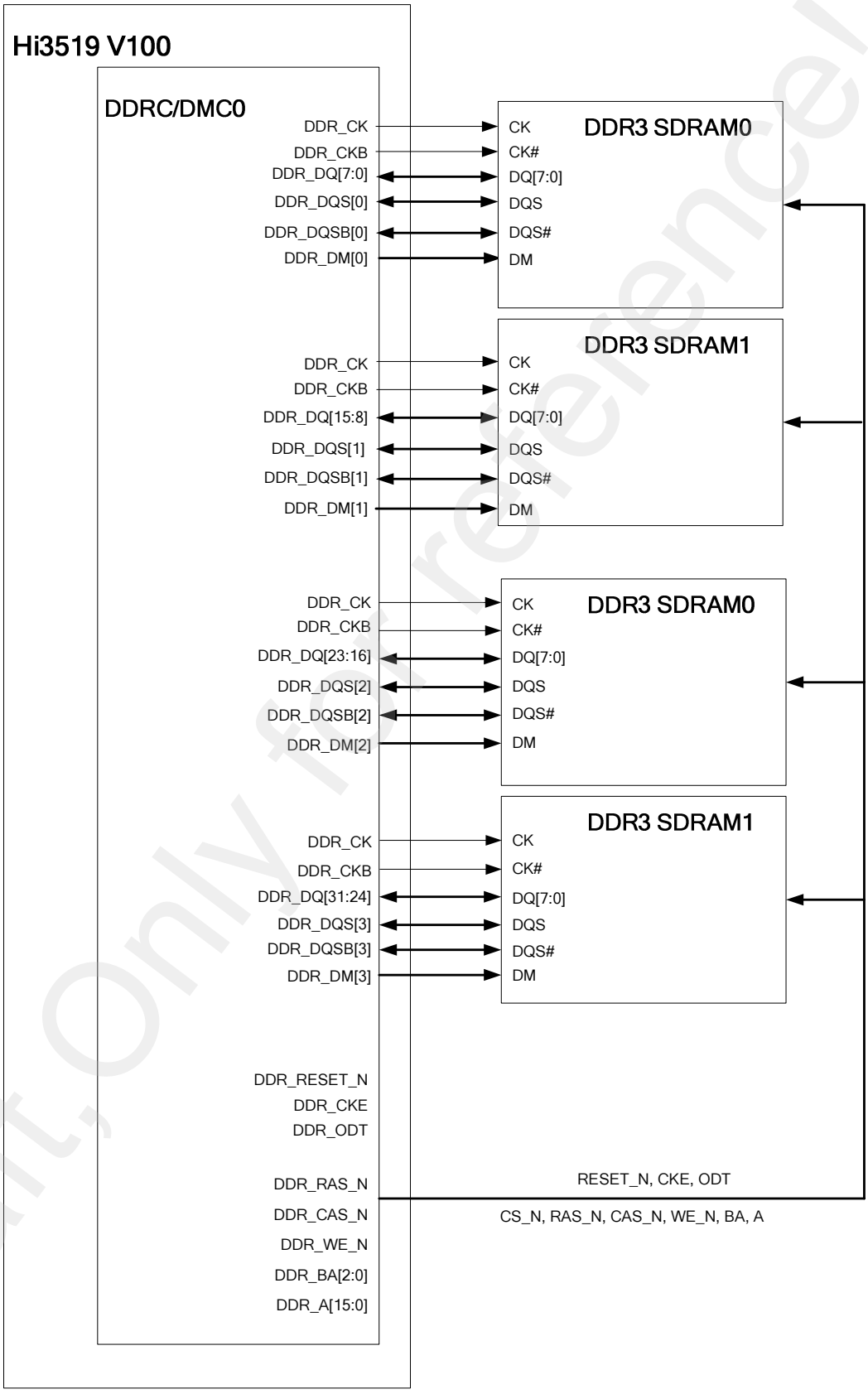


NOTE

The channel connects to two 16-bit DDR3 SDRAMs. The DDRC/DMC0 command control signals (DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[15:0], and DDR_ODT) connect to the command control signals of the DDR3 SDRAM*x* respectively. The DDRC command control bus uses the one-drive-two connection mode.

Figure 4-2 shows the connection between the DDRC channel and four 8-bit DDR3 SDRAMs.

Figure 4-2 Connection between the DDRC channel and four 8-bit DDR3 SDRAMs



NOTE

The DDRC connects to four 8-bit DDR3 SDRAMs. The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], and DDR_A[15:0]) connect to the command control signals of the DDR3 SDRAM*x* respectively. The command control bus of the DDRC uses the one-drive-four connection mode.

4.1.3.2 Function Implementation

As the timings of the DDRC interface comply with the JESD standard, the DDRC can access (read or write) data in the DDR3/DDR4 SDRAM and control the status of the DDR3/DDR4 SDRAM (including automatic refresh and low power control) by sending the command words of the DDR3 SDRAM.

Command Truth Value Table

The DDRC can read and write to the DDR3/DDR4 SDRAM and control command words. Table 4-2 lists the command truth values of the DDRC. For details, see the JEDEC standard and component data sheet.

Table 4-2 Command truth values of the DDR3

Function	DDR3_CKE	DDR3_CSN	DDR3_RASN	DDR3_CASN	DDR3_WEN	DDR3_ADR			DDR3_BA
						15:11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	V	L	V	BA
PRECHARGE ALL	H	L	L	H	L	V	H	V	V
AUTO REFRESH	H	L	L	L	H	V	V	V	V
SELF REFRESH ENTRY	H->L	L	L	L	H	V	V	V	V
SELF REFRESH EXIT	L->H	L	H	H	H	V	V	V	V
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

H: high level; L: low level; V: valid; X: ignored.

ZQ calibration long (ZQCL): starts ZQ calibration on the DDR3 SDRAM when it is initialized during power-on.

ZQ calibration short (ZQCS): starts ZQ calibration on the DDR3 SDRAM when its ambient environment is changed.

The DDRC can read and write to the DDR4 SDRAM and control command words. Table 4-3 lists the command truth values of the DDRC. For details, see the JEDEC standard and component data sheet.

Table 4-3 Command truth values of the DDR4

FUNCTION	DDR4_CKE	DDR4_CSN	DDR4_ACTN	DDR4_RASN/A DR16	DDR4_CASN/A DR15	DDR4_WEN/A DR14	DDR4_ADR			DDR4_BG	DDR4_BA
							13:11	AP(10)	9:0		
DESELECT	H	H		X	X	X	X	X	X	X	X
ACTIVE	H	L	L	Row address			V	V	V	BG	BA
READ	H	L	H	H	L	H	V	V	V	BG	BA
WRITE	H	L	H	H	L	L	V	V	V	BG	BA
PRECHARGE	H	L	H	L	H	L	V	L	V	BG	BA
PRECHARGE ALL	H	L	H	L	H	L	V	H	V	V	V
AUTO REFRESH	H	L	H	L	L	H	V	V	V	V	V
SELF REFRESH ENTRY	H->L	L	H	L	L	H	V	V	V	V	V
SELF REFRESH EXIT	L->H	L	H	H	H	H	V	V	V	V	V
MODE REGISTER SET	H	L	H	L	L	L	V	V	V	V	V
ZQCL	H	L	H	H	H	L	V	H	V	V	V
ZQCS	H	L	H	H	H	L	V	L	V	V	V

H: high level; L: low level; V: valid; X: ignored.

ZQ calibration long (ZQCL): starts ZQ calibration on the DDR4 SDRAM when it is initialized during power-on.

ZQ calibration short (ZQCS): starts ZQ calibration on the DDR4 SDRAM when its ambient environment is changed.

Auto Refresh

When DDRC_CFG_TIMING2[taref] is set to a non-zero value, the DDRC refreshes the DDR3/DDR4 SDRAM by automatically generating a periodical auto refresh command. At ambient temperature, the DDR3/DDR4 SDRAM is required to implement 8,192 auto-refresh

operations within 64 ms. That is, the auto-refresh cycle is 7.8 μs (for details about the actual value, see the corresponding component manual). The relationship between the value of DDRC_CFG_TIMING2[taref] (taref) and the auto-refresh cycle T (T = 7.8 μs) is as follows:

T ≥ taref x (16 x DDR clock cycle)

When DDRC_CFG_TIMING2[taref] is configured, the internal counter of the DDRC automatically loads the taref value and then counts in decremented mode. When the count value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two modes of low-power management: common low-power mode and auto-refresh low-power mode.

When DDRC_CFG_PD[pd_en] is set to 1 to enable the SDRAM low-power mode, and the system is idle (the DDR is not read or written through the DDRC bus interface for a period), the DDR3/DDR4 SDRAM enters the common low-power mode automatically.

To switch the system mode to standby mode, you can force the DDR3/DDR4 SDRAM to enter the auto-refresh mode by setting DDRC_CTRL_SREF[sref_req] to 1. In this mode, the power consumption of the DDR3/DDR4 SDRAM is minimized, data in the DDR3/DDR4 SDRAM is retained, but the system cannot access the DDR3/DDR4 SDRAM.

Arbitration Mechanism

The DDRC schedules commands by using the priority scheduling algorithms. In addition, the DDRC can control the command requests by using traffic control and timeout control. The two auxiliary scheduling methods can be enabled separately or simultaneously as required.

1. Priority scheduling

Eight priorities (0−7) are provided. The priority of each advanced eXtensible interface (AXI) is configured separately as follows:

Step 1 Select the priority mapping mode by configuring AXI_QOS_MAP[pri_map_mode]. If AXI_QOS_MAP[pri_map_mode] is set to 1, the index is obtained by using the system bus associated signal of the command; if AXI_QOS_MAP[pri_map_mode] is set to 0, AXI_QOS_MAP[id_map_idx] needs to be configured to select any three bits in the command ID to obtain the index.

Step 2 Configure AXI_QOS_WRPRIn and AXI_QOS_RDPRIn.

Step 3 The DDRC queries a value from the eight preset values in AXI_QOS_WRPRIn or AXI_QOS_RDPRIn based on the priority index corresponding to each command, and adds this value to the read/write command sent to the bus as the priority attribute of the command. Then the DDRC internal arbiter schedules the commands that raise arbitration requests based on the priority attributes to implement highly effective access to the DDR3 SDRAM.

----End

- Priority adaptation is supported. The priority adaptation function of each port can be enabled by configuring AXI_QOS_ADPTn to ensure that commands with lower priorities will be arbitrated by level. The priority of a command is automatically

increased to a higher level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one. The priority increase cycle is (adpt_prd x 16).

- The read and write commands from the same port are aggregated and arbitrated according to either of the following two rules:
  - The commands are arbitrated based on the arrival time. When the read and write commands are sent, the ones from the same port that arrive earlier are arbitrated first. When commands from two ports arrive simultaneously, the read commands are arbitrated before the write commands.
  - The commands are arbitrated based on the priorities.

    When the commands are of different priorities, the commands from the port with the highest arbitration priority are arbitrated first.

    When the commands are of the same priority, the commands from the port that has not been arbitrated for the longest time are arbitrated first.

2. Traffic control

The traffic is controlled by configuring QOSB_FLUX_EN[flux_en] and grouping the traffic according to the command ID as required. The DDRC allocates each group of traffic to ensure the bandwidth of each port when the traffic is heavy.

3. Timeout control

The mapping mode for the timeout attribute of the command is selected by configuring QOSB_TIMEOUT_MODE[timeout_mode], which is similar to the priority mapping mode. In configured mapping mode, the QoSBuf module in the DDRC queries a value from the 16 preset timeout values based on the timeout index corresponding to each command (the value 0 indicates that the timeout function is disabled), and adds this value to the command as the timeout value of the command. In the DDRC, commands with timeout attributes forcibly prevent commands without timeout attributes from raising arbitration requests and immediately raise arbitration requests when the waiting time elapses.

Traffic Statistics and Command Latency Statistics

The DDRC supports traffic statistics. The interface read and write traffic statistics can be collected to determine whether dynamic frequency scaling (DFS) is required, that is, whether to increase or reduce the DDRC frequency. The DDRC can collect the read and write traffic statistics of a specific ID, or the overall read and write traffic statistics. The DDRC can also collect DDR interface usage statistics. The statistic counter supports the continuous counts and one-time count. When counting continuously, the counter is a non-saturating counter, and it is wrapped when the maximum count is reached to facilitate the continuous count. Therefore, the system needs to read the count value before the counter is wrapped. When counting for only one time, the counter stops counting when the statistic time elapses. The system can obtain the instantaneous traffic and latency by using this function.

The DDRC can collect command latency statistics, including the maximum latency of the read and write access to a specific ID and the accumulative latency statistics.

The process for collecting statistics is as follows:

Step 1 Set the statistic mode to continuous triggering or one-time triggering by configuring DDRC_CFG_PERF[perf_mode]. If the one-time triggering is selected, set the perf_prd field to configure the statistic cycle.

Step 2 Set the ID for which statistics are to be collected by configuring DDRC_CFG_STAID.

Step 3 Set the mask value of the ID by configuring DDRC_CFG_STAIDMSK. The DDRC determines whether to collect statistics of the current access based on sta_idmask and the accessed ID. Statistics of multiple IDs can be collected by using this method.

Step 4 Enable the statistic function by configuring DDRC_CTRL_PERF[perf_en]. For the one-time count, counting is complete when DDRC_CTRL_PERF[perf_en] restores to 0. For the continuous count, the software needs to write 0 to DDRC_CTRL_PERF[perf_en] to stop counting.

Step 5 Observe the collected statistics by using DDRC_HIS_FLUX_WR, DDRC_HIS_FLUX_RD, DDRC_HIS_FLUX_WCMD, DDRC_HIS_FLUX_RCMD, DDRC_HIS_FLUXID_WR, DDRC_HIS_FLUXID_RD, DDRC_HIS_FLUXID_WCMD, DDRC_HIS_FLUXID_RCMD, DDRC_HIS_WLATCNT0, DDRC_HIS_WLATCNT1, DDRC_HIS_RLATCNT0, DDRC_HIS_RLATCNT1, and DDRC_HIS_INHERE_RLAT_CNT.

----End

Address Mapping

The DDRC can convert the access address of the system bus into that of the DDR SDRAM. The four mapping modes RRBC (Rank_row_bank_col), RRBC (Row_rank_bank_col), RRCBC (Rank_row_col_bank_col), and RRCBC (Row_rank_col_bank_col) can be implemented by configuring AXI_REGION_ATTRIB. The bit widths of the row address and column address and the DDR SDRAM can be set by configuring DDRC_CFG_RNKVOL[mem_row] and DDRC_CFG_RNKVOL[mem_col]. The DDRC converts the system bus address into the address of the DDR SDRAM based on the address mapping algorithm.

The following describes the mapping algorithm for the system bus address and DDR SDRAM address by using the RRCBC (Rank_row_col_bank_col) mode as an example. Assume that the system bus address is BUSADR[31:0], the valid address is BUSADR[m – 1:0], and the address for the DDR3 SDRAM is DDRADR[15:0]. When DDRADR[15:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when DDRADR[15:0] serves as the column address, its valid address is DDRCOL[y – 1:0]. In addition, the bank address for the DDR SDRAM is DDRBA[z – 1:0] and the width of the storage data bus of the DDRC is DW. In this case, the value of AXI_REGION_ATTRIB[ch_mode] is 2'b01 (the case when the value of AXI_REGION_ATTRIB[ch_mode] is 2'b11 is not discussed here), and the address mapping relationship is as follows:

The bank interleaving granularity is selected by configuring AXI_REGION_ATTRIB[bnk_mod]. If this field is set to 3b101 (when the 32-bit components are connected), the interleaving granularity is 256 bytes.

BUSADR[m − 1:0] = {DDRROW[x − 1:0], DDRCOL[y − 1:6], DDRBA[z − 1:0], DDRCOL[5:0], 2{b0}}

Table 4-4 and Table 4-5 describe the address mapping modes of the DDR3 SDRAM and DDR4 SDRAM respectively.

Table 4-4 DDRC DDR3 address mapping in 32-bit mode

Memory Type			DDR BA				DDR ADR									
Mbit x bw	Row Address Width	Column Address Width	2	1	0	Row Address or Column Address	14	13	12	11	10 / AP	9	8	7	6	[5:0]
512 Mbits; 8 banks															-	-
32 x 16	12	10	10	9	8	Row	-	-	-	26	25	24	23	22	21	[20:15]
						Col	-	-	-	-	AP	14	13	12	11	[7:2]
1024 Mbits; 8 banks															-	-
64 x 16	13	10	10	9	8	Row	-	-	27	26	24	24	23	22	21	[20:15]
						Col	-	-	-	-	AP	14	13	12	11	[7:2]
2048 Mbits; 8 banks															-	-
128 x 16	13	10	10	9	8	Row	-	28	27	26	25	24	23	22	21	[20:15]
						Col	-	-	-	-	AP	14	13	12	11	[7:2]
4096 Mbits; 8 banks															-	-
256 x 16	14	10	10	9	8	Row	29	28	27	26	25	24	23	22	21	[20:15]
						Col	-	-	-	-	AP	14	13	12	11	[7:2]

Table 4-5 DDRC DDR4 address mapping in 32-bit mode (BG NUM = 2)

Memory Type		Column Address Width	BA		BG	Row Address or Column Address	DDR ADR									
Mbit x bw	Row Address Width		1	0	0		15	14	13	12	11	10/AP	9	8	7	6	[5:0]
2048 Mbits; 8 banks; 4 bank groups																	
128 x 16	14	10	10	9	8	Row	-	-	28	27	26	25	24	23	22	21	[20:15]
						Col	-	-	-	-	-	AP	1	13	1	1	[7:2]

Memory Type	Row Address Width	Column Address Width	BA		BG	Row Address or Column Address	DDR ADR											
Mbit x bw			1	0	0		15	14	13	12	11	10/AP	9	8	7	6	[5:0]	
												4			2	1		
4096 Mbits; 8 banks; 4 bank groups																		
256 x 16	15	10	10	9	8	Row	-	29	28	27	26	25	24	23	22	21	[20:15]	
						Col	-	-	-	-	-	AP	14	13	12	11	[7:2]	
8192 Mbits; 8 banks; 4 bank groups																		
512 x 16	16	10	10	9	8	Row	30	29	28	27	26	25	24	23	22	21	[25:15]	
						Col	-	-	-	-	-	AP	14	13	12	11	[7:2]	

4.1.4 Operating Mode

4.1.4.1 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDR3/DDR4 SDRAM must be reinitialized according to the following initialization processes.

4.1.4.2 Initializing the DDR SDRAM

After power-on, the system can access the DDR SDRAM only when the DDR SDRAM is initialized. Before initializing the DDR SDRAM, note the following:

- Power on the DDR SDRAM by following the JEDEC standard.
- Initialize the DDR SDRAM after the system runs in normal mode.

The total capacity of DDR SDRAM connected to the DDRC is 8 Gbits. The DDR SDRAMs can be two 16-bit DDR SDRAMs (4 Gbits each) or four 8-bit DDR SDRAM (2 Gbits each). The following describes the procedure for initializing the DDR subsystem when the ratio of the working frequency of the DDRC to that of the DDR3/DDR4 SDRAM is 1:2:

Step 1 Set the DDRC_CFG_SREF register of DMC0 to 0x0 to exit the self-refresh mode.

Step 2 Query the DDRC_CURR_FUNC register of DMC0 by using software. If bit[0] of this register is 1'b0, go to step 3.

Step 3 Configure the operating mode, clock frequency, and timing parameters of DMC0. The related registers involve DDRC_CFG_WORKMODE, DDRC_CFG_RNKVOL, DDRC_CFG_TIMING0, DDRC_CFG_TIMING1, DDRC_CFG_TIMING2, DDRC_CFG_TIMING3, DDRC_CFG_TIMI

NG4, DDRC_CFG_TIMING5, DDRC_CFG_TIMING6, DDRC_CFG_PD, DDRC_CFG_DDRPHY, DDRC_CFG_ODT.

Step 4 Configure the DDRC_CFG_DDRMODE register of DMC0 to select the external DDR type.

Step 5 Configure the operating mode and time parameters of each DDR PHY connected to DMC0 respectively, DDR PHY I/O drive, ODT impedance, and the delay parameter for the read and write command channels. The related registers involve PHYTIMER0, PHYTIMER1, PLLTIMER, DLYMEASCTRL, DRAMCFG, ACPHYCTL4, DRAMTIMER0, DRAMTIMER1, DRAMTIMER2, DRAMTIMER3, DRAMTIMER4, DRAMTIMER5, IOCTL (Static_reg), MISC, MODEREG01, MODEREG23, MODEREG45, MODEREG67, PHYCTRL0, ACPHYBOUND.

Step 6 Configure the RNK2RNK, DMSEL, and DQSSEL (Static_reg) register of DDR PHY0 to select the swap modes of the ADDR/CMD signal and DQ/DQS signal.

Step 7 Configure the PHYINITCTRL register of each DDR PHY connected to DMC0 to initialize DDRPHY0.

Step 8 Wait until the PHYINITCTRL of DDRPHY0 is 0. That is, the initialization of DDRPHY0 is complete.

Step 9 Configure DDRC_CFG_TIMING2 bit[10:0] of DMC0 to enable the auto-refresh command transmit function.

Step 10 Configure the AXI_REGION_MAP register of AXI to configure the DDR address area mapping.

Step 11 Configure the AXI_REGION_ATTRIB register of AXI to configure the DDR address area attribute.

Step 12 Set the DMC0 register DDRC_CFG_SREF to 0x2 to deassert back pressure.

----End

After the preceding steps are complete, the DDR3/DDR4 DRAM works properly.

NOTE

The register values may vary according to the DDR type, but the procedure is the same.

4.1.5 AXI Registers of the DDRC

4.1.5.1 Register Summary

Table 4-6 describes AXI registers.

Table 4-6 Summary of AXI registers (base address: 0x1206_0000)

Offset Address	Register	Description	Page
0x004	AXI_CFG_LOCK	Lock control register	4-14
0x008	AXI_CKG	Module clock gating register	4-14
0x020	AXI_ACTION	AXI operating mode register	4-15
0x100 + 0x10 x *regions*	AXI_REGION_MAP	Address area mapping register	4-16

Offset Address	Register	Description	Page
0x104 + 0x10 x *regions*	AXI_REGION_ATTRIB	Address area attribute register	4-17
0x108 + 0x10 x *regions*	AXI_REGION_SCRMBL	Address scrambling code mode register for address areas	4-20
0x200 + 0x10 x *ports*	AXI_QOS_MAP	Command priority mapping mode register	4-21
0x204 + 0x10 x *ports*	AXI_QOS_WRPRIn	Write command priority mapping table register	4-23
0x208 + 0x10 x *ports*	AXI_QOS_RDPRIn	Read command priority mapping table register	4-25
0x20C + 0x10 x *ports*	AXI_QOS_ADPTn	Priority adaptation cycle mapping table register	4-26
0x300 + 0x10 x *ports*	AXI_OSTD_PRTn	Port command outstanding (OSTD) restriction register	4-28
0x304 + 0x10 x *ports*	AXI_OSTD_PRT_STn	Port command OSTD statistics register0}	4-29
0x400 + 0x10 x *groups*	AXI_OSTD_GROUPn	Command OSTD register for the port group	4-29
0x404 + 0x10 x *groups*	AXI_OSTD_PRIn0	Priority-based port group command OSTD restriction register 0	4-30
0x408 + 0x10 x *groups*	AXI_OSTD_PRIn1	Priority-based port group command OSTD restriction register 1	4-31
0x40C + 0x10 x *groups*	AXI_OSTD_GROUP_STn	Command OSTD statistics register for the port group	4-33
0x600	AXI_STATUS	Port operating mode register	4-33
0x610	AXI_INT_STATUS	Interrupt status register	4-34

Table 4-7 describes the value ranges and meanings of variables in the offset addresses for AXI registers.

Table 4-7 Variables in the offset addresses for AXI registers

Variable	Value Range	Description
regions	0–16	Number of address areas
ports	0–8	Number of AXI ports
groups	0–4	Number of groups for the port command OSTD statistics

4.1.5.2 Register Description

AXI_CFG_LOCK

AXI_CFG_LOCK is a lock control register.

Offset Address	Register Name	Total Reset Value
0x004	AXI_CFG_LOCK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								apb_cfg_lock
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	apb_cfg_lock	Lock control of all the register configuration modules (AXI_IF/SEC/DMC/PUB) in the MDDRC 0: unlocked 1: locked (None of the AXI_IF configuration registers can be accessed except this register. Therefore, the power consumption is reduced.)

AXI_CKG

AXI_CKG is a module clock gating register.

Offset Address	Register Name	Total Reset Value
0x008	AXI_CKG	0x000F_1FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			sta_ckg_dmc	reserved	dyn_ckg_rdr	dyn_ckg_axi	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19:16]	RW	sta_ckg_dmc	Static clock gating for each DMC When sta_ckg_dmc[n] is 0, the clocks for the DMC*n* and the corresponding PHY utility block (PUB) are disabled. When sta_ckg_dmc[n] is 1, the clocks for the DMC*n* and the corresponding PUB are enabled. *n* = 2 or 3: reserved
[15:13]	RO	reserved	Reserved
[12]	RW	dyn_ckg_rdr	Dynamic clock gating for the reorder module 0: The clock is always enabled. 1: The clock is automatically disabled when the module is idle.
[11:0]	RW	dyn_ckg_axi	Dynamic clock gating for each AXI port When dyn_ckg_axi[n] is 0, the clock for AXI port *n* is always enabled. When dyn_ckg_axi[n] is 1, the clock is automatically disabled when modules in AXI port *n* are idle.

AXI_ACTION

AXI_ACTION is an AXI operating mode register.

Offset Address	Register Name	Total Reset Value
0x020	AXI_ACTION	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wr_rcv_mode								reserved										rd_wrap_split_en	exclusive_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19:8]	RW	wr_rcv_mode	Anti-deadlock mode enable When wr_rcv_mode[n] is 0, the anti-deadlock mode for port *n* is disabled. When wr_rcv_mode[n] is 1, the anti-deadlock mode for port *n* is enabled. **NOTE** • Whether to enable the anti-deadlock mode depends on bus architecture requirements • When the anti-deadlock mode is enabled, the OSTD of the write command is restricted to 1.
[7:2]	RO	reserved	Reserved
[1]	RW	rd_wrap_split_en	Wrap read command split enable 0: no split. The address is wrapped by the DMC. 1: split
[0]	RW	exclusive_en	Exclusive command enable 0: disabled 1: enabled

AXI_REGION_MAP

AXI_REGION_MAP is an address area mapping register.

Offset Address: 0x100 + 0x10 x *regions* (*regions* = 0−15)

Register Name: AXI_REGION_MAP

Total Reset Value: 0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					rgn_en / reserved / rgn_size	rgn_base_addr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rgn_en	Current address area enable 0: disabled 1: enabled
[11]	RO	reserved	Reserved

[10:8]	RW	rgn_size	Size of the current address area 0x0: 16 MB 0x1: 32 MB. In this case, rgn_base_addr/ch_offset[0] must be set to 0. 0x2: 64 MB. In this case, rgn_base_addr/ch_offset[1:0] must be set to 0. 0x3: 128 MB. In this case, rgn_base_addr/ ch _offset[2:0] must be set to 0. 0x4: 256 MB. In this case, rgn_base_addr/ ch _offset[3:0] must be set to 0. 0x5: 512 MB. In this case, rgn_base_addr/ ch _offset[4:0] must be set to 0. 0x6: 1 GB. In this case, rgn_base_addr/ ch _offset[5:0] must be set to 0. 0x7: 2 GB. In this case, rgn_base_addr/ ch _offset[6:0] must be set to 0. NOTE • The preceding configuration is valid when the address bit width is 32 bits. The meaning of the configured value varies according to the address bit width. For example, when the address bit width is 40 bits, if this field is set to 0x3, the size of the current address area is 32 GB. In this case, rgn_base_addr[2:0] must be set to 0. • When the address mapping mode is the dual-channel-interleaved mode, rgn_size cannot be set to 0. When the addresses of four channels are interleaved, rgn_size cannot be set to 0 or 1.
[7:0]	RW	rgn_base_addr	Base address of the current address area (upper eight bits) NOTE The area address alignment granularity varies according to the address bit width because only the upper eight bits of the address can be configured. • When the address bit width is 32 bits, the lower 24 bits of the base address of the address area are 0 and the area address is 16-MB-aligned. • When the address bit width is 40 bits, the lower 32 bits of the base address of the address area are 0 and the area address is 4-GB-aligned. Only the 32-bit address bit width is supported in this version.

AXI_REGION_ATTRIB

AXI_REGION_ATTRIB is an address area attribute register.

Offset Address: 0x104 + 0x10 x *regions* (*regions* = 0−15)

Register Name: AXI_REGION_ATTRIB

Total Reset Value: 0x0001_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		bnk_mod		reserved		rnk_mod		reserved				addr_aligned				ch_offset								reserved		ch_intlv		ch_mode		ch_start	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	bnk_mod	Bank interleaving granularity in the channel of the current address area (the interleaving granularity varies according to the component) 8 bytes*2^n (8-bit components) 16 bytes*2^n (16-bit components) 32 bytes*2^n (32-bit components) 64 bytes*2^n (64-bit components) n=0−7 **NOTE** The bank interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).
[27:26]	RO	reserved	Reserved
[25:24]	RW	rnk_mod	Rank interleaving mode of the channel of the current address area 0x0: The configuration in the DMC is used. 0x1: a single independent rank address 0x2: Two rank addresses are interleaved. 0x3: Four rank addresses are interleaved. Only one channel is supported in this version and the channel supports only one rank.
[23:19]	RO	reserved	Reserved

[18:16]	RW	addr_aligned	Address boundary alignment granularity of the current address area 0x0: 8 bytes (valid only when the DMC data bit width is 64 bits) 0x1: 16 bytes 0x2: 32 bytes 0x3: 64 bytes 0x4: 128 bytes 0x5: 256 bytes 0x6: 512 bytes 0x7: 1 KB **NOTE** • Commands that cross the address alignment boundary will be split. • The address alignment granularity must be less than or equal to the bank interleaving granularity (bnk_mod). • When addresses are interleaved, the address alignment granularity must be less than or equal to the address interleaving granularity (ch_intlv). • When the address is independent, the address alignment granularity must be less than or equal to the page size of the DDR.
[15:8]	RW	ch_offset	Offset address of the current address area in the channel (upper eight bits) **NOTE** The offset address is used to replace the upper eight bits of the address in the channel to implement the offset of the mapping address in the channel. The offset address varies according to the address bit width. • Bits [31:24] of the 32-bit address after channel mapping can be replaced. • Bits [39:32] of the 40-bit address after channel mapping can be replaced. Only the 32-bit address bit width is supported in this version.
[7:6]	RO	reserved	Reserved
[5:4]	RW	ch_intlv	Address interleaving granularity of the current address area (invalid in single independent channel address mode) 0x0: 128 bytes 0x1: 256 bytes 0x2: 512 bytes 0x3: 1 KB **NOTE** • Commands are alternately sent to multiple channels based on this granularity. • When channels are interleaved, the address interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).

[3:2]	RW	ch_mode	Channel mapping mode of the current address area 0x0: no mapping 0x1: The address of a single channel is mapped to the channel, and the address is independent 0x2: The addresses of two channels are mapped to the channel, and the addresses are interleaved. 0x3: The addresses of four channels are mapped to the channel, and the addresses are interleaved. **NOTE** • Commands that attempt to access the unmapped address areas are processed as incorrect commands. In this case, interrupts are reported, command information is recorded, and the SLVERR response is returned from the AXI bus. • Only one channel (DMC0) is supported in this version.
[1:0]	RW	ch_start	Mapping start channel of the current address area 0x0: channel 0 0x1: channel 1 0x2: channel 2 0x3: channel 3 **NOTE** • In single-channel mapping mode, the mapping start channel can be any channel. • In dual-channel mapping mode, the mapping start channel must be channel 0 (addresses of channel 0 and channel 1 are interleaved) or channel 2 (addresses of channel 2 and channel 3 are interleaved). • In quad-channel mapping mode, the mapping start channel must be channel 0 (addresses of channels 0−3 are interleaved). • Only one channel (DMC0) is supported in this version.

AXI_REGION_SCRMBL

AXI_REGION_SCRMBL is an address scrambling code mode register for address areas.

Offset Address	Register Name	Total Reset Value
0x108 + 0x10 x *regions* (*regions* = 0−15)	AXI_REGION_SCRMBL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bnk_scrmbl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved. This field is fixed at 0.

[3:0]	RW	bnk_scrmbl	Bank address scrambling code mode 0x0: no scrambling code In single-channel mode 0x1: addr[14:12] = addr[14:12] XOR addr[19:17] 0x2: addr[14:12] = addr[14:12] XOR addr[20:18] 0x3: addr[14:12] = addr[14:12] XOR addr[21:19] 0x4: addr[14:12] = addr[14:12] XOR addr[22:20] 0x5: addr[14:12] = addr[14:12] XOR addr[23:21] 0x6: addr[14:12] = addr[14:12] XOR addr[24:22] 0x7: addr[14:12] = addr[14:12] XOR addr[25:23] Other values: reserved In dual-channel mode (bnk_scrmbl based on the address exchange of ch_scrmbl) 0x1: addr[15:13] = addr[15:13] XOR addr[20:18] 0x2: addr[15:13] = addr[15:13] XOR addr[21:19] 0x3: addr[15:13] = addr[15:13] XOR addr[22:20] 0x4: addr[15:13] = addr[15:13] XOR addr[23:21] 0x5: addr[15:13] = addr[15:13] XOR addr[24:22] 0x6: addr[15:13] = addr[15:13] XOR addr[25:23] 0x7: addr[15:13] = addr[15:13] XOR addr[26:24] Other values: reserved NOTE addr indicates the bus address.

AXI_QOS_MAP

AXI_QOS_MAP is a command priority mapping mode register.

Offset Address	Register Name	Total Reset Value
0x200 + 0x10 x *ports* (*ports* = 0–8)	AXI_QOS_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										qos_rever	rw_arb_mode	reserved							pri_map_mode	id_map_idx											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	qos_rever	QoS inversion enable (for the priority arbitration of the read and write commands from the same port) 0: Priority 0 (axqos = 0) is the lowest priority. 1: Priority 0 (axqos = 0) is the highest priority. **NOTE** This register is valid only when rw_arb_mode is 1.
[20]	RW	rw_arb_mode	Arbitration mode for the read and write commands from the same port 0: The arbitration is based on the command read/write type. • The command that arrives first is arbitrated first. • When the read and write commands arrive simultaneously (or the backpressure is imposed on them simultaneously), the read command is arbitrated before the write command. 1: The arbitration is based on the command priority. • The command that arrives first is arbitrated first. • When the read and write commands arrive simultaneously (or the backpressure is imposed on them simultaneously), the command with a higher priority is arbitrated first. • If the priorities of the read and write commands are the same, the command that is not arbitrated last time is arbitrated according to the least recently used (LRU) rule.
[19:13]	RO	reserved	Reserved

[12]	RW	pri_map_mode	Priority mapping mode of the read/write command 0: Any three bits in the command ID or associated signal are used as the mapping index. 1: Any three bits in the lower 16 bits of the command ID are used as the mapping index. **NOTE** The mapping index is obtained by using either of the preceding methods, and the command priority is obtained by mapping the index to the priority lookup table. The lookup table indicates the description of AXI_QOS_WRPRI or AXI_QOS_RDPRI.
[11:0]	RW	id_map_idx	Three methods for selecting bits in the command ID as the mapping index when the command ID is used to map the priority id_map_idx[11:8]: Any one bit in the lower 16 bits of the command ID is selected as idx[2]. id_map_idx[7:4]: Any one bit in the lower 16 bits of the command ID is selected as idx[1]. id_map_idx[3:0]: Any one bit in the lower 16 bits of the command ID is selected as idx[0]. For example, if id_map_idx is set to 0x3A0, ID[3], ID[10], and ID[0] of the command form idx[2:0], which is used to map the command priority from the priority lookup table. The lookup table indicates the description of AXI_QOS_WRPRI or AXI_QOS_RDPRI. **NOTE** The command ID indicates the original command ID.

AXI_QOS_WRPRIn

AXI_QOS_WRPRIn is a write command priority mapping table register.

Offset Address	Register Name	Total Reset Value
0x204 + 0x10 x *ports* (*ports* = 0−8)	AXI_QOS_WRPRIn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	wr_pri7			reserved	wr_pri6			reserved	wr_pri5			reserved	wr_pri4			reserved	wr_pri3			reserved	wr_pri2			reserved	wr_pri1			reserved	wr_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:28]	RW	wr_pri7	Priority of the write command when the mapping index is 7 0x0: highest priority … 0x7: lowest priority
[27]	RO	reserved	Reserved
[26:24]	RW	wr_pri6	Priority of the write command when the mapping index is 6 0x0: highest priority … 0x7: lowest priority
[23]	RO	reserved	Reserved
[22:20]	RW	wr_pri5	Priority of the write command when the mapping index is 5 0x0: highest priority … 0x7: lowest priority
[19]	RO	reserved	Reserved
[18:16]	RW	wr_pri4	Priority of the write command when the mapping index is 4 0x0: highest priority … 0x7: lowest priority
[15]	RO	reserved	Reserved
[14:12]	RW	wr_pri3	Priority of the write command when the mapping index is 3 0x0: highest priority … 0x7: lowest priority
[11]	RO	reserved	Reserved
[10:8]	RW	wr_pri2	Priority of the write command when the mapping index is 2 0x0: highest priority … 0x7: lowest priority
[7]	RO	reserved	Reserved
[6:4]	RW	wr_pri1	Priority of the write command when the mapping index is 1 0x0: highest priority … 0x7: lowest priority
[3]	RO	reserved	Reserved

[2:0]	RW	wr_pri0	Priority of the write command when the mapping index is 0 0x0: highest priority … 0x7: lowest priority

AXI_QOS_RDPRIn

AXI_QOS_RDPRIn is a read command priority mapping table register.

Offset Address	Register Name	Total Reset Value
0x208 + 0x10 x *ports* (*ports* = 0−8)	AXI_QOS_RDPRIn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rd_pri7			reserved	rd_pri6			reserved	rd_pri5			reserved	rd_pri4			reserved	rd_pri3			reserved	rd_pri2			reserved	rd_pri1			reserved	rd_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	rd_pri7	Priority of the read command when the mapping index is 7 0x0: highest priority … 0x7: lowest priority
[27]	RO	reserved	Reserved
[26:24]	RW	rd_pri6	Priority of the read command when the mapping index is 6 0x0: highest priority … 0x7: lowest priority
[23]	RO	reserved	Reserved
[22:20]	RW	rd_pri5	Priority of the read command when the mapping index is 5 0x0: highest priority … 0x7: lowest priority
[19]	RO	reserved	Reserved

[18:16]	RW	rd_pri4	Priority of the read command when the mapping index is 4 0x0: highest priority … 0x7: lowest priority
[15]	RO	reserved	Reserved
[14:12]	RW	rd_pri3	Priority of the read command when the mapping index is 3 0x0: highest priority … 0x7: lowest priority
[11]	RO	reserved	Reserved
[10:8]	RW	rd_pri2	Priority of the read command when the mapping index is 2 0x0: highest priority … 0x7: lowest priority
[7]	RO	reserved	Reserved
[6:4]	RW	rd_pri1	Priority of the read command when the mapping index is 1 0x0: highest priority … 0x7: lowest priority
[3]	RO	reserved	Reserved
[2:0]	RW	rd_pri0	Priority of the read command when the mapping index is 0 0x0: highest priority … 0x7: lowest priority

AXI_QOS_ADPTn

AXI_QOS_ADPTn is a priority adaptation cycle mapping table register.

Offset Address	Register Name	Total Reset Value
0x20C + 0x10 x *ports* (*ports* = 0−8)	AXI_QOS_ADPTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wr_adpt_high				reserved	wr_adpt_lvl			wr_adpt_low				reserved				rd_adpt_high				reserved	rd_adpt_lvl			rd_adpt_low			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	wr_adpt_high	Write command priority adaptation cycle (high-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[23]	RO	reserved	Reserved
[22:20]	RW	wr_adpt_lvl	Write command priority adaptation cycle threshold 0x0−0x1: reserved 0x2−0x7: When the priority of a command is greater than or equal to the threshold, the command is mapped to the high-level cycle. Otherwise, the command is mapped to the low-level cycle. For example: 0x5: The priority adaptation cycle of write commands with priorities 2−5 is configured in wr_adpt_high, and that of write commands with priorities 6−7 is configured in wr_adpt_low.
[19:16]	RW	wr_adpt_low	Write command priority adaptation cycle (low-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[15:12]	RO	reserved	Reserved

[11:8]	RW	rd_adpt_high	Read command priority adaptation cycle (high-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[7]	RO	reserved	Reserved
[6:4]	RW	rd_adpt_lvl	Read command priority adaptation cycle threshold 0x0−0x1: reserved 0x2−0x7: When the priority of a command is greater than or equal to the threshold, the command is mapped to the high-level cycle. Otherwise, the command is mapped to the low-level cycle. For example: 0x5: The priority adaptation cycle of read commands with priorities 2−5 is configured in rd_adpt_high, and that of read commands with priorities 6−7 is configured in rd_adpt_low.
[3:0]	RW	rd_adpt_low	Read command priority adaptation cycle (low-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.

AXI_OSTD_PRTn

AXI_OSTD_PRTn is a port command OSTD restriction register.

Offset Address	Register Name	Total Reset Value
0x300 + 0x10 x *ports* (*ports* = 0−8)	AXI_OSTD_PRTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								prt_ostd_lvl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:0]	RW	prt_ostd_lvl	Command OSTD threshold of a port 0x00: The number of command OSTDs of a port is not limited. 0x01−0x7F: maximum number of command OSTDs allowed by the port **NOTE** • In this document, the number of OSTDs is the number of commands in the back-end module QoSBuf. • In this document, the threshold cannot be greater than the command queue depth of the QoSBuf that is specified by setting parameters.

AXI_OSTD_PRT_STn

AXI_OSTD_PRT_STn is a port command OSTD statistics register.

Offset Address	Register Name	Total Reset Value
0x304 + 0x10 x *ports* (*ports* = 0−8)	AXI_OSTD_PRT_STn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								prt_ostd_st							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RO	prt_ostd_st	Command OSTD statistics of a port

AXI_OSTD_GROUPn

AXI_OSTD_GROUPn is a command OSTD register for the port group.

Offset Address	Register Name	Total Reset Value
0x400 + 0x10 x *groups* (*groups* = 0−3)	AXI_OSTD_GROUPn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				group_ostd_sel												reserved								group_ostd_lvl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:16]	RW	group_ostd_sel	Port select of a group When group_ostd_sel[n] is 0, port *n* is not selected. When group_ostd_sel[n] is 1, port *n* is selected. **NOTE** Only the selected ports are involved in the OSTD statistics of the port group.
[15:7]	RO	reserved	Reserved
[6:0]	RW	group_ostd_lvl	Command OSTD threshold of a port group 0x00: The number of command OSTDs of the port group is not limited. 0x01−0x7F: maximum number of accumulated command OSTDs allowed by the port group **NOTE** • The number of the command OSTDs of a port group is the sum of the command OSTDs of all the ports selected by the port group. • When the number of command OSTDs exceeds the threshold, all the ports in the port group are blocked.

AXI_OSTD_PRIn0

AXI_OSTD_PRIn0 is priority-based port group command OSTD restriction register 0.

Offset Address	Register Name	Total Reset Value
0x404 + 0x10 x *groups* (*groups* = 0−3)	AXI_OSTD_PRIn0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pri3_ostd_lvl							reserved	pri2_ostd_lvl							reserved	pri1_ostd_lvl							reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:24]	RW	pri3_ostd_lvl	Priority 3 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[23]	RO	reserved	Reserved
[22:16]	RW	pri2_ostd_lvl	Priority 2 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[15]	RO	reserved	Reserved
[14:8]	RW	pri1_ostd_lvl	Priority 1 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[7:0]	RO	reserved	Reserved

AXI_OSTD_PRIn1

AXI_OSTD_PRIn1 is priority-based port group command OSTD restriction register 1.

Offset Address	Register Name	Total Reset Value
0x408 + 0x10 x *groups* (*groups* = 0–3)	AXI_OSTD_PRIn1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pri7_ostd_lvl							reserved	pri6_ostd_lvl							reserved	pri5_ostd_lvl							reserved	pri4_ostd_lvl						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:24]	RW	pri7_ostd_lvl	Priority 7 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01–0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[23]	RO	reserved	Reserved
[22:16]	RW	pri6_ostd_lvl	Priority 6 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01–0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[15]	RO	reserved	Reserved

[14:8]	RW	pri5_ostd_lvl	Priority 5 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[7]	RO	reserved	Reserved
[6:0]	RW	pri4_ostd_lvl	Priority 4 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.

AXI_OSTD_GROUP_STn

AXI_OSTD_GROUP_STn is a command OSTD statistics register for the port group.

Offset Address	Register Name	Total Reset Value
0x40C + 0x10 x *groups* (*groups* = 0−3)	AXI_OSTD_GROUP_STn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								group_ostd_st							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RO	group_ostd_st	Command OSTD statistics of a port group

AXI_STATUS

AXI_STATUS is a port operating mode register.

Offset Address	Register Name	Total Reset Value
0x600	AXI_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				axi_if_busy											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	axi_if_busy	Operating mode of each AXI port When axi_prt_busy[n] is 0, AXI port *n* is idle. When axi_prt_busy[n] is 1, AXI port *n* is processing commands or data.

AXI_INT_STATUS

AXI_INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x610	AXI_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				int_ports											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	int_ports	Interrupt source indicator When interrupt_ports[n] is 1, the interrupt source is port *n*. **NOTE** When the command does not pass the security permission check and the interrupt is enabled, the corresponding port generates interrupts.

4.1.6 QOSBUF Registers of the DDRC

4.1.6.1 Register Summary

Table 4-8 describes QoSBuf registers.

Table 4-8 Summary of QoSBuf registers (base address: 0x1206_4000)

Offset Address	Register	Description	Page
0x000	QOSB_PUSH_CTRL	QoSBuf push configuration register	4-38
0x004	QOSB_ADPT_CTRL	QoSBuf adaptation configuration register	4-38
0x008 + 0x4 x *fids*	QOSB_FLUX_ID	QoSBuf matched ID register for traffic statistics	4-39
0x024 + 0x4 x *fids*	QOSB_FLUX_ID_MASK	QoSBuf traffic statistics ID mask register	4-39
0x040	QOSB_FLUX_PRD	QoSBuf traffic statistical period register	4-40
0x044 + 0x4 x *fgps*	QOSB_FLUX_LVL	QoSBuf traffic statistical threshold register	4-40
0x064	QOSB_FLUX_EN	QoSBuf traffic statistics enable register	4-41
0x068 + 0x4 x *chans*	QOSB_BANK_CTRL	QoSBuf bank rotating control register	4-41
0x078 + 0x4 x *chans*	QOSB_GREEN_CTRL	QoSBuf green channel control register	4-42
0x088	QOSB_BUF_BYP	QoSBuf bypass control register	4-43
0x08C + 0x4 x *chans*	QOSB_WBUF_CTRL	QoSBuf write command priority adjustment control register	4-44
0x09C	QOSB_WRTOUT0	QoSBuf write command timeout period register 0	4-45
0x0A0	QOSB_WRTOUT1	QoSBuf write command timeout period register 1	4-45
0x0A4	QOSB_WRTOUT2	QoSBuf write command timeout period register 2	4-46
0x0A8	QOSB_WRTOUT3	QoSBuf write command timeout period register 3	4-46
0x0AC	QOSB_RDTOUT0	QoSBuf read command timeout period register 0	4-47
0x0B0	QOSB_RDTOUT1	QoSBuf read command timeout period register 1	4-47
0x0B4	QOSB_RDTOUT2	QoSBuf read command timeout period register 2	4-48
0x0B8	QOSB_RDTOUT3	QoSBuf read command timeout period register 3	4-49

Offset Address	Register	Description	Page
0x0BC	QOSB_WRTOUT_MAP	QoSBuf write command timeout mapping mode control register	4-49
0x0D0	QOSB_RDTOUT_MAP	QoSBuf read command timeout mapping mode control register	4-50
0x0D4	QOSB_WRAGE0	QoSBuf write command aging configuration register 0	4-51
0x0D8	QOSB_WRAGE1	QoSBuf write command aging configuration register 1	4-51
0x0DC	QOSB_RDAGE0	QoSBuf read command aging configuration register 0	4-52
0x0E0	QOSB_RDAGE1	QoSBuf read command aging configuration register 1	4-53
0x0E4	QOSB_WRAGE_MAP	QoSBuf write command aging mapping mode control register	4-54
0x0E8	QOSB_RDAGE_MAP	QoSBuf read command aging mapping mode control register	4-55
0x0EC	QOSB_ROWHIT_PRILVL	QoSBuf row-hit priority threshold register	4-55
0x0F0	QOSB_ROWHIT_PRI	QoSBuf row-hit priority control register	4-57
0x0F4	QOSB_ROWHIT_CTRL	QoSBuf row-hit enable register	4-57
0x108	QOSB_CKG_CFG	QoSBuf clock control register	4-59
0x10C + 0x4 x *chans*	QOSB_DMC_LVL	QoSBuf threshold control register for commands that enter the DMC module	4-59
0x120	QOSB_CFG_PERF	QoSBuf performance statistics mode configuration register	4-60
0x124	QOSB_CMD_SUM	QoSBuf accumulated command count register	4-60
0x128	QOSB_SLOT_STAT0	QoSBuf queue status register 0	4-61
0x12C	QOSB_SLOT_STAT1	QoSBuf queue status register 1	4-61
0x130	QOSB_SLOT_STAT2	QoSBuf queue status register 2	4-62
0x134	QOSB_SLOT_STAT3	QoSBuf queue status register 3	4-62

Offset Address	Register	Description	Page
0x140 + 0x4 x *chans*	QOSB_WBUF_STAT0	QoSBuf write buffer status register 0	4-62
0x150 + 0x4 x *chans*	QOSB_WBUF_STAT1	QoSBuf write buffer status register 1	4-63
0x160 + 0x4 x *chans*	QOSB_RDRBUF_STAT	Buffer status register for the Reorder module	4-63
0x170	QOSB_INTMSK	QoSBuf interrupt mask register	4-64
0x174	QOSB_RINT	QoSBuf raw interrupt register	4-64
0x178	QOSB_INTSTS	QoSBuf interrupt status register	4-65
0x180	QOSB_CMD_CNT	QoSBuf command statistics register	4-65
0x190 + 0x4 x *chans*	QOSB_RNK_CNT	QoSBuf command (in each rank) statistics register	4-66
0x1A0 + 0x4 x *chans*	QOSB_BNK_CNT0	QoSBuf command (in each bank) statistics register 0	4-66
0x1B0 + 0x4 x *chans*	QOSB_BNK_CNT1	QoSBuf command (in each bank) statistics register 1	4-67
0x1C0 + 0x4 x *chans*	QOSB_BNK_CNT2	QoSBuf command (in each bank) statistics register 2	4-67
0x1D0 + 0x4 x *chans*	QOSB_BNK_CNT3	QoSBuf command (in each bank) statistics register 3	4-68
0x1E0	QOSB_OSTD_CNT	QoSBuf OSTD command (in each channel) statistics register	4-68
0x1E4	QOSB_WR_CMD_SUM	QoSBuf accumulated write command count register	4-68
0x1E8	QOSB_RD_CMD_SUM	QoSBuf accumulated read command count register	4-69
0x1F0	QOSB_TIMEOUT_MODE	QoSBuf timeout mode selection register	4-69
0x1F4	QOSB_WBUF_PRI_CTRL	QoSBuf write buffer priority adjustment control register	4-70
0x1F8	QOSB_RHIT_CTRL	QoSBuf row-hit priority adjustment control register	4-71

Table 4-9 describes the value ranges and meanings of variables in the offset addresses for QoSBuf registers.

Table 4-9 Variables in the offset addresses for QoSBuf registers

Variable	Value Range	Description
chans	0–1	Number of channels
fgps	0–7	Number of groups whose traffic statistics is collected
fids	0–6	Number of matched IDs during traffic statistics

4.1.6.2 Register Description

QOSB_PUSH_CTRL

QOSB_PUSH_CTRL is a QosBuf push configuration register.

Offset Address	Register Name	Total Reset Value
0x000	QOSB_PUSH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													mid_push_en	addr_push_en	id_push_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	mid_push_en	Push enable for commands with the same MID 0: disabled 1: enabled
[1]	RW	addr_push_en	Push enable for commands with the same address 0: disabled 1: enabled
[0]	RW	id_push_en	Push enable for commands with the same ID 0: disabled 1: enabled

QOSB_ADPT_CTRL

QOSB_ADPT_CTRL is a QoSBuf adaptation configuration register.

Offset Address	Register Name	Total Reset Value
0x004	QOSB_ADPT_CTRL	0x0000_0FF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												adpt_share_cnt																reserved			adpt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:4]	RW	adpt_share_cnt	Adapt counter for lower bits. When the value of this counter decreases to 0, the counter for upper bits corresponding to each CMD decreases by 1.
[3:1]	RO	reserved	Reserved
[0]	RW	adpt_en	Adapt enable 0: disabled 1: enabled

QOSB_FLUX_ID

QOSB_FLUX_ID is a QoSBuf matched ID register for traffic statistics.

Offset Address	Register Name	Total Reset Value
0x008 + 0x4 x *fids* (*fids* = 0–6)	QOSB_FLUX_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flux_id	Matched ID for traffic statistics. The ID ranges from 0 to 6, and each ID corresponds to a statistics group. If the traffic ID matches none of the seven IDs, the traffic is included in the default group.

QOSB_FLUX_ID_MASK

QOSB_FLUX_ID_MASK is a QoSBuf traffic statistics ID mask register.

Offset Address	Register Name	Total Reset Value
0x024 + 0x4 x *fids* (*fids* = 0–6)	QOSB_FLUX_ID_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flux_id_mask	QoSBuf traffic statistics ID mask, corresponding to QOSB_FLUX_ID 0: Bits of the corresponding ID are ignored. 1: Bits of the corresponding ID are compared.

QOSB_FLUX_PRD

QOSB_FLUX_PRD is a QoSBuf traffic statistical period register.

Offset Address	Register Name	Total Reset Value
0x040	QOSB_FLUX_PRD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																flux_prd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	flux_prd	Traffic statistical period

QOSB_FLUX_LVL

QOSB_FLUX_LVL is a QoSBuf traffic statistical threshold register.

Offset Address	Register Name	Total Reset Value
0x044 + 0x4 x *fgps* (*fgps* = 0–7)	QOSB_FLUX_LVL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flux_lvl																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	flux_lvl	Traffic statistical threshold. During the statistical period, the priority of the command is decreased to the lowest one when the traffic exceeds the threshold.

QOSB_FLUX_EN

QOSB_FLUX_EN is a QoSBuf traffic statistics enable register.

Offset Address	Register Name	Total Reset Value
0x064	QOSB_FLUX_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															flux_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	flux_en	Traffic statistics enable 0: disabled 1: enabled

QOSB_BANK_CTRL

QOSB_BANK_CTRL is a QoSBuf bank rotating control register.

Offset Address	Register Name	Total Reset Value
0x068 + 0x4 x *chans* (*chans* = 0−1)	QOSB_BANK_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ba_cnt_lvl				reserved			ba_intleav_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	ba_cnt_lvl	Bank conflict threshold. When the number of commands with the same bank address exceeds the threshold, bank conflict occurs. Otherwise, there is no bank conflict.
[3:1]	RO	reserved	Reserved
[0]	RW	ba_intleav_en	QoSBuf bank rotating enable 0: disabled 1: enabled

QOSB_GREEN_CTRL

QOSB_GREEN_CTRL is a QoSBuf green channel control register.

Offset Address	Register Name	Total Reset Value
0x078 + 0x4 x *chans* (*chans* = 0−1)	QOSB_GREEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								green_lvl				reserved			green_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:4]	RW	green_lvl	Green channel threshold. That is, the empty locations above this threshold are reserved for green channels. For example, if there are 12 DMC queues (queues 0−11) and the threshold is 9, queues 10 and 11 are reserved for green channels. NOTE • When this field is set to N, the actual number of allowed commands is (N + 1) because of the pipeline issue. • This register cannot be dynamically configured when it is being accessed.
[3:1]	RO	reserved	Reserved
[0]	RW	green_en	Green channel enable (channels are not controlled separately, which needs to be optimized later) 0: disabled 1: enabled

QOSB_BUF_BYP

QOSB_BUF_BYP is a QoSBuf bypass control register.

Offset Address	Register Name	Total Reset Value
0x088	QOSB_BUF_BYP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								qos_buf_byp
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	qos_buf_byp	QoSBuf bypass control x0: forcible non-bypass mode. That is, all the commands enter the QoSBuf module when the value is set to 00 or 10. 01: whether to bypass depends on the queue status in the DMC 11: forcible bypass mode. None of the commands enters the QoSBuf module. NOTE These modes need to be configured before the access. The dynamic configuration is forbidden during the access.

QOSB_WBUF_CTRL

QOSB_WBUF_CTRL is a QoSBuf write command priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x08C + 0x4 x *chans* (*chans* = 0−1)	QOSB_WBUF_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbuf_ptun_en	wbuf_pri2			wbuf_lvl2								reserved	wbuf_pri1			wbuf_lvl1								wbuf_lvl0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbuf_ptun_en	Write command priority adjustment enable 0: disabled 1: enabled
[30:28]	RW	wbuf_pri2	Priority of write buffer threshold 2
[27:20]	RW	wbuf_lvl2	Write buffer threshold 2. When the number of commands increasingly reaches the threshold, if the priorities of the write commands are lower than wbuf_pri2, the priorities of the write commands are set to wbuf_pri2. If the priorities of the write commands are higher than wbuf_pri2, the priorities of the write commands are restored to their previous priorities. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.
[19]	RO	reserved	Reserved
[18:16]	RW	wbuf_pri1	Priority of write buffer threshold 1 priority
[15:8]	RW	wbuf_lvl1	Write buffer threshold 1. When the number of commands increasingly or decreasingly reaches the threshold, if the priorities of the write commands are lower than wbuf_pri1, the priorities of the write commands are set to wbuf_pri1. If the priorities of the write commands are higher than wbuf_pri1, the priorities of the write commands are restored to their previous priorities. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.
[7:0]	RW	wbuf_lvl0	Write buffer threshold 0. When the number of commands decreasingly reaches the threshold, the priorities of the write commands are decreased to the lowest priority. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.

QOSB_WRTOUT0

QOSB_WRTOUT0 is QoSBuf write command timeout period register 0.

Offset Address	Register Name	Total Reset Value
0x09C	QOSB_WRTOUT0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_tout3		wr_tout2		wr_tout1		wr_tout0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout3	Write command timeout period (level 3) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout2	Write command timeout period (level 2) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout1	Write command timeout period (level 1) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout0	Write command timeout period (level 0) 0x0: The timeout function is disabled. 0x1−0xFF: *n* x 4 clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bits. That is, the lower two bits are fixed at 0.

QOSB_WRTOUT1

QOSB_WRTOUT1 is QoSBuf write command timeout period register 1.

Offset Address	Register Name	Total Reset Value
0x0A0	QOSB_WRTOUT1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_tout7		wr_tout6		wr_tout5		wr_tout4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout7	Write command timeout period (level 7) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout6	Write command timeout period (level 6) The configuration mode is the same as that of wr_tout0.

[15:8]	RW	wr_tout5	Write command timeout period (level 5) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout4	Write command timeout period (level 4) The configuration mode is the same as that of wr_tout0.

QOSB_WRTOUT2

QOSB_WRTOUT2 is QoSBuf write command timeout period register 2.

Offset Address	Register Name	Total Reset Value
0x0A4	QOSB_WRTOUT2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_tout11		wr_tout10		wr_tout9		wr_tout8	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout11	Write command timeout period (level 11) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout10	Write command timeout period (level 10) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout9	Write command timeout period (level 9) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout8	Write command timeout period (level 8) The configuration mode is the same as that of wr_tout0.

QOSB_WRTOUT3

QOSB_WRTOUT3 is QoSBuf write command timeout period register 3.

Offset Address	Register Name	Total Reset Value
0x0A8	QOSB_WRTOUT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_tout15		wr_tout14		wr_tout13		wr_tout12	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout15	Write command timeout period (level 15) The configuration mode is the same as that of wr_tout0.

[23:16]	RW	wr_tout14	Write command timeout period (level 14) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout13	Write command timeout period (level 13) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout12	Write command timeout period (level 12) The configuration mode is the same as that of wr_tout0.

QOSB_RDTOUT0

QOSB_RDTOUT0 is QoSBuf read command timeout period register 0.

Offset Address	Register Name	Total Reset Value
0x0AC	QOSB_RDTOUT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout3								rd_tout2								rd_tout1								rd_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout3	Read command timeout period (level 3) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout2	Read command timeout period (level 2) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout1	Read command timeout period (level 1) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout0	Read command timeout period (level 0) 0x0: The timeout function is disabled. 0x1−0xFF: *n* x 4 clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bits. That is, the lower two bits are fixed at 0.

QOSB_RDTOUT1

QOSB_RDTOUT1 is QoSBuf read command timeout period register 1.

Offset Address	Register Name	Total Reset Value
0x0B0	QOSB_RDTOUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout7								rd_tout6								rd_tout5								rd_tout4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout7	Read command timeout period (level 7) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout6	Read command timeout period (level 6) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout5	Read command timeout period (level 5) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout4	Read command timeout period (level 4) The configuration mode is the same as that of rd_tout0.

QOSB_RDTOUT2

QOSB_RDTOUT2 is QoSBuf read command timeout period register 2.

Offset Address	Register Name	Total Reset Value
0x0B4	QOSB_RDTOUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout11								rd_tout10								rd_tout9								rd_tout8							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout11	Read command timeout period (level 11) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout10	Read command timeout period (level 10) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout9	Read command timeout period (level 9) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout8	Read command timeout period (level 8) The configuration mode is the same as that of rd_tout0.

QOSB_RDTOUT3

QOSB_RDTOUT3 is QoSBuf read command timeout period register 3.

Offset Address	Register Name	Total Reset Value
0x0B8	QOSB_RDTOUT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_tout15		rd_tout14		rd_tout13		rd_tout12	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout15	Read command timeout period (level 15) The configuration mode is the same as that ofrd_tout0.
[23:16]	RW	rd_tout14	Read command timeout period (level 14) The configuration mode is the same as that ofrd_tout0.
[15:8]	RW	rd_tout13	Read command timeout period (level 13) The configuration mode is the same as that ofrd_tout0.
[7:0]	RW	rd_tout12	Read command timeout period (level 12) The configuration mode is the same as that ofrd_tout0.

QOSB_WRTOUT_MAP

QOSB_WRTOUT_MAP is a QoSBuf write command timeout mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0BC	QOSB_WRTOUT_MAP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	wrtout_map3	reserved	wrtout_map2	reserved	wrtout_map1	reserved	wrtout_map0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	wrtout_map3	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved

[20:16]	RW	wrtout_map2	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	wrtout_map1	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	wrtout_map0	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map0 indicates the position of bit 0 in the ID.

QOSB_RDTOUT_MAP

QOSB_RDTOUT_MAP is a QoSBuf read command timeout mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0D0	QOSB_RDTOUT_MAP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	rdtout_map3	reserved	rdtout_map2	reserved	rdtout_map1	reserved	rdtout_map0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	rdtout_map3	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	rdtout_map2	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	rdtout_map1	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved

[4:0]	RW	rdtout_map0	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map0 indicates the position of bit 0 in the ID.

QOSB_WRAGE0

QOSB_WRAGE0 is QoSBuf write command aging configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0D4	QOSB_WRAGE0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_age_prd7	wr_age_prd6	wr_age_prd5	wr_age_prd4	wr_age_prd3	wr_age_prd2	wr_age_prd1	wr_age_prd0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd7	Write command aging cycle (level 7) For details, see wr_age_prd0.
[27:24]	RW	wr_age_prd6	Write command aging cycle (level 6) For details, see wr_age_prd0.
[23:20]	RW	wr_age_prd5	Write command aging cycle (level 5) For details, see wr_age_prd0.
[19:16]	RW	wr_age_prd4	Write command aging cycle (level 4) For details, see wr_age_prd0.
[15:12]	RW	wr_age_prd3	Write command aging cycle (level 3) For details, see wr_age_prd0.
[11:8]	RW	wr_age_prd2	Write command aging cycle (level 2) For details, see wr_age_prd0.
[7:4]	RW	wr_age_prd1	Write command aging cycle (level 1) For details, see wr_age_prd0.
[3:0]	RW	wr_age_prd0	Write command aging cycle (level 0) 0x0: The aging function is disabled. 0x1−0xF: (*n* x 16) clock cycles

QOSB_WRAGE1

QOSB_WRAGE1 is QoSBuf write command aging configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0D8	QOSB_WRAGE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_age_prd15	wr_age_prd14	wr_age_prd13	wr_age_prd12	wr_age_prd11	wr_age_prd10	wr_age_prd9	wr_age_prd8
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd15	Write command aging cycle (level 15) For details, see wr_age_prd0.
[27:24]	RW	wr_age_prd14	Write command aging cycle (level 14) For details, see wr_age_prd0.
[23:20]	RW	wr_age_prd13	Write command aging cycle (level 13) For details, see wr_age_prd0.
[19:16]	RW	wr_age_prd12	Write command aging cycle (level 12) For details, see wr_age_prd0.
[15:12]	RW	wr_age_prd11	Write command aging cycle (level 11) For details, see wr_age_prd0.
[11:8]	RW	wr_age_prd10	Write command aging cycle (level 10) For details, see wr_age_prd0.
[7:4]	RW	wr_age_prd9	Write command aging cycle (level 9) For details, see wr_age_prd0.
[3:0]	RW	wr_age_prd8	Write command aging cycle (level 8) For details, see wr_age_prd0.

QOSB_RDAGE0

QOSB_RDAGE0 is QoSBuf read command aging configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0DC	QOSB_RDAGE0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_age_prd7	rd_age_prd6	rd_age_prd5	rd_age_prd4	rd_age_prd3	rd_age_prd2	rd_age_prd1	rd_age_prd0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd7	Read command aging cycle (level 7) For details, see rd_age_prd0.

[27:24]	RW	rd_age_prd6	Read command aging cycle (level 6) For details, see rd_age_prd0.
[23:20]	RW	rd_age_prd5	Read command aging cycle (level 5) For details, see rd_age_prd0.
[19:16]	RW	rd_age_prd4	Read command aging cycle (level 4) For details, see rd_age_prd0.
[15:12]	RW	rd_age_prd3	Read command aging cycle (level 3) For details, see rd_age_prd0.
[11:8]	RW	rd_age_prd2	Read command aging cycle (level 2) For details, see rd_age_prd0.
[7:4]	RW	rd_age_prd1	Read command aging cycle (level 1) For details, see rd_age_prd0.
[3:0]	RW	rd_age_prd0	Read command aging cycle (level 0) 0x0: The aging function is disabled. 0x1−0xF: (*n* x 16) clock cycles

QOSB_RDAGE1

QOSB_RDAGE1 is QoSBuf read command aging configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0E0	QOSB_RDAGE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_age_prd15	rd_age_prd14	rd_age_prd13	rd_age_prd12	rd_age_prd11	rd_age_prd10	rd_age_prd9	rd_age_prd8
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd15	Read command aging cycle (level 15) For details, see rd_age_prd0.
[27:24]	RW	rd_age_prd14	Read command aging cycle (level 14) For details, see rd_age_prd0.
[23:20]	RW	rd_age_prd13	Read command aging cycle (level 13) For details, see rd_age_prd0.
[19:16]	RW	rd_age_prd12	Read command aging cycle (level 12) For details, see rd_age_prd0.
[15:12]	RW	rd_age_prd11	Read command aging cycle (level 11) For details, see rd_age_prd0.

[11:8]	RW	rd_age_prd10	Read command aging cycle (level 10) For details, see rd_age_prd0.
[7:4]	RW	rd_age_prd9	Read command aging cycle (level 9) For details, see rd_age_prd0.
[3:0]	RW	rd_age_prd8	Read command aging cycle (level 8) For details, see rd_age_prd0.

QOSB_WRAGE_MAP

QOSB_WRAGE_MAP is a QoSBuf write command aging mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0E4	QOSB_WRAGE_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wrage_map3				reserved				wrage_map2				reserved				wrage_map1				reserved				wrage_map0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	wrage_map3	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	wrage_map2	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	wrage_map1	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	wrage_map0	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map0 indicates the position of bit 0 in the ID.

QOSB_RDAGE_MAP

QOSB_RDAGE_MAP is a QoSBuf read command aging mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0E8	QOSB_RDAGE_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rdage_map3				reserved				rdage_map2				reserved				rdage_map1				reserved				rdage_map0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	rdage_map3	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	rdage_map2	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	rdage_map1	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	rdage_map0	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map0 indicates the position of bit 0 in the ID.

QOSB_ROWHIT_PRILVL

QOSB_ROWHIT_PRILVL is a QoSBuf row-hit priority threshold register.

Offset Address	Register Name	Total Reset Value
0x0EC	QOSB_ROWHIT_PRILVL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	ch3_rowhit_pri_lvl			reserved			ch2_rowhit_pri_lvl				reserved				ch1_rowhit_pri_lvl				reserved				ch0_rowhit_pri_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	ch3_rowhit_pri_lvl	Channel 3 priority threshold If the current priority is lower than ch3_rohit_pri_lvl, the priority is changed to ch3_rowhit_pri1. If the current priority is higher than ch3_rohit_pri_lvl, the priority is changed to ch3_rowhit_pri0.
[11]	RO	reserved	Reserved
[10:8]	RW	ch2_rowhit_pri_lvl	Channel 2 priority threshold If the current priority is lower than ch2_rohit_pri_lvl, the priority is changed to ch2_rowhit_pri1. If the current priority is higher than ch2_rohit_pri_lvl, the priority is changed to ch2_rowhit_pri0.
[7]	RO	reserved	Reserved
[6:4]	RW	ch1_rowhit_pri_lvl	Channel 1 priority threshold If the current priority is lower than ch1_rohit_pri_lvl, the priority is changed to ch1_rowhit_pri1. If the current priority is higher than ch1_rohit_pri_lvl, the priority is changed to ch1_rowhit_pri0.
[3]	RO	reserved	Reserved
[2:0]	RW	ch0_rowhit_pri_lvl	Channel 0 priority threshold If the current priority is lower than ch0_rohit_pri_lvl, the priority is changed to ch0_rowhit_pri1. If the current priority is higher than ch0_rohit_pri_lvl, the priority is changed to ch0_rowhit_pri0.

QOSB_ROWHIT_PRI

QOSB_ROWHIT_PRI is a QoSBuf row-hit priority control register.

Offset Address	Register Name	Total Reset Value
0x0F0	QOSB_ROWHIT_PRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ch3_rowhit_pri1			reserved	ch3_rowhit_pri0			reserved	ch2_rowhit_pri1			reserved	ch2_rowhit_pri0			reserved	ch1_rowhit_pri1			reserved	ch1_rowhit_pri0			reserved	ch0_rowhit_pri1			reserved	ch0_rowhit_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	ch3_rowhit_pri1	See ch3_rowhit_pri_lvl.
[27]	RO	reserved	Reserved
[26:24]	RW	ch3_rowhit_pri0	See ch3_rowhit_pri_lvl.
[23]	RO	reserved	Reserved
[22:20]	RW	ch2_rowhit_pri1	See ch2_rowhit_pri_lvl.
[19]	RO	reserved	Reserved
[18:16]	RW	ch2_rowhit_pri0	See ch2_rowhit_pri_lvl.
[15]	RO	reserved	Reserved
[14:12]	RW	ch1_rowhit_pri1	See ch1_rowhit_pri_lvl.
[11]	RO	reserved	Reserved
[10:8]	RW	ch1_rowhit_pri0	See ch1_rowhit_pri_lvl.
[7]	RO	reserved	Reserved
[6:4]	RW	ch0_rowhit_pri1	See ch0_rowhit_pri_lvl.
[3]	RO	reserved	Reserved
[2:0]	RW	ch0_rowhit_pri0	See ch0_rowhit_pri_lvl.

QOSB_ROWHIT_CTRL

QOSB_ROWHIT_CTRL is a QoSBuf row-hit enable register.

Offset Address	Register Name	Total Reset Value
0x0F4	QOSB_ROWHIT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ch3_dual_flow_en	ch2_dual_flow_en	ch1_dual_flow_en	ch0_dual_flow_en	ch3_row_hit_en	ch2_row_hit_en	ch1_row_hit_en	ch0_row_hit_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ch3_dual_flow_en	Channel 3 row-hit dual-stream enable 0: disabled 1: enabled
[6]	RW	ch2_dual_flow_en	Channel 2 row-hit dual-stream enable 0: disabled 1: enabled
[5]	RW	ch1_dual_flow_en	Channel 1 row-hit dual-stream enable 0: disabled 1: enabled
[4]	RW	ch0_dual_flow_en	Channel 0 row-hit dual-stream enable 0: disabled 1: enabled
[3]	RW	ch3_row_hit_en	Channel 3 row-hit enable 0: disabled 1: enabled
[2]	RW	ch2_row_hit_en	Channel 2 row-hit enable 0: disabled 1: enabled
[1]	RW	ch1_row_hit_en	Channel 1 row-hit enable 0: disabled 1: enabled
[0]	RW	ch0_row_hit_en	Channel 0 row-hit enable 0: disabled 1: enabled

QOSB_CKG_CFG

QOSB_CKG_CFG is a QoSBuf clock control register.

Offset Address	Register Name	Total Reset Value
0x108	QOSB_CKG_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															dyn_ck_gate
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	dyn_ck_gate	Dynamic clock gating for the QoSBuf module 0: The clock is always enabled. 1: The clock gating is automatic when the module is idle.

QOSB_DMC_LVL

QOSB_DMC_LVL is a QoSBuf threshold control register for commands that enter the DMC module.

Offset Address	Register Name	Total Reset Value
0x10C + 0x4 x *chans* (*chans* = 0−1)	QOSB_DMC_LVL	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dmc_cmd_full_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	dmc_cmd_full_lvl	Number of QoSBuf commands that enter the DMC module. When this threshold is reached, the DMC queue is full. **NOTE** • When this field is set to *N*, the actual number of commands that enter the DMC module is (*N* + 1) because of the pipeline issue. • This register cannot be dynamically configured when it is being accessed.

QOSB_CFG_PERF

QOSB_CFG_PERF is a QoSBuf performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x120	QOSB_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		perf_en	perf_mode	perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	perf_en	Performance statistics enable 1: enabled 0: disabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts the cyclic count. When perf_mode is 1, this bit is automatically cleared after the counting is complete.
[28]	RW	perf_mode	Performance statistical mode 0: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 1: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. **NOTE** The maximum statistical result retains after an overflow occurs.
[27:0]	RW	perf_prd	Performance statistical cycle 0x0: invalid 0x1−0xFFFFFFF: statistical cycle The actual statistical cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This configuration is valid only when perf_mode is 1. When perf_mode is 0, counters related to performance statistics keep counting.

QOSB_CMD_SUM

QOSB_CMD_SUM is a QoSBuf accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x124	QOSB_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_cmd_sum	Accumulated value of the commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_SLOT_STAT0

QOSB_SLOT_STAT0 is QoSBuf queue status register 0.

Offset Address	Register Name	Total Reset Value
0x128	QOSB_SLOT_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_l	Status of bits 0−31 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT1

QOSB_SLOT_STAT1 is QoSBuf queue status register 1.

Offset Address	Register Name	Total Reset Value
0x12C	QOSB_SLOT_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_m0	Status of bits 32−63 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT2

QOSB_SLOT_STAT2 is QoSBuf queue status register 2.

Offset Address	Register Name	Total Reset Value
0x130	QOSB_SLOT_STAT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_m1	Status of bits 64−95 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT3

QOSB_SLOT_STAT3 is QoSBuf queue status register 3.

Offset Address	Register Name	Total Reset Value
0x134	QOSB_SLOT_STAT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_h	Status of bits 96−127 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_WBUF_STAT0

QOSB_WBUF_STAT0 is QoSBuf write buffer status register 0.

Offset Address	Register Name	Total Reset Value
0x140 + 0x4 x *chans* (*chans* = 0−1)	QOSB_WBUF_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	buf_ldata_valid_l	Status of write buffers 0−31 in the QoSBuf. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_WBUF_STAT1

QOSB_WBUF_STAT1 is QoSBuf write buffer status register 1.

Offset Address	Register Name	Total Reset Value
0x150 + 0x4 x *chans* (*chans* = 0−1)	QOSB_WBUF_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	buf_ldata_valid_h	Status of write buffers 32−63 in the QoSBuf. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_RDRBUF_STAT

QOSB_RDRBUF_STAT is a buffer status register for the Reorder module.

Offset Address	Register Name	Total Reset Value
0x160 + 0x4 x *chans* (*chans* = 0−1)	QOSB_RDRBUF_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	e_vld																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	e_vld	Status of reorder buffers 0−31 in the Reorder. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_INTMSK

QOSB_INTMSK is a QoSBuf interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x170	QOSB_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	qos_stat_int_mask	QoSBuf command statistics interrupt mask enable 1: masked 0: enabled

QOSB_RINT

QOSB_RINT is a QoSBuf raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x174	QOSB_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_rint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	INT_WC	qos_stat_rint	QoSBuf command statistics interrupt. Writing 1 clears the interrupt.

QOSB_INTSTS

QOSB_INTSTS is a QoSBuf interrupt status register.

Offset Address	Register Name	Total Reset Value
0x178	QOSB_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_intsts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	INT	qos_stat_intsts	QoSBuf command statistics interrupt

QOSB_CMD_CNT

QOSB_CMD_CNT is a QoSBuf command statistics register.

Offset Address	Register Name	Total Reset Value
0x180	QOSB_CMD_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								qos_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	INT	qos_cmd_cnt	Number of commands in the QoSBuf, including those on the pipeline

QOSB_RNK_CNT

QOSB_RNK_CNT is a QoSBuf command (in each rank) statistics register.

Offset Address	Register Name	Total Reset Value
0x190 + 0x4 x *chans* (*chans* = 0−1)	QOSB_RNK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rnk0_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	rnk0_cmd_cnt	Number of rank 0 commands in the current channel in the QoSBuf

QOSB_BNK_CNT0

QOSB_BNK_CNT0 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1A0 + 0x4 x *chans* (*chans* = 0−1)	QOSB_BNK_CNT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bnk3_cmd_cnt								bnk2_cmd_cnt								bnk1_cmd_cnt								bnk0_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	bnk3_cmd_cnt	Number of bank 3 commands in the current channel in the DMC

[23:16]	RO	bnk2_cmd_cnt	Number of bank 2 commands in the current channel in the DMC
[15:8]	RO	bnk1_cmd_cnt	Number of bank 1 commands in the current channel in the DMC
[7:0]	RO	bnk0_cmd_cnt	Number of bank 0 commands in the current channel in the DMC

QOSB_BNK_CNT1

QOSB_BNK_CNT1 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1B0 + 0x4 x *chans* (*chans* = 0−1)	QOSB_BNK_CNT1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk7_cmd_cnt		bnk6_cmd_cnt		bnk5_cmd_cnt		bnk4_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk7_cmd_cnt	Number of bank 7 commands in the current channel in the DMC
[23:16]	RO	bnk6_cmd_cnt	Number of bank 6 commands in the current channel in the DMC
[15:8]	RO	bnk5_cmd_cnt	Number of bank 5 commands in the current channel in the DMC
[7:0]	RO	bnk4_cmd_cnt	Number of bank 4 commands in the current channel in the DMC

QOSB_BNK_CNT2

QOSB_BNK_CNT2 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1C0 + 0x4 x *chans* (*chans* = 0−1)	QOSB_BNK_CNT2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk11_cmd_cnt		bnk10_cmd_cnt		bnk9_cmd_cnt		bnk8_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk11_cmd_cnt	Number of bank 11 commands in the current channel in the DMC
[23:16]	RO	bnk10_cmd_cnt	Number of bank 10 commands in the current channel in the DMC
[15:8]	RO	bnk9_cmd_cnt	Number of bank 9 commands in the current channel in the DMC
[7:0]	RO	bnk8_cmd_cnt	Number of bank 8 commands in the current channel in the DMC

QOSB_BNK_CNT3

QOSB_BNK_CNT3 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1D0 + 0x4 x *chans* (*chans* = 0−1)	QOSB_BNK_CNT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk15_cmd_cnt		bnk14_cmd_cnt		bnk13_cmd_cnt		bnk12_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk15_cmd_cnt	Number of bank 15 commands in the current channel in the DMC
[23:16]	RO	bnk14_cmd_cnt	Number of bank 14 commands in the current channel in the DMC
[15:8]	RO	bnk13_cmd_cnt	Number of bank 13 commands in the current channel in the DMC
[7:0]	RO	bnk12_cmd_cnt	Number of bank 12 commands in the current channel in the DMC

QOSB_OSTD_CNT

QOSB_OSTD_CNT is a QoSBuf OSTD command (in each channel) statistics register.

Offset Address	Register Name	Total Reset Value
0x1E0	QOSB_OSTD_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				ch1_cmd_ostd		ch0_cmd_ostd	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	ch1_cmd_ostd	Number of OSTD commands in channel 1 in the QoSBuf
[7:0]	RO	ch0_cmd_ostd	Number of OSTD commands in channel 0 in the QoSBuf

QOSB_WR_CMD_SUM

QOSB_WR_CMD_SUM is a QoSBuf accumulated write command count register.

Offset Address	Register Name	Total Reset Value
0x1E4	QOSB_WR_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_wr_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_wr_cmd_sum	Accumulated value of the write commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_RD_CMD_SUM

QOSB_RD_CMD_SUM is a QoSBuf accumulated read command count register.

Offset Address	Register Name	Total Reset Value
0x1E8	QOSB_RD_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_rd_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_rd_cmd_sum	Accumulated value of the read commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_TIMEOUT_MODE

QOSB_TIMEOUT_MODE is a QoSBuf timeout mode selection register.

Offset Address	Register Name	Total Reset Value
0x1F0	QOSB_TIMEOUT_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							timeout_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	timeout_mode	Read/Write command timeout mapping mode select 0: The timeout mode is mapped by using the ID and there are 16 levels of timeout periods. For details about the definition of each level, see QOSB_WRTOUT0 to QOSB_WRTOUT3 or QOSB_RDTOUT0 to QOSB_RDTOUT3. 1: The timeout mode is mapped by using the priority and there are eight levels of timeout periods. The levels in the priority mapping table are the same as the lower eight levels in the ID mapping table.

QOSB_WBUF_PRI_CTRL

QOSB_WBUF_PRI_CTRL is a QoSBuf write buffer priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x1F4	QOSB_WBUF_PRI_CTRL	0x0020_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wbuf_hcnt				wbuf_lcnt			
Reset	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	wbuf_hcnt	The value of this field is used by the internal counter only when the number of write commands reaches the value of QOSB_WBUF_CTRL[wbuf_lvl2] (write buffer threshold 2). When the number reaches wbuf_lvl2, the internal counter starts counting. The priorities of the write commands in the write buffer are increased to pri2 until the count value reaches wbuf_hcnt. Note: pri2 indicates the priority of the write buffer threshold 2. For details, see QOSB_WBUF_CTRL[wbuf_pri2].

[15:0]	RW	wbuf_lcnt	The value of this field is used by the internal counter only when the number of write commands reaches the value of QOSB_WBUF_CTRL[wbuf_lvl2] (write buffer threshold 2) and the count value has already reached wbuf_hcnt. When the count value reaches wbuf_hcnt, the internal counter starts counting again. The priorities of the write commands are increased to pril1 until the count value reaches wbuf_lcnt. If the count value is 0, the priorities of the write commands are always pri2. Note: pri1 indicates the priority of the write buffer threshold 1. For details, see QOSB_WBUF_CTRL[wbuf_pri1].

QOSB_RHIT_CTRL

QOSB_RHIT_CTRL is a QoSBuf row-hit priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x1F8	QOSB_RHIT_CTRL	0x00FF_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rhit_hcnt																rhit_lcnt															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	rhit_hcnt	Time allowed to maintain the row-hit command stream Note: The row-hit command stream is forcibly disconnected when the time for maintaining the row-hit command stream reaches rhit_hcnt. Then the internal counter starts counting again, and the row-hit command stream is allowed to raise the arbitration request until the count value reaches rhit_lcnt.
[15:0]	RW	rhit_lcnt	Duration that the row-hit command stream is disconnected Note: The row-hit command stream is forcibly disconnected when the time for maintaining the row-hit command stream reaches rhit_hcnt. Then the internal counter starts counting again, and the row-hit command stream is allowed to raise the arbitration request until the count value reaches rhit_lcnt.

4.1.7 DMC Registers of the DDRC

4.1.7.1 Register Summary

NOTE

The **rnks** variable in the offset address for DDRC registers indicates the number of ranks for the component. Its value can only be 0.

Table 4-10 describes DMC registers.

Table 4-10 Summary of DMC registers (DMC0 base address: 0x1206_8000)

Offset Address	Register	Description	Page
0x000	DDRC_CTRL_SREF	DDRC self-refresh control register	4-76
0x00C	DDRC_CTRL_SFC	DDRC software configuration command start register	4-77
0x010	DDRC_CTRL_PERF	DDRC performance statistics control register	4-77
0x020	DDRC_CFG_SREF	DDR self-refresh configuration register	4-78
0x024	DDRC_CFG_INIT	DDR initialization configuration register	4-79
0x028	DDRC_CFG_PD	DDR power-down status register	4-79
0x02C	DDRC_CFG_AREF	DDRC auto-refresh mode register	4-81
0x040	DDRC_CFG_WORKMODE	DDRC operating mode register	4-82
0x044	DDRC_CFG_WORKMODE2	DDRC operating mode register	4-84
0x050	DDRC_CFG_DDRMODE	DDR operating mode register	4-84
0x058	DDRC_CFG_SCRAMB	DDR data scrambling configuration register	4-88
0x060 + 0x4 x *rnks*	DDRC_CFG_RNKVOL	DDRC-controlled DDR capacity configuration register	4-89
0x0A0+ 0x4 x *rnks*	DDRC_CFG_ODT	DDR ODT configuration register	4-91
0x0F0	DDRC_CFG_EMRS01	Configuration register for DDR mode register 0 and mode register 1	4-91
0x0F4	DDRC_CFG_EMRS23	Configuration register for DDR mode register 2 and mode register 3	4-92
0x0F8	DDRC_CFG_EMRS45	Configuration register for DDR mode register 4 and mode register 5	4-92
0x0FC	DDRC_CFG_EMRS67	Configuration register for DDR mode register 6 and mode register 7	4-93

Offset Address	Register	Description	Page
0x100	DDRC_CFG_TIMING0	DDRC timing parameter register 0	4-94
0x104	DDRC_CFG_TIMING1	DDRC timing parameter register 1	4-95
0x108	DDRC_CFG_TIMING2	DDRC timing parameter register 2	4-96
0x10C	DDRC_CFG_TIMING3	DDRC timing parameter register 3	4-97
0x110	DDRC_CFG_TIMING4	DDRC timing parameter register 4	4-98
0x114	DDRC_CFG_TIMING5	DDRC timing parameter register 5	4-98
0x118	DDRC_CFG_TIMING6	DDRC timing parameter register 6	4-99
0x11C	DDRC_CFG_TIMING7	DDRC timing parameter register 7	4-100
0x140	DDRC_CFG_BLDATA	DDRC pre-received write data configuration register	4-100
0x144	DDRC_CFG_DMCLVL	DDRC command queue depth threshold configuration register	4-101
0x200	DDRC_CFG_DDRPHY	DDR I/O configuration register	4-101
0x20C	DDRC_CFG_SFC_TIM	DDRC software configuration DDR command timing register	4-102
0x210	DDRC_CFG_SFC	DDRC software DDR command attribute register	4-103
0x214	DDRC_CFG_SFC_ADDR0	Read/Write memory address register 0 for the software configuration module	4-104
0x218	DDRC_CFG_SFC_ADDR1	Read/Write memory address register 1 for the software configuration module	4-105
0x21C	DDRC_CFG_SFC_WDATA0	Write data register 0 for the software configuration module	4-105
0x220	DDRC_CFG_SFC_WDATA1	Write data register 1 for the software configuration module	4-106

Offset Address	Register	Description	Page
0x224	DDRC_CFG_SFC_WDATA2	Write data register 2 for the software configuration module	4-106
0x228	DDRC_CFG_SFC_WDATA3	Write data register 3 for the software configuration module	4-106
0x254	DDRC_CFG_STADAT	DDRC data statistics control register	4-107
0x258	DDRC_CFG_DATMIN	DMC data counting minimum threshold register	4-108
0x25C	DDRC_CFG_DATMAX	DMC data counting maximum threshold register	4-108
0x260	DDRC_CFG_STACMD	DDR performance statistics mode register	4-109
0x264	DDRC_CFG_CMDMIN	DMC command counting minimum threshold register	4-110
0x268	DDRC_CFG_CMDMAX	DMC command counting maximum threshold register	4-110
0x270	DDRC_CFG_PERF	DDRC performance statistics mode register	4-111
0x274	DDRC_CFG_STAID	DDRC performance statistics command ID register	4-112
0x278	DDRC_CFG_STAIDMSK	DDR performance statistics command ID mask register	4-112
0x280	DDRC_INTMSK	DDRC interrupt mask register	4-113
0x284	DDRC_RINT	DDRC raw interrupt register	4-114
0x288	DDRC_INTSTS	DDRC interrupt status register	4-115
0x290	DDRC_CURR_STATUS	DDRC status register	4-116
0x294	DDRC_CURR_FUNC	DDRC FUNC module status register	4-117
0x298	DDRC_CURR_FUNC2	DDRC FUNC2 module status register	4-118
0x2A0	DDRC_CURR_EXECST	DDRC command state machine status register	4-118
0x2A4	DDRC_CURR_WGFIFOST	DDRC write data FIFO status register	4-119

Offset Address	Register	Description	Page
0x380	DDRC_HIS_FLUX_WR	DDRC all write command traffic statistics register	4-119
0x384	DDRC_HIS_FLUX_RD	DDRC all read command traffic statistics register	4-120
0x388	DDRC_HIS_FLUX_WCMD	DDRC all write command count register	4-120
0x38C	DDRC_HIS_FLUX_RCMD	DDRC all read command count register	4-121
0x390	DDRC_HIS_FLUXID_WR	DDRC specified ID write traffic statistics registers	4-121
0x394	DDRC_HIS_FLUXID_RD	DDRC specified ID read traffic statistics registers	4-122
0x0398	DDRC_HIS_FLUXID_WCMD	DDRC all ID write command count register	4-122
0x039C	DDRC_HIS_FLUXID_RCMD	DDRC all ID read command count register	4-123
0x3A0	DDRC_HIS_WLATCNT0	DDRC specified ID write command latency statistics register 0	4-123
0x3A4	DDRC_HIS_WLATCNT1	DDRC specified ID write command latency statistics register 1	4-124
0x3A8	DDRC_HIS_RLATCNT0	DDRC specified ID read command latency statistics register 0	4-124
0x3AC	DDRC_HIS_RLATCNT1	DDRC specified ID read command latency statistics register 1	4-125
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	Read channel inherent latency register	4-125
0x3B4	DDRC_STAT_RPT	Read pointer to the DMC accumulated command count register	4-126
0x3B8	DDRC_HIS_CMD_SUM	DMC accumulated command count register	4-126
0x3BC	DDRC_HIS_DAT_SUM	DMC accumulated data count register	4-126
0x4A8	DDRC_HIS_SFC_RDATA0	Software configuration read data register 0	4-127

Offset Address	Register	Description	Page
0x4AC	DDRC_HIS_SFC_RDATA1	Software configuration read data register 1	4-127
0x4B0	DDRC_HIS_SFC_RDATA2	Software configuration read data register 2	4-128
0x4B4	DDRC_HIS_SFC_RDATA3	Software configuration read data register 3	4-128

4.1.7.2 Register Description

DDRC_CTRL_SREF

DDRC_CTRL_SREF is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_CTRL_SREF	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								sref_done	sref_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	sref_done	DDR PHY self-refresh done 0: normal operating mode 1: The transition from 0 to 1 indicates that the DDR PHY completes all required operations after exiting the self-refresh status and the DMC can accept new requests.
[0]	RW	sref_req	SDRAM self-refresh request 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_CTRL_SFC

DDRC_CTRL_SFC is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x00C	DDRC_CTRL_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC 0: The command is not executed or the parameter is automatically cleared after the command is executed. 1: The command is requested to be executed.

DDRC_CTRL_PERF

DDRC_CTRL_PERF is a DDRC performance statistics enable register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL_PERF	0x0014_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															perf_en
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	perf_en	Performance statistics mode 0: disabled 1: enabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When perf_mode is 1, this bit is automatically cleared after counting is complete.

DDRC_CFG_SREF

DDRC_CFG_SREF is a DDRC self-refresh configuration register.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CFG_SREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asref_en																sref_arefnum				reserved			clk_switch	reserved			sref_odis	reserved			asref_fast_wakeup	sref_cc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	asref_en	SDRAM automatic self-refresh enable 0: disabled 1: enabled **NOTE** Each rank corresponds to one control bit. The rank automatically enters the self-refresh status only when DDRC_CFG_PD[PD_EN] and the asref_en corresponding to the rank are valid. This function is not supported in this version.
[15:12]	RW	sref_arefnum	Number of self-refresh operations initiated after DDR3/DDR4 SDRAM exits the self-refresh status during the DFS process 0x0: No self-refresh operation is initiated. 0x1–0xF: *n*
[11:9]	RO	reserved	Reserved
[8]	RW	clk_switch	DDRC low-power clock switch. Whether to back press AXI interface command when the DDRC enters the low-power status (DDR self-refresh) 0: The interface commands are not back pressed, and an error is returned directly. 1: The interface commands are back pressed, and the original command is executed after the clock is switched.
[7:5]	RO	reserved	Reserved
[4]	RW	sref_odis	Output disable for the DDR command and data I/O in self-refresh mode 0: enabled 1: disabled **NOTE** The configuration is a static configuration. It is recommended that this bit be set to 1 to disable the output of the DDR command and data I/O after the DDR enters the self-refresh status. It is recommended that this bit be set to 0 to enable the output of the DDR command and data I/O before

			the DDR exits the self-refresh status.
[3:2]	RO	reserved	Reserved
[1]	RW	asref_fast_wakeup	AUTO SELFREFRESH 快速唤醒使能。 0: enabled 1: disabled
[0]	RW	sref_cc	SDRAM clock control in self-refresh mode 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled.

DDRC_CFG_INIT

DDRC_CFG_INIT is a DDR initialization configuration register.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CFG_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								init_arefnum							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	init_arefnum	Number of auto-refresh operations when the DDR3/DDR4 SDRAM is being initialized 0x0–0x2: two 0x3–0xF: *n*

DDRC_CFG_PD

DDRC_CFG_PD is a DDR power-down status register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CFG_PD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asref_prd												t_clk_cke				pd_prd												reserved	pd_cc	pd_ac	pd_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	asref_prd	SDRAM self-refresh cycle. When the DDRC does not receive any command in consecutive asref_prd cycles, it forces the SDRAM to enter the self-refresh status. When a command is received, the DDRC forces the SDRAM to exit the self-refresh status. 0x0−0xFFF: (n x 16) clock cycles **NOTE** This field is valid only when asref_en is 1.
[19:16]	RW	t_clk_cke	Relationship between CLK and CKE 0x0−0x7: Delay relative to CKE when the DDR PHY disables the DDR3/DDR4 clock. The delay is related to the DDR PHY. **NOTE** This field can be set to 0 when the clock is disabled.
[15:4]	RW	pd_prd	SDRAM power-down cycle. When the DDRC does not receive any command in consecutive pd_prd cycles, it forces the SDRAM to enter the power-down status. When a command is received, the DDRC forces the SDRAM to exit the power-down status. 0x00: not enter the power-down status 0x01−0xFFF: *n* clock cycles **NOTE** This field is valid only when pd_en is 1.
[3]	RO	reserved	Reserved
[2]	RW	pd_cc	SDRAM clock control in power-down mode 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled. **NOTE** This function cannot be used in DDR3/DDR4 mode.
[1]	RW	pd_ac	SDRAM address command dynamic disable in power-down mode 0: enable the pin output 1: disable the pin output **NOTE** This field is valid when pd_en is enabled. The control pins do not include CKE, ODT, CSN, and RESET_N.

[0]	RW	pd_en	Automatic power-down enable for the SDRAM 1: enabled 0: disabled

DDRC_CFG_AREF

DDRC_CFG_AREF is a DDRC auto-refresh mode register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_CFG_AREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aref_alarm_num								reserved	pstpnd_level		aref_alarm_en	aref_dual_rank	aref_opt	aref_mode		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	aref_alarm_num	The auto-refresh command is forced to be transmitted if a specific number of auto-refresh commands cannot be transmitted. 0x0–0xFF: lack of (*n* + 1) auto-refresh commands **NOTE** Only one auto-refresh command is considered when *n* is 255 because the upper bits are lost after the bits of the 8-bit counter are carried. In optimization mode (when aref_opt is 1), an alarm is generated when the number of postponed commands is greater than or equal to 15.
[7]	RO	reserved	Reserved
[6:5]	RW	pstpnd_level	Threshold for the number of postponed commands in optimized auto-refresh mode 11: 8 10: 4 01: 2 00: 1
[4]	RW	aref_alarm_en	Auto-refresh loss alarm enable (AREF function) 0: disabled 1: enabled

[3]	RW	aref_dual_rank	REF command transmit mode select 0: The REF commands are transmitted to only one rank each time. 1: The REF commands are transmitted to two ranks each time.
[2]	RW	aref_opt	Auto-refresh optimization enable 0: disabled 1: enabled When this function is enabled, it is recommended that aref_mode be set to 00. The DMC dynamically detects whether the DDR is idle during each auto-refresh. If the DDR is idle, the AREF commands are transmitted; otherwise, the DMC waits until nine AREF cycles are reached. Then the DMC forcibly terminates the DDR access and inserts AREF commands.
[1:0]	RW	aref_mode	Auto-refresh mode 00: An auto-refresh operation is performed every one tREFI cycle. 01: Three auto-refresh operations are performed every three tREFI cycles. 10: Four auto-refresh operations are performed every five tREFI cycles. 11: Eight auto-refresh operations are performed every nine tREFI cycles. Optimized auto-refresh mode 00: The maximum number of postponed commands is 1. 01: The maximum number of postponed commands is 2. 10: The maximum number of postponed commands is 4. 11: The maximum number of postponed commands is 8.

DDRC_CFG_WORKMODE

DDRC_CFG_WORKMODE is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_CFG_WORKMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		hdr_mode	read_mode	addr_mode		intlv_en	wrap_en	reserved				apre_en	func_clkon	data_clkon	cmd_clkon	clk_ratio
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved

[13]	RW	hdr_mode	DFI interface mode select 0: SDR mode 1: HDR mode The Hi3519 V100 supports only the HDR mode.
[12]	RW	read_mode	DDRC read mode 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC.
[11:10]	RW	addr_mode	DDR address line reverse mode select 00: The address is set to all 1s when the DDR is idle. 01: The status of the previous command is retained when the DDR is idle. 10: The status opposite to the previous status is restored when the DDR is idle. 11: reserved
[9]	RW	intlv_en	DMC burst interleave enable 0: disabled 1: enabled In DDR4 mode, the performance is best when this field is set to 1. In other modes, it is recommended that this field be set to 0.
[8]	RW	wrap_en	Wrap command optimization enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	apre_en	Auto-precharge enable 0: disabled 1: enabled
[3]	RW	func_clkon	Functional module clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[2]	RW	data_clkon	Data channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[1]	RW	cmd_clkon	Command channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.

[0]	RW	clk_ratio	Operating mode of the DDRC 0: The ratio of the DDRC frequency to the PHY frequency is 1:1. 1: The ratio of the frequency of the DDRC to the frequency of the PHY is 1:2. **NOTE** This field is fixed at 1 in this version.

DDRC_CFG_WORKMODE2

DDRC_CFG_WORKMODE2 is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x044	DDRC_CFG_WORKMODE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				openpage_time												rank_disable															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:16]	RW	openpage_time	Open page delay control 0x0−0x1: The open page function is disabled. 0x2−0x3fff: open page delay **NOTE** The open page function is disabled when DDRC_CFG_WORKMODE[apre_en] is enabled.
[15:0]	RW	rank_disable	Rank disable 0: normal operating mode 1: The auto-refresh/power-down/self-refresh function of a rank is disabled.

DDRC_CFG_DDRMODE

DDRC_CFG_DDRMODE is a DDR operating mode register.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_CFG_DDRMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		bank_mode		reserved		bank_xor		asref_zqc_en	sref_zqc_en	rank		rank_mode		odt_on	zqc_en	reserved		scramb_en	dbi_en	bc_en		cmd_2t_en	rd_2t_pre	wr_2t_pre	brstlen	brstlen2	reserved		mem_width		dram_type	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	bank_mode	Bank interleaving mode For 8-bit bus width: 000: 8-byte banks are interleaved. 001: 16-byte banks are interleaved. … 111: 1 KB banks are interleaved. For 16-bit bus width: 000: 16-byte banks are interleaved. 001: 32-byte banks are interleaved. … 111: 2 KB banks are interleaved. For 32-bit bus width: 000: 32-byte banks are interleaved. 001: 64-byte banks are interleaved. … 111: 4 KB banks are interleaved. For 64-bit bus width: 000: 64-byte banks are interleaved. 001: 128-byte banks are interleaved. … 111: 8 KB banks are interleaved. **NOTE** When the AXI is set to a non-zero value, this field must be set to 000 and the AXI configuration mode is used. When the AXI is set to 000, the DMC configuration mode is used.
[27:26]	RO	reserved	Reserved

[25:24]	RW	bank_xor	Scrambling enable for the bank address and row address 0: disabled 1: The bank address and offset address 0 are scrambled. 2: The bank address and offset address 1 are scrambled. 3: The bank address and offset address 2 are scrambled.
[23]	RW	asref_zqc_en	SDRAM ZQ enable when the ASREF exits. 0: disabled 1: enabled
[22]	RW	sref_zqc_en	SDRAM ZQ enable when the SREF exits. 0: disabled 1: enabled NOTE • This field is valid only for the DDR4/DDR3 SDRAM and is set to 0 by default. • In addition, the value of this field cannot be dynamically changed during the self-refresh exit process.
[21:20]	RW	rank	Number of DDRC ranks 00: 1 01: 2 10: 3 11: 4 NOTE When the number of external DDR ranks is greater than 4, this field is used to control four groups of ranks (0−3, 4−7, 8−11, and 12−16).
[19:18]	RW	rank_mode	Rank interleaving mode 00: single rank mode 01: single rank mode 10: Two ranks are interleaved. 11: Four ranks are interleaved. NOTE Multiple ranks can be interleaved only when the configuration of these ranks is the same; otherwise, unpredictable errors may occur.
[17]	RW	odt_on	Whether the ODT signal output to the SDRAM is fixed 0: The signal is automatically controlled by the DDRC. 1: The output is fixed at the wodt configuration of rank 0.
[16]	RW	zqc_en	AREF ZQ command enable 0: disabled 1: enabled
[15]	RO	reserved	Reserved

[14]	RW	scramb_en	Data scrambling enable (The scrambling code is generated by using the address, and exclusive ORed with the data to reduce synchronous inversion). 0: disabled 1: enabled
[13]	RW	dbi_en	DDR4 DBI enable 0: disabled 1: enabled
[12]	RW	bc_en	DDR3 burst chop mode 0: disabled 1: enabled
[11]	RO	reserved	Reserved. This bit must be fixed at 1'b0.
[10]	RW	rd_2t_pre	DDR4 read 2T preamble enable 0: disabled 1: enabled
[9]	RW	wr_2t_pre	DDR4 write 2T preamble enable 0: disabled 1: enabled
[8]	RW	brstlen	Burst length of the DDRC When brstlen2 is set to 0: 0: BL4 1: BL8 When brstlen2 is set to 1: 0: BL16 1: BL32 The burst length of the DDR3/DDR4 SDRAM can be set to only burst 8. **NOTE** The burst length is related to the clock ratio of the DMC to the PHY. The burst length is BLx/n (x indicates the burst type, that is, 4, 8, 16, or 32. n indicates that the clock ratio of the DMC to the PHY is 1:n). For example, when the clock ratio is 1:2, to set the DDRC burst length to BL32, set brstlen to 0 and brstlen2 to 1.
[7:5]	RO	reserved	Reserved
[4]	RW	apre_en	Auto precharge function enable 0: disabled 1: enabled
[7]	RW	brstlen2	Burst length 2 of the DDRC 0: basic mode 1: extended mode This field works with brstlen.

[6]	RO	reserved	Reserved
[5:4]	RW	mem_width	Bit width of the storage data bus 00: 8 bits 01: 16 bits 10: 32 bits 11: 64 bits
[3:0]	RW	dram_type	External memory type 110: DDR3 111: DDR4 Other values: reserved

DDRC_CFG_SCRAMB

DDRC_CFG_SCRAMB is a DDR data scrambling configuration register.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_CFG_SCRAMB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dbi_low_act	rd_dbi_en	wr_dbi_en	reserved											scramb_seed_type	reserved			scramb_seed_sort			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	dbi_low_act	DBI active level 0: active high 1: active low
[17]	RW	rd_dbi_en	Read DBI enable 0: disabled 1: enabled
[16]	RW	wr_dbi_en	Read DBI enable 0: disabled 1: enabled
[15:5]	RO	reserved	Reserved

[4]	RW	scramb_seed_type	Address mode for scrambling 0: Use the CS and BA for scrambling. 1: Use the CS, BA, and low bits of the row address for scrambling.
[3]	RO	reserved	Reserved
[2:0]	RW	scramb_seed_sort	Address arrangement mode for scrambling 000: CS_BA_COL arrangement 001: CS_COL_BA arrangement 010: COL_CS_BA arrangement 011: COL_BA_CS arrangement 100: BA_CS_COL arrangement 101: BA_COL_CS arrangement Other values: reserved

DDRC_CFG_RNKVOL

DDRC_CFG_RNKVOL is a DDRC-controlled DDR capacity configuration register.

Offset Address	Register Name	Total Reset Value
0x060 + 0x4 x *rnks* (*rnks* = 0)	DDRC_CFG_RNKVOL	0x0000_0022

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															mem_x4	reserved			mem_map	mem_bankgroup			mem_bank	reserved			mem_row	reserved			mem_col
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	mem_x4	4-bit external component combination mode 0: 8-/16-/32-bit external components are combined. 1: 4-bit external components are combined.
[15:14]	RO	reserved	Reserved

[13:12]	RW	mem_map	Address translation mode of the SDRAM 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW}= AXI_Address 10: {Rank, Row, Ba, Col, cs, Col, DW}= AXI_Address 11: {Rank, Ba, Row, Col, cs, Col, DW}= AXI_Address This parameter can be set to 10 or 11 only when DDRC_CONFIG1[dual_ch] is valid. When there are multiple ranks, the configuration must be the same for each rank. This field must be set to 00 in the current version.
[11:10]	RW	mem_bankgroup	Number of bank groups in a single SDRAM 00: 1 bank group 01: 2 bank groups 10: 4 bank groups 11: reserved NOTE This field is valid only in DDR4 mode.
[9:8]	RW	mem_bank	Number of banks of a single SDRAM 00: 4 banks 01: 8 banks 10:16 banks 11: reserved
[7]	RO	reserved	Reserved
[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits 101: 16 bits Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits Other values: reserved

DDRC_CFG_ODT

DDRC_CFG_ODT is a DDR ODT configuration register.

Offset Address	Register Name	Total Reset Value
0x0A0 + 0x4 x *rnks* (*rnks* = 0)	DDRC_CFG_ODT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rodt																wodt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rodt	ODT read enable for other RANKs when the current RANK transmits the read command 0: disabled 1: enabled
[15:0]	RW	wodt	ODT write enable for other RANKs when the current RANK transmits the write command 0: disabled 1: enabled

DDRC_CFG_EMRS01

DDRC_CFG_EMRS01 is a configuration register for DDR mode register 0 and mode register 1.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_CFG_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDR3/DDR4 SDRAM extended mode register 1 This field corresponds to valid bits 13−0 of mode register 1 (MR1) in the DDR3/DDR4 SDRAM manual. MR1[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS01 bit[31:30] are reserved and set to 2'b00. For details about MR1, see the DDR3/DDR4 SDRAM manual.
[15:0]	RW	mrs	DDR3/DDR4 SDRAM mode register This field corresponds to valid bits 13−0 of mode register 0 (MR0) in the DDR3/DDR4 SDRAM manual. MR0[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS01 bit[15:14] are

			reserved and set to 2'b00. For details about MR0, see the DDR3/DDR4 SDRAM manual.

DDRC_CFG_EMRS23

DDRC_CFG_EMRS23 is a configuration register for DDR mode register 2 and mode register 3.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_CFG_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDR3/DDR4 SDRAM extended mode register 3 This field corresponds to valid bits 13−0 of mode register 3 (MR3) in the DDR3/DDR4 SDRAM manual. MR3[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS23 bit[31:30] are reserved and set to 2'b00. For details about MR3, see the DDR3/DDR4 SDRAM manual.
[15:0]	RW	emrs2	DDR3/DDR4 SDRAM extended mode register 2 This field corresponds to valid bits 13−0 of mode register 2 (MR2) in the DDR3/DDR4 SDRAM manual. MR2[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS23 bit[15:14] are reserved and set to 2'b00. For details about MR2, see the DDR3/DDR4 SDRAM manual.

DDRC_CFG_EMRS45

DDRC_CFG_EMRS45 is a configuration register for DDR mode register 4 and mode register 5.

Offset Address	Register Name	Total Reset Value
0x0F8	DDRC_CFG_EMRS45	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs5																emrs4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs5	DDR4 SDRAM extended mode register 5 This field corresponds to valid bits 13−0 of mode register 5 (MR5) in the DDR4 SDRAM manual. MR5[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS45 bit[31:30] are reserved and set to 2'b00. For details about MR5, see the DDR4 SDRAM manual.
[15:0]	RW	emrs4	DDR4 SDRAM extended mode register 4 This field corresponds to valid bits 13−0 of mode register 4 (MR4) in the DDR4 SDRAM manual. MR4[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS45 bit[15:14] are reserved and set to 2'b00. For details about MR4, see the DDR4 SDRAM manual.

DDRC_CFG_EMRS67

DDRC_CFG_EMRS67 is a configuration register for DDR mode register 6 and mode register 7.

Offset Address	Register Name	Total Reset Value
0x0FC	DDRC_CFG_EMRS67	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs7																emrs6															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs7	DDR4 SDRAM extended mode register 7 This field corresponds to valid bits 13−0 of mode register 7 (MR7) in the DDR4 SDRAM manual. MR7[15:14] of most DDRs are not used. DDRC_CFG_EMRS67 bit[31:30] are reserved and set to 2'b00. For details about MR7, see the DDR4 SDRAM manual.
[15:0]	RW	emrs6	DDR4 SDRAM extended mode register 6 This field corresponds to valid bits 13−0 of mode register 6 (MR6) in the DDR4 SDRAM manual. MR6[15:14] of most DDR SDRAMs are not used. DDRC_CFG_EMRS67 bit[15:14] are reserved and set to 2'b00. For details about MR6, see the DDR4 SDRAM manual.

DDRC_CFG_TIMING0

DDRC_CFG_TIMING0 is DDRC timing parameter register 0.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_CFG_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved	tras	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the load mode register (LMR) command. The value is tMRD for the DDR3 and DDR4. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command 0x0–0x3: 3 clock cycles 0x4–0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command 0x00–0x01: 1 clock cycle 0x02–0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved
[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles Others: Reserved.

DDRC_CFG_TIMING1

DDRC_CFG_TIMING1 is DDRC timing parameter register 1.

Offset Address	Register Name	Total Reset Value
0x084	DDRC_CFG_TIMING1	0xFF22_15FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1 0
Name	tsre		trtw	twl	tcl		reserved		trfc	
Reset	1 1 1 1	1 1 1 1	0 0 1 0	0 0 1 0	0 0 0 1	0 1	0	1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command 0x0: reserved 0x01–0xFF: (*n* x 4) clock cycles This field is set to the larger value between tXSDLL and tXS for the DDR3/DDR4 SDRAM.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command 0x0–0x1: 1 clock cycle 0x2–0xF: (*n* + 1) clock cycles **NOTE** In DDR4/DDR3 mode, the field value depends on the latency of the board, package, and I/O.
[19:15]	RW	twl	Number of wait cycles from the write command to the write data command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles. **NOTE** The clock cycle is the DDR3/DDR4 clock cycle.
[14:10]	RW	tcl	Column address strobe (CAS) latency from the read command to the read data operation 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles **NOTE** The clock cycle is the DDR3/DDR4 clock cycle.
[9]	RO	reserved	Reserved

[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00: reserved 0x01–0x1FF: *n* clock cycles

DDRC_CFG_TIMING2

DDRC_CFG_TIMING2 is DDRC timing parameter register 2.

Offset Address	Register Name	Total Reset Value
0x108	DDRC_CFG_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved				tfaw								reserved				taref							
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the self-refresh mode 0x0: reserved 0x1–0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last write data to the write-to-read command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands 0x00–0x3F: *n* clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved

[10:0]	RW	taref	Number of auto-refresh cycles 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x *n*) clock cycles. For example, 0x008 indicates 128 (16 x 8) clock cycles. The interval tREFI is 7800/16/tclk. Tclk is twice the running cycle of the SDRAM.

DDRC_CFG_TIMING3

DDRC_CFG_TIMING3 is DDRC timing parameter register 3.

Offset Address	Register Name	Total Reset Value
0x10C	DDRC_CFG_TIMING3	0xFFFF_E0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles 0x000: The ZQCS command is forbidden. 0x001–0x3FF: (*n* x 128) AREF cycles The number of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:13]	RW	tzqinit	Number of ZQ initialization delay cycles 0x0–0x1FF: (n x 4) clock cycles The value needs to be set to the larger value between tZQINIT and tDLLK.
[12:8]	RW	taond	Number of ODT enable/disable cycles In DDR3/DDR4 mode, this value is set to tWL – 2 (tWL is DDRC_CFG_TIMING1[twl]).
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode 0x0–0xF: n clock cycles (in decimal) For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3/DDR4 mode, the field value is the larger value between tXP and tCKE.
[3:0]	RW	trtp	Wait delay from the read command to the disable command 0x0–0x2: 2 clock cycles 0x3–0xF: *n* clock cycles

			Trtp is calculated as follows: Trtp = AL + BL/2 + Max (trtp, 2) – 2

DDRC_CFG_TIMING4

DDRC_CFG_TIMING4 is DDRC timing parameter register 4.

Offset Address	Register Name	Total Reset Value
0x110	DDRC_CFG_TIMING4	0x01FF_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tmod				twlo				reserved															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:20]	RW	tmod	Delay from the MRS command to ODT and ZQCL validity 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles
[19:0]	RO	reserved	Reserved

DDRC_CFG_TIMING5

DDRC_CFG_TIMING5 is DDRC timing parameter register 5.

Offset Address	Register Name	Total Reset Value
0x114	DDRC_CFG_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tdqsckmax				reserved	tdqsck			reserved				tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:24]	RW	tdqsckmax	Maximum output access time of DQS relative to CK. This field can be ignored in DDR3/DDR4 mode.
[23]	RO	reserved	Reserved

[22:20]	RW	tdqsck	Output access time of DQS relative to CK. This field can be ignored and retains the default value in DDR3/DDR4 mode.
[19:16]	RO	reserved	Reserved
[15:8]	RW	tzqcs	ZQCS calibration delay cycle 0x0−0xFF: (*n* x 2) clock cycles The field value must be greater than or equal to 10 because of the DMC design.
[7:5]	RO	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery 0x0−0x1: one clock cycle 0x2−0x1F: *n* clock cycles **NOTE** When the DFS is required, tWR must be set based on the highest chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_TIMING6

DDRC_CFG_TIMING6 is DDRC timing parameter register 6.

Offset Address	Register Name	Total Reset Value
0x118	DDRC_CFG_TIMING6	0x0000_00FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		trrd_l	twtr_l	tccd_l	todt_sft	tcksrx	tcksre
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	trrd_l	Number of trrd wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[19:16]	RW	twtr_l	Number of twtr wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[15:12]	RW	tccd_l	Number of tccd wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[11:8]	RO	reserved	Reserved

[7:4]	RW	tcksrx	tCKSRX for the DDR3 or DDR4. Number of advanced valid beats before the DDR exits the self-refresh status. 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[3:0]	RW	tcksre	tCKSRE for the DDR3 or DDR4. Number of beats to be retained after the DDR enters the self-refresh status. 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles

DDRC_CFG_TIMING7

DDRC_CFG_TIMING7 is DDRC timing parameter register 7.

Offset Address	Register Name	Total Reset Value
0x11c	DDRC_CFG_TIMING7	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		dim_trtr	dim_twtw	rnk_trtr	rnk_twtw	rnk_trtw	rnk_twtr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	dimm_trtr	Extra delay of read-to-read switching between DIMMs based on rnk_trtr, for matching the maximum skew between DIMMs
[19:16]	RW	dimm_twtw	Extra delay of write-to-write switching between DIMMs based on rnk_twtw, for matching the maximum skew between DIMMs
[15:12]	RW	rnk_trtr	Read-to-read delay between ranks
[11:8]	RW	rnk_twtw	Write-to-write delay between ranks
[7:4]	RW	rnk_trtw	Read-to-write delay between ranks
[3:0]	RW	rnk_twtr	Write-to-read delay between ranks

DDRC_CFG_BLDATA

DDRC_CFG_BLDATA is a DDRC pre-received write data configuration register.

Offset Address	Register Name	Total Reset Value
0x140	DDRC_CFG_BLDATA	0x0000_0002

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							bl_data

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	bl_data	Number of DMC data segments corresponding to each DDR command in the current mode 0x0–0xF: *n* data segments

DDRC_CFG_DMCLVL

DDRC_CFG_DMCLVL is a DDRC command queue depth threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x144	DDRC_CFG_DMCLVL	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				mbist_que_level				reserved				que_level			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	mbist_que_level	Number of command buffers started by the DMC when the MTEST or MCLR function is used 0x0: 1 0x1−0x10: 1−16. The maximum value is related to the code.
[7:5]	RO	reserved	Reserved
[4:0]	RW	que_level	Depth of the command register FIFO in the DMC 0x1−0x10: depth of *n* commands Other values: reserved

DDRC_CFG_DDRPHY

DDRC_CFG_DDRPHY is a DDR I/O configuration register.

Offset Address	Register Name	Total Reset Value
0x200	DDRC_CFG_DDRPHY	0x001F_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wr_busy_dly				reserved			phy_upden	trdlat				reserved			phy_zqen	reserved			rcv_pdr
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RW	wr_busy_dly	Gating enable for the data beat in the PHY The value of this field must be greater than (WL + 2). This field can be set to 0x1F in scenarios that do not have high requirements on power consumption.
[15:13]	RO	reserved	Reserved
[12]	RW	phy_upden	Enable of the DDRC response to dfi_phyupd_en of the DDR PHY 0: disabled 1: enabled
[11:8]	RW	trdlat	Inherent delay of the DDR PHY 0x0−0xF: (n + 1) clock cycles This field needs to be set to 8 when synopsys3/2phy is used.
[7:0]	RO	reserved	Reserved

DDRC_CFG_SFC_TIM

DDRC_CFG_SFC_TIM is a DDRC software DDR configuration command timing register.

Offset Address	Register Name	Total Reset Value
0x20C	DDRC_CFG_SFC_TIM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wait_time															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	wait_time	Wait period after the DDR command configured by the SFC is executed. This field is valid only when DDRC_CFG_SFC[wait_en] is 1.

DDRC_CFG_SFC

DDRC_CFG_SFC is a DDRC software DDR command attribute register.

Offset Address	Register Name	Total Reset Value
0x210	DDRC_CFG_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wait_en	pre_dis	cmd_mrs																		reserved								cmd_type			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wait_en	Enable for exiting a period after the command execution is complete 0: disabled 1: enabled The wait period is configured in DDRC_CFG_SFC_TIM.
[30]	RW	pre_dis	Precharge command transmit disable 0: The precharge command is transmitted before the SFC command. 1: The precharge command is not transmitted before the SFC command, and the corresponding command is transmitted directly.
[29:12]	RW	cmd_mrs	Value of the DDR mode register when the LMR command is configured. This field is used to select a beat as the valid data during the RDMRS or RD operation.
[11:4]	RO	reserved	Reserved

[3:0]	RW	cmd_type	DDR command configuration 0000: enter the deep power-down status 0001: exit the deep power down mode 0010: LMR command 0011: ZQCL command. 0100: write command 0101: read command 0110: precharge all command 0111: read MRS command 1000: AREF command 1001: enter the self-refresh status 1010: exit the self-refresh status 1011: DDR4 PDA command. The data scrambling function must be disabled during the transmission of this command. 1111: DFI_CTRL_UPD_REQ/DFI_CTRL_UPD_ACK handshake for requesting the PHY to enter the refresh mode (this operation is not supported in this version)

DDRC_CFG_SFC_ADDR0

DDRC_CFG_SFC_ADDR0 is read/write memory address register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x214	DDRC_CFG_SFC_ADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfc_row																				sfc_col											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	sfc_row	Row address for the memory that is read or written by the software configuration module The maximum address bit width is related to the specifications of the connected component.
[11:0]	RW	sfc_col	Column address for the memory that is read or written by the software configuration module **NOTE** The DDRC access address must be aligned based on the current DMC bit width. For example, if the current DMC bit width is 128 bits: When the 64-/72-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:1], 1'b0}. When the 32-/36-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:2]0.2'b0}.

DDRC_CFG_SFC_ADDR1

DDRC_CFG_SFC_ADDR1 is read/write memory address register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x218	DDRC_CFG_SFC_ADDR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfc_rank																reserved												sfc_bank			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sfc_rank	ddr_rank for executing commands 0: not execute 1: execute **NOTE** Note: Each bit controls a rank. For the DDR4 SDRAM, the bank group is selected based on sfc_rank. The bank group varies according to the bank. Therefore, the write mode register or write command cannot be sent to multiple ranks at the same time, and can be sent to only one rank at a time.
[15:4]	RO	reserved	Reserved
[3:0]	RW	sfc_bank	Bank address for the memory that is read or written by the software configuration module **NOTE** For the DDR4 SDRAM, the lower bits indicate the bank group. For example, for the component with four bank groups, sfc_bank[1:0] indicate the bank group; for the component with two bank groups, sfc_bank[0] indicates the bank group.

DDRC_CFG_SFC_WDATA0

DDRC_CFG_SFC_WDATA0 is write data configuration register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x21C	DDRC_CFG_SFC_WDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata0	Bits 31−0 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA1

DDRC_CFG_SFC_WDATA1 is write data configuration register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x220	DDRC_CFG_SFC_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata1	Bits 63−32 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA2

DDRC_CFG_SFC_WDATA2 is write data configuration register 2 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x224	DDRC_CFG_SFC_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata2	Bits 95−64 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA3

DDRC_CFG_SFC_WDATA3 is write data configuration register 3 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x228	DDRC_CFG_SFC_WDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata3																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata3	Bits 127−96 of the written data of the software configuration module

DDRC_CFG_STADAT

DDRC_CFG_ STADAT is a DDRC data statistics control register.

Offset Address	Register Name	Total Reset Value
0x254	DDRC_CFG_ STADAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	dat_stat_en	dat_stat_mode	dat_stat_prd																												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	dat_stat_en	DDR data statistics enable 0: disabled 1: enabled **NOTE** When dat_stat _mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When dat_stat _mode is 1, this bit is automatically cleared after the counting is complete.
[29:28]	RW	dat_stat_mode	Data statistical mode 2'b00: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 2'b01: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. When the statistical period is reached, an interrupt is reported. 2'b10: threshold-based trigger mode. When the statistical period is reached, if the counting value is within the threshold, no interrupt is reported. In this case, a counting is started again until the counting value exceeds the threshold. Then an interrupt is reported and the counting stops. Others: Reserved **NOTE** When dat_stat_mode is set to 2'b01 or 2'b10, the statistical result retains after an overflow occurs. When dat_stat_mode is set to 2'b00, the statistical

			value is wrapped after an overflow occurs.
[27:0]	RW	dat_stat_prd	Data statistical period 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical period The actual statistical period is (load_stat_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This configuration is valid only when load_stat_mode is 2'b01 or 2'b10. When load_stat_mode is 0, counters related to performance statistics keep counting.

DDRC_CFG_DATMIN

DDRC_CFG_DATMIN is a DMC data counting minimum threshold register.

Offset Address	Register Name	Total Reset Value
0x258	DDRC_CFG_ DATMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_dat_min																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dmc_dat_min	Minimum threshold for data statistics. When the data statistical value is less than or equal to this threshold, an interrupt is reported. **NOTE** The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_DATMAX

DDRC_CFG_DATMAX is a DMC data counting maximum threshold register.

Offset Address	Register Name	Total Reset Value
0x25c	DDRC_CFG_ DATMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_dat_max																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:0]	RW	dmc_dat_max	Maximum threshold for data statistics. When the data statistical value is greater than or equal to this threshold, an interrupt is reported. **NOTE** The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_STACMD

DDRC_CFG_STACMD is a DDR performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_CFG_ STACMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		load_stat_en		Load_stat_mode				load_stat_prd																							
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	load_stat_en	DDR load statistics enable 0: disabled 1: enabled **NOTE** When dat_stat_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When load_stat_mode is 1, this bit is automatically cleared after the counting is complete.
[29:28]	RW	load_stat _mode	Load statistical mode 2'b00: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 2'b01: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. When the statistical period is reached, an interrupt is reported. 2'b10: threshold-based trigger mode. When the statistical period is reached, if the counting value is within the threshold, no interrupt is reported. In this case, a counting is started again until the counting value exceeds the threshold. Then an interrupt is reported and the counting stops. Others: Reserved **NOTE** If the load statistical result exceeds the maximum counting value, the

			statistical result is wrapped after an overflow occurs.
[27:0]	RW	load_stat_prd	Load statistical period 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical period The actual statistical cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This configuration is valid only when perf_mode is 1. When perf_mode is 0, counters related to performance statistics keep counting.

DDRC_CFG_CMDMIN

DDRC_CFG_CMDMIN is a DMC command counting minimum threshold register.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_CFG_ CMDMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	dmc_cmd_min						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dmc_cmd_min	Minimum threshold for command statistics. When the command statistical value is less than or equal to this threshold, an interrupt is reported. **NOTE** The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_CMDMAX

DDRC_CFG_CMDMAX is a DMC command counting maximum threshold register.

Offset Address	Register Name	Total Reset Value
0x268	DDRC_CFG_ CMDMAX	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	dmc_cmd_max						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:0]	RW	dmc_cmd_max	Maximum threshold for command statistics. When the command statistical value is greater than or equal to this threshold, an interrupt is reported. NOTE The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_PERF

DDRC_CFG_PERF is a DDRC performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x270	DDRC_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				flux_en	perf_mode	perf_prd																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	flux_en	DMC traffic monitoring enable 0: disabled 1: enabled When traffic monitoring is enabled, the statistics module provides the number of cycles occupied by the DDR interface by ID to each request port. The traffic can be controlled by using this field and the port traffic setting function.
[28]	RW	perf_mode	Performance statistical mode 0: continuous trigger mode. The performance counter continues to count. This ensures no overflow within 1s in continuous count mode. 1: single trigger mode. When the performance statistics time reaches perf_prd, the count value is retained and counting stops. NOTE The maximum statistical result retains after an overflow occurs.
[27:0]	RW	perf_prd	Performance statistics cycle 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical cycles The actual statistics cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC.

			NOTE This field is valid only when perf_mode is 1. When perf_mode is 0, the performance counter keeps on counting.

DDRC_CFG_STAID

DDRC_CFG_STAID is a DDRC performance statistics command ID register.

Offset Address	Register Name	Total Reset Value
0x274	DDRC_CFG_STAID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sta_id															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sta_id	Performance statistics by a specified ID. This field works with sta_idmask.

DDRC_CFG_STAIDMSK

DDRC_CFG_STAIDMSK is a DDR performance statistics command ID mask register.

Offset Address	Register Name	Total Reset Value
0x278	DDRC_CFG_STAIDMSK	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sta_idmask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sta_idmask	Specified ID mask The DDRC performance statistics register collects statistics only for specified ID commands. Cmd_id (ID of the command in the DDRC) & sta_idmask = sta_id

DDRC_INTMSK

DDRC_INTMSK is a DDRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rdtimeout_int_mask	reserved		stacmd_min_int_mask	reserved			sref_err_int_mask	reserved			flux_int_mask	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	aref_alarm_int_mask	DDR AREF command interrupt mask 0: enabled 1: masked
[15]	RO	reserved	Reserved
[14]	RW	stadat_max_int_mask	DDR data counting overflow interrupt mask 0: enabled 1: masked
[13]	RW	stadat_min_int_mask	DDR data counting period expire or underflow interrupt mask 0: enabled 1: masked
[12]	RW	rdtimeout_int_mask	DDR PHY read data timeout interrupt mask 0: enabled 1: masked
[11]	RO	reserved	Reserved
[10]	RW	stacmd_max_int_mask	DDR load counting overflow interrupt mask 1: masked 0: enabled
[9]	RW	stacmd_min_int_mask	DDR load counting period expire or underflow interrupt mask 0: enabled 1: masked
[8:6]	RO	reserved	Reserved

[5]	RW	sref_err_int_mask	Command interface access error interrupt mask in DDR self-refresh mode 0: enabled 1: masked
[4:2]	RO	reserved	Reserved
[1]	RW	flux_int_mask	DDR FLUX statistical period reach interrupt mask 0: enabled 1: masked
[0]	RO	reserved	Reserved

DDRC_RINT

DDRC_RINT is a DDRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_rint	reserved	stadat_max_rint	stadat_min_rint	rdtimeout_rint	reserved	stacmd_max_rint	stacmd_min_rint	reserved			sref_err_rint	reserved			flux_rint	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT_WC	aref_alarm_rint	DDR AREF command error raw interrupt. Writing 1 clears the interrupt.
[15]	RO	reserved	Reserved
[14]	INT_WC	stadat_max_rint	DDR data counting above the upper threshold interrupt. Writing 1 clears the interrupt.
[13]	INT_WC	stadat_min_rint	DDR data counting period expire or below the lower threshold interrupt. Writing 1 clears the interrupt.
[12]	INT_WC	rdtimeout_rint	DDR PHY read data timeout raw interrupt. Writing 1 clears the interrupt.
[11]	RO	reserved	Reserved
[10]	INT_WC	stacmd_max_rint	DDR load counting above the upper threshold interrupt. Writing 1 clears the interrupt.

[9]	INT_WC	stacmd_min_rint	DDR load counting period expire or below the lower threshold interrupt. Writing 1 clears the interrupt.
[8:6]	RO	reserved	Reserved
[5]	INT_WC	sref_err_rint	Self-refresh interface command access interrupt. Writing 1 clears the interrupt.
[4:2]	RO	reserved	Reserved
[1]	RW	flux_rint	DDR FLUX statistics period reach interrupt. Writing 1 clears the interrupt.
[0]	RO	reserved	Reserved

DDRC_INTSTS

DDRC_INTSTS is a DDRC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_intsts	reserved	stadat_max_intsts	stadat_min_intsts	rdtimeout_intsts	reserved	stacmd_max_intsts	stacmd_min_intsts	reserved			sref_err_intsts	reserved			flux_intsts	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT	aref_alarm_intsts	DDR AREF command error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RO	reserved	Reserved
[14]	INT	stadat_max_intsts	DDR data counting overflow interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[13]	INT	stadat_min_intsts	DDR data counting period expire or underflow interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[12]	INT	rdtimeout_intsts	DDR PHY read data timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	reserved	Reserved
[10]	INT	stacmd_max_intsts	DDR load counting overflow interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	INT	stacmd_min_intsts	DDR load counting period expire or underflow interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8:6]	RO	reserved	Reserved
[5]	INT	sref_err_intsts	Self-refresh interface command access interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4:2]	RO	reserved	Reserved
[1]	RW	flux_intsts	DDR FLUX statistics period reach interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	reserved	Reserved

DDRC_CURR_STATUS

DDRC_CURR_STATUS is a DDRC status register.

Offset Address	Register Name	Total Reset Value
0x290	DDRC_CURR_STATUS	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							busy_func	reserved			busy_dmc	reserved			busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved

[8]	RO	busy_func	Status of the DDRC FUNC module. This field is in the SREF status during reset. 0: idle 1: A command is being processed.
[7:5]	RO	reserved	Reserved
[4]	RO	busy_dmc	Status of the DDRC DMC 0: idle 1: A command is being processed.
[3:1]	RO	reserved	Reserved
[0]	RO	busy	Overall status of the DDRC 0: idle 1: A command is being processed.

DDRC_CURR_FUNC

DDRC_CURR_FUNC is a DDRC FUNC module status register.

Offset Address	Register Name	Total Reset Value
0x294	DDRC_CURR_FUNC	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	4	3	2	1	0
Name	reserved																			in_sfc	reserved			aref_opt_stat	reserved						in_sref
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	in_sfc	DDRC SFC status 0: idle 1: An SFC command is being processed.
[11:9]	RO	reserved	Reserved
[8]	RO	aref_opt_stat	Auto-refresh optimization mode status 0: The DDR exits the optimization mode 1: The DDR is in optimization mode. NOTE

			Before the DDR SDRAM enters the self-refresh status through configuration or requests over the csysreq interface, ensure that the DDR SDRAM exits the auto-refresh optimization mode. This is because some postponed commands may not be transmitted in self-refresh optimization mode.
[7:1]	RO	reserved	Reserved
[0]	RO	in_sref	DDR self-refresh status 0: normal 1: self-refresh.

DDRC_CURR_FUNC2

DDRC_CURR_FUNC2 is a DDRC FUNC2 module status register.

Offset Address	Register Name	Total Reset Value
0x298	DDRC_CURR_FUNC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	in_asref	DDRC automatic self-refresh status 0: normal status 1: automatic self-refresh status Each bit represents a rank.
[15:0]	RO	in_pd	DDRC power-down status 0: normal status 1: power-down status Each bit represents a rank.

DDRC_CURR_EXECST

DDRC_CURR_EXECST is a DDRC command state machine status register.

Offset Address	Register Name	Total Reset Value
0x2A0	DDRC_CURR_EXECST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	Controller command type 0: read command 1: write command
[15:0]	RO	dmc_cv	Controller command validity flag 0: invalid 1: valid

DDRC_CURR_WGFIFOST

DDRC_CURR_WGFIFOST is a DDRC write data FIFO status register.

Offset Address	Register Name	Total Reset Value
0x2A4	DDRC_CURR_WGFIFOST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wgntfifo_e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wgntfifo_e	WGNT_FIFO empty or full status. The empty status indicates that all written data is received, and the non-empty status indicates that the written data is not completely received. 0: not empty 1: empty

DDRC_HIS_FLUX_WR

DDRC_HIS_FLUX_WR is a DDRC all write command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x380	DDRC_HIS_FLUX_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr	Write traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RD

DDRC_HIS_FLUX_RD is a DDRC all read command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x384	DDRC_HIS_FLUX_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd	Read traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_WCMD

DDRC_HIS_FLUX_WCMD is a DDRC all write command count register.

Offset Address	Register Name	Total Reset Value
0x388	DDRC_HIS_FLUX_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr_cmd																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr_cmd	Write command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RCMD

DDRC_HIS_FLUX_RCMD is a DDRC all read command count register.

Offset Address	Register Name	Total Reset Value
0x38C	DDRC_HIS_FLUX_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd_cmd	Read command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WR

DDRC_HIS_FLUXID_WR is a DDRC specified ID write traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x390	DDRC_HIS_FLUXID_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr	Write traffic statistics of the master with the specified ID of

			the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** The unit is the DMC data bit width (128 bits).

DDRC_HIS_FLUXID_RD

DDRC_HIS_FLUXID_RD is a DDRC specified ID read traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x394	DDRC_HIS_FLUXID_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd	Read traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** The unit is the DMC data bit width (128 bits).

DDRC_HIS_FLUXID_WCMD

DDRC_HIS_FLUXID_WCMD is a DDRC all ID write command count register.

Offset Address	Register Name	Total Reset Value
0x0398	DDRC_HIS_FLUXID_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr_cmd																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr_cmd	Read traffic statistics of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RCMD

DDRC_HIS_FLUXID_RCMD is a DDRC all ID read command count register.

Offset Address	Register Name	Total Reset Value
0x039C	DDRC_HIS_FLUXID_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd_cmd	Read command count of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT0

DDRC_HIS_WLATCNT0 is DDRC specified ID write command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A0	DDRC_HIS_WLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_max																wlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wlatcnt_max	Maximum latency of the write command with the specified ID of

			the DDRC This field is cleared when the next statistics start.
[15:0]	RO	wlatcnt_min	Minimum latency of the write command with the specified ID of the DDRC. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT1

DDRC_HIS_WLATCNT1 is DDRC specified ID write command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3A4	DDRC_HIS_WLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	wlatcnt_all	Accumulated latency of the write command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the write command with the specified ID by dividing wlatcnt_all by fluxid_wr_cmd.

DDRC_HIS_RLATCNT0

DDRC_HIS_RLATCNT0 is a DDRC specified ID read command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A8	DDRC_HIS_RLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_max																rlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	rlatcnt_max	Maximum latency of the read command with the specified ID of the DDRC The actual maximum read latency is rlatcnt_max plus

			inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.
[15:0]	RO	rlatcnt_min	Minimum latency of the read command with the specified ID of the DDRC Note that the actual minimum read latency is rlatcnt_min plus inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_RLATCNT1

DDRC_HIS_RLATCNT1 is DDRC specified ID read command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3AC	DDRC_HIS_RLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rlatcnt_all	Accumulated latency of the read command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the read command with the specified ID by using rlatcnt_all/fluxid_rd_cmd+inhere_rlatcnt.

DDRC_HIS_INHERE_RLAT_CNT

DDRC_HIS_INHERE_RLAT_CNT is a read channel inherent latency register.

Offset Address	Register Name	Total Reset Value
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																inhere_rlatcnt															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	inhere_rlatcnt	Inherent latency of the read data channel for the DDRC and PHY. The actual latency can be obtained only by using this register and rlatcnt_min, rlatcnt_max, rlatcnt_all, and fluxid_rd_cmd.

DDRC_STAT_RPT

DDRC_STAT_RPT is a read pointer to the DMC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3B4	DDRC_STAT_RPT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														stacmd_rpt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	stacmd_rpt	In threshold-based statistical mode, the latest eight statistical results are stored. This pointer is used to indicate the statistical result that the DDRC_HIS_CMD_SUM or DDRC_HIS_DAT_SUM reading result points to. 000: latest statistical result 001: second latest statistical result … 111: seventh latest statistical result

DDRC_HIS_CMD_SUM

DDRC_HIS_CMD_SUM is a DDRC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3B8	DDRC_HIS_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dmc_cmd_sum	Accumulated value of the commands that are temporarily stored in the DMC in the cycle. The value is wrapped if an overflow occurs.

DDRC_HIS_DAT_SUM

DDRC_HIS_CMD_SUM is a DDRC accumulated data count register.

Offset Address	Register Name	Total Reset Value
0x3BC	DDRC_HIS_DAT_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dmc_dat_sum	Accumulated value of data that are temporarily stored in the DMC in the cycle. The value is wrapped if an overflow occurs.

DDRC_HIS_SFC_RDATA0

DDRC_HIS_SFC_RDATA0 is SFC read data register 0.

Offset Address	Register Name	Total Reset Value
0x4A8	DDRC_HIS_SFC_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata0	Bits 31−0 of the data read by the SFC

DDRC_HIS_SFC_RDATA1

DDRC_HIS_SFC_RDATA1 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4AC	DDRC_HIS_SFC_RDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata1	Bits 63−32 of the data read by the SFC

DDRC_HIS_SFC_RDATA2

DDRC_HIS_SFC_RDATA2 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B0	DDRC_HIS_SFC_RDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata2	Bits 95−64 of the data read by the SFC

DDRC_HIS_SFC_RDATA3

DDRC_HIS_SFC_RDATA3 is software configuration read data register 3.

Offset Address	Register Name	Total Reset Value
0x4B4	DDRC_HIS_SFC_RDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata3	Bits 127−96 of the data read by the SFC

4.2 Flash Memory Controller

4.2.1 Overview

The flash memory controller (FMC) provides memory controller interfaces for connecting to external SPI NAND flash, SPI NOR flash or NAND flash to access data.

4.2.2 Features

The FMC has the following features:

- Provides one 9 KB (8192 bytes+1024 bytes) on-chip buffer for improving the read speed.
- Supports two external CSs (SPI NAND flash or SPI NOR flash).
- Supports one external CS (NAND flash).
- Supports the SPI NAND flash, SPI NOR flash, and NAND flash.
- Supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.
- Supports data reading in DDR STR mode.
- Supports the SPI NAND flash with the following specifications:
  - 2 KB or 4 KB page size
  - 64 pages/block
- Supports the NAND flash with the following specifications:
  - 2 KB, 4 KB, 8 KB, or 16 KB page size
  - 64/128/256/512 pages/block
  - 8-bit NAND flash
  - Asynchronous NAND flash
- Allows the system to boot from CS0 of the SPI NOR flash, SPI NAND flash, or NAND flash.
  - Provides 1 MB boot space.
  - Automatically sends the reset command of the flash and then performs data read operations in boot mode. The reset command is sent only in SPI NAND flash mode or NAND flash mode.
  - Automatically skips bad blocks (for the SPI NAND flash and NAND flash). A maximum of four consecutive bad blocks can be skipped.
  - Supports the adaptive boot function (for the SPI NAND flash and NAND flash). The FMC automatically obtains the correct page size, error checking and correction (ECC) type, and block size.
  - Supports dual boot images (for the SPI NAND flash and NAND flash).
  - Supports the 1-wire and 4-wire boot modes for the SPI NAND flash and 1-wire boot mode for the SPI NOR flash.
  - Supports boot from the SPI NOR flash in 3-byte or 4-byte address mode.
- Supports the direct memory access (DMA) read and write functions of the SPI NOR flash, SPI NAND flash, and NAND flash.
  - Supports the read and write operations in internal DMA mode for the SPI NAND flash and NAND flash. You can write only the entire page and read the entire page or only the control information (read only the OOB).

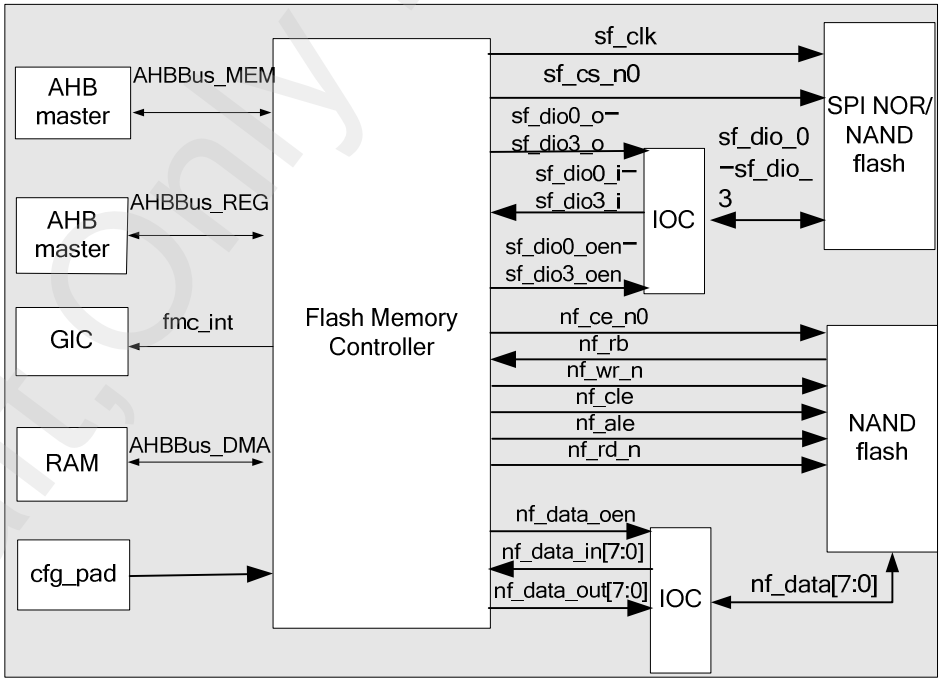
  - Supports the DMA read and write operations for the SPI NOR flash. The length of the data read or written can be configured.
- Supports manual configurations of commands only in ECC0 mode.
- Supports the ECC function for the SPI NAND flash and NAND flash.
  - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, 28-bit/1 KB, 40-bit/1 KB, and 64-bit/1 KB Bose-Chaudhuri-Hocquenghem (BCH) code ECC (1 KB means the 1 KB level but not exactly 1024 bytes.)
  - Enable and disable of the ECC function and ECC code generation
  - Data read and write operations in ECC0 mode (transparent transmission)
  - No incorrect reporting of uncorrectable ECC errors when empty pages (data is 0xFF) are read
- Supports the randomizer only in non-ECC0 mode when the page size is 8 KB or 16 KB. It is disabled in other modes.
- Supports seven types of interrupts: operation completion interrupt, programming failure interrupt, correctable ECC error interrupt, ECC alarm interrupt, uncorrectable ECC error interrupt, advanced high-performance bus (AHB) operation error interrupt, and DMA transfer error interrupt.
- Supports the low-power mode. The unused modules can be disabled.

4.2.3 Function Description

4.2.3.1 Interface Block Diagram

The FMC is used for interaction between the AHB and external flash memories. Figure 4-3 shows the block diagram of FMC interfaces.

Figure 4-3 Block diagram of FMC interfaces



In Figure 4-3, the pin names such as sf_clk indicate the names of pins in the FMC. Table 4-11 describes the mapping between the names of FMC pins and the names of external pins. In the following sections, the pin names related to interface description indicate the names of FMC pins.

Table 4-11 Mapping between the names of FMC pins and the names of chip pins

FMC Pin Name	Chip Pin Name
sf_clk	NF_DQ1
sf_dio_0	NF_DQ3
sf_dio_1	NF_REN
sf_dio_2	NF_RDY
sf_dio_3	NF_DQ0
sf_cs_n0	NF_CSN
sf_cs_n1	NF_DQ7
nf_ce_n0	NF_CSN
nf_wr_b	NF_RDY
nf_wr_n	NF_WEN
nf_cle	NF_CLE
nf_ale	NF_ALE
nf_rd_n	NF_REN
nf_data[0]~nf_data[7]	NF_DQ0~NF_DQ7

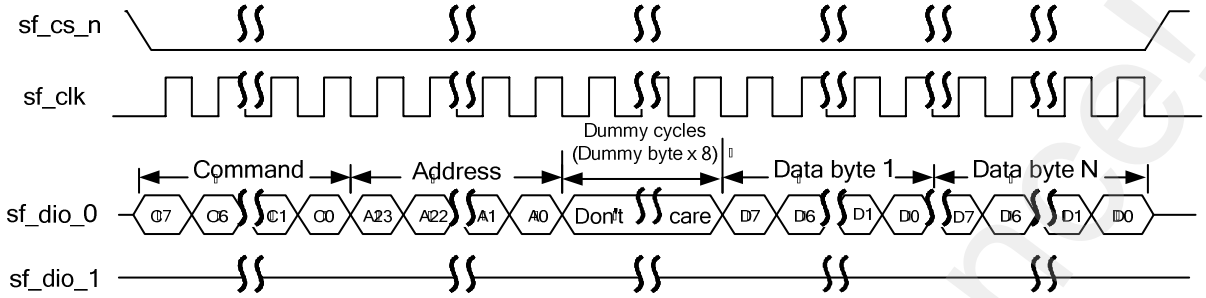
4.2.3.2 Interfaces

The FMC supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI. The standard SPI, dual I/O SPI, and quad I/O SPI support the SDR, DTR, and DDR modes.

Standard SPI

The standard SPI is connected to a 1-bit data input line and a 1-bit data output line. Figure 4-4 shows the write timing of the standard SPI.

Figure 4-4 Write timing of the standard SPI

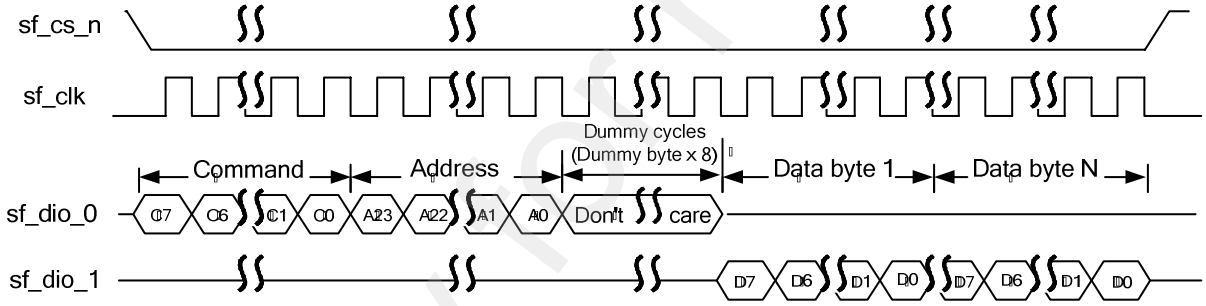


Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is output in single-bit serial mode through the sf_dio_0 line.

Figure 4-5 shows the read timing of the standard SPI.

Figure 4-5 Read timing of the standard SPI



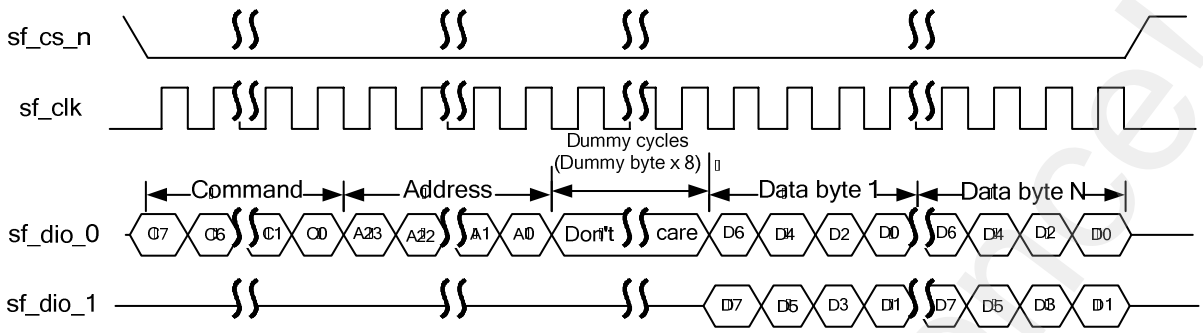
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is input in single-bit serial mode through the sf_dio_1 line.

Dual-Output/Dual-Input SPI

Figure 4-6 shows the timing of the dual-output/dual-input SPI.

Figure 4-6 Timing of the dual-output/dual-input SPI



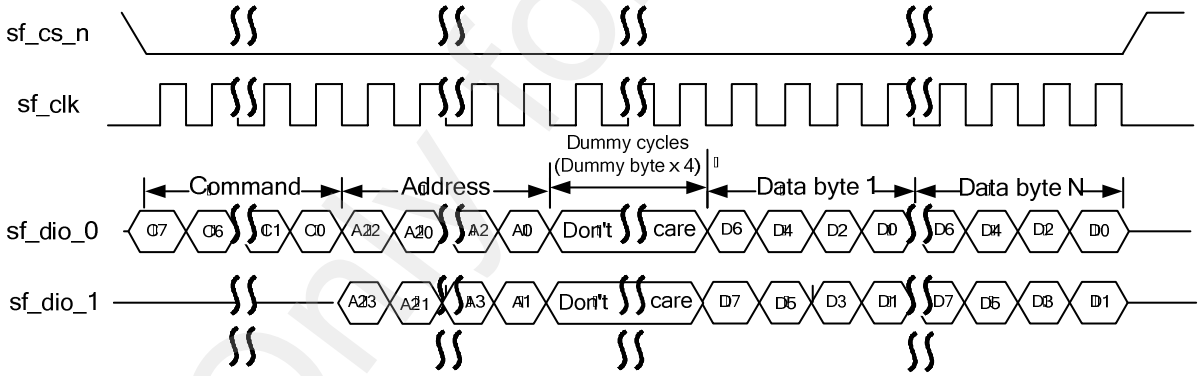
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- The data bytes are output (written) or input (read) in 2-bit mode through the sf_dio_0 or sf_dio_1 line.

Dual I/O SPI

Figure 4-7 and Figure 4-8 show the timings of the dual I/O SPI.

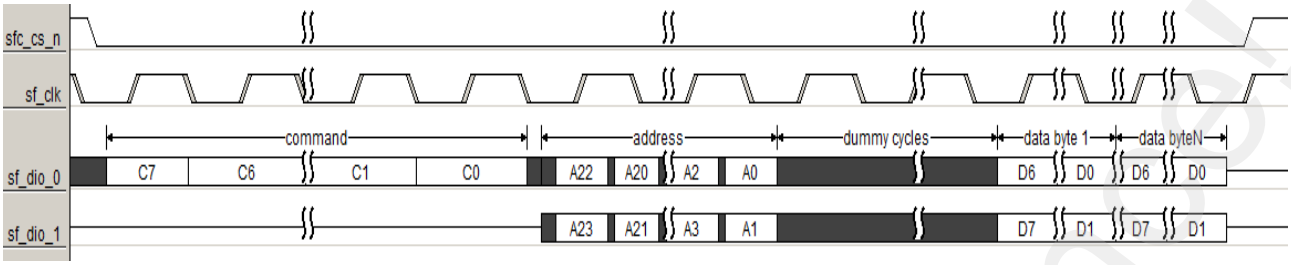
Figure 4-7 SDR timing of the dual I/O SPI



Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 2-bit mode through the sf_dio_0 or sf_dio_1 line.
- The data bytes are output (written) or input (read) in 2-bit mode through the sf_dio_0 or sf_dio_1 line.

Figure 4-8 DDR/DTR timing of the dual I/O SPI



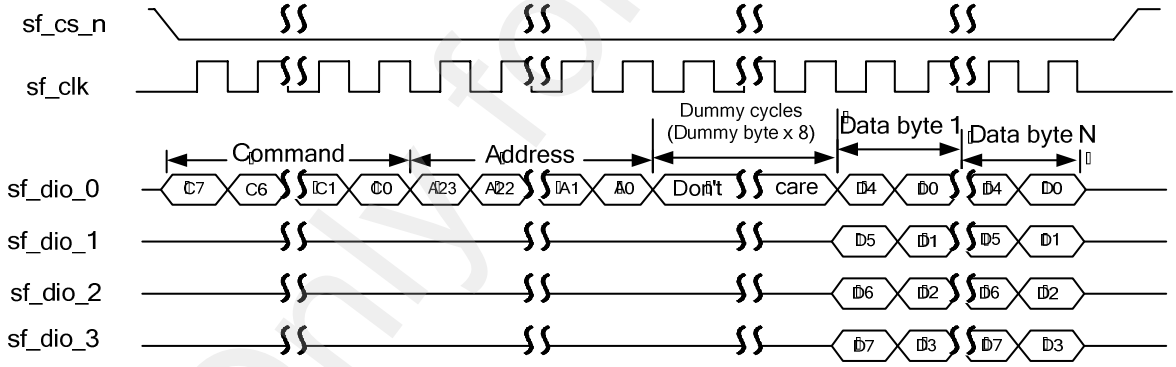
Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 2-bit dual-edge active mode through the sf_dio_0 or sf_dio_1 line.
- Data is input (read) in 2-bit dual-edge active mode through the sf_dio_0 or sf_dio_1 line.
- Only the read operation is supported in DDR/DTR mode.

Quad-Output/Quad-Input SPI

Figure 4-9 shows the timing of the quad-output/quad-input SPI.

Figure 4-9 Timing of the quad-output/quad-input SPI



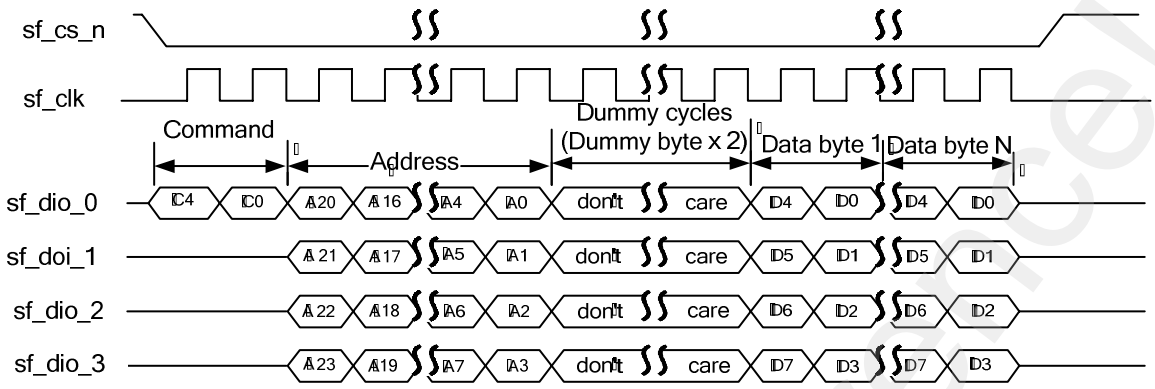
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is output (written) or input (read) in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

Quad I/O SPI

Figure 4-10 and Figure 4-11 show the timings of the quad I/O SPI.

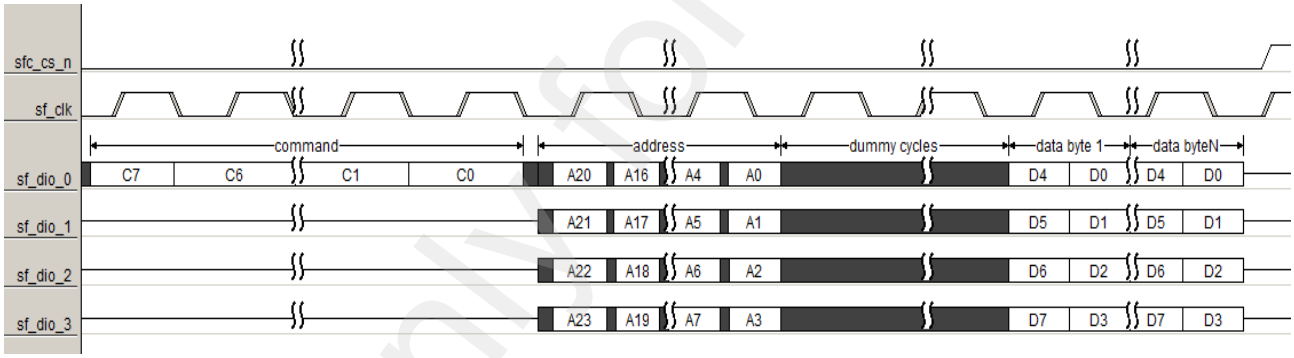
Figure 4-10 SDR timing of the quad I/O SPI



Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.
- The data bytes are output (written) or input (read) in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

Figure 4-11 DDR/DTR timing of the quad I/O SPI



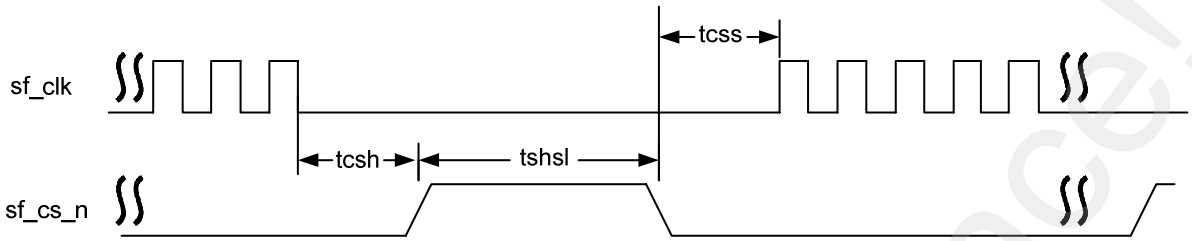
Note the following:

- The command cycles are output in single-bit single-edge data serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 4-bit dual-edge mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.
- Data is input in 4-bit dual-edge sampling mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

4.2.3.3 SPI Timings

Figure 4-12 shows the SPI timings and related parameters.

Figure 4-12 SPI output timing



NOTE

- The timings are configured in the TIMING_SPI_CFG register.
- tcsh indicates the CS hold time.
- tcss indicates the CS setup time.
- tshsl indicates the CS deselect time.

4.2.3.4 SPI NAND Flash Address

Table 4-12 describes the address allocation of the SPI NAND flash. The first and second bytes indicate the column address, whereas the third, fourth, and fifth bytes indicate the row address.

Table 4-12 Address allocation of the SPI NAND flash

Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1st byte	A0	A1	A2	A3	A4	A5	A6	A7
2nd byte	A8	A9	A10	A11	A12*	A13*	0	0
3rd byte	A12	A13	A14	A15	A16	A17	A18	A19
4th byte	A20	A21	A22	A23	A24	A25	A26	A27
5th byte*	A28*	A29*	0	0	0	0	0	0

NOTE

- Bits A0−A11 are configured as the valid column address when the page size is 2 KB. Bits A0−A12 are configured as the valid column address when the page size is 4 KB.
- Bit A12 (2 KB page size) and bit A13 (4 KB page size) indicate the plane address only for Micron flash memories. Other vendors do not have the concept of plane address.
- Whether bits A28 and A29 are required depends on the flash memory. If the two bits are not used, the outputs are 0.

When the read and write commands of the SPI NAND flash are issued, the column and row addresses are configured based on the following operations:

- For the write operation, the column address is configured during the loading process and the row address is configured during the programming process.
- For the read operation, the row address is configured when the page is read to cache and the column address is configured during the read operation.

In internal DMA mode, the address command is issued by the FMC. FMC_ADDRL and FMC_ADDRH are configured by software based on the operation address. The configuration values of FMC_ADDRL and FMC_ADDRH are 1st byte−4th byte and 5th byte respectively.

NOTE

- If the page size is 2 KB, bit A12 indicates the plane address. Other meanings of bit A12 are not supported; otherwise, the results of the read and write operations will be affected.
- If the page size is 4 KB, bit A13 indicates the plane address. Other meanings of bit A13 are not supported; otherwise, the results of the read and write operations will be affected.

4.2.3.5 Boot Function

The FMC is in boot mode by default. The chip can boot by reading data directly from the flash memory. The CPU can directly read the data stored in the address ranging from 0x00_0000 to 0x0F_FFFF. The size of the entire address space is 1 MB.

SPI NOR Flash

The address space of the SPI NOR flash is consecutive. The 1 MB boot data is directly mapped to address space 0x00_0000 to 0x0F_FFFF of the SPI NOR flash.

SPI NAND Flash and NAND Flash

For the SPI NAND flash and NAND flash, the address space is inconsecutive and bad blocks may exist. As a result, the 1 MB boot data cannot be directly mapped to the flash. To implement the boot operation, ECC_TYPE, PAGE_SIZE, and BLOCK_SIZE are also required for address decoding.

The FMC supports the adaptive boot function, that is, it can automatically adapt to ECC_TYPE, PAGE_SIZE, and BLOCK_SIZE of the flash based on the block 0 data. The FMC requires that physical block 0 be a good block, and it can automatically skip other bad blocks.

During the boot process, the FMC automatically skips bad blocks, searches for good blocks, and reads the boot information. It can skip at most four consecutive bad blocks. If there are five consecutive bad physical blocks, the boot fails. During the entire boot process, there can be multiple bad block skipping processes. When a good block is found, a bad block skipping process ends; if a bad blocks is found, a new bad block skipping process starts.

Table 4-13 describes the specifications supported by the SPI NAND flash and NAND flash respectively in boot mode.

Table 4-13 Specifications supported in adaptive boot mode

ECC[a] (Bit)	Page_size[c] (KB)	Block_size[b] (Pages/Block)	SPI NAND	NAND
8	2	64 (SPI NAND) 64/128/256 (NAND)	Supported	Supported
	4		Supported	Supported
24	2		Supported	Supported
	4		Supported	Supported
	8	64/128/256/512 (NAND)	/	Supported
40	8		/	Supported

ECC[a] (Bit)	Page_size[c] (KB)	Block_size[b] (Pages/Block)	SPI NAND	NAND
	16		/	Supported
64	8		/	Supported
	16		/	Supported

a: The SPI NAND flash supports only the 8-bit and 24-bit ECC modes during the boot process.

b: The SPI NAND flash supports only the 64 Block_size (64 pages/block) during the boot process.

c: The randomizer is enabled when the page size is 8 KB or 16 KB during the boot process.

Dual-Image Function

For the SPI NAND flash and NAND flash, if uncorrectable errors occur during the boot process, the FMC automatically triggers the dual-image function. To be specific, the FMC jumps to the same page of the backup image to read the boot data.

CAUTION

Image 0 and image 1 are required to be stored in two consecutive good blocks respectively (at most four bad blocks are allowed between the two good blocks).

4.2.3.6 Operations in Register Mode

The registers related to the operation command and address are configured by using software. Then the corresponding command is issued by configuring the FMC_OP register. The FMC issues a command to the flash memory according to the value configured by software. If data needs to be transferred to the flash memory, the internal buffer is used.

Operations such as reading ID, setting feature, and erasing are performed in this mode.

In register mode, all the operations related to the flash memory can be combined, and commands related to the address and data transfer can be issued separately.

4.2.3.7 Operations in Internal DMA Mode

The FMC can perform read and write operations in internal DMA mode for improving the access speed. In internal DMA mode, the FMC can directly access the DDR through the bus.

- DMA write operation: For the SPI NOR flash, data with any length can be transferred from any address of the DDR and written to any address of the flash memory. For the SPI NAND flash and NAND flash, the write operation is performed only by page.
- DMA read operation: For the SPI NOR flash, data with any length can be transferred from any address of the flash memory and written to any address of the DDR. For the SPI NAND flash and NAND flash, the entire page is read or only the OOB is read.
- Only-OOB read operation: When the software requires only software management information such as the bad block flag and empty block flag, only the control information needs to be read. In this case, only the OOB is read in DMA mode.

4.2.3.8 ECC

For the SPI NAND flash, the FMC supports ECC. Four ECC modes are supported, including 8-bit/1 KB ECC mode, 16-bit/1 KB ECC mode, 24-bit/1 KB ECC mode, and 28-bit/1 KB ECC mode. In 8-bit/1 KB ECC mode, errors occur in at most eight bits of the checked 1 KB data can be corrected.

For the NAND flash, the FMC supports six ECC modes, including the 8-bit/1 KB ECC mode, 16-bit/1 KB ECC mode, 24-bit/1 KB ECC mode, 28-bit/1 KB ECC mode, 40-bit/1 KB ECC mode, and 64-bit/1 KB ECC mode. The page sizes supported by the ECC modes are different. For details, see the related data structures.

The OOB information is added to the data with ECC protection, and then the ECC is added. The error correction algorithm runs by the error correction unit (1 KB). For example, the ECC is calculated for (DATA+OOB). If the page size is 2 KB, data in each error correction unit is (DATA+OOB)/2; if the page size is 4 KB, data in each error correction unit is (DATA+OOB)/4.

- The OOB is part of the software management information. For details, see the (BB+CTRL) part in the data structure.
- DATA indicates the real data. DATA indicates 2048-byte data when the page size is 2 KB and 4096-byte data when the page size is 4 KB.

During the boot process, the SPI NAND flash supports only the 8-bit and 24-bit ECC modes. The flash requires 4-bit/512 bytes and 8-bit/512 bytes ECC modes (the error correction unit is 512 bytes in the component manual). In normal mode, the SPI NAND flash also supports the 16-bit and 28-bit ECC modes. If the spare area of the flash is sufficient for storing the check code, the 16-bit/1 KB ECC mode can be used for the flash that requires 4-bit/512 bytes ECC mode to improve the reliability. For the NAND flash, the 8-bit/1 KB, 24-bit/1 KB, 40-bit/1 KB, and 64-bit/1 KB ECC modes are supported during the boot process. In normal mode, the NAND flash also supports the 16-bit/1 KB and 28-bit/1 KB ECC modes.

When the maximum error correction capability is exceeded, the uncorrectable error interrupt is reported. The FMC supports the alarm interrupt. When the number of error bits during one error correction operation is greater than or equal to the configured error threshold (FMC_ERR_THD), an error alarm interrupt is reported. If error bits occur in one or more error correction units and the number of error bits in each error correction unit is less than the error threshold and uncorrectable error value, the correctable error interrupt flag FMC_INT[err_val_int] is changed to 1.

When the data on a page is read, if uncorrectable errors occur in one error correction unit, the uncorrectable error interrupt is reported. If an error alarm interrupt is reported for an error correction unit, the error correction alarm status is reported. If the number of error correction bits is less than the error threshold, the correctable error interrupt status is reported.

The FMC does not support ECC check for the SPI NOR flash. If FMC_CFG[ecc_type] is 0, the SPI NAND flash works in non-ECC check mode and the FMC transfers data directly from the flash without data structure processing.

4.2.3.9 Randomizer

To improve the data storage stability, the FMC provides the randomizer for the large-capacity MLC NAND flash for randomizing data.

After the randomizer is enabled, the FMC randomizes data and then writes data to the flash during the write operation, and derandomizes data read from the flash and then writes data to the buffer during the read operation.

CAUTION

- In ECC0 mode or when the SPI NOR flash is used, the FMC internally disables the randomizer regardless of the configured value of GLOBAL_CFG[randomizer_en].
- The randomizer is internally disabled when the page size is 2 KB or 4 KB.
- After the randomizer is enabled, an uncorrectable error occurs when data in the block that has just been erased is read because data on the page is 0xFF and data is uncorrectable after it is derandomized.

4.2.3.10 Timeout

The FMC provides the timeout mechanism for the DMA write operation. When waiting for the completion of the DMA write operation, the FMC continuously sends the **get feature** command to query whether the write operation is complete. For the SPI NOR flash, the operation is complete when the SPI NOR flash sends the **RDSR** command; for the NAND flash, the operation is complete when the RB is pulled up. If the FMC wait time exceeds the configured value of FMC_TIMEOUT_WR[timeout_wr], the DMA write operation is ended and the FMC_INT[op_fail] interrupt is reported.

For the NAND flash, if the RB is pulled up before timeout occurs during the DMA write operation, the FMC automatically issues a status register reading command and stores the read value in FM_STATUS[fm_status]. If bit 0 of the status register is 1, the DMA write operation fails and the FMC reports the FMC_INT[op_fail] interrupt.

4.2.4 Working Process

4.2.4.1 Initialization Process

The initialization process is as follows:

Step 1 (Optional; when the timing parameters need to be adjusted) Configure TIMING_SPI_CFG (for the SPI NAND flash or SPI NOR flash) or PND_PWIDTH_CFG (for the NAND flash) based on the flash memory.

Step 2 Configure the interface type, ecc_type and page size of the flash memory in the FMC configuration register (FMC_CFG) according to the manual of the connected flash.

Step 3 Switch the address mode of the SPI NOR flash to the 4-byte address mode if the default address mode is 3-byte address mode. For details, see section 4.2.4.4 "Process of Changing the Address Mode of the SPI NOR Flash."

Step 4 Issue operations based on the operation configuration registers.

----End

4.2.4.2 FMC_OP Operation Process (Register Operation Mode)

To read the IDs of the component registers or configure component registers by configuring FMC_OP, perform the following steps:

Step 1 Set ecc_type of the FMC_CFG register to 0.

Step 2 Write the expected operation data from the buffer access start address for a register write operation (for example, configure the flash memory configuration register).

Step 3 Configure the operation command, operation address, and number of data segments to be read or written as required in FMC_CMD, FMC_ADDRL, and FMC_DATA_NUM respectively.

Step 4 Configure FMC_OP_CFG based on the component commands that are issued by configuring FMC_OP.

Step 5 Configure FMC_OP to issue commands. For details about the configuration value, see the description of FMC_OP.

Step 6 Check whether the operation is complete by querying of FMC_OP bit[0] in query mode and FMC_INT[op_done_init] in interrupt mode. If FMC_OP bit[0] or FMC_INT[op_done_init] is 1, the operation is complete.

Step 7 Read the value of the component register from the buffer that stores the read results in step 6.

----End

4.2.4.3 Process of Reading the Component Status

To read the component status, perform the following steps:

Step 1 Set FMC_OP[read_status_en] and FMC_OP[reg_op_start] to 1 to issue the component status read command.

Step 2 Store the read result in FMC_FLASH_INFO.

----End

4.2.4.4 Process of Changing the Address Mode of the SPI NOR Flash

The SPI NOR flash supports the 3-byte and 4-byte address modes. You can specify the default address mode by pulling up or pulling down the corresponding pin, and dynamically change the address mode by configuring registers after the chip boots.

If the default address mode is the 3-byte address mode and the address mode of the flash memory is 4-byte address mode, perform the following steps to change the address mode after the chip boots:

Step 1 Ensure that the operations on the SPI NOR flash are complete.

Step 2 Configure the related registers to issue the command for changing the address mode of the flash memory to 4-byte address mode in register mode according to the flash memory requirements.

Step 3 Set FMC_CFG [spi_nor_addr_mode] to 1 to change the address mode of the SPI NOR flash from the 3-byte address mode to 4-byte address mode.

----End

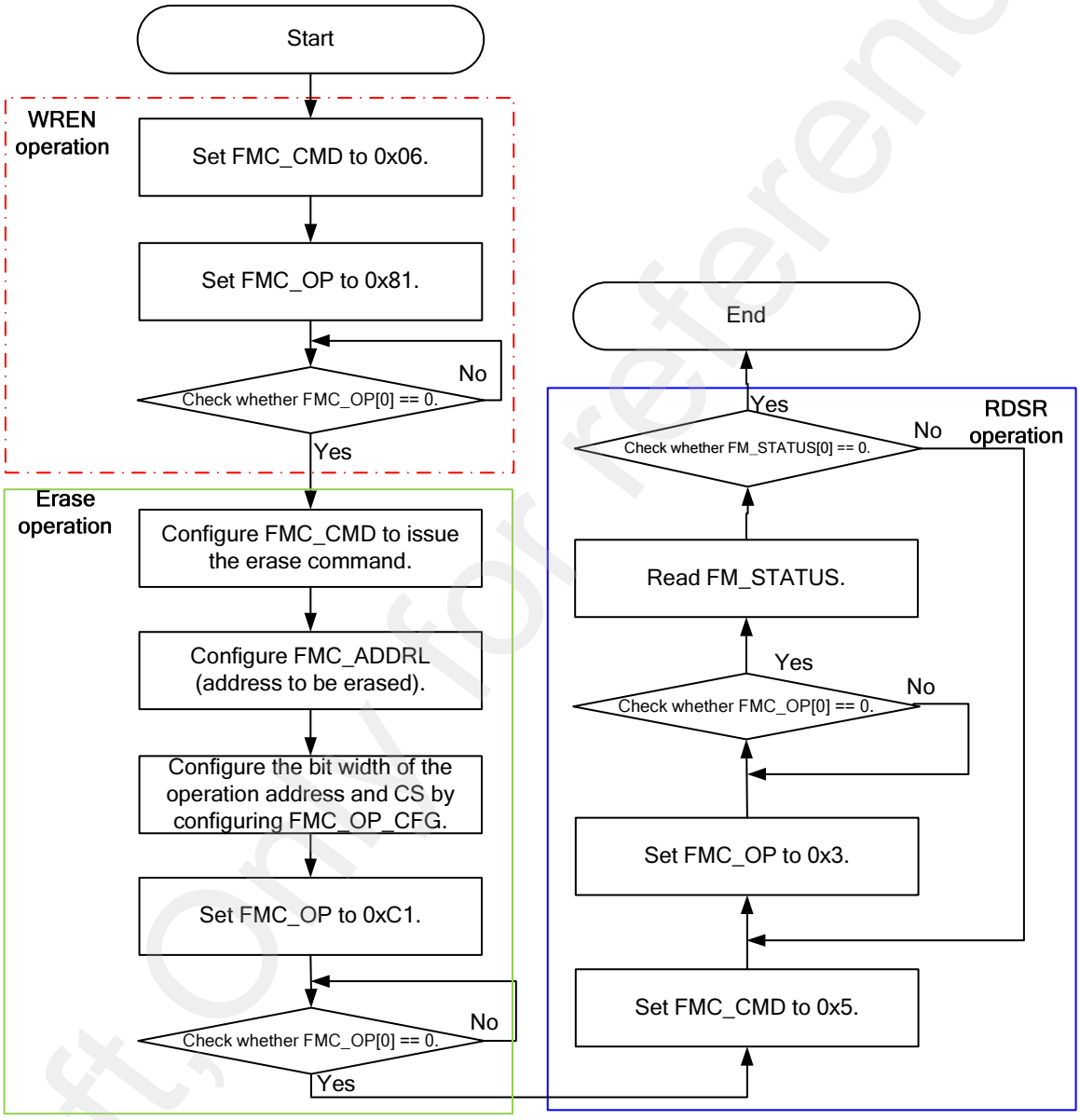
NOTE

For details about the command for changing the address mode of the SPI NOR flash, see the related flash manual.

4.2.4.5 Erase Operation Process (SPI NAND flash and SPI NOR flash)

The data in the flash memory must be erased before the program operation is performed. Note that the write enable (WREN) operation must be performed before the erase operation. Figure 4-13 shows an example of erase operation process in query mode.

Figure 4-13 Example of erase operation process



NOTE

- Figure 4-13 shows the erase operation process in query mode. If the interrupt mode is used, check whether FMC_INT[op_done_init] is 1; if yes, the operation is complete.
- During the erase operation, configure the erase instruction and operation address according to the manual of the corresponding flash.

4.2.4.6 FMC_OP Erase Operation Process (NAND Flash)

For the NAND flash, to erase CS0 in NFC_OP mode, perform the following steps:

Step 1 Set FMC_CFG[op_mode] to 1 to ensure that the FMC is in normal mode.

Step 2 Write the address of the block to be erased to FMC_ADDRL and the erase command 0xD060 to FMC_CMD.

Step 3 Write 0x30 to FMC_OP_CFG, which means that CS0 is selected as the component to be operated and 3-byte address needs to be sent.

Step 4 Write 0xDB to FMC_OP to start the CS0 erase operation (and the operation of automatically reading the status register).

Step 5 In query mode, FMC_OP[reg_op_start] is checked. If the value is 0, the operation ends. In interrupt mode, FMC_INT[op_done_int] is checked. If the value is 1, the operation ends. Otherwise, repeat this step until the operation ends.

Step 6 Read FM_STATUS[fm_status] to check whether the erase operation is successful.

----End

4.2.4.7 Process of Reading Data in Internal DMA Mode (FMC_OP_CTRL Read Operation)

To read data in internal DMA mode, perform the following steps:

Step 1 Set FMC_CFG[op_mode] to 1 to ensure that the FMC is in normal mode.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

CAUTION

For the SPI NOR flash, the number of address cycles during the DMA operation is determined by FMC_CFG[spi_nor_addr_mode]. The 3-byte and 4-byte address modes are supported. For the SPI NAND flash and NAND flash, the FMC uses the 5-byte address mode by default and the address mode cannot be configured.

Step 3 Configure the start address for storing data in the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_.

- For the SPI NOR flash, FMC_DMA_SADDR_ does not need to be configured.
- For the SPI NAND flash and NAND flash, if only the OOB is read, only FMC_DMA_SADDR_ needs to be configured.

CAUTION

- For the SPI NAND flash and NAND flash, the DDR address must be 4-byte-aligned.

- For the SPI NAND flash and NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.

Step 4 Configure FMC_DMA_LEN. For the SPI NOR flash, FMC_DMA_LEN needs to be set to the length of the read data; for the SPI NAND flash and NAND flash in ECC0 mode, FMC_DMA_LEN needs to be set to the length of data in the spare area. This register does not need to be configured for other operations.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued read command.

- For the SPI NAND flash and SPI NOR flash, FMC_OP_CFG[dummy_num] and FMC_OP_CFG[mem_if_type] need to be configured based on the number of dummy cycles in the read timings of the SPI flash and the SPI type.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Set bit[0] of FMC_OP_CTRL to 1 to issue the flash read command.

- Set FMC_OP_CTRL[rw_op] to 0 to select the DMA read operation.
- For the SPI NAND flash and NAND flash, if only the OOB is read, FMC_OP_CTRL[rd_op_sel] needs to be configured.
- Configure FMC_OP_CTRL[rd_opcode] based on the instruction of the flash read operation.

Step 7 Check whether the read operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] or FMC_INT[op_done_int] is 1, the read operation is complete, and data is written to the DDR.

----End

4.2.4.8 Process of Writing Data in Internal DMA Mode (FMC_OP_CTRL Read Operation)

To write data in internal DMA mode, perform the following steps:

Step 1 Set FMC_CFG[op_mode] to 1 to ensure that the FMC is in normal mode.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

CAUTION

For the SPI NOR flash, the number of address cycles during the DMA operation is determined by FMC_CFG[spi_nor_addr_mode]. The 3-byte and 4-byte address modes are supported. For the SPI NAND flash and NAND flash, the FMC uses the 5-byte address mode by default and the address mode cannot be configured.

Step 3 Configure the start address for transferring data from the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB. For the SPI NOR flash, FMC_DMA_SADDR_OOB does not need to be configured.

CAUTION

- For the SPI NAND flash and NAND flash, the DDR address must be 4-byte-aligned.
- For the SPI NAND flash and NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.

Step 4 Configure FMC_DMA_LEN. For the SPI NOR flash, FMC_DMA_LEN needs to be set to the length of the read data; for the SPI NAND flash and NAND flash in ECC0 mode, FMC_DMA_LEN needs to be set to the length of data in the spare area. This register does not need to be configured for other operations.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued write command.

- For the SPI NAND flash and NAND flash, Configure FMC_OP_CFG[mem_if_type] based on the SPI required for the write operation.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Configure FMC_OP_CTRL to issue corresponding commands.

- Set FMC_OP_CTRL[rw_op] to 1 to select the DMA write operation.
- For the SPI NAND flash and NAND flash, configure FMC_OP_CTRL[wr_opcode] based on the instruction of the flash program operation.

Step 7 Check whether the write operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] is 0 or FMC_INT[op_done_int] is 1, the write operation is complete, and data is written to the flash memory.

----End

4.2.4.9 Notes

Note the following:

- You must reset the SPI NAND flash and NAND flash before use or after exceptions occur.
- You are advised not to configure registers when FMC_OP_CTRL [dma_op_ready] or FMC_OP [reg_op_start] is 1, indicating that the controller is performing an operation. Otherwise, the operation may become abnormal.

4.2.5 Data Structures (NAND Flash/SPI NAND Flash)

There are two types of FMC data. One is the original user data, the other is the data converted by the FMC and stored in the NAND flash in non-ECC0 mode. In non-ECC0 mode, the original user data and data converted by the FMC have fixed data structures as well as data member length and position. In ECC0 mode, the user data is written or read without being changed by the FMC.

In ECC0 mode, the FMC transparently transmits data. During the write operation, the FMC directly writes the data in the buffer to the flash; during the read operation, the FMC directly writes the data read from the flash to the buffer.

In non-ECC0 mode, when the flash is written, the user data processing by the FMC involves ECC code generation and data reconstitution. The FMC implements ECC encoding in the

internal buffer, generates the ECC code, and reconstitutes buffer data, and writes data to the flash. When the flash is read, the data processing by the FMC involves flash data reconstitution and ECC. The FMC reconstitutes data read from the flash, writes data to the internal buffer, and implements ECC in the buffer.

In non-ECC0 mode, data in the buffer and data in the flash have different structures. Table 4-14 describes the length of each data segment in various non-ECC0 modes.

Table 4-14 Data structure length in various non-ECC0 modes

ECC[a] (Bit)	ecc_len[b] (Byte)	Page_size (Byte)	oob_len[c] (Byte)	sec_len[d] (Byte)
4-bit/512 bytes (8/1 KB)	14	2048	30 + 2	1040
		4096		1032
8-bit/512 bytes (16/1 KB)	28	2048	6 + 2	1028
		4096	14 + 2	
24-bit/1 KB	42	2048	30 + 2	1040
		4096		1032
		8192		1028
40-bit/1 KB	70	8192	30 + 2	1028
		16384		1026
64-bit/1 KB[e]	112	8192	30 + 2	1028
		16384		1026

a: The 4-bit/512 bytes mode is equivalent to the 8-bit/1 KB mode, and the 8-bit/512 bytes mode is equivalent to the 16-bit/1 KB mode.

b: **ecc_len** indicates the length of ECC code generated by each error correction unit.

c: **oob_len** indicates the length of the redundant area visible to the upper-layer software, which consists of the CTRL and BB.

d: **sec_len** indicates the length of the data area in each error correction unit. **sec_len** is calculated as follows: sec_len = 1024 + (oob_len x 1024)/Page_size

e: The length of each ECC error correction unit is 1 KB. 1KB means the 1 KB level but not exactly 1024 bytes. For example, the length of the error correction unit (**sec_len**) ranges from 1026 bytes to 1040 bytes, and the lengths are all represented as 1 KB.

The following describes each data segment by taking the write operation as an example:

When the FMC writes data to the flash, data is consecutively stored in the format of data+ECC. However, special processing is required for the OOB data.

- The BB identity needs to be stored in the position of **page_size** on the flash page. That is, when the page size is 2 KB, 4 KB, 8 KB, or 16 KB, the BB data is stored in the first two bytes of the 2048, 4096, 8192, or 16384 bytes. In this way, the storage of the original data or ECC data is affected.

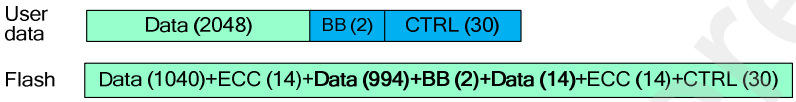
- The CTRL data needs to be stored at the end of the valid data. Therefore, the storage format of the last data segment in the flash is data (excluding BB data and CTRL data)+ECC+CTRL.

4.2.5.2 4-Bit ECC Mode (8-Bit/1 KB Error Correction Performance)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-14 shows the structure of data in the buffer and flash.

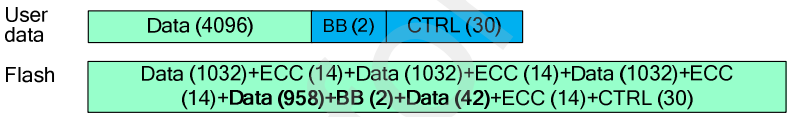
Figure 4-14 Data structure when the page size is 2 KB in 4-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-15 shows the structure of data in the buffer and flash.

Figure 4-15 Data structure when the page size is 4 KB in 4-bit ECC mode

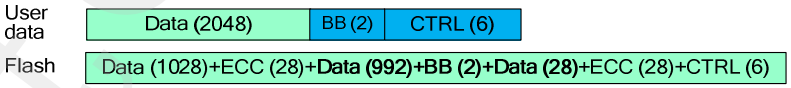


4.2.5.3 8-Bit ECC Mode (16-Bit/1 KB Error Correction Performance)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 8 bytes. Figure 4-16 shows the structure of data in the buffer and flash.

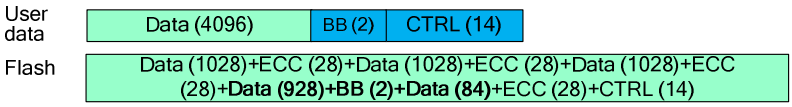
Figure 4-16 Data structure when the page size is 2 KB in 8-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 16 bytes. Figure 4-17 shows the structure of data in the buffer and flash.

Figure 4-17 Data structure when the page size is 4 KB in 8-bit ECC mode

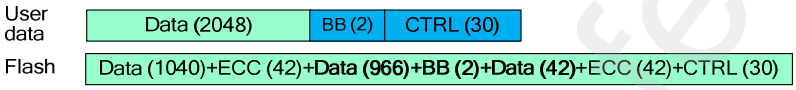


4.2.5.4 24-Bit ECC Mode (24-Bit/1 KB Error Correction Performance)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-18 shows the structure of data in the buffer and flash.

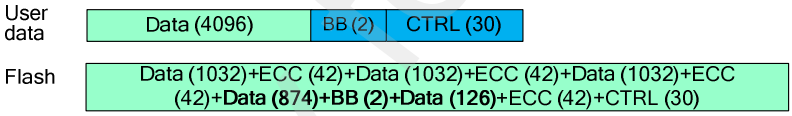
Figure 4-18 Data structure when the page size is 2 KB in 24-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-19 shows the structure of data in the buffer and flash.

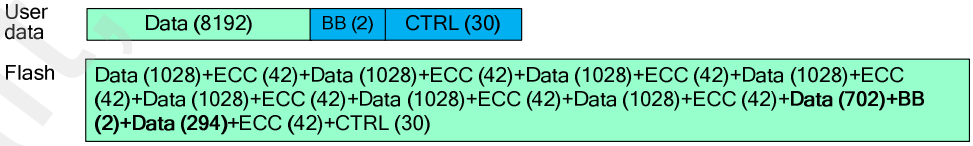
Figure 4-19 Data structure when the page size is 4 KB in 24-bit ECC mode



8 KB Page Size

When the page size is 8 KB, the size of the redundant area available to software is 32 bytes. Figure 4-20 shows the structure of data in the buffer and flash.

Figure 4-20 Data structure when the page size is 8 KB in 24-bit ECC mode

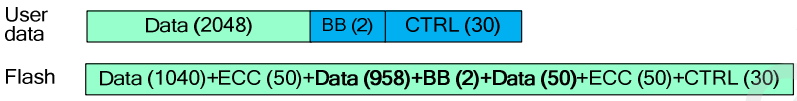


4.2.5.5 28-Bit ECC Mode (28-Bit/1 KB Error Correction Performance)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-21 shows the structure of data in the buffer and flash.

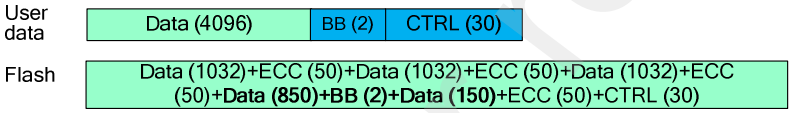
Figure 4-21 Data structure when the page size is 2 KB in 28-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-22 shows the structure of data in the buffer and flash.

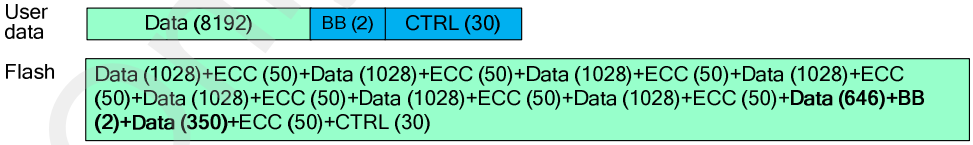
Figure 4-22 Data structure when the page size is 4 KB in 28-bit ECC mode



8 KB Page Size

When the page size is 8 KB, the size of the redundant area available to software is 32 bytes. Figure 4-23 shows the structure of data in the buffer and flash.

Figure 4-23 Data structure when the page size is 8 KB in 28-bit ECC mode

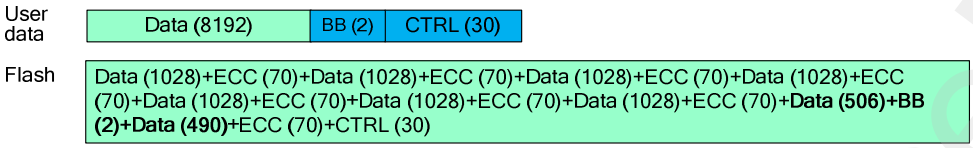


4.2.5.6 40-Bit ECC Mode (40-Bit/1 KB Error Correction Performance)

8 KB Page Size

When the page size is 8 KB, the size of the redundant area available to software is 32 bytes. Figure 4-24 shows the structure of data in the buffer and flash.

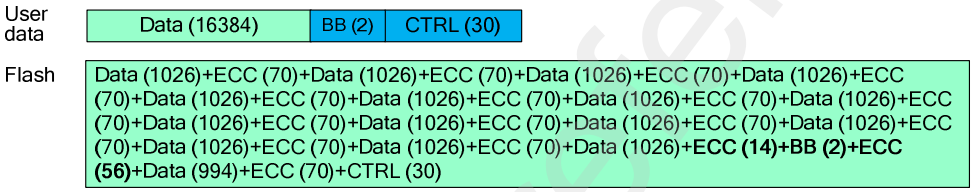
Figure 4-24 Data structure when the page size is 8 KB in 40-bit ECC mode



16 KB Page Size

When the page size is 16 KB, the size of the redundant area available to software is 32 bytes. Figure 4-25 shows the structure of data in the buffer and flash.

Figure 4-25 Data structure when the page size is 16 KB in 40-bit ECC mode

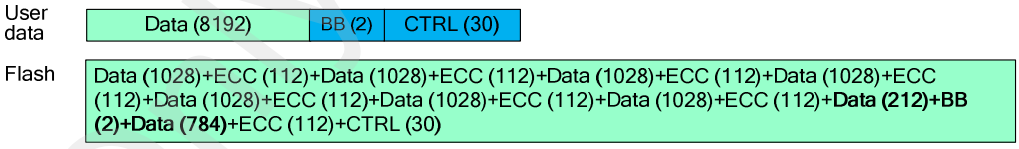


4.2.5.7 64-Bit ECC Mode (40-Bit/1 KB Error Correction Performance)

8 KB Page Size

When the page size is 8 KB, the size of the redundant area available to software is 32 bytes. Figure 4-26 shows the structure of data in the buffer and flash.

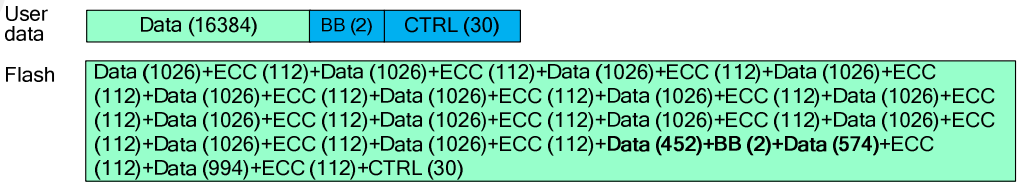
Figure 4-26 Data structure when the page size is 8 KB in 64-bit ECC mode



16 KB Page Size

When the page size is 16 KB, the size of the redundant area available to software is 32 bytes. Figure 4-27 shows the structure of data in the buffer and flash.

Figure 4-27 Data structure when the page size is 16 KB in 64-bit ECC mode



4.2.6 ECC Mode Selection

The ECC IP used by the controller processes data based on 1 KB data block. Therefore, the ECC performance of the controller is described in the format of *n* bits/1 KB, for example, 8 bits/1 KB or 24 bits/1 KB. To ensure component reliability, the recommended ECC performance of 1 bit/512 bytes, 4 bits/512 bytes, or 8 bits/512 bytes is provided in the component data sheet. The ECC performance of 8 bits/1 KB is equivalent to that of 4 bits/512 bytes. When you select the ECC mode for the controller, note the following:

- The priority of the ECC performance of the controller is higher than or equal to that of the recommended ECC performance.

  For example, if the recommended ECC performance is 1 bit/512 bytes or 4 bits/512 bytes, the controller can select the ECC mode with the performance of 8 bits/1 KB.
- The component page size must be greater than or equal to the required storage size of the ECC mode for the controller.

  For example, if the component page size is (2 KB + 64 bytes), the controller cannot select the ECC mode with the performance of 24 bits/1 KB because the required storage size of this ECC mode is (2 KB + 116 bytes). For details about the required storage size for the ECC mode, see section 4.2.5 "Data Structures (NAND Flash/SPI NAND Flash)."

4.2.7 FMC Registers

Table 4-15 describes FMC registers.

Table 4-15 Summary of FMC registers (base address of 0x1400_0000)

Offset Address	Register	Description	Page
0x0000	FMC_CFG	Component configuration register	4-155
0x0004	GLOBAL_CFG	Global configuration register	4-156
0x0008	TIMING_SPI_CFG	SPI timing configuration register	4-159
0x000C	PND_PWIDTH_CFG	Read/Write pulse width configuration register	4-159
0x0010	PND_OPIDLE_CFG	Operation interval configuration register	4-160
0x0018	FMC_INT	Interrupt status register	4-160
0x001C	FMC_INT_EN	Interrupt enable register	4-162
0x0020	FMC_INT_CLR	Interrupt clear register	4-164
0x0024	FMC_CMD	Command word configuration register	4-165
0x0028	FMC_ADDRH	Upper-byte component address configuration register	4-165
0x002C	FMC_ADDRL	Lower-four-byte component address configuration register	4-165

Offset Address	Register	Description	Page
0x0030	FMC_OP_CFG	Operation configuration register	4-166
0x0034	SPI_OP_ADDR	Operation address configuration register	4-167
0x0038	FMC_DATA_NUM	Data length register	4-167
0x003C	FMC_OP	Operation register	4-167
0x0040	FMC_DMA_LEN	DMA operation length register	4-169
0x0048	FMC_DMA_AHB_CTRL	DMA AHB bus control register	4-169
0x004C	FMC_DMA_SADDR_D0	DDR start address register 0 for DMA operations	4-170
0x0050	FMC_DMA_SADDR_D1	DDR start address register 1 for DMA operations	4-171
0x0054	FMC_DMA_SADDR_D2	DDR start address register 2 for DMA operations	4-171
0x0058	FMC_DMA_SADDR_D3	DDR start address register 3 for DMA operations	4-171
0x005C	FMC_DMA_SADDR_OOB	DDR OOB information storage start address register for DMA operations	4-172
0x0068	FMC_OP_CTRL	DMA operation control register	4-172
0x006C	FMC_TIMEOUT_WR	Write operation timeout register	4-173
0x0070	FMC_OP_PARA	OP operation parameter selection register	4-174
0x0074	FMC_BOOT_SET	Boot setting register	4-175
0x0078	FMC_LP_CTRL	Low-power control register	4-175
0x007C	FMC_LOCK	Lock address configuration register	4-176
0x0080	FMC_LOCK_SA0	Lock start address 0 configuration register	4-177
0x0084	FMC_LOCK_EA0	Lock end address 0 configuration register	4-177
0x0088	FMC_LOCK_SA1	Lock start address 1 configuration register	4-178

Offset Address	Register	Description	Page
0x008C	FMC_LOCK_EA1	Lock end address 1 configuration register	4-178
0x0090	FMC_LOCK_SA2	Lock start address 2 configuration register	4-178
0x0094	FMC_LOCK_EA2	Lock end address 2 configuration register	4-179
0x0098	FMC_LOCK_SA3	Lock start address 3 configuration register	4-179
0x009C	FMC_LOCK_EA3	Lock end address 3 configuration register	4-179
0x00A0	FMC_EXPCMD	Extended page command register	4-180
0x00A4	FMC_EXBCMD	Extended block command register	4-180
0x00A8	FMC_ERR_THD	ECC alarm threshold register	4-181
0x00AC	FMC_FLASH_INFO	Component status register	4-181
0x00B8	FMC_OP_CNT	FMC operation issuing times register	4-182
0x00BC	FMC_VERSION	Version register	4-182
0x00C0	FMC_ERR_NUM0_BUF0	SPI NAND flash and NAND Flash error correction information 0 statistics register for the first buffer operation	4-183
0x00C4	FMC_ERR_NUM1_BUF0	NAND flash error correction information 1 statistics register for the first buffer operation	4-183
0x00C8	FMC_ERR_NUM0_BUF1	NAND flash error correction statistics register 0 for the second buffer operation	4-184
0x00CC	FMC_ERR_NUM1_BUF1	NAND flash error correction statistics register 1 for the second buffer operation	4-184
0x00D0	FMC_ERR_ALARM_ADDRH	Upper-byte ECC alarm flash address register	4-184
0x00D4	FMC_ERR_ALARM_ADDRL	Lower-byte ECC alarm flash address register	4-185
0x00D8	FMC_ECC_INVALID_ADDRH	Upper-byte ECC uncorrectable address register	4-185

Offset Address	Register	Description	Page
0x00DC	FMC_ECC_INVALID_ADDRL	Lower-byte ECC uncorrectable address register	4-186
0x0E0	FMC_READ_TIMING_TUNE	Sampling point tuning register during the async NAND read operation	4-186
0x100	FMC_EXP_OP_CTRL	Extended operation control register	4-187
0x104	FMC_EXP_ADDRH	Upper-byte extended component address configuration register	4-188
0x108	FMC_EXP_ADDRL	Lower-four-byte extended component address configuration register	4-188
0x10C	FMC_EXP_DMA_SADDR_D0	DDR start address register 0 for extended DMA operations	4-189
0x110	FMC_EXP_DMA_SADDR_D1	DDR start address register 1 for extended DMA operations	4-189
0x114	FMC_EXP_DMA_SADDR_D2	DDR start address register 2 for extended DMA operations	4-189
0x118	FMC_EXP_DMA_SADDR_D3	DDR start address register 3 for extended DMA operations	4-190
0x11C	FMC_EXP_DMA_SADDR_OOB	DDR OOB information storage start address register for extended DMA operations	4-190
0x120	FMC_EXP_INT	Extended operation interrupt status register	4-191
0x124	FMC_EXP_INT_EN	Extended operation interrupt enable register	4-192
0x128	FMC_EXP_INT_CLR	Extended operation interrupt clear register	4-193
0x12C	FMC_EXP_ERR_NUM0_BUF0	Extended operation error correction information 0 statistics register for the first buffer operation	4-194
0x130	FMC_EXP_ERR_NUM1_BUF0	Extended operation error correction information 1 statistics register for the first buffer operation	4-195
0x13C	FMC_EXP_ERR_NUM0_BUF1	Extended operation error correction statistics register 0 for the second buffer operation	4-195

Offset Address	Register	Description	Page
0x140	FMC_EXP_ERR_NUM1_BUF1	Extended operation error correction statistics register 1 for the second buffer operation	4-196

4.2.8 Register Description

FMC_CFG

FMC_CFG is a component configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	FMC_CFG	0x0000_1820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					spi_nor_addr_mode	block_size		ecc_type			page_size		flash_sel		op_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[12:11]	RW	spi_nand_sel	Vendor of the SPI NAND flash, valid only when the internal ECC mode is used for the SPI NAND flash 01: Winbond 10: ESMT 11: Micron Other values: other vendors
[10]	RW	spi_nor_addr_mode	SPI address mode (valid only for the SPI NOR flash) 0 (default): 3-byte address mode 1: 4-byte address mode The reset value depends on the SFC_EMMC_BOOT_MODE pin.
[9:8]	RW	block_size	Block size of the NAND flash 00: 64 pages 01: 128 pages 10: 256 pages 11: 512 pages

[7:5]	RW	ecc_type	ECC type of the controller 000: no ECC 001: 8-bit ECC 010: 16-bit ECC 011: 24-bit ECC 100: 28-bit ECC 101: 40-bit ECC 110: 64-bit ECC 111: reserved
[4:3]	RW	page_size	Page size of the SPI NAND/NAND flash 00: 2 KB 01: 4 KB 10: 8 KB 11: 16 KB
[2:1]	RW	flash_sel	Flash type select 00: SPI NOR flash 01: SPI NAND flash 10: NAND flash 11: reserved The reset value depends on the BOOT_SEL0/BOOT_SEL1/SFC_DEVICE_MOD pin.
[0]	RW	op_mode	FMC operation mode 0: boot mode 1: normal mode

GLOBAL_CFG

GLOBAL_CFG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	GLOBAL_CFG	0x0000_00C4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sample_point				ddr_mode	reserved		edo_mode	rb_sel	cs_ctrl	wp_en	rd_delay			randomizer_en	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	sample_point	Sampling point select based on the delay parameter of the component in DDR mode. The frequency of the sampling clock is four times that of the interface read/write clock. The delay is the lowest when the field value is 0x0, and highest when the field value is 0xB. 0x0: The sampling point is 2 sampling clock cycles after the valid edge. 0x1: The sampling point is 2.5 sampling clock cycles after the valid edge. 0x2: The sampling point is 3 sampling clock cycles after the valid edge. 0x3: The sampling point is 3.5 sampling clock cycles after the valid edge. 0x4: The sampling point is 4 sampling clock cycles after the valid edge. 0x5: The sampling point is 4.5 sampling clock cycles after the valid edge. 0x6: The sampling point is 5 sampling clock cycles after the valid edge. 0x7: The sampling point is 5.5 sampling clock cycles after the valid edge. 0x8: The sampling point is 6 sampling clock cycles after the valid edge. 0x9: The sampling point is 6.5 sampling clock cycles after the valid edge. 0xA: The sampling point is 7 sampling clock cycles after the valid edge. 0xB: The sampling point is 7.5 sampling clock cycles after the valid edge. Other values: reserved

[11]	RW	ddr_mode	DDR mode enable 0: normal SDR mode 1: DDR mode
[10]	RO	reserved	Reserved
[9]	RW	edo_mode	Whether to use the EDO mode for the read operation of the NAND flash (the FMC needs to be set to the EDO mode if the NAND flash is switched to the EDO mode) 0: no 1: yes
[8]	RW	rb_sel	Whether multiple NAND flash memories share a read/busy signal. This field is valid when multiple external NAND flash memories (multiple CSs) are connected. 0: The NAND flash memories share a ready/busy signal. 1: The NAND flash memories use their own ready/busy signals. When only one NAND flash memory is connected, only ce0 and ready_busy 0 are used.
[7]	RW	cs_ctrl	CS control 0: The CS signal is always valid. 1: The CS signal is pulled up when the RB signal is pulled down and the component is in working status. The SPI does not support the RB signal. Therefore, the configuration is invalid for the SPI.
[6]	RW	wp_en	Write protection enable for the WP pin. When this bit is enabled, the chip outputs 0 to the WP pin. 0: disabled 1: enabled
[5:3]	RW	rd_delay	Number of delayed cycles (of the component working clock) for reading data from the SPI flash (in SDR mode) 000 (default): no delay 001: 0.5 cycle 010: 1 cycle 011: 1.5 cycles 100: 2 cycles 101: 2.5 cycles 110: 3 cycles 111: 3.5 cycles
[2]	RW	randomizer_en	Randomizer enable. The default value is 1. However, the logic automatically disables the randomizer when the page size is 2 KB or 4 KB. When the randomizer is enabled, data read/write from/to the flash is descrambled/scrambled. 0: disabled 1: enabled
[1:0]	RO	reserved	Reserved

TIMING_SPI_CFG

TIMING_SPI_CFG is an SPI timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	TIMING_SPI_CFG	0x0000_006F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				tcsh				tcss				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	tcss	CS setup time 000−111: (*n* + 1) interface clock cycles (*n* = 0, 1, 2, …, 7)
[3:0]	RW	tshsl	CS deselect time. It is equal to the interval between two flash operations. 0000−1111: (*n* + 1) interface clock cycles (*n* = 0, 1, 2, …, 15)

PND_PWIDTH_CFG

PND_PWIDTH_CFG is a read/write pulse width configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	PND_PWIDTH_CFG	0x0000_0333

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rw_hcnt				r_lcnt				w_lcnt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	rw_hcnt	High-level width of the read/write signal of the NAND flash 0x1−0xF: 2 to 16 interface clock cycles
[7:4]	RW	r_lcnt	Low-level width of the read signal of the NAND flash 0x1−0xF: 2 to 16 interface clock cycles
[3:0]	RW	w_lcnt	Low-level width of the write signal of the NAND flash 0x1−0xF: 2 to 16 interface clock cycles

PND_OPIDLE_CFG

PND_OPIDLE_CFG is an operation interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	PND_OPIDLE_CFG	0x0008_8880

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												frb_wait				cmd1_wait				addr_wait				cmd2_wait				wait_ready_wait			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	frb_wait	Number of delayed cycles after a read/write command is sent. After the delay, the ready signal is detected to check whether its level is high. Number of delayed interface clock cycles = frb_wait x 8
[15:12]	RW	cmd1_wait	Number of wait cycles after command 1 is sent Number of delayed interface clock cycles = cmd1_wait x 8
[11:8]	RW	addr_wait	Number of wait cycles after the address is sent 0x0−0xF: configured value Number of delayed interface clock cycles = addr_wait x 8
[7:4]	RW	cmd2_wait	Number of wait cycles after command 2 is sent Number of delayed interface clock cycles = cmd2_wait x 8
[3:0]	RW	wait_ready_wait	Number of delayed cycles after the level of the ready signal of the NAND flash is changed to high. After the delay, the read signal is sent to start the read operation. Number of delayed cycles = frb_idle x 2

FMC_INT

FMC_INT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	FMC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							cache_page_done_int	ahb_op_int	wr_lock_int	dma_err_int	err_alarm_int	err_inval_int	err_val_int	op_fail_int	op_done_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	cache_page_done_int	Interrupt generated when the cache read operation for data on one page of the NAND flash is complete 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	ahb_op_int	CPU read/write internal buffer interrupt enable when the FMC is reading/writing data from/to the flash memory 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	wr_lock_int	Lock address write operation interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	dma_err_int	DMA transfer bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	err_alarm_int	ECC alarm interrupt. An interrupt is generated when the number of error bits reaches the preset threshold. 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RO	err_inval_int	Uncorrectable ECC error interrupt In 8-bit ECC mode, if errors occur in eight or more bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in 16 or more bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in 24 or more bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in 28 or more bits of the checked 1024-byte data, an interrupt is generated. In 40-bit ECC mode, if errors occur in 40 or more bits of the checked 1024-byte data, an interrupt is generated. In 64-bit ECC mode, if errors occur in 64 or more bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err_val_int	Correctable ECC error interrupt In 8-bit ECC mode, if errors occur in one to eight bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in one to 16 bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in one to 24 bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in one to 28 bits of the checked 1024-byte data, an interrupt is generated. In 40-bit ECC mode, if errors occur in one to 40 bits of the checked 1024-byte data, an interrupt is generated. In 64-bit ECC mode, if errors occur in one to 64 bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	op_fail_int	Programming (timeout) failure interrupt in DMA mode 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	op_done_int	Current controller operation completion interrupt. This bit is automatically cleared when the operation register is written. 0: No interrupt is generated. 1: An interrupt is generated.

FMC_INT_EN

FMC_INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x001C	FMC_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							cache_page_done_int_en	ahb_op_int_en	wr_lock_int_en	dma_err_int_en	err_alarm_int_en	err_inval_int_en	err_val_int_en	op_fail_int_en	op_done_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	cache_page_done_int_en	Enable for the interrupt generated when the cache read operation for data on one page of the NAND flash is complete 0: disabled 1: enabled
[7]	RW	ahb_op_int_en	CPU read/write internal buffer error interrupt enable when the FMC is reading/writing data from/to the flash memory 0: disabled 1: enabled
[6]	RW	wr_lock_int_en	Lock address write error interrupt enable 0: disabled 1: enabled
[5]	RW	dma_err_int_en	DMA transfer bus error interrupt enable 0: disabled 1: enabled
[4]	RW	err_alarm_int_en	ECC alarm interrupt enable. An interrupt is generated when the number of error bits reaches the threshold 0: disabled 1: enabled
[3]	RW	err_inval_int_en	ECC uncorrectable error interrupt enable 0: disabled 1: enabled
[2]	RW	err_val_int_en	ECC correctable error interrupt enable 0: disabled 1: enabled

[1]	RW	op_fail_int_en	Programming operation failure interrupt enable 0: disabled 1: enabled
[0]	RW	op_done_int_en	Current operation completion interrupt enable of the FMC 0: disabled 1: enabled

FMC_INT_CLR

FMC_INT_CLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0020	FMC_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							cache_page_done_int_clr	ahb_op_int_clr	wr_lock_int_clr	dma_err_int_clr	err_alarm_int_clr	err_inval_int_clr	err_val_int_clr	op_fail_int_clr	op_done_int_clr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[8]	WO	cache_page_done_int_clr	cache_page_done interrupt clear. Writing 1 clears the interrupt.
[7]	WC	ahb_op_int_clr	ahb_op_err interrupt clear. Writing 1 clears the interrupt.
[6]	WO	wr_lock_int_clr	wr_lock_err interrupt clear. Writing 1 clears the interrupt.
[5]	WC	dma_err_int_clr	DMA transfer bus error interrupt clear. Writing 1 clears the interrupt.
[4]	WC	err_alarm_int_clr	err_alarm interrupt clear. Writing 1 clears the interrupt.
[3]	WC	err_inval_int_clr	err_invalid interrupt clear. Writing 1 clears the interrupt.
[2]	WC	err_val_int_clr	err_valid interrupt clear. Writing 1 clears the interrupt.
[1]	WC	op_fail_int_clr	op_fail interrupt clear. Writing 1 clears the interrupt.
[0]	WC	op_done_int_clr	op_done interrupt clear. Writing 1 clears the interrupt.

FMC_CMD

FMC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	FMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cmd2								cmd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	cmd2	Second command sent to the NAND flash by the FMC
[7:0]	RW	cmd1	First command sent to the NAND/SPI NOR/SPI NAND flash by the FMC

FMC_ADDRH

FMC_ADDRH is an upper-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	FMC_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	addrh	Upper bytes of the operation address for the SPI NAND flash

FMC_ADDRL

FMC_ADDRL is a lower-four-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	FMC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addrl	Lower four bytes of the operation address for the flash (component address for the SPI NOR flash)

FMC_OP_CFG

FMC_OP_CFG is an operation configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	FMC_OP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fm_cs	force_cs_en	mem_if_type		addr_num				dummy_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	fm_cs	CS corresponding to the flash to be operated 0: CS0 1: CS1
[10]	RW	force_cs_en	CS forcible pull-down enable 0: disabled 1: enabled
[9:7]	RW	mem_if_type	SPI flash interface type select (read operation) 000: standard SPI 001: dual-Input/Dual-output/SPI 010: dual I/O SPI 011: quad-Input/Dual-output/ SPI 100: quad I/O SPI 101−111: reserved

[6:4]	RW	addr_num	Number of bytes of the address sent to the flash
[3:0]	RW	dummy_num	Number of bytes to be operated for dummy_en (one byte is equivalent to two clock cycles in 4-wire mode, four clock cycles in 2-wire mode, or eight clock cycles in 1-wire mode)

SPI_OP_ADDR

SPI_OP_ADDR is an operation address configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	SPI_OP_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_op_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	spi_op_addr	Operation address of the SPI NOR/NAND flash. The operation address of the SPI flash is issued for each operation. This address is different from that described in FMC_ADDRL and FMC_ADDRH.

FMC_DATA_NUM

FMC_DATA_NUM is a data length register.

Offset Address	Register Name	Total Reset Value
0x0038	FMC_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				op_data_num											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	op_data_num	Length of data to be processed during one operation. This register needs to be configured when there is data transmission and does not need to be configured for the DMA operations and AHB direct access. This register is valid only in ECC0 mode.

FMC_OP

FMC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x003C	FMC_OP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							dummy_en	cmd1_en	addr_en	write_data_en	reserved			read_data_en	read_status_en	reg_op_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	dummy_en	Dummy byte transfer enable after the address operation is enabled 0: disabled 1: enabled
[7]	RW	cmd1_en	Enable for transmitting command 1 to the flash 0: disabled 1: enabled
[6]	RW	addr_en	Enable for writing the operation address to the flash 0: disabled 1: enabled
[5]	RW	write_data_en	Enable for writing data to the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[4]	RW	cmd2_en	Enable for sending command 2 to the NAND flash 0: disabled 1: enabled
[3]	RW	wait_ready_en	Enable for waiting the high-level ready/busy signal (for the NAND flash) 0: disabled 1: enabled
[2]	RW	read_data_en	Enable for reading data from the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.

[1]	RW	read_status_en	Read component status register enable. When this bit is set to 1, the command 0x70 for reading the status is sent to the NAND flash and the status data is read from the NAND flash. Then the returned data is written to the fm_status field of the NANDC status register instead of the internal buffer. 0: disabled 1: enabled
[0]	RWSC	reg_op_start	Controller status when commands are issued by configuring the FMC_OP register 0: The controller is ready. This bit can be set only to 1 when software issues the command, indicating that the logic is enabled. 1: The controller is busy. This bit is automatically set to 0 after the operation is complete, indicating that the logic is complete.

FMC_DMA_LEN

FMC_DMA_LEN is a DMA operation length register.

Offset Address	Register Name	Total Reset Value
0x0040	FMC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dma_len																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dma_len	Data transfer length during DMA operations (in byte) This field is used to configure the length of data in the spare data when the SPI NAND flash and NAND flash uses the ECC0 mode. This field is used to configured the length of data required for the DMA read/write operation of the SPI NOR flash.

FMC_DMA_AHB_CTRL

FMC_DMA_AHB_CTRL is a DMA AHB control register.

Offset Address	Register Name	Total Reset Value
0x0048	FMC_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													burst16_en	burst8_en	burst4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	burst16_en	Burst16 enable 0: disabled 1: enabled
[1]	RW	burst8_en	Burst8 enable 0: disabled 1: enabled
[0]	RW	burst4_en	Burst4 enable 0: disabled 1: enabled

FMC_DMA_SADDR_D0

FMC_DMA_SADDR_D0 is DDR start address register 0 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x004C	FMC_DMA_SADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d0	For the SPI NOR flash, this register indicates the DDR start address for DMA operations. For the SPI NAND flash, this register indicates the base address of DDR operation data for DMA operations.

FMC_DMA_SADDR_D1

FMC_DMA_SADDR_D1 is DDR start address register 1 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0050	FMC_DMA_SADDR_D1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d1	For the NAND flash, this register indicates base address 1 of the DDR operation data for DMA operations. The configuration is invalid when the page size is 2 KB or 4 KB.

FMC_DMA_SADDR_D2

FMC_DMA_SADDR_D2 is DDR start address register 2 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0054	FMC_DMA_SADDR_D2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d2	For the NAND flash, this register indicates base address 2 of the DDR operation data for DMA operations. The configuration is valid only when the page size is 16 KB.

FMC_DMA_SADDR_D3

FMC_DMA_SADDR_D3 is DDR start address register 3 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0058	FMC_DMA_SADDR_D3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d3	For the NAND flash, this register indicates base address 3 of the DDR operation data for DMA operations. The configuration is valid only when the page size is 16 KB.

FMC_DMA_SADDR_OOB

FMC_DMA_SADDR_OOB is a DDR OOB information storage start address register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x005C	FMC_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_oob	DDR base address for the OOB area that stores the data to be read or written

FMC_OP_CTRL

FMC_OP_CTRL is a DMA operation control register.

Offset Address	Register Name	Total Reset Value
0x0068	FMC_OP_CTRL	0x0003_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rd_opcode								wr_opcode								reserved				rd_op_sel		reserved			rw_op	dma_op_ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	rd_opcode	SPI NAND/SPI NOR flash, DMA read command, non-bus mode (FAST_READ/READ/DUAL_READ)
[15:8]	RW	wr_opcode	SPI NAND/SPI NOR flash, DMA write command
[7:6]	RO	reserved	Reserved
[5:4]	RW	rd_op_sel	Area of data to be read 00: Data on the entire page is read. 01: Only the OOB data is read. 10: reserved 11: reserved
[3:2]	RO	reserved	Reserved
[1]	RW	rw_op	DMA write/read mode select 0: DMA read mode 1: DMA write mode
[0]	RWSC	dma_op_ready	Controller status when commands are issued by configuring the FMC_OP_CTRL register 0: The controller is ready. This bit can be set only to 1 when software issues the command, indicating that the logic is enabled. 1: The controller is busy. This bit is automatically set to 0 after the operation is complete, indicating that the logic is complete.

FMC_TIMEOUT_WR

FMC_TIMEOUT_WR is a write operation timeout register.

Offset Address	Register Name	Total Reset Value
0x006C	FMC_TIMEOUT_WR	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								timeout_wr																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	timeout_wr	Program operation busy wait time, timeout period. The timeout period is in the unit of one interface clock cycle for the NAND /SPI NAND/SPI NOR flash.

FMC_OP_PARA

FMC_OP_PARA is an OP operation parameter selection register.

Offset Address	Register Name	Total Reset Value
0x0070	FMC_OP_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rd_oob_only	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rd_oob_only	Only the sector that stores the OOB information is read when the flash read command is issued.
[0]	RW	last_segment	The internal buffer operates only 8 KB data at a time. This bit indicates whether the last 8 KB data segment is transferred for the component with the page size greater than 8 KB (16 KB or greater). This bit is used when the operation data is 16 KB, and does not need to be configured for DMA operations. 0: The data segment that is being operated is not the last 8 KB data segment. 1: The data segment that is being operated is the last 8 KB data segment.

FMC_BOOT_SET

FMC_BOOT_SET is a boot setting register.

Offset Address	Register Name	Total Reset Value
0x0074	FMC_BOOT_SET	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											boot_otp_cfg	device_ecc_sel	two_image_boot	boot_quad_mode	boot_page0_cfg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	boot_otp_cfg	Component configuration information, that is, the mode in which the fmc_cfg register is configured 0: adaptive boot mode 1: OTP mode
[3]	RW	device_ecc_sel	Whether to use the internal ECC for the SPI NAND flash 0: no 1: yes
[2]	RW	two_image_boot	Whether to use the dual-image boot mode for the NAND flash 0: no 1: yes
[1]	RW	boot_quad_mode	Whether to use the 4-wire boot mode for the SPI NAND flash. The reset value depends on the SFC_EMMC_BOOT_MODE pin. 0: no. The 1-wire boot mode is used. 1: yes
[0]	RW	boot_page0_cfg	Data format conversion enable for the NAND/SPI NAND flash 0: The data format is not converted. The traversal operation is not performed during the boot process. 1: The data format is adaptively converted. The traversal operation is performed during the boot process.

FMC_LP_CTRL

FMC_LP_CTRL is a low-power control register.

Offset Address	Register Name	Total Reset Value
0x0078	FMC_LP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clk_gate_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	clk_gate_en	Clock gating select. If the clock gating is enabled, the low-power design is used and the module working clocks are disabled by logic. 0: All clocks are enabled. 1: Clocks are disabled according to the low-power design.

FMC_LOCK

FMC_LOCK is a lock address configuration register.

Offset Address	Register Name	Total Reset Value
0x007C	FMC_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lock_excmd_en	lock_en	global_lock_en	lock_down
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	lock_excmd_en	Address write-protection enable for the extended write command (new command added for new components) 0: disabled 1: enabled

[2]	RW	lock_en	Flash lock enable 0: disabled 1: enabled
[1]	RW	global_lock_en	Flash global lock enable 0: disabled 1: enabled
[0]	RW	lock_down	Flash lock mode 0: lock mode 1: lock-down mode. This bit retains the value 1 after it is set to 1 once. It can be set to 0 only during hardware reset.

FMC_LOCK_SA0

FMC_LOCK_SA0 is a lock start address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x0080	FMC_LOCK_SA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_saddr0																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_saddr0	Lock start address 0, corresponding to the page address

FMC_LOCK_EA0

FMC_LOCK_EA0 is a lock end address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x0084	FMC_LOCK_EA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_eaddr0																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_eaddr0	Lock end address 0, corresponding to the page address

FMC_LOCK_SA1

FMC_LOCK_SA1 is a lock start address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x0088	FMC_LOCK_SA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_saddr1																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_saddr1	Lock start address 1, corresponding to the page address

FMC_LOCK_EA1

FMC_LOCK_EA1 is a lock end address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x008C	FMC_LOCK_EA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_eaddr1																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_eaddr1	Lock end address 1, corresponding to the page address

FMC_LOCK_SA2

FMC_LOCK_SA2 is a lock start address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x0090	FMC_LOCK_SA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_saddr2																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:0]	RW	flash_lock_saddr2	Lock start address 2, corresponding to the page address

FMC_LOCK_EA2

FMC_LOCK_EA2 is a lock end address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	FMC_LOCK_EA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_eaddr2																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_eaddr2	Lock end address 2, corresponding to the page address

FMC_LOCK_SA3

FMC_LOCK_SA3 is a lock start address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x0098	FMC_LOCK_SA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_saddr3																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_saddr3	Lock start address 3, corresponding to the page address

FMC_LOCK_EA3

FMC_LOCK_EA3 is a lock end address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x009C	FMC_LOCK_EA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								flash_lock_eaddr3																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	flash_lock_eaddr3	Lock end address 3, corresponding to the page address

FMC_EXPCMD

FMC_EXPCMD is an extended page command register.

Offset Address	Register Name	Total Reset Value
0x00A0	FMC_EXPCMD	0x8080_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ex_pcmd3								ex_pcmd2								ex_pcmd1								ex_pcmd0							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ex_pcmd3	Write command 3 for the flash extended page
[23:16]	RW	ex_pcmd2	Write command 2 for the flash extended page
[15:8]	RW	ex_pcmd1	Write command 1 for the flash extended page
[7:0]	RW	ex_pcmd0	Write command 0 for the flash extended page

FMC_EXBCMD

FMC_EXBCMD is an extended block command register.

Offset Address	Register Name	Total Reset Value
0x00A4	FMC_EXBCMD	0x0000_6060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ex_bcmd1								ex_bcmd0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:8]	RW	ex_bcmd1	Write command 1 for the flash extended block
[7:0]	RW	ex_bcmd0	Write command 0 for the flash extended block

FMC_ERR_THD

FMC_ERR_THD is an ECC alarm threshold register.

Offset Address	Register Name	Total Reset Value
0x00A8	FMC_ERR_THD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_thd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fmc_err_thd	ECC alarm threshold. When the number of error bits reaches the threshold, an ECC alarm interrupt is triggered. NOTE • If an uncorrectable ECC error occurs, an uncorrectable interrupt is reported regardless of the register value. • When the register value is set to 0 or 1, an alarm interrupt is reported as long as an error occurs. • When the configured value exceeds the number of correctable error bits, no alarm interrupt is reported regardless of the number of error bits. Only the correctable error interrupt and uncorrectable error interrupt are generated.

FMC_FLASH_INFO

FMC_FLASH_INFO is a component status register.

Offset Address	Register Name	Total Reset Value
0x00AC	FMC_FLASH_INFO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_bb_flag								bb_flag								exp_flash_status								flash_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	exp_bb_flag	Uncorrected data corresponding to the bad block flag of the current page when the extended operation of reading only the OOB data or reading the page is issued

[23:16]	RO	bb_flag	Uncorrected data corresponding to the bad block flag of the current page when the only the OOB data or the page is read
[15:8]	RO	exp_flash_status	Status register value read by the FMC from the flash during extended operations
[7:0]	RO	flash_status	Status register value read by the FMC from the flash during normal operations. For details about the meanings of bits 7–0, see the flash component manual.

FMC_OP_CNT

FMC_OP_CNT is an FMC operation issuing times register.

Offset Address	Register Name	Total Reset Value
0x00B8	FMC_OP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																op_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	op_cnt	Times of operations on the component. The counter increases by 1 each time the operation register is configured. The count value remains unchanged when the maximum value is reached. Reading this field clears the count value. This register is used only for debugging.

FMC_VERSION

FMC_VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x00BC	FMC_VERSION	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	FMC V100

FMC_ERR_NUM0_BUF0

FMC_ERR_NUM0_BUF0 is an SPI NAND flash and NAND flash error correction information 0 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00C0	FMC_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf0	Error bit count for the first 4 KB data during the first buffer operation of the NAND flash with the page size of 2 KB, 4 KB, 8 KB, or 16 KB bit[31:24]: number of error bits in the fourth 1 KB data segment bit[23:16]: number of error bits in the third 1 KB data segment bit[15:8]: number of error bits in the second 1 KB data segment bit[7:0]: number of error bits in the first 1 KB data segment

FMC_ERR_NUM1_BUF0

FMC_ERR_NUM1_BUF0 is a NAND flash error correction information 1 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00C4	FMC_ERR_NUM1_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num1_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf0	Error bit count for the last 4 KB data during the first buffer operation of the NAND flash with the page size of 8 KB or 16 KB bit[31:24]: number of error bits in the eighth 1 KB data segment bit[23:16]: number of error bits in the seventh 1 KB data segment bit[15:8]: number of error bits in the sixth 1 KB data segment bit[7:0]: number of error bits in the fifth 1 KB data segment

FMC_ERR_NUM0_BUF1

FMC_ERR_NUM0_BUF1 is NAND flash error correction statistics register 0 for the second buffer operation.

Offset Address	Register Name	Total Reset Value
0x00C8	FMC_ERR_NUM0_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf1	Error bit count register 0 during the second buffer operation of the NAND flash with the page size of 16 KB bit[31:24]: number of error bits in the fourth 1 KB data segment bit[23:16]: number of error bits in the third 1 KB data segment bit[15:8]: number of error bits in the second 1 KB data segment bit[7:0]: number of error bits in the first 1 KB data segment

FMC_ERR_NUM1_BUF1

FMC_ERR_NUM1_BUF1 is NAND flash error correction statistics register 1 for the second buffer operation.

Offset Address	Register Name	Total Reset Value
0x00CC	FMC_ERR_NUM1_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num1_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num1_buf1	Error bit count register 1 during the second buffer operation of the NAND flash with the page size of 16 KB bit[31:24]: number of error bits in the eighth 1 KB data segment bit[23:16]: number of error bits in the seventh 1 KB data segment bit[15:8]: number of error bits in the sixth 1 KB data segment bit[7:0]: number of error bits in the fifth 1 KB data segment

FMC_ERR_ALARM_ADDRH

FMC_ERR_ALARM_ADDRH is an upper-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D0	FMC_ERR_ALARM_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_alarm_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_err_alarm_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ERR_ALARM_ADDRL

FMC_ERR_ALARM_ADDRL is a lower-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D4	FMC_ERR_ALARM_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fmc_err_alarm_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fmc_err_alarm_addrl	Lower bytes of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ECC_INVALID_ADDRH

FMC_ECC_INVALID_ADDRH is an upper-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00D8	FMC_ECC_INVALID_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_ecc_invalid_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_ecc_invalid_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

FMC_ECC_INVALID_ADDRL

FMC_ECC_INVALID_ADDRL is a lower-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00DC	FMC_ECC_INVALID_ADDRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fmc_ecc_invalid_addrl							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	fmc_ecc_invalid_addrl	Lower bytes of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

FMC_READ_TIMING_TUNE

FMC_READ_TIMING_TUNE is a sampling point tuning register during the async NAND read operation.

Offset Address	Register Name	Total Reset Value
0x0E0	FMC_READ_TIMING_TUNE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							read_timing_tune
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved
[2:0]	RW	read_timing_tune	Sampling data tuning by software during the async NAND read operation. The number of delayed interface clock cycles for the sampling point when data is read from the async NAND flash is determined based on the current interface frequency and internal delay. 000: no delay. Data is sampled at the rising edge of the rd signal. 001: Data is sampled one interface clock cycle after the rising edge of the rd signal. 010: Data is sampled two interface clock cycles after the rising

			edge of the rd signal. 011: Data is sampled three interface clock cycles after the rising edge of the rd signal. 100: Data is sampled four interface clock cycles after the rising edge of the rd signal. 101: Data is sampled five interface clock cycles after the rising edge of the rd signal. 110: Data is sampled six interface clock cycles after the rising edge of the rd signal. 111: Data is sampled seven interface clock cycles after the rising edge of the rd signal.

FMC_EXP_OP_CTRL

FMC_EXP_OP_CTRL is an extended operation control register.

Offset Address	Register Name	Total Reset Value
0x100	FMC_EXP_OP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										exp_rd_op_sel		reserved			exp_rw_op	exp_dma_op_ready	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	exp_rd_op_sel	Area of data to be read (extended operation) 00: Data on the entire page is read. 01: Only the OOB data is read. 1X: reserved
[3:2]	RO	reserved	Reserved
[1]	RW	exp_rw_op	Issued component read/write type (extended operation) 0: DMA read operation 1: DMA write operation

[0]	RWSC	exp_dma_op_ready	Enable for issuing operations 0: The FMC is ready (this bit is automatically cleared by the FMC). 1: The FMC is busy (this bit is set to 1 by software). This bit is set to 1 when software issues operations, and is automatically cleared by the FMC after the operation is complete. Software can set this bit only to 1.

FMC_EXP_ADDRH

FMC_EXP_ADDRH is an upper-byte extended component address configuration register.

Offset Address	Register Name	Total Reset Value
0x104	FMC_EXP_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								exp_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	exp_addrh	Upper bytes of the operation address of the flash (extended operation)

FMC_EXP_ADDRL

FMC_EXP_ADDRL is a lower-four-byte extended component address configuration register. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x108	FMC_EXP_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_addrl	Lower four bytes of the operation address of the flash (extended operation)

FMC_EXP_DMA_SADDR_D0

FMC_EXP_DMA_SADDR_D0 is DDR start address register 0 for extended DMA operations. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x10C	FMC_EXP_DMA_SADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d0	Base address of DDR operation data during extended DMA operations for the SPI NAND flash

FMC_EXP_DMA_SADDR_D1

FMC_EXP_DMA_SADDR_D1 is DDR start address register 1 for extended DMA operations.

Offset Address	Register Name	Total Reset Value
0x110	FMC_EXP_DMA_SADDR_D1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d1	Base address 1 of the DDR operation data during extended DMA operations for the NAND flash. The configuration is invalid when the page size is 2 KB or 4 KB.

FMC_EXP_DMA_SADDR_D2

FMC_EXP_DMA_SADDR_D2 is DDR start address register 2 for extended DMA operations. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x114	FMC_EXP_DMA_SADDR_D2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d2	Base address 2 of the DDR operation data during extended DMA operations for the NAND flash. The configuration is valid only when the page size is 16 KB.

FMC_EXP_DMA_SADDR_D3

FMC_EXP_DMA_SADDR_D3 is DDR start address register 3 for extended DMA operations.

Offset Address	Register Name	Total Reset Value
0x118	FMC_EXP_DMA_SADDR_D3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_d3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_d3	Base address 3 of the DDR operation data during extended DMA operations for the NAND flash. The configuration is valid only when the page size is 16 KB.

FMC_EXP_DMA_SADDR_OOB

FMC_EXP_DMA_SADDR_OOB is a DDR OOB information storage start address register for extended DMA operations. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x11C	FMC_EXP_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	exp_dma_mem_saddr_oob	DDR base address for reading/writing data in the OOB area (extended operation)

FMC_EXP_INT

FMC_EXP_INT is an extended operation interrupt status register.

Offset Address	Register Name	Total Reset Value
0x120	FMC_EXP_INT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5	4	3	2	1	0
Name	reserved							exp_dma_err_int	exp_err_alarm_int	exp_err_inval_int	exp_err_val_int	exp_op_fail_int	exp_op_done_int
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RO	exp_dma_err_int	DMA transfer bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	exp_err_alarm_int	ECC alarm interrupt. An interrupt is generated when the number of error bits reaches the configured threshold. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	exp_err_inval_int	Uncorrectable ECC error interrupt In 8-bit ECC mode, an interrupt is generated when there are eight or more error bits in the checked 1024-byte data. In 16-bit ECC mode, an interrupt is generated when there are 16 or more error bits in the checked 1024-byte data. In 24-bit ECC mode, an interrupt is generated when there are 24 or more error bits in the checked 1024-byte data. In 28-bit ECC mode, an interrupt is generated when there are 28 or more error bits in the checked 1024-byte data. In 40-bit ECC mode, an interrupt is generated when there are 40 or more error bits in the checked 1024-byte data. In 64-bit ECC mode, an interrupt is generated when there are 64 or more error bits in the checked 1024-byte data. 0: No interrupt is generated. 1: An interrupt is generated.

[2]	RO	exp_err_val_int	Correctable ECC error interrupt In 8-bit ECC mode, an interrupt is generated when there are 1−8 error bits in the checked 1024-byte data. In 16-bit ECC mode, an interrupt is generated when there are 1−16 error bits in the checked 1024-byte data. In 24-bit ECC mode, an interrupt is generated when there are 1−24 error bits in the checked 1024-byte data. In 28-bit ECC mode, an interrupt is generated when there are 1−28 error bits in the checked 1024-byte data. In 40-bit ECC mode, an interrupt is generated when there are 1−40 error bits in the checked 1024-byte data. In 64-bit ECC mode, an interrupt is generated when there are 1−64 error bits in the checked 1024-byte data. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	exp_op_fail_int	Programming failure interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	exp_op_done_int	Current extended FMC operation completion interrupt This bit is automatically cleared when the operation register is written. 0: No interrupt is generated. 1: An interrupt is generated.

FMC_EXP_INT_EN

FMC_EXP_INT_EN is an extended operation interrupt enable register. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x124	FMC_EXP_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										exp_dma_err_int_en	exp_err_alarm_int_en	exp_err_inval_int_en	exp_err_val_int_en	exp_op_fail_int_en	exp_op_done_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	exp_dma_err_int_en	DMA transfer bus error interrupt enable 0: disabled 1: enabled
[4]	RW	exp_err_alarm_int_en	ECC alarm interrupt enable. An interrupt is generated when the number of error bits reaches the configured threshold. 0: disabled 1: enabled
[3]	RW	exp_err_inval_int_en	Uncorrectable ECC error interrupt enable 0: disabled 1: enabled
[2]	RW	exp_err_val_int_en	Correctable ECC error interrupt enable 0: disabled 1: enabled
[1]	RW	exp_op_fail_int_en	Programming failure interrupt enable 0: disabled 1: enabled
[0]	RW	exp_op_done_int_en	Current extended FMC operation completion interrupt enable 0: disabled 1: enabled

FMC_EXP_INT_CLR

FMC_EXP_INT_CLR is an extended operation interrupt clear register. This register is used only for internal reference.

Offset Address	Register Name	Total Reset Value
0x128	FMC_EXP_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										exp_dma_err_int_clr	exp_err_alarm_int_clr	exp_err_inval_int_clr	exp_err_val_int_clr	exp_op_fail_int_clr	exp_op_done_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	WO	exp_dma_err_int_clr	DMA transfer bus error interrupt clear. Writing 1 clears the interrupt.
[4]	WO	exp_err_alarm_int_clr	exp_err_alarm interrupt clear. Writing 1 clears the interrupt.
[3]	WO	exp_err_inval_int_clr	exp_err_invalid interrupt clear. Writing 1 clears the interrupt.
[2]	WO	exp_err_val_int_clr	exp_err_valid interrupt clear. Writing 1 clears the interrupt.
[1]	WO	exp_op_fail_int_clr	exp_op_fail interrupt clear. Writing 1 clears the interrupt.
[0]	WO	exp_op_done_int_clr	exp_op_done interrupt clear. Writing 1 clears the interrupt.

FMC_EXP_ERR_NUM0_BUF0

FMC_EXP_ERR_NUM0_BUF0 is an extended operation error correction information 0 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x12C	FMC_EXP_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	exp_err_num0_buf0	Error bit count for the first 4 KB data during the first buffer operation of the flash with the page size of 2 KB, 4 KB, 8 KB, or 16 KB bit[31:24]: number of error bits in the fourth 1 KB data segment bit[23:16]: number of error bits in the third 1 KB data segment bit[15:8]: number of error bits in the second 1 KB data segment bit[7:0]: number of error bits in the first 1 KB data segment

FMC_EXP_ERR_NUM1_BUF0

FMC_EXP_ERR_NUM1_BUF0 is an extended operation error correction information 1 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x130	FMC_EXP_ERR_NUM1_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num1_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	exp_err_num1_buf0	Error bit count for the last 4 KB data during the first buffer operation of the flash with the page size of 8 KB or 16 KB bit[31:24]: number of error bits in the eighth 1 KB data segment bit[23:16]: number of error bits in the seventh 1 KB data segment bit[15:8]: number of error bits in the sixth 1 KB data segment bit[7:0]: number of error bits in the fifth 1 KB data segment

FMC_EXP_ERR_NUM0_BUF1

FMC_EXP_ERR_NUM0_BUF1 is an extended operation error correction statistics register 0 for the second buffer operation.

Offset Address	Register Name	Total Reset Value
0x13C	FMC_EXP_ERR_NUM0_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num0_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	exp_err_num0_buf1	Error bit count register 0 during the second buffer operation of the flash with the page size of 16 KB bit[31:24]: number of error bits in the fourth 1 KB data segment bit[23:16]: number of error bits in the third 1 KB data segment bit[15:8]: number of error bits in the second 1 KB data segment bit[7:0]: number of error bits in the first 1 KB data segment

FMC_EXP_ERR_NUM1_BUF1

FMC_EXP_ERR_NUM1_BUF1 is an extended operation error correction statistics register 1 for the second buffer operation.

Offset Address	Register Name	Total Reset Value
0x140	FMC_EXP_ERR_NUM1_BUF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_err_num1_buf1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	exp_err_num1_buf1	Error bit count register 1 during the second buffer operation of the flash with the page size of 16 KB bit[31:24]: number of error bits in the eighth 1 KB data segment bit[23:16]: number of error bits in the seventh 1 KB data segment bit[15:8]: number of error bits in the sixth 1 KB data segment bit[7:0]: number of error bits in the fifth 1 KB data segment

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Tables

5 GSF

5.1 Overview

The gigabit switch fabric (GSF) receives and transmits data over two Ethernet ports at 10/100/1000 Mbit/s in full-duplex or half-duplex mode. The Ethernet port exchanges data with the CPU port, and supports the energy efficient Ethernet (EEE) and wake on LAN (WoL) functions.

5.2 Function Description

The GSF has the following features:

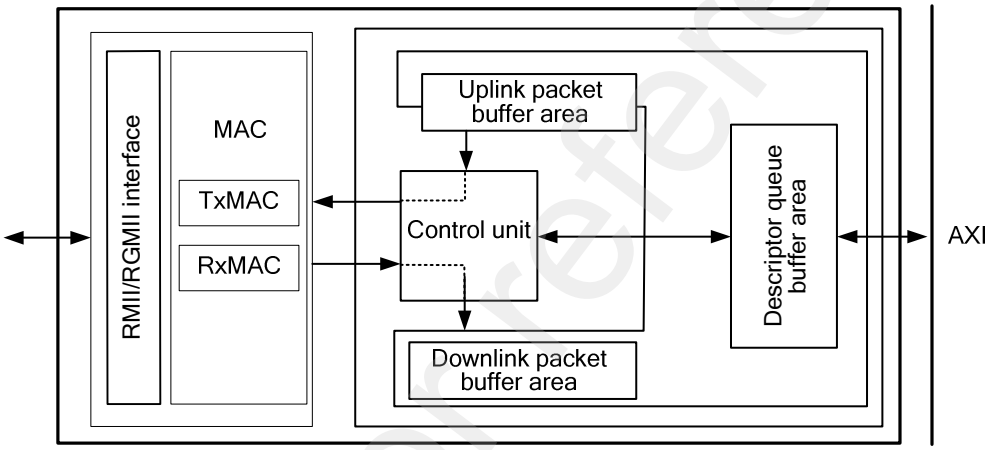
- Supports 10/100/1000 Mbit/s rate.
- Supports the full-duplex or half-duplex mode.
- Supports the reduced media independent interface (RMII), and reduced gigabit media independent interface (RGMII) interfaces.
- Provides the management data input/output (MDIO) interface.
- Supports frame length effectiveness detection and discards long and short frames.
- Supports the cyclic redundancy check (CRC) on receive (RX) frames and discards frames with CRC errors.
- Supports the CRC on transmit (TX) frames.
- Supports short frame filling.
- Supports outloop (that is, line-side loopback) in full-duplex mode.
- Supports count of RX and TX frames.
- Supports filtering of broadcast, multicast, and unicast frames.
- Supports configurable speed control processing of the control packets, IP packets, and broadcast or multicast packets.
- Supports packet filtering.
- Supports the enqueue interrupt and timeout interrupt modes.
- Supports buffer of RX and TX packets.
- Supports EEE.
- Supports WoL.
- Supports scatter gather (SG).

- Supports the checksum offload engine (COE) in the RX and TX directions.
- Supports TCP segment offload (TSO).
- Supports UDP fragment offload (UFO).

5.3 General Data Flow

Figure 5-1 shows the overall data flow of the GSF GE ports.

Figure 5-1 GSF general data flow



5.4 Port Function Configuration Description

5.4.1 Managing RX and TX Frames

The CPU manages addresses for storing RX and TX frames by configuring the descriptor queue buffer area.

- During reception, the Ethernet module checks whether data packets received from external networks are valid, and then stores the valid packets to the device description repository (DDR) over the bus based on the packet buffer information, including the start address for the packet buffer and packet buffer depth, configured by the CPU.
- During transmission, the Ethernet module obtains the corresponding packets in the DDR over the bus based on the packet buffer information, including the start address for the packet buffer and packet length, configured by the CPU, then packages and transmits the packets to network interfaces.

5.4.2 Configuring Descriptor Queues in RX and TX DDR Buffers

During transmission, the CPU configures the two buffer queues stored in the DDR. During reception, the CPU configures another two buffer queues. The start addresses for the buffer queues are word addresses. A descriptor contains four words and specifies the information

about a packet buffer. Table 5-1 describes the data structure of the first two words in the descriptor of the RX and TX buffers.

Table 5-1 Data structure of the first two words in the descriptor of the RX and TX buffers

Name	Width (Bit)	Description
DataBudSAddr	32	Start address of the packet buffer. The byte address format is supported.
DescVld	1	Whether the flag of the descriptor is valid 0: invalid 1: valid
DataLen	11	Valid data volume in the packet buffer (unit: byte)
BufLen	11	Packet buffer depth (unit: byte)

NOTE

The maximum frame length in the RX direction is 1.6 KB, and therefore the space allocated for storing each frame must be greater than 1.6 KB. It is recommended that the space for storing each frame be (1600 + 128) bytes to ensure sufficient space for storing network packet data.

Table 5-2 Data structure of the first two words in the TX buffer

Name	Bit	Bit Name	Description
desc_word1	[31:0]	DataBufSAddr	If the current descriptor is a non-SG descriptor, this bit indicates the start address of the packet buffer. If the current descriptor is an SG descriptor, this bit indicates the start address of the Level-2 linked list.
desc_word2	[31]	hw_own	Ownership of the current descriptor 0: software 1: logic
	[30]	sg_flag	Whether the SG is supported 0: not supported 1: supported Note: When sg_flag is set to 0, tso_flag must be set to 0.
	[29]	coe_flag	Whether checksum offload is executed 0: no 1: yes
	[28]	tso_flag	Whether TSO is executed 0: no 1: yes

Name	Bit	Bit Name	Description
	[27]	reserved	Reserved
	[26:16]	data_len	When sg_flag is set to 1, this bit indicates the size of the mss in the fragmented packet. When sg_flag is set to 0, this bit indicates the size of the whole packet.
	[15:11]	nfrags_num	Number of nfrags in the SK buffer specified by the current descriptor. The maximum number is 17.
	[10]	vlan_flag	Whether the current packet has a VLAN flag 0: no 1: yes
	[9]	ip_version	IP protocol version of the current packet 0: IPv4 1: IPv6
	[8]	protocol_type	Type of the transmission layer protocol of the current packet 0: TCP 1: UDP
	[7:4]	ip_hdr_len	Length of the IP header of the current packet, in the unit of word (four bytes) If the current packet is an IPv4 packet, the length of the IP header is 5 to 15 words. If the current packet is an IPv6 packet, the length of the IP header is 10 words.
	[3:0]	protocol_hdr_len	If the current packet is a TCP packet, this bit indicates the length of the TCP header, in the unit of word (four bytes). The length ranges from 5 to 15 words. If the current packet is a UDP packet, this bit indicates the length of the UDP header, in the unit of word (four bytes). The length is two words.

5.4.3 Managing RX Interrupts

Generating Interrupts

If the RX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, an RX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the rx_bq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[17].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[7:0].

  Enable the RX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, an RX timeout interrupt is generated. If the requirements for triggering the RX enqueue and timeout interrupts are met, only the RX enqueue interrupt is generated.
- Enable the rx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[28].
- Configure the rx_bq enqueue timeout raw interrupt threshold register RX_BQ_IN_TIMEOUT_TH.

Clearing Interrupts

After the CPU receives an RX enqueue interrupt or RX timeout interrupt, it writes 1 to clear the RX enqueue interrupt and RX timeout interrupt.

5.4.4 Managing TX Interrupts

Generating Interrupts

If the TX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, a TX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the tx_rq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[19].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[23:16].
- Enable the TX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, a TX timeout interrupt is generated. If the requirements for triggering the TX enqueue and timeout interrupts are met, only the TX enqueue interrupt is generated.
- Enable the tx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[29].
- Configure the tx_rq enqueue timeout raw interrupt threshold register TX_RQ_IN_TIMEOUT_TH.

Clearing Interrupts

After the CPU receives a TX enqueue interrupt or TX timeout interrupt, it writes 1 to clear the TX enqueue interrupt and TX timeout interrupt.

5.4.5 Configuring the Working Status of the PHY Chip

The GSF provides the MDIO interface to manage the physical layer entity sublayer (PHY) chip. The PHY chip can be written or read through the MDIO interface.

The procedure for reading the PHY chip is as follows:

- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[12:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 2'b10 to start the MDIO read operation.
- The MDIO writes the data read from the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0.
- The CPU queries the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] to obtain the data read by the MDIO from the external PHY chip.

The procedure for writing the PHY chip is as follows:

- The CPU writes the data to be transmitted to the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0].
- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[9:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 1 to start the MDIO write operation.
- The MDIO writes the value of the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0] to the corresponding PHY internal registers and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0x0.

5.4.6 Switching Operating Modes

The GSF supports the following operating modes and switches between the modes: RMII (10/100 Mbit/s), and RGMII (10/100/1000 Mbit/s). The operating mode is switched as follows:

Step 1 Set the corresponding GSF clock and soft reset control register 0x120100CC PERI_CRG51 to 0xe implement the reset, configure bit[8:0] of the GMAC interface control register PERI_CRG59, and set PERI_CRG51 to 0xa to clear the reset so that the configured operating mode takes effect.

Step 2 Enable the MODE_CHANGE_EN register, configure the MAC port rate mode register PORT_MODE, and then disable the MODE_CHANGE_EN register.

NOTE

Do not perform the configuration when the chip is working properly. You are advised to perform the configuration when the chip is initialized.

----End

5.5 Typical Applications

5.5.1 Ethernet Flow Control

The GSF can control the RX packet flow. That is, the GSF discards the subsequent packets when the number of RX packets exceeds the preset maximum quantity.

The GSF controls the flow of the following three types of packets:

- Control packets
- Service packets
- Multicast or broadcast packets

Flow Control of the Control Packets

The flow of control packets is controlled in the following scenarios:

- Within a specified time segment (indicated by T), a limited number of control packets are allowed to pass through. When the count exceeds the configured upper threshold, the subsequent packets are discarded. The time limit T is measured by 125 μs, which is equal to the configured upper threshold.
- If the number of RX addresses of the RX configuration FIFO is less than the number of limited addresses, all RX control packets pass through preferentially. IP packets are filtered out and discarded no matter whether the IP packet flow is controlled or the number of IP packets reaches the configured upper threshold for flow control.

To control the flow of control packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[20] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[15:0].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].
- Configure the flow control RX address count register CRF_RX_LEFT_NUM.

Flow Control of Service Packets

The flow control of service packets is the same as that of control packets in the first scenario. In the second scenario, all IP packets will be discarded.

To control the flow of service packets (for example, IP packets), the following configurations are required:

- Set the control register CONTROL_WORD bit[21] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[31:16].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].

Flow Control of Broadcast or Multicast Packets

The time limit for flow control of broadcast or multicast packets is 1 μs. Within the time limit, if the count of packets passing through exceeds the upper threshold, the subsequent broadcast or multicast packets are discarded.

To control the flow of broadcast or multicast packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[16] to 1.
- Configure the flow control packet count register for broadcast or multicast packets CRF_BM_PKT_THRSLD.
- Configure the flow control time threshold register for broadcast and multicast packets CRF_BM_TIME_THRSLD.

5.5.2 WoL

The WoL supports wake-up using wake-up frames and magic packets.

Wake_up Frame

The following describes how to configure the filter template by using template 1 as an example (four templates in total):

- Configure valid byte selection register 1 FILTER_0_BYTE_MASK.
- Configure filter template enable register 1 FILTER_COMMAND.
- Configure the CRC position offset register FILTER_OFFSET.
- Configure the software-expected CRC value register FILTER0_1_CRC.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[2] to 1 to enable wake_up frame reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a wake-up frame is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

Magic Packet

To receive magic packets, the following configurations are required:

- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode, and set PMT_CTRL_STAUTS bit[1] to 1 to enable the magic packet reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a magic packet is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

5.6 Register Summary

Table 5-3 describes GSF registers.

Table 5-3 Summary of GSF registers (base address: 0x1005_0000)

Offset Address	Register	Description	Page
0x00000000	STATION_ADDR_LOW	Local MAC address register	5-17
0x00000004	STATION_ADDR_HIGH	Local MAC address register	5-17
0x00000008	DUPLEX_SEL_RGMII	Half-duplex selection register	5-18
0x0000000C	FD_FC_TYPE	Flow control frame type domain register	5-18
0x00000014	COL_DISTANCE	Single retransmission packet length threshold register	5-19
0x0000001C	FC_TX_TIMER	Flow control time parameter register	5-19
0x00000020	FD_FC_ADDR_LOW	Flow control frame destination address lower 32 bits register	5-19
0x00000024	FD_FC_ADDR_HIGH	Flow control frame destination address upper 16 bits register	5-20
0x00000030	IPG_TX_TIMER	TX frame inter-packet gap (IPG) register	5-20
0x00000038	PAUSE_THR	TX flow control frame IPG register	5-21
0x0000003C	MAX_FRM_SIZE	Maximum frame length register	5-21
0x00000040	PORT_MODE	Port status register	5-22
0x00000044	PORT_EN	Channel enable register	5-22
0x00000048	PAUSE_EN	Flow control enable register	5-23
0x00000050	SHORT_RUNTS_THR	Short frame threshold register	5-23
0x00000054	DROP_UNK_CTL_FRM	Drop enable register for unknown control frames	5-24
0x00000060	TRANSMIT_CONTROL	Common configuration register	5-24
0x00000064	REC_FILT_CONTROL	RX frame filter control register	5-25
0x00000068	PORT_MC_ADDR_LOW	Multicast address register	5-26
0x0000006C	PORT_MC_ADDR_HIGH	Multicast address register	5-26
0x00000070	MAC_CLR	MAC clear register	5-27
0x00000080	RX_OCTETS_OK_CNT	Byte count register for valid RX frames	5-27

Offset Address	Register	Description	Page
0x00000084	RX_OCTETS_BAD_CNT	Byte count register for error RX frames	5-28
0x00000088	RX_UC_PKTS	MAC frame count register for RX unicast frames	5-28
0x0000008C	RX_MC_PKTS	Frame count register for RX multicast frames	5-28
0x00000090	RX_BC_PKTS	Frame count register for RX broadcast frames	5-29
0x00000094	RX_PKTS_64OCTETS	Frame count register for RX 64-byte frames	5-29
0x00000098	RX_PKTS_65TO127OCTETS	Frame count register for RX frames ranging from 65 bytes to 127 bytes in length	5-29
0x0000009C	RX_PKTS_128TO255OCTETS	Frame count register for RX frames ranging from 128 bytes to 255 bytes in length	5-30
0x000000A0	RX_PKTS_255TO511OCTETS	Frame count register for RX frames ranging from 256 bytes to 511 bytes in length	5-30
0x000000A4	RX_PKTS_512TO1023OCTETS	Frame count register for RX frames ranging from 512 bytes to 1023 bytes in length	5-30
0x000000A8	RX_PKTS_1024TO1518OCTETS	Frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length	5-31
0x000000AC	RX_PKTS_1519TOMAXOCTETS	Frame count register for RX frames ranging from 1519 bytes to the maximum in length	5-31
0x000000B0	RX_FCS_ERRORS	Frame count register for RX frames with CRC errors	5-32
0x000000B4	RX_TAGGED	Frame count register for RX frames with tags	5-32
0x000000B8	RX_DATA_ERR	Frame count register for RX frames with data errors	5-32
0x000000BC	RX_ALIGN_ERRORS	Frame count register for RX frames with byte-alignment errors	5-33
0x000000C0	RX_LONG_ERRORS	Frame count register for RX oversized frames	5-33
0x000000C4	RX_JABBER_ERRORS	Frame count register for RX oversized frames	5-33

Offset Address	Register	Description	Page
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	Frame count register for RX flow control frames	5-34
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	Frame count register for RX non-flow-control frames	5-34
0x000000D0	RX_VERY_LONG_ERR_CNT	Frame count register for RX long frames	5-35
0x000000D4	RX_RUNT_ERR_CNT	Frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length	5-35
0x000000D8	RX_SHORT_ERR_CNT	Frame count register for RX frames less than 96 bits in length	5-36
0x00000100	OCTETS_TRANSMITTED_OK	Byte count register for TX normal packets	5-36
0x00000104	OCTETS_TRANSMITTED_BAD	Byte count register for TX bad packets	5-36
0x00000108	TX_UC_PKTS	Frame count register for TX unicast frames	5-37
0x0000010C	TX_MC_PKTS	Frame count register for TX multicast frames	5-37
0x00000110	TX_BC_PKTS	Frame count register for TX broadcast frames	5-37
0x00000114	TX_PKTS_64OCTETS	Frame count register for TX 64-byte frames	5-38
0x00000118	TX_PKTS_65TO127OCTETS	Frame count register for TX frames ranging from 65 bytes to 127 bytes in length	5-38
0x0000011C	TX_PKTS_128TO255OCTETS	Frame count register for TX frames ranging from 128 bytes to 255 bytes in length	5-39
0x00000120	TX_PKTS_255TO511OCTETS	Frame count register for TX frames ranging from 256 bytes to 511 bytes in length	5-39
0x00000124	TX_PKTS_512TO1023OCTETS	Frame count register for TX frames ranging from 512 bytes to 1023 bytes in length	5-40
0x00000128	TX_PKTS_1024TO1518OCTETS	Frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length	5-40

Offset Address	Register	Description	Page
0x0000012C	TX_PKTS_1519TOMAXOCTETS	Frame count register for TX frames greater than 1519 bytes in length	5-41
0x00000144	TX_EXC_COL_ERR_CNT	Count register for packets whose number reaches the maximum retransmission number threshold	5-41
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	Count register for transmission failures caused by oversized frames	5-42
0x00000150	TX_UNDERRUN	Count register for transmission failures caused by internal errors	5-42
0x00000154	TX_TAGGED	Frame count register for TX VLAN frames	5-43
0x00000158	TX_CRC_ERROR	Frame count register for TX frames with valid lengths and CRC errors	5-43
0x0000015C	TX_PAUSE_FRAMES	Frame count register for TX PAUSE frames	5-43
0x000001A8	LINE_LOOP_BACK	Loopback register on the MAC line side	5-44
0x000001B0	CF_CRC_STRIP	CRC strip enable register	5-44
0x000001B4	MODE_CHANGE_EN	Port mode change enable register	5-45
0x000001C0	COL_SLOT_TIME	Count register for half-duplex collision retransmission intervals	5-45
0x000001DC	LOOP_REG	Loopback supplement register	5-46
0x000001E0	RECV_CONTROL	RX control register	5-46
0x000001E8	VLAN_CODE	VLAN code register	5-47
0x000001EC	RX_OVERRUN_CNT	FIFO overrun count register	5-47
0x000001F4	RX_LENGTHFIELD_ERR_CNT	Frame count register for RX frames containing PADs	5-47
0x000001F8	RX_FAIL_COMMA_CNT	COMMA count register for byte delimitation	5-48
0x00000200	MAC_SA_ADDR_L	Source MAC address register	5-48
0x00000204	MAC_SA_ADDR_H	Source MAC address register	5-49
0x00000208	MAC_DA_ADDR_L	Destination MAC address register	5-49
0x0000020C	MAC_DA_ADDR_H	Destination MAC address register	5-49
0x00000210	CRF_MIN_PACKET	Minimum filter packet length register	5-50
0x00000214	CONTROL_WORD	Control register	5-50

Offset Address	Register	Description	Page
0x00000218	FLOW_CTRL_PKG_THRSLD	Flow control packet count register	5-52
0x0000021C	CRF_FLOW_TIME_THRSLD	Flow control time register	5-52
0x00000220+4*m	FILTER_LISTm (m ranging from 0 to 15)	Filter list register	5-53
0x00000260	CRF_UDP_NO	UDP port number register	5-53
0x00000264	CRF_TX_FIFO_THRSLD	TX FIFO threshold register	5-54
0x00000268	CRF_RX_FIFO_THRSLD	RX FIFO threshold register	5-54
0x00000280	ERR_GIVEN_PKG_CNT	Count register for dropped packets caused by the frame tailors marked as errors	5-55
0x00000284	SHORT_ERR_PKT_CNT	Short error packet count register	5-55
0x00000288	ERR_FRM_TYPE_CNT	Count register for dropped packets caused by the frame types not listed in the filter list	5-56
0x0000028C	ERR_IP_TYPE_CNT	Count register for dropped packets caused by the IP types not listed in the filter list	5-56
0x00000290	ERR_UDP_CNT	Count register for filtered packets caused by UDP port numbers beyond the specified range	5-57
0x00000294	OVER_FLOW_CNT	Count register for dropped packets caused by the full RX FIFO	5-57
0x00000298	OVER_LENGTH_CNT	Count register for dropped packets whose sizes exceed the upper threshold of the PMU	5-57
0x000002A4	RX_PAUSE_EN	Flow control frame enable register in the RX direction	5-58
0x000002A8	CRF_CFF_DATA_NUM	Configuration FIFO data count register	5-58
0x000002AC	FLOW_OUT_IP_CNT	Count register for dropped IP packets caused by flow control	5-59
0x000002B0	FLOW_OUT_CTRL_CNT	Count register for dropped control packets caused by flow control	5-59
0x00000340	CRF_TX_PAUSE	TX flow control frame control register	5-60

Offset Address	Register	Description	Page
0x00000344	CRF_RX_LEFT_NUM	Flow control RX address count register	5-60
0x00000348	CRF_CTRL_0_TYPE	Control packet type 0 register	5-61
0x0000034C	CRF_CTRL_1_TYPE	Control packet type 1 register	5-61
0x00000350	CRF_CTRL_2_TYPE	Control packet type 2 register	5-61
0x00000354	CRF_CTRL_3_TYPE	Control packet type 3 register	5-62
0x00000358	CRF_BM_PKT_THRSLD	Count threshold register for broadcast/multicast packets under flow control	5-62
0x0000035C	CRF_BM_TIME_THRSLD	Flow control time threshold register for broadcast and multicast packets	5-63
0x000003C0	MDIO_SINGLE_CMD	MDIO single operation register	5-63
0x000003C4	MDIO_SINGLE_DATA	MDIO read/write data register	5-64
0x000003CC	MDIO_CTL	MDIO control register	5-64
0x000003D0	MDIO_RDATA_STATUS	MDIO read data status register	5-66
0x00000500	RX_FQ_START_ADDR	Start address register for the idle descriptor queue	5-66
0x00000504	RX_FQ_DEPTH	Depth register for the idle descriptor queue	5-66
0x00000508	RX_FQ_WR_ADDR	Write address register for the idle descriptor queue	5-67
0x0000050C	RX_FQ_RD_ADDR	Read address register for the idle descriptor queue	5-68
0x00000510	RX_FQ_VLDDESC_CNT	Valid descriptor number register for the idle descriptor queue	5-68
0x00000514	RX_FQ_ALRMPTY_TH	Almost-empty threshold register for the idle descriptor queue	5-69
0x00000518	RX_FQ_REG_EN	Enable register related to idle descriptor queue in the RX direction	5-69
0x0000051C	RX_FQ_ALFULL_TH	Almost-full threshold register for the idle descriptor queue	5-70
0x00000520	RX_BQ_START_ADDR	Start address register for the rx_buff descriptor queue	5-70
0x00000524	RX_BQ_DEPTH	Depth register for the rx_buff descriptor queue	5-71

Offset Address	Register	Description	Page
0x00000528	RX_BQ_WR_ADDR	Write address register for the rx_buff descriptor queue	5-72
0x0000052C	RX_BQ_RD_ADDR	Read address register for the rx_buff descriptor queue	5-72
0x00000530	RX_BQ_FREE_DESC_CNT	Writable descriptor count register for the rx_buff descriptor queue	5-73
0x00000534	RX_BQ_ALEMPTY_TH	Almost-empty threshold register for the rx_buff descriptor queue	5-73
0x00000538	RX_BQ_REG_EN	Enable register related to rx_buff descriptor queue	5-74
0x0000053C	RX_BQ_ALFULL_TH	Almost-full threshold register for the rx_buff descriptor queue	5-75
0x00000580	TX_BQ_START_ADDR	Start address register for the tx_buff descriptor queue	5-75
0x00000584	TX_BQ_DEPTH	Depth register for the tx_buff descriptor queue	5-76
0x00000588	TX_BQ_WR_ADDR	Write address register for the tx_buff descriptor queue	5-76
0x0000058C	TX_BQ_RD_ADDR	Read address register for the tx_buff descriptor queue	5-77
0x00000590	TX_BQ_VLDDESC_CNT	Valid descriptor number register for the tx_buff descriptor queue	5-77
0x00000594	TX_BQ_ALEMPTY_TH	Almost-empty threshold register for the tx_buff descriptor queue	5-78
0x00000598	TX_BQ_REG_EN	Enable register related to tx_buff descriptor queue	5-78
0x0000059C	BQ1_ALFULL_TH	Almost-full threshold register for the tx_buff descriptor queue	5-79
0x000005A0	TX_RQ_START_ADDR	Start address register for the tx_rq descriptor queue	5-79
0x000005A4	TX_RQ_DEPTH	Depth register for the tx_rq descriptor queue	5-80
0x000005A8	TX_RQ_WR_ADDR	Write address register for the tx_rq descriptor queue	5-80
0x000005AC	TX_RQ_RD_ADDR	Read address register for the tx_rq descriptor queue	5-80
0x000005B0	TX_RQ_FREE_DESC_CNT	Writable descriptor count register for the tx_rq descriptor queue	5-81

Offset Address	Register	Description	Page
0x000005B4	TX_RQ_ALEMPTY_TH	Almost-empty threshold register for the tx_rq descriptor queue	5-81
0x000005B8	TX_RQ_REG_EN	Enable register related to the tx_rq descriptor queue	5-82
0x000005BC	TX_RQ_ALFULL_TH	Almost-full threshold register for the tx_rq descriptor queue	5-83
0x000005C0	RAW_PMU_INT	PMU raw interrupt status register	5-83
0x000005C4	ENA_PMU_INT	PMU raw interrupt enable register	5-86
0x000005C8	STATUS_PMU_INT	PMU interrupt status register	5-90
0x000005CC	DESC_WR_RD_ENA	cff read/write descriptor enable register	5-93
0x000005D8	IN_QUEUE_TH	rx_bq or tx_rq enqueue interrupt threshold register	5-94
0x000005DC	OUT_QUEUE_TH	rx_fq or tx_bq dequeue interrupt threshold register	5-94
0x000005E0	RX_BQ_IN_TIMEOUT_TH	rx_bq enqueue timeout raw interrupt threshold register	5-95
0x000005E4	TX_RQ_IN_TIMEOUT_TH	tx_rq enqueue timeout raw interrupt threshold register	5-95
0x000005E8	STOP_CMD	RX and TX packet control stop register	5-96
0x000005EC	FLUSH_CMD	Recycle descriptor enable register	5-96
0x00000800	U_EEE_INTR_SRC	LPI status register in the RX and TX directions	5-97
0x00000804	U_EEE_INTR_EN	Interrupt mask and enable register in the RX and TX directions	5-98
0x00000808	U_EEE_ENABLE	EEE enable signal register	5-100
0x0000080C	U_EEE_TIMER	LPI time threshold register	5-101
0x00000810	U_EEE_LINK_STATUS	EEE status register	5-101
0x00000814	U_EEE_TIME_CLK_CNT	Timing pulse count register	5-102
0x00000A00	PMT_CTRL_STAUTS	PMT control and status register	5-102
0x00000A04	FILTER_0_BYTE_MASK	PMT valid byte selection register 0	5-104
0x00000A08	FILTER_1_BYTE_MASK	PMT valid byte selection register 1	5-104
0x00000A0C	FILTER_2_BYTE_MASK	PMT valid byte selection register 2	5-105
0x00000A10	FILTER_3_BYTE_MASK	PMT valid byte selection register 3	5-105

Offset Address	Register	Description	Page
0x00000A14	FILTER_COMMAND	PMT template selection and multicast enable register	5-106
0x00000A18	FILTER_OFFSET	CRC position offset register	5-107
0x00000A1C	FILTER0_1_CRC	Software-expected CRC value 0 and 1 register	5-108
0x00000A20	FILTER2_3_CRC	Software-expected CRC value 2 and 3 register	5-108

5.7 Register Description

STATION_ADDR_LOW

STATION_ADDR_LOW is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000000	STATION_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	station_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	station_addr_low	Lower 32 bits for the source MAC address of MAC_CORE

STATION_ADDR_HIGH

STATION_ADDR_HIGH is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000004	STATION_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																station_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	station_addr_high	Upper 16 bits of the source MAC address of MAC_CORE. The default configurations can be used.

DUPLEX_SEL_RGMII

DUPLEX_SEL_RGMII is a half-duplex selection register.

Offset Address	Register Name	Total Reset Value
0x00000008	DUPLEX_SEL_RGMII	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							duplex_sel_rgmii
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	duplex_sel_rgmii	Half-duplex selection signal 0: half duplex 1: full duplex

FD_FC_TYPE

FD_FC_TYPE is a flow control frame type domain register.

Offset Address	Register Name	Total Reset Value
0x0000000C	FD_FC_TYPE	0x0000_8808

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				fd_fc_type			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_type	Flow control frame type domain in full-duplex mode

COL_DISTANCE

COL_DISTANCE is a single retransmission packet length threshold register.

Offset Address	Register Name	Total Reset Value
0x00000014	COL_DISTANCE	0x0000_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						col_distance									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	col_distance	Single retransmission packet length threshold

FC_TX_TIMER

FC_TX_TIMER is a flow control time parameter register.

Offset Address	Register Name	Total Reset Value
0x0000001C	FC_TX_TIMER	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fc_tx_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fc_tx_timer	Parameter of the time period during which flow control frames are transmitted. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

FD_FC_ADDR_LOW

FD_FC_ADDR_LOW is a flow control frame destination address lower 32 bits register.

Offset Address	Register Name	Total Reset Value
0x00000020	FD_FC_ADDR_LOW	0xC200_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fd_fc_addr_low																															
Reset	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:0]	RW	fd_fc_addr_low	Lower 32 bits of the destination address of the flow control frame

FD_FC_ADDR_HIGH

FD_FC_ADDR_HIGH is a flow control frame destination address upper 16 bits register.

Offset Address	Register Name	Total Reset Value
0x00000024	FD_FC_ADDR_HIGH	0x0000_0180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_fc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_addr_high	Upper 16 bits of the destination address of the flow control frame

IPG_TX_TIMER

IPG_TX_TIMER is a TX frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000030	IPG_TX_TIMER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ipg_tx_timer							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ipg_tx_timer	TX frame IPG, in the unit of byte

PAUSE_THR

PAUSE_THR is a TX flow control frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000038	PAUSE_THR	0x0000_002F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pause_thr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	pause_thr	IPG of the flow control frame. If the flow control time is longer than the IPG, the MAC transmits the flow control frame automatically. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

MAX_FRM_SIZE

MAX_FRM_SIZE is a maximum frame length register.

Offset Address	Register Name	Total Reset Value
0x0000003C	MAX_FRM_SIZE	0x0000_05EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_frm_size											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	max_frm_size	Maximum frame length on the MAC side If the length of an RX frame is greater than the maximum length, the RX frame is regarded as an oversized frame. When the length of a frame to be transmitted is greater than the maximum length, the frame is broken up and then transmitted as an error frame.

PORT_MODE

PORT_MODE is a port status register.

Offset Address	Register Name	Total Reset Value
0x00000040	PORT_MODE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														port_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	port_mode	Current MAC port mode 000: 10 Mbit/s 001: 100 Mbit/s 101: 1000 Mbit/s Other values: reserved

PORT_EN

PORT_EN is a channel enable register.

Offset Address	Register Name	Total Reset Value
0x00000044	PORT_EN	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx en	rx en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_en	TX channel enable 0: disabled 1: enabled
[1]	RW	rx_en	RX channel enable 0: disabled 1: enabled

[0]	RO	reserved	Reserved

PAUSE_EN

PAUSE_EN is a flow control enable register.

Offset Address	Register Name	Total Reset Value
0x00000048	PAUSE_EN	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx fdfc	rx fdfc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_fdfc	Flow control frame transmit enable in full-duplex mode 0: disabled 1: enabled
[0]	RW	rx_fdfc	Flow control frame response enable in full-duplex mode 0: disabled 1: enabled

SHORT_RUNTS_THR

SHORT_RUNTS_THR is a short frame threshold register.

Offset Address	Register Name	Total Reset Value
0x00000050	SHORT_RUNTS_THR	0x0000_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												short_runts_thr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	short_runts_thr	Short frame threshold (for statistics only)

DROP_UNK_CTL_FRM

DROP_UNK_CTL_FRM is a drop enable register for unknown control frames.

Offset Address	Register Name	Total Reset Value
0x00000054	DROP_UNK_CTL_FRM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															drop_unk_ctl_frm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	drop_unk_ctl_frm	Processing method of the unknown control frames 0: The unknown control frames are forwarded normally. 1: The unknown control frames are dropped.

TRANSMIT_CONTROL

TRANSMIT_CONTROL is a common configuration register.

Offset Address	Register Name	Total Reset Value
0x00000060	TRANSMIT_CONTROL	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pad_enable	crc_add	reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pad_enable	PAD addition enable 0: disabled 1: enabled
[6]	RW	crc_add	FCS addition enable 0: enabled 1: disabled

[5:0]	RO	reserved	Reserved

REC_FILT_CONTROL

REC_FILT_CONTROL is an RX frame filter control register.

Offset Address	Register Name	Total Reset Value
0x00000064	REC_FILT_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										crc_err_pass	pause_frm_pass	vlan_drop_en	bc_drop_en	mc_match_en	uc_match_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	crc_err_pass	CRC error frame filter enable 0: disabled 1: enabled
[4]	RW	pause_frm_pass	Flow control frame filter enable 0: disabled. This bit takes effect only when flow control is enabled, which is transmitted to the software. 1: enabled. This bit takes effect only when flow control is enabled, which is not transmitted to the software.
[3]	RW	vlan_drop_en	VLAN frame filter enable 0: disabled 1: enabled
[2]	RW	bc_drop_en	Broadcast frame filter enable 0: disabled 1: enabled
[1]	RW	mc_match_en	Multicast frame enable with unmatched DA filter 0: disabled 1: enabled
[0]	RW	uc_match_en	Unicast frame enable with unmatched DA filter 0: disabled 1: enabled

PORT_MC_ADDR_LOW

PORT_MC_ADDR_LOW is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x00000068	PORT_MC_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_mc_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_mc_addr_low	Lower 32 bits of the multicast address, used to check whether the multicast frames match

PORT_MC_ADDR_HIGH

PORT_MC_ADDR_HIGH is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x0000006C	PORT_MC_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																port_mc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	port_mc_addr_high	Upper 16 bits of the multicast address, used to check whether the multicast frames match

MAC_CLR

MAC_CLR is a MAC clear register.

Offset Address	Register Name	Total Reset Value
0x00000070	MAC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												soft_rst_mdio	soft_rst_mii	soft_rst_rx	soft_rst_tx
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	soft_rst_mdio	MDIO clear signal 0: invalid 1: valid
[2]	RW	soft_rst_mii	MII clear signal 0: invalid 1: valid
[1]	RW	soft_rst_rx	RX clear signal 0: invalid 1: valid
[0]	RW	soft_rst_tx	TX clear signal 0: invalid 1: valid

RX_OCTETS_OK_CNT

RX_OCTETS_OK_CNT is a byte count register for valid RX frames.

Offset Address	Register Name	Total Reset Value
0x00000080	RX_OCTETS_OK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_ok_cnt	Count of bytes of the valid RX frames, ranging from DA to FCS

RX_OCTETS_BAD_CNT

RX_OCTETS_BAD_CNT is a byte count register for error RX frames.

Offset Address	Register Name	Total Reset Value
0x00000084	RX_OCTETS_BAD_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rx_octets_bad_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_bad_cnt	Count of bytes of the frames with CRC errors and alignment errors

RX_UC_PKTS

RX_UC_PKTS is a MAC frame count register for RX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000088	RX_UC_PKTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rx_uc_pkts_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_uc_pkts_cnt	Count of RX unicast frames, excluding bad frames

RX_MC_PKTS

RX_MC_PKTS is a frame count register for RX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000008C	RX_MC_PKTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rx_mc_pkts_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	rx_mc_pkts_cnt	Count of RX multicast frames, excluding bad frames

RX_BC_PKTS

RX_BC_PKTS is a frame count register for RX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000090	RX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_bc_pkts_cnt	Count of RX broadcast frames, excluding bad frames

RX_PKTS_64OCTETS

RX_PKTS_64OCTETS is a frame count register for RX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000094	RX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_64oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_64oct_cnt	Count of RX 64-byte frames, including bad frames

RX_PKTS_65TO127OCTETS

RX_PKTS_65TO127OCTETS is a frame count register for RX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000098	RX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_65to127_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_65to127_oct_cnt	Count of RX frames ranging from 65 bytes to 127 bytes in length, including bad frames

RX_PKTS_128TO255OCTETS

RX_PKTS_128TO255OCTETS is a frame count register for RX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000009C	RX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_128to255_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_128to255_oct_cnt	Count of RX frames ranging from 128 bytes to 255 bytes in length, including bad frames

RX_PKTS_255TO511OCTETS

RX_PKTS_255TO511OCTETS is a frame count register for RX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A0	RX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_256to511_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_256to511_oct_cnt	Count of RX frames ranging from 256 bytes to 511 bytes in length, including bad frames

RX_PKTS_512TO1023OCTETS

RX_PKTS_512TO1023OCTETS is a frame count register for RX frames ranging from 512 bytes to 1023 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A4	RX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_512to1023_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_512to1023_oct_cnt	Count of RX frames ranging from 512 bytes to 1023 bytes in length, including bad frames

RX_PKTS_1024TO1518OCTETS

RX_PKTS_1024TO1518OCTETS is a frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A8	RX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1024to1518_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1024to1518_oct_cnt	Count of RX frames ranging from 1024 bytes to 1518 bytes in length, including bad frames

RX_PKTS_1519TOMAXOCTETS

RX_PKTS_1519TOMAXOCTETS is a frame count register for RX frames ranging from 1519 bytes to the maximum in length.

Offset Address	Register Name	Total Reset Value
0x000000AC	RX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1519tomax_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1519tomax_oct_cnt	Count of RX frames ranging from 1519 bytes to the maximum in length, including bad frames

RX_FCS_ERRORS

RX_FCS_ERRORS is a frame count register for RX frames with CRC errors.

Offset Address	Register Name	Total Reset Value
0x000000B0	RX_FCS_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fcs_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fcs_errors	Count of RX frames with CRC errors, excluding short frames

RX_TAGGED

RX_TAGGED is a frame count register for RX frames with tags.

Offset Address	Register Name	Total Reset Value
0x000000B4	RX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_tagged	Count of RX frames with tags

RX_DATA_ERR

RX_DATA_ERR is a frame count register for RX frames with data errors.

Offset Address	Register Name	Total Reset Value
0x000000B8	RX_DATA_ERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_data_err																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_data_err	Count of RX frames with data errors

RX_ALIGN_ERRORS

RX_ALIGN_ERRORS is a frame count register for RX frames with byte-alignment errors.

Offset Address	Register Name	Total Reset Value
0x000000BC	RX_ALIGN_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_align_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_align_errors	Count of RX frames with byte-alignment errors

RX_LONG_ERRORS

RX_LONG_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C0	RX_LONG_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_long_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_long_errors	Count of RX oversized frames (without CRC errors)

RX_JABBER_ERRORS

RX_JABBER_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C4	RX_JABBER_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_jabber_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_jabber_errors	Count of RX oversized frames with CRC errors or non-integer byte count

RX_PAUSE_MACCONTROL_FRAMCOUNTER

RX_PAUSE_MACCONTROL_FRAMCOUNTER is a frame count register for RX flow control frames.

Offset Address	Register Name	Total Reset Value
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pause_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pause_maccontrol_framecounter	Count of RX flow control frames. The CRC must be correct when it is valid.

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER is a frame count register for RX non-flow-control frames.

Offset Address	Register Name	Total Reset Value
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_unknown_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_unknown_maccontrol_framecounter	Count of RX non-flow control frames

RX_VERY_LONG_ERR_CNT

RX_VERY_LONG_ERR_CNT is a frame count register for RX long frames.

Offset Address	Register Name	Total Reset Value
0x000000D0	RX_VERY_LONG_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_very_long_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_very_long_err_cnt	Count of RX long frames (with the length more than twice the maximum frame length)

RX_RUNT_ERR_CNT

RX_RUNT_ERR_CNT is a frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D4	RX_RUNT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_runt_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_runt_err_cnt	Count of RX frames less than 64 bytes but greater than or equal to 12 bytes in length

RX_SHORT_ERR_CNT

RX_SHORT_ERR_CNT is a frame count register for RX frames less than 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D8	RX_SHORT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_short_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_short_err_cnt	Count of RX frames less than 12 bytes in length.

OCTETS_TRANSMITTED_OK

OCTETS_TRANSMITTED_OK is a byte count register for TX normal packets.

Offset Address	Register Name	Total Reset Value
0x00000100	OCTETS_TRANSMITTED_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_ok	Count of bytes of the transmitted normal packets, excluding the preambles and SFDs

OCTETS_TRANSMITTED_BAD

OCTETS_TRANSMITTED_BAD is a byte count register for TX bad packets.

Offset Address	Register Name	Total Reset Value
0x00000104	OCTETS_TRANSMITTED_BAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_bad																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_bad	Count of bytes of the TX bad packets

TX_UC_PKTS

TX_UC_PKTS is a frame count register for TX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000108	TX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_uc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_uc_pkts	Count of TX unicast frames, excluding bad packets

TX_MC_PKTS

TX_MC_PKTS is a frame count register for TX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000010C	TX_MC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_mc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_mc_pkts	Count of TX multicast frames, excluding bad packets

TX_BC_PKTS

TX_BC_PKTS is a frame count register for TX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000110	TX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_bc_pkts	Count of TX broadcast frames, excluding bad packets

TX_PKTS_64OCTETS

TX_PKTS_64OCTETS is a frame count register for TX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000114	TX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_64octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_64octets	Count of TX 64-byte frames, including bad packets

TX_PKTS_65TO127OCTETS

TX_PKTS_65TO127OCTETS is a frame count register for TX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000118	TX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_65to127octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_65to127octets	Count of TX frames ranging from 65 bytes to 127 bytes in length, including bad packets

TX_PKTS_128TO255OCTETS

TX_PKTS_128TO255OCTETS is a frame count register for TX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000011C	TX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_128to255octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_128to255octets	Count of TX frames ranging from 128 bytes to 255 bytes in length, including bad packets

TX_PKTS_255TO511OCTETS

TX_PKTS_255TO511OCTETS is a frame count register for TX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000120	TX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_256to511octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_256to511octets	Count of TX frames ranging from 256 bytes to 511 bytes in length, including bad packets

TX_PKTS_512TO1023OCTETS

TX_PKTS_512TO1023OCTETS is a frame count register for TX frames ranging from 512 bytes to 1023 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000124	TX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_512to1023octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_512to1023octets	Count of TX frames ranging from 512 bytes to 1023 bytes in length, including bad packets

TX_PKTS_1024TO1518OCTETS

TX_PKTS_1024TO1518OCTETS is a frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000128	TX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1024to1518octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1024to1518octets	Count of TX frames ranging from 1024 bytes to 1518 bytes in length, including bad packets

TX_PKTS_1519TOMAXOCTETS

TX_PKTS_1519TOMAXOCTETS is a frame count register for TX frames greater than 1519 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000012C	TX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1519tomaxoctes																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1519tomaxoctes	Count of TX frames greater than 1519 bytes in length, including bad packets

TX_EXC_COL_ERR_CNT

TX_EXC_COL_ERR_CNT is a count register for packets whose number reaches the maximum retransmission number threshold.

Offset Address	Register Name	Total Reset Value
0x00000144	TX_EXC_COL_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_exc_col_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_exc_col_err_cnt	Count of packets whose number reaches the maximum retransmission number threshold

TX_EXCESSIVE_LENGTH_DROP

TX_EXCESSIVE_LENGTH_DROP is a count register for transmission failures caused by oversized frames.

Offset Address	Register Name	Total Reset Value
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_excessive_length_drop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_excessive_length_drop	Count of transmission failures caused by oversized frames

TX_UNDERRUN

TX_UNDERRUN is a count register for transmission failures caused by internal errors.

Offset Address	Register Name	Total Reset Value
0x00000150	TX_UNDERRUN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_underrun																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_underrun	Count of transmission failures caused by internal errors

TX_TAGGED

TX_TAGGED is a frame count register for TX VLAN frames.

Offset Address	Register Name	Total Reset Value
0x00000154	TX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_tagged	Count of TX VLAN frames The value of the Type field equals to that of the 0x8100 packet.

TX_CRC_ERROR

TX_CRC_ERROR is a frame count register for TX frames with valid lengths and CRC errors.

Offset Address	Register Name	Total Reset Value
0x00000158	TX_CRC_ERROR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_crc_error																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_crc_error	Count of TX frames with valid lengths and CRC errors

TX_PAUSE_FRAMES

TX_PAUSE_FRAMES is a frame count register for TX PAUSE frames.

Offset Address	Register Name	Total Reset Value
0x0000015C	TX_PAUSE_FRAMES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pause_frames																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pause_frames	Count of TX PAUSE frames

LINE_LOOP_BACK

LINE_LOOP_BACK is a loopback register on the MAC line side.

Offset Address	Register Name	Total Reset Value
0x000001A8	LINE_LOOP_BACK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								line_loop_back
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	line_loop_back	MAC line-side loopback enable 0: disabled 1: enabled

CF_CRC_STRIP

CF_CRC_STRIP is a CRC strip enable register.

Offset Address	Register Name	Total Reset Value
0x000001B0	CF_CRC_STRIP	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								cf_crc_strip
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cf_crc_strip	RX CRC strip enable on the MAC side 0: disabled. The four bytes of the CRC are regarded as part of the packet. 1: enabled. The four bytes of the CRC are stripped from the packet.

MODE_CHANGE_EN

MODE_CHANGE_EN is a port mode change enable register.

Offset Address	Register Name	Total Reset Value
0x000001B4	MODE_CHANGE_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mode_change_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mode_change_en	port_mode change enable 0: disabled 1: enabled

COL_SLOT_TIME

COL_SLOT_TIME is a count register for half-duplex collision retransmission intervals.

Offset Address	Register Name	Total Reset Value
0x000001C0	COL_SLOT_TIME	0x0000_40FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cf2bc_slottime				cf2bc_random_seed	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RW	cf2bc_slottime	Interval for half-duplex collision retransmission
[7:0]	RW	cf2bc_random_seed	Random multiple radix for half-duplex collision retransmission

LOOP_REG

LOOP_REG is a loopback supplement register.

Offset Address	Register Name	Total Reset Value
0x000001DC	LOOP_REG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cf_ext_drive_lp	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	cf_ext_drive_lp	Generation of the read/write enable signals of the MAC data during loopback on the line side 0: The read/write enable signals are generated in the MAC. 1: The read/write enable signals are generated based on the MAC enable signals read by the downlink FIFO.
[0]	RO	reserved	Reserved

RECV_CONTROL

RECV_CONTROL is an RX control register.

Offset Address	Register Name	Total Reset Value
0x000001E0	RECV_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											runt_pkt_en	strip_pad_en	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

[4]	RW	runt_pkt_en	Transparent transmission enable of the RX short frames 0: discarded and not transmitted to the software 1: transmitted to the software
[3]	RW	strip_pad_en	PAD for stripping RX frames enable 0: disabled 1: enabled
[2:0]	RO	reserved	Reserved

VLAN_CODE

VLAN_CODE is a VLAN code register.

Offset Address	Register Name	Total Reset Value
0x000001E8	VLAN_CODE	0x0000_8100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cf_vlan_code															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	cf_vlan_code	Ethernet Type field configuration

RX_OVERRUN_CNT

RX_OVERRUN_CNT is a FIFO overrun count register.

Offset Address	Register Name	Total Reset Value
0x000001EC	RX_OVERRUN_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_overrun_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_overrun_cnt	Count of FIFO overruns on the MAC application side

RX_LENGTHFIELD_ERR_CNT

RX_LENGTHFIELD_ERR_CNT is a frame count register for RX frames containing PADs.

Offset Address	Register Name	Total Reset Value
0x000001F4	RX_LENGTHFIELD_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_lengthfield_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_lengthfield_err_cnt	Count of RX frames containing PADs and with the length of not 64 bytes when the PAD strip enable is valid

RX_FAIL_COMMA_CNT

RX_FAIL_COMMA_CNT is a COMMA count register for byte delimitation.

Offset Address	Register Name	Total Reset Value
0x000001F8	RX_FAIL_COMMA_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fail_comma_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fail_comma_cnt	Count of COMMA codes when two or more COMMA codes exist during byte delimitation

MAC_SA_ADDR_L

MAC_SA_ADDR_L is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000200	MAC_SA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_sa_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_sa_addr_l	Lower 32 bits of the source MAC address used by the PMU, which are inserted into the lower 32 bits of the source address (SA) field

MAC_SA_ADDR_H

MAC_SA_ADDR_H is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000204	MAC_SA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mac_sa_addr_h																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	mac_sa_addr_h	Upper 16 bits of the source MAC address used by the PMU

MAC_DA_ADDR_L

MAC_DA_ADDR_L is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000208	MAC_DA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_da_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_da_addr_l	Lower 32 bits of the destination MAC address used by the PMU, which are inserted into the lower 32 bits of the destination address field

MAC_DA_ADDR_H

MAC_DA_ADDR_H is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x0000020C	MAC_DA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_tx_max_packet												mac_da_addr_h																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:16]	RW	crf_tx_max_packet	Maximum length of the normal and SG packets allowed by the PMU
[15:0]	RW	mac_da_addr_h	Upper 16 bits of the destination MAC address used by the PMU

CRF_MIN_PACKET

CRF_MIN_PACKET is a minimum filter packet length register.

Offset Address	Register Name	Total Reset Value
0x00000210	CRF_MIN_PACKET	0x0000_0F2A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tso_version												reserved								crf_tx_min_packet				reserved				crf_rx_min_packet			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:20]	RO	tso_version	TSO version 100: single-byte combination version 200: SG or COE version 300: TSO version
[19:14]	RO	reserved	Reserved
[13:8]	RW	crf_tx_min_packet	Minimum length of the TX packet. The default length is 15 bytes.
[7:6]	RO	reserved	Reserved
[5:0]	RW	crf_rx_min_packet	Minimum length of the RX packet. The default length is 42 bytes.

CONTROL_WORD

CONTROL_WORD is a control register.

Offset Address	Register Name	Total Reset Value
0x00000214	CONTROL_WORD	0x00C0_0640

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						crf_tx_standard	reserved			crf_ip_flow_ctrl	crf_ctrl_flow_ctrl	reserved		crf_filt_unused_pkg	crf_bm_flow_ctrl	crf_peel_dsa	crf_add_da_sa	crf_large_packet											
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	crf_tx_standard	Configuration standard for the transmit waterline of the TX FIFO 0: The standard is set based on the packet and empty threshold. If the TX FIFO contains a complete packet or the number of valid data items in the TX FIFO is equal to or greater than the threshold multiplied by 4, a read request is sent to the MAC. 1: The standard is set based on the packet. If the TX FIFO contains a complete packet, a read request is sent to the MAC.
[24:22]	RO	reserved	Reserved
[21]	RW	crf_ip_flow_ctrl	IP packet flow control enable 0: disabled 1: enabled
[20]	RW	crf_ctrl_flow_ctrl	Control packet flow control enable 0: disabled 1: enabled
[19:18]	RO	reserved	Reserved
[17]	RW	crf_filt_unused_pkg	Invalid packets filter enable 0: disabled 1: enabled
[16]	RW	crf_bm_flow_ctrl	Multicast/broadcast packet flow control enable 0: disabled 1: enabled
[15]	RW	crf_peel_dsa	DA/SA stripping control enable 0: disabled 1: enabled

[14]	RW	crf_add_da_sa	DA/SA addition control enable 0: disabled 1: enable
[13:0]	RW	crf_large_packet	Maximum length configured for packets. The default length is 1600 bytes (maximum length of packets used by the PMU).

FLOW_CTRL_PKG_THRSLD

FLOW_CTRL_PKG_THRSLD is a flow control packet number threshold register.

Offset Address	Register Name	Total Reset Value
0x00000218	FLOW_CTRL_PKG_THRSLD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_ip_pkg_thrsld																crf_ctrl_pkg_thrsld															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	crf_ip_pkg_thrsld	Upper threshold of the number of IP packets. When the number of IP packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.
[15:0]	RW	crf_ctrl_pkg_thrsld	Upper threshold of the number of control packets. When the number of control packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.

CRF_FLOW_TIME_THRSLD

CRF_FLOW_TIME_THRSLD is a flow control time register.

Offset Address	Register Name	Total Reset Value
0x0000021C	CRF_FLOW_TIME_THRSLD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_flow_time_thrsld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_flow_time_thrsld	Flow control time, measured by 125 μs Flow control time T = (crf_flow_time_thrsld + 1) x 125 μs

FILTER_LISTm

FILTER_LISTm (*m* ranging from 0 to 15) is a filter list register.

Offset Address	Register Name	Total Reset Value
0x00000220 + 4 x m	FILTER_LISTm	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														crf_filt_cfg0	crf_filt_id0	crf_filt_frm_type0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	crf_filt_cfg0	Configured row or not 0: not configured 1: configured The content of this list needs to be parsed only when crf_filt_cfg is set to 1. Otherwise, the content of this list can be ignored.
[16]	RW	crf_filt_id0	Type of the list 0: MAC frame 1: IP
[15:0]	RW	crf_filt_frm_type0	Configured filter type When the ID is 0, 16 bits of crf_filt_frm_type are valid. When the ID is 1, the lower 8 bits of crf_filt_frm_type are valid, and the upper 8 bits are ignored.

CRF_UDP_NO

CRF_UDP_NO is a UDP port number register.

Offset Address	Register Name	Total Reset Value
0x00000260	CRF_UDP_NO	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_udp_max_no																reserved															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_udp_max_no	Maximum number of the UDP ports
[15:0]	RO	reserved	Reserved

CRF_TX_FIFO_THRSLD

CRF_TX_FIFO_THRSLD is a TX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x00000264	CRF_TX_FIFO_THRSLD	0x0271_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								crf_tx_p_full_th								reserved				crf_tx_p_empty_th											
Reset	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	crf_tx_p_full_th	Upper threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, packets are not transferred from the SDRAM. After the threshold is set, the TX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD bit[13:0] < 8192 – 4(crf_tx_p_full_th)
[15:11]	RO	reserved	Reserved
[10:0]	RW	crf_tx_p_empty_th	Lower threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, data can be read from the FX FIFO. It is recommended that this threshold be set to 0x14.

CRF_RX_FIFO_THRSLD

CRF_RX_FIFO_THRSLD is an RX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x00000268	CRF_RX_FIFO_THRSLD	0x0E10_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_rx_p_full_th												reserved				crf_rx_p_empty_th											
Reset	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	crf_rx_p_full_th	Upper threshold of the RX FIFO When the number of valid data packets in the RX FIFO quadruples crf_rx_p_full_th, new packets are not written to the RX FIFO. After the threshold is set, the RX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD[13:0] < (8192 – 4(crf_rx_p_full_th)
[15:12]	RO	reserved	Reserved
[11:0]	RW	crf_rx_p_empty_th	Lower threshold of the RX FIFO. When the number of valid data packets in the RX FIFO quadruples crf_rx_p_empty_th, data can be read from the RX FIFO. This threshold must be set to 0x200 at least.

ERR_GIVEN_PKG_CNT

ERR_GIVEN_PKG_CNT is a count register for dropped packets caused by the frame tailors marked as errors.

Offset Address	Register Name	Total Reset Value
0x00000280	ERR_GIVEN_PKG_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_given_pkg_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_given_pkg_cnt	Count of dropped packets caused by the frame tailors marked as errors

SHORT_ERR_PKT_CNT

SHORT_ERR_PKT_CNT is a short error packet count register.

Offset Address	Register Name	Total Reset Value
0x00000284	SHORT_ERR_PKT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	short_err_pkt_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	short_err_pkt_cnt	Count of short error packets

ERR_FRM_TYPE_CNT

ERR_FRM_TYPE_CNT is a count register for dropped packets caused by the frame types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x00000288	ERR_FRM_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_frm_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_frm_type_cnt	Count of dropped packets caused by the frame types not listed in the filter list

ERR_IP_TYPE_CNT

ERR_IP_TYPE_CNT is a count register for dropped packets caused by the IP types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x0000028C	ERR_IP_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_ip_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_ip_type_cnt	Count of the dropped packets caused by the IP types not listed in the filter list

ERR_UDP_CNT

ERR_UDP_CNT is a count register for filtered packets caused by UDP port numbers beyond the specified range.

Offset Address	Register Name	Total Reset Value
0x00000290	ERR_UDP_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	err_udp_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	err_udp_cnt	Count of filtered packets caused by UDP port numbers beyond the specified range

OVER_FLOW_CNT

OVER_FLOW_CNT is a count register for dropped packets caused by the full RX FIFO.

Offset Address	Register Name	Total Reset Value
0x00000294	OVER_FLOW_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	over_flow_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	over_flow_cnt	Count of dropped packets caused by the full RX FIFO

OVER_LENGTH_CNT

OVER_LENGTH_CNT is a count register for dropped packets whose size exceeds the upper threshold of the PMU.

Offset Address	Register Name	Total Reset Value
0x00000298	OVER_LENGTH_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	over_length_cnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RC	over_length_cnt	Count of dropped packets whose size exceeds the upper threshold of the PMU

RX_PAUSE_EN

RX_PAUSE_EN is a flow control frame enable register in the RX direction.

Offset Address	Register Name	Total Reset Value
0x000002A4	RX_PAUSE_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								rx_fifo_pause_en	rx_bq_pause_en	rx_fq_pause_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fifo_pause_en	rx_fifo flow control frame enable 0: disabled 1: enabled
[1]	RW	rx_bq_pause_en	rx_bq flow control frame enable 0: disabled 1: enabled
[0]	RW	rx_fq_pause_en	rx_fq flow control frame enable 0: disabled 1: enabled

CRF_CFF_DATA_NUM

CRF_CFF_DATA_NUM is a configuration FIFO data count register.

Offset Address	Register Name	Total Reset Value
0x000002A8	CRF_CFF_DATA_NUM	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	crf_rx_cfg_num				crf_tx_cfg_num						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_rx_cfg_num	Count of valid descriptors remained in the rx_fq FIFO
[15:0]	RW	crf_tx_cfg_num	Count of valid descriptors remained in the tx_bq FIFO

FLOW_OUT_IP_CNT

FLOW_OUT_IP_CNT is a count register for dropped IP packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002AC	FLOW_OUT_IP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ip_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ip_cnt	Count of dropped IP packets caused by flow control

FLOW_OUT_CTRL_CNT

FLOW_OUT_CTRL_CNT is a count register for dropped control packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002B0	FLOW_OUT_CTRL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ctrl_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ctrl_cnt	Count of dropped control packets caused by flow control

CRF_TX_PAUSE

CRF_TX_PAUSE is a TX flow control frame control register.

Offset Address	Register Name	Total Reset Value
0x00000340	CRF_TX_PAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crf_tx_pause_auto
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	crf_tx_pause_auto	Flow control frame control register, specifying the way in which the MAC transmits flow control frames 0: The MAC determines whether to transmit flow control frames according to the actual traffic. When the RX FIFO of the PMU is full or to be full, the MAC transmits flow control frames automatically. 1: The MAC is forced to transmit flow control frames.

CRF_RX_LEFT_NUM

CRF_RX_LEFT_NUM is a flow control RX address count register.

Offset Address	Register Name	Total Reset Value
0x00000344	CRF_RX_LEFT_NUM	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_rx_left_num							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_rx_left_num	When the remaining count of addresses in the RX configuration FIFO is less than the configured value, the control packets are allowed to pass only. The data packets are filtered out.

CRF_CTRL_0_TYPE

CRF_CTRL_0_TYPE is a control packet type 0 register.

Offset Address	Register Name	Total Reset Value
0x00000348	CRF_CTRL_0_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_0_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_0_type	Control packet type 0. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_1_TYPE

CRF_CTRL_1_TYPE is a control packet type 1 register.

Offset Address	Register Name	Total Reset Value
0x0000034C	CRF_CTRL_1_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_1_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_1_type	Control packet type 1. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_2_TYPE

CRF_CTRL_2_TYPE is a control packet type 2 register.

Offset Address	Register Name	Total Reset Value
0x00000350	CRF_CTRL_2_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_2_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_2_type	Control packet type 2. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_3_TYPE

CRF_CTRL_3_TYPE is a control packet type 3 register.

Offset Address	Register Name	Total Reset Value
0x00000354	CRF_CTRL_3_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_3_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	crf_ctrl_3_type	Control packet type 3. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_BM_PKT_THRSLD

CRF_BM_PKT_THRSLD is a count threshold register for broadcast/multicast packets under flow control.

Offset Address	Register Name	Total Reset Value
0x00000358	CRF_BM_PKT_THRSLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_bm_pkt_thrsld																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	crf_bm_pkt_thrsld	Upper threshold of the number of broadcast/multicast packets under flow control. When the number of broadcast/multicast packets that are received during the flow control time exceeds the configured value, the flow is controlled; otherwise, the flow is not controlled.

CRF_BM_TIME_THRSLD

CRF_BM_TIME_THRSLD is a flow control time threshold register for broadcast and multicast packets.

Offset Address	Register Name	Total Reset Value
0x0000035C	CRF_BM_TIME_THRSLD	0x0000_2710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												crf_bm_time_thrsld																				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	crf_bm_time_thrsld	Flow control time threshold for broadcast and multicast packets, measured by 1 μs. When the count equals the configured threshold, a time limit is reached.

MDIO_SINGLE_CMD

MDIO_SINGLE_CMD is an MDIO single operation register.

Offset Address	Register Name	Total Reset Value
0x000003C0	MDIO_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											mdio_cmd	reserved			op_code	reserved				phy_addr				reserved				reg_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RW	mdio_cmd	Operation completion through the MDIO indicator 0: The operation through the MDIO is complete. 1: The operation through the MDIO starts.

[19:18]	RO	reserved	Reserved
[17:16]	RW	op_code	MDIO operation type 00: Reserved 01: Write 10: Read 11: Reserved
[15:13]	RO	reserved	Reserved
[12:8]	RW	phy_addr	5 bits of the external PHY address
[7:5]	RO	reserved	Reserved
[4:0]	RW	reg_addr	Internal address of the PHY component

MDIO_SINGLE_DATA

MDIO_SINGLE_DATA is an MDIO read/write data register.

Offset Address	Register Name	Total Reset Value
0x000003C4	MDIO_SINGLE_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdio_rd_data																mdio_wr_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	mdio_rd_data	Data that is read back from the external PHY through the MDIO
[15:0]	RW	mdio_wr_data	Data that is written through the MDIO

MDIO_CTL

MDIO_CTL is an MDIO control register.

Offset Address	Register Name	Total Reset Value
0x000003CC	MDIO_CTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												mdio_in_work	mdio_in_work_en	autoscan_en	mdc_speed
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	mdio_in_work	Single operation through the MDIO indicator 0: The single operation is not performed. 1: The single operation is performed.
[2]	RW	mdio_in_work_en	MDIO_IN_WORK bit validity indicator 0: The MDIO_IN_WORK bit is invalid. 1: The MDIO_IN_WORK bit is valid.
[1]	RW	autoscan_en	Automatic detection enable 0: disabled 1: enabled (It controls the automatic scanning enable for all the PHY addresses. The value can be set to 1 because there is only one PHY currently.)
[0]	RW	mdc_speed	Frequency of the MDIO interface clock 0: The frequency of the MDIO interface clock is 2.5 MHz. 1: The frequency of the MDIO interface clock is 18 MHz.

MDIO_RDATA_STATUS

MDIO_RDATA_STATUS is an MDIO read data status register.

Offset Address	Register Name	Total Reset Value
0x000003D0	MDIO_RDATA_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdio_rdata_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RC	mdio_rdata_status	Whether the data read by the MDIO is valid 0: valid 1: invalid

RX_FQ_START_ADDR

RX_FQ_START_ADDR is a start address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000500	RX_FQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fq_start_addr	Start address of the idle descriptor queue. When rx_fq_start_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_FQ_DEPTH

RX_FQ_DEPTH is a depth register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000504	RX_FQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fq_depth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	fq_depth	Depth of the idle descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_fq_depth_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

RX_FQ_WR_ADDR

RX_FQ_WR_ADDR is a write address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000508	RX_FQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_wr_addr	Write address of the idle descriptor queue in the RX direction.

RX_FQ_RD_ADDR

RX_FQ_WR_ADDR is a read address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000050C	RX_FQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_rd_addr	Read address of the idle descriptor queue in the RX direction. When rx_fq_rd_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_rd_addr_en is set to 0, the register is read-only.

RX_FQ_VLDDESC_CNT

RX_FQ_VLDDESC_CNT is a valid descriptor number register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000510	RX_FQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	fq_vlddesc_cnt	Count of valid descriptors in the idle descriptor queue in the RX direction

RX_FQ_ALRMPTY_TH

RX_FQ_ALRMPTY_TH is an almost-empty threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000514	RX_FQ_ALRMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_low_th																fq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_low_th	Lower flow control threshold of the rx_fq queue. If the count of valid descriptors is less than or equal to the value of fq_pause_low_th, a signal for sending flow control frames is generated.
[15:0]	RW	fq_alempty_th	Almost-empty threshold of the idle descriptor queue in the RX direction

RX_FQ_REG_EN

RX_FQ_REG_EN is an enable register related to the idle descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000518	RX_FQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_fq_start_addr_en	rx_fq_depth_en	rx_fq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fq_start_addr_en	Software write enable for the RX_FQ_START_ADDR register 0: The RX_FQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_FQ_START_ADDR register can be written.

[1]	RW	rx_fq_depth_en	Software write enable for the RX_FQ_DEPTH register 0: The RX_FQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_FQ_DEPTH register can be written.
[0]	RW	rx_fq_rd_addr_en	Software write enable for the RX_FQ read address register 0: The RX_FQ read address register is protected, and software cannot be written. 1: Software of the RX_FQ read address register can be written.

RX_FQ_ALFULL_TH

RX_FQ_ALFULL_TH is an almost-full threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000051C	RX_FQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_hi_th																fq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_hi_th	Upper flow control threshold for the rx_fq queue. If the count of valid descriptors is greater than or equal to the value of fq_pause_hi_th, a signal for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	fq_alfull_th	Almost-full threshold of the idle descriptor queue in the RX direction

RX_BQ_START_ADDR

RX_BQ_START_ADDR is a start address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000520	RX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_bq_start_addr	Start address of the buff descriptor queue in the RX direction. When rx_bq_start_addr_en in the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_BQ_DEPTH

RX_BQ_DEPTH is a depth register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000524	RX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rx_bq_depth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	rx_bq_depth	Depth of the buff descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_bq_depth_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

RX_BQ_WR_ADDR

RX_BQ_WR_ADDR is a write address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000528	RX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_wr_addr	Write address of the buff descriptor queue in the RX direction. When rx_bq_wr_addr_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_wr_addr_en is set to 0, the register is read-only.

RX_BQ_RD_ADDR

RX_BQ_RD_ADDR is a read address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000052C	RX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_rd_addr	Read address of the buff descriptor queue in the RX direction

RX_BQ_FREE_DESC_CNT

RX_BQ_FREE_DESC_CNT is a writable descriptor count register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000530	RX_BQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rx_bq_free_desc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rx_bq_free_desc_cnt	Count of writable descriptors in the buff descriptor queue in the RX direction

RX_BQ_ALEMPTY_TH

RX_BQ_ALEMPTY_TH is an almost-empty threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000534	RX_BQ_ALEMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_low_th																rx_bq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_low_th	Flow control threshold of the rx_bq queue. If the count of writable descriptors is less than or equal to the value of bq_pause_low_th, an indicator for sending flow control frames is generated.
[15:0]	RW	rx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the RX direction

RX_BQ_REG_EN

RX_BQ_REG_EN is an enable register related to the buff descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000538	RX_BQ_REG_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								rx_bq_start_addr_en	rx_bq_depth_en	rx_bq_wr_addr_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_bq_start_addr_en	Software write enable for the RX_BQ_START_ADDR register 0: The RX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_BQ_START_ADDR register can be written.
[1]	RW	rx_bq_depth_en	Software write enable for the RX_BQ_DEPTH register 0: The RX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_BQ_DEPTH register can be written.
[0]	RW	rx_bq_wr_addr_en	Software write enable for the RX_BQ write address register 0: The RX_BQ write address register is protected, and software cannot be written. 1: Software of the RX_BQ write address register can be written.

RX_BQ_ALFULL_TH

RX_BQ_ALFULL_TH is an almost-full threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000053C	RX_BQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_hi_th																rx_bq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_hi_th	Upper flow control threshold for the rx_bq queue. If the count of writable descriptors is greater than or equal to the value of bq_pause_hi_th, the indicator for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	rx_bq_alfull_th	Almost-full threshold of the buff descriptor queue in the RX direction

TX_BQ_START_ADDR

TX_BQ_START_ADDR is a start address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000580	TX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_bq_start_addr	Start address of the buff descriptor queue in the TX direction. When tx_bq_start_addr_en in the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

TX_BQ_DEPTH

TX_BQ_DEPTH is a depth register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000584	TX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_depth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_bq_depth	Depth of the buff descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_bq_depth_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_BQ_WR_ADDR

TX_BQ_WR_ADDR is a write address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000588	TX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_wr_addr	Write address of the buff descriptor queue in the TX direction

TX_BQ_RD_ADDR

TX_BQ_RD_ADDR is a read address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000058C	TX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_rd_addr	Read address of the buff descriptor queue in the TX direction. When rx_bq_rd_addr_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_rd_addr_en is set to 0, the register is read-only.

TX_BQ_VLDDESC_CNT

TX_BQ_VLDDESC_CNT is a valid descriptor number register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000590	TX_BQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_vlddesc_cnt	Count of valid descriptors in the buff descriptor queue in the TX direction

TX_BQ_ALEMPTY_TH

TX_BQ_ALEMPTY_TH is an almost-empty threshold register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000594	TX_BQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_alempty_th																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the TX direction

TX_BQ_REG_EN

TX_BQ_REG_EN is an enable register related to the buff descriptor queue in the TX direction.

Offset Address	Register Name	Total Reset Value
0x00000598	TX_BQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx_bq_start_addr_en	tx_bq_depth_en	tx_bq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_bq_start_addr_en	Software write enable for the TX_BQ_START_ADDR register 0: The TX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_BQ_START_ADDR register can be written.

[1]	RW	tx_bq_depth_en	Software write enable for the TX_BQ_DEPTH register 0: The TX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_BQ_DEPTH register can be written.
[0]	RW	tx_bq_rd_addr_en	Software write enable for the TX_BQ read address register 0: The TX_BQ read address register is protected, and software cannot be written. 1: Software of the TX_BQ read address register can be written.

BQ1_ALFULL_TH

BQ1_ALFULL_TH is an almost-full threshold register for the buff1 descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000059C	BQ1_ALFULL_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bq1_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bq1_alfull_th	Almost-full threshold of the buff1 descriptor queue in the TX direction

TX_RQ_START_ADDR

TX_RQ_START_ADDR is a start address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A0	TX_RQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_rq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_rq_start_addr	Start address of the recycle descriptor queue in the TX direction. When tx_rq_start_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

TX_RQ_DEPTH

TX_RQ_DEPTH is a depth register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A4	TX_RQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_rq_depth	Depth of the recycle descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_rq_depth_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_RQ_WR_ADDR

TX_RQ_WR_ADDR is a write address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A8	TX_RQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_wr_addr	Write address of the recycle descriptor queue in the TX direction. When tx_rq_wr_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_wr_addr_en is set to 0, the register is read-only.

TX_RQ_RD_ADDR

TX_RQ_RD_ADDR is a read address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005AC	TX_RQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_rd_addr	Read address of the recycle descriptor queue in the TX direction.

TX_RQ_FREE_DESC_CNT

TX_RQ_FREE_DESC_CNT is a writable descriptor count register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B0	TX_RQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_free_desc_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_free_desc_cnt	Count of writable descriptors in the recycle descriptor queue in the TX direction

TX_RQ_ALEMPTY_TH

TX_RQ_ALEMPTY_TH is an almost-empty threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B4	TX_RQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alempty_th																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	tx_rq_alempty_th	Almost-empty threshold of the recycle descriptor queue in the TX direction

TX_RQ_REG_EN

TX_RQ_REG_EN is an enable register related to the tx_rq descriptor queue

Offset Address	Register Name	Total Reset Value
0x000005B8	TX_RQ_REG_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								tx_rq_start_addr_en	tx_rq_depth_en	tx_rq_wr_addr_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_rq_start_addr_en	Software write enable for the TX_RQ_START_ADDR register 0: The TX_RQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_RQ_START_ADDR register can be written.
[1]	RW	tx_rq_depth_en	Software write enable for the TX_RQ_DEPTH register 0: The TX_RQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_RQ_DEPTH register can be written.
[0]	RW	tx_rq_wr_addr_en	Software write enable for the TX_RQ write address register 0: The TX_RQ write address register is protected, and software cannot be written. 1: Software of the TX_RQ write address register can be written.

TX_RQ_ALFULL_TH

TX_RQ_ALFULL_TH is an almost-full threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005BC	TX_RQ_ALFULL_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_alfull_th	Almost-full threshold of the recycle descriptor queue in the TX direction

RAW_PMU_INT

RAW_PMU_INT is a PMU raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000005C0	RAW_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	raw_mac_fifo_err_int	raw_tx_rq_in_timeout_int	raw_rx_bq_in_timeout_int	raw_txoutcff_full_int	raw_txoutcff_empty_int	raw_txcff_full_int	raw_txcff_empty_int	raw_rxoutcff_full_int	raw_rxoutcff_empty_int	raw_rxcff_full_int	raw_rxcff_empty_int	raw_tx_rq_in_int	raw_tx_bq_out_int	raw_rx_bq_in_int	raw_rx_fq_out_int	raw_tx_rq_empty_int	raw_tx_rq_full_int	raw_tx_rq_alempty_int	raw_tx_rq_alfull_int	raw_tx_bq_empty_int	raw_tx_bq_full_int	raw_tx_bq_alempty_int	raw_tx_bq_alfull_int	raw_rx_bq_empty_int	raw_rx_bq_full_int	raw_rx_bq_alempty_int	raw_rx_bq_alfull_int	raw_rx_fq_empty_int	raw_rx_fq_full_int	raw_rx_fq_alempty_int	raw_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	raw_mac_fifo_err_int	Raw interrupt of FIFO empty and full errors in the MAC address, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[29]	RW	raw_tx_rq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the RQ queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[28]	RW	raw_rx_bq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the BQ queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[27]	RW	raw_txoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[26]	RW	raw_txoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[25]	RW	raw_txcff_full_int	Raw interrupt of full DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[24]	RW	raw_txcff_empty_int	Raw interrupt of empty DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[23]	RW	raw_rxoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[22]	RW	raw_rxoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[21]	RW	raw_rxcff_full_int	Raw interrupt of full DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[20]	RW	raw_rxcff_empty_int	Raw interrupt of empty DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[19]	RW	raw_tx_rq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the tx_rq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[18]	RW	raw_tx_bq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the tx_bq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	RW	raw_rx_bq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the rx_bq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RW	raw_rx_fq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the rx_fq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15]	RW	raw_tx_rq_empty_int	Raw interrupt of the empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[14]	RW	raw_tx_rq_full_int	Raw interrupt of the full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[13]	RW	raw_tx_rq_alempty_int	Raw interrupt of the almost-empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[12]	RW	raw_tx_rq_alfull_int	Raw interrupt of the almost-full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	RW	raw_tx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	RW	raw_tx_bq_full_int	Raw interrupt of the full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	RW	raw_tx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[8]	RW	raw_tx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7]	RW	raw_rx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	raw_rx_bq_full_int	Raw interrupt of the full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RW	raw_rx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RW	raw_rx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RW	raw_rx_fq_empty_int	Raw interrupt of the empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RW	raw_rx_fq_full_int	Raw interrupt of the full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RW	raw_rx_fq_alempty_int	Raw interrupt of the almost-empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RW	raw_rx_fq_alfull_int	Raw interrupt of the almost-full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

ENA_PMU_INT

ENA_PMU_INT is a PMU raw interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x000005C4	ENA_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ena_mac_fifo_err_int	ena_tx_rq_in_timeout_int	ena_rx_bq_in_timeout_int	ena_txoutcff_full_int	ena_txoutcff_empty_int	ena_txcff_full_int	ena_txcff_empty_int	ena_rxoutcff_full_int	ena_rxoutcff_empty_int	ena_rxcff_full_int	ena_rxcff_empty_int	ena_tx_rq_in_int	ena_tx_bq_out_int	ena_rx_bq_in_int	ena_rx_fq_out_int	ena_tx_rq_empty_int	ena_tx_rq_full_int	ena_tx_rq_alempty_int	ena_tx_rq_alfull_int	ena_tx_bq_empty_int	ena_tx_bq_full_int	ena_tx_bq_alempty_int	ena_tx_bq_alfull_int	ena_rx_bq_empty_int	ena_rx_bq_full_int	ena_rx_bq_alempty_int	ena_rx_bq_alfull_int	ena_rx_fq_empty_int	ena_rx_fq_full_int	ena_rx_fq_alempty_int	ena_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	ena_mac_fifo_err_int	Internal FIFO empty and full error interrupt enable in the MAC address 0: disabled 1: enabled
[29]	RW	ena_tx_rq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the RQ queue in the TX direction 0: disabled 1: enabled
[28]	RW	ena_rx_bq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the BQ queue in the RX direction 0: disabled 1: enabled
[27]	RW	ena_txoutcff_full_int	Full DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[26]	RW	ena_txoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[25]	RW	ena_txcff_full_int	Full DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled
[24]	RW	ena_txcff_empty_int	Empty DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled

[23]	RW	ena_rxoutcff_full_int	Full DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[22]	RW	ena_rxoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[21]	RW	ena_rxcff_full_int	Full DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[20]	RW	ena_rxcff_empty_int	Empty DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[19]	RW	ena_tx_rq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the tx_rq queue in the TX direction 0: disabled 1: enabled
[18]	RW	ena_tx_bq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the tx_bq queue in the TX direction 0: disabled 1: enabled
[17]	RW	ena_rx_bq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the rx_bq queue in the RX direction 0: disabled 1: enabled
[16]	RW	ena_rx_fq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the rx_fq queue in the RX direction 0: disabled 1: enabled
[15]	RW	ena_tx_rq_empty_int	Empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[14]	RW	ena_tx_rq_full_int	Full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[13]	RW	ena_tx_rq_alempty_int	Almost-empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled

[12]	RW	ena_tx_rq_alfull_int	Almost-full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[11]	RW	ena_tx_bq_empty_int	Empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[10]	RW	ena_tx_bq_full_int	Full buff descriptor queue interrupt enable in the TX direction 1: enabled 0: disabled
[9]	RW	ena_tx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[8]	RW	ena_tx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[7]	RW	ena_rx_bq_empty_int	Empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[6]	RW	ena_rx_bq_full_int	Full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[5]	RW	ena_rx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[4]	RW	ena_rx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[3]	RW	ena_rx_fq_empty_int	Empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[2]	RW	ena_rx_fq_full_int	Full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

[1]	RW	ena_rx_fq_alempty_int	Almost-empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[0]	RW	ena_rx_fq_alfull_int	Almost-full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

STATUS_PMU_INT

STATUS_PMU_INT is a PMU interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000005C8	STATUS_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	status_mac_fifo_err_int	status_tx_rq_in_timeout_int	status_rx_bq_in_timeout_int	status_txoutcff_full_int	status_txoutcff_empty_int	status_txcff_full_int	status_txcff_empty_int	status_rxoutcff_full_int	status_rxoutcff_empty_int	status_rxcff_full_int	status_rxcff_empty_int	status_tx_rq_in_int	status_tx_bq_out_int	status_rx_bq_in_int	status_rx_fq_out_int	status_tx_rq_empty_int	status_tx_rq_full_int	status_tx_rq_alempty_int	status_tx_rq_alfull_int	status_tx_bq_empty_int	status_tx_bq_full_int	status_tx_bq_alempty_int	status_tx_bq_alfull_int	status_rx_bq_empty_int	status_rx_bq_full_int	status_rx_bq_alempty_int	status_rx_bq_alfull_int	status_rx_fq_empty_int	status_rx_fq_full_int	status_rx_fq_alempty_int	status_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	status_mac_fifo_err_int	Status of the MAC internal FIFO empty and full error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[29]	RW	status_tx_rq_in_timeout_int	Status of the TX RQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[28]	RW	status_rx_bq_in_timeout_int	Status of the RX BQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[27]	RW	status_txoutcff_full_int	Status of the TX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[26]	RW	status_txoutcff_empty_int	Status of the TX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RW	status_txcff_full_int	Status of the TX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RW	status_txcff_empty_int	Status of the TX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[23]	RW	status_rxoutcff_full_int	Status of the RX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[22]	RW	status_rxoutcff_empty_int	Status of the RX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[21]	RW	status_rxcff_full_int	Status of the RX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RW	status_rxcff_empty_int	Status of the RX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RW	status_tx_rq_in_int	Status of the tx_rq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RW	status_tx_bq_out_int	Status of the tx_bq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	status_rx_bq_in_int	Status of the rx_bq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	status_rx_fq_out_int	Status of the rx_fq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[15]	RW	status_tx_rq_empty_int	Status of the TX recycle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	status_tx_rq_full_int	Status of the TX recycle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	status_tx_rq_alempty_int	Status of the TX recycle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RW	status_tx_rq_alfull_int	Status of the TX recycle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RW	status_tx_bq_empty_int	Status of the TX buff descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RW	status_tx_bq_full_int	Status of the TX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RW	status_tx_bq_alempty_int	Status of the TX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RW	status_tx_bq_alfull_int	Status of the TX buff descriptor queue almost-full interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[7]	RW	status_rx_bq_empty_int	Status of the RX buff descriptor queue empty interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[6]	RW	status_rx_bq_full_int	Status of the RX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RW	status_rx_bq_alempty_int	Status of the RX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	status_rx_bq_alfull_int	Status of the RX buff descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RW	status_rx_fq_empty_int	Status of the RX idle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RW	status_rx_fq_full_int	Status of the RX idle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RW	status_rx_fq_almpty_int	Status of the RX idle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	status_rx_fq_alfull_int	Status of the RX idle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

DESC_WR_RD_ENA

DESC_WR_RD_ENA is a cff read/write descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x000005CC	DESC_WR_RD_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_outcff_wr_desc_ena	rx_cff_rd_desc_ena	tx_outcff_wr_desc_ena	tx_cff_rd_desc_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	rx_outcff_wr_desc_ena	RX_OUTCFF write descriptor to RX_BQ enable in the RX direction 0: disabled 1: enabled
[2]	RW	rx_cff_rd_desc_ena	RX_CFF read descriptor from the idle descriptor queue enable in the RX direction 0: disabled 1: enabled

[1]	RW	tx_outcff_wr_desc_ena	TX_OUTCFF write descriptor to TX_RQ enable in the TX direction 0: disabled 1: enabled
[0]	RW	tx_cff_rd_desc_ena	TX_CFF read descriptor from TX_BQ enable in the TX direction 0: disabled 1: enabled

IN_QUEUE_TH

IN_QUEUE_TH is an rx_bq or tx_rq enqueue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05D8	IN_QUEUE_TH	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rq_in_th								reserved								rx_bq_in_th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	tx_rq_in_th	Threshold for reporting descriptor enqueue interrupts in the TX direction. The threshold must be greater than or equal to 1.
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_bq_in_th	Threshold for reporting descriptor enqueue interrupts in the RX direction. The threshold must be greater than or equal to 1.

OUT_QUEUE_TH

OUT_QUEUE_TH is an rx_fq or tx_bq dequeue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05DC	OUT_QUEUE_TH	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_bq_out_th								reserved								rx_fq_out_th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:16]	RW	tx_bq_out_th	Threshold for reporting descriptor dequeue interrupts in the TX direction
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_fq_out_th	Threshold for reporting descriptor dequeue interrupts in the RX direction

RX_BQ_IN_TIMEOUT_TH

RX_BQ_IN_TIMEOUT_TH is an rx_bq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E0	RX_BQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_bq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_bq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the BQ queue in the RX direction

TX_RQ_IN_TIMEOUT_TH

TX_RQ_IN_TIMEOUT_TH is a tx_rq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E4	TX_RQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_rq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the RQ queue in the TX direction

STOP_CMD

STOP_CMD is an RX and TX packet control stop register.

Offset Address	Register Name	Total Reset Value
0x05E8	STOP_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx_stop_en	rx_stop_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_stop_en	Packet TX stop enable 0: disabled 1: enabled
[0]	RW	rx_stop_en	Packet RX stop enable 0: disabled 1: enabled

FLUSH_CMD

FLUSH_CMD is a recycle descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x05EC	FLUSH_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_flush_cmd	rx_flush_cmd	tx_flush_flag_down	tx_flush_flag_up	rx_flush_flag_down	rx_flush_flag_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	tx_flush_cmd	Recycle descriptor command in the TX direction, instructing the descriptors to enter the tx_rq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[4]	RW	rx_flush_cmd	Recycle descriptor command in the RX direction, instructing the descriptors to enter the rx_bq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[3]	RW	tx_flush_flag_down	Recycle descriptor stop indicator in the TX direction. After descriptors are recycled, the logic sets tx_flush_flag to 1, and the software writes 1 to clear the register.
[2]	RW	tx_flush_flag_up	Recycle descriptor stop indicator in the TX direction. After RX and TX packets are stopped, the logic sets tx_flush_flag to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.
[1]	RW	rx_flush_flag_down	Recycle descriptor stop indicator in the RX direction. After descriptors are recycled, the logic sets rx_flush_flag_down to 1, and the software writes 1 to clear the register.
[0]	RW	rx_flush_flag_up	Recycle descriptor indicator in the RX direction. After RX packets are stopped, the logic sets rx_flush_flag_up to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.

U_EEE_INTR_SRC

U_EEE_INTR_SRC is an LPI status register in the RX and TX directions.

Offset Address	Register Name	Total Reset Value
0x0800	U_EEE_INTR_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_lpi_cond	rx_leave_lpi	rx_entry_lpi	tx_leave_lpi	tx_entry_lpi
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	tx_lpi_cond	LPI status in the TX direction 0: The TX FIFO and TX descriptors cannot be empty simultaneously. 1: The TX FIFO and TX descriptors are empty simultaneously.
[3]	RW	rx_leave_lpi	LPI exit in the RX direction 0: not exited 1: exited
[2]	RW	rx_entry_lpi	LPI enter in the RX direction 0: not entered 1: entered
[1]	RW	tx_leave_lpi	LPI exit in the TX direction 0: not exited 1: exited
[0]	RW	tx_entry_lpi	LPI enter in the TX direction 0: not entered 1: entered

U_EEE_INTR_EN

U_EEE_INTR_EN is an interrupt mask and enable register in the RX and TX directions.

Offset Address	Register Name	Total Reset Value
0x0804	U_EEE_INTR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_lpi_cond_msk	rx_leave_lpi_msk	rx_entry_lpi_msk	tx_leave_lpi_msk	tx_entry_lpi_msk	tx_lpi_cond_en	rx_leave_lpi_en	rx_entry_lpi_en	tx_leave_lpi_en	tx_entry_lpi_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	tx_lpi_cond_msk	LPI status interrupt mask in the TX direction 0: not masked 1: masked
[8]	RW	rx_leave_lpi_msk	LPI status exit interrupt mask in the RX direction 0: not masked 1: masked
[7]	RW	rx_entry_lpi_msk	LPI status enter interrupt mask in the RX direction 0: not masked 1: masked
[6]	RW	tx_leave_lpi_msk	LPI status exit interrupt mask in the TX direction 0: not masked 1: masked
[5]	RW	tx_entry_lpi_msk	LPI status enter interrupt mask in the TX direction 0: not masked 1: masked
[4]	RW	tx_lpi_cond_en	LPI status interrupt enable in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[3]	RW	rx_leave_lpi_en	LPI status interrupt enable exit in the RX direction 0: Disable interrupts. 1: Enable interrupts.
[2]	RW	rx_entry_lpi_en	LPI status interrupt enable enter in the RX direction 0: Disable interrupts. 1: Enable interrupts.

[1]	RW	tx_leave_lpi_en	LPI status interrupt enable exit in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[0]	RW	tx_entry_lpi_en	LPI status interrupt enable enter in the TX direction 0: Disable interrupts. 1: Enable interrupts.

U_EEE_ENABLE

U_EEE_ENABLE is an EEE enable signal register.

Offset Address	Register Name	Total Reset Value
0x0808	U_EEE_ENABLE	0x00F4_2400

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	eee_ls_timer							gmii_mode	cond_intr_keep	tx_lpi_assert	eee_enable
Reset	0 0 0 0	0 0 0 0	1 1 1 1	0 1 0 0	0 0 1 0	0 1 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	Buffer time for the buffer software to enable the hardware to enter the LPI when phy_link_sts is set to 1. The default time is 1s.
[3]	RW	gmii_mode	GMII mode select 0: MII mode 1: GMII mode
[2]	RW	cond_intr_keep	Interrupt signal TX frequency 0: The hardware sends only one tx_lpi_cond interrupt. 1: The interrupt is enabled on the rising edge of each clock in LPI mode in the TX direction.
[1]	RW	tx_lpi_assert	Software configuring the hardware to enter the LPI state 0: The hardware does not enter the LPI state. 1: The hardware enters the LPI state.
[0]	RW	eee_enable	EEE module enable 0: disabled 1: enabled

U_EEE_TIMER

U_EEE_TIMER is an LPI time threshold register.

Offset Address	Register Name	Total Reset Value
0x080C	U_EEE_TIMER	0x001E_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lpi_tw_timer																lpi_cond_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	lpi_tw_timer	Wake-up time of the register from the LPI mode to normal mode. The default time is 30 μs.
[15:0]	RW	lpi_cond_timer	Duration when the TX FIFO and EX_DESC are empty at the same time. When the duration is equal to the value of lpi_cond_timer, the register enters the LPI mode.

U_EEE_LINK_STATUS

U_EEE_LINK_STATUS is an EEE status register.

Offset Address	Register Name	Total Reset Value
0x0810	U_EEE_LINK_STATUS	0x0000_3F20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_cnt																eee_tx_lpi_stay	eee_rx_lpi_stay_ff3	version										reserved	eee_auto	eee_hold_txdesc_read	phy_link_sts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	intr_cnt	EEE interrupt count
[15]	RO	eee_tx_lpi_stay	Whether the TX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.
[14]	RO	eee_rx_lpi_stay_ff3	Whether the RX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.

[13:4]	RO	version	Logical version number
[3]	RO	reserved	Reserved
[2]	RW	eee_auto	Automatic EEE entry and exit 0: The logic enters or exits the EEE mode by using the software and logic interrupt. 1: The logic automatically enters or exits the EEE without the intervention of software.
[1]	RW	eee_hold_txdesc_read	Whether the MAC can obtain packets from the TX FIFO in LPI status 0: yes 1: no
[0]	RW	phy_link_sts	PHY connection state 0: link_down 1: link_up

U_EEE_TIME_CLK_CNT

U_EEE_TIME_CLK_CNT is a timing pulse count register.

Offset Address	Register Name	Total Reset Value
0x0814	U_EEE_TIME_CLK_CNT	0x0000_007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_period_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:0]	RW	clk_period_cnt	Count register used to generate a 1 μs timing pulse in the hardware. The clock cycle is 8 ns when the clock frequency is 125 MHz.

PMT_CTRL_STAUTS

PMT_CTRL_STAUTS is a PMT control and status register.

Offset Address	Register Name	Total Reset Value
0x0A00	PMT_CTRL_STAUTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						scr_wkupfrm_glbucast	reserved		rcvd_wkup_frm	rcvd_mgk_pkt	reserved	scr_intr_en	scr_wkupfrm_en	scr_mgkpkt_en	scr_power_down
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	scr_wkupfrm_glbucast	Whether the unicast frame used to configure the MAC address is the wake-up frame 0: The unicast frame is not regarded as the wake-up frame. 1: The unicast frame used to configure the MAC address is regarded as the valid wake-up frame.
[8:7]	RO	reserved	Reserved
[6]	RW	rcvd_wkup_frm	Whether a wake_up frame is received 0: no 1: yes
[5]	RW	rcvd_mgk_pkt	Whether the magic packet is received. 0: no 1: yes
[4]	RO	reserved	Reserved
[3]	RW	scr_intr_en	PMT interrupt enable 0: disabled 1: enabled
[2]	RW	scr_wkupfrm_en	wake_up frame receive enable 0: disabled 1: enabled
[1]	RW	scr_mgkpkt_en	Magic packet receive enable 0: disabled 1: enabled
[0]	RW	scr_power_down	Power-down mode enable 0: Exit the power-down mode. 1: Enter the power-down mode.

FILTER_0_BYTE_MASK

FILTER_0_BYTE_MASK is PMT valid byte selection register 0.

Offset Address	Register Name	Total Reset Value
0x0A04	FILTER_0_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter0bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter0bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask. If a bit is 1, the corresponding byte is valid.

FILTER_1_BYTE_MASK

FILTER_1_BYTE_MASK is PMT valid byte selection register 1.

Offset Address	Register Name	Total Reset Value
0x0A08	FILTER_1_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter1bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_2_BYTE_MASK

FILTER_2_BYTE_MASK is PMT valid byte selection register 2.

Offset Address	Register Name	Total Reset Value
0x0A0C	FILTER_2_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter2bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter2bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_3_BYTE_MASK

FILTER_3_BYTE_MASK is PMT valid byte selection register 3.

Offset Address	Register Name	Total Reset Value
0x0A10	FILTER_3_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter3bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_COMMAND

FILTER_COMMAND is a PMT template selection and multicast enable register.

Offset Address	Register Name	Total Reset Value
0x0A14	FILTER_COMMAND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wkupfrm_filter3mcast	reserved		wkupfrm_filter3en	reserved				wkupfrm_filter2mcast	reserved		wkupfrm_filter2en	reserved				wkupfrm_filter1mcast	reserved		wkupfrm_filter1en	reserved				wkupfrm_filter0mcast	reserved		wkupfrm_filter0en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	wkupfrm_filter3mcast	Address type specified by template 3 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[26:25]	RO	reserved	Reserved.
[24]	RW	wkupfrm_filter3en	Filter template 3 enable 0: disabled 1: enabled
[23:20]	RO	reserved	Reserved
[19]	RW	wkupfrm_filter2mcast	Address type specified by template 2 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[18:17]	RO	reserved	Reserved
[16]	RW	wkupfrm_filter2en	Filter template 2 enable 0: disabled 1: enabled
[15:12]	RO	reserved	Reserved

[11]	RW	wkupfrm_filter1mcast	Address type specified by template 1 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[10:9]	RO	reserved	Reserved.
[8]	RW	wkupfrm_filter1en	Filter template 1 enable 0: disabled 1: enabled
[7:4]	RO	reserved	Reserved
[3]	RW	wkupfrm_filter0mcast	Address type specified by template 0 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[2:1]	RO	reserved	Reserved.
[0]	RW	wkupfrm_filter0en	Filter template 0 enable 0: disabled 1: enabled

FILTER_OFFSET

FILTER_OFFSET is a CRC position offset register.

Offset Address	Register Name	Total Reset Value
0x0A18	FILTER_OFFSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wkupfrm_filter3offset		wkupfrm_filter2offset		wkupfrm_filter1offset		wkupfrm_filter0offset	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wkupfrm_filter3offset	Template 3 of the four templates, used to calculate the CRC position offset
[23:16]	RW	wkupfrm_filter2offset	Template 2 of the four templates, used to calculate the CRC position offset
[15:8]	RW	wkupfrm_filter1offset	Template 1 of the four templates, used to calculate the CRC position offset
[7:0]	RW	wkupfrm_filter0offset	Template 0 of the four templates, used to calculate the CRC position offset

FILTER0_1_CRC

FILTER0_1_CRC is a software-expected CRC value 0 and 1 register.

Offset Address	Register Name	Total Reset Value
0x0A1C	FILTER0_1_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1crc																wkupfrm_filter0crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter1crc	CRC value expected by software of template 1 in the four templates
[15:0]	RW	wkupfrm_filter0crc	CRC value expected by software of template 1

FILTER2_3_CRC

FILTER2_3_CRC is a software-expected CRC value 2 and 3 register.

Offset Address	Register Name	Total Reset Value
0x0A20	FILTER2_3_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3crc																wkupfrm_filter2crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter3crc	CRC value expected by software of template 3
[15:0]	RW	wkupfrm_filter2crc	CRC value expected by software of template 2

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Figures

6 Video Encoder

6.1 VEDU

The encoding unit consists of the video encoding units (VEDU) and JPEG encoder (JPGE). The VEDU supports H.264 and H.265 encoding, and the JPGE supports JPEG and MJPEG encoding.

6.1.1 Overview

The VEDU is a CODEC that supports H.264 and H.265 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, short delay, and low power consumption.

6.1.2 Features

The VEDU has the following features:

- Supports ITU-T H.265 main profile @level 6.1 main-tier encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four prediction unit (PU) types of 64x64, 32x32, 16x16, and 8x8 for inter-prediction
  - Four PU types of 32x32, 16x16, 8x8, and 4x4 for intra-prediction
  - Skip mode and merge mode with a maximum of two candidate points to be merged
  - Four transform unit (TU) types of 32x32, 16x16, 8x8, and 4x4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
  - IPCM encoding
- Supports ITU-T H.264 main profile @level 5 main-tier encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Two prediction unit (PU) types of 16x16, and 8x8 for inter-prediction
  - Four PU types of 16x16, 8x8, and 4x4 for intra-prediction
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
  - IPCM encoding

- Supports H.264 scalable video coding (SVC) time-domain layering (SVC-T).
- Supports the input picture format of semi-planar YCbCr4:2:0.
- Supports H.264/H.265 multi-stream encoding with the performance of 8-megapixel (3840 x 2160)@30 fps+720p@30 fps.
- Supports configurable picture resolutions.
  - Minimum picture resolution: 128 x 128 (H.265) or 192 x 144 (H.264)
  - Maximum picture resolution: 4608 x 4608
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding.
  - A maximum of eight ROIs
  - Independent enable/disable control for the encoding function of each ROI
- Supports on-screen display (OSD) encoding protection that can be enabled or disabled.
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlaying anywhere (the maximum OSD size is the picture size)
  - 129-level alpha blending
  - OSD overlaying control
- Supports color-to-gray encoding.
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP.
- Supports the output bit rate ranging from 2 kbit/s to 100 Mbit/s.

CAUTION

The VEDU encoding protection function applies only to the OSD overlaid on the VEDU.

6.1.3 Function Description

Figure 6-1 shows the functional block diagram of the VEDU.

Based on related protocols and algorithms, the VEDU supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding, stream generation, de-blocking filtering, and SAO (H.265). The ARM software controls the bit rate and handles interrupts.

Before the VEDU is enabled for video encoding, software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Input picture buffer

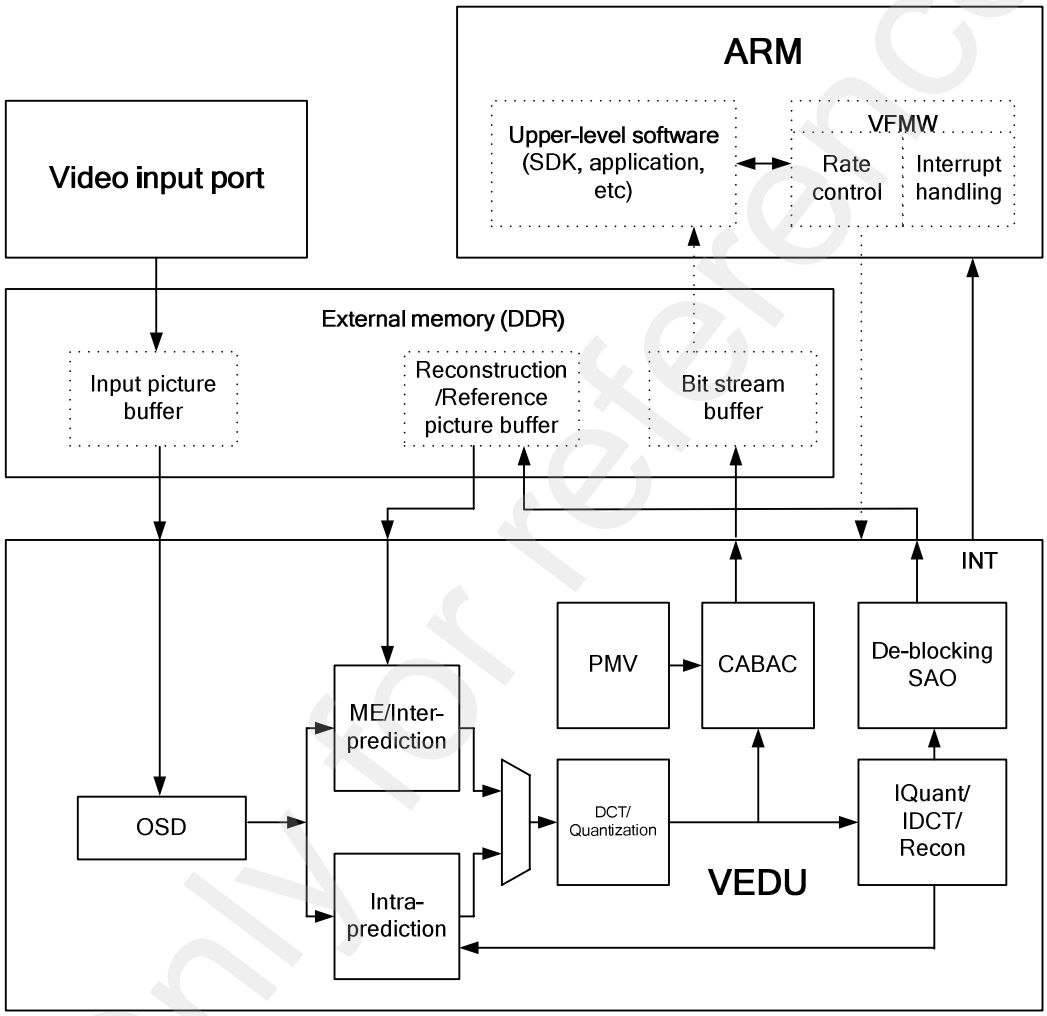
  The VEDU reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.
- Reconstruction/Reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.

- Stream buffer

  This buffer stores encoded streams. The VEDU writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-1 Encoding functional block diagram of the VEDU



6.2 JPGE

6.2.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports 67.1-megapixel snapshot or HD MJPEG encoding.

6.2.2 Features

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding.
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0 and YCbCr4:2:2.
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports JPEG encoding:
  - 8-megapixel (3840 x 2160)@30 fps
  - 12-megapixel (4224 x 2816)@20 fps
  - 16-megapixel (4608 x 3456)@15 fps
- Supports configurable picture resolutions.
  - Minimum picture resolution: 32 x 32
  - Maximum picture resolution: 8192 x 8192
- Supports the picture width or height step of 2.
- Supports configurable quantization tables. Two quantization tables are provided for the Y, Cb, and Cr components (the Cb and Cr components share one quantization table).
- Supports the color-to-gray function.

6.2.3 Function Description

Figure 6-2 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

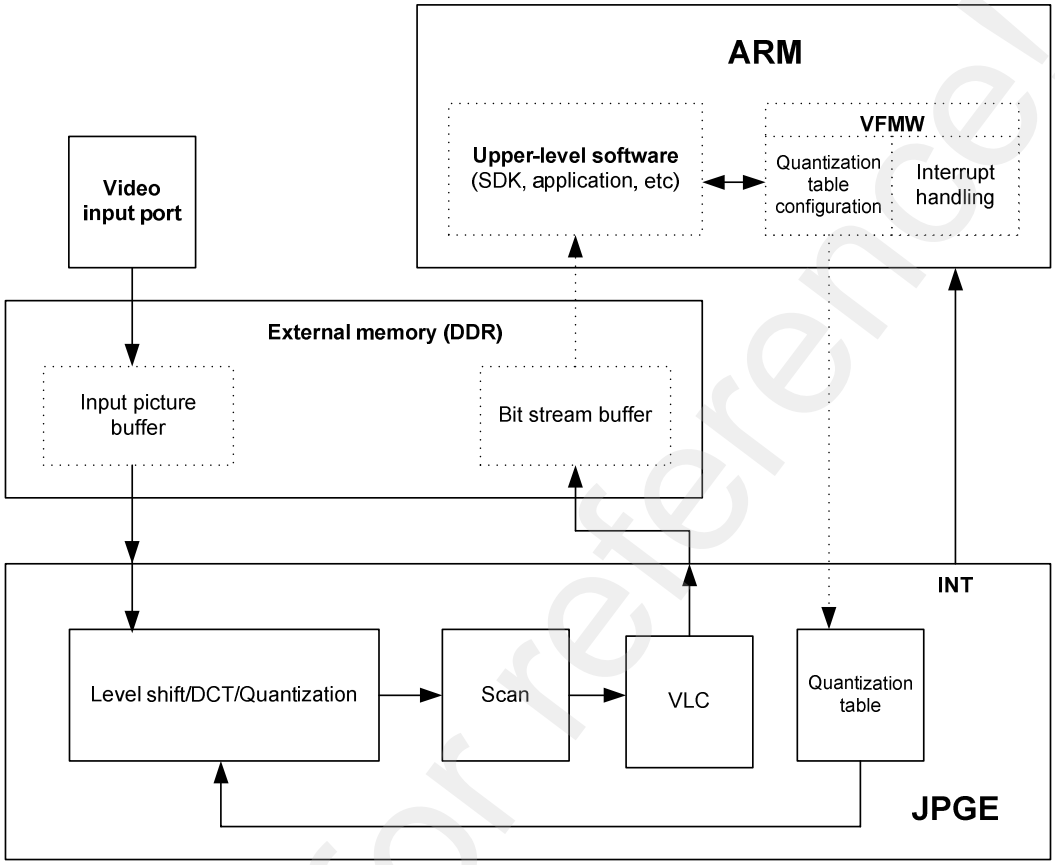
Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-2 Encoding functional block diagram of the JPGE



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7 Video and Graphics Processing

7.1 TDE

7.1.1 Overview

The two-dimensional engine (TDE) draws graphics using hardware. This significantly reduces the CPU usage and improves the utilization of the memory bandwidth. The TDE reads and writes the information about the bitmap data, filtering/scaling coefficients, parameters of linked list nodes, and linked list over the advanced eXtensible bus (AXI) master interface. By using the advanced peripheral bus (AHB) interface, the TDE obtains the CPU register configuration information.

The graphics data interface includes two channels. Their functions are as follows:

- Channel 1 implements direct copy and direct filling during a single-source operation.
- Channel 2 implements complicated functions such as scaling during a single-source operation.
- Channel 1 works with channel 2 to implement color blending.

7.1.2 Function Description

The TDE has the following features:

- Channel 1 supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, halfword.
- Channel 2 supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8.
- The output picture supports the formats of ARGB4444, ARGB1555, ARGB8888, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, byte, halfword.
- Supports only the little-endian system.
- Allows the formats of source bitmap 1, source bitmap 2, and output bitmaps to be configured separately.
- Supports gamma correction and adjustable contrast and luminance.
- Supports direct copy.
- Supports direct filling.
- Supports 2D resize.

- Supports clip.
- Supports alpha blending.
- Supports colorkey.
- Supports clip mask.
- Supports inverse scanning.
- Provides status interrupts.

7.2 VPSS

7.2.1 Overview

The video processing subsystem (VPSS) implements video processing. It supports Gaussian 3D adaptive noise reduction (NR) as well as video covering, cropping, scaling, mirroring, flipping, and single-component luminance processing.

The VPSS has the following features:

- Processing of video sources with 4096-pixel width using a single frame in online or offline mode
- A maximum of four video output channels including three encoding channels and one display channel
- Output of eight video regions covered by solid quadrilaterals (the concave quadrilateral is converted into a triangle)
- Video cropping four three output channels (two encoding channels and one display channel)
- Video data compression
- Register configuration using the linked list in offline mode and register configuration using the APB in online mode
- Span of 4 KB boundary
- Input or output data format of semi-planar 420/422
- Outstanding configuration
- Memory low-power mode by using clock gating
- Low delay
- Single-component luminance processing

7.2.2 Features

The following describes the major features:

- Gaussian NR: The NR module removes the Gaussian noises from pictures by configuring parameters. Then pictures become smooth and the encoding bit rate is reduced.
- Scaling: Low-frequency filtering is supported when the input and output resolutions are different. In online mode, the large stream channel supports 1:1 scaling, whereas other channels support zoom-out or 1:1 scaling and do not support zoom-in. In offline mode, only the large stream channel supports zoom-in (at most 16x zoom-in), whereas other channels support zoom-out (at most 15x zoom-out).

7.3 VGS

7.3.1 Overview

The video graphics system (VGS) implements video and graphics processing. The functions include OSD overlaying, luminance region statistics, video cropping, video covering, and rotation.

The VGS has the following features:

- Processing of video sources with the 4096-pixel width by using a single frame in offline mode
- One video output channel
- Overlaying of the OSD and video in one region
- OSD input format of ARGB1555, ARGB4444, or ARGB8888
- Configuration of register linked lists
- Span of 4 KB boundary
- Linear storage for input/output data
- Video data compression
- Rotation by 90º or 270º
- One video region covered by the solid or dashed quadrilateral (the concave quadrilateral is converted into a triangle)
- Video cropping
- Outstanding configuration
- Memory low-power mode by using clock gating
- Statistics of the region luminance sum
- Single-component luminance processing

7.3.2 Features

The following describes the major features:

- Video covering: A video region is covered by the solid or dashed quadrilateral (the concave quadrilateral is converted into a triangle).
- Scaling: Low-frequency filtering is supported when the input and output resolutions are different. At most 15.5x zoom-out and 16x zoom-in are supported.

7.4 GDC

7.4.1 Overview

The geometric distortion correction (GDC) module implements picture distortion correction.

The GDC module has the following features:

- Processing of video sources with the maximum resolution of 16 megapixels by using a single frame in offline mode

- Maximum processing performance of 8 megapixels@30 fps when only one mode is enabled
- Input and output of YUV semi-planar420 pictures
- 360°, 180°, and normal fisheye correction models
- Top mount, wall mount, and desk mount installation modes
- Pan-tilt-zoom (PTZ) function in three fisheye correction modes
- 20% lens distortion correction (LDC)
- Configuration of register linked lists
- Span of 4 KB boundary
- Linear storage for input and output data
- Input of uncompressed video pictures and output of compressed video data
- Outstanding configuration
- Memory low-power mode by using clock gating

7.4.2 Features

- Fisheye correction: After the fisheye function is enabled, the output resolution can be configured based on the selected visible region and correction model to ensure that the picture quality is optimal after correction.
- Installation modes: Three installation modes are supported. In actual application scenarios, the installation mode and correction model need to be selected as required to ensure that the correction effect is optimal.

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Tables

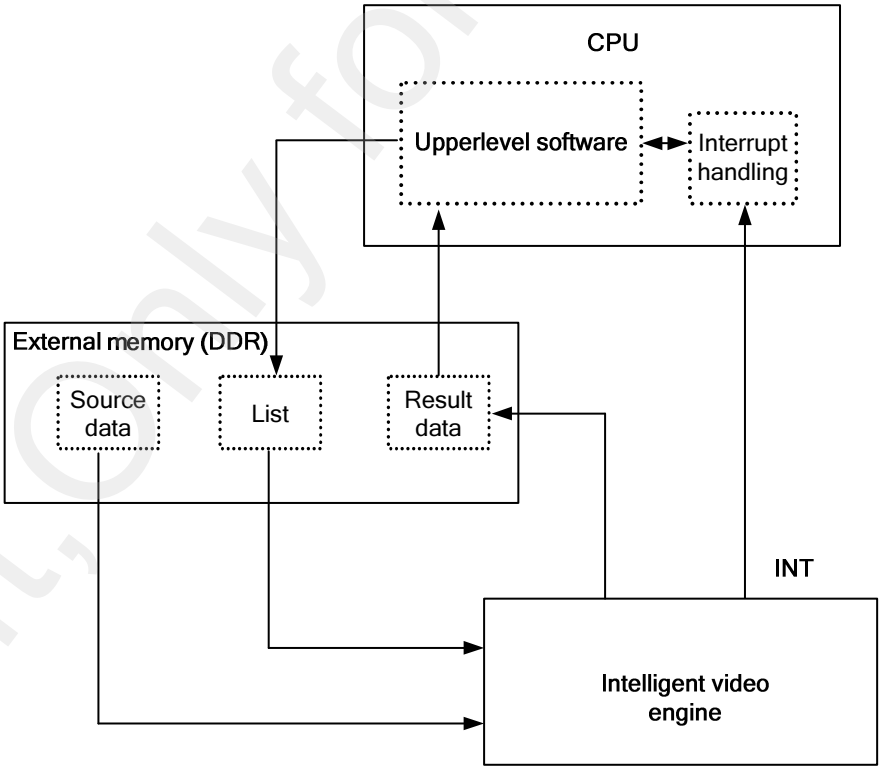
8 Intelligent Video Engine

8.1 IVE

8.1.1 Overview

The intelligent video engine (IVE) module is used to accelerate hardware processing. It provides a series of basic calculation functions and some time-consuming functions used in the intelligent analysis algorithm.

Figure 8-1 Position of the IVE in the system



8.1.2 Function Description

The IVE has the following features:

- DMA: Supports direct copying, alternative copying, and memory filling.
- Filter: Supports 5x5 template filtering.
- Color space conversion (CSC): Supports the color space conversion of YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV.
- FilterAndCSC: Combines 5x5 template filtering and CSC.
- Sobel: Supports the Sobel-like gradient calculation of 5x5 template.
- MagAndAng/Canny: Supports 5x5 template calculation and Canny edge extraction.
- Erode: Supports 5x5 template erode.
- Dilate: Supports 5x5 template dilate.
- Thresh\Thresh_S16\Thresh_U16: Supports image thresh processing.
- And\Or\Xor: Supports the AND, OR, or XOR operation on two images.
- Add\Sub: Deals with the weighted plus and minus of two images.
- Integ: Supports the integral calculation.
- Hist: Supports the histogram statistics.
- Map: Assigns values to images by using 256-level mapping.
- 16BitTo8Bit: Performs linear conversion from 16-bit data to 8-bit data.
- OrdStatFilter: Supports the sequence statistic filtering, including the median filtering, maximum filtering, and minimum filtering.
- Bernsen: Supports Bernsen thresh.
- NCC: Calculates the correlation coefficients of two images with the same size.
- CCL: Marks connected regions.
- GMM: Creates the GMM for a gray scale image and RGB image.
- LBP: Supports the calculation in simple partial thresh mode.
- NormGrad: Performs a normalized gradient calculation.
- LKOpticalFlow: Tracks the LK optical flow.
- STCorner: Detects the ShiTomasi point.
- GradFg: Supports the gradient foreground calculation.
- MatchBgModel\UpdateBgModel: Supports background match and background refresh.
- ANN_MLP_Predict: Predicts ANN_MLP.
- SVM_Predict: Predicts SVS_MLP.
- Resize: Supports scaling of bilinear and regional images.
- GMM2: Creates the GMM quickly for the gray scale image and RGB image.
- CNN: Calculates the convolutional neural network (CNN).
- SAD: This function calculates the accumulated sum of the absolute pixel differences corresponding to two images by block.
- Supports separate soft reset.
- Supports 128-bit AXI bus and 32-bit APB.
- Supports linked-list interrupt, node interrupt, and timeout interrupt.
- Supports input formats including SP400, semi-planar 420 (SP420), semi-planar 422 (SP422), package, and planar.

- Supports output formats including SP400, SP420, SP422, package, and planar.
- Supports non-16-byte-aligned read and write addresses for some operators.

8.1.3 Operating Mode

8.1.3.1 Input and Output Data Formats

The w and h in Figure 8-2 to Figure 8-12 indicate the width and height of images in pixels. Unless otherwise specified, the sequence for storing data is the same as that in the little endian system. The following sections use word as the storage unit. In actual applications, the data alignment format varies with operators. The input and output format for operators described in section8.1.3.2 "Supported Functions" are also different.

Figure 8-2 SP422 storage format

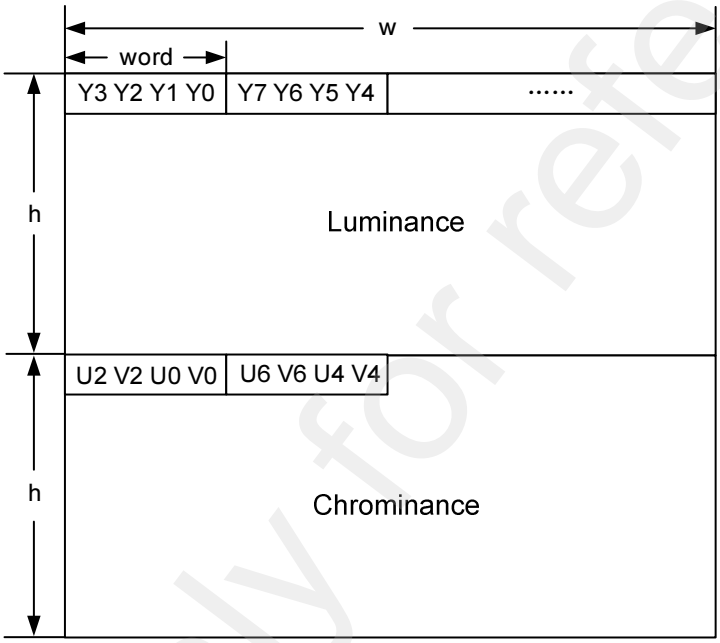


Figure 8-3 SP420 storage format

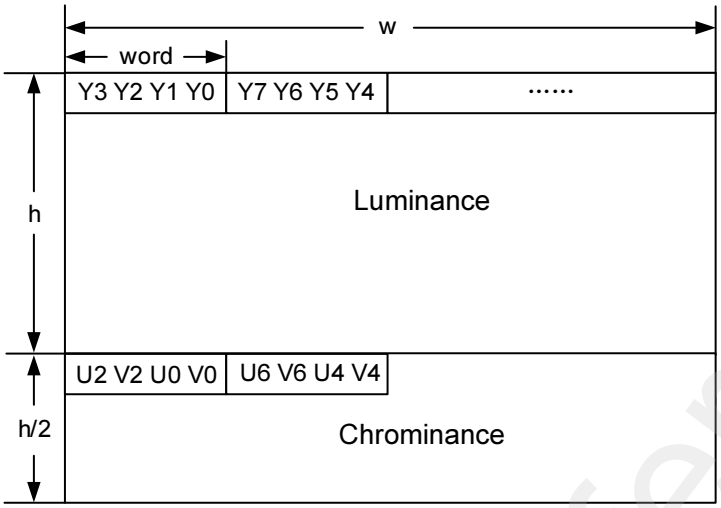


Figure 8-4 Storage format of the 8-bit single component data in the memory

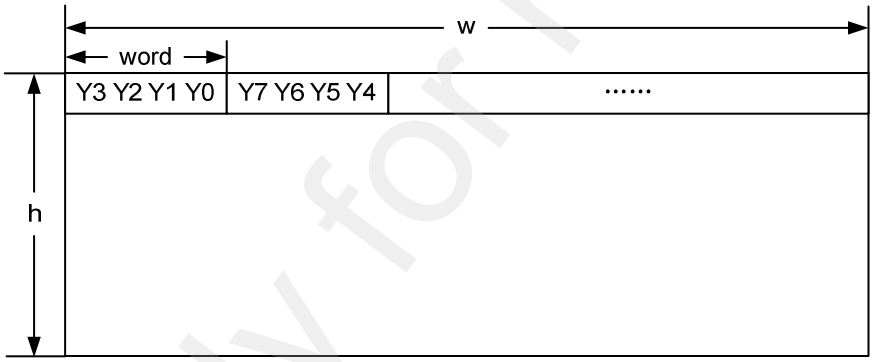


Figure 8-5 Package storage format

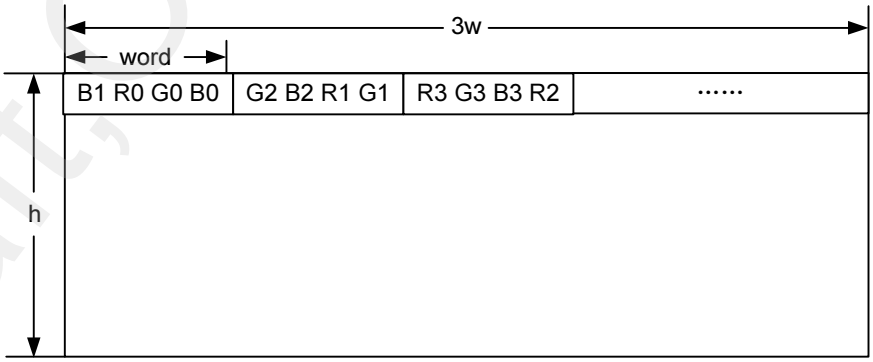


Figure 8-6 Planar storage format

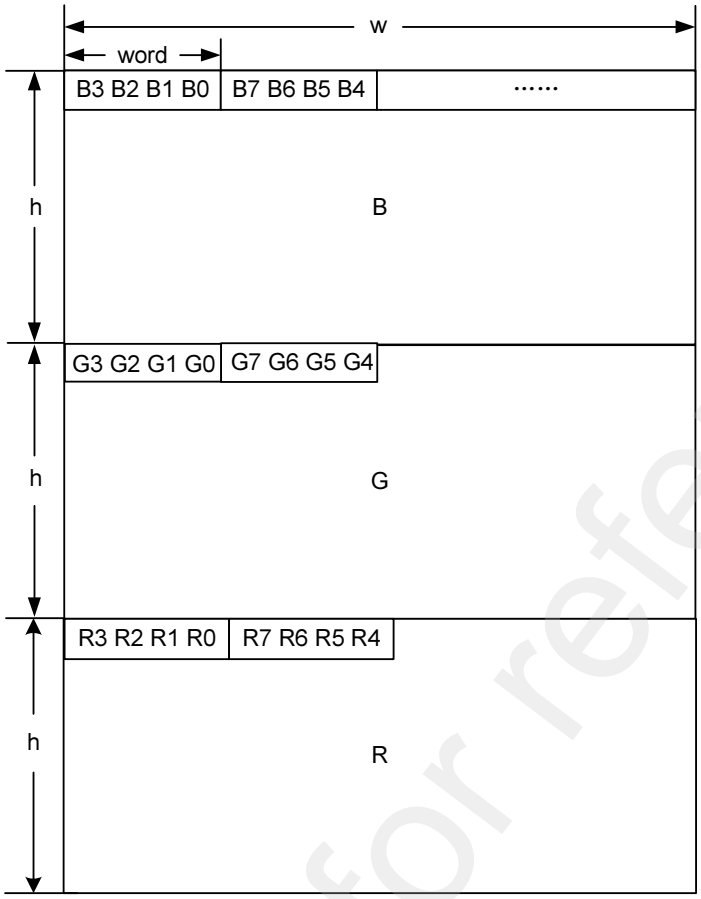


Figure 8-7 Storage format of the 16-bit single component data in the memory

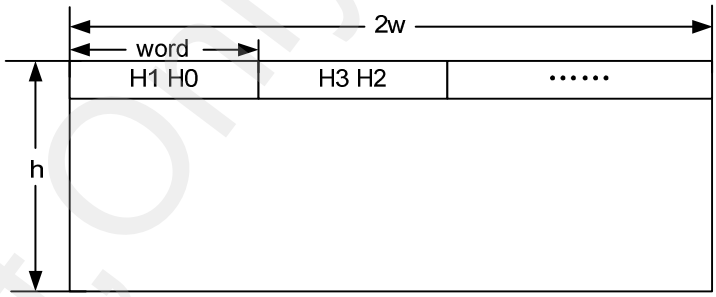


Figure 8-8 Storage format of the 32-bit single component data in the memory

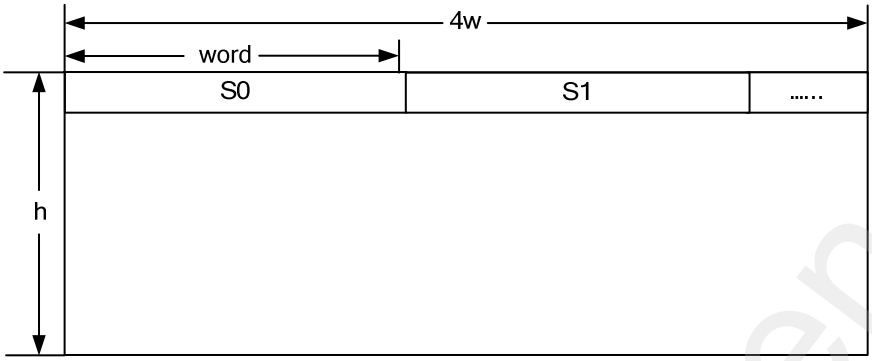


Figure 8-9 Storage format of the 64-bit single component data in the memory

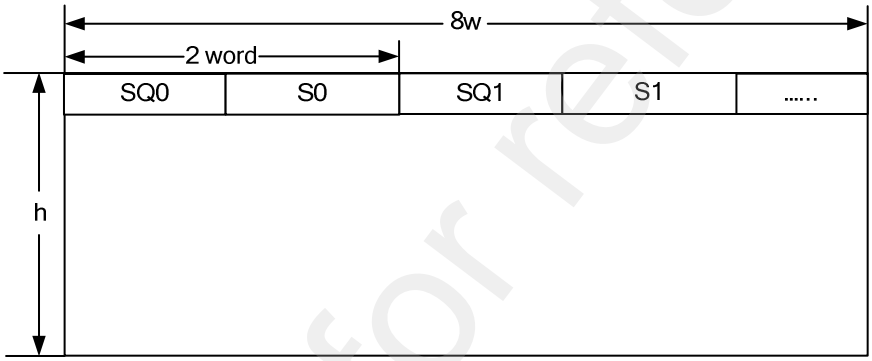


Figure 8-10 Storage format of NCC output data in the memory

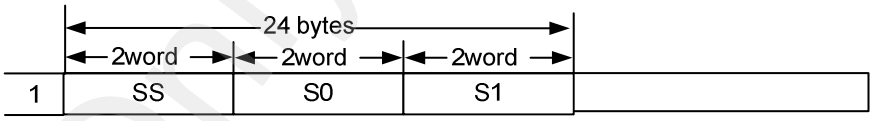
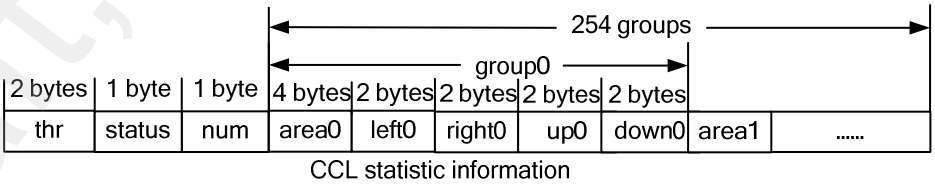
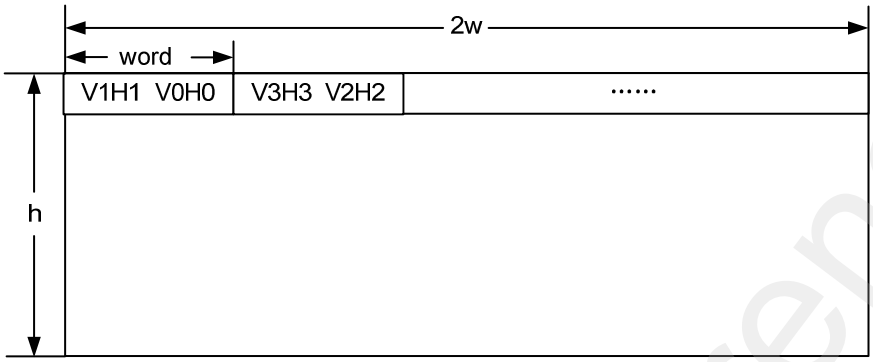


Figure 8-11 Storage format of CCL statistics in the memory (in sequence)



CCL statistic information

Figure 8-12 Storage format of 16-bit interleaving data (in the horizontal and vertical directions) in the memory



8.1.3.2 Supported Functions

DMA

1. Direct copy mode

This mode allows you to quickly transfer the data of rectangle regions. In this mode, the source data is transferred to the destination region through the internal fast channel, and directly overwrites the data of the destination region.

- Region size (byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

2. Alternative copy mode

This mode allows you to transfer the data of rectangle regions indirectly. In this mode, the source data with a specified size is transferred to the destination region at a specified distance in horizontal and vertical directions.

- Region size (byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.
- Others: The width of the source data must be an integral multiple of the distance.

3. Memset mode (3 bytes)

This mode allows you to set the memory in rectangle regions, and fill the destination region by three bytes.

- Region size (byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.

- Input and output formats: No input data is available. The output is 8-bit single component data, as shown in Figure 8-4.

4. Memset mode (8 bytes)

This mode allows you to set the memory in rectangle regions, with 8 byte as the unit for filling the target region.

- Region size (byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: There is no input data. The output is 8-bit single component data, as shown in Figure 8-4.

Filter

The source image is filtered based on the 5x5 template and then output.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- The following lists the three input and output formats:
  - Both the input and output are 8-bit single component data, as shown in Figure 8-4.
  - Both the input and output are SP420 data, as shown in Figure 8-3.
  - Both the input and output are SP422 data, as shown in Figure 8-2.

CSC

The YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV CSC is supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar
  - Package > SP420; package > SP422
  - Planar > SP420; planar > SP422

  Figure 8-3 and Figure 8-2 show the SP420 format and SP422 format respectively.

  Figure 8-5 shows the package format.

  Figure 8-6 shows the planar format.

FilterAndCSC

The YUV SP420/SP422 image is filtered based on the 5x5 template, the YUV2RGB CSC is implemented, and then the picture is output.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output formats:

- SP420 > package; SP420 > planar
- SP422 > package; SP422 > planar

Figure 8-3 and Figure 8-2 show the SP420 format and SP422 format respectively.

Figure 8-5 shows the package format.

Figure 8-6 shows the planar format.

Sobel

Vertical and horizontal Sobel filtering is implemented based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output formats:
  - The input is the 8-bit single-component image, as shown in Figure 8-4.
  - Only H or V is output, as shown in Figure 8-7.
  - Both H and V are output, as shown in Figure 8-7.

MagAndAng

The magnitude and angle of the picture gradient are calculated. The thresh operation for TO_ZERO is supported.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output formats:
  - The input is the 8-bit single-component image, as shown in Figure 8-5.
  - The output is the 16-bit single-component amplitude image, as shown in Figure 8-7.
  - The output is the 8-bit single-component angle image, as shown in Figure 8-4.

Dilate

A binary image can be dilated based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 8-4.

Erode

A binary image can be eroded based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

Thresh

The thresh operation is performed on an image using a fixed threshold. Eight configurable modes are supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

And

The AND operation is implemented for source data 2 and source data 1, and the result is output to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single component data of source 1.
  - The input is an 8-bit single component data of source 2.
  - The output is the 8-bit single component destination data, as shown in Figure 8-4.

Sub

The subtraction operation is implemented for source data 2 and source data 1, and the result is output to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - An 8-bit single component minuend.
  - An 8-bit single component subtrahend.
  - The 8-bit single component destination data, as shown in Figure 8-4

Or

The OR operation is implemented for source data 2 and source data 1, and the result is output to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The two input images are 8-bit single component images.
  - The output is the 8-bit single component image, as shown in Figure 8-4.

Integral

The sum integrogram and square sum integrogram are calculated, and the sum integrogram, square sum integrogram can be output separately or together (the accumulated component sum occupied the lower 28 bits, and the accumulated component square sum occupied the upper 36 bits).

- Resolution: 32 x 16 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 8-4.
  - As shown in Figure 8-8, if a sum integrogram is outputted, the output is a 32-bit single component image. As shown in Figure 8-9, if a square sum integrogram is outputted or is outputted by combining with a sum integrogram, the output is a 64-bit single component image.

Histogram

The 256-segment histogram statistics are supported. The input is a single component, and the output is the statistics of a 32-bit 256-segment histogram.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 8-4.
  - The output is the 32-bit single component data of the statistic result, as shown in Figure 8-8.

Thresh_S16

The thresh operation from the 16-bit signed data to 8-bit signed data is supported. Four comparison modes are supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 8-7.
  - The output is the converted 8-bit single component data, as shown in Figure 8-4.

Thresh_U16

The thresh operation from the 16-bit unsigned data to 8-bit unsigned data is supported. Four comparison modes are supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 8-7.
  - The output is the converted 8-bit single component data, as shown in Figure 8-4.

16BitTo8Bit

The linear conversion from the 16-bit data to 8-bit data is supported. It supports four comparison modes.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit data, as shown in Figure 8-7.
  - The output is the converted 8-bit data, as shown in Figure 8-4.

OrdStatFilter

The median filtering, maximum value filtering, and minimum value filtering for sequential statistics based on a 3x3 template are supported.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output formats: Both the input and output are 8-bit single component images, as shown in Figure 8-4.

Map

The source data is mapped by using the 256-segment 8-bit unsigned mapping table or 16-bit unsigned/signed mapping table, and the new data is output.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 8-4.
  - The input is the 8-bit or 16-bit mapping table with a fixed length of 256 entries.
  - The output is the 8-bit single component data or 16-bit data after mapping, as shown Figure 8-4 and Figure 8-7.

Add

The sum of the weighted values of two gray scale images is calculated. The weights of the two images can be separately configured.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.
  - The output is the sum of data of 8-bit single component image, as shown Figure 8-4.

Xor

The XOR operation on data of two binary images is supported.

- Resolution: 64 x 64 to 1920 x 1080. The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.
  - The output is the 8-bit single component data after performing the Xor operation, as shown in Figure 8-4.

NCC

The cross correlation coefficients of two gray scale images with the same resolution are calculated.

- Resolution: 20 x 20 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.
  - The output contains three types of data, namely the accumulative product of two images, accumulative product of square sum of image 1, and the accumulative product of square sum of image 2 (in sequence), as shown in Figure 8-10.

CCL

The eight or four connected regions of the binary image are marked.

- Resolution: 64 x 64 to 1280 x 720 (Width x Height < 1024 x 1024)
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image, as shown in Figure 8-4.
  - The 16-bit output data indicates the minimum area of the output valid connected components.
  - The 8-bit output data indicates whether the area of the detected connected components is greater than the threshold.
  - The output is the coordinate and area of the circumscribed rectangle for each connected component, as shown in Figure 8-11. The original image is changed to an 8-bit single component image after the labeling of the connected components, as shown in Figure 8-4.

GMM

The GMM background modeling for the gray scale images and RGB package images is supported. Three or five Gaussian models are supported.

- Resolution: 64 x 64 to 1280 x 720
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:

- The input is an 8-bit single component image or RGB package image, as shown in Figure 8-4 and Figure 8-5.
- The input is the model data.
- The output is the 8-bit single component foreground binary image, as shown in Figure 8-4.
- The output is the updated model data.
- The output is the background data and the corresponding input is an 8-bit single component image or RGB package image, as shown in Figure 8-4 and Figure 8-5.

CannyHysEdge

The thresh processing for magnetic hysteresis and suppression on non-maximum values are supported. The strong and weak edge images and coordinates of strong edges are output.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component angle image, as shown in Figure 8-4.
  - The input is a 16-bit single component amplitude image, as shown in Figure 8-7.
  - The output is an 8-bit single edge mark image, as shown in Figure 8-4.
  - The output is a 32-bit single component data stack, as shown in Figure 8-8.
  - The output is the number of the 32-bit stack.

LBP

The texture information about a partial region of an image is extracted in LBP partial binary mode.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input data format:
  - The input is the 8-bit single component data.
  - The output is the 8-bit single component destination data, as shown in Figure 8-4.

NormGrad

The normalized gradient is calculated, and the gradient components are normalized to 8-bit data.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 8-4.
  - When out_fmt is set to 0x00, 0x01, or 0x02, the output is the 8-bit single component data, as shown in Figure 8-4. When out_fmt is set to 0x03, the output is the 16-bit interleaving data of H and V, as shown in Figure 8-12.

LKOpticalFlow

The LK optical flow motion estimation is implemented. The multi-layer pyramid input is supported, the number of layers is configurable (1−4), and at most 500 corners are supported.

- Resolution: at least 64 x 64 and at most 1920 x 1080 for the pyramid image at each layer
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single-component single-/multi-layer pyramid image of the previous frame. The image at each layer is shown in Figure 8-4.
  - The input is the 8-bit single-component single-/multi-layer pyramid image of the current frame. The image at each layer is shown in Figure 8-4.
  - The input is the corner coordinates of the previous frame. Each coordinate is represented by two 32-bit data segments, which indicate the horizontal coordinate and vertical coordinate respectively. The valid bits are bit[21:0].
  - The corner coordinates of the current frame can serve as the input (only when the initial optical flow is used) and the output.
  - The output mode is configurable. The value 0 indicates that only the corner coordinates of the current frame are output; the value 1 indicates that the coordinates and tracing status information of the corner for the current frame are output; the value 2 indicates that the coordinates, tracing status information, and tracing result residual estimation information of the corner for the current frame are output.

STBoxFltAndEigCalc

The box filtering is implemented during the Shi-Tomasi-like corner calculation, and the response value and maximum response value of the corner are calculated.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input data and output data format:
  - The input is the vertical and horizontal 16-bit interleaving data, as shown in Figure 8-12.
  - The output is the 16-bit single component data, as shown in Figure 8-7.
  - The output is a 16-bit maxEig.

STCandiCorner

The corners are filtered from the Shi-Tomasi-like candidate corners.

- Resolution: 64 x 64 to 1920 x 1080. The resolution of the inputted two images should be the same.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image.
  - The output is the 8-bit single component image, as shown in Figure 8-4.

GradFg

The gradient foreground image data is calculated based on the gradient information of the background image and the current frame image.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the background differential foreground images, as shown in Figure 8-4.
  - The input is the current gradient interleaving images.
  - The input is the background gradient interleaving images, as shown in Figure 8-12.
  - The output is gradient foreground images, as shown in Figure 8-4.

MatchBgModel

The background model matching based on the code book is implemented.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output data formats:
  - The input is an 8-bit single component current gray image.
  - The input is the foreground status flag (8-bit single component), as shown in Figure 8-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is the frame differential images (8-bit single component)
  - The output is the forehead status flag (8-bit single component), as shown in Figure 8-4.
  - The output is the 24-byte model data.
  - The output is a 64-bit statistic value.

UpdateBgModel

The background model update based on the code book is implemented.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the stride of each output component must be the same.
- Input and output data formats:
  - The input is the foreground status flag (8-bit single component), as shown in Figure 8-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is a background gray image (8-bit single component)
  - The output is a gray image in the change state (8-bit single component)
  - The output is a foreground image in the change state (8-bit single component), as shown in Figure 8-4.

- The output is the pixel life period in the change state (16-bit single component), as shown in Figure 8-7.
- The output is the 24-byte model data.
- The output is a 64-bit statistic value.

ANN_MLP_Predict

The ANN_MLP prediction of a single feature sample is implemented. At most six hidden layers and 64 sample vector inputs are supported. The maximum number of supported neurons is 1024 for the input layer and 256 for each of the remaining layers.

- Address alignment mode: Input and output addresses must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 32-bit eigenvector data for the input layer, as shown in Figure 8-8.
  - The input is the 8-bit model data, as shown in Figure 8-4.
  - The input is the 16-bit lookup table data, as shown in Figure 8-7.
  - The output is the 32-bit output layer data, as shown in Figure 8-8.

SVM_Predict

The SVM prediction of a single feature sample is implemented. At most 1024-dimension input vectors are supported.

- Address alignment mode: Input and output addresses must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 32-bit eigenvector data, as shown in Figure 8-8.
  - The input is the 8-bit supporting component, as shown in Figure 8-4.
  - The input is the 16-bit lookup table data, as shown in Figure 8-7.
  - The input is the 8-bit decision function, as shown in Figure 8-4.
  - The output is the 16-bit prediction vote result component, as shown in Figure 8-7.

Resize

Bilinear interpolation scaling and area interpolation scaling are implemented. At most 64 picture inputs are supported. The horizontal/vertical scaling ratio (a multiple) is 1−16. However, the horizontal scaling ratio and the vertical scaling ratio cannot be 1 at the same time.

- Resolution: 32 x 12 to 1920 x 1080
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single-component image or RGB planar image, as shown in Figure 8-4 and Figure 8-6.
  - The output is the scaled image, the format of which is the same as that of the input image.
- Scaling mode: The scaling mode for images in one task must be the same.

GMM2

The GMM background modeling is implemented. The input can be the gray scale image or RGB package image. The number of Gaussian models can be 1−5.

- Resolution: 64 x 64 to 1280 x 720
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single-component image or RGB package image, as shown in Figure 8-4z and Figure 8-5.
  - The input is the 16-bit pixel factor image. The upper eight bits of the pixel factor are the update duration and the lower eight bits are the sensitivity information, as shown in Figure 8-7.
  - The input is the model data.
  - The output is the 8-bit single-component foreground binary image, as shown in Figure 8-4.
  - The output is the updated model data.
  - The output is the background image, the type of which is the same as that of the input image.
  - The output is the 8-bit model hitting information, as shown in Figure 8-4. The lower one bit indicates whether the model is hit or not, and the upper seven bits indicate the index of the hitting model.

CNN

The array image processing is supported. At most 64 image blocks can be input for each operation.

- Resolution: The value range of the width is 16−80, and the value range of the height is [16, 1280/width].
- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit image data or RGB planar image data, as shown in Figure 8-4 and Figure 8-6 respectively. The type and resolution of images in the array must be the same as those of the model.
  - The input is the model data.
  - The output is N eigenvectors with at most 1024 dimensions. N is the number of input images. The eigenvectors serve as the inputs of CNN fully-connected layer.

SAD

This function calculates the accumulated sum of the absolute pixel differences corresponding to two images by block.

- The resolution ranges from 64 x 64 to 1920 x 1080. The width and height of the image must be an integral multiple of the block size.
- Address alignment mode: The input and output addresses and strides must be byte-aligned.
- Input and output data formats:

- The inputs are two 8-bit single-component images with the same resolution, as shown in Figure 8-4.
- The results of output depend on the configured value of out_fmt:

  In multiplexed 16-bit SAD output mode, the 16-bit SAD image is output based on the specified block size and the 8-bit SAD binary image after thresh processing is output, as shown in Figure 8-7 and Figure 8-4 respectively.

  In multiplexed 8-bit SAD output mode, the 8-bit SAD image is output based on the specified block size and the 8-bit SAD binary image after thresh processing is output, as shown in Figure 8-4.

  In single 16-bit SAD output mode, the 16-bit SAD image is output based on the specified block size, as shown in Figure 8-7.

  In single 8-bit SAD output mode, the 8-bit SAD image is output based on the specified block size, as shown in Figure 8-4.

  In single binary image SAD output mode, the 8-bit SAD binary image after thresh processing is output based on the specified block size, as shown in Figure 8-4.

8.1.4 Register Summary

Table 8-1 describes IVE registers.

Table 8-1 Summary of IVE registers (base address: 0x1104_0000)

Offset Address	Register	Description
0x0000	IVE_START	IVE start configuration register
0x0004	INT_EN	IVE interrupt enable register
0x0008	INT_RW	IVE clear interrupt register
0x000C	INT_STATUS	IVE interrupt status register
0x0010	LIST_POINTER	Linked list start address register
0x0014	IVE_STATUS	IVE working status register
0x0018	IVE_TASK_ID	ID register for the tasks processed by the IVE at the previous time
0x0030	NODE_CLK_VALUE	Register for the number of cycles consumed by the preceding node
0x0034	CLK_GT_EN	Clock gating of the IVE internal module
0x0040	NODE_DONE_CNT	Register for the number of processed nodes
0x0044	LIST_DONE_CNT	Register for the number of processed linked lists
0x0054	AXI_INFO	Read and write outstanding number register
0x0060	IVE_OVER_TIME_THR	Overtime interrupt threshold register
0x0064	IVE_OVER_TIME_CNT	Register for the dynamic counting number of the operator working cycle

Offset Address	Register	Description
0x0068	CHAIN_STAT_CLK_VALUE	Register for the number of cycles consumed by the preceding linked list
0x006C	CHAIN_CYCLE_CNT	Register for the counting number of the current linked list cycles

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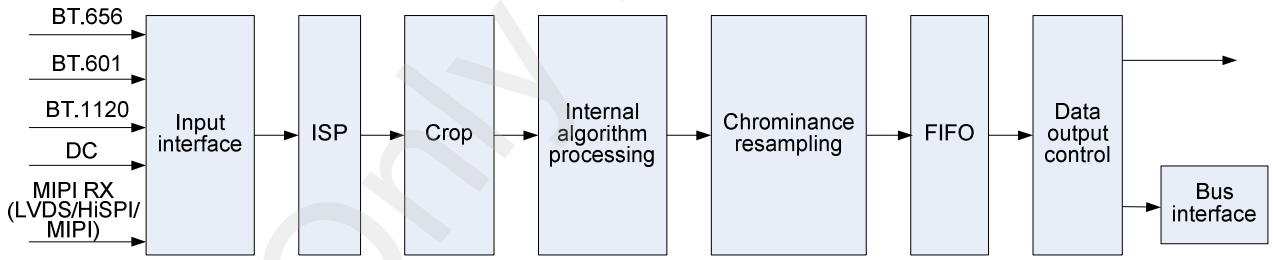
9 Video Interfaces

9.1 VICAP

9.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface, BT.601 interface, BT.1120 interface, digital camera (DC) interface, or mobile industry processor interface receiver (MIPI RX), and stores the data in the specified addresses of the memory or transmits the data to the video processing subsystem (VPSS). Note that the MIPI RX includes the MIPI, low-voltage differential signal (LVDS), and high-speed serial pixel interface (HiSPI). The VICAP module has a built-in image signal processor (ISP) that can directly receive external raw data (Bayer RGB data). Figure 9-1 shows the functional block diagram of the VICAP module.

Figure 9-1 Functional block diagram of the VICAP module



9.1.2 Features

The VICAP module has the following features:

- Maximum input resolution of 4608 x 3456
- One external interface with maximum 16-bit width
- One internal interface and 1-channel video processing in interlaced or progressive input mode
- BT.656, BT.601, BT.1120, DC, MIPI, LVDS, and HiSPI timings
- SMPTE293M or ITU-R BT.1358 timing (480p/576p)
- Flash trigger

- Shutter trigger
- Sensor master/slave mode
- Built-in ISP
- Data obtained in a specified window
- Data output to the DDR in offline mode or to the VPSS in online mode
- Output storage modes
  - SPYCbCr 4:2:2 mode
  - SPYCbCr 4:2:0 mode

9.1.3 Function Description

9.1.3.1 Typical Applications

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR or transmits data to the VPSS online. By using different function modes configured by the system, the VICAP module can be connected to different external VI interfaces, supporting multiple external input devices.

The VICAP module has 23 pins, one clock, two external sync signals (multiplexed with other pins), 16 data lines, one shutter trigger signal (multiplexed with other pins), one camera flash trigger signal (multiplexed with other pins), and two pins that output the sensor slave-mode timing.

It has one port and one channel. The port parses the timings of an interconnected chip, and the channel processes one video signal.

The VICAP module supports the following typical inputs:

- 1-channel 8-megapixel
- 1-channel 2-megapixel

9.1.3.2 Function Implementation

ITU-R BT.656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of the active line data respectively. In video data streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 9-1 shows the format of the ITU-R BT.656 line data.

Table 9-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				**Line Blanking Region**					**Timing Reference Code**				**YCbCr 4:2:2 with 720 Active Pixels**						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between the SAV and EAV depends on the special bit H. Both the SAV and EAV include the vertical blanking bit V and field indicator bit F. For details about the SAV and EAV, see Table 9-2.

Table 9-2 Formats of the SAV and EAV

Bit[7]	Bit[6] (F)	Bit[5] (V)	Bit[4] (H)	Bit[3:0] (P3–P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits can be used to correct 1-bit error and detect 2-bit errors. Table 9-3 describes the valid SAV and EAV values.

Table 9-3 Valid SAV and EAV values

Encoding	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	N/A
EAV	10011101	1	N/A
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	N/A
EAV	11011010	2	N/A
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits (P0, P1, P2, and P3) provide the error correction function. They are determined by the F, V, and H bits. See Table 9-4.

Table 9-4 ITU-R BT.656 error-correcting codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0

F	V	H	P3	P2	P1	P0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

P0 = F^V^H

P1 = F^V

P2 = F^H

P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 9-2 shows the vertical timing of the 525-line 60 field/s video system, and Figure 9-3 shows the vertical timing of the 625-line 50 field/s video system.

Figure 9-2 Vertical timing of the 525-line 60 field/s video system

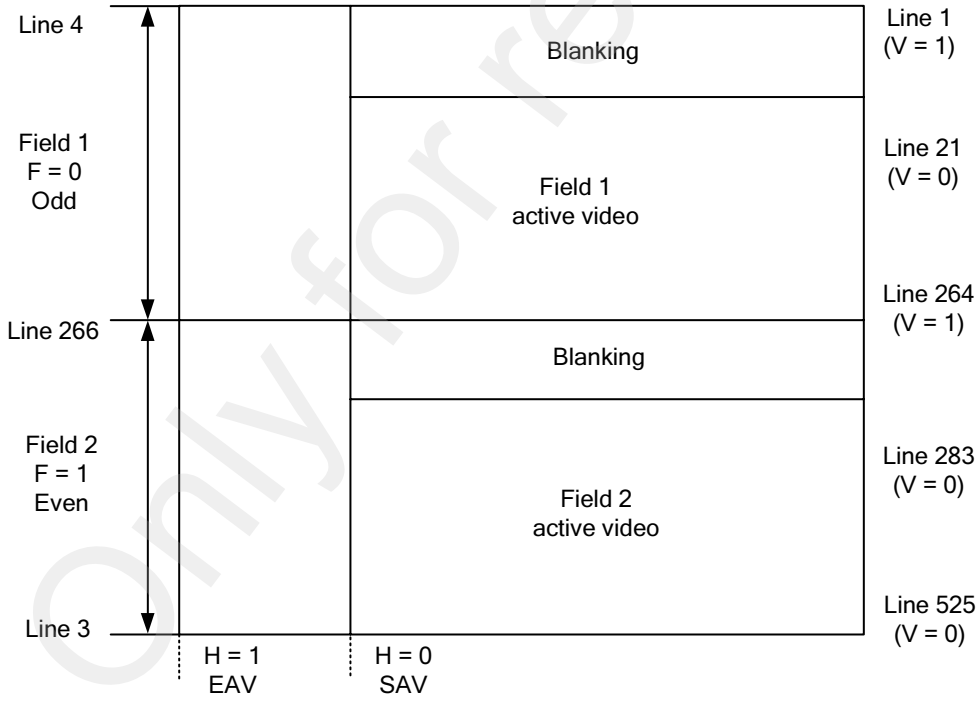
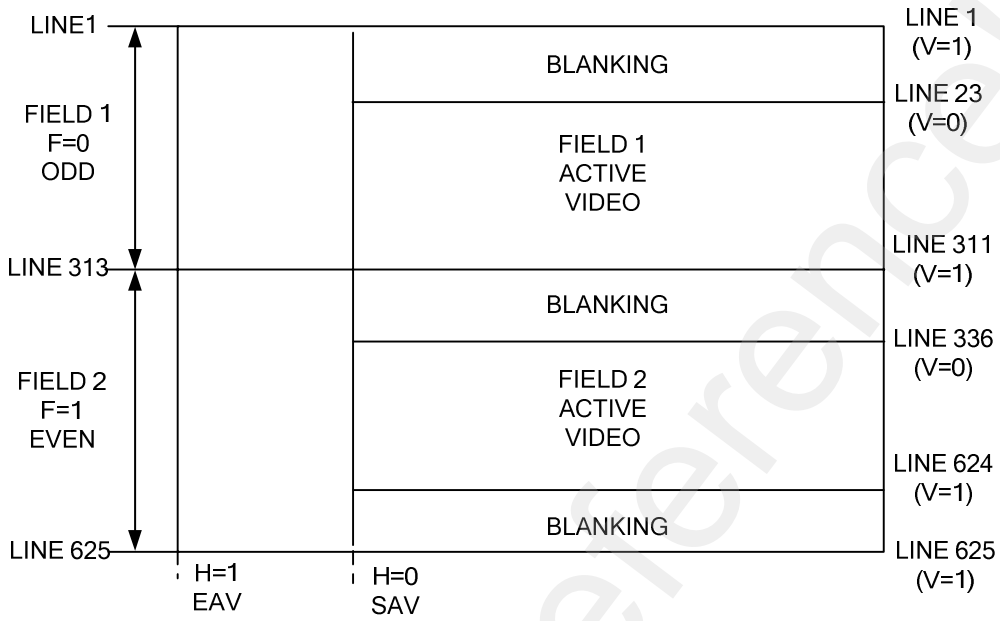


Figure 9-3 Vertical timing of the 625-line 50 field/s video system



NOTE

The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

BT.1120 (HD) Interface Timings

The VICAP module supports the HD interface timings with separated Y/C inputs. In this case, two data ports are required. One is used to transfer luminance and the other one is used to transfer chrominance, as shown in Figure 9-4 and Figure 9-5.

Figure 9-4 Horizontal input timing of the HD interface

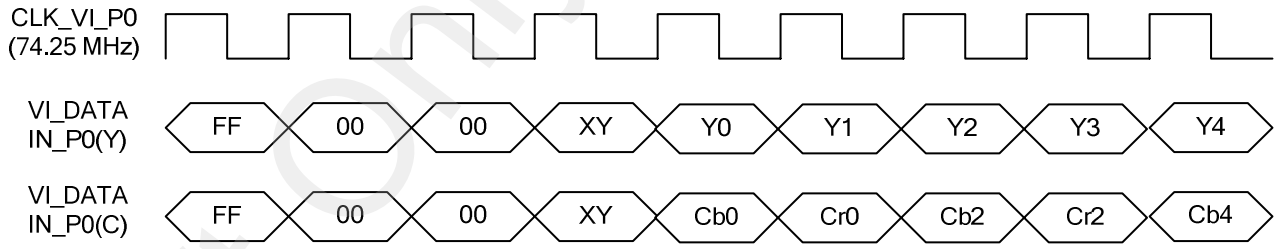
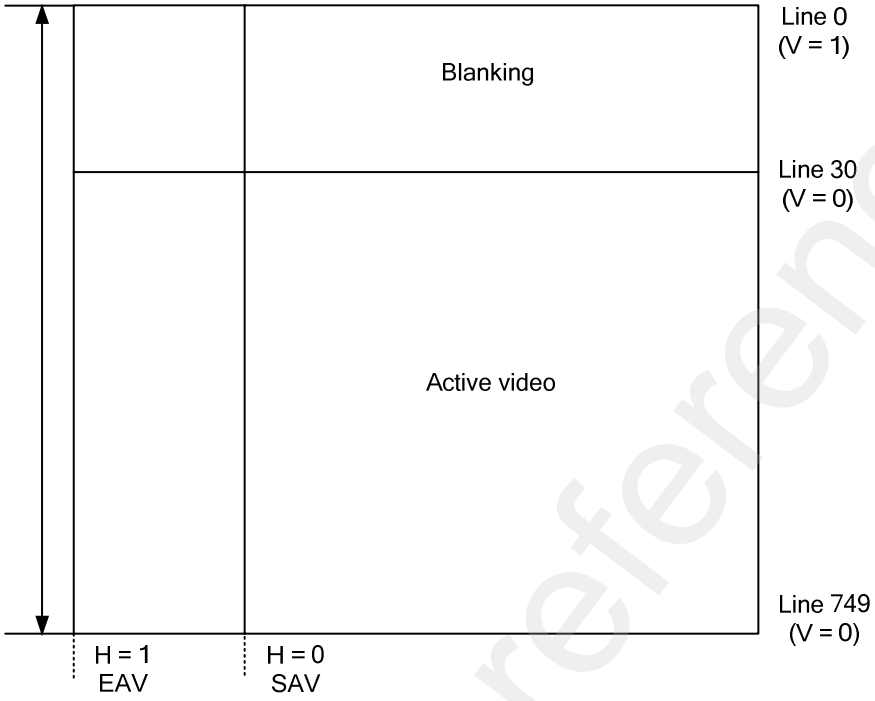


Figure 9-5 Vertical input timing of the HD interface

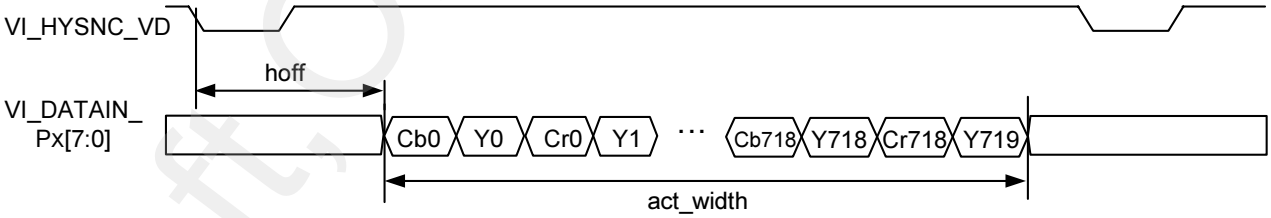


ITU-R BT.601 YCbCr4:2:2

1. Horizontal timing

The horizontal pulse indicates the start of a new line, as shown in Figure 9-6. After hoff clock cycles, an input signal passes the line front blanking region and enters the line active data region. The value of hoff is 244 in the NTSC 525-line system or 264 in the PAL 625-line system. After act_width clock cycles, the input signal passes the line active data region and enters the line back blanking region. The value of act_width can be configured, and the typical value is 720 or 704. In addition, the horizontal sync (HS) polarity is configurable.

Figure 9-6 ITU-R BT.601 horizontal timing



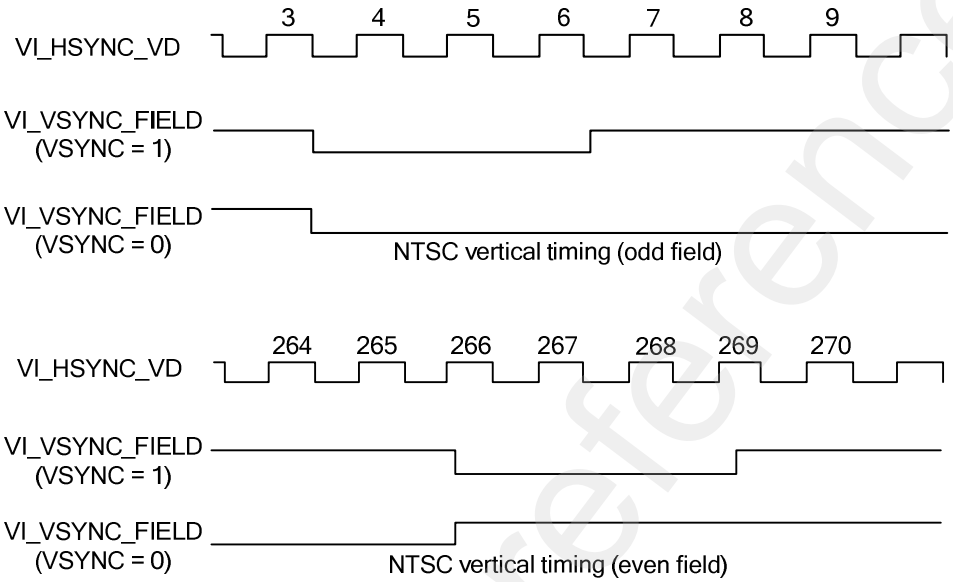
2. Vertical timings

Based on the ITU-R BT.601 recommendation, the signals VSYNC and FIELD are vertical sync (VS) signals. The VSYNC pulse or FIELD transition indicates the start of the odd field or even field. The VICAP module supports two vertical synchronization methods.

Figure 9-7 shows VI VS timings in the NTSC standard (525 lines), and Figure 9-8 shows VI VS timings in the PAL standard (625 lines). VI_HSYNC_VD indicates the HS pulse, and

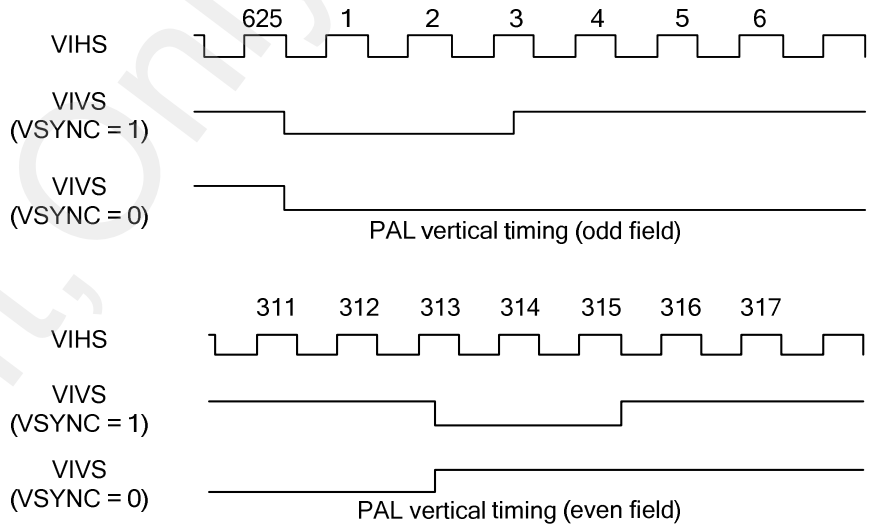
VI_VSYNC_FIELD indicates the VS pulse when VSYNC is 1 or field sync signal when VSYNC is 0.

Figure 9-7 VS timings in the NTSC standard



In NTSC interlaced scanning mode, the level of the VS signal in field 1 becomes low in the start position of line 4, retains low for three consecutive lines, and then becomes high in the start position of line 7. The VICAP module receives 240-line data from line 22 to line 261. The level of the VS signal in field 2 becomes low in the middle of line 266, retains low for three consecutive lines, and then becomes high in the middle of line 269. The VICAP module receives 240-line data from line 285 to line 524.

Figure 9-8 VS timings in the PAL standard



In PAL interlaced scanning mode, the level of the VS signal in field 1 becomes low in the start position of line 1, retains low for 2.5 consecutive lines, and then becomes high in the middle of line 3. The VICAP module receives 288-line data from line 24 to line 310. The level of the VS signal in field 2 becomes low in the middle of line 313, retains low for 2.5 consecutive lines, and then becomes high in the start position of line 316. The VICAP module receives 288-line data from line 336 to line 623.

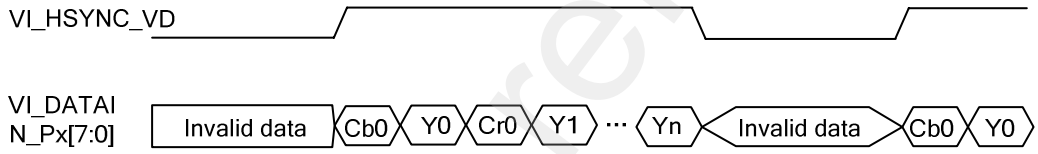
The preceding timings are typical BT.601 vertical timings. The number of lines from the start of the field to the active line, the number of field active lines, and VS polarity can be configured.

DC Interface Timings

1. Horizontal timing

When a DC is connected to the VICAP module, VI_HSYNC_VD is the data valid signal. The polarity of this signal is configurable. Figure 9-9 shows the DC horizontal timing.

Figure 9-9 DC horizontal timing



2. Vertical timing

The VICAP module supports the vertical pulse timing and vertical line active timing, as shown in Figure 9-10 and Figure 9-11. The VS polarity is configurable.

Figure 9-10 DC vertical pulse timing

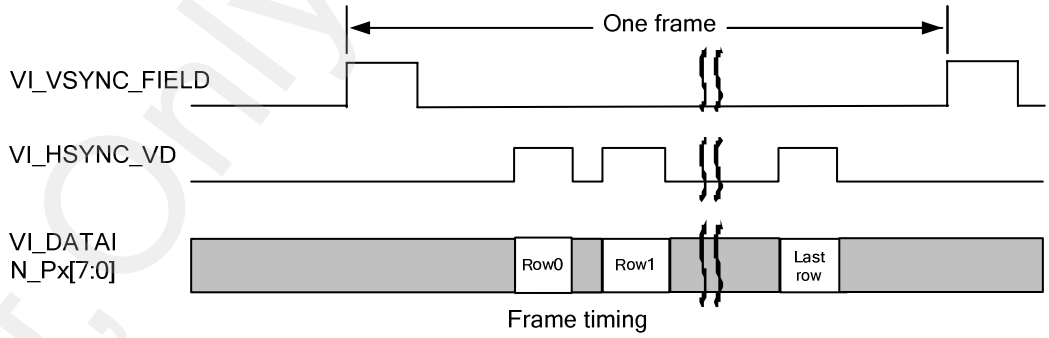
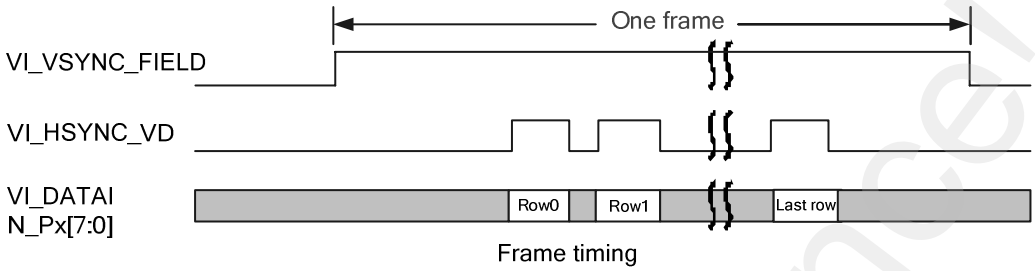


Figure 9-11 DC vertical line active timing

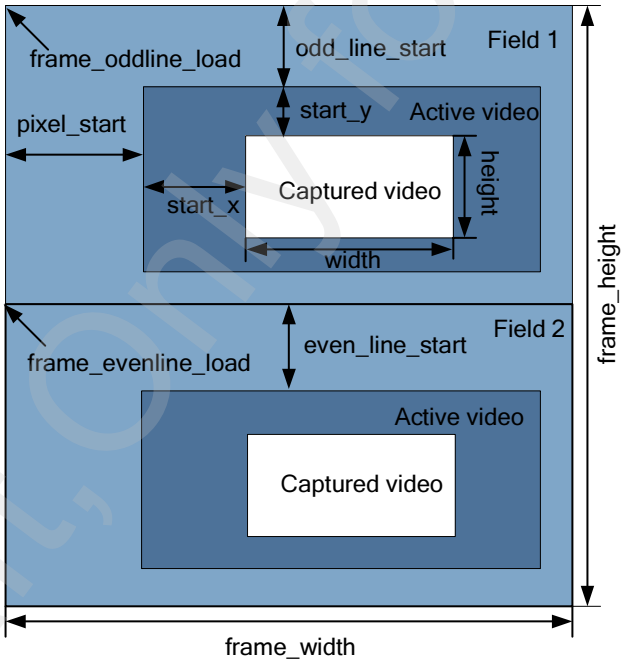


The preceding two timings are the same from the aspect of internal processing of the VICAP module. To be specific, the VICAP module considers the start of a frame after it detects a rising edge or a falling edge, and then detects the data active signal to check whether the current data is active.

9.1.3.3 Image Cropping

As shown in Figure 9-12, an active video starts from the end of the horizontal blanking region and vertical blanking region. The actual view range, however, is within the active video range. That is, compared with the boundary of the active video, the boundary of the actual view is shrunk, which avoids the boundary effect.

Figure 9-12 Relationship between the active video area and the horizontal/vertical blanking regions



9.1.3.4 Image Storage Modes

The supported image storage modes include:

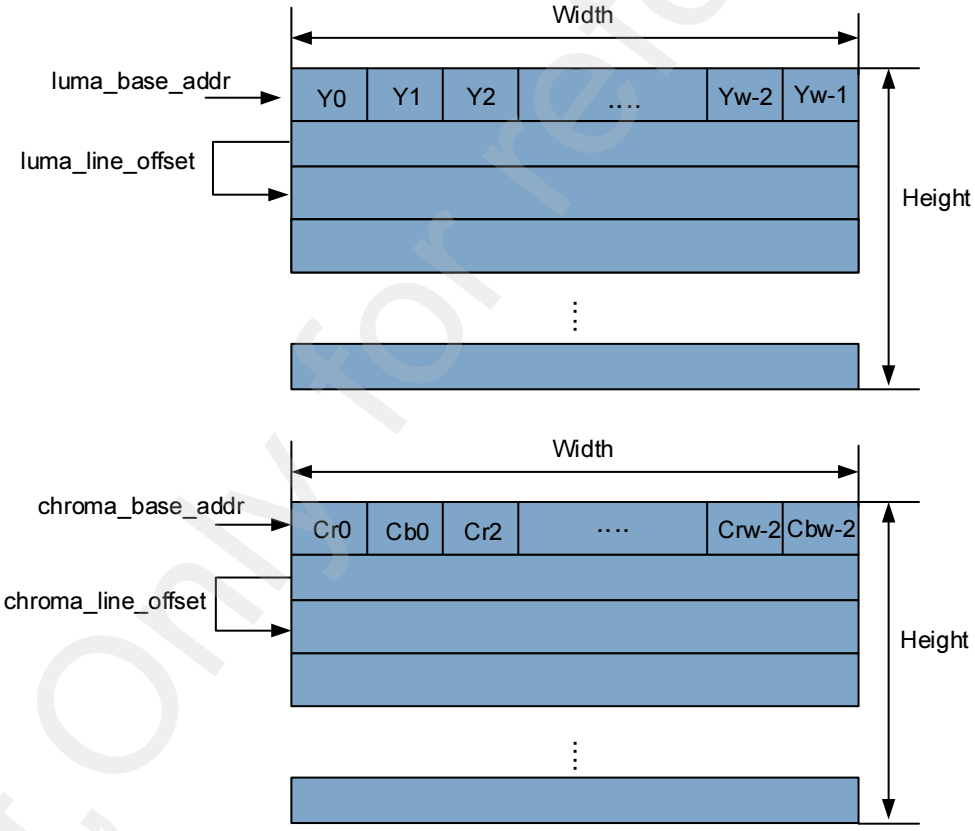
1. YUV data storage

- Semi-planar YCbCr storage mode

  After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.
- For one line, the luminance component and chrominance component are stored separately and consecutively.
- For two consecutive lines, data is stored based on the **offset** parameter that defines the storage stride between the beginnings of two lines.
- The storage positions of the luminance component and chrominance component in the DDR are specified by the start address **base_addr**.

Figure 9-13 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

Figure 9-13 YCbCr4:2:2 storage mode

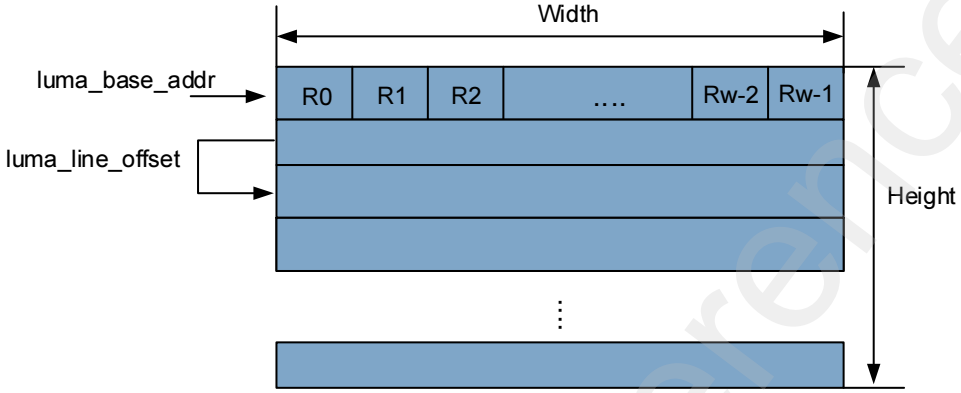


2. Raw data storage

- The raw data is stored in single-component mode.
- The raw data is consecutively stored in one line.
- For two consecutive lines, data is stored based on the **offset** parameter that defines the storage stride between the beginnings of two lines.
- The storage positions of the luminance component and chrominance component in the DDR are specified by the start address **base_addr**.

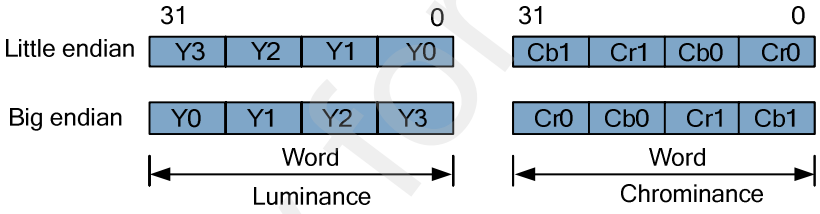
Figure 9-14 shows the mode of storing the raw data captured by the VICAP module.

Figure 9-14 Raw data storage mode



In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word in big-endian mode or little-endian mode. Figure 9-15 shows the big-endian and little-endian storage modes of the luminance and chrominance components.

Figure 9-15 Big-endian and little-endian storage modes



The VICAP module supports only the DDR that stores data in little-endian mode.

9.1.4 Operating Mode

9.1.4.1 reg_newer Function

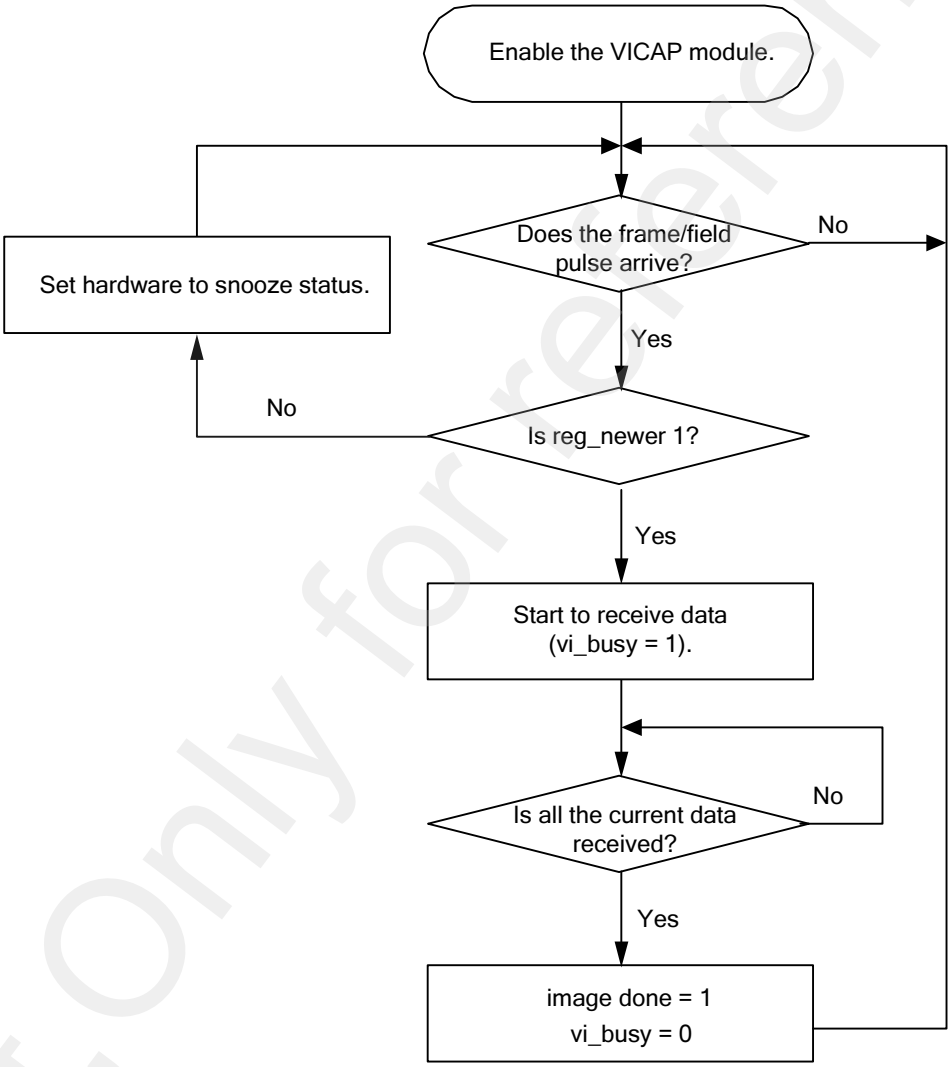
- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configures the VICAP attribute register.
  - Writes 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts receiving data, generates the register update interrupt (reg_update_int), and sets the hardware to busy state.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:

- If reg_newer is 0, the VICAP module does not receive the data of the next field or frame.
- If reg_newer is 1, the VICAP module receives the data of the next field or frame.

9.1.4.2 VICAP Hardware Workflow

Figure 9-16 shows the VICAP hardware workflow.

Figure 9-16 VICAP hardware workflow

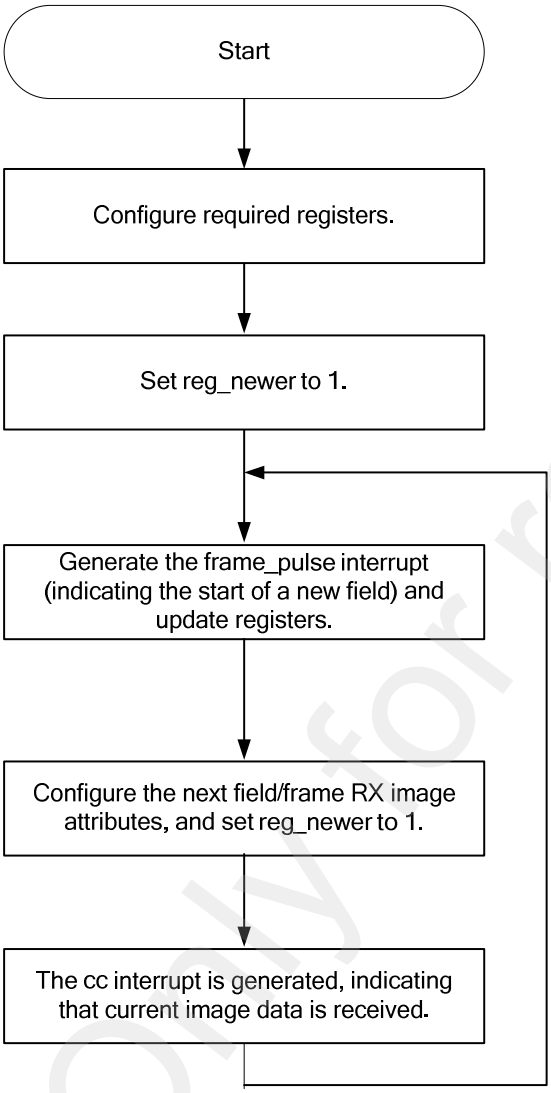


Each time after the VICAP module receives the data of a field or frame, it checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, software has updated or checked corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer is 1 and a new field or frame arrives.

9.1.4.3 Software Configuration Workflow

Figure 9-17 shows the software configuration process in interrupt mode.

Figure 9-17 Software Configuration



When the BT.656, BT.1120, MIPI Rx, or DC interface is used, timing registers do not need to be configured. If the BT.601 interface is used, timing registers including VS registers and HS registers need to be configured.

9.1.5 Register Summary

Table 9-5 describes VICAP registers.

Table 9-5 Summary of VICAP registers (base address: 0x1138_0000)

Offset Address	Register	Description	Page
0x0000	WK_MODE	Global operating mode configuration register	9-19
0x0010	AXI_CFG	Bus configuration register	9-19
0x0014	MAC_CFG	MAC configuration register	9-20
0x0030	CH_SEL	Channel input data selection register	9-21
0x0040	DES_SEL	DES input data selection register	9-21
0x0050	ISP_SEL	ISP input data selection register	9-22
0x0060	CHN_MODE	Bus read/write rate control mode register	9-23
0x0070	BUF_MODE	LINE_BUF input data selection register	9-24
0x00A0	SLAVE_MODE_CFG	Sensor slave mode configuration register	9-25
0x00B0	SLAVE_MODE_VS_TIME	VS output period configuration register in sensor slave mode	9-26
0x00B4	SLAVE_MODE_HS_TIME	HS output period configuration register in sensor slave mode	9-26
0x00B8	SLAVE_MODE_VS_CYC	VS output pulse validity signal duration configuration register in sensor slave mode	9-26
0x00BC	SLAVE_MODE_HS_CYC	HS output pulse validity signal duration configuration register in sensor slave mode	9-27
0x00E0	APB_TIMEOUT	APB timeout register	9-27
0x00F0	VICAP_INT	Interrupt indicator register	9-28
0x00F8	VICAP_INT_MASK	Interrupt mask register	9-29
0x0100	PT_INTF_MOD	Port mode register	9-30
0x0110	PT_OFFSET0	Component 0 offset register	9-31
0x0114	PT_OFFSET1	Component 1 offset register	9-31
0x0118	PT_OFFSET2	Component 2 offset register	9-32
0x0120	PT_BT656_CFG	BT.656 configuration register	9-32
0x0130	PT_UNIFY_TIMING_CFG	Timing configuration register	9-34

Offset Address	Register	Description	Page
0x0134	PT_GEN_TIMING_CFG	Timing recovery module configuration register	9-35
0x0140	PT_UNIFY_DATA_CFG	Data configuration register	9-36
0x0144	PT_GEN_DATA_CFG	Data generation module configuration register	9-37
0x0148	PT_GEN_DATA_COEF	Data generation module coefficient register	9-39
0x014C	PT_GEN_DATA_INIT	Data generation module initial value configuration register	9-39
0x0150	PT_YUV444_CFG	YUV444 configuration register	9-40
0x0160	PT_FSTART_DLY	Port fstart interrupt delay register	9-40
0x0180	PT_INTF_HFB	Horizontal front blanking width register	9-40
0x0184	PT_INTF_HACT	Horizontal active width register	9-41
0x0188	PT_INTF_HBB	Horizontal back blanking width register	9-41
0x018C	PT_INTF_VFB	Vertical front blanking width register	9-42
0x0190	PT_INTF_VACT	Vertical active width register	9-42
0x0194	PT_INTF_VBB	Vertical back blanking width register	9-42
0x0198	PT_INTF_VBFB	Vertical bottom front blanking width register	9-43
0x019C	PT_INTF_VBACT	Vertical bottom active width register	9-43
0x01A0	PT_INTF_VBBB	Vertical bottom back blanking width register	9-43
0x01A4	PT_ID_CFG	ID configuration register	9-44
0x01B0	PT_FLASH_CFG	Flash configuration register	9-45
0x01C0	PT_FLASH_CYC0	Flash timing 0 width register	9-46
0x01C4	PT_FLASH_CYC1	Flash timing 1 width register	9-46
0x01D0	PT_SHUTTER_CYC0	Shutter timing 0 width register	9-46

Offset Address	Register	Description	Page
0x01D4	PT_SHUTTER_CYC1	Shutter timing 1 width register	9-47
0x01D8	PT_SHUTTER_CYC2	Shutter timing 2 width register	9-47
0x01DC	PT_SHUTTER_CYC3	Shutter timing 3 width register	9-47
0x01E0	PT_STATUS	Port status register	9-48
0x01E4	PT_BT656_STATUS	BT.656 status register	9-48
0x01EC	PT_SIZE	Input image size register	9-49
0x01F0	PT_INT	Port interrupt indicator register	9-49
0x01F8	PT_INT_MASK	Port interrupt mask register	9-50
0x0200	DES_CTRL	DES control register	9-51
0x0204	DES_REG_NEWER	Capture control register	9-51
0x0210	DES_ID_CFG	DES RX ID selection register	9-52
0x0220	DES_CROP_CFG	Crop enable register	9-52
0x0230	DES_CROP0_START	Crop start position register for region 0	9-53
0x0234	DES_CROP0_SIZE	Crop size configuration register for region 0	9-53
0x0270	DES_CFG	DES configuration register	9-54
0x0284	DES_SIZE	DES storage size register	9-55
0x0290	DES_FADDR	DES storage base address register	9-55
0x0294	DES_STRIDE	DES storage line stride register	9-55
0x029C	DES_BUF_CFG	DES bus buffer control register	9-56
0x02F0	DES_INT	DES raw interrupt register	9-56
0x02F8	DES_MASK	DES interrupt mask register	9-57
0x0500	LINE_BUF_CFG	LINE_BUF control register	9-58
0x0504	LINE_BUF_REG_NEWER	LINE_BUF update register	9-58
0x0510	LINE_BUF_ID_CFG	LINE_BUF RX ID selection register	9-59
0x0514	LINE_BUF_ADAPTER_CFG	Timing adaptation register	9-59

Offset Address	Register	Description	Page
0x0520	LINE_BUF_CROP_CFG	Crop enable register	9-60
0x0530	LINE_BUF_CROP0_START	Crop start position register for region 0	9-60
0x0534	LINE_BUF_CROP0_SIZE	Crop size configuration register for region 0	9-61
0x0550	LINE_BUF_WIDTH	LINE_BUF image width register	9-61
0x0554	LINE_BUF_HEIGHT	LINE_BUF image height register	9-62
0x05F0	LINE_BUF_INT	LINE_BUF raw interrupt register	9-62
0x05F8	LINE_BUF_MASK	LINE_BUF interrupt mask register	9-63
0x0600	SRC_CTRL	SRC control register	9-64
0x0604	SRC_REG_NEWER	Capture control register	9-65
0x0670	SRC_CFG	SRC configuration register	9-66
0x0684	SRC_SIZE	SRC storage size register	9-66
0x0690	SRC_FADDR	SRC storage base address register	9-67
0x0694	SRC_STRIDE	SRC storage line stride register	9-67
0x069C	SRC_BUF_CFG	SRC bus buffer control register	9-68
0x06F0	SRC_INT	SRC raw interrupt register	9-68
0x06F8	SRC_MASK	SRC interrupt mask register	9-69
0x1000	CH_CTRL	Channel control register	9-70
0x1004	CH_REG_NEWER	Capture control register	9-71
0x1010	CH_ADAPTER_CFG	Timing adaptation register	9-71
0x1034	CH_DLY_CFG	Channel input image start interrupt delay configuration register	9-72
0x1080	CH_WCH_Y_CFG	Y component configuration register for the WCH module	9-72
0x1084	CH_WCH_Y_SIZE	Y component storage size register for the WCH module	9-73
0x1090	CH_WCH_Y_FADDR	Y component storage base address register for the WCH module	9-74

Offset Address	Register	Description	Page
0x1094	CH_WCH_Y_HADDR	Y component header information storage base address register for the WCH module	9-74
0x1098	CH_WCH_Y_STRIDE	Y component line offset register for the WCH module	9-75
0x109C	CH_WCH_Y_BUF_CFG	CH_DES bus buffer control register	9-75
0x10A0	CH_WCH_C_CFG	C component configuration register for the WCH module	9-76
0x10A4	CH_WCH_C_SIZE	C component storage size register for the WCH module	9-77
0x10B0	CH_WCH_C_FADDR	C component storage base address register for the WCH module	9-77
0x10B4	CH_WCH_C_HADDR	C component header information storage base address register for the WCH module	9-78
0x10B8	CH_WCH_C_STRIDE	C component line offset register for the WCH module	9-78
0x10BC	CH_WCH_C_BUF_CFG	CH_DES bus buffer control register	9-78
0x10E8	CH_Y_OUT_SIZE	Channel luminance output size indicator register	9-79
0x10EC	CH_C_OUT_SIZE	Channel chrominance output size indicator register	9-79
0x10F0	CH_INT	Channel raw interrupt register	9-80
0x10F8	CH_INT_MASK	Channel interrupt mask register	9-81
0x1100	CH_Y_CROP_CFG	Luminance crop enable register	9-81
0x1110	CH_Y_CROP0_START	Crop start position register for luminance region 0	9-82
0x1114	CH_Y_CROP0_SIZE	Crop size register for luminance region 0	9-82
0x1120	CH_C_CROP_CFG	Chrominance crop enable register	9-83
0x1130	CH_C_CROP0_START	Crop start position register for chrominance region 0	9-83
0x1134	CH_C_CROP0_SIZE	Crop size register for chrominance region 0	9-84

9.1.6 Register Description

WK_MODE

WK_MODE is a global operating mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_DB58

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ros_mem_ema				rft_mem_emab				rft_mem_emaa				rfs_mem_emaw		rfs_mem_ema				reserved		mem_power_mode	power_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:14]	RW	ros_mem_ema	Speed adjustment configuration for the Q end of the read-only memory
[13:11]	RW	rft_mem_emab	Speed adjustment configuration for the D end of the dual-port memory
[10:8]	RW	rft_mem_emaa	Speed adjustment configuration for the Q end of the dual-port memory
[7:6]	RW	rfs_mem_emaw	Speed adjustment configuration for the D end of the single-port memory
[5:3]	RW	rfs_mem_ema	Speed adjustment configuration for the Q end of the single-port memory
[2]	RO	reserved	Reserved
[1]	RW	mem_power_mode	Memory idle power-off mode enable 0: disabled 1: enabled
[0]	RW	power_mode	Clock mode 0: The low-power mode is disabled. 1: The low-power mode is enabled.

AXI_CFG

AXI_CFG is a bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																r_outstanding				reserved				w_outstanding				reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:12]	RW	r_outstanding	Number of read request outstandings Value range: [1, 16]
[11:9]	RO	reserved	Reserved
[8:4]	RW	w_outstanding	Number of write request outstandings Value range: [1, 8]
[3:0]	RO	reserved	Reserved

MAC_CFG

MAC_CFG is a MAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																r_req_prio								w_req_prio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	r_req_prio	Read request arbitration priority 0: low priority 1: high priority bit[8]: SRC0 read request priority bit[9]: SRC1 read request priority bit[10]: SRC2 read request priority bit[11]: SRC3 read request priority bit[12]: reserved bit[13]: reserved bit[14]: reserved bit[15]: reserved

[7:0]	RW	w_req_prio	Write request arbitration priority 0: low priority 1: high priority bit[0]: DES0 write request priority bit[1]: DES1 write request priority bit[2]: DES2 write request priority bit[3]: WCH_Y write request priority bit[4]: WCH_C write request priority bit[5]: reserved bit[6]: reserved bit[7]: reserved

CH_SEL

CH_SEL is a channel input data selection register.

Offset Address	Register Name	Total Reset Value
0x0030	CH_SEL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							ch_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	ch_sel	Channel input data select 000: The channel connects to ISP_BE. 001: The channel connects to PT (for debugging). 010: The channel connects to LINE_BUF (for debugging). 011: The channel connects to ISP_FE (for debugging). Other values: reserved

DES_SEL

DES_SEL is a DES input data selection register.

Offset Address	Register Name	Total Reset Value
0x0040	DES_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															des_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	des2_sel	DES2 input data select 000: The DES connects to the port. 001: The DES connects to LINE_BUF. 010: The DES connects to the FPN. 011: The DES connects to the FSP_FE. 100: The DES connects to the IR output. Other values: reserved
[7]	RO	reserved	Reserved
[6:4]	RW	des1_sel	DES1 input data select 000: The DES connects to the port. 001: The DES connects to LINE_BUF. 010: The DES connects to the FPN. 011: The DES connects to the FSP_FE. 100: The DES connects to the IR output. Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	des0_sel	DES0 input data select 000: The DES connects to the port. 001: The DES connects to LINE_BUF. 010: The DES connects to the FPN. 011: The DES connects to the FSP_FE. 100: The DES connects to the IR output. Other values: reserved

ISP_SEL

ISP_SEL is an ISP input data selection register.

Offset Address	Register Name	Total Reset Value
0x0050	ISP_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															af_sel	reserved												reserved			isp_fe_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	af_sel	AF input data select 0: The AF connects to ISP_FE. 1: The AF connects to ISP_BE. Other values: reserved
[15:7]	RO	reserved	Reserved
[6:4]	RW	isp_be_sel	ISP_BE input data select 000: ISP_BE connects to ISP_FE (for the raw input). 001: ISP_BE connects to LINE_BUF (for the YUV input). 011: ISP_BE connects to SRC0 (for debugging). 100: ISP_BE connects to SRC1 (for debugging). 101: ISP_BE connects to SRC2 (for debugging). 110: ISP_BE connects to SRC3 (for debugging). Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	isp_fe_sel	ISP_FE input data select 000: ISP_FE connects to LINE_BUF (for the raw input). 001: ISP_FE connects to SRC0. 010: ISP_FE connects to SRC1. 011: ISP_FE connects to SRC2. 100: ISP_FE connects to SRC3. Other values: reserved

CHN_MODE

CHN_MODE is a bus read/write rate control mode register.

Offset Address	Register Name	Total Reset Value
0x0060	CHN_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										chn2_mode		chn1_mode		chn_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	chn2_mode	SRC2/DES2 bus read/write rate control mode (used when SRC2 shares the buffer with DES2) 00: no rate control 01: The rate of SRC2 is controlled to ensure that it is lower than the DES2 write rate (read after write) 10: The rate of DES2 is controlled to ensure that it is lower than the SRC2 read rate (write after read) 11: reserved
[3:2]	RW	chn1_mode	SRC1/DES1 bus read/write rate control mode (used when SRC1 shares the buffer with DES1) 00: no rate control 01: The rate of SRC1 is controlled to ensure that it is lower than the DES1 write rate (read after write) 10: The rate of DES1 is controlled to ensure that it is lower than the SRC1 read rate (write after read) 11: reserved
[1:0]	RW	chn0_mode	SRC0/DES0 bus read/write rate control mode (used when SRC0 shares the buffer with DES0) 00: no rate control 01: The rate of SRC0 is controlled to ensure that it is lower than the DES0 write rate (read after write) 10: The rate of DES0 is controlled to ensure that it is lower than the SRC0 read rate (write after read) 11: reserved

BUF_MODE

BUF_MODE is a LINE_BUF input data selection register.

Offset Address	Register Name	Total Reset Value
0x0070	BUF_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															buf_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	buf_mode	Input data mode of LINE_BUF 0: raw data 1: YUV422

SLAVE_MODE_CFG

SLAVE_MODE_CFG is a sensor slave mode configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	SLAVE_MODE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vs_enable	hs_enable	reserved												vs_inv	hs_inv	hs_dly_cyc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vs_enable	VS output enable 0: disabled 1: enabled
[30]	RW	hs_enable	HS output enable 0: disabled 1: enabled
[29:18]	RW	reserved	Reserved
[17]	RW	vs_inv	VS output polarity 0: active high 1: active low

[16]	RW	hs_inv	HS output polarity 0: active high 1: active low
[15:0]	RW	hs_dly_cyc	Delay period of the HS output relative to the VS output (unit: cycle)

SLAVE_MODE_VS_TIME

SLAVE_MODE_VS_TIME is a VS output period configuration register in sensor slave mode.

Offset Address	Register Name	Total Reset Value
0x00B0	SLAVE_MODE_VS_TIME	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vs_time																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vs_time	VS output period (unit: cycle)

SLAVE_MODE_HS_TIME

SLAVE_MODE_HS_TIME is an HS output period configuration register in sensor slave mode.

Offset Address	Register Name	Total Reset Value
0x00B4	SLAVE_MODE_HS_TIME	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hs_time																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hs_time	HS output period (unit: cycle)

SLAVE_MODE_VS_CYC

SLAVE_MODE_VS_CYC is a VS output pulse validity signal duration configuration register in sensor slave mode.

Offset Address	Register Name	Total Reset Value
0x00B8	SLAVE_MODE_VS_CYC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vs_cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vs_cyc	Duration of the VS output validity signal (unit: cycle)

SLAVE_MODE_HS_CYC

SLAVE_MODE_HS_CYC is an HS output pulse validity signal duration configuration register in sensor slave mode.

Offset Address	Register Name	Total Reset Value
0x00BC	SLAVE_MODE_HS_CYC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hs_cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hs_cyc	Duration of the HS output validity signal (unit: cycle)

APB_TIMEOUT

APB_TIMEOUT is an APB timeout register.

Offset Address	Register Name	Total Reset Value
0x00E0	APB_TIMEOUT	0x8000_0180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved															timeout															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timeout enable 0: disabled 1: enabled
[30:16]	RO	reserved	Reserved

[15:0]	RW	timeout	Timeout threshold (in APB clock)

VICAP_INT

VICAP_INT is an interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_isp_be	int_isp_fe	reserved						int_buf	int_src3	int_src2	int_src1	int_buf	int_src1	int_des1	int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	int_isp_be	ISP_BE interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	int_isp_fe	ISP_FE interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[15:10]	RO	reserved	Reserved
[9]	RO	int_buf	LINE_BUF interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	int_src3	SRC3 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	int_src2	SRC2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	int_src1	SRC1 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_src0	SRC0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

[4]	RO	int_des2	DES2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_des1	DES1 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_des0	DES0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_ch	Channel interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_pt	Port interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

VICAP_INT_MASK

VICAP_INT_MASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_isp_be	int_isp_fe	reserved						int_buf	int_src3	int_src2	int_src1	int_src0	int_des2	int_des1	int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	int_isp_be	ISP_BE interrupt enable 0: masked 1: enabled
[16]	RW	int_isp_fe	ISP_FE interrupt enable 0: masked 1: enabled
[15:10]	RO	reserved	Reserved

[9]	RW	int_buf	LINE_BUF interrupt enable 0: masked 1: enabled
[8]	RW	int_src3	SRC3 interrupt enable 0: masked 1: enabled
[7]	RW	int_src2	SRC2 interrupt enable 0: masked 1: enabled
[6]	RW	int_src1	SRC1 interrupt enable 0: masked 1: enabled
[5]	RW	int_src0	SRC0 interrupt enable 0: masked 1: enabled
[4]	RW	int_des2	DES2 interrupt enable 0: masked 1: enabled
[3]	RW	int_des1	DES1 interrupt enable 0: masked 1: enabled
[2]	RW	int_des0	DES0 interrupt enable 0: masked 1: enabled
[1]	RW	int_ch	Channel interrupt enable 0: masked 1: enabled
[0]	RW	int_pt	Port interrupt enable 0: masked 1: enabled

PT_INTF_MOD

PT_INTF_MOD is a port mode register.

Offset Address	Register Name	Total Reset Value
0x0100	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Port enable 0: disabled 1: enabled
[30:1]	RO	reserved	Reserved
[0]	RW	mode	Timing mode 0: external sync 1: BT.656

PT_OFFSET0

PT_OFFSET0 is a component 0 offset register.

Offset Address	Register Name	Total Reset Value
0x0110	PT_OFFSET0	0xFFF0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 0 offset

PT_OFFSET1

PT_OFFSET1 is a component 1 offset register.

Offset Address	Register Name	Total Reset Value
0x0114	PT_OFFSET1	0xFFF0_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 1 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 1 offset

PT_OFFSET2

PT_OFFSET2 is a component 2 offset register.

Offset Address	Register Name	Total Reset Value
0x0118	PT_OFFSET2	0xFFF0_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 2 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 2 offset

PT_BT656_CFG

PT_BT656_CFG is a BT.656 configuration register.

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31]	RW	enable	BT.656 enable 0: disabled 1: enabled
[30:11]	RO	reserved	Reserved
[10]	RW	field_inv	Reverse control 0: not reversed 1: reversed
[9]	RW	vsync_inv	Reverse control 0: not reversed 1: reversed
[8]	RW	hsync_inv	Reverse control 0: not reversed 1: reversed
[7:4]	RO	reserved	Reserved
[3:0]	RW	mode	Mode select mode[0] 0: hsync is not an active signal. 1: hsync is an active signal. mode[1] 0: The hsync output is active low. 1: The hsync output is active high. mode[3:2] 00: Component 0 is parsed. 01: Component 1 is parsed. 10: Component 2 is parsed. 11: reserved

PT_UNIFY_TIMING_CFG

PT_UNIFY_TIMING_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	field_inv, field_sel	reserved	vsync_mode, vsync_inv, vsync_sel	reserved, hsync_mode, hsync_and	hsync_inv, hsync_sel	reserved	de_inv, de_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	field_inv	Field inverse (level-1 field processing) 0: not inverted 1: inverted
[25:24]	RW	field_sel	Field source select (level-0 field processing) 00: input field 01: input vsync 10: detected based on the relationship between vsync and hsync 11: fixed at 0
[23:21]	RO	reserved	Reserved
[20:19]	RW	vsync_mode	vsync processing mode (level-2 vsync processing) 00: not processed 01: detect the rising edge 10: detect the rising edge and falling edge 11: reserved
[18]	RW	vsync_inv	vsync inversion (level-1 vsync processing) 0: not inverted 1: inverted
[17:16]	RW	vsync_sel	vsync source select (level-0 vsync processing) 00: input vsync 01: input field 10: fixed at 0 11: reserved
[15]	RO	reserved	Reserved

[14:13]	RW	hsync_mode	hsync processing mode (level-3 hsync processing) 0: not processed 1: detect the rising edge
[12:11]	RW	hsync_and	Whether hsync is operated with the result of level-1 vsync processing (level-2 hsync processing) 00: not processed 01: ANDed 10: exclusive ORed 11: reserved
[10]	RW	hsync_inv	hsync inversion (level-1 hsync processing) 0: not inverted 1: inverted
[9:8]	RW	hsync_sel	hsync source select (level-0 hsync processing) 00: input hsync 01: input de 10: fixed at 0 11: reserved
[7:3]	RO	reserved	Reserved
[2]	RW	de_inv	de inversion (level-1 de processing) 0: not inverted 1: inverted
[1:0]	RW	de_sel	de source select (level-0 de processing) 00: input de 01: result of level-2 hsync processing 10: fixed at 1 11: fixed at 0

PT_GEN_TIMING_CFG

PT_GEN_TIMING_CFG is a timing recovery module configuration register.

Offset Address	Register Name	Total Reset Value
0x0134	PT_GEN_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reserved																											vsync_mode	hsync_mode	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timing recovery enable (timings are recovered based on timing parameters) 0: disabled 1: enabled
[30]	RW	mode	Timing recovery mode (timings are recovered based on timing parameters) 0: Timings are generated based on the input valid signal of PT. 1: Timings are internally calculated and generated.
[29:3]	RO	reserved	Reserved
[2]	RW	vsync_mode	vsync recovery 0: not recovered 1: recovered
[1]	RW	hsync_mode	hsync recovery 0: not recovered 1: recovered
[0]	RO	reserved	Reserved

PT_UNIFY_DATA_CFG

PT_UNIFY_DATA_CFG is a data configuration register.

Offset Address	Register Name	Total Reset Value
0x0140	PT_UNIFY_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											uv_seq	yc_seq	comp_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Data separation enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3]	RW	uv_seq	CbCr sequence 0: CbCr 1: CrCb
[2]	RW	yc_seq	YC sequence 0: CY 1: YC
[1:0]	RW	comp_num	Data component select 00: component 1 01: component 2 10: component 3 11: reserved

PT_GEN_DATA_CFG

PT_GEN_DATA_CFG is a data generation module configuration register.

Offset Address	Register Name	Total Reset Value
0x0144	PT_GEN_DATA_CFG	0x0000_00E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							data0_move	data1_move	data2_move	vsync_reset	hsync_reset	vsync_move	hsync_move	de_move
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1

Bits	Access	Name	Description
[31]	RW	enable	Data generation enable. Data is generated based on the data generation parameter. 0: disabled 1: enabled
[30:8]	RO	reserved	Reserved
[7]	RW	data0_move	Whether data 0 increases progressively 0: no 1: yes
[6]	RW	data1_move	Whether data 1 increases progressively 0: no 1: yes
[5]	RW	data2_move	Whether data 2 increases progressively 0: no 1: yes
[4]	RW	vsync_reset	Whether to reset data based on the VS signal 0: not reset 1: reset
[3]	RW	hsync_reset	Whether to reset data based on the HS signal 0: not reset 1: reset
[2]	RW	vsync_move	Whether the VS signal data increases progressively 0: no 1: yes
[1]	RW	hsync_move	Whether the HS signal data increases progressively 0: no 1: yes

[0]	RW	de_move	Whether the de signal data increases progressively 0: no 1: yes

PT_GEN_DATA_COEF

PT_GEN_DATA_COEF is a data generation module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0148	PT_GEN_DATA_COEF	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inc_frame								step_frame								inc_space								step_space							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	inc_frame	Incremental value between data frames. The incremental values are accumulated in the upper eight bits of data.
[23:16]	RW	step_frame	Interval for data frame increment. The configured value is the actual value minus 1. The value 0 indicates the increment by frame.
[15:8]	RW	inc_space	Incremental value between data pixels. The incremental values are accumulated in the upper 10 bits of data.
[7:0]	RW	step_space	Interval for data pixel increment. The value 0 indicates the increment by pixel.

PT_GEN_DATA_INIT

PT_GEN_DATA_INIT is a data generation module initial value configuration register.

Offset Address	Register Name	Total Reset Value
0x014C	PT_GEN_DATA_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								data2								data1								data0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	data2	Initial V/B value
[15:8]	RW	data1	Initial U/G value

[7:0]	RW	data0	Initial Y/R value

PT_YUV444_CFG

PT_YUV444_CFG is a YUV444 configuration register.

Offset Address	Register Name	Total Reset Value
0x0150	PT_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable for converting YUV422 signals into YUV444 signals 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

PT_FSTART_DLY

PT_FSTART_DLY is a port fstart interrupt delay register.

Offset Address	Register Name	Total Reset Value
0x0160	PT_FSTART_DLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fstart_dly																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fstart_dly	fstart interrupt delay time, in the unit of the port clock

PT_INTF_HFB

PT_INTF_HFB is a horizontal front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0180	PT_INTF_HFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hfb	Horizontal front blanking width

PT_INTF_HACT

PT_INTF_HACT is a horizontal active width register.

Offset Address	Register Name	Total Reset Value
0x0184	PT_INTF_HACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hact	Horizontal active width (in clock cycle)

PT_INTF_HBB

PT_INTF_HBB is a horizontal back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0188	PT_INTF_HBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hbb	Horizontal back blanking width

PT_INTF_VFB

PT_INTF_VFB is a vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x018C	PT_INTF_VFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vfb	Vertical front blanking width

PT_INTF_VACT

PT_INTF_VACT is a vertical active width register.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vact	Vertical active width

PT_INTF_VBB

PT_INTF_VBB is a vertical back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0194	PT_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	vbb	Vertical back blanking width

PT_INTF_VBFB

PT_INTF_VBFB is a vertical bottom front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0198	PT_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbfb	Vertical bottom front blanking width

PT_INTF_VBACT

PT_INTF_VBACT is a vertical bottom active width register.

Offset Address	Register Name	Total Reset Value
0x019C	PT_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbact	Vertical bottom active width

PT_INTF_VBBB

PT_INTF_VBBB is a vertical bottom back blanking width register.

Offset Address	Register Name	Total Reset Value
0x01A0	PT_INTF_VBBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbbb	Vertical bottom back blanking width

PT_ID_CFG

PT_ID_CFG is an ID configuration register.

Offset Address	Register Name	Total Reset Value
0x01A4	PT_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reset	reserved																							id_det		id_max		id			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	ID generation enable 0: disabled 1: enabled
[30]	RW	mode	ID generation mode 0: automatic mode (the ID automatically increases for each frame) 1: non-automatic mode (the ID depends on the configured value)
[29]	WO	reset	In automatic mode, setting this field to 1 restores the ID of the next frame to the initial value. This field is automatically cleared after restoration.
[28:6]	RO	reserved	Reserved
[5:4]	RW	id_det	ID of the frame whose width and height are detected
[3:2]	RW	id_max	Maximum ID in automatic mode
[1:0]	RW	id	Initial ID in automatic mode or generated ID in non-automatic mode

PT_FLASH_CFG

PT_FLASH_CFG is a flash configuration register.

Offset Address	Register Name	Total Reset Value
0x01B0	PT_FLASH_CFG	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_sel				reserved									shutter_times	shutter_phase	shutter_en	reserved															flash_phase	flash_en
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	id_sel	Trigger frame ID 0x1: triggered by using the start interrupt of the frame whose ID is 0 0x2: triggered by using the start interrupt of the frame whose ID is 1 0x4: triggered by using the start interrupt of the frame whose ID is 2 0x8: triggered by using the start interrupt of the frame whose ID is 3
[27:19]	RO	reserved	Reserved
[18]	RW	shutter_times	Shutter pulse times 0: twice 1: once
[17]	RW	shutter_phase	Shutter signal reverse 0: not reversed 1: reversed
[16]	WO	shutter_en	Shutter trigger enable. This field is automatically cleared. 0: disable 1: enable
[15:2]	RO	reserved	Reserved
[1]	RW	flash_phase	Flash signal reverse 0: not reversed 1: reversed
[0]	WO	flash_en	Flash trigger enable. This field is automatically cleared. 0: disable 1: enable

PT_FLASH_CYC0

PT_FLASH_CYC0 is a flash timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01C0	PT_FLASH_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 0 (in PT clock). The configured value is the actual value minus 1.

PT_FLASH_CYC1

PT_FLASH_CYC1 is a flash timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01C4	PT_FLASH_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 1 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC0

PT_SHUTTER_CYC0 is a shutter timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01D0	PT_SHUTTER_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 0 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC1

PT_SHUTTER_CYC1 is a shutter timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01D4	PT_SHUTTER_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 1 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC2

PT_SHUTTER_CYC2 is a shutter timing 2 width register.

Offset Address	Register Name	Total Reset Value
0x01D8	PT_SHUTTER_CYC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 2 (in PT clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC3

PT_SHUTTER_CYC3 is a shutter timing 3 width register.

Offset Address	Register Name	Total Reset Value
0x01DC	PT_SHUTTER_CYC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 3 (in PT clock). The configured value is the actual value minus 1.

PT_STATUS

PT_STATUS is a port status register.

Offset Address	Register Name	Total Reset Value
0x01E0	PT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										id		field	vsync	hsync	de
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RO	id	Port output ID
[3]	RO	field	Field output over the port
[2]	RO	vsync	vsync signal output over the port
[1]	RO	hsync	hsync signal over the port
[0]	RO	de	de signal output over the port

PT_BT656_STATUS

PT_BT656_STATUS is a BT.656 status register.

Offset Address	Register Name	Total Reset Value
0x01E4	PT_BT656_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																seav								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	seav	Synchronization code
[7:0]	RO	reserved	Reserved

PT_SIZE

PT_SIZE is an input image size register.

Offset Address	Register Name	Total Reset Value
0x01EC	PT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Image height
[15:0]	RO	width	Image width

PT_INT

PT_INT is a port interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x01F0	PT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	WC	height_err	Status of the image height change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	width_err	Status of the image width change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

PT_INT_MASK

PT_INT_MASK is a port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	PT_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved

[2]	RW	height_err	Image height change interrupt enable 0: masked 1: enabled
[1]	RW	width_err	Image width change interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Frame/Field start interrupt enable 0: masked 1: enabled

DES_CTRL

DES_CTRL is a DES control register.

Offset Address	Register Name	Total Reset Value
0x0200	DES_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							bit_width							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	DES enable 0: disabled 1: enabled
[30:6]	RO	reserved	Reserved
[5:0]	RW	bit_width	Data width 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

DES_REG_NEWER

DES_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x0204	DES_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_newer	DES update. This bit is automatically cleared for each frame. 0: not updated (frames are discarded) 1: updated

DES_ID_CFG

DES_ID_CFG is a DES RX ID selection register (instant register).

Offset Address	Register Name	Total Reset Value
0x0210	DES_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	id_sel	ID of the data received by the DES 0: Data with this ID is filtered. 1: Data with this ID is received. bit[0]: DES RX enable for data with the ID 0 bit[1]: DES RX enable for data with the ID 1 bit[2]: DES RX enable for data with the ID 2 bit[3]: DES RX enable for data with the ID 3

DES_CROP_CFG

DES_CROP_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x0220	DES_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

DES_CROP0_START

DES_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x0230	DES_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which images start to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which images start to be captured

DES_CROP0_SIZE

DES_CROP0_SIZE is a crop size register for region 0.

Offset Address	Register Name	Total Reset Value
0x0234	DES_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

DES_CFG

DES_CFG is a DES configuration register.

Offset Address	Register Name	Total Reset Value
0x0270	DES_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmp_en	k_coef_range							reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cmp_en	DES channel frame compression enable 0: disabled 1: enabled 0x300−0x3FF: address space of the DES1 register 0x400−0x4FF: address space of the DES2 register
[30:27]	RW	k_coef_range	Frame compression rate of the DES channel. The value range is [7,12]. The typical value is the data bit width minus 1. The configured value is 12 when the data bit width is 14 bits.
[26:0]	RO	reserved	Reserved

DES_SIZE

DES_SIZE is a DES storage size register.

Offset Address	Register Name	Total Reset Value
0x0284	DES_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

DES_FADDR

DES_FADDR is a DES storage base address register.

Offset Address	Register Name	Total Reset Value
0x0290	DES_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	DES storage base address

DES_STRIDE

DES_STRIDE is a DES storage line stride register.

Offset Address	Register Name	Total Reset Value
0x0294	DES_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Line stride for the DES channel frame

DES_BUF_CFG

DES_BUF_CFG is a DES bus buffer control register.

Offset Address	Register Name	Total Reset Value
0x029C	DES_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	buf_thd	Bus buffer depth

DES_INT

DES_INT is a DES raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x02F0	DES_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

DES_MASK

DES_MASK is a DES interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x02F8	DES_MASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RW	field_throw	Field/Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable 0: masked 1: enabled

LINE_BUF_CFG

LINE_BUF_CFG is a LINE_BUF control register.

Offset Address	Register Name	Total Reset Value
0x0500	LINE_BUF_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable				reserved																											vsync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	LINE_BUF enable 0: disabled 1: enabled
[30:1]	RO	reserved	Reserved
[0]	RW	vsync_mode	Frame discarding mode control signal 0: Both data and the VS signal are discarded during frame discarding. 1: Only data is discarded during frame discarding.

LINE_BUF_REG_NEWER

LINE_BUF_REG_NEWER is a LINE_BUF update register.

Offset Address	Register Name	Total Reset Value
0x0504	LINE_BUF_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	reg_newer	LINE_BUF update. This bit is automatically cleared for each frame.

LINE_BUF_ID_CFG

LINE_BUF_ID_CFG is a LINE_BUF RX ID selection register (instant register).

Offset Address	Register Name	Total Reset Value
0x0510	LINE_BUF_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	id_sel	ID of the data received by the LINE_BUF 0: Data with this ID is filtered. 1: Data with this ID is received. bit[0]: LINE_BUF RX enable for data with the ID 0 bit[1]: LINE_BUF RX enable for data with the ID 1 bit[2]: LINE_BUF RX enable for data with the ID 2 bit[3]: LINE_BUF RX enable for data with the ID 3

LINE_BUF_ADAPTER_CFG

LINE_BUF_ADAPTER_CFG is a timing adaptation register.

Offset Address	Register Name	Total Reset Value
0x0514	LINE_BUF_ADAPTER_CFG	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vsync_mode	hsync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vsync_mode	Whether to delay the VS signal 0: no 1: yes
[0]	RW	hsync_mode	Whether to delay the HS signal 0: no 1: yes

LINE_BUF_CROP_CFG

LINE_BUF_CROP_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x0520	LINE_BUF_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

LINE_BUF_CROP0_START

LINE_BUF_CROP0_START is a crop start position register for region 0 (instant register).

Offset Address	Register Name	Total Reset Value
0x0530	LINE_BUF_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which images start to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which images start to be captured

LINE_BUF_CROP0_SIZE

LINE_BUF_CROP0_SIZE is a crop size configuration register for region 0 (instant register).

Offset Address	Register Name	Total Reset Value
0x0534	LINE_BUF_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

LINE_BUF_WIDTH

LINE_BUF_WIDTH is a LINE_BUF image width register.

Offset Address	Register Name	Total Reset Value
0x0550	LINE_BUF_WIDTH	0x077F_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				line_buf_thd												reserved				line_buf_width											
Reset	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	line_buf_thd	Threshold for starting the LINE_BUF RAM read operation
[15:13]	RO	reserved	Reserved
[12:0]	RW	line_buf_width	LINE_BUF image width

LINE_BUF_HEIGHT

LINE_BUF_HEIGHT is a LINE_BUF image height register.

Offset Address	Register Name	Total Reset Value
0x0554	LINE_BUF_HEIGHT	0x0000_0437

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_buf_height											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	line_buf_height	LINE_BUF image height

LINE_BUF_INT

LINE_BUF_INT is a LINE_BUF raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x05F0	LINE_BUF_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	reserved	reserved	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

LINE_BUF_MASK

LINE_BUF_MASK is a LINE_BUF interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x05F8	LINE_BUF_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	reserved	reserved	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable 0: masked 1: enabled
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	RW	fstart	Field/Frame start interrupt enable 0: masked 1: enabled

SRC_CTRL

SRC_CTRL is an SRC control register.

Offset Address	Register Name	Total Reset Value
0x0600	SRC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							bit_width							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	SRC enable 0: disabled 1: enabled 0x600−0x6FF: address space of the SRC0 register 0x700−0x7FF: address space of the SRC1 register 0x800−0x8FF: address space of the SRC2 register 0x900−0x9FF: address space of the SRC3 register
[30:6]	RO	reserved	Reserved
[5:0]	RW	bit_width	SRC read data bit width 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

SRC_REG_NEWER

SRC_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x0604	SRC_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	reg_newer	SRC update. This bit is automatically cleared for each frame. 0: not updated (frames are discarded) 1: updated

SRC_CFG

SRC_CFG is an SRC configuration register.

Offset Address	Register Name	Total Reset Value
0x0670	SRC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_en	k_coef_range			reserved																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dcmp_en	SRC read channel frame compress enable 0: disabled 1: enabled
[30:27]	RW	k_coef_range	Frame compression rate of the SRC channel. The value range is [7,12]. The configuration during decompression must be the same as the that during data compression. The typical value is the bit width minus 1. The configured value is 12 when the bit width is 14 bits.
[26:0]	RO	reserved	Reserved

SRC_SIZE

SRC_SIZE is an SRC storage size register.

Offset Address	Register Name	Total Reset Value
0x0684	SRC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

SRC_FADDR

SRC_FADDR is an SRC storage base address register.

Offset Address	Register Name	Total Reset Value
0x0690	SRC_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	SRC storage base address

SRC_STRIDE

SRC_STRIDE is an SRC storage line stride register.

Offset Address	Register Name	Total Reset Value
0x0694	SRC_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Line stride for the SRC channel frame

SRC_BUF_CFG

SRC_BUF_CFG is an SRC bus buffer control register.

Offset Address	Register Name	Total Reset Value
0x069C	SRC_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	buf_thd	Depth of the bus buffer

SRC_INT

SRC_INT is an SRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x06F0	SRC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5]	WC	dcmp_wrong	Status of the decompress error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

SRC_MASK

SRC_MASK is an SRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x06F8	SRC_MASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5	4	3	2	1	0
Name	reserved							dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5]	RW	dcmp_wrong	Decompress error interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	update_cfg	Register update interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable 0: masked 1: enabled

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x1000	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																													mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable 0: disabled 1: enabled
[30:2]	RO	reserved	Reserved

[1:0]	RW	mode	Channel mode 00: normal mode 01: single-component (luminance) mode 10: single-component (chrominance) mode Other values: reserved

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x1004	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_newer	Channel update. This bit is automatically cleared for each frame.

CH_ADAPTER_CFG

CH_ADAPTER_CFG is a timing adaptation register.

Offset Address	Register Name	Total Reset Value
0x1010	CH_ADAPTER_CFG	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vsync_mode	hsync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[1]	RW	vsync_mode	Whether to perform delay processing on the vsync signal The delay processing is performed on the vsync signal only when both sharpen and uvnr are enabled. 0: not processed 1: processed
[0]	RW	hsync_mode	Whether to perform delay processing on the hsync signal 0: not processed 1: processed

CH_DLY_CFG

CH_DLY_CFG is a channel input image start interrupt delay configuration register.

Offset Address	Register Name	Total Reset Value
0x1034	CH_DLY_CFG	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_dly_cfg																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	v_dly_cfg	Number of delayed vertical lines
[15:0]	RO	reserved	Reserved

CH_WCH_Y_CFG

CH_WCH_Y_CFG is a Y component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1080	CH_WCH_Y_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	bit_width		reserved											flip	mirror	head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled

[30:20]	RO	reserved	Reserved
[19]	RW	interleave	Progressive/Interlaced flag 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storing. 1: The output data interlaced and needs to be interleaved as frames for storing.
[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data interlaced and needs to be interleaved as frames for storing. 0: top field 1: bottom field
[17:16]	RW	bit_width	Data width 00: 8 bits 10: 16 bits Other values: reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2]	RW	head_tword	Header information stride 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)
[1]	RW	cmp_mode	Compressed segment length 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable 0: disabled 1: enabled

CH_WCH_Y_SIZE

CH_WCH_Y_SIZE is a Y component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1084	CH_WCH_Y_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

CH_WCH_Y_FADDR

CH_WCH_Y_FADDR is a Y component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1090	CH_WCH_Y_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the Y component

CH_WCH_Y_HADDR

CH_WCH_Y_HADDR is a Y component header information storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1094	CH_WCH_Y_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the Y component header information

CH_WCH_Y_STRIDE

CH_WCH_Y_STRIDE is a Y component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1098	CH_WCH_Y_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the Y component

CH_WCH_Y_BUF_CFG

CH_WCH_Y_BUF_CFG is a CH_DES bus buffer control register.

Offset Address	Register Name	Total Reset Value
0x109C	CH_WCH_Y_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	buf_thd	Bus buffer depth

CH_WCH_C_CFG

CH_WCH_C_CFG is a C component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A0	CH_WCH_C_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	bit_width		reserved											flip	mirror	head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled
[30:20]	RO	reserved	Reserved
[19]	RW	interleave	Progressive/Interlaced flag 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storing. 1: The output data interlaced and needs to be interleaved as frames for storing.
[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data interlaced and needs to be interleaved as frames for storing. 0: top field 1: bottom field
[17:16]	RW	bit_width	Data width 00: 8 bits 10: 16 bits Other values: reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2]	RW	head_tword	Header information stride 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)

[1]	RW	cmp_mode	Compressed segment length 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable 0: disabled 1: enabled

CH_WCH_C_SIZE

CH_WCH_C_SIZE is a C component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A4	CH_WCH_C_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

CH_WCH_C_FADDR

CH_WCH_C_FADDR is a C component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B0	CH_WCH_C_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the C component

CH_WCH_C_HADDR

CH_WCH_C_HADDR is a C component header information storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B4	CH_WCH_C_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the C component header information

CH_WCH_C_STRIDE

CH_WCH_C_STRIDE is a C component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B8	CH_WCH_C_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the C component

CH_WCH_C_BUF_CFG

CH_WCH_C_BUF_CFG is a CH_DES bus buffer control register.

Offset Address	Register Name	Total Reset Value
0x10BC	CH_WCH_C_BUF_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																buf_thd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	buf_thd	Bus buffer depth

CH_Y_OUT_SIZE

CH_Y_OUT_SIZE is a channel luminance image output size indicator register.

Offset Address	Register Name	Total Reset Value
0x10E8	CH_Y_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Image height
[15:0]	RO	width	Image width

CH_C_OUT_SIZE

CH_C_OUT_SIZE is a channel chrominance image output size indicator register.

Offset Address	Register Name	Total Reset Value
0x10EC	CH_C_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Image height
[15:0]	RO	width	Image width

CH_INT

CH_INT is a channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10F0	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	WC	fstart_dly	Status of the delayed field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14:5]	RO	reserved	Reserved
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10F8	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved										update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	fstart_dly	Delayed field/frame start interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.
[14:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	field_throw	Field/Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Field/Frame start interrupt enable 0: masked 1: enabled

CH_Y_CROP_CFG

CH_Y_CROP_CFG is a luminance crop enable register.

Offset Address	Register Name	Total Reset Value
0x1100	CH_Y_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

CH_Y_CROP0_START

CH_Y_CROP0_START is a crop start position register for luminance region 0.

Offset Address	Register Name	Total Reset Value
0x1110	CH_Y_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the image starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the image starts to be captured

CH_Y_CROP0_SIZE

CH_Y_CROP0_SIZE is a crop size register for luminance region 0.

Offset Address	Register Name	Total Reset Value
0x1114	CH_Y_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

CH_C_CROP_CFG

CH_C_CROP_CFG is a luminance crop enable register.

Offset Address	Register Name	Total Reset Value
0x1120	CH_C_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

CH_C_CROP0_START

CH_C_CROP0_START is a crop start position register for chrominance region 0.

Offset Address	Register Name	Total Reset Value
0x1130	CH_C_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the image starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the image starts to be captured

CH_C_CROP0_SIZE

CH_C_CROP0_SIZE is a crop size register for chrominance region 0.

Offset Address	Register Name	Total Reset Value
0x1134	CH_C_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

9.2 VDP

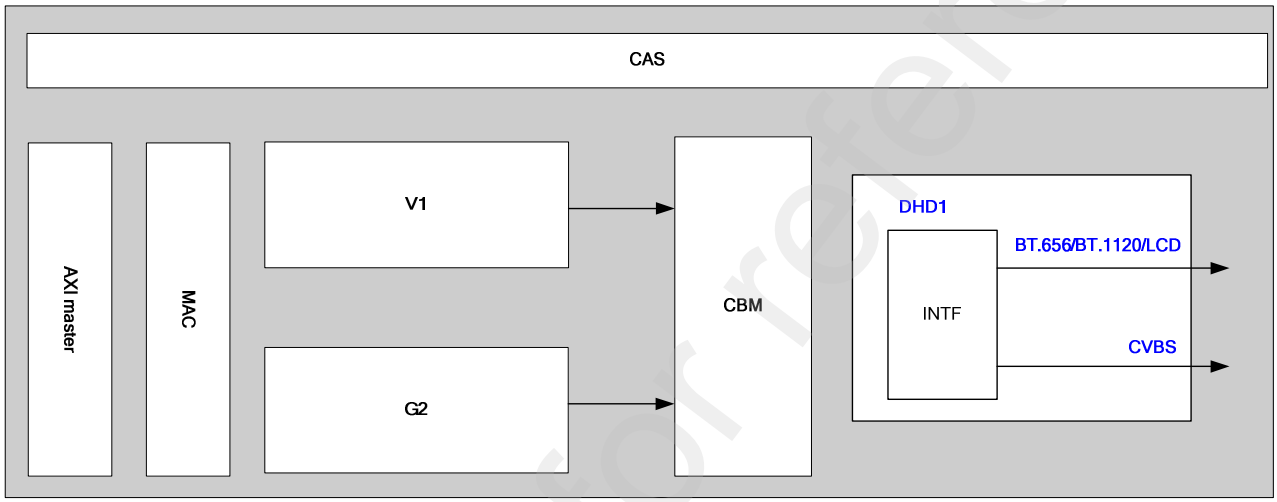
9.2.1 Overview

The video display processor (VDP) reads video and graphics data from the memory, overlays the data at the video and graphics layers, and transmits the data through the display channel.

9.2.2 Architecture

Figure 9-17 shows the block diagram of the VDP.

Figure 9-17 Block diagram of the VDP



The following describes the major concepts:

- Surface: data path of bus inputs. The surface reads and processes the bus data of a layer. The surfaces include the video layer V1 and graphics layer G2.
- Display channel: It includes the HD display channel DHD1.
- Crossbar mixer (CBM): It supports overlapping of the video layer and graphics layer.
- Memory access controller (MAC): Each module reads data from the memory over the AXI bus. The MAC arbitrates the requests from all surfaces.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers

  Include the bus configuration registers, interrupt registers, and version register.
- Surface registers

  Include the video layer configuration registers and graphics layer configuration registers.
- Display channel registers

  Include the DHD1 configuration registers.

The VDP has the following features:

- Digital output interface that supports the ITU-R BT.656 output, 16-bit parallel LCD output, 6-/8-bit serial LCD output, and ITU-R BT.1120 output
- Video layer (V1)
- Graphics layer (G2)
- Overlay
- One video channel. It has a separate vertical timing interrupt (indicating the end of a field/frame) and a low bandwidth interrupt.
- Analog output interface that supports the CVBS output

9.2.3 Operating Mode

9.2.3.1 Clock Configurations

The VDP clock source can be set to either of the following clocks:

Interface output clock source: U_VPLL

For details, see the description of the PERI_CRG17 and PERI_CRG18 for 3.2.2 section.

9.2.3.2 Reset

The VDP supports a hard reset signal and a soft reset signal.

CAUTION

Before soft-resetting the AXI bus, do as follows:

- Disable all layers.
- Configure the bus reset request after the next field/frame interrupt is detected.

9.2.3.3 Bus Configurations

AXI Master

The VDP provides one master interface to improve bus access efficiency.

The VDP supports the AXI master. The data read/write requests of V1 and G2 can be implemented by using the master.

The VDP supports multiple IDs that cannot be dynamically switched.

APB Register Configuration

The VDP registers are read and written over the APB interface. The base address for VDP registers is 0x1100_0000, the register addressing space is 64 KB, and the address offset range is 0x0000–0xFFFF.

Outstanding Configuration

The depth of the AXI master outstanding ranges from 0 to 7. When the outstanding depth is set to 0, the AXI master does not operate the bus.

9.2.3.4 Digital Output Interfaces

The VDP supports three digital interface output modes: ITU-R BT.656, ITU-R BT.1120 and LCD RGB.

9.2.3.5 Interrupts

VDP interrupts are classified into:

- Vertical timing interrupt
- Low bandwidth interrupt
- DAC no-load interrupt

Vertical Timing Interrupt

The position of generating the vertical timing interrupt can be configured.

- The VDP supports one vertical timing interrupt, indicating the end of a frame or field.
- The interrupt can be generated by frame or field.
- In progressive display mode, the vertical timing interrupt must be generated by frame.
- In interlaced display mode, the vertical timing interrupt can be generated by frame or field. You are advised to set the interrupt generation mode to generation by field for HD and generation by frame for SD.
- Interrupt mask can be configured.
- The threshold for the vertical timing interrupt can be configured.
- Each interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP allows the low bandwidth status to be reported by using an interrupt.

- The VDP supports one low bandwidth interrupt, indicating low bandwidth of a frame or field.
- The interrupt can be masked.
- Each interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

9.2.4 Function Description

9.2.4.1 Video Layer

Features

The video layer has the following features:

- Uncompressed and losslessly compressed data sources
- Input pixel formats of semi-planar420, semi-planar400, and semi-planar422
- Minimum input resolution of 32 x 32 and maximum input resolution of 1920 x 1080
- Minimum output resolution of 32 x 32 and maximum output resolution of 1920 x 1080
- A multiple of 2 for the input horizontal resolution
- A multiplier of 4 for the interlaced 420 input vertical resolution and a multiple of 2 for the other input vertical resolutions

- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, uncompressed data source (2-byte-aligned), and compressed data source (16-byte-aligned)
- User-defined source luminance and chrominance stride, 16-byte-aligned
- Vertical chrominance up sampling, replication mode
- Horizontal chrominance up sampling (IFIR), replication mode, bilinear interpolation, and 16-order half-band filtering
- Color space conversion (CSC) and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255

DCMP (Decompression)

The data resource read by the VDP may be compressed data, which reduces the bandwidth. V1 decompresses the compressed data to restore it to original YCbCr pixels.

Horizontal Cropping

The input can be cropped horizontally.

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422. V1 converts the data format in replication mode.

422-444 (Horizontal Chrominance Up Sampling)

Horizontal chrominance up sampling converts the YUV422 data format into YUV444.

This function can be implemented in three ways:

- Replication
- Bilinear interpolation
- 16-order half-band filtering

CSC

- CSC among YCbCr, BT.601, RGB, and BT.709
- Adjustment of luminance, hue, and saturation

9.2.4.2 Graphics Layer

Features

The graphics layer has the following features:

- Input pixel formats of ARGB1555, ARGB4444 and ARGB8888
- Minimum input resolution of 32 x 32 and maximum input resolution of 1920 x 1080
- Minimum output resolution of 32 x 32 and maximum output resolution of 1920 x 1080
- A multiple of 2 for the input horizontal or vertical resolution
- Interlaced mode and progressive mode

- Frame update and field update
- User-defined source start address, 128-bit-aligned (16-byte-aligned)
- User-defined source stride, 128-bit-aligned (16-byte-aligned)
- CSC
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255
- Enabling or disabling of the pixel alpha, and alpha0 or alpha1 for the image in ARGB1555 format with pixel alpha
- Color key processing
- Premultiplication

CSC

CSC between RGB2YCbCr601 and RGB2YCbCr709 is supported.

Alpha Processing

The alpha value sources of the graphics layer are as follows:

- Pixel alpha value: overlay attribute of a pixel
- Global alpha value: overlay attributes of a layer

There is a special pixel alpha value. In ARGB1555 format, the alpha value is only one bit. This bit is the index of the alpha value but not the actual alpha value. The index value is used to select the actual alpha value from the alpha register. When the index value is 0, alpha0 is selected; when the index value is other values, alpha1 is selected.

Color key

- The key mode is configurable. The pixels inside or outside the range can be selected for key processing.
- The key bit can be masked.

Premultiplication

Input data can be premultiplied data. In this case, the color key function must be disabled.

9.2.4.3 Overlaying

The VDP supports overlaying of V1 and G2.

Features

- Bottom-to-top overlaying
- User-defined overlaying background color
- User-defined priority of the overlaid surface

9.2.4.4 Display Channel

Video Channel Features

- DHD1 can function as an HD or SD output channel.

- Only one output timing is supported in an application scenario. HD and SD timings cannot be output at the same time.
- The following typical output timings are supported: 1080p, 1080i, 720p, 720i, PAL, NTSC.

Timing Configuration

The VDP output interfaces support typical and non-typical timings to connect to different interfaces.

CAUTION

Interfaces must be disabled before timing parameters are configured and be enabled after configuration.

9.2.4.5 BT.1120 HD Output Interface

Features

- 10 bits to 8 bits dither
- YCbCr444-to-YCbCr422 horizontal chrominance down sampling (DFIR)
- Clipping for data clamp (16−235 value range for the Y component and 16−240 value range for the C component according to the interface protocol)
- Typical output timings of 720p, 1080p, and 1080i
- Bypass mode; truncation and point discarding for dither and DFIR
- 16-bit data with the Y component in the upper bits and C component in the lower bits by default (the positions of the Y and C components can be exchanged)

9.2.4.6 BT.656 SD Output Interface

Features

- 10 bits to 8 bits dither
- YCbCr444-to-YCbCr422 horizontal chrominance down sampling (DFIR)
- Clipping for data clamp (16−235 value range for the Y component and 16−240 value range for the C component according to the interface protocol)
- Typical output timings of NTSC and PAL

9.2.4.7 CVBS SD Output Interface

Features

- Clipping for data clamp (64−940 value range for the Y component and 64−960 value range for the C component)
- Digital simulation for the digitalized analog TV encoder (DATE)
- VDAC automatic detection for the DATE
- Typical output timings of NTSC and PAL

9.2.4.8 RGB LCD Output Interface

Features

- 8-bit/6-bit serial RGB output with adjustable bit sequence (including the reverse sequence)
- 16-bit parallel RGB output in the default sequence of R, G, B (the B, G, R sequence is also supported)
- RGB serial output in the sequence of R, G, B. The lower eight bits of the 16 bits are output.
- Maximum 27 MHz output clock

9.2.5 Register Summary

Table 9-6 describes VDP registers.

Table 9-6 Summary of VDP registers (base address: 0x1100_0000)

Offset Address	Register	Description	Page
0x0000	VOCTRL	VO control register	9-96
0x0004	VOINTSTA	VO interrupt status register (read-only)	9-97
0x0008	VOMSKINTSTA	VO masked interrupt status register	9-98
0x000C	VOINTMSK	VDP interrupt mask register	9-99
0x0010	VDPVERSION1	VDP version register 1	9-100
0x0014	VDPVERSION2	VDP version register 2	9-100
0x0020	VOMEM_CTR	VDP memory debugging control register	
0x0034	VOAXICTRL	VO AXI bus configuration register	9-101
0x0100	VO_MUX	VO interface multiplexing register	9-102
0x0108	VO_MUX_TESTSYNC	VO interface test register	9-102
0x010C	VO_MUX_TESTDATA	VO interface test data register	9-103
0x0120	VO_DAC_CTRL	VO DAC control register	9-103
0x0134	VO_DAC_0_CTRL	VO DAC 0 channel control register	9-104
0x0140	VO_DAC_STAT0	VO DAC status 0 register	9-105
0x1000	V1_CTRL	V1 configuration register	9-106

Offset Address	Register	Description	Page
0x1004	V1_UPD	V1 channel update enable register	9-108
0x1028	V1_IRESO	V1 input resolution register	9-108
0x102C	V1_ORESO	V1 output resolution register	9-108
0x1034	V1_DCMP_SGMT_CROP	Input segment decompression crop register	9-109
0x1038	V1_CBMPARA	V1 overlay parameter register	9-109
0x1044	V1_CPOS	Horizontal crop coordinate register for the source image	9-110
0x1060	V1_DFPOS	V1 surface start position (in the display window) register	9-110
0x1064	V1_DLPOS	V1 surface end position (in the display window)	9-111
0x1080	V1_CSC_IDC	V1 CSC input DC component register	9-111
0x1084	V1_CSC_ODC	V1 CSC output DC component register	9-112
0x1088	V1_CSC_IODC	V1 CSC input/output DC component register	9-113
0x108C	V1_CSC_P0	V1 CSC parameter 0 register	9-113
0x1090	V1_CSC_P1	V1 CSC parameter 1 register	9-114
0x1094	V1_CSC_P2	V1 CSC parameter 2 register	9-114
0x1098	V1_CSC_P3	V1 CSC parameter 3 register	9-115
0x109C	V1_CSC_P4	V1 CSC parameter 4 register	9-115
0x1204	V1_P0LADDR	V1 luminance address register	9-116
0x1208	V1_P0CADDR	V1 chrominance address register	9-116
0x120C	V1_P0STRIDE	V1 stride register	9-117
0x1640	V1_LADDROFFSET	Offset (luminance compressed data address relative to the header information address) register, valid only when the decompression function is enabled	9-117
0x1644	V1_CADDROFFSET	Offset (chrominance compressed data address relative to the header information address) register, valid only when the decompression function is enabled	9-117
0x1720	V1_DCMP_LSTATE0	Decompression status register 0 for the V1 luminance channel	9-118
0x1724	V1_DCMP_LSTATE1	Decompression status register 1 for the V1 luminance channel	9-118

Offset Address	Register	Description	Page
0x1728	V1_DCMP_CSTATE0	Decompression status register 0 for the V1 chrominance channel	9-118
0x172C	V1_DCMP_CSTATE1	Decompression status register 1 for the V1 chrominance channel	9-119
0x1730	V1_DCMPERRCLR	V1 decompression error status clear register	9-119
0x1734	V1_DCMP_ERR	V1 decompression error signal register	9-120
0x7000	G2_CTRL	G2 configuration register	9-120
0x7004	G2_UPD	G2 update enable register	9-122
0x7010	G2_ADDR	G2 address register	9-122
0x701C	G2_STRIDE	G2 stride register	9-123
0x7020	G2_IRESO	G2 input resolution register	9-123
0x7024	G2_SFPOS	G2 surface read data start position (in the source bitmap) register	9-124
0x7030	G2_CBMPARA	Overlay parameter register	9-124
0x7034	G2_CKEYMAX	Maximum color key value register	9-125
0x7038	G2_CKEYMIN	Minimum color key value register	9-126
0x703C	G2_CMASK	Color key mask value register	9-126
0x7080	G2_DFPOS	G2 surface start position (in the display window) register	9-127
0x7084	G2_DLPOS	G2 surface end position (in the display window) register	9-127
0x70C0	G2_CSC_IDC	G2 CSC input DC component register	9-128
0x70C4	G2_CSC_ODC	G2 CSC output DC component register	9-129
0x70C8	G2_CSC_IODC	G2 CSC input/output DC component register	9-129
0x70CC	G2_CSC_P0	G2 CSC parameter 0 register	9-130
0x70D0	G2_CSC_P1	G2 CSC parameter 1 register	9-130
0x70D4	G2_CSC_P2	G2 CSC parameter 2 register	9-131
0x70D8	G2_CSC_P3	G2 CSC parameter 3 register	9-132
0x70DC	G2_CSC_P4	G2 CSC parameter 4 register	9-132

Offset Address	Register	Description	Page
0xB420	CBM_BKG2	CBM mixer 2 overlay background color register	9-132
0xB428	CBM_MIX2	CBM mixer 2 priority configuration register	9-133
0xC400	DHD1_CTRL	DHD1 global control register	9-134
0xC404	DHD1_VSYNC	Top field VS timing register in interlaced output mode or frame VS timing register in progressive output mode	9-135
0xC408	DHD1_HSYNC1	HS configuration register in interlaced or progressive output mode	9-135
0xC40C	DHD1_HSYNC2	HS configuration register in interlaced or progressive output mode	9-136
0xC410	DHD1_VPLUS	Bottom field VS timing register in interlaced output mode	9-136
0xC414	DHD1_PWR	Sync signal pulse width register	9-137
0xC418	DHD1_VTTHD3	Vertical timing threshold register	9-137
0xC41C	DHD1_VTTHD	Vertical timing threshold register	9-138
0xC4B0	DHD1_PARATHD	PARA coefficient update point threshold register	9-139
0xC4C0	DHD1_START_POS	DHD1 start signal start position register	9-139
0xC4F0	DHD1_STATE	DHD1 status register	9-140
0xD200	BT_CTRL	BT.656/BT.1120 control register	9-140
0xD210	BT_CLIP0_L	BT.656/BT.1120 clip lowest threshold register	9-141
0xD214	BT_CLIP0_H	BT.656/BT.1120 clip highest threshold register	9-142
0xD280	BT_DITHER0_CTRL	BT.656/BT.1120 dither control register	9-142
0xD284	BT_DITHER0_COEF0	BT.656/BT.1120 dither coefficient 0 register	9-143
0xD288	BT_DITHER0_COEF1	BT.656/BT.1120 dither coefficient 1 register	9-144
0xD400	LCD_CTRL	LCD control register	9-144
0xD408	LCD_SYNC_INV	Sync signal polarity configuration register in LCD external sync timing input mode	9-145

Offset Address	Register	Description	Page
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0xF204	DATE_COEFF1	Amplitude configuration register	9-150
0xF208	DATE_COEFF2	DATE coefficient 2 register	9-151
0xF20C	DATE_COEFF3	DATE coefficient 3 register	9-151
0xF210	DATE_COEFF4	DATE coefficient 4 register	9-151
0xF214	DATE_COEFF5	DATE coefficient 5 register.	9-152
0xF218	DATE_COEFF6	DATE coefficient 6 register	9-152
0xF254	DATE_COEFF21	Output matrix control register	9-153
0xF258	DATE_COEFF22	Discrete time oscillator (DTO) initial phase configuration register	9-154
0xF25C	DATE_COEFF23	VIDEO_OUT delay configuration register	9-154
0xF260	DATE_COEFF24	Color burst start position register	9-154
0xF280	DATE_ISRMASK	Interrupt mask register	9-155
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0xF294	DATE_COEFF37	Up-sampling filtering coefficient 1 register	9-156
0xF298	DATE_COEFF38	Up-sampling filtering coefficient 2 register	9-157
0xF29C	DATE_COEFF39	Up-sampling filtering coefficient 3 register	9-157
0xF2A0	DATE_COEFF40	Up-sampling filtering coefficient 4 register	9-157
0xF2A4	DATE_COEFF41	Up-sampling filtering coefficient 5 register	9-158
0xF2A8	DATE_COEFF42	Up-sampling filtering coefficient 6 register	9-158

Offset Address	Register	Description	Page
0xF2C0	DATE_DACDET1	DAC automatic detection register 1	9-159
0xF2C4	DATE_DACDET2	DAC automatic detection register 2	9-159
0xF2C8	DATE_COEFF50	Over-sampling filtering coefficient 1 register	9-160
0xF2CC	DATE_COEFF51	Over-sampling filtering coefficient 2 register	9-160
0xF2D0	DATE_COEFF52	Over-sampling filtering coefficient 3 register	9-160
0xF2D4	DATE_COEFF53	Over-sampling filtering coefficient 4 register	9-161
0xF2D8	DATE_COEFF54	Over-sampling filtering coefficient 5 register	9-161
0xF2DC	DATE_COEFF55	Over-sampling filtering coefficient 6 register	9-162
0xF2E0	DATE_COEFF56	Over-sampling round-off register	9-162
0xF2E4	DATE_COEFF57	CVBS gain control register	9-163
0xF2E8	DATE_COEFF58	Component gain control register	9-164
0xF2EC	DATE_COEFF59	Clip control bit register	9-164

9.2.6 Register Description

VOCTRL

VOCTRL is a VO control register. It is used to configure the arbitration mode of surface bus requests.

Offset Address	Register Name	Total Reset Value
0x0000	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	reserved																											m0_arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_ck_gt_en	VDP clock gating enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3:0]	RW	m0_arb_mode	Arbitration mode of data requests of internal surface buses of VO MAC0 0x0: polling 0x1: graphics layer first Other values: reserved

VOINTSTA

VOINTSTA is a VO interrupt status register (read-only).

Offset Address	Register Name	Total Reset Value
0x0004	VOINTSTA	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dhd1uf_int	reserved	reserved	dhd1vtthd1_int	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	dhd1uf_int	DHD1 low-bandwidth alarm interrupt 0: An interrupt is reported. 1: No interrupt is reported.

[6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4]	RO	dhd1vtthd1_int	DHD1 vertical timing interrupt 1 0: An interrupt is reported. 1: No interrupt is reported.
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x0008	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			vdac0_unload_int	reserved	reserved	reserved	reserved	dhd1uf_clr	reserved	reserved	dhd1vtthd1_clr	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	vdac0_unload_int	DAC0 offload interrupt 0: An interrupt is reported. 1: No interrupt is reported.
[11]	RO	reserved	Reserved
[10]	RO	reserved	Reserved
[9]	RO	reserved	Reserved
[8]	RO	reserved	Reserved
[7]	WC	dhd1uf_clr	DHD1 low-bandwidth alarm interrupt 0: An interrupt is reported. 1: No interrupt is reported.
[6]	RO	reserved	Reserved

[5]	RO	reserved	Reserved
[4]	WC	dhd1vtthd1_clr	DHD1 vertical timing interrupt 1 0: An interrupt is reported. 1: No interrupt is reported.
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

VOINTMSK

VOINTMSK is a VDP interrupt mask register. It corresponds to VOINTSTA. When the corresponding bit is set to 1, the interrupt is enabled; when the corresponding bit is set to 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0x000C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dhd1uf_intmsk	reserved	reserved	dhd1vtthd1_intmsk	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	dhd1uf_intmsk	Mask for the DHD1 low-bandwidth alarm interrupt 0: masked 1: enabled
[6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4]	RW	dhd1vtthd1_intmsk	Mask for DHD1 vertical timing interrupt 1 0: masked 1: enabled
[3:0]	RO	reserved	Reserved

VDPVERSION1

VDPVERSION1 is VDP version register 1.

Offset Address	Register Name	Total Reset Value
0x0010	VDPVERSION1	0x7675_6F76

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion1																															
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion1	VDP version 1

VDPVERSION2

VDPVERSION2 is VDP version register 2.

Offset Address	Register Name	Total Reset Value
0x0014	VDPVERSION2	0x3031_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion2																															
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion2	VDP version 2

VOMEM_CTRL

VOMEM_CTRL is a VDP memory debugging control register.

Offset Address	Register Name	Total Reset Value
0x0024	VOMEM_CTRL	0x0000_1B0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		rft_emab		rft_emaa				reserved				rfs_emaw		rfs_ema	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:11]	RW	rft_emab	Speed adjustment for the EMAB end of the RFT memory
[10:8]	RW	rft_emaa	Speed adjustment for the EMAA end of the RFT memory
[7:5]	RO	reserved	Reserved
[4:3]	RW	rfs_emaw	Speed adjustment for the EMAW end of the RFS memory
[2:0]	RW	rfs_ema	Speed adjustment for the EMA end of the RFS memory

VOAXICTRL

VOAXICTRL is a VO AXI bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	VOAXICTRL	0x1110_0111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																m0_v0_id_sel				reserved								m0_outstd_rid0			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	m0_v0_id_sel	M0 multiple read ID output enable 0: One ID is output. 1: Multiple IDs are output.
[14:4]	RO	reserved	Reserved
[3:0]	RW	m0_outstd_rid0	Read ID0 outstanding of AXI master 0. The value ranges from 0 to 7.

VO_MUX

VO_MUX is a VO interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0x0100	VO_MUX	0x0001_6540

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	digital_sel	reserved						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	digital_sel	Digital interface data select. The default value is 0. 0x0: BT.1120 0x1: BT.656 0x2: LCD Other values: reserved
[27:0]	RO	reserved	Reserved

VO_MUX_TESTSYNC

VO_MUX_TESTSYNC is a VO interface test register.

Offset Address	Register Name	Total Reset Value
0x0108	VO_MUX_TESTSYNC	0x0110_0104

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	vo_test_en	reserved						test_field	test_vsync	test_hsync	test_dv
Reset	0 0 0 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	vo_test_en	VDP output interface test mode enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved

[3]	RW	test_field	Test value of the field signal
[2]	RW	test_vsync	Test value of the vsync signal
[1]	RW	test_hsync	Test value of the hsync signal
[0]	RW	test_dv	Test value of the dv signal

VO_MUX_TESTDATA

VO_MUX_TESTDATA is a VO interface test data register.

Offset Address	Register Name	Total Reset Value
0x010C	VO_MUX_TESTDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				test_data																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RW	test_data	Output data in test mode The output of DAC channels is the lower 10 bits of the register value, the output of the BT.1120 channel is the lower 16 bits of the register value, the output of the LCD channel is bits 29−22, 19−12, and 9−2 of the register, and the output of other channels is the register value. The output is in the RGB or YUV format from upper bits to lower bits.

VO_DAC_CTRL

VO_DAC_CTRL is a VO DAC control register.

Offset Address	Register Name	Total Reset Value
0x0120	VO_DAC_CTRL	0x2000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									envbg	pdchopper	enextref	reserved				dac_reg_rev															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	envbg	VBG reference voltage enable 0: disabled 1: enabled
[21]	RW	pdchopper	VBG chopper enable 0: enabled 1: disabled
[20]	RW	enextref	VBG output test enable 0: The internal VBG is used. The VBG is not output to the test pin. 1: The VBG is output for external tests.
[19:16]	RO	reserved	Reserved
[15:0]	RW	dac_reg_rev	The test is reserved.

VO_DAC_0_CTRL

VO_DAC_0_CTRL is a VO DAC 0 channel control register.

Offset Address	Register Name	Total Reset Value
0x0134	VO_DAC_0_CTRL	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dac0en	reserved																					dac0gc						reserved		cablectr0	
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dac0en	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dac0gc	DAC output amplitude control The output voltage of the DAC at full scale ranges from 0.52 V to 1.37 V. The output amplitude is adjusted in 64 phases and the adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + Gain x 0.358 (mA) 000000: 0.52 V … 111111: 1.37 V
[3:2]	RO	reserved	Reserved
[1:0]	RW	cablectr0	DAC VREF_CABLE reference voltage adjustment 00: normal by default 01: −10% 10: −20% 11: +10%

VO_DAC_STAT0

VO_DAC_STAT0 is a VO DAC status 0 register.

Offset Address	Register Name	Total Reset Value
0x0140	VO_DAC_STAT0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cableout0	reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	cableout0	cableout0 feedback signal
[15:0]	RO	reserved	Reserved

V1_CTRL

V1_CTRL is a V1 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1000	V1_CTRL	0x0000_0000

Bit	31	30 29 28	27 26 25 24	23	22	21	20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5 4	3 2 1 0
Name	surface_en	reserved	reserved	crop_en	reserved	precharge_en	precharge_mode	ifir_mode	reserved	lm_rmode	chm_rmode	reserved	dcmp_en	reserved	ifmt
Reset	0	0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant) 0: disabled 1: enabled
[30:29]	RO	reserved	Reserved
[28]	RW	die_rd_en	Chrominance channel read repeat enable (valid only when the input is 420 data) 0: disabled 1: enabled
[27:24]	RO	reserved	Reserved

[23]	RW	crop_en	Crop enable (non-instant) 0: disabled 1: enabled
[22]	RO	reserved	Reserved
[21]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[20]	RW	precharge_mode	Pre-charge mode of the FDR FIFO 0: hardware mode. Hardware automatically enters the pre-charge status on the frame trailer. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode 00: reserved 01: chrominance IFIR replication mode 10: bilinear interpolation 11: 16-order half-band filtering
[17:16]	RO	reserved	Reserved
[15:14]	RW	lm_rmode	Luminance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[13:12]	RW	chm_rmode	Chrominance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[11:9]	RO	reserved	Reserved
[8]	RW	dcmp_en	Decompression enable 0: disable 1:enable
[7:4]	RO	reserved	Reserved
[3:0]	RW	ifmt	Format of the input data 0x1: SPYCbCr400 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

V1_UPD

V1_UPD is a V1 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x1004	V1_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

V1_IRESO

V1_IRESO is a V1 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1028	V1_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ih	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	iw	Width (in pixel). The configured value is the actual width minus 1.

V1_ORESO

V1_ORESO is a V1 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x102C	V1_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	oh	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	ow	Width (in pixel). The configured value is the actual width minus 1.

V1_DCMP_SGMT_CROP

V1_DCMP_SGMT_CROP is an input segment decompression crop register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1034	V1_DCMP_SGMT_CROP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dcmp_xlsgmt				dcmp_xfsgmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	dcmp_xlsgmt	End segment for segment decompression
[3:0]	RW	dcmp_xfsgmt	Start segment for segment decompression

V1_CBMPARA

V1_CBMPARA is a V1 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1038	V1_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates completely transparent.

V1_CPOS

V1_CPOS is a horizontal crop coordinate register for the source image.

Offset Address	Register Name	Total Reset Value
0x1044	V1_CPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								src_xlpos												src_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	src_xlpos	End coordinates for horizontally cropping the source image
[11:0]	RW	src_xfpos	Start coordinates for horizontally cropping the source image

V1_DFPOS

V1_DFPOS is a V1 surface start position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1060	V1_DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_yfpos	Start coordinates of the display column The frame height is referenced and its unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row

V1_DLPOS

V1_DLPOS is a V1 surface end position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1064	V1_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_ylpos	End coordinates of the display column The frame height is referenced and its unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row

V1_CSC_IDC

V1_CSC_IDC is a V1 CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1080	V1_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_en	cscidc1														cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of the input U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc0	DC parameter of the input V/B component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_ODC

V1_CSC_ODC is a V1 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1084	V1_CSC_ODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_sign_mode	cscodc1														cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of the output U/G component. The MSB is the signed bit. The value is expressed as a two's complement.

[10:0]	RW	cscodc0	DC parameter of the output Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_IODC

V1_CSC_IODC is a V1 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1088	V1_CSC_IODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cscodc2												cscidc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:11]	RW	cscodc2	DC parameter of the output V/B component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc2	DC parameter of the input Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_P0

V1_CSC_P0 is a V1 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x108C	V1_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp01															reserved	cscp00														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp01	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved

[14:0]	RW	cscp00	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P1

V1_CSC_P1 is a V1 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1090	V1_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp10	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp02	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P2

V1_CSC_P2 is a V1 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1094	V1_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:16]	RW	cscp12	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp11	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P3

V1_CSC_P3 is a V1 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1098	V1_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp21															reserved	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp21	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp20	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P4

V1_CSC_P4 is a V1 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x109C	V1_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscp22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	cscp22	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_P0LADDR

V1_P0LADDR is a V1 luminance address register.

Offset Address	Register Name	Total Reset Value
0x1204	V1_P0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Luminance start address for the video layer

V1_P0CADDR

V1_P0CADDR is a V1 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x1208	V1_P0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address for the video layer

V1_P0STRIDE

V1_P0STRIDE is a V1 stride register.

Offset Address	Register Name	Total Reset Value
0x120C	V1_P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of the video layer (valid in semi-planar format), 128-bit alignment
[15:0]	RW	surface_stride	Stride of the video layer buffer (luminance stride in semi-planar format), 128-bit alignment

V1_LADDROFFSET

V1_LADDROFFSET is an offset (luminance compressed data address relative to the header information address) register (non-instant register). This register is valid only when the decompression function is enabled.

Offset Address	Register Name	Total Reset Value
0x1640	V1_LADDROFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	laddr_offset																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	laddr_offset	Offset of the luminance compressed data address relative to the header information address

V1_CADDROFFSET

V1_CADDROFFSET is an offset (chrominance compressed data address relative to the header information address) register (non-instant register). This register is valid only when the decompression function is enabled.

Offset Address	Register Name	Total Reset Value
0x1644	V1_CADDROFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	caddr_offset																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	caddr_offset	Offset of the chrominance compressed data address relative to the header information address

V1_DCMP_LSTATE0

V1_DCMP_LSTATE0 is decompression status register 0 for the V1 luminance channel.

Offset Address	Register Name	Total Reset Value
0x1720	V1_DCMP_LSTATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_l_state0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dcmp_l_state0	Decompression status register 0 for the V1 luminance channel

V1_DCMP_LSTATE1

V1_DCMP_LSTATE1 is decompression status register 1 for the V1 luminance channel.

Offset Address	Register Name	Total Reset Value
0x1724	V1_DCMP_LSTATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_l_state1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dcmp_l_state1	Decompression status register 1 for the V1 luminance channel

V1_DCMP_CSTATE0

V1_DCMP_CSTATE0 is decompression status register 0 for the V1 chrominance channel.

Offset Address	Register Name	Total Reset Value
0x1728	V1_DCMP_CSTATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_c_state0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dcmp_c_state0	Decompression status register 0 for the V1 chrominance channel

V1_DCMP_CSTATE1

V1_DCMP_CSTATE1 is decompression status register 1 for the V1 chrominance channel.

Offset Address	Register Name	Total Reset Value
0x172C	V1_DCMP_CSTATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_c_state1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dcmp_c_state1	Decompression status register 1 for the V1 chrominance channel

V1_DCMPERRCLR

V1_DCMPERRCLR is a V1 decompression error status clear register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x1730	V1_DCMPERRCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dcmp_c_errclr	dcmp_1_errclr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[1]	WC	dcmp_c_errclr	Decompression error status clear for the chrominance channel 0: not cleared 1: cleared
[0]	WC	dcmp_l_errclr	Decompression error status clear for the luminance channel 0: not cleared 1: cleared

V1_DCMP_ERR

V1_DCMP_ERR is a V1 decompression error signal register.

Offset Address	Register Name	Total Reset Value
0x1734	V1_DCMP_ERR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								dcmp_c_wrong	dcmp_l_wrong
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	dcmp_c_wrong	Decompression error signal for the chrominance channel 0: No decompression error occurs. 1: A decompression error occurs.
[0]	RO	dcmp_l_wrong	Decompression error signal for the luminance channel 0: No decompression error occurs. 1: A decompression error occurs.

G2_CTRL

G2_CTR is a G2 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7000	G2_CTRL	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	nosec_flag	reserved		upd_mode	read_mode	reserved				precharge_en	precharge_mode	reserved										bitext		ifmt							
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant) 0: disabled 1: enabled
[30]	RW	nosec_flag	Operation security attribute flag for the bus interface 0: security attribute 1: non-security attribute
[29:28]	RO	reserved	Reserved
[27]	RW	upd_mode	Update mode 0: update by fame 1: update by field
[26]	RW	read_mode	Data read mode 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25:22]	RO	reserved	Reserved
[21]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[20]	RW	precharge_mode	Pre-charge mode of the FDR FIFO 0: hardware mode. Hardware automatically enters the pre-charge status on the frame trailer. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[19:10]	RO	reserved	Reserved

[9:8]	RW	bitext	Bit extend mode of the input bitmap 00: extend 0s to lower bits 10: extend the value of the MSB to a lower bit 11: extend the values of upper bits to lower bits
[7:0]	RW	ifmt	Format of the input data 0x48: ARGB4444 0x49: ARGB1555 Other values: reserved

G2_UPD

G2_UPD is a G2 update enable register.

Offset Address	Register Name	Total Reset Value
0x7004	G2_UPD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								regup
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

G2_ADDR

G2_ADDR is a G2 address register. When the horizontal pixel offsets, the address is calculated by following the description of G2_SFPOS.

Offset Address	Register Name	Total Reset Value
0x7010	G2_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address for the surface frame buffer

G2_STRIDE

G2_STRIDE is a G2 stride register.

Offset Address	Register Name	Total Reset Value
0x701C	G2_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	surface_stride	Frame buffer stride

G2_IRESO

G2_IRESO is a G2 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7020	G2_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ih	Height (in line). The configured value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.

[11:0]	RW	iw	Width (in pixel). The configured value is the actual width minus 1. Note: The actual layer width must be an even number.

G2_SFPOS

G2_SFPOS is a G2 surface read data start position (in the source bitmap) register (non-instant register)

If the read position is not 128-bit-word-aligned, this register indicates the number of pixels required for completing a 128-bit word. Note: The start position offset must be less than or equal to a 128-bit word. The exceeded part is expressed by an address.

The details are as follows:

The following assumes that the start address for the graphics layer of the source image is addr_ori, the address configured for the logical physical layer is addr_offset, the graphics layer offset is offsetp pixels, and the data format of the graphics layer is bpp (for example, the bpp for ARGB8888 is 32). The offset is calculated as follows:

G2ADDR = addr_offset = addr_ori + int (offsetp x bpp/128)

G2SFPOS = offset%128

where int means the rounding operation, and % means the modulo operation.

Offset Address	Register Name	Total Reset Value
0x7024	G2_SFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								src_xfpos							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RW	src_xfpos	Start horizontal coordinate of the source image. The value 0 indicates the first pixel of a line.

G2_CBMPARA

G2_CBMPARA is a G2 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7030	G2_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_mode	key_en	premult_en	palpha_en	reserved				galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	key_mode	Color key mode 0: The color is regarded as the color key when the following condition is met: Keymin ≤ Pixel ≤ Keymax 1: The color is regarded as the color key when either of the following conditions is met: Pixel ≤ Keymin or Pixel ≥ Keymax
[14]	RW	key_en	Color key enable 0: disabled 1: enabled
[13]	RW	premult_en	Whether the input bitmap is a premultiplied bitmap 0: non-premultiplied bitmap 1: premultiplied bitmap
[12]	RW	palpha_en	Pixel alpha enable 0: disabled 1: enabled
[11:8]	RO	reserved	Reserved
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates completely transparent.

G2_CKEYMAX

G2_CKEYMAX is a maximum color key value register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7034	G2_CKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of the color key R component
[15:8]	RW	keyg_max	Maximum value of the color key G component
[7:0]	RW	keyb_max	Maximum value of the color key B component

G2_CKEYMIN

G2_CKEYMIN is a minimum color key value register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x7038	G2_CKEYMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va1								keyr_min								keyg_min								keyb_min							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of the color key R component
[15:8]	RW	keyg_min	Minimum value of the color key G component
[7:0]	RW	keyb_min	Minimum value of the color key B component

G2_CMASK

G2_CMASK is a color key mask register (non-instant register).

The value 1 indicates that a pixel bit is retained during color key comparison; the value 0 indicates that a pixel bit is forcibly set to 0 during color comparison no matter whether the bit is 0 or 1.

Offset Address	Register Name	Total Reset Value
0x703C	G2_CMASK	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		kmsk_r		kmsk_g		kmsk_b	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	kmsk_r	R component of the masked color key
[15:8]	RW	kmsk_g	G component of the masked color key
[7:0]	RW	kmsk_b	B component of the masked color key

G2_DFPOS

G2_DFPOS is a G2 surface start position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x7080	G2_DFPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		disp_yfpos			disp_xfpos		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_yfpos	Column start coordinates
[11:0]	RW	disp_xfpos	Row start coordinates

G2_DLPOS

G2_DLPOS is a G2 surface end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x7084	G2_DLPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		disp_ylpos			disp_xlpos		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_ylpos	Column end coordinates
[11:0]	RW	disp_xlpos	Row end coordinates

G2_CSC_IDC

G2_CSC_IDC is a G2 CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x70C0	G2_CSC_IDC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	csc_mode	csc_en	cscidc1		cscidc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:23]	RW	csc_mode	This field is valid only when the G2 CSC coefficients are fixed. 000: reserved 001: YUV2YUV 010: YUV601_RGB 011: YUV709_RGB 100: YUV2YUV_709_601 101: YUV2YUV_601_709 110: RGB2YUV_601 111: RGB2YUV_709
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled
[21:11]	RO	cscidc1	DC parameter of the input U/G component. The MSB is the signed bit. The value is expressed as a two's complement.

[10:0]	RO	cscidc0	DC parameter of the input V/B component. The MSB is the signed bit. The value is expressed as a two's complement.

G2_CSC_ODC

G2_CSC_ODC is a G2 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x70C4	G2_CSC_ODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_sign_mode	cscodc1		cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RO	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RO	cscodc1	DC parameter of the output U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RO	cscodc0	DC parameter of the output Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

G2_CSC_IODC

G2_CSC_IODC is a G2 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x70C8	G2_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2		cscidc2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved

[21:11]	RO	cscodc2	DC parameter of the output V/B component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RO	cscidc2	DC parameter of the input Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

G2_CSC_P0

G2_CSC_P0 is a G2 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70CC	G2_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp01															reserved	cscp00														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RO	cscp01	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RO	cscp00	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P1

G2_CSC_P1 is a G2 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D0	G2_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RO	cscp10	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RO	cscp02	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P2

G2_CSC_P2 is a G2 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D4	G2_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RO	cscp12	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RO	cscp11	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P3

G2_CSC_P3 is a G2 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70D8	G2_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RO	cscp21	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RO	cscp20	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

G2_CSC_P4

G2_CSC_P4 is a G2 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x70DC	G2_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RO	cscp22	5.10 data format that consists of a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

CBM_BKG2

CBM_BKG2 is a CBM mixer 2 overlay background color register.

Offset Address	Register Name	Total Reset Value
0xB420	CBM_BKG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cbm_bkgy2								cbm_bkgcb2								cbm_bkgcr2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	cbm_bkgy2	Overlay background color of CBM mixer 2, Y component
[19:10]	RW	cbm_bkgcb2	Overlay background color of CBM mixer 2, Cb component
[9:0]	RW	cbm_bkgcr2	Overlay background color of CBM mixer 2, Cr component

CBM_MIX2

CBM_MIX2 is a CBM mixer 2 priority configuration register (instant register). The register configuration takes effect only when the VS signal is valid. mixer_prio_x is overly layer priority *x*.

Offset Address	Register Name	Total Reset Value
0xB428	CBM_MIX2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	mixer_prio1	Drive layer of CBM mixer 2 with priority 1 0x0: no drive layer 0x9: V1 0xA: G2 Other values: reserved
[3:0]	RW	mixer_prio0	Drive layer of CBM mixer 2 with priority 0 0x0: no drive layer 0x9: V1 0xA: G2 Other values: reserved

DHD1_CTRL

DHD1_CTRL is a DHD1 global control register. You must configure all bits of this register before configuring DHD1_CTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xC400	DHD1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	cbar_en	cbar_sel	reserved																		precharge_en	precharge_mode	reserved				iop	reserved			regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant). Data is output over the interface only when this field is enabled. 0: disabled 1: enabled
[30]	RW	cbar_en	Color bar enable. The color bar is output over the interface when this field is enabled. 0: disabled 1: enabled
[29]	RW	cbar_sel	Color space select for the output color bar (instant) 0: VGA 1: YPbPr
[28:11]	RO	reserved	Reserved.
[10]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[9]	RW	precharge_mode	Pre-charge mode of AFIFO 0: hardware mode. Hardware automatically enters the pre-charge status in the vertical blanking region. 1: software mode. Software controls whether to enter or exit the pre-charge status.
[8:5]	RO	reserved	Reserved

[4]	RW	iop	Display mode (non-instant) 0: interlaced display 1: progressive display
[3:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

DHD1_VSYNC

DHD1_VSYNC is a top field VS timing register in interlaced output mode or frame VS timing register in progressive output mode. This register is a non-instant register.

Offset Address	Register Name	Total Reset Value
0xC404	DHD1_VSYNC	0x0011_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	vfb	In interlaced output mode: top vertical front blanking (TVFB) In progressive output mode: vertical front blanking (VFB)
[19:12]	RW	vbb	In interlaced output mode: top vertical back blanking (TVBB) In progressive output mode: vertical back blanking (VBB)+vertical pulse width (VPW)
[11:0]	RW	vact	In interlaced output mode: height of an active image on the top field In progressive output mode: height of an active image in a frame. The configured value is the actual value minus 1.

DHD1_HSYNC1

DHD1_HSYNC1 is an HS configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC408	DHD1_HSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal back blanking (HBB), in pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region

DHD1_HSYNC2

DHD1_HSYNC2 is an HS configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC40C	DHD1_HSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hmid	Bottom VS active pixel (active region)
[15:0]	RW	hfb	HFB, in pixel

DHD1_VPLUS

DHD1_VPLUS is a bottom field VS timing in interlaced output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC410	DHD1_VPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	bvfb	Bottom vertical front blanking (BVFB) in interlaced output mode
[19:12]	RW	bvbb	Bottom vertical back blanking (BVBB)+VPW in interlaced output

			mode
[11:0]	RW	bvact	Height of an active image in the bottom field in interlaced output mode The configured value is the actual value minus 1.

DHD1_PWR

DHD1_PWR is a sync signal pulse width register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC414	DHD1_PWR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		vpw		hpw			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	vpw	VPW. The configured value is the actual value minus 1.
[15:0]	RW	hpw	Horizontal pulse width (HPW). The configured value is the actual value minus 1.

DHD1_VTTHD3

DHD1_VTTHD3 is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xC418	DHD1_VTTHD3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd4_mode	reserved			vtmgthd4												thd3_mode	reserved			vtmgthd3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	thd4_mode	Mode of generating threshold 4 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.

[30:29]	RO	reserved	Reserved
[28:16]	RW	vtmgthd4	Vertical timing threshold 4 for simultaneously triggering DHD and DSD. The start time of the DSD interface timing is later than that of the DHD interface timing and is equal to the number of lines configured in vtmgthd4.
[15]	RW	thd3_mode	Mode of generating threshold 3 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[14:13]	RO	reserved	Reserved
[12:0]	RW	vtmgthd3	Vertical timing threshold 3. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd3_int] interrupt is triggered.

DHD1_VTTHD

DHD1_VTTHD is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xC41C	DHD1_VTTHD	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd2_mode	reserved			vtmgthd2												thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	thd2_mode	Mode of generating threshold 2 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[30:29]	RO	reserved	Reserved
[28:16]	RW	vtmgthd2	Vertical timing threshold 2. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd2_int] interrupt is triggered.
[15]	RW	thd1_mode	Mode of generating threshold 1 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.

[14:13]	RO	reserved	Reserved
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHD1_PARATHD

DHD1_PARATHDis a PARA coefficient update point threshold register.

Offset Address	Register Name	Total Reset Value
0xC4B0	DHD1_PARATHD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_en	reserved																							para_thd								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dfs_en	DFS enable 0: disabled 1: enabled
[30:6]	RW	reserved	Reserved
[5:0]	RW	para_thd	PARA coefficient update point threshold. It indicates the line after the vertical back blanking where the update point occurs. This field is valid only after DFS is enabled.

DHD1_START_POS

DHD1_START_POS is a DHD1 start signal start position register.

Offset Address	Register Name	Total Reset Value
0xC4C0	DHD1_START_POS	0x0000_0805

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																timing_start_pos								start_pos							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:8]	RW	timing_start_pos	Number of lines before the active region where the timing_gen state machine starts to work

[7:0]	RW	start_pos	Number of lines before the active region where the start signal is generated in online mode

DHD1_STATE

DHD1_STATE is a DHD1 status register.

Offset Address	Register Name	Total Reset Value
0xC4F0	DHD1_STATE	0x0000_0006

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved		count_int		vcnt				bottom_field	vblank	vback_blank
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RO	count_int	DHD1 interrupt count. The count value is increased by 1 each time a vertical timing interrupt is reported.
[15:3]	RO	vcnt	Active display line count of DHD1
[2]	RO	bottom_field	DHD1 top/bottom field indicator 0: top field 1: bottom field
[1]	RO	vblank	DHD1 blanking region indicator 0: active region 1: blanking region
[0]	RO	vback_blank	DHD1 back blanking region indicator 0: non-back blanking region 1: blanking region

BT_CTRL

BT_CTRL is a BT.656/BT.1120 control register.

Offset Address	Register Name	Total Reset Value
0xD200	BT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		bt1120_bypass		reserved				yc_mode				reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	bt1120_bypass	BT.1120 bypass mode 0: disabled 1: enabled
[29:25]	RO	reserved	Reserved
[24]	RW	yc_mode	BT.1120 Y/C exchange 0: Y for upper bits and C for lower bits 1: Y for lower bits and C for upper bits
[23:0]	RO	reserved	Reserved

BT_CLIP0_L

BT_CLIP0_L is a BT.656/BT.1120 clip lowest threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xD210	BT_CLIP0_L	0x0100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_cl2								clip_cl1								clip_cl0											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_cl2	Lowest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_cl1	Lowest threshold Cb/G of component 1, unsigned integer

[9:0]	RW	clip_cl0	Lowest threshold Cr/B of component 0, unsigned integer

BT_CLIP0_H

BT_CLIP0_H is a BT.656/BT.1120 clip highest threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xD214	BT_CLIP0_H	0x0EB3_C0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_ch2												clip_ch1								clip_ch0							
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_ch2	Highest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_ch1	Highest threshold Cb/G of component 1, unsigned integer
[9:0]	RW	clip_ch0	Highest threshold Cr/B of component 0, unsigned integer

BT_DITHER0_CTRL

BT_DITHER0_CTRL is a BT.656/BT.1120 dither control register.

Offset Address	Register Name	Total Reset Value
0xD280	BT_DITHER0_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md				reserved																											
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select 000: 12-bit inputs, 10-bit outputs, no dithering, and direct bit truncation 001: 12-bit inputs, 10-bit outputs, and time-domain dithering 010: 12-bit inputs, 10-bit outputs, and spatial-domain dithering 011: 12-bit inputs, 8-bit outputs, and time-domain and spatial-domain dithering 100: 12-bit inputs, 10-bit outputs, and round off 101: 12-bit inputs, 8-bit outputs, and round off Other values: reserved
[28:0]	RO	reserved	Reserved

BT_DITHER0_COEF0

BT_DITHER0_COEF0 is a BT.656/BT.1120 dither coefficient 0 register.

Offset Address	Register Name	Total Reset Value
0xD284	BT_DITHER0_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 for time-domain dithering
[23:16]	RW	dither_coef2	Coefficient 2 for time-domain dithering
[15:8]	RW	dither_coef1	Coefficient 1 for time-domain dithering
[7:0]	RW	dither_coef0	Coefficient 0 for time-domain dithering

BT_DITHER0_COEF1

BT_DITHER0_COEF1 is a BT.656/BT.1120 dither coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xD288	BT_DITHER0_COEF1	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef7								dither_coef6								dither_coef5								dither_coef4							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 for time-domain dithering
[23:16]	RW	dither_coef6	Coefficient 6 for time-domain dithering
[15:8]	RW	dither_coef5	Coefficient 5 for time-domain dithering
[7:0]	RW	dither_coef4	Coefficient 4 for time-domain dithering

LCD_CTRL

LCD_CTRL is an LCD control register.

Offset Address	Register Name	Total Reset Value
0xD400	LCD_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	reserved	lcd_serial_mode	lcd_serial_perd	lcd_parallel_order	lcd_data_inv	lcd_parallel_mode	reserved	reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RO	reserved	Reserved
[29]	RW	lcd_serial_mode	LCD mode 0: parallel mode 1: serial mode

[28]	RW	lcd_serial_perd	Number of output single-pixel clock cycles in serial LCD mode 0: 3 1: 4
[27]	RW	lcd_parallel_order	LCD parallel output sequence 0: RGB 1: BGR
[26]	RW	lcd_data_inv	Inversion of the LCD output bits 0: Bits 15−0 or bits 23−0 are from upper bits to lower bits. 1: Bits 0−15 or bits 0−23 are from upper bits to lower bits.
[25]	RW	lcd_parallel_mode	Bit width mode of the LCD parallel output 0: RGB565 1: RGB888
[24]	RO	reserved	Reserved
[23:0]	RO	reserved	Reserved

LCD_SYNC_INV

LCD_SYNC_INV is a sync signal polarity configuration register in LCD external sync timing input mode. The setting of this register takes effect immediately after configuration, that is, the polarity of the corresponding sync signal is immediately affected.

Offset Address	Register Name	Total Reset Value
0xD408	LCD_SYNC_INV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												f_inv	vs_inv	hs_inv	dv_inv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	f_inv	Output phase inversion enable for the odd/even field indicator signal (instant) 0: disabled 1: enabled
[2]	RW	vs_inv	Output phase inversion enable for the VS pulse (instant) 0: disabled 1: enabled

[1]	RW	hs_inv	Output phase inversion enable for the HS pulse (instant) 0: disabled 1: enabled
[0]	RW	dv_inv	Output phase inversion enable for the data validity signal (instant) 0: disabled 1: enabled

DATE_COEFF0

DATE_COEFF0 is a standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xF200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved	pal_half_en	pbpr_lpf_en	scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel		sync_mode_sel				sync_mode_scart	length_sel	agc_amp_sel	luma_dl				reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth of the chrominance low-pass filter 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL standards, the black level is 7.5 IRE higher than the blanking level; for other standards, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28]	RO	reserved	Reserved
[27]	RW	pal_half_en	PAL half line reduction enable 0: disabled 1: enabled

[26]	RW	pbpr_lpf_en	Component chrominance low-pass filtering enable 0: disabled 1: enabled
[25]	RW	scanline	Number of scanned lines in each frame based on standards. For the (M) NTSC, NTSC-J, and (M) PAL standards, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL standards, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame
[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable 0: no filtering 1: filtering
[22]	RW	fm_sel	FMSECAM frequency modulation select 0: SIN mode 1: COS mode
[21:18]	RW	style_sel	CVBS/S-Video output signal standard when this bit works with the scanline bit When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (M) NTSC standard 0x2: NTSC-J standard 0x4: (M) PAL standard When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (B, D, G, H, I) PAL standard 0x2: (N) PAL standard 0x4: (Nc) PAL standard 0x8: SECAM standard Other values: reserved

[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals during component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output or G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when intf_sel is set to 100 and rgb_en is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control for the components of three channels 0: Component sync output is configured based on sync_mode_sel bit[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.
[14]	RW	length_sel	Active width of each video line (in pixel) 0: output according to the line active pixel width in BT.601 mode. 1: output according to the line active pixel width in BT.470 mode When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line standard or 712 pixels for the 525-line standard. Currently, the BT.601 mode and BT.470 mode cannot be dynamically switched. You can change the mode only after reset. The BT.601 mode is recommended, and this mode is the default mode after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on the off-chip configuration. DATE_COEFF1[amp_outside]

[12:9]	RW	luma_dl	Lead or lag-behind offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luminance signal. 1: The chrominance signal leads the luminance signal. bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001−111: The chrominance signal leads or lags behind the luminance signal by one to seven units.
[8]	RO	reserved	Reserved
[7:6]	RW	oversam_en	Level-1 over-sampling enable. Both luminance over-sampling and chrominance over-sampling are controlled. bit[7]: luminance over-sampling enable 0: disabled 1: enabled bit[6]: chrominance over-sampling enable 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 over-sampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable 0: disabled 1: enabled
[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE_COEFF1

DATE_COEFF1 is an amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xF204	DATE_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode				dac_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude
[28]	RW	cvbs_limit_en	CVBS amplitude limit control 0: not limited 1: limited
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the video programming system (VPS) data 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the copy generation management system (CGMS) data 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data 0: from upper bits to lower bits 1: from lower bits to upper bits
[23]	RW	c_limit_en	Chrominance amplitude limit control 0: not limited 1: limited
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC

[12]	RW	date_test_en	Test valid signal
[11:10]	RW	date_test_mode	Test mode signal
[9:0]	RW	dac_test	DAC test value input

DATE_COEFF2

DATE_COEFF2 is a DATE coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF208	DATE_COEFF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef02																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef02	DATE coefficient 2 register

DATE_COEFF3

DATE_COEFF3 is a DATE coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF20C	DATE_COEFF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef03																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RW	coef03	DATE coefficient 3 register

DATE_COEFF4

DATE_COEFF4 is a DATE coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF210	DATE_COEFF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef04																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RW	coef04	DATE coefficient 4 register

DATE_COEFF5

DATE_COEFF5 is a DATE coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF214	DATE_COEFF5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef05																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:0]	RW	coef05	DATE coefficient 5 register

DATE_COEFF6

DATE_COEFF6 is a DATE coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF218	DATE_COEFF6	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef06_0	reserved															coef06_1															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	coef06_0	DATE coefficient 6 register 0
[30:23]	RO	reserved	Reserved
[22:0]	RW	coef06_1	DATE coefficient 6 register 1

DATE_COEFF21

DATE_COEFF21 is an output matrix control register.

Offset Address	Register Name	Total Reset Value
0xF254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dac0_in_sel	
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	dac0_in_sel	DAC0 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE_COEFF22

DATE_COEFF22 is a DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xF258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								video_phase_delta							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	video_phase_delta	DTO initial phase

DATE_COEFF23

DATE_COEFF23 is a VIDEO_OUT delay configuration register.

Offset Address	Register Name	Total Reset Value
0xF25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dac0_out_dly	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	dac0_out_dly	DAC0 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.

DATE_COEFF24

DATE_COEFF24 is a color burst start position register.

Offset Address	Register Name	Total Reset Value
0xF260	DATE_COEFF24	0x0001_2C99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:0]	RW	burst_start	Color burst start position

DATE_ISRMASK

DATE_ISRMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xF280	DATE_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	tt_mask	Teletext interrupt mask 0: enabled 1: masked

DATE_ISRSTATE

DATE_ISRSTATE is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0xF284	DATE_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	tt_status	Teletext interrupt status After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears the interrupt.

DATE_ISR

DATE_ISR is an interrupt register.

Offset Address	Register Name	Total Reset Value
0xF288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	tt_int	Teletext interrupt. It shows the interrupt status after tt_status is masked by tt_mask.

DATE_COEFF37

DATE_COEFF37 is an up-sampling filtering coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF294	DATE_COEFF37	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y1_coeff3								fir_y1_coeff2								fir_y1_coeff1								fir_y1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_y1_coeff3	Coefficient 13 for luminance up-sampling and filtering
[23:16]	RW	fir_y1_coeff2	Coefficient 12 for luminance up-sampling and filtering
[15:8]	RW	fir_y1_coeff1	Coefficient 11 for luminance up-sampling and filtering
[7:0]	RW	fir_y1_coeff0	Coefficient 10 for luminance up-sampling and filtering

DATE_COEFF38

DATE_COEFF38 is an up-sampling filtering coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF298	DATE_COEFF38	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff1																fir_y2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff1	Coefficient 21 for luminance up-sampling and filtering
[15:0]	RW	fir_y2_coeff0	Coefficient 20 for luminance up-sampling and filtering

DATE_COEFF39

DATE_COEFF39 is an up-sampling filtering coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF29C	DATE_COEFF39	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff3																fir_y2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff3	Coefficient 23 for luminance up-sampling and filtering
[15:0]	RW	fir_y2_coeff2	Coefficient 22 for luminance up-sampling and filtering

DATE_COEFF40

DATE_COEFF40 is an up-sampling filtering coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c1_coeff3								fir_c1_coeff2								fir_c1_coeff1								fir_c1_coeff0							

Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_c1_coeff3	Coefficient 13 for chrominance up-sampling and filtering
[23:16]	RW	fir_c1_coeff2	Coefficient 12 for chrominance up-sampling and filtering
[15:8]	RW	fir_c1_coeff1	Coefficient 11 for chrominance up-sampling and filtering
[7:0]	RW	fir_c1_coeff0	Coefficient 10 for chrominance up-sampling and filtering

DATE_COEFF41

DATE_COEFF41 is an up-sampling filtering coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2A4	DATE_COEFF41	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff1																fir_c2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff1	Coefficient 21 for chrominance up-sampling and filtering
[15:0]	RW	fir_c2_coeff0	Coefficient 20 for chrominance up-sampling and filtering

DATE_COEFF42

DATE_COEFF42 is an up-sampling filtering coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2A8	DATE_COEFF42	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff3																fir_c2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff3	Coefficient 23 for chrominance up-sampling and filtering
[15:0]	RW	fir_c2_coeff2	Coefficient 22 for chrominance up-sampling and filtering

DATE_DACDET1

DATE_DACDET1 is DAC automatic detection register 1.

Offset Address	Register Name	Total Reset Value
0xF2C0	DATE_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_line								reserved								vdac_det_high							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	det_line	Line of the detected level
[15:10]	RO	reserved	Reserved
[9:0]	RW	vdac_det_high	Detected level

DATE_DACDET2

DATE_DACDET2 is DAC automatic detection register 2.

Offset Address	Register Name	Total Reset Value
0xF2C4	DATE_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved											det_pixel_wid				reserved								det_pixel_sta							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC automatic detection enable 0: disabled 1: enabled
[30:27]	RO	reserved	Reserved
[26:16]	RW	det_pixel_wid	Level width
[15:11]	RO	reserved	Reserved
[10:0]	RW	det_pixel_sta	Start position of a line

DATE_COEFF50

DATE_COEFF50 is an over-sampling filtering coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF2C8	DATE_COEFF50	0x07FF_07FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 11 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 10 for luminance over-sampling and filtering

DATE_COEFF51

DATE_COEFF51 is an over-sampling filtering coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF2CC	DATE_COEFF51	0x07FF_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 21 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 20 for luminance over-sampling and filtering

DATE_COEFF52

DATE_COEFF52 is an over-sampling filtering coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF2D0	DATE_COEFF52	0x0000_07FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 31 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 30 for luminance over-sampling and filtering

DATE_COEFF53

DATE_COEFF53 is an over-sampling filtering coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2D4	DATE_COEFF53	0x07BF_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 41 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 40 for luminance over-sampling and filtering

DATE_COEFF54

DATE_COEFF54 is an over-sampling filtering coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2D8	DATE_COEFF54	0x0135_0135

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											

Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 51 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 50 for luminance over-sampling and filtering

DATE_COEFF55

DATE_COEFF55 is an over-sampling filtering coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2DC	DATE_COEFF55	0x000C_07BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 61 for luminance over-sampling and filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 60 for luminance over-sampling and filtering

DATE_COEFF56

DATE_COEFF56 is an over-sampling round-off register.

Offset Address	Register Name	Total Reset Value
0xF2E0	DATE_COEFF56	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															oversam2_round_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	oversam2_round_en	Round-off enable during 2x up-sampling 0: disabled 1: enabled

DATE_COEFF57

DATE_COEFF57 is a CVBS gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E4	DATE_COEFF57	0x0080_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cvbs_gain_en	reserved							ycvbs_gain								u_gain								v_gain							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cvbs_gain_en	CVBS gain enable 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved
[23:16]	RW	ycvbs_gain	Gain control of the luminance component Y
[15:8]	RW	u_gain	Gain control of the chrominance component U

[7:0]	RW	v_gain	Gain control of the chrominance component V

DATE_COEFF58

DATE_COEFF58 is a component gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E8	DATE_COEFF58	0x0080_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	comp_gain_en	reserved							ycomp_gain								pb_gain								pr_gain							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	comp_gain_en	Component gain enable 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved
[23:16]	RW	ycomp_gain	Gain control of the luminance component Y
[15:8]	RW	pb_gain	Gain control of the chrominance component U
[7:0]	RW	pr_gain	Gain control of the chrominance component V

DATE_COEFF59

DATE_COEFF59 is a clip control bit register.

Offset Address	Register Name	Total Reset Value
0xF2EC	DATE_COEFF59	0x0001_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															cb_gain_polar	reserved		cr_os_clip_fullrange	cb_os_clip_fullrange	reserved		v_os_clip_fullrange	u_os_clip_fullrange	reserved			y_os_clip_fullrange	reserved		clpf_clip_fullrange	ynotch_clip_fullrange
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	cb_gain_polar	Chrominance subcarrier polarity control 0: negative gain 1: positive gain
[15:14]	RO	reserved	Reserved
[13]	RW	cr_os_clip_fullrange	Cr component clip enable on the up-sampling module 0: disabled 1: enabled
[12]	RW	cb_os_clip_fullrange	Cb component clip enable on the up-sampling module 0: disabled 1: enabled
[11:10]	RO	reserved	Reserved
[9]	RW	v_os_clip_fullrange	V component clip enable on the up-sampling module 0: disabled 1: enabled
[8]	RW	u_os_clip_fullrange	U component clip enable on the up-sampling module 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	y_os_clip_fullrange	Y component clip enable on the up-sampling module 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved

[1]	RW	clpf_clip_fullrange	Chrominance low-pass module clip enable 0: disabled 1: enabled
[0]	RW	ynotch_clip_fullrange	Luminance notch module clip enable. 0: disabled 1: enabled

9.3 MIPI RX

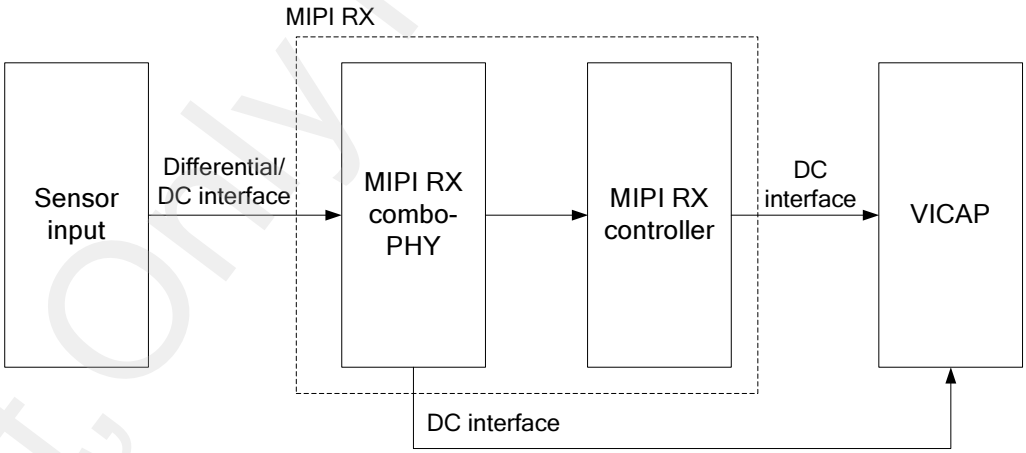
9.3.1 Overview

The MIPI RX receives LVDSs that carry raw video data (Bayer RGB data), converts the signals into the digital camera (DC) timing, and transfers it to the downstream VICAP module.

The MIPI RX supports serial video signal inputs such as the MIPI D-PHY, LVDS, and HiSPI. The serial video interfaces provide more bandwidth to enhance transmission stability. The MIPI RX is also compatible with the DC video interface, supports the 3.3 V/1.8 V DC parallel input, and requires a less number of chip pins while providing better compatibility.

The MIPI RX consists of the combo-PHY and controller. Figure 9-18 shows the MIPI RX workflow and its position in the system.

Figure 9-18 MIPI RX workflow and its position in the system



9.3.2 Features

The MIPI RX has the following features:

- MIPI D-PHY interface with at most eight lanes, up to 1.5 Gbit/s per lane
- LVDS/Sub-LVDS/HiSPI interface with at most 12 lanes, up to 1.5 Gbit/s per lane
- CMOS parallel 1.8 V/3.3 V input

- Raw8, raw10, raw12, raw14, or raw16 data parsing
- 4-frame WDR and multiple WDR timings
- Endian mode configuration for LVDS or HiSPI mode pixel or synchronization code
- Configuration of channel quantity and sequence

9.3.3 Function Description

9.3.3.1 Typical Applications

The MIPI RX is a collection unit that supports multiple differential video input interfaces. It is used for converting interface timings. It can receive data through the MIPI, LVDS, sub-LVDS, HiSPI, or DC interface. Depending on the function configuration, the MIPI RX allows data transmission at various rates and transmission of images in various resolutions, and supports multiple image sensors.

The MIPI RX supports at most 2-link/8-lane MIPI input and 3-link/12-lane LVDS/sub-LVDS/HiSPI input. Each link can use its own external input clock. Link 1 and link 2 can use the clock of link 0 by configuring the corresponding register. The input pins can be multiplexed to support single-ended DC or BT.1120 channel inputs, thereby providing better compatibility with fewer chip pins.

Table 9-7 lists the interfaces supported by the MIPI RX.

Table 9-7 Interfaces supported by the MIPI RX

Interface Type	Common Mode Voltage	Differential Mode Voltage	Maximum Clock Frequency	Maximum Data Rate per Lane
D-PHY	200 mV	200 mV	500 MHz	1.5 Gbit/s
Sub-LVDS	900 mV	150 mV	500 MHz	1.5 Gbit/s
LVDS	1.25 V	350 mV	500 MHz	1.5 Gbit/s
HiSPI (HiVCM)	900 mV	280 mV	500 MHz	1.5 Gbit/s
HiSPI (SLVS)	200 mV	200 mV	500 MHz	1.5 Gbit/s
CMOS parallel	1.8 V	1.8 V	150 MHz	150 Mbit/s
CMOS parallel	3.3 V	3.3 V	150 MHz	150 Mbit/s

The MIPI RX only converts the interface timings, and does not process image data formats. It supports any resolution and frame rate as long as the bandwidth requirement is met. The MIPI RX bandwidth is limited by the interface data rate and internal processing speed of the Combo PHY. The Combo PHY interface supports the maximum interface rate of 1.5 Gbit/s per lane and maximum internal processing speed of 600 megapixels/s.

NOTE

The maximum bandwidth supported by the Combo PHY interface is (1.5 Gbit/s x number of lanes). The maximum internal processing capability is (600 megapixels x pixel bit width). In the actual application, the maximum operating rate of the MIPI RX is limited by the smaller value between the maximum bandwidth and the maximum internal processing capability.

9.3.3.2 Function Implementation

Data Format of the MIPI Interface

MIPI specifications are developed and maintained by different working groups and cover diverse application requirements for use in different fields. The MIPI RX supports the D-PHY and CSI-2. D-PHY stipulates the rules of transmission at the physical layer, and CSI-2 stipulates the format and protocol of camera output data packets.

(1) D-PHY

D-PHY is a high-speed physical layer standard released by the MIPI Alliance. The standard stipulates the physical specifications and transmission protocols at the physical layer for hosts and peripherals. D-PHY uses the LVDS technology with 200 mV source synchronization. The data rate of each channel ranges from 80 Mbit/s to 1500 Mbit/s. D-PHY can work in either low-power (LP) or high-speed (HS) mode.

(2) CSI-2

CSI-2 is a camera data protocol that stipulates the data packet format used for communication between hosts and peripherals.

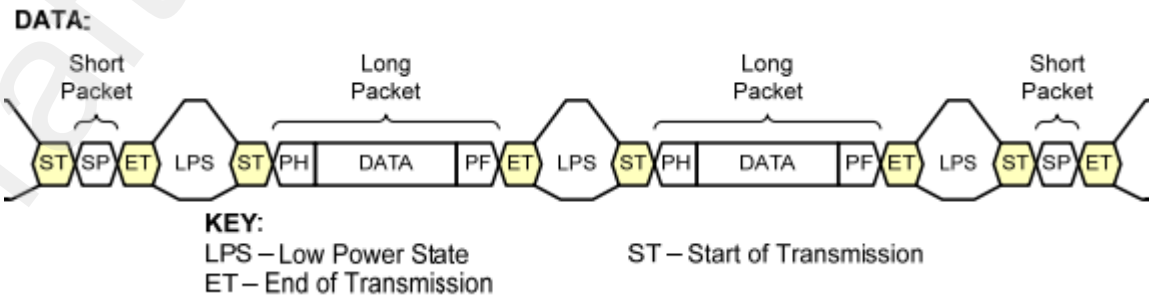
CSI-2 supports image application in different pixel formats, and the smallest unit for data transmission is byte. An appropriate number of data channels can be selected to attain enhanced CSI-2 performance. CSI-2 specifies how the TX end packetizes pixel data into bytes and how multiple data channels are allocated and managed. Byte data is organized in data packets, which are transmitted between the start of transmission (SoT) and the end of transmission (EoT). The RX end parses the data packets based on the applicable protocol and restores the pixel data.

The MIPI RX can parse pixel data in RAW8, RAW10, RAW12, RAW14 or RAW16 format.

CSI-2 data packets can be long or short and contain parity codes for parity check and error correction.

Both long and short packets are transmitted between the SoT and EoT. D-PHY works in LP mode in gaps of data transmission. Figure 9-19 shows the mechanism for transmitting CSI-2 data packets. PH and PF mean packet header and packet footer, respectively.

Figure 9-19 CSI-2 data packet transmission mechanism



Long packets are used to transmit effective pixel data in five parts: Data ID, Word Count, ECC, Payload, and Checksum.

Data ID comprises Virtual Channel and Data Type. Virtual Channel controls the channel used for transmission and can specify channel multiplexing so that different channels will transmit different data. Data Type specifies the type of data.

Word Count indicates the amount of data to be received by the RX end.

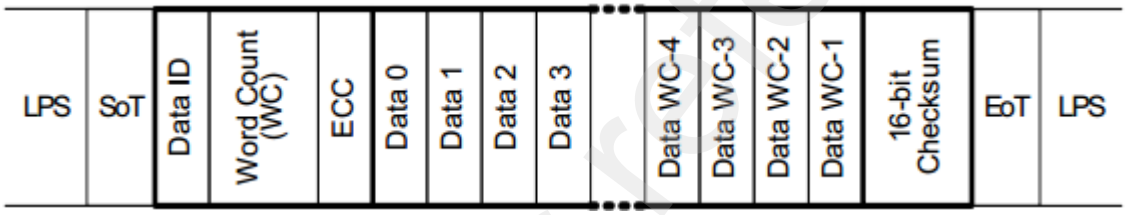
ECC is 8-bit error correction code that can be used to detect and correct errors in Data Type and Word Count.

Payload is the pixel data to be transmitted.

Checksum is generated by a linear feedback shift register and is used to check payload data.

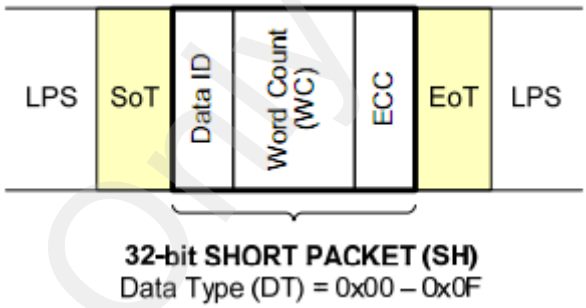
Figure 9-20 shows the format of a long packet.

Figure 9-20 CSI-2 long packet format



Short packets are used to transmit synchronization information in three parts: Data ID, Word Count, and ECC. Figure 9-21 shows its format.

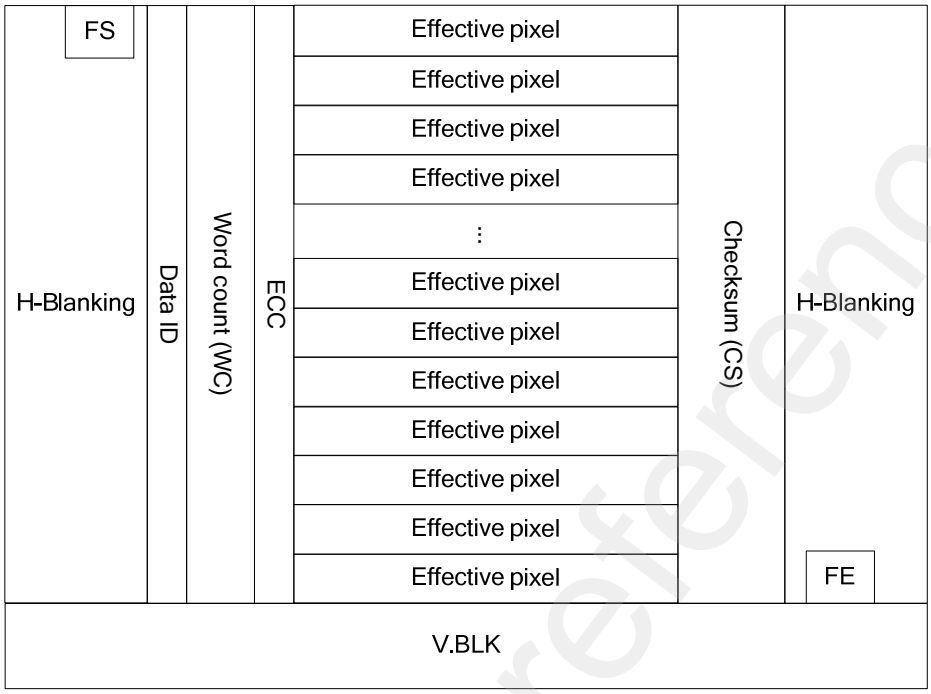
Figure 9-21 CSI-2 short packet format



Linear Mode of the MIPI Interface

Figure 9-22 shows the video transfer format in linear mode of the MIPI interface. FS indicates the start of the frame, and FE indicates the end of the frame. The 32-bit data packet in each line consists of the virtual channel and data type information of the current line.

Figure 9-22 Image data format of the MIPI interface



WDR Modes of the MIPI Interface

The MIPI RX supports three WDR modes of the MIPI interface.

- MIPI WDR mode 1: The virtual channel (VC) is used to distinguish the long exposure data and short exposure data.
- MIPI WDR mode 2: The data type (DT) is used to distinguish the long exposure data and short exposure data.
- MIPI WDR mode 3: Data is transferred in DOL WDR mode.

Figure 9-23 shows data transfer in WDR mode that uses the VC. The short FS and FE packets as well as long data packets contain the VC information. The MIPI RX controller detects the long/short exposure data based on the VC information in the short/long packet, adds a 2-bit signal flag to each line of data, and outputs the data, signal flag, and DC timing to the VICAP module, where demultiplexing is implemented.

Figure 9-23 Data transfer in WDR mode of the MIPI interface (the VC is used)

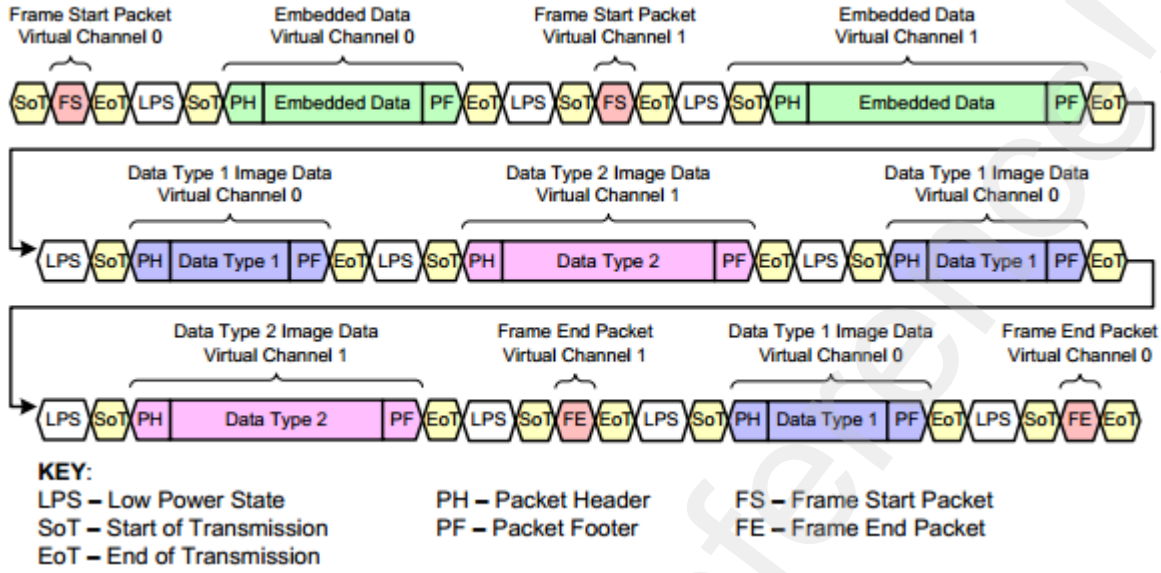


Figure 9-24 shows data transfer in WDR mode that uses the DT. The frame with different exposure lengths uses one group of short FS and FE packets. The header of the long packet contains the DT information. The bit width of the DT0 raw data may be different from that of the DT1 raw data. The MIPI RX controller distinguishes the long and short exposure data based on the DT information, adds a 2-bit signal flag to each line of data, and outputs the data, signal flag, and DC timing to the VICAP module, where demultiplexing is implemented.

Figure 9-24 Data transfer in WDR mode of the MIPI interface (the DT is used)

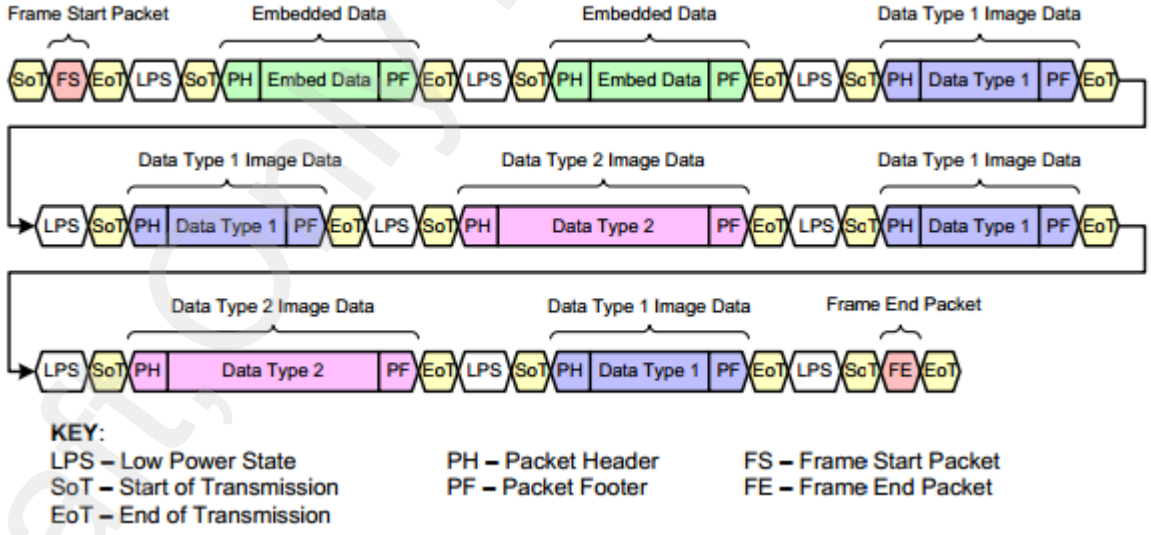
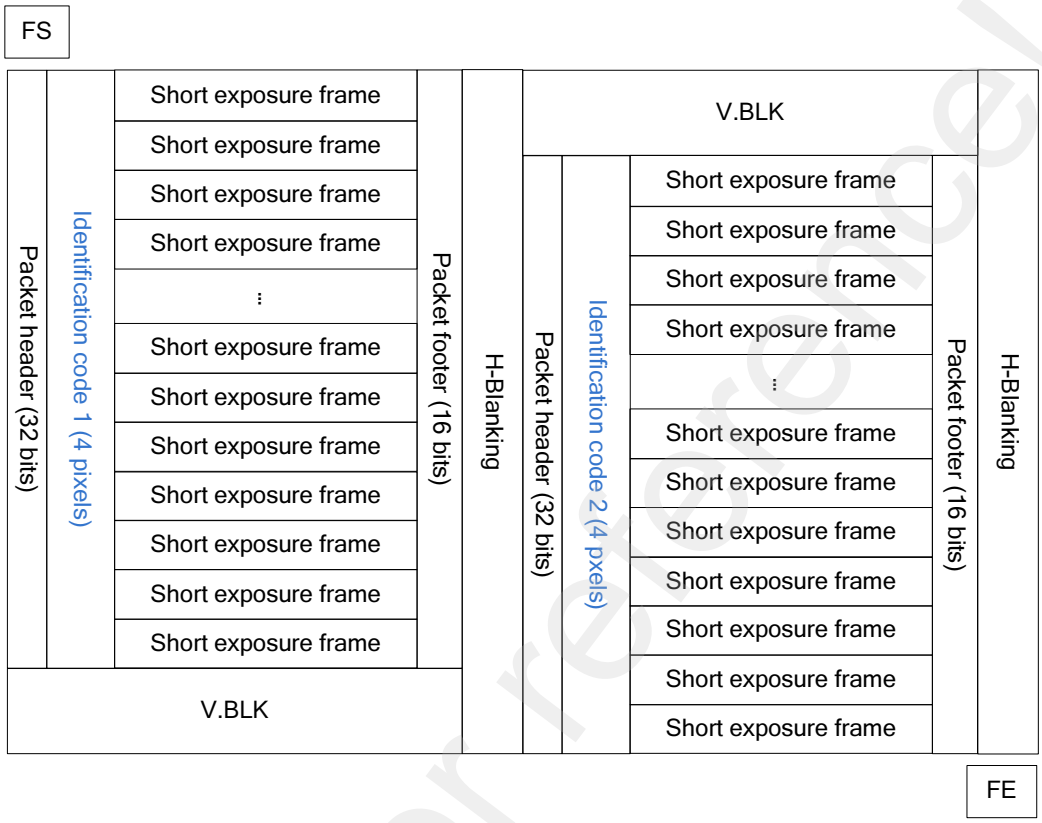


Figure 9-25 shows data transfer in DOL WDR mode of the MIPI interface. The long and short exposure data uses one group of short FS and FE packets. The first four pixels in each line are the identification codes for distinguishing the long exposure data and short exposure data.

Figure 9-25 Data transfer in DOL WDR mode of the MIPI interface



NOTE

The image sensor supports the frame interleaved WDR mode and line interleaved WDR mode. The timings and data formats for the two modes are the same. This section takes the line interleaved WDR mode as an example.

Input Data Format of the LVDS Interface

The LVDS is widely used in front-end cameras. It identifies data of the blanking region and active region by synchronization code.

NOTE

For the LVDS, there are only the electrical transfer specifications but no standard protocols on the timing and data format. The sub-LVDS is a differential signal technology with ultra-low voltage swing. The common mode/differential mode voltage of the sub-LVDS is lower than that of the LVDS. Compared with the LVDS, the sub-LVDS is more suitable for image sensor applications. The sub-LVDS can be considered as one type of LVDS. In the following sections, sub-LVDS is also called LVDS.

The Combo PHY interface of the MIPI RX converts the differential serial data into parallel data. Then the MIPI RX controller splits and combines the parallel data, extracts the synchronization code, and parses the pixel data.

In LVDS transmission mode, frame or line synchronization signals are integrated into data streams. In data streams, SOF and EOF indicate the start and end of a frame, whereas SOL and EOL indicate the start and end of a line. In a data stream, each of SOF, EOF, SOL, and EOL consists of four fields, and the bit width and pixel data of each field are consistent. The first three fields are fixed reference codes, and the fourth field is used to identify the start of end of a frame or line. Table 9-8 illustrates the LVDS synchronization code format.

Table 9-8 LVDS synchronization code format

Field	Bit Width	Synchronization Code			
		SOL/SAV (Valid Line)	EOL/EAV (Valid Line)	SOF/SAV (Invalid Line)	EOF/EAV (Invalid Line)
First code	8 bits	FFh	FFh	FFh	FFh
	10 bits	3FFh	3FFh	3FFh	3FFh
	12 bits	FFFh	FFFh	FFFh	FFFh
	14 bits	3FFFh	3FFFh	3FFFh	3FFFh
Second code	8 bits	00h	00h	00h	00h
	10 bits	000h	000h	000h	000h
	12 bits	000h	000h	000h	000h
	14 bits	0000h	0000h	0000h	0000h
Third code	8 bits	00h	00h	00h	00h
	10 bits	000h	000h	000h	000h
	12 bits	000h	000h	000h	000h
	14 bits	0000h	0000h	0000h	0000h
Fourth code	8 bits	XXh	XXh	XXh	XXh
	10 bits	XXXh	XXXh	XXXh	XXXh
	12 bits	XXXh	XXXh	XXXh	XXXh
	14 bits	XXXXh	XXXXh	XXXXh	XXXXh

NOTE

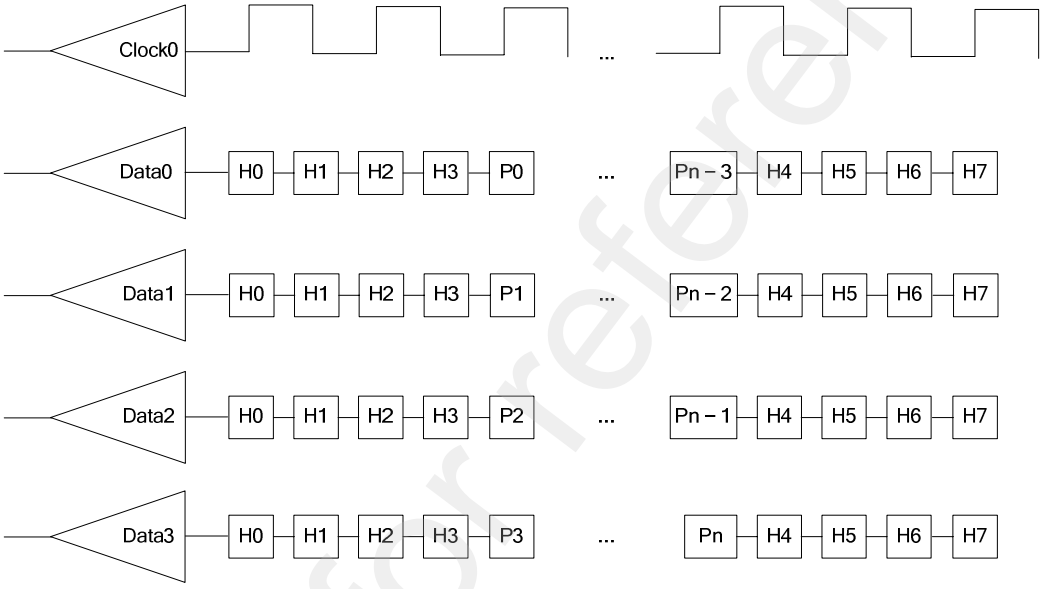
The first three fields of the synchronization code are fixed, and the fourth field identifies the start or end of a frame or line. The value of the fourth field is specified by image sensor vendors and therefore it varies according to vendors. Table 9-9 describes an implementation mode.

Table 9-9 Sample of the fourth field of the LVDS synchronization code

Field	Bit Width	Synchronization code			
		SAV(Valid line)	EAV(Valid line)	SAV(Invalid line)	EAV(Invalid line)
Fourth code	8 bits	80h	9Dh	ABh	B6h
	10 bits	200h	274h	2ACh	2D8h
	12 bits	800h	9D0h	AB0h	B60h
	14 bits	2000h	2740h	2AC0h	2D80h

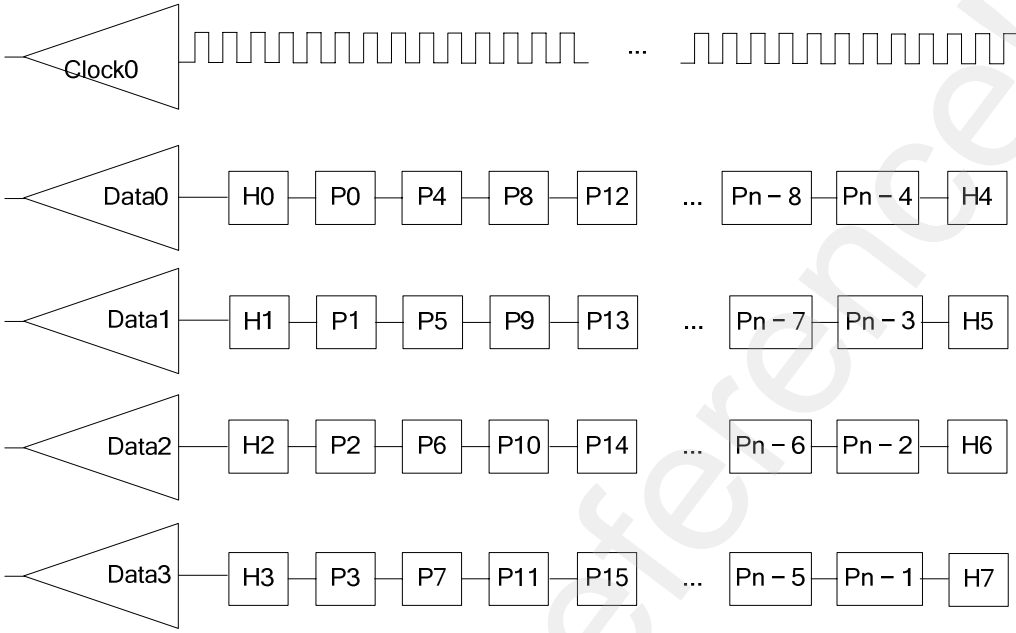
Figure 9-26 shows how LVDS synchronization code and pixel data are transmitted on each of the four channels. H indicates the synchronization code, and P indicates pixel. The bit widths of H and P are consistent with that of a single output pixel of the image sensor. In each data channel, the synchronization code with four-pixel bit width is transmitted before pixel data. The distribution of pixel data is related to the number of channels. Data is transmitted in series, and the endian mode is configurable in the MIPI RX.

Figure 9-26 LVDS synchronization code and image transfer mode 1



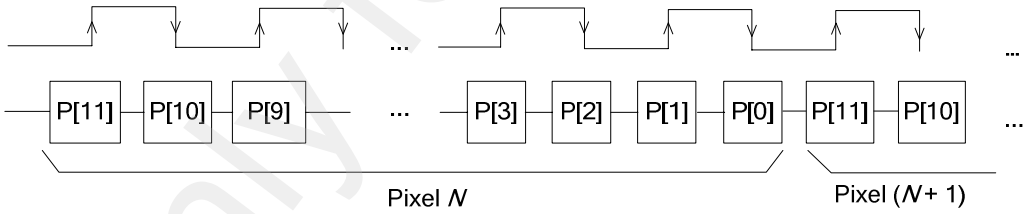
In another LVDS transfer mode, the four fields of the synchronization code are allocated to and transmitted in different channels. As shown in Figure 9-27, H0 to H3 are simultaneously transmitted in four data channels. The transfer mode of the pixel data in Figure 9-27 is the same as that in Figure 9-26.

Figure 9-27 LVDS synchronization code and image transfer mode 2



The synchronization codes and pixel data are transmitted in serial mode, and the data endian mode is configurable in the MIPI RX. Figure 9-28 shows the timing in which the image sensor outputs a single pixel by taking the raw12 data and big-endian mode as an example.

Figure 9-28 LVDS timing of a single pixel



Linear Mode of the LVDS Interface

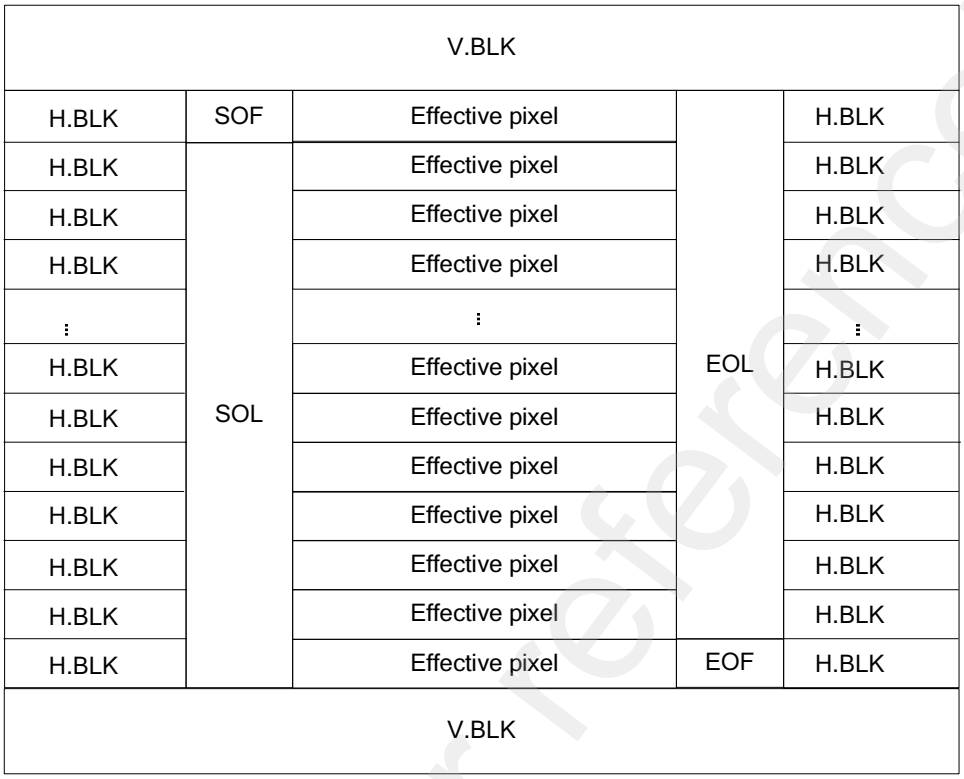
Two LVDS synchronization modes are available. In one mode, SAV (Invalid) and EAV (Invalid) identify invalid data of the blanking region whereas SAV (Valid) and EAV (Valid) identify pixel data of the active region. Figure 9-29 shows this synchronization mode.

Figure 9-29 LVDS synchronization mode 1

H.BLK	SAV (invalid line)	V.BLK	EAV (invalid line)	H.BLK
H.BLK		V.BLK		H.BLK
H.BLK		V.BLK		H.BLK
H.BLK	SAV (valid line)	Effective pixel	EAV (valid line)	H.BLK
H.BLK		Effective pixel		H.BLK
⋮		⋮		⋮
H.BLK		Effective pixel		H.BLK
H.BLK		Effective pixel		H.BLK
H.BLK		Effective pixel		H.BLK
H.BLK		Effective pixel		H.BLK
H.BLK		Effective pixel		H.BLK
H.BLK		Effective pixel		H.BLK
H.BLK	SAV (invalid line)	V.BLK	EAV (invalid line)	H.BLK
⋮		⋮		⋮
H.BLK		V.BLK		H.BLK
H.BLK		V.BLK		H.BLK

In the other mode, SOF identifies the start of the first line in the active region, EOF identifies the end of the last line in the active region, and SOL and EOL identify the start and end of the other lines in the active region. Figure 9-30 shows this synchronization mode.

Figure 9-30 LVDS synchronization mode 2



WDR Modes of the LVDS Interface

The MIPI RX supports four WDR transfer modes of the LVDS interface.

- LVDS WDR mode 1: a WDR mode with the SOF-EOF flag. In this mode, the long and short exposure frames have independent synchronization codes.
- LVDS WDR mode 2: a DOL WDR mode with the SAV-EAV flag. In this mode, the synchronization code consists of four fields, and the long and short exposure frames have independent synchronization codes.
- LVDS WDR mode 3: a DOL WDR mode with the SAV-EAV flag. In this mode, the synchronization code consists of five fields, and the long and short exposure frames have independent synchronization codes.
- LVDS WDR mode 4: a DOL WDR mode with the SAV-EAV flag. In this mode, the synchronization code consists of four fields, the long and short exposure frames share one group of synchronization codes, and there are blanking regions between the long exposure data and short exposure data.

The MIPI RX compares the received synchronization code value with the preconfigured value in the register based on the mode configuration, determines whether the received image frame is a long exposure frame or a short exposure frame based on the comparison result, identifies the image frame type in a specific way, and implements demultiplexing in the VICAP module.

Figure 9-31 shows the LVDS WDR mode 1. The type of the synchronization code for the long exposure video data is different from that of the synchronization code for the short exposure video data. Data with different exposure lengths is distinguished by using the synchronization code.

Figure 9-31 LVDS WDR mode 1 (two frames)

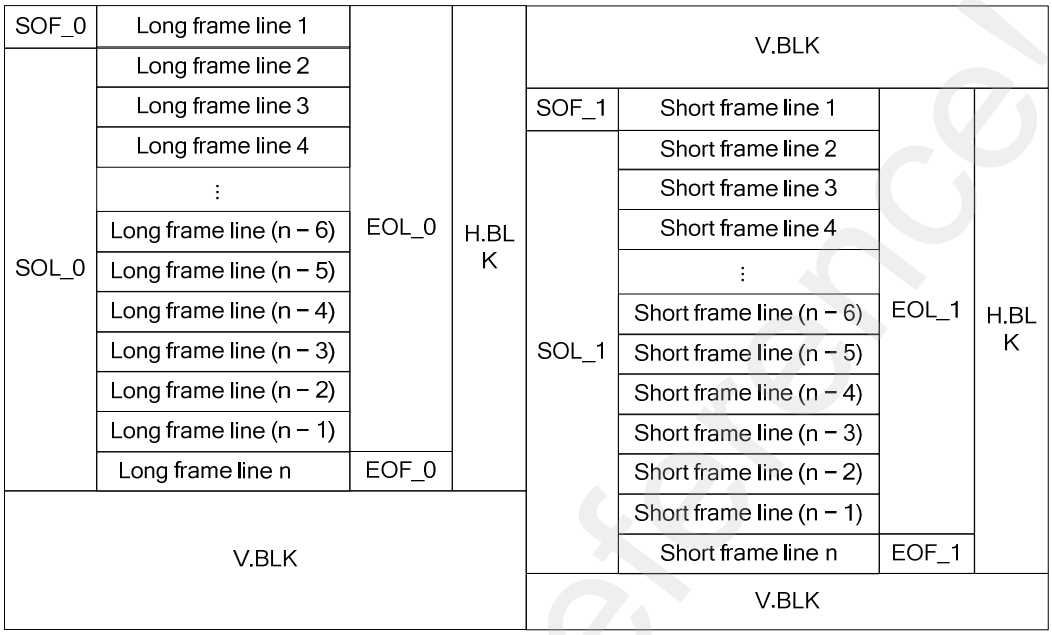
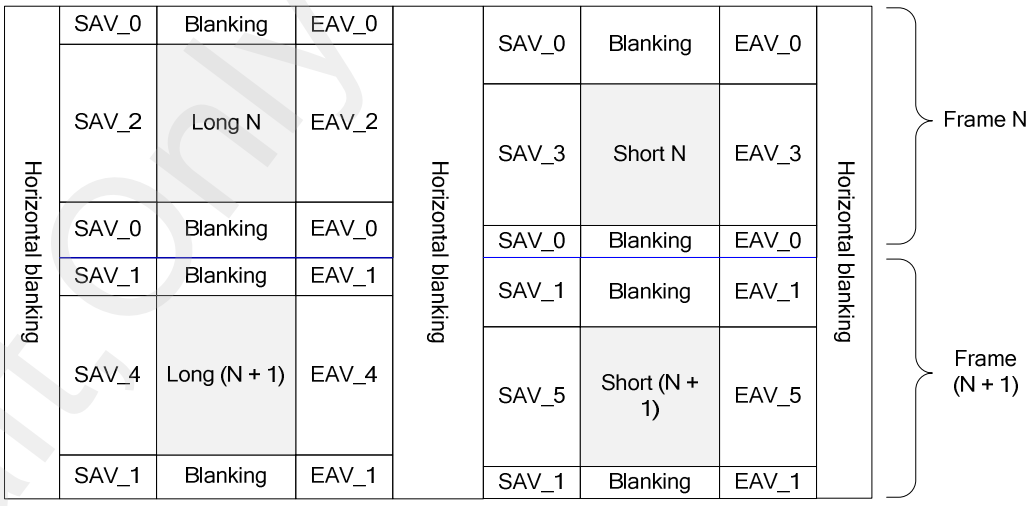


Figure 9-32 shows the LVDS WDR mode 2. In this mode, the SAV-EAV is used for synchronization, the long and short exposure frames have independent synchronization codes, and the synchronization code of frame N is different from that of frame (N + 1).

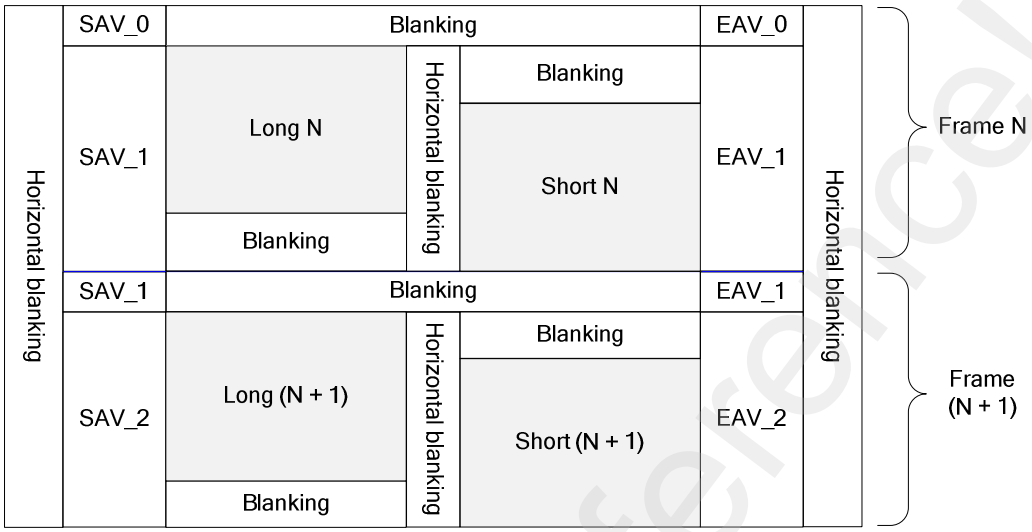
The LVDS WDR mode 3 is similar to LVDS WDR mode 2 except that the synchronization code in mode 3 consists of five fields.

Figure 9-32 LVDS WDR mode 2 (two frames)



In LVDS WDR mode 4, the SAV-EAV is used for synchronization, and the long and short exposure frames use one group of synchronization codes. There are blanking regions between the long exposure data and short exposure data, and the values of pixels in the blanking regions are fixed. Figure 9-33 shows the image transfer timing.

Figure 9-33 LVDS WDR mode 4 (two frames)



HiSPI Data Format

HiSPI, formulated by Aptina, includes the HiSPI physical layer protocol and HiSPI specification. The HiSPI physical layer protocol stipulates the electrical specifications and timing parameters, whereas the HiSPI specification defines the data packetizing modes.

The HiSPI specification stipulates two physical layer electric standards (HiVCM and SLVS) and four data transmission modes (Packetized-SP, Streaming-SP, Streaming-S, and ActiveStart-SP8).

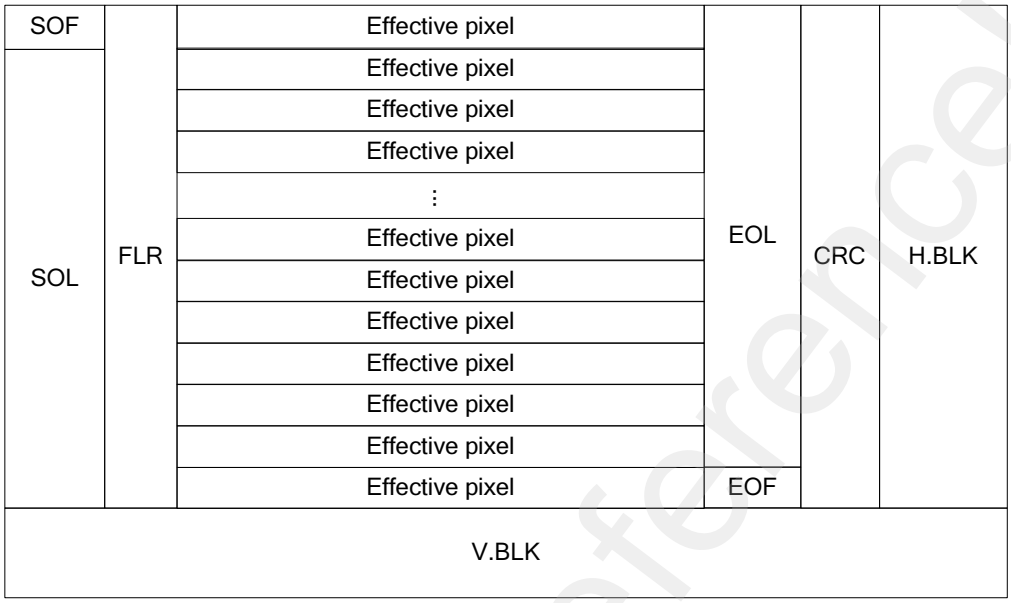
The MIPI RX supports the HiVCM and SLVS electric standards and supports the Packetized-SP and Streaming-SP mode.

HiSPI Linear Mode

In Packetized-SP mode, the image sensor identifies the start of the first line in the active region by using the SOF, the end of the last line in the active region by using the EOF, and the start as well end of other lines in the active region by using SOL and EOL respectively. This synchronization method is similar to that in Figure 9-30 except that CRC and FLR can be added to data packets in Packetized-SP mode. Figure 9-34 shows the data format in HiSPI Packetized-SP mode.

The MIPI RX can check whether the matching of SOF-EOF and SOL-EOL is correct. However, it does not process the CRC and FLR data.

Figure 9-34 Data format in HiSPI Packetized-SP mode



The other three HiSPI transfer modes (Streaming-SP, Streaming-S, and ActiveStart-SP8) are similar to the Packetized-SP mode except that they differ in the calibration mode of the synchronization code. Table 9-10 describes the differences between the four HiSPI transfer modes. SOF and EOF indicate the start and end of the frame in the active region respectively; SOL and EOL indicate the start and end of the line in the active region respectively; SAV indicates the start of the line in the blanking region.

Table 9-10 HiSPI transfer modes

Synchronization Code	Packetized-SP	Streaming-SP	Streaming-S	ActiveStart-SP8
SOF	Required	Required	Unsupported	Required
SOL	Required	Required	Required	Required
EOF	Required	Unsupported	Unsupported	Unsupported
EOL	Required	Unsupported	Unsupported	Unsupported
SAV	Unsupported	Required	Required	Unsupported

The MIPI RX supports the preceding four modes. All the four fields of a synchronization code can be transmitted in each channel (as shown in Figure 9-26), or the four fields can be allocated to and transmitted in different channels (as shown in Figure 9-27).

HiSPI WDR Mode

The synchronization code in HiSPI WDR mode is the same as that in linear mode. There are blanking regions between the long exposure data and short exposure data. The first several lines of short exposure data are not the active pixel region and are stuffed with fixed values. Figure 9-35 shows the timing in HiSPI WDR mode.

Figure 9-35 HiSPI WDR mode

<table>
<tr><td>SOF</td><td>Long frame line 1</td><td rowspan="12">EOL</td><td rowspan="12">H.BLK</td><td rowspan="12">SOL</td><td>T2 padding</td><td rowspan="12">EOL</td><td rowspan="12">H.BLK</td></tr>
<tr><td rowspan="11">SOL</td><td>Long frame line 2</td><td>Short frame line 1</td></tr>
<tr><td>Long frame line 3</td><td>Short frame line 2</td></tr>
<tr><td>Long frame line 4</td><td>Short frame line 3</td></tr>
<tr><td>⋮</td><td>Short frame line 4</td></tr>
<tr><td>Long frame line (n − 3)</td><td>⋮</td></tr>
<tr><td>Long frame line (n − 2)</td><td>Short frame line (n − 3)</td></tr>
<tr><td>Long frame line (n − 1)</td><td>Short frame line (n − 2)</td></tr>
<tr><td>Long frame line n</td><td>Short frame line (n − 1)</td></tr>
<tr><td rowspan="2">T1 padding</td><td>Short frame line n</td><td>EOF</td></tr>
<tr><td>SOV</td><td>V.BLK</td><td>EOV</td><td></td><td>SOV</td><td>V.BLK</td><td>EOV</td><td></td></tr>
</table>

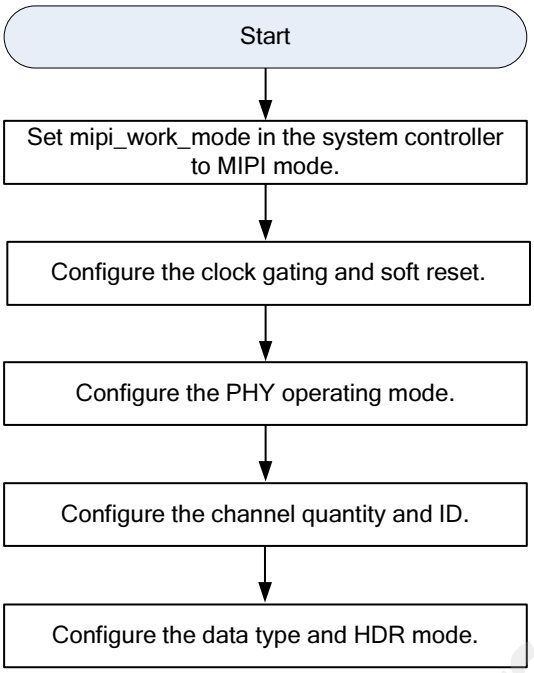
9.3.4 Operating Mode of the MIPI RX Controller

The MIPI RX controller supports the MIPI, LVDS, and HiSPI modes. The software configuration in each mode contains two parts: controller and combo-PHY.

9.3.4.1 MIPI Mode Configuration Process

In MIPI mode, the required channel quantity, data type, and WDR mode for data transmission as well as PHY operating mode need to be configured. The frame or line synchronization information in MIPI mode is contained in the data packet. The controller parses the data packet and restores the pixel data. Figure 9-36 shows the software configuration process in MIPI mode.

Figure 9-36 MIPI RX configuration process in MIPI mode

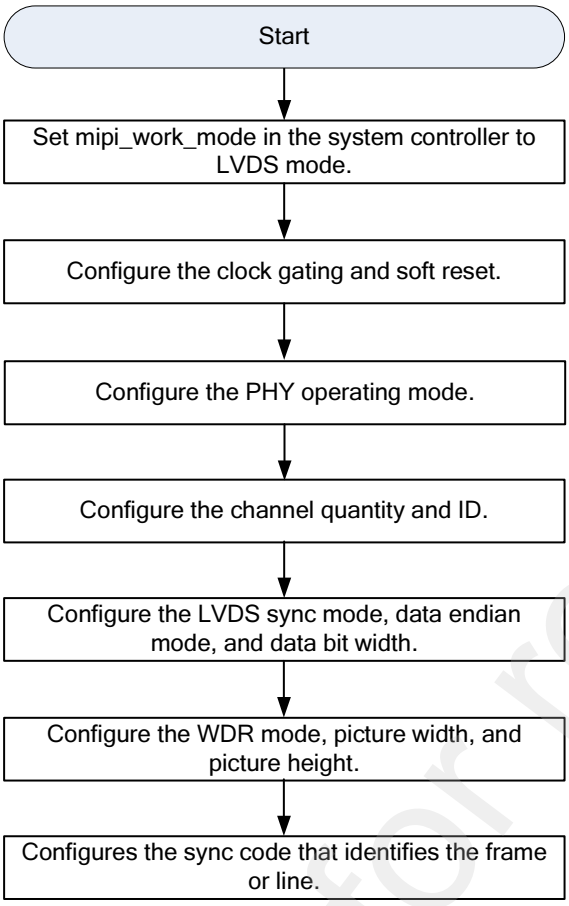


9.3.4.2 LVDS and HiSPI Mode Configuration Process

In LVDS/HiSPi mode, configure the type of raw data, endian mode, synchronization mode, WDR mode and image size registers. In LVDS mode, a synchronization code is used to identify frame or line synchronization information. Depending on the type of raw data, the synchronization code can be 8, 10, 12, 14, or 16 bits.

Figure 9-37 shows the software configuration process in LVDS and HiSPI modes.

Figure 9-37 MIPI RX configuration process in LVDS and HiSPI modes



9.3.5 MIPI RX Register Summary

Table 9-11 describes the MIPI RX registers.

Table 9-11 Summary of MIPI RX registers (base address: 0x1130_0000)

Offset Address	Register	Description	Page
0x0000	PHY_MODE_LINK0	Link 0 PHY operating mode register	9-203
0x0004	PHY_SKEW_LINK0	Link 0 PHY channel delay adjustment register	9-204
0x0008	PHY_EN_LINK0	Link 0 PHY channel enable register	9-205
0x0018	PHY_DATA_LINK0	Link 0 PHY output parallel data register	9-207
0x001C	PHY_PH_MIPI_LINK0	Link 0 MIPI data packet header register	9-207

Offset Address	Register	Description	Page
0x0020	PHY_DATA_MIPI_LINK0	Link 0 MIPI mode data register	9-208
0x0024	PHY_SYNC_DCT_LINK0	Link 0 PHY LVDS mode synchronization header detection control register	9-208
0x0030	PHY_SYNC_CODE0_LINK0	Link 0 PHY LVDS mode synchronization header register 0	9-209
0x0034	PHY_SYNC_CODE1_LINK0	Link 0 PHY LVDS mode synchronization header register 1	9-209
0x0038	PHY_SYNC_CODE2_LINK0	Link 0 PHY LVDS mode synchronization header register 2	9-210
0x003C	PHY_SYNC_CODE3_LINK0	Link 0 PHY LVDS mode synchronization header register 3	9-210
0x01F0	MIPI_CIL_INT_RAW_LINK0	Link 0 MIPI CIL raw interrupt status register	9-211
0x01F4	MIPI_CIL_INT_LINK0	Link 0 MIPI CIL interrupt status register	9-212
0x01F8	MIPI_CIL_INT_MSK_LINK0	Link 0 MIPI CIL interrupt mask register	9-213
0x0200	PHY_MODE_LINK1	Link 1 PHY operating mode register	9-215
0x0204	PHY_SKEW_LINK1	Link 1 PHY channel delay adjustment register	9-216
0x0208	PHY_EN_LINK1	Link 1 PHY channel enable register	9-217
0x0218	PHY_DATA_LINK1	Link 1 PHY output parallel data register	9-218
0x021C	PHY_PH_MIPI_LINK1	Link 1 MIPI data packet header register	9-219
0x0220	PHY_DATA_MIPI_LINK1	Link 1 MIPI mode data register	9-219
0x0224	PHY_SYNC_DCT_LINK1	Link 1 PHY LVDS mode synchronization header detection control register	9-219

Offset Address	Register	Description	Page
0x0230	PHY_SYNC_CODE0_LINK1	Link 1 PHY LVDS mode synchronization header register 0	9-220
0x0234	PHY_SYNC_CODE1_LINK1	Link 1 PHY LVDS mode synchronization header register 1	9-221
0x0238	PHY_SYNC_CODE2_LINK1	Link 1 PHY LVDS mode synchronization header register 2	9-221
0x023C	PHY_SYNC_CODE3_LINK1	Link 1 PHY LVDS mode synchronization header register 3	9-222
0x03F0	MIPI_CIL_INT_RAW_LINK1	Link 1 MIPI CIL raw interrupt status register	9-222
0x03F4	MIPI_CIL_INT_LINK1	Link 1 MIPI CIL interrupt status register	9-223
0x03F8	MIPI_CIL_INT_MSK_LINK1	Link 1 MIPI CIL interrupt mask register	9-225
0x0400	PHY_MODE_LINK2	Link 2 PHY operating mode register	9-226
0x0404	PHY_SKEW_LINK2	Link 2 PHY channel delay adjustment register	9-228
0x0408	PHY_EN_LINK2	Link 2 PHY channel enable register	9-229
0x0418	PHY_DATA_LINK2	Link 2 PHY output parallel data register	9-230
0x041C	PHY_PH_MIPI_LINK2	Link 2 MIPI data packet header register	9-230
0x0420	PHY_DATA_MIPI_LINK2	Link 2 MIPI mode data register	9-231
0x0424	PHY_SYNC_DCT_LINK2	Link 2 PHY LVDS mode synchronization header detection control register	9-231
0x0430	PHY_SYNC_CODE0_LINK2	Link 2 PHY LVDS mode synchronization header register 0	9-232
0x0434	PHY_SYNC_CODE1_LINK2	Link 2 PHY LVDS mode synchronization header register 1	9-232

Offset Address	Register	Description	Page
0x0438	PHY_SYNC_CODE2_LINK2	Link 2 PHY LVDS mode synchronization header register 2	9-233
0x043C	PHY_SYNC_CODE3_LINK2	Link 2 PHY LVDS mode synchronization header register 3	9-233
0x05F0	MIPI_CIL_INT_RAW_LINK2	Link 2 MIPI CIL raw interrupt status register	9-234
0x05F4	MIPI_CIL_INT_LINK2	Link 2 MIPI CIL interrupt status register	9-235
0x05F8	MIPI_CIL_INT_MSK_LINK2	Link 2 MIPI CIL interrupt mask register	9-236
0x0800	PHY_CHN_CTRL	PHY ID selection register	9-238
0x0804	PHY_LP_SELECT	PHY 1 LP mode signal selection register	9-238
0x080C	MIPI_MEM_CTRL	Memory control register	9-239
0x0810	LANE_EN	Lane enable register	9-240
0x0814	MIPI_PHYCFG_MODE	MIPI PHY configuration mode register	9-241
0x0818	MIPI_PHYCFG_EN	MIPI PHY configuration enable register	9-242
0x081C	MIPI_CIL_CTRL	MIPI CIL control register	9-242
0x0820	MIPI_SRST_CFG	MIPI core soft reset register	9-243
0x0EF0	MIPI_CHN0_INT_RAW	MIPI channel 0 raw interrupt status register	9-244
0x0EF4	MIPI_CHN0_INT	MIPI channel 0 interrupt status register	9-245
0x0EF8	MIPI_CHN0_INT_MSK	MIPI channel 0 interrupt mask register	9-246
0x1004	MIPI0_LANES_NUM	MIPI 0 enabled data channel quantity register	9-248
0x100C	MIPI0_MAIN_INT_ST	MIPI 0 global interrupt status register	9-248
0x1010	MIPI0_DI_1	MIPI 0 controller data ID 1 register	9-249

Offset Address	Register	Description	Page
0x1014	MIPI0_DI_2	MIPI 0 controller data ID 2 register	9-251
0x1060	MIPI0_PKT_INTR_ST	MIPI 0 packet interrupt status register	9-252
0x1064	MIPI0_PKT_INTR_MSK	MIPI 0 packet interrupt mask register	9-253
0x1070	MIPI0_PKT_INTR2_ST	MIPI 0 packet interrupt status register 2	9-254
0x1074	MIPI0_PKT_INTR2_MSK	MIPI 0 packet interrupt mask register 2	9-255
0x1080	MIPI0_FRAME_INTR_ST	MIPI 0 frame interrupt status register	9-257
0x1084	MIPI0_FRAME_INTR_MSK	MIPI 0 frame interrupt mask register	9-259
0x1090	MIPI0_LINE_INTR_ST	MIPI 0 line interrupt status register	9-260
0x1094	MIPI0_LINE_INTR_MSK	MIPI 0 line interrupt mask register	9-263
0x1100	MIPI0_USERDEF_DT	MIPI 0 pixel bit width configuration register for the user-defined data type	9-265
0x1104	MIPI0_USER_DEF	MIPI 0 user-defined data type enable configuration register	9-266
0x1108	MIPI0_CTRL_MODE_HS	MIPI 0 operating mode enable register	9-267
0x1200	MIPI0_DOL_ID_CODE0	MIPI 0 DOL mode frame identification register 0	9-267
0x1204	MIPI0_DOL_ID_CODE1	MIPI 0 DOL mode frame identification register 1	9-267
0x1208	MIPI0_DOL_ID_CODE2	MIPI 0 DOL mode frame identification register 2	9-268
0x1230	MIPI0_CTRL_MODE_PIXEL	MIPI 0 output operating mode enable register	9-268
0x1240	MIPI0_DUMMY_PIX_REG	MIPI 0 dummy line pixel value register	9-269

Offset Address	Register	Description	Page
0x1250	MIPI0_IMGSIZE0_STATIS	MIPI 0 VC 0 transferred image size register	9-270
0x1254	MIPI0_IMGSIZE1_STATIS	MIPI 0 VC 1 transferred image size register	9-270
0x1258	MIPI0_IMGSIZE2_STATIS	MIPI 0 VC 2 transferred image size register	9-271
0x125C	MIPI0_IMGSIZE3_STATIS	MIPI 0 VC 3 transferred image size register	9-271
0x12F0	MIPI0_CTRL_INT_RAW	MIPI 0 read data error raw interrupt status register	9-271
0x12F4	MIPI0_CTRL_INT	MIPI 0 read data error interrupt status register	9-272
0x12F8	MIPI0_CTRL_INT_MSK	MIPI 0 read data error interrupt mask register	9-273
0x1300	LVDS0_WDR	LVDS WDR control register	9-274
0x1304	LVDS0_DOLSCD_HBLK	LVDS SCD control register 0	9-276
0x130C	LVDS0_IMGSIZE	LVDS image size register	9-276
0x1310	LVDS0_CTRL	LVDS control register	9-276
0x1314	LVDS0_CROP_START	LVDS cropping register	9-278
0x1320	LVDS0_LANE0_SOF_01	Lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode	9-278
0x1324	LVDS0_LANE0_SOF_23	Lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode	9-279
0x1328	LVDS0_LANE0_EOF_01	Lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode	9-279
0x132C	LVDS0_LANE0_EOF_23	Lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode	9-280

Offset Address	Register	Description	Page
0x1330	LVDS0_LANE0_SOL_01	Lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode	9-280
0x1334	LVDS0_LANE0_SOL_23	Lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode	9-281
0x1338	LVDS0_LANE0_EOL_01	Lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode	9-281
0x133C	LVDS0_LANE0_EOL_23	Lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode	9-282
0x1340	LVDS0_LANE1_SOF_01	Lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode	9-282
0x1344	LVDS0_LANE1_SOF_23	Lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode	9-283
0x1348	LVDS0_LANE1_EOF_01	Lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode	9-283
0x134C	LVDS0_LANE1_EOF_23	Lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode	9-284
0x1350	LVDS0_LANE1_SOL_01	Lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode	9-284
0x1354	LVDS0_LANE1_SOL_23	Lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode	9-285
0x1358	LVDS0_LANE1_EOL_01	Lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode	9-285
0x135C	LVDS0_LANE1_EOL_23	Lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode	9-286
0x1360	LVDS0_LANE2_SOF_01	Lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode	9-286
0x1364	LVDS0_LANE2_SOF_23	Lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode	9-287

Offset Address	Register	Description	Page
0x1368	LVDS0_LANE2_EOF_01	Lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode	9-287
0x136C	LVDS0_LANE2_EOF_23	Lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode	9-288
0x1370	LVDS0_LANE2_SOL_01	Lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode	9-288
0x1374	LVDS0_LANE2_SOL_23	Lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode	9-289
0x1378	LVDS0_LANE2_EOL_01	Lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode	9-289
0x137C	LVDS0_LANE2_EOL_23	Lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode	9-290
0x1380	LVDS0_LANE3_SOF_01	Lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode	9-290
0x1384	LVDS0_LANE3_SOF_23	Lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode	9-291
0x1388	LVDS0_LANE3_EOF_01	Lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode	9-291
0x138C	LVDS0_LANE3_EOF_23	Lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode	9-292
0x1390	LVDS0_LANE3_SOL_01	Lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode	9-292
0x1394	LVDS0_LANE3_SOL_23	Lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode	9-293
0x1398	LVDS0_LANE3_EOL_01	Lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode	9-293
0x139C	LVDS0_LANE3_EOL_23	Lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode	9-294

Offset Address	Register	Description	Page
0x13A0	LVDS0_LANE4_SOF_01	Lane 4 SOF synchronization code configuration register in LVDS or HiSPI mode	9-294
0x13A4	LVDS0_LANE4_SOF_23	Lane 4 SOF synchronization code configuration register in LVDS or HiSPI mode	9-295
0x13A8	LVDS0_LANE4_EOF_01	Lane 4 EOF synchronization code configuration register in LVDS or HiSPI mode	9-295
0x13AC	LVDS0_LANE4_EOF_23	Lane 4 EOF synchronization code configuration register in LVDS or HiSPI mode	9-296
0x13B0	LVDS0_LANE4_SOL_01	Lane 4 SOL synchronization code configuration register in LVDS or HiSPI mode	9-296
0x13B4	LVDS0_LANE4_SOL_23	Lane 4 SOL synchronization code configuration register in LVDS or HiSPI mode	9-297
0x13B8	LVDS0_LANE4_EOL_01	Lane 4 EOL synchronization code configuration register in LVDS or HiSPI mode	9-297
0x13BC	LVDS0_LANE4_EOL_23	Lane 4 EOL synchronization code configuration register in LVDS or HiSPI mode	9-298
0x13C0	LVDS0_LANE5_SOF_01	Lane 5 SOF synchronization code configuration register in LVDS or HiSPI mode	9-298
0x13C4	LVDS0_LANE5_SOF_23	Lane 5 SOF synchronization code configuration register in LVDS or HiSPI mode	9-299
0x13C8	LVDS0_LANE5_EOF_01	Lane 5 EOF synchronization code configuration register in LVDS or HiSPI mode	9-299
0x13CC	LVDS0_LANE5_EOF_23	Lane 5 EOF synchronization code configuration register in LVDS or HiSPI mode	9-300
0x13D0	LVDS0_LANE5_SOL_01	Lane 5 SOL synchronization code configuration register in LVDS or HiSPI mode	9-300
0x13D4	LVDS0_LANE5_SOL_23	Lane 5 SOL synchronization code configuration register in LVDS or HiSPI mode	9-301

Offset Address	Register	Description	Page
0x13D8	LVDS0_LANE5_EOL_01	Lane 5 EOL synchronization code configuration register in LVDS or HiSPI mode	9-301
0x13DC	LVDS0_LANE5_EOL_23	Lane 5 EOL synchronization code configuration register in LVDS or HiSPI mode	9-302
0x13E0	LVDS0_LANE6_SOF_01	Lane 6 SOF synchronization code configuration register in LVDS or HiSPI mode	9-302
0x13E4	LVDS0_LANE6_SOF_23	Lane 6 SOF synchronization code configuration register in LVDS or HiSPI mode	9-303
0x13E8	LVDS0_LANE6_EOF_01	Lane 6 EOF synchronization code configuration register in LVDS or HiSPI mode	9-303
0x13EC	LVDS0_LANE6_EOF_23	Lane 6 EOF synchronization code configuration register in LVDS or HiSPI mode	9-304
0x13F0	LVDS0_LANE6_SOL_01	Lane 6 SOL synchronization code configuration register in LVDS or HiSPI mode	9-304
0x13F4	LVDS0_LANE6_SOL_23	Lane 6 SOL synchronization code configuration register in LVDS or HiSPI mode	9-305
0x13F8	LVDS0_LANE6_EOL_01	Lane 6 EOL synchronization code configuration register in LVDS or HiSPI mode	9-305
0x13FC	LVDS0_LANE6_EOL_23	Lane 6 EOL synchronization code configuration register in LVDS or HiSPI mode	9-306
0x1400	LVDS0_LANE7_SOF_01	Lane 7 SOF synchronization code configuration register in LVDS or HiSPI mode	9-306
0x1404	LVDS0_LANE7_SOF_23	Lane 7 SOF synchronization code configuration register in LVDS or HiSPI mode	9-307
0x1408	LVDS0_LANE7_EOF_01	Lane 7 EOF synchronization code configuration register in LVDS or HiSPI mode	9-307
0x140C	LVDS0_LANE7_EOF_23	Lane 7 EOF synchronization code configuration register in LVDS or HiSPI mode	9-308

Offset Address	Register	Description	Page
0x1410	LVDS0_LANE7_SOL_01	Lane 7 SOL synchronization code configuration register in LVDS or HiSPI mode	9-308
0x1414	LVDS0_LANE7_SOL_23	Lane 7 SOL synchronization code configuration register in LVDS or HiSPI mode	9-309
0x1418	LVDS0_LANE7_EOL_01	Lane 7 EOL synchronization code configuration register in LVDS or HiSPI mode	9-309
0x141C	LVDS0_LANE7_EOL_23	Lane 7 EOL synchronization code configuration register in LVDS or HiSPI mode	9-310
0x1420	LVDS0_LANE8_SOF_01	Lane 8 SOF synchronization code configuration register in LVDS or HiSPI mode	9-310
0x1424	LVDS0_LANE8_SOF_23	Lane 8 SOF synchronization code configuration register in LVDS or HiSPI mode	9-311
0x1428	LVDS0_LANE8_EOF_01	Lane 8 EOF synchronization code configuration register in LVDS or HiSPI mode	9-311
0x142C	LVDS0_LANE8_EOF_23	Lane 8 EOF synchronization code configuration register in LVDS or HiSPI mode	9-312
0x1430	LVDS0_LANE8_SOL_01	Lane 8 SOL synchronization code configuration register in LVDS or HiSPI mode	9-312
0x1434	LVDS0_LANE8_SOL_23	Lane 8 SOL synchronization code configuration register in LVDS or HiSPI mode	9-313
0x1438	LVDS0_LANE8_EOL_01	Lane 8 EOL synchronization code configuration register in LVDS or HiSPI mode	9-313
0x143C	LVDS0_LANE8_EOL_23	Lane 8 EOL synchronization code configuration register in LVDS or HiSPI mode	9-314
0x1440	LVDS0_LANE9_SOF_01	Lane 9 SOF synchronization code configuration register in LVDS or HiSPI mode	9-314
0x1444	LVDS0_LANE9_SOF_23	Lane 9 SOF synchronization code configuration register in LVDS or HiSPI mode	9-315

Offset Address	Register	Description	Page
0x1448	LVDS0_LANE9_EOF_01	Lane 9 EOF synchronization code configuration register in LVDS or HiSPI mode	9-315
0x144C	LVDS0_LANE9_EOF_23	Lane 9 EOF synchronization code configuration register in LVDS or HiSPI mode	9-316
0x1450	LVDS0_LANE9_SOL_01	Lane 9 SOL synchronization code configuration register in LVDS or HiSPI mode	9-316
0x1454	LVDS0_LANE9_SOL_23	Lane 9 SOL synchronization code configuration register in LVDS or HiSPI mode	9-317
0x1458	LVDS0_LANE9_EOL_01	Lane 9 EOL synchronization code configuration register in LVDS or HiSPI mode	9-317
0x145C	LVDS0_LANE9_EOL_23	Lane 9 EOL synchronization code configuration register in LVDS or HiSPI mode	9-318
0x1460	LVDS0_LANE10_SOF_01	Lane 10 SOF synchronization code configuration register in LVDS or HiSPI mode	9-318
0x1464	LVDS0_LANE10_SOF_23	Lane 10 SOF synchronization code configuration register in LVDS or HiSPI mode	9-319
0x1468	LVDS0_LANE10_EOF_01	Lane 10 EOF synchronization code configuration register in LVDS or HiSPI mode	9-319
0x146C	LVDS0_LANE10_EOF_23	Lane 10 EOF synchronization code configuration register in LVDS or HiSPI mode	9-320
0x1470	LVDS0_LANE10_SOL_01	Lane 10 SOL synchronization code configuration register in LVDS or HiSPI mode	9-320
0x1474	LVDS0_LANE10_SOL_23	Lane 10 SOL synchronization code configuration register in LVDS or HiSPI mode	9-321
0x1478	LVDS0_LANE10_EOL_01	Lane 10 EOL synchronization code configuration register in LVDS or HiSPI mode	9-321
0x147C	LVDS0_LANE10_EOL_23	Lane 10 EOL synchronization code configuration register in LVDS or HiSPI mode	9-322

Offset Address	Register	Description	Page
0x1480	LVDS0_LANE11_SOF_01	Lane 11 SOF synchronization code configuration register in LVDS or HiSPI mode	9-322
0x1484	LVDS0_LANE11_SOF_23	Lane 11 SOF synchronization code configuration register in LVDS or HiSPI mode	9-323
0x1488	LVDS0_LANE11_EOF_01	Lane 11 EOF synchronization code configuration register in LVDS or HiSPI mode	9-323
0x148C	LVDS0_LANE11_EOF_23	Lane 11 EOF synchronization code configuration register in LVDS or HiSPI mode	9-324
0x1490	LVDS0_LANE11_SOL_01	Lane 11 SOL synchronization code configuration register in LVDS or HiSPI mode	9-324
0x1494	LVDS0_LANE11_SOL_23	Lane 11 SOL synchronization code configuration register in LVDS or HiSPI mode	9-325
0x1498	LVDS0_LANE11_EOL_01	Lane 11 EOL synchronization code configuration register in LVDS or HiSPI mode	9-325
0x149C	LVDS0_LANE11_EOL_23	Lane 11 EOL synchronization code configuration register in LVDS or HiSPI mode	9-326
0x14A0	LVDS0_LANE0_NXT_SOF_01	Lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-326
0x14A4	LVDS0_LANE0_NXT_SOF_23	Lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-327
0x14A8	LVDS0_LANE0_NXT_EOF_01	Lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-327
0x14AC	LVDS0_LANE0_NXT_EOF_23	Lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-328
0x14B0	LVDS0_LANE0_NXT_SOL_01	Lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-328
0x14B4	LVDS0_LANE0_NXT_SOL_23	Lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-329

Offset Address	Register	Description	Page
0x14B8	LVDS0_LANE0_NXT_EOL_01	Lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-329
0x14BC	LVDS0_LANE0_NXT_EOL_23	Lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-330
0x14C0	LVDS0_LANE1_NXT_SOF_01	Lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-330
0x14C4	LVDS0_LANE1_NXT_SOF_23	Lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-331
0x14C8	LVDS0_LANE1_NXT_EOF_01	Lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-331
0x14CC	LVDS0_LANE1_NXT_EOF_23	Lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-332
0x14D0	LVDS0_LANE1_NXT_SOL_01	Lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-332
0x14D4	LVDS0_LANE1_NXT_SOL_23	Lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-333
0x14D8	LVDS0_LANE1_NXT_EOL_01	Lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-333
0x14DC	LVDS0_LANE1_NXT_EOL_23	Lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-334
0x14E0	LVDS0_LANE2_NXT_SOF_01	Lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-334
0x14E4	LVDS0_LANE2_NXT_SOF_23	Lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-335
0x14E8	LVDS0_LANE2_NXT_EOF_01	Lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-335
0x14EC	LVDS0_LANE2_NXT_EOF_23	Lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-336

Offset Address	Register	Description	Page
0x14F0	LVDS0_LANE2_NXT_SOL_01	Lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-336
0x14F4	LVDS0_LANE2_NXT_SOL_23	Lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-337
0x14F8	LVDS0_LANE2_NXT_EOL_01	Lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-337
0x14FC	LVDS0_LANE2_NXT_EOL_23	Lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-338
0x1500	LVDS0_LANE3_NXT_SOF_01	Lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-338
0x1504	LVDS0_LANE3_NXT_SOF_23	Lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-339
0x1508	LVDS0_LANE3_NXT_EOF_01	Lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-339
0x150C	LVDS0_LANE3_NXT_EOF_23	Lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-340
0x1510	LVDS0_LANE3_NXT_SOL_01	Lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-340
0x1514	LVDS0_LANE3_NXT_SOL_23	Lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-341
0x1518	LVDS0_LANE3_NXT_EOL_01	Lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-341
0x151C	LVDS0_LANE3_NXT_EOL_23	Lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-342
0x1520	LVDS0_LANE4_NXT_SOF_01	Lane 4 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-342
0x1524	LVDS0_LANE4_NXT_SOF_23	Lane 4 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-343

Offset Address	Register	Description	Page
0x1528	LVDS0_LANE4_NXT_EOF_01	Lane 4 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-343
0x152C	LVDS0_LANE4_NXT_EOF_23	Lane 4 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-344
0x1530	LVDS0_LANE4_NXT_SOL_01	Lane 4 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-344
0x1534	LVDS0_LANE4_NXT_SOL_23	Lane 4 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-345
0x1538	LVDS0_LANE4_NXT_EOL_01	Lane 4 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-345
0x153C	LVDS0_LANE4_NXT_EOL_23	Lane 4 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-346
0x1540	LVDS0_LANE5_NXT_SOF_01	Lane 5 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-346
0x1544	LVDS0_LANE5_NXT_SOF_23	Lane 5 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-347
0x1548	LVDS0_LANE5_NXT_EOF_01	Lane 5 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-347
0x154C	LVDS0_LANE5_NXT_EOF_23	Lane 5 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-348
0x1550	LVDS0_LANE5_NXT_SOL_01	Lane 5 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-348
0x1554	LVDS0_LANE5_NXT_SOL_23	Lane 5 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-349
0x1558	LVDS0_LANE5_NXT_EOL_01	Lane 5 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-349
0x155C	LVDS0_LANE5_NXT_EOL_23	Lane 5 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-350

Offset Address	Register	Description	Page
0x1560	LVDS0_LANE6_NXT_SOF_01	Lane 6 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-350
0x1564	LVDS0_LANE6_NXT_SOF_23	Lane 6 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-351
0x1568	LVDS0_LANE6_NXT_EOF_01	Lane 6 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-351
0x156C	LVDS0_LANE6_NXT_EOF_23	Lane 6 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-352
0x1570	LVDS0_LANE6_NXT_SOL_01	Lane 6 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-352
0x1574	LVDS0_LANE6_NXT_SOL_23	Lane 6 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-353
0x1578	LVDS0_LANE6_NXT_EOL_01	Lane 6 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-353
0x157C	LVDS0_LANE6_NXT_EOL_23	Lane 6 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-354
0x1580	LVDS0_LANE7_NXT_SOF_01	Lane 7 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-354
0x1584	LVDS0_LANE7_NXT_SOF_23	Lane 7 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-355
0x1588	LVDS0_LANE7_NXT_EOF_01	Lane 7 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-355
0x158C	LVDS0_LANE7_NXT_EOF_23	Lane 7 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-356
0x1590	LVDS0_LANE7_NXT_SOL_01	Lane 7 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-356
0x1594	LVDS0_LANE7_NXT_SOL_23	Lane 7 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-357

Offset Address	Register	Description	Page
0x1598	LVDS0_LANE7_NXT_EOL_01	Lane 7 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-357
0x159C	LVDS0_LANE7_NXT_EOL_23	Lane 7 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-358
0x15A0	LVDS0_LANE8_NXT_SOF_01	Lane 8 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-358
0x15A4	LVDS0_LANE8_NXT_SOF_23	Lane 8 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-359
0x15A8	LVDS0_LANE8_NXT_EOF_01	Lane 8 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-359
0x15AC	LVDS0_LANE8_NXT_EOF_23	Lane 8 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-360
0x15B0	LVDS0_LANE8_NXT_SOL_01	Lane 8 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-360
0x15B4	LVDS0_LANE8_NXT_SOL_23	Lane 8 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-361
0x15B8	LVDS0_LANE8_NXT_EOL_01	Lane 8 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-361
0x15BC	LVDS0_LANE8_NXT_EOL_23	Lane 8 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-362
0x15C0	LVDS0_LANE9_NXT_SOF_01	Lane 9 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-362
0x15C4	LVDS0_LANE9_NXT_SOF_23	Lane 9 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-363
0x15C8	LVDS0_LANE9_NXT_EOF_01	Lane 9 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-363
0x15CC	LVDS0_LANE9_NXT_EOF_23	Lane 9 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-364

Offset Address	Register	Description	Page
0x15D0	LVDS0_LANE9_NXT_SOL_01	Lane 9 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-364
0x15D4	LVDS0_LANE9_NXT_SOL_23	Lane 9 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-365
0x15D8	LVDS0_LANE9_NXT_EOL_01	Lane 9 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-365
0x15DC	LVDS0_LANE9_NXT_EOL_23	Lane 9 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-366
0x15E0	LVDS0_LANE10_NXT_SOF_01	Lane 10 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-366
0x15E4	LVDS0_LANE10_NXT_SOF_23	Lane 10 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-367
0x15E8	LVDS0_LANE10_NXT_EOF_01	Lane 10 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-367
0x15EC	LVDS0_LANE10_NXT_EOF_23	Lane 10 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-368
0x15F0	LVDS0_LANE10_NXT_SOL_01	Lane 10 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-368
0x15F4	LVDS0_LANE10_NXT_SOL_23	Lane 10 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-369
0x15F8	LVDS0_LANE10_NXT_EOL_01	Lane 10 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-369
0x15FC	LVDS0_LANE10_NXT_EOL_23	Lane 10 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-370
0x1600	LVDS0_LANE11_NXT_SOF_01	Lane 11 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-370
0x1604	LVDS0_LANE11_NXT_SOF_23	Lane 11 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-371

Offset Address	Register	Description	Page
0x1608	LVDS0_LANE11_NXT_EOF_01	Lane 11 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-371
0x160C	LVDS0_LANE11_NXT_EOF_23	Lane 11 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-372
0x1610	LVDS0_LANE11_NXT_SOL_01	Lane 11 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-372
0x1614	LVDS0_LANE11_NXT_SOL_23	Lane 11 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-373
0x1618	LVDS0_LANE11_NXT_EOL_01	Lane 11 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-373
0x161C	LVDS0_LANE11_NXT_EOL_23	Lane 11 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-374
0x1620	LVDS0_LI_WORD0	LVDS DOL mode frame 0 LI register	9-374
0x1624	LVDS0_LI_WORD1	LVDS DOL mode frame 1 LI register	9-375
0x1628	LVDS0_LI_WORD2	LVDS DOL mode frame 2 LI register	9-375
0x162C	LVDS0_LI_WORD3	LVDS DOL mode frame 3 LI register	9-376
0x1680	LVDS0_IMGSIZE0_STATIS	LVDS LEF image size statistics register	9-376
0x1684	LVDS0_IMGSIZE1_STATIS	LVDS SEF1 image size statistics register	9-376
0x1688	LVDS0_IMGSIZE2_STATIS	LVDS SEF2 image size statistics register	9-377
0x168C	LVDS0_IMGSIZE3_STATIS	LVDS SEF3 image size statistics register	9-377
0x16F0	LVDS0_CTRL_INT_RAW	LVDS read data raw interrupt status register	9-378
0x16F4	LVDS0_CTRL_INT	LVDS read data interrupt status register	9-380

Offset Address	Register	Description	Page
0x16F8	LVDS0_CTRL_INT_MSK	LVDS read data interrupt mask register	9-383
0x1700	LANE_ID0_CHN0	Link 0 lane priority configuration register	9-386
0x1704	LANE_ID1_CHN0	Link 1 lane priority configuration register	9-386
0x1708	LANE_ID2_CHN0	Link 2 lane priority configuration register	9-387
0x17F0	ALIGN0_INT_RAW	MIPI_ALIGN raw interrupt status register	9-388
0x17F4	ALIGN0_INT	MIPI_ALIGN interrupt status register	9-389
0x17F8	ALIGN0_INT_MSK	MIPI_ALIGN interrupt mask register	9-391

9.3.6 MIPI Register Description

PHY_MODE_LINK0

PHY_MODE_LINK0 is a link 0 PHY operating mode register.

Offset Address	Register Name	Total Reset Value
0x0000	PHY_MODE_LINK0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	phy0_rg_mipi_mode	reserved	phy0_rg_ext_clk_en	reserved	phy0_rg_faclk_en	reserved	phy0_rg_en_lp	reserved	phy0_rg_en_cmos	reserved	phy0_rg_en_clk	phy0_rg_en_d
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved

[24]	RW	phy0_rg_mipi_mode	MIPI/LVDS input mode select. This field is set to 0 when the PHY works in LVDS mode and the common voltage is greater than or equal to 900 mV. 0: The common voltage is 900 mV or higher. 1: The common voltage is lower than 900 mV.
[23:21]	RO	reserved	Reserved
[20]	RW	phy0_rg_ext_clk_en	Differential clock source select 0: PAD input differential clock 1: differential clock of other links
[19:17]	RO	reserved	Reserved
[16]	RW	phy0_rg_faclk_en	Phase of the associated clock for the PHY output data 0: Data is output at the rising edge of the clock. 1: Data is output at the falling edge of the clock.
[15:13]	RO	reserved	Reserved
[12]	RW	phy0_rg_en_lp	PHY LP mode enable. The LP mode is enabled in MIPI mode and disabled in other modes. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved
[8]	RW	phy0_rg_en_cmos	PHY CMOS mode enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	phy0_rg_en_clk	Clock lane enable 0: disabled 1: enabled
[3:0]	RW	phy0_rg_en_d	Data lane enable 0: disabled 1: enabled

PHY_SKEW_LINK0

PHY_SKEW_LINK0 is a link 0 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0004	PHY_SKEW_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phy0_d3_skew				reserved	phy0_d2_skew			reserved	phy0_d1_skew			reserved	phy0_d0_skew			reserved	phy0_clk_skew		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	phy0_d3_skew	Timing delay adjustment for data lane 3. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[15]	RO	reserved	Reserved
[14:12]	RW	phy0_d2_skew	Timing delay adjustment for data lane 2. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[11]	RO	reserved	Reserved
[10:8]	RW	phy0_d1_skew	Timing delay adjustment for data lane 1. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[7]	RO	reserved	Reserved
[6:4]	RW	phy0_d0_skew	Timing delay adjustment for data lane 0. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[3]	RO	reserved	Reserved
[2:0]	RW	phy0_clk_skew	Timing delay adjustment for the clock lane. The phase is delayed by about 62.5 ps each time the register value increases by 1.

PHY_EN_LINK0

PHY_EN_LINK0 is a link 0 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0008	PHY_EN_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							phy0_clk_term_en	phy0_d3_term_en	phy0_d2_term_en	phy0_d1_term_en	phy0_d0_term_en	phy0_da_d3_valid	phy0_da_d2_valid	phy0_da_d1_valid	phy0_da_d0_valid
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	phy0_clk_term_en	Termination matched impedance enable for the clock lane 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[7]	RW	phy0_d3_term_en	Termination matched impedance enable for data lane 3 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[6]	RW	phy0_d2_term_en	Termination matched impedance enable for data lane 2 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[5]	RW	phy0_d1_term_en	Termination matched impedance enable for data lane 1 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[4]	RW	phy0_d0_term_en	Termination matched impedance enable for data lane 0 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[3]	RW	phy0_da_d3_valid	High-speed mode enable for data lane 3 0: disabled 1: enabled
[2]	RW	phy0_da_d2_valid	High-speed mode enable for data lane 2 0: disabled 1: enabled
[1]	RW	phy0_da_d1_valid	High-speed mode enable for data lane 1 0: disabled 1: enabled

[0]	RW	phy0_da_d0_valid	High-speed mode enable for data lane 0 0: disabled 1: enabled

PHY_DATA_LINK0

PHY_DATA_LINK0 is a link 0 PHY output parallel data register.

Offset Address	Register Name	Total Reset Value
0x0018	PHY_DATA_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_data3_mipi								phy0_data2_mipi								phy0_data1_mipi								phy0_data0_mipi							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi	Data received by data lane 3
[23:16]	RO	phy0_data2_mipi	Data received by data lane 2
[15:8]	RO	phy0_data1_mipi	Data received by data lane 1
[7:0]	RO	phy0_data0_mipi	Data received by data lane 0

PHY_PH_MIPI_LINK0

PHY_PH_MIPI_LINK0 is a link 0 MIPI data packet header register.

Offset Address	Register Name	Total Reset Value
0x001C	PHY_PH_MIPI_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_ph3_mipi								phy0_ph2_mipi								phy0_ph1_mipi								phy0_ph0_mipi							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	phy0_ph3_mipi	Data packet header received by data lane 3
[23:16]	RO	phy0_ph2_mipi	Data packet header received by data lane 2
[15:8]	RO	phy0_ph1_mipi	Data packet header received by data lane 1
[7:0]	RO	phy0_ph0_mipi	Data packet header received by data lane 0

PHY_DATA_MIPI_LINK0

PHY_DATA_MIPI_LINK0 is a link 0 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0020	PHY_DATA_MIPI_LINK0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy0_data3_mipi_hs		phy0_data2_mipi_hs		phy0_data1_mipi_hs		phy0_data0_mipi_hs	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi_hs	MIPI data for data lane 3
[23:16]	RO	phy0_data2_mipi_hs	MIPI data for data lane 2
[15:8]	RO	phy0_data1_mipi_hs	MIPI data for data lane 1
[7:0]	RO	phy0_data0_mipi_hs	MIPI data for data lane 0

PHY_SYNC_DCT_LINK0

PHY_SYNC_DCT_LINK0 is a link 0 PHY LVDS mode synchronization header detection control register.

Offset Address	Register Name	Total Reset Value
0x0024	PHY_SYNC_DCT_LINK0	0x0000_0101

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved

[8]	RW	cil0_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received synchronization code is bit 0, bit 1, …, bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received synchronization code is bit 11, bit 10, …, bit 0.
[7]	RO	reserved	Reserved
[6:4]	RW	cil0_split_mode	Transfer type for the synchronization code in LVDS or HiSPI mode 000: per lane mode Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	cil0_raw_type	Type of the raw data to be transmitted in LVDS or HiSPI mode 001: 8-bit raw data 010: 10-bit raw data 011: 12-bit raw data 100: 14-bit raw data 101: 16-bit raw data Other values: reserved

PHY_SYNC_CODE0_LINK0

PHY_SYNC_CODE0_LINK0 is link 0 PHY LVDS mode synchronization header register 0.

Offset Address	Register Name	Total Reset Value
0x0030	PHY_SYNC_CODE0_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_0																cil0_sof0_word4_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_0	Lane 0 SOF synchronization code (for frame $N+1$)
[15:0]	RW	cil0_sof0_word4_0	Lane 0 SOF synchronization code (for frame N)

PHY_SYNC_CODE1_LINK0

PHY_SYNC_CODE1_LINK0 is link 0 PHY LVDS mode synchronization header register 1.

Offset Address	Register Name	Total Reset Value
0x0034	PHY_SYNC_CODE1_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_1																cil0_sof0_word4_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_1	Lane 1 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_1	Lane 1 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE2_LINK0

PHY_SYNC_CODE2_LINK0 is link 0 PHY LVDS mode synchronization header register 2.

Offset Address	Register Name	Total Reset Value
0x0038	PHY_SYNC_CODE2_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_2																cil0_sof0_word4_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_2	Lane 2 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_2	Lane 2 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE3_LINK0

PHY_SYNC_CODE3_LINK0 is link 0 PHY LVDS mode synchronization header register 3.

Offset Address	Register Name	Total Reset Value
0x003C	PHY_SYNC_CODE3_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_3																cil0_sof0_word4_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_3	Lane 3 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_3	Lane 3 SOF synchronization code (for frame *N*)

MIPI_CIL_INT_RAW_LINK0

MIPI_CIL_INT_RAW_LINK0 is a link 0 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F0	MIPI_CIL_INT_RAW_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err0_timeout_ck_raw	err0_timeout_d3_raw	err0_timeout_d2_raw	err0_timeout_d1_raw	err0_timeout_d0_raw	reserved				err0_escape_ck_raw	err0_escape_d3_raw	err0_escape_d2_raw	err0_escape_d1_raw	err0_escape_d0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	err0_timeout_ck_raw	Status of the raw FSM timeout interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	err0_timeout_d3_raw	Status of the raw FSM timeout interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	WC	err0_timeout_d2_raw	Status of the raw FSM timeout interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	WC	err0_timeout_d1_raw	Status of the raw FSM timeout interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	err0_timeout_d0_raw	Status of the raw FSM timeout interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	WC	err0_escape_ck_raw	Status of the raw escape sequence interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[3]	WC	err0_escape_d3_raw	Status of the raw escape sequence interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err0_escape_d2_raw	Status of the raw escape sequence interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err0_escape_d1_raw	Status of the raw escape sequence interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err0_escape_d0_raw	Status of the raw escape sequence interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI_CIL_INT_LINK0

MIPI_CIL_INT_LINK0 is a link 0 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F4	MIPI_CIL_INT_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err0_timeout_ck_st	err0_timeout_d3_st	err0_timeout_d2_st	err0_timeout_d1_st	err0_timeout_d0_st	reserved				err0_escape_ck_st	err0_escape_d3_st	err0_escape_d2_st	err0_escape_d1_st	err0_escape_d0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	err0_timeout_ck_st	Status of the FSM timeout interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	err0_timeout_d3_st	Status of the FSM timeout interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.

[10]	RO	err0_timeout_d2_st	Status of the FSM timeout interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	err0_timeout_d1_st	Status of the FSM timeout interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	err0_timeout_d0_st	Status of the FSM timeout interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	RO	err0_escape_ck_st	Status of the escape sequence interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err0_escape_d3_st	Status of the escape sequence interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err0_escape_d2_st	Status of the escape sequence interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err0_escape_d1_st	Status of the escape sequence interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err0_escape_d0_st	Status of the escape sequence interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CIL_INT_MSK_LINK0

MIPI_CIL_INT_MSK_LINK0 is a link 0 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	MIPI_CIL_INT_MSK_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err0_timeout_ck_msk	err0_timeout_d3_msk	err0_timeout_d2_msk	err0_timeout_d1_msk	err0_timeout_d0_msk	reserved				err0_escape_ck_msk	err0_escape_d3_msk	err0_escape_d2_msk	err0_escape_d1_msk	err0_escape_d0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	err0_timeout_ck_msk	Enable of the FSM timeout interrupt for the clock lane 0: masked 1: enabled
[11]	RW	err0_timeout_d3_msk	Enable of the FSM timeout interrupt for data lane 3 0: masked 1: enabled
[10]	RW	err0_timeout_d2_msk	Enable of the FSM timeout interrupt for data lane 2 0: masked 1: enabled
[9]	RW	err0_timeout_d1_msk	Enable of the FSM timeout interrupt for data lane 1 0: masked 1: enabled
[8]	RW	err0_timeout_d0_msk	Enable of the FSM timeout interrupt for data lane 0 0: masked 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	err0_escape_ck_msk	Enable of the escape sequence interrupt for the clock lane 0: masked 1: enabled
[3]	RW	err0_escape_d3_msk	Enable of the escape sequence interrupt for data lane 3 0: masked 1: enabled

[2]	RW	err0_escape_d2_msk	Enable of the escape sequence interrupt for data lane 2 0: masked 1: enabled
[1]	RW	err0_escape_d1_msk	Enable of the escape sequence interrupt for data lane 1 0: masked 1: enabled
[0]	RW	err0_escape_d0_msk	Enable of the escape sequence interrupt for data lane 0 0: masked 1: enabled

PHY_MODE_LINK1

PHY_MODE_LINK1 is a link 1 PHY operating mode register.

Offset Address	Register Name	Total Reset Value
0x0200	PHY_MODE_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phy1_rg_mipi_mode	reserved			phy1_rg_ext_clk_en	reserved			phy1_rg_faclk_en	reserved			phy1_rg_en_lp	reserved			phy1_rg_en_cmos	reserved			phy1_rg_en_clk	phy1_rg_en_d			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	phy1_rg_mipi_mode	MIPI/LVDS input mode select. This field is set to 0 when the PHY works in LVDS mode and the common voltage is greater than or equal to 900 mV. 0: The common voltage is 900 mV or higher. 1: The common voltage is lower than 900 mV.
[23:21]	RO	reserved	Reserved
[20]	RW	phy1_rg_ext_clk_en	Differential clock source select 0: PAD input differential clock 1: differential clock of other links
[19:17]	RO	reserved	Reserved

[16]	RW	phy1_rg_faclk_en	Phase of the associated clock for the PHY output data 0: Data is output at the rising edge of the clock. 1: Data is output at the falling edge of the clock.
[15:13]	RO	reserved	Reserved
[12]	RW	phy1_rg_en_lp	PHY LP mode enable. The LP mode is enabled in MIPI mode and disabled in other modes. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved
[8]	RW	phy1_rg_en_cmos	PHY CMOS mode enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	phy1_rg_en_clk	Clock lane enable 0: disabled 1: enabled
[3:0]	RW	phy1_rg_en_d	Data lane enable 0: disabled 1: enabled

PHY_SKEW_LINK1

PHY_SKEW_LINK1 is a link 1 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0204	PHY_SKEW_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phy1_d3_skew				reserved				phy1_d2_skew				reserved				phy1_d1_skew				reserved				phy1_d0_skew				reserved				phy1_clk_skew			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	phy1_d3_skew	Timing delay adjustment for data lane 3. The phase is delayed by about 62.5 ps each time the register value increases by 1.

[15]	RO	reserved	Reserved
[14:12]	RW	phy1_d2_skew	Timing delay adjustment for data lane 2. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[11]	RO	reserved	Reserved
[10:8]	RW	phy1_d1_skew	Timing delay adjustment for data lane 1. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[7]	RO	reserved	Reserved
[6:4]	RW	phy1_d0_skew	Timing delay adjustment for data lane 0. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[3]	RO	reserved	Reserved
[2:0]	RW	phy1_clk_skew	Timing delay adjustment for the clock lane. The phase is delayed by about 62.5 ps each time the register value increases by 1.

PHY_EN_LINK1

PHY_EN_LINK1 is a link 1 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0208	PHY_EN_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							phy1_clk_term_en	phy1_d3_term_en	phy1_d2_term_en	phy1_d1_term_en	phy1_d0_term_en	phy1_da_d3_valid	phy1_da_d2_valid	phy1_da_d1_valid	phy1_da_d0_valid
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	phy1_clk_term_en	Termination matched impedance enable for the clock lane 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[7]	RW	phy1_d3_term_en	Termination matched impedance enable for data lane 3 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.

[6]	RW	phy1_d2_term_en	Termination matched impedance enable for data lane 2 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[5]	RW	phy1_d1_term_en	Termination matched impedance enable for data lane 1 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[4]	RW	phy1_d0_term_en	Termination matched impedance enable for data lane 0 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[3]	RW	phy1_da_d3_valid	High-speed mode enable for data lane 3 0: disabled 1: enabled
[2]	RW	phy1_da_d2_valid	High-speed mode enable for data lane 2 0: disabled 1: enabled
[1]	RW	phy1_da_d1_valid	High-speed mode enable for data lane 1 0: disabled 1: enabled
[0]	RW	phy1_da_d0_valid	High-speed mode enable for data lane 0 0: disabled 1: enabled

PHY_DATA_LINK1

PHY_DATA_LINK1 is a link 1 PHY output parallel data register.

Offset Address	Register Name	Total Reset Value
0x0218	PHY_DATA_LINK1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy1_data3_mipi		phy1_data2_mipi		phy1_data1_mipi		phy1_data0_mipi	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_data3_mipi	Data received by data lane 3
[23:16]	RO	phy1_data2_mipi	Data received by data lane 2
[15:8]	RO	phy1_data1_mipi	Data received by data lane 1
[7:0]	RO	phy1_data0_mipi	Data received by data lane 0

PHY_PH_MIPI_LINK1

PHY_PH_MIPI_LINK1 is a link 1 MIPI data packet header register.

Offset Address	Register Name	Total Reset Value
0x021C	PHY_PH_MIPI_LINK1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy1_ph3_mipi		phy1_ph2_mipi		phy1_ph1_mipi		phy1_ph0_mipi	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_ph3_mipi	Data packet header received by data lane 3
[23:16]	RO	phy1_ph2_mipi	Data packet header received by data lane 2
[15:8]	RO	phy1_ph1_mipi	Data packet header received by data lane 1
[7:0]	RO	phy1_ph0_mipi	Data packet header received by data lane 0

PHY_DATA_MIPI_LINK1

PHY_DATA_MIPI_LINK1 is a link 1 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0220	PHY_DATA_MIPI_LINK1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy1_data3_mipi_hs		phy1_data2_mipi_hs		phy1_data1_mipi_hs		phy1_data0_mipi_hs	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy1_data3_mipi_hs	MIPI data for data lane 3
[23:16]	RO	phy1_data2_mipi_hs	MIPI data for data lane 2
[15:8]	RO	phy1_data1_mipi_hs	MIPI data for data lane 1
[7:0]	RO	phy1_data0_mipi_hs	MIPI data for data lane 0

PHY_SYNC_DCT_LINK1

PHY_SYNC_DCT_LINK1 is a link 1 PHY LVDS mode synchronization header detection control register.

Offset Address	Register Name	Total Reset Value
0x0224	PHY_SYNC_DCT_LINK1	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							cil1_code_big_endian	reserved			cil1_split_mode	reserved			cil1_raw_type
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	cil1_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received synchronization code is bit 0, bit 1, …, bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received synchronization code is bit 11, bit 10, …, bit 0.
[7]	RO	reserved	Reserved
[6:4]	RW	cil1_split_mode	Transfer type for the synchronization code in LVDS or HiSPI mode 000: per lane mode Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	cil1_raw_type	Type of the raw data to be transmitted in LVDS or HiSPI mode 001: 8-bit raw data 010: 10-bit raw data 011: 12-bit raw data 100: 14-bit raw data 101: 16-bit raw data Other values: reserved

PHY_SYNC_CODE0_LINK1

PHY_SYNC_CODE0_LINK1 is link 1 PHY LVDS mode synchronization header register 0.

Offset Address	Register Name	Total Reset Value
0x0230	PHY_SYNC_CODE0_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil1_sof1_word4_0																cil1_sof0_word4_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_0	Lane 0 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil1_sof0_word4_0	Lane 0 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE1_LINK1

PHY_SYNC_CODE1_LINK1 is link 1 PHY LVDS mode synchronization header register 1.

Offset Address	Register Name	Total Reset Value
0x0234	PHY_SYNC_CODE1_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil1_sof1_word4_1																cil1_sof0_word4_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_1	Lane 1 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil1_sof0_word4_1	Lane 1 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE2_LINK1

PHY_SYNC_CODE2_LINK1 is link 1 PHY LVDS mode synchronization header register 2.

Offset Address	Register Name	Total Reset Value
0x0238	PHY_SYNC_CODE2_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil1_sof1_word4_2																cil1_sof0_word4_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_2	Lane 2 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil1_sof0_word4_2	Lane 2 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE3_LINK1

PHY_SYNC_CODE3_LINK1 is link 1 PHY LVDS mode synchronization header register 3.

Offset Address	Register Name	Total Reset Value
0x023C	PHY_SYNC_CODE3_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil1_sof1_word4_3																cil1_sof0_word4_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil1_sof1_word4_3	Lane 3 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil1_sof0_word4_3	Lane 3 SOF synchronization code (for frame *N*)

MIPI_CIL_INT_RAW_LINK1

MIPI_CIL_INT_RAW_LINK1 is a link 1 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x03F0	MIPI_CIL_INT_RAW_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				err1_timeout_ck_raw	err1_timeout_d3_raw	err1_timeout_d2_raw	err1_timeout_d1_raw	err1_timeout_d0_raw	reserved				err1_escape_ck_raw	err1_escape_d3_raw	err1_escape_d2_raw	err1_escape_d1_raw	err1_escape_d0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	err1_timeout_ck_raw	Status of the raw FSM timeout interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	err1_timeout_d3_raw	Status of the raw FSM timeout interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[10]	WC	err1_timeout_d2_raw	Status of the raw FSM timeout interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	WC	err1_timeout_d1_raw	Status of the raw FSM timeout interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	err1_timeout_d0_raw	Status of the raw FSM timeout interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	WC	err1_escape_ck_raw	Status of the raw escape sequence interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	err1_escape_d3_raw	Status of the raw escape sequence interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err1_escape_d2_raw	Status of the raw escape sequence interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err1_escape_d1_raw	Status of the raw escape sequence interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err1_escape_d0_raw	Status of the raw escape sequence interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI_CIL_INT_LINK1

MIPI_CIL_INT_LINK1 is a link 1 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x03F4	MIPI_CIL_INT_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err1_timeout_ck_st	err1_timeout_d3_st	err1_timeout_d2_st	err1_timeout_d1_st	err1_timeout_d0_st	reserved				err1_escape_ck_st	err1_escape_d3_st	err1_escape_d2_st	err1_escape_d1_st	err1_escape_d0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	err1_timeout_ck_st	Status of the FSM timeout interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	err1_timeout_d3_st	Status of the FSM timeout interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	err1_timeout_d2_st	Status of the FSM timeout interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	err1_timeout_d1_st	Status of the FSM timeout interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	err1_timeout_d0_st	Status of the FSM timeout interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	RO	err1_escape_ck_st	Status of the escape sequence interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err1_escape_d3_st	Status of the escape sequence interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.

[2]	RO	err1_escape_d2_st	Status of the escape sequence interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err1_escape_d1_st	Status of the escape sequence interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err1_escape_d0_st	Status of the escape sequence interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CIL_INT_MSK_LINK1

MIPI_CIL_INT_MSK_LINK1 is a link 1 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x03F8	MIPI_CIL_INT_MSK_LINK1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err1_timeout_ck_msk	err1_timeout_d3_msk	err1_timeout_d2_msk	err1_timeout_d1_msk	err1_timeout_d0_msk	reserved				err1_escape_ck_msk	err1_escape_d3_msk	err1_escape_d2_msk	err1_escape_d1_msk	err1_escape_d0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	err1_timeout_ck_msk	Enable of the FSM timeout interrupt for the clock lane 0: masked 1: enabled
[11]	RW	err1_timeout_d3_msk	Enable of the FSM timeout interrupt for data lane 3 0: masked 1: enabled
[10]	RW	err1_timeout_d2_msk	Enable of the FSM timeout interrupt for data lane 2 0: masked 1: enabled

[9]	RW	err1_timeout_d1_msk	Enable of the FSM timeout interrupt for data lane 1 0: masked 1: enabled
[8]	RW	err1_timeout_d0_msk	Enable of the FSM timeout interrupt for data lane 0 0: masked 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	err1_escape_ck_msk	Enable of the escape sequence interrupt for the clock lane 0: masked 1: enabled
[3]	RW	err1_escape_d3_msk	Enable of the escape sequence interrupt for data lane 3 0: masked 1: enabled
[2]	RW	err1_escape_d2_msk	Enable of the escape sequence interrupt for data lane 2 0: masked 1: enabled
[1]	RW	err1_escape_d1_msk	Enable of the escape sequence interrupt for data lane 1 0: masked 1: enabled
[0]	RW	err1_escape_d0_msk	Enable of the escape sequence interrupt for data lane 0 0: masked 1: enabled

PHY_MODE_LINK2

PHY_MODE_LINK2 is a link 2 PHY operating mode register.

Offset Address	Register Name	Total Reset Value
0x0400	PHY_MODE_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							phy2_rg_mipi_mode	reserved			phy2_rg_ext_clk_en	reserved			phy2_rg_faclk_en	reserved			phy2_rg_en_lp	reserved			phy2_rg_en_cmos	reserved			phy2_rg_en_clk	phy2_rg_en_d			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	phy2_rg_mipi_mode	MIPI/LVDS input mode select. This field is set to 0 when the PHY works in LVDS mode and the common voltage is greater than or equal to 900 mV. 0: The common voltage is 900 mV or higher. 1: The common voltage is lower than 900 mV.
[23:21]	RO	reserved	Reserved
[20]	RW	phy2_rg_ext_clk_en	Differential clock source select 0: PAD input differential clock 1: differential clock of other links
[19:17]	RO	reserved	Reserved
[16]	RW	phy2_rg_faclk_en	Phase of the associated clock for the PHY output data 0: Data is output at the rising edge of the clock. 1: Data is output at the falling edge of the clock.
[15:13]	RO	reserved	Reserved
[12]	RW	phy2_rg_en_lp	PHY LP mode enable. The LP mode is enabled in MIPI mode and disabled in other modes. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved
[8]	RW	phy2_rg_en_cmos	PHY CMOS mode enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved

[4]	RW	phy2_rg_en_clk	Clock lane enable 0: disabled 1: enabled
[3:0]	RW	phy2_rg_en_d	Data lane enable 0: disabled 1: enabled

PHY_SKEW_LINK2

PHY_SKEW_LINK2 is a link 2 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0404	PHY_SKEW_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phy2_d3_skew				reserved	phy2_d2_skew			reserved	phy2_d1_skew			reserved	phy2_d0_skew			reserved	phy2_clk_skew		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	phy2_d3_skew	Timing delay adjustment for data lane 3. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[15]	RO	reserved	Reserved
[14:12]	RW	phy2_d2_skew	Timing delay adjustment for data lane 2. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[11]	RO	reserved	Reserved
[10:8]	RW	phy2_d1_skew	Timing delay adjustment for data lane 1. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[7]	RO	reserved	Reserved
[6:4]	RW	phy2_d0_skew	Timing delay adjustment for data lane 0. The phase is delayed by about 62.5 ps each time the register value increases by 1.
[3]	RO	reserved	Reserved
[2:0]	RW	phy2_clk_skew	Timing delay adjustment for the clock lane. The phase is delayed by about 62.5 ps each time the register value increases by 1.

PHY_EN_LINK2

PHY_EN_LINK2 is a link 2 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0408	PHY_EN_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							phy2_clk_term_en	phy2_d3_term_en	phy2_d2_term_en	phy2_d1_term_en	phy2_d0_term_en	phy2_da_d3_valid	phy2_da_d2_valid	phy2_da_d1_valid	phy2_da_d0_valid
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	phy2_clk_term_en	Termination matched impedance enable for the clock lane 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[7]	RW	phy2_d3_term_en	Termination matched impedance enable for data lane 3 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[6]	RW	phy2_d2_term_en	Termination matched impedance enable for data lane 2 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[5]	RW	phy2_d1_term_en	Termination matched impedance enable for data lane 1 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[4]	RW	phy2_d0_term_en	Termination matched impedance enable for data lane 0 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[3]	RW	phy2_da_d3_valid	High-speed mode enable for data lane 3 0: disabled 1: enabled
[2]	RW	phy2_da_d2_valid	High-speed mode enable for data lane 2 0: disabled 1: enabled

[1]	RW	phy2_da_d1_valid	High-speed mode enable for data lane 1 0: disabled 1: enabled
[0]	RW	phy2_da_d0_valid	High-speed mode enable for data lane 0 0: disabled 1: enabled

PHY_DATA_LINK2

PHY_DATA_LINK2 is a link 2 PHY output parallel data register.

Offset Address	Register Name	Total Reset Value
0x0418	PHY_DATA_LINK2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy2_data3_mipi		phy2_data2_mipi		phy2_data1_mipi		phy2_data0_mipi	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_data3_mipi	Data received by data lane 3
[23:16]	RO	phy2_data2_mipi	Data received by data lane 2
[15:8]	RO	phy2_data1_mipi	Data received by data lane 1
[7:0]	RO	phy2_data0_mipi	Data received by data lane 0

PHY_PH_MIPI_LINK2

PHY_PH_MIPI_LINK2 is a link 2 MIPI data packet header register.

Offset Address	Register Name	Total Reset Value
0x041C	PHY_PH_MIPI_LINK2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy2_ph3_mipi		phy2_ph2_mipi		phy2_ph1_mipi		phy2_ph0_mipi	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_ph3_mipi	Data packet header received by data lane 3
[23:16]	RO	phy2_ph2_mipi	Data packet header received by data lane 2
[15:8]	RO	phy2_ph1_mipi	Data packet header received by data lane 1
[7:0]	RO	phy2_ph0_mipi	Data packet header received by data lane 0

PHY_DATA_MIPI_LINK2

PHY_DATA_MIPI_LINK2 is a link 2 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0420	PHY_DATA_MIPI_LINK2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy2_data3_mipi_hs		phy2_data2_mipi_hs		phy2_data1_mipi_hs		phy2_data0_mipi_hs	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy2_data3_mipi_hs	MIPI data for data lane 3
[23:16]	RO	phy2_data2_mipi_hs	MIPI data for data lane 2
[15:8]	RO	phy2_data1_mipi_hs	MIPI data for data lane 1
[7:0]	RO	phy2_data0_mipi_hs	MIPI data for data lane 0

PHY_SYNC_DCT_LINK2

PHY_SYNC_DCT_LINK2 is a link 2 PHY LVDS mode synchronization header detection control register.

Offset Address	Register Name	Total Reset Value
0x0424	PHY_SYNC_DCT_LINK2	0x0000_0101

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved

[8]	RW	cil2_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received synchronization code is bit 0, bit 1, …, bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received synchronization code is bit 11, bit 10, …, bit 0.
[7]	RO	reserved	Reserved
[6:4]	RW	cil2_split_mode	Transfer type for the synchronization code in LVDS or HiSPI mode 000: per lane mode Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	cil2_raw_type	Type of the raw data to be transmitted in LVDS or HiSPI mode 001: 8-bit raw data 010: 10-bit raw data 011: 12-bit raw data 100: 14-bit raw data 101: 16-bit raw data Other values: reserved

PHY_SYNC_CODE0_LINK2

PHY_SYNC_CODE0_LINK2 is link 2 PHY LVDS mode synchronization header register 0.

Offset Address	Register Name	Total Reset Value
0x0430	PHY_SYNC_CODE0_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil2_sof1_word4_0																cil2_sof0_word4_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil2_sof1_word4_0	Lane 0 SOF synchronization code (for frame $N+1$)
[15:0]	RW	cil2_sof0_word4_0	Lane 0 SOF synchronization code (for frame N)

PHY_SYNC_CODE1_LINK2

PHY_SYNC_CODE1_LINK2 is link 2 PHY LVDS mode synchronization header register 1.

Offset Address	Register Name	Total Reset Value
0x0434	PHY_SYNC_CODE1_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil2_sof1_word4_1																cil2_sof0_word4_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil2_sof1_word4_1	Lane 1 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil2_sof0_word4_1	Lane 1 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE2_LINK2

PHY_SYNC_CODE2_LINK2 is link 2 PHY LVDS mode synchronization header register 2.

Offset Address	Register Name	Total Reset Value
0x0438	PHY_SYNC_CODE2_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil2_sof1_word4_2																cil2_sof0_word4_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil2_sof1_word4_2	Lane 2 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil2_sof0_word4_2	Lane 2 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE3_LINK2

PHY_SYNC_CODE3_LINK2 is link 2 PHY LVDS mode synchronization header register 3.

Offset Address	Register Name	Total Reset Value
0x043C	PHY_SYNC_CODE3_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil2_sof1_word4_3																cil2_sof0_word4_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil2_sof1_word4_3	Lane 3 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil2_sof0_word4_3	Lane 3 SOF synchronization code (for frame *N*)

MIPI_CIL_INT_RAW_LINK2

MIPI_CIL_INT_RAW_LINK2 is a link 2 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x05F0	MIPI_CIL_INT_RAW_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err2_timeout_ck_raw	err2_timeout_d3_raw	err2_timeout_d2_raw	err2_timeout_d1_raw	err2_timeout_d0_raw	reserved				err2_escape_ck_raw	err2_escape_d3_raw	err2_escape_d2_raw	err2_escape_d1_raw	err2_escape_d0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	err2_timeout_ck_raw	Status of the raw FSM timeout interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	err2_timeout_d3_raw	Status of the raw FSM timeout interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	WC	err2_timeout_d2_raw	Status of the raw FSM timeout interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	WC	err2_timeout_d1_raw	Status of the raw FSM timeout interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	err2_timeout_d0_raw	Status of the raw FSM timeout interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	WC	err2_escape_ck_raw	Status of the raw escape sequence interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[3]	WC	err2_escape_d3_raw	Status of the raw escape sequence interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err2_escape_d2_raw	Status of the raw escape sequence interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err2_escape_d1_raw	Status of the raw escape sequence interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err2_escape_d0_raw	Status of the raw escape sequence interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI_CIL_INT_LINK2

MIPI_CIL_INT_LINK2 is a link 2 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x05F4	MIPI_CIL_INT_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err2_timeout_ck_st	err2_timeout_d3_st	err2_timeout_d2_st	err2_timeout_d1_st	err2_timeout_d0_st	reserved				err2_escape_ck_st	err2_escape_d3_st	err2_escape_d2_st	err2_escape_d1_st	err2_escape_d0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	err2_timeout_ck_st	Status of the FSM timeout interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	err2_timeout_d3_st	Status of the FSM timeout interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.

[10]	RO	err2_timeout_d2_st	Status of the FSM timeout interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	err2_timeout_d1_st	Status of the FSM timeout interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	err2_timeout_d0_st	Status of the FSM timeout interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	RO	err2_escape_ck_st	Status of the escape sequence interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err2_escape_d3_st	Status of the escape sequence interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err2_escape_d2_st	Status of the escape sequence interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err2_escape_d1_st	Status of the escape sequence interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err2_escape_d0_st	Status of the escape sequence interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CIL_INT_MSK_LINK2

MIPI_CIL_INT_MSK_LINK2 is a link 2 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x05F8	MIPI_CIL_INT_MSK_LINK2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err2_timeout_ck_msk	err2_timeout_d3_msk	err2_timeout_d2_msk	err2_timeout_d1_msk	err2_timeout_d0_msk	reserved			err2_escape_ck_msk	err2_escape_d3_msk	err2_escape_d2_msk	err2_escape_d1_msk	err2_escape_d0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	err2_timeout_ck_msk	Enable of the FSM timeout interrupt for the clock lane 0: masked 1: enabled
[11]	RW	err2_timeout_d3_msk	Enable of the FSM timeout interrupt for data lane 3 0: masked 1: enabled
[10]	RW	err2_timeout_d2_msk	Enable of the FSM timeout interrupt for data lane 2 0: masked 1: enabled
[9]	RW	err2_timeout_d1_msk	Enable of the FSM timeout interrupt for data lane 1 0: masked 1: enabled
[8]	RW	err2_timeout_d0_msk	Enable of the FSM timeout interrupt for data lane 0 0: masked 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	err2_escape_ck_msk	Enable of the escape sequence interrupt for the clock lane 0: masked 1: enabled
[3]	RW	err2_escape_d3_msk	Enable of the escape sequence interrupt for data lane 3 0: masked 1: enabled

[2]	RW	err2_escape_d2_msk	Enable of the escape sequence interrupt for data lane 2 0: masked 1: enabled
[1]	RW	err2_escape_d1_msk	Enable of the escape sequence interrupt for data lane 1 0: masked 1: enabled
[0]	RW	err2_escape_d0_msk	Enable of the escape sequence interrupt for data lane 0 0: masked 1: enabled

PHY_CHN_CTRL

PHY_CHN_CTRL is a PHY ID selection register.

Offset Address	Register Name	Total Reset Value
0x0800	PHY_CHN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													phy2_en	phy1_en	phy0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	phy2_en	PHY 2 enable 0: disabled 1: enabled
[1]	RW	phy1_en	PHY 1 enable 0: disabled 1: enabled
[0]	RW	phy0_en	PHY 0 enable 0: disabled 1: enabled

PHY_LP_SELECT

PHY_LP_SELECT is a PHY 1 LP mode signal selection register.

Offset Address	Register Name	Total Reset Value
0x0804	PHY_LP_SELECT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							phy1_lp_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	phy1_lp_sel	PHY 1 LP mode signal select 0: The PHY 1 LP signal comes from PHY 1. 1: The PHY 1 LP signal comes from PHY 0.

MIPI_MEM_CTRL

MIPI_MEM_CTRL is a memory control register.

Offset Address	Register Name	Total Reset Value
0x080C	MIPI_MEM_CTRL	0x0000_0331

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				mem_ck_gt	reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 1 1	0 0 0 1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	mem_ck_gt	MIPI memory clock gating enable 0: disabled 1: enabled. The memory port clock is not inverted when the memory is not read or written.
[11:0]	RO	reserved	Reserved

LANE_EN

LANE_EN is a lane enable register.

Offset Address	Register Name	Total Reset Value
0x0810	LANE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lane11_en	lane10_en	lane9_en	lane8_en	lane7_en	lane6_en	lane5_en	lane4_en	lane3_en	lane2_en	lane1_en	lane0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	lane11_en	Lane 11 enable 0: disabled 1: enabled
[10]	RW	lane10_en	Lane 10 enable 0: disabled 1: enabled
[9]	RW	lane9_en	Lane 9 enable 0: disabled 1: enabled
[8]	RW	lane8_en	Lane 8 enable 0: disabled 1: enabled
[7]	RW	lane7_en	Lane 7 enable 0: disabled 1: enabled
[6]	RW	lane6_en	Lane 6 enable 0: disabled 1: enabled
[5]	RW	lane5_en	Lane 5 enable 0: disabled 1: enabled
[4]	RW	lane4_en	Lane 4 enable 0: disabled 1: enabled

[3]	RW	lane3_en	Lane 3 enable 0: disabled 1: enabled
[2]	RW	lane2_en	Lane 2 enable 0: disabled 1: enabled
[1]	RW	lane1_en	Lane 1 enable 0: disabled 1: enabled
[0]	RW	lane0_en	Lane 0 enable 0: disabled 1: enabled

MIPI_PHYCFG_MODE

MIPI_PHYCFG_MODE is an MIPI PHY configuration mode register.

Offset Address	Register Name	Total Reset Value
0x0814	MIPI_PHYCFG_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mipi0_phycfg_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[2:0]	RW	mipi0_phycfg_mode	MIPI 0 PHY configuration mode 000: The PHY configuration is controlled by PHYCFG_EN and FSM. 001: The PHY configuration is controlled by PHYCFG_EN. 010: The PHY configuration is directly controlled by the value of MIPI_PHYCFG_MODE. 011: The PHY configuration is controlled by the value of MIPI_PHYCFG_MODE and FSM. 100: The PHY configuration is controlled by PHYCFG_EN and FSM, and the clock channel enable is controlled by PHYCFG_EN. Other values: reserved

MIPI_PHYCFG_EN

MIPI_PHYCFG_EN is an MIPI PHY configuration enable register.

Offset Address	Register Name	Total Reset Value
0x0818	MIPI_PHYCFG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															chn0_phycfg_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	chn0_phycfg_en	MIPI 0 PHY configuration enable 0: disabled 1: enabled

MIPI_CIL_CTRL

MIPI_CIL_CTRL is an MIPI CIL control register.

Offset Address	Register Name	Total Reset Value
0x081C	MIPI_CIL_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										clr_en_align	clr_en_lvds	reserved	phycil2_cken	phycil1_cken	phycil0_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	clr_en_align	Forcible set control for the LVDS PRE SYNC module 0: The ALIGN set request is disabled. 1: The ALIGN set request is enabled.
[4]	RW	clr_en_lvds	Forcible set control for the LVDS PRE SYNC module 0: The LVDS CTRL set request is disabled. 1: The LVDS CTRL set request is enabled.
[3]	RO	reserved	Reserved
[2]	RW	phycil2_cken	PHYCIL2 clock gating 0: disabled 1: enabled
[1]	RW	phycil1_cken	PHYCIL1 clock gating 0: disabled 1: enabled
[0]	RW	phycil0_cken	PHYCIL0 clock gating 0: disabled 1: enabled

MIPI_SRST_CFG

MIPI_SRST_CFG is an MIPI core soft reset register.

Offset Address	Register Name	Total Reset Value
0x0820	MIPI_SRST_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mipi_srst_aux
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mipi_srst_aux	MIPI core soft reset 0: not reset 1: reset This reset signal does not affect the register value.

MIPI_CHN0_INT_RAW

MIPI_CHN0_INT_RAW is an MIPI channel 0 raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF0	MIPI_CHN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									int_data_align_raw	int_mipi_ctrl_raw	int_mipi_csi_raw	int_lvds_ctrl_raw	int_phycil2_raw	int_phycil1_raw	int_phycil0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	WC	int_data_align_raw	MIPI ALIGN raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[5]	WC	int_mipi_ctrl_raw	MIPI CTRL raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	WC	int_mipi_csi_raw	MIPI CSI2 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	int_lvds_ctrl_raw	LVDS CTRL raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	int_phycil2_raw	PHYCIL2 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	int_phycil1_raw	PHYCIL1 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	int_phycil0_raw	PHYCIL0 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI_CHN0_INT

MIPI_CHN0_INT is an MIPI channel 0 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF4	MIPI_CHN0_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int_data_align_st	int_mipi_ctrl_st	int_mipi_csi_st	int_lvds_ctrl_st	int_phycil2_st	int_phycil1_st	int_phycil0_st	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6]	RO	int_data_align_st	MIPI ALIGN interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_mipi_ctrl_st	MIPI CTRL interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	int_mipi_csi_st	MIPI CSI2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_lvds_ctrl_st	LVDS CTRL interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_phycil2_st	PHYCIL2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_phycil1_st	PHYCIL1 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_phycil0_st	PHYCIL0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CHN0_INT_MSK

MIPI_CHN0_INT_MSK is an MIPI channel 0 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0EF8	MIPI_CHN0_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									int_data_align_msk	int_mipi_ctrl_msk	int_mipi_csi_msk	int_lvds_ctrl_msk	int_phycil2_msk	int_phycil1_msk	int_phycil0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	int_data_align_msk	MIPI ALIGN interrupt enable 0: masked 1: enabled
[5]	RW	int_mipi_ctrl_msk	MIPI CTRL interrupt enable 0: masked 1: enabled
[4]	RW	int_mipi_csi_msk	MIPI CSI2 interrupt enable 0: masked 1: enabled
[3]	RW	int_lvds_ctrl_msk	LVDS CTRL interrupt enable 0: masked 1: enabled
[2]	RW	int_phycil2_msk	PHYCIL2 interrupt enable 0: masked 1: enabled
[1]	RW	int_phycil1_msk	PHYCIL1 interrupt enable 0: masked 1: enabled
[0]	RW	int_phycil0_msk	PHYCIL0 interrupt enable 0: masked 1: enabled

MIPI0_LANES_NUM

MIPI0_LANES_NUM is an MIPI 0 enabled data channel quantity register.

Offset Address	Register Name	Total Reset Value
0x1004	MIPI0_LANES_NUM	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														lane_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	lane_num	Number of enabled data channels 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8

MIPI0_MAIN_INT_ST

MIPI0_MAIN_INT_ST is an MIPI 0 global interrupt status register.

Offset Address	Register Name	Total Reset Value
0x100C	MIPI0_MAIN_INT_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													status_int_line	status_int_pkt	reserved													status_int_frame_fatal	status_int_pkt_fatal	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RC	status_int_line	Line interrupt status. This bit is set to 1 when any of the bits in the MIPI0_LINE_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_LINE_INTR_ST must be cleared.
[17]	RC	status_int_pkt	Packet interrupt status. This bit is set to 1 when any of the bits in the MIPI0_PKT_INTR2_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_PKT_INTR2_ST must be cleared.
[16:3]	RO	reserved	Reserved
[2]	RC	status_int_frame_fatal	Frame interrupt status. This bit is set to 1 when any of the bits in the MIPI0_FRAME_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_FRAME_INTR_ST must be cleared.
[1]	RC	status_int_pkt_fatal	Packet interrupt status. This bit is set to 1 when any of the bits in the MIPI0_PKT_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_PKT_INTR_ST must be cleared.
[0]	RO	reserved	Reserved

MIPI0_DI_1

MIPI0_DI_1 is an MIPI 0 controller data ID 1 register.

Offset Address	Register Name	Total Reset Value
0x1010	MIPI0_DI_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	di3_vc	Virtual channel ID of data with the ID 3
[29:24]	RW	di3_dt	Type of data with the ID 3 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[23:22]	RW	di2_vc	Virtual channel ID of data with the ID 2
[21:16]	RW	di2_dt	Type of data with the ID 2 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[15:14]	RW	di1_vc	Virtual channel ID of data with the ID 1
[13:8]	RW	di1_dt	Type of data with the ID 1 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[7:6]	RW	di0_vc	Virtual channel ID of data with the ID 0
[5:0]	RW	di0_dt	Type of data with the ID 0 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved

MIPI0_DI_2

MIPI0_DI_2 is an MIPI 0 controller data ID 2 register.

Offset Address	Register Name	Total Reset Value
0x1014	MIPI0_DI_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	di7_vc		di7_dt						di6_vc		di6_dt						di5_vc		di5_dt						di4_vc		di4_dt					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	di7_vc	Virtual channel ID of data with the ID 7
[29:24]	RW	di7_dt	Type of data with the ID 7 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[23:22]	RW	di6_vc	Virtual channel ID of data with the ID 6
[21:16]	RW	di6_dt	Type of data with the ID 6 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[15:14]	RW	di5_vc	Virtual channel ID of data with the ID 5
[13:8]	RW	di5_dt	Type of data with the ID 5 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved
[7:6]	RW	di4_vc	Virtual channel ID of data with the ID 4

[5:0]	RW	di4_dt	Type of data with the ID 4 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 Other values: reserved

MIPI0_PKT_INTR_ST

MIPI0_PKT_INTR_ST is an MIPI 0 packet interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1060	MIPI0_PKT_INTR_ST	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved				err_ecc_double	reserved		vc3_err_crc	vc2_err_crc	vc1_err_crc	vc0_err_crc
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RC	err_ecc_double	Whether the header has at least two uncorrectable ECC errors. This bit is cleared when it is read. 0: No ECC error occurs. 1: ECC errors occur.
[15:4]	RO	reserved	Reserved
[3]	RC	vc3_err_crc	Whether the VC 3 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes
[2]	RC	vc2_err_crc	Whether the VC 2 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes

[1]	RC	vc1_err_crc	Whether the VC 1 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes
[0]	RC	vc0_err_crc	Whether the VC 0 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes

MIPI0_PKT_INTR_MSK

MIPI0_PKT_INTR_MSK is an MIPI 0 packet interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1064	MIPI0_PKT_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															mask_err_ecc_double	reserved												mask_vc3_err_crc		mask_vc2_err_crc		mask_vc1_err_crc		mask_vc0_err_crc	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	mask_err_ecc_double	err_ecc_double interrupt mask 0: masked 1: enabled
[15:4]	RO	reserved	Reserved
[3]	RW	mask_vc3_err_crc	vc3_err_crc interrupt mask 0: masked 1: enabled
[2]	RW	mask_vc2_err_crc	vc2_err_crc interrupt mask 0: masked 1: enabled

[1]	RW	mask_vc1_err_crc	vc1_err_crc interrupt mask 0: masked 1: enabled
[0]	RW	mask_vc0_err_crc	vc0_err_crc interrupt mask 0: masked 1: enabled

MIPI0_PKT_INTR2_ST

MIPI0_PKT_INTR2_ST is MIPI 0 packet interrupt status register 2.

Offset Address	Register Name	Total Reset Value
0x1070	MIPI0_PKT_INTR2_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												vc3_err_ecc_corrected	vc2_err_ecc_corrected	vc1_err_ecc_corrected	vc0_err_ecc_corrected	reserved												err_id_vc3	err_id_vc2	err_id_vc1	err_id_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RC	vc3_err_ecc_corrected	Whether the VC 3 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[18]	RC	vc2_err_ecc_corrected	Whether the VC 2 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[17]	RC	vc1_err_ecc_corrected	Whether the VC 1 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.

[16]	RC	vc0_err_ecc_corrected	Whether the VC 0 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[15:4]	RO	reserved	Reserved
[3]	RC	err_id_vc3	Whether the VC 3 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported
[2]	RC	err_id_vc2	Whether the VC 2 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported
[1]	RC	err_id_vc1	Whether the VC 1 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported
[0]	RC	err_id_vc0	Whether the VC 0 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported

MIPI0_PKT_INTR2_MSK

MIPI0_PKT_INTR2_MSK is MIPI 0 packet interrupt mask register 2.

Offset Address	Register Name	Total Reset Value
0x1074	MIPI0_PKT_INTR2_MSK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18	17	16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved			mask_vc3_err_ecc_corrected	mask_vc2_err_ecc_corrected	mask_vc1_err_ecc_corrected	mask_vc0_err_ecc_corrected	reserved			mask_err_id_vc3	mask_err_id_vc2	mask_err_id_vc1	mask_err_id_vc0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	mask_vc3_err_ecc_corrected	vc3_err_ecc_corrected interrupt mask 0: masked 1: enabled
[18]	RW	mask_vc2_err_ecc_corrected	vc2_err_ecc_corrected interrupt mask 0: masked 1: enabled
[17]	RW	mask_vc1_err_ecc_corrected	vc1_err_ecc_corrected interrupt mask 0: masked 1: enabled
[16]	RW	mask_vc0_err_ecc_corrected	vc0_err_ecc_corrected interrupt mask 0: masked 1: enabled
[15:4]	RO	reserved	Reserved
[3]	RW	mask_err_id_vc3	err_id_vc3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_id_vc2	err_id_vc2 interrupt mask 0: masked 1: enabled

[1]	RW	mask_err_id_vc1	err_id_vc1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_id_vc0	err_id_vc0 interrupt mask 0: masked 1: enabled

MIPI0_FRAME_INTR_ST

MIPI0_FRAME_INTR_ST is an MIPI 0 frame interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1080	MIPI0_FRAME_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												err_frame_data_vc3	err_frame_data_vc2	err_frame_data_vc1	err_frame_data_vc0	reserved				err_f_seq_vc3	err_f_seq_vc2	err_f_seq_vc1	err_f_seq_vc0	reserved				err_f_bndry_match_vc3	err_f_bndry_match_vc2	err_f_bndry_match_vc1	err_f_bndry_match_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RO	err_frame_data_vc3	Whether the last frame of VC 3 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[18]	RO	err_frame_data_vc2	Whether the last frame of VC 2 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[17]	RO	err_frame_data_vc1	Whether the last frame of VC 1 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.

[16]	RO	err_frame_data_vc0	Whether the last frame of VC 0 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[15:12]	RO	reserved	Reserved
[11]	RO	err_f_seq_vc3	Whether the VC 3 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[10]	RO	err_f_seq_vc2	Whether the VC 2 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[9]	RO	err_f_seq_vc1	Whether the VC 1 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[8]	RO	err_f_seq_vc0	Whether the VC 0 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[7:4]	RO	reserved	Reserved
[3]	RO	err_f_bndry_match_vc3	Whether the SOF matches the EOF for the VC 3 channel. This bit is cleared when it is read. 0: yes 1: no
[2]	RO	err_f_bndry_match_vc2	Whether the SOF matches the EOF for the VC 2 channel. This bit is cleared when it is read. 0: yes 1: no
[1]	RO	err_f_bndry_match_vc1	Whether the SOF matches the EOF for the VC 1 channel. This bit is cleared when it is read. 0: yes 1: no
[0]	RO	err_f_bndry_match_vc0	Whether the SOF matches the EOF for the VC 0 channel. This bit is cleared when it is read. 0: yes 1: no

MIPI0_FRAME_INTR_MSK

MIPI0_FRAME_INTR_MSK is an MIPI 0 frame interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1084	MIPI0_FRAME_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mask_err_frame_data_vc3	mask_err_frame_data_vc2	mask_err_frame_data_vc1	mask_err_frame_data_vc0	reserved				mask_err_f_seq_vc3	mask_err_f_seq_vc2	mask_err_f_seq_vc1	mask_err_f_seq_vc0	reserved				mask_err_f_bndry_match_vc3	mask_err_f_bndry_match_vc2	mask_err_f_bndry_match_vc1	mask_err_f_bndry_match_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	mask_err_frame_data_vc3	err_frame_data_vc3 interrupt mask 0: masked 1: enabled
[18]	RW	mask_err_frame_data_vc2	err_frame_data_vc2 interrupt mask 0: masked 1: enabled
[17]	RW	mask_err_frame_data_vc1	err_frame_data_vc1 interrupt mask 0: masked 1: enabled
[16]	RW	mask_err_frame_data_vc0	err_frame_data_vc0 interrupt mask 0: masked 1: enabled
[15:12]	RO	reserved	Reserved
[11]	RW	mask_err_f_seq_vc3	err_f_seq_vc3 interrupt mask 0: masked 1: enabled
[10]	RW	mask_err_f_seq_vc2	err_f_seq_vc2 interrupt mask 0: masked 1: enabled

[9]	RW	mask_err_f_seq_vc1	err_f_seq_vc1 interrupt mask 0: masked 1: enabled
[8]	RW	mask_err_f_seq_vc0	err_f_seq_vc0 interrupt mask 0: masked 1: enabled
[7:4]	RO	reserved	Reserved
[3]	RW	mask_err_f_bndry_match_vc3	err_f_bndry_match_vc3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_f_bndry_match_vc2	err_f_bndry_match_vc2 interrupt mask 0: masked 1: enabled
[1]	RW	mask_err_f_bndry_match_vc1	err_f_bndry_match_vc1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_f_bndry_match_vc0	err_f_bndry_match_vc0 interrupt mask 0: masked 1: enabled

MIPI0_LINE_INTR_ST

MIPI0_LINE_INTR_ST is an MIPI 0 line interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1090	MIPI0_LINE_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								err_l_seq_di7	err_l_seq_di6	err_l_seq_di5	err_l_seq_di4	err_l_seq_di3	err_l_seq_di2	err_l_seq_di1	err_l_seq_di0	reserved								err_l_bndry_match_di7	err_l_bndry_match_di6	err_l_bndry_match_di5	err_l_bndry_match_di4	err_l_bndry_match_di3	err_l_bndry_match_di2	err_l_bndry_match_di1	err_l_bndry_match_di0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RC	err_l_seq_di7	Whether the line sequence of VC 7 and DT 7 is correct. This bit is cleared when it is read. 0: yes 1: no
[22]	RC	err_l_seq_di6	Whether the line sequence of VC 6 and DT 6 is correct. This bit is cleared when it is read. 0: yes 1: no
[21]	RC	err_l_seq_di5	Whether the line sequence of VC 5 and DT 5 is correct. This bit is cleared when it is read. 0: yes 1: no
[20]	RC	err_l_seq_di4	Whether the line sequence of VC 4 and DT 4 is correct. This bit is cleared when it is read. 0: yes 1: no
[19]	RC	err_l_seq_di3	Whether the line sequence of VC 3 and DT 3 is correct. This bit is cleared when it is read. 0: yes 1: no
[18]	RC	err_l_seq_di2	Whether the line sequence of VC 2 and DT 2 is correct. This bit is cleared when it is read. 0: yes 1: no

[17]	RC	err_l_seq_di1	Whether the line sequence of VC 1 and DT 1 is correct. This bit is cleared when it is read. 0: yes 1: no
[16]	RC	err_l_seq_di0	Whether the line sequence of VC 0 and DT 0 is correct. This bit is cleared when it is read. 0: yes 1: no
[15:8]	RO	reserved	Reserved
[7]	RC	err_l_bndry_match_di7	Whether the SOL matches the EOL for VC 7 and DT 7. This bit is cleared when it is read. 0: yes 1: no
[6]	RC	err_l_bndry_match_di6	Whether the SOL matches the EOL for VC 6 and DT 6. This bit is cleared when it is read. 0: yes 1: no
[5]	RC	err_l_bndry_match_di5	Whether the SOL matches the EOL for VC 5 and DT 5. This bit is cleared when it is read. 0: yes 1: no
[4]	RC	err_l_bndry_match_di4	Whether the SOL matches the EOL for VC 4 and DT 4. This bit is cleared when it is read. 0: yes 1: no
[3]	RC	err_l_bndry_match_di3	Whether the SOL matches the EOL for VC 3 and DT 3. This bit is cleared when it is read. 0: yes 1: no
[2]	RC	err_l_bndry_match_di2	Whether the SOL matches the EOL for VC 2 and DT 2. This bit is cleared when it is read. 0: yes 1: no
[1]	RC	err_l_bndry_match_di1	Whether the SOL matches the EOL for VC 1 and DT 1. This bit is cleared when it is read. 0: yes 1: no
[0]	RC	err_l_bndry_match_di0	Whether the SOL matches the EOL for VC 0 and DT 0. This bit is cleared when it is read. 0: yes 1: no

MIPI0_LINE_INTR_MSK

MIPI0_LINE_INTR_MSK is an MIPI 0 line interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1094	MIPI0_LINE_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mask_err_1_seq_di7	mask_err_1_seq_di6	mask_err_1_seq_di5	mask_err_1_seq_di4	mask_err_1_seq_di3	mask_err_1_seq_di2	mask_err_1_seq_di1	mask_err_1_seq_di0	reserved								mask_err_1_bndry_match_di7	mask_err_1_bndry_match_di6	mask_err_1_bndry_match_di5	mask_err_1_bndry_match_di4	mask_err_1_bndry_match_di3	mask_err_1_bndry_match_di2	mask_err_1_bndry_match_di1	mask_err_1_bndry_match_di0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RW	mask_err_1_seq_di7	err_1_seq_di7 interrupt mask 0: masked 1: enabled
[22]	RW	mask_err_1_seq_di6	err_1_seq_di6 interrupt mask 0: masked 1: enabled
[21]	RW	mask_err_1_seq_di5	err_1_seq_di5 interrupt mask 0: masked 1: enabled
[20]	RW	mask_err_1_seq_di4	err_1_seq_di4 interrupt mask 0: masked 1: enabled
[19]	RW	mask_err_1_seq_di3	err_1_seq_di3 interrupt mask 0: masked 1: enabled

[18]	RW	mask_err_1_seq_di2	err_1_seq_di2 interrupt mask 0: masked 1: enabled
[17]	RW	mask_err_1_seq_di1	err_1_seq_di1 interrupt mask 0: masked 1: enabled
[16]	RW	mask_err_1_seq_di0	err_1_seq_di0 interrupt mask 0: masked 1: enabled
[15:8]	RO	reserved	Reserved
[7]	RW	mask_err_1_bndry_match_di7	err_1_bndry_match_di7 interrupt mask 0: masked 1: enabled
[6]	RW	mask_err_1_bndry_match_di6	err_1_bndry_match_di6 interrupt mask 0: masked 1: enabled
[5]	RW	mask_err_1_bndry_match_di5	err_1_bndry_match_di5 interrupt mask 0: masked 1: enabled
[4]	RW	mask_err_1_bndry_match_di4	err_1_bndry_match_di4 interrupt mask 0: masked 1: enabled
[3]	RW	mask_err_1_bndry_match_di3	err_1_bndry_match_di3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_1_bndry_match_di2	err_1_bndry_match_di2 interrupt mask 0: masked 1: enabled
[1]	RW	mask_err_1_bndry_match_di1	err_1_bndry_match_di1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_1_bndry_match_di0	err_1_bndry_match_di0 interrupt mask 0: masked 1: enabled

MIPI0_USERDEF_DT

MIPI0_USERDEF_DT is an MIPI 0 pixel bit width configuration register for the user-defined data type.

Offset Address	Register Name	Total Reset Value
0x1100	MIPI0_USERDEF_DT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				user_def3_dt	reserved / user_def2_dt	reserved / user_def1_dt	reserved / user_def0_dt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	user_def3_dt	Bit width of the transferred pixel when the data type is user_def3 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved
[11]	RO	reserved	Reserved
[10:8]	RW	user_def2_dt	Bit width of the transferred pixel when the data type is user_def2 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved
[7]	RO	reserved	Reserved
[6:4]	RW	user_def1_dt	Bit width of the transferred pixel when the data type is user_def1 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved

[3]	RO	reserved	Reserved
[2:0]	RW	user_def0_dt	Bit width of the transferred pixel when the data type is user_def0 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved

MIPI0_USER_DEF

MIPI0_USER_DEF is an MIPI 0 user-defined data type enable configuration register.

Offset Address	Register Name	Total Reset Value
0x1104	MIPI0_USER_DEF	0x1036_3534

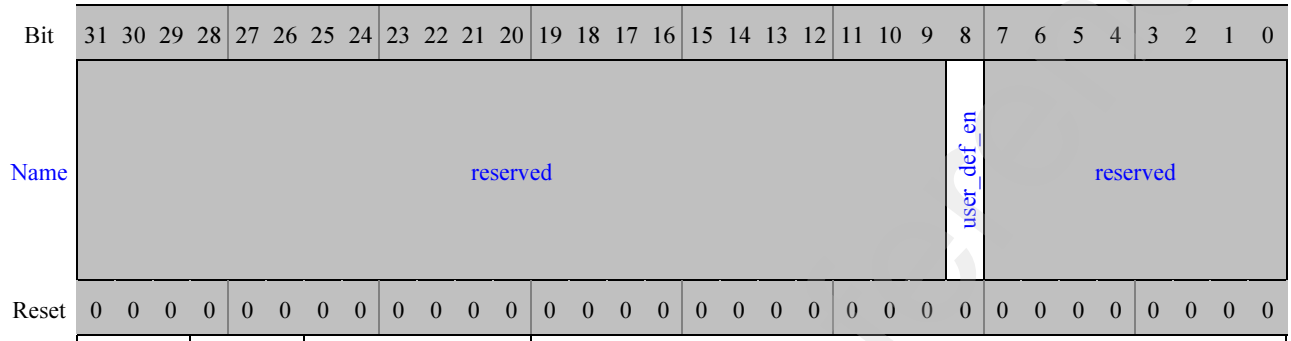
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				user_def3				reserved				user_def2				reserved				user_def1				reserved				user_def0			
Reset	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:24]	RW	user_def3	User-defined data type 3 The value of this field is used for matching the type of the sensor output data. This field works with user_def3_dt.
[23:22]	RO	reserved	Reserved
[21:16]	RW	user_def2	User-defined data type 2 The value of this field is used for matching the type of the sensor output data. This field works with user_def2_dt.
[15:14]	RO	reserved	Reserved
[13:8]	RW	user_def1	User-defined data type 1 The value of this field is used for matching the type of the sensor output data. This field works with user_def1_dt.
[7:6]	RO	reserved	Reserved
[5:0]	RW	user_def0	User-defined data type 0 The value of this field is used for matching the type of the sensor output data. This field works with user_def0_dt.

MIPI0_CTRL_MODE_HS

MIPI0_CTRL_MODE_HS is an MIPI 0 operating mode enable register.

Offset Address	Register Name	Total Reset Value
0x1108	MIPI0_CTRL_MODE_HS	0x0000_0000

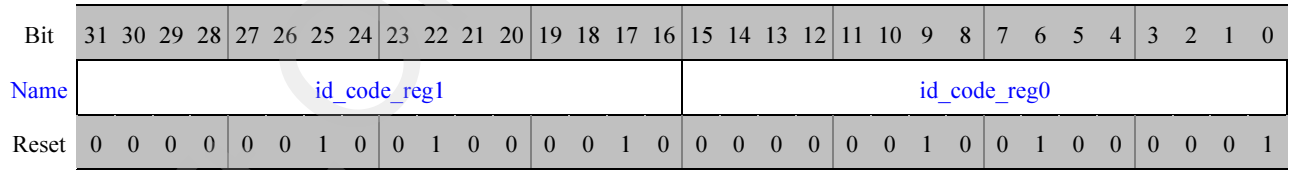


Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	user_def_en	User-defined mode enable 0: disabled 1: enabled
[7:0]	RO	reserved	Reserved

MIPI0_DOL_ID_CODE0

MIPI0_DOL_ID_CODE0 is MIPI 0 DOL mode frame identification register 0.

Offset Address	Register Name	Total Reset Value
0x1200	MIPI0_DOL_ID_CODE0	0x0242_0241



Bits	Access	Name	Description
[31:16]	RW	id_code_reg1	ID of SEF1 frame *N* in MIPI DOL mode
[15:0]	RW	id_code_reg0	ID of LEF frame *N* in MIPI DOL mode

MIPI0_DOL_ID_CODE1

MIPI0_DOL_ID_CODE1 is MIPI 0 DOL mode frame identification register 1.

Offset Address	Register Name	Total Reset Value
0x1204	MIPI0_DOL_ID_CODE1	0x0251_0244

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg3																id_code_reg2															
Reset	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg3	ID of LEF frame *N* + 1 in MIPI DOL mode
[15:0]	RW	id_code_reg2	ID of SEF2 frame *N* in MIPI DOL mode

MIPI0_DOL_ID_CODE2

MIPI0_DOL_ID_CODE2 is MIPI 0 DOL mode frame identification register 2.

Offset Address	Register Name	Total Reset Value
0x1208	MIPI0_DOL_ID_CODE2	0x0254_0252

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg5																id_code_reg4															
Reset	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg5	ID of SEF2 frame *N* + 1 in MIPI DOL mode
[15:0]	RW	id_code_reg4	ID of SEF1 frame *N* + 1 in MIPI DOL mode

MIPI0_CTRL_MODE_PIXEL

MIPI0_CTRL_MODE_PIXEL is an MIPI 0 output operating mode enable register.

Offset Address	Register Name	Total Reset Value
0x1230	MIPI0_CTRL_MODE_PIXEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	stagger_frm_num		stagger_hdr_mode	reserved							mipi_dol_mode	reserved			crop_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:13]	RW	stagger_frm_num	Number of frames in staggered HDR mode 01: 2-frame HDR 10: 3-frame HDR 11: 4-frame HDR Other values: reserved
[12]	RW	stagger_hdr_mode	OmniVision staggered HDR mode enable 0: disabled 1: enabled
[11:5]	RW	reserved	Reserved
[4]	RW	mipi_dol_mode	MIPI DOL mode enable 0: disabled 1: enabled
[3:1]	RO	reserved	Reserved
[0]	RW	crop_en	Cropping enable 0: disabled 1: enabled

MIPI0_DUMMY_PIX_REG

MIPI0_DUMMY_PIX_REG is an MIPI 0 dummy line pixel value register.

Offset Address	Register Name	Total Reset Value
0x1240	MIPI0_DUMMY_PIX_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dummy_pix_reg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dummy_pix_reg	Dummy line pixel value in staggered HDR mode

MIPI0_IMGSIZE0_STATIS

MIPI0_IMGSIZE0_STATIS is an MIPI 0 VC 0 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1250	MIPI0_IMGSIZE0_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	imgheight_statis_vc0																imgwidth_statis_vc0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc0	Height of the previous frame of image transferred by virtual channel 0 in MIPI mode
[15:0]	RO	imgwidth_statis_vc0	Width of the previous frame of image transferred by virtual channel 0 in MIPI mode

MIPI0_IMGSIZE1_STATIS

MIPI0_IMGSIZE1_STATIS is an MIPI 0 VC 1 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1254	MIPI0_IMGSIZE1_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	imgheight_statis_vc1																imgwidth_statis_vc1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc1	Height of the previous frame of image transferred by virtual channel 1 in MIPI mode

[15:0]	RO	imgwidth_statis_vc1	Width of the previous frame of image transferred by virtual channel 1 in MIPI mode

MIPI0_IMGSIZE2_STATIS

MIPI0_IMGSIZE2_STATIS is an MIPI 0 VC 2 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1258	MIPI0_IMGSIZE2_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc2				imgwidth_statis_vc2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc2	Height of the previous frame of image transferred by virtual channel 2 in MIPI mode
[15:0]	RO	imgwidth_statis_vc2	Width of the previous frame of image transferred by virtual channel 2 in MIPI mode

MIPI0_IMGSIZE3_STATIS

MIPI0_IMGSIZE3_STATIS is an MIPI 0 VC 3 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x125C	MIPI0_IMGSIZE3_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc3				imgwidth_statis_vc3			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc3	Height of the previous frame of image transferred by virtual channel 3 in MIPI mode
[15:0]	RO	imgwidth_statis_vc3	Width of the previous frame of image transferred by virtual channel 3 in MIPI mode

MIPI0_CTRL_INT_RAW

MIPI0_CTRL_INT_RAW is an MIPI 0 read data error raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F0	MIPI0_CTRL_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_raw	int_cfifo_rderr_raw	reserved														int_dfifo_wrerr_raw	int_cfifo_wrerr_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	WC	int_dfifo_rderr_raw	MIPI CTRL read data FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	WC	int_cfifo_rderr_raw	MIPI CTRL read command FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:2]	RO	reserved	Reserved
[1]	WC	int_dfifo_wrerr_raw	MIPI CTRL write data FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	int_cfifo_wrerr_raw	MIPI CTRL write command FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI0_CTRL_INT

MIPI0_CTRL_INT is an MIPI 0 read data error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F4	MIPI0_CTRL_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_st	int_cfifo_rderr_st	reserved														int_dfifo_wrerr_st	int_cfifo_wrerr_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	int_dfifo_rderr_st	MIPI CTRL read data FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	int_cfifo_rderr_st	MIPI CTRL read command FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[15:2]	RO	reserved	Reserved
[1]	RO	int_dfifo_wrerr_st	MIPI CTRL write data FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_cfifo_wrerr_st	MIPI CTRL write command FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

MIPI0_CTRL_INT_MSK

MIPI0_CTRL_INT_MSK is an MIPI 0 read data error interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x12F8	MIPI0_CTRL_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_msk	int_cfifo_rderr_msk	reserved														int_dfifo_wrerr_msk	int_cfifo_wrerr_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	int_dfifo_rderr_msk	MIPI CTRL read data FIFO interrupt enable 0: masked 1: enabled
[16]	RW	int_cfifo_rderr_msk	MIPI CTRL read command FIFO interrupt enable 0: masked 1: enabled
[15:2]	RO	reserved	Reserved
[1]	RW	int_dfifo_wrerr_msk	MIPI CTRL write data FIFO interrupt enable 0: masked 1: enabled
[0]	RW	int_cfifo_wrerr_msk	MIPI CTRL write command FIFO interrupt enable 0: masked 1: enabled

LVDS0_WDR

LVDS0_WDR is an LVDS WDR control register.

Offset Address	Register Name	Total Reset Value
0x1300	LVDS0_WDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lvds_wdr_mode				reserved				lvds_wdr_num		reserved				lvds_wdr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	lvds_wdr_mode	LVDS WDR mode select 0x0: WDR mode with the SOF-EOF flag. In this mode, the long exposure frame and short exposure frame have independent synchronization codes. 0x2: HiSPI WDR mode. In this mode, the long and short exposure frames share one SOF-EOF flag, and the first several lines of the short exposure frame are stuffed with 0x04. 0x4: SONY DOL WDR mode. In this mode, the synchronization code consists of four fields, the SAV-EAV flag is used, and the long exposure frame and short exposure frame have independent synchronization codes. 0x5: SONY DOL WDR mode. In this mode, the synchronization code consists of four fields, the SAV-EAV flag is used, the long and short exposure frames share one group of synchronization codes, and there are blanking regions between the long exposure data and short exposure data. 0x6: SONY DOL WDR mode. In this mode, the synchronization code consists of five fields, and the image information does not contain the frame information line. 0xC: SONY DOL WDR mode. In this mode, the synchronization code consists of five fields, and the image information does not contain the frame information line.
[7:6]	RO	reserved	Reserved
[5:4]	RW	lvds_wdr_num	WDR mode configuration 00: reserved 01: 2-frame WDR 10: 3-frame WDR 11: 4-frame WDR
[3:1]	RO	reserved	Reserved

[0]	RW	lvds_wdr_en	WDR enable 0: linear mode 1: WDR mode

LVDS0_DOLSCD_HBLK

LVDS0_DOLSCD_HBLK is LVDS SCD control register 0.

Offset Address	Register Name	Total Reset Value
0x1304	LVDS0_DOLSCD_HBLK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	dol_hblank2			reserved	dol_hblank1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	dol_hblank2	HBLANK2 value in DOL mode
[15:12]	RO	reserved	Reserved
[11:0]	RW	dol_hblank1	HBLANK1 value in DOL mode

LVDS0_IMGSIZE

LVDS0_IMGSIZE is an LVDS image size register.

Offset Address	Register Name	Total Reset Value
0x130C	LVDS0_IMGSIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lvds_imgheight				lvds_imgwidth_lane			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lvds_imgheight	Image height minus 1
[15:0]	RW	lvds_imgwidth_lane	Width of the image transferred in each channel minus 1

LVDS0_CTRL

LVDS0_CTRL is an LVDS control register.

Offset Address	Register Name	Total Reset Value
0x1310	LVDS0_CTRL	0x0000_0310

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												lvds_split_mode				reserved				lvds_crop_en		reserved			lvds_code_big_endian	lvds_pix_big_endian		reserved				lvds_raw_type				reserved				lvds_sync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	lvds_split_mode	Transfer type for the synchronization code in LVDS or HiSPI mode 000: per lane mode Other values: reserved
[15:13]	RO	reserved	Reserved
[12]	RW	lvds_crop_en	Image cropping enable in LVDS or HiSPI mode 0: disabled 1: enabled
[11:10]	RO	reserved	Reserved
[9]	RW	lvds_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received synchronization code is bit 0, bit 1, …, bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received synchronization code is bit 11, bit 10, …, bit 0.
[8]	RW	lvds_pix_big_endian	Serial bit transmission sequence for the valid pixels of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received valid pixels is bit 0, bit 1, …, bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received valid pixels is bit 11, bit 10, …, bit 0.
[7]	RO	reserved	Reserved

[6:4]	RW	lvds_raw_type	Type of the raw data to be transmitted in LVDS or HiSPI mode 001: 8-bit raw data 010: 10-bit raw data 011: 12-bit raw data 100: 14-bit raw data 101: 16-bit raw data Other values: reserved
[3:1]	RO	reserved	Reserved
[0]	RW	lvds_sync_mode	Frame or line synchronization mode in LVDS mode 0: SOF/EOF/SOL/EOL mode. SOF specifies the start of the first line in the active region, EOF specifies the end of the last line in the active region, SOL and EOL specify the start and end of other lines in the active region respectively. 1: SAV/EAV mode. SAV (Invalid) and EAV (Invalid) identify invalid data of the blanking region, whereas SAV (Valid) and EAV (Valid) identify pixel data of the active region.

LVDS0_CROP_START

LVDS0_CROP_START is an LVDS cropping register.

Offset Address	Register Name	Total Reset Value
0x1314	LVDS0_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_start_y																lvds_start_x_lane															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lvds_start_y	Vertical coordinate of the cropping start point
[15:0]	RW	lvds_start_x_lane	Horizontal coordinate of the cropping start point. The configured value is the start pixel to be cropped divided by the number of channels.

LVDS0_LANE0_SOF_01

LVDS0_LANE0_SOF_01 is a lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1320	LVDS0_LANE0_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_1																lane0_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_1	Lane 0 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_0	Lane 0 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE0_SOF_23

LVDS0_LANE0_SOF_23 is a lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1324	LVDS0_LANE0_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_3																lane0_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_3	Lane 0 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_2	Lane 0 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_EOF_01

LVDS0_LANE0_EOF_01 is a lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1328	LVDS0_LANE0_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_1																lane0_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_1	Lane 0 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_0	Lane 0 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE0_EOF_23

LVDS0_LANE0_EOF_23 is a lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x132C	LVDS0_LANE0_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_3																lane0_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_3	Lane 0 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_2	Lane 0 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_SOL_01

LVDS0_LANE0_SOL_01 is a lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1330	LVDS0_LANE0_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sol_1																lane0_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_1	Lane 0 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_0	Lane 0 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE0_SOL_23

LVDS0_LANE0_SOL_23 is a lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1334	LVDS0_LANE0_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sol_3																lane0_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_3	Lane 0 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_2	Lane 0 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_EOL_01

LVDS0_LANE0_EOL_01 is a lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1338	LVDS0_LANE0_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eol_1																lane0_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_1	Lane 0 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_0	Lane 0 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE0_EOL_23

LVDS0_LANE0_EOL_23 is a lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x133C	LVDS0_LANE0_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eol_3																lane0_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_3	Lane 0 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_2	Lane 0 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_SOF_01

LVDS0_LANE1_SOF_01 is a lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1340	LVDS0_LANE1_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sof_1																lane1_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_1	Lane 1 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_0	Lane 1 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE1_SOF_23

LVDS0_LANE1_SOF_23 is a lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1344	LVDS0_LANE1_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sof_3																lane1_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_3	Lane 1 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_2	Lane 1 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_EOF_01

LVDS0_LANE1_EOF_01 is a lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1348	LVDS0_LANE1_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eof_1																lane1_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_1	Lane 1 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_0	Lane 1 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE1_EOF_23

LVDS0_LANE1_EOF_23 is a lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x134C	LVDS0_LANE1_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eof_3																lane1_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_3	Lane 1 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_2	Lane 1 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_SOL_01

LVDS0_LANE1_SOL_01 is a lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1350	LVDS0_LANE1_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sol_1																lane1_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_1	Lane 1 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_0	Lane 1 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE1_SOL_23

LVDS0_LANE1_SOL_23 is a lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1354	LVDS0_LANE1_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sol_3																lane1_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_3	Lane 1 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_2	Lane 1 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_EOL_01

LVDS0_LANE1_EOL_01 is a lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1358	LVDS0_LANE1_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eol_1																lane1_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_1	Lane 1 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_0	Lane 1 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE1_EOL_23

LVDS0_LANE1_EOL_23 is a lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x135C	LVDS0_LANE1_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eol_3																lane1_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_3	Lane 1 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_2	Lane 1 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_SOF_01

LVDS0_LANE2_SOF_01 is a lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1360	LVDS0_LANE2_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_1																lane2_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_1	Lane 2 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_0	Lane 2 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE2_SOF_23

LVDS0_LANE2_SOF_23 is a lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1364	LVDS0_LANE2_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_3																lane2_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_3	Lane 2 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_2	Lane 2 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_EOF_01

LVDS0_LANE2_EOF_01 is a lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1368	LVDS0_LANE2_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_1																lane2_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_1	Lane 2 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_0	Lane 2 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE2_EOF_23

LVDS0_LANE2_EOF_23 is a lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x136C	LVDS0_LANE2_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_3																lane2_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_3	Lane 2 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_2	Lane 2 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_SOL_01

LVDS0_LANE2_SOL_01 is a lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1370	LVDS0_LANE2_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_1																lane2_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_1	Lane 2 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_0	Lane 2 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE2_SOL_23

LVDS0_LANE2_SOL_23 is a lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1374	LVDS0_LANE2_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_3																lane2_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_3	Lane 2 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_2	Lane 2 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_EOL_01

LVDS0_LANE2_EOL_01 is a lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1378	LVDS0_LANE2_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eol_1																lane2_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_1	Lane 2 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_0	Lane 2 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE2_EOL_23

LVDS0_LANE2_EOL_23 is a lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x137C	LVDS0_LANE2_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eol_3																lane2_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_3	Lane 2 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_2	Lane 2 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_SOF_01

LVDS0_LANE3_SOF_01 is a lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1380	LVDS0_LANE3_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sof_1																lane3_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_1	Lane 3 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_0	Lane 3 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE3_SOF_23

LVDS0_LANE3_SOF_23 is a lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1384	LVDS0_LANE3_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sof_3																lane3_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_3	Lane 3 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_2	Lane 3 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_EOF_01

LVDS0_LANE3_EOF_01 is a lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1388	LVDS0_LANE3_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eof_1																lane3_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_1	Lane 3 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_0	Lane 3 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE3_EOF_23

LVDS0_LANE3_EOF_23 is a lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x138C	LVDS0_LANE3_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eof_3																lane3_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_3	Lane 3 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_2	Lane 3 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_SOL_01

LVDS0_LANE3_SOL_01 is a lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1390	LVDS0_LANE3_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sol_1																lane3_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_1	Lane 3 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_0	Lane 3 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE3_SOL_23

LVDS0_LANE3_SOL_23 is a lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1394	LVDS0_LANE3_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sol_3																lane3_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_3	Lane 3 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_2	Lane 3 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_EOL_01

LVDS0_LANE3_EOL_01 is a lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1398	LVDS0_LANE3_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eol_1																lane3_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_1	Lane 3 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_0	Lane 3 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE3_EOL_23

LVDS0_LANE3_EOL_23 is a lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x139C	LVDS0_LANE3_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eol_3																lane3_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_3	Lane 3 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_2	Lane 3 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_SOF_01

LVDS0_LANE4_SOF_01 is a lane 4 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A0	LVDS0_LANE4_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_sof_1																lane4_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_sof_1	Lane 4 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_sof_0	Lane 4 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE4_SOF_23

LVDS0_LANE4_SOF_23 is a lane 4 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A4	LVDS0_LANE4_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_sof_3																lane4_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_sof_3	Lane 4 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_sof_2	Lane 4 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_EOF_01

LVDS0_LANE4_EOF_01 is a lane 4 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A8	LVDS0_LANE4_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_eof_1																lane4_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_eof_1	Lane 4 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_eof_0	Lane 4 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE4_EOF_23

LVDS0_LANE4_EOF_23 is a lane 4 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13AC	LVDS0_LANE4_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_eof_3																lane4_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_eof_3	Lane 4 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_eof_2	Lane 4 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_SOL_01

LVDS0_LANE4_SOL_01 is a lane 4 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B0	LVDS0_LANE4_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_sol_1																lane4_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_sol_1	Lane 4 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_sol_0	Lane 4 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE4_SOL_23

LVDS0_LANE4_SOL_23 is a lane 4 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B4	LVDS0_LANE4_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_sol_3																lane4_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_sol_3	Lane 4 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_sol_2	Lane 4 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_EOL_01

LVDS0_LANE4_EOL_01 is a lane 4 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B8	LVDS0_LANE4_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_eol_1																lane4_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_eol_1	Lane 4 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_eol_0	Lane 4 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE4_EOL_23

LVDS0_LANE4_EOL_23 is a lane 4 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13BC	LVDS0_LANE4_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_eol_3																lane4_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_eol_3	Lane 4 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_eol_2	Lane 4 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_SOF_01

LVDS0_LANE5_SOF_01 is a lane 5 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C0	LVDS0_LANE5_SOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_sof_1				lane5_sof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sof_1	Lane 5 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_sof_0	Lane 5 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE5_SOF_23

LVDS0_LANE5_SOF_23 is a lane 5 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C4	LVDS0_LANE5_SOF_23	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_sof_3				lane5_sof_2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sof_3	Lane 5 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_sof_2	Lane 5 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_EOF_01

LVDS0_LANE5_EOF_01 is a lane 5 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C8	LVDS0_LANE5_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_eof_1																lane5_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_eof_1	Lane 5 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_eof_0	Lane 5 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE5_EOF_23

LVDS0_LANE5_EOF_23 is a lane 5 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13CC	LVDS0_LANE5_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_eof_3																lane5_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_eof_3	Lane 5 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_eof_2	Lane 5 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_SOL_01

LVDS0_LANE5_SOL_01 is a lane 5 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D0	LVDS0_LANE5_SOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_sol_1				lane5_sol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sol_1	Lane 5 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_sol_0	Lane 5 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE5_SOL_23

LVDS0_LANE5_SOL_23 is a lane 5 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D4	LVDS0_LANE5_SOL_23	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_sol_3				lane5_sol_2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_sol_3	Lane 5 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_sol_2	Lane 5 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_EOL_01

LVDS0_LANE5_EOL_01 is a lane 5 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D8	LVDS0_LANE5_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_eol_1				lane5_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eol_1	Lane 5 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_eol_0	Lane 5 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE5_EOL_23

LVDS0_LANE5_EOL_23 is a lane 5 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13DC	LVDS0_LANE5_EOL_23	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane5_eol_3				lane5_eol_2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane5_eol_3	Lane 5 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_eol_2	Lane 5 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_SOF_01

LVDS0_LANE6_SOF_01 is a lane 6 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E0	LVDS0_LANE6_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_sof_1																lane6_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_sof_1	Lane 6 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_sof_0	Lane 6 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE6_SOF_23

LVDS0_LANE6_SOF_23 is a lane 6 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E4	LVDS0_LANE6_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_sof_3																lane6_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_sof_3	Lane 6 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_sof_2	Lane 6 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_EOF_01

LVDS0_LANE6_EOF_01 is a lane 6 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E8	LVDS0_LANE6_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_eof_1																lane6_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_eof_1	Lane 6 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_eof_0	Lane 6 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE6_EOF_23

LVDS0_LANE6_EOF_23 is a lane 6 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13EC	LVDS0_LANE6_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_eof_3																lane6_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_eof_3	Lane 6 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_eof_2	Lane 6 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_SOL_01

LVDS0_LANE6_SOL_01 is a lane 6 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F0	LVDS0_LANE6_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_sol_1																lane6_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_sol_1	Lane 6 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_sol_0	Lane 6 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE6_SOL_23

LVDS0_LANE6_SOL_23 is a lane 6 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F4	LVDS0_LANE6_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_sol_3																lane6_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_sol_3	Lane 6 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_sol_2	Lane 6 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_EOL_01

LVDS0_LANE6_EOL_01 is a lane 6 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F8	LVDS0_LANE6_EOL_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane6_eol_1				lane6_eol_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_eol_1	Lane 6 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_eol_0	Lane 6 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE6_EOL_23

LVDS0_LANE6_EOL_23 is a lane 6 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13FC	LVDS0_LANE6_EOL_23	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane6_eol_3				lane6_eol_2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane6_eol_3	Lane 6 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_eol_2	Lane 6 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_SOF_01

LVDS0_LANE7_SOF_01 is a lane 7 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1400	LVDS0_LANE7_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_sof_1																lane7_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_sof_1	Lane 7 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_sof_0	Lane 7 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE7_SOF_23

LVDS0_LANE7_SOF_23 is a lane 7 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1404	LVDS0_LANE7_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_sof_3																lane7_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_sof_3	Lane 7 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_sof_2	Lane 7 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_EOF_01

LVDS0_LANE7_EOF_01 is a lane 7 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1408	LVDS0_LANE7_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_eof_1																lane7_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_eof_1	Lane 7 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_eof_0	Lane 7 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE7_EOF_23

LVDS0_LANE7_EOF_23 is a lane 7 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x140C	LVDS0_LANE7_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_eof_3																lane7_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_eof_3	Lane 7 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_eof_2	Lane 7 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_SOL_01

LVDS0_LANE7_SOL_01 is a lane 7 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1410	LVDS0_LANE7_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_sol_1																lane7_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_sol_1	Lane 7 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_sol_0	Lane 7 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE7_SOL_23

LVDS0_LANE7_SOL_23 is a lane 7 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1414	LVDS0_LANE7_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_sol_3																lane7_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_sol_3	Lane 7 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_sol_2	Lane 7 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_EOL_01

LVDS0_LANE7_EOL_01 is a lane 7 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1418	LVDS0_LANE7_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_eol_1																lane7_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_eol_1	Lane 7 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_eol_0	Lane 7 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE7_EOL_23

LVDS0_LANE7_EOL_23 is a lane 7 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x141C	LVDS0_LANE7_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_eol_3																lane7_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_eol_3	Lane 7 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_eol_2	Lane 7 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_SOF_01

LVDS0_LANE8_SOF_01 is a lane 8 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1420	LVDS0_LANE8_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_sof_1																lane8_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_sof_1	Lane 8 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_sof_0	Lane 8 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE8_SOF_23

LVDS0_LANE8_SOF_23 is a lane 8 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1424	LVDS0_LANE8_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_sof_3																lane8_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_sof_3	Lane 8 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_sof_2	Lane 8 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_EOF_01

LVDS0_LANE8_EOF_01 is a lane 8 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1428	LVDS0_LANE8_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_eof_1																lane8_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_eof_1	Lane 8 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_eof_0	Lane 8 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE8_EOF_23

LVDS0_LANE8_EOF_23 is a lane 8 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x142C	LVDS0_LANE8_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_eof_3																lane8_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_eof_3	Lane 8 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_eof_2	Lane 8 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_SOL_01

LVDS0_LANE8_SOL_01 is a lane 8 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1430	LVDS0_LANE8_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_sol_1																lane8_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_sol_1	Lane 8 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_sol_0	Lane 8 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE8_SOL_23

LVDS0_LANE8_SOL_23 is a lane 8 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1434	LVDS0_LANE8_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_sol_3																lane8_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_sol_3	Lane 8 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_sol_2	Lane 8 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_EOL_01

LVDS0_LANE8_EOL_01 is a lane 8 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1438	LVDS0_LANE8_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_eol_1																lane8_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_eol_1	Lane 8 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_eol_0	Lane 8 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE8_EOL_23

LVDS0_LANE8_EOL_23 is a lane 8 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x143C	LVDS0_LANE8_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_eol_3																lane8_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_eol_3	Lane 8 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_eol_2	Lane 8 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_SOF_01

LVDS0_LANE9_SOF_01 is a lane 9 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1440	LVDS0_LANE9_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_sof_1																lane9_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_sof_1	Lane 9 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_sof_0	Lane 9 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE9_SOF_23

LVDS0_LANE9_SOF_23 is a lane 9 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1444	LVDS0_LANE9_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_sof_3																lane9_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_sof_3	Lane 9 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_sof_2	Lane 9 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_EOF_01

LVDS0_LANE9_EOF_01 is a lane 9 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1448	LVDS0_LANE9_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_eof_1																lane9_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_eof_1	Lane 9 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_eof_0	Lane 9 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE9_EOF_23

LVDS0_LANE9_EOF_23 is a lane 9 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x144C	LVDS0_LANE9_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_eof_3																lane9_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_eof_3	Lane 9 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_eof_2	Lane 9 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_SOL_01

LVDS0_LANE9_SOL_01 is a lane 9 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1450	LVDS0_LANE9_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_sol_1																lane9_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_sol_1	Lane 9 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_sol_0	Lane 9 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE9_SOL_23

LVDS0_LANE9_SOL_23 is a lane 9 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1454	LVDS0_LANE9_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_sol_3																lane9_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_sol_3	Lane 9 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_sol_2	Lane 9 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_EOL_01

LVDS0_LANE9_EOL_01 is a lane 9 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1458	LVDS0_LANE9_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_eol_1																lane9_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_eol_1	Lane 9 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_eol_0	Lane 9 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE9_EOL_23

LVDS0_LANE9_EOL_23 is a lane 9 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x145C	LVDS0_LANE9_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_eol_3																lane9_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_eol_3	Lane 9 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_eol_2	Lane 9 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_SOF_01

LVDS0_LANE10_SOF_01 is a lane 10 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1460	LVDS0_LANE10_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_sof_1																lane10_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_sof_1	Lane 10 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_sof_0	Lane 10 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE10_SOF_23

LVDS0_LANE10_SOF_23 is a lane 10 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1464	LVDS0_LANE10_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_sof_3																lane10_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_sof_3	Lane 10 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_sof_2	Lane 10 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_EOF_01

LVDS0_LANE10_EOF_01 is a lane 10 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1468	LVDS0_LANE10_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_eof_1																lane10_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_eof_1	Lane 10 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_eof_0	Lane 10 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE10_EOF_23

LVDS0_LANE10_EOF_23 is a lane 10 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x146C	LVDS0_LANE10_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_eof_3																lane10_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_eof_3	Lane 10 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_eof_2	Lane 10 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_SOL_01

LVDS0_LANE10_SOL_01 is a lane 10 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1470	LVDS0_LANE10_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_sol_1																lane10_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_sol_1	Lane 10 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_sol_0	Lane 10 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE10_SOL_23

LVDS0_LANE10_SOL_23 is a lane 10 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1474	LVDS0_LANE10_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_sol_3																lane10_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_sol_3	Lane 10 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_sol_2	Lane 10 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_EOL_01

LVDS0_LANE10_EOL_01 is a lane 10 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1478	LVDS0_LANE10_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_eol_1																lane10_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_eol_1	Lane 10 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_eol_0	Lane 10 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE10_EOL_23

LVDS0_LANE10_EOL_23 is a lane 10 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x147C	LVDS0_LANE10_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_eol_3																lane10_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_eol_3	Lane 10 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_eol_2	Lane 10 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_SOF_01

LVDS0_LANE11_SOF_01 is a lane 11 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1480	LVDS0_LANE11_SOF_01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane11_sof_1				lane11_sof_0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_sof_1	Lane 11 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_sof_0	Lane 11 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE11_SOF_23

LVDS0_LANE11_SOF_23 is a lane 11 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1484	LVDS0_LANE11_SOF_23	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lane11_sof_3				lane11_sof_2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	lane11_sof_3	Lane 11 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_sof_2	Lane 11 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_EOF_01

LVDS0_LANE11_EOF_01 is a lane 11 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1488	LVDS0_LANE11_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_eof_1																lane11_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_eof_1	Lane 11 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_eof_0	Lane 11 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE11_EOF_23

LVDS0_LANE11_EOF_23 is a lane 11 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x148C	LVDS0_LANE11_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_eof_3																lane11_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_eof_3	Lane 11 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_eof_2	Lane 11 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_SOL_01

LVDS0_LANE11_SOL_01 is a lane 11 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1490	LVDS0_LANE11_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_sol_1																lane11_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_sol_1	Lane 11 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_sol_0	Lane 11 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE11_SOL_23

LVDS0_LANE11_SOL_23 is a lane 11 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1494	LVDS0_LANE11_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_sol_3																lane11_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_sol_3	Lane 11 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_sol_2	Lane 11 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_EOL_01

LVDS0_LANE11_EOL_01 is a lane 11 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1498	LVDS0_LANE11_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_eol_1																lane11_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_eol_1	Lane 11 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_eol_0	Lane 11 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE11_EOL_23

LVDS0_LANE11_EOL_23 is a lane 11 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x149C	LVDS0_LANE11_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_eol_3																lane11_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_eol_3	Lane 11 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_eol_2	Lane 11 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_SOF_01

LVDS0_LANE0_NXT_SOF_01 is a lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14A0	LVDS0_LANE0_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sof_1																lane0_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sof_1	Lane 0 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sof_0	Lane 0 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE0_NXT_SOF_23

LVDS0_LANE0_NXT_SOF_23 is a lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14A4	LVDS0_LANE0_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sof_3																lane0_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sof_3	Lane 0 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sof_2	Lane 0 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_EOF_01

LVDS0_LANE0_NXT_EOF_01 is a lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14A8	LVDS0_LANE0_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eof_1																lane0_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_1	Lane 0 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_0	Lane 0 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE0_NXT_EOF_23

LVDS0_LANE0_NXT_EOF_23 is a lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14AC	LVDS0_LANE0_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eof_3																lane0_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_3	Lane 0 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_2	Lane 0 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_SOL_01

LVDS0_LANE0_NXT_SOL_01 is a lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14B0	LVDS0_LANE0_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sol_1																lane0_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_1	Lane 0 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_0	Lane 0 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE0_NXT_SOL_23

LVDS0_LANE0_NXT_SOL_23 is a lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14B4	LVDS0_LANE0_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sol_3																lane0_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_3	Lane 0 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_2	Lane 0 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_EOL_01

LVDS0_LANE0_NXT_EOL_01 is a lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14B8	LVDS0_LANE0_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eol_1																lane0_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_1	Lane 0 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_0	Lane 0 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE0_NXT_EOL_23

LVDS0_LANE0_NXT_EOL_23 is a lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14BC	LVDS0_LANE0_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eol_3																lane0_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_3	Lane 0 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_2	Lane 0 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_SOF_01

LVDS0_LANE1_NXT_SOF_01 is a lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14C0	LVDS0_LANE1_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sof_1																lane1_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_1	Lane 1 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_0	Lane 1 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE1_NXT_SOF_23

LVDS0_LANE1_NXT_SOF_23 is a lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14C4	LVDS0_LANE1_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sof_3																lane1_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_3	Lane 1 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_2	Lane 1 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_EOF_01

LVDS0_LANE1_NXT_EOF_01 is a lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14C8	LVDS0_LANE1_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eof_1																lane1_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_1	Lane 1 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_0	Lane 1 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE1_NXT_EOF_23

LVDS0_LANE1_NXT_EOF_23 is a lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14CC	LVDS0_LANE1_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eof_3																lane1_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_3	Lane 1 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_2	Lane 1 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_SOL_01

LVDS0_LANE1_NXT_SOL_01 is a lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14D0	LVDS0_LANE1_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sol_1																lane1_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sol_1	Lane 1 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sol_0	Lane 1 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE1_NXT_SOL_23

LVDS0_LANE1_NXT_SOL_23 is a lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14D4	LVDS0_LANE1_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sol_3																lane1_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sol_3	Lane 1 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sol_2	Lane 1 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_EOL_01

LVDS0_LANE1_NXT_EOL_01 is a lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14D8	LVDS0_LANE1_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eol_1																lane1_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eol_1	Lane 1 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eol_0	Lane 1 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE1_NXT_EOL_23

LVDS0_LANE1_NXT_EOL_23 is a lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14DC	LVDS0_LANE1_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eol_3																lane1_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eol_3	Lane 1 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eol_2	Lane 1 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_SOF_01

LVDS0_LANE2_NXT_SOF_01 is a lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14E0	LVDS0_LANE2_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sof_1																lane2_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sof_1	Lane 2 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sof_0	Lane 2 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE2_NXT_SOF_23

LVDS0_LANE2_NXT_SOF_23 is a lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14E4	LVDS0_LANE2_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sof_3																lane2_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sof_3	Lane 2 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sof_2	Lane 2 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_EOF_01

LVDS0_LANE2_NXT_EOF_01 is a lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14E8	LVDS0_LANE2_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eof_1																lane2_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eof_1	Lane 2 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eof_0	Lane 2 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE2_NXT_EOF_23

LVDS0_LANE2_NXT_EOF_23 is a lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14EC	LVDS0_LANE2_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eof_3																lane2_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eof_3	Lane 2 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eof_2	Lane 2 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_SOL_01

LVDS0_LANE2_NXT_SOL_01 is a lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14F0	LVDS0_LANE2_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sol_1																lane2_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sol_1	Lane 2 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sol_0	Lane 2 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE2_NXT_SOL_23

LVDS0_LANE2_NXT_SOL_23 is a lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14F4	LVDS0_LANE2_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sol_3																lane2_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sol_3	Lane 2 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sol_2	Lane 2 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_EOL_01

LVDS0_LANE2_NXT_EOL_01 is a lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14F8	LVDS0_LANE2_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eol_1																lane2_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eol_1	Lane 2 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eol_0	Lane 2 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE2_NXT_EOL_23

LVDS0_LANE2_NXT_EOL_23 is a lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x14FC	LVDS0_LANE2_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eol_3																lane2_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eol_3	Lane 2 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eol_2	Lane 2 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_SOF_01

LVDS0_LANE3_NXT_SOF_01 is a lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1500	LVDS0_LANE3_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sof_1																lane3_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_1	Lane 3 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_0	Lane 3 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE3_NXT_SOF_23

LVDS0_LANE3_NXT_SOF_23 is a lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1504	LVDS0_LANE3_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sof_3																lane3_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_3	Lane 3 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_2	Lane 3 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_EOF_01

LVDS0_LANE3_NXT_EOF_01 is a lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1508	LVDS0_LANE3_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eof_1																lane3_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_1	Lane 3 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_0	Lane 3 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE3_NXT_EOF_23

LVDS0_LANE3_NXT_EOF_23 is a lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x150C	LVDS0_LANE3_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eof_3																lane3_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_3	Lane 3 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_2	Lane 3 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_SOL_01

LVDS0_LANE3_NXT_SOL_01 is a lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1510	LVDS0_LANE3_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sol_1																lane3_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_1	Lane 3 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_0	Lane 3 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE3_NXT_SOL_23

LVDS0_LANE3_NXT_SOL_23 is a lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1514	LVDS0_LANE3_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sol_3																lane3_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_3	Lane 3 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_2	Lane 3 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_EOL_01

LVDS0_LANE3_NXT_EOL_01 is a lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1518	LVDS0_LANE3_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eol_1																lane3_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_1	Lane 3 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_0	Lane 3 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE3_NXT_EOL_23

LVDS0_LANE3_NXT_EOL_23 is a lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x151C	LVDS0_LANE3_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eol_3																lane3_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_3	Lane 3 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_2	Lane 3 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_NXT_SOF_01

LVDS0_LANE4_NXT_SOF_01 is a lane 4 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1520	LVDS0_LANE4_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_sof_1																lane4_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sof_1	Lane 4 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_sof_0	Lane 4 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE4_NXT_SOF_23

LVDS0_LANE4_NXT_SOF_23 is a lane 4 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1524	LVDS0_LANE4_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_sof_3																lane4_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sof_3	Lane 4 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_sof_2	Lane 4 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_NXT_EOF_01

LVDS0_LANE4_NXT_EOF_01 is a lane 4 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1528	LVDS0_LANE4_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_eof_1																lane4_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eof_1	Lane 4 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_eof_0	Lane 4 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE4_NXT_EOF_23

LVDS0_LANE4_NXT_EOF_23 is a lane 4 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x152C	LVDS0_LANE4_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_eof_3																lane4_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eof_3	Lane 4 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_eof_2	Lane 4 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_NXT_SOL_01

LVDS0_LANE4_NXT_SOL_01 is a lane 4 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1530	LVDS0_LANE4_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_sol_1																lane4_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sol_1	Lane 4 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_sol_0	Lane 4 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE4_NXT_SOL_23

LVDS0_LANE4_NXT_SOL_23 is a lane 4 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1534	LVDS0_LANE4_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_sol_3																lane4_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_sol_3	Lane 4 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_sol_2	Lane 4 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE4_NXT_EOL_01

LVDS0_LANE4_NXT_EOL_01 is a lane 4 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1538	LVDS0_LANE4_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_eol_1																lane4_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eol_1	Lane 4 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_eol_0	Lane 4 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE4_NXT_EOL_23

LVDS0_LANE4_NXT_EOL_23 is a lane 4 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x153C	LVDS0_LANE4_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane4_nxt_eol_3																lane4_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane4_nxt_eol_3	Lane 4 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane4_nxt_eol_2	Lane 4 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_NXT_SOF_01

LVDS0_LANE5_NXT_SOF_01 is a lane 5 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1540	LVDS0_LANE5_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_sof_1																lane5_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sof_1	Lane 5 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_sof_0	Lane 5 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE5_NXT_SOF_23

LVDS0_LANE5_NXT_SOF_23 is a lane 5 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1544	LVDS0_LANE5_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_sof_3																lane5_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sof_3	Lane 5 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_sof_2	Lane 5 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_NXT_EOF_01

LVDS0_LANE5_NXT_EOF_01 is a lane 5 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1548	LVDS0_LANE5_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_eof_1																lane5_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eof_1	Lane 5 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_eof_0	Lane 5 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE5_NXT_EOF_23

LVDS0_LANE5_NXT_EOF_23 is a lane 5 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x154C	LVDS0_LANE5_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_eof_3																lane5_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eof_3	Lane 5 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_eof_2	Lane 5 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_NXT_SOL_01

LVDS0_LANE5_NXT_SOL_01 is a lane 5 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1550	LVDS0_LANE5_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_sol_1																lane5_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sol_1	Lane 5 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_sol_0	Lane 5 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE5_NXT_SOL_23

LVDS0_LANE5_NXT_SOL_23 is a lane 5 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1554	LVDS0_LANE5_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_sol_3																lane5_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_sol_3	Lane 5 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_sol_2	Lane 5 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE5_NXT_EOL_01

LVDS0_LANE5_NXT_EOL_01 is a lane 5 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1558	LVDS0_LANE5_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_eol_1																lane5_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eol_1	Lane 5 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_eol_0	Lane 5 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE5_NXT_EOL_23

LVDS0_LANE5_NXT_EOL_23 is a lane 5 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x155C	LVDS0_LANE5_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane5_nxt_eol_3																lane5_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane5_nxt_eol_3	Lane 5 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane5_nxt_eol_2	Lane 5 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_NXT_SOF_01

LVDS0_LANE6_NXT_SOF_01 is a lane 6 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1560	LVDS0_LANE6_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_sof_1																lane6_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sof_1	Lane 6 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_sof_0	Lane 6 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE6_NXT_SOF_23

LVDS0_LANE6_NXT_SOF_23 is a lane 6 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1564	LVDS0_LANE6_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_sof_3																lane6_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sof_3	Lane 6 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_sof_2	Lane 6 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_NXT_EOF_01

LVDS0_LANE6_NXT_EOF_01 is a lane 6 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1568	LVDS0_LANE6_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_eof_1																lane6_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eof_1	Lane 6 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_eof_0	Lane 6 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE6_NXT_EOF_23

LVDS0_LANE6_NXT_EOF_23 is a lane 6 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x156C	LVDS0_LANE6_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_eof_3																lane6_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eof_3	Lane 6 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_eof_2	Lane 6 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_NXT_SOL_01

LVDS0_LANE6_NXT_SOL_01 is a lane 6 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1570	LVDS0_LANE6_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_sol_1																lane6_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sol_1	Lane 6 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_sol_0	Lane 6 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE6_NXT_SOL_23

LVDS0_LANE6_NXT_SOL_23 is a lane 6 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1574	LVDS0_LANE6_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_sol_3																lane6_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_sol_3	Lane 6 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_sol_2	Lane 6 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE6_NXT_EOL_01

LVDS0_LANE6_NXT_EOL_01 is a lane 6 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1578	LVDS0_LANE6_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_eol_1																lane6_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eol_1	Lane 6 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_eol_0	Lane 6 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE6_NXT_EOL_23

LVDS0_LANE6_NXT_EOL_23 is a lane 6 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x157C	LVDS0_LANE6_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane6_nxt_eol_3																lane6_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane6_nxt_eol_3	Lane 6 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane6_nxt_eol_2	Lane 6 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_NXT_SOF_01

LVDS0_LANE7_NXT_SOF_01 is a lane 7 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1580	LVDS0_LANE7_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_sof_1																lane7_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sof_1	Lane 7 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_sof_0	Lane 7 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE7_NXT_SOF_23

LVDS0_LANE7_NXT_SOF_23 is a lane 7 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1584	LVDS0_LANE7_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_sof_3																lane7_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sof_3	Lane 7 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_sof_2	Lane 7 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_NXT_EOF_01

LVDS0_LANE7_NXT_EOF_01 is a lane 7 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1588	LVDS0_LANE7_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_eof_1																lane7_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eof_1	Lane 7 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_eof_0	Lane 7 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE7_NXT_EOF_23

LVDS0_LANE7_NXT_EOF_23 is a lane 7 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x158C	LVDS0_LANE7_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_eof_3																lane7_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eof_3	Lane 7 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_eof_2	Lane 7 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_NXT_SOL_01

LVDS0_LANE7_NXT_SOL_01 is a lane 7 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1590	LVDS0_LANE7_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_sol_1																lane7_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sol_1	Lane 7 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_sol_0	Lane 7 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE7_NXT_SOL_23

LVDS0_LANE7_NXT_SOL_23 is a lane 7 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1594	LVDS0_LANE7_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_sol_3																lane7_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_sol_3	Lane 7 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_sol_2	Lane 7 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE7_NXT_EOL_01

LVDS0_LANE7_NXT_EOL_01 is a lane 7 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1598	LVDS0_LANE7_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_eol_1																lane7_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eol_1	Lane 7 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_eol_0	Lane 7 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE7_NXT_EOL_23

LVDS0_LANE7_NXT_EOL_23 is a lane 7 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x159C	LVDS0_LANE7_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane7_nxt_eol_3																lane7_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane7_nxt_eol_3	Lane 7 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane7_nxt_eol_2	Lane 7 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_NXT_SOF_01

LVDS0_LANE8_NXT_SOF_01 is a lane 8 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15A0	LVDS0_LANE8_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_sof_1																lane8_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sof_1	Lane 8 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_sof_0	Lane 8 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE8_NXT_SOF_23

LVDS0_LANE8_NXT_SOF_23 is a lane 8 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15A4	LVDS0_LANE8_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_sof_3																lane8_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sof_3	Lane 8 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_sof_2	Lane 8 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_NXT_EOF_01

LVDS0_LANE8_NXT_EOF_01 is a lane 8 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15A8	LVDS0_LANE8_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_eof_1																lane8_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eof_1	Lane 8 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_eof_0	Lane 8 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE8_NXT_EOF_23

LVDS0_LANE8_NXT_EOF_23 is a lane 8 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15AC	LVDS0_LANE8_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_eof_3																lane8_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eof_3	Lane 8 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_eof_2	Lane 8 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_NXT_SOL_01

LVDS0_LANE8_NXT_SOL_01 is a lane 8 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15B0	LVDS0_LANE8_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_sol_1																lane8_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sol_1	Lane 8 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_sol_0	Lane 8 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE8_NXT_SOL_23

LVDS0_LANE8_NXT_SOL_23 is a lane 8 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15B4	LVDS0_LANE8_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_sol_3																lane8_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_sol_3	Lane 8 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_sol_2	Lane 8 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE8_NXT_EOL_01

LVDS0_LANE8_NXT_EOL_01 is a lane 8 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15B8	LVDS0_LANE8_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_eol_1																lane8_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eol_1	Lane 8 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_eol_0	Lane 8 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE8_NXT_EOL_23

LVDS0_LANE8_NXT_EOL_23 is a lane 8 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15BC	LVDS0_LANE8_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane8_nxt_eol_3																lane8_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane8_nxt_eol_3	Lane 8 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane8_nxt_eol_2	Lane 8 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_NXT_SOF_01

LVDS0_LANE9_NXT_SOF_01 is a lane 9 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15C0	LVDS0_LANE9_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_sof_1																lane9_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sof_1	Lane 9 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_sof_0	Lane 9 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE9_NXT_SOF_23

LVDS0_LANE9_NXT_SOF_23 is a lane 9 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15C4	LVDS0_LANE9_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_sof_3																lane9_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sof_3	Lane 9 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_sof_2	Lane 9 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_NXT_EOF_01

LVDS0_LANE9_NXT_EOF_01 is a lane 9 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15C8	LVDS0_LANE9_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_eof_1																lane9_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eof_1	Lane 9 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_eof_0	Lane 9 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE9_NXT_EOF_23

LVDS0_LANE9_NXT_EOF_23 is a lane 9 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15CC	LVDS0_LANE9_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_eof_3																lane9_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eof_3	Lane 9 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_eof_2	Lane 9 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_NXT_SOL_01

LVDS0_LANE9_NXT_SOL_01 is a lane 9 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15D0	LVDS0_LANE9_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_sol_1																lane9_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sol_1	Lane 9 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_sol_0	Lane 9 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE9_NXT_SOL_23

LVDS0_LANE9_NXT_SOL_23 is a lane 9 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15D4	LVDS0_LANE9_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_sol_3																lane9_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_sol_3	Lane 9 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_sol_2	Lane 9 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE9_NXT_EOL_01

LVDS0_LANE9_NXT_EOL_01 is a lane 9 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15D8	LVDS0_LANE9_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_eol_1																lane9_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eol_1	Lane 9 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_eol_0	Lane 9 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE9_NXT_EOL_23

LVDS0_LANE9_NXT_EOL_23 is a lane 9 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15DC	LVDS0_LANE9_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane9_nxt_eol_3																lane9_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane9_nxt_eol_3	Lane 9 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane9_nxt_eol_2	Lane 9 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_NXT_SOF_01

LVDS0_LANE10_NXT_SOF_01 is a lane 10 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15E0	LVDS0_LANE10_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_sof_1																lane10_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sof_1	Lane 10 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_sof_0	Lane 10 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE10_NXT_SOF_23

LVDS0_LANE10_NXT_SOF_23 is a lane 10 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15E4	LVDS0_LANE10_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_sof_3																lane10_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sof_3	Lane 10 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_sof_2	Lane 10 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_NXT_EOF_01

LVDS0_LANE10_NXT_EOF_01 is a lane 10 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15E8	LVDS0_LANE10_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_eof_1																lane10_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eof_1	Lane 10 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_eof_0	Lane 10 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE10_NXT_EOF_23

LVDS0_LANE10_NXT_EOF_23 is a lane 10 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15EC	LVDS0_LANE10_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_eof_3																lane10_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eof_3	Lane 10 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_eof_2	Lane 10 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_NXT_SOL_01

LVDS0_LANE10_NXT_SOL_01 is a lane 10 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15F0	LVDS0_LANE10_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_sol_1																lane10_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sol_1	Lane 10 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_sol_0	Lane 10 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE10_NXT_SOL_23

LVDS0_LANE10_NXT_SOL_23 is a lane 10 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15F4	LVDS0_LANE10_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_sol_3																lane10_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_sol_3	Lane 10 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_sol_2	Lane 10 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE10_NXT_EOL_01

LVDS0_LANE10_NXT_EOL_01 is a lane 10 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15F8	LVDS0_LANE10_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_eol_1																lane10_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eol_1	Lane 10 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_eol_0	Lane 10 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE10_NXT_EOL_23

LVDS0_LANE10_NXT_EOL_23 is a lane 10 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x15FC	LVDS0_LANE10_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane10_nxt_eol_3																lane10_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane10_nxt_eol_3	Lane 10 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane10_nxt_eol_2	Lane 10 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_NXT_SOF_01

LVDS0_LANE11_NXT_SOF_01 is a lane 11 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1600	LVDS0_LANE11_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_sof_1																lane11_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sof_1	Lane 11 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_sof_0	Lane 11 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE11_NXT_SOF_23

LVDS0_LANE11_NXT_SOF_23 is a lane 11 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1604	LVDS0_LANE11_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_sof_3																lane11_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sof_3	Lane 11 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_sof_2	Lane 11 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_NXT_EOF_01

LVDS0_LANE11_NXT_EOF_01 is a lane 11 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1608	LVDS0_LANE11_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_eof_1																lane11_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eof_1	Lane 11 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_eof_0	Lane 11 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE11_NXT_EOF_23

LVDS0_LANE11_NXT_EOF_23 is a lane 11 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x160C	LVDS0_LANE11_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_eof_3																lane11_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eof_3	Lane 11 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_eof_2	Lane 11 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_NXT_SOL_01

LVDS0_LANE11_NXT_SOL_01 is a lane 11 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1610	LVDS0_LANE11_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_sol_1																lane11_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sol_1	Lane 11 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_sol_0	Lane 11 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE11_NXT_SOL_23

LVDS0_LANE11_NXT_SOL_23 is a lane 11 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1614	LVDS0_LANE11_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_sol_3																lane11_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_sol_3	Lane 11 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_sol_2	Lane 11 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE11_NXT_EOL_01

LVDS0_LANE11_NXT_EOL_01 is a lane 11 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1618	LVDS0_LANE11_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_eol_1																lane11_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eol_1	Lane 11 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_eol_0	Lane 11 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE11_NXT_EOL_23

LVDS0_LANE11_NXT_EOL_23 is a lane 11 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x161C	LVDS0_LANE11_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane11_nxt_eol_3																lane11_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane11_nxt_eol_3	Lane 11 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane11_nxt_eol_2	Lane 11 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LI_WORD0

LVDS0_LI_WORD0 is an LVDS DOL mode frame 0 LI register.

Offset Address	Register Name	Total Reset Value
0x1620	LVDS0_LI_WORD0	0x0211_0201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word0_1																li_word0_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	li_word0_1	LEF line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word0_0	LEF line information in DOL mode (for frame *N*)

LVDS0_LI_WORD1

LVDS0_LI_WORD1 is an LVDS DOL mode frame 1 LI register.

Offset Address	Register Name	Total Reset Value
0x1624	LVDS0_LI_WORD1	0x0212_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word1_1																li_word1_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	li_word1_1	SEF1 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word1_0	SEF1 line information in DOL mode (for frame *N*)

LVDS0_LI_WORD2

LVDS0_LI_WORD2 is an LVDS DOL mode frame 2 LI register.

Offset Address	Register Name	Total Reset Value
0x1628	LVDS0_LI_WORD2	0x0214_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word2_1																li_word2_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RW	li_word2_1	SEF2 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word2_0	SEF2 line information in DOL mode (for frame *N*)

LVDS0_LI_WORD3

LVDS0_LI_WORD3 is an LVDS DOL mode frame 3 LI register.

Offset Address	Register Name	Total Reset Value
0x162C	LVDS0_LI_WORD3	0x0218_0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word3_1																li_word3_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	li_word3_1	SEF3 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word3_0	SEF3 line information in DOL mode (for frame *N*)

LVDS0_IMGSIZE0_STATIS

LVDS0_IMGSIZE0_STATIS is an LVDS LEF image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1680	LVDS0_IMGSIZE0_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight0																lvds_imgwidth0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight0	Height of the image transferred by virtual channel 0 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth0	Width of the image transferred by virtual channel 0 in LVDS or HiSPI mode

LVDS0_IMGSIZE1_STATIS

LVDS0_IMGSIZE1_STATIS is an LVDS SEF1 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1684	LVDS0_IMGSIZE1_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight1																lvds_imgwidth1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight1	Height of the image transferred by virtual channel 1 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth1	Width of the image transferred by virtual channel 1 in LVDS or HiSPI mode

LVDS0_IMGSIZE2_STATIS

LVDS0_IMGSIZE2_STATIS is an LVDS SEF2 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1688	LVDS0_IMGSIZE2_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight2																lvds_imgwidth2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight2	Height of the image transferred by virtual channel 2 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth2	Width of the image transferred by virtual channel 2 in LVDS or HiSPI mode

LVDS0_IMGSIZE3_STATIS

LVDS0_IMGSIZE3_STATIS is an LVDS SEF3 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x168C	LVDS0_IMGSIZE3_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight3																lvds_imgwidth3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight3	Height of the image transferred by virtual channel 3 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth3	Width of the image transferred by virtual channel 3 in LVDS or HiSPI mode

LVDS0_CTRL_INT_RAW

LVDS0_CTRL_INT_RAW is an LVDS read data raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F0	LVDS0_CTRL_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					link2_rderr_raw	link1_rderr_raw	link0_rderr_raw	reserved		lvds_stat_err_raw	lane11_sync_err_raw	lane10_sync_err_raw	lane9_sync_err_raw	lane8_sync_err_raw	lane7_sync_err_raw	lane6_sync_err_raw	lane5_sync_err_raw	lane4_sync_err_raw	lane3_sync_err_raw	lane2_sync_err_raw	lane1_sync_err_raw	lane0_sync_err_raw	link2_hsync_err_raw	link2_vsync_err_raw	link2_wrerr_raw	link1_hsync_err_raw	link1_vsync_err_raw	link1_wrerr_raw	link0_hsync_err_raw	link0_vsync_err_raw	link0_wrerr_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	WC	link2_rderr_raw	Link 2 read data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[25]	WC	link1_rderr_raw	Link 1 read data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[24]	WC	link0_rderr_raw	Link 0 read data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[23:22]	RO	reserved	Reserved
[21]	WC	lvds_stat_err_raw	LVDS status error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[20]	WC	lane11_sync_err_raw	Lane 11 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[19]	WC	lane10_sync_err_raw	Lane 10 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[18]	WC	lane9_sync_err_raw	Lane 9 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	WC	lane8_sync_err_raw	Lane 8 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	WC	lane7_sync_err_raw	Lane 7 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15]	WC	lane6_sync_err_raw	Lane 6 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[14]	WC	lane5_sync_err_raw	Lane 5 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[13]	WC	lane4_sync_err_raw	Lane 4 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[12]	WC	lane3_sync_err_raw	Lane 3 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	lane2_sync_err_raw	Lane 2 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	WC	lane1_sync_err_raw	Lane 1 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[9]	WC	lane0_sync_err_raw	Lane 0 synchronization error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	link2_hsync_err_raw	Link 2 HS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7]	WC	link2_vsync_err_raw	Link 2 VS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	WC	link2_wrerr_raw	Link 2 write data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	WC	link1_hsync_err_raw	Lane 1 HS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	WC	link1_vsync_err_raw	Lane 1 VS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	link1_wrerr_raw	Link 1 write data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	link0_hsync_err_raw	Lane 0 HS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	link0_vsync_err_raw	Lane 0 VS error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	link0_wrerr_raw	Link 0 write data error raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

LVDS0_CTRL_INT

LVDS0_CTRL_INT is an LVDS read data interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F4	LVDS0_CTRL_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					link2_rderr_st	link1_rderr_st	link0_rderr_st	reserved		lvds_stat_err_st	lane11_sync_err_st	lane10_sync_err_st	lane9_sync_err_st	lane8_sync_err_st	lane7_sync_err_st	lane6_sync_err_st	lane5_sync_err_st	lane4_sync_err_st	lane3_sync_err_st	lane2_sync_err_st	lane1_sync_err_st	lane0_sync_err_st	link2_hsync_err_st	link2_vsync_err_st	link2_wrerr_st	link1_hsync_err_st	link1_vsync_err_st	link1_wrerr_st	link0_hsync_err_st	link0_vsync_err_st	link0_wrerr_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	link2_rderr_st	Link 2 read data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	link1_rderr_st	Link 1 read data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	link0_rderr_st	Link 0 read data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[23:22]	RO	reserved	Reserved
[21]	RO	lvds_stat_err_st	LVDS status error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RO	lane11_sync_err_st	Lane 11 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RO	lane10_sync_err_st	Lane 10 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	lane9_sync_err_st	Lane 9 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

[17]	RO	lane8_sync_err_st	Lane 8 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	lane7_sync_err_st	Lane 7 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RO	lane6_sync_err_st	Lane 6 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RO	lane5_sync_err_st	Lane 5 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RO	lane4_sync_err_st	Lane 4 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RO	lane3_sync_err_st	Lane 3 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	lane2_sync_err_st	Lane 2 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	lane1_sync_err_st	Lane 1 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	lane0_sync_err_st	Lane 0 synchronization error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	link2_hsync_err_st	Link 2 HS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	link2_vsync_err_st	Link 2 VS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	link2_wrerr_st	Link 2 write data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

[5]	RO	link1_hsync_err_st	Link 1 HS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	link1_vsync_err_st	Link 1 VS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	link1_wrerr_st	Link 1 write data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	link0_hsync_err_st	Link 0 HS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	link0_vsync_err_st	Link 0 VS error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	link0_wrerr_st	Link 0 write data error interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

LVDS0_CTRL_INT_MSK

LVDS0_CTRL_INT_MSK is an LVDS read data interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x16F8	LVDS0_CTRL_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					link2_rderr_msk	link1_rderr_msk	link0_rderr_msk	reserved		lvds_stat_err_st_msk	lane11_sync_err_msk	lane10_sync_err_msk	lane9_sync_err_msk	lane8_sync_err_msk	lane7_sync_err_msk	lane6_sync_err_msk	lane5_sync_err_msk	lane4_sync_err_msk	lane3_sync_err_msk	lane2_sync_err_msk	lane1_sync_err_msk	lane0_sync_err_msk	link2_hsync_err_msk	link2_vsync_err_msk	link2_wrerr_msk	link1_hsync_err_msk	link1_vsync_err_msk	link1_wrerr_msk	link0_hsync_err_msk	link0_vsync_err_msk	link0_wrerr_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26]	RW	link2_rderr_msk	Link 2 read data error interrupt enable 0: masked 1: enabled
[25]	RW	link1_rderr_msk	Link 1 read data error interrupt enable 0: masked 1: enabled
[24]	RW	link0_rderr_msk	Link 0 read data error interrupt enable 0: masked 1: enabled
[23:22]	RO	reserved	Reserved
[21]	RW	lvds_stat_err_st_msk	LVDS status error interrupt enable 0: masked 1: enabled
[20]	RW	lane11_sync_err_msk	Lane 11 synchronization error interrupt enable 0: masked 1: enabled
[19]	RW	lane10_sync_err_msk	Lane 10 synchronization error interrupt enable 0: masked 1: enabled
[18]	RW	lane9_sync_err_msk	Lane 9 synchronization error interrupt enable 0: masked 1: enabled
[17]	RW	lane8_sync_err_msk	Lane 8 synchronization error interrupt enable 0: masked 1: enabled
[16]	RW	lane7_sync_err_msk	Lane 7 synchronization error interrupt enable 0: masked 1: enabled
[15]	RW	lane6_sync_err_msk	Lane 6 synchronization error interrupt enable 0: masked 1: enabled
[14]	RW	lane5_sync_err_msk	Lane 5 synchronization error interrupt enable 0: masked 1: enabled
[13]	RW	lane4_sync_err_msk	Lane 4 synchronization error interrupt enable 0: masked 1: enabled

[12]	RW	lane3_sync_err_msk	Lane 3 synchronization error interrupt enable 0: masked 1: enabled
[11]	RW	lane2_sync_err_msk	Lane 2 synchronization error interrupt enable 0: masked 1: enabled
[10]	RW	lane1_sync_err_msk	Lane 1 synchronization error interrupt enable 0: masked 1: enabled
[9]	RW	lane0_sync_err_msk	Lane 0 synchronization error interrupt enable 0: masked 1: enabled
[8]	RW	link2_hsync_err_msk	Link 2 HS error interrupt enable 0: masked 1: enabled
[7]	RW	link2_vsync_err_msk	Link 2 VS error interrupt enable 0: masked 1: enabled
[6]	RW	link2_wrerr_msk	Link 2 write data error interrupt enable 0: masked 1: enabled
[5]	RW	link1_hsync_err_msk	Link 1 HS error interrupt enable 0: masked 1: enabled
[4]	RW	link1_vsync_err_msk	Link 1 VS error interrupt enable 0: masked 1: enabled
[3]	RW	link1_wrerr_msk	Link 1 write data error interrupt enable 0: masked 1: enabled
[2]	RW	link0_hsync_err_msk	Link 0 HS error interrupt enable 0: masked 1: enabled
[1]	RW	link0_vsync_err_msk	Link 0 VS error interrupt enable 0: masked 1: enabled

[0]	RW	link0_wrerr_msk	Link 0 write data error interrupt enable 0: masked 1: enabled

LANE_ID0_CHN0

LANE_ID0_CHN0 is a link 0 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1700	LANE_ID0_CHN0	0x0000_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																lane3_id				lane2_id				lane1_id				lane0_id			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	lane3_id	Lane 3 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 3.
[11:8]	RW	lane2_id	Lane 2 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 2.
[7:4]	RW	lane1_id	Lane 1 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 1.
[3:0]	RW	lane0_id	Lane 0 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 0.

LANE_ID1_CHN0

LANE_ID1_CHN0 is a link 1 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1704	LANE_ID1_CHN0	0x0000_7654

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				lane7_id	lane6_id	lane5_id	lane4_id
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	lane7_id	Lane 7 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 7.
[11:8]	RW	lane6_id	Lane 6 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 6.
[7:4]	RW	lane5_id	Lane 5 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 5.
[3:0]	RW	lane4_id	Lane 4 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 4.

LANE_ID2_CHN0

LANE_ID2_CHN0 is a link 2 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1708	LANE_ID2_CHN0	0x0000_BA98

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				lane11_id	lane10_id	lane9_id	lane8_id
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 1	1 0 1 0	1 0 0 1	1 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:12]	RW	lane11_id	Lane 11 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 11.
[11:8]	RW	lane10_id	Lane 10 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 10.
[7:4]	RW	lane9_id	Lane 9 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 9.
[3:0]	RW	lane8_id	Lane 8 channel ID Value range: 0−11 The field value indicates the ID of image sensor channel connected to lane 8.

ALIGN0_INT_RAW

ALIGN0_INT_RAW is an MIPI_ALIGN raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x17F0	ALIGN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err_lane11_raw	err_lane10_raw	err_lane9_raw	err_lane8_raw	err_lane7_raw	err_lane6_raw	err_lane5_raw	err_lane4_raw	err_lane3_raw	err_lane2_raw	err_lane1_raw	err_lane0_raw	err_full_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	err_lane11_raw	MIPI_ALIGN lane 11 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	err_lane10_raw	MIPI_ALIGN lane 10 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[10]	WC	err_lane9_raw	MIPI_ALIGN lane 9 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	WC	err_lane8_raw	MIPI_ALIGN lane 8 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	err_lane7_raw	MIPI_ALIGN lane 7 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7]	WC	err_lane6_raw	MIPI_ALIGN lane 6 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	WC	err_lane5_raw	MIPI_ALIGN lane 5 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	WC	err_lane4_raw	MIPI_ALIGN lane 4 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	WC	err_lane3_raw	MIPI_ALIGN lane 3 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	err_lane2_raw	MIPI_ALIGN lane 2 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err_lane1_raw	MIPI_ALIGN lane 1 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err_lane0_raw	MIPI_ALIGN lane 0 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err_full_raw	MIPI_ALIGN FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

ALIGN0_INT

ALIGN0_INT is an MIPI_ALIGN interrupt status register.

Offset Address	Register Name	Total Reset Value
0x17F4	ALIGN0_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err_lane11_st	err_lane10_st	err_lane9_st	err_lane8_st	err_lane7_st	err_lane6_st	err_lane5_st	err_lane4_st	err_lane3_st	err_lane2_st	err_lane1_st	err_lane0_st	err_full_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	err_lane11_st	MIPI_ALIGN lane 11 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	err_lane10_st	MIPI_ALIGN lane 10 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	err_lane9_st	MIPI_ALIGN lane 9 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	err_lane8_st	MIPI_ALIGN lane 8 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	err_lane7_st	MIPI_ALIGN lane 7 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	err_lane6_st	MIPI_ALIGN lane 6 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	err_lane5_st	MIPI_ALIGN lane 5 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	err_lane4_st	MIPI_ALIGN lane 4 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

[4]	RO	err_lane3_st	MIPI_ALIGN lane 3 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err_lane2_st	MIPI_ALIGN lane 2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err_lane1_st	MIPI_ALIGN lane 1 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err_lane0_st	MIPI_ALIGN lane 0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err_full_st	MIPI_ALIGN FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

ALIGN0_INT_MSK

ALIGN0_INT_MSK is an MIPI_ALIGN interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x17F8	ALIGN0_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				err_lane11_mask	err_lane10_mask	err_lane9_mask	err_lane8_mask	err_lane7_mask	err_lane6_mask	err_lane5_mask	err_lane4_mask	err_lane3_mask	err_lane2_mask	err_lane1_mask	err_lane0_mask	err_full_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	err_lane11_mask	MIPI_ALIGN lane 11 interrupt enable 0: masked 1: enabled

[11]	RW	err_lane10_mask	MIPI_ALIGN lane 10 interrupt enable 0: masked 1: enabled
[10]	RW	err_lane9_mask	MIPI_ALIGN lane 9 interrupt enable 0: masked 1: enabled
[9]	RW	err_lane8_mask	MIPI_ALIGN lane 8 interrupt enable 0: masked 1: enabled
[8]	RW	err_lane7_mask	MIPI_ALIGN lane 7 interrupt enable 0: masked 1: enabled
[7]	RW	err_lane6_mask	MIPI_ALIGN lane 6 interrupt enable 0: masked 1: enabled
[6]	RW	err_lane5_mask	MIPI_ALIGN lane 5 interrupt enable 0: masked 1: enabled
[5]	RW	err_lane4_mask	MIPI_ALIGN lane 4 interrupt enable 0: masked 1: enabled
[4]	RW	err_lane3_mask	MIPI_ALIGN lane 3 interrupt enable 0: masked 1: enabled
[3]	RW	err_lane2_mask	MIPI_ALIGN lane 2 interrupt enable 0: masked 1: enabled
[2]	RW	err_lane1_mask	MIPI_ALIGN lane 1 interrupt enable 0: masked 1: enabled
[1]	RW	err_lane0_mask	MIPI_ALIGN lane 0 interrupt enable 0: masked 1: enabled
[0]	RW	err_full_mask	MIPI_ALIGN FIFO interrupt enable 0: masked 1: enabled

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10 ISP

10.1 Introduction

The image signal processor (ISP) module of Hi3519 V100 supports standard sensor picture data processing. The ISP module provides basic functions such as automatic white balance (AWB), automatic exposure (AE), demosaic, defect pixel correction (DPC), and digital image stabilization (DIS) as well as advanced functions such as wide dynamic range (WDR), dynamic range compression (DRC), and denoising. The picture processing functions supported by the ISP module of Hi3519 V100 are as follows:

- Black level correction (BLC)
- Static and dynamic DPC and defect pixel cluster correction
- Bayer denoising
- Fixed pattern noise (FPN) removal
- Advanced demosaic
- Gamma correction
- DRC
- Sensor built-in WDR
- 4-/3-/2-frame combination WDR
- AWB
- AE
- Automatic focus (AF)
- 3A (AE, AF, AWB) statistics output
- Lens shading correction (LSC)
- Picture sharpening
- DIS
- Automatic anti-fog
- Color management and enhancement

The processing capability of the ISP module is as follows:

- Maximum 14-bit Bayer data input
- Maximum picture resolution of 4608 x 3456
- Minimum picture resolution of 480 x 240
- Maximum frame rate of 15 fps for the 4608 x 3456 resolution

- Maximum frame rate of 30 fps for the 4152 x 2174 resolution
- Minimum horizontal blanking region of 64 pixels
- Minimum vertical blanking region of 30 lines

10.2 Overview

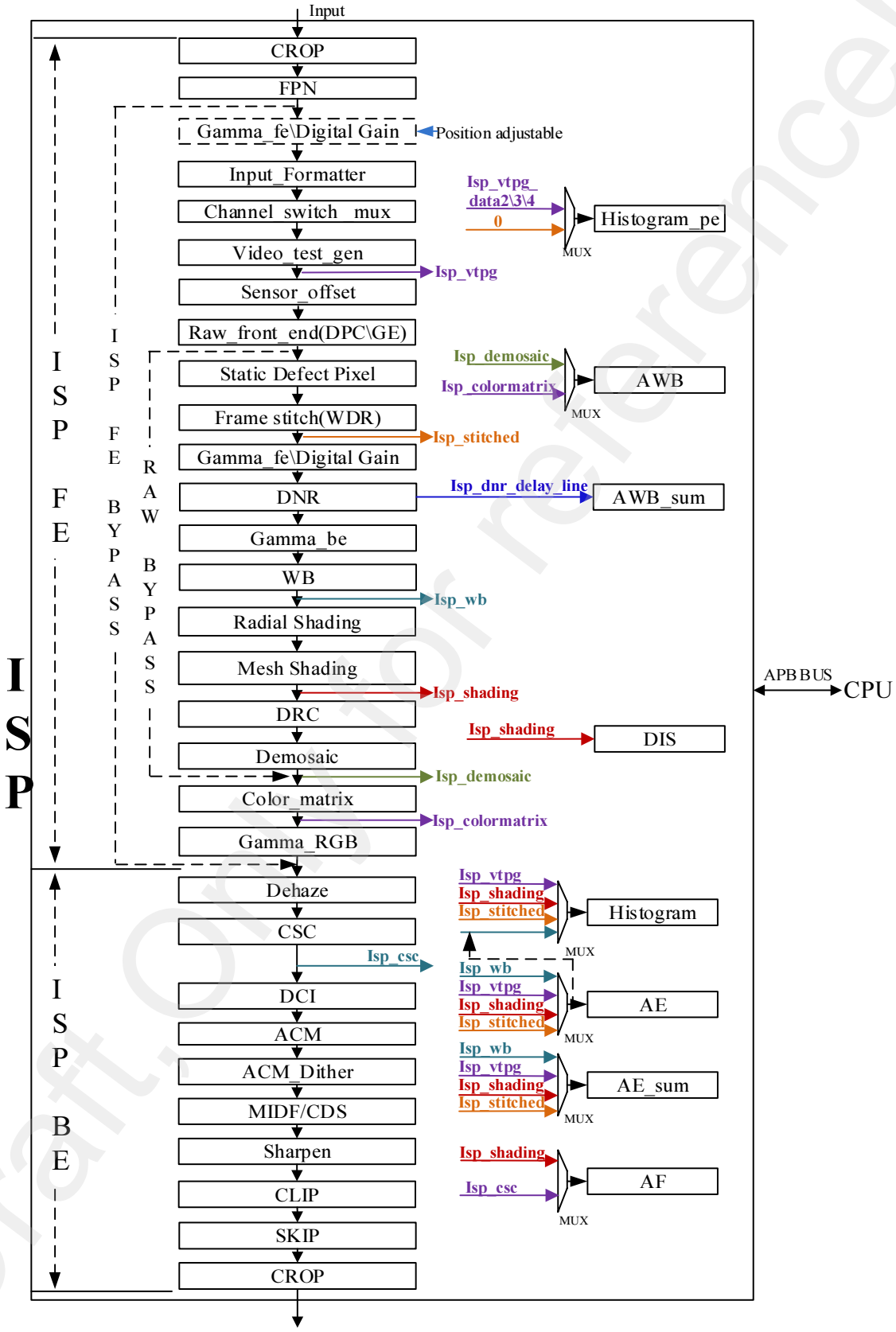
Functional Block Diagram

The base address of ISP registers is 0x11380000. The actual address of an ISP register is the base address plus the corresponding offset address. Figure 10-1 shows the functional block diagram of the ISP module. In this document, ISP_FE indicates the part before the dehaze module in the ISP pipeline, and the ISP_BE indicates the part after the dehaze module as well as the dehaze module in the ISP pipeline.

NOTE

In this document, *U**.* and *S**.* represent the unsigned number and the signed number respectively. For example, U8.8 indicates that the data is an unsigned number consisting of an 8-bit integral part and an 8-bit decimal part. S8.8 indicates that the data is a signed number consisting of an 8-bit integral part (including a sign bit) and an 8-bit decimal part.

Figure 10-1 Functional block diagram of the ISP module



Operating Mode

The ISP module supports the following operating modes:

- Maximum 14-bit raw RGB Bayer data input

  When the input data width is less than 14 bits, the upper bits need to be aligned and the lower bits need to be stuffed with 0s. In this mode, any sequence of the R, Gr, Gb, and B components is supported, and the sequence can be changed by configuring ISPFE_RGGB_START, ISP_DIS_CTRL_F, and ISP_FPN_CTRL_F.

- 4-/3-/2-frame combination WDR
  - 4152 x 2174 resolution supported in 2-frame combination WDR mode
  - 1920 x 1080 resolution supported in 3-/4-frame combination WDR mode
- Infrared (IR) mode

  In this mode, ISP_SKIP_C_CFG in the skip module needs to be set to **0x00000000** so that the C (U and V) component is discarded and the ISP module outputs only the Y component picture data.

- External ISP mode

  The YUV data input is supported in external ISP mode.

Table 10-1 describes the key parameters in external ISP mode.

Table 10-1 Key parameters in external ISP mode

Parameter	Description
BUF_MODE (0x11380070)	Register in the video capture (VICAP) module, indicating the line_buf input data mode 0: raw data 1: YUV422
ISP_SEL bit[6:4] (0x11380050)	ISP_BE input data select 000: ISP_BE connects to ISP_FE (for the raw input). 001: ISP_BE connects to LINE_BUF (for the YUV input). 011: ISP_BE connects to SRC 0 (for debugging). 100: ISP_BE connects to SRC 1 (for debugging). 101: ISP_BE connects to SRC 2 (for debugging). 110: ISP_BE connects to SRC 3 (for debugging). Other values: reserved

  In external ISP mode, ISP_SEL needs to be set to **0x1** to mask the raw field module, and BUF_MODE in the VICAP module needs to be set to **0x1** so that the VICAP line_buf input data is in YUV422 format.

- Adjustable module position

  The positions of the gamma FE/digital gain, AWB, AF, histogram, AE, and AE_SUM modules are adjustable. Table 10-2 describes the module position adjustment parameters.

Table 10-2 Key module position adjustment parameters

ISP_MODULE_POS	Description
ISPFE_AE_SWITCH bit[1:0]	AE statistics position select 00: after the static white balance module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module
ISPFE_AE_SWITCH bit[17:16]	AE sum statistics position select 00: after the static white balance module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module
ISPFE_AWB_SWITCH bit[0]	RGB field AWB statistics module position select 0: before the color matrix 1: after the color matrix
ISPFE_HISTOGRAM_SWITCH bit[1:0]	AE global histogram position select 00: in the same position as the AE module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module
ISPFE_MODULE_BYPASS bit[0]	Module gamma FE/digital gain position select 0: after the WDR stitching module 1: in the front part of ISP_FE
ISPFE_MODULE_BYPASS bit[1]	Digital gain position select 0: after the module FE gamma LUTs 1: before the module FE gamma LUTs
ISP_SEL bit [16] (0x11380050)	AF input data select 0: The AF connects to ISP_FE. 1: The AF connects to ISP_BE.

Memory Read and Write Solutions

Table 10-3 Module direct read/write memory address mapping

Range of the Memory Offset Address	Module to Which the Memory Belongs
0x21200−0x2127C, 0x21280−0x212FC, 0x21300−0x2137C, 0x21380−0x213FC	NOISE_PROFILE_FRAME_STITCH
0x21540−0x21560	DNR_SHADING

Range of the Memory Offset Address	Module to Which the Memory Belongs
0x21580–0x215FC, 0x21600–0x2167C, 0x21680–0x216FC, 0x21700–0x2177C	NOISE_PROFILE_RAW_FRONTEND
0x21800–0x2187C	NOISE_PROFILE_LUT
0x21880–0x218FC	NOISE_PROFILE_DEMOSAIC
0x21900–0x219FC	AEXP_WEIGHT
0x21B00–0x21EFC	AWB_WEIGHT
0x22800–0x22880, 0x23000–0x23400	GAMMA_FE
0x24800–0x24880, 0x25000–0x25400	GAMMA_BE
0x26000–0x26200, 0x26400–0x26600, 0x26800–0x26A00	RADIAL_SHADING
0x28000–0x2DFFC	METERING_MEM
0x30000–0x33FFC	DEFECT_PIXEL_MEM
0x34000–0x34FFC, 0x35000–0x353FC, 0x35400–0x357FC, 0x35800–0x35BFC	HISTOGRAM1_MEM
0x37000–0x37400	GAMMA_RGB_MEM
0x38000–0x38200, 0x38800–0x38A00	DRC
0x39000–0x393FC	CMD_QUEUES
0x3C000–0x3EFFC	MESH_SHADING

Table 10-4 Module indirect read/write memory address mapping

Range of the Memory Offset Address	Module to Which the Memory Belongs
0x62488–0x6249C	DIS
0x63a80–0x63a8C	FPN
0x46280–0x462BC	Dehaze

The ISP memory in Table 10-3 is directly read or written in the same way as the general registers, whereas the ISP memory in Table 10-4 is indirectly read or written. Within the range of the memory address segments, the read data register (RDATA), read address register (RADDR), write data register (WDATA), and write address register (WADDR) are provided. The following describes how to read or write to the ISP memory indirectly.

To read the memory, perform the following steps:

Step 1 Write the start address of the data to be read in the memory to the read address register (RADDR).

Step 2 Read the read data register (RDATA) continuously. The address is automatically incremented by 1 in the logic each time the register is read.

----End

To write to the memory, perform the following steps:

Step 1 Write the start address of data in the memory to the write address register (WADDR).

Step 2 Write data to the write data register (WADDR) continuously. The address is automatically incremented by 1 in the logic each time the register is written.

----End

10.3 Interrupt System

Function Description

The ISP interrupt system supports 23 independent interrupts, among which 16 interrupts (int0−int15 in Table 10-5) can be selected from 22 interrupt sources. The 22 interrupt sources include the AE, AWB, and histogram statistics completion interrupt, and start of frame (SOF) interrupt as well as end of frame (EOF) interrupt for modules in the pipeline. For details, see Table 10-6.

As shown in Table 10-7, the corresponding interrupt is reported after the interrupt vectors of the 22 interrupt sources are configured by setting parameters **interrupt0_source** to **interrupt15_source** based on the description in Table 10-6.

Table 10-5 Interrupt indicator registers

Offset Address	Event	Bit	Description
0x400F0	reserved	31:17	Reserved
	acm_para_finish	16	Status of the ACM lookup table load completion interrupt
	reserved	15:4	Reserved
	fstart_delay	3	Configurable trigger delay interrupt
	cfg_loss	2	Status of the register configuration loss interrupt
	update_cfg	1	Status of the register update interrupt
	fstart	0	ISP SOF interrupt indicator register
0x600F0	reserved	31:18	Reserved
	fe_fstart	17	ISP FE SOF interrupt

Offset Address	Event	Bit	Description
	int_disstat	16	DIS current frame statistics completion interrupt
	int15	15	ISP interrupt 15 indicator register
	int14	14	ISP interrupt 14 indicator register
	int13	13	ISP interrupt 13 indicator register
	int12	12	ISP interrupt 12 indicator register
	int11	11	ISP interrupt 11 indicator register
	int10	10	ISP interrupt 10 indicator register
	int9	9	ISP interrupt 9 indicator register
	int8	8	ISP interrupt 8 indicator register
	int7	7	ISP interrupt 7 indicator register
	int6	6	ISP interrupt 6 indicator register
	int5	5	ISP interrupt 5 indicator register
	int4	4	ISP interrupt 4 indicator register
	int3	3	ISP interrupt 3 indicator register
	int2	2	ISP interrupt 2 indicator register
	int1	1	ISP interrupt 1 indicator register
	int0	0	ISP interrupt 0 indicator register

Table 10-6 Interrupt event sources

Interrupt Type	Interrupt Event Source	Interrupt Vector
Statistics completion interrupt	Automatic exposure	8
	Automatic white balance	9
	Automatic exposure histogram	11

Interrupt Type	Interrupt Event Source	Interrupt Vector
	Per exposure automatic exposure histograms	12
	Automatic exposure sum	13
	Automatic white balance sum	14
SOF interrupt	ISP input	24
	WDR stitch	25
	Static defect pixel	26
	DNR	27
	Shading	28
	DRC	29
	Demosaic	30
	ISP output	31
EOF interrupt	ISP input	16
	WDR stitch	17
	Static defect pixel	18
	DNR	19
	Shading	20
	DRC	21
	Demosaic	22
	ISP output	23

Table 10-7 Key interrupt source parameters

Parameter	Description
interrupt0_source−interrupt15_source (0x20080−0x2009C)	16 independent interrupt select registers. The interrupt sources can be selected from the 22 interrupt sources in Table 10-6. Then the corresponding interrupt vector needs to be written.

Interrupt Timing

The positions of many interrupts are determined by the ISP module switch and register configuration. Figure 10-2 shows the position of each interrupt. Note that the interrupt position is arranged based on the time sequence in a frame. Table 10-8 describes the mapping between the interrupt ID and the interrupt event shown in Figure 10-2, the number of lines

between the interrupt and the first rising edge of VALID_I, and the number of lines between the interrupt and the last falling edge of VALID_I.

Figure 10-2 Interrupt timing

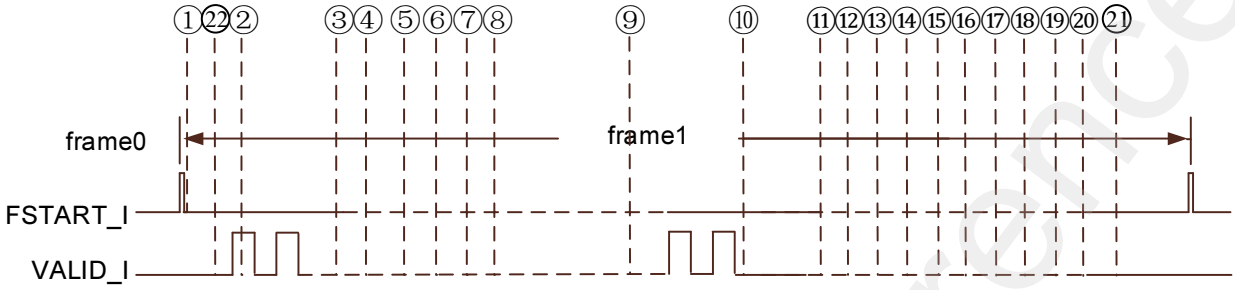


Table 10-8 Mapping between the interrupt ID and the interrupt event

No.	Interrupt Event	Number of Lines Between the Interrupt and the First Rising Edge of VALID_I	Number of Lines Between the Interrupt and the Last Falling Edge of VALID_I
1	fe_fstart/be_fstart/be_update_cfg/be_cfg_loss	N/A	N/A
2	ISP input (24)	0	N/A
3	Static defect pixel (26)	2	N/A
4	WDR stitch (25)	3	N/A
5	DNR (27) Shading (28)	11	N/A
6	DRC (29)	12	N/A
7	Demosaic (30)	16	N/A
8	ISP output (31)	18	N/A
9	int_disstat	N/A	N/A
10	ISP Input (16)	N/A	0
11	Per exposure automatic exposure histograms (12)	N/A	1
12	Static defect pixel (18)	N/A	2
13	WDR stitch (17)	N/A	3
14	DNR (19) Shading (20)	N/A	11
15	DRC (21)	N/A	12

No.	Interrupt Event	Number of Lines Between the Interrupt and the First Rising Edge of VALID_I	Number of Lines Between the Interrupt and the Last Falling Edge of VALID_I
16	Automatic exposure sum (13) Automatic exposure (8)	N/A	14
17	Automatic exposure histogram (11)	N/A	15
18	Demosaic (22)	N/A	16
19	ISP output (23) Auto white balance (9)	N/A	18
20	Auto white balance sum (14)	N/A	21
21	be_fstart_delay	N/A	N/A
22	acm_para_finish	N/A	N/A

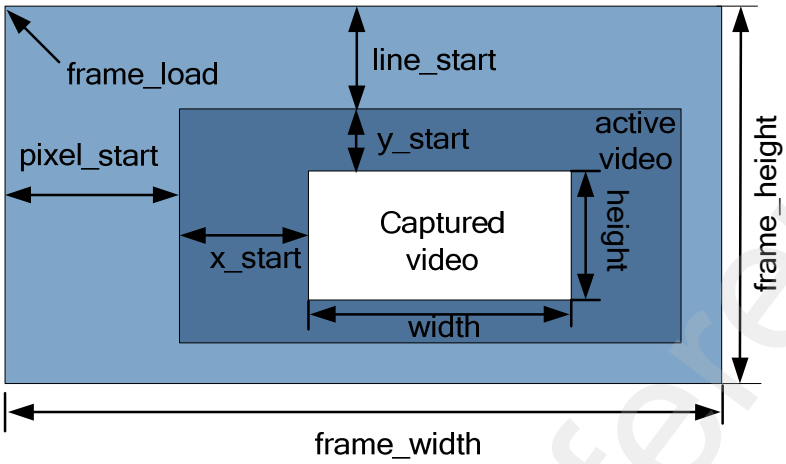
10.4 Module Functions

Crop

The crop module crops the input picture. The actual displayed view area always falls within the valid video range. That is, compared with the valid video area, the actual displayed view area shrinks, which avoids the edge effect.

As shown in Figure 10-3, the crop module crops the valid picture area by configuring y_start, x_start, height, and width.

Figure 10-3 Relationship between the valid picture area and the horizontal/vertical blanking region



FPN

The FPN module corrects the sensor input picture based on the calibrated black frame or black line to remove the FPNs of the sensor.

The FPN module supports calibration and correction in frame mode and line mode. This module needs to be enabled if the FPNs of the connected sensor are obvious, and does not need to be enabled if the the FPNs of the connected sensor are not obvious.

Video test gen

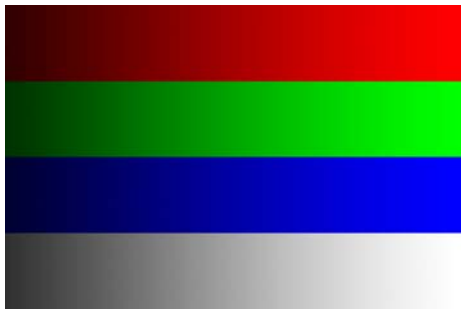
The color_bar module supports the following five picture types:

- Pure color picture configured by VIDEO_TEST_R_BACKGND[rbackgnd], VIDEO_TEST_G_BACKGND[gbackgnd], and VIDEO_TEST_B_BACKGND[bbackgnd]

Figure 10-4 Pure color picture

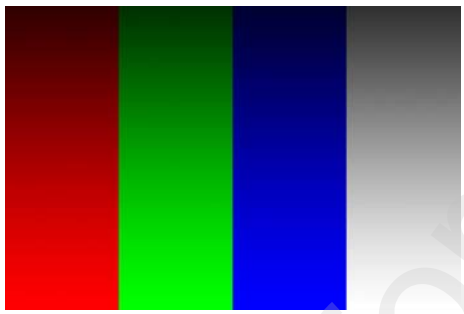
- Picture consisting of four horizontal color stripes. The luminance from left to right is variable and the start value and increment are configurable.

Figure 10-5 Picture consisting of four horizontal color stripes



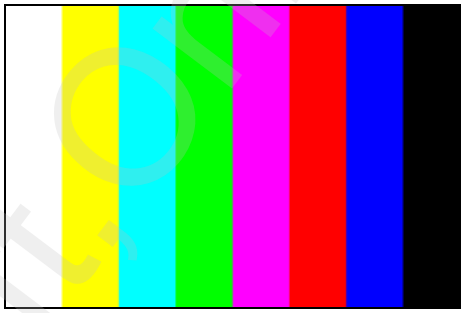
- Picture consisting of four vertical color stripes. The luminance from top to bottom is variable and the start value and increment are configurable.

Figure 10-6 Picture consisting of four vertical color stripes



- Picture consisting of eight vertical color stripes. The luminance is configured by VIDEO_TEST_R_BACKGND[rbackgnd], VIDEO_TEST_G_BACKGND[gbackgnd], and VIDEO_TEST_B_BACKGND[bbackgnd].

Figure 10-7 Picture consisting of eight vertical color stripes



- Picture with a rectangular pure color target area on the pure color background. The background color is configured by VIDEO_TEST_R_BACKGND[rbackgnd], VIDEO_TEST_G_BACKGND gbackgnd], and VIDEO_TEST_B_BACKGND[bbackgnd]. The color of the target area is configured by VIDEO_TEST_R_FOREGND[rforegnd], VIDEO_TEST_G_FOREGND[gforegnd], and VIDEO_TEST_B_FOREGND[bforegnd].

Figure 10-8 Picture with a rectangular pure color target area on the pure color background

Sensor Offset

The sensor offset module provides the sensor BLC function. It compensates four Bayer color channels (R, Gr, Gb, and B) by using four independent parameters (**black00**, **black01**, **black10**, and **black11**).

DPC

The DPC module is used to correct the defect pixels of the sensor, and supports static DPC as well as dynamic DPC. For the static DPC, at most 4096 defect pixels can be corrected, and the defect pixels are corrected after their coordinates are calibrated. For the dynamic DPC, there is no limit on the maximum number of corrected defect pixels, and the coordinates of the defect pixels do not need to be calibrated before correction. The static DPC is more accurate than the dynamic DPC.

GE

The GE module equalizes the Gb and Gr channels when imbalance occurs and improves the picture quality in some scenarios.

WDR

The WDR module supports the multi-frame combination WDR function. In the scenarios with a large dynamic range, the details of the bright and dark regions are still visible.

Gamma FE

The gamma FE module is used to compress the bit width of the picture data. There are two compression modes, or the compression curve can be expressed in two ways. The compression curve can be expressed by two LUTs. LUT0 contains 33 points with 20-bit precision and LUT1 contains 257 points with 20-bit precision. The compression curve can also be expressed by the following formula:

$$y = \frac{2^{32} \times x}{\alpha_{companding} \times 2^{24} + (4096 - \alpha_{companding})}$$

where

x indicates the input picture data, y indicates the output picture data, and $\alpha_{companding} < 4096$

Digital Gain

The digital gain module provides the digital gain, and supports U5.8-precision gain configuration as well as U20-precision black level compensation.

DNR

The DNR module implements picture denoising in the Bayer domain to retain details while removing noises. This module can remove noises for the sensor based on the noise model provided by the user.

Gamma BE

The gamma BE module is used to extend the bit width of the picture data. There are two extension modes, or the extension curve can be expressed in two ways. The extension curve can be expressed by two LUTs. LUT0 contains 33 points with 20-bit precision and LUT1 contains 257 points with 20-bit precision. The extension curve can also be expressed by the following formulas:

$$y = \frac{2^{32} \times x}{\alpha_{decompanding} \times 2^{24} + (4096 - \alpha_{decompanding})}$$

$$\alpha_{decompanding} = \frac{2^{24}}{\alpha_{companding}}$$

where

x indicates the input picture data, y indicates the output picture data, and $\alpha_{decompanding} > 4096$

WB

The WB module provides the white balance function, and configures the gains as well as offsets of the R, Gr, Gb, and B components.

Mesh Shading

The mesh shading module implements LSC. Each pixel provides the 8-bit gains of three components (R, G, and B). At most 12,288 pixels (3 x 64 x 64) can be configured, and other pixels can be obtained through interpolation.

Radial Shading

The radial shading is a backup solution of the mesh shading. Different from the mesh shading that uses the mesh model, the radial shading uses the radial model. In the radial shading module, each color channel (R, G, or B) provides three groups of correction coefficients.

DRC

The DRC module adjusts the display dynamic range of the picture so that the picture display effect on the display device is consistent with the picture observed by human eyes.

Demosaic

The demosaic module converts the raw picture in Bayer format into the RGB picture.

Color Matrix

The color matrix module implements linear correction on the {R, G, B} input by using a standard 3 x 3 matrix. The functions such as saturation adjustment and color correction can be implemented by dynamically adjusting the matrix coefficients.

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} m_{RR} & m_{RG} & m_{RB} \\ m_{GR} & m_{GG} & m_{GB} \\ m_{BR} & m_{BG} & m_{BB} \end{pmatrix} \cdot \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

Gamma_RGB

The gamma-RGB module applies to the three color channels (R, G, and B) and outputs the gamma-RGB adjustment result. The gamma curve consists of 257 nodes (node 0 to node 256). The curve value corresponding to each node is a 16-bit unsigned number. The points between two nodes can be obtained through interpolation. The curve value of node 0 (gamma[0]) is 0 and the curve value of node 256 (gamma[256]) is 0xFFFF.

AF

The AF module collects statistics on picture definition evaluation information and implements AF. The number of picture blocks is configurable. This module supports a maximum of 17 x 15 blocks. The minimum block size is 32 x 32 and the maximum block size is 511 x 511. The definition evaluation information about each zone is provided.

AE

The AE module collects AE statistics. Software adjusts the sensor based on statistics to implement AE. A picture is divided into 17 x 15 (17 lines and 15 columns) regions, and the weight of each region is configurable. The 5-segment histogram statistics are collected on each region and are normalized to 0xFFFF. Therefore, only the statistics of the 0, 1, 3, and 4 segments are stored. The weighted statistics or the statistics of each zone can be read. The global histogram statistics are also provided. As shown in Figure 10-1, the histogram module provides the 1024-segment histogram statistics of one data channel, and the histogram_pe module provides the 256-segment histogram statistics of three data channels.

AWB

The AWB module provides the RGB field white point statistics. Software adjusts the gains of the R, G, and B channels (**Rgain**, **Ggain**, and **Bgain**) based on the statistics to implement the AWB function. The RGB field statistics are after the demosaic module. A picture is divided into 32 x 32 (32 lines and 32 columns) regions. The number of pixels that meet the white point condition is counted for each region, and the average G/R and G/B values of the white points are calculated.

AWB Sum

The AWB sum module provides the Bayer field white point statistics. Software adjusts the gains of the R, G, and B channels (**Rgain**, **Ggain**, and **Bgain**) based on the statistics to

implement the AWB function. The Bayer field statistics are before the WB gain. A picture is divided into 32 x 32 (32 lines and 32 columns) regions. The number of pixels that meet the white point condition is counted for each region, and the average R, G, and B values of the white points are calculated.

Dehaze

The dehaze module provides the powerful zoned anti-fog function and improves video contrast and in the haze scenario. The picture can be divided into multiple regions by configuring ISP_DEHAZE_BLK_NUM. A maximum of 32 x 32 regions are supported.

This module analyzes the picture characteristics of each region, obtains the contrast specifications of each region, and implements pixel enhancement in each region. The enhancement strength of a pixel depends on the contrast specifications of the region this pixel belongs to and those of the neighboring regions.

CSC

The CSC module converts the {R, G, B} input into {Y, U, V} by using the standard 3 x 3 matrix and vector offset, and implements saturation adjustment and color correction by dynamically adjusting the matrix coefficient.

$$\begin{pmatrix} Y \\ U \\ V \end{pmatrix} = \begin{pmatrix} coef00 & coef01 & coef02 \\ coef10 & coef11 & coef12 \\ coef20 & coef21 & coef22 \end{pmatrix} \times \begin{pmatrix} R \\ G \\ B \end{pmatrix} + \begin{pmatrix} out\_dc0 \\ out\_dc1 \\ out\_dc2 \end{pmatrix}$$

The parameters can be changed based on format conversion requirements.

DCI

The DCI module dynamically improves the picture contrast, and automatically adjusts picture luminance and contrast based on the picture luminance statistics to resolve issues (for example, the picture is too dark or too bright, and the contrast is too high or too low) so that excellent display effect can be achieved on the display device.

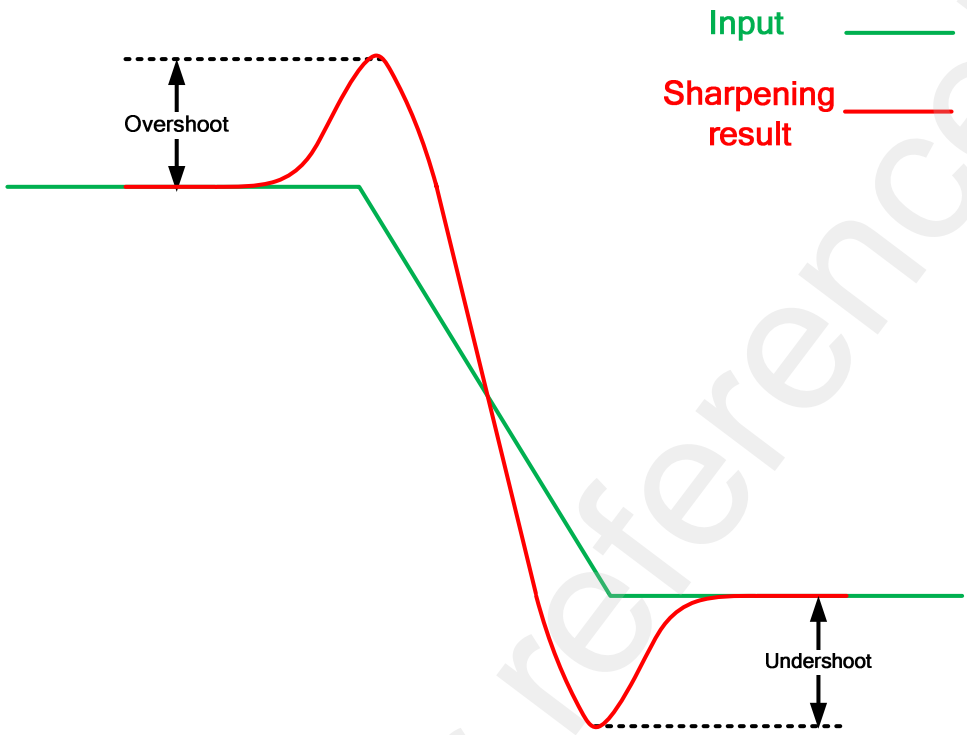
ACM

The ACM implements automatic color management, corrects hue offset, compensates for saturation loss and the performance difference between color gamuts, and enhances specific colors such as the complexion, green, and blue based on user preference and style.

Sharpen

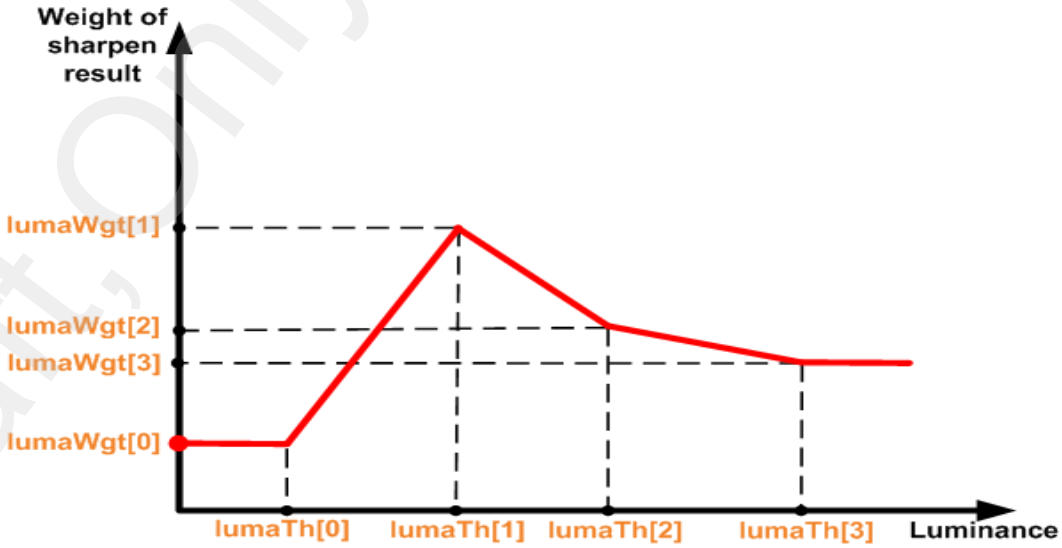
The sharpen module implements picture sharpening to improve picture definition. The sharpening strength can be adjusted by configuring the control parameters **edge_amt** and **sharp_amt**. Note that noises may be amplified if the sharpening strength is too high. Software adjusts parameter configurations based on the ISO value to achieve a balance between the definition and noise suppression while improving the visual effect of the picture.

Figure 10-9 Overshoot and undershoot occurrence during sharpening



In addition, white borders and black borders may appear due to the large positive and negative edge amplification caused by sharpening, as shown in Figure 10-9. The white borders and black borders can be suppressed by adjusting the overshoot and undershoot control parameters.

Figure 10-10 Luminance control sharpening gain curve



As shown in Figure 10-10, the luminance control sharpening gain curve can be adjusted to control the sharpening gains of the bright region and the dark region. In this way, the

definition of the bright region can be improved, and the noises in the dark region can be suppressed.

In addition, the sharpen module can separately control the edge jag strength and detail texture sharpening strength of the picture after sharpening.

MCDS

The MCDS module can convert the YUV444 data to YUV422 or YUV420 data, and implement picture chrominance denoising.

The MCDS module can implement multi-order horizontal filtering in the horizontal direction of the chrominance. When the YUV420 output is required, this module implements average down sampling in the vertical direction of the chrominance. The visual loss caused by picture conversion can be minimized by setting the filtering parameters to appropriate values.

The MCDS module implements denoising only on the picture chrominance component. Therefore, the picture luminance is not affected. The denoising strength of the MCDS module can be adjusted to achieve a balance between chrominance noise removal and color detail reservation.

10.5 Register Summary

Table 10-9 describes ISP registers.

Table 10-9 Summary of ISP registers (base address: 0x1138_0000)

Offset Address	Register	Description	Page
0x12000	ISP_AF_CFG	AF control register	10-52
0x12010	ISP_AF_ZONE	AF block configuration register	10-55
0x12014	ISP_AF_CROP_START	AF picture crop start coordinate register	10-55
0x12018	ISP_AF_CROP_SIZE	AF picture crop size register	10-56
0x1201C	ISP_AF_MEAN_THRES	AF median filtering threshold register	10-56
0x12020	ISP_AF_IIRG0	AF IIR filtering parameter register 0	10-57
0x12024	ISP_AF_IIRG1	AF IIR filtering parameter register 1	10-57
0x12028	ISP_AF_IIRG2	AF IIR filtering parameter register 2	10-58
0x1202C	ISP_AF_IIRG3	AF IIR filtering parameter register 3	10-58
0x12030	ISP_AF_IIRG4	AF IIR filtering parameter register 4	10-59

Offset Address	Register	Description	Page
0x12034	ISP_AF_IIRG5	AF IIR filtering parameter register 5	10-59
0x12038	ISP_AF_IIRG6	AF IIR filtering parameter register 6	10-60
0x1203C	ISP_AF_IIRPL	AF IIR filter preset register	10-61
0x12040	ISP_AF_SHIFT	AF IIR filtering shift parameter register	10-61
0x12050	ISP_AF_FIRH0	AF FIR filtering parameter register 0	10-62
0x12054	ISP_AF_FIRH1	AF FIR filtering parameter register 1	10-63
0x12058	ISP_AF_FIRH2	AF FIR filtering parameter register 2	10-63
0x1205C	ISP_AF_FIRH3	AF FIR filtering parameter register 3	10-64
0x12060	ISP_AF_FIRH4	AF FIR filtering parameter register 4	10-65
0x12078	ISP_AF_ACC_SHIFT	AF cumulative statistics shift register	10-65
0x1207C	ISP_AF_CNT_SHIFT	AF count statistics shift register	10-66
0x12088	ISP_AF_STAT_IND_RADDR	Statistics indirect read address register for AF blocks	10-66
0x1208C	ISP_AF_STAT_IND_RDATA	Statistics indirect read data register for AF blocks	10-67
0x120E4	ISP_AF_CTRL_I	Immediate update control register	10-67
0x120EC	ISP_AF_UPDATE	Configuration update register	10-68
0x120F0	ISP_AF_SIZE	AF picture size register	10-68
0x12100	ISP_AF_IIRTHRE	AF IIR filtering threshold register	10-69
0x12104	ISP_AF_IIRGAIN	AF IIR filtering gain register	10-69
0x12108	ISP_AF_IIRSLOPE	AF IIR filtering slope register	10-70
0x1210C	ISP_AF_IIRDILATE	AF IIR filtering dilate register	10-70
0x12110	ISP_AF_FIRTHRE	AF FIR filtering threshold register	10-71
0x12114	ISP_AF_FIRGAIN	AF FIR filtering gain register	10-72

Offset Address	Register	Description	Page
0x12118	ISP_AF_FIRSLOPE	AF FIR filtering slope register	10-72
0x12120	ISP_AF_IIRTHRE_CORING	AF IIR filter coring threshold register	10-73
0x12124	ISP_AF_IIRPEAK_CORING	AF IIR filter coring peak register	10-73
0x12128	ISP_AF_IIRSLOPE_CORING	AF IIR filter coring slope register	10-74
0x12130	ISP_AF_FIRTHRE_CORING	AF FIR filter coring threshold register	10-74
0x12134	ISP_AF_FIRPEAK_CORING	AF FIR filter coring peak register	10-75
0x12138	ISP_AF_FIRSLOPE_CORING	AF FIR filter coring slope register	10-75
0x12140	ISP_AF_HILIGHT	AF highlight threshold register	10-76
0x12144	ISP_AF_OFFSET	AF offset configuration register	10-76
0x20010	ISPFE_ACTIVE_WIDTH	Picture width register	10-77
0x20014	ISPFE_ACTIVE_HEIGHT	Picture height register	10-77
0x20018	ISPFE_RGGB_START	RGGB mode register	10-78
0x20020	ISPFE_CHANNEL_SELECT	Module video test gen and raw FE input data channel selection register	10-78
0x20024	ISPFE_DELAY_LINE_MEMORY	Module DNR line delay register	10-80
0x20028	ISPFE_FLUSH_HBLANK	Line blanking timing configuration register	10-80
0x2002C	ISPFE_FS_CHANNEL_SELECT	WDR input data channel selection register	10-81
0x20030	ISPFE_CONFIG_BUFFER_MODE	Configuration update mode register	10-82
0x20040	ISPFE_MODULE_BYPASS	ISP FE module bypass register	10-82
0x20044	ISPFE_BYPASS_MODE	ISP FE bypass mode selection register	10-84
0x20048	ISPFE_AE_SWITCH	AE statistics position control register	10-85

Offset Address	Register	Description	Page
0x2004C	ISPFE_AWB_SWITCH	RGB field AWB statistics module position control register	10-86
0x20050	ISPFE_HISTOGRAM_SWITCH	AE global histogram position control register	10-86
0x20058	ISPFE_HISTOGRAM_PE_SWITCH	Per exposure AE global histogram control register	10-87
0x20078	ISPFE_GLOBAL_FSM_RESET	State machine reset register	10-88
0x2007C	ISPFE_FIELD_STATUS	Field signal status register	10-88
0x20080	ISPFE_INTERRUPT01	Interrupt source 0/1 selection register	10-89
0x20084	ISPFE_INTERRUPT23	Interrupt source 2/3 selection register	10-89
0x20088	ISPFE_INTERRUPT45	Interrupt source 4/5 selection register	10-89
0x2008C	ISPFE_INTERRUPT67	Interrupt source 6/7 selection register	10-90
0x20090	ISPFE_INTERRUPT89	Interrupt source 8/9 selection register	10-90
0x20094	ISPFE_INTERRUPT1011	Interrupt source 10/11 selection register	10-91
0x20098	ISPFE_INTERRUPT1213	Interrupt source 12/13 selection register	10-91
0x2009C	ISPFE_INTERRUPT1415	Interrupt source 14/15 selection register	10-92
0x200A0	ISPFE_INTERRUPT_STATUS	Interrupt status register	10-92
0x200A4	ISPFE_INTERRUPT_CLEAR	Interrupt clear register	10-93
0x200C0	SENSOR_OFFSET_WDR_1_BLACK00	WDR_1 BLC R component black level register	10-93
0x200C4	SENSOR_OFFSET_WDR_1_BLACK01	WDR_1 BLC Gr component black level register	10-94
0x200C8	SENSOR_OFFSET_WDR_1_BLACK10	WDR_1 BLC Gb component black level register	10-94
0x200CC	SENSOR_OFFSET_WDR_1_BLACK11	WDR_1 BLC B component black level register	10-94

Offset Address	Register	Description	Page
0x200D0	SENSOR_OFFSET_WDR_2_BLACK00	WDR_2 BLC R component black level register	10-95
0x200D4	SENSOR_OFFSET_WDR_2_BLACK01	WDR_2 BLC Gr component black level register	10-95
0x200D8	SENSOR_OFFSET_WDR_2_BLACK10	WDR_2 BLC Gb component black level register	10-96
0x200DC	SENSOR_OFFSET_WDR_2_BLACK11	WDR_2 BLC B component black level register	10-96
0x200E0	SENSOR_OFFSET_WDR_3_BLACK00	WDR_3 BLC R component black level register	10-96
0x200E4	SENSOR_OFFSET_WDR_3_BLACK01	WDR_3 BLC Gr component black level register	10-97
0x200E8	SENSOR_OFFSET_WDR_3_BLACK10	WDR_3 BLC Gb component black level register	10-97
0x200EC	SENSOR_OFFSET_WDR_3_BLACK11	WDR_3 BLC B component black level register	10-97
0x200F0	SENSOR_OFFSET_WDR_4_BLACK00	WDR_4 BLC R component black level register	10-98
0x200F4	SENSOR_OFFSET_WDR_4_BLACK01	WDR_4 BLC Gr component black level register	10-98
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0x207F4	STATISTICS_PLANE_COUNTED_PE_1	PE plane pixel cumulative sum register 1	10-217
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0x20830	STATISTICS_COUNT_MIN	Bayer field AWB sum statistics pixel quantity register for pixels below the luminance lower limit	10-222
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0x21600−0x2167C	NOISE_PROFILE_RAW_FRONTEND_LUT_2	RAW_FRONTEND noise distribution table 2 register	10-237
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0x21700−0x2177C	NOISE_PROFILE_RAW_FRONTEND_LUT_4	RAW_FRONTEND noise distribution table 4 register	10-238
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0x24800−0x24880	GAMMA_BE0_MEM0	GAMMA_BE0 bank0 lookup table register	10-243
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Offset Address	Register	Description	Page
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0x37800−0x37C00	GAMMA_RGB_MEM1	GAMMA_RGB bank 1 lookup table register	10-248
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0x38800−0x38A00	DRC_REV_MEM	DRC_REV table register	10-249
0x39000−0x393FC	CMD_QUEUES	CMD table register	10-249
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0x400F8	ISP_BE_INT_MASK	ISP interrupt mask register	10-252
0x401E0	ISP_BE_CTRL_F	ISP general update control register	10-253
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0x4086C	ISP_CROP_Y_SIZE	Y component crop size configuration register	10-257
0x40870	ISP_CROP_C_CFG	C component crop enable register	10-258
0x40878	ISP_CROP_C_START	C component crop start position register	10-258
0x4087C	ISP_CROP_C_SIZE	C component crop size configuration register	10-259
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0x41814	ISP_HCDS_SIZE	Horizontal chrominance down sampling input size configuration register	10-266
0x4182C	ISP_MIDF_SIZE	Median filtering input chrominance picture size register	10-267
0x41844	ISP_MCDS_PARA	NR blending ratio and shift register	10-268
0x418F0	ISP_MCDS_SIZE	MCDS input picture size register	10-268
0x45200	ISP_SHARPEN_CFG	Sharpening control register	10-269
0x45210	ISP_SHARPEN_AMT	Sharpening strength register	10-269
0x4521C	ISP_SHARPEN_SHOOTAMT	Sharpening shoot AMT control register	10-270
0x45224	ISP_SHARPEN_EDGEJAG	Jag high-frequency parameter register	10-270
0x45228	ISP_SHARPEN_OSHTJAG	Jag overshoot parameter register	10-270
0x4522C	ISP_SHARPEN_USHTJAG	Jag undershoot parameter register	10-271
0x45230	ISP_SHARPEN_MID0	Sharpening IF filtering coefficient register	10-271
0x45234	ISP_SHARPEN_MID1	Sharpening IF filtering coefficient register	10-272

Offset Address	Register	Description	Page
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0x4523C	ISP_SHARPEN_LINETHD	Sharpening line detection threshold register	10-273
0x45240	ISP_SHARPEN_THD2	Sharpening threshold register 2	10-273
0x45244	ISP_SHARPEN_CTRL	Sharpening control register	10-274
0x45248	ISP_SHARPEN_LUMATH	Luma threshold parameter register	10-275
0x4524C	ISP_SHARPEN_LUMAWGT	Luma weight parameter register	10-275
0x45258	ISP_SHARPEN_OSHTVARTH	Variance threshold parameter register 0	10-276
0x4525C	ISP_SHARPEN_OSHTVAR	Overshoot variance parameter register 0	10-276
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0x45264	ISP_SHARPEN_USHTVAR	Overshoot variance parameter register 1	10-277
0x45268	ISP_SHARPEN_OSHTLUMA	Overshoot luminance parameter register 0	10-277
0x4526C	ISP_SHARPEN_USHTLUMA	Overshoot luminance parameter register 1	10-278
0x45274	ISP_SHARPEN_SHIFT	Shift parameter register	10-278
0x452F0	ISP_SHARPEN_SIZE	Sharpening picture size register	10-279
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0x46214	ISP_DEHAZE_BLK_SIZE	Dehaze block size configuration register	10-280
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0x46228	ISP_DEHAZE_STAT_MODE	Dehaze statistics module control register	10-283
0x4622C	ISP_DEHAZE_NEG_MODE	Dehaze inversion control register	10-283
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0x46234	ISP_DEHAZE_THLD	Dehaze T threshold coefficient configuration register	10-284
0x46238	ISP_DEHAZE_GSTRTH	Dehaze global strength coefficient register	10-285
0x4623C	ISP_DEHAZE_BLTHLD	Dehaze minimum value filtering threshold coefficient configuration register	10-285
0x46240	ISP_DEHAZE_STR_LUT_UPDATE	Dehaze strength table update register	10-286
0x46280	ISP_DEHAZE_MINSTAT_WADDR	Dehaze minimum value statistics write address register	10-286
0x46284	ISP_DEHAZE_MINSTAT_WDATA	Dehaze minimum value statistics write data register	10-286
0x46288	ISP_DEHAZE_MINSTAT_RADDR	Dehaze minimum value statistics read address register	10-287
0x4628C	ISP_DEHAZE_MINSTAT_RDATA	Dehaze minimum value statistics read data register	10-287
0x46290	ISP_DEHAZE_MAXSTAT_WADDR	Dehaze maximum value statistics write address register	10-288
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0x46298	ISP_DEHAZE_MAXSTAT_RADDR	Dehaze maximum value statistics read address register	10-289
0x4629C	ISP_DEHAZE_MAXSTAT_RDATA	Dehaze maximum value statistics read data register	10-289

Offset Address	Register	Description	Page
0x462A0	ISP_DEHAZE_PRESTAT_WADDR	Dehaze previous frame minimum value statistics write address register	10-290
0x462A4	ISP_DEHAZE_PRESTAT_WDATA	Dehaze previous frame minimum value statistics write data register	10-290
0x462A8	ISP_DEHAZE_PRESTAT_RADDR	Dehaze previous frame minimum value statistics read address register	10-291
0x462AC	ISP_DEHAZE_PRESTAT_RDATA	Dehaze previous frame minimum value statistics read data register	10-291
0x462B0	ISP_DEHAZE_LUT_WADDR	Dehaze strength LUT information write address register	10-292
0x462B4	ISP_DEHAZE_LUT_WDATA	Dehaze strength LUT information write data register	10-292
0x462B8	ISP_DEHAZE_LUT_RADDR	Dehaze strength LUT information read address register	10-293
0x462BC	ISP_DEHAZE_LUT_RDATA	Dehaze strength LUT information read data register	10-293
0x462F0	ISP_DEHAZE_SIZE	Dehaze picture size register	10-294
0x51400	ISP_ACM_CTRL	ACM control register	10-294
0x51404	ISP_ACM_ADJ	ACM processed pixel change register	10-295
0x51410	ISP_ACM_SIZE	ACM processed picture size register	10-296
0x51414	ISP_ACM_PARA_ADDR	ACM coefficient configuration loading address register	10-296
0x51420	ISP_ACM_PARA_UP	ACM coefficient configuration update register	10-297
0x51C00	ISP_VPDCICTRL	DCI control register	10-297
0x51C04	ISP_VPDCIHPOS	DCI algorithm horizontal adjustment region register	10-299
0x51C08	ISP_VPDCIVPOS	DCI algorithm vertical adjustment region register	10-299
0x51C0C	ISP_VPDCIHISBLD	DCI histogram statistics weighted coefficient register	10-300

Offset Address	Register	Description	Page
0x51C10	ISP_VPDCIHISOFT	DCI histogram statistics offset register	10-300
0x51C14	ISP_VPDCIHISCOR	DCI histogram coring register	10-301
0x51C18	ISP_VPDCIMERBLD	DCI adjustment unit blend value register	10-301
0x51C1C	ISP_VPDCIADJWGT	DCI manually configured curve weight register	10-302
0x51C20	ISP_VPDCICLIP0	DCI curve 0 weight range register	10-302
0x51C24	ISP_VPDCICLIP1	DCI curve 1 weight range register	10-302
0x51C28	ISP_VPDCICLIP2	DCI curve 2 weight range register	10-303
0x51C2C	ISP_VPDCIGLBGAIN	DCI luminance adjustment unit global gain register	10-303
0x51C30	ISP_VPDCIPOSTHR0	DCI adjustment unit threshold register 0 during positive adjustment	10-304
0x51C34	ISP_VPDCIPOSTHR1	DCI adjustment unit threshold register 1 during positive adjustment	10-304
0x51C38	ISP_VPDCIPOSGAIN0	DCI adjustment unit gain register 0 during positive adjustment	10-305
0x51C3C	ISP_VPDCIPOSGAIN1	DCI adjustment unit gain register 1 during positive adjustment	10-305
0x51C40	ISP_VPDCIPOSSLP0	DCI adjustment unit slope register 0 during positive adjustment	10-306
0x51C44	ISP_VPDCIPOSSLP1	DCI adjustment unit slope register 1 during positive adjustment	10-306
0x51C48	ISP_VPDCIPOSSLP2	DCI adjustment unit slope register 2 during positive adjustment	10-307
0x51C4C	ISP_VPDCINEGTHR0	DCI adjustment unit threshold register 0 during negative adjustment	10-307

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0x51C50	ISP_VPDCINEGTHR1	DCI adjustment unit threshold register 1 during negative adjustment	10-308
0x51C54	ISP_VPDCINEGGAIN0	DCI adjustment unit gain register 0 during negative adjustment	10-308
0x51C58	ISP_VPDCINEGGAIN1	DCI adjustment unit gain register 1 during negative adjustment	10-309
0x51C5C	ISP_VPDCINEGSLP0	DCI adjustment unit slope register 0 during negative adjustment	10-310
0x51C60	ISP_VPDCINEGSLP1	DCI adjustment unit slope register 1 during negative adjustment	10-310
0x51C64	ISP_VPDCINEGSLP2	DCI adjustment unit slope register 2 during negative adjustment	10-311
0x60000	ISPFE_MAX_ADDR	ISP buffer maximum address register	10-311
0x60004	ISPFE_MAX_ADDR2	ISP buffer maximum address register 2	10-311
0x60008	ISPFE_MAX_ADDR_SINTER1	ISP sinter buffer 1 maximum address register	10-312
0x6000C	ISPFE_MAX_ADDR_SINTER2	ISP sinter buffer 2 maximum address register	10-312
0x60010	ISPFE_TIMING	ISP timing configuration register	10-313
0x60014	ISPFE_MAX_ADDR3	ISP buffer maximum address register 3	10-313
0x60018	ISPFE_MAX_ADDR4	ISP buffer maximum address register 4	10-313
0x60020	ISPFE_BYTE_EN	ISP byte enable register	10-314
0x60028	ISPFE_CH_SWITCH	ISP input switch register	10-314
0x6002C	ISPFE_FE_BYPASS_CFG	ISP FE bypass register	10-316
0x60030	ISPFE_CROP_CFG	Crop enable register	10-317
0x60034	ISPFE_CROP_WIN	Crop window register	10-318
0x60038	ISPFE_CROP0_START	Crop start position register for region 0	10-318

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0x6003C	ISPFE_CROP0_SIZE	Crop size configuration register for region 0	10-318
0x600F0	ISPFE_INT	ISP interrupt indicator register	10-319
0x600F8	ISPFE_INT_MASK	ISP interrupt mask register	10-321
0x62400	ISP_DIS_CFG	DIS enable register	10-323
0x62404	ISP_DIS_BLK	Block configuration register	10-323
0x62410	ISP_DIS_V0POS	Vertical PRJ0 block address register	10-324
0x62414	ISP_DIS_V4POS	Vertical PRJ4 block address register	10-325
0x62418	ISP_DIS_V8POS	Vertical PRJ8 block address register	10-325
0x62420	ISP_DIS_V0POSE	Vertical PRJ0 block address register	10-326
0x62424	ISP_DIS_V4POSE	Vertical PRJ4 block address register	10-326
0x62428	ISP_DIS_V8POSE	Vertical PRJ8 block address register	10-327
0x62430	ISP_DIS_H0POS	Horizontal PRJ0 block address register	10-327
0x62434	ISP_DIS_H4POS	Horizontal PRJ4 block address register	10-328
0x62438	ISP_DIS_H8POS	Horizontal PRJ8 block address register	10-328
0x62440	ISP_DIS_H0POSE	Horizontal PRJ0 block address register	10-329
0x62444	ISP_DIS_H4POSE	Horizontal PRJ4 block address register	10-329
0x62448	ISP_DIS_H8POSE	Horizontal PRJ8 block address register	10-330
0x62450	ISP_DIS_RAW_LUMA	Data type register	10-330
0x62454	ISP_DIS_GAMMA_EN	Gamma enable register	10-330
0x62488	ISP_DIS_H_STAT_RADDR	Horizontal statistics read address register	10-331
0x6248C	ISP_DIS_H_STAT_RDATA	Horizontal statistics read data register	10-331

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0x62498	ISP_DIS_V_STAT_RADDR	Vertical statistics read address register	10-332
0x6249C	ISP_DIS_V_STAT_RDATA	Vertical statistics read data register	10-332
0x624E0	ISP_DIS_CTRL_F	DIS general control register	10-333
0x624E4	ISP_DIS_CTRL_I	DIS immediate update register	10-333
0x624EC	ISP_DIS_UPDATE	DIS register update register	10-334
0x63a00	ISP_FPN_CFG	FPN configuration register	10-334
0x63a04	ISP_FPN_CALIB_START	FPN calibration start signal register	10-335
0x63a08	ISP_FPN_CORR_CFG	FPN correction configuration register	10-335
0x63a0C	ISP_FPN_STAT	FPN calibration status register	10-336
0x63a10	ISP_FPN_WHITE_LEVEL	FPN calibration white point configuration register	10-336
0x63a18	ISP_FPN_DIVCOEF	FPN calibration division coefficient register	10-337
0x63a1C	ISP_FPN_FRAMELOG2	FPN calibrated frame quantity register	10-337
0x63a20	ISP_FPN_SUM0	FPN calibration cumulative sum lower-bit register	10-338
0x63a24	ISP_FPN_SUM1	FPN calibration cumulative sum upper-bit register	10-338
0x63a30	ISP_FPN_CORR0	FPN correction configuration register 0	10-339
0x63a34	ISP_FPN_CORR1	FPN correction configuration register 1	10-339
0x63a38	ISP_FPN_CORR2	FPN correction configuration register 2	10-340
0x63a3C	ISP_FPN_CORR3	FPN correction configuration register 3	10-340
0x63a40	ISP_FPN_SHIFT	FPN shift configuration register	10-340
0x63a50	ISP_FPN_MAX_O	FPN maximum output value register	10-341
0x63a54	ISP_FPN_OVERFLOWTHR	FPN correction threshold register	10-341

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0x63a80	ISP_FPN_LINE_WADDR	FPN line mode black line write address register	10-342
0x63a84	ISP_FPN_LINE_WDATA	FPN line mode black line write data register	10-342
0x63a88	ISP_FPN_LINE_RADDR	FPN line mode black line read address register	10-342
0x63a8C	ISP_FPN_LINE_RDATA	FPN line mode black line read data register	10-343
0x63aE0	ISP_FPN_CTRL_F	FPN general control register	10-343
0x63aE4	ISP_FPN_CTRL_I	FPN immediate update control register	10-344
0x63aE8	ISP_FPN_TIMING	FPN output timing configuration register	10-344
0x63aEC	ISP_FPN_UPDATE	FPN register update register	10-345
0x63aF0	ISP_FPN_SIZE	FPN picture size register	10-345

10.6 Register Description

ISP_AF_CFG

ISP_AF_CFG is an AF control register.

Offset Address	Register Name	Total Reset Value
0x22200	ISP_AF_CFG	0x0000_01DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ck_gt_en	reserved						fir1_ldg_en	fir0_ldg_en	iir1_ldg_en	iir0_ldg_en	fir1_lpf_en	fir0_lpf_en	iir1_ds_en	iir0_ds_en	bayer_mode	raw_mode	sqrt_en	mean_en	lpf_en	crop_en	offset_en	squ_mode	peak_mode	iir1_en2	iir1_en1	iir1_en0	iir0_en2	iir0_en1	iir0_en0	en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31]	RW	ck_gt_en	AF clock gating enable 0: disabled 1: enabled
[30:25]	RO	reserved	Reserved

[24]	RW	fir1_ldg_en	Vertical FIR filter luma dependent gain (LDG) enable 1 0: disabled 1: enabled
[23]	RW	fir0_ldg_en	Vertical FIR filter LDG enable 0 0: disabled 1: enabled
[22]	RW	iir1_ldg_en	Horizontal IIR filter LDG enable 1 0: disabled 1: enabled
[21]	RW	iir0_ldg_en	Horizontal IIR filter LDG enable 0 0: disabled 1: enabled
[20]	RW	fir1_lpf_en	Vertical FIR low-pass filter (LPF) enable 1 0: disabled 1: enabled
[19]	RW	fir0_lpf_en	Vertical FIR LPF enable 0 0: disabled 1: enabled
[18]	RW	iir1_ds_en	Horizontal IIR filter down sampling (DS) enable 1 0: disabled 1: enabled
[17]	RW	iir0_ds_en	Horizontal IIR filter DS enable 0 0: disabled 1: enabled
[16:15]	RW	bayer_mode	AF raw format 00: RGGB 01: GRBG 10: GBRG 11: BGGR
[14]	RW	raw_mode	AF data format 0: YUV data 1: raw data
[13]	RW	sqrt_en	AF gamma enable 0: disabled 1: enabled
[12]	RW	mean_en	AF median filtering enable 0: disabled 1: enabled

[11]	RW	lpf_en	AF low-pass filter enable 0: disabled 1: enabled
[10]	RW	crop_en	AF crop enable 0: disabled 1: enabled
[9]	RW	offset_en	offset enable 0: disabled 1: enabled
[8]	RW	squ_mode	Square mode of AF statistics 0: Statistics are directly accumulated. 1: Statistics are accumulated after the square operation.
[7]	RW	peak_mode	Peak value mode of AF statistics 0: All values of a block are selected for statistics. 1: The maximum value in each line of a block is selected for statistics.
[6]	RW	iir1_en2	Enable for IIR2 among the three cascaded IIRs in group 2 0: disabled 1: enabled
[5]	RW	iir1_en1	Enable for IIR1 among the three cascaded IIRs in group 2 0: disabled 1: enabled
[4]	RW	iir1_en0	Enable for IIR0 among the three cascaded IIRs in group 2 0: disabled 1: enabled
[3]	RW	iir0_en2	Enable for IIR2 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[2]	RW	iir0_en1	Enable for IIR1 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[1]	RW	iir0_en0	Enable for IIR0 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[0]	RW	en	AF enable 0: disabled 1: enabled

ISP_AF_ZONE

ISP_AF_ZONE is an AF block configuration register.

Offset Address	Register Name	Total Reset Value
0x12010	ISP_AF_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	vnum	Number of vertical AF blocks (15 blocks at most) Blocks are in the CH_AF_CROP_SIZE region when crop_en is 1. Blocks are in the CH_AF_SIZE region when crop_en is 0.
[7:5]	RO	reserved	Reserved
[4:0]	RW	hnum	Number of horizontal AF blocks (17 blocks at most) Blocks are in the CH_AF_CROP_SIZE region when crop_en is 1. Blocks are in the CH_AF_SIZE region when crop_en is 0.

ISP_AF_CROP_START

ISP_AF_CROP_START is an AF picture crop start coordinate register.

Offset Address	Register Name	Total Reset Value
0x12014	ISP_AF_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				pos_y												reserved				pos_x											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	pos_y	Vertical coordinate of the crop start point
[15:13]	RO	reserved	Reserved
[12:0]	RW	pos_x	Horizontal coordinate of the crop start point

ISP_AF_CROP_SIZE

ISP_AF_CROP_SIZE is an AF picture crop size register.

Offset Address	Register Name	Total Reset Value
0x12018	ISP_AF_CROP_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	vsize	Picture height after AF cropping NOTE The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	hsize	Picture width after AF cropping NOTE The configured value is the actual value minus 1.

ISP_AF_MEAN_THRES

ISP_AF_MEAN_THRES is an AF median filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x1201C	ISP_AF_MEAN_THRES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mean_thres															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	mean_thres	Threshold for AF median filtering

ISP_AF_IIRG0

ISP_AF_IIRG0 is AF IIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12020	ISP_AF_IIRG0	0x00A1_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg0_1								reserved								iirg0_0							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	iirg0_1	g0 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:8]	RO	reserved	Reserved
[7:0]	RW	iirg0_0	g0 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG1

ISP_AF_IIRG1 is AF IIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12024	ISP_AF_IIRG1	0x0244_01BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg1_1								reserved								iirg1_0							
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg1_1	g1 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved

[9:0]	RW	iirg1_0	g1 gain of AF IIR filtering group 0 **NOTE** The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG2

ISP_AF_IIRG2 is AF IIR filtering parameter register 2.

Offset Address	Register Name	Total Reset Value
0x12028	ISP_AF_IIRG2	0x0328_0328

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg2_1								reserved								iirg2_0							
Reset	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg2_1	g2 gain of AF IIR filtering group 1 **NOTE** The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg2_0	g2 gain of AF IIR filtering group 0 **NOTE** The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG3

ISP_AF_IIRG3 is AF IIR filtering parameter register 3.

Offset Address	Register Name	Total Reset Value
0x1202C	ISP_AF_IIRG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg3_1								reserved								iirg3_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved

[25:16]	RW	iirg3_1	g3 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg3_0	g3 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG4

ISP_AF_IIRG4 is AF IIR filtering parameter register 4.

Offset Address	Register Name	Total Reset Value
0x12030	ISP_AF_IIRG4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg4_1								reserved								iirg4_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg4_1	g4 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg4_0	g4 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG5

ISP_AF_IIRG5 is AF IIR filtering parameter register 5.

Offset Address	Register Name	Total Reset Value
0x12034	ISP_AF_IIRG5	0x0284_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg5_1								reserved								iirg5_0							
Reset	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg5_1	g5 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg5_0	g5 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG6

ISP_AF_IIRG6 is AF IIR filtering parameter register 6.

Offset Address	Register Name	Total Reset Value
0x12038	ISP_AF_IIRG6	0x033C_033C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg6_1								reserved								iirg6_0							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg6_1	g6 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg6_0	g6 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRPL

ISP_AF_IIRPL is an AF IIR filter preset register.

Offset Address	Register Name	Total Reset Value
0x1203C	ISP_AF_IIRPL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					iirpls_1			iirplg_1								reserved					iirpls_0			iirplg_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:24]	RW	iirpls_1	Preset shift for AF IIR filter group 1
[23:16]	RW	iirplg_1	Preset gain for AF IIR filter group 1
[15:11]	RO	reserved	Reserved
[10:8]	RW	iirpls_0	Preset shift for AF IIR filter group 0
[7:0]	RW	iirplg_0	Preset gain for AF IIR filter group 0

ISP_AF_SHIFT

ISP_AF_SHIFT is an AF IIR filtering shift parameter register.

Offset Address	Register Name	Total Reset Value
0x12040	ISP_AF_SHIFT	0x0027_1027

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	iirshift1_3			reserved	iirshift1_2			reserved	iirshift1_1			reserved	iirshift1_0			reserved	iirshift0_3			reserved	iirshift0_2			reserved	iirshift0_1			reserved	iirshift0_0		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	iirshift1_3	Shift adjustment for IIR2 in AF IIR filtering group 1
[27]	RO	reserved	Reserved

[26:24]	RW	iirshift1_2	Shift adjustment for IIR1 in AF IIR filtering group 1
[23]	RO	reserved	Reserved
[22:20]	RW	iirshift1_1	Shift adjustment for IIR0 in AF IIR filtering group 1
[19]	RO	reserved	Reserved
[18:16]	RW	iirshift1_0	Input shift adjustment for AF IIR filtering group 1 Note the following: iirg0_1 ≥ 128, iirshift0_0 ≥ 4 iirg0_1 ≥ 64, iirshift0_0 ≥ 3 iirg0_1 ≥ 32, iirshift0_0 ≥ 2 iirg0_1 ≥ 16, iirshift0_0 ≥ 1
[15]	RO	reserved	Reserved
[14:12]	RW	iirshift0_3	Shift adjustment for IIR2 in AF IIR filtering group 0
[11]	RO	reserved	Reserved
[10:8]	RW	iirshift0_2	Shift adjustment for IIR1 in AF IIR filtering group 0
[7]	RO	reserved	Reserved
[6:4]	RW	iirshift0_1	Shift adjustment for IIR0 in AF IIR filtering group 0
[3]	RO	reserved	Reserved
[2:0]	RW	iirshift0_0	Input shift adjustment for AF IIR filtering group 0 Note the following: iirg0_1 ≥ 128, iirshift0_0 ≥ 4 iirg0_1 ≥ 64, iirshift0_0 ≥ 3 iirg0_1 ≥ 32, iirshift0_0 ≥ 2 iirg0_1 ≥ 16, iirshift0_0 ≥ 1

ISP_AF_FIRH0

ISP_AF_FIRH0 is AF FIR filtering parameter register 0.

Offset Address	Register Name	Total Reset Value
0x12050	ISP_AF_FIRH0	0x0030_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh0_1				reserved												firh0_0			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved

[21:16]	RW	firh0_1	h0 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh0_0	h0 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH1

ISP_AF_FIRH1 is AF FIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12054	ISP_AF_FIRH1	0x0015_002B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh1_1				reserved												firh1_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh1_1	h1 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh1_0	h1 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH2

ISP_AF_FIRH2 is AF FIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12058	ISP_AF_FIRH2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			firh2_1	reserved			firh2_0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh2_1	h2 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh2_0	h2 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH3

ISP_AF_FIRH3 is AF FIR filtering parameter register 3.

Offset Address	Register Name	Total Reset Value
0x1205C	ISP_AF_FIRH3	0x002B_0015

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			firh3_1	reserved			firh3_0
Reset	0 0 0 0	0 0 0 0	0 0 1 0	1 0 1 1	0 0 0 0	0 0 0 0	0 0 0 1	0 1 0 1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh3_1	h3 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh3_0	h3 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH4

ISP_AF_FIRH4 is AF FIR filtering parameter register 4.

Offset Address	Register Name	Total Reset Value
0x12060	ISP_AF_FIRH4	0x0010_0010

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			firh4_1	reserved			firh4_0
Reset	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh4_1	h4 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh4_0	h4 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_ACC_SHIFT

ISP_AF_ACC_SHIFT is an AF cumulative statistics shift register.

Offset Address	Register Name	Total Reset Value
0x12078	ISP_AF_ACC_SHIFT	0x0002_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			acc_shift_y	acc_shift1_v	acc_shift0_v	acc_shift1_h	acc_shift0_h
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	acc_shift_y	Luminance Y statistics shift (0−15). Y in CH_AF_STAT_RDATA is shifted.
[15:12]	RW	acc_shift1_v	Shift of vertical FIR filtering statistics in group 1 (0−15). V2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	acc_shift0_v	Shift of vertical FIR filtering statistics in group 0 (0−15). V1 in CH_AF_STAT_RDATA is shifted.

[7:4]	RW	acc_shift1_h	Shift of horizontal IIR filtering statistics in group 1 (0−15). H2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	acc_shift0_h	Shift of horizontal IIR filtering statistics in group 0 (0−15). H1 in CH_AF_STAT_RDATA is shifted.

ISP_AF_CNT_SHIFT

ISP_AF_CNT_SHIFT is an AF count statistics shift register.

Offset Address	Register Name	Total Reset Value
0x1207C	ISP_AF_CNT_SHIFT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt_shift_y				cnt_shift1_v				cnt_shift0_v				cnt_shift1_h				cnt_shift0_h			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	cnt_shift_y	Luminance (Y) count value shift
[15:12]	RW	cnt_shift1_v	Shift of the vertical FIR filtering statistics in group 1 (0−15). vcnt2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	cnt_shift0_v	Shift of the vertical FIR filtering statistics in group 0 (0−15). vcnt1 in CH_AF_STAT_RDATA is shifted.
[7:4]	RW	cnt_shift1_h	Shift of the horizontal IIR filtering statistics in group 1 (0−15). hcnt2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	cnt_shift0_h	Shift of the horizontal IIR filtering statistics in group 0 (0−15). hcnt1 in CH_AF_STAT_RDATA is shifted.

ISP_AF_STAT_IND_RADDR

ISP_AF_STAT_IND_RADDR is a statistics indirect read address register for AF blocks.

Offset Address	Register Name	Total Reset Value
0x12088	ISP_AF_STAT_IND_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	af_stat_ind_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	af_stat_ind_raddr	Statistics indirect read address register for AF blocks

ISP_AF_STAT_IND_RDATA

ISP_AF_STAT_IND_RDATA is a statistics indirect read data register for AF blocks.

Offset Address	Register Name	Total Reset Value
0x1208C	ISP_AF_STAT_IND_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	af_stat_ind_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	af_stat_ind_rdata	Statistics indirect read data register for AF blocks V1, H1, V2, H2, Y, hcnt1, hcnt2, vcnt1, vcnt2, and ycnt information about each block is collected for statistics. The following is the information for each address: 0x01: {V1 (16 bits), H1 (16 bits)} of block 1 0x02: {V2 (16 bits), H2 (16 bits)} of block 1 0x03: {ycnt (16 bits), Y (16 bits)} of block 1 0x04: {vcnt2 (8 bits), vcnt1 (8 bits), hcnt2 (8 bits), cnt1(8bit)} of block 1 0x05: {V1 (16 bits), H1 (16 bits)} of block 2 … The same rule applies to other values. Note the following: V1 indicates the vertical FIR filtering statistics of group 1. V2 indicates the vertical FIR filtering statistics of group 2. H1 indicates the horizontal IIR filtering statistics of group 1. H2 indicates the horizontal IIR filtering statistics of group 2. Y indicates luminance statistics. vcnt1 indicates the number of times that the FIR filtering value is above the threshold. vcnt2 indicates the number of times that the FIR filtering value is above the threshold. hcnt1 indicates the number of times that the IIR filtering value is above the threshold. hcnt2 indicates the number of times that the IIR filtering value is above the threshold.

ISP_AF_CTRL_I

ISP_AF_CTRL_I is an immediate update control register.

Offset Address	Register Name	Total Reset Value
0x120E4	ISP_AF_CTRL_I	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	ISP update mode 0: update mode specified in ISP_AF_UPDATE 1: frame update mode

ISP_AF_UPDATE

ISP_AF_UPDATE is a configuration update register.

Offset Address	Register Name	Total Reset Value
0x120EC	ISP_AF_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update	ISP update. This bit is automatically cleared for each frame.

ISP_AF_SIZE

ISP_AF_SIZE is an AF picture size register.

Offset Address	Register Name	Total Reset Value
0x120F0	ISP_AF_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	vsize	Height of the AF input picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	hsize	Width of the AF input picture. The configured value is the actual value minus 1.

ISP_AF_IIRTHRE

ISP_AF_IIRTHRE is an AF IIR filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x12100	ISP_AF_IIRTHRE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	iir_thre1_h								iir_thre1_l								iir_thre0_h								iir_thre0_l							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	iir_thre1_h	Upper limit of the luma dependent threshold for AF IIR filter group 1
[23:16]	RW	iir_thre1_l	Lower limit of the luma dependent threshold for AF IIR filter group 1
[15:8]	RW	iir_thre0_h	Upper limit of the luma dependent threshold for AF IIR filter group 0
[7:0]	RW	iir_thre0_l	Lower limit of the luma dependent threshold for AF IIR filter group 0

ISP_AF_IIRGAIN

ISP_AF_IIRGAIN is an AF IIR filtering gain register.

Offset Address	Register Name	Total Reset Value
0x12104	ISP_AF_IIRGAIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	iir_gain1_h								iir_gain1_l								iir_gain0_h								iir_gain0_l							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	iir_gain1_h	Luma dependent high gain for AF IIR filter group 1
[23:16]	RW	iir_gain1_l	Luma dependent low gain for AF IIR filter group 1
[15:8]	RW	iir_gain0_h	Luma dependent high gain for AF IIR filter group 0
[7:0]	RW	iir_gain0_l	Luma dependent low gain for AF IIR filter group 0

ISP_AF_IIRSLOPE

ISP_AF_IIRSLOPE is an AF IIR filtering slope register.

Offset Address	Register Name	Total Reset Value
0x12108	ISP_AF_IIRSLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iir_slope1_h				iir_slope1_l				reserved								iir_slope0_h				iir_slope0_l			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	iir_slope1_h	Luma dependent high slope for AF IIR filter group 1
[19:16]	RW	iir_slope1_l	Luma dependent low slope for AF IIR filter group 1
[15:8]	RO	reserved	Reserved
[7:4]	RW	iir_slope0_h	Luma dependent high slope for AF IIR filter group 0
[3:0]	RW	iir_slope0_l	Luma dependent low slope for AF IIR filter group 0

ISP_AF_IIRDILATE

ISP_AF_IIRDILATE is an AF IIR filtering dilate register.

Offset Address	Register Name	Total Reset Value
0x1210C	ISP_AF_IIRDILATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					iir_dilate1	reserved	iir_dilate0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	iir_dilate1	Obtaining the maximum value among *n* surrounding pixels for calculating the IIR1 luma dependent gain 000: The maximum value among eight surrounding pixels is used. 001: The maximum value among 16 surrounding pixels is used. 010: The maximum value among 24 surrounding pixels is used. 011: The maximum value among 32 surrounding pixels is used. 100: The maximum value among 40 surrounding pixels is used. 101: The maximum value among 48 surrounding pixels is used. 110: The maximum value among 56 surrounding pixels is used. 111: The maximum value among 64 surrounding pixels is used.
[7:3]	RO	reserved	Reserved
[2:0]	RW	iir_dilate0	Obtaining the maximum value among *n* surrounding pixels for calculating the IIR0 luma dependent gain 000: The maximum value among eight surrounding pixels is used. 001: The maximum value among 16 surrounding pixels is used. 010: The maximum value among 24 surrounding pixels is used. 011: The maximum value among 32 surrounding pixels is used. 100: The maximum value among 40 surrounding pixels is used. 101: The maximum value among 48 surrounding pixels is used. 110: The maximum value among 56 surrounding pixels is used. 111: The maximum value among 64 surrounding pixels is used.

ISP_AF_FIRTHRE

ISP_AF_FIRTHRE is an AF FIR filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x12110	ISP_AF_FIRTHRE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_thre1_h		fir_thre1_l		fir_thre0_h		fir_thre0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	fir_thre1_h	Luma dependent high threshold for AF FIR filter group 1
[23:16]	RW	fir_thre1_l	Luma dependent low threshold for AF FIR filter group 1
[15:8]	RW	fir_thre0_h	Luma dependent high threshold for AF FIR filter group 0
[7:0]	RW	fir_thre0_l	Luma dependent low threshold for AF FIR filter group 0

ISP_AF_FIRGAIN

ISP_AF_FIRGAIN is an AF FIR filtering gain register.

Offset Address	Register Name	Total Reset Value
0x12114	ISP_AF_FIRGAIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_gain1_h		fir_gain1_l		fir_gain0_h		fir_gain0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	fir_gain1_h	Luma dependent high gain for AF FIR filter group 1
[23:16]	RW	fir_gain1_l	Luma dependent low gain for AF FIR filter group 1
[15:8]	RW	fir_gain0_h	Luma dependent high gain for AF FIR filter group 0
[7:0]	RW	fir_gain0_l	Luma dependent low gain for AF FIR filter group 0

ISP_AF_FIRSLOPE

ISP_AF_FIRSLOPE is an AF FIR filtering slope register.

Offset Address	Register Name	Total Reset Value
0x12118	ISP_AF_FIRSLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								fir_slope1_h				fir_slope1_l				reserved								fir_slope0_h				fir_slope0_l			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	fir_slope1_h	Luma dependent high slope for AF FIR filter group 1
[19:16]	RW	fir_slope1_l	Luma dependent low slope for AF FIR filter group 1
[15:8]	RO	reserved	Reserved
[7:4]	RW	fir_slope0_h	Luma dependent high slope for AF FIR filter group 0
[3:0]	RW	fir_slope0_l	Luma dependent low slope for AF FIR filter group 0

ISP_AF_IIRTHRE_CORING

ISP_AF_IIRTHRE_CORING is an AF IIR filter coring threshold register.

Offset Address	Register Name	Total Reset Value
0x12120	ISP_AF_IIRTHRE_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												iir_thre1_c								reserved								iir_thre0_c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	iir_thre1_c	Coring threshold of AF IIR filter group 1
[15:11]	RO	reserved	Reserved
[10:0]	RW	iir_thre0_c	Coring threshold of AF IIR filter group 0

ISP_AF_IIRPEAK_CORING

ISP_AF_IIRPEAK_CORING is an AF IIR filter coring peak register.

Offset Address	Register Name	Total Reset Value
0x12124	ISP_AF_IIRPEAK_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				iir_peak1_c												reserved				iir_peak0_c											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	iir_peak1_c	Coring peak of AF IIR filter group 1
[15:11]	RO	reserved	Reserved
[10:0]	RW	iir_peak0_c	Coring peak of AF IIR filter group 0

ISP_AF_IIRSLOPE_CORING

ISP_AF_IIRSLOPE_CORING is an AF IIR filter coring slope register.

Offset Address	Register Name	Total Reset Value
0x12128	ISP_AF_IIRSLOPE_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				iir_slope1_c				reserved				iir_slope0_c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	iir_slope1_c	Coring slope of AF IIR filter group 1
[7:4]	RO	reserved	Reserved
[3:0]	RW	iir_slope0_c	Coring slope of AF IIR filter group 0

ISP_AF_FIRTHRE_CORING

ISP_AF_FIRTHRE_CORING is an AF FIR filter coring threshold register.

Offset Address	Register Name	Total Reset Value
0x12130	ISP_AF_FIRTHRE_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fir_thre1_c												reserved				fir_thre0_c											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	fir_thre1_c	Coring threshold of AF FIR filter group 1
[15:11]	RO	reserved	Reserved
[10:0]	RW	fir_thre0_c	Coring threshold of AF FIR filter group 0

ISP_AF_FIRPEAK_CORING

ISP_AF_FIRPEAK_CORING is an AF FIR filter coring peak register.

Offset Address	Register Name	Total Reset Value
0x12134	ISP_AF_FIRPEAK_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fir_peak1_c												reserved				fir_peak0_c											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	fir_peak1_c	Coring peak of AF FIR filter group 1
[15:11]	RO	reserved	Reserved
[10:0]	RW	fir_peak0_c	Coring peak of AF FIR filter group 0

ISP_AF_FIRSLOPE_CORING

ISP_AF_FIRSLOPE_CORING is an AF FIR filter coring slope register.

Offset Address	Register Name	Total Reset Value
0x12138	ISP_AF_FIRSLOPE_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fir_slope1_c				reserved				fir_slope0_c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	fir_slope1_c	Coring slope of AF FIR filter group 1
[7:4]	RO	reserved	Reserved
[3:0]	RW	fir_slope0_c	Coring slope of AF FIR filter group 0

ISP_AF_HILIGHT

ISP_AF_HILIGHT is an AF highlight threshold register.

Offset Address	Register Name	Total Reset Value
0x12140	ISP_AF_HILIGHT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hilight							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hilight	AF luminance count threshold

ISP_AF_OFFSET

ISP_AF_OFFSET is an AF offset configuration register.

Offset Address	Register Name	Total Reset Value
0x12144	ISP_AF_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				offset_gb												reserved				offset_gr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:16]	RW	offset_gb	Offset of the Gb component
[15:14]	RO	reserved	Reserved
[13:0]	RW	offset_gr	Offset of the Gr component

ISPFE_ACTIVE_WIDTH

ISPFE_ACTIVE_WIDTH is a picture width register.

Offset Address	Register Name	Total Reset Value
0x20010	ISPFE_ACTIVE_WIDTH	0x0000_0780

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																active_width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	active_width	Active video width (unit: pixel)

ISPFE_ACTIVE_HEIGHT

ISPFE_ACTIVE_HEIGHT is a picture height register.

Offset Address	Register Name	Total Reset Value
0x20014	ISPFE_ACTIVE_HEIGHT	0x0000_0438

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																active_height															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	active_height	Active video height (unit: line)

ISPFE_RGGB_START

ISPFE_RGGB_START is an RGGB mode register.

Offset Address	Register Name	Total Reset Value
0x20018	ISPFE_RGGB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rggb_start	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	rggb_start	Initial colors of an RGGB picture 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISPFE_CHANNEL_SELECT

ISPFE_CHANNEL_SELECT is a module video test gen and raw FE input data channel selection register.

Offset Address	Register Name	Total Reset Value
0x20020	ISPFE_CHANNEL_SELECT	0x0000_00E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								channel4_select		channel3_select		channel2_select		channel1_select	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:6]	RW	channel4_select	Channel 4 input data select for the module video test gen and raw FE 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[5:4]	RW	channel3_select	Channel 3 input data select for the module video test gen and raw FE 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[3:2]	RW	channel2_select	Channel 2 input data select for the module video test gen and raw FE 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[1:0]	RW	channel1_select	Channel 1 input data select for the module video test gen and raw FE 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data

ISPFE_DELAY_LINE_MEMORY

ISPFE_DELAY_LINE_MEMORY is a module DNR line delay register.

Offset Address	Register Name	Total Reset Value
0x20024	ISPFE_DELAY_LINE_MEMORY	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														delay_line_memory_configuration	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	delay_line_memory_configuration	DNR memory line delay control 00: maximum number of lines; minimum line width 01: 3/4 maximum number of lines; 4/3 minimum line width 1X: 1/2 maximum number of lines; twice minimum line width

ISPFE_FLUSH_HBLANK

ISPFE_FLUSH_HBLANK is a line blanking timing configuration register.

Offset Address	Register Name	Total Reset Value
0x20028	ISPFE_FLUSH_HBLANK	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																flush_hblank															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	flush_hblank	Horizontal line blanking control for the replication line

ISPFE_FS_CHANNEL_SELECT

ISPFE_FS_CHANNEL_SELECT is a WDR input data channel selection register.

Offset Address	Register Name	Total Reset Value
0x2002C	ISPFE_FS_CHANNEL_SELECT	0x0000_00E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fs_channel4_select		fs_channel3_select		fs_channel2_select		fs_channel1_select	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:6]	RW	fs_channel4_select	Channel 4 input data select for the module frame stitch 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[5:4]	RW	fs_channel3_select	Channel 3 input data select for the module frame stitch 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[3:2]	RW	fs_channel2_select	Channel 2 input data select for the module frame stitch 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data
[1:0]	RW	fs_channel1_select	Channel 1 input data select for the module frame stitch 00: channel 1 data 01: channel 2 data 10: channel 3 data 11: channel 4 data

ISPFE_CONFIG_BUFFER_MODE

ISPFE_CONFIG_BUFFER_MODE is a configuration update mode register.

Offset Address	Register Name	Total Reset Value
0x20030	ISPFE_CONFIG_BUFFER_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														config_buffer_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	config_buffer_mode	ISP FE dual-buffer mode select configuration 00: The dual-buffer mode is disabled and the configuration is immediately updated. 01: The configuration update is forbidden, and the configuration is never updated. 10: The module configuration is updated in the vertical blanking of the corresponding module. 11: All module configurations are updated in the ISP FE global vertical blanking.

ISPFE_MODULE_BYPASS

ISPFE_MODULE_BYPASS is an ISP FE module bypass register.

Offset Address	Register Name	Total Reset Value
0x20040	ISPFE_MODULE_BYPASS	0x0000_4A00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			bypass_sensor_offset_wdr	bypass_sensor_offset	reserved					bypass_gamma_rgb	bypass_color_matrix	bypass_demosaic	bypass_drc	bypass_mesh_shading	bypass_radial_shading	bypass_white_balance	bypass_gamma_be_dl	bypass_gamma_be	bypass_dnr	bypass_fs_channel_switch	bypass_digital_gain	bypass_gamma_fe_dl	bypass_gamma_fe	bypass_frame_stitch	bypass_defect_pixel	bypass_raw_frontend	bypass_video_test_gen	bypass_channel_switch	bypass_input_formatter	position_digital_gain	position_gamma_fe
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28]	RW	bypass_sensor_offset_wdr	The sensor offset before the module raw front end is bypassed when this bit is set to 1.
[27]	RW	bypass_sensor_offset	The sensor offset before the module front-end lookup is bypassed when this bit is set to 1.
[26:22]	RO	reserved	Reserved
[21]	RW	bypass_gamma_rgb	The module RGB gamma LUT is bypassed when this bit is set to 1.
[20]	RW	bypass_color_matrix	The module color matrix is bypassed when this bit is set to 1.
[19]	RW	bypass_demosaic	The module demosaic (outputting the raw data) is bypassed when this bit is set to 1.
[18]	RW	bypass_drc	The module DRC is bypassed when this bit is set to 1.
[17]	RW	bypass_mesh_shading	The module mesh shading is bypassed when this bit is set to 1.
[16]	RW	bypass_radial_shading	The module radial shading is bypassed when this bit is set to 1.
[15]	RW	bypass_white_balance	The module static white balance is bypassed when this bit is set to 1.
[14]	RW	bypass_gamma_be_dl	The module back-end gamma block is bypassed when this bit is set to 1.
[13]	RW	bypass_gamma_be	The module back-end gamma LUTs are bypassed when this bit is set to 1.
[12]	RW	bypass_dnr	The module DNR is bypassed when this bit is set to 1.

[11]	RW	bypass_fs_channel_switch	The module frame stitch channel switch is bypassed when this bit is set to 1.
[10]	RW	bypass_digital_gain	The module digital gain is bypassed when this bit is set to 1.
[9]	RW	bypass_gamma_fe_dl	The module front-end gamma block is bypassed when this bit is set to 1.
[8]	RW	bypass_gamma_fe	The module front-end gamma LUTs are bypassed when this bit is set to 1.
[7]	RW	bypass_frame_stitch	The module frame stitching logic is bypassed when this bit is set to 1.
[6]	RW	bypass_defect_pixel	The module static defect pixels are bypassed when this bit is set to 1.
[5]	RW	bypass_raw_frontend	The module raw front end (green equalization and dynamic defect pixel) is bypassed when this bit is set to 1.
[4]	RW	bypass_video_test_gen	The module video test generator is bypassed when this bit is set to 1.
[3]	RW	bypass_channel_switch	The module channel switch is bypassed when this bit is set to 1.
[2]	RW	bypass_input_formatter	The module input formatter is bypassed when this bit is set to 1.
[1]	RW	position_digital_gain	Digital gain position select 0: after the module FE gamma LUTs 1: before the module FE gamma LUTs
[0]	RW	position_gamma_fe	Module gamma FE/digital gain position select 0: after the WDR stitching module 1: in the front part of ISP_FE

ISPFE_BYPASS_MODE

ISPFE_BYPASS_MODE is an ISP FE bypass mode selection register.

Offset Address	Register Name	Total Reset Value
0x20044	ISPFE_BYPASS_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						isp_raw_bypass		reserved								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	isp_raw_bypass	Switching between the normal mode and RGB/YUV422 input mode. In RGB/YUV422 input mode, data is directly inserted after the demosaic module, and the module cropping, scaling, gamma, as well as CSC are valid only for RGB inputs. 0: normal mode 1: The ISP raw processing module is bypassed.
[8:0]	RO	reserved	Reserved

ISPFE_AE_SWITCH

ISPFE_AE_SWITCH is an AE statistics position control register.

Offset Address	Register Name	Total Reset Value
0x20048	ISPFE_AE_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															ae_sum_switch	reserved															ae_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved

[17:16]	RW	ae_sum_switch	AE sum statistics position select 00: after the static white balance module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module
[15:2]	RO	reserved	Reserved
[1:0]	RW	ae_switch	AE statistics position select 00: after the static white balance module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module

ISPFE_AWB_SWITCH

ISPFE_AWB_SWITCH is an RGB field AWB statistics module position control register.

Offset Address	Register Name	Total Reset Value
0x2004C	ISPFE_AWB_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															awb_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	awb_switch	RGB field AWB statistics module position select 0: before the color matrix 1: after the color matrix

ISPFE_HISTOGRAM_SWITCH

ISPFE_HISTOGRAM_SWITCH is an AE global histogram position control register.

Offset Address	Register Name	Total Reset Value
0x20050	ISPFE_HISTOGRAM_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								histogram_switch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	histogram_switch	AE global histogram position select 00: in the same position as the AE module 01: after the video test gen (channel 1) module 10: after the shading module 11: after the WDR frame stitch module

ISPFE_HISTOGRAM_PE_SWITCH

ISPFE_HISTOGRAM_PE_SWITCH is a per exposure AE global histogram control register.

Offset Address	Register Name	Total Reset Value
0x20058	ISPFE_HISTOGRAM_PE_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								histogram_pe_switch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	histogram_pe_switch	Per exposure AE global histogram enable 0: enabled (channels 2−4 after the video test gen module) 1: disabled

ISPFE_GLOBAL_FSM_RESET

ISPFE_GLOBAL_FSM_RESET is a state machine reset register.

Offset Address	Register Name	Total Reset Value
0x20078	ISPFE_GLOBAL_FSM_RESET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								global_fsm_reset
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	global_fsm_reset	FSM synchronous reset signal

ISPFE_FIELD_STATUS

ISPFE_FIELD_STATUS is a field signal status register.

Offset Address	Register Name	Total Reset Value
0x2007C	ISPFE_FIELD_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								field_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RO	field_status	Field signal status

ISPFE_INTERRUPT01

ISPFE_INTERRUPT01 is an interrupt source 0/1 selection register.

Offset Address	Register Name	Total Reset Value
0x20080	ISPFE_INTERRUPT01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												interrupt1_source				reserved												interrupt0_source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt1_source	Interrupt source 1 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt0_source	Interrupt source 0 select

ISPFE_INTERRUPT23

ISPFE_INTERRUPT23 is an interrupt source 2/3 selection register.

Offset Address	Register Name	Total Reset Value
0x20084	ISPFE_INTERRUPT23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												interrupt3_source				reserved												interrupt2_source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt3_source	Interrupt source 3 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt2_source	Interrupt source 2 select

ISPFE_INTERRUPT45

ISPFE_INTERRUPT45 is an interrupt source 4/5 selection register.

Offset Address	Register Name	Total Reset Value
0x20088	ISPFE_INTERRUPT45	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		interrupt5_source		reserved		interrupt4_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt5_source	Interrupt source 5 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt4_source	Interrupt source 4 select

ISPFE_INTERRUPT67

ISPFE_INTERRUPT67 is an interrupt source 6/7 selection register.

Offset Address	Register Name	Total Reset Value
0x2008C	ISPFE_INTERRUPT67	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		interrupt7_source		reserved		interrupt6_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt7_source	Interrupt source 7 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt6_source	Interrupt source 6 select

ISPFE_INTERRUPT89

ISPFE_INTERRUPT89 is an interrupt source 8/9 selection register.

Offset Address	Register Name	Total Reset Value
0x20090	ISPFE_INTERRUPT89	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			interrupt9_source	reserved		interrupt8_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt9_source	Interrupt source 9 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt8_source	Interrupt source 8 select

ISPFE_INTERRUPT1011

ISPFE_INTERRUPT1011 is an interrupt source 10/11 selection register.

Offset Address	Register Name	Total Reset Value
0x20094	ISPFE_INTERRUPT1011	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			interrupt11_source	reserved		interrupt10_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt11_source	Interrupt source 11 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt10_source	Interrupt source 10 select

ISPFE_INTERRUPT1213

ISPFE_INTERRUPT1213 is an interrupt source 12/13 selection register.

Offset Address	Register Name	Total Reset Value
0x20098	ISPFE_INTERRUPT1213	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		interrupt13_source		reserved		interrupt12_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt13_source	Interrupt source 13 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt12_source	Interrupt source 12 select

ISPFE_INTERRUPT1415

ISPFE_INTERRUPT1415 is an interrupt source 14/15 selection register.

Offset Address	Register Name	Total Reset Value
0x2009C	ISPFE_INTERRUPT1415	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		interrupt15_source		reserved		interrupt14_source	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	interrupt15_source	Interrupt source 15 select
[15:6]	RO	reserved	Reserved
[5:0]	RW	interrupt14_source	Interrupt source 14 select

ISPFE_INTERRUPT_STATUS

ISPFE_INTERRUPT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x200A0	ISPFE_INTERRUPT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																interrupt_status															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	interrupt_status	Interrupt event flag

ISPFE_INTERRUPT_CLEAR

ISPFE_INTERRUPT_CLEAR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x200A4	ISPFE_INTERRUPT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																interrupt_clear															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	interrupt_clear	Interrupt event clear. Writing 0 and 1 in sequence to a bit clears the interrupt corresponding to this bit.

SENSOR_OFFSET_WDR_1_BLACK00

SENSOR_OFFSET_WDR_1_BLACK00 is a WDR_1 BLC R component black level register.

Offset Address	Register Name	Total Reset Value
0x200C0	SENSOR_OFFSET_WDR_1_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black00	Black level offset of color channel 00 (R)

SENSOR_OFFSET_WDR_1_BLACK01

SENSOR_OFFSET_WDR_1_BLACK01 is a WDR_1 BLC Gr component black level register.

Offset Address	Register Name	Total Reset Value
0x200C4	SENSOR_OFFSET_WDR_1_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black01	Black level offset of color channel 01 (Gr)

SENSOR_OFFSET_WDR_1_BLACK10

SENSOR_OFFSET_WDR_1_BLACK10 is a WDR_1 BLC Gb component black level register.

Offset Address	Register Name	Total Reset Value
0x200C8	SENSOR_OFFSET_WDR_1_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black10	Black level offset of color channel 10 (Gb)

SENSOR_OFFSET_WDR_1_BLACK11

SENSOR_OFFSET_WDR_1_BLACK11 is a WDR_1 BLC B component black level register.

Offset Address	Register Name	Total Reset Value
0x200CC	SENSOR_OFFSET_WDR_1_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black11	Black level offset of color channel 11 (B)

SENSOR_OFFSET_WDR_2_BLACK00

SENSOR_OFFSET_WDR_2_BLACK00 is a WDR_2 BLC R component black level register.

Offset Address	Register Name	Total Reset Value
0x200D0	SENSOR_OFFSET_WDR_2_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black00	Black level offset of color channel 00 (R)

SENSOR_OFFSET_WDR_2_BLACK01

SENSOR_OFFSET_WDR_2_BLACK01 is a WDR_2 BLC Gr component black level register.

Offset Address	Register Name	Total Reset Value
0x200D4	SENSOR_OFFSET_WDR_2_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black01	Black level offset of color channel 01 (Gr)

SENSOR_OFFSET_WDR_2_BLACK10

SENSOR_OFFSET_WDR_2_BLACK10 is a WDR_2 BLC Gb component black level register.

Offset Address	Register Name	Total Reset Value
0x200D8	SENSOR_OFFSET_WDR_2_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black10	Black level offset of color channel 10 (Gb)

SENSOR_OFFSET_WDR_2_BLACK11

SENSOR_OFFSET_WDR_2_BLACK11 is a WDR_2 BLC B component black level register.

Offset Address	Register Name	Total Reset Value
0x200DC	SENSOR_OFFSET_WDR_2_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black11	Black level offset of color channel 11 (B)

SENSOR_OFFSET_WDR_3_BLACK00

SENSOR_OFFSET_WDR_3_BLACK00 is a WDR_3 BLC R component black level register.

Offset Address	Register Name	Total Reset Value
0x200E0	SENSOR_OFFSET_WDR_3_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	black00	Black level offset of color channel 00 (R)

SENSOR_OFFSET_WDR_3_BLACK01

SENSOR_OFFSET_WDR_3_BLACK01 is a WDR_3 BLC Gr component black level register.

Offset Address	Register Name	Total Reset Value
0x200E4	SENSOR_OFFSET_WDR_3_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black01	Black level offset of color channel 01 (Gr)

SENSOR_OFFSET_WDR_3_BLACK10

SENSOR_OFFSET_WDR_3_BLACK10 is a WDR_3 BLC Gb component black level register.

Offset Address	Register Name	Total Reset Value
0x200E8	SENSOR_OFFSET_WDR_3_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black10	Black level offset of color channel 10 (Gb)

SENSOR_OFFSET_WDR_3_BLACK11

SENSOR_OFFSET_WDR_3_BLACK11 is a WDR_3 BLC B component black level register.

Offset Address	Register Name	Total Reset Value
0x200EC	SENSOR_OFFSET_WDR_3_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black11	Black level offset of color channel 11 (B)

SENSOR_OFFSET_WDR_4_BLACK00

SENSOR_OFFSET_WDR_4_BLACK00 is a WDR_4 BLC R component black level register.

Offset Address	Register Name	Total Reset Value
0x200F0	SENSOR_OFFSET_WDR_4_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black00	Black level offset of color channel 00 (R)

SENSOR_OFFSET_WDR_4_BLACK01

SENSOR_OFFSET_WDR_4_BLACK01 is a WDR_4 BLC Gr component black level register.

Offset Address	Register Name	Total Reset Value
0x200F4	SENSOR_OFFSET_WDR_4_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black01	Black level offset of color channel 01 (Gr)

SENSOR_OFFSET_WDR_4_BLACK10

SENSOR_OFFSET_WDR_4_BLACK10 is a WDR_4 BLC Gb component black level register.

Offset Address	Register Name	Total Reset Value
0x200F8	SENSOR_OFFSET_WDR_4_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black10	Black level offset of color channel 10 (Gb)

SENSOR_OFFSET_WDR_4_BLACK11

SENSOR_OFFSET_WDR_4_BLACK11 is a WDR_4 BLC B component black level register.

Offset Address	Register Name	Total Reset Value
0x200FC	SENSOR_OFFSET_WDR_4_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black11	Black level offset of color channel 11 (B)

INPUTPORT_HC_LIMIT

INPUTPORT_HC_LIMIT is an input port horizontal count limit configuration register.

Offset Address	Register Name	Total Reset Value
0x20108	INPUTPORT_HC_LIMIT	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hc_limit															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	hc_limit	Horizontal count limit value (for example, 0, 1, …, hc_limit – 1, hc_limit, 0, 1, …)

INPUTPORT_HC_START0

INPUTPORT_HC_START0 is input port horizontal start register 0.

Offset Address	Register Name	Total Reset Value
0x2010C	INPUTPORT_HC_START0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hcstart0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hcstart0	Start value of ACL gating signal window 0

INPUTPORT_HC_SIZE0

INPUTPORT_HC_SIZE0 is input port horizontal size register 0.

Offset Address	Register Name	Total Reset Value
0x20110	INPUTPORT_HC_SIZE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hcsize0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hcsize0	Size of ACL gating signal window 0

INPUTPORT_HC_START1

INPUTPORT_HC_START1 is input port horizontal start register 1.

Offset Address	Register Name	Total Reset Value
0x20114	INPUTPORT_HC_START1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hcstart1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hcstart1	Start value of HS gating signal window 1

INPUTPORT_HC_SIZE1

INPUTPORT_HC_SIZE1 is input port horizontal size register 1.

Offset Address	Register Name	Total Reset Value
0x20118	INPUTPORT_HC_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hcsize1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hcsize1	Size of HS gating signal window 1

INPUTPORT_VC_LIMIT

INPUTPORT_VC_LIMIT is an input port vertical count limit configuration register.

Offset Address	Register Name	Total Reset Value
0x2011C	INPUTPORT_VC_LIMIT	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vclimit															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vclimit	Vertical count limit value (for example, 0, 1, …, vclimit – 1, vclimit, 0, 1, …)

INPUTPORT_VC_START

INPUTPORT_VC_START is an input port vertical start register.

Offset Address	Register Name	Total Reset Value
0x20120	INPUTPORT_VC_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vcstart															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vcstart	Start value of ACL gating signal window 2

INPUTPORT_VC_SIZE

INPUTPORT_VC_SIZE is an input port vertical size register.

Offset Address	Register Name	Total Reset Value
0x20124	INPUTPORT_VC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vcsize															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vcsize	Size of ACL gating signal window 2

INPUTPORT_CTRL

INPUTPORT_CTRL is an input port control register.

Offset Address	Register Name	Total Reset Value
0x20130	INPUTPORT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								freezeconfig	reserved					moderequest	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	freezeconfig	Input port configuration freeze 0: normal operation 1: The previous configuration status is retained.
[6:3]	RO	reserved	Reserved
[2:0]	RW	moderequest	Input port start and stop 000: safe stop 001: safe start 010: emergency stop 011: emergency start 100: reserved 101: safer start 110: reserved 111: reserved

INPUTPORT_STATUS

INPUTPORT_STATUS is an input port status register.

Offset Address	Register Name	Total Reset Value
0x20134	INPUTPORT_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							modestatus
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RO	modestatus	Input port status monitoring Bit[0] 1: started 0: stopped Bit[2:1]: reserved

INPUT_FORMATTER_MODE

INPUT_FORMATTER_MODE is an input formatter mode control register.

Offset Address	Register Name	Total Reset Value
0x20140	INPUT_FORMATTER_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				input_bitwidth_select	reserved	mode_out	reserved	mode_in
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved

[17:16]	RW	input_bitwidth_select	Input data width select 00: 12 bits 01: 14 bits 10: 16 bits 11: 20 bits
[15:11]	RO	reserved	Reserved
[10:8]	RW	mode_out	Output mode select 000: 4-channel data inputs 001: 2-channel data linear mapping 010: 3-channel data linear mapping 011: 4-channel data linear mapping Other values: reserved
[7:5]	RO	reserved	Reserved
[4:0]	RW	mode_in	Input mode

INPUT_FORMATTER_FACTORML

INPUT_FORMATTER_FACTORML is an input formatter exposure ratio (long frame to medium frame) register.

Offset Address	Register Name	Total Reset Value
0x20144	INPUT_FORMATTER_FACTORML	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																factorml															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:0]	RW	factorml	Exposure ratio of the long frame to the medium frame, 6.12-bit fixed-point value

INPUT_FORMATTER_FACTORMS

INPUT_FORMATTER_FACTORMS is an input formatter exposure ratio (short frame to medium frame) register.

Offset Address	Register Name	Total Reset Value
0x20148	INPUT_FORMATTER_FACTORMS	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				factorms											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	factorms	Exposure ratio of the short frame to the medium frame, 1.12-bit fixed-point value

INPUT_FORMATTER_BLACKLEVEL

INPUT_FORMATTER_BLACKLEVEL is an input formatter sensor black level register.

Offset Address	Register Name	Total Reset Value
0x2014C	INPUT_FORMATTER_BLACKLEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				blacklevel											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	blacklevel	Sensor black level

INPUT_FORMATTER_KNEEPOINT01

INPUT_FORMATTER_KNEEPOINT01 is an input formatter knee point 0/1 register.

Offset Address	Register Name	Total Reset Value
0x20150	INPUT_FORMATTER_KNEEPOINT01	0x0580_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kneepoint1																kneepoint0															
Reset	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	kneepoint1	Knee point 1
[15:0]	RW	kneepoint0	Knee point 0

INPUT_FORMATTER_KNEEPOINT2

INPUT_FORMATTER_KNEEPOINT2 is an input formatter knee point 2 register.

Offset Address	Register Name	Total Reset Value
0x20154	INPUT_FORMATTER_KNEEPOINT2	0x0000_0881

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																kneepoint2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	kneepoint2	Knee point 2

INPUT_FORMATTER_SLOPESELECT

INPUT_FORMATTER_SLOPESELECT is an input formatter compression table slope selection register.

Offset Address	Register Name	Total Reset Value
0x20158	INPUT_FORMATTER_SLOPESELECT	0x0906_0402

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				slope3select				reserved				slope2select				reserved				slope1select				reserved				slope0select			
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	slope3select	Slope 3 of the compression table (4 bits)
[23:20]	RO	reserved	Reserved
[19:16]	RW	slope2select	Slope 2 of the compression table (4 bits)
[15:12]	RO	reserved	Reserved
[11:8]	RW	slope1select	Slope 1 of the compression table (4 bits)
[7:4]	RO	reserved	Reserved
[3:0]	RW	slope0select	Slope 0 of the compression table (4 bits)

VIDEO_TEST_GEN_CTRL

VIDEO_TEST_GEN_CTRL is a VIDEO_TEST_GEN control register.

Offset Address	Register Name	Total Reset Value
0x20160	VIDEO_TEST_GEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bayer_rgb_o_sel	bayer_rgb_i_sel	test_pattern_off_on
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	bayer_rgb_o_sel	Output format select 0: Bayer 1: RGB
[1]	RW	bayer_rgb_i_sel	Input format select 0: Bayer 1: RGB
[0]	RW	test_pattern_off_on	Test pattern enable 0: disabled 1: enabled

VIDEO_TEST_PATTREN_TYPE

VIDEO_TEST_PATTREN_TYPE is a VIDEO_TEST_GEN mode type selection register.

Offset Address	Register Name	Total Reset Value
0x20164	VIDEO_TEST_PATTREN_TYPE	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								patterntype							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:0]	RW	patterntype	Mode type select 0x00: pure color 0x01: horizontal gradient 0x02: vertical gradient 0x03: vertical stripe 0x04: rectangle Other values: white target on a black background

VIDEO_TEST_R_BACKGND

VIDEO_TEST_R_BACKGND is a VIDEO_TEST_GEN R component background value register.

Offset Address	Register Name	Total Reset Value
0x20168	VIDEO_TEST_R_BACKGND	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rbackgnd	16-bit MSB-aligned R component background value

VIDEO_TEST_G_BACKGND

VIDEO_TEST_G_BACKGND is a VIDEO_TEST_GEN G component background value register.

Offset Address	Register Name	Total Reset Value
0x2016C	VIDEO_TEST_G_BACKGND	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	gbackgnd	16-bit MSB-aligned G component background value

VIDEO_TEST_B_BACKGND

VIDEO_TEST_B_BACKGND is a VIDEO_TEST_GEN B component background value register.

Offset Address	Register Name	Total Reset Value
0x20170	VIDEO_TEST_B_BACKGND	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bbackgnd	16-bit MSB-aligned B component background value

VIDEO_TEST_R_FOREGND

VIDEO_TEST_R_FOREGND is a VIDEO_TEST_GEN R component foreground value register.

Offset Address	Register Name	Total Reset Value
0x20174	VIDEO_TEST_R_FOREGND	0x0000_8FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rforegnd	16-bit MSB-aligned R component foreground value

VIDEO_TEST_G_FOREGND

VIDEO_TEST_G_FOREGND is a VIDEO_TEST_GEN G component foreground value register.

Offset Address	Register Name	Total Reset Value
0x20178	VIDEO_TEST_G_FOREGND	0x0000_8FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	gforegnd	16-bit MSB-aligned G component foreground value

VIDEO_TEST_B_FOREGND

VIDEO_TEST_B_FOREGND is a VIDEO_TEST_GEN B component foreground value register.

Offset Address	Register Name	Total Reset Value
0x2017C	VIDEO_TEST_B_FOREGND	0x0000_8FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bforegnd	16-bit MSB-aligned B component foreground value

VIDEO_TEST_RGB_GRADIENT

VIDEO_TEST_RGB_GRADIENT is a VIDEO_TEST_GEN channel 1/2 RGB gradient increment register.

Offset Address	Register Name	Total Reset Value
0x20180	VIDEO_TEST_RGB_GRADIENT	0x3CAA_3CAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgbgradient2																rgbgradient															
Reset	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	rgbgradient2	RGB gradient increment of channel 2, 4.12-bit unsigned fixed-point number

[15:0]	RW	rgbgradient	Increment (0−15) of each pixel for the RGB gradient of channel 1, 4.12-bit unsigned fixed-point number

VIDEO_TEST_RGB_GRADIENT_START

VIDEO_TEST_RGB_GRADIENT_START is a VIDEO_TEST_GEN channel 3/4 RGB gradient increment register.

Offset Address	Register Name	Total Reset Value
0x20184	VIDEO_TEST_RGB_GRADIENT_START	0x3CAA_3CAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgbgradient4																rgbgradient3															
Reset	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	rgbgradient4	RGB gradient increment of channel 4, 4.12-bit unsigned fixed-point number
[15:0]	RW	rgbgradient3	RGB gradient increment of channel 3, 4.12-bit unsigned fixed-point number

VIDEO_TEST_RGB_GRADIENT_START12

VIDEO_TEST_RGB_GRADIENT_START12 is a VIDEO_TEST_GEN channel 1/2 RGB gradient start value register.

Offset Address	Register Name	Total Reset Value
0x20188	VIDEO_TEST_RGB_GRADIENT_START12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgb_gradient_start_2																rgb_gradient_start															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rgb_gradient_start_2	Start value of the RGB gradient for channel 2
[15:0]	RW	rgb_gradient_start	16-bit start value of the RGB gradient for channel 1, aligned with the MSB of the bit width

VIDEO_TEST_RGB_GRADIENT_START34

VIDEO_TEST_RGB_GRADIENT_START34 is a VIDEO_TEST_GEN channel 3/4 RGB gradient start value register.

Offset Address	Register Name	Total Reset Value
0x2018C	VIDEO_TEST_RGB_GRADIENT_START34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgb_gradient_start_4																rgb_gradient_start_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rgb_gradient_start_4	Start value of the RGB gradient for channel 4
[15:0]	RW	rgb_gradient_start_3	Start value of the RGB gradient for channel 3

VIDEO_TEST_RECT_TOP

VIDEO_TEST_RECT_TOP is a VIDEO_TEST_GEN line ID register for the top and bottom of the rectangle.

Offset Address	Register Name	Total Reset Value
0x20190	VIDEO_TEST_RECT_TOP	0x0100_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		rect_bot														reserved		rect_top													
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:16]	RW	rect_bot	ID of the line where the rectangle bottom is located
[15:14]	RO	reserved	Reserved
[13:0]	RW	rect_top	ID of the line where the rectangle top is located

VIDEO_TEST_RECT_LEFT

VIDEO_TEST_RECT_LEFT is a VIDEO_TEST_GEN pixel ID register for the left part of the rectangle.

Offset Address	Register Name	Total Reset Value
0x20194	VIDEO_TEST_RECT_LEFT	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rectleft											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	rectleft	ID of the pixel where the left part of the rectangle is located

VIDEO_TEST_RECT_RIGHT

VIDEO_TEST_RECT_RIGHT is a VIDEO_TEST_GEN pixel ID register for the right part of the rectangle.

Offset Address	Register Name	Total Reset Value
0x20198	VIDEO_TEST_RECT_RIGHT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rectright											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	rectright	ID of the pixel where the right part of the rectangle is located

SENSOR_OFFSET_BLACK00

SENSOR_OFFSET_BLACK00 is an R component black level register.

Offset Address	Register Name	Total Reset Value
0x201A0	SENSOR_OFFSET_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black00																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black00	Black level offset of color channel 00 (R)

SENSOR_OFFSET_BLACK01

SENSOR_OFFSET_BLACK01 is a Gr component black level register.

Offset Address	Register Name	Total Reset Value
0x201A4	SENSOR_OFFSET_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black01																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black01	Black level offset of color channel 01 (Gr)

SENSOR_OFFSET_BLACK10

SENSOR_OFFSET_BLACK10 is a Gb component black level register.

Offset Address	Register Name	Total Reset Value
0x201A8	SENSOR_OFFSET_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black10																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black10	Black level offset of color channel 10 (Gb)

SENSOR_OFFSET_BLACK11

SENSOR_OFFSET_BLACK11 is a B component black level register.

Offset Address	Register Name	Total Reset Value
0x201AC	SENSOR_OFFSET_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black11																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19:0]	RW	black11	Black level offset of color channel 11 (B)

NP_RAW_FRONTEND1_EXP_THRESH

NP_RAW_FRONTEND1_EXP_THRESH is an NP_RAW_FRONTEND1 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201B0	NP_RAW_FRONTEND1_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																expthresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	expthresh	Threshold of the long/short exposure data

NP_RAW_FRONTEND1_SHORT_RATIO

NP_RAW_FRONTEND1_SHORT_RATIO is an NP_RAW_FRONTEND1 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201B4	NP_RAW_FRONTEND1_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								shortratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	shortratio	Short exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND1_LONG_RATIO

NP_RAW_FRONTEND1_LONG_RATIO is an NP_RAW_FRONTEND1 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201B8	NP_RAW_FRONTEND1_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								longratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	longratio	Long exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND1_OFF

NP_RAW_FRONTEND1_OFF is an NP_RAW_FRONTEND1 noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x201BC	NP_RAW_FRONTEND1_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

NP_RAW_FRONTEND2_EXP_THRESH

NP_RAW_FRONTEND2_EXP_THRESH is an NP_RAW_FRONTEND2 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201C0	NP_RAW_FRONTEND2_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																expthresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	expthresh	Threshold of the long/short exposure data

NP_RAW_FRONTEND2_SHORT_RATIO

NP_RAW_FRONTEND2_SHORT_RATIO is an NP_RAW_FRONTEND2 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201C4	NP_RAW_FRONTEND2_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								shortratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	shortratio	Short exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND2_LONG_RATIO

NP_RAW_FRONTEND2_LONG_RATIO is an NP_RAW_FRONTEND2 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201C8	NP_RAW_FRONTEND2_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								longratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	longratio	Long exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND2_OFF

NP_RAW_FRONTEND2_OFF is an NP_RAW_FRONTEND2 noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x201CC	NP_RAW_FRONTEND2_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

NP_RAW_FRONTEND3_EXP_THRESH

NP_RAW_FRONTEND3_EXP_THRESH is an NP_RAW_FRONTEND3 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201D0	NP_RAW_FRONTEND3_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																expthresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	expthresh	Threshold of the long/short exposure data

NP_RAW_FRONTEND3_SHORT_RATIO

NP_RAW_FRONTEND3_SHORT_RATIO is an NP_RAW_FRONTEND3 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201D4	NP_RAW_FRONTEND3_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								shortratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	shortratio	Short exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND3_LONG_RATIO

NP_RAW_FRONTEND3_LONG_RATIO is an NP_RAW_FRONTEND3 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201D8	NP_RAW_FRONTEND3_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								longratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	longratio	Long exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND3_OFF

NP_RAW_FRONTEND3_OFF is an NP_RAW_FRONTEND3 noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x201DC	NP_RAW_FRONTEND3_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

NP_RAW_FRONTEND4_EXP_THRESH

NP_RAW_FRONTEND4_EXP_THRESH is an NP_RAW_FRONTEND4 noise threshold register.

Offset Address	Register Name	Total Reset Value
0x201E0	NP_RAW_FRONTEND4_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																exp_thresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	exp_thresh	Threshold of the long/short exposure data

NP_RAW_FRONTEND4_SHORT_RATIO

NP_RAW_FRONTEND4_SHORT_RATIO is an NP_RAW_FRONTEND4 noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201E4	NP_RAW_FRONTEND4_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								short_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	short_ratio	Short exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND4_LONG_RATIO

NP_RAW_FRONTEND4_LONG_RATIO is an NP_RAW_FRONTEND4 noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x201E8	NP_RAW_FRONTEND4_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								long_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	long_ratio	Long exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_RAW_FRONTEND4_OFF

NP_RAW_FRONTEND4_OFF is an NP_RAW_FRONTEND4 noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x201EC	NP_RAW_FRONTEND4_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

RAW_FRONTEND1_CTRL1

RAW_FRONTEND1_CTRL1 is an RAW_FRONTEND1 module control register.

Offset Address	Register Name	Total Reset Value
0x20200	RAW_FRONTEND1_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bright_disable	dark_disable	reserved		show_dynamic_defect_pixel	dp_enable	reserved	ge_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	bright_disable	Bright spot detection control 0: enabled 1: disabled
[6]	RW	dark_disable	Dark spot detection control 0: enabled 1: disabled
[5:4]	RO	reserved	Reserved
[3]	RW	show_dynamic_defect_pixel	Display of detected defect pixels 0: disabled 1: enabled
[2]	RW	dp_enable	Dynamic defect pixel detection enable 0: disabled 1: enabled
[1]	RO	reserved	Reserved
[0]	RW	ge_enable	Green balance enable 0: disabled 1: enabled

RAW_FRONTEND1_GE_STRENGTH

RAW_FRONTEND1_GE_STRENGTH is an RAW_FRONTEND1 GE strength register.

Offset Address	Register Name	Total Reset Value
0x20204	RAW_FRONTEND1_GE_STRENGTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge_strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ge_strength	Green balance strength, configured during calibration

RAW_FRONTEND1_DEBUG_SEL

RAW_FRONTEND1_DEBUG_SEL is an RAW_FRONTEND1 debugging register.

Offset Address	Register Name	Total Reset Value
0x20208	RAW_FRONTEND1_DEBUG_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																debug_sel															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	debug_sel	Debugging port select

RAW_FRONTEND1_DP_THRESHOLD

RAW_FRONTEND1_DP_THRESHOLD is an RAW_FRONTEND1 dynamic defect pixel detection threshold register.

Offset Address	Register Name	Total Reset Value
0x2020C	RAW_FRONTEND1_DP_THRESHOLD	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dp_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dp_threshold	Threshold for defect pixel detection

RAW_FRONTEND1_GE_THRESHOLD

RAW_FRONTEND1_GE_THRESHOLD is an RAW_FRONTEND1 GE threshold register.

Offset Address	Register Name	Total Reset Value
0x20210	RAW_FRONTEND1_GE_THRESHOLD	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ge_threshold	Green balance threshold

RAW_FRONTEND1_DP_SLOPE

RAW_FRONTEND1_DP_SLOPE is an RAW_FRONTEND1 HP masking function slope register.

Offset Address	Register Name	Total Reset Value
0x20214	RAW_FRONTEND1_DP_SLOPE	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dp_slope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dp_slope	Slope of the HP masking function

RAW_FRONTEND1_GE_SLOPE

RAW_FRONTEND1_GE_SLOPE is an RAW_FRONTEND1 GE masking function slope register.

Offset Address	Register Name	Total Reset Value
0x20218	RAW_FRONTEND1_GE_SLOPE	0x0000_00AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge_slope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ge_slope	Slope of the GE masking function

RAW_FRONTEND1_GE_SENS

RAW_FRONTEND1_GE_SENS is an RAW_FRONTEND1 GE module edge sensitivity control register.

Offset Address	Register Name	Total Reset Value
0x2021C	RAW_FRONTEND1_GE_SENS	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge_sens							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ge_sens	Edge sensitivity control of the green balance module

RAW_FRONTEND1_DPDEV_THRESHOLD

RAW_FRONTEND1_DPDEV_THRESHOLD is an RAW_FRONTEND1 control register for the dynamic DPC effect on the edges.

Offset Address	Register Name	Total Reset Value
0x20220	RAW_FRONTEND1_DPDEV_THRESHOLD	0x0000_0266

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dpdev_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dpdev_threshold	Control of the dynamic DPC effect on the edges

RAW_FRONTEND1_LINE_THRESH

RAW_FRONTEND1_LINE_THRESH is an RAW_FRONTEND1 direction control register for the dynamic DPC near the edges.

Offset Address	Register Name	Total Reset Value
0x20224	RAW_FRONTEND1_LINE_THRESH	0x0000_0150

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	line_thresh	Direction control for the dynamic DPC near the edges

RAW_FRONTEND1_DP_BLEND

RAW_FRONTEND1_DP_BLEND is RAW_FRONTEND1 dynamic DPC directional/non-directional replacement value blending control register 10.

Offset Address	Register Name	Total Reset Value
0x20228	RAW_FRONTEND1_DP_BLEND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dp_blend							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	dp_blend	Blending control for the directional and non-directional replacement values of dynamic DPC. If this field is set to 0x00, the detected default is replaced by the non-directional replacement value; if this field is set to 0xFF, the detected fault is replaced by the directional replacement value.

RAW_FRONTEND1_SIGMA_IN

RAW_FRONTEND1_SIGMA_IN is an RAW_FRONTEND1 artificial noise estimation register.

Offset Address	Register Name	Total Reset Value
0x2022C	RAW_FRONTEND1_SIGMA_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sigma_in											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	sigma_in	Artificial noise estimation

RAW_FRONTEND1_THRESH_SHORT

RAW_FRONTEND1_THRESH_SHORT is an RAW_FRONTEND1 short exposure data noise threshold control register.

Offset Address	Register Name	Total Reset Value
0x20230	RAW_FRONTEND1_THRESH_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								thresh_short							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	thresh_short	Noise threshold of short exposure data, 4.4-bit unsigned floating-point number

RAW_FRONTEND1_THRESH_LONG

RAW_FRONTEND1_THRESH_LONG is an RAW_FRONTEND1 long exposure data noise threshold control register.

Offset Address	Register Name	Total Reset Value
0x20234	RAW_FRONTEND1_THRESH_LONG	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								thresh_long							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:0]	RW	thresh_long	Noise threshold of long exposure data, 4.4-bit unsigned floating-point number

RAW_FRONTEND2_CTRL1

RAW_FRONTEND2_CTRL1 is RAW_FRONTEND2 module control register 1.

Offset Address	Register Name	Total Reset Value
0x20240	RAW_FRONTEND2_CTRL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						bright_disable	dark_disable	reserved		show_dynamic_defect_pixel	dp_enable	reserved	ge_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	bright_disable	Bright spot detection control 0: enabled 1: disabled
[6]	RW	dark_disable	Dark spot detection control 0: enabled 1: disabled
[5:4]	RO	reserved	Reserved
[3]	RW	show_dynamic_defect_pixel	Display of detected defect pixels 0: disabled 1: enabled
[2]	RW	dp_enable	Dynamic defect pixel detection enable 0: disabled 1: enabled
[1]	RO	reserved	Reserved

[0]	RW	ge_enable	Green balance enable 0: disabled 1: enabled

RAW_FRONTEND2_GE_STRENGTH

RAW_FRONTEND2_GE_STRENGTH is an RAW_FRONTEND2 GE strength register.

Offset Address	Register Name	Total Reset Value
0x20244	RAW_FRONTEND2_GE_STRENGTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge_strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ge_strength	Green balance strength, configured during calibration

RAW_FRONTEND2_DP_THRESHOLD

RAW_FRONTEND2_DP_THRESHOLD is an RAW_FRONTEND2 dynamic defect pixel detection threshold register.

Offset Address	Register Name	Total Reset Value
0x2024C	RAW_FRONTEND2_DP_THRESHOLD	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dp_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dp_threshold	Threshold for defect pixel detection

RAW_FRONTEND2_GE_THRESHOLD

RAW_FRONTEND2_GE_THRESHOLD is an RAW_FRONTEND2 GE threshold register.

Offset Address	Register Name	Total Reset Value
0x20250	RAW_FRONTEND2_GE_THRESHOLD	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ge_threshold	Green balance threshold

RAW_FRONTEND2_DP_SLOPE

RAW_FRONTEND2_DP_SLOPE is an RAW_FRONTEND2 HP masking function slope register.

Offset Address	Register Name	Total Reset Value
0x20254	RAW_FRONTEND2_DP_SLOPE	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dp_slope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dp_slope	Slope of the HP masking function

RAW_FRONTEND2_GE_SLOPE

RAW_FRONTEND2_GE_SLOPE is an RAW_FRONTEND2 GE masking function slope register.

Offset Address	Register Name	Total Reset Value
0x20258	RAW_FRONTEND2_GE_SLOPE	0x0000_00AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge_slope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ge_slope	Slope of the GE masking function

RAW_FRONTEND2_GE_SENS

RAW_FRONTEND2_GE_SENS is an RAW_FRONTEND2 GE module edge sensitivity control register.

Offset Address	Register Name	Total Reset Value
0x2025C	RAW_FRONTEND2_GE_SENS	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge_sens							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ge_sens	Edge sensitivity control of the green balance module

RAW_FRONTEND2_DPDEV_THRESHOLD

RAW_FRONTEND2_DPDEV_THRESHOLD is an RAW_FRONTEND2 control register for the dynamic DPC effect on the edges.

Offset Address	Register Name	Total Reset Value
0x20260	RAW_FRONTEND2_DPDEV_THRESHOLD	0x0000_0266

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dpdev_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	dpdev_threshold	Control of the dynamic DPC effect on the edges

RAW_FRONTEND2_LINE_THRESH

RAW_FRONTEND2_LINE_THRESH is an RAW_FRONTEND2 direction control register for the dynamic DPC near the edges.

Offset Address	Register Name	Total Reset Value
0x20264	RAW_FRONTEND2_LINE_THRESH	0x0000_0150

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	line_thresh	Direction control for the dynamic DPC near the edges

RAW_FRONTEND2_DP_BLEND

RAW_FRONTEND2_DP_BLEND is RAW_FRONTEND2 dynamic DPC directional/non-directional replacement value blending control register 10.

Offset Address	Register Name	Total Reset Value
0x20268	RAW_FRONTEND2_DP_BLEND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dp_blend							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	dp_blend	Blending control for the directional and non-directional replacement values of dynamic DPC. If this field is set to 0x00, the detected default is replaced by the non-directional replacement value; if this field is set to 0xFF, the detected fault is replaced by the directional replacement value.

RAW_FRONTEND2_SIGMA_IN

RAW_FRONTEND2_SIGMA_IN is an RAW_FRONTEND2 artificial noise estimation register.

Offset Address	Register Name	Total Reset Value
0x2026C	RAW_FRONTEND2_SIGMA_IN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					sigma_in		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	sigma_in	Artificial noise estimation

RAW_FRONTEND2_THRESH_SHORT

RAW_FRONTEND2_THRESH_SHORT is an RAW_FRONTEND2 short exposure data noise threshold control register.

Offset Address	Register Name	Total Reset Value
0x20270	RAW_FRONTEND2_THRESH_SHORT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						thresh_short	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	thresh_short	Noise threshold of short exposure data, 4.4-bit unsigned floating-point number

RAW_FRONTEND2_THRESH_LONG

RAW_FRONTEND2_THRESH_LONG is an RAW_FRONTEND2 long exposure data noise threshold control register.

Offset Address	Register Name	Total Reset Value
0x20274	RAW_FRONTEND2_THRESH_LONG	0x0000_0030

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						thresh_long	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:0]	RW	thresh_long	Noise threshold of long exposure data, 4.4-bit unsigned floating-point number

STATIC_DPC_MULTI_CH_MODE

STATIC_DPC_MULTI_CH_MODE is a STATIC_DPC static DPC 4K/2K mode selection register.

Offset Address	Register Name	Total Reset Value
0x20280	STATIC_DPC_MULTI_CH_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								multi_ch_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	multi_ch_mode	4K/2K mode select 00: 4-channel 4K mode 01: 2-channel 4K mode 10: 2-channel 2K mode 11: reserved

STATIC_DPC_CTRL

STATIC_DPC_CTRL is a static defect pixel module control register.

Offset Address	Register Name	Total Reset Value
0x20284	STATIC_DPC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			detection_trigger2	show_static_defect_pixels2	enable2	show_reference2	pointer_reset2	reserved				detection_trigger1	show_static_defect_pixels1	enable1	show_reference1	pointer_reset1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	detection_trigger2	The defect pixel detection is started upon the 0-1 edge jump.
[11]	RW	show_static_defect_pixels2	Display of the detected defect pixels 0: not displayed 1: displayed
[10]	RW	enable2	DPC enable 0: disabled 1: enabled
[9]	RW	show_reference2	Display of the reference value (used for comparison with the actual value) for implementing defect pixel detection
[8]	RW	pointer_reset2	Set of the defect pixel table pointer for each frame. This field is configured when the slave MCU writes the defect pixel table.
[7:5]	RO	reserved	Reserved
[4]	RW	detection_trigger1	The defect pixel detection is started upon the 0-1 edge jump.
[3]	RW	show_static_defect_pixels1	Display of the detected defect pixels 0: not displayed 1: displayed
[2]	RW	enable1	DPC enable 0: disabled 1: enabled

[1]	RW	show_reference1	Display of the reference value (used for comparison with the actual value) for implementing defect pixel detection 0: not displayed 1: displayed
[0]	RW	pointer_reset1	Set of the defect pixel table pointer for each frame. This field is configured when the slave MCU writes the defect pixel table.

STATIC_DPC_OVERFLOW

STATIC_DPC_OVERFLOW is a static defect pixel module table overflow flag register.

Offset Address	Register Name	Total Reset Value
0x20288	STATIC_DPC_OVERFLOW	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5 4	3 2 1	0
Name	reserved						overflow2	reserved		overflow1
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	overflow2	Table 2 overflow flag 0: no overflow 1: overflow
[7:1]	RO	reserved	Reserved
[0]	RO	overflow1	Table 1 overflow flag 0: no overflow 1: overflow

STATIC_DPC_COUNT

STATIC_DPC_COUNT is a static defect pixel module detected defect pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x2028C	STATIC_DPC_COUNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	defect_pixel_count2			reserved	defect_pixel_count1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	defect_pixel_count2	Number of detected defect pixels
[15:12]	RO	reserved	Reserved
[11:0]	RO	defect_pixel_count1	Number of detected defect pixels

STATIC_DPC_TABLE_START

STATIC_DPC_TABLE_START is a static defect pixel module defect pixel start address register.

Offset Address	Register Name	Total Reset Value
0x20290	STATIC_DPC_TABLE_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	table_start2			reserved	table_start1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	table_start2	Address of the first defect pixel in the defect pixel table
[15:12]	RO	reserved	Reserved
[11:0]	RO	table_start1	Address of the first defect pixel in the defect pixel table

STATIC_DPC_COUNT_IN

STATIC_DPC_COUNT_IN is a static defect pixel module written defect pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x20294	STATIC_DPC_COUNT_IN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	defect_pixel_count_in2			reserved	defect_pixel_count_in1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	defect_pixel_count_in2	Number of defect pixels that are written to the table
[15:12]	RO	reserved	Reserved
[11:0]	RW	defect_pixel_count_in1	Number of defect pixels that are written to the table

WDR_CTRL

WDR_CTRL is a WDR control register.

Offset Address	Register Name	Total Reset Value
0x202A0	WDR_CTRL	0x0F00_C001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved	long_short_thresh			rsvd4	reserved	alpha_slope_from_zero	wdr_mode	rsvd3	enable_np	reserved	rsvd2	rsvd1	rsvd0
Reset	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	long_short_thresh	Threshold. Data above this threshold is obtained from a shorter exposure range.
[15:13]	RW	rsvd4	Not configurable
[12:8]	RO	reserved	Reserved

[7]	RW	alpha_slope_from_zero	Starting point of the alpha slope 0: 1/exposure ratio 1: 0
[6]	RW	wdr_mode	WDR mode select 0: disabled 1: frame switching mode
[5]	RW	rsvd3	Not configurable
[4]	RW	enable_np	Not configurable
[3]	RO	reserved	Reserved
[2]	RW	rsvd2	Not configurable
[1]	RW	rsvd1	Not configurable
[0]	RW	rsvd0	Not configurable

WDR_LONG_CTRL1

WDR_LONG_CTRL1 is WDR long exposure control register 1.

Offset Address	Register Name	Total Reset Value
0x202A4	WDR_LONG_CTRL1	0x0100_0C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				long_exposure_ratio												reserved				long_long_thresh											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	long_exposure_ratio	Exposure ratio, 6.6-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	long_long_thresh	Threshold. Data below this threshold is obtained from a longer exposure range.

WDR_LONG_CTRL2

WDR_LONG_CTRL2 is WDR long exposure control register 2.

Offset Address	Register Name	Total Reset Value
0x202A8	WDR_LONG_CTRL2	0x0080_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								long_stitch_correct								reserved								long_stitch_error_thresh							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	long_stitch_correct	Adjustable error range of the sensor exposure ratio for the blending region, 1.7-bit unsigned fixed-point number
[15:8]	RO	reserved	Reserved
[7:0]	RW	long_stitch_error_thresh	Detection of the strength of the stitching error caused by motion

WDR_LONG_STITCH_ERROR_LIMIT

WDR_LONG_STITCH_ERROR_LIMIT is a WDR long exposure strength configuration register.

Offset Address	Register Name	Total Reset Value
0x202AC	WDR_LONG_STITCH_ERROR_LIMIT	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												long_stitch_error_limit																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	long_stitch_error_limit	Long exposure strength. The detection of the stitching error that is below this strength is disabled.

WDR_MED_CTRL1

WDR_MED_CTRL1 is WDR medium exposure control register 1.

Offset Address	Register Name	Total Reset Value
0x202B0	WDR_MED_CTRL1	0x0F00_C000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				med_short_thresh												rsvd2				reserved								rsvd1	reserved		rsvd0	reserved
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	med_short_thresh	Threshold. Data above this threshold is obtained from a shorter exposure range.
[15:13]	RW	rsvd2	Not configurable
[12:6]	RO	reserved	Reserved
[5]	RW	rsvd1	Not configurable
[4:2]	RO	reserved	Reserved
[1]	RW	rsvd0	Not configurable
[0]	RO	reserved	Reserved

WDR_MED_CTRL2

WDR_MED_CTRL2 is WDR medium exposure control register 2.

Offset Address	Register Name	Total Reset Value
0x202B4	WDR_MED_CTRL2	0x0100_0C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				med_exposure_ratio												reserved				med_long_thresh											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	med_exposure_ratio	Exposure ratio, 6.6-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	med_long_thresh	Threshold. Data below this threshold is obtained from a longer exposure range.

WDR_MED_CTRL3

WDR_MED_CTRL3 is WDR medium exposure control register 3.

Offset Address	Register Name	Total Reset Value
0x202B8	WDR_MED_CTRL3	0x0080_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								med_stitch_correct								reserved								med_stitch_error_thresh							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	med_stitch_correct	Adjustable error range of the sensor exposure ratio for the blending region, 1.7-bit unsigned fixed-point number
[15:8]	RO	reserved	Reserved
[7:0]	RW	med_stitch_error_thresh	Detection of the strength of the stitching error caused by motion

WDR_MED_STITCH_ERROR_LIMIT

WDR_MED_STITCH_ERROR_LIMIT is a WDR medium exposure strength configuration register.

Offset Address	Register Name	Total Reset Value
0x202BC	WDR_MED_STITCH_ERROR_LIMIT	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												med_stitch_error_limit																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	med_stitch_error_limit	Medium exposure strength. The detection of the stitching error that is below this strength is disabled.

WDR_SHORT_CTRL1

WDR_SHORT_CTRL1 is WDR short exposure control register 1.

Offset Address	Register Name	Total Reset Value
0x202C0	WDR_SHORT_CTRL1	0x0F00_C000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				short_short_thresh												rsvd2				reserved								rsvd1	reserved			rsvd0	reserved
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	short_short_thresh	Threshold. Data above this threshold is obtained from a shorter exposure range.
[15:13]	RW	rsvd2	Not configurable
[12:6]	RO	reserved	Reserved
[5]	RW	rsvd1	Not configurable
[4:2]	RO	reserved	Reserved
[1]	RW	rsvd0	Not configurable
[0]	RO	reserved	Reserved

WDR_SHORT_CTRL2

WDR_SHORT_CTRL2 is WDR short exposure control register 2.

Offset Address	Register Name	Total Reset Value
0x202C4	WDR_SHORT_CTRL2	0x0100_0C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				short_exposure_ratio												reserved				short_long_thresh											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	short_exposure_ratio	Exposure ratio, 6.6-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	short_long_thresh	Threshold. Data below this threshold is obtained from a longer exposure range.

WDR_SHORT_CTRL3

WDR_SHORT_CTRL3 is WDR short exposure control register 3.

Offset Address	Register Name	Total Reset Value
0x202C8	WDR_SHORT_CTRL3	0x0080_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								short_stitch_correct								reserved								short_stitch_error_thresh							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	short_stitch_correct	Adjustable error range of the sensor exposure ratio for the blending region, 1.7-bit unsigned fixed-point number
[15:8]	RO	reserved	Reserved
[7:0]	RW	short_stitch_error_thresh	Detection of the strength of the stitching error caused by motion

WDR_SHORT_STITCH_ERROR_LIMIT

WDR_SHORT_STITCH_ERROR_LIMIT is a WDR short exposure strength configuration register.

Offset Address	Register Name	Total Reset Value
0x202CC	WDR_SHORT_STITCH_ERROR_LIMIT	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												short_stitch_error_limit																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	short_stitch_error_limit	Short exposure strength. The detection of the stitching error that is below this strength is disabled.

WDR_BLACK_LEVEL_LONG

WDR_BLACK_LEVEL_LONG is a WDR long exposure input black level register.

Offset Address	Register Name	Total Reset Value
0x202D0	WDR_BLACK_LEVEL_LONG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black_level_long											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black_level_long	Black level of the input long exposure frame

WDR_BLACK_LEVEL_MEDIUM1

WDR_BLACK_LEVEL_MEDIUM1 is WDR medium exposure input black level register 1.

Offset Address	Register Name	Total Reset Value
0x202D4	WDR_BLACK_LEVEL_MEDIUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black_level_medium1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black_level_medium1	Black level of the input medium exposure frame

WDR_BLACK_LEVEL_MEDIUM2

WDR_BLACK_LEVEL_MEDIUM2 is WDR medium exposure input black level register 2.

Offset Address	Register Name	Total Reset Value
0x202D8	WDR_BLACK_LEVEL_MEDIUM2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black_level_medium2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black_level_medium2	Black level of the input medium exposure frame

WDR_BLACK_LEVEL_SHORT

WDR_BLACK_LEVEL_SHORT is a WDR short exposure input black level register.

Offset Address	Register Name	Total Reset Value
0x202DC	WDR_BLACK_LEVEL_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				black_level_short											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	black_level_short	Black level of the input short exposure frame

WDR_BLACK_LEVEL_OUT

WDR_BLACK_LEVEL_OUT is a WDR module output black level register.

Offset Address	Register Name	Total Reset Value
0x202E0	WDR_BLACK_LEVEL_OUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black_level_out																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black_level_out	Module output black level

WDR_MODE_IN

WDR_MODE_IN is a WDR input mode selection register.

Offset Address	Register Name	Total Reset Value
0x202E4	WDR_MODE_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mode_in	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	mode_in	WDR input mode select 00: 4-channel input 01: 2-channel input 10: 3-channel input 11: 4-channel input

FRONTEND_LUT_CTRL

FRONTEND_LUT_CTRL is a FRONTEND_LUT control register.

Offset Address	Register Name	Total Reset Value
0x20300	FRONTEND_LUT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_priority	reserved																	bank_select_1	bank_select_0	reserved		offset_mode_1	offset_mode_0	reserved					enable_dl	enable1	enable0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mcu_priority	CPU port priority 0: low 1: high
[30:14]	RO	reserved	Reserved
[13]	RW	bank_select_1	Valid memory bank switching for LUT 1
[12]	RW	bank_select_0	Valid memory bank switching for LUT 0
[11:10]	RO	reserved	Reserved

[9]	RW	offset_mode_1	Mapping mode of the black level offset region for LUT 1 0: manual curve mapping mode 1: automatic curve mapping mode
[8]	RW	offset_mode_0	Mapping mode of the black level offset region for LUT 0 0: manual curve mapping mode 1: automatic curve mapping mode
[7:3]	RO	reserved	Reserved
[2]	RW	enable_dl	Front-end LUT DL enable 0: disabled 1: enabled
[1]	RW	enable1	Front-end LUT 1 enable 0: disabled 1: enabled
[0]	RW	enable0	Front-end LUT 0 enable 0: disabled 1: enabled

FRONTEND_LUT_MCU_READY

FRONTEND_LUT_MCU_READY is a FRONTEND_LUT status indicator register.

Offset Address	Register Name	Total Reset Value
0x20304	FRONTEND_LUT_MCU_READY	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mcu_ready_1	mcu_ready_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	mcu_ready_1	LUT 1 status indicator. If this bit is set to 1, LUT 1 is ready to receive data from the CPU.
[0]	RO	mcu_ready_0	LUT 0 status indicator. If this bit is set to 1, LUT 0 is ready to receive data from the CPU.

FRONTEND_LUT_ALPHA

FRONTEND_LUT_ALPHA is a FRONTEND_LUT alpha parameter register.

Offset Address	Register Name	Total Reset Value
0x20308	FRONTEND_LUT_ALPHA	0x0000_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				alpha			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:0]	RW	alpha	Front-end alpha parameter, 6.12-bit fixed-point value

DG_GAIN

DG_GAIN is a sensor digital gain register.

Offset Address	Register Name	Total Reset Value
0x20310	DG_GAIN	0x0000_0100

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					gain		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	gain	Sensor digital gain, 5.8-bit unsigned number

DG_OFFSET

DG_OFFSET is a DG black level compensation register.

Offset Address	Register Name	Total Reset Value
0x20314	DG_OFFSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			offset				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19:0]	RW	offset	Black level compensation

DNR_CTRL

DNR_CTRL is a DNR control register.

Offset Address	Register Name	Total Reset Value
0x20320	DNR_CTRL	0x0000_041C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				int_config				rm_enable	int_select	filter_select	enable	rsvd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	int_config	Strength blending with the unprocessed mosaic
[7]	RW	rm_enable	LSC enable 0: disabled 1: enabled
[6]	RW	int_select	Strength filter select enable 0: disabled 1: enabled
[5]	RW	filter_select	NR filter fine-tuning 0: disabled 1: enabled
[4]	RW	enable	NR enable 0: disabled 1: enabled
[3:0]	RW	rsvd	Not configurable

DNR_RM_CENTER_X

DNR_RM_CENTER_X is a DNR shadow graph horizontal coordinate register.

Offset Address	Register Name	Total Reset Value
0x20324	DNR_RM_CENTER_X	0x0000_0280

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rm_center_x															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rm_center_x	Horizontal coordinate of the shadow graph

DNR_RM_CENTER_Y

DNR_RM_CENTER_Y is a DNR shadow graph vertical coordinate register.

Offset Address	Register Name	Total Reset Value
0x20328	DNR_RM_CENTER_Y	0x0000_0168

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rm_center_y															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rm_center_y	Vertical coordinate of the shadow graph

DNR_RM_OFF_CENTER_MULT

DNR_RM_OFF_CENTER_MULT is a DNR normalized factor register.

Offset Address	Register Name	Total Reset Value
0x2032C	DNR_RM_OFF_CENTER_MULT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rm_off_center_mult															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rm_off_center_mult	Normalized factor for extending the radial table to the picture edges. The normalized factor is calculated as follows: Normalized factor = $2^{31}/R^2$ (R indicates the furthest distance between the center coordinates and picture edge pixels)

DNR_THRESH_H01

DNR_THRESH_H01 is a DNR noise threshold register at horizontal spatial-domain high frequencies.

Offset Address	Register Name	Total Reset Value
0x20330	DNR_THRESH_H01	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		thresh_1h		reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	thresh_1h	Noise threshold at horizontal spatial-domain high frequencies
[15:0]	RO	reserved	Reserved

DNR_THRESH_H24

DNR_THRESH_H24 is a DNR noise threshold register at horizontal spatial-domain low frequencies.

Offset Address	Register Name	Total Reset Value
0x20334	DNR_THRESH_H24	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		thresh_4h		reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	thresh_4h	Noise threshold at horizontal spatial-domain low frequencies
[15:0]	RO	reserved	Reserved

DNR_THRESH_V01

DNR_THRESH_V01 is a DNR noise threshold register at vertical spatial-domain high frequencies.

Offset Address	Register Name	Total Reset Value
0x20338	DNR_THRESH_V01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								thresh_1v								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	thresh_1v	Noise threshold at vertical spatial-domain high frequencies
[15:0]	RO	reserved	Reserved

DNR_THRESH_V24

DNR_THRESH_V24 is a DNR noise threshold register at vertical spatial-domain low frequencies.

Offset Address	Register Name	Total Reset Value
0x2033C	DNR_THRESH_V24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								thresh_4v								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	thresh_4v	Noise threshold at vertical spatial-domain low frequencies
[15:0]	RO	reserved	Reserved

DNR_THRESH_SHORT

DNR_THRESH_SHORT is a DNR noise threshold adjustment register for short exposure data.

Offset Address	Register Name	Total Reset Value
0x20344	DNR_THRESH_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								thresh_short							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	thresh_short	Noise threshold adjustment for short exposure data

DNR_THRESH_LONG

DNR_THRESH_LONG is a DNR noise threshold adjustment register for long exposure data.

Offset Address	Register Name	Total Reset Value
0x20348	DNR_THRESH_LONG	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								thresh_long							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	thresh_long	Noise threshold adjustment for long exposure data

DNR_STRENGTH1

DNR_STRENGTH1 is a DNR noise suppression effect register for high spatial frequencies.

Offset Address	Register Name	Total Reset Value
0x20350	DNR_STRENGTH1	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								strength_1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	strength_1	Noise suppression effect of high spatial frequencies

DNR_STRENGTH4

DNR_STRENGTH4 is a DNR noise suppression effect register for low spatial frequencies.

Offset Address	Register Name	Total Reset Value
0x20358	DNR_STRENGTH4	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								strength_4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	strength_4	Noise suppression effect of low spatial frequencies

BACKEND_LUT_CRTL

BACKEND_LUT_CRTL is a BACKEND_LUT control register.

Offset Address	Register Name	Total Reset Value
0x20360	BACKEND_LUT_CRTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_priority	reserved																	bank_select_1	bank_select_0	reserved		offset_mode_1	offset_mode_0	reserved				enable_dl	enable1	enable0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mcu_priority	CPU port priority 0: low 1: high
[30:14]	RO	reserved	Reserved
[13]	RW	bank_select_1	Memory bank select for LUT 1 0: memory bank 0 1: memory bank 1
[12]	RW	bank_select_0	Memory bank select for LUT 0 0: memory bank 0 1: memory bank 1

[11:10]	RO	reserved	Reserved
[9]	RW	offset_mode_1	Mapping mode of the black level offset region for LUT 1 0: manual curve mapping mode 1: automatic curve mapping mode
[8]	RW	offset_mode_0	Mapping mode of the black level offset region for LUT 0 0: manual curve mapping mode 1: automatic curve mapping mode
[7:3]	RO	reserved	Reserved
[2]	RW	enable_dl	Back-end LUT DL enable 0: disabled 1: enabled
[1]	RW	enable1	Back-end LUT 1 enable 0: disabled 1: enabled
[0]	RW	enable0	Back-end LUT 0 enable 0: disabled 1: enabled

BACKEND_LUT_MCU_READY

BACKEND_LUT_MCU_READY is a BACKEND_LUT status indicator register.

Offset Address	Register Name	Total Reset Value
0x20364	BACKEND_LUT_MCU_READY	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mcu_ready_1	mcu_ready_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	mcu_ready_1	LUT 1 status indicator. If this bit is set to 1, LUT 1 is ready to receive data from the CPU.
[0]	RO	mcu_ready_0	LUT 0 status indicator. If this bit is set to 1, LUT 0 is ready to receive data from the CPU.

BACKEND_LUT_ALPHA

BACKEND_LUT_ALPHA is a BACKEND_LUT alpha parameter register.

Offset Address	Register Name	Total Reset Value
0x20368	BACKEND_LUT_ALPHA	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																alpha															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:0]	RW	alpha	Front-end alpha parameter, 6.12-bit fixed-point value

NP_FOR_DNR_EXP_THRESH

NP_FOR_DNR_EXP_THRESH is an NP_FOR_DNR noise threshold register.

Offset Address	Register Name	Total Reset Value
0x20370	NP_FOR_DNR_EXP_THRESH	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																exp_thresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	exp_thresh	Threshold of the long/short exposure data

NP_FOR_DNR_SHORT_RATIO

NP_FOR_DNR_SHORT_RATIO is an NP_FOR_DNR noise short exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x20374	NP_FOR_DNR_SHORT_RATIO	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								short_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:0]	RW	short_ratio	Short exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_FOR_DNR_LONG_RATIO

NP_FOR_DNR_LONG_RATIO is an NP_FOR_DNR noise long exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x20378	NP_FOR_DNR_LONG_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								long_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	long_ratio	Long exposure noise ratio, 6.2-bit unsigned fixed-point number

NP_FOR_DNR_OFF

NP_FOR_DNR_OFF is an NP_FOR_DNR noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x2037C	NP_FOR_DNR_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

WB_GAIN00

WB_GAIN00 is a WB module R component gain register.

Offset Address	Register Name	Total Reset Value
0x20380	WB_GAIN00	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gain00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	gain00	Multiple of color channel R, 4.8-bit unsigned fixed-point number

WB_GAIN01

WB_GAIN01 is a WB module Gr component gain register.

Offset Address	Register Name	Total Reset Value
0x20384	WB_GAIN01	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gain01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	gain01	Multiple of color channel Gr, 4.8-bit unsigned fixed-point number

WB_GAIN10

WB_GAIN10 is a WB module Gb component gain register.

Offset Address	Register Name	Total Reset Value
0x20388	WB_GAIN10	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gain10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	gain10	Multiple of color channel Gb, 4.8-bit unsigned fixed-point number

WB_GAIN11

WB_GAIN11 is a WB module B component gain register.

Offset Address	Register Name	Total Reset Value
0x2038C	WB_GAIN11	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gain11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	gain11	Multiple of color channel B, 4.8-bit unsigned fixed-point number

BLC_BLACK00

BLC_BLACK00 is a BLC R component black level offset register.

Offset Address	Register Name	Total Reset Value
0x203A0	BLC_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black00																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black00	Black level offset of color channel R

BLC_BLACK01

BLC_BLACK01 is a BLC Gr component black level offset register.

Offset Address	Register Name	Total Reset Value
0x203A4	BLC_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black01																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black01	Black level offset of color channel Gr

BLC_BLACK10

BLC_BLACK10 is a BLC Gb component black level offset register.

Offset Address	Register Name	Total Reset Value
0x203A8	BLC_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black10																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black10	Black level offset of color channel Gb

BLC_BLACK11

BLC_BLACK11 is a BLC B component black level offset register.

Offset Address	Register Name	Total Reset Value
0x203AC	BLC_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												black11																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black11	Black level offset of color channel B

RADIAL_SHADING_CTRL

RADIAL_SHADING_CTRL is a Radial_Shading module control register.

Offset Address	Register Name	Total Reset Value
0x203B0	RADIAL_SHADING_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mcupriority	reserved						enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	mcupriority	CPU write priority of the radial shading LUTs 0: low 1: high
[6:1]	RO	reserved	Reserved
[0]	RW	enable	LSC enable 0: disabled 1: enabled

RADIAL_SHADING_MCU_READY

RADIAL_SHADING_MCU_READY is a Radial_Shading LUT status register.

Offset Address	Register Name	Total Reset Value
0x203B4	RADIAL_SHADING_MCU_READY	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mcuready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	mcuready	If this bit is set to 1, the LUT is ready to receive data from the CPU.

RADIAL_SHADING_RX

RADIAL_SHADING_RX is a Radial_Shading R component center X coordinate register.

Offset Address	Register Name	Total Reset Value
0x203B8	RADIAL_SHADING_RX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerr_x															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerr_x	Horizontal coordinate of the center of the red shading map

RADIAL_SHADING_RY

RADIAL_SHADING_RY is a Radial_Shading R component center Y coordinate register.

Offset Address	Register Name	Total Reset Value
0x203BC	RADIAL_SHADING_RY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerr_y															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerr_y	Vertical coordinate of the center of the red shading map

RADIAL_SHADING_GX

RADIAL_SHADING_GX is a Radial_Shading G component center X coordinate register.

Offset Address	Register Name	Total Reset Value
0x203C0	RADIAL_SHADING_GX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerg_x															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerg_x	Horizontal coordinate of the center of the green shading map

RADIAL_SHADING_GY

RADIAL_SHADING_GY is a Radial_Shading G component center Y coordinate register.

Offset Address	Register Name	Total Reset Value
0x203C4	RADIAL_SHADING_GY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerg_y															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerg_y	Vertical coordinate of the center of the green shading map

RADIAL_SHADING_BX

RADIAL_SHADING_BX is a Radial_Shading B component center X coordinate register.

Offset Address	Register Name	Total Reset Value
0x203C8	RADIAL_SHADING_BX	0x0000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerb_x															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerb_x	Horizontal coordinate of the center of the blue shading map

RADIAL_SHADING_BY

RADIAL_SHADING_BY is a Radial_Shading B component center Y coordinate register.

Offset Address	Register Name	Total Reset Value
0x203CC	RADIAL_SHADING_BY	0x0000_021C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerb_y															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	centerb_y	Vertical coordinate of the center of the blue shading map

RADIAL_SHADING_MULTR

RADIAL_SHADING_MULTR is a Radial_Shading red radial table normalized factor register.

Offset Address	Register Name	Total Reset Value
0x203D0	RADIAL_SHADING_MULTR	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																off_center_multr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	off_center_multr	Normalized factor for extending the red radial table to the picture edges. The normalized factor is calculated as follows: Normalized factor = $2^{31}/R^2$ (R indicates the furthest distance between the center coordinates and picture edge pixels)

RADIAL_SHADING_MULTG

RADIAL_SHADING_MULTG is a Radial_Shading green radial table normalized factor register.

Offset Address	Register Name	Total Reset Value
0x203D4	RADIAL_SHADING_MULTG	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																off_center_multg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	off_center_multg	Normalized factor for extending the green radial table to the picture edges. The normalized factor is calculated as follows: Normalized factor = $2^{31}/R^2$ (R indicates the furthest distance between the center coordinates to picture edge pixels)

RADIAL_SHADING_MULTB

RADIAL_SHADING_MULTB is a Radial_Shading blue radial table normalized factor register.

Offset Address	Register Name	Total Reset Value
0x203D8	RADIAL_SHADING_MULTB	0x0000_06EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																off_center_multb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	off_center_multb	Normalized factor for extending the blue radial table to the picture edges. The normalized factor is calculated as follows: Normalized factor = $2^{31}/R^2$ (R indicates the furthest distance between the center coordinates to picture edge pixels)

MESH_SHADING_CTRL

MESH_SHADING_CTRL is a Mesh_Shading control register.

Offset Address	Register Name	Total Reset Value
0x203E0	MESH_SHADING_CTRL	0x3F3F_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mesh_height				reserved				mesh_width				reserved		mesh_page_b		mesh_page_g		mesh_page_r		reserved				mesh_scale			mesh_show	enable
Reset	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:24]	RW	mesh_height	Number of vertical nodes minus 1
[23:22]	RO	reserved	Reserved
[21:16]	RW	mesh_width	Number of horizontal nodes minus 1
[15:14]	RO	reserved	Reserved
[13:12]	RW	mesh_page_b	Memory page corresponding to blue component correction
[11:10]	RW	mesh_page_g	Memory page corresponding to green component correction
[9:8]	RW	mesh_page_r	Memory page corresponding to red component correction
[7:5]	RO	reserved	Reserved
[4:2]	RW	mesh_scale	Precision and maximum gain range 000: 0−2 001: 0−4 010: 0−8 011: 0−16 100: 1−2 101: 1−3 110: 1−5 111: 1−9 Note: The gain is a floating-point value.
[1]	RW	mesh_show	LSC debugging enable 0: disabled 1: enabled
[0]	RW	enable	LSC enable 0: disabled 1: enabled

MESH_SHADING_RELOAD

MESH_SHADING_RELOAD is a Mesh_Shading buffer update register.

Offset Address	Register Name	Total Reset Value
0x203E4	MESH_SHADING_RELOAD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mesh_reload
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mesh_reload	Buffer update triggered when the bit value is changed from 0 to 1

MESH_SHADING_ALPHAMODE

MESH_SHADING_ALPHAMODE is a Mesh_Shading entry alpha blending mode register.

Offset Address	Register Name	Total Reset Value
0x203F0	MESH_SHADING_ALPHAMODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mesh_alpha_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	mesh_alpha_mode	Alpha blending mode for Mesh_Shading entries 00: no alpha blending 01: 2 banks (odd/even byte) 10: 4 banks 11: reserved

MESH_SHADING_ALPHA_BANK

MESH_SHADING_ALPHA_BANK is a Mesh_Shading blending bank selection register.

Offset Address	Register Name	Total Reset Value
0x203F4	MESH_SHADING_ALPHA_BANK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			mesh_alpha_bank_b	reserved	mesh_alpha_bank_g	reserved	mesh_alpha_bank_r
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	mesh_alpha_bank_b	Bank select for B component blending 000: 0 + 1 001: 1 + 2 010: 2:3 011: 3 + 0 100: 0 + 2 101: 1 + 3 11X: reserved
[15:11]	RO	reserved	Reserved
[10:8]	RW	mesh_alpha_bank_g	Bank select for G component blending 000: 0 + 1 001: 1 + 2 010: 2:3 011: 3 + 0 100: 0 + 2 101: 1 + 3 11X: reserved
[7:3]	RO	reserved	Reserved

[2:0]	RW	mesh_alpha_bank_r	Bank select for R component blending 000: 0 + 1 001: 1 + 2 010: 2:3 011: 3 + 0 100: 0 + 2 101: 1 + 3 11X: reserved

MESH_SHADING_ALPHA

MESH_SHADING_ALPHA is a Mesh_Shading alpha blending coefficient register.

Offset Address	Register Name	Total Reset Value
0x203F8	MESH_SHADING_ALPHA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		mesh_alpha_b		mesh_alpha_g		mesh_alpha_r	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mesh_alpha_b	Alpha blending coefficient of the B component
[15:8]	RW	mesh_alpha_g	Alpha blending coefficient of the G component
[7:0]	RW	mesh_alpha_r	Alpha blending coefficient of the R component

MESH_SHADING_STRENGTH

MESH_SHADING_STRENGTH is a Mesh_Shading correction strength control register.

Offset Address	Register Name	Total Reset Value
0x203FC	MESH_SHADING_STRENGTH	0x0000_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				mesh_strength			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	mesh_strength	Mesh correction strength, 4.12-bit. For example, the value 0 indicates no correction, and the value 4096 indicates the correction of the matched mesh data. This field can be used to to reduce the shading correction strength based on the AE.

DRC_ENABLE

DRC_ENABLE is a DRC enable register.

Offset Address	Register Name	Total Reset Value
0x20400	DRC_ENABLE	0x0000_4629

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rsvd3		reserved		rsvd2				reserved		rsvd1		reserved		rsvd0		reserved			drc_on
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	1	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:14]	RW	rsvd3	Not configurable
[13:11]	RO	reserved	Reserved
[10:8]	RW	rsvd2	Not configurable
[7]	RO	reserved	Reserved
[6:5]	RW	rsvd1	Not configurable
[4]	RO	reserved	Reserved
[3]	RW	rsvd0	Not configurable
[2:1]	RO	reserved	Reserved
[0]	RW	drc_on	DRC enable 0: disabled 1: enabled

DRC_CTRL

DRC_CTRL is a DRC module control register.

Offset Address	Register Name	Total Reset Value
0x20408	DRC_CTRL	0x0040_8012

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		slope_min		slope_max		variance_intensity	variance_space
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 1	0 0 1 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	slope_min	Limit on the minimum slope (gain) generated by the adaptive algorithm
[15:8]	RW	slope_max	Limit on the maximum slope (gain) generated by the adaptive algorithm
[7:4]	RW	variance_intensity	Algorithm luminance sensitivity
[3:0]	RW	variance_space	Algorithm spatial-domain sensitivity

DRC_BLACK_LEVEL

DRC_BLACK_LEVEL is a DRC black level register.

Offset Address	Register Name	Total Reset Value
0x20410	DRC_BLACK_LEVEL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			black_level				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	black_level	DRC black level. DRC is not implemented for pixels with the values below the field value.

DRC_WHITE_LEVEL

DRC_WHITE_LEVEL is a DRC white level register.

Offset Address	Register Name	Total Reset Value
0x20414	DRC_WHITE_LEVEL	0x000F_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												white_level																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	white_level	DRC white level. DRC is not implemented for pixels with the values above the field value.

DRC_MCU_READY

DRC_MCU_READY is a DRC LUT status indicator register.

Offset Address	Register Name	Total Reset Value
0x20438	DRC_MCU_READY	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													mcu_ready_rev	mcu_ready_fwd	mcu_priority
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RO	mcu_ready_rev	rev_percept LUT status indicator. If this bit is set to 1, the LUT is ready to receive data from the CPU.
[1]	RO	mcu_ready_fwd	fwd_percept LUT status indicator. If this bit is set to 1, the LUT is ready to receive data from the CPU.
[0]	RO	mcu_priority	CPU write priority of the LUT 0: low 1: high

DEMOSAIC_VH_SLOPE

DEMOSAIC_VH_SLOPE is a demosaic vertical/horizontal blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x20480	DEMOSAIC_VH_SLOPE	0x0000_00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vh_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	vh_slope	Slope of the vertical/horizontal blending threshold, 4.4-bit logarithm

DEMOSAIC_AA_SLOPE

DEMOSAIC_AA_SLOPE is a demosaic angle blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x20484	DEMOSAIC_AA_SLOPE	0x0000_00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								aa_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	aa_slope	Slope of the angle blending threshold, 4.4-bit logarithm

DEMOSAIC_VA_SLOPE

DEMOSAIC_VA_SLOPE is a demosaic VH-AA (VA) blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x20488	DEMOSAIC_VA_SLOPE	0x0000_00AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								va_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	va_slope	Slope of the VH-AA (VA) blending threshold, 4.4-bit logarithm

DEMOSAIC_UU_SLOPE

DEMOSAIC_UU_SLOPE is a demosaic undefined blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x2048C	DEMOSAIC_UU_SLOPE	0x0000_00AD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								uu_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	uu_slope	Slope of the undefined blending threshold, 4.4-bit logarithm

DEMOSAIC_SAT_SLOPE

DEMOSAIC_SAT_SLOPE is a demosaic saturation blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x20490	DEMOSAIC_SAT_SLOPE	0x0000_005D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sat_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	sat_slope	Slope of the saturation blending threshold, 2.6-bit linear value

DEMOSAIC_VH_THRESH

DEMOSAIC_VH_THRESH is a demosaic vertical/horizontal blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x20494	DEMOSAIC_VH_THRESH	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vh_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	vh_thresh	Threshold for the vertical/horizontal blending range

DEMOSAIC_AA_THRESH

DEMOSAIC_AA_THRESH is a demosaic angle blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x20498	DEMOSAIC_AA_THRESH	0x0000_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				aa_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	aa_thresh	Threshold for the angle blending range

DEMOSAIC_VA_THRESH

DEMOSAIC_VA_THRESH is a demosaic VA blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x2049C	DEMOSAIC_VA_THRESH	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				va_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	va_thresh	Threshold for the VA blending range

DEMOSAIC_UU_THRESH

DEMOSAIC_UU_THRESH is a demosaic undefined blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x204A0	DEMOSAIC_UU_THRESH	0x0000_0171

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				uu_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	uu_thresh	Threshold for the undefined blending range

DEMOSAIC_SAT_THRESH

DEMOSAIC_SAT_THRESH is a demosaic saturation blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x204A4	DEMOSAIC_SAT_THRESH	0x0000_0171

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sat_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	sat_thresh	Threshold for the saturation blending range, 2.9-bit signed number

DEMOSAIC_VH_OFFSET

DEMOSAIC_VH_OFFSET is a demosaic vertical/horizontal blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204A8	DEMOSAIC_VH_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vh_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	vh_offset	Offset of the vertical/horizontal blending threshold

DEMOSAIC_AA_OFFSET

DEMOSAIC_AA_OFFSET is a demosaic angle blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204AC	DEMOSAIC_AA_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				aa_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	aa_offset	Offset of the angle blending threshold

DEMOSAIC_VA_OFFSET

DEMOSAIC_VA_OFFSET is a demosaic VA blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B0	DEMOSAIC_VA_OFFSET	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				va_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	va_offset	Offset of the VA blending threshold

DEMOSAIC_UU_OFFSET

DEMOSAIC_UU_OFFSET is a demosaic undefined blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B4	DEMOSAIC_UU_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				uu_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	uu_offset	Offset of the undefined blending threshold

DEMOSAIC_SAT_OFFSET

DEMOSAIC_SAT_OFFSET is a demosaic saturation blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204B8	DEMOSAIC_SAT_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sat_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	sat_offset	Offset of the saturation blending threshold, 2.9-bit

DEMOSAIC_SHARP_ALT_D

DEMOSAIC_SHARP_ALT_D is a demosaic directional sharpening mask strength register.

Offset Address	Register Name	Total Reset Value
0x204BC	DEMOSAIC_SHARP_ALT_D	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharp_alt_d							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	sharp_alt_d	Strength of the directional sharpening mask, 4.4-bit signed number

DEMOSAIC_SHARP_ALT_UD

DEMOSAIC_SHARP_ALT_UD is a demosaic non-directional sharpening mask strength register.

Offset Address	Register Name	Total Reset Value
0x204C0	DEMOSAIC_SHARP_ALT_UD	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharp_alt_ud							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	sharp_alt_ud	Strength of the non-directional sharpening mask, 4.4-bit signed number

DEMOSAIC_LUM_THRESH

DEMOSAIC_LUM_THRESH is a demosaic directional sharpening luminance threshold register.

Offset Address	Register Name	Total Reset Value
0x204C4	DEMOSAIC_LUM_THRESH	0x0000_0060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lum_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	lum_thresh	Threshold for the directional sharpening luminance

DEMOSAIC_NP_OFFSET

DEMOSAIC_NP_OFFSET is a demosaic configured noise offset register.

Offset Address	Register Name	Total Reset Value
0x204C8	DEMOSAIC_NP_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	np_offset	Configured noise offset, 4.4-bit logarithm

DEMOSAIC_DMSC_CONFIG

DEMOSAIC_DMSC_CONFIG is a demosaic debugging output selection register.

Offset Address	Register Name	Total Reset Value
0x204CC	DEMOSAIC_DMSC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dmsc_config							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	dmsc_config	Debugging output select. The value 0x00 indicates the normal mode.

DEMOSAIC_AC_THRESH

DEMOSAIC_AC_THRESH is a demosaic AC blending range threshold register.

Offset Address	Register Name	Total Reset Value
0x204D0	DEMOSAIC_AC_THRESH	0x0000_01B3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ac_thresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ac_thresh	Threshold for the AC blending range, 2.9-bit signed number

DEMOSAIC_AC_SLOPE

DEMOSAIC_AC_SLOPE is a demosaic AC blending threshold slope register.

Offset Address	Register Name	Total Reset Value
0x204D4	DEMOSAIC_AC_SLOPE	0x0000_00CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ac_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ac_slope	Slope of the AC blending threshold, 2.6-bit linear value

DEMOSAIC_AC_OFFSET

DEMOSAIC_AC_OFFSET is a demosaic AC blending threshold offset register.

Offset Address	Register Name	Total Reset Value
0x204D8	DEMOSAIC_AC_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ac_offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	ac_offset	Offset of the AC blending threshold, 2.9-bit signed number

DEMOSAIC_FC_SLPOE

DEMOSAIC_FC_SLPOE is a demosaic false color correction slope (strength) register.

Offset Address	Register Name	Total Reset Value
0x204DC	DEMOSAIC_FC_SLPOE	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fc_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fc_slope	False color correction slope (strength)

DEMOSAIC_FC_ALIAS_SLPOE

DEMOSAIC_FC_ALIAS_SLPOE is a demosaic false color correction slope (strength) register.

Offset Address	Register Name	Total Reset Value
0x204E0	DEMOSAIC_FC_ALIAS_SLPOE	0x0000_0055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fc_alias_slope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fc_alias_slope	False color correction slope (strength) when the saturation value is in U2.6 format

DEMOSAIC_FC_ALIAS_THRESH

DEMOSAIC_FC_ALIAS_THRESH is a demosaic anti-false color threshold register.

Offset Address	Register Name	Total Reset Value
0x204E4	DEMOSAIC_FC_ALIAS_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fc_alias_thresh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fc_alias_thresh	Anti-false color threshold when the saturation value is in U0.8 format

DEMOSAIC_NP_OFF

DEMOSAIC_NP_OFF is a demosaic noise black level offset register.

Offset Address	Register Name	Total Reset Value
0x204EC	DEMOSAIC_NP_OFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								np_off_reflect	np_off						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	np_off_reflect	Method of obtaining values below the black level 0: The input of the first table is repeated. 1: The part below the black level on the noise curve is mapped.
[6:0]	RW	np_off	Noise black level offset

DEMOSAIC_SHARP

DEMOSAIC_SHARP is a demosaic sharpening strength register.

Offset Address	Register Name	Total Reset Value
0x204F0	DEMOSAIC_SHARP	0x1010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sad_amp								sharp_alt_lu								sharp_alt_ldu								sharp_alt_ld							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	sad_amp	SAD amplifier, 4.4-bit unsigned number
[23:16]	RW	sharp_alt_lu	L_Lu sharpening strength, 4.4-bit unsigned number
[15:8]	RW	sharp_alt_ldu	L_Ldu sharpening strength, 4.4-bit unsigned number
[7:0]	RW	sharp_alt_ld	L_Ld sharpening strength, 4.4-bit unsigned number

DEMOSAIC_MIN_THRESHOLD

DEMOSAIC_MIN_THRESHOLD is a demosaic threshold register.

Offset Address	Register Name	Total Reset Value
0x204F4	DEMOSAIC_MIN_THRESHOLD	0x1F48_1F33

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				min_ud_strength												reserved				min_d_strength											
Reset	0	0	0	1	1	1	1	1	0	1	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	min_ud_strength	L_Lu non-directional minimum threshold, 12-bit signed number, binary complement
[15:13]	RO	reserved	Reserved
[12:0]	RW	min_d_strength	L_L directional minimum threshold, 12-bit signed number, binary complement

DEMOSAIC_SHARPEN_ALG_SELECT

DEMOSAIC_SHARPEN_ALG_SELECT is a demosaic new sharpening algorithm switching register.

Offset Address	Register Name	Total Reset Value
0x204F8	DEMOSAIC_SHARPEN_ALG_SELECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sharpen_alg_select
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	sharpen_alg_select	Whether to switch to the new sharpening algorithm 0: no 1: yes

COLOR_MATRIX_COEFFT_RR

COLOR_MATRIX_COEFFT_RR is a COLOR_MATRIX R-R multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20500	COLOR_MATRIX_COEFFT_RR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftr_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftr_r	R-R multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_RG

COLOR_MATRIX_COEFFT_RG is a COLOR_MATRIX R-G multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20504	COLOR_MATRIX_COEFFT_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftr_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftr_g	R-G multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_RB

COLOR_MATRIX_COEFFT_RB is a COLOR_MATRIX R-B multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20508	COLOR_MATRIX_COEFFT_RB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftr_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftr_b	R-B multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_GR

COLOR_MATRIX_COEFFT_GR is a COLOR_MATRIX G-R multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x2050C	COLOR_MATRIX_COEFFT_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftg_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftg_r	G-R multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_GG

COLOR_MATRIX_COEFFT_GG is a COLOR_MATRIX G-G multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20510	COLOR_MATRIX_COEFFT_GG	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftg_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftg_g	G-G multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_GB

COLOR_MATRIX_COEFFT_GB is a COLOR_MATRIX G-B multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20514	COLOR_MATRIX_COEFFT_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftg_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftg_b	G-B multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_BR

COLOR_MATRIX_COEFFT_BR is a COLOR_MATRIX B-R multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20518	COLOR_MATRIX_COEFFT_BR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftb_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftb_r	B-R multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_BG

COLOR_MATRIX_COEFFT_BG is a COLOR_MATRIX B-G multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x2051C	COLOR_MATRIX_COEFFT_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftb_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	coefftb_g	B-G multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_BB

COLOR_MATRIX_COEFFT_BB is a COLOR_MATRIX B-B multiple matrix coefficient register.

Offset Address	Register Name	Total Reset Value
0x20520	COLOR_MATRIX_COEFFT_BB	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefftb_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	coefftb_b	B-B multiple matrix coefficient, 4.8-bit signed fixed-point number

COLOR_MATRIX_CTRL

COLOR_MATRIX_CTRL is a COLOR_MATRIX enable register.

Offset Address	Register Name	Total Reset Value
0x20524	COLOR_MATRIX_CTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved

[0]	RW	enable	Color_Matrix enable 0: disabled 1: enabled

COLOR_MATRIX_COEFFT_WBR

COLOR_MATRIX_COEFFT_WBR is a COLOR_MATRIX R WB gain register.

Offset Address	Register Name	Total Reset Value
0x20528	COLOR_MATRIX_COEFFT_WBR	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft_wb_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	coefft_wb_r	WB gain of the R component, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_WBG

COLOR_MATRIX_COEFFT_WBG is a COLOR_MATRIX G WB gain register.

Offset Address	Register Name	Total Reset Value
0x2052C	COLOR_MATRIX_COEFFT_WBG	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft_wb_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	coefft_wb_g	WB gain of the G component, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_WBB

COLOR_MATRIX_COEFFT_WBB is a COLOR_MATRIX B WB gain register.

Offset Address	Register Name	Total Reset Value
0x20530	COLOR_MATRIX_COEFFT_WBB	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coefft_wb_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	coefft_wb_b	WB gain of the B component, 4.8-bit signed fixed-point number

COLOR_MATRIX_COEFFT_FOG_OFFSETR

COLOR_MATRIX_COEFFT_FOG_OFFSETR is a COLOR_MATRIX R offset register.

Offset Address	Register Name	Total Reset Value
0x20534	COLOR_MATRIX_COEFFT_FOG_OFFSETR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				coefft_fog_offset_r											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	coefft_fog_offset_r	R component offset, 12-bit unsigned integer

COLOR_MATRIX_COEFFT_FOG_OFFSETG

COLOR_MATRIX_COEFFT_FOG_OFFSETG is a COLOR_MATRIX G offset register.

Offset Address	Register Name	Total Reset Value
0x20538	COLOR_MATRIX_COEFFT_FOG_OFFSETG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				coefft_fog_offset_g											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	coefft_fog_offset_g	G component offset, 12-bit unsigned integer

COLOR_MATRIX_COEFFT_FOG_OFFSETB

COLOR_MATRIX_COEFFT_FOG_OFFSETB is a COLOR_MATRIX B offset register.

Offset Address	Register Name	Total Reset Value
0x2053C	COLOR_MATRIX_COEFFT_FOG_OFFSETB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				coefft_fog_offset_b												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	coefft_fog_offset_b	B component offset, 12-bit unsigned integer

GAMMA_RGB_CTRL

GAMMA_RGB_CTRL is a GAMMA_RGB control register.

Offset Address	Register Name	Total Reset Value
0x20580	GAMMA_RGB_CTRL	0x0000_0081

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mcu_priority	reserved			bank_select	reserved			enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	mcu_priority	CPU write priority of the LUT 0: low 1: high
[6:5]	RO	reserved	Reserved
[4]	RW	bank_select	LUT RAM bank select for GAMMA_RGB 0: bank 0 1: bank 1

[3:1]	RO	reserved	Reserved
[0]	RW	enable	Gamma RGB enable 0: disabled 1: enabled

GAMMA_RGB_MCU_READY

GAMMA_RGB_MCU_READY is a GAMMA_RGB LUT status indicator register for data reception from the CPU.

Offset Address	Register Name	Total Reset Value
0x20584	GAMMA_RGB_MCU_READY	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							mcu_ready
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	mcu_ready	If this bit is set to 1, the LUT is ready to receive data from the CPU.

DITHER_CTRL

DITHER_CTRL is a dither control register.

Offset Address	Register Name	Total Reset Value
0x20680	DITHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											shift_mode	reserved		dither_amount		enable_dither	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	shift_mode	Output mode select 0: The output is LSB-aligned. 1: The output is MSB-aligned.
[3]	RO	reserved	Reserved
[2:1]	RW	dither_amount	Mode select 00: The output bit width is adjusted to nine bits. 01: The output bit width is adjusted to eight bits. 10: The output bit width is adjusted to seven bits. 11: The output bit width is adjusted to six bits.
[0]	RW	enable_dither	Dither module enable 0: disabled 1: enabled

STATISTICS_HIST_THRESH_0_1

STATISTICS_HIST_THRESH_0_1 is a bin 0/1 boundary histogram threshold register.

Offset Address	Register Name	Total Reset Value
0x20700	STATISTICS_HIST_THRESH_0_1	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hist_thresh_0_1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hist_thresh_0_1	Histogram threshold of the bin 0/1 boundary

STATISTICS_HIST_THRESH_1_2

STATISTICS_HIST_THRESH_1_2 is a bin 1/2 boundary histogram threshold register.

Offset Address	Register Name	Total Reset Value
0x20704	STATISTICS_HIST_THRESH_1_2	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hist_thresh_1_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hist_thresh_1_2	Histogram threshold of the bin 1/2 boundary

STATISTICS_HIST_THRESH_3_4

STATISTICS_HIST_THRESH_3_4 is a bin 2/3 boundary histogram threshold register.

Offset Address	Register Name	Total Reset Value
0x20708	STATISTICS_HIST_THRESH_3_4	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hist_thresh_3_4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hist_thresh_3_4	Histogram threshold of the bin2/3 boundary

STATISTICS_HIST_THRESH_4_5

STATISTICS_HIST_THRESH_4_5 is a bin 3/4 boundary histogram threshold register.

Offset Address	Register Name	Total Reset Value
0x2070C	STATISTICS_HIST_THRESH_4_5	0x0000_00E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hist_thresh_4_5							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hist_thresh_4_5	Histogram threshold of the bin 3/4 boundary

STATISTICS_HIST_0

STATISTICS_HIST_0 is a bin 0 normalized histogram register.

Offset Address	Register Name	Total Reset Value
0x20720	STATISTICS_HIST_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hist_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	hist_0	Normalized histogram of bin 0

STATISTICS_HIST_1

STATISTICS_HIST_1 is a bin 1 normalized histogram register.

Offset Address	Register Name	Total Reset Value
0x20724	STATISTICS_HIST_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hist_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	hist_1	Normalized histogram of bin 1

STATISTICS_HIST_3

STATISTICS_HIST_3 is a bin 3 normalized histogram register.

Offset Address	Register Name	Total Reset Value
0x20728	STATISTICS_HIST_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hist3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	hist3	Normalized histogram of bin 3

STATISTICS_HIST_4

STATISTICS_HIST_4 is a bin 4 normalized histogram register.

Offset Address	Register Name	Total Reset Value
0x2072C	STATISTICS_HIST_4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hist_4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	hist_4	Normalized histogram of bin 4

STATISTICS_AEXP_NODES_USED

STATISTICS_AEXP_NODES_USED is an AE active region register.

Offset Address	Register Name	Total Reset Value
0x20730	STATISTICS_AEXP_NODES_USED	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aexp_nodes_used_vert								aexp_nodes_used_horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:8]	RW	aexp_nodes_used_vert	Number of AE vertical active regions
[7:0]	RW	aexp_nodes_used_horiz	Number of AE horizontal active regions

STATISTICS_WHITE_LEVEL_AWB

STATISTICS_WHITE_LEVEL_AWB is an RGB field AWB statistics white point luminance upper limit register.

Offset Address	Register Name	Total Reset Value
0x20740	STATISTICS_WHITE_LEVEL_AWB	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						white_level_awb									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	white_level_awb	Luminance data upper limit for the white points of RGB field AWB statistics

STATISTICS_BLACK_LEVEL_AWB

STATISTICS_BLACK_LEVEL_AWB is an RGB field AWB statistics white point luminance lower limit register.

Offset Address	Register Name	Total Reset Value
0x20744	STATISTICS_BLACK_LEVEL_AWB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						black_level_awb									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	black_level_awb	Luminance data lower limit for the white points of RGB field AWB statistics

STATISTICS_CR_REF_MAX_AWB

STATISTICS_CR_REF_MAX_AWB is an RGB field AWB statistics white point chrominance R/G upper limit register.

Offset Address	Register Name	Total Reset Value
0x20748	STATISTICS_CR_REF_MAX_AWB	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_max_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_max_awb	Chrominance R/G upper limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CR_REF_MIN_AWB

STATISTICS_CR_REF_MIN_AWB is an RGB field AWB statistics white point chrominance R/G lower limit register.

Offset Address	Register Name	Total Reset Value
0x2074C	STATISTICS_CR_REF_MIN_AWB	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_min_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_min_awb	Chrominance R/G lower limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_REF_MAX_AWB

STATISTICS_CB_REF_MAX_AWB is an RGB field AWB statistics white point chrominance B/G upper limit register.

Offset Address	Register Name	Total Reset Value
0x20750	STATISTICS_CB_REF_MAX_AWB	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_max_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	cb_ref_max_awb	Chrominance B/G upper limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_REF_MIN_AWB

STATISTICS_CB_REF_MIN_AWB is an RGB field AWB statistics white point chrominance B/G lower limit register.

Offset Address	Register Name	Total Reset Value
0x20754	STATISTICS_CB_REF_MIN_AWB	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_min_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cb_ref_min_awb	Chrominance B/G lower limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_AWB_RG

STATISTICS_AWB_RG is an RGB field AWB statistics G/R average value register.

Offset Address	Register Name	Total Reset Value
0x20758	STATISTICS_AWB_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				awb_rg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	awb_rg	G/R average value of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_AWB_BG

STATISTICS_AWB_BG is an RGB field AWB statistics G/B average value register.

Offset Address	Register Name	Total Reset Value
0x2075C	STATISTICS_AWB_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				awb_bg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	awb_bg	G/B average value of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_AWB_SUM

STATISTICS_AWB_SUM is an RGB field AWB statistics white point quantity register.

Offset Address	Register Name	Total Reset Value
0x20760	STATISTICS_AWB_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	awb_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	awb_sum	Number of white points for RGB field AWB statistics, 32-bit integer

STATISTICS_AWB_STATS_MODE

STATISTICS_AWB_STATS_MODE is an RGB field AWB statistics output mode selection register.

Offset Address	Register Name	Total Reset Value
0x20768	STATISTICS_AWB_STATS_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															awb_stats_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	awb_stats_mode	Output mode select for RGB field AWB statistics 0: legacy (G/R, B/R) 1: current (R/G, B/G)

STATISTICS_AWB_NODES_USED

STATISTICS_AWB_NODES_USED is an RGB field AWB statistics zone quantity register.

Offset Address	Register Name	Total Reset Value
0x20770	STATISTICS_AWB_NODES_USED	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																awb_nodes_used_vert								awb_nodes_used_horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	awb_nodes_used_vert	Number of AWB vertical regions
[7:0]	RW	awb_nodes_used_horiz	Number of AWB horizontal regions

STATISTICS_CR_REF_HIGH_AWB

STATISTICS_CR_REF_HIGH_AWB is an RGB field AWB statistics white point chrominance R/G hexagon upper limit register.

Offset Address	Register Name	Total Reset Value
0x20780	STATISTICS_CR_REF_HIGH_AWB	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_high_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_high_awb	Chrominance R/G hexagon upper limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CR_REF_LOW_AWB

STATISTICS_CR_REF_LOW_AWB is an RGB field AWB statistics white point chrominance R/G hexagon lower limit register.

Offset Address	Register Name	Total Reset Value
0x20784	STATISTICS_CR_REF_LOW_AWB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cr_ref_low_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_low_awb	Chrominance R/G hexagon lower limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_REF_HIGH_AWB

STATISTICS_CB_REF_HIGH_AWB is an RGB field AWB statistics white point chrominance B/G hexagon upper limit register.

Offset Address	Register Name	Total Reset Value
0x20788	STATISTICS_CB_REF_HIGH_AWB	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_high_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	cb_ref_high_awb	Chrominance B/G hexagon upper limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_REF_LOW_AWB

STATISTICS_CB_REF_LOW_AWB is an RGB field AWB statistics white point chrominance B/G hexagon lower limit register.

Offset Address	Register Name	Total Reset Value
0x2078C	STATISTICS_CB_REF_LOW_AWB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cb_ref_low_awb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	cb_ref_low_awb	Chrominance B/G hexagon lower limit for the white points of RGB field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_PLANE_TOTAL_0

STATISTICS_PLANE_TOTAL_0 is plane processed pixel quantity register 0.

Offset Address	Register Name	Total Reset Value
0x207A0	STATISTICS_PLANE_TOTAL_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_total_0																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_0	Number of pixels processed by plane 0

STATISTICS_PLANE_TOTAL_1

STATISTICS_PLANE_TOTAL_1 is plane processed pixel quantity register 1.

Offset Address	Register Name	Total Reset Value
0x207A4	STATISTICS_PLANE_TOTAL_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																plane_total_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_1	Number of pixels processed by plane 1

STATISTICS_PLANE_TOTAL_2

STATISTICS_PLANE_TOTAL_2 is plane processed pixel quantity register 2.

Offset Address	Register Name	Total Reset Value
0x207A8	STATISTICS_PLANE_TOTAL_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																plane_total_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_2	Number of pixels processed by plane 2

STATISTICS_PLANE_TOTAL_3

STATISTICS_PLANE_TOTAL_3 is plane processed pixel quantity register 3.

Offset Address	Register Name	Total Reset Value
0x207AC	STATISTICS_PLANE_TOTAL_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																plane_total_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_3	Number of pixels processed by plane 3

STATISTICS_PLANE_COUNTED_0

STATISTICS_PLANE_COUNTED_0 is plane pixel cumulative sum register 0.

Offset Address	Register Name	Total Reset Value
0x207B0	STATISTICS_PLANE_COUNTED_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_counted_0																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_0	Cumulative sum of plane 0 pixels

STATISTICS_PLANE_COUNTED_1

STATISTICS_PLANE_COUNTED_1 is plane pixel cumulative sum register 1.

Offset Address	Register Name	Total Reset Value
0x207B4	STATISTICS_PLANE_COUNTED_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_counted_1																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_1	Cumulative sum of plane 1 pixels

STATISTICS_PLANE_COUNTED_2

STATISTICS_PLANE_COUNTED_2 is plane pixel cumulative sum register 2.

Offset Address	Register Name	Total Reset Value
0x207B8	STATISTICS_PLANE_COUNTED_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_counted_2																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:0]	RO	plane_counted_2	Cumulative sum of plane 2 pixels

STATISTICS_PLANE_COUNTED_3

STATISTICS_PLANE_COUNTED_3 is plane pixel cumulative sum register 3.

Offset Address	Register Name	Total Reset Value
0x207BC	STATISTICS_PLANE_COUNTED_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								plane_counted_3																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_3	Cumulative sum of plane 3 pixels

STATISTICS_HISTOGRAM_CTRL

STATISTICS_HISTOGRAM_CTRL is a histogram control register.

Offset Address	Register Name	Total Reset Value
0x207C0	STATISTICS_HISTOGRAM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					plane_mode	offsety	skipy					offsetx	skipx		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved

[10:8]	RW	plane_mode	Split mode select 000: All planes are collected and placed in one histogram. 001: The four collected Bayer planes are placed in four independent banks respectively. 010: reserved 011: reserved 100: The collected planes with the odd horizontal and vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 101: The collected planes with the even horizontal coordinates and odd vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 110: The collected planes with the odd horizontal coordinates and even vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 111: The collected planes with the even horizontal and vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1.
[7]	RW	offsety	Start line select 0: line 1 1: line 2
[6:4]	RW	skipy	Histogram extraction interval in the vertical direction 000: every pixel 001: every two pixels 010: every three pixels 011: every four pixels 100: every five pixels 101: every eight pixels Other values: every nine pixels
[3]	RW	offsetx	Start column select 0: column 1 1: column 2
[2:0]	RW	skipx	Histogram extraction interval in the horizontal direction 000: every two pixels 001: every three pixels 010: every four pixels 011: every five pixels 100: every eight pixels Other values: every nine pixels

STATISTICS_SCALE

STATISTICS_SCALE is a scaling control register.

Offset Address	Register Name	Total Reset Value
0x207C4	STATISTICS_SCALE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						scale_top	scale_bottom
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	scale_top	Top scaling ratio 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved
[3:0]	RW	scale_bottom	Bottom scaling ratio 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved

STATISTICS_TOTAL_PIXELS

STATISTICS_TOTAL_PIXELS is a statistics processed pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x207C8	STATISTICS_TOTAL_PIXELS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	total_pixels							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_pixels	Number of processed pixels (the skipped x and y are also counted)

STATISTICS_COUNTED_PIXELS

STATISTICS_COUNTED_PIXELS is a statistics accumulated pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x207CC	STATISTICS_COUNTED_PIXELS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	counted_pixels							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	counted_pixels	Number of accumulated pixels (non-zero weight)

STATISTICS_PE_HISTOGRAM_CTRL

STATISTICS_PE_HISTOGRAM_CTRL is a PE control register.

Offset Address	Register Name	Total Reset Value
0x207D0	STATISTICS_PE_HISTOGRAM_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					plane_mode_pe	offset_y_pe / skip_y_pe	offset_x_pe / skip_x_pe
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved

[10:8]	RW	plane_mode_pe	Split mode select 000: All planes are collected and placed in one histogram. 001: The four collected Bayer planes are placed in four independent banks respectively. 010: reserved 011: reserved 100: The collected planes with the odd horizontal and vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 101: The collected planes with the even horizontal coordinates and odd vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 110: The collected planes with the odd horizontal coordinates and even vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1. 111: The collected planes with the even horizontal and vertical coordinates are placed in bank 0, and the remaining planes are placed in bank 1.
[7]	RW	offset_y_pe	Start line select 0: line 1 1: line 2
[6:4]	RW	skip_y_pe	Histogram extraction interval in the vertical direction 000: every pixel 001: every two pixels 010: every three pixels 011: every four pixels 100: every five pixels 101: every eight pixels Other values: every nine pixels
[3]	RW	offset_x_pe	Start column select 0: column 1 1: column 2
[2:0]	RW	skip_x_pe	Histogram extraction interval in the horizontal direction 000: every two pixels 001: every three pixels 010: every four pixels 011: every five pixels 100: every eight pixels Other values: every nine pixels

STATISTICS_PE_SCALE

STATISTICS_PE_SCALE is a PE scaling control register.

Offset Address	Register Name	Total Reset Value
0x207D4	STATISTICS_PE_SCALE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								scale_top_pe				scale_bottom_pe			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	scale_top_pe	Top scaling ratio 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved
[3:0]	RW	scale_bottom_pe	Bottom scaling ratio 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved

STATISTICS_PE_TOTAL_PIXELS

STATISTICS_PE_TOTAL_PIXELS is a PE processed pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x207D8	STATISTICS_PE_TOTAL_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_pixels_pe																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_pixels_pe	Number of processed pixels (the skipped x and y are also counted)

STATISTICS_PE_COUNTED_PIXELS

STATISTICS_PE_COUNTED_PIXELS is a PE accumulated pixel quantity register.

Offset Address	Register Name	Total Reset Value
0x207DC	STATISTICS_PE_COUNTED_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	counted_pixels_pe																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	counted_pixels_pe	Number of accumulated pixels (non-zero weight)

STATISTICS_PLANE_TOTAL_PE_0

STATISTICS_PLANE_TOTAL_PE_0 is PE plane processed pixel quantity register 0.

Offset Address	Register Name	Total Reset Value
0x207E0	STATISTICS_PLANE_TOTAL_PE_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_total_pe_0																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_pe_0	Number of pixels processed by each plane

STATISTICS_PLANE_TOTAL_PE_1

STATISTICS_PLANE_TOTAL_PE_1 is PE plane processed pixel quantity register 1.

Offset Address	Register Name	Total Reset Value
0x207E4	STATISTICS_PLANE_TOTAL_PE_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_total_pe_1																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_pe_1	Number of pixels processed by each plane

STATISTICS_PLANE_TOTAL_PE_2

STATISTICS_PLANE_TOTAL_PE_2 is PE plane processed pixel quantity register 2.

Offset Address	Register Name	Total Reset Value
0x207E8	STATISTICS_PLANE_TOTAL_PE_2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	plane_total_pe_2						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_pe_2	Number of pixels processed by each plane

STATISTICS_PLANE_TOTAL_PE_3

STATISTICS_PLANE_TOTAL_PE_3 is PE plane processed pixel quantity register 3.

Offset Address	Register Name	Total Reset Value
0x207EC	STATISTICS_PLANE_TOTAL_PE_3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	plane_total_pe_3						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_total_pe_3	Number of pixels processed by each plane

STATISTICS_PLANE_COUNTED_PE_0

STATISTICS_PLANE_COUNTED_PE_0 is PE plane pixel cumulative sum register 0.

Offset Address	Register Name	Total Reset Value
0x207F0	STATISTICS_PLANE_COUNTED_PE_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_counted_pe_0																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_pe_0	Cumulative sum of pixels on each plane

STATISTICS_PLANE_COUNTED_PE_1

STATISTICS_PLANE_COUNTED_PE_1 is PE plane pixel cumulative sum register 1.

Offset Address	Register Name	Total Reset Value
0x207F4	STATISTICS_PLANE_COUNTED_PE_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plane_counted_pe_1																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_pe_1	Cumulative sum of pixels on each plane

STATISTICS_PLANE_COUNTED_PE_2

STATISTICS_PLANE_COUNTED_PE_2 is PE plane pixel cumulative sum register 2.

Offset Address	Register Name	Total Reset Value
0x207F8	STATISTICS_PLANE_COUNTED_PE_2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	plane_counted_pe_2						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_pe_2	Cumulative sum of pixels on each plane

STATISTICS_PLANE_COUNTED_PE_3

STATISTICS_PLANE_COUNTED_PE_3 is PE plane pixel cumulative sum register 3.

Offset Address	Register Name	Total Reset Value
0x207FC	STATISTICS_PLANE_COUNTED_PE_3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	plane_counted_pe_3						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RO	plane_counted_pe_3	Cumulative sum of pixels on each plane

STATISTICS_SUM_R

STATISTICS_SUM_R is a normalized R component pixel sum register.

Offset Address	Register Name	Total Reset Value
0x20800	STATISTICS_SUM_R	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				sum_r			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RO	sum_r	Normalized R component pixel sum

STATISTICS_SUM_RG

STATISTICS_SUM_RG is a normalized Gr component pixel sum register.

Offset Address	Register Name	Total Reset Value
0x20804	STATISTICS_SUM_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sum_rg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sum_rg	Normalized Gr component pixel sum

STATISTICS_SUM_BG

STATISTICS_SUM_BG is a normalized Gb component pixel sum register.

Offset Address	Register Name	Total Reset Value
0x20808	STATISTICS_SUM_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sum_bg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sum_bg	Normalized Gb component pixel sum

STATISTICS_SUM_B

STATISTICS_SUM_B is a normalized B component pixel sum register.

Offset Address	Register Name	Total Reset Value
0x2080C	STATISTICS_SUM_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sum_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sum_b	Normalized B component pixel sum

STATISTICS_AE_SUM_NODES_USED

STATISTICS_AE_SUM_NODES_USED is an AE_SUM active region register.

Offset Address	Register Name	Total Reset Value
0x20810	STATISTICS_AE_SUM_NODES_USED	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ae_sum_nodes_used_vert								ae_sum_nodes_used_horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	ae_sum_nodes_used_vert	Number of vertical active regions
[7:0]	RW	ae_sum_nodes_used_horiz	Number of horizontal active regions

STATISTICS_AVG_R

STATISTICS_AVG_R is a Bayer field AWB sum statistics R component average value register.

Offset Address	Register Name	Total Reset Value
0x20820	STATISTICS_AVG_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avg_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	avg_r	Average value of the R component for Bayer field AWB sum statistics

STATISTICS_AVG_G

STATISTICS_AVG_G is a Bayer field AWB sum statistics G component average value register.

Offset Address	Register Name	Total Reset Value
0x20824	STATISTICS_AVG_G	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avg_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	avg_g	Average value of the G component for Bayer field AWB sum statistics

STATISTICS_AVG_B

STATISTICS_AVG_B is a Bayer field AWB sum statistics B component average value register.

Offset Address	Register Name	Total Reset Value
0x20828	STATISTICS_AVG_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avg_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RO	avg_b	Average value of the B component for Bayer field AWB sum statistics

STATISTICS_COUNT_ALL

STATISTICS_COUNT_ALL is a Bayer field AWB sum statistics normalized pixel quantity register for pixels that meet the white point conditions.

Offset Address	Register Name	Total Reset Value
0x2082C	STATISTICS_COUNT_ALL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																count_all															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	count_all	Number of pixels that meet the white point conditions (for Bayer field AWB sum statistics)

STATISTICS_COUNT_MIN

STATISTICS_COUNT_MIN is a Bayer field AWB sum statistics pixel quantity register for pixels below the luminance lower limit.

Offset Address	Register Name	Total Reset Value
0x20830	STATISTICS_COUNT_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																count_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	count_min	Number of pixels below the luminance lower limit (for Bayer field AWB sum statistics)

STATISTICS_COUNT_MAX

STATISTICS_COUNT_MAX is a Bayer field AWB sum statistics pixel quantity register for pixels above the luminance upper limit.

Offset Address	Register Name	Total Reset Value
0x20834	STATISTICS_COUNT_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																count_max															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	count_max	Number of pixels above the luminance upper limit (for Bayer field AWB sum statistics)

STATISTICS_AWB_SUM_NODES_USED

STATISTICS_AWB_SUM_NODES_USED is an AWB_SUM active region register.

Offset Address	Register Name	Total Reset Value
0x20838	STATISTICS_AWB_SUM_NODES_USED	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																awb_sum_nodes_used_vert								awb_sum_nodes_used_horiz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	awb_sum_nodes_used_vert	Number of vertical active regions
[7:0]	RW	awb_sum_nodes_used_horiz	Number of horizontal active regions

STATISTICS_MIN_THRESHOLD

STATISTICS_MIN_THRESHOLD is a Bayer field AWB sum statistics white point luminance lower limit register.

Offset Address	Register Name	Total Reset Value
0x2083C	STATISTICS_MIN_THRESHOLD	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				min_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	min_threshold	Luminance lower limit for the white points of Bayer field AWB sum statistics

STATISTICS_MAX_THRESHOLD

STATISTICS_MAX_THRESHOLD is a Bayer field AWB sum statistics white point luminance upper limit register.

Offset Address	Register Name	Total Reset Value
0x20840	STATISTICS_MAX_THRESHOLD	0x0000_0FF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_threshold	Luminance upper limit for the white points of Bayer field AWB sum statistics

STATISTICS_AWB_SUM_CLIP

STATISTICS_AWB_SUM_CLIP is an AWB sum clipping register.

Offset Address	Register Name	Total Reset Value
0x20844	STATISTICS_AWB_SUM_CLIP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								max_clip	min_clip
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	max_clip	Upper threshold clipping for the AWB sum
[0]	RW	min_clip	Lower threshold clipping for the AWB sum

STATISTICS_CR_REF

STATISTICS_CR_REF is a Bayer field AWB statistics white point chrominance R/G upper/lower limit register.

Offset Address	Register Name	Total Reset Value
0x20848	STATISTICS_CR_REF	0x0040_01FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cr_ref_min_awb_sum			reserved	cr_ref_max_awb_sum		
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cr_ref_min_awb_sum	Chrominance R/G lower limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_max_awb_sum	Chrominance R/G upper limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_REF

STATISTICS_CB_REF is a Bayer field AWB statistics white point chrominance B/G upper/lower limit register.

Offset Address	Register Name	Total Reset Value
0x2084C	STATISTICS_CB_REF	0x0040_01FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cb_ref_min_awb_sum			reserved	cb_ref_max_awb_sum		
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cb_ref_min_awb_sum	Chrominance B/G lower limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	cb_ref_max_awb_sum	Chrominance B/G upper limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CR_HL_REF

STATISTICS_CR_HL_REF is a Bayer field AWB statistics white point chrominance R/G hexagon limit register.

Offset Address	Register Name	Total Reset Value
0x20850	STATISTICS_CR_HL_REF	0x0000_0FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cr_ref_low_awb_sum			reserved	cr_ref_high_awb_sum		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cr_ref_low_awb_sum	Chrominance R/G hexagon lower limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_high_awb_sum	Chrominance R/G hexagon upper limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number

STATISTICS_CB_HL_REF

STATISTICS_CB_HL_REF is a Bayer field AWB statistics white point chrominance B/G hexagon limit register.

Offset Address	Register Name	Total Reset Value
0x20854	STATISTICS_CB_HL_REF	0x0000_0FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cb_ref_low_awb_sum			reserved	cb_ref_high_awb_sum		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cb_ref_low_awb_sum	Chrominance B/G hexagon lower limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number
[15:12]	RO	reserved	Reserved
[11:0]	RW	cb_ref_high_awb_sum	Chrominance B/G hexagon upper limit for the white points of Bayer field AWB statistics, 4.8-bit unsigned fixed-point number

FRAME_STATS_ACTIVE_WIDTH_MIN

FRAME_STATS_ACTIVE_WIDTH_MIN is a minimum width register.

Offset Address	Register Name	Total Reset Value
0x20910	FRAME_STATS_ACTIVE_WIDTH_MIN	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	active_width_min							
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:0]	RO	active_width_min	Minimum width

FRAME_STATS_ACTIVE_WIDTH_MAX

FRAME_STATS_ACTIVE_WIDTH_MAX is a maximum width register.

Offset Address	Register Name	Total Reset Value
0x20914	FRAME_STATS_ACTIVE_WIDTH_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_width_max	Maximum width

FRAME_STATS_ACTIVE_WIDTH_SUM

FRAME_STATS_ACTIVE_WIDTH_SUM is an active width sum register.

Offset Address	Register Name	Total Reset Value
0x20918	FRAME_STATS_ACTIVE_WIDTH_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_width_sum	Active width sum

FRAME_STATS_ACTIVE_WIDTH_NUM

FRAME_STATS_ACTIVE_WIDTH_NUM is an active width register.

Offset Address	Register Name	Total Reset Value
0x2091C	FRAME_STATS_ACTIVE_WIDTH_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_width_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_width_num	Active width

FRAME_STATS_ACTIVE_HEIGHT_MIN

FRAME_STATS_ACTIVE_HEIGHT_MIN is a minimum height register.

Offset Address	Register Name	Total Reset Value
0x20920	FRAME_STATS_ACTIVE_HEIGHT_MIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_height_min																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	active_height_min	Minimum height

FRAME_STATS_ACTIVE_HEIGHT_MAX

FRAME_STATS_ACTIVE_HEIGHT_MAX is a maximum height register.

Offset Address	Register Name	Total Reset Value
0x20924	FRAME_STATS_ACTIVE_HEIGHT_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_height_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_height_max	Maximum height

FRAME_STATS_ACTIVE_HEIGHT_SUM

FRAME_STATS_ACTIVE_HEIGHT_SUM is an active height sum register.

Offset Address	Register Name	Total Reset Value
0x20928	FRAME_STATS_ACTIVE_HEIGHT_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_height_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_height_sum	Active height sum

FRAME_STATS_ACTIVE_HEIGHT_NUM

FRAME_STATS_ACTIVE_HEIGHT_NUM is an active height register.

Offset Address	Register Name	Total Reset Value
0x2092C	FRAME_STATS_ACTIVE_HEIGHT_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	active_height_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	active_height_num	Active height

FRAME_STATS_HBLANK_MIN

FRAME_STATS_HBLANK_MIN is a minimum horizontal blanking register.

Offset Address	Register Name	Total Reset Value
0x20930	FRAME_STATS_HBLANK_MIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_min																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	hblank_min	Minimum horizontal blanking

FRAME_STATS_HBLANK_MAX

FRAME_STATS_HBLANK_MAX is a maximum horizontal blanking register.

Offset Address	Register Name	Total Reset Value
0x20934	FRAME_STATS_HBLANK_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hblank_max	Maximum horizontal blanking

FRAME_STATS_HBLANK_SUM

FRAME_STATS_HBLANK_SUM is a horizontal blanking sum register.

Offset Address	Register Name	Total Reset Value
0x20938	FRAME_STATS_HBLANK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hblank_sum	Horizontal blanking sum

FRAME_STATS_HBLANK_NUM

FRAME_STATS_HBLANK_NUM is a horizontal blanking register.

Offset Address	Register Name	Total Reset Value
0x2093C	FRAME_STATS_HBLANK_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hblank_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hblank_num	Horizontal blanking

FRAME_STATS_VBLANK_MIN

FRAME_STATS_VBLANK_MIN is a minimum vertical blanking register.

Offset Address	Register Name	Total Reset Value
0x20940	FRAME_STATS_VBLANK_MIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_min																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	vblank_min	Minimum vertical blanking

FRAME_STATS_VBLANK_MAX

FRAME_STATS_VBLANK_MAX is a maximum vertical blanking register.

Offset Address	Register Name	Total Reset Value
0x20944	FRAME_STATS_VBLANK_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_max																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	vblank_max	Maximum vertical blanking

FRAME_STATS_VBLANK_SUM

FRAME_STATS_VBLANK_SUM is a vertical blanking sum register.

Offset Address	Register Name	Total Reset Value
0x20948	FRAME_STATS_VBLANK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	vblank_sum	Vertical blanking sum

FRAME_STATS_VBLANK_NUM

FRAME_STATS_VBLANK_NUM is a vertical blanking register.

Offset Address	Register Name	Total Reset Value
0x2094C	FRAME_STATS_VBLANK_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vblank_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	vblank_num	Vertical blanking

NOISE_PROFILE_WDR_4

NOISE_PROFILE_WDR_4 is a WDR 4 noise offset register.

Offset Address	Register Name	Total Reset Value
0x21004	NOISE_PROFILE_WDR_4	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								long_noise_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:0]	RW	long_noise_offset	Noise offset, 5.4-bit unsigned floating-point number

NOISE_PROFILE_WDR_3

NOISE_PROFILE_WDR_3 is a WDR 3 noise offset register.

Offset Address	Register Name	Total Reset Value
0x21014	NOISE_PROFILE_WDR_3	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								med1_noise_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:0]	RW	med1_noise_offset	Noise offset, 5.4-bit unsigned floating-point number

NOISE_PROFILE_WDR_2

NOISE_PROFILE_WDR_2 is a WDR 2 noise offset register.

Offset Address	Register Name	Total Reset Value
0x21024	NOISE_PROFILE_WDR_2	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								med2_noise_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved

[8:0]	RW	med2_noise_offset	Noise offset, 5.4-bit unsigned floating-point number

NOISE_PROFILE_WDR_1

NOISE_PROFILE_WDR_1 is a WDR 1 noise offset register.

Offset Address	Register Name	Total Reset Value
0x21034	NOISE_PROFILE_WDR_1	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								short_noise_offset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:0]	RW	short_noise_offset	Noise offset, 5.4-bit unsigned floating-point number

NOISE_PROFILE_FRAME_STITCH_LUT_1

NOISE_PROFILE_FRAME_STITCH_LUT_1 is a FRAME_STITCH noise distribution table 1 register.

Offset Address	Register Name	Total Reset Value
0x21200−0x2127C	NOISE_PROFILE_FRAME_STITCH_LUT_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight_lut_3								weight_lut_2								weight_lut_1								weight_lut_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_FRAME_STITCH_LUT_2

NOISE_PROFILE_FRAME_STITCH_LUT_2 is a FRAME_STITCH noise distribution table 2 register.

Offset Address	Register Name	Total Reset Value
0x21280−0x212FC	NOISE_PROFILE_FRAME_STITCH_LUT_2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight_lut_3		weight_lut_2		weight_lut_1		weight_lut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_FRAME_STITCH_LUT_3

NOISE_PROFILE_FRAME_STITCH_LUT_3 is a FRAME_STITCH noise distribution table 3 register.

Offset Address	Register Name	Total Reset Value
0x21300−0x2137C	NOISE_PROFILE_FRAME_STITCH_LUT_3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight_lut_3		weight_lut_2		weight_lut_1		weight_lut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_FRAME_STITCH_LUT_4

NOISE_PROFILE_FRAME_STITCH_LUT_4 is a FRAME_STITCH noise distribution table 4 register.

Offset Address	Register Name	Total Reset Value
0x21380−0x213FC	NOISE_PROFILE_FRAME_STITCH_LUT_4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight_lut_3								weight_lut_2								weight_lut_1								weight_lut_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

DNR_SHADING

DNR_SHADING is a radial LUT 0 register.

Offset Address	Register Name	Total Reset Value
0x21540−0x2155C	DNR_SHADING	0x1010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rm_shading_lut_3								rm_shading_lut_2								rm_shading_lut_1								rm_shading_lut_0							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rm_shading_lut_3	Radial LUT data 3 (33 data segments in total)
[23:16]	RW	rm_shading_lut_2	Radial LUT data 2 (33 data segments in total)
[15:8]	RW	rm_shading_lut_1	Radial LUT data 1 (33 data segments in total)
[7:0]	RW	rm_shading_lut_0	Radial LUT data 0 (33 data segments in total)

DNR_SHADING_LAST

DNR_SHADING_LAST is a radial LUT 1 register.

Offset Address	Register Name	Total Reset Value
0x21560	DNR_SHADING_LAST	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rm_shading_lut_32							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	rm_shading_lut_32	Radial LUT data 32 (last one of the 33 data segments)

NOISE_PROFILE_RAW_FRONTEND_LUT_1

NOISE_PROFILE_RAW_FRONTEND_LUT_1 is a RAW_FRONTEND noise distribution table 1 register.

Offset Address	Register Name	Total Reset Value
0x21580−0x215FC	NOISE_PROFILE_RAW_FRONTEND_LUT_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight_lut_3								weight_lut_2								weight_lut_1								weight_lut_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_RAW_FRONTEND_LUT_2

NOISE_PROFILE_RAW_FRONTEND_LUT_2 is a RAW_FRONTEND noise distribution table 2 register.

Offset Address	Register Name	Total Reset Value
0x21600−0x2167C	NOISE_PROFILE_RAW_FRONTEND_LUT_2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight_lut_3		weight_lut_2		weight_lut_1		weight_lut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_RAW_FRONTEND_LUT_3

NOISE_PROFILE_RAW_FRONTEND_LUT_3 is a RAW_FRONTEND noise distribution table 3 register.

Offset Address	Register Name	Total Reset Value
0x21680−0x216FC	NOISE_PROFILE_RAW_FRONTEND_LUT_3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight_lut_3		weight_lut_2		weight_lut_1		weight_lut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_RAW_FRONTEND_LUT_4

NOISE_PROFILE_RAW_FRONTEND_LUT_4 is a RAW_FRONTEND noise distribution table 4 register.

Offset Address	Register Name	Total Reset Value
0x21700−0x2177C	NOISE_PROFILE_RAW_FRONTEND_LUT_4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight_lut_3		weight_lut_2		weight_lut_1		weight_lut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weight_lut_3	Noise distribution weight 3, calculated during the calibration
[23:16]	RW	weight_lut_2	Noise distribution weight 2, calculated during the calibration
[15:8]	RW	weight_lut_1	Noise distribution weight 1, calculated during the calibration
[7:0]	RW	weight_lut_0	Noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_LUT

NOISE_PROFILE_LUT is a DNR noise distribution table register.

Offset Address	Register Name	Total Reset Value
0x21800−0x2187C	NOISE_PROFILE_LUT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weightlut_3		weightlut_2		weightlut_1		weightlut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3	DNR noise distribution weight 3, calculated during the calibration
[23:16]	RW	weightlut_2	DNR noise distribution weight 2, calculated during the calibration
[15:8]	RW	weightlut_1	DNR noise distribution weight 1, calculated during the calibration
[7:0]	RW	weightlut_0	DNR noise distribution weight 0, calculated during the calibration

NOISE_PROFILE_DEMOSAIC_LUT

NOISE_PROFILE_DEMOSAIC_LUT is a demosaic noise distribution table register.

Offset Address	Register Name	Total Reset Value
0x21880–0x218FC	NOISE_PROFILE_DEMOSAIC_LUT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weightlut_3		weightlut_2		weightlut_1		weightlut_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	weightlut_3	Demosaic noise distribution weight 3
[23:16]	RW	weightlut_2	Demosaic noise distribution weight 2
[15:8]	RW	weightlut_1	Demosaic noise distribution weight 1
[7:0]	RW	weightlut_0	Demosaic noise distribution weight 0

AEXP_WEIGHT

AEXP_WEIGHT is an AE block weight register.

Offset Address	Register Name	Total Reset Value
0x21900–0x219F8	AEXP_WEIGHT	0x0F0F_0F0F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	aexp_weight0_3	reserved	aexp_weight0_2	reserved	aexp_weight0_1	reserved	aexp_weight0_0
Reset	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	aexp_weight0_3	AE block weight 0_3
[23:20]	RO	reserved	Reserved
[19:16]	RW	aexp_weight0_2	AE block weight 0_2
[15:12]	RO	reserved	Reserved
[11:8]	RW	aexp_weight0_1	AE block weight 0_1
[7:4]	RO	reserved	Reserved
[3:0]	RW	aexp_weight0_0	AE block weight 0_0

AEXP_WEIGHT_LAST

AEXP_WEIGHT_LAST is an AE last block weight register.

Offset Address	Register Name	Total Reset Value
0x219FC	AEXP_WEIGHT_LAST	0x000F_0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												aexp_weight16_14				reserved				aexp_weight16_13				reserved				aexp_weight16_12			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	aexp_weight16_14	AE block weight 16_14
[15:12]	RO	reserved	Reserved
[11:8]	RW	aexp_weight16_13	AE block weight 16_13
[7:4]	RO	reserved	Reserved
[3:0]	RW	aexp_weight16_12	AE block weight 16_12

AWB_WEIGHT

AWB_WEIGHT is an AWB block weight register.

Offset Address	Register Name	Total Reset Value
0x21B00–0x21EFC	AWB_WEIGHT	0x0F0F_0F0F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				awb_weight0_3				reserved				awb_weight0_2				reserved				awb_weight0_1				reserved				awb_weight0_0			
Reset	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	awb_weight0_3	AWB block weight 0_3
[23:20]	RO	reserved	Reserved
[19:16]	RW	awb_weight0_2	AWB block weight 0_2
[15:12]	RO	reserved	Reserved
[11:8]	RW	awb_weight0_1	AWB block weight 0_1
[7:4]	RO	reserved	Reserved
[3:0]	RW	awb_weight0_0	AWB block weight 0_0

GAMMA_FE0_MEM0

GAMMA_FE0_MEM0 is a GAMMA_FE0 bank 0 lookup table register.

Offset Address	Register Name	Total Reset Value
0x22800–0x22880	GAMMA_FE0_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_FE0 bank 0 lookup table

GAMMA_FE0_MEM1

GAMMA_FE0_MEM1 is a GAMMA_FE0 bank 1 lookup table register.

Offset Address	Register Name	Total Reset Value
0x22900–0x22980	GAMMA_FE0_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_FE0 bank 1 lookup table

GAMMA_FE1_MEM0

GAMMA_FE1_MEM0 is a GAMMA_FE1 bank 0 lookup table register.

Offset Address	Register Name	Total Reset Value
0x23000–0x23400	GAMMA_FE1_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19:0]	RW	data0	GAMMA_FE1 bank 0 lookup table

GAMMA_FE1_MEM1

GAMMA_FE1_MEM1 is a GAMMA_FE1 bank 1 lookup table register.

Offset Address	Register Name	Total Reset Value
0x23800−0x23C00	GAMMA_FE1_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_FE1 bank 1 lookup table

GAMMA_BE0_MEM0

GAMMA_BE0_MEM0 is a GAMMA_BE0 bank 0 lookup table register.

Offset Address	Register Name	Total Reset Value
0x24800−0x24880	GAMMA_BE0_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_BE0 bank 0 lookup table

GAMMA_BE0_MEM1

GAMMA_BE0_MEM1 is a GAMMA_BE0 bank 1 lookup table register.

Offset Address	Register Name	Total Reset Value
0x24900–0x24980	GAMMA_BE0_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_BE0 bank 1 lookup table

GAMMA_BE1_MEM0

GAMMA_BE1_MEM0 is a GAMMA_BE1 bank 0 lookup table register.

Offset Address	Register Name	Total Reset Value
0x25000–0x25400	GAMMA_BE1_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_BE1 bank 0 lookup table

GAMMA_BE1_MEM1

GAMMA_BE1_MEM1 is a GAMMA_BE1 bank 1 lookup table register.

Offset Address	Register Name	Total Reset Value
0x25800–0x25C00	GAMMA_BE1_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	GAMMA_BE1 bank 1 lookup table

RADIAL_SHADING_MEM_R

RADIAL_SHADING_MEM_R is a RADIAL_SHADING R component lookup table register.

Offset Address	Register Name	Total Reset Value
0x26000–0x26200	RADIAL_SHADING_MEM_R	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	data0	RADIAL_SHADING R component lookup table

RADIAL_SHADING_MEM_G

RADIAL_SHADING_MEM_G is a RADIAL_SHADING G component lookup table register.

Offset Address	Register Name	Total Reset Value
0x26400–0x26600	RADIAL_SHADING_MEM_G	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	data0	RADIAL_SHADING G component lookup table

RADIAL_SHADING_MEM_B

RADIAL_SHADING_MEM_B is a RADIAL_SHADING B component lookup table register.

Offset Address	Register Name	Total Reset Value
0x26800–0x26A00	RADIAL_SHADING_MEM_B	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	data0	RADIAL_SHADING B component lookup table

METERING_MEM

METERING_MEM is an AE/AWB (sum) statistics register.

Offset Address	Register Name	Total Reset Value
0x28000–0x2DFFC	METERING_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data0	AE/AWB (sum) statistics

DEFECT_PIXEL_MEM

DEFECT_PIXEL_MEM is a static defect pixel table register.

Offset Address	Register Name	Total Reset Value
0x30000–0x33FFC	DEFECT_PIXEL_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								data0																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:0]	RW	data0	Static defect pixel table

HISTOGRAM1_MEM

HISTOGRAM1_MEM is histogram statistics register 1.

Offset Address	Register Name	Total Reset Value
0x34000–0x34FFC	HISTOGRAM1_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data0	Histogram statistics

HISTOGRAM2_MEM

HISTOGRAM2_MEM is histogram statistics register 2.

Offset Address	Register Name	Total Reset Value
0x35000–0x353FC	HISTOGRAM2_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data0	Histogram statistics

HISTOGRAM3_MEM

HISTOGRAM3_MEM is histogram statistics register 3.

Offset Address	Register Name	Total Reset Value
0x35400–0x357FC	HISTOGRAM3_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data0	Histogram statistics

HISTOGRAM4_MEM

HISTOGRAM4_MEM is histogram statistics register 4.

Offset Address	Register Name	Total Reset Value
0x35800–0x35BFC	HISTOGRAM4_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data0	Histogram statistics

GAMMA_RGB_MEM0

GAMMA_RGB_MEM0 is a GAMMA_RGB bank 0 lookup table register.

Offset Address	Register Name	Total Reset Value
0x37000–0x37400	GAMMA_RGB_MEM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				data0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	data0	257-node lookup table for GAMMA_RGB bank 0

GAMMA_RGB_MEM1

GAMMA_RGB_MEM1 is a GAMMA_RGB bank 1 lookup table register.

Offset Address	Register Name	Total Reset Value
0x37800–0x37C00	GAMMA_RGB_MEM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				data0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	data0	257-node lookup table for GAMMA_RGB bank 1

DRC_FWD_MEM

DRC_FWD_MEM is a DRC_FWD table register.

Offset Address	Register Name	Total Reset Value
0x38000–0x38200	DRC_FWD_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	DRC_FWD table

DRC_REV_MEM

DRC_REV_MEM is a DRC_REV table register.

Offset Address	Register Name	Total Reset Value
0x38800–0x38A00	DRC_REV_MEM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												data0																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	data0	DRC_REV table

CMD_QUEUES

CMD_QUEUES is a CMD table register.

Offset Address	Register Name	Total Reset Value
0x39000–0x393FC	CMD_QUEUES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data0	CMD table

SHADING_MEM

SHADING_MEM is a mesh shading table register.

Offset Address	Register Name	Total Reset Value
0x3C000–0x3EFFC	SHADING_MEM	0x4040_4040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data0																															
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data0	Mesh shading table

ISP_BE_FSTART_DELAY

ISP_BE_FSTART_DELAY is an ISP adjustable interrupt trigger time configuration register.

Offset Address	Register Name	Total Reset Value
0x40094	ISP_BE_FSTART_DELAY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delay																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	delay	Trigger time of adjustable interrupts

ISP_BE_USER_DEFINE0

ISP_BE_USER_DEFINE0 is user-defined register 0.

Offset Address	Register Name	Total Reset Value
0x400A0	ISP_BE_USER_DEFINE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	user_define0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	user_define0	User-defined register 0

ISP_BE_USER_DEFINE1

ISP_BE_USER_DEFINE1 is user-defined register 1.

Offset Address	Register Name	Total Reset Value
0x400A4	ISP_BE_USER_DEFINE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	user_define1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	user_define1	User-defined register 1

ISP_BE_INT

ISP_BE_INT is an ISP interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x400F0	ISP_BE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															acm_para_finish	reserved												fstart_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	WC	acm_para_finish	Status of the ACM LUT loading completion interrupt. Writing 1 clears this interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15:4]	RO	reserved	Reserved
[3]	WC	fstart_delay	Status of the configurable trigger delay interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[2]	WC	cfg_loss	Status of the register configuration loss interrupt. Writing 1 clears this interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears this interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the ISP SOF interrupt. Writing 1 clears this interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_BE_INT_MASK

ISP_BE_INT_MASK is an ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x400F8	ISP_BE_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															acm_para_finish	reserved												int_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	acm_para_finish	ACM LUT loading completion interrupt enable 0: masked 1: enabled
[15:4]	RO	reserved	Reserved
[3]	RW	int_delay	Configurable trigger delay interrupt enable 0: masked 1: enabled
[2]	RW	cfg_loss	Register configuration loss interrupt enable 0: masked 1: enabled

[1]	RW	update_cfg	Register update interrupt enable 0: masked 1: enabled
[0]	RW	fstart	ISP SOF interrupt enable 0: masked 1: enabled

ISP_BE_CTRL_F

ISP_BE_CTRL_F is an ISP general update control register.

Offset Address	Register Name	Total Reset Value
0x401E0	ISP_BE_CTRL_F	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rggb_cfg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	rggb_cfg	RGGB sequence 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_BE_CTRL_I

ISP_BE_CTRL_I is an ISP immediate update control register.

Offset Address	Register Name	Total Reset Value
0x401E4	ISP_BE_CTRL_I	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								update_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	ISP register update mode 0: update mode specified in ISP_BE_REG_UPDATE 1: frame update mode

ISP_BE_TIMING_CFG

ISP_BE_TIMING_CFG is an output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x401E8	ISP_BE_TIMING_CFG	0x0000_0080

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved					fix_timing			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:1]	RW	fix_timing	Manual timing parameter configuration. The length of the generated line blanking region is configured.
[0]	RO	reserved	Reserved

ISP_BE_REG_UPDATE

ISP_BE_REG_UPDATE is a register update register.

Offset Address	Register Name	Total Reset Value
0x401EC	ISP_BE_REG_UPDATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							update
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update	ISP update. This bit is automatically cleared for each frame.

ISP_CLIP_Y_CFG

ISP_CLIP_Y_CFG is a luminance clamping configuration register.

Offset Address	Register Name	Total Reset Value
0x40800	ISP_CLIP_Y_CFG	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	max				min			
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum luminance clamping value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum luminance clamping value. When the data bit width is less than 16 bits, the upper bits are valid.

ISP_CLIP_C_CFG

ISP_CLIP_C_CFG is a chrominance clamping configuration register.

Offset Address	Register Name	Total Reset Value
0x40804	ISP_CLIP_C_CFG	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	max				min			
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum chrominance clamping value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum chrominance clamping value. When the data bit width is less than 16 bits, the upper bits are valid.

ISP_SKIP_Y_CFG

ISP_SKIP_Y_CFG is a Y component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x40810	ISP_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	skip_cfg							
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration for the Y component

ISP_SKIP_C_CFG

ISP_SKIP_C_CFG is a C component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x40818	ISP_SKIP_C_CFG	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	skip_cfg							
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration for the C component

ISP_CROP_Y_CFG

ISP_CROP_Y_CFG is a Y component crop enable register.

Offset Address	Register Name	Total Reset Value
0x40860	ISP_CROP_Y_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							n0_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

ISP_CROP_Y_START

ISP_CROP_Y_START is a Y component crop start position register.

Offset Address	Register Name	Total Reset Value
0x40868	ISP_CROP_Y_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the picture starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the picture starts to be captured

ISP_CROP_Y_SIZE

ISP_CROP_Y_SIZE is a Y component crop size configuration register.

Offset Address	Register Name	Total Reset Value
0x4086C	ISP_CROP_Y_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

ISP_CROP_C_CFG

ISP_CROP_C_CFG is a C component crop enable register.

Offset Address	Register Name	Total Reset Value
0x40870	ISP_CROP_C_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

ISP_CROP_C_START

ISP_CROP_C_START is a C component crop start position register.

Offset Address	Register Name	Total Reset Value
0x40878	ISP_CROP_C_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the picture starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the picture starts to be captured

ISP_CROP_C_SIZE

ISP_CROP_C_SIZE is a C component crop size configuration register.

Offset Address	Register Name	Total Reset Value
0x4087C	ISP_CROP_C_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

ISP_Y_SUM0

ISP_Y_SUM0 is an input picture luminance statistics lower-bit register.

Offset Address	Register Name	Total Reset Value
0x40880	ISP_Y_SUM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Lower 32 bits of the luminance statistics

ISP_Y_SUM1

ISP_Y_SUM1 is an input picture luminance statistics upper-bit register.

Offset Address	Register Name	Total Reset Value
0x40884	ISP_Y_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Upper 32 bits of the luminance statistics

ISP_CSC_CFG

ISP_CSC_CFG is a CSC enable register.

Offset Address	Register Name	Total Reset Value
0x41500	ISP_CSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	CSC enable 0: disabled 1: enabled

ISP_CSC_COEF0

ISP_CSC_COEF0 is CSC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x41510	ISP_CSC_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01															reserved	coef00															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef01	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef00	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF1

ISP_CSC_COEF1 is CSC coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x41514	ISP_CSC_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10															reserved	coef02															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef10	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[16]	RO	reserved	Reserved

[15:1]	RW	coef02	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF2

ISP_CSC_COEF2 is CSC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x41518	ISP_CSC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12															reserved	coef11															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef12	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef11	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF3

ISP_CSC_COEF3 is CSC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x4151C	ISP_CSC_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21															reserved	coef20															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef21	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef20	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF4

ISP_CSC_COEF4 is CSC coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x41520	ISP_CSC_COEF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															reserved	coef22															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef22	CSC coefficient Its format is S5.10. The value is a signed number consisting of a 4-bit integral part and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_IN_DC0

ISP_CSC_IN_DC0 is CSC input DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41530	ISP_CSC_IN_DC0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	in_dc1			reserved	in_dc0			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	in_dc1	DC offset of the input G component, signed integer
[20:16]	RO	reserved	Reserved
[15:5]	RW	in_dc0	DC offset of the input R component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_IN_DC1

ISP_CSC_IN_DC1 is CSC input DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41534	ISP_CSC_IN_DC1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			reserved	in_dc2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RO	reserved	Reserved
[15:5]	RW	in_dc2	DC offset of the input B component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_OUT_DC0

ISP_CSC_OUT_DC0 is CSC output DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41540	ISP_CSC_OUT_DC0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	out_dc1			reserved	out_dc0			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	out_dc1	DC offset of the output U component, signed integer
[20:16]	RO	reserved	Reserved
[15:5]	RW	out_dc0	DC offset of the output Y component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_OUT_DC1

ISP_CSC_OUT_DC1 is CSC output DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41544	ISP_CSC_OUT_DC1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			reserved	out_dc2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RO	reserved	Reserved
[15:5]	RW	out_dc2	DC offset of the output V component, signed integer
[4:0]	RO	reserved	Reserved

ISP_MCDS_CFG

ISP_MCDS_CFG is an MCDS control register.

Offset Address	Register Name	Total Reset Value
0x41800	ISP_MCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											midf_en	uv2c_mode	uv2c_en	vcds_en	hcds_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	midf_en	MCDSILTER enable 0: disabled 1: enabled
[3]	RW	uv2c_mode	UV2C bypass mode 0: The U component data is output. 1: The V component data is output.
[2]	RW	uv2c_en	UV2C enable for converting the internal dual-component (U and V) data into the single component (C) data 0: disabled 1: enabled
[1]	RW	vcds_en	Vertical chrominance down sampling enable 0: disabled 1: enabled
[0]	RW	hcds_en	Horizontal chrominance down sampling enable 0: disabled 1: enabled

ISP_HCDS_SIZE

ISP_HCDS_SIZE is a horizontal chrominance down sampling input size configuration register.

Offset Address	Register Name	Total Reset Value
0x41814	ISP_HCDS_SIZE	0x077F_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				width_out												reserved				width_in											
Reset	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	width_out	U/V line width (in pixel) of the output picture during horizontal chrominance down sampling. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width_in	U/V line width (in pixel) of the input picture. The configured value is the actual value minus 1.

ISP_MIDF_SIZE

ISP_MIDF_SIZE is a median filtering input chrominance picture size register.

Offset Address	Register Name	Total Reset Value
0x4182C	ISP_MIDF_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Picture height after vertical chrominance down sampling. The configured value is the actual height minus 1. For example, if the actual picture height is 720, this field needs to be set to **719**.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width after vertical chrominance down sampling (UV-to-C conversion). The configured value is the actual width minus 1. For example, if the actual picture width is 1280, this field needs to be set to **1279**.

ISP_MCDS_PARA

ISP_MCDS_PARA is an NR blending ratio and shift register.

Offset Address	Register Name	Total Reset Value
0x41844	ISP_MCDS_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				midf_bldr				reserved				limit				reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	midf_bldr	MIDF blending ratio, 5-bit unsigned number. The value range is 0−16.
[23]	RO	reserved	Reserved
[22:16]	RW	limit	Limit for the coring function. The value range is 0−127.
[15:0]	RO	reserved	Reserved

ISP_MCDS_SIZE

ISP_MCDS_SIZE is an MCDS input picture size register.

Offset Address	Register Name	Total Reset Value
0x418F0	ISP_MCDS_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Input picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, this field needs to be set to **1079**.
[15:13]	RO	reserved	Reserved

[12:0]	RW	width	Input picture width. The configured value is the actual value minus 1. For example, if the actual picture width is 1920, this field needs to be set to **1919**.

ISP_SHARPEN_CFG

ISP_SHARPEN_CFG is a sharpening control register.

Offset Address	Register Name	Total Reset Value
0x45200	ISP_SHARPEN_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Sharpening enable 0: disabled 1: enabled

ISP_SHARPEN_AMT

ISP_SHARPEN_AMT is a sharpening strength register.

Offset Address	Register Name	Total Reset Value
0x45210	ISP_SHARPEN_AMT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				edge_amt												reserved				sharp_amt											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	edge_amt	Edge enhancement strength (u, 12.0). (u, 12.0) indicates that the value is an unsigned number consisting of a 12-bit integral part and a 0-bit decimal part. The same rule applies to the meanings of other fields of sharpening registers.
[15:12]	RO	reserved	Reserved
[11:0]	RW	sharp_amt	Detail enhancement strength (u, 12.0)

ISP_SHARPEN_SHOOTAMT

ISP_SHARPEN_SHOOTAMT is a sharpening shoot AMT control register.

Offset Address	Register Name	Total Reset Value
0x4521C	ISP_SHARPEN_SHOOTAMT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		over_amt		reserved		under_amt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	over_amt	Overshoot control coefficient (u, 8.0)
[15:8]	RO	reserved	Reserved
[7:0]	RW	under_amt	Undershoot control coefficient (u, 8.0)

ISP_SHARPEN_EDGEJAG

ISP_SHARPEN_EDGEJAG is a jag high-frequency parameter register.

Offset Address	Register Name	Total Reset Value
0x45224	ISP_SHARPEN_EDGEJAG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					edgejagamt		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	edgejagamt	Jag high-frequency gain, 12-bit unsigned integer

ISP_SHARPEN_OSHTJAG

ISP_SHARPEN_OSHTJAG is a jag overshoot parameter register.

Offset Address	Register Name	Total Reset Value
0x45228	ISP_SHARPEN_OSHTJAG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								oshtjagamt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	oshtjagamt	Jag overshoot gain, 8-bit unsigned integer

ISP_SHARPEN_USHTJAG

ISP_SHARPEN_USHTJAG is a jag undershoot parameter register.

Offset Address	Register Name	Total Reset Value
0x4522C	ISP_SHARPEN_USHTJAG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ushtjagamt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ushtjagamt	Jag undershoot gain, 8-bit unsigned integer

ISP_SHARPEN_MID0

ISP_SHARPEN_MID0 is a sharpening IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x45230	ISP_SHARPEN_MID0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp02								mid_tmp01								mid_tmp00							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp02	IF filtering coefficient 02 (s, 8.0). (s, 8.0) indicates that the value is a signed number consisting of an 8-bit integral part and a 0-bit decimal part. The same rule applies to the meanings of other fields of sharpening registers.
[15:8]	RW	mid_tmp01	IF filtering coefficient 01 (s, 8.0)
[7:0]	RW	mid_tmp00	IF filtering coefficient 00 (s, 8.0)

ISP_SHARPEN_MID1

ISP_SHARPEN_MID1 is a sharpening IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x45234	ISP_SHARPEN_MID1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp12								mid_tmp11								mid_tmp10							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp12	IF filtering coefficient 12 (s, 8.0)
[15:8]	RW	mid_tmp11	IF filtering coefficient 11 (s, 8.0)
[7:0]	RW	mid_tmp10	IF filtering coefficient 10 (s, 8.0)

ISP_SHARPEN_MID2

ISP_SHARPEN_MID2 is a sharpening IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x45238	ISP_SHARPEN_MID2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp22								mid_tmp21								mid_tmp20							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp22	IF filtering coefficient 22 (s, 8.0)
[15:8]	RW	mid_tmp21	IF filtering coefficient 21 (s, 8.0)
[7:0]	RW	mid_tmp20	IF filtering coefficient 20 (s, 8.0)

ISP_SHARPEN_LINETHD

ISP_SHARPEN_LINETHD is a sharpening line detection threshold register.

Offset Address	Register Name	Total Reset Value
0x4523C	ISP_SHARPEN_LINETHD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								line_thd2								reserved								line_thd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	line_thd2	Line detection threshold 2 (u, 8.0)
[15:8]	RO	reserved	Reserved
[7:0]	RW	line_thd1	Line detection threshold 1 (u, 8.0)

ISP_SHARPEN_THD2

ISP_SHARPEN_THD2 is sharpening threshold register 2.

Offset Address	Register Name	Total Reset Value
0x45240	ISP_SHARPEN_THD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								edge_thd2								reserved								sharp_thd2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	edge_thd2	Edge enhancement threshold (u, 10.0)
[15:10]	RO	reserved	Reserved
[9:0]	RW	sharp_thd2	Detail enhancement threshold (u, 10.0)

ISP_SHARPEN_CTRL

ISP_SHARPEN_CTRL is a sharpening control register.

Offset Address	Register Name	Total Reset Value
0x45244	ISP_SHARPEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											jagctrl	shtlumamod	shtvarctrl	lumactrl	enpixsel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	jagctrl	Whether to use the jag control switch 0: no 1: yes
[3]	RW	shtlumamod	Whether to use the luminance to control the overshoot 0: no 1: yes
[2]	RW	shtvarctrl	Variance control enable 0: disabled 1: enabled

[1]	RW	lumactrl	Luminance control 0: disabled 1: enabled
[0]	RW	enpixsel	Overshoot suppression 0: The original value is selected. 1: The maximum/minimum field value is selected.

ISP_SHARPEN_LUMATH

ISP_SHARPEN_LUMATH is a luma threshold parameter register.

Offset Address	Register Name	Total Reset Value
0x45248	ISP_SHARPEN_LUMATH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lumath3								lumath2								lumath1								lumath0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	lumath3	Luminance control threshold 3
[23:16]	RW	lumath2	Luminance control threshold 2
[15:8]	RW	lumath1	Luminance control threshold 1
[7:0]	RW	lumath0	Luminance control threshold 0

ISP_SHARPEN_LUMAWGT

ISP_SHARPEN_LUMAWGT is a luma weight parameter register.

Offset Address	Register Name	Total Reset Value
0x4524C	ISP_SHARPEN_LUMAWGT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lumawgt3								lumawgt2								lumawgt1								lumawgt0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	lumawgt3	Luminance weight 3
[23:16]	RW	lumawgt2	Luminance weight 2
[15:8]	RW	lumawgt1	Luminance weight 1
[7:0]	RW	lumawgt0	Luminance weight 0

ISP_SHARPEN_OSHTVARTH

ISP_SHARPEN_OSHTVARTH is variance threshold parameter register 0.

Offset Address	Register Name	Total Reset Value
0x45258	ISP_SHARPEN_OSHTVARTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	overvarth1			reserved		overvarth0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	overvarth1	Overshoot variance threshold 1
[15:10]	RO	reserved	Reserved
[9:0]	RW	overvarth0	Overshoot variance threshold 0

ISP_SHARPEN_OSHTVAR

ISP_SHARPEN_OSHTVAR is overshoot variance parameter register 0.

Offset Address	Register Name	Total Reset Value
0x4525C	ISP_SHARPEN_OSHTVAR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						overvaramt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	overvaramt	Overshoot variance gain

ISP_SHARPEN_USHTVARTH

ISP_SHARPEN_USHTVARTH is variance threshold parameter register 1.

Offset Address	Register Name	Total Reset Value
0x45260	ISP_SHARPEN_USHTVARTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								undervarth1								reserved								undervarth0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	undervarth1	Undershoot variance threshold 1
[15:10]	RO	reserved	Reserved
[9:0]	RW	undervarth0	Undershoot variance threshold 0

ISP_SHARPEN_USHTVAR

ISP_SHARPEN_USHTVAR is overshoot variance parameter register 1.

Offset Address	Register Name	Total Reset Value
0x45264	ISP_SHARPEN_USHTVAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								undervaramt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	undervaramt	Undershoot variance gain

ISP_SHARPEN_OSHTLUMA

ISP_SHARPEN_OSHTLUMA is overshoot luminance parameter register 0.

Offset Address	Register Name	Total Reset Value
0x45268	ISP_SHARPEN_OSHTLUMA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	overlumawgt1								overlumawgt0								overlumath1								overlumath0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	overlumawgt1	Luminance weight 1
[23:16]	RW	overlumawgt0	Luminance weight 0
[15:8]	RW	overlumath1	Luminance threshold 1
[7:0]	RW	overlumath0	Luminance threshold 0

ISP_SHARPEN_USHTLUMA

ISP_SHARPEN_USHTLUMA is overshoot luminance parameter register 1.

Offset Address	Register Name	Total Reset Value
0x4526C	ISP_SHARPEN_USHTLUMA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	underlumawgt1								underlumawgt0								underlumath1								underlumath0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	underlumawgt1	Luminance weight 1
[23:16]	RW	underlumawgt0	Luminance weight 0
[15:8]	RW	underlumath1	Luminance threshold 1
[7:0]	RW	underlumath0	Luminance threshold 0

ISP_SHARPEN_SHIFT

ISP_SHARPEN_SHIFT is a shift parameter register.

Offset Address	Register Name	Total Reset Value
0x45274	ISP_SHARPEN_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												limit				maxshift								minshift							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	limit	Limit for the coring function
[15:8]	RW	maxshift	Maximum field shift
[7:0]	RW	minshift	Minimum field shift

ISP_SHARPEN_SIZE

ISP_SHARPEN_SIZE is a sharpening picture size register.

Offset Address	Register Name	Total Reset Value
0x452F0	ISP_SHARPEN_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, this field needs to be set to **1079**.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, if the actual picture height is 1920, this field needs to be set to **1919**.

ISP_DEHAZE_CFG

ISP_DEHAZE_CFG is a dehaze enable register.

Offset Address	Register Name	Total Reset Value
0x46200	ISP_DEHAZE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Dehaze enable 0: disabled 1: enabled

ISP_DEHAZE_PRE_UPDATE

ISP_DEHAZE_PRE_UPDATE is a dehaze statistics update register.

Offset Address	Register Name	Total Reset Value
0x46210	ISP_DEHAZE_PRE_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															pre_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	pre_update	Dehaze statistics configuration update. This bit is automatically cleared for each frame.

ISP_DEHAZE_BLK_SIZE

ISP_DEHAZE_BLK_SIZE is a dehaze block size configuration register.

Offset Address	Register Name	Total Reset Value
0x46214	ISP_DEHAZE_BLK_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								block_sizeh								reserved								block_sizev							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	block_sizeh	Horizontal block size. The configured value is the actual value minus 1.
[15:9]	RO	reserved	Reserved
[8:0]	RW	block_sizev	Vertical block size. The configured value is the actual value minus 1.

ISP_DEHAZE_BLK_SUM

ISP_DEHAZE_BLK_SUM is a dehaze block quantity register.

Offset Address	Register Name	Total Reset Value
0x46218	ISP_DEHAZE_BLK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								block_sum							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	block_sum	Number of dehaze blocks. The configured value is calculated as follows: Configured value = Number of horizontal blocks x (Number of vertical blocks − 1)

ISP_DEHAZE_DC_SIZE

ISP_DEHAZE_DC_SIZE is a dehaze bilinear interpolation point quantity configuration register.

Offset Address	Register Name	Total Reset Value
0x4621C	ISP_DEHAZE_DC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						dc_numh						dc_numv			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:5]	RW	dc_numh	Number of bilinear interpolation horizontal points. The configured value is the actual number of horizontal blocks minus 1.
[4:0]	RW	dc_numv	Number of bilinear interpolation vertical points. The configured value is the actual number of vertical blocks minus 1.

ISP_DEHAZE_X

ISP_DEHAZE_X is a configuration register for the horizontal phase difference between the pixels of the dehaze enlarged picture.

Offset Address	Register Name	Total Reset Value
0x46220	ISP_DEHAZE_X	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phase_x																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	phase_x	Horizontal phase difference between the pixels of the enlarged picture, unsigned integer. The configured value is calculated as follows: Configured value = Horizontal block size x (1<<22)

ISP_DEHAZE_Y

ISP_DEHAZE_Y is a configuration register for the vertical phase difference between the pixels of the dehaze enlarged picture.

Offset Address	Register Name	Total Reset Value
0x46224	ISP_DEHAZE_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phase_y																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	phase_y	Vertical phase difference between the pixels of the enlarged picture, unsigned integer. The configured value is calculated as follows: Configured value = Horizontal block size x (1<<22)

ISP_DEHAZE_STAT_MODE

ISP_DEHAZE_STAT_MODE is a dehaze statistics module control register.

Offset Address	Register Name	Total Reset Value
0x46228	ISP_DEHAZE_STAT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															max_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	max_mode	Maximum value statistics control 0: Mean filtering is performed on RGB components, and then the RGB components corresponding to the maximum RGB sum of each window are counted. 1: The RGB components corresponding to the maximum RGB sum of each window are counted.

ISP_DEHAZE_NEG_MODE

ISP_DEHAZE_NEG_MODE is a dehaze inversion control register.

Offset Address	Register Name	Total Reset Value
0x4622C	ISP_DEHAZE_NEG_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															neg_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	neg_mode	Inversion mode control 0: normal mode 1: inversion mode

ISP_DEHAZE_AIR

ISP_DEHAZE_AIR is a dehaze airglow configuration register.

Offset Address	Register Name	Total Reset Value
0x46230	ISP_DEHAZE_AIR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		air_r										air_g										air_b									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	air_r	Airglow A corresponding to the R channel
[19:10]	RW	air_g	Airglow A corresponding to the G channel
[9:0]	RW	air_b	Airglow A corresponding to the B channel

ISP_DEHAZE_THLD

ISP_DEHAZE_THLD is a dehaze T threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x46234	ISP_DEHAZE_THLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						thld									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	thld	T threshold coefficient, unsigned integer

ISP_DEHAZE_GSTRTH

ISP_DEHAZE_GSTRTH is a dehaze global strength coefficient register.

Offset Address	Register Name	Total Reset Value
0x46238	ISP_DEHAZE_GSTRTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gstrth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	gstrth	G calculation coefficient, unsigned integer

ISP_DEHAZE_BLTHLD

ISP_DEHAZE_BLTHLD is a dehaze minimum value filtering threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x4623C	ISP_DEHAZE_BLTHLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						bltthld									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	bltthld	Threshold coefficient of the minimum value filtering, unsigned integer

ISP_DEHAZE_STR_LUT_UPDATE

ISP_DEHAZE_STR_LUT_UPDATE is a dehaze strength table update register.

Offset Address	Register Name	Total Reset Value
0x46240	ISP_DEHAZE_STR_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															str_lut_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	str_lut_update	Configuration update for the dehaze strength table. This bit is automatically cleared for each frame.

ISP_DEHAZE_MINSTAT_WADDR

ISP_DEHAZE_MINSTAT_WADDR is a dehaze minimum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x46280	ISP_DEHAZE_MINSTAT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								minstat_waddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:0]	RW	minstat_waddr	Write address of the dehaze minimum value statistics. The value range is 0−511.

ISP_DEHAZE_MINSTAT_WDATA

ISP_DEHAZE_MINSTAT_WDATA is a dehaze minimum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x46284	ISP_DEHAZE_MINSTAT_WDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		minstat_wdata_h		reserved		minstat_wdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	minstat_wdata_h	ID of the block with the larger ID between the two blocks to which the dehaze minimum value statistics are written
[15:10]	RO	reserved	Reserved
[9:0]	RW	minstat_wdata_l	ID of the block with the smaller ID between the two blocks to which the dehaze minimum value statistics are written

ISP_DEHAZE_MINSTAT_RADDR

ISP_DEHAZE_MINSTAT_RADDR is a dehaze minimum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x46288	ISP_DEHAZE_MINSTAT_RADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						minstat_raddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:0]	RW	minstat_raddr	Read address of the dehaze minimum value statistics. The value range is 0−511.

ISP_DEHAZE_MINSTAT_RDATA

ISP_DEHAZE_MINSTAT_RDATA is a dehaze minimum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x4628C	ISP_DEHAZE_MINSTAT_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		minstat_rdata_h		reserved		minstat_rdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	minstat_rdata_h	ID of the block with the larger ID between the two blocks from which the dehaze minimum value statistics are read
[15:10]	RO	reserved	Reserved
[9:0]	RO	minstat_rdata_l	ID of the block with the smaller ID between the two blocks from which the dehaze minimum value statistics are read

ISP_DEHAZE_MAXSTAT_WADDR

ISP_DEHAZE_MAXSTAT_WADDR is a dehaze maximum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x46290	ISP_DEHAZE_MAXSTAT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						maxstat_waddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	maxstat_waddr	Write address of the dehaze maximum value statistics. The value range is 0−1023.

ISP_DEHAZE_MAXSTAT_WDATA

ISP_DEHAZE_MAXSTAT_WDATA is a dehaze maximum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x46294	ISP_DEHAZE_MAXSTAT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				maxstat_wdata																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RW	maxstat_wdata	Write data of the dehaze maximum value statistics

ISP_DEHAZE_MAXSTAT_RADDR

ISP_DEHAZE_MAXSTAT_RADDR is a dehaze maximum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x46298	ISP_DEHAZE_MAXSTAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								maxstat_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	maxstat_raddr	Read address of the dehaze maximum value statistics. The value range is 0−1023.

ISP_DEHAZE_MAXSTAT_RDATA

ISP_DEHAZE_MAXSTAT_RDATA is a dehaze maximum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x4629C	ISP_DEHAZE_MAXSTAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				maxstat_rdata																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RO	maxstat_rdata	Read data of the dehaze maximum value statistics (R: bit[29:20]; G: bit[19:10]; B: bit[9:0])

ISP_DEHAZE_PRESTAT_WADDR

ISP_DEHAZE_PRESTAT_WADDR is a dehaze previous frame minimum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x462A0	ISP_DEHAZE_PRESTAT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						prestat_waddr									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	prestat_waddr	Write address of the dehaze previous frame minimum value statistics. The value range is 0−511.

ISP_DEHAZE_PRESTAT_WDATA

ISP_DEHAZE_PRESTAT_WDATA is a dehaze previous frame minimum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x462A4	ISP_DEHAZE_PRESTAT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								prestat_wdata_h								reserved								prestat_wdata_l							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	prestat_wdata_h	ID of the block with the larger ID between the two blocks to which the dehaze previous frame minimum value statistics are written
[15:10]	RO	reserved	Reserved
[9:0]	RW	prestat_wdata_l	ID of the block with the smaller ID between the two blocks to which the dehaze previous frame minimum value statistics are written

ISP_DEHAZE_PRESTAT_RADDR

ISP_DEHAZE_PRESTAT_RADDR is a dehaze previous frame minimum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x462A8	ISP_DEHAZE_PRESTAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								prestat_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	prestat_raddr	Read address of the dehaze previous frame minimum value statistics. The value range is 0−511.

ISP_DEHAZE_PRESTAT_RDATA

ISP_DEHAZE_PRESTAT_RDATA is a dehaze previous frame minimum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x462AC	ISP_DEHAZE_PRESTAT_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		prestat_rdata_h		reserved		prestat_rdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RO	prestat_rdata_h	ID of the block with the larger ID between the two blocks from which the dehaze previous frame minimum value statistics are read
[15:10]	RO	reserved	Reserved
[9:0]	RO	prestat_rdata_l	ID of the block with the smaller ID between the two blocks from which the dehaze previous frame minimum value statistics are read

ISP_DEHAZE_LUT_WADDR

ISP_DEHAZE_LUT_WADDR is a dehaze strength LUT information write address register.

Offset Address	Register Name	Total Reset Value
0x462B0	ISP_DEHAZE_LUT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						lut_waddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	lut_waddr	Write address of the dehaze strength LUT information. The value range is 0−255.

ISP_DEHAZE_LUT_WDATA

ISP_DEHAZE_LUT_WDATA is a dehaze strength LUT information write data register.

Offset Address	Register Name	Total Reset Value
0x462B4	ISP_DEHAZE_LUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	lut_wdata	Write data of the dehaze strength LUT information

ISP_DEHAZE_LUT_RADDR

ISP_DEHAZE_LUT_RADDR is a dehaze strength LUT information read address register.

Offset Address	Register Name	Total Reset Value
0x462B8	ISP_DEHAZE_LUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	lut_raddr	Read address of the dehaze strength LUT information. The value range is 0−255.

ISP_DEHAZE_LUT_RDATA

ISP_DEHAZE_LUT_RDATA is a dehaze strength LUT information read data register.

Offset Address	Register Name	Total Reset Value
0x462BC	ISP_DEHAZE_LUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_rdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	lut_rdata	Read data of the dehaze strength LUT information

ISP_DEHAZE_SIZE

ISP_DEHAZE_SIZE is a dehaze picture size register.

Offset Address	Register Name	Total Reset Value
0x462F0	ISP_DEHAZE_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Window height (in line). The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Window width (in pixel). The configured value is the actual value minus 1.

ISP_ACM_CTRL

ISP_ACM_CTRL is an ACM control register.

Offset Address	Register Name	Total Reset Value
0x51400	ISP_ACM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm_en	acm_dbg_en	acm_stretch	acm_cliprange	acm_cliporwrap	reserved							acm_dbg_pos										acm_dbg_mode	acm_cbcrthr								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	acm_en	ACM module enable 0: disabled (the data output is bypassed) 1: enabled (luminance and contrast adjustment is implemented)

[30]	RW	acm_dbg_en	ACM debugging enable. When acm_dbg_en is valid, the original picture is displayed on the left part of the screen, and the picture processed by ABC is displayed on the right part of the screen.
[29]	RW	acm_stretch	Input pixel range 0: Y 64RO940, C 64-960 1: Y 0-1023, C 0-1023
[28]	RW	acm_cliprange	Output pixel range 0: Y 64-940, C 64-960 1: Y 0-1023, C 0-1023
[27]	RW	acm_cliporwrap	Hue component value limit after ACM 0: The hue component is wrapped around to fall within [0, 1023]. 1: The hue component is clipped to fall within [0, 1023].
[26:23]	RO	reserved	Reserved
[22:10]	RW	acm_dbg_pos	ACM debugging position
[9]	RW	acm_dbg_mode	ACM debugging mode 0: The original picture is displayed on the left part, and the picture processed by ACM is displayed on the right part. 1: The picture processed by ACM is displayed on the left part, and the original picture is displayed on the right part.
[8:0]	RW	acm_cbcrthr	ACM algorithm enable threshold, 9-bit unsigned number (ranging from 0 to 255)

ISP_ACM_ADJ

ISP_ACM_ADJ is an ACM processed pixel change register.

Offset Address	Register Name	Total Reset Value
0x51404	ISP_ACM_ADJ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				acm_gain0								acm_gain1								acm_gain2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	acm_gain0	Control coefficient of the luminance adjustment range. The value range is 0−512.

[19:10]	RW	acm_gain1	Control coefficient of the hue adjustment range. The value range is 0–512.
[9:0]	RW	acm_gain2	Control coefficient of the saturation adjustment range. The value range is 0–512.

ISP_ACM_SIZE

ISP_ACM_SIZE is an ACM processed picture size register.

Offset Address	Register Name	Total Reset Value
0x51410	ISP_ACM_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Picture height (in pixel). The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1.

ISP_ACM_PARA_ADDR

ISP_ACM_PARA_ADDR is an ACM coefficient configuration loading address register.

Offset Address	Register Name	Total Reset Value
0x51414	ISP_ACM_PARA_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm_para_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	acm_para_addr	Address for loading ACM coefficients

ISP_ACM_PARA_UP

ISP_ACM_PARA_UP is an ACM coefficient configuration update register.

Offset Address	Register Name	Total Reset Value
0x51420	ISP_ACM_PARA_UP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															para_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	para_up	Parameter update. This bit is automatically cleared for each frame.

ISP_VPDCICTRL

ISP_VPDCICTRL is a DCI control register.

Offset Address	Register Name	Total Reset Value
0x51C00	ISP_VPDCICTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_en	dci_dbg_en	dci_scene_flg	dci_man_adj0	dci_man_adj1	dci_man_adj2	dci_cbcrcmp_en	dci_cbcrsta_en	dci_in_range	dci_out_range	dci_shift_ctrl		dci_histlpf_en	reserved		dci_dbg_mode	reserved		dci_hist_wgt_en	dci_dbg_pos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dci_en	DCI enable 0: disabled (the data output is bypassed) 1: enabled (the luminance and contrast adjustment is implemented)
[30]	RW	dci_dbg_en	DCI demo mode enable 0: disabled 1: The original picture is displayed on the left part of the screen, and the picture processed by the DCI module is displayed on the right part of the screen.

[29]	RW	dci_scene_flg	DCI scenario switch enable 0: disabled 1: enabled
[28]	RW	dci_man_adj0	Adjustment mode of curve 0 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[27]	RW	dci_man_adj1	Adjustment mode of curve 1 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[26]	RW	dci_man_adj2	Adjustment mode of curve 2 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[25]	RW	dci_cbcrcmp_en	DCI chrominance compensation enable 0: The DCI algorithm does not adjust the chrominance component. 1: The DCI algorithm adjusts the chrominance component.
[24]	RW	dci_cbcrsta_en	Histogram statistics select 0: Histogram statistics are collected only on the luminance component. 1: Histogram statistics are collected on the weighted Y, Cb, and Cr components.
[23]	RW	dci_in_range	Input range 0: limited range (Y ranges from 64 to 940 and C ranges from 64 to 960 for the input 10-bit pixel data) 1: full range (Y ranges from 0 to 1023 and C ranges from 0 to 1023 for the input 10-bit pixel data)
[22]	RW	dci_out_range	Output range 0: limited range (Y ranges from 64 to 940 and C ranges from 64 to 960 for the output 10-bit pixel data) 1: full range (Y ranges from 0 to 1023 and C ranges from 0 to 1023 for the output 10-bit pixel data)
[21:20]	RW	dci_shift_ctrl	DCI histogram statistics shift control 00: shifted rightwards by six bits 01: shifted rightwards by seven bits 10: shifted rightwards by eight bits 11: shifted rightwards by nine bits
[19]	RW	dci_histlpf_en	Histogram low-pass filtering enable 0: disabled 1: enabled
[18:17]	RO	reserved	Reserved

[16]	RW	dci_dbg_mode	DCI demo mode 0: The original picture is displayed on the left part of the screen, and the picture adjusted by the DCI module is displayed on the right part of the screen. 1: The picture adjusted by the DCI module is displayed on the left part of the screen, and the original picture is displayed on the right part of the screen.
[15:14]	RO	reserved	Reserved
[13]	RW	dci_hist_wgt_en	Histogram statistical method select 0: The original histogram is used. 1: The weighted histogram is used.
[12:0]	RW	dci_dbg_pos	DCI debugging position

ISP_VPDCIHPOS

ISP_VPDCIHPOS is a DCI algorithm horizontal adjustment region register.

Offset Address	Register Name	Total Reset Value
0x51C04	ISP_VPDCIHPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_hstart												dci_hend												reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	dci_hstart	Start value of the horizontal active region of the DCI algorithm
[18:6]	RW	dci_hend	End value of the horizontal active region of the DCI algorithm
[5:0]	RO	reserved	Reserved

ISP_VPDCIVPOS

ISP_VPDCIVPOS is a DCI algorithm vertical adjustment region register.

Offset Address	Register Name	Total Reset Value
0x51C08	ISP_VPDCIVPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_vstart												dci_vend												reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	dci_vstart	Start value of the vertical active region of the DCI algorithm

[18:6]	RW	dci_vend	End value of the vertical active region of the DCI algorithm
[5:0]	RO	reserved	Reserved

ISP_VPDCIHISBLD

ISP_VPDCIHISBLD is a DCI histogram statistics weighted coefficient register.

Offset Address	Register Name	Total Reset Value
0x51C0C	ISP_VPDCIHISBLD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_cbcrsta_y		dci_cbcrsta_cb		dci_cbcrsta_cr		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_cbcrsta_y	Weighted coefficient of the Y component when histogram statistics are added. It is an 8-bit signed number and the MSB is the sign bit.
[23:16]	RW	dci_cbcrsta_cb	Weighted coefficient of the Cb component when histogram statistics are added. It is an 8-bit signed number and the MSB is the sign bit.
[15:8]	RW	dci_cbcrsta_cr	Weighted coefficient of the Cr component when histogram statistics are added. It is an 8-bit signed number and the MSB is the sign bit.
[7:0]	RO	reserved	Reserved

ISP_VPDCIHISOFT

ISP_VPDCIHISOFT is a DCI histogram statistics offset register.

Offset Address	Register Name	Total Reset Value
0x51C10	ISP_VPDCIHISOFT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_cbcrsta_oft				reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RW	dci_cbcrsta_oft	Offset when histogram statistics are added. It is a 9-bit signed number and the MSB is the sign bit.
[22:0]	RO	reserved	Reserved

ISP_VPDCIHISCOR

ISP_VPDCIHISCOR is a DCI histogram coring register.

Offset Address	Register Name	Total Reset Value
0x51C14	ISP_VPDCIHISCOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_histcor_thr0								dci_histcor_thr1								dci_histcor_thr2								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_histcor_thr0	Coring threshold for histogram 0
[23:16]	RW	dci_histcor_thr1	Coring threshold for histogram 1
[15:8]	RW	dci_histcor_thr2	Coring threshold for histogram 2
[7:0]	RO	reserved	Reserved

ISP_VPDCIMERBLD

ISP_VPDCIMERBLD is a DCI adjustment unit blend value register.

Offset Address	Register Name	Total Reset Value
0x51C18	ISP_VPDCIMERBLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_metrc_abld0								dci_metrc_abld1				dci_metrc_abld2				dci_hist_abld								dci_org_abld						reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	dci_metrc_abld0	Weighted alpha blend value of the current frame for metric 0
[25:20]	RW	dci_metrc_abld1	Weighted alpha blend value of the current frame for metric 1
[19:14]	RW	dci_metrc_abld2	Weighted alpha blend value of the current frame for metric 2
[13:8]	RW	dci_hist_abld	Weighted alpha blend value of the current histogram and the previous histogram
[7:2]	RW	dci_org_abld	Alpha blend value when the luminance component is adjusted
[1:0]	RO	reserved	Reserved

ISP_VPDCIADJWGT

ISP_VPDCIADJWGT is a DCI manually configured curve weight register.

Offset Address	Register Name	Total Reset Value
0x51C1C	ISP_VPDCIADJWGT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_man_adjwgt0								dci_man_adjwgt1								dci_man_adjwgt2								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_man_adjwgt0	Weighted value of curve 0 in manual mode
[23:16]	RW	dci_man_adjwgt1	Weighted value of curve 1 in manual mode
[15:8]	RW	dci_man_adjwgt2	Weighted value of curve 2 in manual mode
[7:0]	RO	reserved	Reserved

ISP_VPDCICLIP0

ISP_VPDCICLIP0 is a DCI curve 0 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C20	ISP_VPDCICLIP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow0								dci_wgt_cliphigh0								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow0	Lower limit of the weighted value of curve 0
[23:16]	RW	dci_wgt_cliphigh0	Upper limit of the weighted value of curve 0
[15:0]	RO	reserved	Reserved

ISP_VPDCICLIP1

ISP_VPDCICLIP1 is a DCI curve 1 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C24	ISP_VPDCICLIP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow1								dci_wgt_cliphigh1								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow1	Lower limit of the weighted value of curve 1
[23:16]	RW	dci_wgt_cliphigh1	Upper limit of the weighted value of curve 1
[15:0]	RO	reserved	Reserved

ISP_VPDCICLIP2

ISP_VPDCICLIP2 is a DCI curve 2 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C28	ISP_VPDCICLIP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow2								dci_wgt_cliphigh2								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow2	Lower limit of the weighted value of curve 2
[23:16]	RW	dci_wgt_cliphigh2	Upper limit of the weighted value of curve 2
[15:0]	RO	reserved	Reserved

ISP_VPDCIGLBGAIN

ISP_VPDCIGLBGAIN is a DCI luminance adjustment unit global gain register.

Offset Address	Register Name	Total Reset Value
0x51C2C	ISP_VPDCIGLBGAIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_glb_gain0								dci_glb_gain1				dci_glb_gain2				reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	dci_glb_gain0	Global gain 0 when the luminance component is adjusted

[25:20]	RW	dci_glb_gain1	Global gain 1 when the luminance component is adjusted
[19:14]	RW	dci_glb_gain2	Global gain 2 when the luminance component is adjusted
[13:0]	RO	reserved	Reserved

ISP_VPDCIPOSTHR0

ISP_VPDCIPOSTHR0 is DCI adjustment unit threshold register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C30	ISP_VPDCIPOSTHR0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_thr1		dci_gainpos_thr2		dci_gainpos_thr3		dci_gainpos_thr4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr1	Threshold 1 for the luminance (Y) when the picture is adjusted from dark to bright
[23:16]	RW	dci_gainpos_thr2	Threshold 2 for the luminance (Y) when the picture is adjusted from dark to bright
[15:8]	RW	dci_gainpos_thr3	Threshold 3 for the luminance (Y) when the picture is adjusted from dark to bright
[7:0]	RW	dci_gainpos_thr4	Threshold 4 for the luminance (Y) when the picture is adjusted from dark to bright

ISP_VPDCIPOSTHR1

ISP_VPDCIPOSTHR1 is DCI adjustment unit threshold register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C34	ISP_VPDCIPOSTHR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_thr5		dci_gainpos_thr6		dci_gainpos_thr7		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr5	Threshold 5 for the luminance (Y) when the picture is adjusted from dark to bright
[23:16]	RW	dci_gainpos_thr6	Threshold 6 for the luminance (Y) when the picture is adjusted from dark to bright

[15:8]	RW	dci_gainpos_thr7	Threshold 7 for the luminance (Y) when the picture is adjusted from dark to bright
[7:0]	RO	reserved	Reserved

ISP_VPDCIPOSGAIN0

ISP_VPDCIPOSGAIN0 is DCI adjustment unit gain register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C38	ISP_VPDCIPOSGAIN0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_cbcr0	dci_gainpos_cbcr1	dci_gainpos_cbcr2	dci_gainpos_cbcr3	dci_gainpos_cbcr4	dci_gainpos_cbcr5	dci_gainpos_cbcr6	dci_gainpos_cbcr7
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from dark to bright
[27:24]	RW	dci_gainpos_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from dark to bright
[23:20]	RW	dci_gainpos_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from dark to bright
[19:16]	RW	dci_gainpos_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from dark to bright
[15:12]	RW	dci_gainpos_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from dark to bright
[11:8]	RW	dci_gainpos_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from dark to bright
[7:4]	RW	dci_gainpos_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from dark to bright
[3:0]	RW	dci_gainpos_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from dark to bright

ISP_VPDCIPOSGAIN1

ISP_VPDCIPOSGAIN1 is DCI adjustment unit gain register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C3C	ISP_VPDCIPOSGAIN1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_cbcr8	reserved						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from dark to bright
[27:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP0

ISP_VPDCIPOSSLP0 is DCI adjustment unit slope register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C40	ISP_VPDCIPOSSLP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp0			dci_gainpos_slp1		dci_gainpos_slp2		reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp0	Slope of region 1 when the picture is adjusted from dark to bright, 10-bit signed number
[21:12]	RW	dci_gainpos_slp1	Slope of region 2 when the picture is adjusted from dark to bright, 10-bit signed number
[11:2]	RW	dci_gainpos_slp2	Slope of region 3 when the picture is adjusted from dark to bright, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP1

ISP_VPDCIPOSSLP1 is DCI adjustment unit slope register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C44	ISP_VPDCIPOSSLP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp3			dci_gainpos_slp4		dci_gainpos_slp5		reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp3	Slope of region 4 when the picture is adjusted from dark to bright, 10-bit signed number
[21:12]	RW	dci_gainpos_slp4	Slope of region 5 when the picture is adjusted from dark to bright, 10-bit signed number
[11:2]	RW	dci_gainpos_slp5	Slope of region 6 when the picture is adjusted from dark to bright, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP2

ISP_VPDCIPOSSLP2 is DCI adjustment unit slope register 2 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C48	ISP_VPDCIPOSSLP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp6			dci_gainpos_slp7		reserved		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp6	Slope of region 7 when the picture is adjusted from dark to bright, 10-bit signed number
[21:12]	RW	dci_gainpos_slp7	Slope of region 8 when the picture is adjusted from dark to bright, 10-bit signed number
[11:0]	RO	reserved	Reserved

ISP_VPDCINEGTHR0

ISP_VPDCINEGTHR0 is DCI adjustment unit threshold register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C4C	ISP_VPDCINEGTHR0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_thr1		dci_gainneg_thr2		dci_gainneg_thr3		dci_gainneg_thr4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr1	Threshold 1 for the luminance (Y) when the picture is adjusted from bright to dark
[23:16]	RW	dci_gainneg_thr2	Threshold 2 for the luminance (Y) when the picture is adjusted from bright to dark
[15:8]	RW	dci_gainneg_thr3	Threshold 3 for the luminance (Y) when the picture is adjusted from bright to dark
[7:0]	RW	dci_gainneg_thr4	Threshold 4 for the luminance (Y) when the picture is adjusted from bright to dark

ISP_VPDCINEGTHR1

ISP_VPDCINEGTHR1 is DCI adjustment unit threshold register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C50	ISP_VPDCINEGTHR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_thr5		dci_gainneg_thr6		dci_gainneg_thr7		reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr5	Threshold 5 for the luminance (Y) when the picture is adjusted from bright to dark
[23:16]	RW	dci_gainneg_thr6	Threshold 6 for the luminance (Y) when the picture is adjusted from bright to dark
[15:8]	RW	dci_gainneg_thr7	Threshold 7 for the luminance (Y) when the picture is adjusted from bright to dark
[7:0]	RO	reserved	Reserved

ISP_VPDCINEGGAIN0

ISP_VPDCINEGGAIN0 is DCI adjustment unit gain register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C54	ISP_VPDCINEGGAIN0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_cbcr0	dci_gainneg_cbcr1	dci_gainneg_cbcr2	dci_gainneg_cbcr3	dci_gainneg_cbcr4	dci_gainneg_cbcr5	dci_gainneg_cbcr6	dci_gainneg_cbcr7
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from bright to dark
[27:24]	RW	dci_gainneg_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from bright to dark
[23:20]	RW	dci_gainneg_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from bright to dark
[19:16]	RW	dci_gainneg_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from bright to dark
[15:12]	RW	dci_gainneg_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from bright to dark
[11:8]	RW	dci_gainneg_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from bright to dark
[7:4]	RW	dci_gainneg_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from bright to dark
[3:0]	RW	dci_gainneg_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from bright to dark

ISP_VPDCINEGGAIN1

ISP_VPDCINEGGAIN1 is DCI adjustment unit gain register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C58	ISP_VPDCINEGGAIN1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_cbcr8	reserved						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from bright to dark
[27:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP0

ISP_VPDCINEGSLP0 is DCI adjustment unit slope register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C5C	ISP_VPDCINEGSLP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp0		dci_gainneg_slp1		dci_gainneg_slp2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp0	Slope of region 1 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp1	Slope of region 2 when the picture is adjusted from bright to dark, 10-bit signed number
[11:2]	RW	dci_gainneg_slp2	Slope of region 3 when the picture is adjusted from bright to dark, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP1

ISP_VPDCINEGSLP1 is DCI adjustment unit slope register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C60	ISP_VPDCINEGSLP1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp3		dci_gainneg_slp4		dci_gainneg_slp5			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp3	Slope of region 4 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp4	Slope of region 5 when the picture is adjusted from bright to dark, 10-bit signed number
[11:2]	RW	dci_gainneg_slp5	Slope of region 6 when the picture is adjusted from bright to dark, 10-bit signed number

[1:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP2

ISP_VPDCINEGSLP2 is DCI adjustment unit slope register 2 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C64	ISP_VPDCINEGSLP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainneg_slp6												dci_gainneg_slp7								reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp6	Slope of region 7 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp7	Slope of region 8 when the picture is adjusted from bright to dark, 10-bit signed number
[11:0]	RO	reserved	Reserved

ISPFE_MAX_ADDR

ISPFE_MAX_ADDR is an ISP buffer maximum address register.

Offset Address	Register Name	Total Reset Value
0x60000	ISPFE_MAX_ADDR	0x0000_090F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr	Maximum address for the ISP FE buffer

ISPFE_MAX_ADDR2

ISPFE_MAX_ADDR2 is ISP buffer maximum address register 2.

Offset Address	Register Name	Total Reset Value
0x60004	ISPFE_MAX_ADDR2	0x0000_090F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr2	Maximum address for ISP FE buffer 2

ISPFE_MAX_ADDR_SINTER1

ISPFE_MAX_ADDR_SINTER1 is an ISP sinter buffer 1 maximum address register.

Offset Address	Register Name	Total Reset Value
0x60008	ISPFE_MAX_ADDR_SINTER1	0x0000_060F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_sinter1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr_sinter1	Maximum address for sinter buffer 1

ISPFE_MAX_ADDR_SINTER2

ISPFE_MAX_ADDR_SINTER2 is an ISP sinter buffer 2 maximum address register.

Offset Address	Register Name	Total Reset Value
0x6000C	ISPFE_MAX_ADDR_SINTER2	0x0000_030F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr_sinter2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr_sinter2	Maximum address for sinter buffer 2

ISPFE_TIMING

ISPFE_TIMING is an ISP timing configuration register.

Offset Address	Register Name	Total Reset Value
0x60010	ISPFE_TIMING	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								vsync_sel	hsync_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	vsync_sel	Toggle processing control for vsync 0: not processed 1: processed
[0]	RW	hsync_sel	hsync source select 0: input hsync 1: input de

ISPFE_MAX_ADDR3

ISPFE_MAX_ADDR3 is ISP buffer maximum address register 3.

Offset Address	Register Name	Total Reset Value
0x60014	ISPFE_MAX_ADDR3	0x0000_051F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					max_addr3		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 1	1 1 1 1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr3	Maximum address for ISP FE buffer 3

ISPFE_MAX_ADDR4

ISPFE_MAX_ADDR4 is ISP buffer maximum address register 4.

Offset Address	Register Name	Total Reset Value
0x60018	ISPFE_MAX_ADDR4	0x0000_051F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_addr4											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	max_addr4	Maximum address for ISP FE buffer 4

ISPFE_BYTE_EN

ISPFE_BYTE_EN is an ISP byte enable register.

Offset Address	Register Name	Total Reset Value
0x60020	ISPFE_BYTE_EN	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												byte_en			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	byte_en	Byte enable 0: disabled 1: enabled

ISPFE_CH_SWITCH

ISPFE_CH_SWITCH is an ISP input switch register.

Offset Address	Register Name	Total Reset Value
0x60028	ISPFE_CH_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											isp_ch_switch_4	reserved			isp_ch_switch_3	reserved			isp_ch_switch_2	reserved			isp_ch_switch_1	reserved			isp_ch_switch_0	reserved			isp_ch_switch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	isp_ch_switch_4	ISP FPN black frame input data select 000: channel 0 input 001: channel 1 input 010: channel 2 input 011: channel 3 input 100: FPN black frame input Other values: FPN black frame input
[19]	RO	reserved	Reserved
[18:16]	RW	isp_ch_switch_3	Input data select for ISP channel 3 000: channel 0 input 001: channel 1 input 010: channel 2 input 011: channel 3 input 100: FPN black frame input Other values: channel 3 input
[15]	RO	reserved	Reserved
[14:12]	RW	isp_ch_switch_2	Input data select for ISP channel 2 000: channel 0 input 001: channel 1 input 010: channel 2 input 011: channel 3 input 100: FPN black frame input Other values: channel 2 input
[11]	RO	reserved	Reserved

[10:8]	RW	isp_ch_switch_1	Input data select for ISP channel 1 000: channel 0 input 001: channel 1 input 010: channel 2 input 011: channel 3 input 100: FPN black frame input Other values: channel 1 input
[7]	RO	reserved	Reserved
[6:4]	RW	isp_ch_switch_0	Input data select for ISP channel 0 000: channel 0 input 001: channel 1 input 010: channel 2 input 011: channel 3 input 100: FPN black frame input Other values: channel 0 input
[3:1]	RO	reserved	Reserved
[0]	RW	isp_ch_switch_en	ISP input switch enable 0: disabled 1: enabled

ISPFE_FE_BYPASS_CFG

ISPFE_FE_BYPASS_CFG is an ISP FE bypass register.

Offset Address	Register Name	Total Reset Value
0x6002C	ISPFE_FE_BYPASS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	input_mode				reserved																											bypass_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	input_mode	ISP input mode select 00: 16-bit linear input (channel 0 data is valid after channel switch) 01: 12-bit WDR input for each channel 10: one 16-bit extended input (channel 0 is valid after ch_switch), or one 12-bit input (channel 3 is valid after ch_switch) 11: two 12-bit inputs (channels 0 and 3 are valid after ch_switch)
[29:1]	RO	reserved	Reserved
[0]	RW	bypass_en	ISP FE bypass enable 0: Data passes the ISP FE module. 1: Data bypasses the ISP FE module.

ISPFE_CROP_CFG

ISPFE_CROP_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x60030	ISPFE_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														n1_en	n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	n1_en	Region 1 enable 0: disabled 1: enabled

[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

ISPFE_CROP_WIN

ISPFE_CROP_WIN is a crop window register.

Offset Address	Register Name	Total Reset Value
0x60034	ISPFE_CROP_WIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Window height (in line). The configured value is the actual value minus 1.
[15:0]	RW	width	Window width (in pixel). The configured value is the actual value minus 1.

ISPFE_CROP0_START

ISPFE_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x60038	ISPFE_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	y_start																x_start															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	y_start	ID of the line from which the picture starts to be captured
[15:0]	RW	x_start	ID of the pixel from which the picture starts to be captured

ISPFE_CROP0_SIZE

ISPFE_CROP0_SIZE is a crop size configuration register for region 0.

Offset Address	Register Name	Total Reset Value
0x6003C	ISPFE_CROP0_SIZE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:0]	RW	width	Width (in pixel) of a line in the obtained picture. The configured value is the actual value minus 1.

ISPFE_INT

ISPFE_INT is an ISP interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x600F0	ISPFE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														fe_fstart	int_disstat	int15	int14	int13	int12	int11	int10	int9	int8	int7	int6	int5	int4	int3	int2	int1	int0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	WC	fe_fstart	ISP FE SOF interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	WC	int_disstat	DIS current frame statistics completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15]	WC	int15	ISP interrupt 15. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[14]	WC	int14	ISP interrupt 14. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	WC	int13	ISP interrupt 13. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[12]	WC	int12	ISP interrupt 12. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[11]	WC	int11	ISP interrupt 11. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[10]	WC	int10	ISP interrupt 10. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	WC	int9	ISP interrupt 9. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	WC	int8	ISP interrupt 8. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	WC	int7	ISP interrupt 7. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	int6	ISP interrupt 6. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	int5	ISP interrupt 5. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	int4	ISP interrupt 4. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	int3	ISP interrupt 3. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[2]	WC	int2	ISP interrupt 2. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	int1	ISP interrupt 1. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	int0	ISP interrupt 0. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

ISPFE_INT_MASK

ISPFE_INT_MASK is an ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x600F8	ISPFE_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														fe_fstart_en	int_disstat_en	int15_en	int14_en	int13_en	int12_en	int11_en	int10_en	int9_en	int8_en	int7_en	int6_en	int5_en	int4_en	int3_en	int2_en	int1_en	int0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	fe_fstart_en	ISP FE SOF interrupt mask 0: masked 1: enabled
[16]	RW	int_disstat_en	DIS current frame statistics completion interrupt mask 0: masked 1: enabled
[15]	RW	int15_en	ISP interrupt 15 mask 0: masked 1: enabled
[14]	RW	int14_en	ISP interrupt 14 mask 0: masked 1: enabled

[13]	RW	int13_en	ISP interrupt 13 mask 0: masked 1: enabled
[12]	RW	int12_en	ISP interrupt 12 mask 0: masked 1: enabled
[11]	RW	int11_en	ISP interrupt 11 mask 0: masked 1: enabled
[10]	RW	int10_en	ISP interrupt 10 mask 0: masked 1: enabled
[9]	RW	int9_en	ISP interrupt 9 mask 0: masked 1: enabled
[8]	RW	int8_en	ISP interrupt 8 mask 0: masked 1: enabled
[7]	RW	int7_en	ISP interrupt 7 mask 0: masked 1: enabled
[6]	RW	int6_en	ISP interrupt 6 mask 0: masked 1: enabled
[5]	RW	int5_en	ISP interrupt 5 mask 0: masked 1: enabled
[4]	RW	int4_en	ISP interrupt 4 mask 0: masked 1: enabled
[3]	RW	int3_en	ISP interrupt 3 mask 0: masked 1: enabled
[2]	RW	int2_en	ISP interrupt 2 mask 0: masked 1: enabled

[1]	RW	int1_en	ISP interrupt 1 mask 0: masked 1: enabled
[0]	RW	int0_en	ISP interrupt 0 mask 0: masked 1: enabled

ISP_DIS_CFG

ISP_DIS_CFG is a DIS enable register.

Offset Address	Register Name	Total Reset Value
0x62400	ISP_DIS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															work_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	work_en	DIS enable 0: disabled 1: enabled

ISP_DIS_BLK

ISP_DIS_BLK is a block configuration register.

Offset Address	Register Name	Total Reset Value
0x62404	ISP_DIS_BLK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								srch_range							srch_range_0	reserved								blk_size							blk_size_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:17]	RW	srch_range	Upper seven bits of the search range. The value range is 4−64.
[16]	RO	srch_range_0	Lowest bit of the search range, fixed at 0
[15:9]	RO	reserved	Reserved
[8:1]	RW	blk_size	Upper eight bits of the side length of the square block. The value range is 8−128.
[0]	RO	blk_size_0	Lowest bit of the side length of the square block, fixed at 0

ISP_DIS_V0POS

ISP_DIS_V0POS is a vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x62410	ISP_DIS_V0POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the vertical PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_V4POS

ISP_DIS_V4POS is a vertical PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x62414	ISP_DIS_V4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the vertical PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_V8POS

ISP_DIS_V8POS is a vertical PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x62418	ISP_DIS_V8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the vertical PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_V0POSE

ISP_DIS_V0POSE is a vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x62420	ISP_DIS_V0POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		ver		reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_V4POSE

ISP_DIS_V4POSE is a vertical PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x62424	ISP_DIS_V4POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		ver		reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_V8POSE

ISP_DIS_V8POSE is a vertical PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x62428	ISP_DIS_V8POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H0POS

ISP_DIS_H0POS is a horizontal PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x62430	ISP_DIS_H0POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the horizontal PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H4POS

ISP_DIS_H4POS is a horizontal PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x62434	ISP_DIS_H4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the horizontal PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H8POS

ISP_DIS_H8POS is a horizontal PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x62438	ISP_DIS_H8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the horizontal PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H0POSE

ISP_DIS_H0POSE is a horizontal PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x62440	ISP_DIS_H0POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ0 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H4POSE

ISP_DIS_H4POSE is a horizontal PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x62444	ISP_DIS_H4POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ4 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_H8POSE

ISP_DIS_H8POSE is a horizontal PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x62448	ISP_DIS_H8POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.
[15:12]	RO	reserved	Reserved
[11:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ8 block. The lowest bit of the coordinate value is excluded, and therefore the number of register bits is reduced by 1.

ISP_DIS_RAW_LUMA

ISP_DIS_RAW_LUMA is a data type register.

Offset Address	Register Name	Total Reset Value
0x62450	ISP_DIS_RAW_LUMA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															raw_luma
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	raw_luma	Input data type 0: YUV 1: RAW

ISP_DIS_GAMMA_EN

ISP_DIS_GAMMA_EN is a gamma enable register.

Offset Address	Register Name	Total Reset Value
0x62454	ISP_DIS_GAMMA_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gamma_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	gamma_en	Gamma enable 0: disabled 1: enabled

ISP_DIS_H_STAT_RADDR

ISP_DIS_H_STAT_RADDR is a horizontal statistics read address register.

Offset Address	Register Name	Total Reset Value
0x62488	ISP_DIS_H_STAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	h_stat_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	h_stat_raddr	h_delta, h_sad, and h_mv information about each block. Each address contains only one piece of information. For example: 0x00: h_delta[15:0] of block 0 0x01: h_sad[23:0] of block 0 0x02: h_mv[8:0] of block 0 … The same rule applies to other values.

ISP_DIS_H_STAT_RDATA

ISP_DIS_H_STAT_RDATA is a horizontal statistics read data register.

Offset Address	Register Name	Total Reset Value
0x6248C	ISP_DIS_H_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	h_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	h_stat_rdata	Horizontal statistics

ISP_DIS_V_STAT_RADDR

ISP_DIS_V_STAT_RADDR is a vertical statistics read address register.

Offset Address	Register Name	Total Reset Value
0x62498	ISP_DIS_V_STAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	v_stat_raddr	v_delta, v_sad, and v_mv information about each block. Each address contains only one piece of information. For example: 0x00: v_delta[15:0] of block 0 0x01: v_sad[23:0] of block 0 0x02: v_mv[8:0] of block 0 … The same rule applies to other values.

ISP_DIS_V_STAT_RDATA

ISP_DIS_V_STAT_RDATA is a vertical statistics read data register.

Offset Address	Register Name	Total Reset Value
0x6249C	ISP_DIS_V_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	v_stat_rdata	Vertical statistics

ISP_DIS_CTRL_F

ISP_DIS_CTRL_F is a DIS general control register.

Offset Address	Register Name	Total Reset Value
0x624E0	ISP_DIS_CTRL_F	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							rggb_cfg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	rggb_cfg	RGGB sequence 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_DIS_CTRL_I

ISP_DIS_CTRL_I is a DIS immediate update register.

Offset Address	Register Name	Total Reset Value
0x624E4	ISP_DIS_CTRL_I	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							update_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	ISP update mode 0: reg_newer update mode 1: frame update mode

ISP_DIS_UPDATE

ISP_DIS_UPDATE is a DIS register update register.

Offset Address	Register Name	Total Reset Value
0x624EC	ISP_DIS_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update	ISP update. This bit is automatically cleared for each frame.

ISP_FPN_CFG

ISP_FPN_CFG is an FPN configuration register.

Offset Address	Register Name	Total Reset Value
0x63a00	ISP_FPN_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						line_frame	calib_corr	reserved							enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	line_frame	FPN frame/line mode select 0: frame mode 1: line mode
[8]	RW	calib_corr	FPN correction/calibration mode select 0: correction mode 1: calibration mode
[7:1]	RO	reserved	Reserved

[0]	RW	enable	FPN enable 0: disabled 1: enabled

ISP_FPN_CALIB_START

ISP_FPN_CALIB_START is an FPN calibration start signal register.

Offset Address	Register Name	Total Reset Value
0x63a04	ISP_FPN_CALIB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															calib_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	calib_start	FPN calibration start signal. This bit is automatically cleared.

ISP_FPN_CORR_CFG

ISP_FPN_CORR_CFG is an FPN correction configuration register.

Offset Address	Register Name	Total Reset Value
0x63a08	ISP_FPN_CORR_CFG	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												correct3_en	correct2_en	correct1_en	correct0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3]	RW	correct3_en	FPN correction enable for channel 3 0: disabled 1: enabled
[2]	RW	correct2_en	FPN correction enable for channel 2 0: disabled 1: enabled
[1]	RW	correct1_en	FPN correction enable for channel 1 0: disabled 1: enabled
[0]	RW	correct0_en	FPN correction enable for channel 0 0: disabled 1: enabled

ISP_FPN_STAT

ISP_FPN_STAT is an FPN calibration status register.

Offset Address	Register Name	Total Reset Value
0x63a0C	ISP_FPN_STAT	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	hcnt				reserved	vcnt	reserved		busy
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:16]	RO	hcnt	Number of lines
[15:14]	RO	reserved	Reserved
[13:8]	RO	vcnt	Number of calibrated frames
[7:1]	RO	reserved	Reserved
[0]	RO	busy	FPN calibration status 0: idle 1: calibrated

ISP_FPN_WHITE_LEVEL

ISP_FPN_WHITE_LEVEL is an FPN calibration white point configuration register.

Offset Address	Register Name	Total Reset Value
0x63a10	ISP_FPN_WHITE_LEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				white_level											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	white_level	FPN calibration white point configuration

ISP_FPN_DIVCOEF

ISP_FPN_DIVCOEF is an FPN calibration division coefficient register.

Offset Address	Register Name	Total Reset Value
0x63a18	ISP_FPN_DIVCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				divcoef											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	divcoef	FPN calibration division coefficient

ISP_FPN_FRAMELOG2

ISP_FPN_FRAMELOG2 is an FPN calibrated frame quantity register.

Offset Address	Register Name	Total Reset Value
0x63a1C	ISP_FPN_FRAMELOG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cpi_fpn_framelog2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	cpi_fpn_framelog2	Number of FPN calibrated frames. The configured value is obtained by taking the logarithm of the number of frames to 2.

ISP_FPN_SUM0

ISP_FPN_SUM0 is an FPN calibration cumulative sum lower-bit register.

Offset Address	Register Name	Total Reset Value
0x63a20	ISP_FPN_SUM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Lower bits of the FPN calibration cumulative sum

ISP_FPN_SUM1

ISP_FPN_SUM1 is an FPN calibration cumulative sum upper-bit register.

Offset Address	Register Name	Total Reset Value
0x63a24	ISP_FPN_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Upper bits of the FPN calibration cumulative sum

ISP_FPN_CORR0

ISP_FPN_CORR0 is FPN correction configuration register 0.

Offset Address	Register Name	Total Reset Value
0x63a30	ISP_FPN_CORR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction offset

ISP_FPN_CORR1

ISP_FPN_CORR1 is FPN correction configuration register 1.

Offset Address	Register Name	Total Reset Value
0x63a34	ISP_FPN_CORR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction offset

ISP_FPN_CORR2

ISP_FPN_CORR2 is FPN correction configuration register 2.

Offset Address	Register Name	Total Reset Value
0x63a38	ISP_FPN_CORR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction offset

ISP_FPN_CORR3

ISP_FPN_CORR3 is FPN correction configuration register 3.

Offset Address	Register Name	Total Reset Value
0x63a3C	ISP_FPN_CORR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength, U8.8
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction offset

ISP_FPN_SHIFT

ISP_FPN_SHIFT is an FPN shift configuration register.

Offset Address	Register Name	Total Reset Value
0x63a40	ISP_FPN_SHIFT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	frame_calib_shift	reserved	out_shift	reserved	in_shift	reserved	fpn_shift
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	frame_calib_shift	Number of left shift bits for the last output frame during frame calibration
[23:20]	RO	reserved	Reserved
[19:16]	RW	out_shift	Number of left shift bits for the output
[15:12]	RO	reserved	Reserved
[11:8]	RW	in_shift	Number of right shift bits for the input
[7:4]	RO	reserved	Reserved
[3:0]	RW	fpn_shift	Number of right shift bits for the input FPN

ISP_FPN_MAX_O

ISP_FPN_MAX_O is an FPN maximum output value register.

Offset Address	Register Name	Total Reset Value
0x63a50	ISP_FPN_MAX_O	0x0000_3FFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				max_o			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	max_o	Maximum value of the FPN output

ISP_FPN_OVERFLOWTHR

ISP_FPN_OVERFLOWTHR is an FPN correction threshold register.

Offset Address	Register Name	Total Reset Value
0x63a54	ISP_FPN_OVERFLOWTHR	0x0000_3FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				overflowthr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	overflowthr	FPN correction threshold

ISP_FPN_LINE_WADDR

ISP_FPN_LINE_WADDR is an FPN line mode black line write address register.

Offset Address	Register Name	Total Reset Value
0x63a80	ISP_FPN_LINE_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fpn_line_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_waddr	Write address of the black line in FPN line mode

ISP_FPN_LINE_WDATA

ISP_FPN_LINE_WDATA is an FPN line mode black line write data register.

Offset Address	Register Name	Total Reset Value
0x63a84	ISP_FPN_LINE_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fpn_line_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_wdata	Write data of the black line in FPN line mode

ISP_FPN_LINE_RADDR

ISP_FPN_LINE_RADDR is an FPN line mode black line read address register.

Offset Address	Register Name	Total Reset Value
0x63a88	ISP_FPN_LINE_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fpn_line_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_raddr	Read address of the black line in FPN line mode

ISP_FPN_LINE_RDATA

ISP_FPN_LINE_RDATA is an FPN line mode black line read data register.

Offset Address	Register Name	Total Reset Value
0x63a8C	ISP_FPN_LINE_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fpn_line_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_rdata	Read data of the black line in FPN line mode

ISP_FPN_CTRL_F

ISP_FPN_CTRL_F is an FPN general control register.

Offset Address	Register Name	Total Reset Value
0x63aE0	ISP_FPN_CTRL_F	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rggb_cfg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[1:0]	RW	rggb_cfg	RGGB sequence 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_FPN_CTRL_I

ISP_FPN_CTRL_I is an FPN immediate update control register.

Offset Address	Register Name	Total Reset Value
0x63aE4	ISP_FPN_CTRL_I	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update_mode	ISP update mode 0: register update mode 1: frame update mode

ISP_FPN_TIMING

ISP_FPN_TIMING is an FPN output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x63aE8	ISP_FPN_TIMING	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cpi_fix_timing_stat											reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:1]	RW	cpi_fix_timing_stat	Manual timing parameter configuration. The length of the generated line blanking region is configured.
[0]	RO	reserved	Reserved

ISP_FPN_UPDATE

ISP_FPN_UPDATE is an FPN register update register.

Offset Address	Register Name	Total Reset Value
0x63aEC	ISP_FPN_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	update	ISP update. This bit is automatically cleared for each frame.

ISP_FPN_SIZE

ISP_FPN_SIZE is an FPN picture size register.

Offset Address	Register Name	Total Reset Value
0x63aF0	ISP_FPN_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, this field needs to be set to **1079**.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, if the actual picture width is 1920, this field needs to be set to **1919**.

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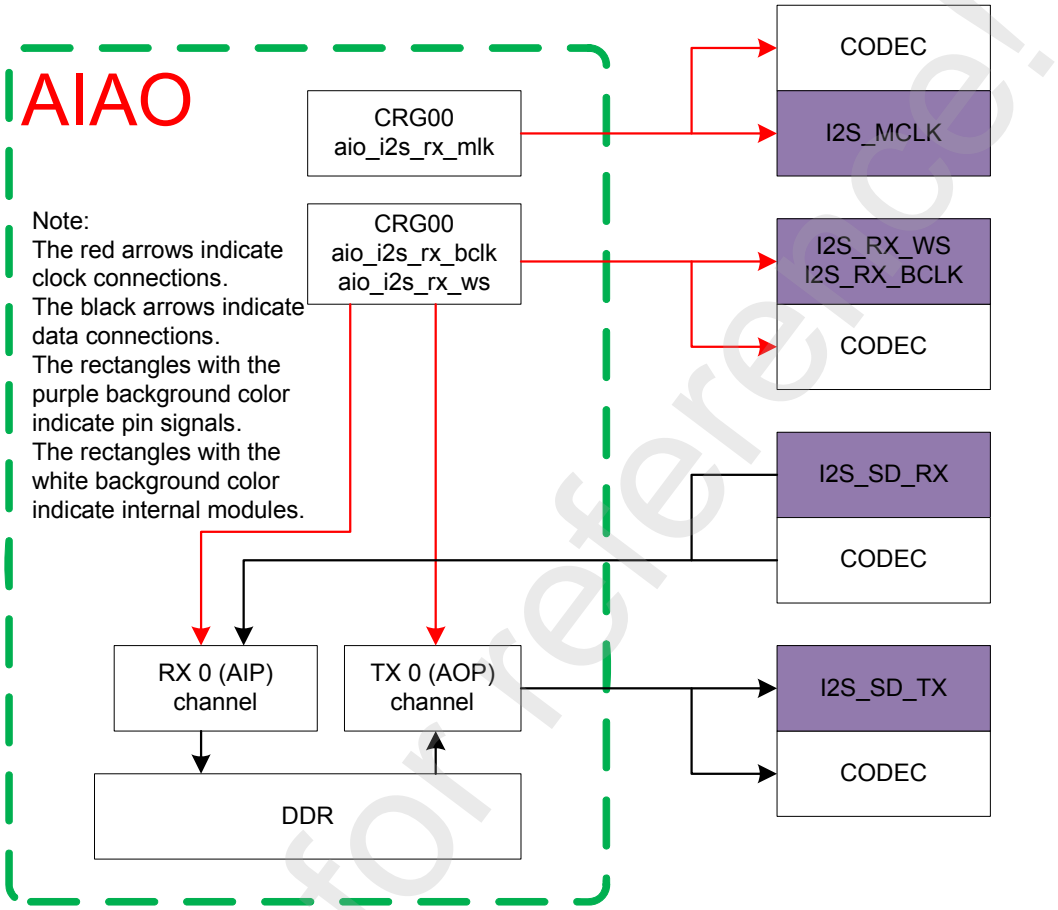
11 Audio Interfaces

11.1 AIAO

11.1.1 Overview

The audio input/output (AIAO) interface is used to connect to the off-chip audio coder/decoder (CODEC) to input and output audio data, implementing the recording, talkback, and playback functions. Hi3519 V100 has an integrated AIAO interface that includes one audio input port (AIP) and one audio output port (AOP) and supported stereo inputs and outputs. Figure 11-1 shows the block diagram of the Hi3519 V100 AIAO.

Figure 11-1 Block diagram of the Hi3519 V100 AIAO



11.1.2 Features

The AIAO interface supports the pulse code modulation (PCM) mode and inter-IC sound (I^2S) mode. The AIAO interface reads data from or writes data to the memory in DMA mode.

PCM Interfaces

The PCM interfaces have the following features:

- Transmit or receive the 16-bit linear PCM code from a channel in master mode.
- Support only short pulse sync signals in frame sync signals (the duration of those sync signals is one clock cycle). The PCM interfaces can work in both the standard mode and customized mode.
- Separately enable or disable input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

I^2S Interfaces

The I^2S interfaces have the following features:

- Transmit or receive 16- or 24-bit stereo data in master mode.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Separately enables or disables input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

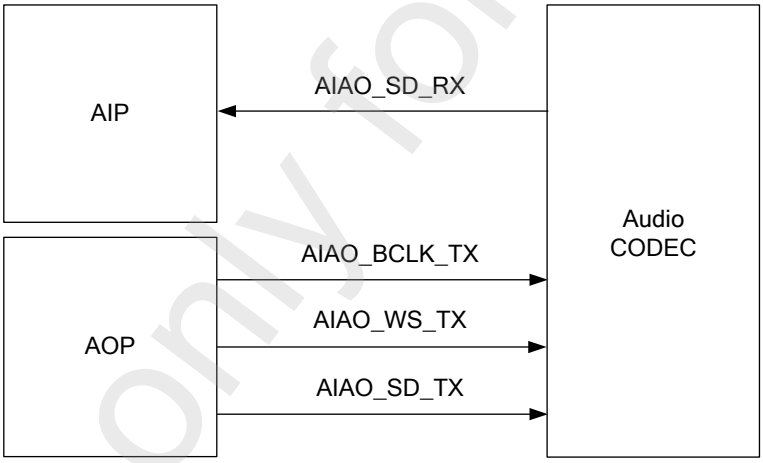
11.1.3 Function Description

Typical Application

Hi3519 V100 provides one AIP and one AOP. Their functions are as follows:

- The AIP supports data reception in PCM or I^2S mode.
- The AOP supports music playback in PCM or I^2S mode.
- The AIP supports interconnection with the internal audio CODEC in I^2S master mode or interconnection with the external analog-to-digital converter (ADC) in PCM/I^2S master mode to implement voice sampling.
- The AOP supports interconnection with the internal audio CODEC in I^2S master mode or interconnection with the external digital-to-analog converter (DAC) in PCM/I^2S master mode to implement music playback.

Figure 11-2 Connection diagram over the 4-line I^2S/PCM interface in master mode



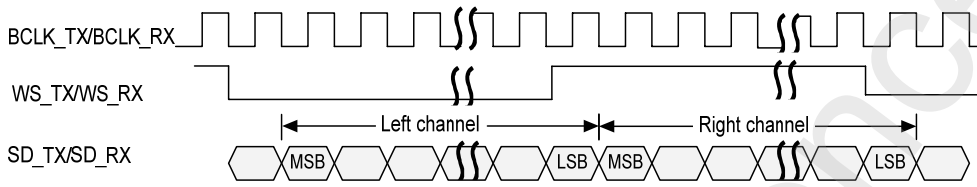
Function Principle

The AIP receives the audio data after the analog-to-digital (AD) conversion performed by the internal audio CODEC or external ADC over the I^2S or PCM interface, and stores the data into the cyclic FIFO created for the AIP. Then, the CPU fetches the data and stores it. In this way, audio recording is complete.

AOP reads audio data from the cyclic buffer and sends the audio data to the interconnected audio CODEC over the I^2S or PCM interface at a specified sampling rate. The internal audio CODEC or external ADC performs digital-to-analog (DA) conversion on the audio data and plays the audio.

Figure 11-3 shows the supported I²S interface timing when the external I²S interface is connected.

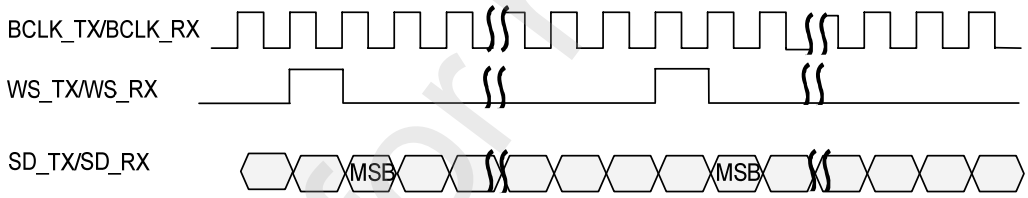
Figure 11-3 I²S interface timing



The I²S interface transmits data in most significant bit (MSB) first mode. Data and WS signals are sent at the falling edge of the BCLK and sampled at the rising edge of the BCLK. The data is delayed by one BCLK cycle compared with WS signals.

When the external PCM interface is connected, the PCM standard timing and data left-aligned timing are supported. Figure 11-4 shows the timing of the PCM interface in standard mode.

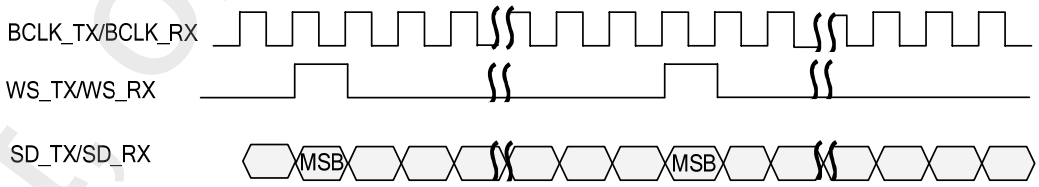
Figure 11-4 Timing of the PCM interface in standard mode



The PCM interface transmits data in MSB first mode. Data and WS signals are sent and sampled at the rising edge of the BCLK. In standard mode, the data is delayed by one BCLK cycle compared with WS signals.

Figure 11-5 shows the timing of the PCM interface in customized mode.

Figure 11-5 Timing of the PCM interface in customized mode



In customized mode, data and WS pulses start to be sent when they are in the same cycle.

11.1.4 Operating Mode

Channel Multiplexing Configuration

As there is only one AIP/AOP, the internal audio CODEC and the external ADC/DAC connected to the I²S/PCM interface cannot work simultaneously.

If the system MISC registers i2s_pad_enable and audio_enable are set to 1 and 0 respectively, the AIP/AOP connects to the external I^{2}S/PCM pin. If i2s_pad_enable and audio_enable are set to 0 and 1 respectively, the AIP/AOP connects to the internal audio CODEC.

Clock Gating and Configuration

Before enabling the AIAO interface for audio recording or playback, you must enable clock gating of the related channels (AIP/AOP). To enable clock gating, perform the following steps:

Step 1 Set the system CRG register PERI_CRG35 to 0x2 to deassert the reset on the AIAO and enable clock gating.

Step 2 Configure the AIAO registers I2S_CRG_CFG0_00 and I2S_CRG_CFG1_00 to select appropriate frequency division coefficients. Note that the MCLK/WS frequency division ratio in the i2s1_fs_sel register for the audio CODEC must be consistent with the configuration in this step when the internal audio CODEC is used.

----End

Soft Reset

The two internal channels (AIP and AOP) of the AIAO module support separate soft reset. When the AIAO module is reset, the two channels are reset at the same time.

Recording Process

The following example assumes that the audio channels are stereo channels in I^{2}S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 1188 MHz clock, and the AIAO clock of the system controller is enabled. To record data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_00 to 0x152EF0 to set the MCLK output frequency to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_00 to 0x00000133 to enable the clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set RX_IF_ATTRI to 0xe4800005 to set the operating mode of the RX channel to I^{2}S stereo mode and sampling precision to 16 bits.

Step 4 Configure RX_BUFF_SADDR to set a 24-bit start address for the allocated DDR (for example, 0x0085fe81), set RX_BUFF_SIZE to the size of the allocated DDR buffer (for example, 0x0000f000), set RX_BUFF_WPTR and RX_BUFF_RPTR to 0x0 to initialize the write and read pointers, and set RX_TRANS_SIZE to the data transfer length (for example, 0x00000f00).

Step 5 Configure RX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set RX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 6 Set RX_DSP_CTRL to 0x10000000 to enable the RX channel. Then the RX channel starts recording.

Step 7 Read RX_BUFF_WPTR and RX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that data is fetched before the cyclic buffer is full and the updated read address for the cyclic buffer is written to RX_BUFF_RPTR. Otherwise, overflow occurs in the cyclic buffer and the audio is discontinuous.

Step 8 After recording, write 0x00000000 to RX_DSP_CTRL and query RX_DSP_CTRL until its value is 0x20000000, which indicates that the RX channel stops working.

----End

CAUTION

Configure the AIP clock before starting the AIP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.

Playback Process

The following assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 1188 MHz clock, and the AIAO clock of the system controller is enabled. To play data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_00 to 0x152EF0 to set the MCLK output frequency to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_00 to 0x00000133 to enable the clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set TX_IF_ATTRI to 0xe4000005 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 4 Set TX_BUFF_SADDR to the start address for the allocated buffer (for example, 0x00452548), set TX_BUFF_SIZE to the size of the allocated buffer, set TX_BUFF_WPTR and TX_BUFF_RPTR to 0x0, and set TX_TRANS_SIZE to the data transfer length. For details, see step 5 in the "Recording Process" section.

Step 5 Configure TX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set TX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 6 Set TX_DSP_CTRL to 0x10000000 to enable the playback channel.

Step 7 Read TX_BUFF_WPTR and TX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that new audio data is stuffed before the cyclic buffer is empty and the updated write address for the cyclic buffer is written to TX_BUFF_WPTR. Otherwise, an underflow occurs in the cyclic buffer and the audio is discontinuous.

Step 8 After playback, write 0x00000000 to TX_DSP_CTRL to stop the playback channel and query TX_DSP_CTRL until its value is 0x20000000, which indicates that the playback channel stops working.

----End

CAUTION

- Configure AOP clock before starting AOP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.
- Ensure that the minimum available space of the AOP cyclic buffer is 32 bytes when writing data to the cyclic buffer and updating TX_BUFF_WPTR.

11.1.5 Register Summary

Table 11-1 describes AIAO registers.

Table 11-1 Summary of AIAO registers (base address: 0x1108_0000)

Offset Address	Register	Description	Page
0x0000	AIAO_INT_ENA	AIAO interrupt enable register	11-8
0x0004	AIAO_INT_STATUS	AIAO interrupt status register	11-9
0x0008	AIAO_INT_RAW	AIAO raw interrupt register	11-10
0x0100	I2S_CRG_CFG0_00	I^2S00 CRG configuration register 0	11-10
0x0104	I2S_CRG_CFG1_00	I^2S00 CRG configuration register 1	11-11
0x0144	I2S_CRG_CFG1_08	I^2S08 CRG configuration register 1	11-11
0x1000	RX_IF_ATTRI	Interface attribute configuration register for the RX channel	11-13
0x1004	RX_DSP_CTRL	RX channel control register	11-14
0x1080	RX_BUFF_SADDR	DDR buffer start address register for the RX channel	11-15
0x1084	RX_BUFF_SIZE	DDR buffer size register for the RX channel	11-15
0x1088	RX_BUFF_WPTR	DDR buffer write address register for the RX channel	11-15
0x108C	RX_BUFF_RPTR	DDR buffer read address register for the RX channel	11-16
0x1090	RX_BUFF_ALFULL_TH	DDR buffer almost full threshold register for the RX channel	11-16
0x1094	RX_TRANS_SIZE	Data transfer length register for the RX channel	11-17
0x10A0	RX_INT_ENA	Interrupt enable register for the RX channel	11-17
0x10A4	RX_INT_RAW	Raw interrupt register for the RX channel	11-18

Offset Address	Register	Description	Page
0x10A8	RX_INT_STATUS	Interrupt status register for the RX channel	11-19
0x10AC	RX_INT_CLR	Interrupt clear register for the RX channel	11-20
0x2000	TX_IF_ATTRI	Interface attribute configuration register for the TX channel	11-21
0x2004	TX_DSP_CTRL	TX channel control register	11-23
0x2080	TX_BUFF_SADDR	DDR buffer start address register for the TX channel	11-25
0x2084	TX_BUFF_SIZE	DDR buffer size register for the TX channel	11-25
0x2088	TX_BUFF_WPTR	DDR buffer write address register for the TX channel	11-26
0x208C	TX_BUFF_RPTR	DDR buffer read address register for the TX channel	11-26
0x2090	TX_BUFF_ALEMPTY_TH	DDR buffer almost empty threshold register for the TX channel	11-27
0x2094	TX_TRANS_SIZE	Data transfer length register for the TX channel	11-27
0x20A0	TX_INT_ENA	Interrupt enable register for the TX channel	11-27
0x20A4	TX_INT_RAW	Raw interrupt register for the TX channel	11-29
0x20A8	TX_INT_STATUS	Interrupt status register for the TX channel	11-30
0x20AC	TX_INT_CLR	Interrupt clear register for the TX channel	11-31

11.1.6 Register Description

AIAO_INT_ENA

AIAO_INT_ENA is an AIAO interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0000	AIAO_INT_ENA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			tx_ch0_int_ena	reserved			rx_ch0_int_ena

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved
[16]	RW	tx_ch0_int_ena	TX channel 0 interrupt enable 0: disabled 1: enabled
[15:1]	RW	reserved	Reserved
[0]	RW	rx_ch0_int_ena	RX channel 0 interrupt enable 0: disabled 1: enabled

AIAO_INT_STATUS

AIAO_INT_STATUS is an AIAO interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	AIAO_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_status	reserved															rx_ch0_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	tx_ch0_int_status	Interrupt status of TX channel 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:1]	RO	reserved	Reserved
[0]	RO	rx_ch0_int_status	Interrupt status of RX channel 0 0: No interrupt is generated. 1: An interrupt is generated.

AIAO_INT_RAW

AIAO_INT_RAW is an AIAO raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	AIAO_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_raw	reserved															rx_ch0_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	tx_ch0_int_raw	Raw interrupt of TX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:1]	RO	reserved	Reserved
[0]	RO	rx_ch0_int_raw	Raw interrupt of RX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

I2S_CRG_CFG0_00

I2S_CRG_CFG0_00 is I^2S00 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0100	I2S_CRG_CFG0_00	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				aiao_mclk_div																											
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:0]	RW	aiao_mclk_div	Configured value of the frequency division clock of the MCLK. The configured value is calculated as follows: (Target MCLK frequency/PLL frequency of the MCLK clock source) x 2^27. For details about the PLL frequency of the MCLK clock source, see section 3.2 "Clock" in chapter 3 "System" in the *Hi3519 V100 Economical HD IP Camera SoC Data Sheet*.

I2S_CRG_CFG1_00

I2S_CRG_CFG1_00 is I^{2}S00 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0104	I2S_CRG_CFG1_00	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						aiao_srst_req	aiao_cken	reserved			aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	aiao_srst_req	Independent soft reset request of the RX 0 channel 0: deassert reset 1: reset
[8]	RW	aiao_cken	MCLK/BCLK/WS clock gating for CRG00 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.

[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

I2S_CRG_CFG1_08

I2S_CRG_CFG1_08 is I²S08 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0144	I2S_CRG_CFG1_08	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						aiao_srst_req		reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	aiao_srst_req	Independent soft reset request of the TX 0 channel 0: deassert reset 1: reset
[8:0]	RO	reserved	Reserved

RX_IF_ATTRI

RX_IF_ATTRI is an interface attribute configuration register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1000	RX_IF_ATTRI	0xE400_0004

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7	6 5 4	3 2	1 0
Name	reserved		rx_sd_source_sel	reserved	rx_trackmode	rx_sd_offset		reserved	rx_ch_num	rx_i2s_precision	rx_mode
Reset	1 1 1 0	0 1 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 1	0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	rx_sd_source_sel	This bit is set to 0x1000 in normal mode.
[19]	RO	reserved	Reserved
[18:16]	RW	rx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** rx_trackmode is still valid in 1-channel RX mode.
[15:8]	RW	rx_sd_offset	PCM timing mode 0x0: left-aligned mode 0x1: standard mode Other values: reserved
[7]	RW	reserved	Reserved
[6:4]	RW	rx_ch_num	Number of RX channels 00: 1 01: 2 Other values: reserved

[3:2]	RW	rx_i2s_precision	Data sampling precision I²S mode: 01: 16 bits 10: 24 bits Other values: reserved PCM mode: 01: 16 bits Other values: reserved
[1:0]	RW	rx_mode	Interface mode of the RX channel 00: I²S mode 01: PCM mode Other values: reserved

RX_DSP_CTRL

RX_DSP_CTRL is an RX channel control register.

Offset Address	Register Name	Total Reset Value
0x1004	RX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		rx_disable_done	rx_enable	bypass_en	reserved																										
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	rx_disable_done	RX channel disable completion identifier 0: not complete 0: complete
[28]	RW	rx_enable	RX channel start/stop control bit 0: stop 1: start
[27]	RW	bypass_en	Data processing disable bit. The control function still takes effect after data processing is disabled. 0: Data processing is implemented normally. 1: Operations such as trackmode are not implemented.

[26:0]	RO	reserved	Reserved

RX_BUFF_SADDR

RX_BUFF_SADDR is a DDR buffer start address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1080	RX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_buff_saddr	Start address for the DDR buffer of RX channel 0. Its unit is byte. **NOTE** The start address must be 128x8-bit-aligned.

RX_BUFF_SIZE

RX_BUFF_SIZE is a DDR buffer size register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1084	RX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_size	DDR buffer size of the RX channel. Its unit is byte. **NOTE** The buffer size must be an integral multiple of 128 bytes.

RX_BUFF_WPTR

RX_BUFF_WPTR is a DDR buffer write address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1088	RX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_wptr	Write address for the DDR buffer of the RX channel. Its unit is byte. **NOTE** • The write address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The write address must be 128x2-bit-aligned.

RX_BUFF_RPTR

RX_BUFF_RPTR is a DDR buffer read address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x108C	RX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_rptr	Read address for the DDR buffer of the RX channel. Its unit is byte. **NOTE** • The read address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The software operation is performed by byte, and the hardware operation is performed based on 128 x 2-bit alignment.

RX_BUFF_ALFULL_TH

RX_BUFF_ALFULL_TH is a DDR buffer almost full threshold register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1090	RX_BUFF_ALFULL_TH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		rx_buff_alfull_th					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_alfull_th	Almost full threshold for the DDR buffer of the RX channel. Its unit is byte. If the available space of the DDR buffer is below the almost full threshold, the almost full raw interrupt is generated. **NOTE** If the rx_alfull_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x40.

RX_TRANS_SIZE

RX_TRANS_SIZE is data transfer length register for the RX interrupt.

Offset Address	Register Name	Total Reset Value
0x1094	RX_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		rx_trans_size					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_trans_size	After the RX channel receives the audio data with the length of rx_trans_size (in byte), a transfer completion interrupt is generated.

RX_INT_ENA

RX_INT_ENA is an interrupt enable register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A0	RX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_if_full_lost_int_ena	reserved	rx_stop_int_ena	reserved	rx_bfifo_full_int_ena	rx_alfull_int_ena	rx_full_int_ena	rx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rx_if_full_lost_int_ena	Interface data full loss raw interrupt enable for the RX channel 0: disabled 1: enabled
[6]	RO	reserved	Reserved
[5]	RW	rx_stop_int_ena	Stop interrupt enable for the RX channel 0: disabled 1: enabled
[4]	RO	reserved	Reserved
[3]	RW	rx_bfifo_full_int_ena	Bus fifo overflow interrupt enable for the RX channel 0: disabled 1: enabled
[2]	RW	rx_alfull_int_ena	DDR buffer almost full interrupt enable for the RX channel 0: disabled 1: enabled
[1]	RW	rx_full_int_ena	DDR buffer full interrupt for the RX channel 0: disabled 1: enabled
[0]	RW	rx_trans_int_ena	Transfer completion interrupt enable for the RX channel 0: disabled 1: enabled

RX_INT_RAW

RX_INT_RAW is a raw interrupt register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A4	RX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_if_full_lost_int_raw	reserved	rx_stop_int_raw	reserved	rx_bfifo_full_int_raw	rx_alfull_int_raw	rx_full_int_raw	rx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	rx_if_full_lost_int_raw	Data full lost raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	reserved	Reserved
[5]	RO	rx_stop_int_raw	Stop raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_bfifo_full_int_raw	Bus FIFO overflow raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	rx_alfull_int_raw	DDR buffer almost full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	rx_full_int_raw	DDR buffer full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	rx_trans_int_raw	Transfer completion raw interrupt of the RX interrupt 0: No raw interrupt is generated. 1: A raw interrupt is generated.

RX_INT_STATUS

RX_INT_STATUS is an interrupt status register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A8	RX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_if_full_lost_int_status	reserved	rx_stop_int_status	reserved	rx_bfifo_full_int_status	rx_alfull_int_status	rx_full_int_status	rx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_if_full_lost_int_status	Status of the data full loss interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	reserved	Reserved
[5]	RO	rx_stop_int_status	Status of the stop interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_bfifo_full_int_status	Status of the bus fifo overflow interrupt of the RC channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_alfull_int_status	Status of the DDR buffer almost full interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_full_int_status	Status of the DDR buffer full interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_trans_int_status	Status of the transfer completion interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.

RX_INT_CLR

RX_INT_CLR is an interrupt clear register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10AC	RX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_if_full_lost_int_clear	reserved	rx_stop_int_clear	reserved	rx_bfifo_full_int_clear	rx_alfull_int_clear	rx_full_int_clear	rx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	tx_if_full_lost_int_clear	Data full loss interrupt clear for the TX channel 0: not cleared 1: cleared
[6]	RO	reserved	Reserved
[5]	WC	rx_stop_int_clear	Stop interrupt clear for the RX channel 0: not cleared 1: cleared
[4]	RO	reserved	Reserved
[3]	WC	rx_bfifo_full_int_clear	Bus fifo overflow interrupt clear for the RX channel 0: not cleared 1: cleared
[2]	WC	rx_alfull_int_clear	DDR buffer almost full interrupt clear for the RX channel 0: not cleared 1: cleared
[1]	WC	rx_full_int_clear	DDR buffer full interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WO	rx_trans_int_clear	Transfer completion interrupt clear for the RX interrupt 0: not cleared 1: cleared

TX_IF_ATTRI

TX_IF_ATTRI is an interface attribute configuration register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2000	TX_IF_ATTRI	0xE400_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_trackmode				tx_sd_offset								reserved				tx_ch_num		tx_i2s_precision	tx_mode
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	tx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** tx_trackmode is still valid in 1-channel TX mode.
[15:8]	RW	tx_sd_offset	PCM timing mode 0x0: left-aligned mode 0x1: standard mode Other values: reserved
[7:6]	RO	reserved	Reserved
[5:4]	RW	tx_ch_num	Select of the TX channel 00: Data is transmitted by one audio channel. 01: Data is transmitted by two audio channels as stereo. Other values: reserved

[3:2]	RW	tx_i2s_precision	Data sampling precision I^{2}S mode: 01: 16 bits 10: 24 bits Other values: reserved PCM mode: 01: 16 bits Other values: reserved
[1:0]	RW	tx_mode	Interface mode of the TX channel 00: I^{2}S mode 01: PCM mode Other values: reserved

TX_DSP_CTRL

TX_DSP_CTRL is a TX channel control register.

Offset Address	Register Name	Total Reset Value
0x2004	TX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		tx_disable_done	tx_enable	bypass_en	reserved			fade_out_rate				fade_in_rate				reserved	volume							reserved						mute_fade_en	mute_en
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	tx_disable_done	TX channel disable completion identifier 0: not complete 1: complete
[28]	RW	tx_enable	TX channel start/stop control bit 0: stop 1: start

[27]	RW	bypass_en	Data processing disable bit. The control function still takes effect after data processing is disabled. 0: Data processing is implemented normally. 1: Operations such as trackmode and volume processing are not implemented.
[26:24]	RO	reserved	Reserved
[23:20]	RW	fade_out_rate	Fade-out rate 0000: The fade-out rate changes every one sampling point. 0001: The fade-out rate changes every two sampling points. 0110: The fade-out rate changes every four sampling points. 0011: The fade-out rate changes every eight sampling points. 0100: The fade-out rate changes every 16 sampling points. 0101: The fade-out rate changes every 32 sampling points. 0110: The fade-out rate changes every 64 sampling points. 0111: The fade-out rate changes every 128 sampling points. Other values: reserved
[19:16]	RW	fade_in_rate	Fade-in rate 0000: The fade-in rate changes every one sampling point. 0001: The fade-in rate changes every two sampling points. 0010: The fade-in rate changes every four sampling points. 0011: The fade-in rate changes every eight sampling points. 0100: The fade-in rate changes every 16 sampling points. 0101: The fade-in rate changes every 32 sampling points. 0110: The fade-in rate changes every 64 sampling points. 0111: The fade-in rate changes every 128 sampling points. Other values: reserved
[15]	RO	reserved	Reserved
[14:8]	RW	volume	Volume. The volume is incremented by 1 dB when the field value is incremented by 1. 0x00−0x28: mute 0x29: −80 dB 0x2A: −79 dB … 0x75: −4 dB 0x77: −2 dB 0x79: 0 dB 0x7B: +2 dB 0x7D: +4 dB 0x7F: +6 dB (maximum value)
[7:2]	RO	reserved	Reserved.

[1]	RW	mute_fade_en	Mute fade-in/fade-out control 0: disabled 1: enabled
[0]	RW	mute_en	Mute control 0: not muted 1: muted

TX_BUFF_SADDR

TX_BUFF_SADDR is a DDR buffer start address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2080	TX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_buff_saddr	Start address for the DDR buffer of the TX channel. Its unit is byte. **NOTE** The start address must be 128x8-bit-aligned.

TX_BUFF_SIZE

TX_BUFF_SIZE is a DDR buffer size register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2084	TX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_size	DDR buffer size of the TX channel. Its unit is byte. **NOTE** The buffer size must be an integral multiple of 128 bytes.

TX_BUFF_WPTR

TX_BUFF_WPTR is a DDR buffer write address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2088	TX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_wptr	Write address for the DDR buffer of the TX channel **NOTE** • The write address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The available space of the TX buffer must be greater than or equal to 128 bytes. • The software operation is performed by byte, and the hardware operation is performed by 128 x 2 bytes.

TX_BUFF_RPTR

TX_BUFF_RPTR is a DDR buffer read address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x208C	TX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_rptr	Read address for the DDR buffer of the TX channel **NOTE** • The read address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The address must be 128x2-bit-aligned.

TX_BUFF_ALEMPTY_TH

TX_BUFF_ALEMPTY_TH is a DDR buffer almost empty threshold register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2090	TX_BUFF_ALEMPTY_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_alempty_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_alempty_th	Almost empty threshold for the DDR buffer of the TX channel. Its unit is byte. If the available space of the DDR buffer is below the almost empty threshold, the almost empty raw interrupt is generated. **NOTE** If the tx_alempty_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x20.

TX_TRANS_SIZE

TX_TRANS_SIZE is a data transfer length register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2094	TX_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_trans_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_trans_size	After the TX channel transmits the audio data with the length of tx_trans_size (in byte), a transfer completion interrupt is generated.

TX_INT_ENA

TX_INT_ENA is an interrupt enable register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A0	TX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_ena	tx_mfade_int_ena	tx_stop_int_ena	tx_ififo_empty_int_ena	tx_bfifo_empty_int_ena	tx_alempty_int_ena	tx_empty_int_ena	tx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	tx_dat_break_int_ena	Interface data break interrupt enable for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	tx_mfade_int_ena	Mute fade-in/fade-output completion interrupt enable for the TX channel 0: disabled 1: enabled
[5]	RW	tx_stop_int_ena	Stop interrupt enable for the TX channel 0: disabled 1: enabled
[4]	RW	tx_ififo_empty_int_ena	Interface fifo underflow interrupt enable for the TX channel 0: disabled 1: enabled
[3]	RW	tx_bfifo_empty_int_ena	Bus fifo underflow interrupt enable for the TX channel 0: disabled 1: enabled
[2]	RW	tx_alempty_int_ena	DDR buffer almost empty interrupt enable for the TX channel 0: disabled 1: enabled
[1]	RW	tx_empty_int_ena	DDR buffer empty interrupt for the TX channel 0: disabled 1: enabled

[0]	RW	tx_trans_int_ena	Transfer completion interrupt enable for the TX channel 0: disabled 1: enabled

TX_INT_RAW

TX_INT_RAW is a raw interrupt register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A4	TX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_raw	tx_mfade_int_raw	tx_stop_int_raw	tx_ififo_empty_int_raw	tx_bfifo_empty_int_raw	tx_alempty_int_raw	tx_empty_int_raw	tx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_raw	Interface data break raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	tx_mfade_int_raw	Mute fade-in/fade-output completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RO	tx_stop_int_raw	Stop raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	tx_ififo_empty_int_raw	Interface fifo underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RO	tx_bfifo_empty_int_raw	Bus fifo underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[2]	RO	tx_alempty_int_raw	DDR buffer almost empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	tx_empty_int_raw	DDR buffer empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	tx_trans_int_raw	Transfer completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

TX_INT_STATUS

TX_INT_STATUS is an interrupt status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A8	TX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_status	tx_mfade_int_status	tx_stop_int_status	tx_ififo_empty_int_status	tx_bfifo_empty_int_status	tx_alempty_int_status	tx_empty_int_status	tx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_status	Status of the interface data break interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	tx_mfade_int_status	Status of the mute fade-in/fade-output completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	tx_stop_int_status	Status of the stop interrupt of the TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[4]	RO	tx_ififo_empty_int_status	Status of the interface FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_bfifo_empty_int_status	Status of the bus FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	tx_alempty_int_status	DDR buffer almost empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_empty_int_status	Status of the DDR buffer empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	tx_trans_int_status	Status of the transfer completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.

TX_INT_CLR

TX_INT_CLR is an interrupt clear register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20AC	TX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_clear	tx_mfade_int_clear	tx_stop_int_clear	tx_ififo_empty_int_clear	tx_bfifo_empty_int_clear	tx_alempty_int_clear	tx_empty_int_clear	tx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_clear	Interface data break interrupt clear for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[6]	WC	tx_mfade_int_clear	Mute fade-in/fade-output completion interrupt clear for the TX channel 0: not cleared 1: cleared
[5]	WC	tx_stop_int_clear	Stop interrupt clear for the TX channel 0: not cleared 1: cleared
[4]	WC	tx_ififo_empty_int_clear	Interface fifo underflow interrupt clear for the TX channel 0: not cleared 1: cleared
[3]	WC	tx_bfifo_empty_int_clear	Bus fifo underflow interrupt clear for the TX channel 0: not cleared 1: cleared
[2]	WC	tx_alempty_int_clear	DDR buffer almost empty interrupt clear for the TX channel 0: not cleared 1: cleared
[1]	WC	tx_empty_int_clear	DDR buffer empty interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WC	tx_trans_int_clear	Transfer completion interrupt clear for the TX channel 0: not cleared 1: cleared

11.2 Audio CODEC

11.2.1 Overview

The Hi3519 V100 is integrated with high-performance audio CODECs, including high-quality stereo playback DAC (96 dB DR A-weighted), two single-ended line outputs or one differential line output; high-quality stereo recording ADC (93 dB DR A-weighted), two single-ended stereo inputs or one differential input; –1.5 dB to 30 dB MIC input, and for the gain ranging from –1.5 dB to 0 dB, the gain control step is 1.5 dB; for the gain ranging from 0 dB to 30 dB, the gain control step is 2 dB. The boost gain is 20 dB. The I^2S data interface supports the 8 kHz and 192 kHz standard sampling rates simultaneously and supports digital mixing.

11.2.2 Features

The audio CODEC module has the following features:

- 96 dBA DR stereo DAC

- Single-ended stereo line output or one differential line output
- DAC digital volume control range: –121 dB to +6 dB, at 1 dB step
- 93 dBA DR stereo ADC
- Analog volume control range of ADC channel: –1.5 dB to 30 dB, at 2 dB step. The boost gain is 20 dB.
- Digital volume control range of ADC channel: –96 dB to 30 dB, at 1 dB step
- Two alternative single-ended stereo inputs or one differential input
- Provides internal MIC biasing
- Master and slave I^2S data interfaces, supporting 24 bits, 20 bits, 18 bits, and 16 bits, in binary format
- Audio sampling frequencies: 48 kHz, 44.1 kHz, and 32 kHz

  The sampling frequencies of each series are as follows:
  - The 32 kHz sampling frequencies series include 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz.
  - The 44.1 kHz sampling frequencies series include 11.025 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, and 176.4 kHz.
  - The 48 kHz sampling frequencies series include 12 kHz, 24 kHz, 48 kHz, 96 kHz, and 192 kHz.
  - The jitter tolerance of the analog clock CLKIN is 50 ps RMS.

11.2.3 Function Description

The audio CODEC module provides the recording and playing function. In the case of audio recording, analog signals are input from the MIC or line-in end, the gain is amplified at the analog part, and the signals converted into digital signals and output from the I^2S interface. Stereo recording is supported. In the case of playback, audio signals are input through the I^2S interface, converted into analog signals by the DAC, and then output. Stereo playing is supported.

Recording Mode

In recording mode, the MIC or line-in signals are input from the analog input end, processed by using the programmable gain method, converted by the ADC, filtered and volume-adjusted at the digital part, and finally output from the I^2S interface. Then, the entire recording procedure is complete.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Input analog audio signals to start recording. Signals are then output from the I^2S interface.

----End

Playing Mode

In playing mode, audio signals are transmitted from the I^2S interface to the DAC digital part for filtering and volume control, filtering is performed at the analog part, and finally output by the line-out end.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Transmit signals from the I^2S interface, and then output analog audio signals from the lineout end.

----End

11.2.4 Register Summary

The audio CODEC is directly controlled by the peripheral controller registers with the base address of 0x1203_0000. The offset addresses of these registers range from 0x00A0 to 0x00D8. That is, no interface is provided for controlling the audio CODEC.

11.2.5 Register Description

For details about the registers related to the audio CODEC, see section 3.5.5.1 "Register Summary" and section 3.5.5.2 "Register Description."

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12 Peripherals

12.1 I²C Controller

12.1.1 Overview

The inter-integrated circuit (I^2C) module is used to read or write to the slave device connected on the I^2C bus through the CPU. When writing data to and reading data from the slave device, the CPU configures the I^2C configuration register over the bus and transmits the control information and the data to be used to the I^2C data communication register. After parsing the commands, the I^2C module transmits the data of the data channel register to the slave device over I^2C bus and notifies the CPU of the final status to the CPU by using interrupts after transmitting the data. The CPU reads data from the slave device in the similar way.

12.1.2 Function Description

The I^2C module has the following features:

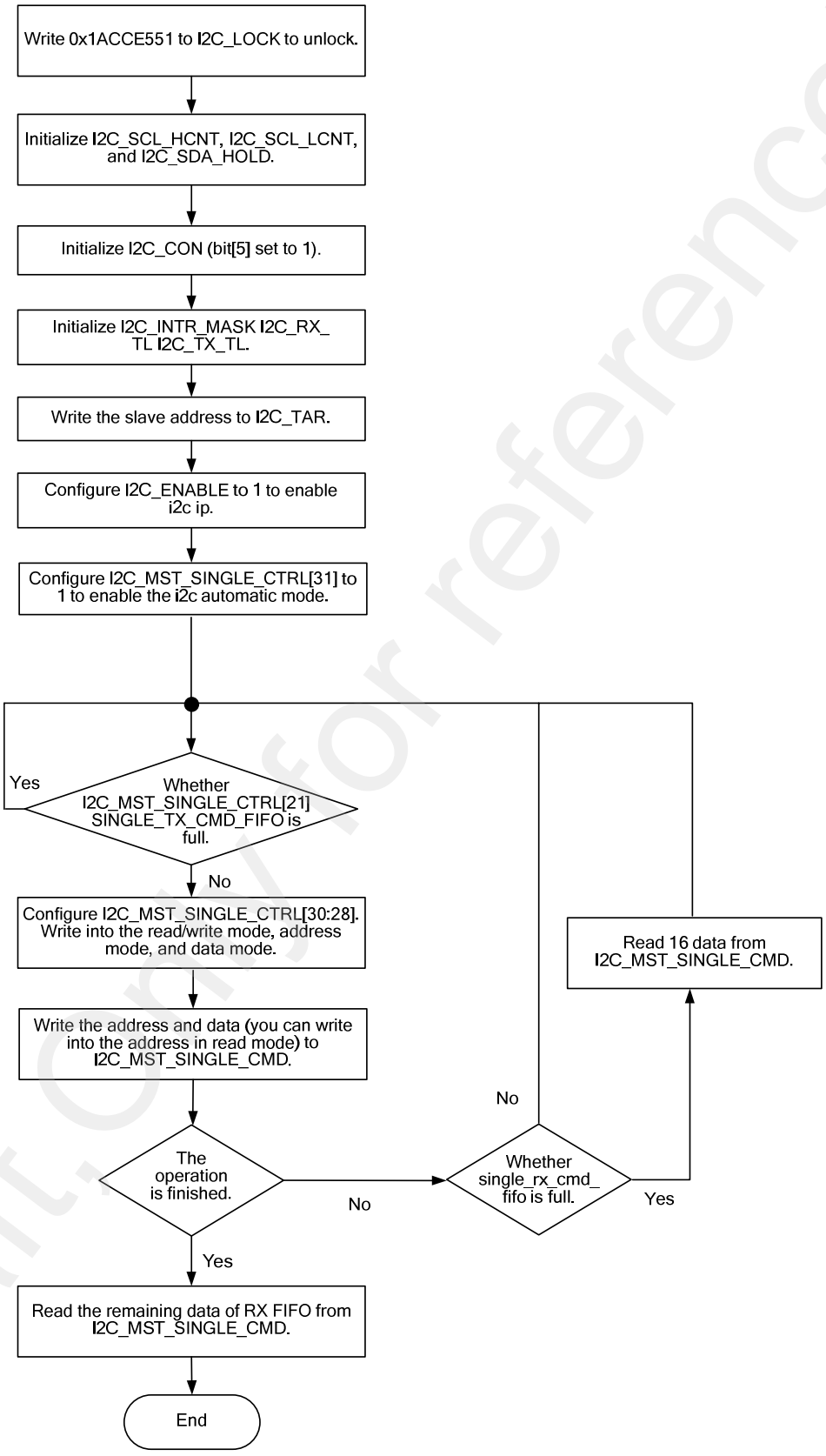
- Hi3519 V100 provides the master I^2C interface. The frequency of the I^2C working reference clock is 50 MHz.
- Supports the bus arbitration in the case of multiple master devices.
- Supports clock synchronization and bit and byte waiting.
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- CBUS components are not supported.
- Supports the DMA operation.

12.1.3 Operating Mode

Process of Receiving and Transmitting Data by a Single Operation through the I²C Master

Figure 12-1 shows the process of receiving data by a single operation through the I^2C master.

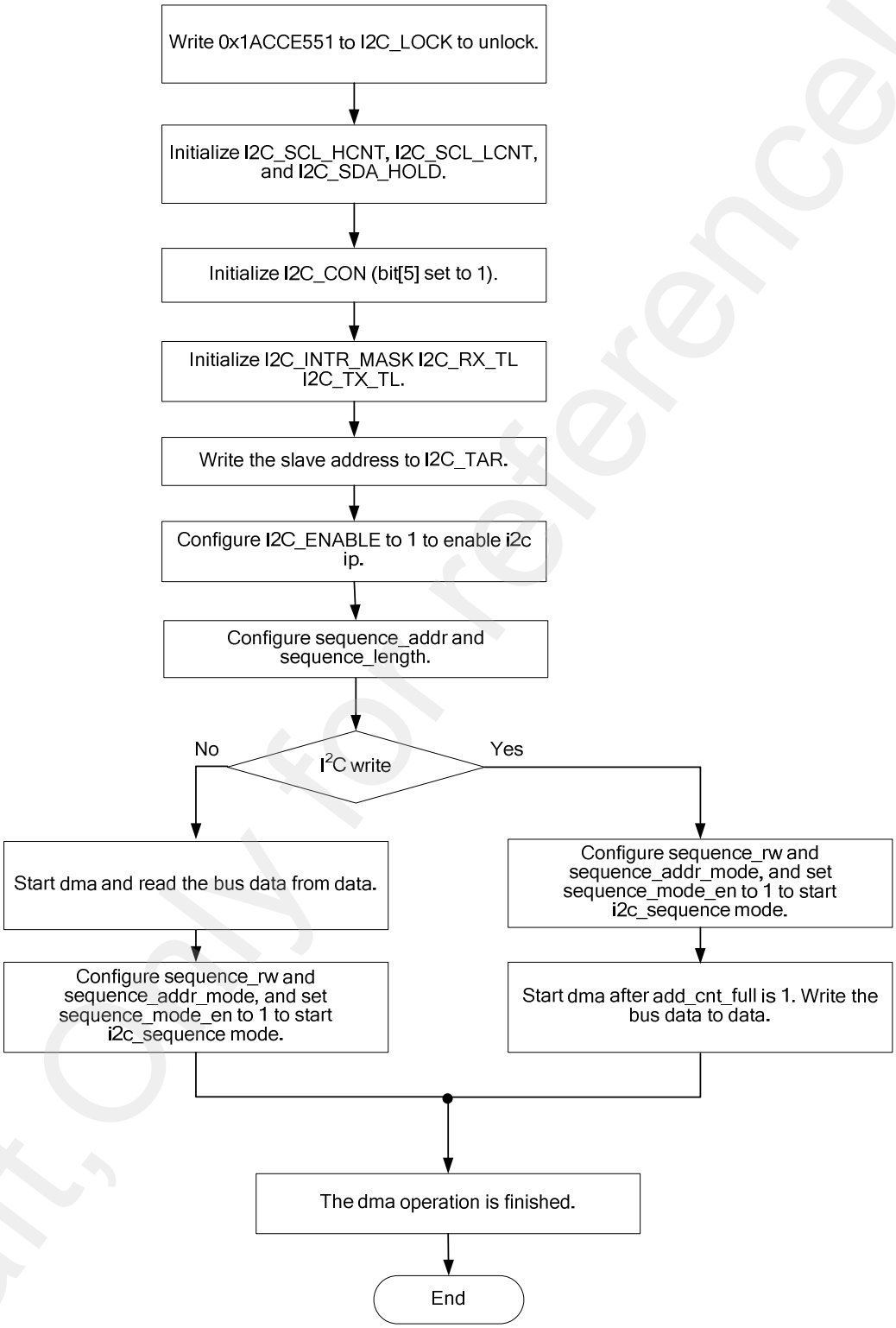
Figure 12-1 Process of receiving data by a single operation through the I²C master



Process of Continuously Receiving and Transmitting Data by the I²C Master

Figure 12-2 shows process of continuously receiving and transmitting data by the I^{2}C master.

Figure 12-2 Process of continuously receiving and transmitting data by the I²C master



12.1.4 Register Summary

Hi3519 V100 has four I²C modules. Table 12-1 describes I²C registers.

Table 12-1 Summary of I²C registers (the base addresses for I²C0, I²C1, I²C2, and I²C3 registers are 0x1211_0000, 0x1211_1000, 0x1211_2000, and 0x1211_3000 respectively)

Offset Address	Register	Description	Page
0x000	I2C_CON	I²C control register	12-6
0x004	I2C_TAR	I²C access slave device address register	12-7
0x010	I2C_DATA_CMD	I²C data operation register	12-8
0x01C	I2C_SCL_HCNT	I²C_SCL high level configuration register.	12-8
0x020	I2C_SCL_LCNT	I²C_SCL low level configuration register.	12-9
0x02C	I2C_INTR_STAT	I²C masked interrupt status register	12-10
0x030	I2C_INTR_MASK	I²C interrupt mask register	12-11
0x034	I2C_INTR_RAW	I²C raw interrupt status register	12-13
0x038	I2C_RX_TL	RX_FIFO threshold configuration register	12-15
0x03C	I2C_TX_TL	TX_FIFO threshold configuration register	12-15
0x040	I2C_CLR_INTR	I²C interrupt clear register	12-16
0x06C	I2C_ENABLE	I²C enable register	12-16
0x070	I2C_STATUS	I²C status register	12-16
0x074	I2C_TXFLR	TX_FIFO valid data indicator register	12-18
0x078	I2C_RXFLR	RX_FIFO valid data indicator register	12-18
0x07C	I2C_SDA_HOLD	SDA hold time register	12-18
0x080	I2C_TX_ABRT_SRC	I²C TX failure interrupt source register	12-19
0x088	I2C_DMA_CR	I²C DMA interface control register	12-21
0x08C	I2C_DMA_TDLR	TX_FIFO DMA operation threshold register	12-21
0x090	I2C_DMA_RDLR	RX_FIFO DMA operation threshold register	12-22
0x0A0	I2C_SCL_SWITCH	I²C anti-suspend enable register	12-22

Offset Address	Register	Description	Page
0x0A4	I2C_SCL_SIM	I^{2}C anti-suspend analog register	12-23
0x0AC	I2C_LOCK	I^{2}C lock register	12-24
0x00B0	I2C_MST_SINGLE_CTRL	I2C_MST_SINGLE_CTRL register	12-24
0x00B4	I2C_MST_SINGLE_CMD	I2C_MST_SINGLE_CMD register	12-27
0x00B8	I2C_SEQUENCE_CMD0	I2C_SEQUENCE_CMD0 register	12-27
0x00BC	I2C_SEQUENCE_CMD1	I2C_SEQUENCE_CMD1 register	12-29
0x00C0	I2C_SEQUENCE_CMD2	I2C_SEQUENCE_CMD2 register	12-29

12.1.5 Register Description

I2C_CON

I2C_CON is an I^{2}C control register.

Offset Address	Register Name	Total Reset Value
0x000	I2C_CON	0x0000_0065

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						restart_en	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0	0 1 0 1

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5]	RW	restart_en	Restart command TX enable in master mode 0: disabled 1: enabled **NOTE** If the Restart function is disabled, the following functions are not supported: 1. Sending the start bit 2. High-speed mode 3. Read operation in 10-bit addressing mode 4. Combined addressing mode
[4:0]	RO	reserved	Reserved

I2C_TAR

I2C_TAR is an I^2C access slave device address register.

Offset Address	Register Name	Total Reset Value
0x004	I2C_TAR	0x0000_002C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				master_10bit	special	gc_or_start	i2c_tar								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	master_10bit	Address length in master mode 0: 7 bits 1: 10 bits
[11]	RW	special	General call or start byte function enable 0: disabled 1: enabled
[10]	RW	gc_or_start	I^2C command to be executed when the Special bit is 1 0: general call command (After the general call command is sent, you can perform only write operations. If you perform read operations, tx_abort interrupt is triggered. For details about the definition.) 1: start byte command

[9:0]	RW	i2c_tar	Slave address that is accessed by the I²C when I²C acts as a master device **NOTE** If the address length of the slave device is set to 7 bits, only bit [6:0] are valid.

I2C_DATA_CMD

I2C_DATA_CMD is an I²C data operation register.

Offset Address	Register Name	Total Reset Value
0x010	I2C_DATA_CMD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						data	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	data	Data to be transmitted or received through the I²C bus Read: The data received from the I²C bus is read. Write: The written data is transmitted to the I²C.

I2C_SCL_HCNT

I2C_SCL_HCNT is an I²C_SCL high level configuration register.

Offset Address	Register Name	Total Reset Value
0x01C	I2C_SCL_HCNT	0x0000_0010

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				i2c_scl_hcnt			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	i2c_scl_hcnt	High-level time of the SCL clock. The timing unit is the 50 MHz I²C working reference clock. It is recommended that the field value be 1/2 of the SCL clock cycle in standard mode and be 0.36 of the SCL clock in fast mode. That is, i2c_scl_hcnt is calculated as follows: In standard mode: i2c_scl_hcnt = (fi2c/fSCL) x 0.5 In fast mode: i2c_scl_hcnt = (fi2c/fSCL) x 0.36 For example, if the 400 kHz SCL clock works in fast mode, i2c_scl_hcnt is 45 (0.36 x 50 MHz/400 kHz). **NOTE** 1. The field must be configured to obtain the appropriate I/O timing before data is transmitted through the I²C bus. 2. You can perform write operations only when the I²C interface is disabled (I2C_ENABLE = 0).

I2C_SCL_LCNT

I2C_FS_SCL_LCNT is an I²C_SCL low level configuration register.

Offset Address	Register Name	Total Reset Value
0x020	I2C_SCL_LCNT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_scl_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_scl_lcnt	Low-level time of the SCL clock. The timing unit is the 50 MHz I²C working reference clock. It is recommended that the field value be 1/2 of the SCL clock cycle in standard mode and be 0.64 of the SCL clock in fast mode. That is, i2c_scl_lcnt is calculated as follows: In standard mode: i2c_scl_lcnt = (fi2c/fSCL) x 0.5 In fast mode: i2c_scl_lcnt = (fi2c/fSCL) x 0.64 For example, if the 400 kHz SCL clock works in fast mode, i2c_scl_lcnt is 80 (0.64 x 50 MHz/400 kHz). **NOTE** 1. The field must be correctly configured to obtain the appropriate I/O timing before data is transmitted through the I²C bus. 2. You can perform write operations only when the I²C interface is disabled (I2C_ENABLE = 0).

I2C_INTR_STAT

I2C_INTR_STAT is an interrupt status register after the I^2C is masked.

Offset Address	Register Name	Total Reset Value
0x02C	I2C_INTR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RO	gen_call	Status of the interrupt indicating that a general call request is received 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	start_det	Status of the start detect interrupt indicating the I^2C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	stop_det	Status of the start detect interrupt indicating the I^2C bus interface has the STOP condition 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	activity	Activity interrupt status. The I^2C activity status is recorded until the interrupt is cleared. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	reserved	Reserved
[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Status of the interrupt indicating that TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_full	Status of the interrupt indicating that RX_FIFO reaches or is above the threshold 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_under	Read data overflow (that is, the CPU reads the FIFO when RX_FIFO is empty) interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

I2C_INTR_MASK

I2C_INTR_MASK is an I^2C interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x030	I2C_INTR_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call_mask	start_det_mask	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	gen_call_mask	Interrupt mask when a general call request is received 0: not masked 1: masked
[10]	RW	start_det_mask	Start detect interrupt mask 0: not masked 1: masked

[9]	RW	stop_det	Stop detect interrupt mask 0: not masked 1: masked
[8]	RW	activity	Activity interrupt mask 0: not masked 1: masked
[7]	RO	reserved	Reserved
[6]	RW	tx_abrt	TX abort interrupt mask 0: not masked 1: masked
[5]	RO	reserved	Reserved
[4]	RW	tx_empty	Interrupt mask when TX_FIFO reaches or is below the threshold 0: not masked 1: masked
[3]	RW	tx_over	TX_FIFO overflow interrupt mask 0: not masked 1: masked
[2]	RW	rx_full	Interrupt mask when RX_FIFO reaches or is below the threshold 0: not masked 1: masked
[1]	RW	rx_over	RX_FIFO overflow interrupt mask 0: not masked 1: masked
[0]	RW	rx_under	Interrupt mask when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: not masked 1: masked

I2C_INTR_RAW

I2C_INTR_RAW is an I²C raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x034	I2C_INTR_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RO	gen_call	Interrupt status when a general call request is received 0: No interrupt is generated. 1: The slave receives the general call. **NOTE** This bit is set to 1 only when the general call request is received and confirmed. This value is retained unless being cleared.
[10]	RO	start_det	Start detect interrupt status, indicating whether the I²C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: The START or RESTART condition is detected.
[9]	RO	stop_det	Stop detect interrupt status, indicating whether the I²C bus interface has the STOP condition 0: No interrupt is generated. 1: The STOP condition is detected.
[8]	RO	activity	Activity interrupt status. The I²C activity status is recorded until the interrupt is cleared. 0: idle 1: busy
[7]	RO	reserved	Reserved

[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When this bit is set to 1, the I2C_TX_ABRT_SRC register indicates the reason for sending the interrupt. If this bit is set to a value, the I^2C clears TX_FIFO. TX_FIFO remains in this state until the interrupt is cleared. After the interrupt is cleared, TX_FIFO reads more data over the APB interface.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Interrupt status when TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When data amount of TX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, TX_FIFO is cleared.
[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_full	Interrupt status when RX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 when RX_FIFO reaches or is below the threshold set by I2C_RX_TL. When RX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, RX_FIFO and this interrupt are automatically cleared.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 if RX_FIFO is full but still receives bytes from the external I^2C device. The I^2C responds to data received over the I^2C bus. However, bytes received after RX_FIFO is full are lost.
[0]	RO	rx_under	Interrupt status when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: No interrupt is generated. 1: An interrupt is generated.

I2C_RX_TL

I2C_RX_TL is an RX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x038	I2C_RX_TL	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	rx_tl	RX_FIFO threshold NOTE Valid values: 0–15. The actual value is the configured value plus 1. An rx_full interrupt is triggered when the number of data items in RX_FIFO is greater than or equal to the value. The upper threshold is configured as the RX_FIFO depth by default if the configured value is greater than the RX_FIFO depth.

I2C_TX_TL

I2C_TX_TL is a TX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x03C	I2C_TX_TL	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	tx_tl	TX_FIFO threshold NOTE Valid values: 0–15. The actual value is equal to the configured value. A tx_empty interrupt is triggered when the amount of data in TX_FIFO is less than or equal to the value. The upper threshold is configured as the TX_FIFO depth by default if the configured value is greater than the TX_FIFO depth.

I2C_CLR_INTR

I2C_CLR_INTR is an I^{2}C interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x040	I2C_CLR_INTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clr_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	clr_intr	Combined interrupts, all independent interrupts, and the I2C_TX_ABRT_SRC register are cleared when 1 is written to this bit.

I2C_ENABLE

I2C_ENABLE is an I^{2}C enable register.

Offset Address	Register Name	Total Reset Value
0x06C	I2C_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	enable	I^{2}C enable 0: disabled 1: enabled

I2C_STATUS

I2C_STATUS is an I^{2}C status register.

Offset Address	Register Name	Total Reset Value
0x070	I2C_STATUS	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									reserved	mst_activity	rx_fifo_full	rx_fifo_nempty	tx_fifo_nempty	tx_fifo_full	i2c_activity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RO	mst_activity	I^2C master activity status 0: The master enters the idle state, and the I^2C is deactivated. 1: The master does not enter the idle state, and the I^2C is activated.
[4]	RO	rx_fifo_full	RX_FIFO full flag 0: not full 1: full
[3]	RO	rx_fifo_nempty	RX_FIFO non-empty flag 0: empty 1: non-empty
[2]	RO	tx_fifo_nempty	TX_FIFO empty flag 0: non-empty 1: empty
[1]	RO	tx_fifo_full	TX_FIFO non-full flag 0: full 1: not full
[0]	RO	i2c_activity	I^2C operating status 0: idle 1: active

I2C_TXFLR

I2C_TXFLR is a TX_FIFO valid data indicator register.

Offset Address	Register Name	Total Reset Value
0x074	I2C_TXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	tx_flr	Number of valid data items in TX_FIFO The register is cleared when or a tx_abort interrupt is generated.

I2C_RXFLR

I2C_RXFLR is an RX_FIFO valid data indicator register.

Offset Address	Register Name	Total Reset Value
0x078	I2C_RXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	rx_flr	Number of valid data items in RX_FIFO The register is cleared when a tx_abort interrupt is generated.

I2C_SDA_HOLD

I2C_SDA_HOLD is an SDA hold time register.

Offset Address	Register Name	Total Reset Value
0x07C	I2C_SDA_HOLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sda_hold_fs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sda_hold_fs	SDA hold time. The unit is 20 ns. It is recommended that sda_hold_fs be set to I2C_SCL_LCNT[i2c_fs_lcnt]/2. **NOTE** 1. This bit indicates the delay from the SCL falling edge to SDA change. The SDA changes after the SCL falling edge and the delay (value of sda_hold_fs x cycle of i2c_clk). 2. This bit must be set based on the speed mode.

I2C_TX_ABRT_SRC

I2C_TX_ABRT_SRC is an I^{2}C TX failure interrupt source register.

Offset Address	Register Name	Total Reset Value
0x080	I2C_TX_ABRT_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved	reserved	reserved	arb_lost	reserved	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	reserved	abrt_sbyte_ackdet	reserved	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	reserved	Reserved
[14]	RO	reserved	Reserved
[13]	RO	reserved	Reserved

[12]	RO	arb_lost	Whether an error occurs after the master loses the bus control permission 0: No error occurs. 1: An error occurs.
[11]	RO	reserved	Reserved
[10]	RO	abrt_10b_rd_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and the master attempts to initiate a read operation in 10-bit mode 0: No error occurs. 1: An error occurs.
[9]	RO	abrt_sbyte_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and a user attempts to initiate a start operation 0: No error occurs. 1: An error occurs.
[8]	RO	reserved	Reserved
[7]	RO	abrt_sbyte_ackdet	Whether an error occurs when the master sends a start command and receives a response 0: No error occurs. 1: An error occurs. (The slave does not need to respond to the start command.)
[6]	RO	reserved	Reserved
[5]	RO	abrt_gcall_read	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request, but the user initiates a read operation after the request.
[4]	RO	abrt_gcall_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request but does not receive a response from the slave over the bus.
[3]	RO	abrt_txdata_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: After the master sends an address and receives a response from the slave, the master sends data to the slave but does not receive any response.
[2]	RO	abrt_10addr2_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[10:8] the second time but does not receive any response from the slave when the master operates in 10-bit mode.

[1]	RO	abrt_10addr1_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[7:0] the first time but does not receive any response from the slave when the master operates in 10-bit mode.
[0]	RO	abrt_7b_addr_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends an address but does not receive the response from any slave on the bus when the master operates in 7-bit mode.

I2C_DMA_CR

I2C_DMA_CR is an I^{2}C DMA interface control register.

Offset Address	Register Name	Total Reset Value
0x088	I2C_DMA_CR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								rdmae	tdmae
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rdmae	DMA enable for the TX FIFO 0: disabled 1: enabled
[0]	RW	tdmae	DMA enable for the RX FIFO 0: disabled 1: enabled

I2C_DMA_TDLR

I2C_DMA_TDLR is a TX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x08C	I2C_DMA_TDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_txtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_txtl	TX FIFO DMA threshold. When the number of data items of the TX FIFO is less than or equal to this value, a DMA operation request is sent. The DMA moves data to the TX FIFO.

I2C_DMA_RDLR

I2C_DMA_RDLR is an RX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x090	I2C_DMA_RDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_rxtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_rxtl	RX FIFO DMA threshold. When the number of data items of the TX FIFO is greater than or equal to this value, a DMA operation request is sent. The DMA moves data of the RX FIFO to the specified destination. The actual value is equal to the configured value plus 1.

I2C_SCL_SWITCH

I2C_SCL_SWITCH is an I^2C anti-suspend enable register.

Offset Address	Register Name	Total Reset Value
0x0A0	I2C_SCL_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_switch	Master simulate SCL signal enable 0: disabled 1: enabled

I2C_SCL_SIM

I2C_SCL_SIM is an I^2C anti-suspend analog register.

Offset Address	Register Name	Total Reset Value
0x0A4	I2C_SCL_SIM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_sim
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_sim	SCL enable signals simulated by the master 0: The output SCL is 0. 1: The output SCL is 1.

I2C_LOCK

I2C_LOCK is an I^2C lock register.

Offset Address	Register Name	Total Reset Value
0x0AC	I2C_LOCK	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															i2c_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	i2c_lock	I^2C lock register. To unlock the register, write 1ACCE551 to the register. To lock the register, write other values. When this register is read: 0: The register is unlocked, and all registers can be configured. 1: The register is locked, and only this register can be configured.

I2C_MST_SINGLE_CTRL

I2C_MST_SINGLE_CTRL is an I2C_MST_SINGLE_CTRL register.

Offset Address	Register Name	Total Reset Value
0x00B0	I2C_MST_SINGLE_CTRL	0x0030_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_model_en	single_model	single_addr_model	single_data_model	single_mst_tx_abrt_clr	single_tx_cmd_fifo_over_clr	single_rx_cmd_fifo_under_clr	single_rx_cmd_fifo_over_clr	single_mst_tx_abrt	single_tx_cmd_fifo_over	single_tx_cmd_fifo_not_full	single_tx_cmd_fifo_empty	reserved				single_tx_cmd_fifo_cnt				single_rx_cmd_fifo_under	single_rx_cmd_fifo_over	single_rx_cmd_fifo_full	single_rx_cmd_fifo_not_empty	reserved				single_rx_cmd_fifo_cnt			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	single_model_en	I^{2}C master single operation enable control 0: disabled 1: enabled
[30]	RW	single_model	I^{2}C master single operation mode control 0: write 1: read
[29]	RW	single_addr_model	I^{2}C master single operation address mode control 0: The slave register has an 8-bit address width. 1: The slave register has a 16-bit address width.
[28]	RW	single_data_model	I^{2}C master single operation data mode control 0: The slave register has an 8-bit data width. 1: The slave register has a 16-bit data width.
[27]	WC	single_mst_tx_abrt_clr	Transmission failure indicator clear in single-operation mode
[26]	WC	single_tx_cmd_fifo_over_clr	SINGLE_TX_FIFO overflow indicator clear
[25]	WC	single_rx_cmd_fifo_under_clr	SINGLE_RX_FIFO read data overflow indicator clear
[24]	WC	single_rx_cmd_fifo_over_clr	SINGLE_RX_FIFO overflow indicator clear
[23]	RO	single_mst_tx_abrt	Transmission failure indicator in single-operation mode 0: No transmission failure occurs. 1: A transmission failure occurs.

[22]	RO	single_tx_cmd_fifo_over	SINGLE_TX_FIFO overflow indicator 0: Data in SINGLE_TX_FIFO does not overflow. 1: Data in SINGLE_TX_FIFO overflows.
[21]	RO	single_tx_cmd_fifo_not_full	SINGLE_TX_FIFO non-full indicator 0: SINGLE_TX_FIFO is full. The FIFO has at least 16 data items. 1: SINGLE_TX_FIFO is not full. The FIFO has less than 16 data items.
[20]	RO	single_tx_cmd_fifo_empty	SINGLE_TX_FIFO empty indicator 0: There is data in the FIFO. 1: There is no data in the FIFO.
[19:17]	RO	reserved	Reserved
[16:12]	RO	single_tx_cmd_fifo_cnt	Number of valid data items in SINGLE_TX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL bit[31] set to 0).
[11]	RO	single_rx_cmd_fifo_under	Overflow status when read data overflows (The CPU reads the FIFO when SINGLE_RX_FIFO is empty.) 0: No read data overflows. 1: Read data overflows.
[10]	RO	single_rx_cmd_fifo_over	SINGLE_RX_FIFO overflow status 0: Data in SINGLE_RX_FIFO does not overflow. 1: Data in SINGLE_RX_FIFO overflows.
[9]	RO	single_rx_cmd_fifo_full	SINGLE_RX_FIFO full indicator 0: SINGLE_RX_FIFO is not full. The FIFO has less than 16 data items. 1: SINGLE_RX_FIFO is full. The FIFO has at least 16 data items.
[8]	RO	single_rx_cmd_fifo_not_empty	SINGLE_RX_FIFO non-empty indicator 0: There is no data in the FIFO. 1: There is data in the FIFO.
[7:5]	RO	reserved	Reserved
[4:0]	RO	single_rx_cmd_fifo_cnt	Number of valid data items in SINGLE_RX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL bit[31] set to 0).

I2C_MST_SINGLE_CMD

I2C_MST_SINGLE_CMD is an I2C_MST_SINGLE_CMD register.

Offset Address	Register Name	Total Reset Value
0x00B4	I2C_MST_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_addr																single_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	WO	single_addr	Address of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.
[15:0]	RW	single_data	Data of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD0

I2C_SEQUENCE_CMD0 is an I2C_SEQUENCE_CMD0 register.

Offset Address	Register Name	Total Reset Value
0x00B8	I2C_SEQUENCE_CMD0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_mode_en	sequential_rw	sequential_addr_mode		reserved				add_cnt_full	sequential_busy	sequential_finish		sequential_tx_fifo_cnt																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sequential_mode_en	Sequential mode enable (This function must be used together with the DMA.) 0: disabled 1: enabled
[30]	RW	sequential_rw	Operation type in sequential mode 0: read 1: write
[29:28]	RW	sequential_addr_mode	Start address type in sequential mode 00: 8 bits 01: 16 bits 10: 24 bits 11: 32 bits
[27:23]	RO	reserved	Reserved
[22]	RO	add_cnt_full	Start address transmission completion indicator, indicating that the DMA can be started
[21]	RO	sequential_busy	Operation busy indicator in sequential mode
[20]	RO	sequential_finish	Operation completion indicator in sequential mode
[19:0]	RO	sequential_tx_fifo_cnt	Number of completed operations in sequential mode

I2C_SEQUENCE_CMD1

I2C_SEQUENCE_CMD1 is an I2C_SEQUENCE_CMD1 register.

Offset Address	Register Name	Total Reset Value
0x00BC	I2C_SEQUENCE_CMD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_addr	Start address in sequential mode NOTE The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD2

I2C_SEQUENCE_CMD2 is an I2C_SEQUENCE_CMD2 register.

Offset Address	Register Name	Total Reset Value
0x00C0	I2C_SEQUENCE_CMD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_length																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_length	Sequential mode length The configured value is the actual value minus 1.

12.2 UART

12.2.1 Overview

The universal asynchronous receiver transmitter (UART) is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect Hi3519 V100 with the UART of an external chip so that the two chips can communicate with each other.

Hi3519 V100 provides five UART units (UART0 to UART4).

- UART0: 2-wire UART for debugging
- UART1/2: 4-wire UART
- UART3/4: 2-wire UART

12.2.2 Features

The UART unit has the following features:

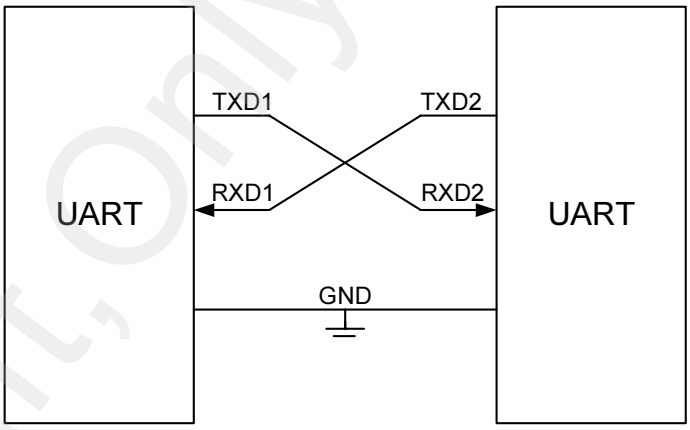
- Supports 64x8-bit transmit first-in, first-out (FIFO) and 64x12-bit RX FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports RX FIFO interrupts, TX FIFO interrupts, RX timeout interrupts, and error interrupts.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the TX/RX function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA operations.

12.2.3 Function Description

Application Block Diagram

Figure 12-3 shows the typical application of the UART.

Figure 12-3 Typical application block diagram of the UART

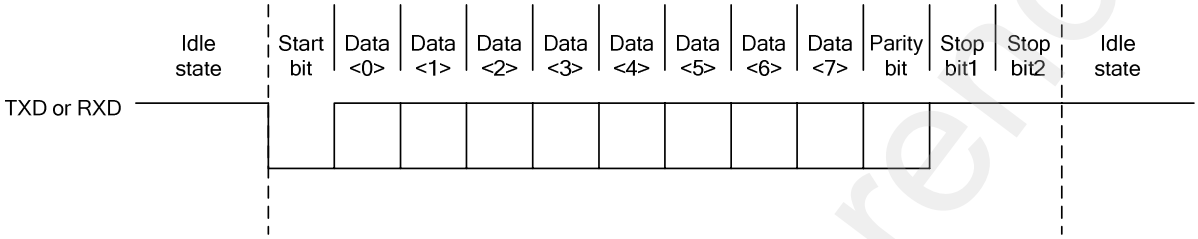


The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 12-4. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 12-4 Frame format of the UART



The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

  It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.

- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.

- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the

  UART_LCR_H register.

- Stop signal (stop bit)

  It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

12.2.4 Operating Mode

12.2.4.1 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock/(16 x Clock divider). The frequency of the UART reference clock is 24 MHz by default.

The clock frequency divider consists of the integral part and the fractional part that correspond to UART_IBRD and UART_FBRD respectively.

For example, assume that the frequency of the UART reference clock is 24 MHz. If UART_IBRD is set to 0x1E and UART_FBRD is set to 0x00, the current baud rate is calculated as follows: 24/(16 x 30) = 0.005 Mbit/s

The typical UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.

The following examples show how to calculate the clock divider and how to configure the clock divider register:

If the required baud rate is 230,400 bit/s and the frequency of the UART reference clock is 24 MHz, the clock divider is calculated as follows: $(24x10^6)/(16 \times 230,400) = 6.5104$. The integral part IBRD is 6 and the fractional part FBRD is 0.5104.

To calculate the value of the 6-bit UART_FBRD register, do as follows: calculate the value of *m* by using the following formula: $m = integer (FBRD \times 2^n + 0.5) = (0.5104 \times 2^6 + 0.5) = 33$(n = the width of UART_FBRD). Then set UART_IBRD to 0x0006 and set UART_FBRD to 0x21.

If the fractional part of the frequency divider is set to 33, the actual divisor of the baud rate is 6 + 33/64 = 6.5156, the baud rate is (24 x 16)/(16 x 605156) = 230,216.7107, and the error rate is (230,216.7107 – 230,400)/230,400 x 100 = -0.07956%.

The maximum error rate is 1/64 x 100 = 1.56% when the 6-bit UART_FBRD is used. If the value of *m* is 1, the total error rate is greater than 64 clock cycles.

12.2.4.2 Soft Reset

The UART controller can be separately reset by configuring the CRG registers.

- The UART0 controller can be separately reset by setting PERI_CRG57[uart0_srst_req] to 1.
- The UART1 controller can be separately reset by setting PPERI_CRG57[uart1_srst_req] to 1.
- The UART2 controller can be separately reset by setting PERI_CRG57[uart2_srst_req] to 1.
- The UART3 controller can be separately reset by setting PERI_CRG57[uart3_srst_req] to 1.
- The UART4 controller can be separately reset by setting PERI_CRG57[uart4_srst_req] to 1.

NOTE

For details about reset registers, see section 3.2.7 "Register Description."

After reset, the configuration registers are restored to default values. Therefore, these registers must be initialized again.

12.2.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to UART_CR bit[0] to disable the UART.

Step 2 Write to UART_IBRD and UART_FBRD to configure the transfer rate.

Step 3 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 4 Configure UART_IFLS to set the thresholds of TX and RX FIFOs.

Step 5 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.

Step 6 Write 1 to UART_CR bit[0] to enable the UART.

----End

Data Transmission

To transmit data, perform the following steps:

Step 1 Write the data to be transmitted to UART_DR and start data transmission.

Step 2 In query mode, check the TX_FIFO status by reading UART_FR bit[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.

Step 3 Check whether the UART transmits all data by reading UART_FR bit[7]. If UART_FR bit[7] is 1, the UART transmits all data.

----End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.
- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

12.2.4.4 Data Transfer in DMA Mode

Initialization

To initialize the UART, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Write values to UART_IBRD and UART_FBRD to configure the data transfer rate.

Step 3 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 4 Configure UART_IFLS to set the TX and RX FIFO thresholds.

Step 5 If the driver runs in interrupt mode, set UART_IMSC to enable corresponding interrupts. If the driver runs in query mode, disable the generation of corresponding interrupts.

Step 6 Write 1 to UART_CR[uarten] to enable the UART.

----End

Data Transfer

To transmit data, perform the following steps (the following is an example using the DMA to transmit data):

Step 1 Configure the DMA data channel, including the transfer source address, transfer destination address, number of data items to be transferred, and transfer type. For details, see the description in xx "DMAC."

Step 2 Set UART_DMACR to 0x2 to enable the DMA transfer function of the UART.

Step 3 Check whether the data is transferred completely based on the interrupt report status of the DMA. If all data is transferred, disable the DMA transfer function of the UART.

----End

Data Reception

To receive data, perform the following steps (the following is an example using the DMA to receive data):

Step 1 Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data items to be transferred, and transfer type.

Step 2 Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.

Step 3 Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

----End

12.2.5 Register Summary

Hi3519 V100 provides five UART units: UART0, UART1, UART2, UART3, and UART4. Their base addresses are as follows:

- The base address of UART0 registers is 0x1210_0000.
- The base address of UART1 registers is 0x1210_1000.
- The base address of UART2 registers is 0x1210_2000.
- The base address of UART3 registers is 0x1210_3000.
- The base address of UART4 registers is 0x1210_4000.

Table 12-2 describes the UART registers.

Table 12-2 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	12-35
0x004	UART_RSR	Receive status register or error clear register	12-36
0x018	UART_FR	Flag register	12-37

Offset Address	Register	Description	Page
0x024	UART_IBRD	Integral baud rate register	12-38
0x028	UART_FBRD	Fractional baud rate register	12-38
0x02C	UART_LCR_H	Line control register	12-39
0x030	UART_CR	Control register	12-40
0x034	UART_IFLS	Interrupt FIFO threshold select register	12-42
0x038	UART_IMSC	Interrupt mask register	12-43
0x03C	UART_RIS	Raw interrupt status register	12-44
0x040	UART_MIS	Masked interrupt status register	12-45
0x044	UART_ICR	Interrupt clear register	12-46
0x048	UART_DMACR	DMA control register	12-47

12.2.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	RO	reserved	Reserved
[11]	RO	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the RX FIFO is full.
[10]	RO	be	Break error 0: No break error occurs. 1: A break error occurs. That is, the time of RX data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.

[9]	RO	pe	Parity error 0: No parity error occurs. 1: A parity error occurs.
[8]	RO	fe	Frame error 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3]	RW	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and an overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error 0: No break error occurs. 1: A break error occurs. A break error occurs when the time of the RX data signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.

[1]	RW	pe	Parity error 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of

			UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is empty.
[3]	RO	busy	UART busy/idle status 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the TX FIFO is not empty.
[2:0]	RO	reserved	Reserved

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.

- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (216 - 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a line control register. The registers UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated, UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RW	sps	Parity select When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame 00: 5 bits 01: 6 bits 10: 7 bits

			11: 8 bits
[4]	RW	fen	TX/RX FIFO enable 0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The RX logic does not check for the 2-bit stop bit during data reception.
[2]	RW	eps	Parity select during data transmission and reception 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H[fen] is 0, this bit becomes invalid.
[1]	RW	pen	Parity enable 0: The parity is disabled. 1: The parity is generated on the TX side and checked on the RX side.
[0]	RW	brk	Break transmit 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. **NOTE** This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear UART_LCR_H[fen].

Step 4 Configure UART_CR.

Step 5 Write 1 to UART_CR[uarten] to enable the UART.

----End

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable 0: disabled 1: enabled. The data reception request is raised only when the RX FIFO has available space.
[13:12]	RO	reserved	Reserved
[11]	RW	rts	Request transmit This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.
[7]	RW	lbe	Loopback enable 0: disabled 1: UARTTXD is looped back to UARTRXD.

[6:1]	RO	reserved	Reserved
[0]	RW	uarten	UART enable 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	rxiflsel	RX interrupt FIFO threshold select. An RX interrupt is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: RX FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101–111: reserved
[2:0]	RW	txiflsel	TX interrupt FIFO threshold select. A TX interrupt is triggered when any of the following conditions is met: 000: TX FIFO ≤ 1/8 full 001: TX FIFO ≤ 1/4 full 011: TX FIFO ≤ 3/4 full 010: TX FIFO ≤ 1/2 full 100: TX FIFO ≤ 7/8 full 101–111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RW	oeim	Mask status of the overflow error interrupt 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt 0: masked 1: not masked
[6]	RW	rtim	Mask status of the RX timeout interrupt 0: masked 1: not masked
[5]	RW	txim	Mask status of the TX interrupt 0: masked 1: not masked
[4]	RW	rxim	Mask status of the RX interrupt 0: masked 1: not masked
[3:0]	RO	reserved	Reserved

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oeris	Status of the raw overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txris	Status of the raw TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oemis	Status of the masked overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txmis	Status of the masked TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	WO	oeic	Overflow error interrupt clear 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear 0: invalid 1: cleared
[6]	WO	rtic	RX timeout interrupt clear 0: invalid 1: cleared
[5]	WO	txic	TX interrupt clear 0: invalid 1: cleared
[4]	WO	rxic	RX interrupt clear 0: invalid 1: cleared
[3:0]	RO	reserved	Reserved

UART_DMACR

UART_DMACR is a DMA control register. It is used to enable or disable the DMAs of the TX and RX FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	RO	reserved	Reserved
[2]	RW	dmaonerr	DMA enable for the RX channel when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is invalid.
[1]	RW	txdmae	TX FIFO DMA enable 0: disabled 1: enable
[0]	RW	rxdmae	RX FIFO DMA enable 0: disabled 1: enable

12.3 SPI

12.3.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

12.3.2 Features

CAUTION

- Hi3519 V100 has three serial peripheral interfaces (SPIs). SPI0/2 supports a chip select (CS), whereas SPI1 supports two CSs.
- Hi3519 V100 SPIs are master interfaces. The working reference clock is the APB bus clock. SPI_CLK output by the SPI supports the maximum working frequency of 24.75 MHz.

The SPI controller has the following features:

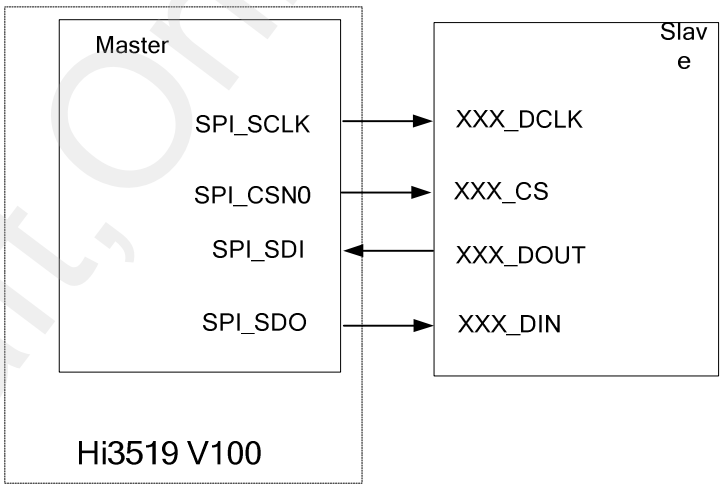
- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as an RX FIFO and the other one acts as a TX FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

12.3.3 Function Description

Typical Application

Figure 12-5 shows the application block diagram when the SPI is connected to a slave device. The default CS pin SPI_CSN0 is used.

Figure 12-5 Application block diagram when the SPI is connected to a single slave device



12.3.4 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 12-6 to Figure 12-13 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

1. **SPO = 0, SPH = 0**

Figure 12-6 shows the SPI single frame format.

Figure 12-6 SPI single frame format (SPO = 0, SPH = 0)

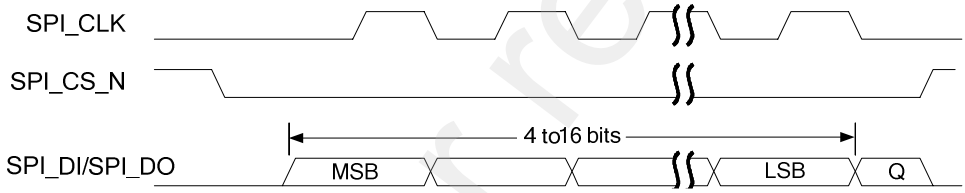
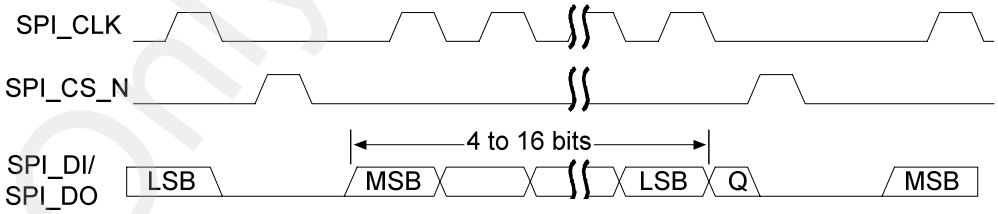


Figure 12-7 shows the SPI continuous frame format.

Figure 12-7 SPI continuous frame format (SPO = 0, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SIP_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. At this time, both the master and slave data become

valid. The SPI_CLK pin changes to high level in the next half SPI_CLK clock cycle. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For continuous transfer, the SPI_CS_N signal must pull up the SPI_CLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CS_N signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

2. **SPO = 0, SPH = 1**

Figure 12-8 shows the SPI single frame format.

Figure 12-8 SPI single frame format (SPO = 0, SPH = 1)

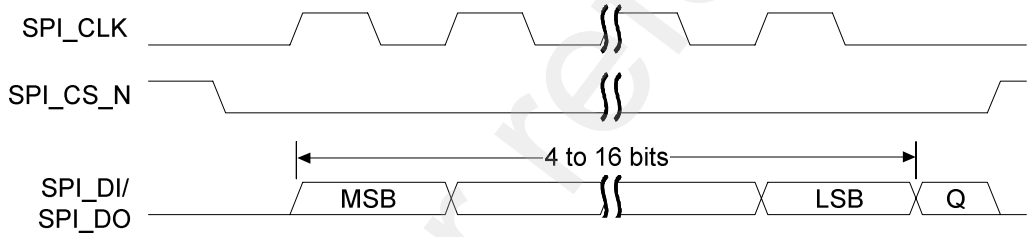
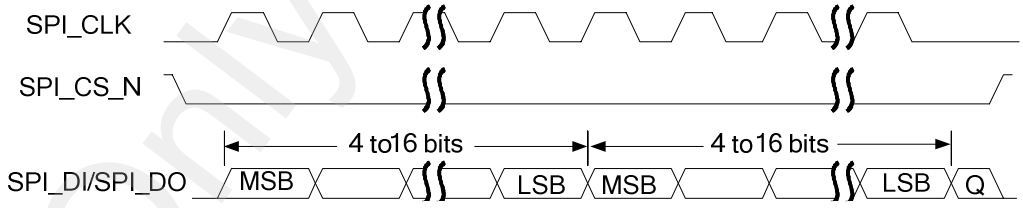


Figure 12-9 shows the SPI continuous frame format.

Figure 12-9 SPI continuous frame format (SPO = 0, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer start if the SPI_CS_N signal is set to low. The master and slave data become valid on their respective transfer line half SPI_CLK clock cycle later. In addition, SPI_CLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For a continuous transfer, SPI_CS_N remains low between the transfers of two words. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

3. **SPO = 1, SPH = 0**

Figure 12-10 shows the SPI single frame format.

Figure 12-10 SPI single frame format (SPO = 1, SPH = 0)

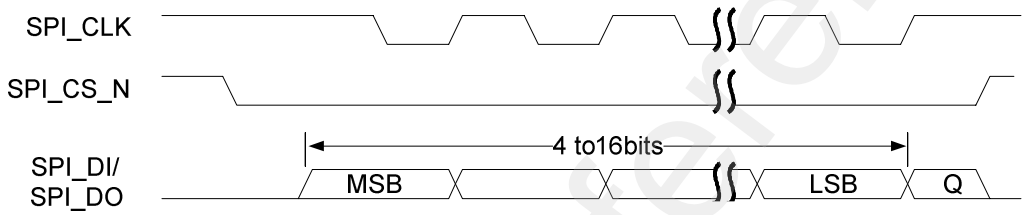
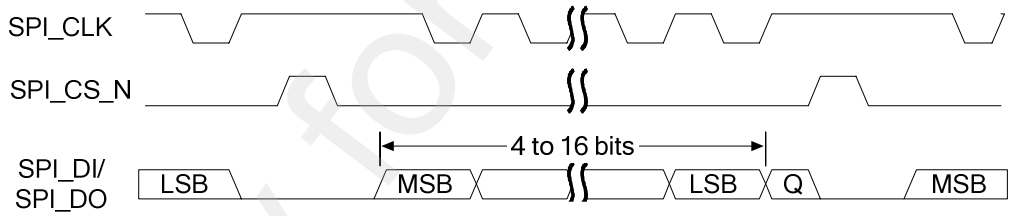


Figure 12-11 shows the SPI continuous frame format.

Figure 12-11 SPI continuous frame format (SPO = 1, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level after one SPI_CLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CS_N signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the

internal serial device register. SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

4. **SPO = 1, SPH = 1**

Figure 12-12 shows the SPI single frame format.

Figure 12-12 SPI single frame format (SPO = 1, SPH = 1)

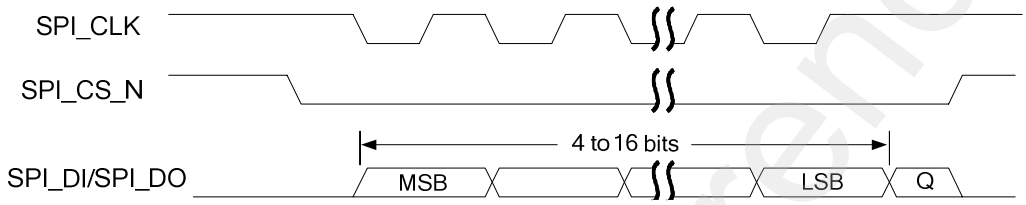
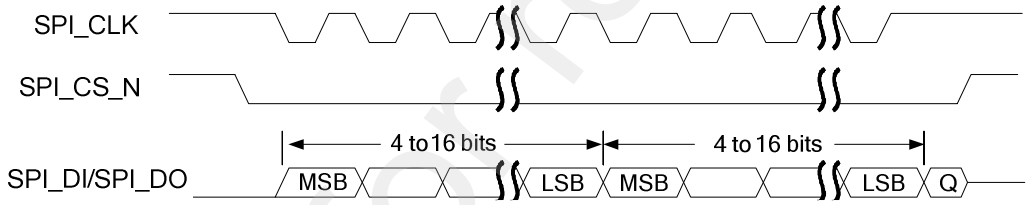


Figure 12-13 shows the SPI continuous frame format.

Figure 12-13 SPI continuous frame format (SPO = 1, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. Half SPI_CLK clock cycle later, the master data and slave data are valid on respective transfer line. In addition, SPI_CLK becomes valid from a falling edge of SPI_CLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock. If a single word is being transmitted, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CS_N signal remains low. SPI_CS_N is restored to high level one SPI_CLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CS_N remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

5. **Interface timings**

Figure 12-14 SPI timings

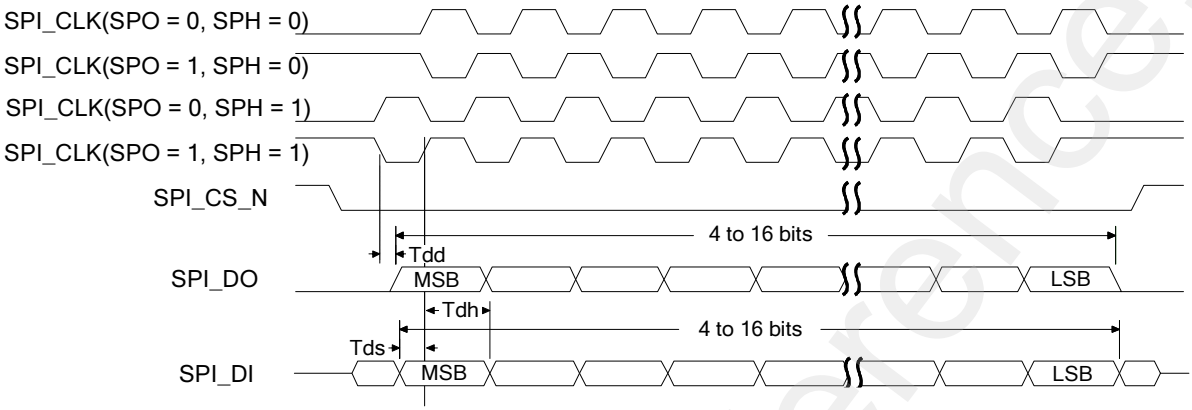


Table 12-3 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	–3.5	5	ns
Tds	Input control signal setup time	23	None	ns
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 12-15 shows the TI synchronous serial single frame format.

Figure 12-15 TI synchronous serial single frame format

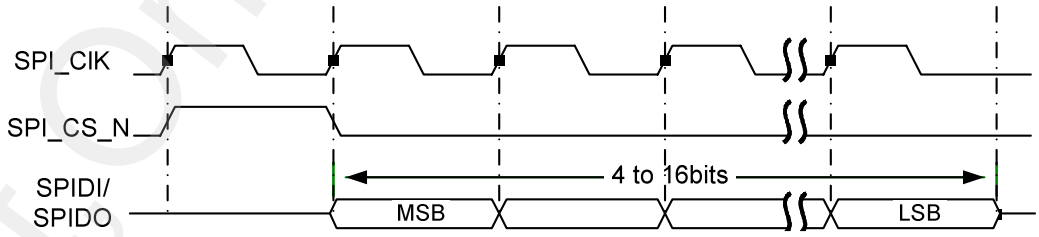
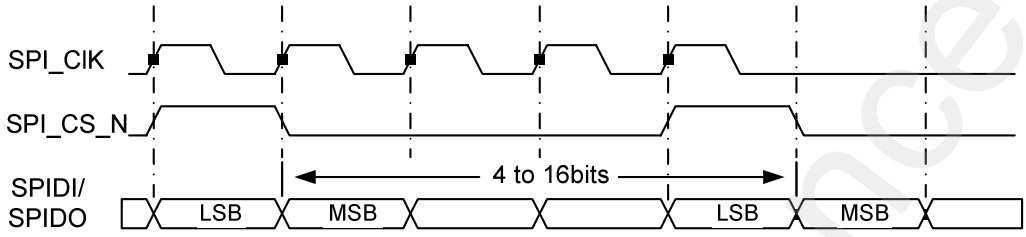


Figure 12-16 shows the TI synchronous serial continuous frame format.

Figure 12-16 TI synchronous serial continuous frame format



When the SPI is idle in this mode:

- The SPI_CK signal is set to low.
- The SPI_CS_N signal is set to low.
- The transfer data line SPI_DO retains high impedance.

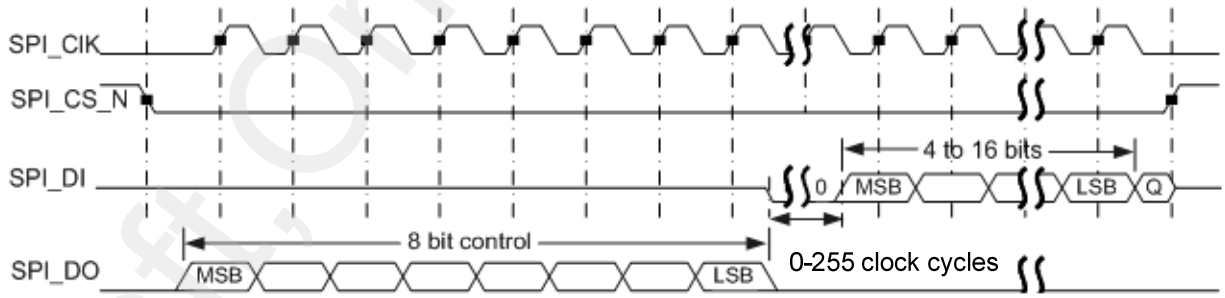
If there is data in the TX FIFO, SPI_CS_N generates a high-level pulse in one SPI_CK clock cycle. Then, the data to be transmitted is transferred from the TX FIFO to the TX logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_DO on the next rising edge of the SPI_CK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_CK clock. The RX serial register transmits the data to the RX FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 12-17 shows the national semiconductor microwire single frame format.

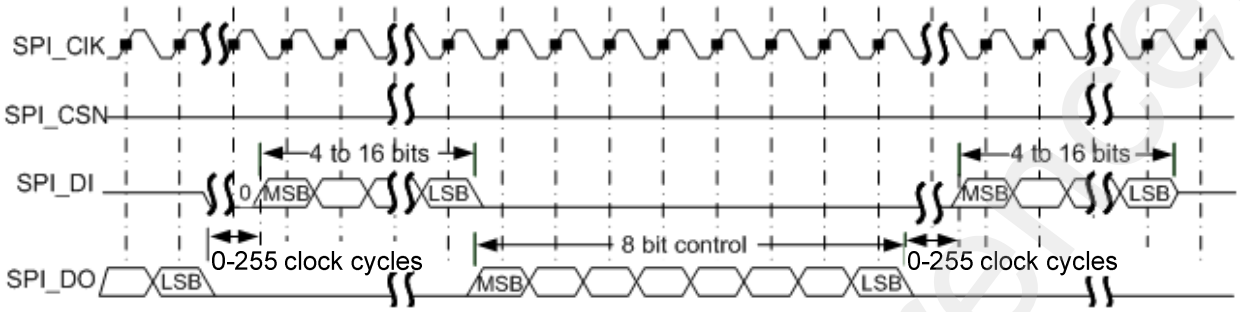
Figure 12-17 National semiconductor microwire single frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

Figure 12-18 shows the national semiconductor microwire continuous frame format.

Figure 12-18 National semiconductor microwire continuous frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high level.
- The TX data signal SPI_DO is forced to low level.

Writing one control byte to the TX FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CS_N. The data of the TX FIFO is sent to the serial shift register. The MSB of the 8-bit control frame is transmitted to the SPI_DO pin. During frame transfer, SPI_CS_N remains low. Whereas SPI_DI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_CLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_DI on the falling edge of the SPI_CK clock. For a single data transfer, SPI_CS_N is pulled up at the end of the frame one clock cycle after the last bit is written to the RX serial register. In this way, the RX data is transmitted to the RX FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CS_N retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_CLK clock.

12.3.5 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

Clock and Reset

The frequency of the output SPI clock is calculated as follows:

Fsspclkout = Fsspclk/[CPSDVR x (1 + SCR)]

Fsspclk is the working reference clock of the SPI and its value is 1/4 of the bus clock (49.5MHz).

For details about CPSDVR and SCR, query the corresponding registers.

The SPI of Hi3519 V100 supports separately soft reset, which is controlled by the PERI_CRG57 bit[6:4] register. To disable the soft reset on the SPI, write 0 to corresponding bits. To enable soft-reset on the SPI, write 1 to corresponding bits. The default value is 0 when the SPI is powered on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  RX FIFO interrupt request. When there are four or more valid data segments in the RX FIFO, the interrupt is set to 1.
- SPITXINTR

  TX FIFO interrupt request. When there are four or less valid data segments in the TX FIFO, the interrupt is set to 1.
- SPIRORINTR

  RX overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the RX shift register rather than the FIFO.
- SPIRTINTR

  RX timeout interrupt request. When the RX FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the RX FIFO needs to be transmitted. When the RX FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.
- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to SPICR1[sse] to disable the SPI.

Step 2 Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.

Step 3 Configure SPICPSR to set the required clock divider.

Step 4 In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.

Step 5 Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.

Step 6 Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

----End

Data Transfer in Query Mode

The full status of the TX or RX FIFO is not considered, because the depth of the TX FIFO or RX FIFO is 512.

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to enable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Poll SPISR until SPISR[BSY] is 0, SPISR[TFE] is 1, and SPISR[RNE] is 1. If SPISR[BSY] is 0, the bus is busy; if SPISR[TFE] is 1, the TX FIFO is empty; if SPISR[RNE] is 1, the RX FIFO is not empty.

Step 4 Read data until the RX FIFO is empty. You can check whether the RX FIFO is empty by querying SPISR[RNE].

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in Interrupt Mode

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to disable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 4 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in DMA Mode

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Write 1 to SPICR1[sse] to disable the SPI.

Step 3 Transmit data.

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SPI TX FIFO for the data transfer.
3. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.

Step 4 Receive data

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SSP RX FIFO for the data transfer.
3. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

12.3.6 Register Summary

Table 12-4 describes the registers.

- The base address of SPI0 registers is 0x1212_0000.
- The base address of SPI1 registers is 0x1212_1000.
- The base address of SPI2 registers is 0x1212_2000.

Table 12-4 Summary of SPI registers

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	12-59
0x004	SPICR1	Control register 1	12-60

Offset Address	Register	Description	Page
0x008	SPIDR	Data register	12-61
0x00C	SPISR	Status register	12-62
0x010	SPICPSR	Clock divider register	12-62
0x014	SPIIMSC	Interrupt mask register	12-63
0x018	SPIRIS	Raw interrupt status register	12-64
0x01C	SPIMIS	Masked interrupt status register	12-64
0x020	SPIICR	Interrupt clear register	12-65
0x024	SPIDMACR	DMA control register	12-65
0x028	SPITXFIFOCR	TX FIFO control register	12-66
0x02C	SPIRXFIFOCR	RX FIFO control register	12-67

12.3.7 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the TX and RX bit rates of the SPI. The formula is as follows: FSSPCLK/(CPSDVSR (1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPICLKOUT phase. For details, see section 12.3.4 "Peripheral Bus Timings."
[6]	RW	SPO	SPICLKOUT polarity. For details, see section 12.3.4 "Peripheral Bus Timings."
[5:4]	RW	FRF	Frame format select. 00: Motorola SPI frame format

			01: TI synchronous serial frame format 10: National microwire frame format 11: reserved
[3:0]	RW	DSS	Data width 0011: 4 bits 1000: 9 bits 1101: 14 bits 0100: 5 bits 1001: 10 bits 1110: 15 bits 0101: 6 bits 1010: 11 bits 1111: 16 bits 0110: 7 bits 1011: 12 bits 0111: 8 bits 1100: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved	mode_altasens	reserved	BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.

[7]	RO	reserved	Reserved
[6]	RO	mode_altasens	0: The CS signal is automatically generated by the chip logic based on the selected timing. 1: The CS signal is controlled by the SPI enable when the Motorola SPI frame format is used. If the SPI is enabled, the CS signal is pulled down; otherwise, the CS signal is pulled up.
[5]	RO	reserved	Reserved
[4]	RW	BigEnd	Data endian mode 0: little endian 1: big endian
[3]	RO	reserved	Reserved
[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: reserved
[1]	RW	SSE	SPI enable 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode 0: A normal serial port operation is enabled. 1: The output of the TX serial shift register is connected to the input of the RX serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	TX or RX FIFO Read: RX FIFO Write: TX FIFO If the data is less than 16 bits, the data must be aligned to the right. The TX logic ignores the unused upper bits, and the RX logic

			automatically aligns the data to the right.

SPISR

SPISR is a status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved
[4]	RW	BSY	SPI busy flag 0: idle 1: busy
[3]	RW	RFF	Whether the RX FIFO is full 0: not full 1: full
[2]	RW	RNE	Whether the RX FIFO is not empty 0: empty 1: not empty
[1]	RW	TNF	Whether the TX FIFO is not full 0: full 1: not full
[0]	RW	TFE	Whether the TX FIFO is empty 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	Reserved
[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the input clock SPICLK. The LSB is read as 0.

SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved
[3]	RW	TXIM	TX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the TX FIFO. 1: The interrupt is not masked when only half of or less data is left in the TX FIFO.
[2]	RW	RXIM	RX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the RX FIFO. 1: The interrupt is not masked when only half of or less data is left in the RX FIFO.
[1]	RW	RTIM	RX timeout interrupt mask 0: masked 1: not masked

[0]	RW	RORIM	RX overflow interrupt mask 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the RX FIFO is full, the SPI stops transmitting data.

SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXRIS	Raw TX FIFO interrupt status
[2]	RO	RXRIS	Raw RX FIFO interrupt status
[1]	RO	RTRIS	Raw RX timeout interrupt status
[0]	RO	RORRIS	Raw RX overflow interrupt status

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXMIS	Status of the masked TX FIFO interrupt
[2]	RO	RXMIS	Status of the masked RX FIFO interrupt
[1]	RO	RTMIS	Status of the masked RX timeout interrupt
[0]	RO	RORMIS	Status of the masked RX overflow interrupt

SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved
[1]	RO	RTIC	RX timeout interrupt clear
[0]	RO	RORIC	RX overflow interrupt clear

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved
[1]	WO	TXDMAE	DMA TX FIFO enable 0: disabled 1: enabled
[0]	WO	RXDMAE	DMA RX FIFO enable 0: disabled 1: enabled

SPITXFIFOCR

SPITXFIFOCR is a TX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	TXINTSize	Threshold for generating the TX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64

			110: 64 111: 64
[2:0]	RW	DMATXBRSize	Threshold for generating the TX FIFO request DMA transfer burst. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – DMATXBRSize), DMATXBREQ is valid. The width of the TX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

SPIRXFIFOCR

SPIRXFIFOCR is an RX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	RXINTSize	Threshold for generating the RX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the RX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the

			RX FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the TX FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

12.4 3-Wire SPI

Hi3519 V100 provides one 3-wire SPI for interconnection with the MN34120 sensor.

12.4.1 Operating Mode

The 3-wire SPI uses the APB clock as the internal working clock. To initialize the SPI interface clock, you need to calculate the SPI clock ratio based on the required frequency of the SPI clock and write the value to the SPI_3WIRE_COEF0register.

For example, if the required frequency of the SPI clock is 1 MHz, spi_clk_div is calculated as follows: spi_clk_div = (50 MHz/1 MHz)/2 – 1 = 24 (0x18 in hexadecimal). Therefore, spi_clk_div needs to be set to 0x18.

To read the SPI data, perform the following steps:

Step 1 Write the address of the read register to SPI_3WIRE_COEF1[spi_add], and write 1 to SPI_3WIRE_COEF1[spi_rw].

Step 2 Write 1 to SPI_3WIRE_COEF2[start] to start the read operation.

Step 3 Query SPI_3WIRE_COEF2[spi_busy] until this bit is 0.

Step 4 Read the required data from SPI_3WIRE_COEF2[spi_rdata].

----End

To write the SPI data, perform the following steps:

Step 1 Write the address and data of the write register to SPI_3WIRE_COEF1[spi_add] and SPI_3WIRE_COEF1[spi_wdata], and write 0 to SPI_3WIRE_COEF1[spi_rw].

Step 2 Write 1 to SPI_3WIRE_COEF2[start] to start the write operation.

Step 3 Query SPI_3WIRE_COEF2[spi_busy] until this bit is 0.

----End

12.4.2 spi_3wire_reg Register Summary

Table 12-5 describes the 3-wire SPI registers.

Table 12-5 Summary of 3-wire SPI registers (base address: 0x1212_4000)

Offset Address	Register	Description	Page
0x0000	SPI_3WIRE_COEF0	3-Wire SPI configuration register 0	12-69
0x0004	SPI_3WIRE_COEF1	3-Wire SPI configuration register 1	12-69
0x000C	SPI_3WIRE_COEF2	3-Wire SPI configuration register 2	12-70

12.4.3 spi_3wire_reg Register Description

SPI_3WIRE_COEF0

SPI_3WIRE_COEF0 is 3-wire SPI configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_3WIRE_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	spi_clk_div	SPI clock ratio. The value range is 1−255. spi_clk_div is used for generating the SPI clock. spi_clk_div is calculated as follows: spi_clk_div = (FAPBCLK/FSPICLK)/2 − 1 where FAPBCLK is the APB clock frequency. For example, the bus clock frequency is 50 MHz and the expected frequency of the SPI clock is 1 MHz, spi_clk_div is calculated as follows: spi_clk_div = (50 MHz/1 MHz)/2 – 1 =24

SPI_3WIRE_COEF1

SPI_3WIRE_COEF1 is 3-wire SPI configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_3WIRE_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_rw	spi_add															spi_wdata															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	spi_rw	SPI read/write operation select 0: write 1: read
[30:16]	RW	spi_add	SPI operation address
[15:0]	RW	spi_wdata	SPI write data

SPI_3WIRE_COEF2

SPI_3WIRE_COEF2 is 3-wire SPI configuration register 2.

Offset Address	Register Name	Total Reset Value
0x000C	SPI_3WIRE_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														spi_busy	start	spi_rdata															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	spi_busy	SPI operation status bit 1: The SPI bus is busy. 0: The SPI bus is idle.
[16]	RW	start	SPI read/write operation start. The operation can be started only when spi_busy is 0. The read back value is 0, which is meaningless.
[15:0]	RO	spi_rdata	SPI read data

12.5 MMC/SD/SDIO Controller

12.5.1 Function Description

Functional Block Diagram

The MMC/SD/SDIO controller (MMC controller for short) controls the read/write operations on the secure digital (SD) card and multimedia card (MMC), and supports various extended devices such as Bluetooth and Wi-Fi devices based on the secure digital input/output (SDIO) protocol. Hi3519 V100 provides three MMC controllers for controlling the SD card, MMC, and SDIO device.

The MMC0 controller controls the devices that comply with the following protocols:

- Secure Digital Memory (SD mem-version 3.0)
- Secure Digital I/O (SDIO-version 3.0)

The MMC1 controller controls the devices that comply with the following protocols:

- Secure Digital Memory (SD mem-version 3.0)
- Secure Digital I/O (SDIO-version 3.0)

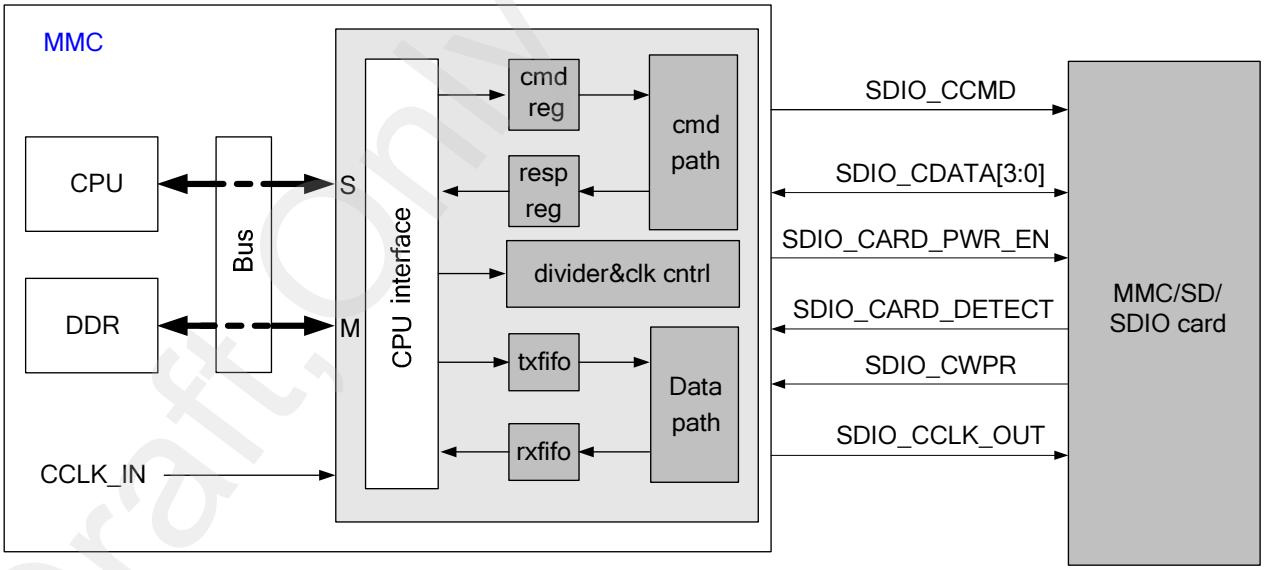
The MMC2 controller controls the devices that comply with the protocol MultiMediaCard (eMMC-version 5.0).

NOTE

To support the eMMC-version 5.0 protocol, the kernel version must be 3.16 or later.

Figure 12-19 shows the functional block diagram of the MMC controller.

Figure 12-19 Functional block diagram of the MMC controller



NOTE

S indicates slave interface and M indicates master interface.

Connected to the system through the internal bus, the MMC controller consists of the following parts:

- Command path

  It is used to transmit commands and receive responses.
- Data path

  It is used to perform data read and write operations by working with the command path.
- Interface clock control unit

  It is used to change the frequency of the interface clock as required and enable or disable the interface clock. SDIO_CLK_OUT can be generated by dividing CCLK_IN.

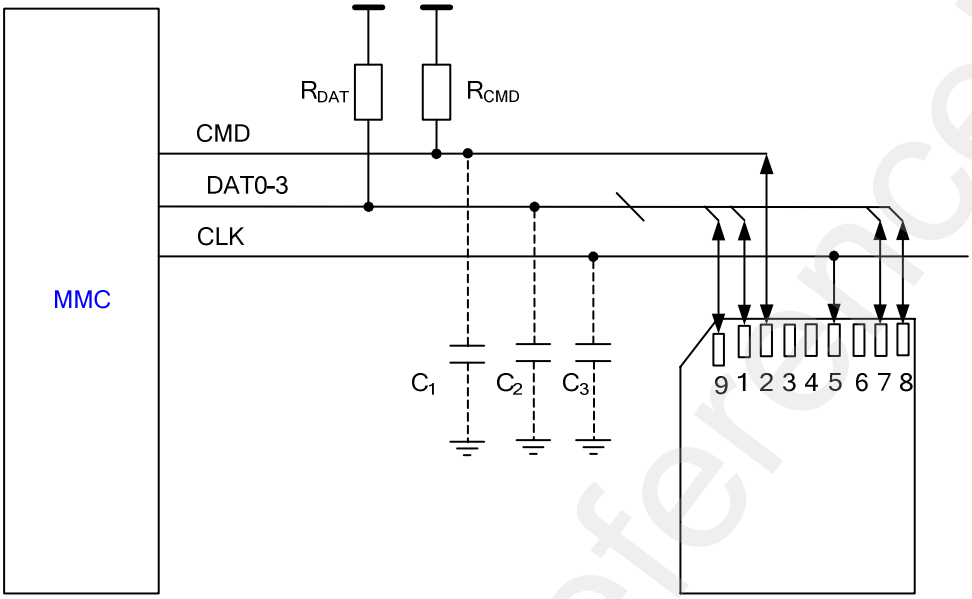
The MMC controller has the following features:

- Transfers data by using the internal direct memory access controller (IDMAC).
- Supports the ADMA3 transfer mode and allows commands to be transferred in queue.
- Supports multi-packet interrupts and timeout interrupts.
- Supports automatic detection of responses.
- Supports one TX FIFO and one RX FIFO. The depth of each FIFO is 256 words.
- Supports configurable burst size during DMA transfer and configurable FIFO threshold.
- Supports FIFO overflow and underflow interrupts to avoid errors during data transfer.
- Supports the cyclic redundancy check (CRC) generation and check for data and commands.
- Supports programmable frequency of the interface clock.
- Disables the MMC clock and interface clock in low-power mode.
- Supports 1-bit, 4-bit or 8-bit data width based on the connected component.
- Reads or writes data blocks with the size of 1 byte to 65,535 bytes.
- Reads/writes stream data from/to the MMC card.
- Supports the suspend operation, resume operation, and read wait operation on the SDIO card.
- Supports 4-bit and 8-bit DDR SDRAMs, and the GO_PRE_IDLE_STATE command for MMC 4.41.
- Supports hardware reset for eMMC 4.41.
- Supports 4-bit and 8-bit HS200 (1.8 V voltage), CMD21, CMD49, and the voltage of 3.3 V or 1.8 V for eMMC 4.5.
- Supports the HS400 mode for eMMC 5.0.

Typical Application

Figure 12-20 shows the typical application circuit of the MMC controller.

Figure 12-20 Typical application circuit of the MMC controller



The MMC controller exchanges commands and data with the connected card over a clock signal line, a bidirectional command signal line, and four bidirectional data signal lines. Both the command signal line and data signal lines work in pull-up mode. Table 12-6 describes the pull-up resistors and the load capacitance of each signal line.

Table 12-6 Load parameters of signal lines

Parameter	Min.	Max.	Description
R_{DAT} R_{CMD}	10 kΩ	100 kΩ	Pull-up resistors
Load capacitance Cx	None	30 pF	$C_x = C_{mmchost} + C_{bus} + C_{card}$The maximum capacitance of each card (C_{card}) is 10 pF; therefore, the sum of $C_{mmchost}$ and C_{bus} must be less than 30 pF.
Inductance of each signal line	None	16 nH	Fpp ≤ 20 MHz

CAUTION

Besides the signal lines in Figure 12-20, the card slot also provides the mechanical write protection signal and card detection signal. However, the signal interfaces are not provided in Figure 12-20.

Commands and Responses

All interactions between the MMC controller and the card, including initializing the card, reading/writing to registers, querying the status, and transferring data, are implemented by using commands.

A MMC command is a segment of 48-bit serial data consisting of a start bit, a transmission bit, a command sequence, a CRC bit, and an end bit. After receiving a command, the card returns a 48-bit or a 136-bit response based on the command type.

Figure 12-21 Format of an MMC command

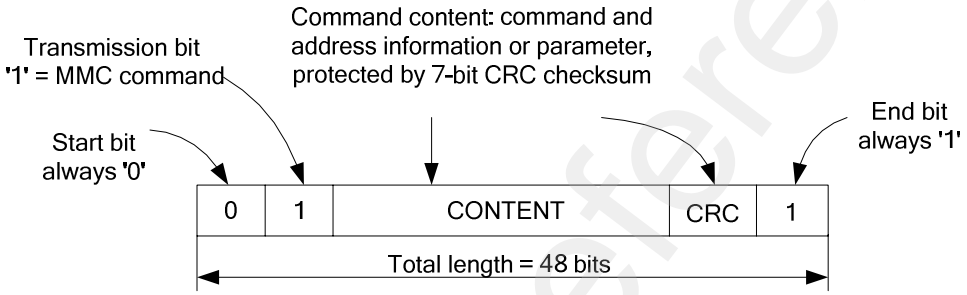
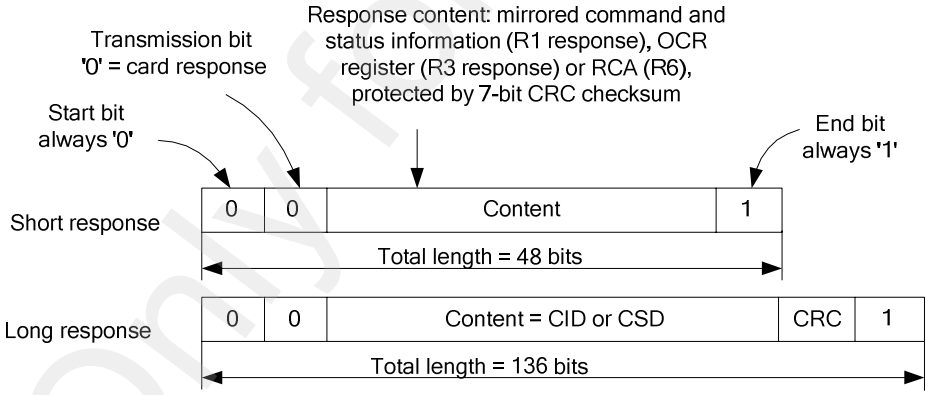


Figure 12-22 Format of the response to an MMC command



Commands are classified into the following two types based on whether data is transferred:

- Non-data transfer command

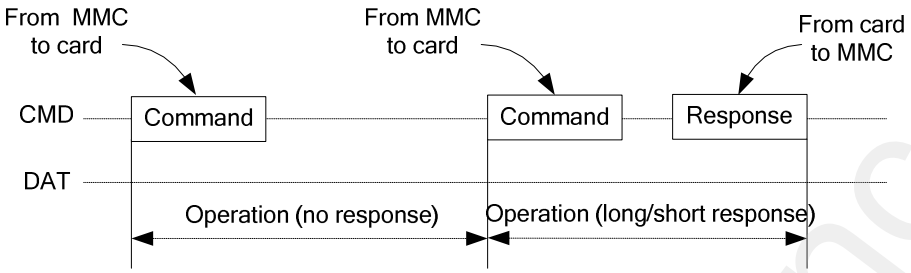
  The MMC controller transmits/receives commands to/from the card through the command signal line.
- Data transfer command

  Besides the interaction on the command line, data is also transferred through the data lines DAT0 to DAT3.

1. Non-data transfer command

Figure 12-23 shows the operations between the MMC controller and the card by running a non-data transfer command.

Figure 12-23 Operations by running an MMC non-data transfer command



2. Data transfer command

The MMC supports the following data transfer commands:

- Stream data read/write command

  Only the MMC card supports the stream data read/write command. In this case, only the data line DAT0 is used for data transfer, and no CRC check is performed.

- Single-block read/write command

  After this command is executed, one single data block is read and written each time. No stop command is required for stopping each data transfer.

- Multi-block read/write command
  - Predefined block count mode

    Before the multi-block read/write command is executed, the block count command is transmitted to specify the number of data blocks to be transferred.
  - Open-ended mode

    After a read/write command is transmitted, a stop command is required for stopping data transfer at the end of data transfer.

  The difference between the two modes lies on how the MMC controller notifies the card of the end of each data transfer. The SD card supports only the open-ended mode, whereas the MMC supports both modes.

  The multi-block read/write command for the SDIO card is different from the preceding two modes. To be specific, the command parameter contains the number of data blocks to be transferred when the read/write command is transmitted.

Responses are classified into the following three types:

- Command without response

  For example, the card reset command.

- Short response command

  For example, the data transfer command and card status query command.

- Long response command

  This type of commands are used to read only the information about the card identification (CID) and card specific data (CSD) registers of a card.

Data Transfer

The single-block read/write command and the multi-block read/write command are widely used during data transfer. The data block during the data transfer of the SD card and MMC is 512 bytes; the block size during the data transfer of the SDIO card can be customized

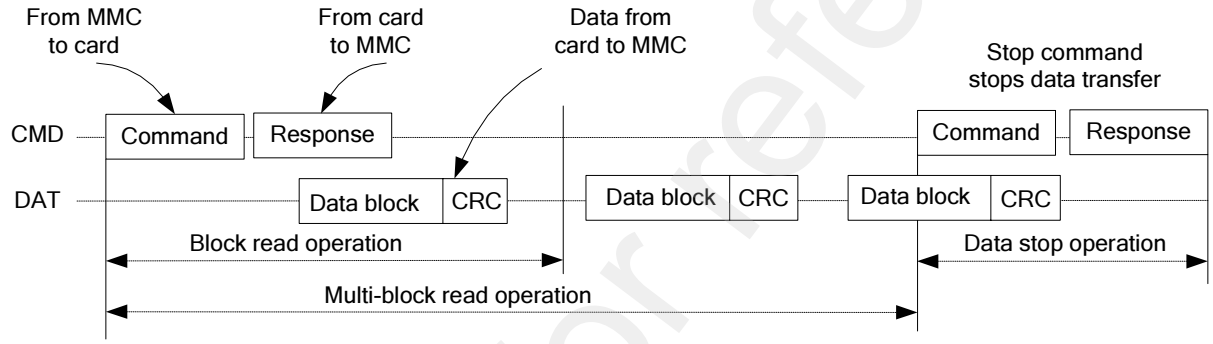
NOTE

During the data transfer by using the block read/write command, the total data amount to be transferred must be an integral multiple of the block size.

All data transfer commands are short response commands with data transferred through data lines. Figure 12-24 and Figure 12-25 show the relationships among the commands, responses, and timings of data lines.

1. Single-block and multi-block read operations

Figure 12-24 Single-block and multi-block read operations

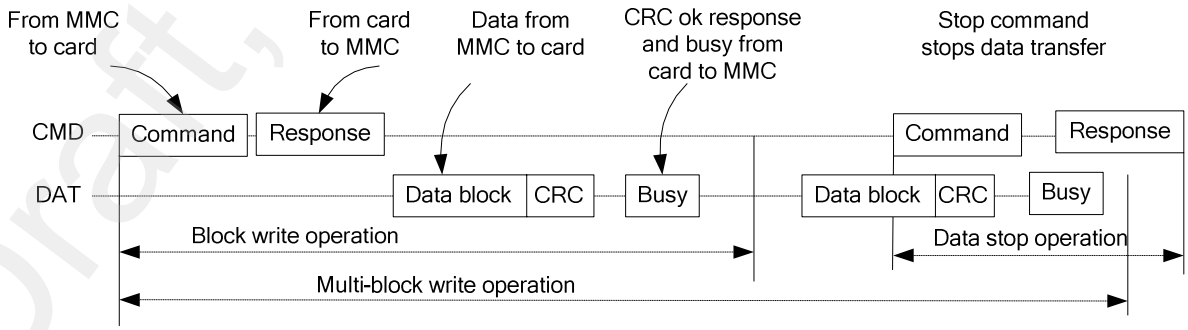


The MMC controller transmits a single-block or multi-block command to a card. When a response is being received, data is received by blocks. Each data block contains a CRC check bit for ensuring the integrity of the transferred data.

In a single-block read operation, the data transfer is completed after the MMC controller receives a data block. In a multi-block read operation, the MMC controller needs to transmit a stop command to end the data transfer after receiving multiple data blocks only in open-ended mode.

2. Single-block and multi-block read operations

Figure 12-25 Single-block and multi-block write operations



The MMC controller transmits a single-block or multi-block command to a card. After receiving a response, the MMC controller starts to transmit data to the card by blocks. Each data block contains a CRC bit. The card performs CRC on each data block and transfers the CRC status to the MMC controller. This ensures that data is transferred properly.

In a single-block write operation, the data transfer is completed after the MMC controller transmits a data block. In a multi-block write operation, the MMC controller needs to transmit a stop command to end the data transfer after transmitting multiple data blocks only in open-ended mode. After a write operation, the card may be busy in programming the flash memory. The MMC controller can perform the next operation on the card only after it confirms that the card is not busy by querying the status of the signal line DAT0.

3. Data transfer format

During the block read/write operations, the 1- or 4-bit data line can be used to transfer data between the MMC controller and the card. Before a data transfer command is transmitted, the data transfer widths of the MMC controller and card must be the same (1 bit or 4 bits). You can set the data bit width of the MMC controller by configuring MMC_CTYPE and set the data bit width of the card by transmitting the corresponding command.

Figure 12-26 shows the data transfer format in 1-bit mode, and Figure 12-27 shows the data transfer format in 4-bit mode.

Figure 12-26 Data transfer format in 1-bit mode

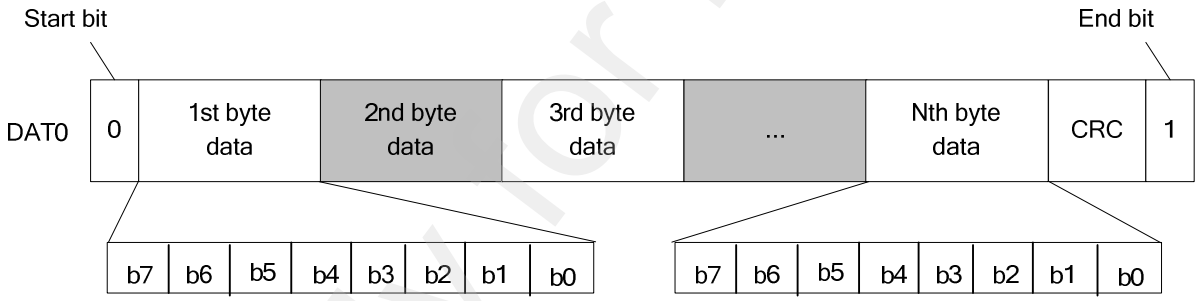
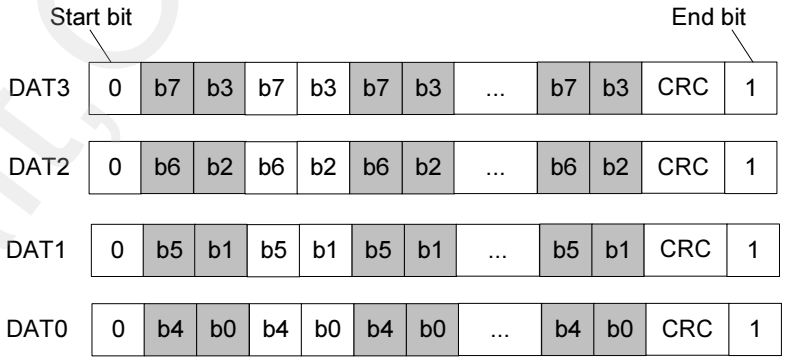


Figure 12-27 Data transfer format in 4-bit mode



Speed Mode and Voltage Switching Supported by SD3.0

The MMC controller supports SD 3.0 ultra high speed (UHS-1) and allows the voltage to be switched in SD mode. Table 12-7 describes the relationship between the transmission modes and voltages.

Table 12-7 Transmission mode

Mode	Input Clock (MHz)	Clock on the Card Side	Maximum Data Bit Width	Voltage
SDR104	200 MHz	200 MHz	4 bits	1.8 V
SDR50	100 MHz	100 MHz	4 bits	1.8 V
DDR50	50 MHz	50 MHz	4 bits	1.8 V
SDR25	50 MHz	50 MHz	4 bits	1.8 V
SDR12	25 MHz	25 MHz	4 bits	1.8 V
HS	50 MHz	50 MHz	4 bits	3.3 V
DS	25 MHz	25 MHz	4 bits	3.3 V
HS400	150 MHz	150 MHz	8 bits	1.8 V
HS200	200 MHz	200 MHz	8 bits	1.8 V
DDR-4bit	50 MHz	50 MHz	4 bits	3.3 V
DDR-8bit	100 MHz	50 MHz	8 bits	3.3 V
MMC HS	50 MHz	50 MHz	4 bits	3.3 V

12.5.2 Application Notes

NOTE

For details about clock reset registers, see section 3.2.7 "Register Description."

Clock Gating

When the software completes the current command or data transfer and does not start a new data transfer, the SDIO_CCLK_OUT clock can be disabled if the MMC controller is idle.

Perform the following steps:

Step 1 Read MMC_STATUS.

Step 2 If both MMC_STATUS[Command fsm_states] and MMC_STATUS[data_state_mc_busy] are 0, write 0 to MMC_CTRL to mask the MMC interrupt and enable the DMA request, and go to step 3. If any of the two fields is not 0, wait and go to step 1.

Step 3 Write 0 to PERI_CRG49 bit[9], bit[1], and bit[17] to disable the SDIO0, SDIO1, and SDIO2(eMMC) clocks respectively.

NOTE

To enable the SDIO0, SDIO1, and SDIO2 working clocks, write 1 to PERI_CRG49 bit[9], bit[1], and bit[17] respectively.

----End

Soft Reset

If the MMC controller cannot be restored to the idle state due to data transfer exceptions, you can write 1 to PERI_CRG49 bit[8], bit[0], and bit[16] to soft-reset the SDIO0, SDIO1, and SDIO2(eMMC) modules. In addition, you can query MMC_STATUS[Data_busy] to check whether the MMC controller is idle.

You are advised to soft-reset the MMC controller after hot-plugging the card and before using the MMC controller.

Configuring the Working Clock

Before using the MMC controller, you need to set the frequency of its working clock. You can set the frequencies of the SDIO0, SDIO1, and SDIO2(eMMC) working clocks by configuring PERI_CRG49 bit[12:10], bit[4:2], and bit[20:18] respectively.

Configuring the Interface Clock

Clock frequencies vary according to the MMCs complying with different protocols and the status of MMCs. The MMC controller provides an internal even frequency divider that generates appropriate interface clocks by dividing the frequency of the working clock. The relationship between the frequencies of the working clock CCLK_IN and the interface clock SDIO_CCLK_OUT of the MMC controller is as follows:

$F_{SDIO\_CCLK\_OUT} = F_{CCLK\_IN}/(2 \times clk\_divider)$

Where, clk_divider is the value of MMC_CLKDIV[clk_divider]. Clock frequencies vary according to card types. The maximum value of $F_{SDIO\_CCLK\_OUT}$ is 200 MHz.

Before changing the clock frequency of an MMC, ensure that no data or command is being transferred. In addition, to avoid the occurrence of glitches in the output clock of the MMC, you need to perform the following steps:

Step 1 Disable the interface clock.

Set MMC_CLKNA to 0x0000_0000, set MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only], and MMC_CMD[Wait_prvdata_complete] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 2 Set the clock divider.

Configure MMC_CLKDIV based on the required clock frequency, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 3 Enable the interface clock again.

Set MMC_CLKENA to 0x0000_0001, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

----End

CAUTION

The values of MMC_CMD and MMC_CMD are loaded only after MMC_CLKDIV[Start_cmd] and MMC_CLKENA[Update_clk_only] are set to 1. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically. If a command is being executed, a hardware locked error (HLE) interrupt is generated. In this case, you need to clear the interrupt, and then transmit a command again.

When a command is being executed or data is being transferred, the clock parameter values of the card cannot be changed.

Initialization

Before commands and data are exchanged between a card and the MMC controller, the MMC controller needs to be initialized. Perform the following steps:

Step 1 Configure the frequency of the working clock of the MMC controller. For details, see "Working Clock Configuration" in section 12.5.2 "Application Notes."

Step 2 Soft-reset the MMC controller after the card is powered on and the command and data signal lines are pulled up and become stable. For details, see "Soft Reset" in section 12.5.2 "Application Notes."

Step 3 Clear interrupts. Set all bits of MMC_RINTSTS bit[15:0] to 1 to clear raw interrupt status bits.

Step 4 Configure MMC_INTMASK. Set all bits of MMC_INTMASK bit[15:0] to 1 to enable all interrupt sources.

If data is transferred in DMA mode, set MMC_INTMASK bit[4] and MMC_INTMASK bit[5] to 0 to mask the TX/RX FIFO data request interrupts.

Step 5 Set MMC_CTRL[Int_enable] to 1 to enable the MMC interrupt.

Step 6 Configure the timeout parameter register MMC_TMOUT.

Step 7 Configure the FIFO parameter register MMC_FIFOTH.

----End

After the preceding steps, the interface clock can be configured and commands can be transmitted to the card.

Non-Data Transfer Command

If the MMC controller receives a response (correct response, error response, or timeout response) after transmitting a command, the MMC controller sets MMC_RINTSTS bit[2] to 1. Short responses are stored in MMC_RESP0, and long responses are stored in MMC_RESP0 to MMC_RESP3. MMC_RESP3 bit[31] is the MSB, and MMC_RESP0 bit[0] is the LSB.

After a command is transmitted, its error status is reflected by the response command and the corresponding error bit of MMC_RINTSTS.

To transmit a non-data transfer command, perform the following steps:

Step 1 Set the corresponding command parameters of MMC_CMDARG.

Step 2 Configure the command register MMC_CMD based on the description in Table 12-8.

Step 3 Wait until the MMC controller runs the command. If the command is executed, the MMC controller clears MMC_CMD[Start_cmd] automatically.

Step 4 Check whether an HLE interrupt is generated by MMC_RINTSTS bit[12].

Step 5 Wait until the command is executed. If the MMC controller receives a response (correct response, error response, or timeout response), the MMC controller sets MMC_RINTSTS bit[2] to 1. This indicates that the command is executed.

Step 6 Check whether there is any response exception and read the response value if necessary.

You can check the response timeout error, response CRC error, and response error by reading MMC_RINTSTS bit[8], MMC_RINTSTS bit[6], and MMC_RINTSTS bit[1] respectively.

----End

CAUTION

The values of MMC_CMD, MMC_CMDARG, MMC_BYTCNT, and MMC_BLKSIZ are loaded only after MMC_CMDARG[Start_cmd] is set to 1 and MMC_CMD[Update_clock_registers_only] is set to 0. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically.

If other commands are being executed, an HLE interrupt is generated. In this case, you need to perform the preceding operations again. When a non-data transfer command is executed, the values of MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 12-8 Default values of MMC_CMD when a non-data transfer command is executed

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
data_transfer_expected	0	Indicates a non-data transfer command.
card_number	0	-
cmd_index	Cmd index	Command index
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.

Parameter	Value	Description
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
response_length	0	Indicates that this bit is set to 1 when the response is a long response.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
Wait_prvdata_complete	1 or 0	Indicates that the MMC controller must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status during data transfer or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading a Single Data Block or Multiple Data Blocks

To read a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the number of bytes to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for reading data to MMC_CMDARG.

Step 5 Configure MMC_CMD according to the description in Table 12-9.

For the SD card or MMC, you need to read a single data block by running CMD17, and read multiple data blocks by running CMD18; for the SDIO card, you need to read a single data block or multiple data blocks by running CMD53.

The MMC controller starts to run commands after MMC_CMD is written. After commands are transferred to the bus, the cmd_done interrupt is generated.

Step 6 Check the values of MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10]. If any or both of them are 1, read the data in the FIFO by reading MMC_DATA. This ensures that the MMC controller can receive the subsequent data. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. In this case, you can transmit a stop command to stop the data transfer by using the software.

Step 7 If MMC_RINTSTS bit[3] is 1, data transfer is complete. In this case, read the remaining data in the FIFO by reading MMC_DATA.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."

----End

Table 12-9 Default values of MMC_CMD when a single data block or multiple data blocks are read

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."
transfer_mode	0	Indicates block transfer.
read/write	0	Indicates that data is read from the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	Indicates the command index.
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Writing a Single Data Block or Multiple Data Blocks

To write a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the size of the data to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for writing data to MMC_CMDARG.

Step 5 Write data to the FIFO by writing to MMC_DATA. The FIFO needs to be filled with data completely at the very beginning.

Step 6 Configure MMC_CMD according to the description in Table 12-10.

For the SD card or MMC, you need to write a single data block by running CMD24, and write multiple data blocks by running CMD25; for the SDIO card, you need to write a single data block or multiple data blocks by running CMD53.

Step 7 Check the values of MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If any or both of them are 1, fill the FIFO with data by writing to MMC_DATA. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. If necessary, you can transmit a stop command to stop the data transfer by using the software. If MMC_RINTSTS bit[3] is 1, data transfer is complete.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."

Step 9 Query and wait until the value of MMC_STATUS[data_busy] is changed from 1 to 0.

----End

Table 12-10 Default values of MMC_CMD when a single data block or multiple data blocks are written

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."

Parameter	Value	Description
transfer_mode	0	Indicates block transfer.
read_write	1	Indicates that data is written to the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	-
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

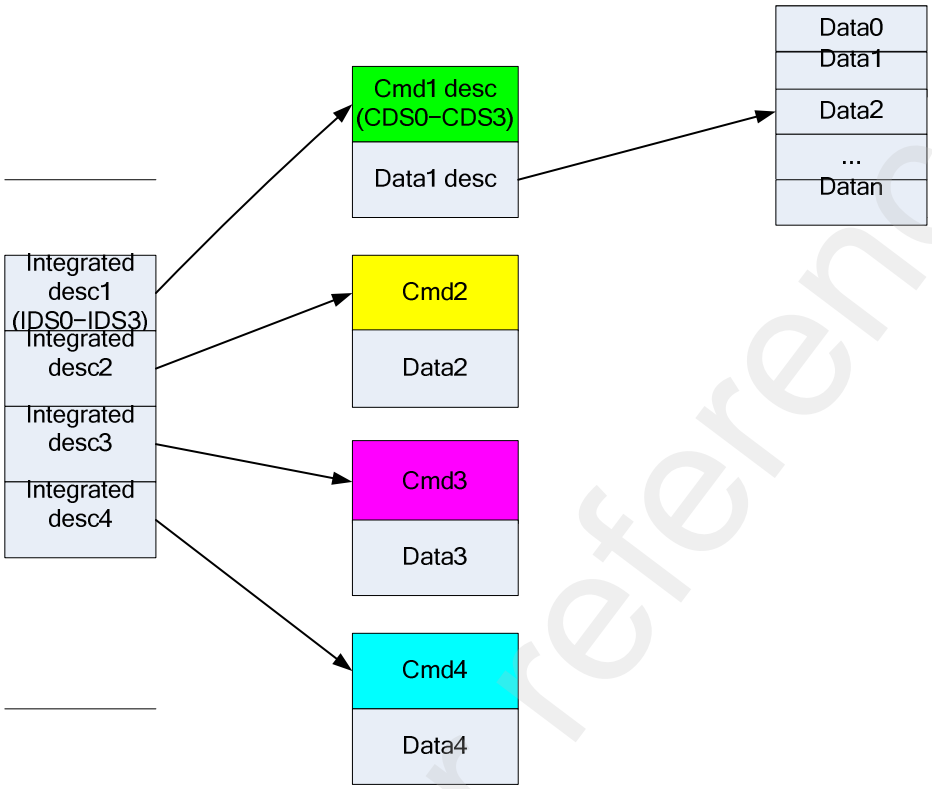
Reading/Writing Stream Data

The modes of reading/writing stream data are the same as those of reading/writing data blocks, except that MMC_CMD[Transfer_mode] needs to be set to 1. During a stream data transfer, the auto-stop function is required.

Transferring Data in ADMA3 Mode

Figure 12-28 illustrates the structures of the data descriptor and the command descriptor.

Figure 12-28 Overall descriptor structure



- Integrated descriptor structure

IDS0 indicates the control information of the integrated descriptor. Table 12-11 describes the definition of each bit in IDS0.

Table 12-11 Definition of each bit of IDS0

Bit	Name	Description
31	OWN	Descriptor attribute indicator 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the ADMA3 This bit is cleared after the internal ADMA3 completes data transfer.
30	RES	Reserved
29	INT	Whether to report multi-packet interrupt 0: not report 1: report
28:0	RES	Reserved

IDS1 indicates the address information of the command descriptor. Table 12-12 describes the definition of each bit in IDS1.

Table 12-12 Definition of each bit of IDS1

Bit	Name	Description
31:0	CMD_ADDR	Address of the command descriptor, pointing to the address of the command to be sent

- Command descriptor structure

CDS0 indicates the data block size. Table 12-13 describes the definition of each bit of CDS0.

Table 12-13 Definition of each bit of CDS0

Bit	Name	Description
31:16	RES	Reserved
15:0	BLK_SIZE	Size of the transferred data block

CDS1 indicates the length of transferred data. Table 12-14 describes the definition of each bit of CDS1.

Table 12-14 Definition of each bit of CDS1

Bit	Name	Description
31:0	BYTECNT	Length of the data block to be transferred

CDS2 indicates the command parameter value. Table 12-15 describes the definition of each bit of CDS2.

Table 12-15 Definition of each bit of CDS2

Bit	Name	Description
31:0	CMD_ARG	Command parameter value

CDS3 indicates the command configuration value. Table 12-16 describes the definition of each bit of CDS3.

Table 12-16 Definition of each bit of CDS3

Bit	Name	Description
31:0	CMD	Command register value

- The structure of the data descriptor is the same as that of the IDMAC descriptor in Descriptor.

Initializing the ADMA3

Step 1 Configure ADMA_DEEPTH to set the command queue depth.

Step 2 Configure ADMA_TIMEOUT to set the timeout time.

Step 3 Configure ADMA_IDS_ADDR to set the start address of the integrated descriptor.

Step 4 Configure MMC_IDINTEN to mask unnecessary registers.

Step 5 Configure ADMA_CONTROL to enable the ADMA3.

Step 6 Create the integrated descriptor, command descriptor, and data descriptor linked lists, and configure ADMA_ID_WRPTR to set the pointer addresses of valid commands.

Step 7 The ADMA3 attempts to obtain descriptors from the descriptor linked lists.

----End

Transferring Data by Using the IDMAC

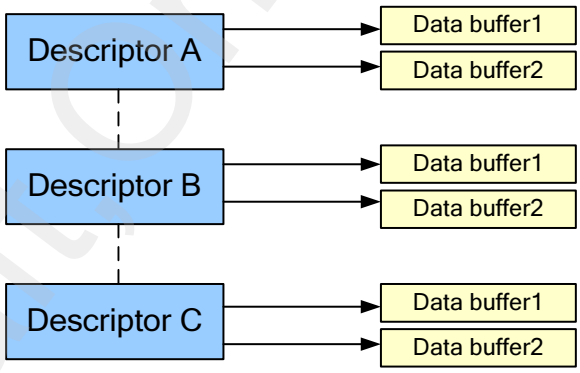
The MMC controller has an embedded IDMAC that transfers data from the original address to the destination address based on the specified descriptor.

Descriptor

The IDMAC supports the following two types of descriptors:

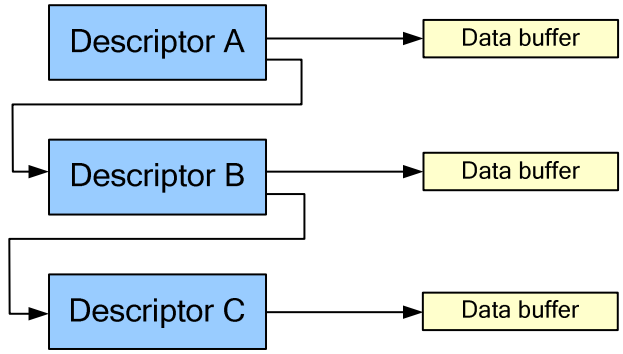
- Dual-buffer descriptor. For this type of descriptor, the span between two descriptors is determined by the DSL bit of MMC_BMOD. Figure 12-29 shows the structure of the dual-buffer descriptor.

Figure 12-29 Structure of the dual-buffer descriptor



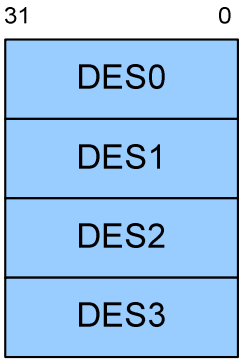
- Linked descriptor. For this type of descriptor, each descriptor points to a unique buffer and the next descriptor. Figure 12-30 shows the structure of the linked descriptor.

Figure 12-30 Structure of the linked descriptor



Each descriptor must be word-aligned, and each descriptor contains 16-byte control and status information. Figure 12-31 shows the internal structure of 32-bit descriptors.

Figure 12-31 Internal structure of 32-bit descriptors



DES0 is used to protect the control and status information. Table 12-17 describes the definition of each bit.

Table 12-17 Definition of each bit of DES0

Bits	Register	Description
31	OWN	Indicates the attributes of the descriptor. 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the IDMAC. After data is transferred by using the IDMAC, the IDMAC clears this bit.
30	CES	Indicates the error status when a card is read. 0: No error occurs. 1: An error occurs.
29:6	RES	Reserved

Bits	Register	Description
5	ER	Indicates the link end of the descriptor. 0: The descriptor is not the last one on the link. 1: The descriptor is the last one on the link. This bit is valid only for the dual-buffer descriptor.
4	CH	Indicates the definition of the second address in DES3. 0: The second address in DES3 is the address of the second buffer. 1: The second address in DES3 is the address of the next descriptor. When this bit is 1, DES1[25:13] must be 0.
3	FS	Indicates that the descriptor contains the first data buffer when this bit is 1. If the size of the first data buffer is 0, the next descriptor contains the start data.
2	LD	Indicates that the descriptor points to the last data buffer when this bit is 1.
1	DIC	Indicates that the data transfer completion interrupt is masked when this bit is 1.
0	RES	Reserved

DES1 is used to specify the buffer size. Table 12-18 describes the definition of each bit of DES1.

Table 12-18 Definition of each bit of DES1

Bits	Register	Description
31: 26	RES	Reserved
25: 13	BS2	Indicates the number of bytes in the second data buffer. This value must be an integral multiple of 4. This bit is invalid when DES0[4] is 1.
12: 0	BS1	Indicates the number of bytes in the first data buffer. This value must be an integral multiple of 4.

DES2 is the address pointer of the first data buffer. Table 12-19 describes the definition of each bit of DES2.

Table 12-19 Definition of each bit of DES2

Bits	Register	Description
31: 0	BAP1	Indicates the physical address of the first data buffer. The address must be word-aligned.

DES3 indicates the second address. Table 12-20 describes the definition of each bit of DES3.

Table 12-20 Definition of each bit of DES3

Bits	Register	Description
31: 0	BAP2	Indicates the physical address of the second data buffer when dual-buffer descriptors are used, or indicates the physical address of the next descriptor when DES0[4] is 1.

Initialization

Perform the following steps:

Step 1 Configure MMC_BMOD to set bus parameters.

Step 2 Configure MMC_IDINTEN to mask unnecessary registers.

Step 3 Create TX/RX descriptor linked lists, configure MMC_DBADDR, and set the start address.

Step 4 The IDMAC attempts to obtain descriptors from the descriptor linked lists.

----End

Transmission

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, set DES0 bit[31] (OWN bit) to 1, and provide data buffers.

Step 2 Write data commands to MMC_CMD.

Step 3 Set TX_Wmark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from data buffers to the internal FIFO of the MMC controller when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Reception

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, and set the DES0 bit[31] (OWN bit) to 1.

Step 2 Write read commands to MMC_CMD.

Step 3 Set RX_WMark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from the internal FIFO of the MMC controller to the external data buffers when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Auto-Stop Function Configuration

When multiple data blocks are read or written, a stop command is required to stop each data transfer. The stop command can be transmitted in non-data transfer command mode or by using the auto-stop function.

The auto-stop function is applicable in the following scenarios:

- SD card

  Multi-block read/write operation by running CMD18 or CMD25
- MMC
  - Stream data read/write operation
  - Multi-block read/write operation in open-ended mode by running CMD18 or CMD25

Before using the auto-stop function of the MMC controller, you are advised to perform the followings steps:

Step 1 Set MMC_CMD[Send_auto_stop] to 1 during the block transfer command operation.

Step 2 After data transfer, the MMC controller automatically transmits a stop command to enable the card to restore to the corresponding state.

Step 3 Read MMC_RINTSTS[auto_cmd_done] to check whether the stop command is executed. The response is stored in MMC_RESP1.

----End

Stopping or Aborting the Data Transfer

The stop command is used to interrupt the data transfer between the MMC controller and the card, whereas the abort command is used to interrupt the I/O data transfer only in SDIO_IOONLY or SDIO_COMBO mode.

The two commands are used as follows:

- Stop command

This command can be transmitted at any time during data transfer, because this command is used to stop the data transfer. In this case, you need to set MMC_CMD bit[5:0] to CMD12, MMC_CMD bit[14] to 1, and MMC_CMD bit[13] to 0.

- Abort command

  This command is available only for SDIO_IOONLY or SDIO_COMBO. To abort the data transfer, you need to configure the CCCR[ASx] register of the SDIO card by running the CMD52 command.

Suspend and Resume Operations

An SDIO card can store the data of a maximum of seven functional devices. The MMC controller can suspend the data transfer of a device by performing the suspend operation. Then the SD interface bus is available for another device with higher priority. After the device with higher priority transfers data, the MMC controller can resume the suspended data transfer of the previous device.

The suspend and resume operations are implemented by configuring the corresponding bits of the CCCR register of the SDIO card. The CCCR register is written or read by running the CMD52 command.

To implement a suspend operation, perform the following steps:

Step 1 Query the SBS bit of the CCCR register to check whether the SDIO card supports suspend and resume operations.

Step 2 Query the FSx and bus status (BS) bits of the CCCR register to check whether the functional device to be suspended is transferring data.

If the BS bit is 1, the device specified by the FSx bit is transferring data.

Step 3 Set the bus release (BR) bit of the CCCR register to 1 to suspend the current data transfer.

Step 4 Check whether the BS and the BR bits of the CCCR register are cleared.

The BS bit retains 1 when the data bus is being used. The BR bit retains 1 before the bus is released completely. When both the BR and BS bits are 0, the data transfer of the selected functional device is suspended.

Step 5 If the current read operation is suspended, MMC_CTRL[Abort_read_data] needs to be set to 1 to restart the data transfer function of the MMC controller after the suspend operation. Then MMC_CTRL[Abort_read_data] is cleared automatically.

Step 6 Read MMC_TCBCNT to query the number of transferred bytes.

----End

To implement a resume operation, perform the following steps:

Step 1 Query the transfer status of the card to check whether the bus is idle.

Step 2 If the card is disconnected, run the CMD7 command to select it. The card status can be queried by running the CMD52 or CMD53 command.

Step 3 Check whether the device to be resumed is ready for data transfer by querying the RF bit of the CCCR register. If the RF bit is 1, the device is ready for data transfer.

Step 4 Run the CMD52 command to write the device ID to the FS bit of the CCCR register to resume the data transfer, and enable the MMC controller to enter the data transfer state (that is, write the block size to MMC_BLKSIZ, and write the amount of remaining data to be transferred to MMC_BYTCNT).

For details about the configuration of MMC_CMDARG, see Table 12-21. The configuration of MMC_CMD is similar to the configuration during block transfer.

Step 5 The data transfer is resumed after the CMD52 command is transmitted successfully. Read the resume data flag (DF) bit of the SDIO device. If this bit is 1, data transfer starts when the transfer function is resumed. If this bit is 0, no data is ready for transferring.

Step 6 If the DF bit is 0, the MMC generates a data timeout error interrupt a period of time later during data read.

----End

Table 12-21 Reference configuration of MMC_CMDARG when the resume operation is performed

MMC_CMDARG	Value	Description
Bit[31]	1	Indicates the read/write flag.
Bit[30:28]	0	Indicates the ID of a functional device that accesses the CCCR register.
Bit[27]	1	Indicates the real-time flag, that is, write-to-read.
Bit[26]	None	-
Bit[25:9]	0x0D	Indicates the register address.
Bit[8]	None	-
Bit[7:0]	ID of the functional device that is resumed	Indicates write data.

CAUTION

The MMC controller cannot be woken up after the system enters the low-power mode.

Read Wait Operation

The read wait operation is performed to suspend the data transfer of the device that is using the SDIO card. The MMC controller determines the duration of pausing the data transfer.

To implement a read wait operation, perform the following steps:

Step 1 Check whether the card supports the read wait operation.

You can read the SRW bit of the CCCR register by running the CMD52 command. If the SRW bit is 1, all the devices supporting the card support the read wait operation.

Step 2 Set MMC_CTRL[Read_wait] to 1.

Step 3 If you want to resume the data transfer, clear MMC_CTRL[Read_wait].

----End

12.5.3 Register Summary

Table 12-22 describes the MMC registers.

Table 12-22 Summary of MMC registers (the base address for SDIO0 is 0x100C_0000, SDIO1 is 0x100D_0000, and eMMC is 0x100E_0000)

Offset Address	Register	Description	Page
0x0000	MMC_CTRL	MMC control register	12-97
0x0004	MMC_PWREN	Power_en control register	12-99
0x0008	MMC_CLKDIV	Clock divider register	12-99
0x0010	MMC_CLKENA	Clock enable register	12-100
0x0014	MMC_TMOUT	Timeout register	12-100
0x0018	MMC_CTYPE	Card type register	12-101
0x001C	MMC_BLKSIZ	Block size configuration register	12-101
0x0020	MMC_BYTCNT	Block transfer count register	12-102
0x0024	MMC_INTMASK	Interrupt mask register	12-102
0x0028	MMC_CMDARG	Command parameter register	12-103
0x002C	MMC_CMD	Command register	12-104
0x0030	MMC_RESP0	Response register 0	12-107
0x0034	MMC_RESP1	Response register 1	12-107
0x0038	MMC_RESP2	Response register 2	12-107
0x003C	MMC_RESP3	Response register 3	12-108
0x0040	MMC_MINTSTS	Masked interrupt status register	12-108
0x0044	MMC_RINTSTS	Raw interrupt status register	12-109
0x0048	MMC_STATUS	Status register	12-110
0x004C	MMC_FIFOTH	FIFO threshold register	12-112
0x0050	MMC_CDETECT	Card detection register	12-113

Offset Address	Register	Description	Page
0x0054	MMC_WRTPRT	Card write protection register	12-113
0x005C	MMC_TCBCNT	Count of bytes transmitted to the card register	12-114
0x0060	MMC_TBBCNT	Count of bytes transmitted from the bus interface unit (BIU) FIFO register	12-114
0x0064	MMC_DEBNCE	Dejitter count register	12-115
0x0074	MMC_UHS_REG	UHS-1 register	12-115
0x0078	MMC_CARD_RSTN	eMMC reset control register	12-116
0x0080	MMC_BMOD	Bus mode register	12-117
0x0084	MMC_PLDMND	Poll demand register	12-118
0x0088	MMC_DBADDR	Base address register of the descriptor linked list	12-118
0x008C	MMC_IDSTS	IDMAC status register	12-119
0x0090	MMC_IDINTEN	IDMAC interrupt enable register	12-121
0x0094	MMC_DSCADDR	Address register of the current descriptor	12-123
0x0098	MMC_BUFADDR	Address register of the current data buffer	12-123
0x00B0	ADMA_CONTROL	ADMA3 control register	12-124
0x00B4	ADMA_IDS_ADDR	Queue start address register	12-125
0x00B8	ADMA_DEEPTH	Queue depth register	12-125
0x00BC	ADMA_ID_RDPTR	Queue read pointer register	12-125
0x00C0	ADMA_ID_WRPTR	Queue write pointer register	12-126
0x00C4	ADMA_TIMEOUT	Timeout configuration register	12-126
0x0100	MMC_CARDTHRCTL	Threshold control register	12-129
0x0108	MMC_UHS_REG_EXT	UHS extension register	12-127

Offset Address	Register	Description	Page
0x010C	MMC_DDR_REG	eMMC 4.5 DDR start bit detection control register	12-128
0x0110	MMC_ENABLE_SHIFT	Phase shift register	12-129
0x0200	MMC_DATA	Data register (entrance address of the FIFO)	12-129

12.5.4 Register Description

MMC_CTRL

MMC_CTRL is a MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						use_internal_dmac	reserved																abort_read_data	send_irq_response	read_wait	reserved	int_enable	reserved	dma_reset	fifo_reset	controller_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	Use_internal_dmac	Whether to transfer data by using the IDMAC 0: The CPU transfers data by using the slave interface. 1: The CPU transfers data by using the IDMAC.
[24:9]	RO	reserved	Reserved
[8]	RW	Abort_read_data	Whether to abort the data transfer during data read 0: invalid 1: After transmitting a suspend command during data read, the software polls the card to check when suspend occurs. After the suspend occurs, the software sets the bit to 1. This enables the data transfer state machine to be restored to idle state for the next block transfer. After the state machine restores to the idle status, this bit is cleared automatically.

[7]	RW	Send_irq_response	TX interrupt response control 0: invalid 1: An interrupt request (IRQ) response is transmitted automatically. After the response is transmitted, this bit is cleared automatically. To wait for the interrupt generated by the MMC controller, the host transmits the CMD40 command and waits for the interrupt response from the MMC controller. If you do not want the host to keep in the interrupt wait state, set this bit to 1 and transmit the CMD40 command to restore the host to the idle state.
[6]	RW	Read_wait	Read wait control 0: disabled 1: enabled This bit is valid only for the SDIO card that supports the read wait function.
[5]	RO	reserved	Reserved.
[4]	RW	Int_enable	Global interrupt enable 0: disabled 1: enabled The interrupt output is valid only when this bit is valid and the interrupt source is enabled.
[3]	RO	reserved	Reserved
[2]	RW	Dma_reset	Soft reset control for the internal DMAC 0: invalid 1: reset the internal DMA interface This bit is automatically reset after two AHB clock cycles.
[1]	RW	Fifo_reset	Soft reset control for the internal FIFO 0: invalid 1: reset the FIFO pointer This bit is reset automatically after the reset operation is complete.
[0]	RW	Controller_reset	Soft reset control for the controller 0: invalid 1: reset the MMC/SD/SDIO host module

MMC_PWREN

MMC_PWREN is a Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Power_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	Power_enable	Power control 0: power off 1: power on

MMC_CLKDIV

MMC_CLKDIV is a clock divider register that shows the ratio of the frequency of the module output clock to the frequency of the input clock. For example, if the module input clock is 40 MHz and the register value is set to 1, the output clock is 20 MHz.

The clock divider is 2 x N. If the value of *N* is 0x0, it indicates no frequency division (2 x 0 = 0); if the value of *N* is 0x1, the frequency is divided by 2; if the value of *N* is 0xFF, the frequency is divided by 510.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								clk_divider0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	clk_divider0	SDIO clock divider. The clock divider is 2 x *n*. If the value of *n* is 0, it indicates no frequency division; if the value of *n* is 1, the frequency is divided by 2; if the value of *n* is 0xFF, the frequency is divided by 510.

MMC_CLKENA

MMC_CLKENA is a clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															cclk_low_power	reserved															cclk_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	cclk_low_power	Card low-power control for disabling the card clock 0: non lower-power mode 1: low-power mode When the card is idle, the card clock is disabled. This function is used only for the MMC and SD card, because the card clock of the SDIO card must be retained for detecting interrupts.
[15:1]	RO	reserved	Reserved
[0]	RW	cclk_enable	Card clock enable 0: disabled 1: enabled

MMC_TMOUT

MMC_TMOUT is a timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_timeout																								response_timeout							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	data_timeout	Timeout during the data transfer of the card, in unit of the mmc_clk cycle of the card. The timeout is also the data starvation timeout of the CPU

[7:0]	RW	response_timeout	Response timeout, in unit of the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is a card type register.

Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															card_width	reserved															card_width1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	card_width_0	Card bus width 0: non-8-bit mode 1: 8-bit mode The card configuration details are as follows: If bit[16] is 0, the card bus width is set to the 1-bit mode or 4-bit mode. In this case, the bus width depends on the value of bit[0].
[15:1]	RO	reserved	Reserved
[0]	RW	card_width_1	Bus width of the card 0: 1-bit mode 1: 4-bit mode

MMC_BLKSIZ

MMC_BLKSIZ is a block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																block_size															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	block_size	Block size. The initial size of each block is 512 bytes.

MMC_BYTCNT

MMC_BYTCNT is a block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Byte_count	Number of transferred bytes. The number must be an integral multiple of the block size. If the data transfer is not block transfer, this register must be set to 0. In this case, the software needs to transmit a stop or an abort command to control the data transfer.

MMC_INTMASK

MMC_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sdio_int_mask	Int_mask														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved

[16]	RW	sdio_int_mask	Interrupt mask control 0: masked 1: enabled
[15:0]	RW	int_mask	Interrupt mask 0: masked 1: enabled Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation-by-host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_CMDARG

MMC_CMDARG is a command parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_arg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_arg	Command parameter that is transferred to the card. The command parameter is related to the protocol, and each command corresponds to a command parameter.

MMC_CMD

MMC_CMD is a command register.

Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	start_cmd	reserved	use_hold_reg	volt_switch	boot_mode	disable_boot	expect_boot_ack	enable_boot	reserved		update_clock_registes_only	card_number					send_initialization	stop_abort_cmd	wait_prvdata_complete	send_auto_stop	transfer_mode	read_write	data_transfer_expected	check_response_crc	response_length	response_expect	cmd_index					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	start_cmd	Start control 0: do not start 1: start a command After the command is transferred to the card interface unit (CIU), this bit is cleared. The CPU does not allow modifications to this register. Otherwise, an HLE interrupt is generated. After transmitting a command, the CPU queries this bit, and transmits the next command when the value of this bit changes to 0.
[30]	RO	reserved	Reserved
[29]	RW	use_hold_reg	Whether to use the hold register 0: The CMD and DATA signals transmitted to the MMC do not pass through the hold register. 1: The CMD and DATA signals transmitted to the MMC pass through the hold register.
[28]	RW	volt_switch	Voltage switching enable 0: disabled 1: enabled
[27]	RW	boot_mode	Boot mode 0: boot mode 1: alternative boot mode

[26]	RW	disable_boot	Boot disable If the software enables this bit and the Start_cmd bit at the same time, the controller aborts the boot operation. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[25]	RW	expect_boot_ack	Boot response enable If the software enables this bit and the Enable_boot bit at the same time, the controller detects the boot response signal in "0–1–0" sequence.
[24]	RW	enable_boot	Boot enable This bit is available when the boot mode is mandatory. If the software enables this bit and the Start_cmd bit, the controller pulls down the CMD signal to start the boot process. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[23:22]	RO	reserved	Reserved
[21]	RW	update_clock_registers_only	Automatic update 0: The normal command sequence is used. That is, the values of MMC_CMD, MMC_CMDARG, MMC_TMOUT, MMC_CTYPE, MMC_BLKSIZ, and MMC_BYTCNT are transferred from the BIU to the CIU. The CIU uses the new values of registers when running new commands. 1: No command is transmitted, and only the clock register values in the card clock domain are updated. The values of MMC_CLKDIV and MMC_CLKENA are transferred to the card clock domain. The card clock can be changed (frequency change and clock enable) even no command is transmitted. Each time the card clock is changed; this bit must be set to 1. In this case, no command is transmitted to the card, and no command done interrupt is generated.
[20:16]	RW	card_number	Serial number of the card that is being used
[15]	RW	send_initialization	Whether to transmit the initialization sequence 0: do not transmit the initialization sequence before transmitting the Send_initialization command (high level in 80 clock cycles) 1: transmit the initialization sequence before transmitting the Send_initialization command When a card is powered on, the initialization sequence must be transmitted for initialization before any command is transmitted. That is, this bit must be set to 1.

[14]	RW	stop_abort_cmd	Whether to transmit the stop/abort command when data is being transferred in open-ended mode or in fixed length mode. 0: do not transmit the stop/abort command 1: transmit the stop/abort command for stopping the current data transfer
[13]	RW	wait_prvdata_complete	Whether to transmit a command immediately 0: transmit a command immediately even though the previous data transfer is not complete 1: transmit a command only when the previous data transfer is complete The typical value is 0. If this bit is set to 0, the transfer status can be read during data transfer, and the interrupt transfer is supported.
[12]	RW	send_auto_stop	Whether to transmit the stop command 0: do not transmit the stop command after data transfer 1: transmit the stop command after data transfer In non-data transfer mode, this bit is ignored.
[11]	RW	transfer_mode	Transfer mode 0: block transfer mode 1: stream transfer mode In non-data transfer mode, this bit is ignored.
[10]	RW	read_write	Read/write control 0: read data from the card 1: write data to the card In non-data transfer mode, this bit is ignored.
[9]	RW	data_transfer_expected	Data transfer indicator 0: No data is output from the card. 1: Data is output from the card.
[8]	RW	check_response_crc	Whether to perform the CRC check 0: Do not check the CRC response. 1: Check the CRC response. No valid CRC is returned when some commands are responded. To prevent the host from performing CRC, the software needs to disable this function based on related commands.
[7]	RW	response_length	Response length 0: Short responses are output from the card 1: Long responses are output from the card The length of a long response is 128 bits, whereas the length of a short response is 32 bits.

[6]	RW	response_expect	Whether to output response 0: No response is output from the card. 1: Responses are output from the card.
[5:0]	RW	cmd_index	Command index

MMC_RESP0

MMC_RESP0 is response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response0	Bit[31:0] of a response

MMC_RESP1

MMC_RESP1 is response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response1	Bit[63:32] of a long response After the CIU transmits an auto-stop command, the corresponding response is stored in this register, and the response to the previous command is still stored in MMC_RESP0. The auto-stop command is available only during data transfer, and the corresponding response is always a short response.

MMC_RESP2

MMC_RESP2 is response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response2	Bit[95:64] of a long response

MMC_RESP3

MMC_RESP3 is response register 3.

Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response3	Bit[127:96] of a long response

MMC_MINTSTS

MMC_MINTSTS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sdio_interrupt	int_status														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	sdio_interrupt	Interrupt mask status

			The SDIO interrupt is valid only when MMC_INTMASK [sdio_int_mask] is enabled. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card.
[15:0]	RO	int_status	Status of each interrupt Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_RINTSTS

MMC_RINTSTS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				sdio_interrupt	int_status		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	sdio_interrupt	Raw status of an interrupt 0: No SDIO interrupt is output from the card.

			1: An SDIO interrupt is output from the card. The value of the interrupt status bit is independent of the interrupt mask status.
[15:0]	RW	int_status	Raw status of each interrupt. Writing 1 clears the bits, and writing 0 has no effect. The value of the interrupt status bit is independent of the interrupt mask status. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DRTO)/Boot Data Start (BDS) Bit[8]: response timeout (RTO)/Boot Ack Received (BAR) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_STATUS

MMC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fifo_count												response_index				data_state_mc_busy		data_busy		reserved				commandfsm_states				fifo_full		fifo_empty		fifo_tx_watermark		fifo_rx_watermark	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:17]	RO	fifo_count	FIFO count

[16:11]	RO	response_index	Serial number of the previous response, including the response to the auto-stop command
[10]	RO	data_state_mc_busy	0: The data TX/RX state machine is idle. 1: The data TX/RX state machine is busy.
[9]	RO	data_busy	This field value depends on the reverse level of DATA0. 0: idle (DATA0 is high level) 1: busy (DATA0 is low level)
[8]	RO	reserved	Reserved
[7:4]	RO	commandfsm_states	Status of the command state machine 0x0: idle 0x1: send init sequence 0x2: Tx cmd start bit 0x3: Tx cmd tx bit 0x4: Tx cmd index + arg 0x5: Tx cmd crc7 0x6: Tx cmd end bit 0x7: Rx resp start bit 0x8: Rx resp IRQ response 0x9: Rx resp tx bit 0xA: Rx resp cmd idx 0xB: Rx resp data 0xC: Rx resp crc7 0xD: Rx resp end bit 0xE: Cmd path wait NCC 0xF: wait, CMD-to-response turnaround
[3]	RO	fifo_full	FIFO full flag 0: empty 1: full
[2]	RO	fifo_empty	FIFO empty flag 0: not empty 1: empty
[1]	RO	fifo_tx_watermark	Whether the FIFO reaches the TX threshold 0: no 1: yes
[0]	RO	fifo_rx_watermark	Whether the FIFO reaches the RX threshold 0: no 1: yes

MMC_FIFOTH

MMC_FIFOTH is a FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x60FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		Multiple_Transaction_Size		rx_wmark												reserved				tx_wmark											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	Multiple_Transaction_Size	Transferred burst length 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 256
[27:16]	RW	rx_wmark	FIFO threshold during data read. If the data amount in the FIFO is above the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: RX_WMark ≤ FIFO_DEPTH – 2 Recommendation: A request is raised when the value of [(FIFO_DEPTH/2) – 1] is above the threshold.
[15:12]	RO	reserved	Reserved

[11:0]	RW	tx_wmark	FIFO threshold during data transmission. If the data amount in the FIFO is below the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: TX_WMark ≤ FIFO_DEPTH – 2 Recommendation: This field must be less than or equal to FIFO_DEPTH/2.

MMC_CDETECT

MMC_CDETECT is a card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															card_detect_n
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	card_detect_n	Card detection signal The value depends on the SDIO_CARD_DETECT pin.

MMC_WRTPRT

MMC_WRTPRT is a card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								write_protect
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	write_protect	Card write protection signal The value depends on the SDIO_CWPR pin.

MMC_TCBCNT

MMC_TCBCNT is a count of bytes transmitted to the card register.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	trans_card_byte_count							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	trans_card_byte_count	Count of bytes transmitted from the CIU to the card When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_TBBCNT

MMC_TBBCNT is a count of bytes transmitted from the BIU FIFO register.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_count	Count of bytes transferred between the CPU/DMA and BIU FIFO When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_DEBNCE

MMC_DEBNCE is a dejitter count register.

Offset Address	Register Name	Total Reset Value
0x0064	MMC_DEBNCE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								debounce_count																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	debounce_count	Number of bus clock cycles used by the dejitter filter logic. Generally, the dejitter duration ranges from 5 ms to 25 ms.

MMC_UHS_REG

MMC_UHS_REG is a UHS-1 register.

Offset Address	Register Name	Total Reset Value
0x0074	MMC_UHS_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															ddr_reg	reserved															volt_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved
[16]	RW	ddr_reg	DDR mode control 0: non-DDR mode 1: DDR mode
[15:1	RO	reserved	Reserved
[0]	RW	volt_reg	Voltage mode control Bit 1 and bit 0 control the voltage modes of eMMC and SDIO respectively. The following takes bit 0 as an example: 0: 3.3 V 1: 1.8 V

MMC_CARD_RSTN

MMC_CARD_RSTN is an eMMC reset control register.

Offset Address	Register Name	Total Reset Value
0x0078	MMC_CARD_RSTN	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															card_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	card_reset	eMMC reset. The control pin is CARD_RESET. 0: reset 1: deassert reset

MMC_BMOD

MMC_BMOD is a bus mode register.

Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pbl			de	dsl					fb	swr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	pbl	Length of the IDMAC burst transfer 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 256
[7]	RW	de	IDMAC enable 0: disabled 1: enabled
[6:2]	RW	dsl	Span between two descriptors, that is, number of words between two non-linked descriptors. This bit is valid only for the dual-buffer descriptor.
[1]	RW	fb	Fixed burst length type 0: single and INCR burst types 1: single, INCR4, INCR8, and INCR16 burst types
[0]	RW	swr	Soft reset control for the internal register of the IDMAC 0: not reset 1: reset After reset, this bit is automatically cleared one clock cycle later.

MMC_PLDMND

MMC_PLDMND is a poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	pd	If DES0[OWN] is 0, the IDMAC enters the suspend state. The CPU can write any value to this register to enable the IDMAC to obtain descriptors again.

MMC_DBADDR

MMC_DBADDR is a base address register of the descriptor linked list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sdl	Start address of the descriptor linked list, that is, the base address of the first descriptor

MMC_IDSTS

MMC_IDSTS is an IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		cmd_lock_err	ids_ownbit_err	ids_queue_overflow	resp_check_err	packet_int	packet_timeout_int	auto_stop_err	ids_queue_full	ids_queue_empty	adma3_fsm				fsm				eb			ais	nis	reserved		ces	du	reserved	fbe	ri	ti
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RWC	cmd_lock_err	Command conflict 0: The commands are normal. 1: Command conflicts occur.
[28]	RWC	ids_ownbit_err	Own bit error 0: The own bit is normal. 1: The own bit has errors.
[27]	RWC	ids_queue_overflow	Queue overflow 0: No overflow occurs. 1: Overflow occurs.
[26]	RWC	resp_check_err	Response error detection 0: No error occurs. 1: An error occurs.
[25]	RWC	packet_int	Multi-packet interrupt 0: No multi-packet interrupt is generated. 1: A multi-packet interrupt is generated.
[24]	RWC	packet_timeout_int	Timeout interrupt 0: No timeout interrupt is generated. 1: A timeout interrupt is generated.
[23]	RWC	auto_stop_err	Hardware stop error detection 0: No error occurs. 1: An error occurs.

[22]	RWC	ids_queue_full	Whether the queue is full 0: no 1: yes
[21]	RWC	ids_queue_empty	Whether the queue is empty 0: no 1: yes
[20:17]	RO	adma3_fsm	Current state of the ADMA3 state machine 0x0: ADMA3_IDLE 0X1: ADMA3_FIDS 0X2: ADMA3_SREG 0X3: ADMA3_CMD 0X4: ADMA3_TRANS 0X5: ADMA3_DESC_CLOSE 0X6: ADMA3_AUTO_STOP 0X7: ADMA3_WAIT Other values: reserved
[16:13]	RO	fsm	Current state of the IDMAC state machine 0x0: DMA_IDLE 0x1: DMA_SUSPEND 0x2: DESC_RD 0x3: DESC_CHK 0x4: DMA_RD_REQ_WAIT 0x5: DMA_WR_REQ_WAIT 0x6: DMA_RD 0x7: DMA_WR 0x8: DESC_CLOSE Other values: reserved
[12:10]	RW	eb	Bus error type 001: The transmit operation is aborted. 010: The receive operation is aborted. Other values: reserved
[9]	RW	ais	Abnormal total interrupt. The value of this bit is obtained after the values of FBE, DU, and CES bits are ORed. Writing 1 clears this bit.
[8]	RW	nis	Normal total interrupt. The value of this bit is obtained after the values of the TI and RI bits are ORed. Writing 1 clears this bit.
[7:6]	RO	reserved	Reserved
[5]	RW	ces	Card error indicator. This bit indicates the card status when data is being received.

			0: No error occurs. 1: An error occurs.
[4]	RW	du	Descriptor invalid interrupt. When DES0[OWN] is 0, this bit is set to 1. Writing 1 clears this bit.
[3]	RO	reserved	Reserved
[2]	RW	fbe	Fatal bus error interrupt. If this bit is set to 1, the IDMAC stops all accesses through the bus. Writing 1 clears this bit.
[1]	RW	ri	Reception completion interrupt. This bit indicates that the data of a descriptor is received. Writing 1 clears this bit. 0: The reception is not complete. 0: The reception is complete.
[0]	RW	ti	Transmission completion interrupt. This bit indicates that a descriptor finishes transmitting data. Writing 1 clears this bit. 0: The transmission is not complete. 1: The transmission is complete.

MMC_IDINTEN

MMC_IDINTEN is an IDMAC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		cmd_lock_err	ids_ownbit_err	ids_queue_overflow	resp_check_err	packet_int	packet_timeout_int	auto_stop_err	ids_queue_full	ids_queue_empty	adma3_fsm					fsm						ai	ni	reserved		ces	du	reserved	fbe	ri	ti
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	cmd_lock_err	Command conflict interrupt enable 0: disabled 1: enabled

[28]	RW	ids_ownbit_err	Own bit error interrupt enable 0: disabled 1: enabled
[27]	RW	ids_queue_overflow	Queue overflow interrupt enable 0: disabled 1: enabled
[26]	RW	resp_check_err	Response error detection interrupt enable 0: disabled 1: enabled
[25]	RW	packet_int	Multi-packet interrupt enable 0: disabled 1: enabled
[24]	RW	packet_timeout_int	Timeout interrupt enable 0: disabled 1: enabled
[23]	RW	auto_stop_err	Hardware stop error detection interrupt enable 0: disabled 1: enabled
[22]	RW	ids_queue_full	Queue full interrupt enable 0: disabled 1: enabled
[21]	RW	ids_queue_empty	Queue empty interrupt enable 0: disabled 1: enabled
[20:17]	RO	adma3_fsm	Reserved
[16:10]	RO	fsm	Reserved
[9]	RW	ai	Abnormal interrupt enable 0: disabled 1: The FBE, DU, and CES interrupts are enabled.
[8]	RW	ni	Normal interrupt enable 0: disabled 1: The TI and RI interrupts are enabled.
[7:6]	RO	reserved	Reserved
[5]	RW	ces	Card error interrupt enable 0: disabled 1: enabled

[4]	RW	du	Descriptor invalid interrupt enable 0: disabled 1: enabled
[3]	RO	reserved	Reserved
[2]	RW	fbe	Fatal bus error interrupt enable 0: disabled 1: enabled
[1]	RW	ri	RX interrupt enable 0: disabled 1: enabled
[0]	RW	ti	TX interrupt enable 0: disabled 1: enabled

MMC_DSCADDR

MMC_DSCADDR is an address register of the current descriptor.

Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	had																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	had	Descriptor pointer. The value is automatically refreshed during data transfer. The register points to the start address of the descriptor that will be used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is an address register of the current data buffer.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hba																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hba	Data buffer pointer. The value is automatically refreshed during data transfer. The register points to the start address of the data buffer that is being used by the IDMAC.

ADMA_CONTROL

ADMA_CONTROL is an ADMA3 control register.

Offset Address	Register Name	Total Reset Value
0x00B0	ADMA_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											resp_check_en	soft_change_rdptr_en	packet_int_en	adma3_restart	adma3_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	resp_check_en	Response error detection function enable 0: disabled 1: enabled
[3]	RW	soft_change_rdptr_en	Software rewrite logic read pointer function enable 0: disabled 1: enabled
[2]	RW	packet_int_en	Multi-packet interrupt enable 0: disabled 1: enabled
[1]	RW	adma3_restart	ADMA3 restart enable 0: disabled 1: enabled
[0]	RW	adma3_enable	ADMA3 enable 0: disabled 1: enabled

ADMA_IDS_ADDR

ADMA_IDS_ADDR is a queue start address register.

Offset Address	Register Name	Total Reset Value
0x00B4	ADMA_IDS_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ids_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ids_start_addr	Start address of the integrated descriptor

ADMA_DEEPTH

ADMA_DEEPTH is a queue depth register.

Offset Address	Register Name	Total Reset Value
0x00B8	ADMA_DEEPTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ids_deepth																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ids_deepth	Depth of the integrated descriptor

ADMA_ID_RDPTR

ADMA_ID_RDPTR is a queue read pointer register.

Offset Address	Register Name	Total Reset Value
0x00BC	ADMA_ID_RDPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ids_rdptr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ids_rdptr	Read pointer of the integrated descriptor

ADMA_ID_WRPTR

ADMA_ID_WRPTR is a queue write pointer register.

Offset Address	Register Name	Total Reset Value
0x00C0	ADMA_ID_WRPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ids_wrptr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ids_wrptr	Write pointer of the integrated descriptor

ADMA_TIMEOUT

ADMA_TIMEOUT is a timeout configuration register.

Offset Address	Register Name	Total Reset Value
0x00C4	ADMA_TIMEOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timeout_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timeout_count	Timeout count configuration for the multi-packet timeout interrupt

MMC_CARDTHRCTL

MMC_CARDTHRCTL is a threshold control register.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_CARDTHRCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cardrdthreshold												reserved															

Name	Bit
cardwrthr_en	2
BsyClrIntEn	1
cardrdthr_en	0

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27:16]	RW	cardrdthreshold	Read threshold The maximum value is 512.
[15:3]	RW	reserved	Reserved
[2]	RW	cardwrthr_en	Write threshold enable 0: disabled 1: enabled
[1]	RW	BsyClrIntEn	Busy clear interrupt enable 0: disabled 1: enabled
[0]	RW	cardrdthr_en	Read threshold enable 0: disabled 1: enabled

MMC_UHS_REG_EXT

MMC_UHS_REG_EXT is a UHS extension register.

Offset Address	Register Name	Total Reset Value
0x0108	MMC_UHS_REG_EXT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								clk_drv_phase_ctrl				reserved				clk_smpl_phase_ctrl				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved

[25:23]	RW	clk_drv_phase_ctrl	clk_in_drv clock phase control 000: 0° 001: 45° 010: 90° 011: 135° 100: 180° 101: 225° 110: 270° 111: 315°
[22:19]	RO	reserved	Reserved
[18:16]	RW	clk_smpl_phase_ctrl	clk_in_sample clock phase control 000: 0° 001: 45° 010: 90° 011: 135° 100: 180° 101: 225° 110: 270° 111: 315°
[15:0]	RO	reserved	Reserved

MMC_DDR_REG

MMC_DDR_REG is an eMMC 4.5 DDR start bit detection control register.

Offset Address	Register Name	Total Reset Value
0x010C	MMC_DDR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hs400_mode	reserved																													half_start_bit	reserved

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hs400_mode	HS400 mode control 0: non-HS400 mode 1: HS400 mode
[30:2]	RO	reserved	Reserved
[1]	RW	half_start_bit	For the eMMC4.5 component, when this bit is set to 1'b1, RINTSTS[15] is set to 1 when CMD12 is received in DDR mode.
[0]	RO	reserved	Reserved

MMC_ENABLE_SHIFT

MMC_ENABLE_SHIFT is a phase shift register.

Offset Address	Register Name	Total Reset Value
0x0110	MMC_ENABLE_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														Enable Phase Shift Register_0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved
[1:0]	RW	Enable Phase Shift Register_0	phase shift control 00: default phase shift 01: Phase shift on the next rising edge 10: Phase shift on the next falling edge 11: Reserved

MMC_DATA

MMC_DATA is a data register (entrance address of the FIFO). The FIFO overflow must be read first before the data is read from or written to the FIFO.

Offset Address	Register Name	Total Reset Value
0x0200	MMC_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data	Address for reading/writing to the FIFO. If the address ranges from 0x200 to 0x200 + FIFO_DEPTH, the FIFO is selected.

12.6 IR Interface

12.6.1 Overview

The infrared (IR) module receives data over the IR interface.

12.6.2 Features

The IR module has the following features:

- Allows you to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the RX data overflow interrupt, RX data frame format error interrupt, RX data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the RX symbol overflow interrupt, RX symbol interrupt, symbol timeout interrupt, and combined interrupt.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.
- Supports the reference clock frequency ranging from 1 MHz to 128 MHz and controls the clock frequency divider by software programming, enabling the frequency of the working clock to be prescaled to 1 MHz.

12.6.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the ARM system. The ARM system performs corresponding operations according to the received codes, which implements expected functions. The IR module connects to the APB of the ARM subsystem. When the chip is in the low-power state (the CPU is at a low frequency), the IR module generates an

interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Table 12-23 to Table 12-25 describe the code formats of the received infrared data.

NOTE

The values in Table 12-23 to Table 12-25 are tested before and may not be accurate. Therefore, they are only for reference.

Table 12-23 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		NEC with Simple Repeat Code			
		uPD6121G	D6121/BU5777/D1913	LC7461M-C13	AEHA
Lead code (10 µs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 µs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 µs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 µs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 µs)		55	55	55	42.2
Frame length (10 µs)		108,00	10,800	10,800	8,777.6 – 12,828.8
Valid data bit		32	32	42	48

Table 12-24 Code formats of the received infrared data (NEC with full repeat code)

Data Format		NEC with Full Repeat Code						
		uPD6121G	LC7461M-C13	MN6024-C5D6	MN6014-C6D6	MATNEW	MN6030	PANASONIC
Lead code	LEAD_S	900	900	337.6	349.2	348.8	349	352

Data Format		NEC with Full Repeat Code						
		uPD6121G	LC7461M-C13	MN6024-C5D6	MN6014-C6D6	MATNEW	MN6030	PANASONIC
(10 µs)	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 µs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 µs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 µs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 µs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400
Valid data bit		32	42	22	24	48	22	22

Table 12-25 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 µs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 µs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 µs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 µs)		56	None	None	None	None
Frame length (10 µs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

12.6.3.1 NEC with Simple Repeat Code

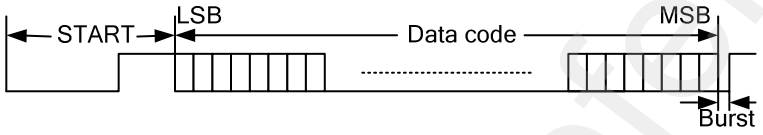
Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

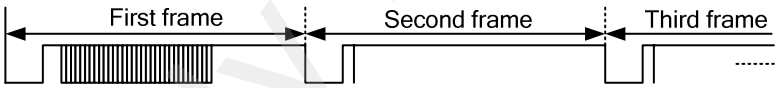
Figure 12-32 shows the frame format of transmitting a single NEC with simple repeat code.

Figure 12-32 Frame format for transmitting a single NEC with simple repeat code



If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure 12-33 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 12-33 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously



Code Format

Figure 12-34 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

Figure 12-34 Definitions of bit0 and bit1 of the NEC with simple repeat code

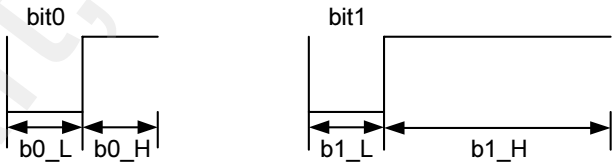


Figure 12-35 shows the format for transmitting a single NEC with simple repeat code. Figure 12-36 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 12-35 Format for transmitting a single NEC with simple repeat code

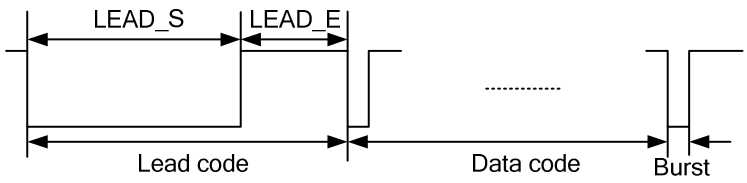
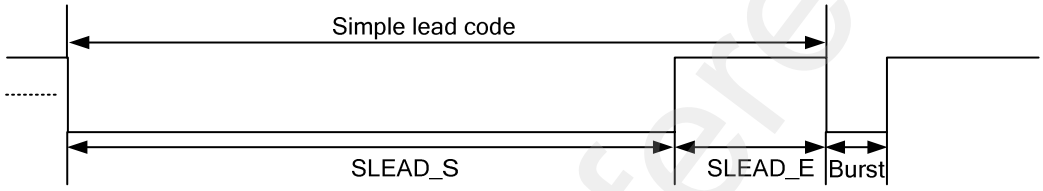


Figure 12-36 Code format for transmitting consecutive NEC with simple repeat codes



NOTE

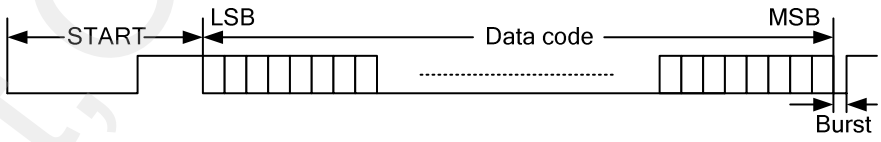
- The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 12-23 to Table 12-25.
- The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

12.6.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, its LSB is received first. Burst signal: It is used to receive the last data bit. Figure 12-37 shows the frame format for transmitting a single NEC with full repeat code.

Figure 12-37 Frame format for transmitting a single NEC with full repeat code



If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 12-38 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 12-38 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

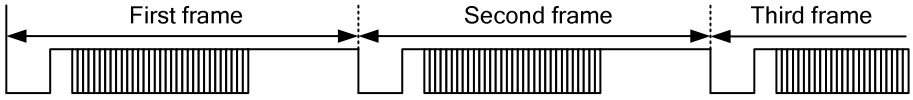


Figure 12-37 and Figure 12-38 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

Code Format

Figure 12-39 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 12-39 Definitions of bit0 and bit1 of the NEC with full repeat code

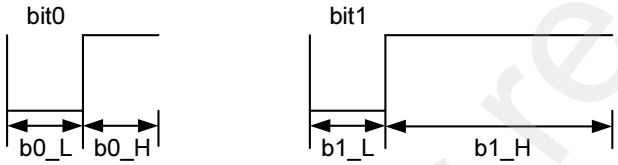
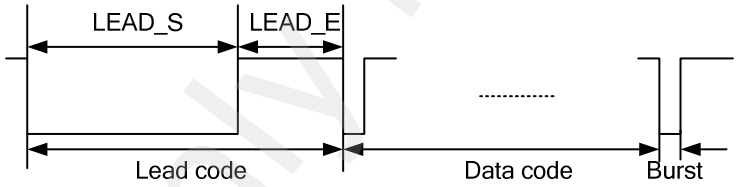


Figure 12-40 shows the format for transmitting a single NEC with full repeat code.

Figure 12-40 Format for transmitting a single NEC with full repeat code



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 12-23 to Table 12-25.

12.6.3.3 TC9012 Code

Frame Format

CAUTION

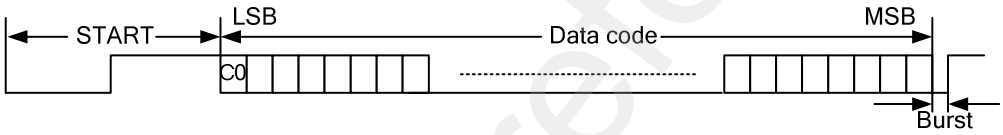
According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

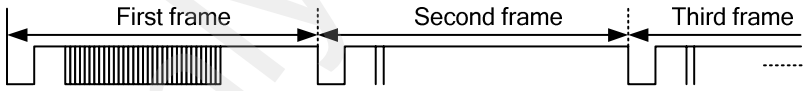
Figure 12-41 shows the frame format for transmitting a single TC9012 code.

Figure 12-41 Frame format for transmitting a single TC9012 code



When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 12-42 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 12-42 Frame format for transmitting TC9012 codes by pressing the key continuously



Code Format

Figure 12-43 shows the definitions of bit0 and bit1 of the TC9012 code.

Figure 12-43 Definitions of bit0 and bit1 of the TC9012 code

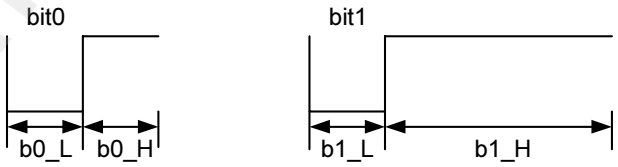


Figure 12-44 shows the format for transmitting a single TC9012 code.

Figure 12-44 Format for transmitting a single TC9012 code

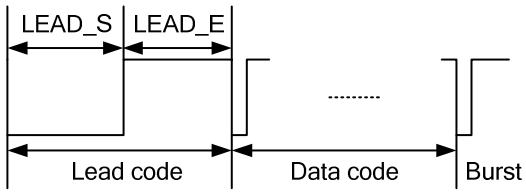


Figure 12-45 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

Figure 12-45 Format for transmitting consecutive TC9012 codes (C0 = 1)

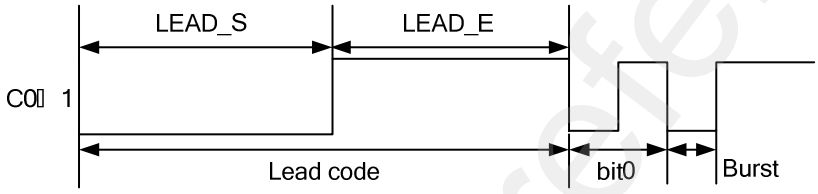
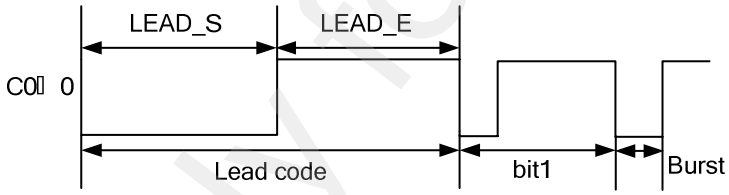


Figure 12-46 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 12-46 Format for transmitting consecutiveTC9012 codes (C0 = 0)



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 12-23 to Table 12-25. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

12.6.3.4 SONY Code

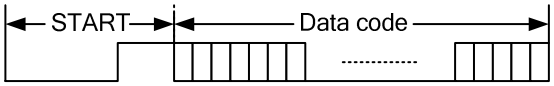
Frame Format

A SONY code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

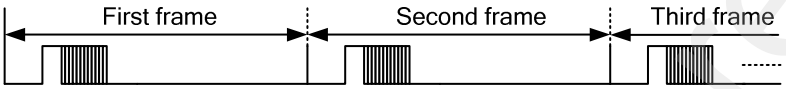
During reception, the LSB is received first. Figure 12-47 shows the frame format for transmitting a single SONY code.

Figure 12-47 Frame format for transmitting a single SONY code



When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 12-48 shows the frame format for continuously transmitting SONY codes by pressing the key.

Figure 12-48 Frame format for continuously transmitting SONY codes by pressing the key



Code Format

Figure 12-49 shows the definitions of bit0 and bit1 of a SONY code.

Figure 12-49 Definitions of bit0 and bit1 of a SONY code

NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 12-23 to Table 12-25.

12.6.4 Operating Mode

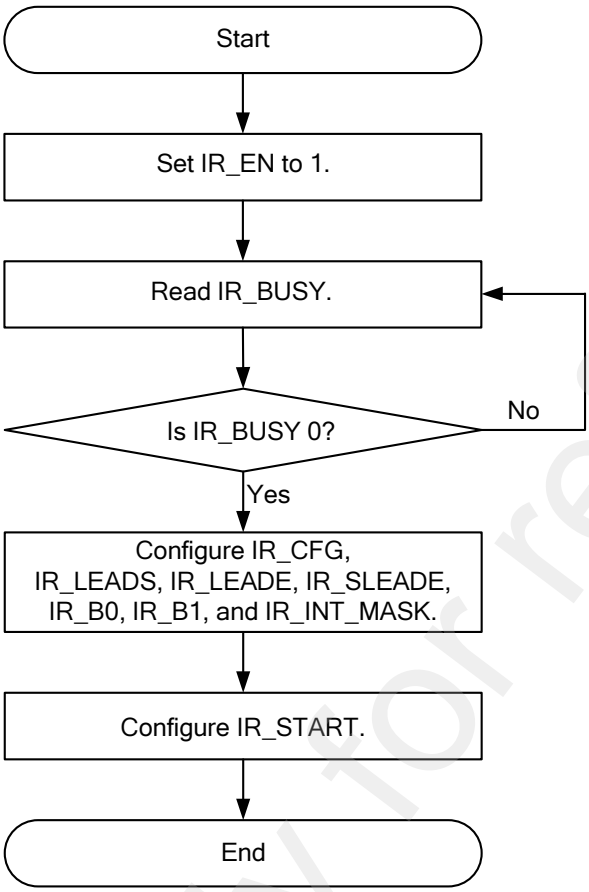
Soft Reset

When PERI_CRG57[ir_srst_req] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 12-50 shows the process of initializing the IR module.

Figure 12-50 Process of initializing the IR module



To initialize the IR module, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Set IR_EN bit [0] to 1 to enable the IR receive module.

Step 3 Read IR_BUSY to check the current status of the IR module.

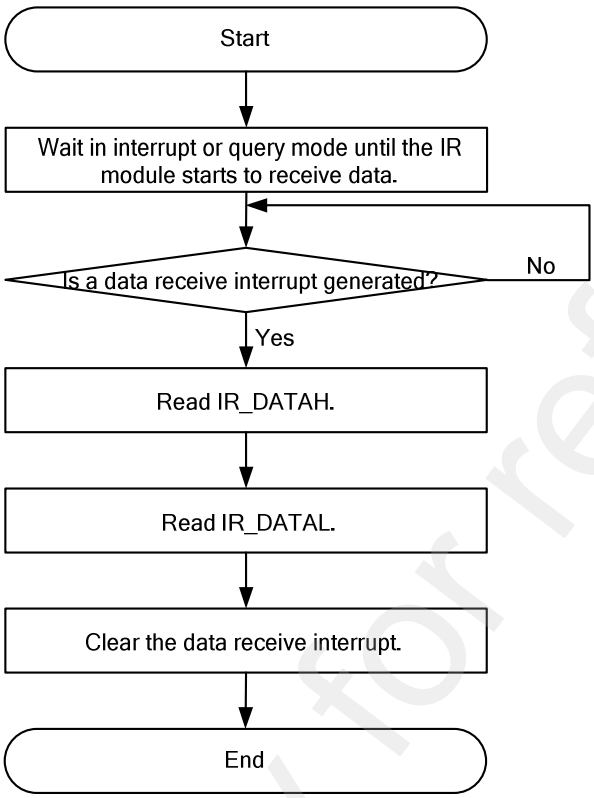
- If the value of IR_BUSY is 1, the IR module is busy. Then continue to read IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.
- If the value of IR_BUSY is 0, the IR module is idle. Then go to Step 4.

Step 4 Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK. Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.

Step 5 Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

----End

Figure 12-51 Process of reading the decoded data



To read the decoded data, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Wait in interrupt or query mode until data frames are received.

- In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[intms_rcv]. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, repeat Step 2 to wait for an interrupt.
- In query mode, continuously read the value of IR_INT_STATUS[intrs_rcv] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, the IR module does not receive any data frame. Then, repeat Step 2 to continue the query.

Step 3 Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.

Step 4 Read IR_DATAL.

Step 5 Clear the data receive interrupt.

----End

12.6.5 Register Summary

Table 12-26 describes IR registers.

Table 12-26 Summary of IR registers (base address: 0x120F_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	12-142
0x004	IR_CFG	IR configuration register	12-142
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	12-144
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	12-145
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	12-146
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	12-147
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	12-148
0x01C	IR_BUSY	Configuration busy flag register	12-149
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)	12-150
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR received symbol width register (IR_CFG[ir_mode] = 1)	12-151
0x028	IR_INT_MASK	IR interrupt mask register	12-151
0x02C	IR_INT_STATUS	IR interrupt status register	12-154
0x030	IR_INT_CLR	IR interrupt clear register	12-156
0x034	IR_START	IR start configuration register	12-157

12.6.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

CAUTION

Before configuring other registers, you must set IR_EN[ir_en] to 1 by using software. When IR_EN[ir_en] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ir_en	IR receive module enable 0: disabled 1: enabled

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before configuring this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value is retained after configuration.

The reference clock frequency supported by the IR module ranges from 1 MHz to 128 MHz. The relationship between the frequency and the clock frequency divider ir_freq is as follows:

- When the reference clock frequency is 1 MHz, ir_freq must be set to 0x00.
- If the reference clock frequency is 128 MHz, ir_freq must be set to 0x7F.

When the frequency of the IR reference clock is not an integer ranging from 1 MHz to 128 MHz, the clock frequency divider is rounded off. For example, if the reference clock frequency is 12.1 MHz, the clock frequency divider is 0x0B; if the reference clock frequency is 12.8 MHz, the clock frequency divider is 0x0C.

The relationship between the frequency offset and the count deviation is as follows: If the base frequency is f and the frequency variation is D_f, the frequency offset ratio is D_f/f. If the count deviation of the counter is Dcnt, and the judge level width is s (in μs), the count deviation Dcnt is calculated as follows: Dcnt = |0.1 x s x ratio|Therefore, when the clock has frequency offset, the valid range of the parameter value needs to be changed. If the frequency increases, the corresponding margin range is changed to [min + Dcnt, max + Dcnt]. Where, min and max indicate the margins without frequency offset. If the frequency decreases, the offset range is changed to [min – Dcnt, max – Dcnt]. Take the margin of the start bit in the lead code as an example. If the base frequency is 100 MHz, and the frequency increases by 0.1 MHz, then the ratio is 0.001 (0.1/100). Assume that s is 9000 μs. Dcnt is calculated as follows: Dcnt = |0.1 x 9,000 x 0.001| = 1. In this case, the margin range of ir_leads must be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_max_level_width																ir_format		ir_bits						ir_mode	ir_freq						
Reset	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[ir_mode] is 0. Indicates the maximum level width (in 10 μs) of a symbol whenIR_CFG[ir_mode] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Indicates the data code format when IR_CFG[ir_mode] is 0. 00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 12-23 to Table 12-25. Indicates the symbol format when IR_CFG[ir_mode] is 1. bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.
[13:8]	RW	ir_bits	Indicates the number of data bits in a frame when IR_CFG[ir_mode] is 0. 0x00–0x2F: 1–48 data bits in a frame

			0x30–0x3F: reserved If ir_bits is set to a value ranging from 0x30 to 0x3F by using software, the setting has no effect and the original value is retained. Indicates the symbol receive interrupt threshold when IR_CFG[ir_mode] is 1. bit[13]: reserved bit[12:8]: 0x0–0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock 0x00–0x7F: correspond to the working clock divider 1–128 respectively.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set Register Description[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specified code types, see the values of LEAD_S in Table 12-23 to Table 12-25.

- For a pulse width whose typical value is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC
- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example. If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								cnt_leads_min								reserved								cnt_leads_max							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code 0x000–0x007: reserved
[15:10]	RO	reserved	Reserved
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code 0x000–0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 12-23 to Table 12-25.

- For the pulse width whose typical value is greater than or equal to 400 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6

- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leade_min								reserved								cnt_leade_max							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code 0x000–0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 12-23 to Table 12-25.

- For a pulse width whose typical value is greater than or equal to 225 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3
- For a pulse width whose typical value is less than 225 (10 μs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_sleade_min								reserved								cnt_sleade_max							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code 0x000–0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type to accurately judging bit0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 12-23 to Table 12-25. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43
- For details about the typical value of the SONY code, see the values of B0_L in Table 12-23 to Table 12-25. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0 0x000–0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 12-23 to Table 12-25. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB
- For details about the typical value of the SONY code, see the values of B1_L in Table 12-23 to Table 12-25. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved								cnt1_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1 0x000–0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	ir_busy	Busy status flag 0: idle state. In this case, software can configure data. 1: busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 12-23 to Table 12-25.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RO	ir_datah	Indicates the upper 16 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the symbol count in the symbol FIFO when IR_CFG[ir_mode] is 1. bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO

IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR receive symbol width register (IR_CFG[ir_mode] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Indicates the lower 32 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the width of the symbol received by the IR module when IR_CFG[ir_mode] is 1. The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

CAUTION

- Before setting this register, you must set IR_EN[ir_en] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[ir_mode] is 0, IR_INT_MASK bit[3:0] are valid; when IR_CFG[ir_mode] is 1, IR_INT_MASK bit[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- RX data overflow interrupt

  If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw RX data overflow error interrupt is reported.
- RX data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw RX frame format error interrupt is reported.
- RX data frame interrupt

  After a complete frame data is received, a raw RX data frame interrupt is reported.
- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.
- RX symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw RX symbol overflow error interrupt is reported.
- RX symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw RX symbol interrupt is reported.
- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_frame_error	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[16]	RW	intm_symb_rcv	RX N symbol interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[15:4]	RO	reserved	Reserved
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[2]	RW	intm_overflow	RX data overflow interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[1]	RW	intm_frame_error	RX data frame format error interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[0]	RW	intm_rcv	RX data frame interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked

IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_frame_error	intms_rcv	reserved				intrs_overrun	intrs_time_out	intrs_symb_rcv		reserved				intrs_release	intrs_overflow	intrs_frame_error	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	intms_symb_rcv	Masked RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	RO	reserved	Reserved
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.

[18]	RO	intms_overflow	Masked RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	intms_frame_error	Masked RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	RO	reserved	Reserved
[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	RO	reserved	Reserved
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	intrs_frame_error	Raw RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.

IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_CLR bit[3:0] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_CLR bit[18:16] are valid.

Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_framerr	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	WC	intc_overrun	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared
[16]	WC	intc_symb_rcv	When IR_CFG[ir_mode] is 1, this bit indicates whether the RX symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	RO	reserved	Reserved
[3]	WC	intc_release	When IR_CFG[ir_mode] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared

[2]	WC	intc_overflow	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data overflow error interrupt request is cleared. 0: no effect 1: cleared
[1]	WC	intc_framerr	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame format error interrupt request is cleared. 0: no effect 1: cleared
[0]	WC	intc_rcv	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame interrupt request is cleared. 0: no effect 1: cleared If an RX data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	ir_start	IR start configuration register

12.7 GPIO

12.7.1 Overview

Hi3519 V100 supports 14 groups of general purpose input/output (GPIO) pins, that is, GPIO0 to GPIO13. Each group of GPIO pins provides eight programmable input/output pins (GPIO13 has only four pins). Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

The GPIO can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) signal provides an indicator to the interrupt controller, indicating that an interrupt occurs.

CAUTION

- For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins and control modes, see *Hi3519V100_PINOUT_EN.xlsx*.
- For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.

12.7.2 Features

Each GPIO pin can be configured as input or output.

- As input, each GPIO pin can act as an interrupt source.
- As output, each GPIO can be set to 0 or 1 separately.

12.7.3 Operating Mode

Interface Reset

The GPIO is reset during chip power-on reset or system reset, and GPIO pins are in input state after being reset.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

Step 1 Enable the required GPIO pins by configuring corresponding pins according to the description of multiplexing registers.

Step 2 Configure the GPIO as input or output by using the GPIO_DIR register.

Step 3 When the GPIO pins are in input mode, read the GPIO_DATA register to check the input signal value. When the GPIO pins are in output mode, write the output value to the GPIO_DATA register to control the output level of the GPIO pins.

----End

CAUTION

When the GPIO pins are in output mode, do not enable the GPIO interrupt. Otherwise, the GPIO interrupt will be generated when output signals meet interrupt generation conditions.

Interrupt Operation

The GPIO interrupt is controlled through seven registers (such as GPIO_IS). These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of the GPIO, see section 3.3 "Interrupt Systems."

When multiple interrupts are generated at the same time, these interrupts are combined into an interrupt and then reported. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt Systems."

The GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status, respectively. GPIO_IEV controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status.

Perform the following operations to configure GPIO pins to the interrupt mode:

Step 1 Select the edge-sensitive mode or level-sensitive mode by configuring the GPIO_IS register.

Step 2 Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.

Step 3 If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

Step 4 Write 0xFF to the GPIO_IC register to clear the interrupt.

Step 5 Set the GPIO_IE to 1 to enable the interrupt.

----End

CAUTION

Ensure that data in GPIO pins is stable during initialization to prevent pseudo interrupts.

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

12.7.4 Register Summary

Table 12-27 lists the base addresses for 14 groups of GPIO registers.

Table 12-27 Base addresses for 14 groups of GPIO registers

Register	Base Address
GPIO13	0x1214_D000
GPIO12	0x1214_C000
GPIO11	0x1214_B000
GPIO10	0x1214_A000
GPIO9	0x1214_9000
GPIO8	0x1214_8000
GPIO7	0x1214_7000
GPIO6	0x1214_6000
GPIO5	0x1214_5000
GPIO4	0x1214_4000
GPIO3	0x1214_3000
GPIO2	0x1214_2000
GPIO1	0x1214_1000
GPIO0	0x1214_0000

Table 12-28 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO13 also have the same internal GPIO registers.

NOTE

- Register address of GPIOn = GPIOn base address + Offset address of the register
- The value of n ranges from 0 to 13.

Table 12-28 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000–0x3FC	GPIO_DATA	GPIO data register	12-161

Offset Address	Register	Description	Page
0x400	GPIO_DIR	GPIO direction control register	12-162
0x404	GPIO_IS	GPIO interrupt trigger register	12-163
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	12-163
0x40C	GPIO_IEV	GPIO interrupt trigger event register	12-164
0x410	GPIO_IE	GPIO interrupt mask register	12-164
0x414	GPIO_RIS	GPIO raw interrupt status register	12-165
0x418	GPIO_MIS	GPIO masked interrupt status register	12-165
0x41C	GPIO_IC	GPIO interrupt clear register	12-166

12.7.5 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example:

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA bit[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA bit[7] is valid.

Offset Address	Register Name	Total Reset Value
0x000–0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit can be controlled separately. 0: input 1: output

GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: No interrupt occurs. 1: An interrupt is generated.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid. 1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: no effect 1: cleared

12.8 PCIe

12.8.1 Overview

The peripheral component interconnect express (PCIe) module is used for extension of the serial advanced technology attachment (SATA) interface and Ethernet port, Wi-Fi, and cascade between chips.

12.8.2 Features

The PCIe controller of the Hi3519 V100 has the following features:

- Supports the PCIe Gen2 X1 controller.
- Supports one VC and one TC.
- Supports root complex (RC) and end point (EP) modes
- Supports DMA.

12.8.3 Signal Description

Table 12-29 describes PCIe interface signals.

Table 12-29 PCIe interface signals

Signal	Direction	Description	Corresponding Pin
Refclk_m	I	Negative terminal of the PCIe reference clock pin	PCIE_REFCLKM

Signal	Direction	Description	Corresponding Pin
Refclk_p	I	Positive terminal of the PCIe reference clock pin	PCIE_REFCLKP
Rx_m	I	Negative terminal of the PCIe RX differential signal	USB3_PCIE_RXM
Rx_p	I	Positive terminal of the PCIe RX differential signal	USB3_PCIE_RXP
Tx_m	O	Negative terminal of the PCIe TX differential signal	USB3_PCIE_TXM
Tx_p	O	Positive terminal of the PCIe TX differential signal	USB3_PCIE_TXP

CAUTION

For Hi3519 V100, the PCIe interface signals are multiplexed with the USB 3.0 port signals. When these signals are used as PCIe interface signals, the USB 3.0 function is unavailable.

If the VO_DATA7 connects to a pull-up resistor, the interface is set to the PCIe mode.

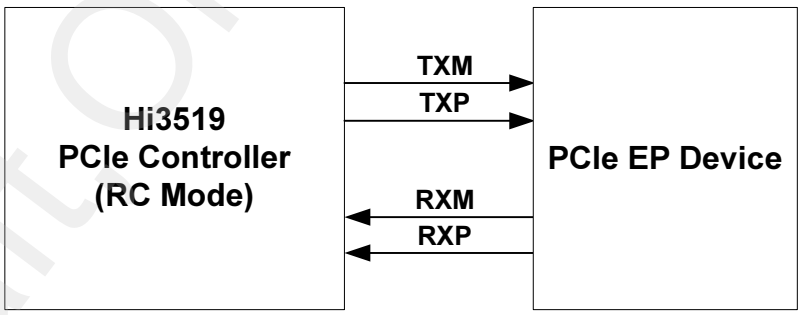
12.8.4 Function Description

RC Mode

In RC mode, the PCIe controller of the Hi3519 V100 can connect to other PCIe EP devices

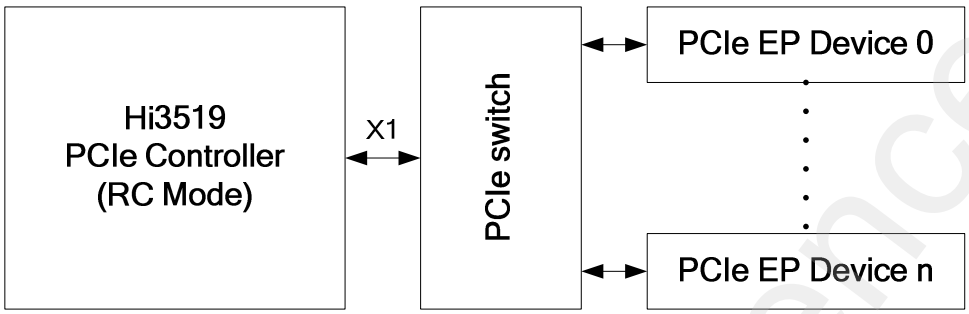
Figure 12-52 shows the application block diagram of the PCIe controller in RC mode.

Figure 12-52 Application block diagram of the PCIe controller (connecting to an EP device in RC mode)



The PCIe controller of the Hi3519V100 can connect to the PCIe switch for expansion. Figure 12-53 shows the application block diagram of the PCIe controller and the PCIe switch in RC mode.

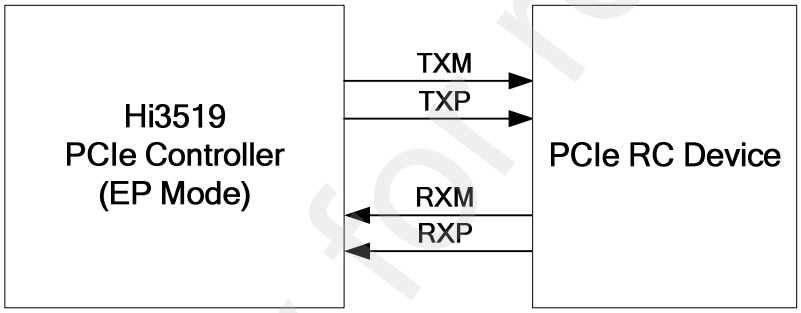
Figure 12-53 Application block diagram of the connection between the PCIe controller and the PCIe switch in RC mode



EP Mode

In EP mode, the PCIe controller of the Hi3519V100can connect to other PCIe RC devices or the PCIe switch for expansion. Figure 12-54 shows the application block diagram in EP mode.

Figure 12-54 Application block diagram of the PCIe controller in EP mode



12.8.5 Operating Mode

12.8.5.1 Clock and Reset

Clock

The PCIe PHY needs a 100 MHz reference clock, which comes from either of the following sources:

- Internal CRG of Hi3519 V100

  Connect VO_DATA5 to a pull-down resistor. In this case, the PCIe interface clock pin is set to the output mode. Hi3519 V100 uses the clock generated by the internal CRG as the PHY reference clock and outputs this internal differential clock to the peer-end device as the reference clock through the PCIe clock pin.

- External PCIe differential clock

  Connect VO_DATA5 to a pull-up resistor. In this case, the PCIe interface clock pin is set to input mode. Hi3519 V100 uses the external differential clock as the PHY reference clock.

Soft Reset

The software can reset the PCIe by using the PCIe reset register PERI_CRG44. For details, see the description of the PERI_CRG44 register in section 3.2.5 "Register Description."

12.8.5.2 Enabling the PCIe Controller

To enable the PCIe controller, perform the following steps:

CAUTION

- Do not enable the PCIe controller before initializing the corresponding system controllers.
- The initialization and direction of the links are the processes of configuring and initializing the physical layers of the devices, ports, and the related links. This enables the links to transfer packets properly. The establishment of the links is automatically established by the hardware. That is, after the PCIe controller is initialized and enabled, the links are automatically established and no software intervention is required.
- Do not initiate any PCI Express transaction before the PCIe links are established.
- The software can check whether the PCIe controller is connected to the peer end device by querying the system control register MISC_CTRL75[pcie_rdlh_link_up].
- For details, see the definitions of the MISC_CTRL75 register.

Step 1 Disable the PCIe controller by writing 0 to the PCIe internal system control register PCIE_SYS_CTRL7[pcie_app_ltssm_enable].

Step 2 Enable the PCIe controller clock by setting the CRG register PERI_CRG44.

Step 3 Set the working mode of the PCIe controller (RC mode or EP mode) by setting the PCIe internal system control register PCIE_SYS_CTRL70[pcie_device_type].

Step 4 Reset the PCIe controller by writing 1 to the CRG register PERI_CRG44[pcie_bus_srst_req].

Step 5 Deassert the reset on the PCIe controller by writing 0 to the CRG register PERI_CRG44[pcie_bus_srst_req].

Step 6 Set the class code registers of the corresponding controllers by writing to 0x060400 (the bridge device of the PCIs) when in RC mode. The class code registers of the PCIe controller is in the configuration register space of the respective PCIe.

Step 7 Enable the PCIe controller by writing 1 to the PCIe internal system control register PCIE_SYS_CTRL7[pcie_app_ltssm_enable]. After the PCIe controller is enabled, it starts to create a link.

----End

12.8.5.3 Initiating the PCIe Transaction by the CPU

By using the local bus interface, the CPU can initiate the bus read and write operation that can be translated into the corresponding PCIe transaction.

Configuration Transaction

The CPU can initiate a configuration transaction only in RC mode.

According to section 12.8.5.5 "Address Translation", the configuration transaction address spaces of PCIe controller is 0x20000000−0x27FFFFFF.

The address translation unit (ATU) of PCIe controller translates the operation on local bus within the address range 0x20000000−0x27FFFFFF into the corresponding PCIe configuration transaction.

When the CPU initiates a bus read/write request on the local bus and the fields of the bus address are as configured as shown in Figure 12-55, PCIe controller can initiate a configuration read/write transaction.

Figure 12-55 Definition of the local address fields of the PCIe controller configuration transaction

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	4				BUS_ID								DEV_ID					FUN_ID			REG_NUM										0	

- BUS_ID: target bus ID of the configuration transaction.
- DEV_ID: target device ID of the configuration transaction.
- FUN_ID: target function ID of the configuration transaction.
- REG_NUM: target register ID of the configuration transaction.

CAUTION

Before initiating type 0 and type 1 configuration transactions, the ATU in the PCIe controller must implement CFG type 0 and CFG type 1 configuration transaction translation regions. For details about the configuration, see the followings:

Assume that the bus ID of the PCIe controller 0 is I, the bus ID of the lower-level device is J (J = I + 1), and the sub bus ID of bus J is K (K = I + 2).

According to the PCIe protocol, PCIe controller initiates a type 0 configuration operation to bus J and initiates a type 1 configuration operation to the bus whose bus ID is greater than J.

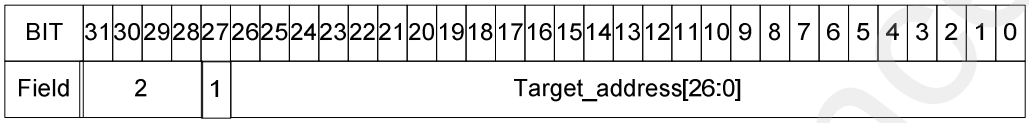
Therefore, an address translation region must be created to translate the local bus address within the region of 0x20J00000–0x20JFFFFF into the address translation region of the type 0 configuration operation. In addition, another address translation region must be created to translate the local bus address within the range of 0x20K00000–0x27FFFFFF into the address translation region of the type 1 configuration transaction.

Memory Transaction

In RC or EP mode, the bus read/write operations initiated by the CPU in the memory transaction address space are translated into the PCIe memory read/write transaction on the PCIe bus.

When the CPU initiates a bus read/write request on the local bus and the fields of the bus address are as configured shown in Figure 12-56, PCIe controller can initiate a memory read/write transaction.

Figure 12-56 Definition of the local address fields of the PCIe controller memory transaction



CAUTION

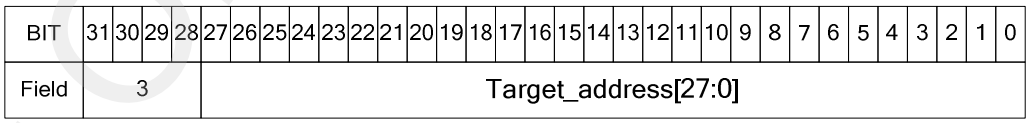
If the original address set by the ATU of the PCIe controller 0 is not within the translation region of 0x28000000−0x2FFFFFFF, the addresses that are within 0x28000000−0x2FFFFFFF on the bus address are not translated. In this case, the PCIe controller 0 can only initiate the memory transaction within the address of 0x28000000−0x2FFFFFFF.

If the PCIe controller is required to initiate the memory transaction outside the address of 0x28000000−0x2FFFFFFF, such as the memory transaction within the address of 0x50000000–0x5FFFFFFF, the PCIe controller must create an address translation region that can implement the mapping between 0x28000000−0x2FFFFFFF and 0x50000000–0x5FFFFFFF. After the address translation region is created, the read and write transaction within the 0x28000000−0x2FFFFFFF address initiated on the local bus can be translated into the memory read and write transaction within the 0x50000000–0x5FFFFFFF address.

I/O transaction

When the CPU initiates a bus read/write request on the local bus and the fields of the bus address are as configured as shown in Figure 12-57, PCIe controller can initiate an I/O read/write transaction.

Figure 12-57 Definition of the local address fields of the PCIe controller I/O transaction



CAUTION

The ATU in the PCIe controller must implement the I/O transaction translation region to translate the operations on the local bus into the PCIe I/O transaction. The operation address initiated on the local bus must be within the range of original address of the I/O transaction translation region.

The I/O transaction is used for compatibility with the PCI card. No dedicated I/O address space is reserved.

However, addresses 0x20000000−0x27FFFFFF (PCIe configuration transaction space) and addresses 0x28000000−0x2FFFFFFF (PCIe memory transaction space) can be used as the I/O address space. The remaining unallocated addresses can be used for I/O transaction translation.

For example, if the PCIe controller needs to initiate an I/O transaction that is not within the addresses 0x28000000−0x2FFFFFF (such as a memory transaction within the addresses 0x50000000−0x5FFFFFFF), the PCIe controller needs to create an address translation region to implement address mapping from addresses 0x28000000−0x2FFFFFF to addresses 0x50000000−0x5FFFFFFF. In this way, the read and write transactions within the addresses 0x28000000−0x2FFFFFF that are initiated by the CPU on the local bus can be translated into the memory read and write transactions within the addresses 0x50000000−0x5FFFFFFF by using the ATU.

12.8.5.4 Initiating a PCIe Transaction by the DMA

The PCIe controller contains a DMA controller. The DMA controller has a DMA read channel and a DMA write channel. The DMA controller in the PCIe controller is used for the memory read and write transactions of large data volume to improve the data transfer rate.

The DMA controller can implement the following memory read/write transactions:

- DMA write: A data block is transferred from the local memory space to the memory space of the peer end device.
- DMA read: A data block is transferred from the peer end device to the local memory space.

The full-duplex operations of the DMA read channel and the DMA write channel can be implemented by configuring the DMA control register. That is, the DMA read and write operations can be performed simultaneously.

DMA Control Register

The software can configure the DMA transfer by using the DMA control register, and also can enable and disable the DMA transfer by using the DMA control register. The DMA control register is in the space of the configuration register of the PCIe register. For details about the definition of the DMA control register, see the description of the PCIe registers in section 12.8.6.4

CAUTION

To reduce the configuration register space occupied by the DMA control register, some of the DMA control register addresses are shared by the DMA read channel and write channel. When these registers need to be configured, the software configures the DMA channel index register DMA_CH_INDEX to indicate the subsequent operated target in these register is the write channel control register or the read channel control register. The DMA control registers mentioned above are the following registers:

- The DMA_CH_CTRL register
- TheDMA_TRANS_SIZE register

- The DMA_SAR_LOW register and the DMA_SAR_HIGH register
- The DMA_DAR_LOW register and the DMA_DAR_HIGH register

For example, to set the DMA transfer length of the DMA read channel 0 to 1024 bytes by the software, perform the following steps:

- The software sets DMA_CH_INDEX [ch_dir] to 1 to indicate the subsequent operated target register is the read channel control register.
- The software sets DMA_TRANS_SIZE to 0x400 to indicate the transfer length is 1024 bytes.

Enabling DMA Read/Write Channels

The DMA channels are disabled by default after the system is reset. The PCIe DMA channels are available only after the DMA read and write channels are enabled.

- To enable the DMA read channel, set the dma_rd_engine_en bit of the DMA_RD_ENGINE_EN register to 1.
- To enable the DMA write channel, set the dma_wr_engine_en bit of the DMA_WR_ENGINE_EN register to 1.

Source Address (SAR) and Target Address (DAR) of the DMA

DMA write: SAR is the local memory space, and DAR is the memory space of the peer end device.

DMA read: SAR is the memory space of the peer end device, and DAR is the local memory space.

The DMA transfer SAR can be specified by configuring the DMA_SAR_LOW and DMA_SAR_HIGH registers corresponding to the DMA read/write channel and the DMA transfer DAR can be specified by setting the DMA_DAR_LOW and DMA_DAR_HIGH registers corresponding to the DMA read/write channel. For details about the DMA SAR and DAR registers, see the definition of the PCIe DMA control register.

During the DMA transfer, the SAR and DAR registers are incremented. The SAR of obtaining data in the current DMA transfer and the DAR of the current write data can be specified by reading the values of the SAR and DAR registers.

Both the SAR and the DAR of the DMA are double-byte aligned. Therefore, the two lowest bits must be set to 0. The two lowest bits are fixed at 0 during data transfer.

DMA Transfer Length

The transfer length for the DMA read/write operation is determined by the DMA_TRANS_SIZE register corresponding to the DMA read/write channel. The value of the DMA_TRANS_SIZE register indicates the bytes of the data that is requested to be transferred. The value of the DMA_TRANS_SIZE register is decremented during the DMA transfer. The remaining bytes to be transferred can be queried by reading the DMA_TRANS_SIZE register. The value of the register is 0 after all date is transferred.

The DMA transfer length ranges from 1 byte to 4 GB.

Starting the DMA Transfer

After the control register in the DMA read channel is configured, the DMA read transfer can be started by writing 0 to the rd_doorbell_num bit of the DMA_RD_DOORBELL register.

After the control register in the DMA read channel is configured, the DMA write transfer can be started by writing 0 to the rwr_doorbell_num bit of the DMA_WR_DOORBELL register.

Stopping the DMA transfer

To stop the DMA read or write transfer manually during the DMA transfer, you can configure the registers as follows:

- To stop the DMA read transfer, write 1 to the dma_rd_stop bit of the DMA_RD_DOORBELL register.
- To stop the DMA write transfer, write1 to the dma_rd_stop bit of the DMA_RD_DOORBELL register.

If no error occurs during the DMA transfer, the DMA transfer is stopped automatically after all data is transferred.

DMA Interrupt

The following two types of interrupts are generated in the DMA channel:

- Complete interrupt. This interrupt indicates that the DMA completes a data transfer.
- Abort interrupt. This interrupt indicates a data transfer by the DMA is aborted, or an error occurs during data transfer.

The DMA read and write channels share an interrupt. After the CPU receives the local interrupt of the PCIe DMA, you can check the interrupt occurrence position (in the DMA read channel or the DMA read channel) and interrupt type (complete interrupt or abort interrupt) by querying DMA_RD_INT_STAT and DMA_WR_INT_STAT. For details, see the description of the DMA_RD_INT_STAT register and the DMA_WR_INT_STAT register.

The complete interrupt or the abort interrupt in the corresponding read or write channel can be cleared by configuring DMA_RD_INT_CLR and DMA_WR_INT_CLR. For details, see the description of DMA_RD_INT_CLR and DMA_WR_INT_CLR.

12.8.5.5 Address Translation

Address Space

Each PCIe controller of the Hi3519V100 uses the following three address spaces:

- Configuration register space: The CPU can access the configuration register of the PCIe controller by using this space.
- Memory and I/O transaction address space: The CPU can initiate a PCIe memory transaction or an I/O transaction by using this space.
- Configuration transaction address space: The CPU can initiate a PCIe configuration read/write transaction by using this space.

Table 12-30 describes the three address spaces used by PCIe controller.

Table 12-30 Address spaces of PCIe controller

Address Space Type	Size	Start Address	End Address	Description
PCIe internal configuration register space	4 KB	0x12160000	0x12160FFF	The space is the configuration register space defined by the PCIe protocol and the PCIe internal system control register space.
PCIe internal system control register space	4 KB	0x12161000	0x12161FFF	The space is the PCIe internal system control register space.
Memory and I/O transaction address space	128 MB	0x20000000	0x27FFFFFF	The read/write operation in this space will be translated into the memory or I/O transaction defined by the PCIe protocol on the PCIe link. In this case, the address translation function is required. For details, see the description of "ATU."
Configuration transaction address space	128 MB	0x28000000	0x2FFFFFFF	The read/write operation in this space will be translated into type 0 configuration transaction or type 1 configuration transaction defined by the PCIe protocol on the PCIe link. In this case, the address translation function is required. For details, see the description of "ATU."

The target address of the configuration register space is the address of the PCIe controller, and the target addresses of other spaces are the addresses of the peer end devices that connect to the PCIe controller. The ATU translates the read/write transactions in different address spaces into the corresponding PCIe transactions, or translates the target addresses.

ATU

The configurations for the transaction type translation and the target address translation may be different in different applications. The Hi3535 provides the ATU to translate different read/write operations at different addresses on the local bus into PCIe transaction. The ATU can also translate target addresses.

The Hi3519 V100 provides six address translation regions on the TX side and the RX side respectively. Each of the address translation regions converts one type of transaction or address.

The ATU on the TX side supports the translation between the address of the local bus operation and the PCIe transaction type, or between the address for the local bus operation and the PCIe transaction address.

Figure 12-58 shows how to translate the local operation address into the PCIe transaction address. If the original address of the local bus is within the range of address translation region A, the ATU translates the local operation address into the address translated by the address region, and the PCIe transaction address on the PCIe bus is replaced by the translated address.

Figure 12-58 PCIe transaction address translation on the TX side

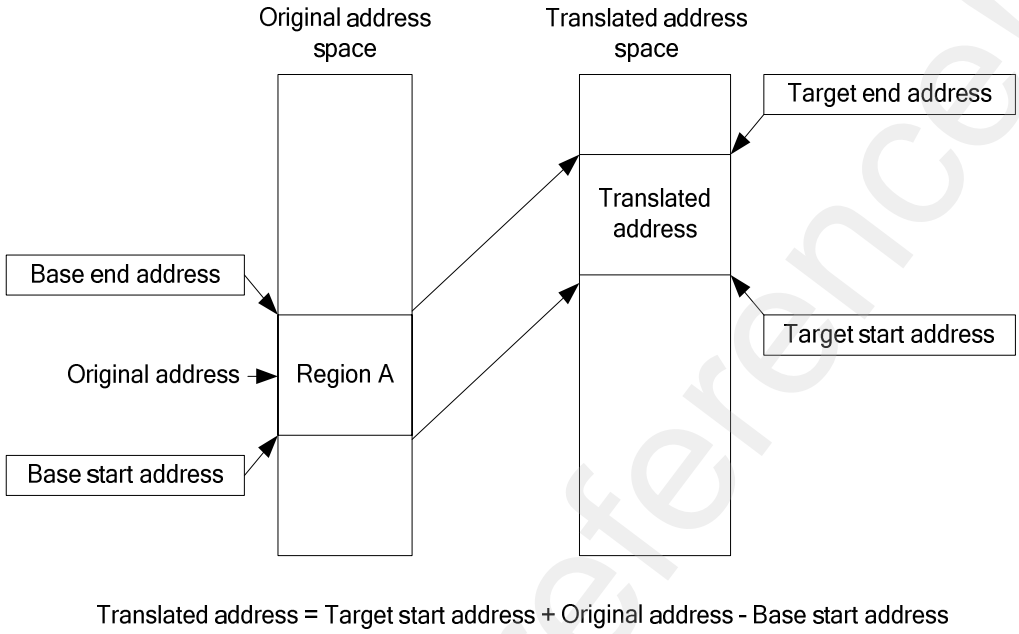
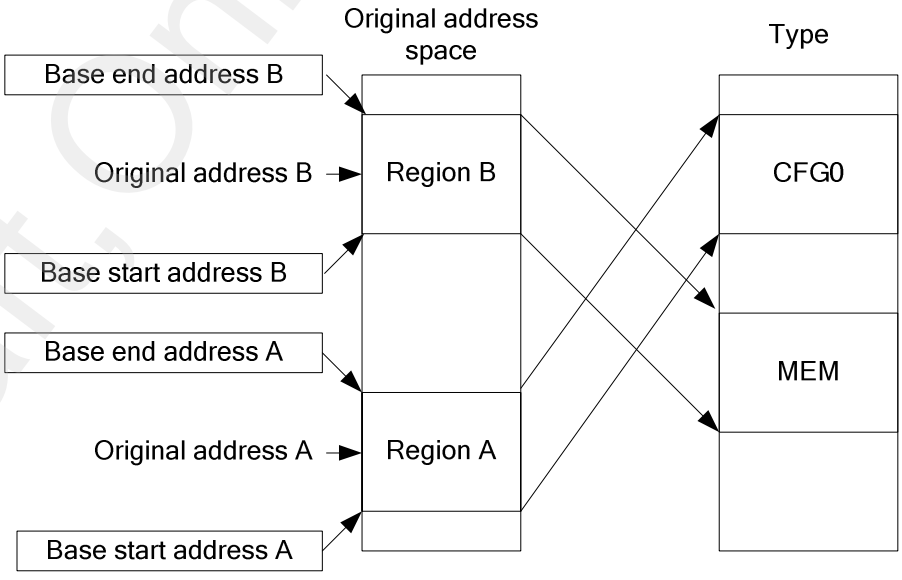


Figure 12-59 shows how to translate the local operation address into the PCIe transaction type. The address translation region A is configured as the translation region that translates certain address range into the PCIe configuration 0 transaction (CFG Type 0). The operation of the local operation address within the address translation region A will be translated into the CFG0 operation on the PCIe bus. The address translation region B is configured as the translation region that translates certain address range into the PCIe memory transaction. The operation of the local operation address within the translation region B will be translated into the memory transaction on the PCIe bus.

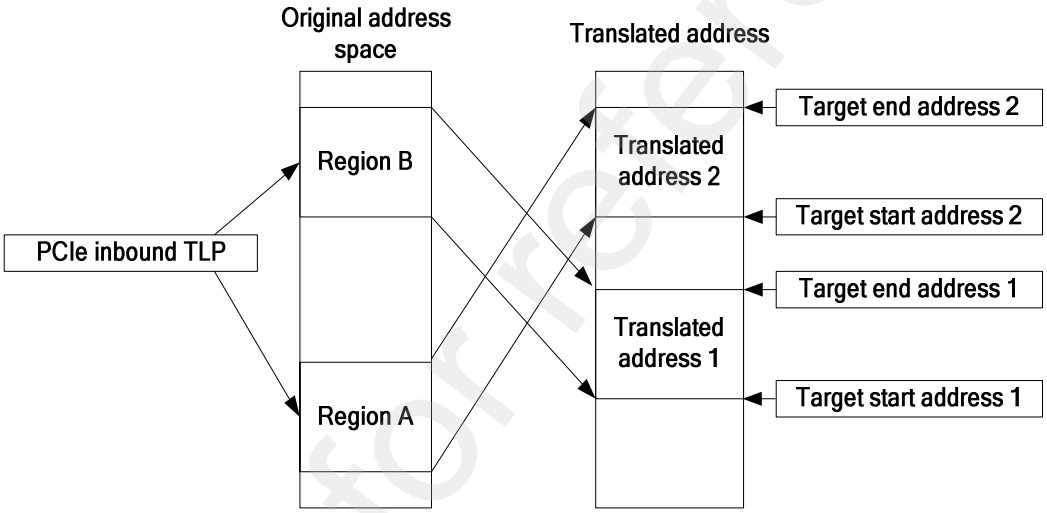
Figure 12-59 PCIe transaction type translation on the TX side



The operations on the local bus can be flexibly translated into the PCIe transactions by configuring each address translation region on the TX side.

Similar to the TX side, the ATU on the RX side can also translate the PCIe transaction into the address of the internal bus. After the PCIe transaction received on the TX side is translated by the address translation region A or B, the corresponding operation can be translated on translated address 1 or translated address 2. If translated address 1 corresponds to the DDR memory address space, the operations that received on the PCIe bus and meet the address translation region conditions can be translated into the operation of the DDR memory space, as shown in Figure 12-60.

Figure 12-60 PCIe transaction address translation on the RX side



ATU Control register

After the system is reset, the ATU on the TX side and the RX side is disabled by default. Therefore, the ATU must be configured and enabled for address translation after the system is reset.

The Hi3519 V100 provides a set of register interfaces to configure the ATU in the PCIe configuration register space. Six address translation regions on the TX side and the RX side can be configured by using this set of registers.

CAUTION

To reduce the configuration register space occupied by the ATU control register, the eight ATU regions on the TX side and the six ATU regions on the RX side are configured by the same set of registers. When one of the twelve ATU regions needs to be configured, the ATU_VIEWPORT register must be configured first to figure out the ATU control register operated by the ATU register are in which ATU region.

For example, to configure the ATU region 3 on the TX side as a valid address translation region, perform the following steps:

- Set ATU_VIEWPORT[atu_reg_region_dir] to 0x0 to indicate the operated target is the ATU region register on the TX side.
- Set ATU_VIEWPORT[atu_reg_region_index] to 0x3 to indicate the operated target is the ATU region 3 on the TX side.
- Set the other ATU register based on the ATU region features.

To configure the ATU, perform the following steps:

Step 1 Set the value of the ATU region number register to the number of the address translation region to be configured.

Step 2 Configure the ATU region lower base address register and the ATU region upper base address register. The target addresses in this region are translated by the ATU where the region number register is located.

Step 3 Configure the ATU region limit address register.

Step 4 Configure the ATU region lower target address register and the ATU region upper target address register.

Step 5 Configure the ATU region control 1 register.

Step 6 Configure the ATU region control 2 register and enable the ATU region.

----End

ATU Configuration

After power-on reset, ATU registers are not configured and the ATU function is disabled. That is, the address and the transaction type cannot be translated. In this case, the operations on the configuration transaction space and I/O transaction space of the local bus initiated address are transferred to the memory transactions on the PCIe bus. The PCIe controller cannot initiate configuration transaction or I/O transaction, and cannot translate addresses.

To enable the PCIe controller to initiate configuration transaction or I/O transaction or implement address translation, you must create an address translation region by using the ATU configuration register.

In RC mode, the RC must provide the functions of translating the operations initiated on the local bus into the configuration transaction on the PCIe bus. To translate the operations on the local bus into different PCIe transaction, the following ATU regions on the TX side must be configured:

- Region 1: It is the type 0 configuration transaction translation region in which the operations on the local bus can be translated into the type 0 configuration transactions (CFG0).
- Region 2: It is the type 1 configuration transaction translation region in which the operations on the local bus can be translated into the type 1 configuration transactions (CFG1).
- Region 3: It is the I/O operation translation region in which the operations on the local bus can be translated into I/O read/write transaction.

The preceding three regions can implement the basic transaction type conversions in RC mode. If necessary, these three regions can be configured based on the actual conditions, and the number of address translation regions also can be added. At most six address translation regions are allowed on the TX side.

To allow the peer end device to access the internal address space of the Hi3519V100 in EP mode, the ATU input regions must be configured as required.

For example, the operation that the peer RC device accesses the Hi3519V100 PCIe BAR0 address space can be mapped into the read/write operation on the DDR space by setting the address translation region 0 on the RX side to the translation region from BAR0 to DDR space in BAR address match mode.

12.8.6 PCIe Controller Registers

PCIe standard registers are included in the space of PCIe controller configuration registers.

When the PCIe controller is set to RC mode, the PCIe configuration register header of type 1 is included in the space; when the PCIe controller is set to EP mode, the PCIe configuration register header of type 0 is included in the space.

For details about the definitions of configuration register headers of type 0 and type 1, see PCIe specifications.

The following describes only the registers defined by PCIe vendors.

12.8.6.1 Register Summary

NOTE

The register base address is 0x1216_0000 for PCIe controller.

Table 12-31 describes the PCIe_iATU registers.

Table 12-31 Summary of the PCIe_iATU registers

Offset Address	Register	Description	Page
0x0900	ATU_VIEWPORT	ATU region number register	12-180
0x0904	ATU_REGION_CTRL1	ATU region control register	12-180
0x0908	ATU_REGION_CTRL2	ATU region control register	12-182
0x090C	ATU_BASE_LOW	ATU region lower base address register	12-185
0x0910	ATU_BASE_HIGH	ATU region upper base address register	12-186
0x0914	ATU_LIMIT	ATU region limit address register	12-186
0x0918	ATU_TARGET_LOW	ATU region lower target address register	12-186

Offset Address	Register	Description	Page
0x091C	ATU_TARGET_HIGH	ATU region upper target address register	12-187

12.8.6.2 Register Description

ATU_VIEWPORT

ATU_VIEWPORT is an ATU region number register.

Offset Address	Register Name	Total Reset Value
0x0900	ATU_VIEWPORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_region_dir	reserved																											atu_reg_region_index			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	atu_reg_region_dir	Region direction The region is the transmit address translation region or the receive address translation region. It is used with the region number to specify ATU region to be used. 0: the transmit address translation region 1: the receive address translation region
[30:4]	RO	reserved	Reserved
[3:0]	RW	atu_reg_region_index	Region number Number of the region that is operated by the address translation control register The region number ranges from 0 to 5.

ATU_REGION_CTRL1

ATU_REGION_CTRL1 is an ATU region control register.

Offset Address	Register Name	Total Reset Value
0x0904	ATU_REGION_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									atu_reg_func_num			reserved		atu_reg_at		reserved				atu_reg_attr		atu_reg_td		atu_reg_tc				atu_reg_type			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	atu_reg_func_num	Function ID Transmit (outbound): When the transmitted TLP packet is in the ATU region, the field of the function ID in the TLP packet is converted into the values of this register. Receive (inbound): When the function ID in the received TLP packet matches the BAR address of the corresponding function ID in this register, the address of the received TLP packet is translated only when the match mode of the receive region is the BAR address match mode.
[19:18]	RO	reserved	Reserved
[17:16]	RW	atu_reg_at	AT field Transmit (outbound): When the transmitted TLP packet is in the ATU region, the AT field in the TLP packet is converted into the value of this register. Receive (inbound): When the AT field in the received TLP packet matches the register, the address of the received TLP is converted.
[15:11]	RO	reserved	Reserved
[10:9]	RW	atu_reg_attr	ATTR field Transmit (outbound): When the transmitted TLP packet is in the ATU region, the ATTR field in the TLP packet is converted into the values of this register. Receive (inbound): When the ATTR field in the received TLP packet matches the register, the address of the received TLP packet is converted.

[8]	RW	atu_reg_td	TD field Transmit (outbound): When the transmitted TLP packet is in the ATU region, the TD field in the TLP packet is converted into the value of this register. Receive (inbound): When the TD field in the received TLP packet matches the register, the address of the received TLP packet is translated.
[7:5]	RW	atu_reg_tc	TC field Transmit (outbound): When the transmitted TLP packet is in the ATU region, the TC field in the TLP packet is converted into the values of this register. Receive (inbound): When the TC field in the received TLP matches the register, the address of the received TLP is translated.
[4:0]	RW	atu_reg_type	TYPE field Transmit (outbound): When the transmitted TLP is in the ATU region, the TYPE field in the TLP packet is converted into the value of this register. Receive (inbound): When the TYPE field in the received TLP packet matches the register, the address of the received TLP packet is translated.

ATU_REGION_CTRL2

ATU_REGION_CTRL2 is an ATU region control register.

Offset Address	Register Name	Total Reset Value
0x0908	ATU_REGION_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_region_enable	atu_reg_in_bar_match	reserved	atu_reg_shift	atu_reg_fuzzy	reserved	atu_reg_rsp_code		reserved		atu_reg_msgcode_match_en	reserved	atu_reg_func_match_en	atu_reg_at_match_en	reserved	atu_reg_attr_match_en	atu_reg_td_match_en	atu_reg_tc_match_en	reserved		atu_reg_bar_num				atu_reg_msg_code							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	atu_reg_region_enable	ATU region enable 0: disabled 1: enabled

[30]	RW	atu_reg_in_bar_match	Receive ATU match mode select Transmit (outbound): no effect Receive (inbound): match mode of receiving the MEM/I/O packets 0: address match mode. When the receive MEM/I/O TLP address matches the address of ATU control register 1, the address is translated. 1: BAR match mode. When the received MEM/I/O TLP address matches the BAR number, the address is translated.
[29]	RO	reserved	Reserved
[28]	RW	atu_reg_shift	Configuration transaction shift function This register is enabled during the configuration type translation. The operation address, bus ID, device ID, and function ID can be translated to access all the configuration spaces by using the 256 MB address space. Transmit (outbound): Assign bits 27–12 of the untranslated address to bits 31–16 bits of the translated address. Receive (inbound): Assign bits 31–16 of the untranslated address to bits 27–12 of the translated address. 0: disabled 1: enabled
[27]	RW	atu_reg_fuzzy	Fuzzy match mode If the fuzzy match mode is enabled, the transaction fuzzy match mode is enabled. 0: disabled 1: enabled
[26]	RO	reserved	Reserved
[25:24]	RW	atu_reg_rsp_code	Complete status code This bit must be set to 0.
[23:22]	RO	reserved	Reserved
[21]	RW	atu_reg_msgcode_match_en	Information code match enable Transmit (outbound): not used Receive (inbound): When the information code match is enabled, the information code of the received TLP packet and atu_reg_msg_code in ATURegionCtrl2 are compared to check whether they match. 0: disabled 1: enabled
[20]	RO	reserved	Reserved

[19]	RW	atu_reg_func_match_en	Function ID match enable Transmit (outbound): not used Receive (inbound): When the function ID match is enabled, function ID of the received TLP packet and atu_reg_func_num in ATURegionCtrl1 are compared to check whether they match. 0: disabled 1: enabled
[18]	RW	atu_reg_at_match_en	AT field match enable Transmit (outbound): not used Receive (inbound): When AT field match is enabled, the AT field of the received TLP packet and atu_reg_at in ATURegionCtrl1 are compared to check whether they match. 0: disabled 1: enabled
[17]	RO	reserved	Reserved
[16]	RW	atu_reg_attr_match_en	ATTR field match enable Transmit (outbound): not used Receive (inbound): When ATTR field match is enabled, the ATTR field of the received TLP packet and the atu_reg_attr in the ATURegionCtrl1are compared to check whether they match. 0: disabled 1: enabled
[15]	RW	atu_reg_td_match_en	TD field match enable Transmit (outbound): not used Receive (inbound): When TD field match is enabled, the TD field of the received TLP packet and the atu_reg_td in the ATURegionCtrl1 are compared to check whether they match. 0: disabled 1: enabled
[14]	RW	atu_reg_tc_match_en	TC field match enable Transmit (outbound): not used Receive (inbound): When TC field match is enabled, the TC field of the received TLP packet and the atu_reg_tc in the ATURegionCtrl1 are compared to check whether they match. 0: disabled 1: enabled
[13:11]	RO	reserved	Reserved

[10:8]	RW	atu_reg_bar_num	BAR number Transmit (outbound): not used Receive (inbound): When the BAR address in the received TLP packet matches the corresponding BAR address of the register, the address in the received TLP packet is translated. 000b: BAR#0 001b: BAR#1 010b: BAR#2 011b: BAR#3 100b: BAR#4 101b: BAR#5 110b: ROM 111b: reserved
[7:0]	RW	atu_reg_msg_code	Information code Transmit (outbound): When the transmitted TLP address matches this region and the atu_reg_type field in the ATURegionCtrl1 is MSG, the register value is set to the value of the MSG field of the translated TLP. Receive (inbound): When atu_reg_msgcode_match_en in ATURegionCtrl2 is enabled and the information code in the received information transaction matches the value of the register, the address in the transaction packet is translated.

ATU_BASE_LOW

ATU_BASE_LOW is an ATU region lower base address register.

Offset Address	Register Name	Total Reset Value
0x090C	ATU_BASE_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_base_low																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	atu_reg_base_low	Bits 31–16 of the start address of this region. When the untranslated address is within the range between start address and address boundary, the address match condition is met. ATUBaseLow and ATUBaseHigh constitute the base address.
[15:0]	RO	reserved	Reserved

ATU_BASE_HIGH

ATU_BASE_HIGH is an ATU region upper base address register.

Offset Address	Register Name	Total Reset Value
0x0910	ATU_BASE_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_base_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	atu_reg_base_high	Upper 32 bits of the base address Bits 63–32 of the start address of this region. When the untranslated address is within the range between start address and address boundary, the address match condition is met. This register is valid only for the 64-bit address. In 32 bits address mode, this register must be set to 0. ATUBaseLow and ATUBaseHigh constitute the base address.

ATU_LIMIT

ATU_LIMIT is an ATU region limit address register.

Offset Address	Register Name	Total Reset Value
0x0914	ATU_LIMIT	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_limit																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	atu_reg_limit	Address limit Bits 31–16 of the start address of this region. When the untranslated address is within the range between start address and address boundary, the address match condition is met.
[15:0]	RO	reserved	Reserved

ATU_TARGET_LOW

ATU_TARGET_LOW is an ATU region lower target address register.

Offset Address	Register Name	Total Reset Value
0x0918	ATU_TARGET_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_trgt_low																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	atu_reg_trgt_low	Lower 32 bits of the target address Bits 31–16 of the translated address. ATUTargetLow and ATUTargetHigh constitute the target address. The address translation formula is as follows: Translated address = Target start address – Base address + Target address Translated address = Target source address – Base address + Target address
[15:0]	RO	reserved	Reserved

ATU_TARGET_HIGH

ATU_TARGET_HIGH is an ATU region upper target address register.

Offset Address	Register Name	Total Reset Value
0x091C	ATU_TARGET_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	atu_reg_trgt_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	atu_reg_trgt_high	Upper 32 bits of the target address Bits 63-32 of the translated address. ATUTargetLow and ATUTargetHigh constitute the target address.

12.8.6.3 Register Summary

NOTE

The register base address is 0x1206_0000 for PCIe controller.

Table 12-32 describes the PCIe_DMA registers.

Table 12-32 Summary of the PCIe_DMA registers

Offset Address	Register	Description	Page
0x097C	DMA_WR_ENGINE_EN	DMA write channel enable register	12-189
0x0980	DMA_WR_DOORBELL	DMA write operation start and stop control register	12-190
0x099C	DMA_RD_ENGINE_EN	DMA read channel enable register	12-191
0x09A0	DMA_RD_DOORBELL	DMA read operation start and stop control register	12-191
0x09BC	DMA_WR_INT_STAT	DMA write operation interrupt status register	12-192
0x09C4	DMA_WR_INT_MASK	DMA write operation interrupt mask register	12-193
0x09C8	DMA_WR_INT_CLR	DMA write operation interrupt clear register	12-193
0x09CC	DMA_WR_ERR_STAT	DMA write operation error status register	12-194
0x09D0	DMA_WR_DONE_IMWR_ADDR_LOW	DMA write done information interrupt lower address register	12-195
0x09D4	DMA_WR_DONE_IMWR_ADDR_HIGH	DMA write done information interrupt upper address register	12-195
0x09D8	DMA_WR_ABORT_IMWR_ADDR_LOW	DMA write abort information interrupt lower address register	12-195
0x09DC	DMA_WR_ABORT_IMWR_ADDR_HIGH	DMA write abort information interrupt upper address register	12-196
0x09E0	DMA_WR_IMWR_DATA_0	DMA write operation information interrupt data register	12-196
0x0A10	DMA_RD_INT_STAT	DMA read operation interrupt status register	12-197
0x0A18	DMA_RD_INT_MASK	DMA read operation interrupt mask register	12-197
0x0A1C	DMA_RD_INT_CLR	DMA read operation interrupt clear register	12-198

Offset Address	Register	Description	Page
0x0A24	DMA_RD_ERR_STAT_LOW	DMA read operation error status lower bit register	12-199
0x0A28	DMA_RD_ERR_STAT_HIGH	DMA read operation error status upper bit register	12-199
0x0A3C	DMA_RD_DONE_IMWR_ADDR_LOW	DMA read done information interrupt lower address register	12-200
0x0A40	DMA_RD_DONE_IMWR_ADDR_HIGH	DMA read done information interrupt upper address register	12-200
0x0A44	DMA_RD_ABORT_IMWR_ADDR_LOW	DMA read abort information interrupt lower address register	12-201
0x0A48	DMA_RD_ABORT_IMWR_ADDR_HIGH	DMA read abort information interrupt upper address register	12-201
0x0A4C	DMA_RD_IMWR_DATA_0	DMA read operation information interrupt data register	12-202
0x0A6C	DMA_CH_INDEX	DMA channel index register	12-202
0x0A70	DMA_CH_CTRL	DMA channel control register	12-203
0x0A78	DMA_TRANS_SIZE	DMA transfer length register	12-204
0x0A7C	DMA_SAR_LOW	DMA lower data source address register	12-204
0x0A80	DMA_SAR_HIGH	DMA upper data source address register	12-205
0x0A84	DMA_DAR_LOW	DMA lower target address register	12-205
0x0A88	DMA_DAR_HIGH	DMA upper target address register	12-206

12.8.6.4 Register Description

DMA_WR_ENGINE_EN

DMA_WR_ENGINE_EN is a DMA write channel enable register.

Offset Address	Register Name	Total Reset Value
0x097C	DMA_WR_ENGINE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															dma_wr_engine_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	dma_wr_engine_en	DMA write channel enable 0: disabled 1: enabled

DMA_WR_DOORBELL

DMA_WR_DOORBELL is a DMA write operation start and stop control register.

Offset Address	Register Name	Total Reset Value
0x0980	DMA_WR_DOORBELL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_wr_stop	reserved																													wr_doorbell_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dma_wr_stop	DMA write channel stop This bit works with wr_doorbell_num to stop the data transfer in the corresponding DMA write channels. 0: no effect 1: Stop current DMA transfer.
[30:3]	RO	reserved	Reserved

[2:0]	RW	wr_doorbell_num	DMA write channel start Start the DMA write transfer by writing 0 to this register. The DMA operation on a write channel starts when the DMA engine detects the write operation on this register. As the PCIe controller supports only one write channel, this register must be set to 0.

DMA_RD_ENGINE_EN

DMA_RD_ENGINE_EN is a DMA read channel enable register.

Offset Address	Register Name	Total Reset Value
0x099C	DMA_RD_ENGINE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															dma_wr_engine_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	dma_wr_engine_en	DMA read channel enable 0: disabled 1: enabled

DMA_RD_DOORBELL

DMA_RD_DOORBELL is a DMA read operation start and stop control register.

Offset Address	Register Name	Total Reset Value
0x09A0	DMA_RD_DOORBELL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_stop	reserved																													rd_doorbell_num	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dma_rd_stop	DMA read channel stop This register works with re_doorbell_num to stop the data transfer in the corresponding DMA read channels. 0: no effect 1: Stop current DMA transfer.
[30:3]	RO	reserved	Reserved
[2:0]	RW	rd_doorbell_num	DMA read channel start Start the DMA read transfer by writing 0 to this register. The DMA operation on a read channel starts when the DMA engine detects the read operation on this register. As the current PCIe controller supports only one read channel, this register must be set to 0.

DMA_WR_INT_STAT

DMA_WR_INT_STAT is a DMA write operation interrupt status register.

Offset Address	Register Name	Total Reset Value
0x09BC	DMA_WR_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															link_el_err_det	reserved															app_rd_err_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	dma_wr_abort_int_stat	Abort interrupt status of the DMA write operation Indicates that the DMA write channel detects errors or the DMA write operation is stopped manually. 0: invalid 1: valid
[15:1]	RO	reserved	Reserved

[0]	RW	dma_wr_done_int_stat	Status of the DMA write operation done interrupt Indicates that a DMA write operation is completed successfully. 0: invalid 1: valid

DMA_WR_INT_MASK

DMA_WR_INT_MASK is a DMA write operation interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x09C4	DMA_WR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dma_wr_abort_int_mask	reserved															dma_wr_done_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	dma_wr_abort_int_mask	Mask of the DMA write operation abort interrupt 0: dma_wr_abort_int_stat generates the edma_int interrupt. 1: dma_wr_abort_int_stat does not generate the edma_int interrupt.
[15:1]	RO	reserved	Reserved
[0]	RW	dma_wr_done_int_mask	Mask of the DMA write operation done interrupt 0: dma_wr_done_int_stat generates the edma_int interrupt. 1: dma_wr_done_int_stat does not generate the edma_int interrupt.

DMA_WR_INT_CLR

DMA_WR_INT_CLR is a DMA write operation interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x09C8	DMA_WR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dma_wr_abort_int_clr	reserved															dma_wr_done_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	dma_wr_abort_int_clr	DMA write operation abort interrupt clear Writing 1 clears the dma_wr_abort_int_stat interrupt status of the DMA_WR_INT_STAT register.
[15:1]	RO	reserved	Reserved
[0]	RW	dma_wr_done_int_clr	DMA write operation done interrupt clear Writing 1 clears the dma_wr_done_int_stat interrupt status of the DMA_WR_INT_STAT register.

DMA_WR_ERR_STAT

DMA_WR_ERR_STAT is a DMA write operation error status register.

Offset Address	Register Name	Total Reset Value
0x09CC	DMA_WR_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															reserved	reserved															app_rd_err_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	reserved	Reserved
[15:1]	RO	reserved	Reserved

[0]	RW	app_rd_err_det	Read data error of the DMA write channel

DMA_WR_DONE_IMWR_ADDR_LOW

DMA_WR_DONE_IMWR_ADDR_LOW is a DMA write done information interrupt lower address register.

Offset Address	Register Name	Total Reset Value
0x09D0	DMA_WR_DONE_IMWR_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_wr_done_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_done_imwr_addr_low	Lower 32 bits of the DMA read done interrupt information address

DMA_WR_DONE_IMWR_ADDR_HIGH

DMA_WR_DONE_IMWR_ADDR_HIGH is a DMA write done information interrupt upper address register.

Offset Address	Register Name	Total Reset Value
0x09D4	DMA_WR_DONE_IMWR_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_wr_done_imwr_addr_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_done_imwr_addr_high	Upper 32 bits of the DMA read done interrupt information address

DMA_WR_ABORT_IMWR_ADDR_LOW

DMA_WR_ABORT_IMWR_ADDR_LOW is a DMA write abort information interrupt lower address register.

Offset Address	Register Name	Total Reset Value
0x09D8	DMA_WR_ABORT_IMWR_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_wr_abort_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_abort_imwr_addr_low	Lower 32 bits of the DMA read abort interrupt information address

DMA_WR_ABORT_IMWR_ADDR_HIGH

DMA_WR_ABORT_IMWR_ADDR_HIGH is a DMA write abort information interrupt upper address register.

Offset Address	Register Name	Total Reset Value
0x09DC	DMA_WR_ABORT_IMWR_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_wr_abort_imwr_addr_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_wr_abort_imwr_addr_high	Upper 32 bits of the DMA read abort interrupt information address

DMA_WR_IMWR_DATA_0

DMA_WR_IMWR_DATA_0 is a DMA write operation information interrupt data register.

Offset Address	Register Name	Total Reset Value
0x09E0	DMA_WR_IMWR_DATA_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dma_wr_imwr_data_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	dma_wr_imwr_data_0	Interrupt information data of DMA write channel 0

DMA_RD_INT_STAT

DMA_RD_INT_STAT is a DMA write operation interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0A10	DMA_RD_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dma_wr_abort_int_stat	reserved															dma_wr_done_int_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	dma_wr_abort_int_stat	Status of the DMA read operation abort interrupt Indicates that the DMA read channel detects errors or the DMA write operation is stopped manually. 0: invalid 1: valid
[15:1]	RO	reserved	Reserved
[0]	RW	dma_wr_done_int_stat	Status of the DMA read operation done interrupt Indicates that a DMA read operation is completed successfully. 0: invalid 1: valid

DMA_RD_INT_MASK

DMA_RD_INT_MASK is a DMA read operation interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0A18	DMA_RD_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dma_wr_abort_int_mask	reserved															dma_wr_done_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	dma_wr_abort_int_mask	Mask of the DMA read operation abort interrupt 0: dma_rd_abort_int_stat generates the edma_int interrupt. 1: dma_rd_abort_int_stat does not generate the edma_int interrupt.
[15:1]	RO	reserved	Reserved
[0]	RW	dma_wr_done_int_mask	Mask of the DMA read operation done interrupt 0: dma_rd_done_int_stat generates the edma_int interrupt. 1: dma_rd_done_int_stat does not generate the edma_int interrupt.

DMA_RD_INT_CLR

DMA_RD_INT_CLR is a DMA read operation interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0A1C	DMA_RD_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															dma_wr_abort_int_clr	reserved															dma_wr_done_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved

[16]	RW	dma_wr_abort_int_clr	DMA read operation abort interrupt clear Writing 1 clears the dma_rd_abort_int_stat interrupt status of the DMA_RD_INT_STAT register.
[15:1]	RO	reserved	Reserved
[0]	RW	dma_wr_done_int_clr	DMA read operation abort interrupt clear Writing 1 clears the dma_rd_done_int_stat interrupt status of the DMA_RD_INT_STAT register.

DMA_RD_ERR_STAT_LOW

DMA_RD_ERR_STAT_LOW is a DMA read operation error status lower bit register.

Offset Address	Register Name	Total Reset Value
0x0A24	DMA_RD_ERR_STAT_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															reserved	reserved															app_rd_err_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	reserved	Reserved
[15:1]	RO	reserved	Reserved
[0]	RW	app_rd_err_det	Advanced eXtensible interface (AXI) bus error response error detected by the DMA read channel

DMA_RD_ERR_STAT_HIGH

DMA_RD_ERR_STAT_HIGH is a DMA read operation error status upper bit register.

Offset Address	Register Name	Total Reset Value
0x0A28	DMA_RD_ERR_STAT_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							dp_err	reserved							to_err	reserved							ca_err	reserved							ur_err

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	dp_err	The DMA channel detects the poisoned data of the peer end device.
[23:17]	RO	reserved	Reserved
[16]	RW	to_err	Read timeout for the DMA channel
[15:9]	RO	reserved	Reserved
[8]	RW	ca_err	The DMA channel detects the completion abort (CA) of the peer end device.
[7:1]	RO	reserved	Reserved
[0]	RW	ur_err	The DMA channel detects the unsupported request (UR) of the peer end device.

DMA_RD_DONE_IMWR_ADDR_LOW

DMA_RD_DONE_IMWR_ADDR_LOW is a DMA read done information interrupt lower address register.

Offset Address	Register Name	Total Reset Value
0x0A3C	DMA_RD_DONE_IMWR_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_done_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_rd_done_imwr_addr_low	Lower 32 bits of the DMA read done interrupt information address

DMA_RD_DONE_IMWR_ADDR_HIGH

DMA_RD_DONE_IMWR_ADDR_HIGH is a DMA read done information interrupt upper address register.

Offset Address	Register Name	Total Reset Value
0x0A40	DMA_RD_DONE_IMWR_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_done_imwr_addr_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_rd_done_imwr_addr_high	Upper 32 bits of the DMA read done interrupt information address

DMA_RD_ABORT_IMWR_ADDR_LOW

DMA_RD_ABORT_IMWR_ADDR_LOW is a DMA read abort information interrupt lower address register.

Offset Address	Register Name	Total Reset Value
0x0A44	DMA_RD_ABORT_IMWR_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_abort_imwr_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_rd_abort_imwr_addr_low	Upper 32 bits of the DMA read abort interrupt information address

DMA_RD_ABORT_IMWR_ADDR_HIGH

DMA_RD_ABORT_IMWR_ADDR_HIGH is a DMA read abort information interrupt upper address register.

Offset Address	Register Name	Total Reset Value
0x0A48	DMA_RD_ABORT_IMWR_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_rd_abort_imwr_addr_high																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_rd_abort_imwr_addr_high	Upper 32 bits of the DMA read abort interrupt information address

DMA_RD_IMWR_DATA_0

DMA_RD_IMWR_DATA_0 is a DMA write operation information interrupt data register.

Offset Address	Register Name	Total Reset Value
0x0A4C	DMA_RD_IMWR_DATA_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dma_wr_imwr_data_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dma_wr_imwr_data_0	Interrupt information data of DMA read channel 0

DMA_CH_INDEX

DMA_CH_INDEX is a DMA channel index register.

Offset Address	Register Name	Total Reset Value
0x0A6C	DMA_CH_INDEX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch_dir	reserved																													reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ch_dir	Channel direction Configuring this bit sets the channel of a register to write channel or read channel. 0: write channel 1: read channel
[30:3]	RO	reserved	Reserved

[2:0]	RO	reserved	Reserved. This bit must be set to 0.

DMA_CH_CTRL

DMA_CH_CTRL is a DMA channel control register.

Offset Address	Register Name	Total Reset Value
0x0A70	DMA_CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addr_trans		traffic_class			traffic_digest	relaxed_order	no_snoop	reserved				fun_num				reserved				reserved				ch_status				local_int_enable			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	addr_trans	PCIe transaction AT bit The AT bit in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[29:27]	RW	traffic_class	PCIe transaction TC bit The TC bit in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[26]	RW	traffic_digest	PCIe transaction TD bit The TD bit in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[25]	RW	relaxed_order	PCIe transaction RO bit The RO bit in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[24]	RW	no_snoop	PCIe transaction NS bit The NS bit in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[23:17]	RO	reserved	Reserved
[16:12]	RW	fun_num	PCIe transaction fun_num bit The function ID in the PCIe memory read/write transaction packet initiated by the DMA is replaced by the member value.
[11:8]	RO	reserved	Reserved
[7]	RO	reserved	Reserved

[6:5]	RW	ch_status	Channel status 00: reserved 01: A DMA transfer is being performed. 10: An error occurs when the DMA channel works. 11: A DMA transfer is completed by the channel successfully or the transfer is stopped manually.
[4]	RO	reserved	Reserved
[3]	RW	local_int_enable	Local DMA interrupt enable After this bit is set to valid, a local DMA interrupt can be transmitted when the DMA transfer is complete or fails. 0: disabled 1: enabled
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

DMA_TRANS_SIZE

DMA_TRANS_SIZE is a DMA transfer length register

Offset Address	Register Name	Total Reset Value
0x0A78	DMA_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_trans_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_trans_size	DMA transfer length The length of the data to be transferred must be written to this register before DMA transfer. The data length ranges from 1 byte to 4 GB. The register value is automatically decremented during the DMA transfer. The register value is the remaining bytes and is 0 after the transfer is complete.

DMA_SAR_LOW

DMA_SAR_LOW is a lower DMA data source address register.

Offset Address	Register Name	Total Reset Value
0x0A7C	DMA_SAR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_sar_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_sar_low	Lower 32 bits of the source address for DMA transfer The start address of the source data must be written to this register before the DMA transfer and the DMA channel obtains the data to be transferred from this start address. The register value is automatically incremented during the DMA transfer. The lower two bits of this register bits must be 0.

DMA_SAR_HIGH

DMA_SAR_HIGH is an upper DMA data source address register.

Offset Address	Register Name	Total Reset Value
0x0A80	DMA_SAR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_sar_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_sar_high	Upper 32 bits of the source address for the DMA transfer data This field must be 0 in 32-bit address mode. This register and DMA_SAR_LOW constitute a 64-bit source address in 64-bit mode.

DMA_DAR_LOW

DMA_DAR_LOW is a lower DMA target address register.

Offset Address	Register Name	Total Reset Value
0x0A84	DMA_DAR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_dar_low																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_dar_low	Lower 32 bits of the target address for the DMA transfer The target address must be written to this register before the DMA transfer and the DMA channel writes the data obtained from the source address to the target address. The values of this register are decremented automatically during the DMA transfer. The lower two bits of this register must be 0.

DMA_DAR_HIGH

DMA_DAR_HIGH is an upper DMA target address register.

Offset Address	Register Name	Total Reset Value
0x0A88	DMA_DAR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_dar_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_dar_high	Upper 32 bits of the target address for the DMA transfer data (upper 32 bits) The bits must be 0 in 32 bits address mode. The register and DMA_DAR_LOW constitute a 64-bit source address in 64-bit mode.

12.9 USB 2.0

12.9.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using in the controller, the following functions are achieved:

- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.

- Provide interfaces (such as the interrupt vector interface) for the driver.

The USB 2.0 device controller supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s) data transfer modes. It also supports host/device intelligent switching.

12.9.2 Function Description

Logic Block Diagram

Figure 12-61 shows the logic block diagram of the USB 2.0 host controller.

Figure 12-61 Logic block diagram of the USB 2.0 host controller

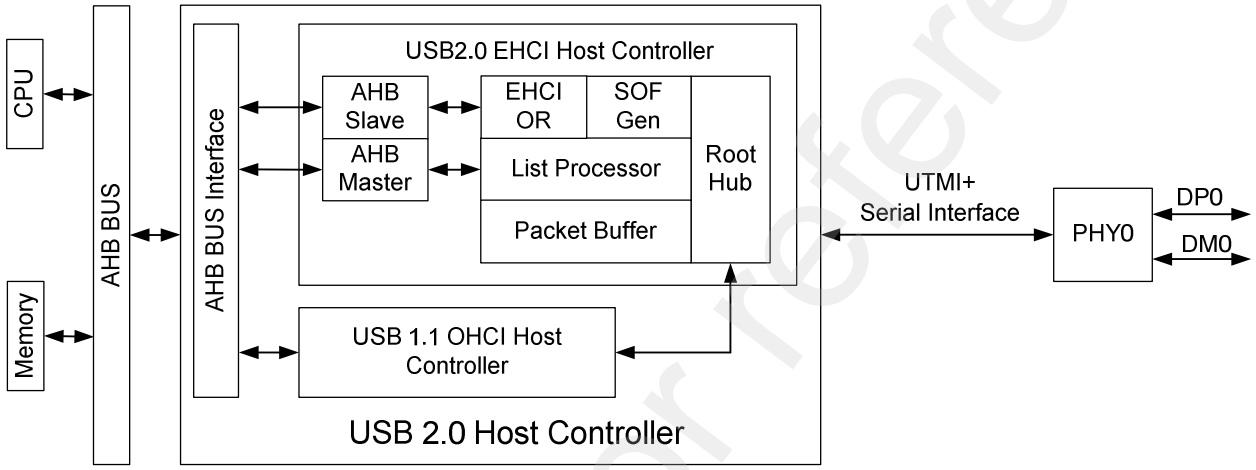
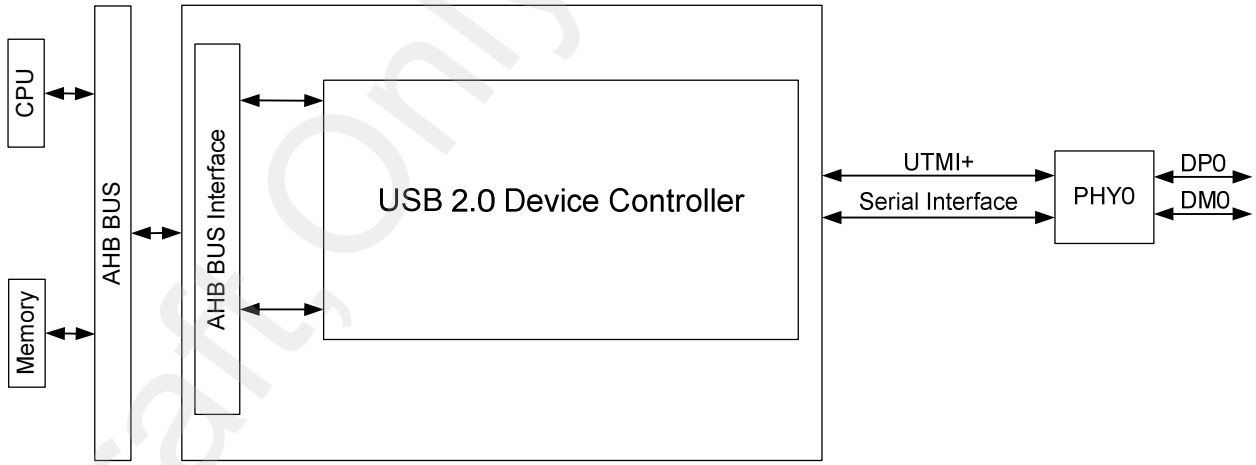


Figure 12-62 shows the logic block diagram of the USB 2.0 device.

Figure 12-62 Logic block diagram of the USB 2.0 device controller



NOTE

- UTMI: USB2.0 transceiver macrocell interface
- EHCI: enhanced host controller interface

- OHCI: open host controller interface

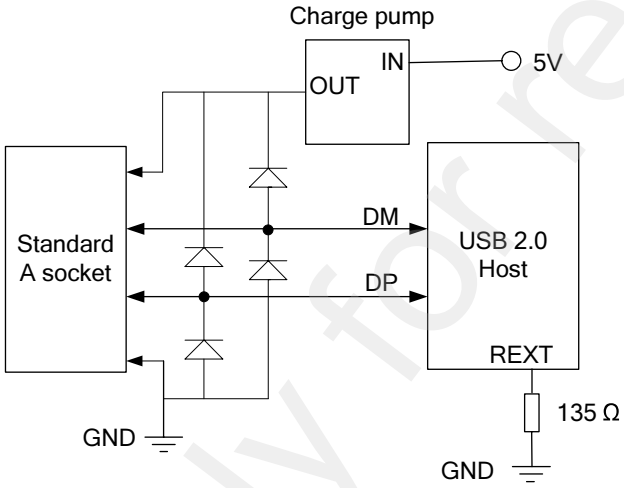
Typical Application

Figure 12-63 shows the reference design of the USB 2.0 host controller.

CAUTION

- The impedance of DP or DM is 45 Ω ±1% and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electro static discharge (ESD) components are used, 1 pF capacitors are recommended.

Figure 12-63 Reference design of the USB 2.0 host controller



Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

The USB 2.0 device controller has the following features:

- Complies with the USB 2.0 standard.

- Supports high-speed, full-speed, and low-speed devices.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.

Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode applies to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.

- Bulk transfer

  This mode applies to transmission and reception of bulk data when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and a large amount of data is delayed. Bulk transfer can be performed after all other types of data have been transferred. In bulk transfer mode, data is transferred between the USB host and the USB device without errors by using an error detection and retransmission mechanism.

- Isochronous transfer

  This mode applies to the data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

  This mode applies to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

12.9.3 Operating Mode

Host/Device Switching

You can configure the MISC_CTRL30[usb_chipid] to operate in host or device mode.

To enable the register to operate in host mode, set MISC_CTRL30[usb_chipid] to 0 and MISC_CTRL30[usb2_phy_dmpulldown] and MISC_CTRL30[usb2_phy_dppulldown] to 1.

To enable the register to operate in device mode, set MISC_CTRL30[usb_chipid] to 1 and MISC_CTRL30[usb2_phy_dmpulldown] and MISC_CTRL30[usb2_phy_dppulldown] to 0.

Pin Polarity Control

The valid polarity of USB_PWREN can be configured by setting MISC_CTRL30[usbpwr_p_ctrl].

The valid polarity of USB0_OVRCUR and USB1_OVRCUR can be configured by setting MISC_CTRL30[usbovr_p_ctrl].

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

Step 1 Write 1 to PERI_CRG45 [usb_phy_port0_treq], PERI_CRG45[usb_phy_req], PERI_CRG45[usb_ctrl_utmi0_req], PERI_CRG45[usb_otg_phy_srst_req], and PERI_CRG45[usb_hrst_req] respectively to reset the USB controller and PHY.

Step 2 Set PERI_CRG45 [usb_cken] to 0 to disable the clocks of the USB 2.0 host controller.

----End

To enable the clock, perform the following steps:

Step 1 Set PERI_CRG45 [usb_cken] to 1 to enable the clocks of the USB 2.0 host controller.

Step 2 Deassert the reset on the USB controller and PHY. For details, see "Reset Deassert"

----End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

Step 1 Delay at least 10 μs.

Step 2 Write 0 to PERI_CRG45[usb_phy_treq] to deassert the POR on the USB PHY.

Step 3 After a delay of at least 1 ms, and write 0 to PERI_CRG45[usb_phy_port0_treq] to deassert the soft reset on USB PHY port 0.

Step 4 After a delay of at least 100 μs, and write 0 to PERI_CRG45[usb_ctrl_utmi0_req], PERI_CRG45[usb_otg_phy_srst_req], and PERI_CRG45[usb_hrst_req] to deassert the soft reset on USB host controller port 0, USB device controller, and USB bus respectively.

----End

Separately Resetting Ports During the Working Process

To reset port separately during the working process, perform the following steps:

Step 1 Write 1 to PERI_CRG45[usb_ctrl_utmi0_req] and PERI_CRG45[usb_otg_phy_srst_req] to soft-reset port0 of the USB controller.

Step 2 Write 1 to PERI_CRG45[usb_phy_port0_treq] to soft-reset port0 of the USB PHY.

Step 3 After a delay of at least 100 μs, write 0 to PERI_CRG45[usb_phy_port0_treq] to deassert the reset on port0 of the USB PHY.

Step 4 Write 0 to PERI_CRG45[usb_ctrl_utmi0_req] and PERI_CRG45[usb_otg_phy_srst_req] to deassert the reset on port 0 of the USB controller.

----End

Variables in the Offset Addresses for USB 2.0 Registers

Table 12-33 describes the value ranges and meanings of the variables in the offset addresses of registers.

Table 12-33 Variables in the offset addresses for USB 2.0 registers

Variable	Value Range	Description
FIFO_num	0–14	Number of FIFOs
n	0–15	Endpoint *n*

12.9.4 Register Summary

USB HOST Register

Table 12-34 describes USB 2.0 registers.

Table 12-34 Summary of USB 2.0 registers (base address: 0x1012_0000)

Offset Address	Register	Description	Page
0x90	INTNREG00	Micro-frame length configuration register	12-215
0x94	INSNREG01	PBUF OUT/IN register	12-215
0x98	INSNREG02	PBUF depth register	12-216
0x9C	INSNREG03	Interrupt memory transfer enable register	12-216
0xA0	INTNREG04	Debug register	12-217
0xA4	INTNREG05	UTMI Vendor Control and status register	12-218
0xA8	INTNREG06	AHB error status register	12-218
0xAC	INTNREG07	AHB error address register	12-219

NOTE

The base address of the EHCI register is 0x1012_0000 and the base address of the OHCI register is 0x1011_0000. The base address of Table 12-34 is that of the EHCI register.

USB Device Register Overview

Table 12-35 describes the UBS device register overview.

Table 12-35 USB device register overview (base address: 0x1013_0000)

Offset Address	Name	Description	Page
0x0000	GOTGCTL	Device behavior control and status query register	12-220
0x0004	GOTGINT	Device interrupt generation indicator/clear register	12-222
0x0008	GAHBCFG	AHB configuration register	12-223
0x000C	GUSBCFG	USB configuration register	12-225
0x0010	GRSTCTL	Reset hardware feature register	12-228
0x0014	GINTSTS	System interrupt register	12-231
0x0018	GINTMSK	System interrupt mask register	12-234
0x001C	GRXSTSR	RX status debug read register	12-237
0x0020	GRXSTSP	RX status read&pop register	12-238
0x0024	GRXFSIZ	RX FIFO size configuration register	12-239
0x0028	GNPTXFSIZ	Non-periodic TX FIFO size configuration register	12-240
0x002C	GNPTXSTS	Non-periodic TX FIFO and non-periodic TX request query register	12-240
0x0030	GI2CCTL	I^2C access register	12-241
0x0034	GPVNDCTL	PHY vendor control register	12-242
0x0038	GGPIO	GPIO register	12-244
0x003C	GUID	User ID query register	12-244
0x0040	GSNPSID	Synopsys ID query register	12-244
0x0044	GHWCFG1	User hardware configuration register 1	12-245
0x0048	GHWCFG2	User hardware configuration register 2	12-245
0x004C	GHWCFG3	User hardware configuration register 3	12-247
0x0050	GHWCFG4	User hardware configuration register 4	12-249
0x0054	GLPMCFG	LPM configuration register	12-251
0x0058	GPWRDN	Power-down register	12-254
0x005C	GDFIFOCFG	DFIFO software configuration register	12-257

Offset Address	Name	Description	Page
0x0060	GADPCTL	ADP timer control and status register	12-257
0x0100	HPTXFSIZ	TX FIFO configuration register	12-260
0x0104 + 0x0004 x FIFO_num	DPTXFSIZN	Device periodic TX FIFO-n size register	12-260
0x0104 + 0x0004 x FIFO_num	DIEPTXFN	Device IN endpoint TX FIFO size register	12-261
0x0800	DCFG	Device configuration register	12-261
0x0804	DCTL	Device control register	12-263
0x0808	DSTS	Device status register	12-264
0x0810	DIEPMSK	Common interrupt mask register for device IN endpoints	12-265
0x0814	DOEPMSK	Common interrupt mask register for device OUT endpoints	12-267
0x0818	DAINT	Interrupt register for all device endpoints	12-268
0x081C	DAINTMSK	Interrupt mask register for all endpoints	12-269
0x0820	DTKNQR1	Device IN token learning sequence queue read register 1	12-270
0x0824	DTKNQR2	Device IN token learning sequence queue read register 2	12-270
0x0830	DTKNQR3	Device IN token learning sequence queue read register 3	12-271
0x0834	DTKNQR4	Device IN token learning sequence queue read register 4	12-271
0x0828	DVBUSDIS	Device VBUS discharge time register	12-272
0x082C	DVBUSPULSE	Device VBUS pulsing time register	12-272
0x0830	DTHRCTL	Device threshold control register	12-272
0x0834	DIEPEMPMSK	FIFO empty interrupt mask register for device IN endpoints	12-274
0x0838	DEACHINT	Interrupt register for each device endpoint	12-274
0x083C	DEACHINTMSK	Interrupt register for each device endpoint	12-275
0x0840 + (0x0004 x *n*)	DIEPEACHMSKN	Interrupt register for each device IN endpoint-n	12-275
0x0880 + (0x0004 x *n*)	DOEPEACHMSKN	Interrupt register for each device OUT endpoint-n	12-277

Offset Address	Name	Description	Page
0x0900	DIEPCTL0	Control register for device control IN endpoint 0	12-278
0x0B00	DOEPCTL0	Control register for device control OUT endpoint 0	12-280
0x0900 + (0x0020 x *n*)	DIEPCTLN	Device IN endpoint-n control register	12-282
0x0B00 + (0x0020 x *n*)	DOEPCTLN	Device OUT endpoint-n control register	12-285
0x0908 + (0x0020 x *n*)	DIEPINTn	Device IN endpoint-n interrupt register	12-288
0x0B08 + (0x0020 x *n*)	DOEPINTn	Device OUT endpoint-n interrupt register	12-291
0x0910	DIEPTSIZ0	Transfer size register for device IN endpoint 0	12-294
0x0B10	DOEPTSIZ0	Transfer size register for device OUT endpoint 0	12-294
0x0910 + (0x0020 x *n*)	DIEPTSIZn	Transfer size register for device IN Endpoint-n	12-295
0x0B10 + (0x0020 x *n*)	DOEPTSIZn	Transfer size register for device OUT endpoint-n	12-296
0x0914 + (0x0020 x *n*)	DIEPDMAN	Device IN endpoint-n DMA address register	12-297
0x0B14 + (0x0020 x *n*)	DOEPDMAN	Device OUT endpoint-n DMA address register	12-297
0x091C + (0x0020 x *n*)	DIEPDMABN	Device IN endpoint-n DMA buffer address register	12-298
0x0B1C + (0x0020 x *n*)	DOEPDMABN	Device OUT endpoint-n DMA buffer address register	12-298
0x0938	DTXFSTSn	Device IN endpoint TX FIFO status register	12-299

12.9.5 Register Description

12.9.5.1 USB HOST Register Description

INTNREG00

INTNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				val											en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:1]	RW	val	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 µs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	en	Micro-frame length register enable 0: disabled 1: enabled

INSNREG01

INTNREG01 is a PBUF out/in configuration register.

Offset Address	Register Name	Total Reset Value
0x94	INSNREG01	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_threshold																in_threshold															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	out_threshold	TX threshold. If the data amount in the PBUF is above the TX threshold, data starts to be transmitted. The depth is measured by 32 bits.
[15:0]	RW	in_threshold	RX threshold. If the data amount in the PBUF is above the RX threshold, data is read from the PBUF. The depth is measured by 32 bits.

INSNREG02

INSNREG02 is a PBUF depth configuration register.

Offset Address	Register Name	Total Reset Value
0x98	INSNREG02	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pbuf_depth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	pbuf_depth	PBUF depth. The depth is measured by 32 bits.

INSNREG03

INSNREG03 is an interrupt memory transfer enable register.

Offset Address	Register Name	Total Reset Value
0x9C	INSNREG03	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dis	ctrl	val		fetch	offset										brk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	dis	256 MHz clock check enable 0: disabled 1: enabled
[13]	RW	ctrl	Line state ignore during TESTSE0 NAK 0: disabled 1: enabled
[12:10]	RW	val	TX-TX turnaround delay addition

[9]	RW	fetch	Instruction fetching from the periodic frame list, valid only in CONFIG1 mode 0: The controller fetches instructions from the periodic linked list only in micro-frame 0. 1: The controller fetches instructions from the periodic linked list in every micro-frame.
[8:1]	RW	offset	Available time offset
[0]	RO	brk_en	Interrupt memory transfer enable 0: disabled 1: enabled

INTNREG04

INTNREG04 is a debug register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_en	nak_reldfix_en	reserved	scaledwn_enum_time		hccparam_en	hcsparam_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	auto_en	Automatic feature enable 0: enabled. The suspend signal is valid when the run/stop bit is reset by software, but the hchalted bit is not set. 1: disabled. The port is not suspended when software clears the run/stop bit. The default value is 0.
[4]	RW	nak_reldfix_en	NAK reload enable 0: enabled 1: disabled
[3]	RO	reserved	Reserved

[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable 0: disabled 1: enabled
[1]	RW	hccparam_en	HCCPARAMS register write enable 0: disabled 1: enabled
[0]	RW	hcsparam_en	HCSPARAMS register write enable 0: disabled 1: enabled

INTNREG05

INTNREG05 is a UTMI Vendor control and status register. It is used to read or write to the UTMI PHY.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														vbusy		vport			vcontrol_loadm	reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	vbusy	The value 1 indicates that the hardware is writing data. This bit is cleared only when the process ends.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12]	RW	vcontrol_loadm	Load enable 0: enabled 1: disabled
[11:0]	RO	reserved	Reserved

INTNREG06

INTNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_capture	reserved																			hbusrt_err				num_beat_err				num_beat_ok			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	err_capture	AHB error
[30:12]	RO	reserved	Reserved
[11:9]	RO	hbusrt_err	hbrust value during a control transfer when an AHB error occurs
[8:4]	RO	num_beat_err	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00–0x10: valid 0x11–0x1F: reserved
[3:0]	RO	num_beat_ok	Number of completed beats during a burst transfer when an AHB error occurs

INTNREG07

INTNREG07 is an AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address during a control transfer when an AHB error occurs

12.9.5.2 USB Device Register Description

GOTGCTL

GOTGCTL is a device behavior control and status query register.

Offset Address	Register Name	Total Reset Value
0x0000	GOTGCTL	0x04C1_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chirpen	multvalidbc					reserved	otgver	bsesvld	asesvld	dbnctime	conidsts	reserved				devhnpen	hstsethnpen	hnpreq	hstnegscs	bvalidovval	bvalidoven	avalidovval	avalidoven	vbvalidovval	vbvalidoven	sesreq	sesreqscs
Reset	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	chirpen	Chirp on enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_BC_SUPPORT is 1. If OTG_BC_SUPPORT is not 1, this bit is reserved.
[26:22]	RO	multvalidbc	BC ACA input Bit[26]: rid_float Bit[25]: rid_gnd Bit[24]: rid_a Bit[23]: rid_b Bit[22]: rid_c
[21]	RO	reserved	Reserved
[20]	RW	otgver	Device version 0: Device version 1.3 1: Device version 2.0
[19]	RO	bsesvld	Transceiver status in device mode 0: B-session invalid 1: B-session valid
[18]	RO	asesvld	Transceiver status in host mode 0: A-session invalid 1: A-session valid

[17]	RO	dbnctime	Dejitter time 0: long dejitter time 1: short dejitter time
[16]	RO	conidsts	USB_ID status 0: 0: The device works in A-device mode. 1: The device works in B-device mode.
[15:12]	RO	reserved	Reserved
[11]	RW	devhnpen	Device HNP enable 0: disabled 1: enabled
[10]	RW	hstsethnpen	Host HNP enable 0: disabled 1: enabled
[9]	RW	hnpreq	HNP request 0: no 1: yes
[8]	RO	hstnegscs	Host negotiation indicator 0: Host negotiation fails. 1: Host negotiation is successful.
[7]	RW	bvalidovval	Bvalid setting 0: Bvalid = 0 1: Bvalid = 1 When GOTGCTL[bvalidoven] is 1, this bit is valid.
[6]	RW	bvalidoven	Bvalid signal overwrite enable 0: Bvalid can be overwritten. 1: Bvalid cannot be overwritten.
[5]	RW	avalidovval	Avalid setting 0: Avalid = 0 1: Avalid = 1 When GOTGCTL[avalidoven] is 1, this bit is valid.
[4]	RW	avalidoven	Avalid signal overwrite enable 0: Avalid can be overwritten. 1: Avalid cannot be overwritten.
[3]	RW	vbvalidovval	vbusvalid setting 0: vbusvalid = 0 1: vbusvalid = 1 When GOTGCTL[vbvalidoven] is 1, this bit is valid.

[2]	RW	vbvalidoven	vbusvalid signal overwrite enable. 0: vbusvalid can be overwritten. 1: vbusvalid cannot be overwritten.
[1]	RW	sesreq	Session request 0: no 1: yes
[0]	RO	sesreqscs	Session request status 0: failure 1: success

GOTGINT

GOTGINT is a device interrupt generation indicator/clear register.

Offset Address	Register Name	Total Reset Value
0x0004	GOTGINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											multvalipchng	dbncedone	adevtoutchg	hstnegdet	reserved							hstnegsucstschng	sesreqsucstschng	reserved						sesenddet	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RO	multvalipchng	An interrupt is generated when the value of at least one ACA pin changes. Setting this bit to 1 clears the interrupt. This bit is valid only when OTG_BC_SUPPORT is 1.
[19]	RO	dbncedone	An interrupt is generated when dejitter is successful. Setting this bit to 1 clears the interrupt. This bit is valid only when the HNP Capable or SRP Capable bit is set to 1.
[18]	RO	adevtoutchg	An interrupt is generated when waiting for the connection of device B times out. Setting this bit to 1 clears the interrupt.
[17]	RO	hstnegdet	An interrupt is generated when host negotiation is detected. Setting this bit to 1 clears the interrupt.
[16:10]	RO	reserved	Reserved

[9]	RO	hstnegsucstschng	An interrupt is generated when the host negotiation request fails or is successful. Setting this bit to 1 clears the interrupt.
[8]	RO	sesreqsucstschng	An interrupt is generated when the session request fails or is successful. Setting this bit to 1 clears the interrupt.
[7:3]	RO	reserved	Reserved
[2]	RO	sesenddet	An interrupt is generated when utmiotg_bvalid is deasserted. Setting this bit to 1 clears the interrupt.
[1:0]	RO	reserved	Reserved

GAHBCFG

GAHBCFG is an AHB configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	GAHBCFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3 2 1 0
Name	reserved		invdescendianness	ahbsingle	notialldmawrit	remmemsupp	reserved		nptxfemplvl	reserved	dmaen	hbstlen	glblintrmsk
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0 0 0 0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	invdescendianness	Descriptor byte invert 0: The descriptor byte sequence is similar to the AHB master byte sequence. 1: When the AHB master byte sequence is big endian, the descriptor byte sequence is little endian. When the AHB master byte sequence is little endian, the descriptor byte sequence is big endian.
[23]	RW	ahbsingle	Transfer in DMA mode 0: The remaining data is transmitted based on the INCR burst size. 1: The remaining data is transmitted based on the single burst size.
[22]	RW	notialldmawrit	DMA write operation notification. This bit is valid only when GAHBCFG[remmemsupp] is 1.

[21]	RW	remmemsupp	Remote memory support 0: int_dma_req and int_dma_done are not set to **1**, and the controller core handles the XferComp interrupt immediately after the DMA write operation is complete. 1: int_dma_req is set to **1** when the HSOTG DMA starts writing data to an external memory; int_dma_done is set to **1** when the transfer of the controller core is complete, indicating that the HSOTG write operation is complete. In this case, the controller core waits until the system sys_dma_done signal becomes valid, and then starts the next DMA transfer.
[20:8]	RO	reserved	Reserved
[7]	RW	nptxfemplvl	Empty status level of the non-periodic TX FIFO 0: The TxFEmp interrupt indicates that the TX FIFO at the IN endpoint is half empty. 1: The TxFEmp interrupt indicates that the TX FIFO at the IN endpoint is empty.
[6]	RO	reserved	Reserved
[5]	RW	dmaen	DMA mode enable 0: The core works in slave mode. 1: The core works in DMA mode.
[4:1]	RW	hbstlen	Burst length/type for both the external and internal DMA modes In external DMA mode: 0x0: 1 word 0x1: 4 words 0x2: 8 words 0x3: 16 words 0x4: 32 words 0x5: 64 words 0x6: 128 words 0x7: 256 words Other values: reserved In internal DMA mode: 0x0: Single 0x1: INCR 0x3: INCR4 0x5: INCR8 0x7: INCR16 Other values: reserved
[0]	RW	glblintrmsk	Global interrupt mask 0: masked 1: not masked

GUSBCFG

GUSBCFG is a USB configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	GUSBCFG	0x0000_1400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	corrupttxpkt	forcedevmode	forcehstmode	txenddelay	usbtrafctl	ic_usbcap	ulpi	indicator	complement	termseldlpulse	ulpiextvbusindicator	ulpiextvbusdrv	ulpiclksusm	ulpiautores	ulpifsls	otgi2csel	phylpwrclksel	reserved	usbtrdtim				hnpcap	srpcap	ddrsel	physel	fsintf	ulpi_utmi_sel	phyif	toutcal		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WO	corrupttxpkt	Unexpected TX packet This bit is for debugging only and is always set to 0.
[30]	RW	forcedevmode	Forcible device mode 0: normal mode 1: forcible device mode
[29]	RW	forcehstmode	Forcible host mode 0: normal mode 1: forcible host mode
[28]	RW	txenddelay	TX end delay enable 0: disabled 1: enabled
[27]	RW	usbtrafctl	USB pull-up/pull-down resistor control (traffic signaling) 0: Pull-up and pull-down resistors are attached. 1: Pull-up and pull-down resistors are detached. **NOTE** This bit is valid only when OTG_ENABLE_IC_USB and USBCFG [ic_usbcap] are 1.
[26]	RO	ic_usbcap	IC_USB enable 0: The IC_USB PHY interface is not selected. 1: The IC_USB PHY interface is selected.
[25]	RW	ulpi	ULPI interface protection enable 0: enabled 1: disabled

[24]	RW	indicator	Indicator pass through 0: The complementary output signal is determined by the vbusvalid comparator. 1: The complementary output signal is not determined by the vbusvalid comparator. When TG_HSPHY_INTERFACE is 1, this bit is read-only. When TG_HSPHY_INTERFACE is 0, this bit is reserved.
[23]	RW	complement	Indicator complement 0: The PHY does not invert the ExternalVbusIndicator signal. 1: The PHY inverts the ExternalVbusIndicator signal.
[22]	RW	termseldlpulse	SRP line pulse drive 0: utmi_txvalid drives the line pulse. 1: utmi_termsel drives the line pulse.
[21]	RW	ulpiextvbusindicator	ULPI external VBUS over-current indicator 0: The PHY uses the internal vbusvalid comparator. 1: The PHY uses the external vbusvalid comparator. This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[20]	RW	ulpiextvbusdrv	ULPI external VBUS drive 0: The PHY uses the internal charge pump to drive VBUS. 1: The PHY uses the external power supply to drive VBUS. **NOTE** This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[19]	RW	ulpiclksusm	ULPI clock suspend 0: The PHY disables the internal clock in suspend mode. 1: The PHY does not disable the internal clock in suspend mode. This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[18]	RW	ulpiautores	ULPI automatic restore 0: The PHY does not use the automatic restore feature. 1: The PHY uses the automatic restore feature. **NOTE** This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[17]	RW	ulpifsls	ULPI FS/LS select 0: ULPI interface 1: ULPI FS/LS serial interface **NOTE** Set GUSBCFG[ulpi_utmi_sel] to 1 before setting this bit.

[16]	RW	otgi2csel	UTMI or I^{2}C interface select 0: UTMI USB 1.1 full-speed interface 1: I^{2}C interface **NOTE** This bit is valid only when OTG_I2C_INTERFACE is 2. Reading this bit returns 0.
[15]	RW	phylpwrclksel	PHY low-power clock select 0: internal 480 MHz PLL clock 1: external 48 MHz clock
[14]	RO	reserved	Reserved
[13:10]	RW	usbtrdtim	USB turnaround time 0101: This field is set to this value when the MAC interface is a 16-bit UTMI+ interface. 1001: This field is set to this value when the MAC interface is an 8-bit UTMI+ interface. Other values: reserved
[9]	RW	hnpcap	HNP enable 0: disabled 1: enabled
[8]	RW	srpcap	SRP enable 0: disabled 1: enabled
[7]	RW	ddrsel	ULPI DDR select 0: single-rate ULPI interface 1: double-rate ULPI interface This bit is valid only when OTG_HSPHY_INTERFACE is 2 or 3.
[6]	RW	physel	USB 2.0 high-speed PHY or USB 1.1 full-speed serial transceiver 0: USB 2.0 high-speed UTMI+ or ULPI PHY interface 1: USB 1.1 full-speed serial transceiver If the USB 1.1 full-speed serial transceiver is not selected, this bit is always 0 and read-only. If the USB 2.0 high-speed PHY is not selected, this bit is always 1 and read-only. If the preceding interface types are not selected (non-zero value), this bit is used to select the interface to be activated, and this bit can be read or written.

[5]	RW	fsintf	Full-speed serial interface select 0: 6-pin unidirectional full-speed serial interface 1: 3-pin bidirectional full-speed serial interface If the USB 1.1 full-speed serial transceiver is not selected, this bit is always 0 and write-only. If the USB 1.1 full-speed interface is selected, this bit can be used to select the 3-pin or 6-pin interface and can be read or written.
[4]	RW	ulpi_utmi_sel	ULPI or UTMI select 0: UTMI+ interface 1: ULPI interface
[3]	RW	phyif	PHY interface 0: 8 bits 1: 16 bits
[2:0]	RW	toutcal	HS/FS timeout calibration High-speed operations: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

GRSTCTL

GRSTCTL is a reset hardware feature register.

Offset Address	Register Name	Total Reset Value
0x0010	GRSTCTL	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahbidle	dmareq	reserved																		txfnum						txfflsh	rxfflsh	intknqflsh		frmcntrrst	reserved	csftrst
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ahbidle	Whether the AHB master state machine is idle 0: no 1: yes

[30]	RO	dmareq	DMA request signal, indicating that the DMA request is being processed. This bit is only for debugging. 0: other cases 1: The DMA request is being processed.
[29:11]	RO	reserved	Reserved
[10:6]	RW	txfnum	TX FIFO ID, which must be updated by using the TX FIFO flush bit. This field cannot be overwritten before the controller core clears the TX FIFO flush bit. 0x0: In host mode, non-periodic TX FIFOs are flushed. During shared FIFO operations, non-periodic TX FIFOs are flushed in device mode. In dedicated FIFO mode, TX FIFO 0 is flushed in device mode. 0x1: In host mode, periodic TX FIFOs are flushed. During shared FIFO operations, periodic TX FIFO 1 is flushed in device mode. In dedicated FIFO mode, TX FIFO 1 is flushed in device mode. 0x2: During shared FIFO operations, periodic TX FIFO 2 is flushed in device mode. In dedicated FIFO mode, TX FIFO 2 is flushed in device mode. 0xF: During shared FIFO operations, periodic TX FIFO 15 is flushed in device mode. In dedicated FIFO mode, TX FIFO 15 is flushed in device mode. 0x10: All TX FIFOs are flushed in device or host mode.
[5]	R_WS_SC	txfflsh	TX FIFO flush This bit can be used to refresh one or all TX FIFOs but FIFOs cannot be refreshed during transactions. This bit can be written only after the application program confirms that the controller core does not read or write to the TX FIFO. It takes eight clock cycles to clear this bit, during which the application program must wait. 0: not flushed 1: flushed
[4]	RO	rxfflsh	RX FIFO flush. However, FIFOs cannot be refreshed during transactions. This bit can be written only after the application program confirms that the controller core does not read or write to the RX FIFO. It takes eight clock cycles to clear this bit, during which the application program must wait. 0: not flushed 1: flushed

[3]	R_WS_SC	intknqflsh	In token sequence learning queue flush This bit is valid only when OTG_EN_DED_TX_FIFO is 0. 0: not flushed 1: flushed
[2]	RO	frmcntrrst	Host frame counter reset This bit is used to reset the frame number counter. When the frame number counter is reset, the ID of next transmitted SOF micro-frames is 0. 0: not reset 1: reset
[1]	RO	reserved	Reserved
[0]	RW	csftrst	Core soft interrupt • All interrupts and the CSR register excluding the following bits are cleared: – PCGCCTL[rstpdwnmodule] – PCGCCTL[gatehclk] – PCGCCTL[pwrclmp] – PCGCCTL[stoppphylpwrclkselclk] – GUSBCFG[phylpwrclksel] – GUSBCFG[ddrsel] – GUSBCFG[physel] – GUSBCFG[fsintf] – GUSBCFG[ulpi_utmi_sel] – GUSBCFG[phyif] – GUSBCFG[txenddelay] – GUSBCFG[termseldlpulse] – GUSBCFG[ulpiclksusm] – GUSBCFG[ulpiautores] – GUSBCFG[ulpifsls] – GGPIO – GPWRDN – GADPCTL – HCFG[fslspclksel] – DCFG[devspd] – DCTL[sftdiscon] • All module state machines are reset to the idle status, and all TX FIFOs and RX FIFOs are refreshed. • All transactions on the AHB master are interrupted as soon as possible, and all USB transactions are immediately interrupted. • When the hibernation or ADP feature is enabled, the PMU module is not soft-reset by the core.

GINTSTS

GINTSTS is a system interrupt register.

Offset Address	Register Name	Total Reset Value
0x0014	GINTSTS	0x0800_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupint	sessreqint	disconnint	conidstschng	lpm_int	ptxfemp	hchint	prtint	resetdet	fetsusp	incomplpincompisoout	incompisoin	oepint	iepint	epmis	rstrdoneint	eopf	isooutdrop	enumdone	usbrst	usbsusp	erlysusp	i2cint	ulpickinti2cckint	goutnakeff	ginnakeff	nptxfemp	rxflvl	sof	otgint	modemis	curmod
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	wkupint	Suspend/Resume detection interrupt. Setting this bit to 1 clears the interrupt.
[30]	RWSC	sessreqint	In host mode, an interrupt is generated when a device session request is detected. In device mode, an interrupt is generated when utmisrp_bvalid is 1. Setting this bit to 1 clears the interrupt.
[29]	RWSC	disconnint	An interrupt is generated when the system detects that the device is disconnected. Setting this bit to 1 clears the interrupt.
[28]	RWSC	conidstschng	An interrupt is generated when the slot ID changes. Setting this bit to 1 clears the interrupt.
[27]	RWSC	lpm_int	In device mode, an interrupt is generated when the device receives an LPM transaction and transmits a response indicating no errors. In host mode, an interrupt is generated when the device receives an LPM transaction and transmits a response indicating no errors, or when the host core completes the preset LPM transactions. **NOTE** This bit is valid only when LPMCapable or OTG_ENABLE_LPM is 1. Setting this bit to 1 clears the interrupt.
[26]	RO	ptxfemp	An interrupt is generated when the periodic TX FIFO is empty or half empty.
[25]	RO	hchint	In host mode, an interrupt is generated in a core channel. This bit is cleared by clearing the corresponding status bit.

[24]	RO	prtint	In host mode, an interrupt is generated when the status of a port of the DWC_otg core changes. **NOTE** This bit is cleared by clearing the corresponding bit in the host port control and status register.
[23]	RWSC	resetdet	In device mode, an interrupt is generated when the device is suspended and the system detects that the USB module is reset in power-down module. In host mode, this interrupt is not generated. **NOTE** Setting this bit to 1 clears the interrupt.
[22]	RWSC	fetsusp	This interrupt is valid only in DMA mode. This interrupt indicates that the core stops obtaining data from IN endpoints.
[21]	RWSC	incomplpincompisoout	In host mode, an interrupt is generated if there are pending transactions. In device mode, an interrupt is generated when there are isochronous OUT transfers to be completed. **NOTE** Setting this bit to 1 clears the interrupt.
[20]	RWSC	incompisoin	An interrupt is generated when there are isochronous IN transfers to be completed. In scatter/gather DMA mode, this interrupt is not generated. **NOTE** Setting this bit to 1 clears the interrupt.
[19]	RO	oepint	In device mode, an interrupt is generated on an OUT endpoint. This interrupt is cleared by clearing the corresponding status bit in the DOEPINT*n* register.
[18]	RO	iepint	In device mode, an interrupt is generated on an IN endpoint. This interrupt is cleared by clearing the corresponding status bit in the DOEPINT*n* register.
[17]	RO	epmis	An interrupt is generated when endpoints mismatch. This bit is valid only during shared FIFO operations. **NOTE** Setting this bit to 1 clears the interrupt.
[16]	RWSC	rstrdoneint	An interrupt is caused by the restore command after hibernation. **NOTE** This bit is valid only when the hibernation function is enabled.
[15]	RWSC	eopf	Periodic frame end interrupt Setting this bit to 1 clears the interrupt.

[14]	RWSC	isooutdrop	Isochronous OUT packet drop interrupt NOTE Setting this bit to 1 clears the interrupt.
[13]	RWSC	enumdone	Speed enumeration completion interrupt NOTE Setting this bit to 1 clears the interrupt.
[12]	RWSC	usbrst	USB reset detection interrupt NOTE Setting this bit to 1 clears the interrupt.
[11]	RWSC	usbsusp	USB suspend detection interrupt NOTE Setting this bit to 1 clears the interrupt.
[10]	RWSC	erlysusp	USB idle 3 ms detection interrupt NOTE Setting this bit to 1 clears the interrupt.
[9]	RWSC	i2cint	An interrupt is generated when I^2C access through the I^2C interface is complete. This bit is enabled only when OTG_I2C_INTERFACE is 1. NOTE Setting this bit to 1 clears the interrupt.
[8]	RWSC	ulpickinti2cckint	When the ULPI Carkit interrupt is generated, the core sets the interrupt bit to 1. This bit is valid only when OTG_ULPI_CARKIT is 1; otherwise, reading this bit returns 0. When the I^2C Carkit interrupt is generated, the core sets the interrupt bit to 1. This bit is valid only when OTG_I2C_INTERFACE is 1; otherwise, reading this bit returns 0. NOTE Setting this bit to 1 clears the interrupt.
[7]	RO	goutnakeff	The global OUT NAK bit in the device control register is set. This interrupt is cleared by clearing the global OUT NAK bit.
[6]	RO	ginnakeff	An interrupt is generated when the global non-periodic IN NAK is set in the device control register.
[5]	RO	nptxfemp	An interrupt is generated when the non-periodic TX FIFO is empty or half empty.
[4]	RO	rxflvl	There is at least a pending packet to be read by the RX FIFO.

[3]	RWSC	sof	In host mode, an SOF, micro-SOF, or keep-active is being transmitted. In device mode, an SOF token is received by the USB module.
[2]	RO	otgint	An OTG even is in progress. This interrupt is cleared by clearing the corresponding bit in the GOTGINT register.
[1]	RWSC	modemis	Mode mismatch interrupt When the core works in device mode, a register in host mode needs to be accessed. When the core works in host mode, a register in device mode needs to be accessed. 0: invalid 1: valid **NOTE** Setting this bit to **1** clears the interrupt.
[0]	RO	curmod	Current operating mode 0: device mode 1: host mode

GINTMSK

GINTMSK is a system interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0018	GINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupintmsk	sessreqintmsk	disconnintmsk	conidstschngmsk	lpm_intmsk	ptxfempmsk	hchintmsk	prtintmsk	resetdetmsk	fetsuspmsk	incomplpmskincompisooutmsk	incompisoinmsk	oepintmsk	iepintmsk	epmismsk	rstrdoneintmsk	eopfmsk	isooutdropmsk	enumdonemsk	usbrstmsk	usbsuspmsk	erlysuspmsk	i2cintmsk	ulpickintmsk	goutnakeffmsk	ginnakeffmsk	nptxfempmsk	rxflvlmsk	sofmsk	otgintmsk	modemismsk	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wkupintmsk	Resume/Remote wakeup detection interrupt mask 0: masked 1: not masked

[30]	RW	sessreqintmsk	Session request/new session detection interrupt mask 0: masked 1: not masked
[29]	RW	disconnintmsk	Disconnect detection interrupt mask 0: masked 1: not masked
[28]	RW	conidstschngmsk	Connector ID status change interrupt mask 0: masked 1: not masked
[27]	RW	lpm_intmsk	LPM transaction RX interrupt mask 0: masked 1: not masked
[26]	RW	ptxfempmsk	Periodic TX FIFO empty interrupt mask 0: masked 1: not masked
[25]	RW	hchintmsk	Host channel interrupt mask 0: masked 1: not masked
[24]	RW	prtintmsk	Host port interrupt mask 0: masked 1: not masked
[23]	RW	resetdetmsk	Reset detection interrupt mask 0: masked 1: not masked
[22]	RW	fetsuspmsk	Data fetch suspended interrupt mask 0: masked 1: not masked
[21]	RW	incomplpmskincompisooutmsk	Incomplete periodic transfer interrupt mask 0: masked 1: not masked Incomplete isochronous OUT transfer interrupt mask 0: masked 1: not masked
[20]	RW	incompisoinmsk	Incomplete isochronous in transfer interrupt mask 0: masked 1: not masked This bit can be enabled only when periodic endpoints are enabled in dedicated TX FIFO mode.

[19]	RW	oepintmsk	OUT endpoint interrupt mask 0: masked 1: not masked
[18]	RW	iepintmsk	IN endpoint interrupt mask 0: masked 1: not masked
[17]	RW	epmismsk	Endpoint mismatch interrupt mask 0: masked 1: not masked
[16]	RW	rstrdoneintmsk	Restore done interrupt mask 0: masked 1: not masked This bit is valid only when the hibernation function is enabled (OTG_EN_PWROPT = 2).
[15]	RW	eopfmsk	End of periodic frame interrupt mask 0: masked 1: not masked
[14]	RW	isooutdropmsk	Device only isochronous OUT packet drop interrupt mask 0: masked 1: not masked
[13]	RW	enumdonemsk	Enumeration done interrupt mask 0: masked 1: not masked
[12]	RW	usbrstmsk	USB reset interrupt mask 0: masked 1: not masked
[11]	RW	usbsuspmsk	USB suspend interrupt mask 0: masked 1: not masked
[10]	RW	erlysuspmsk	Early suspend interrupt mask 0: masked 1: not masked
[9]	RW	i2cintmsk	I^2C interrupt mask 0: masked 1: not masked

[8]	RW	ulpickintmsk	ULPI Carkit interrupt mask 0: masked 1: not masked I^2C Carkit interrupt mask 0: masked 1: not masked
[7]	RW	goutnakeffmsk	Global OUT NAK effective interrupt mask 0: masked 1: not masked
[6]	RW	ginnakeffmsk	Global non-periodic IN NAK effective interrupt mask 0: masked 1: not masked
[5]	RW	nptxfempmsk	Non-periodic TX FIFO empty interrupt mask 0: masked 1: not masked
[4]	RW	rxflvlmsk	RX FIFO non-empty interrupt mask 0: masked 1: not masked
[3]	RW	sofmsk	Start of (micro) frame interrupt mask 0: masked 1: not masked
[2]	RW	otgintmsk	Device interrupt mask 0: masked 1: not masked
[1]	RW	modemismsk	Mode mismatch interrupt mask 0: masked 1: not masked
[0]	RO	reserved	Reserved

GRXSTSR

GRXSTSR is an RX status debugging read register.

Offset Address	Register Name	Total Reset Value
0x001C	GRXSTSR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_devicemode								fn_devicemode				pktsts_devicemode				dpid_devicemode				bcnt_devicemode								chnum_devicemode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved_devicemode	Reserved
[24:21]	RO	fn_devicemode	Number of frames
[20:17]	RO	pktsts_devicemode	Data packet status 0001: global OUT NAK (interrupt triggered) 0010: IN data packet received 0011: IN transfer completion (interrupt triggered) 0101: data toggle error (interrupt triggered) 0111: channel stop (interrupt triggered) Other values: reserved
[16:15]	RO	dpid_devicemode	Data PID of the received packet 00: DATA0 10: DATA1 01: DATA2 11: MDATA
[14:4]	RO	bcnt_devicemode	Byte size of the received IN data packets
[3:0]	RO	chnum_devicemode	Number of channels from which the current data packets are received

GRXSTSP

GRXSTSP is an RX status read&pop register.

Offset Address	Register Name	Total Reset Value
0x0020	GRXSTSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved_devicemode								fn_devicemode				pktsts_devicemode				dpid_devicemode				bcnt_devicemode								chnum_devicemode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved_devicemode	Reserved
[24:21]	RO	fn_devicemode	Number of frames
[20:17]	RO	pktsts_devicemode	Data packet status x01: global OUT NAK (interrupt triggered) x02: IN data packet received x03: IN transfer completion (interrupt triggered) x04: data toggle error (interrupt triggered) x07: channel stop (interrupt triggered) Other values: reserved
[16:15]	RO	dpid_devicemode	Data PID of the received packet 00: DATA0 10: DATA1 01: DATA2 11: MDATA
[14:4]	RO	bcnt_devicemode	Byte size of the received IN data packets
[3:0]	RO	chnum_devicemode	Number of channels from which the current data packets are received

GRXFSIZ

GRXFSIZ is an RX FIFO size configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	GRXFSIZ	0x0000_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rxfdep															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rxfdep	RX FIFO depth. Its value range is 16−32768.

GNPTXFSIZ

GNPTXFSIZ is a non-periodic TX FIFO size configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	GNPTXFSIZ	0x0100_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ineptxf0dep																ineptxf0staddr															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	ineptxf0dep	Depth of IN endpoint TX FIFO 0. Its value range is 16−32768.
[15:0]	RW	ineptxf0staddr	Start address for the TX RAM of IN endpoint FIFO 0

GNPTXSTS

GNPTXSTS is a non-periodic TX FIFO and non-periodic TX request query register.

Offset Address	Register Name	Total Reset Value
0x002C	GNPTXSTS	0x0008_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	nptxqtop							nptxqspcavail								nptxfspcavail															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:24]	RO	nptxqtop	Non-periodic TX request queue top Bit[30:27]: number of channels or endpoints bit[26:25]: 00: IN/OUT token 01: zero-length transmit packet (device IN/host OUT) 10: PING/CSPLIT token 11: channel stop command Bit[24]: stop (the selected channel or endpoint is used for attempting)
[23:16]	RO	nptxqspcavail	Available space for the non-periodic TX request queue 0x0: The non-periodic TX request queue is full. 0x1: One address is available. 0x2: Two addresses are available. 0xn: *n* addresses ($0 \le n \le 8$) are available. Other values: reserved
[15:0]	RO	nptxfspcavail	Total available space for the non-periodic TX request queue 0x0: The non-periodic TX FIFO is full. 0x1: One word is available. 0x2: Two words are available. 0xn: *n* words ($0 \le n \le 32768$) are available. 0x8000: 32768 words are available. Other values: reserved

GI2CCTL

GI2CCTL is an I^{2}C access register.

Offset Address	Register Name	Total Reset Value
0x0030	GI2CCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bsydne	rw	reserved	i2cdatse0	i2cdevadr		i2csuspctl	ack	i2cen	addr							regaddr								rwdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	bsydne	I^{2}C busy/done 0: done 1: busy

[30]	RW	rw	Read/Write indicator 0: write 1: read
[29]	RW	reserved	Reserved
[28]	RW	i2cdatse0	USB mode of the FS interface 0: VP_VM USB mode 1: DAT_SE0 USB mode
[27:26]	RW	i2cdevadr	I^2C device address 00: 7'h2C 01: 7'h2D 10: 7'h2E 11: 7'h2F
[25]	RW	i2csuspctl	I^2C suspend control 0: utmi_suspend_n is used. 1: The suspend bit in the PHY register is edited by using the I^2C write function.
[24]	RO	ack	I^2C ACK 0: NAK 1: ACK
[23]	RW	i2cen	I^2C transaction enable 0: disabled 1: enabled
[22:16]	RW	addr	I^2C slave address
[15:8]	RW	regaddr	I^2C register address
[7:0]	RW	rwdata	I^2C read//write data

GPVNDCTL

GPVNDCTL is a PHY vendor control register.

Offset Address	Register Name	Total Reset Value
0x0034	GPVNDCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disulpidrvr	reserved			vstsdone	vstsbsy	newregreq	reserved	regwr	regaddr							vctrlextregaddr								regdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	disulpidrvr	ULPI interface enable 0: enabled 1: disabled **NOTE** This bit is valid only when OTG_ULPI_CARKIT is 1. Otherwise, reading this bit returns 0.
[30:28]	RO	reserved	Reserved
[27]	RWSC	vstsdone	Vendor control access (done) 0: The new register request is set. 1: Vendor control access ends.
[26]	RO	vstsbsy	Vendor control access (busy) 0: Vendor control access ends. 1: Vendor control access is in progress.
[25]	RWSC	newregreq	New vendor control access 0: no access request 1: new vendor control access request
[24:23]	RO	reserved	Reserved
[22]	RW	regwr	Register read/write 0: read 1: write
[21:16]	RW	regaddr	Register access address
[15:8]	RW	vctrlextregaddr	Address for the UTMI+ vendor control register bit[15:12]: 4-bit parallel output bus addressing bit[11:8]: utmi_vcontrol[3:0]
[7:0]	RW	regdata	Register data This bit is valid after the Vstatus Done bit is set.

GGPIO

GGPIO is a GPIO register.

Offset Address	Register Name	Total Reset Value
0x0038	GGPIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gpo																gpi															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	gpo	General-purpose output, which is driven by gp_o[15:0] of the core
[15:0]	RW	gpi	General-purpose input, which reflects gp_i[15:0] of the core

GUID

GUID is a user ID register.

Offset Address	Register Name	Total Reset Value
0x003C	GUID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userid																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	userid	User ID

GSNPSID

GSNPSID is a Synopsys ID query register.

Offset Address	Register Name	Total Reset Value
0x0040	GSNPSID	0x4F54_300A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	synopsysid																															
Reset	0	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:0]	RW	synopsysid	ID of the current DWC_otg core

GHWCFG1

GHWCFG1 is user hardware configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0044	GHWCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epdir																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	epdir	Endpoint direction The endpoint direction is expressed by two bits. Endpoint bit[31:30]: direction of endpoint 15 bit[29:28]: direction of endpoint 14 ... bit[3:2]: direction of endpoint 1 bit[1:0]: direction of endpoint 0 (always bidirectional) Direction 00: bidirectional (IN and OUT) endpoint 01: IN endpoint 10: OUT endpoint 11: reserved

GHWCFG2

GHWCFG2 is user hardware configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0048	GHWCFG2	0x2284_C850

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	otg_enable_ic_usb	tknqdepth					ptxqdepth		nptxqdepth		reserved	multiprocintrpt	dynfifosizing	periosupport	numhstchnl		numdeveps				fsphytype		hsphytype		singpnt	otgarch	otgmode					
Reset	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RO	otg_enable_ic_usb	IC_USB select enable 0: disabled 1: enabled
[30:26]	RO	tknqdepth	Depth of the IN token sequence learning queue in device mode The value range is 0−30.
[25:24]	RO	ptxqdepth	Depth of the periodic request queue in host mode 00: 2 01: 4 10: 8 11: 16
[23:22]	RO	nptxqdepth	Depth of the non-periodic request queue 00: 2 01: 4 10: 8 Other values: reserved
[21]	RO	reserved	Reserved
[20]	RW	multiprocintrpt	Multi-processor interrupt enable 0: disabled 1: enabled
[19]	RO	dynfifosizing	FIFO size dynamic change enable 0: disabled 1: enabled
[18]	RO	periosupport	Periodic OUT channel support in host mode 0: not supported 1: supported

[17:14]	RO	numhstchnl	Number of host channels 0–15: The value 0 indicates one channel, and the value 15 indicates 16 channels.
[13:10]	RO	numdeveps	Number of device endpoints (excluding endpoint 0) The value range is 1−15.
[9:8]	RO	fsphytype	Type of the full-speed PHY interface 00: The full-speed interface is not supported. 01: The full-speed interface is supported. 10: FS pins share with UTMI+ pins. 11: FS pins share with ULPI pins.
[7:6]	RO	hsphytype	Type of the high-speed PHY interface 00: high-speed interface not supported 01: UTMI+ 10: ULPI 11: UTMI+ and ULPI
[5]	RO	singpnt	Point-to-point 0: multi-point application (hub and split supported) 1: single-point application (hub and split not supported)
[4:3]	RO	otgarch	Device architecture 00: slave only 01: external DMA 10: internal DMA Other values: reserved
[2:0]	RO	otgmode	Operating mode 000: HNP- and SRP-capable OTG (host & device) 001: SRP-capable OTG (host & device) 010: non-HNP and non-SRP capable OTG (host & device) 011: SRP-capable device 100: non-OTG device 101: SRP-Capable host 110: non-OTG host Other values: reserved

GHWCFG3

GHWCFG3 is user hardware configuration register 3.

Offset Address	Register Name	Total Reset Value
0x004C	GHWCFG3	0x0501_54E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfifodepth																lpmmode	bcsupport	hsicmode	adpsupport	rsttype	optfeature	vndctlsupt	i2cintsel	otgen	pktsizewidth			xfersizewidth			
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dfifodepth	DFIFO depth. The value range is 32–32768.
[15]	RO	lpmmode	LPM working mode (configurable)
[14]	RO	bcsupport	Whether the HS device controller supports the battery charger 0: not supported 1: supported
[13]	RO	hsicmode	HSIC mode select 0: The HSIC-capable shares with the UTMI PHY interface 1: The HSIC mode is not selected.
[12]	RO	adpsupport	Whether the device controller has an ADP logic 0: no 1: yes
[11]	RO	rsttype	Reset mode of clock always blocks 0: asynchronous reset 1: synchronous reset
[10]	RO	optfeature	Feature removal Features include the user ID register, GPIO interface ports, and SOF toggle and counter ports. 0: not removed 1: removed
[9]	RO	vndctlsupt	Vendor control interface support 0: not supported 1: supported
[8]	RO	i2cintsel	I^2C interface select 0: not selected 1: selected

[7]	RO	otgen	Device function enable 0: disabled 1: enabled
[6:4]	RO	pktsizewidth	Data packet width 000: 4 bits 001: 5 bits 010: 6 bits 011: 7 bits 100: 8 bits 101: 9 bits 110: 10 bits Other values: reserved
[3:0]	RO	xfersizewidth	Transfer width 0000: 11 bits 0001: 12 bits 1000: 19 bits Other values: reserved

GHWCFG4

GHWCFG4 is user hardware configuration register 4.

Offset Address	Register Name	Total Reset Value
0x0050	GHWCFG4	0x4600_8020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	descdma	descdmaen	ineps				dedfifomode	sessendfltr	bvalidfltr	avalidfltr	vbusvalidfltr	iddgfltr	numctleps				phydatawidth			reserved					extndedhibernation	hibernation	ahbfreq	partialpwrdn	numdevperioeps			
Reset	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	descdma	Scatter/Gather DMA 0: no dynamic configuration 1: dynamic configuration
[30]	RO	descdmaen	PAD slew rate 0: fast 1: slow

[29:26]	RO	ineps	Number of IN endpoints in device mode 0: one IN endpoint 1: two IN endpoints ... 15: 16 IN endpoints
[25]	RO	dedfifomode	Dedicated TX FIFO enable for device IN endpoints 0: disabled 1: enabled
[24]	RO	sessendfltr	session_end filter enable 0: disabled 1: enabled
[23]	RO	bvalidfltr	b_valid filter enable 0: disabled 1: enabled
[22]	RO	avalidfltr	a_valid filter enable 0: disabled 1: enabled
[21]	RO	vbusvalidfltr	VBUS valid filter enable 0: disabled 1: enabled
[20]	RO	iddgfltr	IDDIG filter enable 0: disabled 1: enabled
[19:16]	RO	numctleps	Number of controlled endpoints excluding endpoint 0 in device mode The value range is 0−15.
[15:14]	RO	phydatawidth	Data width of the UTMI+ PHY/ULPI-to-internal UTMI+ wrapper 00: 8 bits 01: 16 bits 10: 8 bit or 16 bits, which is configured by using software Other values: reserved
[13:8]	RO	reserved	Reserved
[7]	RO	extndedhibernation	Extended hibernation enable 0: disabled 1: enabled

[6]	RO	hibernation	Hibernation enable 0: disabled 1: enabled
[5]	RO	ahbfreq	Whether the minimum AHB frequency is lower than 60 MHz 0: no 1: yes
[4]	RO	partialpwrdn	Partial power down enable 0: disabled 1: enabled
[3:0]	RO	numdevperioeps	Number of periodic IN endpoints in device mode The value range is 0−15.

GLPMCFG

GLPMCFG is an LPM configuration register.

Offset Address	Register Name	Total Reset Value
0x0054	GLPMCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	invselhsic	hsiccon	rstrslpsts	enbesl	lpm_retrycnt_sts			sndlpm	lpm_retry_cnt				lpm_chnl_indx				l1resumeok	slpsts	corel1res		hird_thres				enbslpm	bremotewake	hird				appl1res	lpmcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	invselhsic	HSIC select (by using HSIC-invert) enable If if_sel_hsic is 1: InvSelHsic = 1: disabled InvSelHsic = 0: enabled If if_sel_hsic is 0: InvSelHsic = 1: enabled InvSelHsic = 0: disabled

[30]	RW	hsiccon	HSIC-connect Host mode: When this bit is set to 1, the bus HSIC is driven to idle status and waits for the HSIC connect sequence transmitted from the device. Device mode: When this bit is set to 1, the device waits for the HSIC idle line state on the bus. The HSIC connection starts after the idle line state occurs. **NOTE** This bit is valid only when OTG_ENABLE_HSIC is 1; otherwise, reading this bit returns 0.
[29]	RW	rstrslpsts	Restore SlpSts 0: The core enters the shallow sleep mode. 1: The core enters the deep sleep mode.
[28]	RW	enbesl	Best effort service latency (BESL) enable 0: disabled 1: enabled
[27:25]	RO	lpm_retrycnt_sts	LPM retry count This field is used to count the remaining retries.
[24]	RWSC	sndlpm	LPM transaction TX
[23:21]	RW	lpm_retry_cnt	LPM retry count statistics When a device provides error information, this field shows the extra LPM retries of the host before the device validity signal arrives.
[20:17]	RW	lpm_chnl_indx	LPM channel index The number of LPM transaction channels is provided. The core automatically calculates the device address and number of endpoints based on the LPM channel index.
[16]	RO	l1resumeok	Resume from the sleep state 0: resumed 1: not resumed
[15]	RO	slpsts	Port sleep state 0: resume 1: sleep

[14:13]	RO	corel1res	LPM response In device mode, this field reflects the response to the LPM transaction. In host mode, this field indicates the handshake response from the device during LPM transaction. 11: ACK 10: NYET 01: STALL 00: error (no handshake response)
[12:8]	RW	hird_thres	BESL or HIRD threshold
[7]	RW	enblslpm	utmi_sleep_n enable 0: disabled 1: enabled
[6]	RW	bremotewake	Remote wake enable In host mode, the enable signal is transmitted from the wIndex field of the LPM transaction. In device mode (read-only), when the ACK, NYET, or STALL response is transmitted to the LPM transaction, this bit is updated together with the received LPM token, bRemoteWake, and bmAttribute.
[5:2]	RW	hird	When EnBESL is 0: Host-initiated resume period In host mode, this field is assigned by the LPM transaction. In device mode, this field is updated by LPM token HIRD bmAttribute. Sl. No HIRD[3:0] THIRD (µs) 1 4'b0000 50 2 4'b0001 125 3 4'b0010 200 4 4'b0011 275 5 4'b0100 350 6 4'b0101 425 7 4'b0110 500 8 4'b0111 575 9 4'b1000 650 10 4'b1001 725 11 4'b1010 800 12 4'b1011 875 13 4'b1100 950 14 4'b1101 1025 15 4'b1110 1100

			16 4'b1111 1175 When EnBESL is 1: BESL In host mode, the BESL value is transmitted to the LPM transaction In device mode, this field is updated by LPM token BESL bmAttribute.
[1]	RW	appl1res	LPM response 0: NYET 1: ACK
[0]	RW	lpmcap	LPM enable 0: disabled 1: enabled

GPWRDN

GPWRDN is a power down register.

Offset Address	Register Name	Total Reset Value
0x0058	GPWRDN	0x1320_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				multvalidbc				adpint	bsessvld	iddig	linestate	stschngintmsk	stschngint	srpdetectmsk	srpdetect	conndetmsk	connectdet	disconnectdetectmsk	disconnectdetect	resetdetmsk	resetdetected	linestatechangemsk	Instschng	disablevbus	pwrdnswtch	pwrdnrst_n	pwrdnclmp	restore	pmuactv	pmuintsel
Reset	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	multvalidbc	BC ACA input Bit 28 - rid_float Bit 27 - rid_gnd Bit 26 - rid_a Bit 25 - rid_b Bit 24 - rid_c
[23]	RWSC	adpint	An interrupt is generated when the ADP is in progress. Setting this bit to 1 clears this interrupt.

[22]	RO	bsessvld	B session validity 0: B-Valid = 0 1: B-valid = 1
[21]	RO	iddig	IDDIG signal status indicator Current operating mode 0: host mode 1: device mode
[20:19]	RO	linestate	Current line state indicator 00: DM = 0, DP = 0 01: DM = 0, DP = 1 10: DM = 1, DP = 0 11: undefined
[18]	RW	stschngintmsk	StsChng interrupt mask 0: masked 1: not masked
[17]	RWSC	stschngint	StsChng interrupt The bit indicates whether the status of the IDDIG or BSessVld signal changes. 0: not changed 1: changed
[16]	RW	srpdetectmsk	SRPDetect interrupt mask, valid only in host mode 0: not masked 1: masked
[15]	RWSC	srpdetect	SRP detection 0: not detected 1: detected
[14]	RW	conndetmsk	Connection detection interrupt mask 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[13]	RO	connectdet	Connection detection 0: disconnected 1: connected This bit is valid only when OTG_EN_PWROPT is 2.
[12]	RW	disconnectdetectmsk	Disconnection detection interrupt mask 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.

[11]	RWSC	disconnectdetect	Disconnection detection 0: not disconnected 1: disconnected This bit is valid only when OTG_EN_PWROPT is 2.
[10]	RW	resetdetmsk	Reset detection interrupt mask 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[9]	RWSC	resetdetected	Reset detection 0: not reset 1: reset This bit is valid only when OTG_EN_PWROPT is 2.
[8]	RW	linestagechangemsk	Line state change interrupt mask 0: masked 1: not masked This bit is valid only when OTG_EN_PWROPT is 2.
[7]	RWSC	lnstschng	Line state change detection 0: not changed 1: changed This bit is valid only when GPWRDN[pmuactv] is 1 and OTG_EN_PWROPT is 2.
[6]	RW	disablevbus	Vbus disable In host mode: 0: PrtPwr is not 0. 1: PrtPwr is 0. In device mode: 0: The level of the bvalid signal is high. 1: The level of the bvalid signal is low. This bit is valid only when GPWRDN[pmuactv] is 1.
[5]	RW	pwrdnswtch	Power down switch 0: on 1: off
[4]	RW	pwrdnrst_n	Power down reset 0: reset 1: not reset
[3]	RW	pwrdnclmp	Power down beat enable 0: disabled 1: enabled

[2]	RW	restore	Restore 0: DWC_otg is in normal mode. 1: DWC_otg is in restore mode. This bit is valid only when OTG_EN_PWROPT is 2.
[1]	RW	pmuactv	PMU enable 0: disabled 1: enabled
[0]	RW	pmuintsel	PMU interrupt select 0: internal DWC_otg_core interrupt 1: external DWC_otg_core interrupt

GDFIFOCFG

GDFIFOCFG is a DFIFO software configuration register.

Offset Address	Register Name	Total Reset Value
0x005C	GDFIFOCFG	0x0501_0511

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epinfobaseaddr																gdfifocfg															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	epinfobaseaddr	Start address for the EP info controller
[15:0]	RW	gdfifocfg	DFIFO size, which is dynamically configured

GADPCTL

GADPCTL is an ADP timer control and status register.

Offset Address	Register Name	Total Reset Value
0x0060	GADPCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			ar		adptoutmsk	adpsnsintmsk	adpprbintmsk	adptoutint	adpsnsint	adpprbint	adpen	adpres	enasns	enaprb	rtim												prbper			prbdelta	prbdschg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved
[28:27]	RW	ar	Access request 00: read/write 01: read-only 10: write-only 11: reserved
[26]	RW	adptoutmsk	ADP timeout interrupt mask 0: masked 1: not masked **NOTE** This bit is valid only when OTG_Ver is 1.
[25]	RW	adpsnsintmsk	ADP sense interrupt mask 0: masked 1: not masked **NOTE** This bit is valid only when OTG_Ver is 1.
[24]	RWC	adpprbintmsk	ADB probe interrupt mask 0: masked 1: not masked **NOTE** This bit is valid only when OTG_Ver 1.
[23]	RWC	adptoutint	ADP timeout interrupt Setting this bit to 1 clears this interrupt. **NOTE** This bit is valid only when OTG_Ver 1.

[22]	RWC	adpsnsint	ADP sense interrupt Setting this bit to 1 clears this interrupt. **NOTE** This bit is valid only when OTG_Ver 1.
[21]	RWC	adpprbint	ADP probe interrupt Setting this bit to 1 clears this interrupt. **NOTE** This bit is valid only when OTG_Ver 1.
[20]	RW	adpen	ADP enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_Ver 1.
[19]	RWC	adpres	ADP reset 0: not reset 1: reset **NOTE** This bit is valid only when OTG_Ver 1.
[18]	RW	enasns	Sense enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_Ver 1.
[17]	RW	enaprb	Probe enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_Ver 1.
[16:6]	RO	rtim	Ramp time The following is the mapping between the values and 32 kHz clock cycle: 0x000: 1 cycles 0x001: 2 cycles 0x002: 3 cycles ... 0x7FF: 2048 cycles

[5:4]	RW	prbper	Probe period 00: 0.625s to 0.925s (0.775s typically) 01: 1.25s to 1.85s (1.55s typically) 10: 1.9s to 2.6s (2.275s typically) 11: reserved
[3:2]	RW	prbdelta	Probe delta The following is the mapping between the values and 32 kHz clock cycle: 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
[1:0]	RW	prbdschg	Probe discharge TADP_DSCHG time 00: 4 ms 01: 8 ms 10: 16 ms 11: 32 ms

HPTXFSIZ

HPTXFSIZ is a TX FIFO configuration register.

Offset Address	Register Name	Total Reset Value
0x0100	HPTXFSIZ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ptxfsize																ptxfstaddr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ptxfsize	Depth of the host periodic TX FIFO. Its value range is 16−32768.
[15:0]	RW	ptxfstaddr	Start address for the host periodic TX FIFO

DPTXFSIZN

DPTXFSIZN is a device periodic TX FIFO-*n* size register.

NOTE

This register is valid only in shared FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104 + 0x0004 x FIFO_num (FIFO_num = 0–14)	DPTXFSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dptxfsize																dptxfstaddr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dptxfsize	Size of the device periodic TX FIFO The value range is 4–768.
[15:0]	RW	dptxfstaddr	Start address for the device periodic TX FIFO RAM

DIEPTXFN

DIEPTXFN is a device IN endpoint TX FIFO size register.

NOTE

This register is valid only in dedicated FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104 + 0x0004 x FIFO_num (FIFO_num = 0–14)	DIEPTXFN	0x0300_0251

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inepntxfdep																inepntxfstaddr															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	inepntxfdep	Depth of the IN endpoint TX FIFO The value range is 16–32768.
[15:0]	RW	inepntxfstaddr	Start address for the IN endpoint FIFO*n* TX RAM

DCFG

DCFG is a device configuration register.

Offset Address	Register Name	Total Reset Value
0x0800	DCFG	0x8100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	resvalid						perschintvl		descdma	epmiscnt					reserved				endevoutnak	perfrint	devaddr								ena32khzsusp	nzstsouthshk	devspd	
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	resvalid	Resume time control This bit is valid only when DCFG[ena32khzsusp] is 1.
[25:24]	RW	perschintvl	Ratio of the (micro) frames in scatter/gather DMA mode 00: 25% of (micro) frames 01: 50% of (micro) frames 10: 75% of (micro) frames 11: reserved
[23]	RW	descdma	Scatter/Gather DMA enable in device mode 0: disabled 1: enabled
[22:18]	RW	epmiscnt	IN endpoint mismatch statistics
[17:14]	RO	reserved	Reserved
[13]	RW	endevoutnak	Device OUT NAK enable 0: disabled 1: enabled
[12:11]	RW	perfrint	Periodic frame interval 00: 80% of the (micro) frame interval 01: 85% 10: 90% 11: 95%
[10:4]	RW	devaddr	Device address
[3]	RW	ena32khzsusp	32 kHz suspend mode enable 0: disabled 1: enabled
[2]	RW	nzstsouthshk	Non-zero-length status OUT handshake select

[1:0]	RW	devspd	Device speed 00: high speed (30 MHz or 60 MHz USB 2.0 PHY clock) 01: full speed (30 MHz or 60 MHz USB 2.0 PHY clock) 10: low speed (6 MHz USB 1.1 transceiver clock) 11: full speed (48 MHz USB 1.1 transceiver clock)

DCTL

DCTL is a device control register.

Offset Address	Register Name	Total Reset Value
0x0804	DCTL	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														encontonbna	nakonbble	ignrfrmnum	reserved			pwronprgdone	cgoutnak	sgoutnak	cgnpinnak	sgnpinnak	tstctl			goutnaksts	gnpinnaksts	sftdiscon	rmtwkupsig
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	encontonbna	Continue on BNA enable 0: disabled 1: enabled
[16]	RW	nakonbble	NAK on babble error 0: no operation 1: NAK configured on the received babble
[15]	RW	ignrfrmnum	Whether the number of frames on isochronous endpoints is ignored 0: not ignored 1: ignored
[14:12]	RO	reserved	Reserved
[11]	RW	pwronprgdone	Resume from the power-down mode 0: not woken up 1: woken up
[10]	WO	cgoutnak	Global OUT NAK clear 0: no operation 1: cleared

[9]	WO	sgoutnak	Global OUT NAK 0: no operation 1: configured
[8]	WO	cgnpinnak	Global non-periodic IN NAK clear 0: no operation 1: cleared
[7]	WO	sgnpinnak	Global non-periodic IN NAK 0: no operation 1: configured
[6:4]	RW	tstctl	Test control 000: test mode disabled 001: Test_J mode 010: Test_K mode 011: Test_SE0_NAK mode 100: Test_Packet mode 101: Test_Force_Enable Other values: reserved
[3]	RO	goutnaksts	Global OUT NAK status 0: handshake TX 1: NAK handshake TX
[2]	RO	gnpinnaksts	Global non-periodic IN NAK status 0: handshake TX 1: NAK handshake TX
[1]	RW	sftdiscon	Soft disconnection 0: common mode 1: The core drives phy_opmode_o to 2'b01, and then triggers USB disconnection.
[0]	RW	rmtwkupsig	Remote wakeup signal TX 0: not woken up remotely 1: woken up remotely

DSTS

DSTS is a device status query register.

Offset Address	Register Name	Total Reset Value
0x0808	DSTS	0x0007_FF02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								devlnsts				soffn												reserved				errticerr		enumspd		suspsts	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:22]	RO	devlnsts	Logic level of the current USB data line bit[23]: logic level of D+ bit[22]: logic level of D−
[21:8]	RO	soffn	Number of frames or micro frames in the received SOF packets
[7:4]	RO	reserved	Reserved
[3]	RO	errticerr	Irregular error indicator The controller core sets this bit to **1** when any irregular error (for example, phy_rxvalid_i is set to **1** and retains this value for 2 ms due to an PHY error) occurs in the UTMI+ interface. 0: No irregular error occurs in the UTMI+ interface. 1: An irregular error occurs in the UTMI+ interface.
[2:1]	RO	enumspd	Enumeration speed 00: high speed (30 MHz or 60 MHz PHY clock) 01: full speed (30 MHz or 60 MHz PHY clock) 10: low speed (6 MHz PHY clock). 11: full speed (48 MHz PHY clock).
[0]	RO	suspsts	Suspend status. When the suspend conditions are detected, this bit is 1.

DIEPMSK

DIEPMSK is a common interrupt mask register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0810	DIEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nakmsk	reserved			bnainintrmsk	txfifoundrnmsk	reserved	inepnakeffmsk	intknepmismsk	intkntxfempmsk	timeoutmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12:10]	RO	reserved	Reserved
[9]	RW	bnainintrmsk	BNA interrupt mask 0: masked 1: not masked
[8]	RW	txfifoundrnmsk	FIFO underrun interrupt mask 0: masked 1: not masked
[7]	RO	reserved	Reserved
[6]	RW	inepnakeffmsk	IN endpoint NAK effective interrupt mask 0: masked 1: not masked
[5]	RW	intknepmismsk	IN token received with EP mismatch interrupt mask 0: masked 1: not masked
[4]	RW	intkntxfempmsk	IN token received when TX FIFO empty interrupt mask 0: masked 1: not masked
[3]	RW	timeoutmsk	Timeout interrupt mask 0: masked 1: not masked

[2]	RW	ahberrmsk	AHB error interrupt mask 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask 0: masked 1: not masked

DOEPMSK

DOEPMSK is a common interrupt mask register for device OUT endpoints.

Offset Address	Register Name	Total Reset Value
0x0814	DOEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	nyetmsk	nakmsk	bbleerrmsk	reserved		bnaoutintrmsk	outpkterrmsk	reserved	back2backsetupmsk	stsphsercvdmsk	outtknepdismsk	setupmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	nyetmsk	NYET interrupt mask 0: masked 1: not masked
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12]	RW	bbleerrmsk	Babble error interrupt mask 0: masked 1: not masked
[11:10]	RO	reserved	Reserved

[9]	RW	bnaoutintrmsk	BNA interrupt mask 0: masked 1: not masked
[8]	RW	outpkterrmsk	OUT packet error interrupt mask 0: masked 1: not masked
[7]	RO	reserved	Reserved
[6]	RW	back2backsetupmsk	Back-to-back setup packets received interrupt mask 0: masked 1: not masked
[5]	RW	stsphsercvdmsk	Status phase received interrupt mask 0: masked 1: not masked
[4]	RW	outtknepdismsk	W OUT token received when endpoint disabled interrupt mask 0: masked 1: not masked
[3]	RW	setupmsk	Setup phase done interrupt mask 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask 0: masked 1: not masked

DAINT

DAINT is an interrupt register for all device endpoints.

Offset Address	Register Name	Total Reset Value
0x0818	DAINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepint																inepint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	outepint	OUT endpoint interrupt Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RO	inepint	IN endpoint interrupt Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DAINTMSK

DAINTMSK is an interrupt mask register for all endpoints.

Offset Address	Register Name	Total Reset Value
0x081C	DAINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepmsk																inepmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	outepmsk	OUT endpoint interrupt mask Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RW	inepmsk	IN endpoint interrupt mask Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DTKNQR1

DTKNQR1 is device IN token sequence learning queue read register 1.

Offset Address	Register Name	Total Reset Value
0x0820	DTKNQR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6 5	4	3 2 1 0
Name	eptkn						wrapbit	reserved		intknwptr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0	0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 5 Bit[27:24]: endpoint ID of token 4 … Bit[15:12]: endpoint ID of token 1 Bit[11:8]: endpoint ID of token 0
[7]	RO	wrapbit	Wrapping bit 0: The learning queue of the IN token is cleared. 1: The write pointer is wrapped.
[6:5]	RO	reserved	Reserved
[4:0]	RO	intknwptr	IN token queue write pointer

DTKNQR2

DTKNQR2 is device IN token sequence learning queue read register 2.

Offset Address	Register Name	Total Reset Value
0x0824	DTKNQR2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	eptkn							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 13

			Bit[27:24]: endpoint ID of token 12 … Bit[7:4]: endpoint ID of token 7 Bit[3:0]: endpoint ID of token 6

DTKNQR3

DTKNQR3 is device in token sequence learning queue read register 3.

Offset Address	Register Name	Total Reset Value
0x0830	DTKNQR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 21 Bit[27:24]: endpoint ID of token 20 … Bit[7:4]: endpoint ID of token 15 Bit[3:0]: endpoint ID of token 14

DTKNQR4

DTKNQR4 is device IN token sequence learning queue read register 4.

Offset Address	Register Name	Total Reset Value
0x0834	DTKNQR4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Token endpoint ID Four bits are used to indicate the token endpoint ID. Bit[31:28]: endpoint ID of token 29 Bit[27:24]: endpoint ID of token 28

			… Bit[7:4]: endpoint ID of token 23 Bit[3:0]: endpoint ID of token 22

DVBUSDIS

DVBUSDIS is a device VBUS discharge time register.

Offset Address	Register Name	Total Reset Value
0x0828	DVBUSDIS	0x0000_17D7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dvbusdis															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dvbusdis	Device VBUS discharge time

DVBUSPULSE

DVBUSPULSE is a device VBUS pulsing time register.

Offset Address	Register Name	Total Reset Value
0x082C	DVBUSPULSE	0x0000_05B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dvbuspulse											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	dvbuspulse	Device VBUS pulse time

DTHRCTL

DTHRCTL is a device threshold control register.

Offset Address	Register Name	Total Reset Value
0x0830	DTHRCTL	0x0C10_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				arbprken	reserved			rxthrlen							rxthren	reserved				ahbthrratio				txthrlen						isothren	nonisothren
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	arbprken	Arbitrator parking enable 0: disabled 1: enabled
[26]	RO	reserved	Reserved
[25:17]	RW	rxthrlen	RX threshold length
[16]	RW	rxthren	RX threshold enable Some RX FIFO problems may be caused after the RX threshold is enabled, especially when there are RX and babble errors. 0: disabled 1: enabled
[15:13]	RO	reserved	Reserved
[12:11]	RW	ahbthrratio	AHB threshold ratio 00: AHB threshold = MAC threshold 01: AHB threshold = MAC threshold/2 10: AHB threshold = MAC threshold/4 11: AHB threshold = MAC threshold/8
[10:2]	RW	txthrlen	TX threshold length
[1]	RW	isothren	ISO IN endpoint threshold enable 0: disabled 1: enabled
[0]	RW	nonisothren	Non-ISO IN endpoint threshold enable 0: disabled 1: enabled

DIEPEMPMSK

DIEPEMPMSK is a FIFO empty interrupt mask register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0834	DIEPEMPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ineptxfempmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ineptxfempmsk	IN EP TX FIFO empty interrupt mask Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DEACHINT

DEACHINT is an interrupt register for each device endpoint.

Offset Address	Register Name	Total Reset Value
0x0838	DEACHINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepint																echinepint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	echoutepint	OUT endpoint interrupt Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RW	echinepint	IN endpoint interrupt Bit 15: IN endpoint 0 ... Bit 0: IN endpoint 15

DEACHINTMSK

DEACHINTMSK is an interrupt mask register for each device endpoint.

Offset Address	Register Name	Total Reset Value
0x083C	DEACHINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	echoutepmsk																echinepmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	echoutepmsk	OUT endpoint interrupt mask Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15 0: masked 1: not masked
[15:0]	RW	echinepmsk	IN endpoint interrupt mask Bit 16: IN endpoint 0 ... Bit 31: IN endpoint 15 0: masked 1: not masked

DIEPEACHMSKN

DIEPEACHMSKN is an interrupt register for device IN endpoint *n*.

Offset Address: 0x0840 + (0x0004 x *n*) (*n* = 0−15)

Register Name: DIEPEACHMSKN

Total Reset Value: 0x0040_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nakmsk	reserved			bnainintrmsk	txfifoundrnmsk	reserved	inepnakeffmsk	intknepmismsk	intkntxfempmsk	timeoutmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12:10]	RO	reserved	Reserved
[9]	RW	bnainintrmsk	BNA interrupt mask 0: masked 1: not masked
[8]	RW	txfifoundrnmsk	FIFO underrun interrupt mask 0: masked 1: not masked
[7]	RO	reserved	Reserved
[6]	RW	inepnakeffmsk	IN endpoint NAK effective interrupt mask 0: masked 1: not masked
[5]	RW	intknepmismsk	IN token received with EP mismatch interrupt mask 0: masked 1: not masked
[4]	RW	intkntxfempmsk	IN token received when TX FIFO empty interrupt mask 0: masked 1: not masked
[3]	RW	timeoutmsk	Timeout interrupt mask (non-isochronous endpoints) 0: masked 1: not masked

[2]	RW	ahberrmsk	AHB error interrupt mask 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disable interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completion interrupt mask 0: masked 1: not masked

DOEPEACHMSKN

DOEPEACHMSKN is an interrupt register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0880 + (0x0004 x *n*) (*n* = 0−15)	DOEPEACHMSKN	0x0080_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	nyetmsk	nakmsk	bbleerrmsk	reserved		bnaoutintrmsk	outpkterrmsk	reserved	back2backsetup	reserved	outtknepdismsk	setupmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	nyetmsk	NYET interrupt mask 0: masked 1: not masked
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12]	RW	bbleerrmsk	Babble error interrupt mask 0: masked 1: not masked
[11:10]	RO	reserved	Reserved

[9]	RW	bnaoutintrmsk	BNA interrupt mask 0: masked 1: not masked
[8]	RW	outpkterrmsk	OUT packet error interrupt mask 0: masked 1: not masked
[7]	RO	reserved	Reserved
[6]	RW	back2backsetup	Back-to-back setup packets received interrupt mask 0: masked 1: not masked
[5]	RO	reserved	Reserved
[4]	RW	outtknepdismsk	OUT token received when endpoint disabled interrupt mask 0: masked 1: not masked
[3]	RW	setupmsk	Setup phase done interrupt mask 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB error interrupt mask 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completion interrupt mask 0: masked 1: not masked

DIEPCTL0

DIEPCTL0 is a control register for device control IN endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0900	DIEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	txfnum				stall	reserved	eptype		naksts	reserved	usbactep	nextep			reserved								mps			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable When the IN endpoint works in scatter or gather DMA mode, this bit indicates that the descriptor structure and data buffer used for transmitting data have been set up. When the scatter or gather DMA mode is disabled, this bit indicates that data to be transmitted is ready. 0: invalid 1: valid
[30]	RWSC	epdis	Endpoint disable The application program sets this bit to **1** to end the data transmission of this endpoint. This bit is enabled only in DMA mode. 0: invalid 1: valid
[29:28]	RO	reserved	Reserved
[27]	WO	snak	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. The controller core can set this bit of an endpoint after this endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	cnak	NAK clear Writing to this bit clears the NAK bit of the endpoint. 0: invalid 1: valid
[25:22]	RW	txfnum	Number of TX FIFOs

[21]	RWSC	stall	Stall handshake The application program can set this bit. The controller core clears this bit after the endpoint receives the setup packet. 0: invalid 1: valid
[20]	RO	reserved	Reserved
[19:18]	RO	eptype	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	naksts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	reserved	Reserved
[15]	RO	usbactep	USB activation endpoint 0 This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid 1: valid
[14:11]	RO	nextep	Next endpoint This field specifies the ID of the next endpoint that receives data.
[10:2]	RO	reserved	Reserved
[1:0]	RW	mps	Minimum packet size 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DOEPCTL0

DOEPCTL0 is a control register for device control OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B00	DOEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	reserved				stall	snp	eptype		naksts	reserved	usbactep	reserved											mps			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable When the scatter/gather DMA is enabled: 0: The descriptor structure and the data RX function of the data buffer are disabled. 1: The descriptor structure and the data RX function of the data buffer are enabled. When the scatter/gather DMA is disabled: 0: The function of receiving data from the USB module to the memory is disabled. 1: The function of receiving data from the USB module to the memory is enabled.
[30]	RO	epdis	Endpoint disable The application program cannot disable OUT control transfer endpoint 0. 0: enabled 1: disabled
[29:28]	RO	reserved	Reserved
[27]	WO	snak	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. The controller core can set this bit of an endpoint after this endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	cnak	NAK clear Writing to this bit clears the NAK bit of the endpoint. 0: invalid 1: valid
[25:22]	RO	reserved	Reserved

[21]	RWSC	stall	Stall handshake The application program can set this bit. The controller core clears this bit after the endpoint receives the setup packet. 0: invalid 1: valid
[20]	RW	snp	Snooping mode This bit is used to set the endpoint to the snooping mode. In snooping mode, the controller core checks whether the OUT packet is correct after it sends the packet to the application memory. 0: invalid 1: valid
[19:18]	RO	eptype	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	naksts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	reserved	Reserved
[15]	RO	usbactep	USB activation endpoint 0 This bit is always 1, indicating that control endpoint 0 is always valid. 0: invalid 1: valid
[14:2]	RO	reserved	Reserved
[1:0]	RW	mps	Minimum packet size 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DIEPCTLN

DIEPCTLN is a control register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + (0x0020 x *n*) (*n* = 0–15)	DIEPCTLN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EPEna	EPDis	SetD1PID_SetOddFr	SetD0PID_SetEvenFr	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID_EO_FrNum	USBActEP	NextEp			MPS											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable When the scatter or gather DMA is enabled: 0: The descriptor structure and the data TX function of the data buffer are disabled. 1: The descriptor structure and the data TX function of the data buffer are disabled. When the scatter/gather DMA is disabled: 0: The data on endpoints is not ready. 1: The data on endpoints is ready.
[30]	RWSC	EPDis	Endpoint disable This bit applies to the IN and OUT endpoints. The application program can set this bit to **1** to stop the data transmission/reception of an IN/OUT endpoint. 0: enabled 1: disabled
[29]	WO	SetD1PID_SetOddFr	DATA1 PID/odd micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA1 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to odd micro-frames by setting this bit to **1**. 0: invalid 1: valid

[28]	WO	SetD0PID_SetEvenFr	DATA0 PID/even micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA0 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to even micro-frames by setting this bit to **1**. 0: invalid 1: valid
[27]	WO	SNAK	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. For an OUT endpoint, this bit is set after the controller core receives the transfer completion interrupt or the OUT endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	CNAK	NAK clear Writing to this bit clears the NAK bit of an IN/OUT endpoint. 0: invalid 1: valid
[25:22]	RW	TxFNum	Number of TX FIFOs Shared FIFO operation: 0: non-periodic TX FIFO Other values: specified periodic TX FIFO number Dedicated FIFO operation: Number of FIFOs This field is valid only for IN endpoints.
[21]	RW	Stall	Stall handshake This bit applies to the non-control transfer and non-real-time transfer IN and OUT endpoints. If this bit is set to **1**, the application program blocks the token packets transmitted from the USB host controller to the endpoint. 0: invalid 1: valid For the control endpoint (RWSC), this bit is set to **1** by the application program and cleared by the controller core only when the endpoint receives the setup token. 0: invalid 1: valid

[20]	RW	Snp	Snooping mode This bit is used to set the OUT endpoints to the snooping mode. In snooping mode, the controller core does not check whether the OUT packet is correct before sending the packet to the application memory. 0: invalid 1: valid
[19:18]	RW	EPType	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	NAKSts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	DPID_EO_FrNum	Endpoint data PID 0: DATA0 1: DATA1 Even/Odd frame Non-scatter/Gather DMA mode: 0: even frame 1: odd frame Scatter/Gather DMA mode: Reserved
[15]	RWSC	USBActEP	USB activation endpoint This bit applies to the IN and OUT endpoints and indicates whether an endpoint is valid. 0: invalid 1: valid
[14:11]	RW	NextEp	Next endpoint This field specifies the ID of the next endpoint that receives data.
[10:0]	RW	MPS	Maximum packet size

DOEPCTLN

DOEPCTLN is a control register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B00 + (0x0020 x *n*) (*n* = 0–15)	DOEPCTLN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EPEna	EPDis	SetD1PID_SetOddFr	SetD0PID_SetEvenFr	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID_EO_FrNum	USBActEP	NextEp			MPS											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	EPEna	Endpoint enable When the scatter or gather DMA is enabled: 0: The descriptor structure and the data RX function of the data buffer are disabled. 1: The descriptor structure and the data RX function of the data buffer are enabled. When the scatter/gather DMA is disabled: 0: The function of receiving data from the USB module to the memory is disabled. 1: The function of receiving data from the USB module to the memory is enabled.
[30]	RWSC	EPDis	Endpoint disable This bit applies to the IN and OUT endpoints. The application program can set this bit to **1** to stop the data transmission/reception of an IN/OUT endpoint. 0: enabled 1: disabled
[29]	WO	SetD1PID_SetOddFr	DATA1 PID/odd micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA1 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to odd micro-frames by setting this bit to **1**. 0: invalid 1: valid

[28]	WO	SetD0PID_SetEvenFr	DATA0 PID/even micro-frame configuration The data PID of the interrupt endpoint and bulk IN/OUT endpoint can be set to DATA0 by setting this bit to **1**. 0: invalid 1: valid For the real-time IN/OUT endpoint, the odd and even micro-frames can be set to even micro-frames by setting this bit to **1**. 0: invalid 1: valid
[27]	WO	SNAK	NAK configuration Writing to this bit sets the NAK bit of the endpoint to **1**. The application program can use this bit to control the NAK handshake of an endpoint during a transfer. For an OUT endpoint, this bit is set after the controller core receives the transfer completion interrupt or the OUT endpoint receives the setup packet. 0: invalid 1: valid
[26]	WO	CNAK	NAK clear Writing to this bit clears the NAK bit of an IN/OUT endpoint. 0: invalid 1: valid
[25:22]	RW	TxFNum	Number of TX FIFOs Shared FIFO operation: 0: non-periodic TX FIFO Other values: specified periodic TX FIFO.number Dedicated FIFO operation: Number of FIFOs This field is valid only for IN endpoints.
[21]	RW	Stall	Stall handshake (RW) This bit applies to the non-control transfer and non-real-time transfer IN and OUT endpoints. If this bit is set to **1**, the application program blocks the token packets transmitted from the USB host controller to the endpoint. 0: invalid 1: valid For the control endpoint (RWSC), this bit is set to **1** by the application program and cleared by the controller core only when the endpoint receives the setup token. 0: invalid 1: valid

[20]	RW	Snp	Snooping mode This bit is used to set the OUT endpoint to the snooping mode. In snooping mode, the controller core does not check whether the OUT packet is correct before sending the packet to the application memory. 0: invalid 1: valid
[19:18]	RW	EPType	Endpoint type 00: control transfer endpoint 01: real-time transfer endpoint 10: bulk transfer endpoint 11: interrupt transfer endpoint
[17]	RO	NAKSts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	RO	DPID_EO_FrNum	Endpoint data PID 0: DATA0 1: DATA1 Even/Odd frame Non-scatter/Gather DMA mode: 0: even frame 1: odd frame Scatter/Gather DMA mode: Reserved
[15]	RWSC	USBActEP	USB activation endpoint This bit applies to the IN and OUT endpoints and indicates whether an endpoint is valid. 0: invalid 1: valid
[14:11]	RW	NextEp	Next endpoint This field specifies the ID of the next endpoint that receives data.
[10:0]	RW	MPS	Maximum packet size

DIEPINTn

DIEPINTn is an interrupt register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0908 + (0x0020 x *n*) (*n* = 0−15)	DIEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	TxfifoUndm_OutPktErr	TxFEmp	INEPNakEff_Back2BackSETup	INTknEPMis_StsPhseRcvd	INTknTXFEmp_OUTTknEPdis	TimeOUT_SetUp	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15]	RWSC	StupPktRcvd	Whether setup packets are received 0: no 1: yes
[14]	RWSC	NYETIntrpt	NYET interrupt NYET response TX interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[13]	RWSC	NAKIntrpt	NAK interrupt NAK TX interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[12]	RWSC	BbleErrIntrpt	Babble error interrupt Endpoint received babble interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[11]	RWSC	PktDrpSts	Packet drop status interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[10]	RO	reserved	Reserved

[9]	RWSC	BNAIntr	BNA interrupt An interrupt is generated when descriptor access is not ready. 0: An interrupt is cleared. 1: An interrupt is generated.
[8]	RWSC	TxfifoUndrn_OutPktErr	FIFO underrun interrupt An interrupt is generated when the FIFO underrun conditions are transmitted. The interrupt is valid when the following conditions are met: • OTG_EN_DED_TX_FIFO is 1. • Thresholding is enabled. OUT packet error An interrupt is generated when an overrun or CRC error is detected. The interrupt is valid when the following conditions are met: • OTG_EN_DED_TX_FIFO is 1. • Thresholding is enabled.
[7]	RO	TxFEmp	TX FIFO empty status interrupt An interrupt is generated when the TX FIFO is empty or half empty. 0: An interrupt is cleared. 1: An interrupt is generated. **NOTE** This bit is valid only for IN endpoints.
[6]	RWSC	INEPNakEff_Back2BackSETup	IN endpoint NAK effective interrupt An interrupt is generated when the IN endpoint bit is set. Back-to-back setup package received interrupt An interrupt is generated when the core receives more than three back-to-back setup packets. 0: An interrupt is cleared. 1: An interrupt is generated.
[5]	RWSC	INTknEPMis_StsPhseRcvd	An interrupt is generated when the IN tokens with mismatch EP are received. A control write pulse is received. 0: An interrupt is cleared. 1: A control write pulse is received.

[4]	RWSC	INTknTXFEmp_OUTTknEPdis	An interrupt is generated if IN tokens are received when the corresponding TX FIFO is empty. An interrupt is generated if OUT tokens are received when endpoints are disabled. 0: An interrupt is cleared. 1: An interrupt is generated.
[3]	RWSC	TimeOUT_SetUp	Timeout interrupt An interrupt is generated when timeout conditions are detected. Setup phase done interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[2]	RWSC	AHBErr	AHB error interrupt An interrupt is generated when an AHB error occurs during AHB read/write operations in internal DMA mode. 0: An interrupt is cleared. 1: An interrupt is generated.
[1]	RWSC	EPDisbld	Endpoint disable interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[0]	RWSC	XferCompl	Transfer completion interrupt 0: An interrupt is cleared. 1: An interrupt is generated.

DOEPINTn

DOEPINTn is an interrupt register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B08 + (0x0020 x *n*) (*n* = 0−15)	DOEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	TxfifoUndrn_OutPktErr	TxFEmp	INEPNakEff_Back2BackSETup	INTknEPMis_StsPhseRcvd	INTknTXFEmp_OUTTknEPdis	TimeOUT_SetUp	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RWSC	StupPktRcvd	Whether setup packets are received 0: no 1: yes
[14]	RWSC	NYETIntrpt	NYET interrupt NYET response TX interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[13]	RWSC	NAKIntrpt	NAK interrupt NAK TX interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[12]	RWSC	BbleErrIntrpt	Babble error interrupt Endpoint received babble interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[11]	RWSC	PktDrpSts	Packet drop status interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[10]	RO	reserved	Reserved

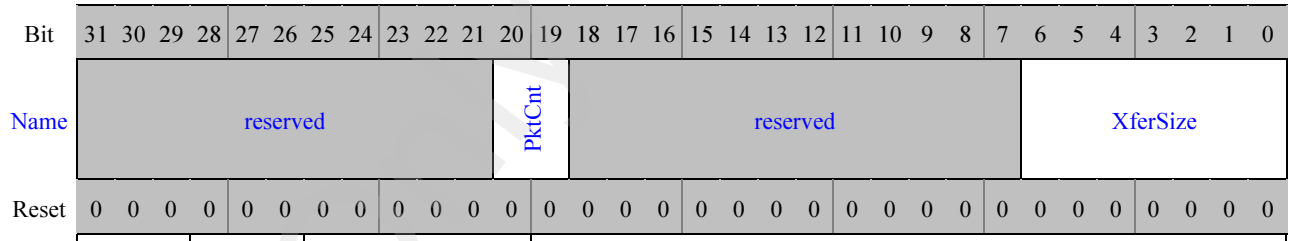
[9]	RWSC	BNAIntr	BNA interrupt An interrupt is generated when descriptor access is not ready. 0: An interrupt is cleared. 1: An interrupt is generated.
[8]	RWSC	TxfifoUndrn_OutPktErr	FIFO underrun interrupt An interrupt is generated when the FIFO underrun conditions are transmitted. The interrupt is valid when the following conditions are met: – OTG_EN_DED_TX_FIFO is 1. – Thresholding is enabled. OUT packet error An interrupt is generated when an overrun or CRC error is detected. The interrupt is valid when the following conditions are met: – OTG_EN_DED_TX_FIFO is 1. – Thresholding is enabled.
[7]	RO	TxFEmp	TX FIFO empty status interrupt An interrupt is generated when the TX FIFO is empty or half empty. This bit is valid only for IN endpoints. 0: An interrupt is cleared. 1: An interrupt is generated.
[6]	RWSC	INEPNakEff_Back2BackSETup	IN endpoint NAK effective interrupt An interrupt is generated when the IN endpoint bit is set. Back-to-back setup package received interrupt An interrupt is generated when the core receives more than three back-to-back setup packets. 0: An interrupt is cleared. 1: An interrupt is generated.
[5]	RWSC	INTknEPMis_StsPhseRcvd	An interrupt is generated when the IN tokens with mismatch EP are received. A control write pulse is received. 0: An interrupt is cleared. 1: An interrupt is generated.
[4]	RWSC	INTknTXFEmp_OUTTknEPdis	An interrupt is generated if IN tokens are received when the corresponding TX FIFO is empty. An interrupt is generated if OUT tokens are received when endpoints are disabled. 0: An interrupt is cleared. 1: An interrupt is generated.

[3]	RWSC	TimeOUT_SetUp	Timeout interrupt An interrupt is generated when timeout conditions are detected. Setup phase done interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[2]	RWSC	AHBErr	AHB error interrupt An interrupt is generated when an AHB error occurs during AHB read/write operations in internal DMA mode. 0: An interrupt is cleared. 1: An interrupt is generated.
[1]	RWSC	EPDisbld	Endpoint disable interrupt 0: An interrupt is cleared. 1: An interrupt is generated.
[0]	RWSC	XferCompl	Transfer completion interrupt 0: An interrupt is cleared. 1: An interrupt is generated.

DIEPTSIZ0

DIEPTSIZ0 is a transfer size register for device IN endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0910	DIEPTSIZ0	0x0000_0000



Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:19]	RW	PktCnt	Number of packets
[18:7]	RO	reserved	Reserved
[6:0]	RW	XferSize	Transferred data size

DOEPTSIZ0

DOEPTSIZ0 is a transfer size register for device OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B10	DOEPTSIZ0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	SUPCnt			reserved								PktCnt	reserved											XferSize							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:29]	RW	SUPCnt	Number of setup packets 00: 0 packet 01: 1 packet 10: 2 packets 11: 3 packets
[28:20]	RO	reserved	Reserved
[19]	RW	PktCnt	Number of packets
[18:7]	RO	reserved	Reserved
[6:0]	RW	XferSize	Transferred data size

DIEPTSIZn

DIEPTSIZn is a transfer size register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0910 + (0x0020 x *n*) (*n* = 0–15)	DIEPTSIZn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	mc_rxdpid_supcnt			PktCnt												XferSize															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved

[30:29]	RW	mc_rxdpid_supcnt	Number of packets (IN endpoint, RW) 00: 0 packet 01: 1 packet 10: 2 packets 11: 3 packets Number of packets (non-periodic IN endpoints, RO) This field is valid only in internal DMA mode. PID of the received data (isochronous OUT endpoints, RO) 00: DATA0 01: DATA2 10: DATA1 11: MDATA Number of setup packets (OUT endpoint, RW) 01: 1 packet 10: 2 packets 11: 3 packets
[28:19]	RW	PktCnt	Number of packets
[18:0]	RW	XferSize	Transferred data size

DOEPTSIZn

DOEPTSIZn is a transfer size register for device OUT endpoint *n*.

Offset Address: 0x0B10 + (0x0020 x *n*) (*n* = 0−15)

Register Name: DOEPTSIZn

Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	mc_rxdpid_supcnt			PktCnt								XferSize																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved

[30:29]	RW	mc_rxdpid_supcnt	Number of packets (IN endpoint, RW) 00: 0 packet 01: 1 packet 10: 2 packets 11: 3 packets Number of packets (non-periodic IN endpoints, RO) This field is valid only in internal DMA mode. PID of the received data (isochronous OUT endpoints, RO) 00: DATA0 01: DATA2 10: DATA1 11: MDATA Number of setup packets (OUT endpoint, RW) 01: 1 packet 10: 2 packets 11: 3 packets
[28:19]	RW	PktCnt	Number of packets
[18:0]	RW	XferSize	Transferred data size

DIEPDMAN

DIEPDMAN is a DMA address register for device IN endpoint *n*.

Offset Address: 0x0914 + (0x0020 x *n*) (*n* = 0−15)
Register Name: DIEPDMAN
Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address

DOEPDMAN

DOEPDMAN is a DMA address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B14 + (0x0020 x n) (*n* = 0−15)	DOEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	DMA address

DIEPDMABN

DIEPDMABN is a DMA buffer address register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x091C + (0x0020 x *n*) (*n* = 0−15)	DIEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address

DOEPDMABN

DOEPDMABN is a DMA buffer address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B1C + (0x0020 x *n*) (*n* = 0−15)	DOEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	DMA buffer address

DTXFSTSn

DTXFSTSn is a TX FIFO status register for device IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0938	DTXFSTSn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																INEPTxFSpcAvail																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	INEPTxFSpcAvail	Available space for the IN endpoint TX FIFO 0x0: The endpoint TX FIFO is full. 0x1: One word is available. 0x2: Two words are available. 0xn: *n* words ($0 \leq n \leq 32768$) are available. 0x8000: 32768 words are available. Other values: reserved

12.10 USB 3.0 DRD

12.10.1 Overview

The USB 3.0 dual role device (DRD) module supports the static operations of the USB 3.0 host and USB 3.0 device. This module can be set to the USB 3.0 host mode or USB 3.0 device mode by configuring the corresponding register. The DRD module supports the 5 Gbit/s transfer rate defined in the USB 3.0 protocol as well as the 480 Mbit/s transfer rate defined in the USB 2.0 protocol. In addition, it fully complies with the eXtensible host controller interface 1.0 (XHCI 1.0) protocol, PHY interface for the PCI Express (PIPE) protocol (for super-speed transfer), and USB 2.0 transceiver macrocell interface (UTMI) protocol (for high-speed transfer). The DRD module has an integrated root hub for extending the USB port or other hubs. The USB 3.0 DRD controller has the following functions:

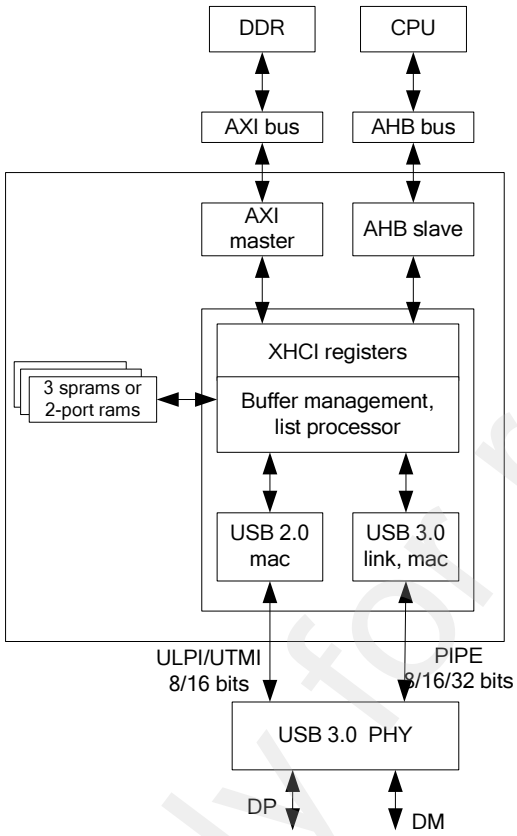
- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted over the USB port.
- Provides interfaces (such as the interrupt vector interface) for the driver.

12.10.2 Function Description

Logical Block Diagram

Figure 12-64 shows the logical block diagram of the USB 3.0 DRD module.

Figure 12-64 Logical block diagram of the USB 3.0 DRD module



NOTE

- UTMI: USB2.0 transceiver macrocell interface
- XHCI: eXtensible host controller interface

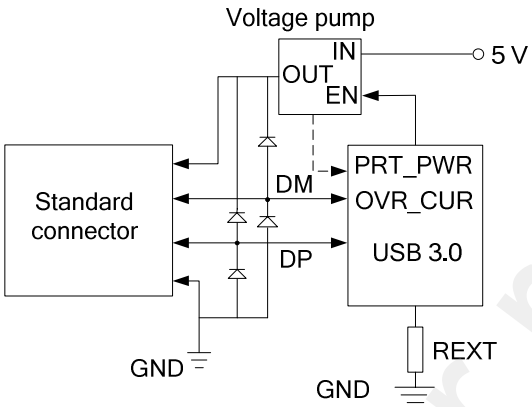
Typical Applications

Figure 12-65 shows the reference design of the USB 3.0 DRD module.

CAUTION

- The single-ended impedance of DP or DM is 45 Ω±1%, and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electro static discharge (ESD) components are used, 1 pF capacitors are recommended.

Figure 12-65 Reference design of the USB 3.0 DRD module



Features

The USB 3.0 DRD module has the following features:

- Complies with the USB 3.0 and USB 2.0 protocols.
- Complies with the XHCI 1.0 protocol.
- Independently works in host or device mode.
- Supports super-speed, high-speed, full-speed, and low-speed devices.
- Supports the USB 2.0 low-power solution and USB 3.0 power consumption states (U0, U1, U2, and U3).
- Supports control transfer, bulk transfer, isochronous transfer, and interrupt transfer in host mode and device mode.
- Supports the internal DMA controller.
- Supports a maximum of 127 devices by using USB hubs.

Function Implementation

The USB 3.0 DRD module supports the following transfer types in host mode:

- Control transfer

  This mode applies to the data transfer between endpoints 0 of the USB host and USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on

the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.

- Bulk transfer

  This mode applies to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and many data transfers are delayed. Bulk transfer is performed after all other types of data transfers are complete. In bulk transfer mode, data is transferred between the USB host and USB device without errors by using an error detection and retransmission mechanism.

- Interrupt transfer

  This mode applies to transfer of small-sized, scattered, and unpredictable data. In this mode, the device is regularly checked for interrupt data to be sent. The query frequency ranges from 1 ms to 255 ms, depending on the device endpoint mode. Typically, the interrupt transfer is unidirectional and only input is available for the USB host.

When the USB 3.0 DRD module works in device mode, control transfer, bulk transfer, isochronous transfer, and interrupt transfer are supported.

12.10.3 Operating Mode

Clock and Reset

The clock and reset registers must be configured before the USB controller is initialized.

To disable the working clock, perform the following steps:

Step 1 Write 0xF9 to PERI_CRG45 to deassert the reset on the USB 2.0 PHY.

Step 2 Write 0x1F01 to PERI_CRG46 so that the USB 2.0 PHY is selected to supply the UTMI clock source of the USB 3.0 controller.

Step 3 Write 0x1 to PERI_CRG43 bit[9] to select the 25 MHz COMPHY reference clock.

Step 4 Write 0x1 to PERI_CRG43 bit[8] to enable the clock gating of COMPHY.

Step 5 Write 0x1 to PERI_CRG43 bit[1] so that the soft-rest mode of the COMPHY port is controlled by PERI_CRG45 bit[0].

Step 6 Write 0x0 to PERI_CRG43 bit[0] to deassert the reset on COMPHY.

Step 7 Write 0x0 to PERI_CRG46 bit[0] to deassert the reset on the USB 3.0 controller.

----End

Host/Device Mode Switchover

The working mode of the DRD controller is switched as follows:

- To set the DRD controller to the host mode, write 2'b01 to PERI_USB3_GCTL[prtcapdir].
- To set the DRD controller to the device mode, write 2'b10 to PERI_USB3_GCTL[prtcapdir].

CAUTION

The host/device working mode can only be statically switched and cannot by dynamically switched.

12.10.4 Register Summary

Table 12-36 describes USB 3.0 registers.

Table 12-36 Summary of USB 3.0 registers (base address: 0x1018_0000)

Offset Address	Register	Description	Page
0xC100	PERI_USB3_GSBUSCFG0	Global SoC bus configuration register 0	12-306
0xC104	PERI_USB3_GSBUSCFG1	Global SoC bus configuration register 1	12-307
0xC108	PERI_USB3_GTXTHRCFG	Global TX threshold control register	12-308
0xC10C	PERI_USB3_GRXTHRCFG	Global RX threshold control register	12-309
0xC110	PERI_USB3_GCTL	Global core control register	12-309
0xC118	PERI_USB3_GSTS	Global status register	12-313
0xC11C	PERI_USB3_GUCTL1	Global user control register 1	12-314
0xC124	PERI_USB3_GGPIO	Global GPIO register	12-315
0xC128	PERI_USB3_GUID	Global user ID register	12-316
0xC12C	PERI_USB3_GUCTL	Global user control register	12-316
0xC130	PERI_USB3_GBUSERRADDR_HI	Global bus error address upper-32-bit register	12-318
0xC134	PERI_USB3_GBUSERRADDR_LO	Global bus error address lower-32-bit register	12-318
0xC138	PERI_USB3_GPRTBIMAP_HI	SS port-bus mapping upper-32-bit register	12-318

Offset Address	Register	Description	Page
0xC13C	PERI_USB3_GPRTBIMAP_LO	SS port-bus mapping lower-32-bit register	12-319
0xC180	PERI_USB3_GPRTBIMAP_HS_HI	HS port-bus mapping upper-32-bit register	12-319
0xC184	PERI_USB3_GPRTBIMAP_HS_LO	HS port-bus mapping lower-32-bit register	12-320
0xC188	PERI_USB3_GPRTBIMAP_FS_HI	FS port-bus mapping upper-32-bit register	12-320
0xC18C	PERI_USB3_GPRTBIMAP_FS	FS port-bus mapping lower-32-bit register	12-320
0xC200	PERI_USB3_GUSB2PHYCFGN	Global USB 2.0 PHY configuration register	12-318
0xC2C0	PERI_USB3_GUSB3PIPECTLN	Global USB 3.0 PIPE control register	12-323
0xC304	PERI_USB3_GTXFIFOSIZN	Global TX FIFO size register	12-326
0xC384	PERI_USB3_GRXFIFOSIZN	Global RX FIFO size register	12-327
0xC410	PERI_USB3_GEVNTADRN_HI	Global event buffer address upper-32-bit register	12-327
0xC414	PERI_USB3_GEVNTADRN_LO	Global event buffer address lower-32-bit register	12-328
0xC418	PERI_USB3_GEVNTSIZN	Global event buffer size register	12-328
0xC41C	PERI_USB3_GEVNTCOUNTN	Global event buffer count register	12-329
0xC610	PERI_USB3_GTXFIFOPRIDEV	Peripheral global TX FIFO DMA priority register	12-329

Offset Address	Register	Description	Page
0xC618	PERI_USB3_GTXFIFOPRIHST	Host global TX FIFO DMA priority register	12-330
0xC61C	PERI_USB3_GRXFIFOPRIHST	Host global RX FIFO DMA priority register	12-330
0xC620	PERI_USB3_GFIFOPRIDBC	Host global performance debug DMA priority register	12-331
0xC624	PERI_USB3_GDMAHLRATIO	High/Low priority ratio register for the host global FIFO DMA	12-331
0xC630	PERI_USB3_GFLADJ	Global frame length adjustment register	12-332
0xC700	PERI_USB3_DCFG	Peripheral configuration register	12-333
0xC704	PERI_USB3_DCTL	Peripheral control register	12-334
0xC708	PERI_USB3_DEVTEN	Peripheral event enable register	12-337
0xC70C	PERI_USB3_DSTS	Peripheral status register	12-338
0xC710	PERI_USB3_DGCMDPAR	Peripheral class command parameter register	12-340
0xC714	PERI_USB3_DGCMD	Peripheral class command register	12-341
0xC718	PERI_USB3_DALEPENA	Peripheral USB endpoint enable register	12-342
0xC810	PERI_USB3_DEPCMDPAR2N	Peripheral endpoint command parameter register 2	12-343
0xC814	PERI_USB3_DEPCMDPAR1N	Peripheral endpoint command parameter register 1	12-343
0xC818	PERI_USB3_DEPCMDPAR0N	Peripheral endpoint command parameter register 0	12-343
0xC81C	PERI_USB3_DEPCMDN	Peripheral physical endpoint command register	12-344

12.10.5 USB3.0 Register Description

PERI_USB3_GSBUSCFG0

PERI_USB3_GSBUSCFG0 is global SoC bus configuration register 0.

Offset Address	Register Name	Total Reset Value
0xC100	PERI_USB3_GSBUSCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	datrdreqinfo				desrdreqinfo				datwrreqinfo				deswrreqinfo				reserved				datbigend	descbigend	reserved		incr256brstena	incr128brstena	incr64brstena	incr32brstena	incr16brstena	incr8brstena	incr4brstena	incrbrstena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	datrdreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Data read request
[27:24]	RW	desrdreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Linked list read request
[23:20]	RW	datwrreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Data write request
[19:16]	RW	deswrreqinfo	AHB-prot/AXI-cache/OCP-ReqInfo Linked list write request
[15:12]	RO	reserved	Reserved
[11]	RW	datbigend	Endian mode for accessing data 0: little endian 1: big endian
[10]	RW	descbigend	Endian mode for accessing the linked list 0: little endian 1: big endian
[9:8]	RO	reserved	Reserved
[7]	RW	incr256brstena	256-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[6]	RW	incr128brstena	128-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[5]	RW	incr64brstena	64-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled

[4]	RW	incr32brstena	32-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[3]	RW	incr16brstena	16-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[2]	RW	incr8brstena	8-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[1]	RW	incr4brstena	4-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled
[0]	RW	incrbrstena	1-beat burst transfer enable for the AHB master INCR 0: disabled 1: enabled

PERI_USB3_GSBUSCFG1

PERI_USB3_GSBUSCFG1 is global SoC bus configuration register 1.

Offset Address	Register Name	Total Reset Value
0xC104	PERI_USB3_GSBUSCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			en1kpage	pipetranslimit				Reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	en1kpage	1 KB boundary select 0: 4 KB boundary 1: 1 KB boundary

[11:8]	RW	pipetranslimit	Number of AXI master outstanding requests 0x0: 1 request 0x1: 2 requests 0x2: 3 requests 0x3: 4 requests … 0xF: 16 requests
[7:0]	RO	reserved	Reserved

PERI_USB3_GTXTHRCFG

PERI_USB3_GTXTHRCFG is a global TX threshold control register.

Offset Address	Register Name	Total Reset Value
0xC108	PERI_USB3_GTXTHRCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		usbtxpktcntsel	reserved	usbtxpktcnt				usbmaxtxburstsize								reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	usbtxpktcntsel	USB TX FIFO threshold select. This field is valid only in super-speed mode. 0: The USB module starts transfer only after all packets are read to the specified TX FIFO. 1: The USB module starts transfer only after specified packets are read to the specified TX FIFO.
[28]	RO	reserved	Reserved
[27:24]	RW	usbtxpktcnt	TX FIFO threshold. The value range is 1−15.
[23:16]	RO	usbmaxtxburstsize	Maximum TX burst size. This field is valid only for the OUT endpoint during bulk transfer, isochronous transfer, or interrupt transfer at a super speed in host mode. The value range is 1−16.
[15:0]	RO	reserved	Reserved

PERI_USB3_GRXTHRCFG

PERI_USB3_GRXTHRCFG is a global RX threshold control register.

Offset Address	Register Name	Total Reset Value
0xC10C	PERI_USB3_GRXTHRCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		usbrxpktcntsel	reserved	usbrxpktcnt				usbmaxrxburstsize				Reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	usbrxpktcntsel	USB RX FIFO threshold select. This field is valid only in super-speed mode. 0: The USB module starts transfer only after all packets are read to the specified RX FIFO. 1: The USB module starts transfer only after specified packets are read to the specified RX FIFO.
[28]	RO	reserved	Reserved
[27:24]	RW	usbrxpktcnt	RX FIFO threshold. The value range is 1−15.
[23:19]	RO	usbmaxrxburstsize	Maximum RX burst size. This field is valid only for the IN endpoint during bulk transfer or interrupt transfer at a super speed in host mode. The value range is 1−16.
[18:0]	RO	reserved	Reserved

PERI_USB3_GCTL

PERI_USB3_GCTL is a global core control register.

Offset Address	Register Name	Total Reset Value
0xC110	PERI_USB3_GCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwrdnscale													masterfiltbypass	bypssetaddr u2rstecn		frmscldwn		prtcapdir		coresoftreset	softipsync	u1u2timerscale	debugattach	ramclksel		scaledown		disscramble	u2exit_lfps	gblhibernationen	dsblclkgtng
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	pwrdnscale	Suspend_clk The Suspend_clk is calculated as follows: GCTL[31:19] x 16 kHz = Suspend_clk **NOTE** 32 kHz < Suspend_clk < 125 MHz
[18]	RW	masterfiltbypass	Filtering select 0: Filtering is enabled when DWC_USB3_EN_BUS_FILTERS is 1. 1: Filtering is disabled regardless of the value of DWC_USB3_EN_BUS_FILTERS.
[17]	RW	bypssetaddr	SetAddress command in device mode 0: The host sends the SetAddress command to the device. 1: The host does not send the SetAddress command to the device. The device reads the value of DCFG[DevAddress] as the address value. Note: This bit is configured only for simulation.
[16]	RW	u2rstecn	Super-speed connection 0: When the super-speed connection fails, the device is in high-speed mode. 1: When the super-speed connection fails, the device waits for more than three cycles. Note: This bit is valid only in device mode.

[15:14]	RW	frmscldwn	SOF/USOF/ITP interval in super-speed or high-speed mode 00: 125 µs 01: 62.5 µs 10: 31.25 µs 11: 15.625 µs The corresponding value needs to be multiplied by 8 in full-speed mode. Maximum packet size of bulk in or bulk out transfer during simulation in xHCI debug mode 00: 1024 bytes 01: 512 bytes 10: 256 bytes 11: 128 bytes
[13:12]	RW	prtcapdir	Port configuration type 00: reserved 01: host configuration 10: device configuration 11: OTG configuration
[11]	RW	coresoftreset	Core soft reset select 0: not reset 1: reset NOTE When the core is soft-reset, all interrupts excluding the interrupts of the following registers are cleared. -GCTL -GUCTL -GSTS -GSNPSID -GGPIO -GUID -GUSB2PHYCFGn -GUSB3PIPECTLn -DCFG -DCTL -DEVTEN -DSTS
[10]	RW	sofitpsync	0: The first port of the UTMI/ULPI PHY is not suspended no matter whether other SS ports are not in the Rx.Detect, SS.Disable, or U3 state. 1: The first port of the UTMI/ULPI PHY is not suspended no matter whether other non-SS ports are not in the non-suspend

			state. **NOTE** This field is valid only when the USB controller is in host mode.
[9]	RW	u1u2timerscale	U1/U2 timer scale-down enable 0: enabled 1: disabled when PERI_USB3_GCTL[5:4] (ScaleDown) is X1
[8]	RW	debugattach	Debug attach signal When this field is set to 1: • After the Ru/Stop bit in the DCTL register is set to 1, the SS controller enters the polling link state without detecting the link of the remote device. • The timeout period for link LFPS polling is infinite. • The timeout period for TS1 polling is infinite.
[7:6]	RW	ramclksel	RAM clock select 00: bus clock 01: PIPE clock 10: PIPE/2 clock 11: reserved **NOTE** In host mode, hardware sets this field to 00 (the ram_clk connects to the bus_clk). Therefore, when the SS port is in P3 state, the PIPE clock is disabled, and the USB 2.0 port does not work.
[5:4]	RW	scaledown	Scale-down timing select In high-speed, full-speed, or low-speed mode: 00: All scale-down timings are disabled, and the actual timings are used for simulation. 01: All scale-down timings excluding the timings related to the following functions are enabled. -Speed enumeration -HNP/SRP -Suspend and resume in host mode 10: Only the scale-down timings related to the suspend and resume functions in device mode are enabled. 11: All scale-down timings are enabled. For the SS mode: In high-speed, full-speed, or low-speed mode: 00: All scale-down timings are disabled, and the actual timings are used for simulation. 01: The SS scale-down timings are enabled, including -The number of TxEq training sequence is reduced to 8. -The LFPS polling burst time is reduced to 100 ns.

			-The LFPS warm reset receive is reduced to 30 µs. 10: TxEq training sequences are not transmitted. 11: All scale-down timings are enabled.
[3]	RW	disscramble	Scrambling enable 1: disabled 0: enabled
[2]	RW	u2exit_lfps	U2 state exit signal 0: The link layer considers the 248 ns LFPS signal as an active U2 state exit signal. 1: The link layer waits 8 µs after detecting an active U2 state exit signal.
[1]	RW	gblhibernationen	Global hibernation enable 0: disabled. When the PMU accepts status switching between D0 and D3, the internal status of the core is not retained or restored. 1: enabled
[0]	RW	dsblclkgtng	Internal clock gating enable 0: enabled 1: disabled when the core is in LPM mode NOTE This field can be set to 1 after power-on reset.

PERI_USB3_GSTS

PERI_USB3_GSTS is a global status register.

Offset Address	Register Name	Total Reset Value
0xC118	PERI_USB3_GSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cbelt												Reserved								otg_ip	bc_ip	adp_ip	host_ip	device_ip	csrtimeout	buserraddrvld	reserved			curmod	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	cbelt	Minimum value among all received device BELT values and the BELT value configured by running the Set Latency Tolerance Value command in host mode

[19:11]	RO	reserved	Reserved
[10]	RO	otg_ip	Indication that an OTG-related interrupt in the OEVT register is waiting for handling 0: There is no indication. 1: There is an indication.
[9]	RO	bc_ip	Indication that a BC-related interrupt in the BCEVT register is waiting for handling 0: There is no indication. 1: There is an indication.
[8]	RO	adp_ip	Indication that an ADP-related interrupt in the ADPEVT register is waiting for handling 0: There is no indication. 1: There is an indication.
[7]	RO	host_ip	Indication that an xHCI-related interrupt in the host event queue is waiting for handling 0: There is no indication. 1: There is an indication.
[6]	RO	device_ip	Indication that an xHCI-related interrupt in the device event queue is waiting for handling 0: There is no indication. 1: There is an indication.
[5]	RO	csrtimeout	Indication that the duration of accessing registers by software exceeds the time defined by DWC_USB3_CSR_ACCESS_TIMEOUT 0: There is no indication. 1: There is an indication.
[4]	RO	buserraddrvld	GBUSERRADDR register validity indicator and start address for the error position 0: There is no indication. 1: There is an indication.
[3:2]	RO	reserved	Reserved
[1:0]	RO	curmod	Current working mode 00: device mode 01: host mode Other values: reserved

PERI_USB3_GUCTL1

PERI_USB3_GUCTL1 is global user control register 1.

Offset Address	Register Name	Total Reset Value
0xC11C	PERI_USB3_GUCTL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																														ovrld_l1_susp_com	loa_filter_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	ovrld_l1_susp_com	If this bit is set to 1, the utmi_l1_suspend_com_n signal will be replaced by the utmi_sleep_n signal. Generally this bit is set to 1 when the PHY enters the L1 sleep mode and stops supplying the clock.
[0]	RW	loa_filter_en	Port disable status detection. When this field is set to 1, the controller sends three consecutive cycles to detect the port status before the port is disabled.

PERI_USB3_GGPIO

PERI_USB3_GGPIO is a global GPIO register.

Offset Address	Register Name	Total Reset Value
0xC124	PERI_USB3_GGPIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gpo																gpi															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	gpo	Drive value of gp_o[15:0]
[15:0]	RO	gpi	Read value of gp_i[15:0]

PERI_USB3_GUID

PERI_USB3_GUID is a global user ID register.

Offset Address	Register Name	Total Reset Value
0xC128	PERI_USB3_GUID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Userid																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	userid	User information including the system version and hardware configuration

PERI_USB3_GUCTL

PERI_USB3_GUCTL is a global user control register.

Offset Address	Register Name	Total Reset Value
0xC12C	PERI_USB3_GUCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	refclkper										noextrdl_	reserved			sprsctrltransen	resbwhseps	cmdevaddr	usbhstlnautoretryen	enoverlapchk	extcapsupten	Csr	dtct	dtft									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	refclkper	Reference clock (ref_clk), in ns For example, if the ref_clk is 125 MHz, this field is set to 8 ns (1/125 MHz).
[21]	RW	noextrdl_	Extra delay between the SOF packet and the first packet 0: The host transmits the first packet 2 ms later after the SOF packet. 1: The host transmits the first packet after the SOF packet without delay.
[20:18]	RW	reserved	Reserved

[17]	RW	sprsctrltransen	Disperse control transfer enable 0: disabled 1: enabled Some devices respond to the control transfer at an extremely slow speed. The devices are abnormal if multiple transfers are performed in a frame or microframe. When this field is set to 1, the host controller disperses a control transfer in multiple frames or microframes.
[16]	RW	resbwhseps	85% of the bandwidth is reserved for high-speed periodic endpoints. This field is valid only in host mode or for host operations in DRD mode.
[15]	RW	cmdevaddr	Device address mode 0: The device address is the slot ID. 1: The device address is incremented based on the address allocation command of each device.
[14]	RW	usbhstlnautoretryen	Automatic retransmission enable for host inputs 0: disabled If an error occurs during host input transfer, the host automatically replies an ACK indicating termination to the device (Retry = 1 and NumP = 0). 1: enabled If automatic retransmission is enabled and an error occurs during host input transfer, the host automatically replies an ACK not indicating termination to the device (Retry = 1 and NumP != 0).
[13]	RW	enoverlapchk	LFPS overlap signal detection enable 0: The LFPS overlap signal is not detected. 1: The LFPS overlap signal is detected to avoid glitches.
[12]	RW	extcapsupten	Reserved
[11]	RW	csr	Extra delay inserted between full-speed BULKOUT transfers 1: not insert 2: insert
[10:9]	RW	dtct	Rough timeout period that the device responds to the host. If this field is set to 0, the timeout period is defined by the DTFT; if this field is not 0, the timeout period is as follows: 00: 0 μs 01: 500 μs 10: 1.5 ms 11: 6.5 ms
[8:0]	RW	dtft	Exact timeout period that the device responds to the host. This field is valid when the DTCT is 0. The exact timeout period (T) is calculated as follows: T = DTFT x 256 x 8 μs

PERI_USB3_GBUSERRADDR_HI

PERI_USB3_GBUSERRADDR_HI is a global bus error address upper-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC130	PERI_USB3_GBUSERRADDR_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Busaddrhi																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	busaddrhi	Upper 32 bits of the error address NOTE This field is valid only when GSTS[BusErrAddrVld] is 1. This field is cleared only during reset. Only the AHB and AXI bus configurations are supported.

PERI_USB3_GBUSERRADDR_LO

PERI_USB3_GBUSERRADDR_LO is a global bus error address lower-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC134	PERI_USB3_GBUSERRADDR_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Busaddrlo																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	busaddrlo	Lower 32 bits of the error address NOTE This field is valid only when GSTS[BusErrAddrVld] is 1. This field is cleared only during reset. Only the AHB and AXI bus configurations are supported.

PERI_USB3_GPRTBIMAP_HI

PERI_USB3_GPRTBIMAP_HI is an SS port-bus mapping upper-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC138	PERI_USB3_GPRTBIMAP_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved

PERI_USB3_GPRTBIMAP_LO

PERI_USB3_GPRTBIMAP_LO is an SS port-bus mapping lower-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC13C	PERI_USB3_GPRTBIMAP_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												binumn			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	binumn	ID of the currently connected SS bus

PERI_USB3_GPRTBIMAP_HS_HI

PERI_USB3_GPRTBIMAP_HS_HI is an HS port-bus mapping upper-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC180	PERI_USB3_GPRTBIMAP_HS_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved

PERI_USB3_GPRTBIMAP_HS_LO

PERI_USB3_GPRTBIMAP_HS_LO is an HS port-bus mapping lower-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC184	PERI_USB3_GPRTBIMAP_HS_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												binumn			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	binumn	ID of the currently connected HS bus

PERI_USB3_GPRTBIMAP_FS_HI

PERI_USB3_GPRTBIMAP_FS_HI is an FS port-bus mapping upper-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC188	PERI_USB3_GPRTBIMAP_FS_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved

PERI_USB3_GPRTBIMAP_FS

PERI_USB3_GPRTBIMAP_FS is an FS port-bus mapping lower-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC18C	PERI_USB3_GPRTBIMAP_FS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												binumn			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3:0]	RW	binumn	ID of the currently connected FS bus

PERI_USB3_GUSB2PHYCFGN

PERI_USB3_GUSB2PHYCFGN is a global USB 2.0 PHY configuration register.

Offset Address	Register Name	Total Reset Value
0xC200	PERI_USB3_GUSB2PHYCFGN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy_soft_rst	u2_freeclk_exists	reserved										ulpi_ext_vbus_indicator	ulpi_ext_vbus_drv	reserved		ulpi_auto_res	reserved	usbtrdtim				xcvrdly	enblslpm	physel	susphy	fsintf	ulpi_utmi_sel	phyif	toutcal		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	phy_soft_rst	UTMI PHY soft-reset by triggering the usb2phy_reset signal. In this case, the ULPI PHY is not reset, because it is reset by configuring the FunctionControl[Reset]. When the core is reset, the core automatically configures vcc_reset_n, xHCI_USBCMD[hcrst], DCTL[SoftReset], or GCTL[SoftReset] to implement reset.
[30]	RW	u2_freeclk_exists	Whether the USB 2.0 PHY provides the free clock 0: no 1: yes
[29:19]	RO	reserved	Reserved
[18]	RW	ulpi_ext_vbus_indicator	ULPI external Vbus indicator 0: The PHY uses the internal Vbus as the comparison voltage. 1: The PHY uses the external Vbus as the comparison voltage.
[17]	RW	ulpi_ext_vbus_drv	ULPI external Vbus driver 0: The PHY uses the internal Vbus voltage driver. 1: The PHY uses the external Vbus voltage driver.
[16]	RO	reserved	Reserved
[15]	RW	ulpi_auto_res	ULPI automatic resume enable 0: disabled

			1: enabled
[14]	RO	reserved	Reserved
[13:10]	RW	usbtrdtim	USB 2 turnaround time, that is, response time after the MAC requests the packet FIFO controller (PFC) to fetch data from the DFIFO (SPRAM) 0x5 for the 16-bit UTMI+ interface 0x9 for the 8-bit UTMI+ or ULPI interface
[9]	RW	xcvrdly	TX/RX delay select. When this bit is set to 1, the delay of 2.5 μs is added between the time Transceiver Select is set to 00 (high speed) and the time TxValid is 0 to transmit the chirp-K handshake signal.
[8]	RW	enblslpm	utmi_sleep_n/utmi_l1_suspend_n signal enable 0: The utmi_sleep_n and utmi_l1_suspend_n signals do not connect to the PHY. 1: The utmi_sleep_n and utmi_l1_suspend_n signals connect to the PHY.
[7]	RW	physel	PHY interface type 0: USB 2.0 high-speed UTMI+ or ULPI PHY interface 1: USB 1.1 full-speed serial interface This bit is set to 1 when it is write-only.
[6]	RW	susphy	USB 2.0 HS/FS/LS PHY suspend 0: not suspended 1: suspended Note: In DRD mode, set this bit to 1 after the core is initialized.
[5]	RW	fsintf	Type of the FS PHY serial interface 0: 6-pin unidirectional FS serial transfer interface 1: 3-pin bidirectional FS serial transfer interface When this bit is read-only, the return value is 0.
[4]	RW	ulpi_utmi_sel	Type of the HS PHY interface 0: UTMI+ 1: ULPI
[3]	RW	phyif	Data width of the UTMI interface 0: 8 bits 1: 16 bits

[2:0]	RW	toutcal	HS/FS timeout calibration The corresponding bit time is added to each PHY clock. HS mode One 30 MHz PHY clock = 16-bit times One 60 MHz PHY clock = 8-bit times FS mode One 30 MHz PHY clock = 0.4-bit times One 60 MHz PHY clock = 0.2-bit times One 48 MHz PHY clock = 0.25-bit times

PERI_USB3_GUSB3PIPECTLN

PERI_USB3_GUSB3PIPECTLN is a global USB 3.0 PIPE control register.

Offset Address	Register Name	Total Reset Value
0xC2C0	PERI_USB3_GUSB3PIPECTLN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy_soft_rst	reserved	u2ssinactp3ok	disrxdetp3	ux_exit_in_px	ping_enhancement_en	u1u2exitfail_to_recov	request_p1p2p3	startrxdetu3rxdet	disrxdetu3rxdet	delayp1p2p3		delay_phy_powerchange	suspend_en	datwidth		abortrxdetinu2	skiprxdet	lfps_p0_align	p3p2_tran_ok	p3exsigp2	lfps_filter	polling_lfps_control	reserved	txswing	txmargin		txdeemphasis		elastic_buffer_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	phy_soft_rst	USB 3.0 soft reset 0: not reset 1: reset
[30]	RW	hstprtcmpl	Reserved
[29]	RW	u2ssinactp3ok	PHY status select in U2/SSInactive status 0: The PHY enters the P2 status. 1: The PHY enters the P3 status.

[28]	RW	disrxdetp3	RX detection enable in P3 status 0: If the PHY is in P3 status and the core requires RX detection, the core performs RX detection in P3 status. 1: If the PHY is in P3 status and the core requires RX detection, the core switches the PHY status to P2 and then performs RX detection. After detection is complete, the core switches the PHY status to P3.
[27]	RW	ux_exit_in_px	PHY status select when the core status is switched 0: The PHY is in P0 status when the core exits the U1, U2, or U3 status. 0: The PHY is in P1, P2, or P3 status when the core exits the U1, U2, or U3 status respectively. NOTE Set this field to 0 when the Synopsys PHY is used.
[26]	RW	ping_enhancement_en	Timeout period changed from 500 ms to 300 ms for the ping command of the downlink port U1 0: not changed 1: changed NOTE Set this field to 0 when the Synopsys PHY is used.
[25]	RW	u1u2exitfail_to_recov	Signal for exiting the P3 status in P2 status. When this field is set to 1, the core sets the PHY status to P2 before transmitting the handshake signal for exiting the U3 status.
[24]	RW	request_p1p2p3	When the core status is switched from U0 to U1, U2, or U3, the core always requests the PHY to switch the status from P0 to P1, P2, or P3 respectively. 0: not switched 1: switched NOTE Set this field to 1 when the Synopsys PHY is used.
[23]	RW	startrxdetu3rxdet	This bit is fixed at 0.
[22]	RW	disrxdetu3rxdet	This bit is fixed at 0.
[21:19]	RW	delayp1p2p3	Delay when the status is switched from P0 to P1, P2, or P3 When the core enters the U1, U2, or U3 status, the time when the P0 status is switched to P1, P2, or P3 is prolonged until Pipe3_RxValid is set to 0 or an 8B10B error occurs. NOTE This function is valid only when bit 18 is set to 1.

[18]	RW	delay_phy_powerchange	PHY status switch delay 0: When the core status is switched from U0 to U1, U2, or U3, the PHY enters the P1, P2, or P3 status without detecting the values of Pipe3_RxElecIlde and pipe3_RxValid. 1: When the core status is switched from U0 to U1, U2, or U3, the time when the PHY enters the P1, P2, or P3 status is delayed until the values of Pipe3_RxElecIlde and pipe3_RxValid are 0. **NOTE** Set this field to 1 when the Synopsys PHY is used.
[17]	RW	suspend_en	USB 3.0 PHY suspend enable 0: not suspended 1: suspended **NOTE** In DRD mode, set this field to 1 after the core is initialized.
[16:15]	RW	datwidth	Data width of the PIPE interface 00: 32 bits 01: 16 bits 10: 8 bits Other: Reserved
[14]	RW	abortrxdetinu2	RX detection abort in U2 status 0: not abort 1: abort When this field is set to 1, the connection status is U2, and the core receives a U2 status exit signal from a remote device, RX detection is not performed. **NOTE** Set this field to 0 when the Synopsys PHY is used.
[13]	RW	skiprxdet	RX detection skip status 0: not skip 1: skip When this field is set to 1, RX detection is skipped if pipe3_RxElecIdle is pulled down.
[12]	RW	lfps_p0_align	When the controller exits the U1, U2, or U3 status, transmitting the LFPS signal is stopped on the clock edge of the PHY P0 status request signal. Otherwise, the LFPS signal is transmitted one cycle earlier. When the PHY status is switched from P1 or P2 to P0, the controller requests data transfer two clock cycles later after the PHY sets PhyStatus.

[11]	RW	p3p2_tran_ok	P2/P3 status switch 0: The PHY enters the intermediate status P0 each time when the PHY status is switched between P2 and P3. 1: The PHY is switched from P2 to P3 or from P3 to P2 without entering the intermediate status P0. NOTE Set this field to 0 when the Synopsys PHY is used.
[10]	RW	p3exsigp2	P3 exit status select If this bit is set to 1, the PHY state is switched from P3 to P2 when the core exits from the U3 state. If this bit is set to 0, the PHY state is switched from P3 to P1 or P0 when the core exits from the U3 state. NOTE Set this field to 0 when the Synopsys PHY is used.
[9]	RW	lfps_filter	LFPS filter 0: not filter 1: filter When this bit is set to 1, the controller filters the LFPS signals from the PHY unless pipe3_Rxelecidle and pipe3_RxValid are deasserted.
[8]	RW	polling_lfps_control	LFPS polling control after RX detection 0: (default value) LFPS polling starts 400 µs later after RX detection. 1: LFPS polling starts after RX detection without delay.
[7]	RO	reserved	Reserved
[6]	RW	txswing	TX swing of the PIPE interface
[5:3]	RW	txmargin	TX margin of the PIPE interface
[2:1]	RW	txdeemphasis	TX preemphasis of the PIPE interface
[0]	RW	elastic_buffer_mode	Elastic buffer mode enable 0: disabled 1: enabled

PERI_USB3_GTXFIFOSIZN

PERI_USB3_GTXFIFOSIZN is a global TX FIFO size register.

Offset Address	Register Name	Total Reset Value
0xC304	PERI_USB3_GTXFIFOSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	txfstaddr_n																txfdep_n															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	txfstaddr_n	Start address for the TX FIFO *n* RAM in the memory
[15:0]	RW	txfdep_n	TX FIFO depth Minimum value: 32 MDWIDTH-bit words Maximum value: 32768 MDWIDTH-bit words

PERI_USB3_GRXFIFOSIZN

PERI_USB3_GRXFIFOSIZN is a global RX FIFO size register.

Offset Address	Register Name	Total Reset Value
0xC384	PERI_USB3_GRXFIFOSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxfstaddr_n																rxfdep_n															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rxfstaddr_n	Start address for the RX FIFO *n* RAM in the memory
[15:0]	RW	rxfdep_n	RX FIFO depth Minimum value: 32 MDWIDTH-bit words Maximum value: 32768 MDWIDTH-bit words

PERI_USB3_GEVNTADRN_HI

PERI_USB3_GEVNTADRN_HI is a global event buffer address upper-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC410	PERI_USB3_GEVNTADRN_HI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	evntadrhi																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWSC	evntadrhi	Upper 32-bit address of the event buffer

PERI_USB3_GEVNTADRN_LO

PERI_USB3_GEVNTADRN_LO is a global event buffer address lower-32-bit register.

Offset Address	Register Name	Total Reset Value
0xC414	PERI_USB3_GEVNTADRN_LO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	evntadrlo																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWSC	evntadrlo	Lower 32-bit address of the event buffer

PERI_USB3_GEVNTSIZN

PERI_USB3_GEVNTSIZN is a global event buffer size register.

Offset Address	Register Name	Total Reset Value
0xC418	PERI_USB3_GEVNTSIZN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	evntintmask	reserved															evntsiz															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	evntintmask	Event interrupt mask

[30:16]	RO	reserved	Reserved
[15:0]	RW	evntsiz	Event buffer size (in byte)

PERI_USB3_GEVNTCOUNTN

PERI_USB3_GEVNTCOUNTN is a global event buffer count register.

Offset Address	Register Name	Total Reset Value
0xC41C	PERI_USB3_GEVNTCOUNTN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				evntcount			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RWSC	evntcount	When this field is read, the number of valid events in the event buffer is returned; when it is written, the hardware automatically decreases the written count value.

PERI_USB3_GTXFIFOPRIDEV

PERI_USB3_GTXFIFOPRIDEV is a peripheral global TX FIFO DMA priority register.

Offset Address	Register Name	Total Reset Value
0xC610	PERI_USB3_GTXFIFOPRIDEV	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							device_txfifo_priority
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	device_txfifo_priority	Priority of the device TX FIFO 0: low 1: high

PERI_USB3_GTXFIFOPRIHST

PERI_USB3_GTXFIFOPRIHST is a host global TX FIFO DMA priority register.

Offset Address	Register Name	Total Reset Value
0xC618	PERI_USB3_GTXFIFOPRIHST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																															host_txfifo_priority
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	host_txfifo_priority	Priority of the host TX FIFO 0: low 1: high

PERI_USB3_GRXFIFOPRIHST

PERI_USB3_GRXFIFOPRIHST is a host global RX FIFO DMA priority register.

Offset Address	Register Name	Total Reset Value
0xC61C	PERI_USB3_GRXFIFOPRIHST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																															host_rxfifo_priority
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	host_rxfifo_priority	Priority of the host RX FIFO 0: low 1: high

PERI_USB3_GFIFOPRIDBC

PERI_USB3_GFIFOPRIDBC is a host global performance debug DMA priority register.

Offset Address	Register Name	Total Reset Value
0xC620	PERI_USB3_GFIFOPRIDBC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																														host_dbc_dma_priority	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	host_dbc_dma_priority	Priority of the host DBC DMA 00: low 01: normal 10: high Other: reserved

PERI_USB3_GDMAHLRATIO

PERI_USB3_GDMAHLRATIO is a high/low priority ratio register for the host global FIFO DMA.

Offset Address	Register Name	Total Reset Value
0xC624	PERI_USB3_GDMAHLRATIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				hst_rxfifo_dma_hilo_priority_ratio				reserved				hst_txfifo_dma_hilo_priority_ratio			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

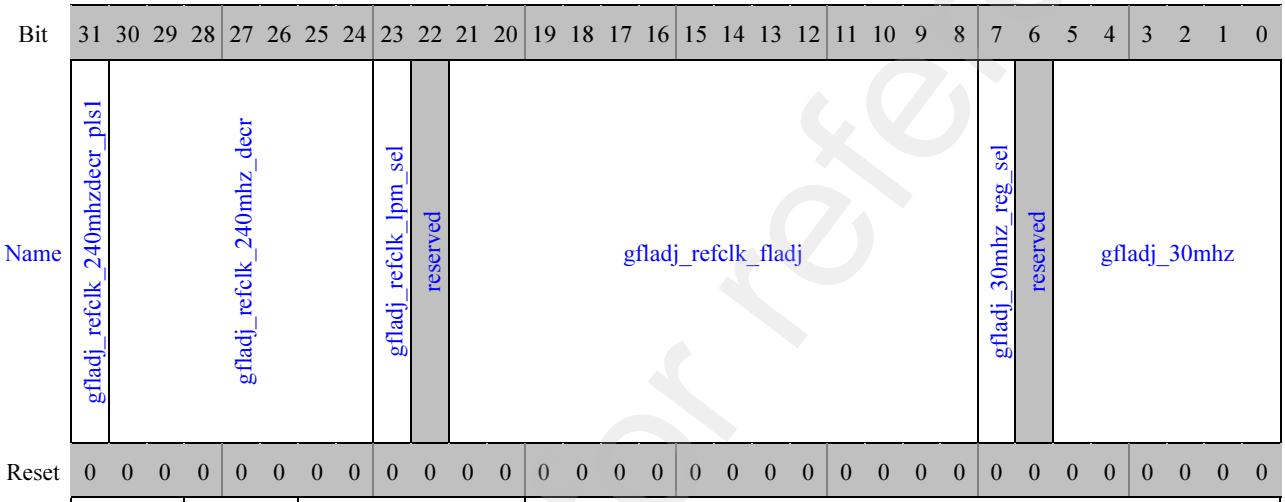
Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	hst_rxfifo_dma_hilo_priority_ratio	High/Low priority ratio of the host RX FIFO DMA

[7:5]	RO	reserved	Reserved
[4:0]	RW	hst_txfifo_dma_hilo_priority_ratio	High/Low priority ratio of the host TX FIFO DMA

PERI_USB3_GFLADJ

PERI_USB3_GFLADJ is a global frame length adjustment register.

Offset Address	Register Name	Total Reset Value
0xC630	PERI_USB3_GFLADJ	0x0000_0000



Bits	Access	Name	Description
[31]	RW	gfladj_refclk_240mhzdecr_pls1	Precision of GFLADJ_REFCLK_240MHZ_DECR/ref_frequency 0: The remainder is less than 0.5. 1: The remainder is greater than or equal to 0.5.
[30:24]	RW	gfladj_refclk_240mhz_decr	Counter value obtained after 240 is divided by ref_clk_frequency GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency
[23]	RW	gfladj_refclk_lpm_sel	SOF/ITP count clock select If this bit is set to 1, the ref_clk is the count clock.
[22]	RO	reserved	Reserved
[21:8]	RW	gfladj_refclk_fladj	SOF/ITP calibration value when bit 23 is 1 FLADJ_REF_CLK_FLADJ = [(125000/ref_clk_period_integer) − (125000/ref_clk_period)] x ref_clk_period
[7]	RW	gfladj_30mhz_reg_sel	SOF/ITP frame length tune signal select 0: The controller tunes the SOF/ITP frame length based on the value of input signal fladj_30mhz_reg. 1: The controller calibrates the SOF/ITP based on the value of PERI_USB3_GFLADJ[gfladj_30mhz].

[6]	RO	reserved	Reserved
[5:0]	RW	gfladj_30mhz	When bit[7] is 1 and the SOF/ITP count clock is the UTMI/ULPI clock, the controller calibrates the SOF/ITP based on this field value.

PERI_USB3_DCFG

PERI_USB3_DCFG is a peripheral configuration register.

Offset Address	Register Name	Total Reset Value
0xC700	PERI_USB3_DCFG	0x0008_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ignore_stream_pp	lpm_capable	number_of_receive_buffers						interrupt_number				reserved				device_address						device_speed		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RW	ignore_stream_pp	Packet pending bit ignore 0: not ignored 1: ignored
[22]	RW	lpm_capable	LPM function enable 0: enabled 1: disabled
[21:17]	RW	number_of_receive_buffers	ID of the RX buffer that is returned in the ACK TP
[16:12]	RW	interrupt_number	ID of the non-endpoint interrupt that is generated by the device
[11:10]	RO	reserved	Reserved
[9:3]	RW	device_address	Device address. The device address is configured each time the device receives the **SetAddress** command. This field is cleared after USB reset.
[2:0]	RW	device_speed	Device transfer rate select 000: high speed 001: full speed

			100: super speed Other values: reserved

PERI_USB3_DCTL

PERI_USB3_DCTL is a peripheral control register.

Offset Address	Register Name	Total Reset Value
0xC704	PERI_USB3_DCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	run_stop	soft_core_reset	reserved		hird_threshold				appl1res			reserved	keepconnect	l1_hibernation_en	controller_restore_state	controller_save_state	reserved			initiate_u2_enable	accept_u2_enable	initiate_u1_enable	accept_u1_enable		ulstchngraq				test_control			reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	run_stop	Device start/stop select The device is started after software writes 1 to this bit. To stop the device, stop all transfers and then write 0 to this bit. This bit is configured in the following cases: 1. Software must write 1 to this bit to initialize the device controller after POR; otherwise, the device controller is unaware that the host has been connected. 2. If software needs to restart the connection when a soft disconnection event occurs or a disconnection event is detected, bit[8:5] must be set to 5 before this bit is set to 1. 3. When the USB is in low-power mode and the USB has two power domains, the core power domain is disabled if software writes 0 to this bit. This bit is set to 1 after software restarts the core power domain and device controller.
[30]	RWSC	soft_core_reset	Core soft reset The configuration of this bit has effect on the interrupts and registers of all clock domains. 1. All interrupts are cleared, and all registers are reset except the following ones: • GCTL • GUCTL

			• GSTS • GSNPSID • GGPIO • GUID • GUSB2PHYCFGn registers • GUSB3PIPECTLn registers • DCFG • DCTL • DEVTEN • DSTS 2. All state machines are restored to the idle state, and all FIFOs are cleared. 3. All transfers on the SoC bus are stopped immediately.
[29]	RO	reserved	Reserved
[28:24]	RW	hird_threshold	HIRD threshold The core generates the utmi_l1_suspend_n signal or utmi_sleep_n signal when the corresponding condition is met. 1. The core generates the utmi_l1_suspend_n signal in the L1 state and switches the PHY to the deep low-power mode when the following conditions are met: • The HIRD value is greater than or equal to HIRD_Thres bit[3:0]. • HIRD_Thres bit[4] is 1. 2. The core generates the utmi_sleep_n signal in the L1 state when the following conditions are met: • The HIRD value is less than HIRD_Thres bit[3:0]. • HIRD_Thres bit[4] is 0.
[23]	RW	appl1res	LPM response configuration When PERI_USB3_DCFG[lpm_capable] is 0, the core does not respond. When PERI_USB3_DCFG[lpm_capable] is 1, the LPM response is as follows: 0: The ACK is returned if the LPM reception/transmission is successful when the following conditions are met: • No check error occurs. • The valid message "bLinkState = 0001B (L1)" is received. • There is no remaining data in the TX FIFFO and the OUT endpoint is not in the flow controller state (except the NYET). 1: The ACK is returned if the LPM reception/transmission is successful when the following conditions are met: • No check error occurs. • The valid message "bLinkState = 0001B (L1)" is received.
[22:20]	RO	reserved	Reserved

[19]	RW	keepconnect	Connection status hold If this bit is set to 1 and the run_stop bit is 0, all related models are saved or restored. In addition, if the link enters the U3 or L2 state, the hibernation request event is enabled.
[18]	RW	l1_hibernation_en	When the keepconnect bit is 1 and this bit is set to 1, if L1 is enabled and the HIRD value is greater than the threshold configured in the hird_threshold bit, the device core generates a hibernation request event.
[17]	RW	controller_restore_state	Controller recovery status After software writes 1 to this bit, the controller immediately sets PERI_USB3_DSTS[rss] to 1. PERI_USB3_DSTS[rss] is set to 0 after the recovery is complete. Note: The value 0 is returned when this bit is read.
[16]	RW	controller_save_state	Controller save status After software writes 1 to this bit, the controller immediately sets PERI_USB3_DSTS[sss] to 1. PERI_USB3_DSTS[sss] is set to 0 after the controller is saved. Note: The value 0 is returned when this bit is read.
[15:13]	RO	reserved	Reserved
[12]	RW	initiate_u2_enable	U2 initialization enable 0: not initialized 1: initialized
[11]	RW	accept_u2_enable	U2 state enable 0: The core refuses to enter the U1 state unless Force_LinkPM_Accep is 1. 1: If no user-end device is waiting, the core agrees to enter the U2 state. Note: Hardware automatically clears this bit after USB reset.
[10]	RW	initiate_u1_enable	U1 initialization enable 0: not initialized 1: initialized
[9]	RW	accept_u1_enable	U1 state enable 0: The core refuses to enter the U1 state unless Force_LinkPM_Accep is 1. 1: If no user-end device is waiting, the core agrees to enter the U1 state. Note: Hardware automatically clears this bit after USB reset.
[8:5]	WO	ulstchngraq	USB/Link state switch request. Software initiates the corresponding state switch request by configuring this field. In SS mode: 0x0: no action

			0x4: SS.Disabled 0x5: Rx.Detect 0x6: SS.Inactive 0x8: recovery 0xA: compliance Other values: reserved In HS, FS, or LS mode: 0x8: remote wakeup request Other values: reserved
[4:1]	RW	test_control	Test control 0x0: The test mode is disabled. 0x1: Test_J mode 0x2: Test_K mode 0x3: Test_SE0_NAK mode 0x4: Test_Packet mode 0x5: Test_Force_Enable Other values: reserved
[0]	RO	reserved	Reserved

PERI_USB3_DEVTEN

PERI_USB3_DEVTEN is a peripheral event enable register.

Offset Address	Register Name	Total Reset Value
0xC708	PERI_USB3_DEVTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						erratic_error_event_enable	reserved	sof_en	u31211_susp_en	hibernation_req_evt_en	wkup_evt_en	ulst_cng_en	connect_done_en	usbrst_en	disconn_evt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved

[9]	RW	erratic_error_event_enable	Irregular error event enable 0: disabled 1: enabled
[8]	RO	reserved	Reserved
[7]	RW	sof_en	SOF packet enable 0: disabled 1: enabled
[6]	RW	u3l2l1_susp_en	U3/L2-L1 suspend event enable 0: disabled 1: enabled
[5]	RW	hibernation_req_evt_en	Hibernation request enable 0: disabled 1: enabled
[4]	RW	wkup_evt_en	Recovery/Remote wakeup detection event enable 0: disabled 1: enabled
[3]	RW	ulst_cng_en	USB/Link state switch event enable 0: disabled 1: enabled
[2]	RW	connect_done_en	Connection completion enable 0: disabled 1: enabled
[1]	RW	usbrst_en	USB reset enable 0: disabled 1: enabled
[0]	RW	disconn_evt_en	Disconnection detection enable 0: disabled 1: enabled

PERI_USB3_DSTS

PERI_USB3_DSTS is a peripheral status register.

Offset Address	Register Name	Total Reset Value
0xC70C	PERI_USB3_DSTS	0x0012_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		dcnrd	reserved			rss	sss	core_idle	devctrlhlt	usb_lnk_st		reserved		soffn														connect_spd			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	dcnrd	Indication that device controller is not ready. The state of the controller is being switched after the controller exits the hibernation state.
[28:26]	RO	reserved	Reserved
[25]	RO	rss	Recovery state This bit is set to 0 after the controller completes the recovery operation.
[24]	RO	sss	Save status This bit is set to 0 after the controller completes the save operation.
[23]	RO	core_idle	Core idle state This bit indicates that the core completes all transfers of the RX FIFO data to the system memory, all linked lists are output, and all event counters are reset to 0.
[22]	RO	devctrlhlt	Device controller suspend This bit is set to 0 when PERI_USB3_DCTL[run_stop] is 1. The core writes 1 to this bit after software writes 0 to PERI_USB3_DCTL[run_stop], the core is in idle state, and the disconnection operation is complete at the next lower layer.
[21:18]	RO	usb_lnk_st	USB/Link status In SS mode: 0x0: U0 0x1: U1 0x2: U2 0x3: U3 0x4: SS_DIS 0x5: RX_DET

			0x6: SS_INACT 0x7: POLL 0x8: RECOV 0x9: HRESET 0xa: CMPLY 0xb: LPBK 0xf: resume/reset Other values: reserved In HS, FS, or LS mode: 0x0: on status 0x2: sleep (L1) status 0x3: suspend (L2) status 0x4: disconnected status (default status) 0x5: early suspend status (valid only when the hibernation function is disabled) 0xe: reset (valid only when the hibernation function is enabled) 0xf: resume (valid only when the hibernation function is enabled) Other values: reserved
[17]	RO	reserved	Reserved
[16:3]	RO	soffn	SOF frame/microframe number In HS mode: Bit[16:6] indicate the number of frames. Bit[5:3] indicate the number of microframes. In FS mode: Bit[16:14] are reserved. Bit[13:3] indicate the number of frames.
[2:0]	RO	connect_spd	Connection speed indicator 000: high speed (the PHY clock frequency is 30 MHz or 60 MHz) 001: full speed (the PHY clock frequency is 30 MHz or 60 MHz) 010: low speed (the PHY clock frequency is 6 MHz) 011: low speed (the PHY clock frequency is 48 MHz) 100: super speed (the PHY clock frequency is 125 MHz or 250 MHz)

PERI_USB3_DGCMDPAR

PERI_USB3_DGCMDPAR is a peripheral class command parameter register.

Offset Address	Register Name	Total Reset Value
0xC710	PERI_USB3_DGCMDPAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter31_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter31_0	Peripheral class command parameter

PERI_USB3_DGCMD

PERI_USB3_DGCMD is a peripheral class command register.

Offset Address	Register Name	Total Reset Value
0xC714	PERI_USB3_DGCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cmd_status	reserved				cmdact	reserved	cmdloc	reserved				cmdtyp			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	cmd_status	Command status 0: The device controller has successfully processed the command. 1: An error occurs when the device controller processes the command.
[14:11]	RO	reserved	Reserved
[10]	RWSC	cmdact	Software sets this bit to 1 to enable the device controller to execute the generated command. This bit is set to 0 after the controller executes the command.
[9]	RO	reserved	Reserved
[8]	WO	cmdloc	Command completion interrupt Note: This bit is set to 1 when PERI_USB3_DCTL[run_stop] is 0.
[7:4]	RO	reserved	Reserved
[3:0]	RW	cmdtyp	Command type

			0x0: reserved 0x1: Configure the endpoint. 0x2: Configure the endpoint transfer source. 0x3: Obtain the endpoint status. 0x4: Set the suspend state. 0x5: Clear the suspend state. 0x6: Start the transfer. 0x7: Update the transfer. 0x8: End the transfer. 0x9: Start the new configuration. Other values: reserved

PERI_USB3_DALEPENA

PERI_USB3_DALEPENA is a peripheral USB endpoint enable register.

Offset Address	Register Name	Total Reset Value
0xC718	PERI_USB3_DALEPENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usbactep																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	usbactep	Whether the USB port is valid for the current configuration and interface. Each of the 32 USB endpoints (input endpoints 0−15 and output endpoints 0−15) is controlled by one bit. The even bits control the output endpoints, and the odd bits control the input endpoints. For example: Bit[0]: USB output endpoint 0 Bit[1]: USB input endpoint 0 Bit[2]: USB output endpoint 1 Bit[3]: USB input endpoint 1 Bit 0 and bit 1 must be configured so that the control endpoints in the physical endpoints can be enabled after USB reset. When the USB reset is detected, the application software clears the bits corresponding to all endpoints except output endpoint 0 and input endpoint 0. When the requirements on register configuration and interface configuration are received, the program sets the endpoint register and the corresponding bits of this register.

PERI_USB3_DEPCMDPAR2N

PERI_USB3_DEPCMDPAR2N is peripheral endpoint command parameter register 2.

Offset Address	Register Name	Total Reset Value
0xC810	PERI_USB3_DEPCMDPAR2N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter2	Peripheral physical endpoint command parameter register 2. This register must be configured before the command is executed.

PERI_USB3_DEPCMDPAR1N

PERI_USB3_DEPCMDPAR1N is peripheral endpoint command parameter register 1.

Offset Address	Register Name	Total Reset Value
0xC814	PERI_USB3_DEPCMDPAR1N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter1	Peripheral physical endpoint command parameter register 1. This register must be configured before the command is executed.

PERI_USB3_DEPCMDPAR0N

PERI_USB3_DEPCMDPAR0N is peripheral endpoint command parameter register 0.

Offset Address	Register Name	Total Reset Value
0xC818	PERI_USB3_DEPCMDPAR0N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	parameter0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	parameter0	Peripheral physical endpoint command parameter register 0. This register must be configured before the command is executed or when the command is being executed. The command requires the 32-bit parameter. Therefore, this register must be configured according to the command register configuration.

PERI_USB3_DEPCMDN

PERI_USB3_DEPCMDN is peripheral physical endpoint command register.

Offset Address	Register Name	Total Reset Value
0xC81C	PERI_USB3_DEPCMDN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	command_parameters																cmd_status				hipri_forcerm	cmd_act	reserved	cmdloc	reserved				cmdtyp			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	command_parameters	Command parameter. The meaning of this field varies according to the command type. For the start transfer command: Bit[31:16] indicate the USB stream ID declared by this transfer. For the start transfer command of the real-time endpoint: Bit[31:16] indicate the number of microframes (frame) for the first TRB application. For the update transfer, end transfer, or start new configuration command: Bit[22:16] indicate the transfer resource index (XferRscIdx). Hardware declares the transfer resource index for the transfer. The start transfer command is responded after the index is returned. The application software declares the transfer resource index for

			the start new configuration command.
[15:12]	RW	cmd_status	Command completion status. This field saves extra information about the command that is executed. The information is the same as that in bit[15:12] of the endpoint command completion event.
[11]	RW	hipri_forcerm	HighPriority: valid only for the start transfer command ForceRM: valid only for the end transfer command
[10]	RW	cmd_act	Software writes 1 to this bit to enable the peripheral endpoint controller to execute the class command. The peripheral controller sets this bit to 0 when the cmd_status bit is valid and the endpoint is ready to receive another command. However, it does not mean that all previously sent commands are executed.
[9]	RO	reserved	Reserved
[8]	RW	cmdloc	Command completion interrupt. The value 1 indicates that the peripheral controller generates a general endpoint command completion event after executing the command. Note: This bit cannot be set to 1 when PERI_USB3_DCTL[run_stop] is 0.
[7:4]	RO	reserved	Reserved
[3:0]	RW	cmdtyp	Type of the command that is required to be executed by the core 0x0: reserved 0x1: Configure the endpoint (64-bit or 96-bit parameter). 0x2: Configure the endpoint transfer resource (32-bit parameter). 0x3: Obtain the endpoint status (no parameter is required). 0x4: Set the stall (no parameter is required). 0x5: Clear the stall (no parameter is required). 0x6: Start the transfer (64-bit parameter). 0x7: Update the transfer (no parameter is required). 0x8: End the transfer (no parameter is required). 0x9: Start the new configuration (no parameter is required). Other values: reserved

12.11 LSADC_CTRL

12.11.1 Overview

The successive approximation register analog-to-digital converter controller (LSADC_CTRL) provides an ADC controller interface to connect to the on-chip LSADC for driving the LSADC developed by HiSilicon and reporting key values.

12.11.2 Features

The LSADC has the following features:

- 3.3 V power voltage, maximum 300 μA working current, and maximum 0.5 μA current in standby static mode
- Maximum scanning frequency of 200000 times per second
- Four independent channels

The LSADC_CTRL has the following features:

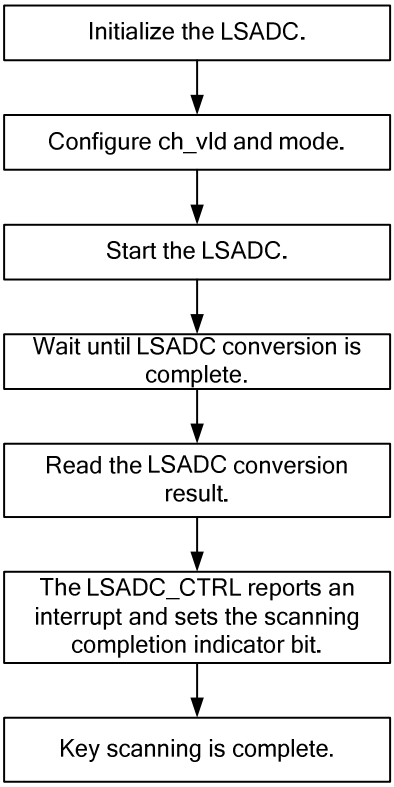
- Single start, one channel scanned at a time, interrupt, query, and no deglitch
- Continuous scanning
  - Channels are polled based on ch_vld.
  - Continuous query is started based on Tscan (scanning interval).
  - Deglitch is performed based on Tglitch and the glitch validity is determined.
  - The LSADC conversion result and corresponding channel IDs are reported.
  - The key press interrupt and key change interrupt are reported.

12.11.3 Operating Mode

Single Scanning Procedure

In single read mode (LSADC_CTRL0[model_sel] = 0), the CPU configures the ID of the channel to scanned, scanning mode, and key value mapping table and starts the LSADC to complete a channel scanning. The LSADC_CTRL obtains the ADC conversion value and sets the conversion completion indicator bit while reporting an interrupt. No deglitch is performed in single read mode.

Figure 12-66 Single scanning procedure



Continuous Scanning Procedure

In continuous scanning mode (LSADC_CTRL0[model_sel] = 1), the CPU configures the continuous scanning interval (Tscan), glitch width (Tglitch), and valid channel ID (ch_vld) based on the application scenario, and starts the LSADC_CTRL. The LSADC_CTRL scans a valid channel within Tscan, and scans the next valid channel when the next scanning time reaches. After all valid channels are scanned, the LSADC_CTRL cyclically scans them again. SeeFigure 12-68. Figure 12-67 illustrates channel polling in continuous scanning mode.

Figure 12-67 Channel polling in continuous scanning mode

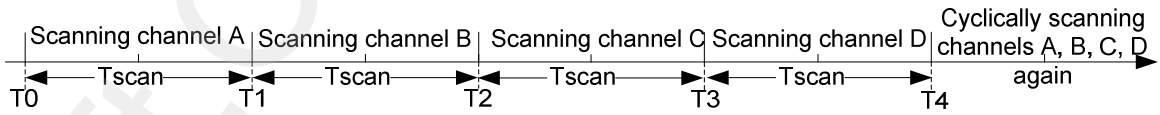
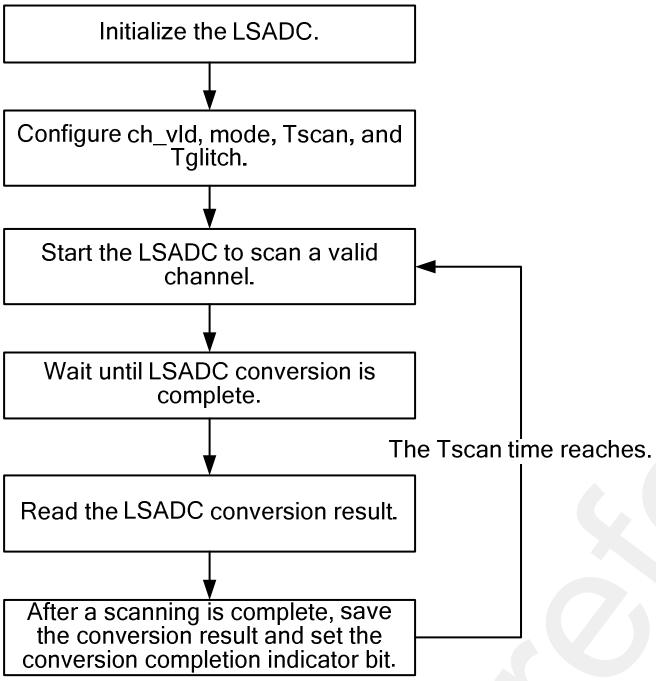


Figure 12-68 Continuous scanning procedure



Deglitch Procedure

The deglitch circuit adopts the majority decision algorithm. In the deglitch window, if the levels sampled by the ADC are the levels when keys are pressed, the value is considered as a valid key value; otherwise, a glitch signal is considered.

In continuous mode, when valid scanning values are obtained after deglitch, a key press interrupt is reported, and the scanning completion indicator bits are set. As there are sampling errors, the precision of the LSADC result is 6 bits.

Hardware deglitch can be enabled or disabled as required.

12.11.4 Register Summary

Table 12-37 describes LSADC_CTRL registers.

Table 12-37 Summary of LSADC_CTRL registers (base address: 0x120E_0000)

Offset Address	Register	Description	Page
0x0000	LSADC_CTRL0	LSADC_CTRL configuration register	12-349
0x0004	LSADC_CTRL1	Deglitch configuration register	12-350
0x0008	LSADC_CTRL2	Scanning interval configuration register	12-351
0x0010	LSADC_CTRL4	Interrupt enable register	12-351
0x0014	LSADC_CTRL5	Interrupt status register	12-352

Offset Address	Register	Description	Page
0x0018	LSADC_CTRL6	Interrupt clear register	12-353
0x001C	LSADC_CTRL7	Start configuration register	12-354
0x0020	LSADC_CTRL8	Stop configuration register	12-354
0x0024	LSADC_CTRL9	Conversion result precision register	12-354
0x0028	LSADC_CTRL10	lsadc_zero register	12-355
0x002C	LSADC_CTRL11	LSADC data hold register 1	12-355
0x0030	LSADC_CTRL12	LSADC data hold register 2	12-356
0x0034	LSADC_CTRL13	LSADC data hold register 3	12-356
0x0038	LSADC_CTRL14	LSADC data hold register 4	12-357

12.11.5 Register Description

LSADC_CTRL0

LSADC_CTRL0 is an LSDAC_CTRL configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	LSADC_CTRL0	0x0000_80FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								lsadc_data_delta				reserved		deglitch_bypass	reserved	lsadc_reset	power_down_model	model_sel	reserved	ch_d_vld	ch_c_vld	ch_b_vld	ch_a_vld	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	lsadc_data_delta	Error range of the LSADC conversion result. In continuous scanning mode, if the difference between two conversion results falls within the error range, the two results are considered as the same.
[19:18]	RO	reserved	Reserved

[17]	RW	deglitch_bypass	Deglitch bypass (used in continuous scanning mode) 0: enabled 1: bypassed
[16]	RO	reserved	Reserved
[15]	RW	lsadc_reset	Whether the LSADC enters the reset status 0: The LSADC exits the reset status. 1: The LSADC enters the reset status.
[14]	RW	power_down_mode l	Whether power_down is supported 0: not supported 1: supported
[13]	RW	model_sel	Scanning mode of the LSADC_CTRL 0: single scanning mode 1: continuous scanning mode
[12]	RO	reserved	Reserved
[11]	RW	ch_d_vld	LSADC channel D validity 0: invalid 1: valid
[10]	RW	ch_c_vld	LSADC channel C validity 0: invalid 1: valid
[9]	RW	ch_b_vld	LSADC channel B validity 0: invalid 1: valid
[8]	RW	ch_a_vld	LSADC channel A validity 0: invalid 1: valid
[7:0]	RO	reserved	Reserved

LSADC_CTRL1

LSADC_CTRL1 is a deglitch configuration register

Offset Address	Register Name	Total Reset Value
0x0004	LSADC_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	glitch_sample																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	glitch_sample	Deglitch time window (in ms typically). When the LSADC conversion result is retained in the deglitch time window, the conversion result is considered as a valid value; otherwise, a glitch is considered. The deglitch time window cannot be 0 in continuous scanning mode.

LSADC_CTRL2

LSADC_CTRL2 is a scanning interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	LSADC_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	time_scan																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	time_scan	Interval of scanning two channels in continuous scanning mode. In the 3 MHz clock domain N/3 MHz, the internal must be 14 cycles longer than the LSADC conversion time. The interval cannot be 0 in continuous scanning mode.

LSADC_CTRL4

LSADC_CTRL4 is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0010	LSADC_CTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_enable	Scanned value valid interrupt enable 0: disabled 1: enabled

LSADC_CTRL5

LSADC_CTRL5 is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	LSADC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											lsadc_auto_busy	int_flag_ind	int_flag_inc	int_flag_inb	int_flag_ina
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved Writing to this field has no effect and reading this field returns 0.
[4]	RO	lsadc_auto_busy	LSADC busy indicator in automatic scanning mode 0: idle 1: busy
[3]	RO	int_flag_ind	Scanned value validity interrupt flag of channel D 0: No interrupt is generated.

			1: An interrupt is generated.
[2]	RO	int_flag_inc	Scanned value validity interrupt flag of channel C 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_flag_inb	Scanned value validity interrupt flag of channel B 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_flag_ina	Scanned value validity interrupt flag of channel A 0: No interrupt is generated. 1: An interrupt is generated.

LSADC_CTRL6

LSADC_CTRL6 is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0018	LSADC_CTRL6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							clr_int_flag_ind	clr_int_flag_inc	clr_int_flag_inb	clr_int_flag_ina
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	clr_int_flag_ind	Channel D interrupt clear 0: not cleared 1: cleared
[2]	WO	clr_int_flag_inc	Channel C interrupt clear 0: not cleared 1: cleared
[1]	WO	clr_int_flag_inb	Channel B interrupt clear 0: not cleared 1: cleared

[0]	WO	clr_int_flag_ina	Channel A interrupt clear 0: not cleared 1: cleared

LSADC_CTRL7

LSADC_CTRL7 is a start configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	LSADC_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	start	LSADC_CTRL start signal. Writing any value to this register starts the LSADC_CTRL.

LSADC_CTRL8

LSADC_CTRL8 is a stop configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	LSADC_CTRL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	stop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	stop	Automatic scanning stop. In automatic scanning mode, writing any value to this register stops automatic scanning of the LSADC_CTRL. Automatic scanning is restarted only after the start bit is enabled.

LSADC_CTRL9

LSADC_CTRL9 is a conversion result precision register.

Offset Address	Register Name	Total Reset Value
0x0024	LSADC_CTRL9	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_active_bit									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_active_bit	LSADC conversion result precision. 10'b1111111111: 10-bit precision 10'b1111111110: 9-bit precision … 10'b1000000000: 1-bit precision

LSADC_CTRL10

LSADC_CTRL10 is an lsadc_zero register.

Offset Address	Register Name	Total Reset Value
0x0028	LSADC_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_zero									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_zero	LSADC value when no key is pressed

LSADC_CTRL11

LSADC_CTRL11 is LSADC data hold register 1.

Offset Address	Register Name	Total Reset Value
0x002C	LSADC_CTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_ina									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_data_ina	Scanned value of LSADC channel A

LSADC_CTRL12

LSADC_CTRL12 is LSADC data hold register 2.

Offset Address	Register Name	Total Reset Value
0x0030	LSADC_CTRL12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_inb									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_data_inb	Scanned value of LSADC channel B

LSADC_CTRL13

LSADC_CTRL13 is LSADC data hold register 3.

Offset Address	Register Name	Total Reset Value
0x0034	LSADC_CTRL13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_inc									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_data_inc	Scanned value of LSADC channel C

LSADC_CTRL14

LSADC_CTRL14 is LSADC data hold register 4.

Offset Address	Register Name	Total Reset Value
0x0038	LSADC_CTRL14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_ind									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_data_ind	Scanned value of LSADC channel D

12.12 PWM

12.12.1 Overview

Hi3519 V100 has eight independent pulse width modulation (PWM) outputs in one group.

12.12.2 Features

Each PWM output has the following features:

- Supports the optional 3 MHz, 24 MHz or 50 MHz clock source.
- Provides an internal 32-bit counter with configurable output frequency. The maximum frequency of the output square waves is 25 MHz (50 MHz/2), and the minimum frequency of the output square waves is 0.007 Hz (3 MHz/4294967296).
- Allows you to set the number of high-level beats (32 bits).
- Provides a 10-bit internal counter and allows you to set the number of pulses. A maximum of 1023 pulses are supported. The number of output pulses can be fixed at a value and the always output mode is supported.
  - When pwmn_keep is set to 0 (PWM*n* indicates the PWM ID), PWM*n* outputs the square waves of a specific number, which depends on the setting of the pwmn_num register.
  - When pwmn_keep is set to 1, PWM*n* always outputs square waves.

12.12.3 Operating Mode

The internal working clock of the PWM module is 3 MHz, 24 MHz or 50 MHz. The following takes PWM0 as an example to configure 1-channel PWM output:

Step 1 Select an appropriate clock source, and calculate the number of required cycles and high-level beats.

Step 2 Write the corresponding values to PWM0_CFG0, PWM0_CFG1, and PWM0_CFG2.

Step 3 Set PWM0_CTRL bit[0] to 1 to enable the PWM output.

----End

For example, to output a 3 kHz waveform with 72.5% high levels and 10 pulses (the duty ratio is 72.5%), calculate the number of high levels as follows:

- If the 3 MHz clock is the source clock, Cycle = 3 MHz/1 kHz ≈ 1000 (0x00003E8 in hexadecimal)
- Number of high levels = Cycle x Duty ratio = 1000 x 72.5% = 725 (0x00002D5 in hexadecimal)

To output a desired waveform, perform the following steps:

Step 1 Write 0x2 to PERI_CRG55, select the 3 MHz clock as the PWM clock source, and enable the PWM clock.

Step 2 Read PWM0_STATE2 bit[10] until it is 0. This indicates that the PWM module is idle and can output square waves.

Step 3 Write 0x0000_03E8 to PWM0_CFG0.

Step 4 Write 0x0000_02D5 to PWM0_CFG1.

Step 5 Write 0x0000_000A to PWM0_CFG2.

Step 6 Write 0x1 to PWM0_CTRL.

NOTE

The following steps can be skipped. They are used to check whether the square wave is output as expected.

Step 7 Read PWM0_STATE2 bit[10] until it is 1. This indicates that the PWM module is outputting square waves.

Step 8 Read PWM0_STATE0 and compare the queried value with 0x0000_03E8.

Step 9 Read PWM0_STATE1 and compare the queried value with 0x0000_02D5.

Step 10 Read PWM0_STATE2 bit[9:0] and compare the queried value with 0x0A. If PWM0_STATE2 bit[10] is 1, the PWM module is outputting square waves. If PWM0_STATE2 bit[10] is 0, the configured number of square waves are output.

----End

12.12.4 Register Summary

The registers of PWM*n* (*n* = 0−7) have the same functions but their base addresses are different. See Table 12-1.

Table 12-1 Base addresses for the registers of PWM*n*

Value of n	Base Address
0	0x1213_0000
1	0x1213_0020
2	0x1213_0040
3	0x1213_0060
4	0x1213_0080
5	0x1213_00A0
6	0x1213_00C0
7	0x1213_00E0

Table 12-2 describes PWM0 registers as an example.

Table 12-2 Summary of PWM0 registers (base address: 0x1213_0000)

Offset Address	Register	Description	Page
0x0000	PWM0_CFG0	PWM0 configuration 0 register	12-359
0x0004	PWM0_CFG1	PWM0 configuration 1 register	12-360
0x0008	PWM0_CFG2	PWM0 configuration 2 register	12-360
0x000C	PWM0_CTRL	PWM0 control register	12-361
0x0010	PWM0_STATE0	PWM0 status 0 register	12-361
0x0014	PWM0_STATE1	PWM0 status 1 register	12-362
0x0018	PWM0_STATE2	PWM0 status 2 register	12-362

12.12.5 Register Description

PWM0_CFG0

PWM0_CFG0 is a PWM0 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	pwm0_period							

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	pwm0_period	Number of cycles for PWM0 **NOTE** The configured value must be greater than or equal to 2.

PWM0_CFG1

PWM0_CFG1 is a PWM0 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm0_duty																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:0]	RW	pwm0_duty	Number of level beats for PWM0. If the number is greater than or equal to the number of cycles, the output level is always high. **NOTE** The configured value must be greater than or equal to 1.

PWM0_CFG2

PWM0_CFG2 is a PWM0 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						pwm0_num									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	pwm0_num	Number of square waves output by PWM0

PWM0_CTRL

PWM0_CTRL is a PWM0 control register.

Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																													pwm0_keep	pwm0_inv	pwm0_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	pwm0_keep	PWM output mode 0: PWM0 outputs a fixed number of square waves. 1: PWM0 always outputs square waves.
[1]	RW	pwm0_inv	PWM output control 0: PWM0 outputs square waves in normal mode. 1: PWM0 outputs square waves in inverted mode.
[0]	RW	pwm0_enable	PWM enable 0: disabled 1: enabled

PWM0_STATE0

PWM0_STATE0 is a PWM0 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm0_period_st																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pwm0_period_st	Number of count cycles for the internal module of PWM0

PWM0_STATE1

PWM0_STATE1 is a PWM0 status 1 register.

Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm0_duty_st																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pwm0_duty_st	Number of high level beats for the internal module of PWM0

PWM0_STATE2

PWM0_STATE2 is a PWM0 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm0_cnt_st								pwm0_keep_st	pwm0_busy	pwm0_period_st									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:12]	RO	pwm0_cnt_st	Number of remaining square waves output by PWM0. This field is valid only when the following conditions are met: pwm0_busy = 1, pwm0_keep_st = 0
[11]	RO	pwm0_keep_st	Square wave output mode for the internal module of PWM0 0: PWM0 outputs a fixed number of square waves 1: PWM0 always outputs square waves.
[10]	RO	pwm0_busy	Working status of PWM0 0: Wave output is complete and PWM0 is idle. 1: PWM0 is outputting square waves.
[9:0]	RO	pwm0_period_st	Number of output square waves for the internal module of PWM0

Contents

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13 Security Modules

13.1 Cipher

13.1.1 Overview

The cipher module supports data encryption and decryption by following the data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The cipher module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

13.1.2 Features

The cipher module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.
- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes respectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of counter with Cipher Block Chaining-Message Authentication Code (CCM), Galois/Counter Mode (GCM), electronic code book (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST SP 800-38A standard.
- Supports the operating modes of ECB, CBC, 1/8/64-CFB, and 1/8/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.

- Provides eight keys (fixed at 128 bits) configured by the key management module. The master CPU supports the write operation but not the read operation.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.
- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

13.1.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a/c/d standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 13-1 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 13-1 3DES encryption of a 3-key operation and a 2-key operation

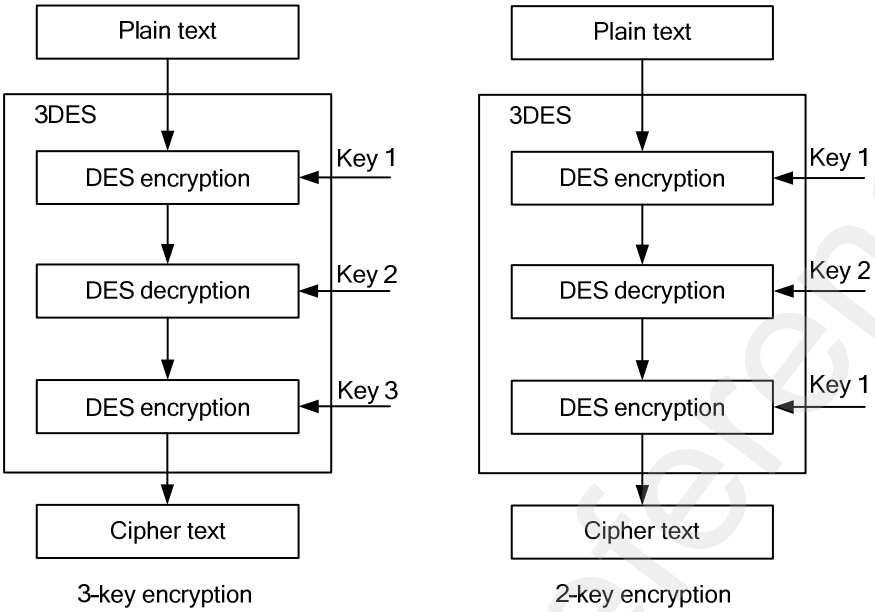
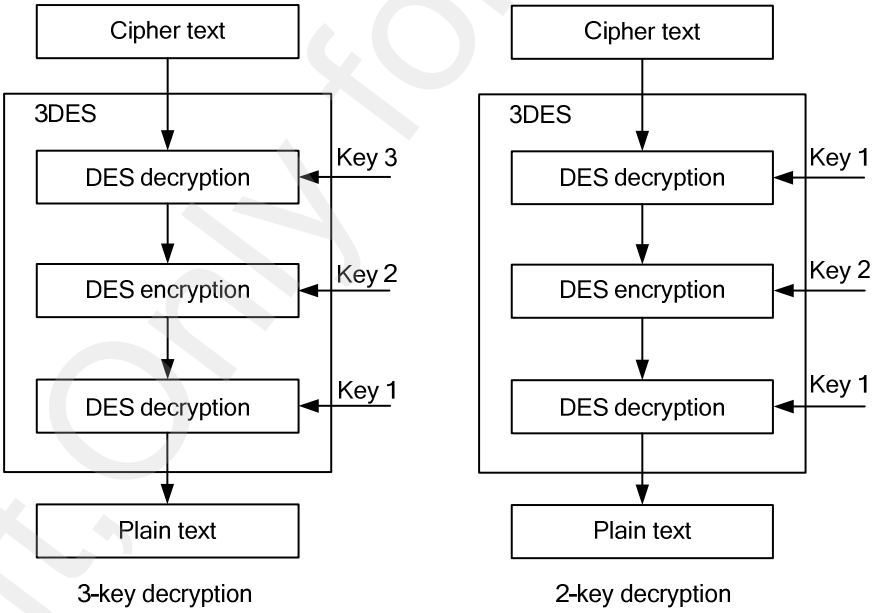


Figure 13-2 shows the 3DES decryption of a 3-key operation and a 2-key operation.

Figure 13-2 3DES decryption of a 3-key operation and a 2-key operation



ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 13-3 shows the ECB mode of the AES and DES algorithms, and Figure 13-4 shows the ECB mode of the 3DES algorithm.

Figure 13-3 ECB mode of the AES and DES algorithms

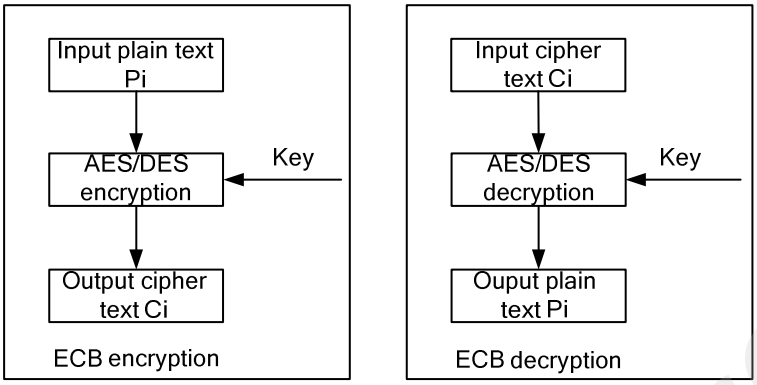
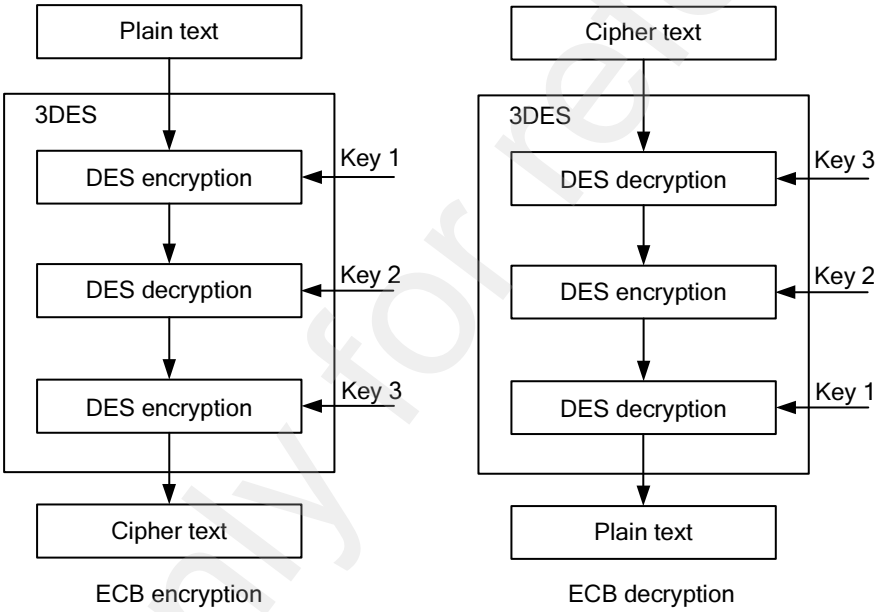


Figure 13-4 ECB mode of the 3DES algorithm



CBC Mode

In CBC mode, the encrypted input plain text block must be exclusively ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text. Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 13-5 shows the CBC mode of the AES and DES algorithms, and Figure 13-6 shows the CBC mode of the 3DES algorithm.

Figure 13-5 CBC mode of the AES and DES algorithms

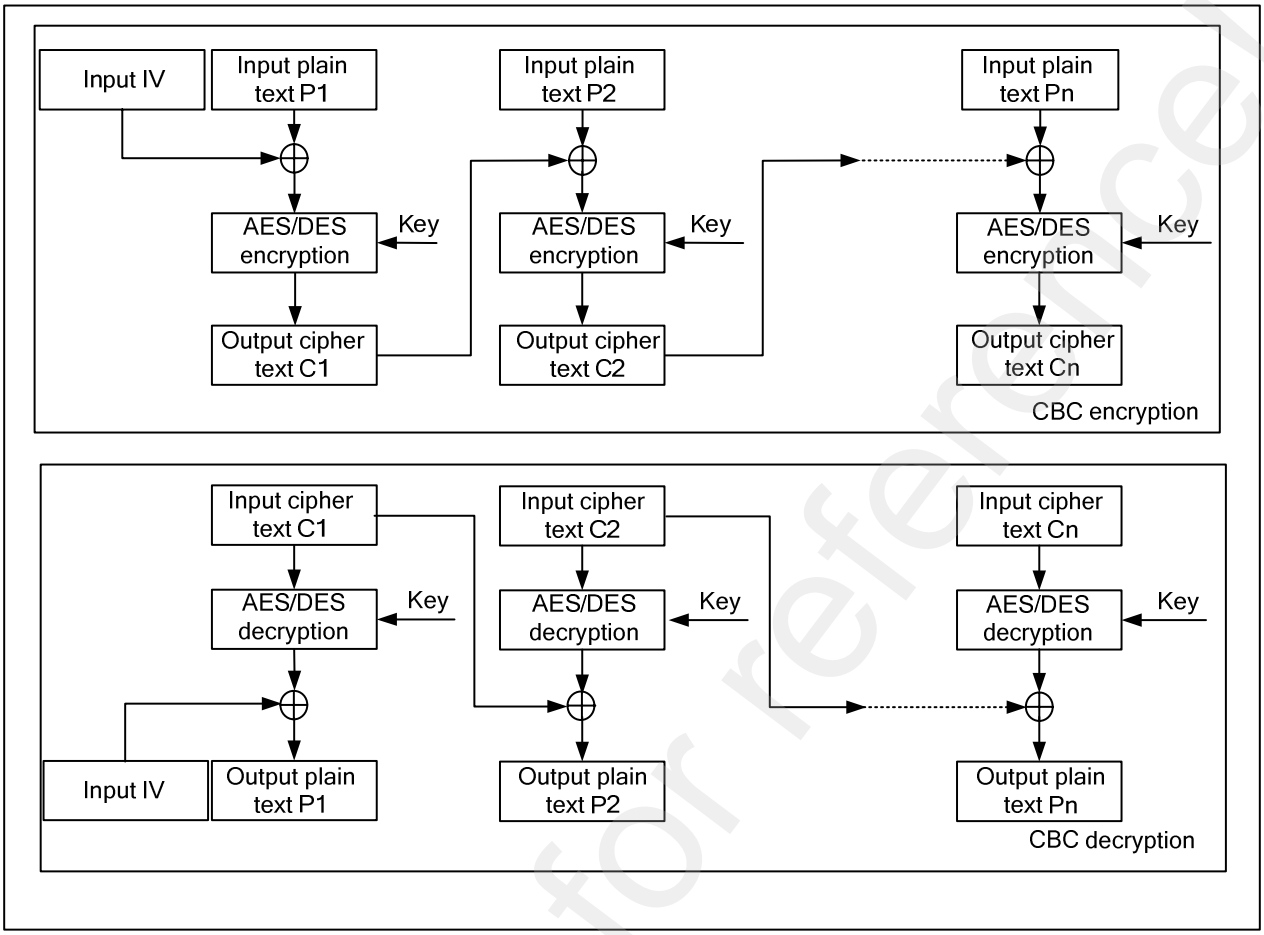
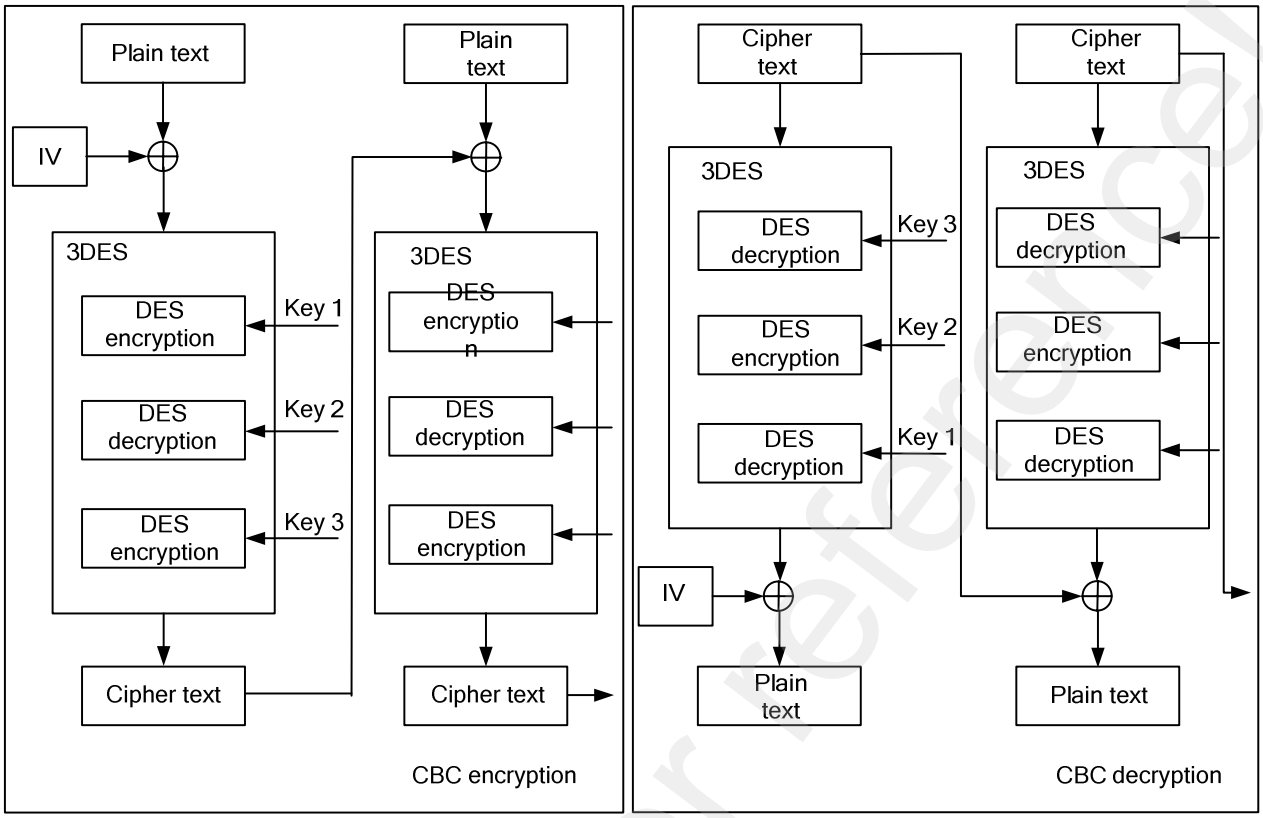


Figure 13-6 CBC mode of the 3DES algorithm



CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 13-7 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 13-8 shows the s-bit CFB mode of the 3DES algorithm.

Figure 13-7 S-bit CFB mode of the AES and DES algorithms

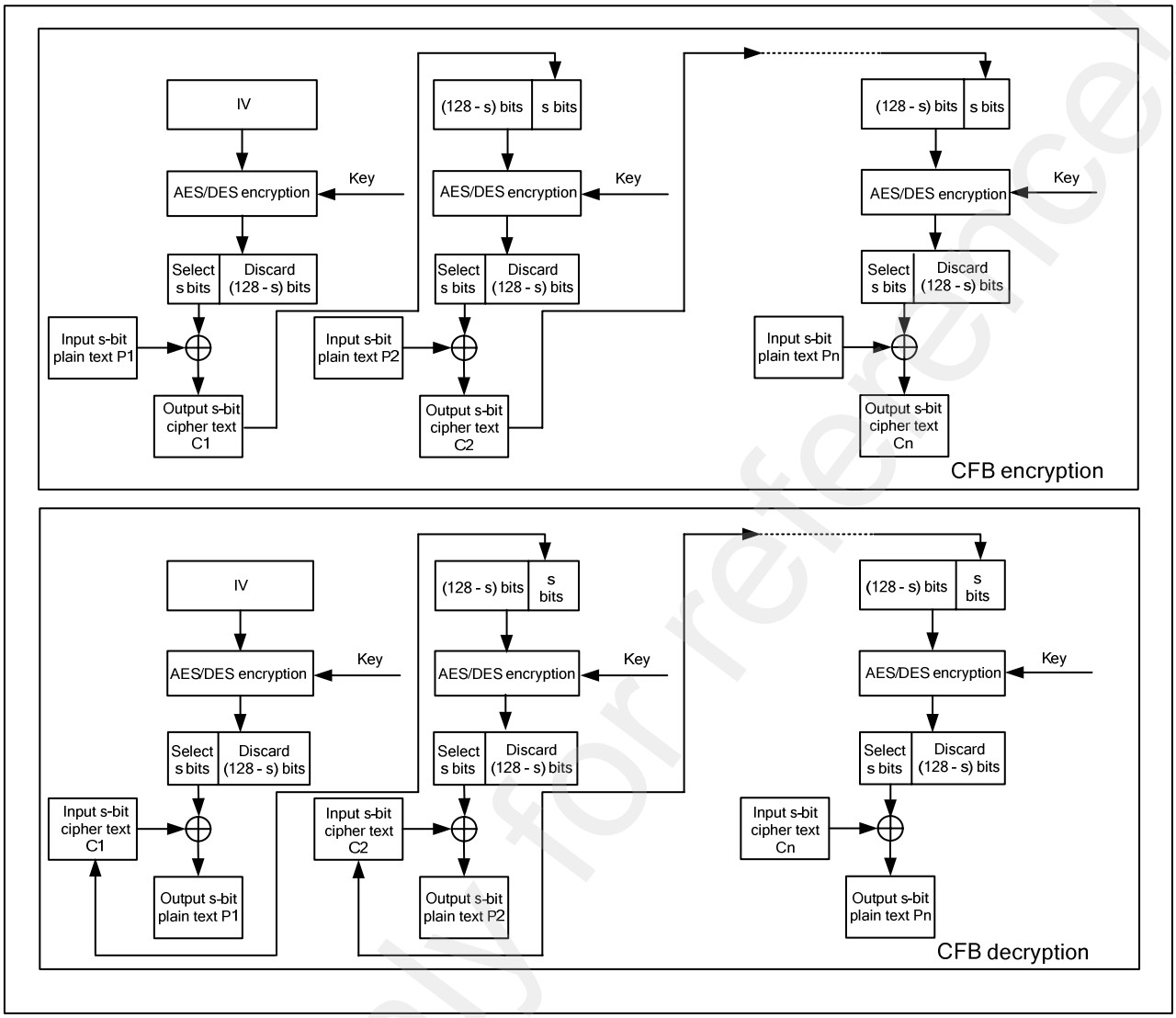
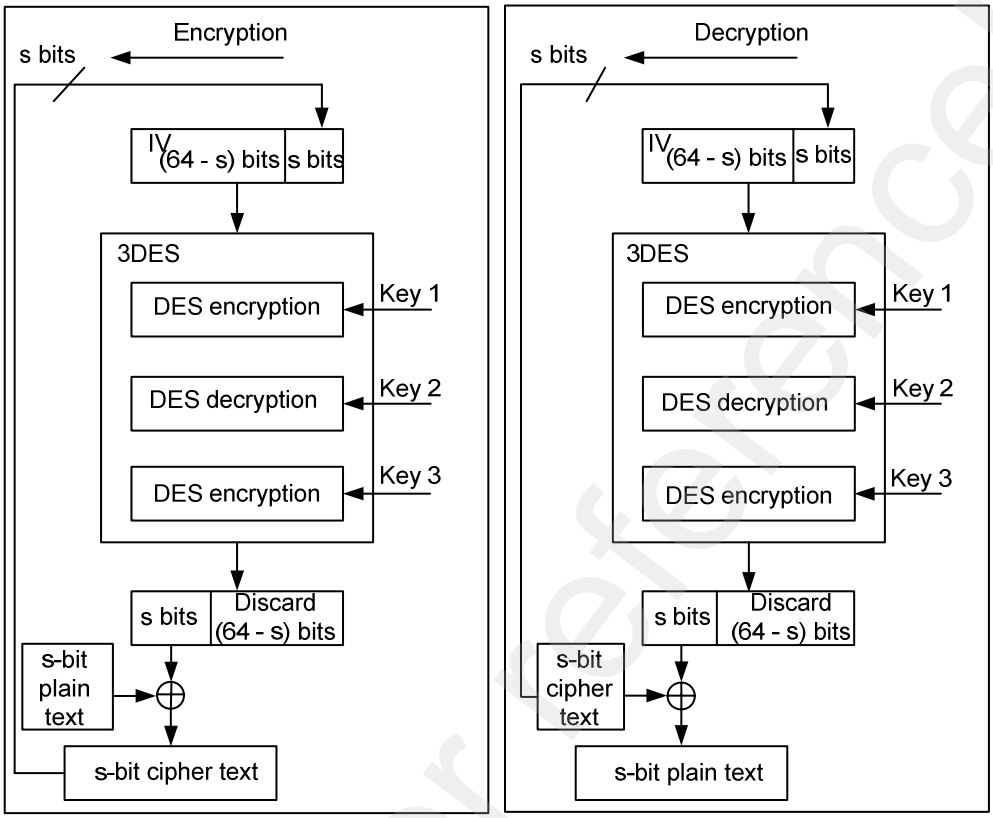


Figure 13-8 S-bit CFB mode of the 3DES algorithm



OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

Figure 13-9 shows the OFB mode of the AES algorithm.

Figure 13-9 OFB mode of the AES algorithm

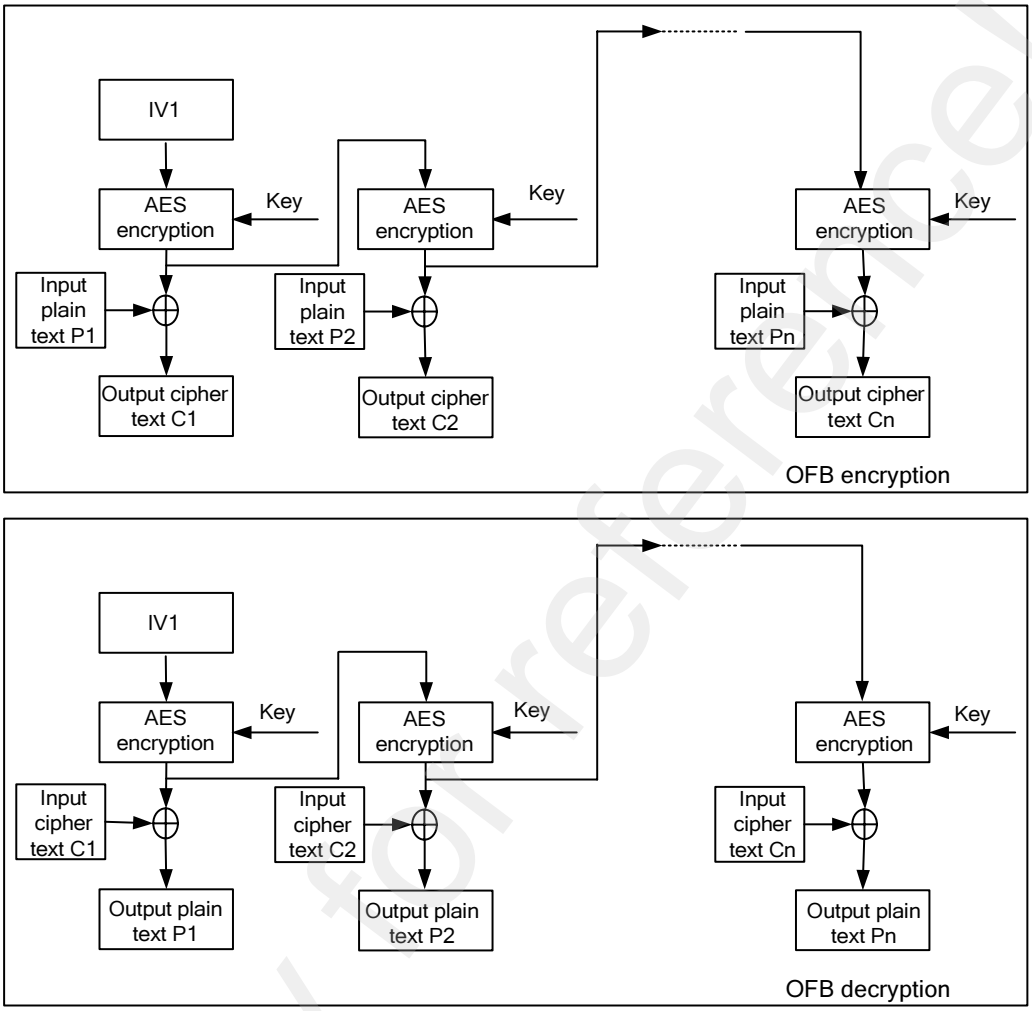


Figure 13-10 shows the s-bit OFB mode of the DES algorithm.

Figure 13-10 S-bit OFB mode of the DES algorithm

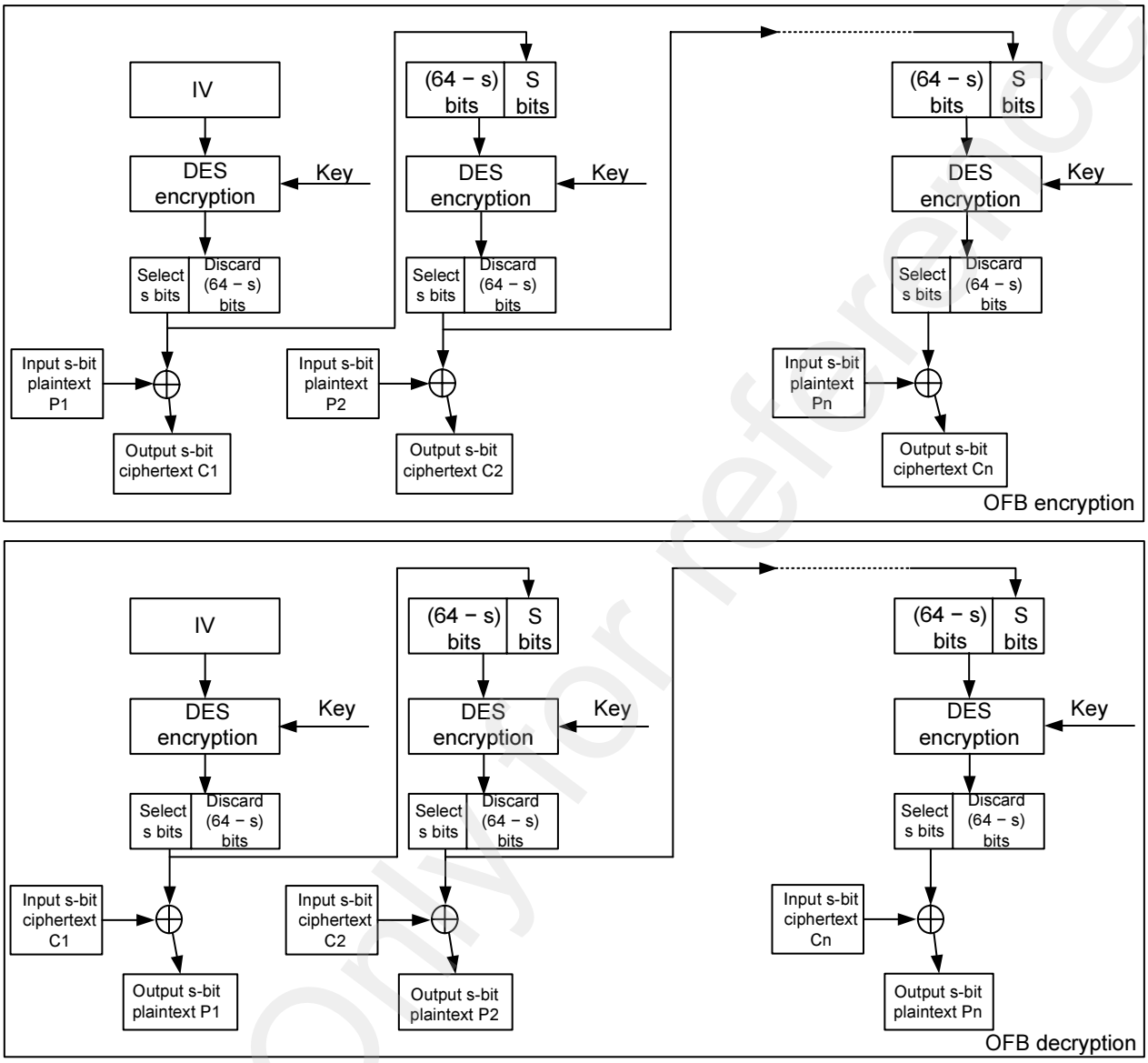
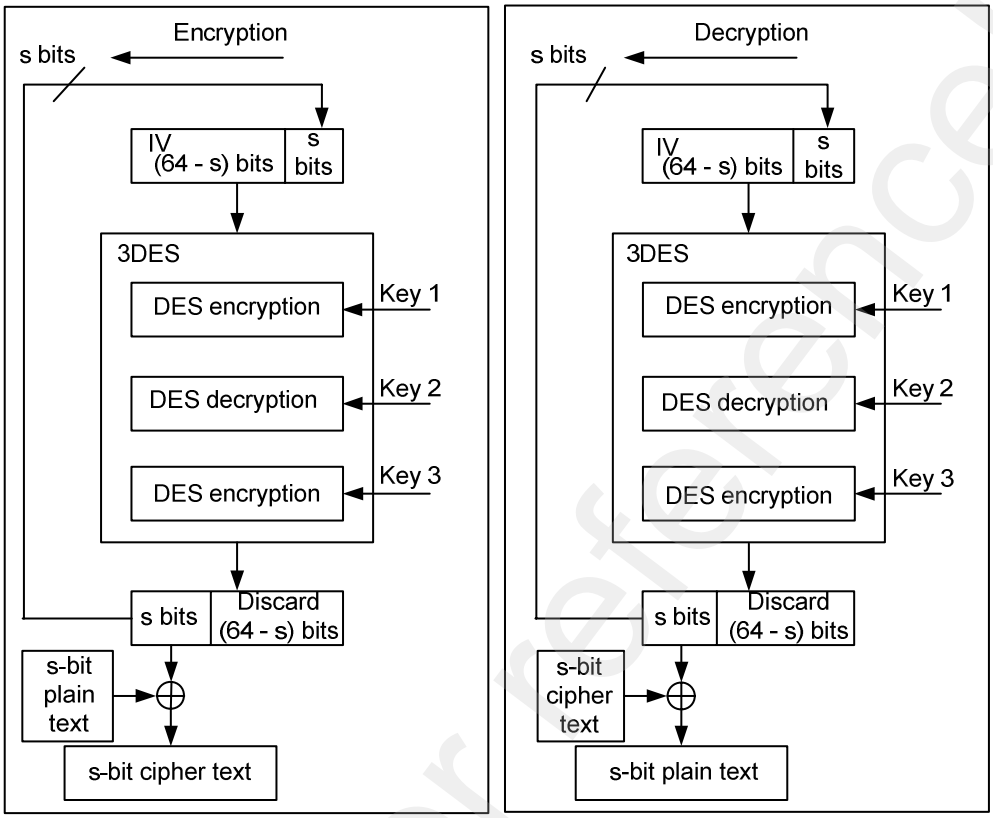


Figure 13-11 shows the s-bit OFB mode of the 3DES algorithm.

Figure 13-11 S-bit OFB mode of the 3DES algorithm



CTR Mode

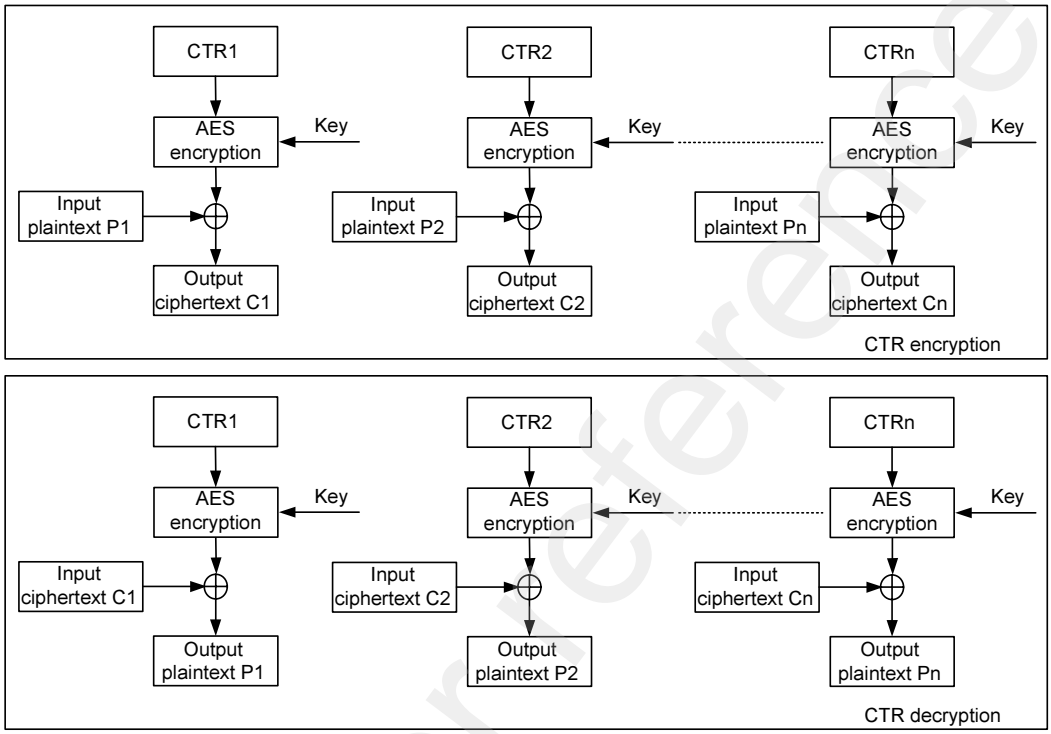
In CTR mode, different data segments are input to the cipher module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE

CTRn is obtained by using the accumulation count mode.

Figure 13-12 shows the CTR mode of the AES algorithm.

Figure 13-12 CTR mode of the AES algorithm

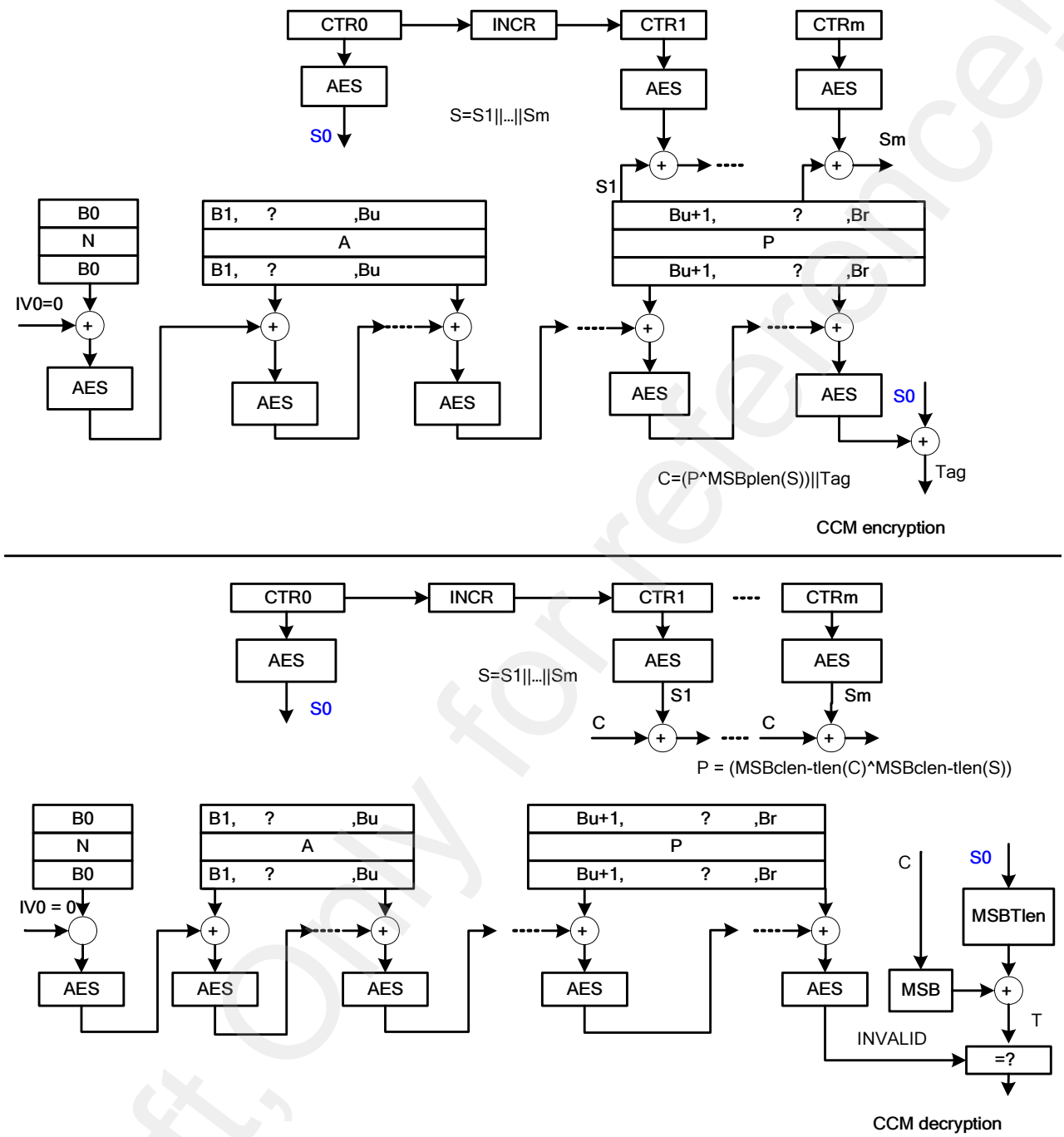


CCM Mode

The CCM mode of the AES algorithm consists of the AES CTR mode and AES CBC mode, which ensures data confidentiality and integrity.

Figure 13-13 shows the CCM mode of the AES algorithm.

Figure 13-13 CCM mode of the AES algorithm

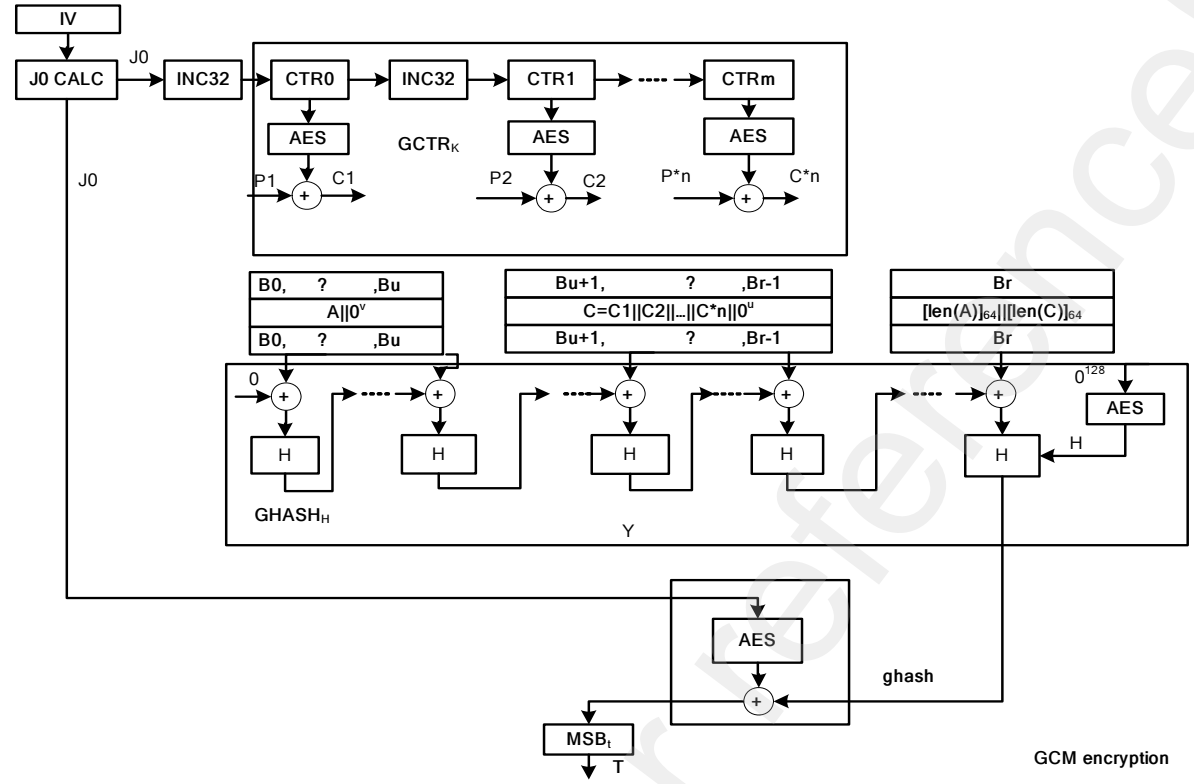


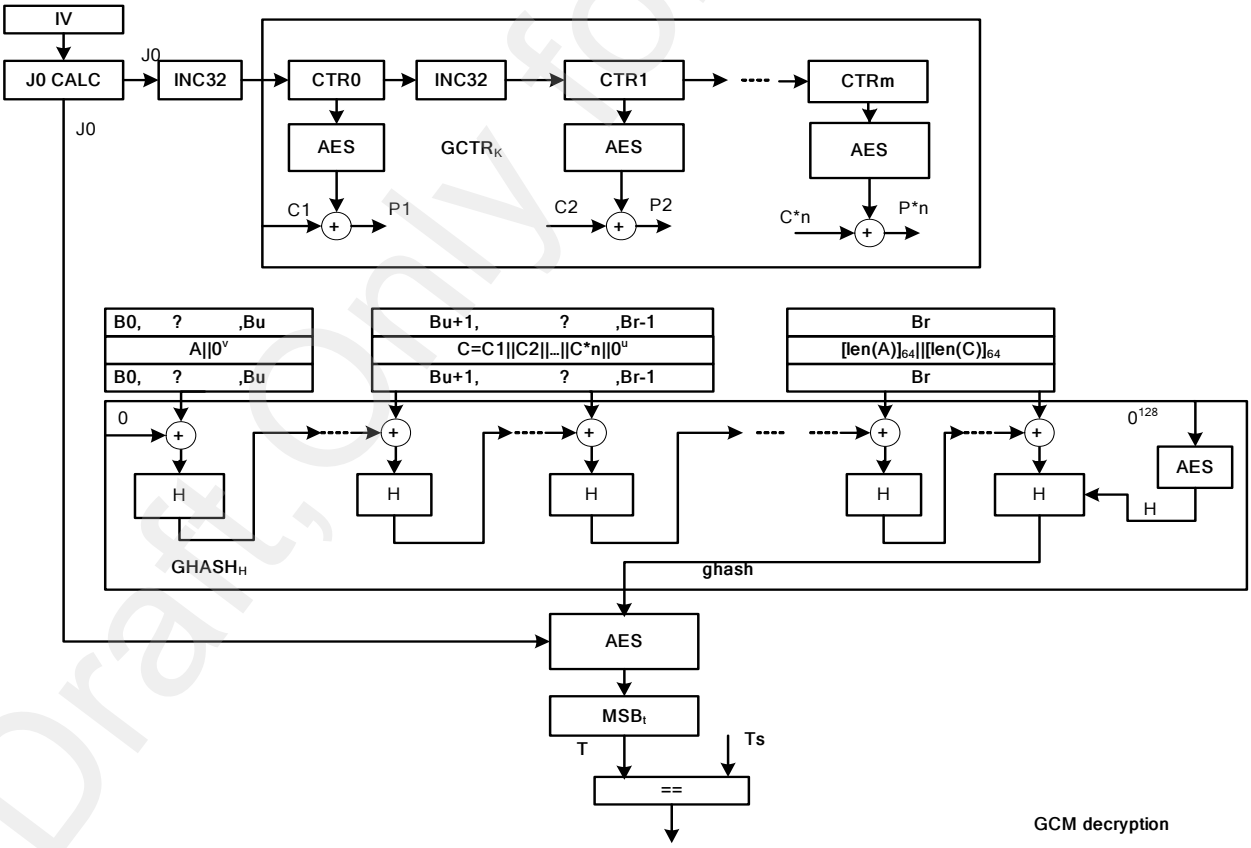
GCM Mode

The GCM mode of the AES algorithm consists of AES CTR and ghash, which ensures data confidentiality and integrity.

Figure 13-14 shows the GCM mode of the AES algorithm.

Figure 13-14 GCM mode of the AES algorithm





13.1.4 Operating Mode

Single-Block Operation Process of the Cipher Module

The cipher module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

----End

Check whether encryption and decryption of channel 0 are complete in either of following ways:

Step 1 Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.

Step 2 Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete. Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

----End

Multi-Block Operation Process of the Cipher Module

The cipher module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

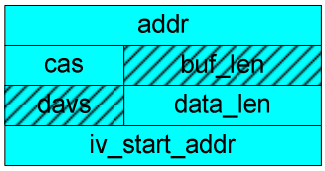
Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

----End

Figure 13-15 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 13-15 Structure of the linked list header of a multi-block encryption/decryption channel

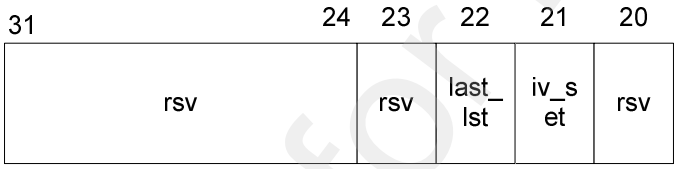


The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is cipher control information.

Figure 13-16 shows the bits of cas.

Figure 13-16 Bits of cas



  - iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
  - last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the cipher module is idle, the cipher clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The cipher module can be soft-reset by configuring the registers of the system controller.

13.1.5 Register Summary

Table 13-1 describes cipher registers.

NOTE

The variable *n* in the offset addresses indicates the channel ID and ranges from 1 to 7.

Table 13-1 Summary of cipher registers (base address: 0x1008_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	Cipher output register for channel 0 (for single-block encryption/decryption)	13-20
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the cipher module	13-21
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	13-22
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the cipher module	13-22
0x0840	CHAN0_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 0	13-24
0x0844	CHAN0_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 0	13-24
0x0848	CHAN1_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 1	13-24
0x084C	CHAN1_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 1	13-25
0x0850	CHAN2_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 2	13-25
0x0854	CHAN2_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 2	13-26
0x0858	CHAN3_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 3	13-26
0x085C	CHAN3_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 3	13-26
0x0860	CHAN4_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 4	13-27
0x0864	CHAN4_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 4	13-27
0x0868	CHAN5_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 5	13-28
0x086C	CHAN5_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 5	13-28
0x0870	CHAN6_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 6	13-28

Offset Address	Register	Description	Page
0x0874	CHAN6_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 6	13-29
0x0878	CHAN7_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 7	13-29
0x087C	CHAN7_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 7	13-30
0x0880	CHAN0_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 0	13-30
0x0884	CHAN0_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 0	13-30
0x0888	CHAN1_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 1	13-31
0x088C	CHAN1_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 1	13-31
0x0890	CHAN2_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 2	13-32
0x0894	CHAN2_GCM_PC_LEN_0	Payload length upper 32 bits register for the AES GCM of channel 2	13-32
0x0898	CHAN3_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 3	13-32
0x089C	CHAN3_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 3	13-33
0x08A0	CHAN4_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 4	13-33
0x08A4	CHAN4_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 4	13-34
0x08A8	CHAN5_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 5	13-34
0x08AC	CHAN5_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 5	13-34
0x08B0	CHAN6_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 6	13-35
0x08B4	CHAN6_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 6	13-35
0x08B8	CHAN7_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 7	13-36
0x08BC	CHAN7_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 7	13-36

Offset Address	Register	Description	Page
0x08C0	CHAN0_3_GCM_IV_LEN	IV length register for the AES GCM of channels 0−3	13-36
0x08C4	CHAN4_7_GCM_IV_LEN	IV length register for the AES GCM of channels 4−7	13-37
0x08CC	CHANn_GCM_IV_LEN_VLD	GCM IV length validity signal register	13-37
0x08D0	CHANn_GCM_TAG_VLD	GCM tag validity signal register	13-38
0x08D4	CHANn_GCM_GHASH_A_END	GCM A calculation end signal register	13-38
0x0900 + 0x10 x *n* + 0x00	CHANn_GCM_TAG_0	GCM tag register 0 for channel *n*	13-39
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_1	GCM tag register 1 for channel *n*	13-39
0x0900 + 0x10 x *n* + 0x08	CHANn_GCM_TAG_2	GCM tag register 2 for channel *n*	13-40
0x0900 + 0x10 x *n* + 0x0C	CHANn_GCM_TAG_3	GCM tag register 3 for channel *n*	13-40
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	13-40
0x1004−0x1010	CHAN0_CIPHER_IVIN	Cipher VI block input register for channel 0	13-42
0x1014−0x1020	CHAN0_CIPHER_DIN	128-bit block input register of the cipher module	13-43
0x1000 + *n* x 0x128	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	13-44
0x1000 + *n* x 0 x128 + 0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	13-44
0x1000 + *n* x 0x128 + 0x8	CHANn_IEMPTY_CNT	Processed data buffer count register for channel n in the input queue	13-45
0x1000 + *n* x 0x128 + 0xC	CHANn_INT_ICNTCFG	Input queue multi-packet interrupt threshold register for channel n	13-45
0x1000 + *n* x 0x128 + 0x10	CHANn_CIPHER_CTRL	Encryption/decryption control register for channel n	13-46
0x1000 + *n* x 0x128 + 0x14	CHANn_SRC_LST_SADDR	Input queue start address register for channel n	13-48
0x1000 + *n* x 0x128 + 0x18	CHANn_IAGE_TIMER	Input queue interrupt aging time configuration register for channel n	13-48

Offset Address	Register	Description	Page
0x1000 + *n* x 0x128 + 0x3C	CHANn_OBUF_NUM	Output queue total depth register for channel n (linked list header count register)	13-49
0x1000 + *n* x 0x128 + 0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	13-49
0x1000 + *n* x 0x128 + 0x44	CHANn_OFULL_CNT	Processed data buffer count register for channel n in the output queue	13-50
0x1000 + *n* x 0x128 + 0x48	CHANn_INT_OCNTCFG	Output queue multi-packet interrupt threshold register for channel n	13-50
0x1000 + *n* x 0x128 + 0x4C	CHANn_DEST_LST_SADDR	Output queue start address register for channel n	13-50
0x1000 + *n* x 0x128 + 0x50	CHANn_OAGE_TIMER	Output queue interrupt aging time configuration register for channel n	13-51
0x1400	INT_STATUS	Interrupt status register	13-52
0x1404	INT_EN	Interrupt enable register	13-53
0x1408	INT_RAW	Raw interrupt status register	13-54
0x140C	RST_STATUS	Reset status indicator register	13-55
0x1410	CHAN0_CFG	Channel 0 configuration register	13-55

13.1.6 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is a cipher output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.

- If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
- If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
- In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the cipher module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the cipher module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the cipher module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is an IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the cipher module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

- CIPHER_KEY bit[63:0] indicates key 1.
- CIPHER_KEY bit[127:64] indicates key 2.
- CIPHER_KEY bit[191:128] indicates key 3.

If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

where

- CIPHER_KEY bit[63:0] indicates key 1.
- CIPHER_KEY bit[127:64] indicates key 2.

- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The cipher module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	Key input of the cipher module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_GCM_A_LEN_0

CHAN0_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0840	CHAN0_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 0 (unit: 8 bits)

CHAN0_GCM_A_LEN_1

CHAN0_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0844	CHAN0_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 0 (unit: 8 bits)

CHAN1_GCM_A_LEN_0

CHAN1_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x0848	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 1 (unit: 8 bits)

CHAN1_GCM_A_LEN_1

CHAN1_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x084C	CHAN1_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 1 (unit: 8 bits)

CHAN2_GCM_A_LEN_0

CHAN2_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0850	CHAN2_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 2 (unit: 8 bits)

CHAN2_GCM_A_LEN_1

CHAN2_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0854	CHAN2_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 2 (unit: 8 bits)

CHAN3_GCM_A_LEN_0

CHAN3_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x0858	CHAN3_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 3 (unit: 8 bits)

CHAN3_GCM_A_LEN_1

CHAN3_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x085C	CHAN3_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 3 (unit: 8 bits)

CHAN4_GCM_A_LEN_0

CHAN4_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x0860	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 4 (unit: 8 bits)

CHAN4_GCM_A_LEN_1

CHAN4_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x0864	CHAN4_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 4 (unit: 8 bits)

CHAN5_GCM_A_LEN_0

CHAN5_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x0868	CHAN5_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan5_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 5 (unit: 8 bits)

CHAN5_GCM_A_LEN_1

CHAN5_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x086C	CHAN5_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan5_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 5 (unit: 8 bits)

CHAN6_GCM_A_LEN_0

CHAN6_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x0870	CHAN6_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 6 (unit: 8 bits)

CHAN6_GCM_A_LEN_1

CHAN6_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x0874	CHAN6_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 6 (unit: 8 bits)

CHAN7_GCM_A_LEN_0

CHAN7_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x0878	CHAN7_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 7 (unit: 8 bits)

CHAN7_GCM_A_LEN_1

CHAN7_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x087C	CHAN7_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 7 (unit: 8 bits)

CHAN0_GCM_PC_LEN_0

CHAN0_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0880	CHAN0_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 0 (unit: 8 bits)

CHAN0_GCM_PC_LEN_1

CHAN0_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0884	CHAN0_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 0 (unit: 8 bits)

CHAN1_GCM_PC_LEN_0

CHAN1_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x0888	CHAN1_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 1 (unit: 8 bits)

CHAN1_GCM_PC_LEN_1

CHAN1_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x088C	CHAN1_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 1 (unit: 8 bits)

CHAN2_GCM_PC_LEN_0

CHAN2_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0890	CHAN2_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 2 (unit: 8 bits)

CHAN2_GCM_PC_LEN_1

CHAN2_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0894	CHAN2_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 2 (unit: 8 bits)

CHAN3_GCM_PC_LEN_0

CHAN3_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x0898	CHAN3_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 3 (unit: 8 bits)

CHAN3_GCM_PC_LEN_1

CHAN3_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x089C	CHAN3_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 3 (unit: 8 bits)

CHAN4_GCM_PC_LEN_0

CHAN4_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x08A0	CHAN4_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 4 (unit: 8 bits)

CHAN4_GCM_PC_LEN_1

CHAN4_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x08A4	CHAN4_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 4 (unit: 8 bits)

CHAN5_GCM_PC_LEN_0

CHAN5_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x08A8	CHAN5_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 5 (unit: 8 bits)

CHAN5_GCM_PC_LEN_1

CHAN5_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x08AC	CHAN5_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 5 (unit: 8 bits)

CHAN6_GCM_PC_LEN_0

CHAN6_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x08B0	CHAN6_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 6 (unit: 8 bits)

CHAN6_GCM_PC_LEN_1

CHAN6_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x08B4	CHAN6_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 6 (unit: 8 bits)

CHAN7_GCM_PC_LEN_0

CHAN7_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x08B8	CHAN7_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 7 (unit: 8 bits)

CHAN7_GCM_PC_LEN_1

CHAN7_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x08BC	CHAN7_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 7 (unit: 8 bits)

CHAN0_3_GCM_IV_LEN

CHAN0_3_GCM_IV_LEN is an IV length register for the AES GCM of channels 0–3.

Offset Address	Register Name	Total Reset Value
0x08C0	CHAN0_3_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved

[28:24]	RW	chan3_gcm_iv_len	IV length of channel 3
[23:21]	RO	reserved	Reserved
[20:16]	RW	chan2_gcm_iv_len	IV length of channel 2
[15:13]	RO	reserved	Reserved
[12:8]	RW	chan1_gcm_iv_len	IV length of channel 1
[7:5]	RO	reserved	Reserved
[4:0]	RW	chan0_gcm_iv_len	IV length of channel 0

CHAN4_7_GCM_IV_LEN

CHAN4_7_GCM_IV_LEN is an IV length register for the AES GCM of channels 4−7.

Offset Address	Register Name	Total Reset Value
0x08C4	CHAN4_7_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	chan7_gcm_iv_len	IV length of channel 7
[23:21]	RO	reserved	Reserved
[20:16]	RW	chan6_gcm_iv_len	IV length of channel 6
[15:13]	RO	reserved	Reserved
[12:8]	RW	chan5_gcm_iv_len	IV length of channel 5
[7:5]	RO	reserved	Reserved
[4:0]	RW	chan4_gcm_iv_len	IV length of channel 4

CHANn_GCM_IV_LEN_VLD

CHANn_GCM_IV_LEN_VLD is a GCM IV length validity signal register.

Offset Address	Register Name	Total Reset Value
0x08CC	CHANn_GCM_IV_LEN_VLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_iv_len_vld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	chann_gcm_iv_len_vld	Whether the IV length of channel *n* is valid after the operation is started in AES GCM mode 0: invalid (the channel length is 0 or greater than 16 bytes) 1: valid

CHANn_GCM_TAG_VLD

CHANn_GCM_TAG_VLD is a GCM tag validity signal register.

Offset Address	Register Name	Total Reset Value
0x08D0	CHANn_GCM_TAG_VLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_tag_vld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RWC	chann_gcm_tag_vld	Whether the tag of channel *n* is valid in AES GCM mode 0: invalid 1: valid. Writing 1 clears this field.

CHANn_GCM_GHASH_A_END

CHANn_GCM_GHASH_A_END is a GCM A calculation end signal register.

Offset Address	Register Name	Total Reset Value
0x08D4	CHANn_GCM_GHASH_A_END	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_ghash_a_end							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RWC	chann_gcm_ghash_a_end	Whether the ghash of channel *n* is finished when the A length is not 0 in AES GCM mode 1: finished. Writing 1 clears this field. 0: not finished

CHANn_GCM_TAG_0

CHANn_GCM_TAG_0 is GCM tag register 0 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x00	CHANn_GCM_TAG_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_0	GCM tag[31:0] for channel *n*

CHANn_GCM_TAG_1

CHANn_GCM_TAG_1 is GCM tag register 1 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_1	GCM tag[63:32] for channel *n*

CHANn_GCM_TAG_2

CHANn_GCM_TAG_2 is GCM tag register 2 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x08	CHANn_GCM_TAG_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_2	GCM tag[95:64] for channel *n*

CHANn_GCM_TAG_3

CHANn_GCM_TAG_3 is GCM tag register 3 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_3	GCM tag[127:96] for channel *n*

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is an encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the cipher module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder				key_sel	reserved	reserved		key_length			ivin_sel	width			alg_sel	mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12]	RO	reserved	Reserved
[11]	RO	reserved	Reserved
[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is a cipher VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the cipher module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the cipher module.

Note the following points when configuring this register:

- If channel 0 is selected for the single-block operation, this register needs to be configured.
- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the cipher module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is an input queue total depth register for channel *n* (*n* = 1–7). This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel

CHANn_IBUF_CNT

CHANn_IBUF_CNT is a pending data buffer count register for channel *n* in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x128 + 0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is a processed buffer count register for channel *n* in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is an input queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_icnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is an encryption/decryption control register for channel *n*.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight												reserved				key_adder				key_sel	byte_seq	ts_vld	key_length			reserved		width		alg_sel		mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	weight	Weighted value of the current channel, in the unit of 64 bytes
[21:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12:11]	RO	reserved	Reserved

[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RO	reserved	Reserved
[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is an input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address for the input queue

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is an input queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iage_timer	Aging interrupt timer

CHANn_OBUF_NUM

CHANn_OBUF_NUM is an output queue total depth register for channel *n*. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	obuf_num	Total depth of the output queue

CHANn_OBUF_CNT

CHANn_OBUF_CNT is a pending data buffer count register for channel *n* in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue

CHANn_OFULL_CNT

CHANn_OFULL_CNT is a processed buffer count register for channel *n* in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is an output queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is an output queue start address register for channel *n*. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address for the output queue

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is an output queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	oage_timer	Aging interrupt timer

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1
[0]	RO	reserved	Reserved

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the cipher module
[30:16]	RO	reserved	Reserved
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6
[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1
[0]	RO	reserved	Reserved

INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	ch0_ibuf_raw	ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7
[14]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6
[13]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5
[12]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4
[11]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3
[10]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2
[9]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0
[7]	RWC	ch7_ibuf_raw	Raw input queue data interrupt for channel 7
[6]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6
[5]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5
[4]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4
[3]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3
[2]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2
[1]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1
[0]	RO	reserved	Reserved

RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rst_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	rst_status	Reset status indicator of the cipher module 0: The cipher module is being reset. 1: The cipher module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	ch0_busy	Status signal of channel 0
[0]	RW	ch0_start	Encryption/Decryption start signal of channel 0

13.2 HASH

13.2.1 Overview

The hash is a module for implementing the SHA1, SHA256, HMAC_SHA1, and HMAC_SHA256 algorithms. The SHA1 and SHA256 algorithms comply with the FIPS 180-2 standard. The HMAC_SHA1 and HMAC_SHA256 algorithms comply with the RFC2104 standard.

The hash module can be used to authenticate data integrity and construct digital signatures.

13.2.2 Features

The hash module has the following features:

- Supports the SHA1, SHA256, HMAC_SHA1, and HMAC_SHA256 algorithms.
- Supports the input data configured by the CPU and read operation in DMA mode.
- Supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The total length is configured by software and the maximum value is $(2^{64} – 64)$ bytes. The message length after padding (by software) is used as the configured data length for the SHA1 and SHA256 algorithms, and the (padded message length + 64 bytes) is used as the configured data length for the HMAC_SHA1 and HMAC_SHA256 algorithms.
- Supports the 128-bit HMAC key configured by hardware (Cipher Hash Key Ctrl) or software.
- Supports configurable initial values for the SHA1 and SHA256 algorithms.

13.2.3 Function Description

The hash module is used to authenticate data integrity and construct digital signatures. The hash module can be set to the initial value update mode (the initial value needs to be configured in this mode) or non-initial value update mode by software. Then the message digest can be calculated by using the SHA1 or SHA256 algorithm. Software can start the HMAC_SHA1 or HMAC_SHA256 algorithm to calculate the MAC. The initial value cannot be configured.

13.2.4 Operating Mode

SHA1 Operation Process in CPU Mode

The CPU configures the input data. An SHA1 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl] to 1 and HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

SHA1 Operation Process in DMA Mode

The DMA reads the input data. An SHA1 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl], HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

SHA256 Operation Process in CPU Mode

The CPU configures the input data. An SHA256 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl] and HASH_CTRL[sha_sel] to 1 and HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

SHA256 Operation Process in DMA Mode

The DMA reads the input data. An SHA256 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel] to 1 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

HMAC_SHA1 Operation Process in CPU Mode

The CPU configures the input data. An HMAC_SHA1 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 1 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

HMAC_SHA1 Operation Process in DMA Mode

The DMA reads the input data. An HMAC_SHA1 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel], HASH_CTRL[small_end_en], HASH_CTRL[sha_init_update_en], HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 0 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

HMAC_SHA256 Operation Process in CPU Mode

The CPU configures the input data. An HMAC_SHA256 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[small_end_en] and HASH_CTRL[sha_init_update_en] to 0 and HASH_CTRL[read_ctrl], HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 1 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 5 and step 6 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

HMAC_SHA256 Operation Process in DMA Mode

The DMA reads the input data. An HMAC_SHA256 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel] to 1 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], HASH_CTRL[small_end_en], HASH_CTRL[sha_init_update_en], and HASH_CTRL[hardkey_sel] to 0 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

Clock Gating

When the hash calculation is not required, you can disable the clock of the hash module to reduce power consumption by configuring the system controller register.

Soft Reset

You can soft-rest the hash module by configuring the system controller register.

13.2.5 Register Summary

Table 13-2 describes hash registers.

Table 13-2 Summary of hash registers (base address: 0x1007_0000)

Offset Address	Register	Description	Page
0x0	TOTAL_LEN1	Hash message total length register (lower 32 bits)	13-62
0x4	TOTAL_LEN2	Hash message total length register (upper 32 bits)	13-62
0x8	HASH_STATUS	Status register	13-63
0xC	HASH_CTRL	Control register	13-64

Offset Address	Register	Description	Page
0x10	SHA_START	Calculation start register	13-65
0x14	DMA_START_ADDR	Read message start address register	13-65
0x18	DMA_LEN	DMA transfer length register	13-65
0x1C	DATA_IN	Input data register	13-66
0x20	REC_LEN1	RX message length register 1	13-66
0x24	REC_LEN2	RX message length register 2	13-67
0x30	SHA_OUT1	Hash output register 1	13-67
0x34	SHA_OUT2	Hash output register 2	13-67
0x38	SHA_OUT3	Hash output register 3	13-68
0x3C	SHA_OUT4	Hash output register 4	13-68
0x40	SHA_OUT5	Hash output register 5	13-69
0x44	SHA_OUT6	Hash output register 6	13-69
0x48	SHA_OUT7	Hash output register 7	13-69
0x4C	SHA_OUT8	Hash output register 8	13-70
0x70	MCU_KEY0	Key 0 (configured by MCU) register	13-70
0x74	MCU_KEY1	Key 1 (configured by MCU) register	13-70
0x78	MCU_KEY2	Key 2 (configured by MCU) register	13-71
0x7C	MCU_KEY3	Key 3 (configured by MCU) register	13-71
0x80	KL_KEY0	Key 0 (configured by kl) register	13-72
0x84	KL_KEY1	Key 1 (configured by kl) register	13-72
0x88	KL_KEY2	Key 2 (configured by kl) register	13-72
0x8C	KL_KEY3	Key 3 (configured by kl) register	13-73
0x90	SHA_INIT1_UPDATE	SHA initial value register 1	13-73
0x94	SHA_INIT2_UPDATE	SHA initial value register 2	13-74
0x98	SHA_INIT3_UPDATE	SHA initial value register 3	13-74
0x9C	SHA_INIT4_UPDATE	SHA initial value register 4	13-74
0xA0	SHA_INIT5_UPDATE	SHA initial value register 5	13-75

Offset Address	Register	Description	Page
0xA4	SHA_INIT6_UPDATE	SHA initial value register 6	13-75
0xA8	SHA_INIT7_UPDATE	SHA initial value register 7	13-75
0xAC	SHA_INIT8_UPDATE	SHA initial value register 8	13-76

13.2.6 Register Description

TOTAL_LEN1

TOTAL_LEN1 is a hash message total length register (lower 32 bits).

Offset Address	Register Name	Total Reset Value
0x0	TOTAL_LEN1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_len1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	total_len1	SHA: lower bits of the padded message length (in byte) HMAC: lower bits of the length (in byte) of (i_key_pad + padded message)

TOTAL_LEN2

TOTAL_LEN2 is a hash message total length register (upper 32 bits).

Offset Address	Register Name	Total Reset Value
0x4	TOTAL_LEN2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_len2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	total_len2	SHA: upper bits of the padded message length (in byte) HMAC: upper bits of the length (in byte) of (i_key_pad + padded message)

HASH_STATUS

HASH_STATUS is an HASH status register.

Offset Address	Register Name	Total Reset Value
0x8	HASH_STATUS	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									error_state				rec_rdy	msg_rdy	dma_rdy	hash_rdy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	len_err	Length correctness flag 0: correct 1: incorrect
[5:4]	RO	error_state	AHB bus status err_state[4] 0: No error occurs on the AHB. 1: An error occurs on the AHB. err_state[5] 0: The AHB slave is idle. 1: The AHB slave is busy.
[3]	RO	rec_rdy	Data RX ready flag for the internal logic (reg_rdy = msg_rdy & dma_rdy) 0: not ready 1: ready
[2]	RO	msg_rdy	Block calculation debugging information 0: The CPU channel is not ready to receive data. 1: The CPU channel is ready to receive data.
[1]	RO	dma_rdy	DMA debugging information 0: A data block is not completely read in DMA mode. 1: A data block is completely read in DMA mode.
[0]	RO	hash_rdy	TOTAL_LEN calculation completion signal 0: The calculation is not complete. 1: The calculation is complete.

HASH_CTRL

HASH_CTRL is an HASH control register.

Offset Address	Register Name	Total Reset Value
0xC	HASH_CTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sha_init_update_en	small_end_en	hardkey_sel	hmac_flag	sha_sel		read_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	sha_init_update_en	SHA initial value update enable. This bit is set to 0 for HMAC. 0: disabled. The default SHA initial value is used. 1: enabled. The value of sha_initn_update is used as the initial value when the SHA calculation starts.
[5]	RW	small_end_en	Word reverse order enable 0: big-endian mode 1: little-endian mode
[4]	RW	hardkey_sel	HMAC key select. This bit is set to 0 for the SHA. 0: kl_key (hardware key) 1: MCU key (software key)
[3]	RW	hmac_flag	Calculation mode select 0: SHA calculation 1: HMAC calculation
[2:1]	RW	sha_sel	Hash mode control 00: SHA1 mode 01: SHA256 mode Other values: reserved, Currently this field can be set to only 00 or 01.
[0]	RW	read_ctrl	Message transfer mode control 0: The message is read by the DMA. 1: The message is read by the CPU.

SHA_START

SHA_START is an SHA computing start register.

Offset Address	Register Name	Total Reset Value
0x10	SHA_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sha_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	sha_start	Hash calculation start signal 0: not start 1: start

DMA_START_ADDR

DMA_START_ADDR is a read message start address register.

Offset Address	Register Name	Total Reset Value
0x14	DMA_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_start_addr	Byte address. The address must be configured as word-aligned by software.

DMA_LEN

DMA_LEN is a DMA transfer length register.

Offset Address	Register Name	Total Reset Value
0x18	DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	segment_len1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	segment_len1	DMA transfer length (in byte), which must be word-aligned After the length is configured, data is read and calculated automatically by the internal logic.

DATA_IN

DATA_IN is an SHA computing input data register.

Offset Address	Register Name	Total Reset Value
0x1C	DATA_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_in																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	data_in	The input data of the message digest needs to be determined through SHA computing, and the input data is configured by the CPU. This register cannot be read when debug_disable is 1.

REC_LEN1

REC_LEN1 is RX message length register 1.

Offset Address	Register Name	Total Reset Value
0x20	REC_LEN1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	receive_byte_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	receive_byte_cnt	Number of bytes calculated by the hash module (64 bytes for each block). This register is cleared when the calculation starts.

REC_LEN2

REC_LEN2 is RX message length register 2.

Offset Address	Register Name	Total Reset Value
0x24	REC_LEN2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	receive_byte_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	receive_byte_cnt	Number of bytes calculated by the hash module (64 bytes for each block). This register is cleared when the calculation starts.

SHA_OUT1

SHA_OUT1 is hash output result register 1.

Offset Address	Register Name	Total Reset Value
0x30	SHA_OUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out1	Bits 0−31 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT2

SHA_OUT2 is hash output result register 2.

Offset Address	Register Name	Total Reset Value
0x34	SHA_OUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out2	Bits 32−63 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT3

SHA_OUT3 is hash output result register 3.

Offset Address	Register Name	Total Reset Value
0x38	SHA_OUT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out3	Bits 64−95 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT4

SHA_OUT4 is hash output result register 4.

Offset Address	Register Name	Total Reset Value
0x3C	SHA_OUT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out4	Bits 96−127 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT5

SHA_OUT5 is hash output result register 5.

Offset Address	Register Name	Total Reset Value
0x40	SHA_OUT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out5	Bits 128−159 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT6

SHA_OUT6 is hash output result register 6.

Offset Address	Register Name	Total Reset Value
0x44	SHA_OUT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out6	This register does not apply to SHA1. This field indicates bits 160−191 of the SHA256 message digest output.

SHA_OUT7

SHA_OUT7 is hash output result register 7.

Offset Address	Register Name	Total Reset Value
0x48	SHA_OUT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out7	This register does not apply to SHA1. This field indicates bits 192−223 of the SHA256 message digest output.

SHA_OUT8

SHA_OUT8 is hash output result register 8.

Offset Address	Register Name	Total Reset Value
0x4C	SHA_OUT8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out8																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out8	This register does not apply to SHA1. This field indicates bits 224−255 of the SHA256 message digest output.

MCU_KEY0

MCU_KEY0 is an HMAC input key register (bits 0−31, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x70	MCU_KEY0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mcu_key0	HMAC input key register (bits 0−31, configured by the CPU) This register cannot be read when debug_disable is 1.

MCU_KEY1

MCU_KEY1 is an HMAC input key register (bits 32−63, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x74	MCU_KEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mcu_key1	HMAC input key register (bits 32−63, configured by the CPU) This register cannot be read when debug_disable is 1.

MCU_KEY2

MCU_KEY2 is an HMAC input key register (bits 64−95, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x78	MCU_KEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mcu_key2	HMAC input key register (bits 64−95, configured by the CPU) This register cannot be read when debug_disable is 1.

MCU_KEY3

MCU_KEY3 is an HMAC input key register (bits 96−127, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x7C	MCU_KEY3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mcu_key3	HMAC input key register (bits 96−127, configured by the CPU) This register cannot be read when debug_disable is 1.

KL_KEY0

KL_KEY0 is an HMAC input key register (bits 0−31, configured by the logic, read-only for the CPU).

Offset Address	Register Name	Total Reset Value
0x80	KL_KEY0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kl_key0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	kl_key0	HMAC input key register (bits 0−31, configured by the logic, read-only for the CPU) This register cannot be read when debug_disable is 1.

KL_KEY1

KL_KEY1 is an HMAC input key register (bits 32−63, configured by the logic, read-only for the CPU).

Offset Address	Register Name	Total Reset Value
0x84	KL_KEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kl_key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	kl_key1	HMAC input key register (bits 32−63, configured by the logic, read-only for the CPU) This register cannot be read when debug_disable is 1.

KL_KEY2

KL_KEY2 is an HMAC input key register (bits 64−95, configured by the logic, read-only for the CPU).

Offset Address	Register Name	Total Reset Value
0x88	KL_KEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kl_key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	kl_key2	HMAC input key register (bits 64−95, configured by the logic, read-only for the CPU) This register cannot be read when debug_disable is 1.

KL_KEY3

KL_KEY3 is an HMAC input key register (bits 96−127, configured by the logic, read-only for the CPU).

Offset Address	Register Name	Total Reset Value
0x8C	KL_KEY3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	kl_key3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	kl_key3	HMAC input key register (bits 96−127, configured by the logic, read-only for the CPU) This register cannot be read when debug_disable is 1.

SHA_INIT1_UPDATE

SHA_INIT1_UPDATE is SHA initial value register 1.

Offset Address	Register Name	Total Reset Value
0x90	SHA_INIT1_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init1_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init1_update	SHA initial value (bits 0−31)

SHA_INIT2_UPDATE

SHA_INIT2_UPDATE is SHA initial value register 2.

Offset Address	Register Name	Total Reset Value
0x94	SHA_INIT2_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init2_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init2_update	SHA initial value (bits 32−63)

SHA_INIT3_UPDATE

SHA_INIT3_UPDATE is SHA initial value register 3.

Offset Address	Register Name	Total Reset Value
0x98	SHA_INIT3_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init3_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init3_update	SHA initial value (bits 64−95)

SHA_INIT4_UPDATE

SHA_INIT4_UPDATE is SHA initial value register 4.

Offset Address	Register Name	Total Reset Value
0x9C	SHA_INIT4_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init4_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init4_update	SHA initial value (bits 96−127)

SHA_INIT5_UPDATE

SHA_INIT5_UPDATE is SHA initial value register 5.

Offset Address	Register Name	Total Reset Value
0xA0	SHA_INIT5_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init5_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init5_update	SHA initial value (bits 128−159)

SHA_INIT6_UPDATE

SHA_INIT6_UPDATE is SHA initial value register 6.

Offset Address	Register Name	Total Reset Value
0xA4	SHA_INIT6_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init6_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init6_update	SHA initial value (bits 160−191)

SHA_INIT7_UPDATE

SHA_INIT7_UPDATE is SHA initial value register 7.

Offset Address	Register Name	Total Reset Value
0xA8	SHA_INIT7_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init7_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init7_update	SHA initial value (bits 192−223)

SHA_INIT8_UPDATE

SHA_INIT8_UPDATE is SHA initial value register 8.

Offset Address	Register Name	Total Reset Value
0xAC	SHA_INIT8_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init8_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init8_update	SHA initial value (bits 224−255)

13.3 RNG_GEN

13.3.1 Overview

RNG_GEN is a module that generates true random numbers in compliance with the FIPS 140-1 random test standard.

13.3.2 Features

The RNG_GEN module has the following features:

- Generates true random numbers.
- Supports three random number sources that can be configured by the CPU.
- Disables the random number sources.

13.3.3 Operating Mode

RNG_GEN Operation Process

The RNG_GEN operation process is as follows:

Step 1 Check whether RNG_STAT[rng_data_count] is greater than or equal to 1. If yes, go to the next step because there are random numbers; if no, wait.

Step 2 Read RNG_FIFO_DATA[rng_fifo_data].

Step 3 Repeat step 1 and step 2 until the required number of random numbers are read.

----End

13.3.4 Register Summary

Table 13-3 describes RNG_GEN registers.

Table 13-3 Summary of RNG_GEN registers (base address: 0x2028_0000)

Offset Address	Register	Description	Page
0x00	RNG_CTRL	RNG control register	13-77
0x04	RNG_FIFO_DATA	RNG FIFO data register	13-78
0x08	RNG_STAT	RNG status register	13-79
0x0C	RNG_DATA_0	RNG data register 0	13-79

13.3.5 Register Description

RNG_CTRL

RNG_CTRL is an RNG control register.

Offset Address	Register Name	Total Reset Value
0x00	RNG_CTRL	0x0000_1082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		low_osc_st1	low_osc_st0	reserved												post_process_depth								post_process_enable	reserved	drop_enable	filter_enable	mix_en	cleardata	osc_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	WC	low_osc_st1	Exception test of the low-frequency oscillator 0: The low-frequency oscillator works properly. 1: The output of the low-frequency oscillator is always 1, and writing this bit clears it.
[29]	WC	low_osc_st0	Exception test of the low-frequency oscillator 0: The low-frequency oscillator works properly. 1: The output of the low-frequency oscillator is always 1, and writing this bit clears it.
[28:16]	RO	reserved	Reserved
[15:8]	RW	post_process_depth	Post-processing mixing depth. A larger value indicates a better random effect and lower speed.

[7]	RW	post_process_enable	Pre-processing enable for the random number. If this function is enabled, the random number generation speed is decreased by 1/(post_process_depth + 1). 0: disabled 1: enabled
[6]	RO	reserved	Reserved
[5]	RW	drop_enable	Enable for discarding two-bit data when the values of the consecutive two bits are the same (00 or 11). If this function is enabled, the random number generation speed is decreased by 1/3. 0: disabled 1: enabled
[4]	RW	filter_enable	Pre-processing filtering enable for the random number. If this function is enabled, the random number generation speed is decreased by 1/4. 0: disabled 1: enabled
[3]	RW	mix_en	Data mixing enable 0: disabled 1: enabled
[2]	WC	cleardata	Random number clear 0: not cleared 1: cleared
[1:0]	RW	osc_sel	Random number source select 00: RNG is disabled. 01: Random number source 1 is used. 10: Random number source 2 is used. 11: Random number source 3 is used.

RNG_FIFO_DATA

RNG_FIFO_DATA is an RNG FIFO data register.

Offset Address	Register Name	Total Reset Value
0x04	RNG_FIFO_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rng_fifo_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rng_fifo_data	You can read the random number by directly reading this register.

RNG_STAT

RNG_STAT is an RNG status register.

Offset Address	Register Name	Total Reset Value
0x08	RNG_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rn_dat_rdy	reserved																													rng_data_count			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	rn_dat_rdy	RNG_DATA_0 ready flag
[30:3]	RO	reserved	Reserved
[2:0]	RO	rng_data_count	Number of 32-bit random numbers in the random number FIFO. The maximum value is 4.

RNG_DATA_0

RNG_DATA_0 is RNG data register 0.

Offset Address	Register Name	Total Reset Value
0x0C	RNG_DATA_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rng_data_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rng_data_0	Random number register 0. The random number to be used by DDRCA cannot be read because debug_disable is 1.

13.4 RSA

13.4.1 Overview

The Rivest-Shamir-Adleman (RSA) is a public key encryption/decryption algorithm implemented through the modular exponentiation operation. The ciphertext is obtained as follows: $C = M^E \bmod N$. The plaintext is obtained as follows: $M=C^D \bmod N$. *M* indicates the plaintext, *C* indicates the ciphertext, *(N, E)* indicates the public key, and *(N, D)* indicates the private key.

The RSA module supports RSA 1024, RSA 2048, and RSA 4096 that comply with the PKCS#1 V1.5/2.1 standard.

The RSA module is used for data encryption/decryption and digital signature verification.

13.4.2 Features

The RSA module has the following features:

- Supports 1024-bit, 2048-bit, and 4096-bit keys.
- Supports the minimum performance of 10 operations per second (OPS) for the 2048-bit key.
- Supports key debugging by using CRC16.
- Clears the random access memories (RAMs) that store the internal RSA keys, packets, and results.

13.4.3 Function Description

The RSA module is used for data encryption/decryption and digital signature verification. The registers are configured by software. Then the RSA module is started to implement the modular exponentiation operation. The RSA module also uses CRC16 to calculate the key stored in the logic and outputs the result for checking whether the key is correct. The RSA module also clears the RAMs that store the internal keys, packets, and results.

13.4.4 Operating Mode

Encrypting/Decrypting Data by Using RSA

Data is encrypted/decrypted by using RSA as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_key_width] to 1 and SEC_RSA_MOD_REG[sec_rsa_mod_sel], SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 0. When SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; when the field value is 1, RSA 2048 is used; when the field value is 2, RSA 4096 is used.

Step 3 Configure SEC_RSA_WPKT_REG[sec_rsa_wpkt_reg]. The configured packet length must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

Step 4 Configure SEC_RSA_WSEC_REG[sec_rsa_wsec_reg]. Set the key parameter N and then E/D. The length of each parameter must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

Step 5 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 6 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 7 Read SEC_RSA_RRSLT_REG[sec_rsa_rrslt_reg]. The length of the read result must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

----End

Debugging the Key by Using CRC16

The key is debugged by using CRC16 as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 0, SEC_RSA_MOD_REG[sec_rsa_mod_sel] to 3, and SEC_RSA_MOD_REG[sec_rsa_key_width] to 1. When SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; when the field value is 1, RSA 2048 is used; when the field value is 2, RSA 4096 is used.

Step 3 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 4 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 5 Read the cyclic redundancy check (CRC) result from SEC_CRC16_REG[sec_rsa_crc16_dat].

----End

Clearing the RAM

The RAM is cleared as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_mod_sel] to 2 and SEC_RSA_MOD_REG[sec_rsa_key_width], SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 1. If SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; if the field value is 1, RSA 2048 is used; if the field value is 2, RSA 4096 is used. If SEC_RSA_MOD_REG[sec_rsa_data0_clr] is 1, the RAM that stores the RSA key is cleared; if the field value is 0, the RAM that stores the RSA key is not cleared. If SEC_RSA_MOD_REG[sec_rsa_data1_clr] is 1, the RAM that stores the RSA packet is cleared; if the field value is 0, the RAM that stores the RSA packet is not cleared. If SEC_RSA_MOD_REG[sec_rsa_data2_clr] is 1, the RAM that stores the RSA result is cleared; if the field value is 0, the RAM that stores the RSA result is not cleared.

Step 3 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 4 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 5 Read SEC_RSA_RPKT_REG[sec_rsa_rpkt_reg] to determine whether the RAM that stores the packet is cleared.

Step 6 Read SEC_RSA_RRSLT_REG[sec_rsa_rrslt_reg] to determine whether the RAM that stores the result is cleared.

Step 7 Check the key through CRC to determine whether the RAM that stores the key is cleared.

----End

13.4.5 Register Summary

Table 13-4 describes RSA registers.

Table 13-4 Summary of RSA registers (base address: 0x2026_0000)

Offset Address	Register	Description	Page
0x50	SEC_RSA_BUSY_REG	Busy status register for the SEC_RSA module	13-82
0x54	SEC_RSA_MOD_REG	Operating mode register for the SEC_RSA module	13-83
0x58	SEC_RSA_WSEC_REG	Key write operation register for the SEC_RSA module	13-84
0x5C	SEC_RSA_WPKT_REG	Packet write operation register for the SEC_RSA module	13-84
0x60	SEC_RSA_RPKT_REG	Packet read operation register for the SEC_RSA module	13-85
0x64	SEC_RSA_RRSLT_REG	Calculation result read operation register for the SEC_RSA module	13-85
0x68	SEC_RSA_START_REG	Modular exponentiation operation configuration start register for the SEC_RSA module	13-85
0x6C	SEC_RSA_ADDR_REG	RAM address register for the key, packet, and result of the SEC_RSA module	13-86
0x70	SEC_RSA_ERROR_REG	Error alarm status register for the SEC_RSA module	13-87
0x74	SEC_CRC16_REG	Key CRC result register for the SEC_RSA module	13-87

13.4.6 Register Description

SEC_RSA_BUSY_REG

SEC_RSA_BUSY_REG is a busy status register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x50	SEC_RSA_BUSY_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sec_rsa_busy_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	sec_rsa_busy_reg	Busy status of the SEC_RSA module 0: idle 1: busy

SEC_RSA_MOD_REG

SEC_RSA_MOD_REG is an operating mode register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x54	SEC_RSA_MOD_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sec_rsa_data2_clr	sec_rsa_data1_clr	sec_rsa_data0_clr	sec_rsa_key_width			sec_rsa_mod_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	sec_rsa_data2_clr	Clear enable for the RAM that stores the RSA result 0: not cleared 1: cleared

[5]	RW	sec_rsa_data1_clr	Clear enable for the RAM that stores the RSA packet 0: not cleared 1: cleared
[4]	RW	sec_rsa_data0_clr	Clear enable for the RAM that stores the RSA key 0: not cleared 1: cleared
[3:2]	RW	sec_rsa_key_width	Key bit width 00: 1024 bits 01: 2048 bits 10: 4096 bits 11: 1024 bits
[1:0]	RW	sec_rsa_mod_sel	Operating mode select 00: modular exponentiation encryption and decryption operation 01: The key is updated, and the modular exponentiation operation is not performed (this mode is not supported currently). 10: The RAM is cleared. 11: The key is checked by using CRC16.

SEC_RSA_WSEC_REG

SEC_RSA_WSEC_REG is a key write operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x58	SEC_RSA_WSEC_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wsec_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	sec_rsa_wsec_reg	Key address configured by the CPU

SEC_RSA_WPKT_REG

SEC_RSA_WPKT_REG is a packet write operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x5C	SEC_RSA_WPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	sec_rsa_wpkt_reg	Packet address configured by the CPU

SEC_RSA_RPKT_REG

SEC_RSA_RPKT_REG is a packet read operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x60	SEC_RSA_RPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_rpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sec_rsa_rpkt_reg	Packet address read by the CPU

SEC_RSA_RRSLT_REG

SEC_RSA_RRSLT_REG is a calculation result read operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x64	SEC_RSA_RRSLT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_rrslt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sec_rsa_rrslt_reg	Calculation result read by the CPU

SEC_RSA_START_REG

SEC_RSA_START_REG is a modular exponentiation operation configuration start register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x68	SEC_RSA_START_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sec_rsa_start_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	sec_rsa_start_reg	CPU configuration start 0: not start 1: start

SEC_RSA_ADDR_REG

SEC_RSA_ADDR_REG is an RAM address register for the key, packet, and result of the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x6C	SEC_RSA_ADDR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_addere_rslt								sec_rsa_addre_pkt								sec_rsa_addre_d								sec_rsa_addr_n							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	sec_rsa_addere_rslt	Result RAM address The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.
[23:16]	RO	sec_rsa_addre_pkt	Packet RAM address The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored or read. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.

[15:8]	RO	sec_rsa_addre_d	RAM address of the key parameter E/D The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.
[7:0]	RO	sec_rsa_addr_n	RAM address of the key parameter N The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.

SEC_RSA_ERROR_REG

SEC_RSA_ERROR_REG is an error alarm status register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x70	SEC_RSA_ERROR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sec_rsa_err1	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	sec_rsa_err1	Alarm when the external input RSA key (N) is an even number (the odd/even feature of the key is not checked when the RAM that stores the key is cleared) 0: The external input key is normal. 1: The external input key (N) is an even number.
[0]	RO	reserved	Reserved

SEC_CRC16_REG

SEC_CRC16_REG is a key CRC result register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x74	SEC_CRC16_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sec_rsa_crc16_dat																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sec_rsa_crc16_dat	CRC result of the key

13.5 Cipher Hash Key Ctrl

13.5.1 Operating Mode

The cipher hash key control module has the following three working modes:

- Burning the key to the one-time programming (OTP)
- Loading the key to the cipher
- Loading the key to the hash

13.5.1.1 Burning the Key to the OTP

Before burning, the data in the OTP is 0. After burning is enabled, the cipher hash key control module burns the corresponding macro unit to 1 based on the key value and OTP address of the key (KL_CTRL[otp_key_add]).

The operation process of burning the key to the OTP is as follows:

Step 1 Assign values to KL_WKEY0, KL_WKEY1, KL_WKEY2, and KL_WKEY3.

Step 2 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0] and KL_STA[ctrl_busy1] are 0.

Step 3 Write the OTP address of the key to KL_CTRL[otp_key_add], and set KL_CTRL[otp_kd_mode] to 1 and KL_CTRL[cipher_kl_mode] and KL_CTRL[hash_kl_mode] to 0 to enable the mode of burning the key to the OTP.

Step 4 Write 1 to KL_CTRL[start] to start the operation.

Step 5 Query KL_STA[key_wt_finish]. If the value changes from 0 to 1, the burning is complete. Note that if KL_STA[key_wt_error] is 1, the burning fails and the key address has been burned before.

----End

13.5.1.2 Loading the Key to the Cipher

The operation process of loading the key to the cipher is as follows:

Step 1 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0] and KL_STA[ctrl_busy1] are 0.

Step 2 Write the OTP address of the key to KL_CTRL[otp_key_add], write the key address for loading the key to the cipher to KL_CTRL[cipher_key_add], and set KL_CTRL[cipher_kl_mode] to 1 and KL_CTRL[otp_kd_mode] and KL_CTRL[hash_kl_mode] to 0 to enable the mode of loading the key to the cipher.

Step 3 Write 1 to KL_CTRL[start] to start the operation.

Step 4 Query KL_STA[cipher_kl_finish]. If the value changes from 0 to 1, the process of loading the key to the cipher is complete.

----End

13.5.1.3 Loading the Key to the Hash

The operation process of loading the key to the hash is as follows:

Step 1 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0] and KL_STA[ctrl_busy1] are 0.

Step 2 Write the OTP address of the key to KL_CTRL[otp_key_add], and set KL_CTRL[hash_kl_mode] to 1 and KL_CTRL[cipher_kl_mode] and KL_CTRL[otp_kd_mode] to 0 to enable the mode of loading the key to the hash.

Step 3 Write 1 to KL_CTRL[start] to start the operation.

Step 4 Query KL_STA[hash_key_read_busy]. If the value changes from 1 to 0, the process of loading the key to the hash is complete.

----End

13.5.2 Register Summary

Table 13-5 describes cipher hash key control registers.

Table 13-5 Summary of cipher hash key control registers (base address: 0x2010_0800)

Offset Address	Register	Description	Page
0x0000	KL_WKEY0	Key burning register 0	13-90
0x0004	KL_WKEY1	Key burning register 1	13-90
0x0008	KL_WKEY2	Key burning register 2	13-90
0x000C	KL_WKEY3	Key burning register 3	13-91
0x0010	KL_CTRL	Key control register	13-91
0x0014	KL_STA	Status indicator register	13-92

13.5.3 Register Description

KL_WKEY0

KL_WKEY0 is key burning register 0.

Offset Address	Register Name	Total Reset Value
0x0000	KL_WKEY0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key0	Key[31:0] that are burnt to the OTP

KL_WKEY1

KL_WKEY1 is key burning register 1.

Offset Address	Register Name	Total Reset Value
0x0004	KL_WKEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key1	Key[63:32] that are burnt to the OTP

KL_WKEY2

KL_WKEY2 is key burning register 2.

Offset Address	Register Name	Total Reset Value
0x0008	KL_WKEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key2	Key[95:64] that are burnt to the OTP

KL_WKEY3

KL_WKEY3 is key burning register 3.

Offset Address	Register Name	Total Reset Value
0x000C	KL_WKEY3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key3	Key[127:96] that are burnt to the OTP

KL_CTRL

KL_CTRL is a key control register.

Offset Address	Register Name	Total Reset Value
0x0010	KL_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					cipher_key_add			reserved				otp_key_add				hash_kl_mode		otp_kd_mode		cipher_kl_mode		start	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	cipher_key_add	Key address for loading the key to the cipher
[7:6]	RW	reserved	Reserved
[5:4]	RW	otp_key_add	Address of the key in the OTP for burning or loading the key
[3]	RW	hash_kl_mode	Enable for loading the key to the hash 0: disabled 1: enabled **NOTE** Only one of hash_kl_mode, otp_kd_mode, and cipher_kl_mode can be set to 1 at a time. That is, only one function takes effect at a time.

[2]	RW	otp_kd_mode	Enable for burning the key to the OTP 0: disabled 1: enabled **NOTE** Only one of hash_kl_mode, otp_kd_mode, and cipher_kl_mode can be set to 1 at a time. That is, only one function takes effect at a time.
[1]	RW	cipher_kl_mode	Enable for loading the key to the cipher 0: disabled 1: enabled **NOTE** Only one of hash_kl_mode, otp_kd_mode, and cipher_kl_mode can be set to 1 at a time. That is, only one function takes effect at a time.
[0]	RW	start	Operation start. Writing 1 to this bit starts the operation. Reading back this bit has no effect. **NOTE** A new operation can be initiated only when ctrl_busy1 and ctrl_busy0 are 0 and ctrl_rdy is 1.

KL_STA

KL_STA is a status indicator register.

Offset Address	Register Name	Total Reset Value
0x0014	KL_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key_wt_finish	key_wt_error	ctrl_busy1	ctrl_busy0	ctrl_rdy	reserved																									hash_key_read_busy	cipher_kl_finish
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	key_wt_finish	Whether the operation of burning the key to the OTP is complete 0: not complete 1: complete
[30]	RO	key_wt_error	Whether an error occurs during the operation of burning the key to the OTP 0: No error occurs. The burning is successful. 1: An error occurs. The key address has been burnt before.

[29]	RO	ctrl_busy1	Controller busy signal 1. A new operation can be initiated only when ctrl_busy1 and ctrl_busy0 are 0 and ctrl_rdy is 1.
[28]	RO	ctrl_busy0	Controller busy signal 0. A new operation can be initiated only when ctrl_busy1 and ctrl_busy0 are 0 and ctrl_rdy is 1.
[27]	RO	ctrl_rdy	Controller ready signal. A new operation can be initiated only when ctrl_busy1 and ctrl_busy0 are 0 and ctrl_rdy is 1.
[26:2]	RO	reserved	Reserved
[1]	RO	hash_key_read_busy	Whether the operation of loading the key to the hash is complete 0: complete 1: not complete The hash encryption and decryption operations are started only after the loading operation is complete.
[0]	RO	cipher_kl_finish	Whether the operation of loading the key to the cipher is complete 0: not complete 1: complete The cipher encryption and decryption operations are started only after the loading operation is complete.

14 Differences Between Hi3519 V100 and Hi3519 V101

Table 14-1 describes the differences between Hi3519 V100 and Hi3519 V101.

Table 14-1 Differences between Hi3519 V100 and Hi3519 V101

Difference	Hi3519 V100	Hi3519 V101
Virtual direct memory access (VDMA)	Not supported	Supported
Network gigabit media access controller (GMAC) I/O coherency	Not supported	Supported
Dual-sensor	Not supported	Supported
Fisheye correction	180°, 360°, and normal basic correction modes	New functions such as projective mapping function (PMF)
Anti-jitter	Basic version	Optimized algorithm and improved performance
Performance	8 megapixels@30 fps+720p@30 fps	8 megapixels@30 fps+1080p@30 fps
Process	TSMC 28HPC	TSMC 28HPC+
Package	15 x 15 TFBGA 0.65 pitch	10 x 10 FC-BGA 0.4 pitch

Contents

A Ordering Information

Figure A-1 shows the Hi3519 V100 mark.

Figure A-1 Hi3519 V100 mark

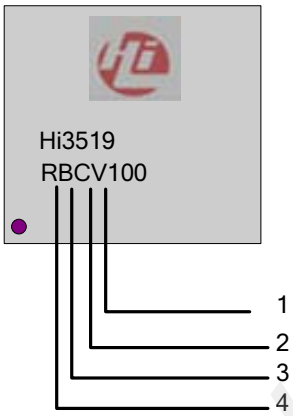


Table A-1 describes the Hi3519 V100 mark.

Table A-1 Meaning of the Hi3519 V100 mark

No.	Item	Description
1	Version number	It indicates the chip version number.
2	Temperature flag	The letter C stands for commercial. It indicates that the chip is for commercial use.
3	Package flag	The letter B indicates the ball grid array (BGA) package.
4	Environmental protection flag	The letter R stands for Restriction of Hazardous Substances (RoHS).